

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Components Group



**The
Power
Semiconductor
Data Book**
for
Design Engineers

TEXAS INSTRUMENTS
INCORPORATED

TERMS, DEFINITIONS, AND TESTING PROCEDURES	1
CROSS-REFERENCE GUIDE	2
PRODUCT SELECTION GUIDES	3
ALPHA-NUMERIC INDEX TO DATA SHEETS	4
SILICON POWER DATA SHEETS	5
GERMANIUM POWER DATA SHEETS	6
THYRISTOR DATA SHEETS	7
TECHNICAL RESPONSE LAB	8
POWER FUNCTIONS	9
POWER SEMICONDUCTOR TECHNOLOGY	10
APPLICATION INFORMATION	11
QUALITY AND RELIABILITY INFORMATION	12

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For Continuing Information on TI Power Semiconductors

This catalog provides technical descriptions and specifications on power semiconductor devices and functions manufactured by Texas Instruments. As a leading manufacturer of power devices, TI is continually developing and introducing new products to the electronics industry.

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**The
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for
Design Engineers**

First Edition



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TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

THE POWER SEMICONDUCTOR DATA BOOK

From the earliest days of transistors, semiconductor circuit designers have needed devices capable of handling the *power* functions of their equipment.

The past twenty years in the semiconductor industry have brought extensive development of power products—germanium power transistors, silicon power transistors, thyristors, and more recently, power function modules. The future will certainly bring even further developments in power devices and functions.

Along with advancements in integrated circuit technology, improvements in power devices will aid equipment design engineers in their efforts toward continual enhancement of functional utility, cost effectiveness, and reliability of designs.

In this 800-page data book, Texas Instruments is pleased to catalog important power semiconductor products available in the industry, and to present technical information on TI's broad line of power transistors, thyristors, and power function products.

You will find essential design information on Germanium and Silicon Power Transistors, SCR's, Triacs, and Power Function modules. In Silicon Power, TI's extensive product line encompasses high-voltage as well as low-voltage, high-safe-operating-area (SOA) designs, power Darlingtons, fast switching types, radiation-tolerant designs, JAN and JANTX types, and both metal can and plastic package types.

Most of the silicon power devices, as well as a broad range of SCR's and Triacs, are offered in TI's specially designed plastic packages. These designs incorporate glass-passivated junctions with thermally-matched epoxy and piece-parts, for high reliability—plus the adaptability for high-volume, cost-effective production.

Section 8 features the Technical Response Lab (TRL). The TRL facility provides a broad capability for custom designs to meet special needs. This capability includes custom silicon chip design for specific electrical performance, together with custom packaging techniques for reliable performance of devices under unique environmental conditions. These high-volume, low-cost, highly-reliable devices, on one hand, and high-performance, custom designs for special applications, on the other, represent TI's two-fold approach to the power market. Thus product coverage is broad, with the capability of serving a very wide range of customer needs.

The data book indices are designed with margin tabs for ease in location of data sheets for specific products, as well as general information categories. Included are an alpha-numeric index to product data sheets and product cross-reference and selection guides.

We sincerely hope you will find this Power Semiconductor Data Book for Design Engineers a valuable addition to your technical library. It represents TI experience since the early 1950's in the design and manufacture of power semiconductor products.

Terms, Definitions, and Testing Procedures

POWER TRANSISTORS

POWER TRANSISTOR SAFETY CONSIDERATIONS

The designer, maker, and user of electrical equipment containing power transistors should give attention to the following points relative to the safety of personnel that may operate the equipment.

The electrical potentials of the collector, emitter, and base terminals on the transistor present an electrical shock hazard when the equipment is energized.

The normal operating case temperature of energized transistors is often high enough to present burn hazards to both operating personnel and flammable material touching the transistor.

If the transistor is falsely turned "on" or fails, power will be applied to the equipment load. Operator safety may be affected by an unexpected energizing of the load.

In the event that an equipment output short or internal fault condition develops, very high surge current can be passed through the transistor. If this condition exceeds transistor ratings for magnitude and duration, the transistor may be damaged; and if the surge is severe enough, internal heating can cause the transistor to rupture and perhaps sustain an arc.

POWER TRANSISTOR STANDARDS

Following are sources of standard material relating to Power Transistors:

EIA and JEDEC Standards:

Electronic Industries Association
2001 Eye St. N.W., Washington, D.C. 20006
Telephone: 202-659-2200

JC-25 Power Transistor Registration Formats RDF-1 to RDF-6

Test Procedures for Verification of Maximum Ratings of Power Transistors—JEDEC Publication No.65

Thermal Resistance Measurements of Conduction Cooled Power Transistors—EIA Standard RS-313-A

JEDEC Recommendations for Letter Symbols, Abbreviations, Terms, and Definitions for Semiconductor Device Data Sheets and Specifications—JEDEC Publication No. 77

Standard List of Values to be used in Power Transistor Device Registration and Minimum Differences for Discreteness of Registration—JEDEC Publication NO. 74

IEC Standards

American National Standards Institute, Inc.
1430 Broadway
New York, N. Y. 10018
Telephone: 212-868-1220

IEC Publication 147: Essential Ratings and Characteristics of Semiconductor Devices and General Principles of Measuring Methods.

IEC Publication 148: Letter Symbols for Semiconductor Devices and Integrated Microcircuits

IEC Publication 191: Mechanical Standardization of Semiconductor Devices.

TERMS AND DEFINITIONS

POWER TRANSISTORS

Military Standards

Commanding Officer, U.S. Naval Publications and Forms Center,
5801 Tabor Avenue, Philadelphia, Pa., 19120.

- MIL-S-19500: Semiconductor Devices, General Specification for
- MIL-STD-105: Sampling Procedures and Tables for Inspection by Attributes
- MIL-STD-202: Test Methods for Electronic and Electrical Component Parts
- MIL-STD-750: Test Methods for Semiconductor Devices
- MIL-STD-883: Test Methods and Procedures for Microelectronics

1

TERMS AND DEFINITIONS

POWER TRANSISTORS

POWER TRANSISTOR TERMS, DEFINITIONS, AND LETTER SYMBOLS

Introduction

This part contains letter symbols, abbreviations, terms, and definitions commonly used with Power Transistors. Most of the information was obtained from JEDEC Publication No. 77. This document and the JC-25 JEDEC registration formats have over-riding authority where any conflict may occur.

1

Power Transistor Terms and Definitions

Term	Definition
base (B, b)*	A region which lies between an emitter and collector of a transistor and into which minority carriers are injected. (Ref. 60 IRE 28.S1)
breakdown	A phenomenon occurring in a reverse-biased semiconductor junction, the initiation of which is observed as a transition from a region of high small-signal resistance to a region of substantially lower small-signal resistance for an increasing magnitude of reverse current. (Ref RS-282 par. 1.38)
breakdown region	A region of the volt-ampere characteristic beyond the initiation of breakdown for an increasing magnitude of reverse current. (Ref RS-282 par. 1.37)
breakdown voltage	The voltage measured at a specified current in a breakdown region. (Ref MIL-S-19500D par. 20.3)
collector (C, c)*	A region through which a primary flow of charge carriers leaves the base. (Ref. 60 IRE 28.S1)
emitter (E, e)*	A region from which charge carriers that are minority carriers in the base are injected into the base. (Ref. 60 IRE 28.S1)
junction, collector	A semiconductor junction normally biased in the high-resistance direction, the current through which can be controlled by the introduction of minority carriers into the base. (Ref. 60 IRE 28.S1)
junction, emitter	A semiconductor junction normally biased in the low-resistance direction to inject minority carriers into the base. (Ref. 60 IRE 28.S1)
open-circuit	A circuit shall be considered as open-circuited if halving the magnitude of the terminating impedance does not produce a change in the parameter being measured greater than the required accuracy of the measurement. (Ref MIL-S-19500D par. 20.8)
reverse current	The current that flows through a semiconductor junction in the reverse direction.

*NOTE: References to base, collector, and emitter symbolism (B, b, C, c, E, and e) refer to the device terminals connected to those regions.

TERMS AND DEFINITIONS

POWER TRANSISTORS

1

Term	Definition
reverse direction	The direction of current flow which results when the n-type semiconductor region is at a positive potential relative to the p-type region.
saturation	A base-current and a collector-current condition resulting in a forward-biased collector junction.
second breakdown	A condition of the transistor, resulting from a lateral current instability, in which the electrical characteristics are determined principally by the spreading resistance of a thermally maintained current constriction. The initiation of second breakdown is observed as a decrease in the voltage sustained by the collector. NOTE: Second breakdown differs from thermal failure in that its initiation can not be predicted from low-voltage thermal resistance measurements. Unless the current and duration in second breakdown are limited, the high junction temperature at the current constriction will result in failure, usually as a collector-to-emitter short-circuit. Second breakdown can occur at positive, negative, or zero base current. (To protect a transistor against second breakdown, see section: "Safe Operating Areas for Power Transistors.")
semiconductor device	A device whose essential characteristics are due to the flow of charge carriers within a semiconductor. (Ref. RS-282 par. 1.09)
semiconductor junction	A region of transition between semiconductor regions of different electrical properties (e.g., n-n+, p-n, p-p+ semiconductors), or between a metal and a semiconductor. (Ref. RS-282 par. 1.0)
short-circuit	A circuit in which doubling the magnitude of the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. (Ref. MIL-S-19500D par. 20.16)
small-signal	A signal which when doubled in magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. (Ref. MIL-S-19500D par. 20.17)
static value	A non-varying value or quantity of measurement at a specified fixed point, or the slope of the line from the origin to the operating point on the appropriate characteristic curve. (Ref. IEEE #255 par. 2.2.1)
terminal	An externally available point of connection to one or more electrodes. (Ref. RS-282 par. 1.14)
thermal resistance (steady-state)	The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium. (Ref. IEEE #223)

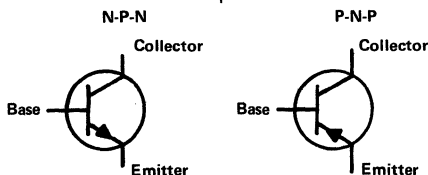
TERMS AND DEFINITIONS POWER TRANSISTORS

1

Term	Definition
transient thermal impedance	The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval causing the change of temperature difference. (Ref. IEEE #223)
transistor	An active semiconductor device capable of providing power amplification and having three or more terminals. (Ref. IEC #147-0 par. 0-2.8)
transistor, junction, multijunction type	A transistor having a base and two or more junctions.

Graphic symbols for emitter, base, collector transistors: (Ref. ANS Y32.2)

NOTE: In the graphic symbols, the envelope is optional if no element is connected to the envelope.



TERMS AND DEFINITIONS

POWER TRANSISTORS

Power Transistor Letter Symbols, Terms, and Definitions

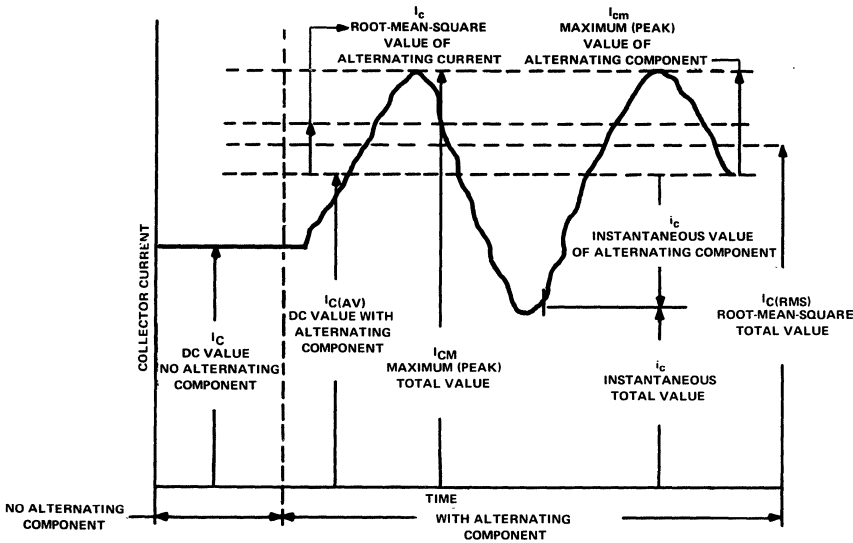
Symbol	Term	Definition
C_{ibo}	open-circuit input capacitance	The capacitance measured across the input terminals (emitter and base) with the collector open-circuited for ac. (Ref. IEEE #255)
C_{obo}	open-circuit output capacitance	The capacitance measured across the output terminals (collector and base) with the input open-circuited to ac. (Ref. IEEE #255)
f_{hfe}	small-signal short-circuit forward current transfer ratio cutoff frequency (common-emitter)	The lowest frequency at which the magnitude of the small-signal short-circuit forward current transfer ratio is 0.707 of its value at a specified low frequency (usually 1 kHz or less). (Ref. IEEE #255)
f_T	transition frequency or frequency at which small-signal forward current transfer ratio (common-emitter) extrapolates to unity	The product of the modulus (magnitude) of the common-emitter small-signal short-circuit forward current transfer ratio, h_{fe} , and the frequency of measurement when this frequency is sufficiently high so that the modulus (magnitude) of h_{fe} is decreasing with a slope of approximately 6 dB per octave. (Ref. IEEE #255)
G_{PE}	large-signal insertion power gain (common-emitter)	The ratio, usually expressed in dB, of the signal power delivered to the load to the large-signal power delivered to the input.
h_{FE}	static forward current transfer ratio (common-emitter)	The ratio of the dc collector current to the dc base current. (Ref. MIL-S-19500D par. 30.28)
h_{fe}	small-signal short-circuit forward current transfer ratio (common-emitter)	The ratio of the ac collector current to the small-signal ac base current with the collector short-circuited to the emitter for ac. (Ref. MIL-S-19500D par. 30.20)
h_{iE}	static input resistance (common-emitter)	The ratio of the dc base-emitter voltage to the dc base current. (Ref. MIL-S-19500D par. 30.29)
h_{ie}	small-signal short-circuit input impedance (common-emitter)	The ratio of the small-signal ac base-emitter voltage to the ac base current with the collector short-circuited to the emitter for ac. (Ref. MIL-S-19500D par. 30.24)
$h_{ie(imag)}$	imaginary part of the small-signal short-circuit input impedance, (common-emitter)	The ratio of the out-of-phase (imaginary) component of the small-signal ac base-emitter voltage to the ac base current with the collector terminal short-circuited to the emitter terminal for ac.
$h_{ie(real)}$	real part of the small-signal short-circuit input impedance, (common-emitter)	The ratio of the in-phase (real) component of the small-signal ac base-emitter voltage to the ac base current with the collector terminal short-circuited to the emitter terminal for ac.
h_{oe}	small-signal open-circuit output admittance, (common-emitter)	The ratio of the ac collector current to the small-signal ac collector-emitter voltage with the base terminal open-circuited to ac. (Ref. MIL-S-19500D par. 30.15)

TERMS AND DEFINITIONS POWER TRANSISTORS

1

Symbol	Term	Definition
$h_{oe(imag)}$	imaginary part of the small-signal open-circuit output admittance, (common-emitter)	The ratio of the ac collector current to the out-of-phase (imaginary) component of the small-signal collector-emitter voltage with the base terminal open-circuited to ac.
$h_{oe(real)}$	real part of the small-signal open-circuit output admittance, (common-emitter)	The ratio of the ac collector current to the in-phase (real) component of the small-signal collector-emitter voltage with the base terminal open-circuited to ac.
I_B , I_C , I_E	current, dc (base-terminal, collector-terminal, emitter-terminal)	The value of the dc current into the terminal indicated by the subscript.
I_b , I_c , I_e	current, rms value of alternating component (base-terminal, collector-terminal, emitter-terminal)	The root-mean-square value of alternating current into the terminal indicated by the subscript.
i_B , i_C , i_E	current, instantaneous total value (base-terminal, collector-terminal, emitter-terminal)	The instantaneous total value of alternating current into the terminal indicated by the subscript.

DIAGRAM ILLUSTRATING FOREGOING CURRENTS (Ref IEEE # 255)



I_{CBO}	collector cutoff current, dc, emitter open	The dc current into the collector terminal when it is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited. (Ref. IEEE #255)
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TERMS AND DEFINITIONS

POWER TRANSISTORS

1

Symbol	Term	Definition
I_{CEO}	collector cutoff current, dc (base open	<p>The dc current into the collector terminal when it is biased in the reverse direction* with respect to the emitter terminal and the base terminal is (as indicated by the first subscript letter as follows):</p> <p>O = open-circuited</p> <p>R = returned to the emitter terminal through a specified resistance.</p> <p>S = short-circuited to the emitter terminal.</p> <p>V = returned to the emitter terminal through a specified voltage.</p> <p>X = returned to the emitter terminal through a specified circuit.</p> <p>(Ref. IEEE #255)</p>
I_{CER}	resistance between base and emitter,	
I_{CES}	base short-circuited to emitter,	
I_{CEV}	voltage between base and emitter,	
I_{CEX}	circuit between base and emitter)	
I_{EBO}	emitter cutoff current, dc, collector open	The dc current into the emitter terminal when it is biased in the reverse direction with respect to the base terminal and the collector terminal is open-circuited. (Ref. IEEE #255)
P_{BE}	power input, dc (to the base, common-emitter)	The product of the dc input current and voltage with the common-emitter circuit configuration.
P_{BE}	power input; instantaneous total (to the base, common-emitter)	The product of the instantaneous input current and voltage with the common-emitter circuit configuration.
P_{OE}	large-signal output power (common-emitter)	The product of the large-signal ac output current and voltage with the common-emitter circuit configuration.
P_T	total nonreactive power input to all terminals	<p>The sum of the products of the dc input currents and voltages, i.e..</p> <p>$V_{BE} \cdot I_B + V_{CE} \cdot I_C$ or</p> <p>$V_{BE} \cdot I_E + V_{CB} \cdot I_C$</p>
P_T	nonreactive power input, instantaneous total, to all terminals	The sum of the products of the instantaneous input currents and voltages.
$r_b' C_c$	collector-base time constant	The product of the intrinsic base resistance and collector capacitance under specified small-signal conditions.

*For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for N-P-N transistors or negative for P-N-P transistors with respect to the emitter terminal.

TERMS AND DEFINITIONS POWER TRANSISTORS

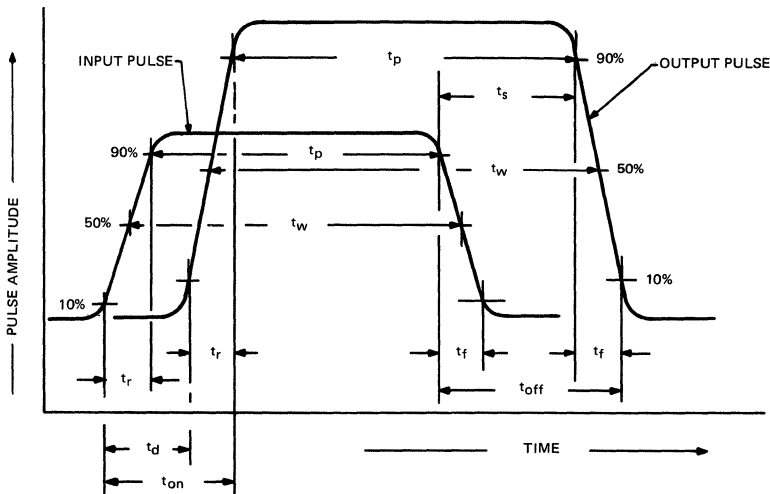
Symbol	Term	Definition
R_{θ} (formerly θ)	thermal resistance	Refer to thermal resistance (steady state), page 1-4.
$R_{\theta CA}$	thermal resistance case-to-ambient	The thermal resistance (steady-state) from the device case to the ambient.
$R_{\theta JA}$ (formerly θ_{J-A})	thermal resistance junction-to-ambient	The thermal resistance (steady-state) from the semiconductor junction (s) to the ambient.
$R_{\theta JC}$ (formerly θ_{J-C})	thermal resistance junction-to-case	The thermal resistance (steady-state) from the semiconductor junction (s) to a stated location on the case.
$R_{\theta JM}$	thermal resistance junction-to-mounting surface	The thermal resistance (steady-state) from the semiconductor junction (s) to a stated location on the mounting surface.
T_A	ambient temperature or free-air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces. (Ref. MIL-S-19500D par. 20.20.1)
T_C	case temperature	The temperature measured at a specified location on the case of a device. (Ref. MIL-S-19500D par. 20.20.2)
T_J	virtual junction temperature	A theoretical temperature based on a simplified representation of the thermal and electrical behavior of the semiconductor device. NOTE: This term (and its definition) is taken from IEC standards. It is particularly applicable to multi-junction semiconductors and is used in this publication to denote the temperature of the active semiconductor element when required in specifications and test methods. The term "junction temperature" is used interchangeably with the term "virtual junction temperature" in this publication.
T_{stg}	storage temperature	The temperature at which the device, without any power applied, is stored. (Ref. MIL-S-19500D par. 20.20.3)
t_d	delay time	The time interval from the point at which the leading edge of the input pulse has reached 10 percent of its maximum amplitude to the point at which the leading edge of the output pulse has reached 10 percent of its maximum amplitude. (Ref. MIL-S-19500D par. 20.13)
t_f	fall time	The time duration during which the trailing edge of a pulse is decreasing from 90 to 10 percent of its maximum amplitude. (Ref. MIL-S-19500D par. 20.12)

TERMS AND DEFINITIONS

POWER TRANSISTORS

Symbol	Term	Definition
t_{off}	turn-off time	The sum of $t_s + t_f$.
t_{on}	turn-on time	The sum of $t_d + t_r$.
t_p	pulse time	The time duration from the point on the leading edge which is 90 percent of the maximum amplitude to the point on the trailing edge which is 90 percent of the maximum amplitude. (Ref. MIL-S-19500D par. 20.15)
t_r	rise time	The time duration during which the amplitude of the leading edge of a pulse is increasing from 10 to 90 percent of its maximum amplitude. (Ref. MIL-S-19500D par. 20.13)
t_s	storage time	The time interval from a point 90 percent of the maximum amplitude on the trailing edge of the input pulse to a point 90 percent of the maximum amplitude on the trailing edge of the output pulse. (Ref. MIL-S-19500D par. 20.14)
t_w	pulse average time	The time duration from the point on the leading edge which is 50 percent of the maximum amplitude to a point on the trailing edge which is 50 percent of the maximum amplitude. (Ref. MIL-S-19500D par. 20.10)

DIAGRAM ILLUSTRATING PULSE TIME SYMBOLOGY



TERMS AND DEFINITIONS

POWER TRANSISTORS

Symbol	Term	Definition
$V_{(BR)CBO}$ (formerly BV_{CBO})	breakdown voltage collector-to-base, emitter open	The breakdown voltage between the collector terminal and the base terminal when the collector terminal is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited. (Ref. IEEE #255)
$V_{(BR)CEO}$ (formerly BV_{CEO})	breakdown voltage, collector-to-emitter with (base open,	<p>The breakdown voltage between the collector terminal and the emitter terminal when the collector terminal is biased in the reverse direction* with respect to the emitter terminal and the base terminal is (as indicated by the last subscript letter as follows):</p> <p>O = open-circuited.</p> <p>R = returned to the emitter terminal through a specified resistance.</p> <p>S = short-circuited to the emitter terminal.</p> <p>V = returned to the emitter terminal through a specified voltage.</p> <p>X = returned to the emitter terminal through a specified circuit.</p> <p>(Ref. IEEE #255)</p>
$V_{(BR)CER}$ (formerly BV_{CER})	resistance between base and emitter,	
$V_{(BR)CES}$ (formerly BV_{CES})	base short-circuited to emitter,	
$V_{(BR)CEV}$ (formerly BV_{CEV})	voltage between base and emitter,	
$V_{(BR)CEX}$ (formerly BV_{CEX})	circuit between base and emitter)	
$V_{(BR)EBO}$ (formerly BV_{EBO})	breakdown voltage, emitter-to-base, collector open	The breakdown voltage between the emitter and base terminals when the emitter terminal is biased in the reverse direction with respect to the base terminal and the collector terminal is open-circuited. (Ref. IEEE #255)
V_{BB} , V_{CC} , V_{EE}	supply voltage, dc (base, collector, emitter)	The dc supply voltage applied to a circuit connected to the reference terminal.
V_{BC} , V_{BE} , V_{CB} , V_{CE} , V_{EB} , V_{EC}	voltage, dc or average (base-to-collector, base-to-emitter, collector-to-base, collector-to-emitter, emitter-to-base, emitter-to-collector)	<p>The dc voltage between the terminal indicated by the first subscript and the reference terminal (stated in terms of the polarity at the terminal indicated by the first subscript).</p>
$V_{BE(sat)}$	saturation voltage, dc, base-to-emitter	

*For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for N-P-N transistors or negative for P-N-P transistors with respect to the emitter terminal.

TERMS AND DEFINITIONS

POWER TRANSISTORS

1

Symbol	Term	Definition
V_{CB0}	collector-to-base voltage, dc, emitter open	The dc voltage between the collector terminal and the base terminal when the emitter terminal is open-circuited.
$V_{CE(sat)}$	saturation voltage, dc, collector-to-emitter	The dc voltage between the collector and the emitter terminals for specified saturation conditions. (Ref. IEEE #255)
V_{CEO}	collector-to-emitter voltage, dc, with (base open,	<p>The dc voltage between the collector terminal and the emitter terminal when the base terminal is (as indicated by the last subscript letter):</p> <p>O = open-circuited.</p> <p>R = returned to the emitter terminal through a specified resistance.</p> <p>S = short-circuited to the emitter terminal.</p> <p>V = returned to the emitter terminal through a specified voltage.</p> <p>X = returned to the emitter terminal through a specified circuit.</p>
V_{CER}	resistance between base and emitter,	
V_{CES}	base short-circuited to emitter,	
V_{CEV}	voltage between base and emitter,	
V_{CEX}	circuit between base and emitter)	
$V_{CEO(sus)}$	sustaining voltage, collector-to-emitter with (base open,	
$V_{CER(sus)}$	resistance between base and emitter,	<p>The collector-to-emitter breakdown voltage at relatively high values of collector current where the breakdown voltage is relatively insensitive to changes in collector current. The base terminal is (as indicated by the third subscript letter as follows):</p> <p>O = open-circuited</p> <p>R = returned to the emitter terminal through a specified resistance</p> <p>S = short-circuited to the emitter terminal</p> <p>V = returned to the emitter terminal through a specified voltage</p> <p>X = returned to the emitter terminal through a specified circuit.</p> <p>NOTE: This would be the transient voltage between the collector and emitter terminals during switching with an inductive load from a forward-biased base-emitter to an external condition described by the third subscript letter.</p>
$V_{CES(sus)}$	base short-circuited to emitter,	
$V_{CEV(sus)}$	voltage between base and emitter,	
$V_{CEX(sus)}$	circuit between base and emitter)	
$V_{EB(f)}$	dc open-circuit voltage (floating potential) (emitter-to-base)	

TERMS AND DEFINITIONS

POWER TRANSISTORS

Symbol	Term	Definition
V_{EBO}	emitter-to-base voltage, dc, collector open	The dc voltage between the emitter terminal and the base terminal with the collector terminal open-circuited.
$Z\theta(t)$ (formerly $\theta(t)$)	transient thermal impedance	Refer to transient thermal impedance, page 1-5.
$Z\theta_{JA}(t)$ (formerly $\theta_{J-A}(t)$)	transient thermal impedance, junction-to-ambient	The transient thermal impedance from the semiconductor junction (s) to the ambient.
$Z\theta_{JC}(t)$ (formerly $\theta_{JC}(t)$)	transient thermal impedance, junction-to-case	The transient thermal impedance from the semiconductor junction (s) to a stated location on the case.

TERMS AND DEFINITIONS

THYRISTORS

THYRISTORS

Thyristor Standards

The documents listed below have overriding authority where any conflict may occur with this data book.

EIA and JEDEC Standards

The thyristor terms and definitions presented in this data book were obtained from EIA Standards Proposal No. 1101. This standard is in the process of publication and will be available from:

Electronic Industries Association
2001 Eye St. N.W.,
Washington, D.C. 20006
Telephone: 202-659-2200

IEEE Standards

Institute of Electrical and Electronic Engineers, Inc.
345 East 47th. Street
New York, N.Y. 10017

IEEE No. 233: Standard Definitions of Terms for Thyristors

International Electrotechnical Commission Standards

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

IEC Publication 147-IC: Essential Ratings and Characteristics of Semiconductor Devices and General Principles of Measuring Methods

IEC Publication 148: Letter Symbols for Semiconductor Devices and Integrated Circuits

IEC Publication 191: Mechanical Standardization of Semiconductor Devices.

Military Standards

Commanding Officer, U.S. Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, Pa., 19120

MIL-S-19500: Semiconductor Devices, General Specification for

MIL-STD-105: Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-202: Test Methods for Electronic and Electrical Component Parts

MIL-STD-750: Test Methods for Semiconductor Devices

Classes of Thyristors

Bidirectional Diode Thyristor

A two-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic. (See Figure 4).

Bidirectional Triode Thyristor

A three-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic. (See Figure 4).

N-Gate Thyristor

A thyristor in which the gate terminal is connected to the N-region adjacent to the region to which the anode terminal is connected and which is normally switched to the on-state by applying a negative signal between gate and anode terminals.

P-Gate Thyristor

A thyristor in which the gate terminal is connected to the P-region adjacent to the region to which the cathode terminal is connected and which is normally switched to the on-state by applying a positive signal between gate and cathode terminals.

Reverse-Blocking Diode Thyristor

A two-terminal thyristor which switches only for positive anode-to-cathode voltages and exhibits a reverse-blocking state for negative anode-to-cathode voltages.

Reverse-Blocking Triode Thyristor

A three-terminal thyristor which switches only for positive anode-to-cathode voltages and exhibits a reverse-blocking state for negative anode-to-cathode voltages.

Reverse-Conducting Diode Thyristor

A two-terminal thyristor which switches only for positive anode-to-cathode voltages and conducts large currents at negative anode-to-cathode voltages comparable in magnitude to the on-state voltage.

Reverse-Conducting Triode Thyristor

A three-terminal thyristor which switches only for positive anode-to-cathode voltages and conducts large currents at negative anode-to-cathode voltages comparable in magnitude to the on-state voltage.

Semiconductor Controlled Rectifier (SCR)

An alternative name used for the reverse-blocking triode thyristor.

NOTE: Although not an official definition, the term unidirectional is sometimes used to describe the single switching class of thyristors consisting of reverse-blocking and reverse-conducting thyristors. This term is useful for comparing or contrasting this class of thyristor with bidirectional thyristors.

Thyristor

A bistable semiconductor device comprising three or more junctions, which can be switched from the off-state to the on-state or vice versa, such switching occurring within at least one quadrant of the principle voltage-current characteristic. (See Figures 1 through 5).

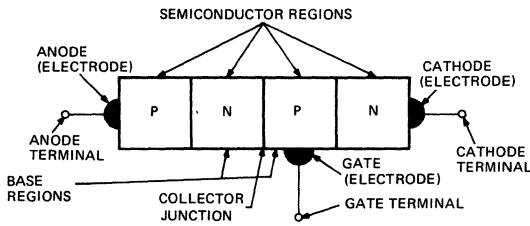
Turn-Off Thyristor

A thyristor which can be switched from the on-state to the off-state and vice versa by applying control signals of appropriate polarities to the gate terminal, with the ratio of triggering power to triggered power appreciably less than one.

TERMS AND DEFINITIONS

THYRISTORS

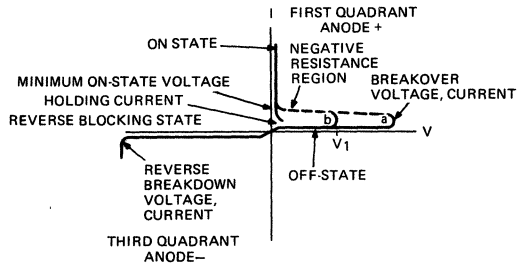
1



Schematic representation of a reverse-blocking triode thyristor.

Note: The gate electrode is connected to the N-type base region in some structures or omitted in the case of a diode thyristor.

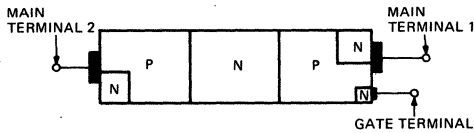
FIGURE 1



Principal voltage-current characteristics (anode-to-cathode voltage-current characteristic) of a typical reverse-blocking thyristor.

Note: Curve "a" applies for zero gate current or a diode thyristor. Curve "b" is with gate trigger current present when off-state voltage is V_1 .

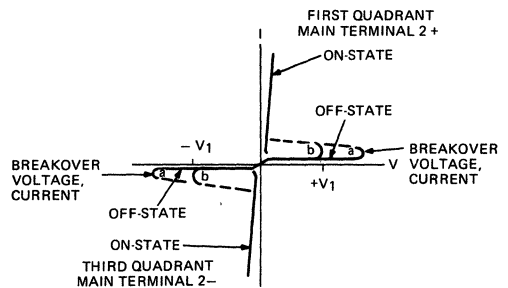
FIGURE 2



Schematic representation of typical bidirectional triode thyristor.

Note: Gate is omitted in a diode bidirectional thyristor.

FIGURE 3



Principal voltage-current characteristic of a typical bidirectional thyristor.

Note: Curve "a" applies for zero gate current or a diode bidirectional thyristor. Curve "b" applies for the case of gate trigger current applied when the off-state voltage is $\pm V_1$.

FIGURE 4

Physical Structure Nomenclature

Anode

The electrode by which current enters the thyristor when the thyristor is in the on-state with the gate open-circuited.

NOTE: This term does not apply to bidirectional thyristors.

Anode Terminal

The terminal which is connected to the anode.

NOTE: This term does not apply to bidirectional thyristors.

Cathode

The electrode by which current leaves the thyristor when the thyristor is in the on-state with the gate open-circuited.

NOTE: This term does not apply to bidirectional thyristors.

Cathode Terminal

The terminal which is connected to the cathode.

NOTE: This term does not apply to bidirectional thyristors.

Collector Junction

The junction across which the polarity of the voltage reverses when switching occurs. (See Figure 1).

Electrode (of a Semiconductor Device)

An electrical and mechanical contact to a region of a semiconductor device.

Gate

An electrode connected to one of the semiconductor regions for introducing control current.

Gate Terminal

A terminal which is connected to a gate.

Junction (of a Semiconductor Device)

A region of transition between semiconductor regions of different electrical properties (e.g., n-n⁺, p-n, p-p⁺ semiconductors), or between a metal and a semiconductor.

Main Terminals

The terminals through which the principal current flows.

Main Terminal 1 (of a Bidirectional Thyristor)

The main terminal which is named "1" by the device manufacturer. This is normally the reference terminal for all voltages.

Main Terminal 2 (of a Bidirectional Thyristor)

The main terminal which is named "2" by the device manufacturer.

Terminal (of a Semiconductor Device)

The externally available point of connection to one or more electrodes.

TERMS AND DEFINITIONS

THYRISTORS

Electrical Characteristic and Rating Terms (See Note at end of section)

Anode-to-Cathode Voltage (Anode Voltage)

The voltage between the anode terminal and the cathode terminal.

NOTE: It is called positive when the anode potential is more positive than the cathode potential, and called negative when the anode potential is less positive than the cathode potential.

Anode-to-Cathode Voltage-Current Characteristic (Anode Characteristic)

A function, usually represented graphically, relating the anode-to-cathode voltage to the principal current with gate current, where applicable, as a parameter.

NOTE: This term does not apply to bidirectional thyristors.

Breakover Point

Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value. (See Figures 2 and 4).

Negative-Differential-Resistance Region

Any portion of the principal voltage-current characteristic in the switching quadrant(s) within which the differential resistance is negative. (See Figures 2 and 4).

Off-Impedance

The differential impedance between the terminals through which the principal current flows when the thyristor is in the off-state at a stated operating point.

Off-State

The condition of the thyristor corresponding to the high-resistance, low-current portion of the principal voltage-current characteristic between the origin and the breakover point(s) in the switching quadrant(s).

On-Impedance

The differential impedance between the terminals through which the principal current flows when the thyristor is in the on-state at a stated operating point.

On-State

The condition of the thyristor corresponding to the low-resistance, low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).

NOTE: In the case of reverse-conducting thyristors, this definition is applicable only for a positive anode-to-cathode voltage.

Principal Voltage

The voltage between the main terminals.

NOTES: 1. In the case of reverse-blocking and reverse-conducting thyristors, the principal voltage is called positive when the anode potential is more positive than the cathode potential, and called negative when the anode potential is less positive than the cathode potential.

2. For bidirectional thyristors, the principal voltage is called positive when the potential of main terminal 2 is more positive than the potential of main terminal 1.

Principal Voltage-Current Characteristic (Principal Characteristic)

The function, usually represented graphically, relating the principal voltage to the principal current with gate current, where applicable, as a parameter.

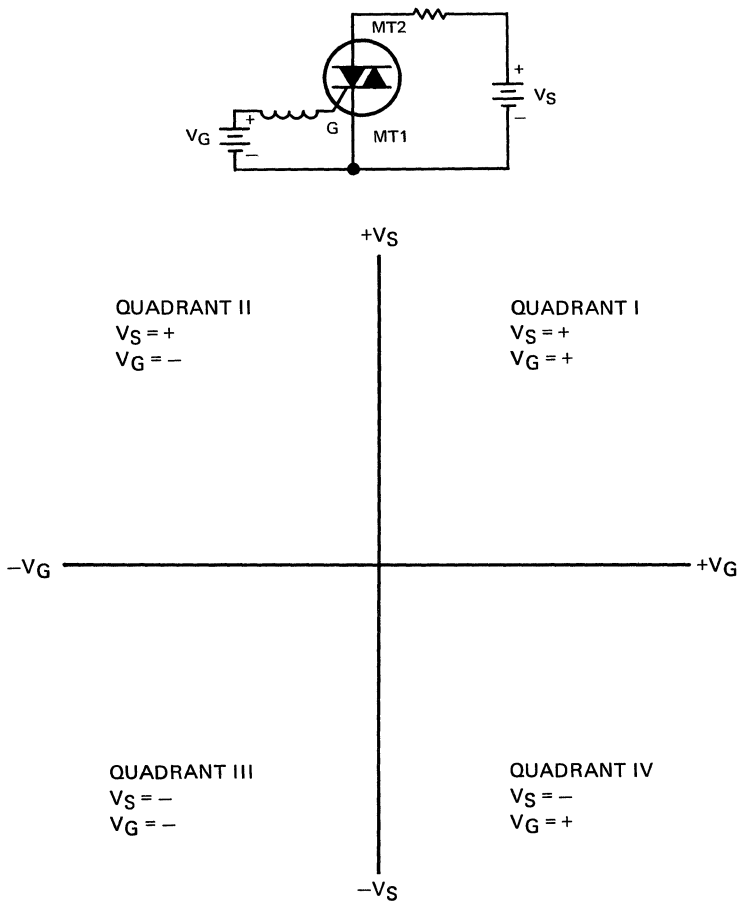
Reverse-Blocking Impedance (of a Reverse-Blocking Thyristor)

The differential impedance between the two terminals through which the principal current flows when the thyristor is in the reverse-blocking state at a stated operating point.

Reverse-Blocking State (of a Reverse-Blocking Thyristor)

The condition of a reverse-blocking thyristor corresponding to the portion of the anode-to-cathode voltage-current characteristic for which reverse currents are of lower magnitude than the reverse breakdown current. (See Figure 2).

QUADRANT DEFINITIONS



The polarities of V_S and V_G are with respect to Main Terminal 1.

FIGURE 5

TERMS AND DEFINITIONS

THYRISTORS

Symbols, Terms and Definitions

Symbol	Term	Definition
$I_{(BO)}$	Static Breakover Current	The principal current at the breakover point.
$i_{(BO)}$	Instantaneous Breakover Current	
$I_{(BR)R}$	Static Reverse Breakdown Current	The principal current at the reverse breakdown voltage.
$i_{(BR)R}$	Instantaneous Reverse Breakdown Current	
$I_{D(RMS)}$	RMS Off-State Current	The principal current when the thyristor is in the off-state.
I_D	Static Off-State Current	
$I_{D(AV)}$	Average Off-State Current	
i_D	Instantaneous Off-State Current	
I_{DM}	Peak Off-State Current	
I_{DRM}	Repetitive Peak Off-State Current	The maximum instantaneous value of the off-state current that results from the application of repetitive peak off-state voltage.
I_G	Static Gate Current	The current that results from the gate voltage. NOTES: 1. Positive gate current refers to conventional current entering the gate terminal. 2. Negative gate current refers to conventional current leaving the gate terminal.
$I_{G(AV)}$	Average Gate Current	
i_G	Instantaneous Gate Current	
I_{GM}	Peak Gate Current	
I_{GD}	Static Gate Nontrigger Current	The maximum gate current which will not cause the thyristor to switch from the off-state to the on-state.
i_{GD}	Instantaneous Gate Nontrigger Current	
I_{GDM}	Peak Gate Nontrigger Current	
I_{GQ}	Static Gate Turn-Off Current	The minimum gate current required to switch a thyristor from the on-state to the off-state.
i_{GQ}	Instantaneous Gate Turn-Off Current	
I_{GQM}	Peak Gate Turn-Off Current	
I_{GT}	Static Gate Trigger Current	The minimum gate current required to switch a thyristor from the off-state to the on-state.
i_{GT}	Instantaneous Gate Trigger Current	
I_{GTM}	Peak Gate Trigger Current	

TERMS AND DEFINITIONS

THYRISTORS

1

Symbol	Term	Definition
I_H	Static Holding Current	The minimum principal current required to maintain the thyristor in the on-state.
i_H	Instantaneous Holding Current	
I_L	Static Latching Current	The minimum principal current required to maintain the thyristor in the on-state immediately after switching from the off-state to the on-state has occurred and the triggering signal has been removed.
i_L	Instantaneous Latching Current	
$I_R(RMS)$	RMS Reverse Current	The current for negative anode-to-cathode voltage.
I_R	Static Reverse Current	
$I_R(AV)$	Average Reverse Current	
i_R	Instantaneous Reverse Current	
I_{RM}	Peak Reverse Current	
I_{RRM}	Repetitive Peak Reverse Current	The maximum instantaneous value of the reverse current that results from the application of repetitive peak reverse voltage.
$I_T(RMS)$	RMS On-State Current	The principal current when the thyristor is in the on-state.
I_T	Static On-State Current	
$I_T(AV)$	Average On-State Current	
i_T	Instantaneous On-State Current	
I_{TM}	Peak On-State Current	
$I_T(OV)$	Overload Peak On-State Current	An on-state current of substantially the same waveshape as the normal on-state current and having a greater value than the normal on-state current.
I_{TRM}	Repetitive Peak On-State Current	The peak value of the on-state current including all repetitive transient currents.
I_{TSM}	Surge (Nonrepetitive) Peak On-State Current	An on-state current of short-time duration and specified waveshape.
P_G	Static Gate Power Dissipation	
$P_G(AV)$	Average Gate Power Dissipation	
p_G	Instantaneous Gate Power Dissipation	
P_{GM}	Peak Gate Power Dissipation	

TERMS AND DEFINITIONS

THYRISTORS

Symbol	Term	Definition
T_A	Free-Air Temperature (Ambient Temperature)	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces. (Ref. MIL-S-19500D par. 20.20.1)
T_C	Case Temperature	The temperature measured at a specified location on the case of a device. (Ref. MIL-S-19500D par. 20.20.2)
T_J	Virtual Junction Temperature (Junction Temperature)	A theoretical temperature based on a simplified representation of the thermal and electrical behavior of the semiconductor device. NOTE: This term (and its definition) is taken from IEC standards. It is particularly applicable to multi-junction semiconductors and is used in this publication to denote the temperature of the active semiconductor element when required in specifications and test methods. The term "junction temperature" is used interchangeably with the term "virtual junction temperature" in this publication.
T_{stg}	Storage Temperature	The temperature at which the device, without any power applied, is stored. (Ref. MIL-S-19500D par. 20.20.3)
t_{gt}	Gate-Controlled Turn-On Time	The time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified low (high) value during switching of a thyristor from the off-state to the on-state by a gate pulse.
t_{gq}	Gate-Controlled Turn-Off Time	The time interval between a specified point at the beginning of the gate pulse and the instant when the principal current has decreased to a specified value during switching from the on-state to the off-state by a gate pulse.
t_q	Circuit-Commutated Turn-Off Time	The time interval between the instant when the principal current has decreased to zero after external switching of the principal voltage circuit, and the instant when the thyristor is capable of supporting a specified principal voltage without turning on.

TERMS AND DEFINITIONS

THYRISTORS

1

Symbol	Term	Definition
R_{θ}	Thermal Resistance	The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium.
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	
$R_{\theta CA}$	Thermal Resistance, Case-to-Ambient	
$V_{(BO)}$	Static Breakover Voltage	The principal voltage at the breakover point.
$v_{(BO)}$	Instantaneous Breakover Voltage	
$V_{(BR)R}$	Static Reverse Breakdown Voltage	The value of negative anode-to-cathode voltage at which the differential resistance between the anode and cathode terminals changes from a high value to a substantially lower value.
$v_{(BR)R}$	Instantaneous Reverse Breakdown Voltage	
$V_{D(RMS)}$	RMS Off-State Voltage	The principal voltage when the thyristor is in the off-state.
V_D	Static Off-State Voltage	
$V_{D(AV)}$	Average Off-State Voltage	
v_D	Instantaneous Off-State Voltage	
V_{DM}	Peak Off-State Voltage	
V_{DRM}	Repetitive Peak Off-State Voltage	The maximum instantaneous value of the off-state voltage which occurs across a thyristor, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.
V_{DSM}	Nonrepetitive Peak Off-State Voltage	The maximum instantaneous value of any non-repetitive transient off-state voltage which occurs across the thyristor.
V_{DWM}	Working Peak Off-State Voltage	The maximum instantaneous value of the off-state voltage which occurs across a thyristor, excluding all repetitive and nonrepetitive transient voltages.
V_G	Static Gate Voltage	The voltage between a gate terminal and a specified main terminal. NOTE: Gate voltage polarity is referenced to the specified main terminal.
$V_{G(AV)}$	Average Gate Voltage	
v_G	Instantaneous Gate Voltage	
V_{GM}	Peak Gate Voltage	

TERMS AND DEFINITIONS

THYRISTORS

1

Symbol	Term	Definition
V _{GD}	Static Gate Nontrigger Voltage	The maximum gate voltage which will not cause the thyristor to switch from the off-state to the on-state.
v _{GD}	Instantaneous Gate Nontrigger Voltage	
V _{GDM}	Peak Gate Nontrigger Voltage	
V _{GQ}	Static Gate Turn-Off Voltage	The gate voltage required to produce the gate turn-off current.
v _{GQ}	Instantaneous Gate Turn-Off Voltage	
V _{GQM}	Peak Gate Turn-Off Voltage	
V _{GT}	Static Gate Trigger Voltage	The gate voltage required to produce the gate trigger current.
v _{GT}	Instantaneous Gate Trigger Voltage	
V _{GTM}	Peak Gate Trigger Voltage	
V _{R(RMS)}	RMS Reverse Voltage	A negative anode-to-cathode voltage.
V _R	Static Reverse Voltage	
V _{R(AV)}	Average Reverse Voltage	
v _R	Instantaneous Reverse Voltage	
V _{RM}	Peak Reverse Voltage	
V _{RRM}	Repetitive Peak Reverse Voltage	The maximum instantaneous value of the reverse voltage which occurs across the thyristor, including all repetitive transient voltages, but excluding all nonrepetitive transient voltages.
V _{RSM}	Nonrepetitive Peak Reverse Voltage	The maximum instantaneous value of any nonrepetitive transient reverse voltage which occurs across a thyristor.
V _{RWM}	Working Peak Reverse Voltage	The maximum instantaneous value of the reverse voltage which occurs across the thyristor, excluding all repetitive and nonrepetitive transient voltages.
V _{T(RMS)}	RMS On-State Voltage	The principal voltage when the thyristor is in the on-state.
V _T	Static On-State Voltage	
V _{T(AV)}	Average On-State Voltage	
v _T	Instantaneous On-State Voltage	
V _{TM}	Peak On-State Voltage	

TERMS AND DEFINITIONS THYRISTORS

Symbol	Term	Definition
$V_T(\text{MIN})$	Static Minimum On-State Voltage	The minimum positive principal voltage for which the differential resistance is zero with the gate open-circuited.
$Z_\theta(t)$	Transient Thermal Impedance	The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval causing the change of temperature difference.
$Z_{\theta JA}(t)$	Transient Thermal Impedance, Junction-to-Ambient	
$Z_{\theta JC}(t)$	Transient Thermal Impedance, Junction-to-Case	

1

ELECTRICAL CHARACTERISTIC TESTS

POWER TRANSISTOR ELECTRICAL CHARACTERISTIC TESTS

INDEX

	Page
General	1-28
Measurements	1-28
Cut-off Current [I_{CEO} , I_{EBO} , I_{CBO} , I_{CEV} , I_{EB1} , I_{EB2} , I_{B1B2}]	1-28
Breakdown Voltage [$V_{(BR)CEX}$, $V_{(BR)CEO}$ or $V_{CEO(sus)}$, $V_{(BR)CES}$, $V_{(BR)EBO}$, $V_{(BR)CER}$]	1-30
Floating Potential [$V_{EB(f)}$]	1-32
Current Gain [h_{FE}]	1-34
Saturation Voltage [$V_{CE(sat)}$]	1-34
Base-to-Emitter Voltage [V_{BE}]	1-35
Open-Circuit Output Capacitance [C_{obo}]	1-36
Small-Signal Short-Circuit Input Impedance [h_{ie} , $h_{ie(real)}$, $h_{ie(imag)}$]	1-37
Small-Signal Open-Circuit Output Admittance [$h_{oe(real)}$]	1-38
Small-Signal Forward Current Transfer Ratio [h_{fe}], Cut-Off Frequency [f_{hfe}], and Frequency at Which $ h_{fe} $ Extrapolates to Unity [f_T]	1-39
Switching Time [t_d , t_r , t_s , t_f]	1-40

ELECTRICAL CHARACTERISTIC TESTS

GENERAL

In this section, accepted test practices are described as a guide to making power transistor characteristic tests. The material has been adapted from the forthcoming JEDEC Publication *Suggested Standards on Power Transistors*. Only those electrical characteristics included in EIA JC-25 registration formats are listed.

MEASUREMENTS

All measurements should be made at thermal equilibrium. A condition of thermal equilibrium is achieved if halving the time between application of power and measurement causes no change in the result within the required accuracy.

The connecting lines shown in the circuit diagrams have no resistance compared to their lowest terminating impedance. Shown are resistors, inductors, and capacitors having an ideal characteristic at the used frequency range. Voltage sources have zero impedance, and current sources have an infinite resistance. All voltmeters and scopes have infinite input resistance and all ammeters have zero resistance, unless otherwise noted.

The listing of the following tests does not imply that all must be performed by either the manufacturer or the user. It is the responsibility of the user and manufacturer to agree to any series of specific tests or test conditions, and the further responsibility of the user to establish meaningful relationship between these tests and the performance of the power transistor in a particular application.

An npn transistor is used in the test methods below. These test methods will also apply to pnp devices by changing polarities. For small-signal measurements, a signal is used which, when doubled in magnitude, does not produce a change in the measured parameter that is greater than the required accuracy.

The transistor connections are shown separate from the test circuits for "DC", "CT", and "P" techniques.

"DC" — D-C continuous condition

"CT" — Curve tracer (60 cycle full rectified sinewave)

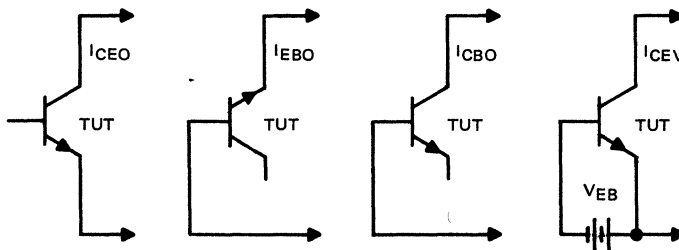
"P" — Pulsed by a 300 μ s, 2% duty cycle pulse

CUT-OFF CURRENT [I_{CEO} , I_{EBO} , I_{CBO} , I_{CEV} , I_{EB1} , I_{EB2} , I_{B1B2}]

Description

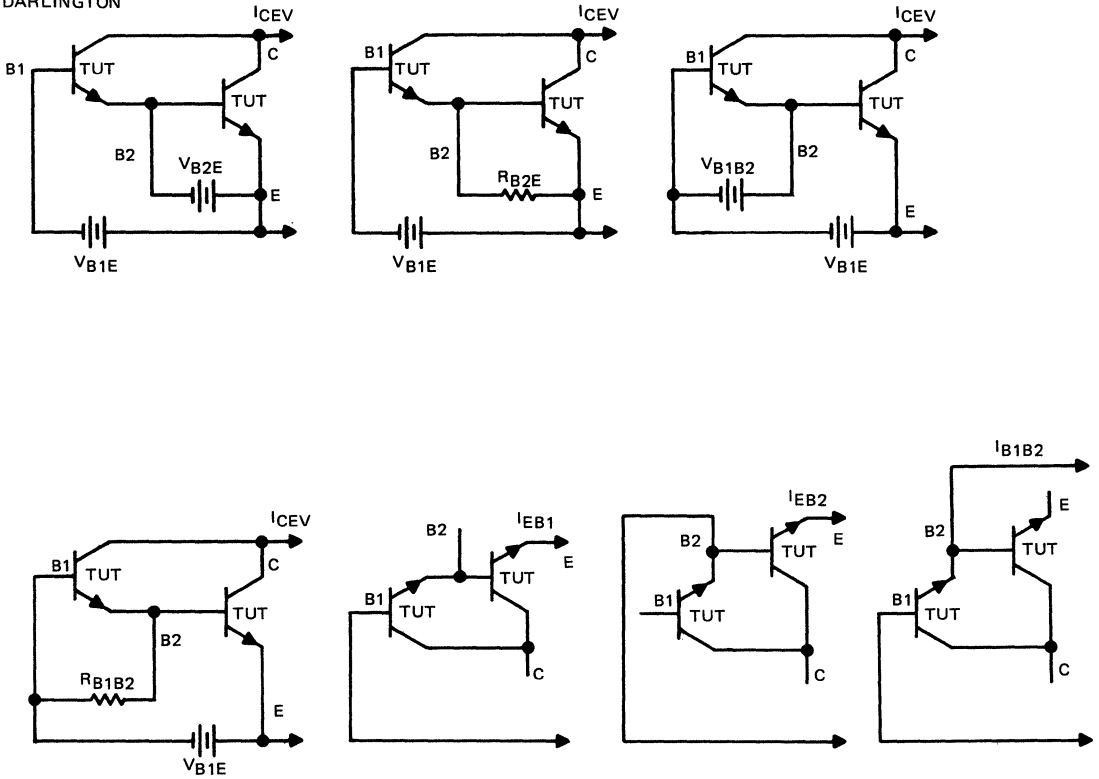
The reverse voltage is applied and the cut-off current is measured. The cut-off current is temperature sensitive. If testing is done at elevated temperature, a heat sink may be necessary to prevent thermal runaway.

Transistor Connections



ELECTRICAL CHARACTERISTIC TESTS

DARLINGTON

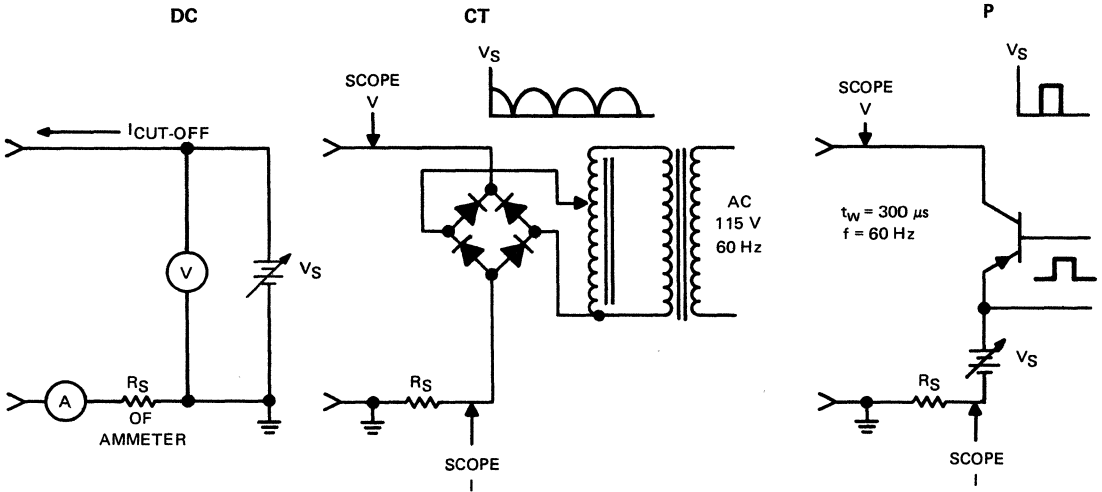


Test Circuits

The supply voltage V_S should equal $R_S I_{CUT-OFF}$ plus the specified test voltage. The current of the transistor in the pulse test circuit has to be small compared to the measured cut-off current. The cut-off current is measured with an ammeter or with an oscilloscope.

ELECTRICAL CHARACTERISTIC TESTS

1



Test Conditions to be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

Voltage applied to the device: V_{CE0} , V_{EB0} , V_{CB0} , V_{CEV} , V_{EB1} , V_{B1B2} , V_{EB2}

Base termination: V_{EB} , V_{B2E} , R_{B2E} , V_{B1B2} , R_{B1B2}

Technique: DC, CT, P

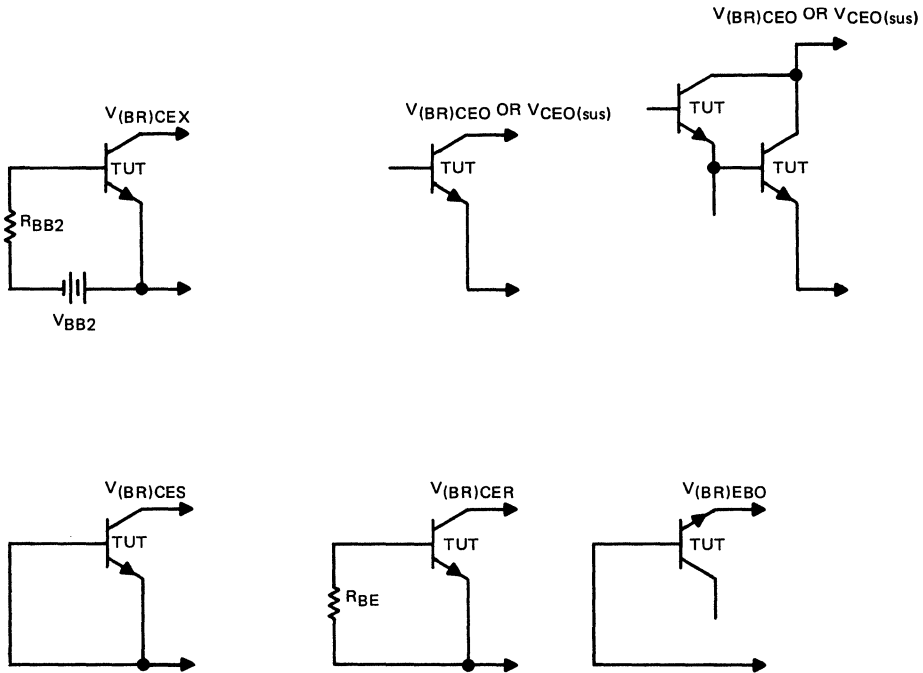
BREAKDOWN VOLTAGE [$V_{(BR)CEX}$, $V_{(BR)CEO}$ OR $V_{CE0(sus)}$, $V_{(BR)CES}$, $V_{(BR)EBO}$, $V_{(BR)CER}$]

Description

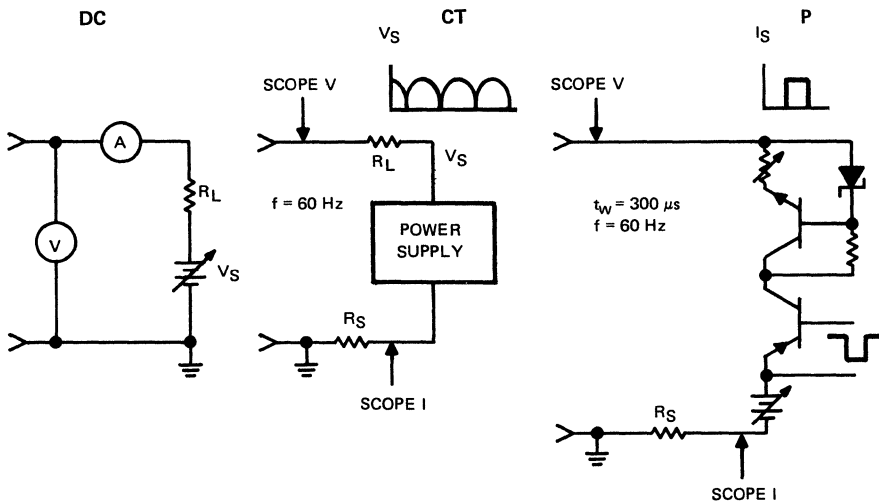
For breakdown measured in the sustaining region, the current should be high enough to ensure that the breakdown voltage is relatively insensitive to current changes.

ELECTRICAL CHARACTERISTIC TESTS

Transistor Connections

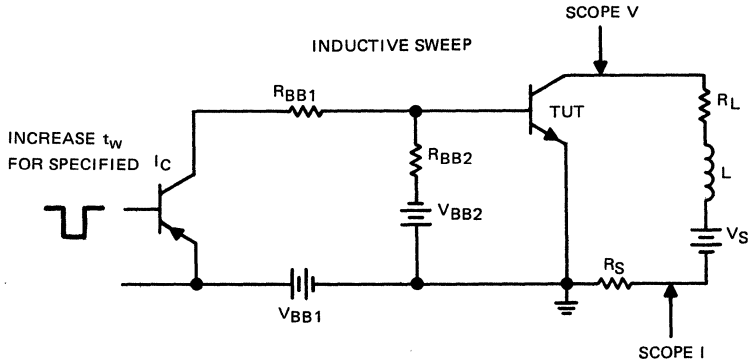


Test Circuits



ELECTRICAL CHARACTERISTIC TESTS

1



In addition to the test circuits for "DC", "CT", and "P", an inductive sweep circuit is shown. This test circuit is particularly useful to measure transistors in their sustaining region.

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

Current applied to the device: I_{CEX} , I_{CEO} , I_{CES} , I_{EBO} , I_{CER}

Base termination: V_{BB2} , V_{BB1} , R_{BB2} , R_{BB1} , R_{BE} , pulse width, duty cycle

Technique: DC, CT, P, Inductive Sweep

Load resistance, inductance, and supply voltage where applicable: R_L , L , V_S

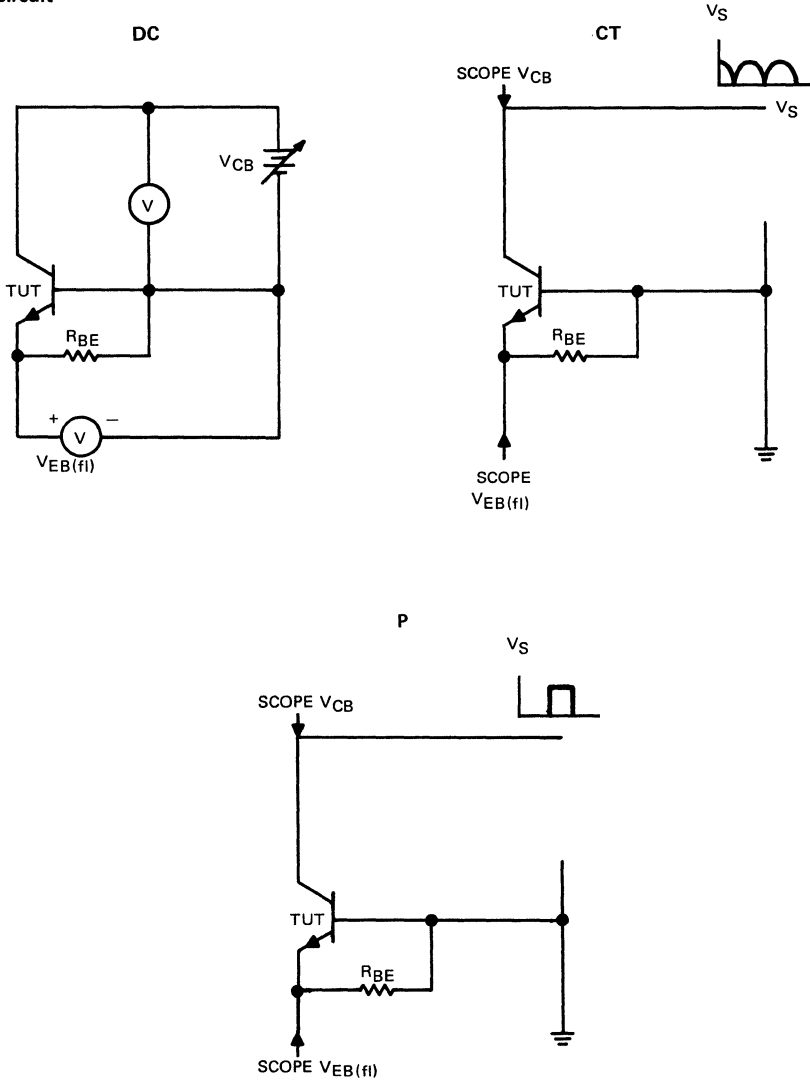
FLOATING POTENTIAL [$V_{EB}(f)$]

Description

This measurement is related to the thickness of the base region.

ELECTRICAL CHARACTERISTIC TESTS

Test Circuit



1

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

Collector-base voltage: V_{CB}

Base-emitter resistance: R_{BE}

Technique: DC, CT, P

ELECTRICAL CHARACTERISTIC TESTS

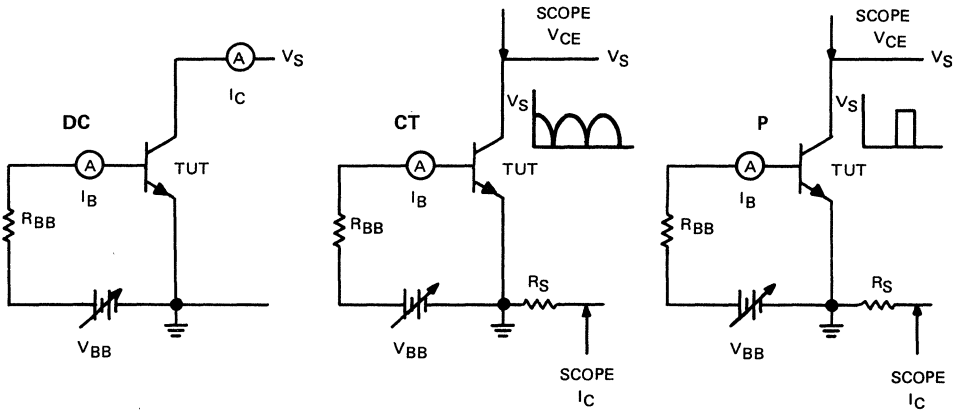
1

CURRENT GAIN [h_{FE}]

Description

The static forward current transfer ratio in the common-emitter configuration is one of the most important gain characteristic for power transistors. It measures the ratio of collector current to base current.

Test Circuit



The current gain is given by $h_{FE} = I_C/I_B$. For the CT and P tests, $V_{BB} \gg \Delta V_{BE}^*$ so that I_B is constant and relatively independent of V_{BE} .

* ΔV_{BE} is the range of V_{BE} for various devices to be tested.

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

Collector-emitter voltage: V_{CE}

Collector current: I_C

Technique: DC, CT, P

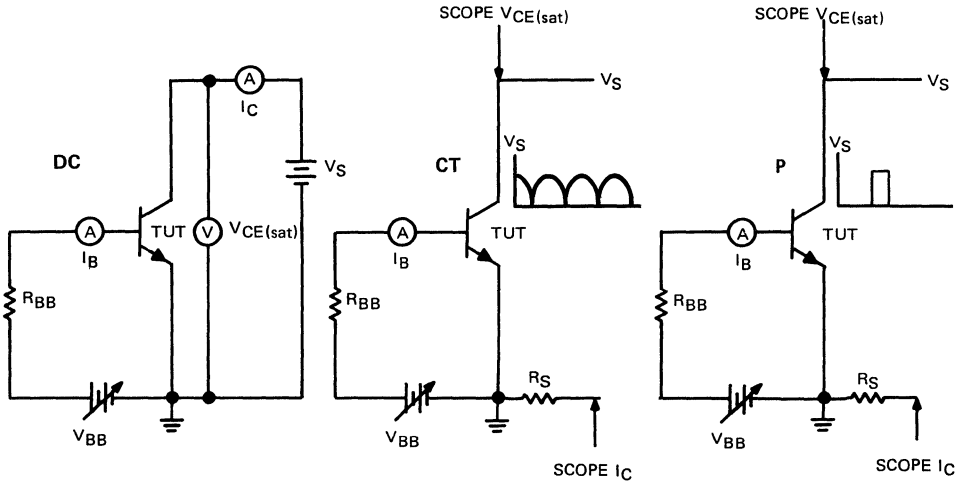
SATURATION VOLTAGE [$V_{CE(sat)}$]

Description

The collector-to-emitter saturation voltage is especially important for switching applications. Together with the collector current, it is the basis to calculate the power dissipation in the "on" state.

ELECTRICAL CHARACTERISTIC TESTS

Test Circuit



For the CT and P tests, $V_{BB} \gg V_{BE}$ in order to make I_B independent of V_{BE} changes during the "on" condition.

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

Collector current: I_C

Base current: I_B

Technique: DC, CT, P

BASE-TO-EMITTER VOLTAGE [V_{BE}]

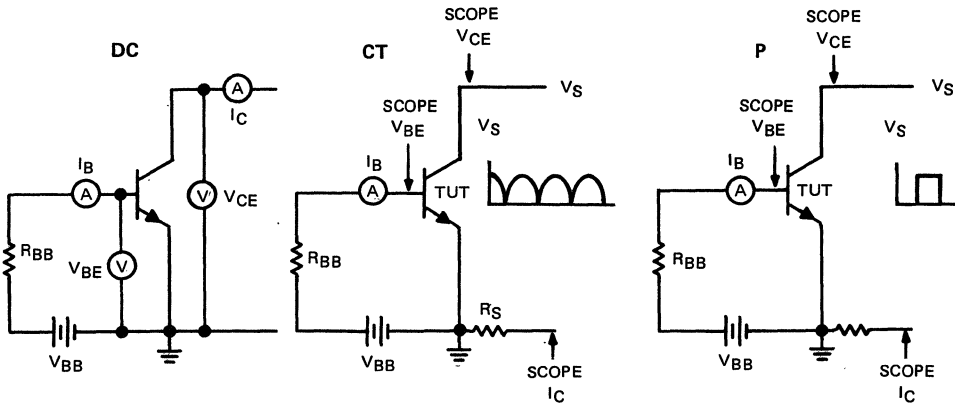
Description

There are two conditions of interest for the static base-to-emitter voltage:

1. The transistor in saturation (commonly referred to as $V_{BE(sat)}$)
2. The transistor out of saturation (V_{BE})

ELECTRICAL CHARACTERISTIC TESTS

Test Circuit



For the CT and P tests, $V_{BB} \gg V_{BE}$ in order to make I_B independent of V_{BE} changes during the "on" condition. The base terminal for Darlington transistors is B1.

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

1. The transistor in saturation: ($V_{BE(\text{sat})}$)

Collector Current: I_C

Base Current: I_B

2. The transistor out of saturation: (V_{BE})

Collector current: I_C

Collector-to-emitter voltage: V_{CE}

Technique: DC, CT, P

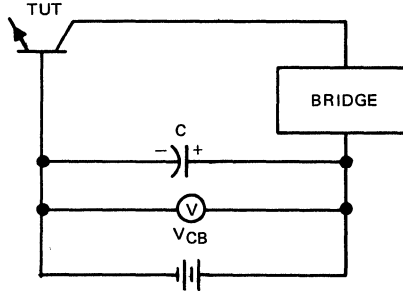
OPEN-CIRCUIT OUTPUT CAPACITANCE [C_{obo}]

Description

The open-circuit output capacitance indicates the frequency limitations of a transistor.

ELECTRICAL CHARACTERISTIC TESTS

Test Circuit



Capacitor C has to be sufficiently large to provide a short-circuit at the test frequency. The bridge has to be nulled with the base-to-collector open. The base terminal for Darlington transistors is B1.

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

Collector-to-base voltage: V_{CB}

Frequency: f

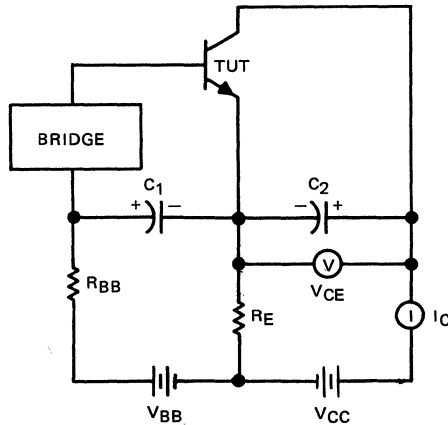
SMALL-SIGNAL SHORT-CIRCUIT INPUT IMPEDANCE [h_{ie} , $h_{ie}(\text{real})$, $h_{ie}(\text{imag})$]

Description

The input impedance is $h_{ie} = V_{be}/I_b$ with $V_{ce} = 0$. The real and imaginary components are important for input matching networks.

Circuits

Capacitors C1 and C2 must represent a short-circuit at the measuring frequency. The bridge must be nulled with a short across the base and emitter terminals and $V_{BB} = 0$. When h_{ie} is measured at 1 kHz, I_b can be measured with a current probe and V_{be} with a scope.



ELECTRICAL CHARACTERISTIC TESTS

Test Conditions To Be Specified

- Case temperature if not $T_C = 25^\circ\text{C}$
- Collector-to-emitter voltage: V_{CE}
- Collector current: I_C
- Frequency: f for $h_{ie}(\text{real})$ and $h_{ie}(\text{imag})$

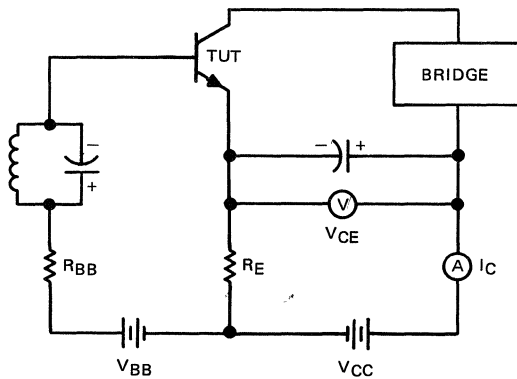
1

SMALL-SIGNAL OPEN-CIRCUIT OUTPUT ADMITTANCE [$h_{oe}(\text{real})$]

Description

The purpose of this test is to determine the real part of the output admittance.

Test Circuit



The L-C network in the base circuit must have a large impedance compared with h_{ie} at the test frequency. Capacitor C_1 shall present a short-circuit at the test frequency.

Test Conditions To Be Specified

- Case temperature if not $T_C = 25^\circ\text{C}$
- Collector-to-emitter voltage: V_{CE}
- Collector current: I_C
- Frequency: f

ELECTRICAL CHARACTERISTIC TESTS

SMALL-SIGNAL FORWARD CURRENT TRANSFER RATIO $[h_{fe}]$, CUT-OFF FREQUENCY $[f_{hfe}]$, AND FREQUENCY AT WHICH $|h_{fe}|$ EXTRAPOLATES TO UNITY $[f_T]$

Description

These measurements indicate the gain h_{fe} and the frequency response capability of transistors. Both measurements are dependent on the operating point.

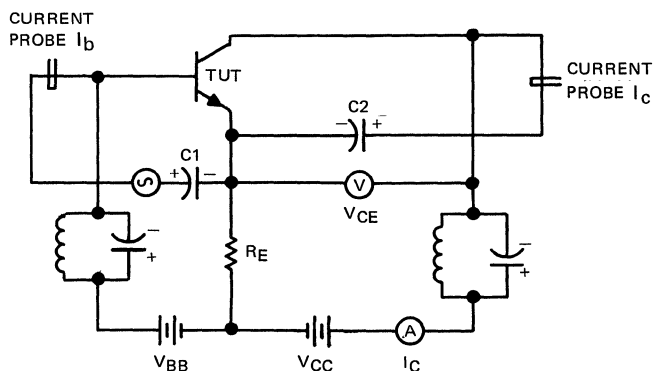
$h_{fe} = I_C / I_B$ (with $V_{ce} = 0$) at low frequency.

f_{hfe} = frequency at which h_{fe} is 3 dB down from its 1-kHz measurement

$f_T = |h_{fe}| \times f$. The absolute small-signal $|h_{fe}|$ has to be measured at a frequency f where $|h_{fe}|$ is decreasing approximately 6 dB per octave.

The measurement as specified does not assure the 6-dB-per-octave region. The 6-dB-per-octave region can be determined by plotting $|h_{fe}|$ versus f .

Test Circuit



The L-C networks must have a very large impedance compared to the capacitors C1 and C2. The amplitude of I_B and I_C is measured with a current probe.

The ac impedance represented by C2, the current probe for I_C , and associated wiring shall be small compared to the output impedance of the Transistor Under Test.

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

Collector-to-emitter voltage: V_{CE}

Collector current: I_C

For h_{fe} and f_T only: f

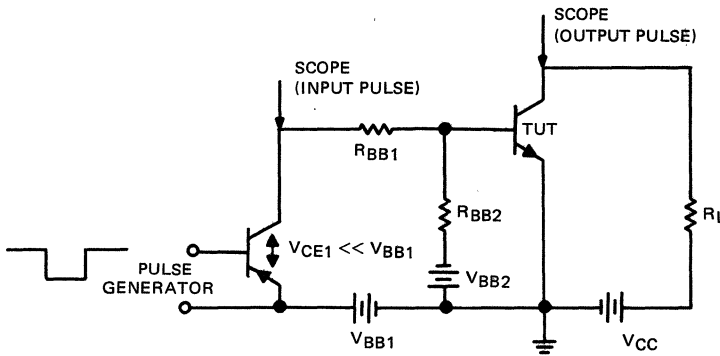
ELECTRICAL CHARACTERISTIC TESTS

SWITCHING TIME [t_d , t_r , t_s , t_f]

Description

It is desirable to minimize the large possible variations in switching circuits. A circuit similar to the following is recommended for switching times registered on the JC-25 RDF-2 format. For definition of t_d , t_r , t_s , and t_f , see section on "Letter Symbols, Abbreviations, Terms, and Definitions." The transistor parameter "rise time" refers to the time interval during which the magnitude of the collector current is increasing and the magnitude of the collector voltage is decreasing.

Test Circuit



The rise and fall time of the input pulse shall be smaller than 10% of the maximum specified rise and fall time of the output pulse. Changing the pulse width t_w by a factor of two should not change the storage time t_s by more than the desired accuracy of the measurement.

Test Conditions To Be Specified

Case temperature if not $T_C = 25^\circ\text{C}$

V_{BB1} , V_{BB2} , V_{CC} , R_{BB1} , R_{BB2} , R_L , t_w and f of pulse generator.

Cross-Reference Guide

CROSS-REFERENCE GUIDE

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N68		T13027	PNP-Ge	2N418		T13031	PNP-Ge
2N101		2N1038	PNP-Ge	2N419		T13029	PNP-Ge
2N102		2N1038	PNP-Ge	2N420		T13029	PNP-Ge
2N141		2N1038	PNP-Ge	2N424	2N424	2N424	NPN-Ge
2N142		2N1038	PNP-Ge	2N424A	2N424A	2N424A	NPN-Ge
2N143		2N1038	PNP-Ge	2N441		2N511	PNP-Ge
2N144		2N1039	PNP-Ge	2N442		2N512	PNP-Ge
2N155		T13027	PNP-Ge	2N443		2N513	PNP-Ge
2N156	T1156	2N2552	PNP-Ge	2N456	2N456	2N456	PNP-Ge
2N158		2N2552	PNP-Ge	2N456A	2N456A	2N456A	PNP-Ge
2N158A		2N2552	PNP-Ge	2N456B	2N456B	2N456B	PNP-Ge
2N173		2N512	PNP-Ge	2N457	2N457	2N457	PNP-Ge
2N174		2N513	PNP-Ge	2N457A	2N457A	2N457A	PNP-Ge
2N174A		2N513A	PNP-Ge	2N457B	2N457B	2N457B	PNP-Ge
2N176		T13027	PNP-Ge	2N458	2N458	2N458	PNP-Ge
2N178		T13027	PNP-Ge	2N458A	2N458A	2N458A	PNP-Ge
2N234A		T13027	PNP-Ge	2N458B	2N458B	2N458B	PNP-Ge
2N235A		T13027	PNP-Ge	2N459		2N3146	PNP-Ge
2N236A		T13028	PNP-Ge	2N459A		2N3146	PNP-Ge
2N242		T13029	PNP-Ge	2N497	2N497	2N497	NPN-Si
2N250	2N250	2N456	PNP-Ge	2N497A	2N497A	2N497A	NPN-Si
2N250A	2N250A	2N456	PNP-Ge	2N498	2N498	2N498	NPN-Si
2N251	2N251	2N456	PNP-Ge	2N498A	2N498A	2N498A	NPN-Si
2N251A	2N251A	2N456	PNP-Ge	2N511	2N511	2N511	PNP-Ge
2N255		T13027	PNP-Ge	2N511A	2N511A	2N511A	PNP-Ge
2N256		T13027	PNP-Ge	2N511B	2N511B	2N511B	PNP-Ge
2N257		T13027	PNP-Ge	2N512	2N512	2N512	PNP-Ge
2N268		T13027	PNP-Ge	2N512A	2N512A	2N512A	PNP-Ge
2N277		2N512	PNP-Ge	2N512B	2N512B	2N512B	PNP-Ge
2N278		2N513	PNP-Ge	2N513	2N513	2N513	PNP-Ge
2N285		T13027	PNP-Ge	2N513A	2N513A	2N513A	PNP-Ge
2N285A		T13027	PNP-Ge	2N513B	2N513B	2N513B	PNP-Ge
2N296		T13030	PNP-Ge	2N514	2N514	2N514	PNP-Ge
2N297		T13028	PNP-Ge	2N514A	2N514A	2N514A	PNP-Ge
2N301		T13027	PNP-Ge	2N514B	2N514B	2N514B	PNP-Ge
2N307		T13027	PNP-Ge	2N538		T13031	PNP-Ge
2N326		T13027	PNP-Ge	2N539		T13031	PNP-Ge
2N350		T13028	PNP-Ge	2N539A		T13031	PNP-Ge
2N351		T13028	PNP-Ge	2N540		T13031	PNP-Ge
2N375		T13031	PNP-Ge	2N553		T13027	PNP-Ge
2N376		T13028	PNP-Ge	2N554		T13027	PNP-Ge
2N378		T13027	PNP-Ge	2N555		T13027	PNP-Ge
2N379		T13029	PNP-Ge	2N561		T13031	PNP-Ge
2N380		T13030	PNP-Ge	2N574		T13031	PNP-Ge
2N389	2N389	2N389	NPN-Si	2N574A		T13031	PNP-Ge
2N389A	2N389A	2N389A	NPN-Si	2N575		T13031	PNP-Ge
2N392		T13027	PNP-Ge	2N575A		T13031	PNP-Ge
2N399		T13028	PNP-Ge	2N618		T13031	PNP-Ge
2N400		T13028	PNP-Ge	2N627		T13027	PNP-Ge
2N401		T13028	PNP-Ge	2N628		T13028	PNP-Ge

CROSS-REFERENCE GUIDE

2

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N629		TI3030	PNP-Ge	2N1029A		TI3027	PNP-Ge
2N630		TI3031	PNP-Ge	2N1029B		TI3031	PNP-Ge
2N637		TI3027	PNP-Ge	2N1029C		2N456A	PNP-Ge
2N637A		TI3031	PNP-Ge	2N1030		2N456A	PNP-Ge
2N637B		TI3146	PNP-Ge	2N1030A		2N456A	PNP-Ge
2N638		TI3027	PNP-Ge	2N1031		TI3027	PNP-Ge
2N638A		TI3028	PNP-Ge	2N1031A		TI3027	PNP-Ge
2N638B		TI3029	PNP-Ge	2N1031B		TI3031	PNP-Ge
2N639		TI3028	PNP-Ge	2N1031C		TI456A	PNP-Ge
2N639A		2N3146	PNP-Ge	2N1032		2N456A	PNP-Ge
2N639B		2N3146	PNP-Ge	2N1032A		2N456A	PNP-Ge
2N656	2N656	2N656	NPN-Si	2N1038	2N1038	2N1038	PNP-Ge
2N656A	2N656A	2N656A	NPN-Si	2N1038-1	2N2552	2N2552	PNP-Ge
2N657	2N657	2N657	NPN-Si	2N1038-2	2N2556	2N2556	PNP-Ge
2N657A	2N657A	2N657A	NPN-Si	2N1039	2N1039	2N1039	PNP-Ge
2N663		TI3027	PNP-Ge	2N1039-1	2N2553	2N2553	PNP-Ge
2N665		TI3029	PNP-Ge	2N1039-2	2N2557	2N2557	PNP-Ge
2N669		TI3027	PNP-Ge	2N1040	2N1040	2N1040	PNP-Ge
2N677		2N511	PNP-Ge	2N1040-1	2N2554	2N2554	PNP-Ge
2N677A		2N512	PNP-Ge	2N1040-2	2N2558	2N2558	PNP-Ge
2N677B		2N513	PNP-Ge	2N1041	2N1041	2N1041	PNP-Ge
2N677C		2N514	PNP-Ge	2N1041-1	2N2555	2N2555	PNP-Ge
2N678		2N511	PNP-Ge	2N1041-2	2N2559	2N2559	PNP-Ge
2N678A		2N512	PNP-Ge	2N1042	2N1042	2N1042	PNP-Ge
2N678B		2N513	PNP-Ge	2N1042-1	2N2560	2N2560	PNP-Ge
2N678C		2N514	PNP-Ge	2N1042-2	2N2564	2N2564	PNP-Ge
2N876		2N3005	SCR	2N1043	2N1043	2N1043	PNP-Ge
2N877		2N3005	SCR	2N1043-1	2N2561	2N2561	PNP-Ge
2N878		2N3006	SCR	2N1043-2	2N2565	2N2565	PNP-Ge
2N879		2N3007	SCR	2N1044	2N1044	2N1044	PNP-Ge
2N880		2N3008	SCR	2N1044-1	2N2562	2N2562	PNP-Ge
2N881		2N3008	SCR	2N1044-2	2N2566	2N2566	PNP-Ge
2N884		2N3001	SCR	2N1045	2N1045	2N1045	PNP-Ge
2N885		2N3001	SCR	2N1045-1	2N2563	2N2563	PNP-Ge
2N886		2N3002	SCR	2N1045-2	2N2567	2N2567	PNP-Ge
2N887		2N3003	SCR	2N1046	2N1046	2N1907	PNP-Ge
2N888		2N3004	SCR	2N1046A	2N1046A	2N1907	PNP-Ge
2N889		2N3004	SCR	2N1046B	2N1046B	2N1907	PNP-Ge
2N948		2N3001	SCR	2N1047	2N1047	2N1047	NPN-Si
2N949		2N3002	SCR	2N1047A	2N1047A	2N1047A	NPN-Si
2N950		2N3003	SCR	2N1047B	2N1047B	2N1047B	NPN-Si
2N1011		TI3028	PNP-Ge	2N1048	2N1048	2N1048	NPN-Si
2N1014		2N456A	PNP-Ge	2N1048A	2N1048A	2N1048A	NPN-Si
2N1015		2N3713	NPN-Si	2N1048B	2N1048B	2N1048B	NPN-Si
2N1016		2N3713	NPN-Si	2N1049	2N1049	2N1049	NPN-Si
2N1021	2N1021	2N456A	PNP-Ge	2N1049A	2N1049A	2N1049A	NPN-Si
2N1021A	2N1021A	2N456A	PNP-Ge	2N1049B	2N1049B	2N1049B	NPN-Si
2N1022	2N1022	2N456A	PNP-Ge	2N1050	2N1050	2N1050	NPN-Si
2N1022A	2N1022A	2N456A	PNP-Ge	2N1050A	2N1050A	2N1050A	NPN-Si
2N1029		TI3027	PNP-Ge	2N1050B	2N1050B	2N1050B	NPN-Si

CROSS-REFERENCE GUIDE

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N1069		2N3713	NPN-Si	2N1293		TI3028	PNP-Ge
2N1070		2N3713	NPN-Si	2N1295		2N3146	PNP-Ge
2N1120		TI3031	PNP-Ge	2N1297		2N3146	PNP-Ge
2N1136		TI3027	PNP-Ge	2N1314		TI3027	PNP-Ge
2N1136A		TI3028	PNP-Ge	2N1320		2N1038	PNP-Ge
2N1136B		TI3027	PNP-Ge	2N1322		2N1038	PNP-Ge
2N1137		2N456A	PNP-Ge	2N1324		2N1038	PNP-Ge
2N1137A		2N456A	PNP-Ge	2N1326		2N1041	PNP-Ge
2N1137B		2N456A	PNP-Ge	2N1328		2N1038	PNP-Ge
2N1138		TI3027	PNP-Ge	2N1359	CTI	TI3027	PNP-Ge
2N1138A		2N456A	PNP-Ge	2N1360	CTI	TI3027	PNP-Ge
2N1138B		2N456A	PNP-Ge	2N1362	CTI	2N3146	PNP-Ge
2N1146		2N456A	PNP-Ge	2N1364	CTI	2N3146	PNP-Ge
2N1146A		2N456A	PNP-Ge	2N1365	CTI	2N3146	PNP-Ge
2N1146B		2N456B	PNP-Ge	2N1437		2N3146	PNP-Ge
2N1146C		2N456A	PNP-Ge	2N1438		2N3146	PNP-Ge
2N1147		2N456A	PNP-Ge	2N1465		2N3146	PNP-Ge
2N1147A		2N456A	PNP-Ge	2N1466		2N3146	PNP-Ge
2N1147B		2N456A	PNP-Ge	2N1470		2N3713	NPN-Si
2N1147C		2N456A	PNP-Ge	2N1487		2N3713	NPN-Si
2N1159		2N456A	PNP-Ge	2N1488		2N3714	NPN-Si
2N1160		2N456A	PNP-Ge	2N1489		2N4913	NPN-Si
2N1162		2N456A	PNP-Ge	2N1490		2N4914	NPN-Si
2N1162A		2N456A	PNP-Ge	2N1501		TI3028	PNP-Ge
2N1163		2N456A	PNP-Ge	2N1502		TI3028	PNP-Ge
2N1163A		2N456A	PNP-Ge	2N1504		2N3146	PNP-Ge
2N1168		TI3027	PNP-Ge	2N1529	2N1529	2N1529	PNP-Ge
2N1172		TI3027	PNP-Ge	2N1530	2N1530	2N1530	PNP-Ge
2N1176		2N1038	PNP-Ge	2N1531	2N1531	2N1531	PNP-Ge
2N1183		2N1038	PNP-Ge	2N1532	2N1532	2N1532	PNP-Ge
2N1183A		2N1038	PNP-Ge	2N1533	2N1533	2N1533	PNP-Ge
2N1183B		2N1039	PNP-Ge	2N1534	2N1534	2N1534	PNP-Ge
2N1184		2N2564	PNP-Ge	2N1534A		TI3027	PNP-Ge
2N1184A		2N2564	PNP-Ge	2N1535	2N1535	2N1535	PNP-Ge
2N1184B		2N2565	PNP-Ge	2N1535A		TI3027	PNP-Ge
2N1202		2N3146	PNP-Ge	2N1536	2N1536	2N3028	PNP-Ge
2N1203		2N3146	PNP-Ge	2N1536A		TI3028	PNP-Ge
2N1208		2N3715	NPN-Si	2N1537	2N1537	TI3030	PNP-Ge
2N1209		2N1724	NPN-Si	2N1537A		TI3030	PNP-Ge
2N1210		2N1722	NPN-Si	2N1538	2N1538	2N3146	PNP-Ge
2N1211		2N1722	NPN-Si	2N1539	2N1539	TI3027	PNP-Ge
2N1212		2N1724	NPN-Si	2N1540	2N1540	TI3027	PNP-Ge
2N1227		TI3027	PNP-Ge	2N1540A		TI3028	PNP-Ge
2N1235	2N1235	2N1235	NPN-Si	2N1541	2N1541	TI3028	PNP-Ge
2N1260	2N1260	2N1260	NPN-Si	2N1541A		TI3028	PNP-Ge
2N1261		TI3030	PNP-Ge	2N1542	2N1542	TI3031	PNP-Ge
2N1262		TI3030	PNP-Ge	2N1542A		TI3031	PNP-Ge
2N1263		TI3030	PNP-Ge	2N1543	2N1543	2N3146	PNP-Ge
2N1291		TI3027	PNP-Ge	2N1544	2N1544	TI3027	PNP-Ge

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CROSS-REFERENCE GUIDE

2

TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS
2N1544A		TI3027	PNP-Ge	2N1647		2N2150	NPN-Si
2N1545	2N1545	TI3027	PNP-Ge	2N1648		2N2150	NPN-Si
2N1545A		TI3027	PNP-Ge	2N1649		2N2150	NPN-Si
2N1546	2N1546	TI3029	PNP-Ge	2N1650		2N2151	NPN-Si
2N1546A		TI3029	PNP-Ge	2N1660		2N1722	NPN-Si
2N1547	2N1547	TI3031	PNP-Ge	2N1661		2N1722	NPN-Si
2N1547A		TI3031	PNP-Ge	2N1662		2N1722	NPN-Si
2N1548	2N1548	2N3146	PNP-Ge	2N1666		TI3027	PNP-Ge
2N1549		TI3027	PNP-Ge	2N1667		TI3027	PNP-Ge
2N1549A		TI3027	PNP-Ge	2N1668		TI3027	PNP-Ge
2N1550		TI3027	PNP-Ge	2N1669		TI3027	PNP-Ge
2N1550A		TI3027	PNP-Ge	2N1690	2N1690	2N1690	NPN-Si
2N1551		TI3029	PNP-Ge	2N1691	2N1691	2N1691	NPN-Si
2N1551A		TI3029	PNP-Ge	2N1702		2N4913	NPN-Si
2N1552		TI3031	PNP-Ge	2N1714	2N1714	2N1714	NPN-Si
2N1552A		TI3031	PNP-Ge	2N1715	2N1715	2N1715	NPN-Si
2N1553		TI3027	PNP-Ge	2N1716	2N1716	2N1716	NPN-Si
2N1553A		TI3027	PNP-Ge	2N1717	2N1717	2N1717	NPN-Si
2N1554		TI3027	PNP-Ge	2N1718	2N1718	2N1718	NPN-Si
2N1554A		TI3027	PNP-Ge	2N1719	2N1719	2N1719	NPN-Si
2N1555		2N456B	PNP-Ge	2N1720	2N1720	2N1720	NPN-Si
2N1555A		2N456B	PNP-Ge	2N1721	2N1721	2N1721	NPN-Si
2N1556		2N1021A	PNP-Ge	2N1722	2N1722	2N1722	NPN-Si
2N1556A		2N1021A	PNP-Ge	2N1722A	2N1722A	2N1722A	NPN-Si
2N1557		2N514	PNP-Ge	2N1723	2N1723	2N3716	NPN-Si
2N1557A		2N514	PNP-Ge	2N1724	2N1724	2N1724	NPN-Si
2N1558		2N514	PNP-Ge	2N1724A	2N1724A	2N1724A	NPN-Si
2N1558A		2N514A	PNP-Ge	2N1725	2N1725	2N1725	NPN-Si
2N1559		2N514A	PNP-Ge	2N1755		2N2552	PNP-Ge
2N1559A		2N514A	PNP-Ge	2N1756		2N2554	PNP-Ge
2N1560		2N514B	PNP-Ge	2N1757		2N2555	PNP-Ge
2N1560A		2N514B	PNP-Ge	2N1758		2N2555	PNP-Ge
2N1595	2N1595	2N1595	SCR	2N1759		2N2564	PNP-Ge
2N1596	2N1596	2N1596	SCR	2N1760		2N2566	PNP-Ge
2N1597	2N1597	2N1597	SCR	2N1761		2N2567	PNP-Ge
2N1598	2N1598	2N1598	SCR	2N1762		2N2567	PNP-Ge
2N1599	2N1599	2N1599	SCR	2N1772A		TIC116A	SCR
2N1600		TIC116A	SCR	2N1773A		TIC116B	SCR
2N1601		TIC116B	SCR	2N1774A		TIC116B	SCR
2N1602		TIC116B	SCR	2N1775A		TIC116C	SCR
2N1603		TIC116C	SCR	2N1776A		TIC116C	SCR
2N1604		TIC116D	SCR	2N1777A		TIC116D	SCR
2N1616		2N1724	NPN-Si	2N1778A		TIC116E	SCR
2N1616A		2N1724	NPN-Si	2N1870A		TIC39Y	SCR
2N1617		2N1724	NPN-Si	2N1871A		TIC39F	SCR
2N1617A		2N1724	NPN-Si	2N1872A		TIC39A	SCR
2N1618		2N1724	NPN-Si	2N1873A		TIC39B	SCR
2N1618A		2N1724	NPN-Si	2N1874A		TIC39B	SCR
2N1620		2N1724	NPN-Si	2N1876		TIC39Y	SCR

CROSS-REFERENCE GUIDE

TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS
2N1877		TIC39F	SCR	2N2111		2N3846	NPN-Si
2N1878		TIC39A	SCR	2N2112		2N3846	NPN-Si
2N1879		TIC39B	SCR	2N2113		2N3846	NPN-Si
2N1880		TIC39B	SCR	2N2114		2N3846	NPN-Si
2N1881		2N1595	SCR	2N2116		2N3846	NPN-Si
2N1882		2N1596	SCR	2N2117		2N3846	NPN-Si
2N1883		2N1596	SCR	2N2118		2N3846	NPN-Si
2N1884		2N1597	SCR	2N2119		2N3846	NPN-Si
2N1885		2N1597	SCR	2N2120		2N3846	NPN-Si
2N1899		2N4002	NPN-Si	2N2123		2N4002	NPN-Si
2N1901		2N4002	NPN-Si	2N2124		2N4002	NPN-Si
2N1905		2N1046	PNP-Ge	2N2125		2N3847	NPN-Si
2N1906		2N1907	PNP-Ge	2N2126		2N3847	NPN-Si
2N1907	2N1907	2N1907	PNP-Ge	2N2127		2N3847	NPN-Si
2N1908	2N1908	2N1908	PNP-Ge	2N2130		2N4002	NPN-Si
2N1931		2N1596	SCR	2N2131		2N4002	NPN-Si
2N1932		2N1597	SCR	2N2132		2N3847	NPN-Si
2N1933		2N1598	SCR	2N2133		2N3847	NPN-Si
2N1934		2N1598	SCR	2N2137		2N2552	PNP-Ge
2N1935		2N1598	SCR	2N2138		2N2552	PNP-Ge
2N1936	2N1936	2N3846	NPN-Si	2N2138A		2N2552	PNP-Ge
2N1937	2N1937	2N3846	NPN-Si	2N2139		2N2554	PNP-Ge
2N1940		T13027	PNP-Ge	2N2139A		2N2554	PNP-Ge
2N2008		2N2987	NPN-Si	2N2140		2N2555	PNP-Ge
2N2009		TIC39Y	SCR	2N2140A		2N2555	PNP-Ge
2N2010		TIC39F	SCR	2N2141		2N2555	PNP-Ge
2N2011		TIC39A	SCR	2N2141A		2N2555	PNP-Ge
2N2012		TIC39B	SCR	2N2147		2N1907	PNP-Ge
2N2013		TIC39C	SCR	2N2148		2N1908	PNP-Ge
2N2014		TIC39D	SCR	2N2150	2N2150	2N2150	NPN-Si
2N2015		2N3713	NPN-Si	2N2151	2N2151	2N2151	NPN-Si
2N2016		2N3714	NPN-Si	2N2196		2N2987	NPN-Si
2N2017	CTI	2N2989	NPN-Si	2N2197		2N2987	NPN-Si
2N2018	CTI	CTI	NPN-Si	2N2201		2N2987	NPN-Si
2N2019	CTI	CTI	NPN-Si	2N2202		2N2987	NPN-Si
2N2020	CTI	CTI	NPN-Si	2N2203		2N2987	NPN-Si
2N2021	CTI	CTI	NPN-Si	2N2204		2N2987	NPN-Si
2N2032	CTI	CTI	NPN-Si	2N2226		2N4002	NPN-Si
2N2033	CTI	CTI	NPN-Si	2N2227		2N4003	NPN-Si
2N2034	CTI	CTI	NPN-Si	2N2288		2N1046	PNP-Ge
2N2035		CTI	NPN-Si	2N2291		2N1907	PNP-Ge
2N2036		CTI	NPN-Si	2N2294		2N1907	PNP-Ge
2N2067		2N2553	PNP-Ge	2N2304		CTI	NPN-Si
2N2068		2N2555	PNP-Ge	2N2305		2N3713	NPN-Si
2N2106		2N497	NPN-Si	2N2308		CTI	NPN-Si
2N2107		2N656	NPN-Si	2N2322		TIC39Y	SCR
2N2108		2N656	NPN-Si	2N2323		TIC39F	SCR
2N2109		2N3846	NPN-Si	2N2324		TIC39A	SCR
2N2110		2N3846	NPN-Si	2N2325		TIC39B	SCR

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CROSS-REFERENCE GUIDE

2

TI DIRECT TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N2326		TIC39B	SCR
2N2327		TIC39C	SCR
2N2328		TIC39C	SCR
2N2329		TIC39D	SCR
2N2338		2N3713	NPN-Si
2N2339		CTI	NPN-Si
2N2344		TIC39C	SCR
2N2345		TIC39F	SCR
2N2346		TIC39A	SCR
2N2347		TIC39B	SCR
2N2348		TIC39B	SCR
2N2383		2N1722	NPN-Si
2N2384		2N1724	NPN-Si
2N2405		2N2987	NPN-Si
2N2434		2N3146	PNP-Ge
2N2444		2N3146	PNP-Ge
2N2445		2N3146	PNP-Ge
2N2472		2N2987	NPN-Si
2N2482		2N797	NPN-Ge
2N2552	2N2552	2N2552	PNP-Ge
2N2553	2N2553	2N2553	PNP-Ge
2N2554	2N2554	2N2554	PNP-Ge
2N2555	2N2555	2N2555	PNP-Ge
2N2556	2N2556	2N2556	PNP-Ge
2N2557	2N2557	2N2557	PNP-Ge
2N2558	2N2558	2N2558	PNP-Ge
2N2559	2N2559	2N2559	PNP-Ge
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2N2561	2N2561	2N2561	PNP-Ge
2N2562	2N2562	2N2562	PNP-Ge
2N2563	2N2563	2N2563	PNP-Ge
2N2564	2N2564	2N2564	PNP-Ge
2N2565	2N2565	2N2565	PNP-Ge
2N2566	2N2566	2N2566	PNP-Ge
2N2567	2N2567	2N2567	PNP-Ge
2N2632	CTI	2N3998	NPN-Si
2N2633	CTI	2N3998	NPN-Si
2N2634	CTI	2N3998	NPN-Si
2N2657	CTI	2N3418	NPN-Si
2N2658	CTI	2N3418	NPN-Si
2N2659	2N2659	2N2659	PNP-Ge
2N2660	2N2660	2N2660	PNP-Ge
2N2661	2N2661	2N2661	PNP-Ge
2N2662	2N2662	2N2662	PNP-Ge
2N2663	2N2663	2N2663	PNP-Ge
2N2664	2N2664	2N2664	PNP-Ge
2N2665	2N2665	2N2665	PNP-Ge
2N2666	2N2666	2N2666	PNP-Ge

TI DIRECT TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N2667	2N2667	2N2667	PNP-Ge
2N2668	2N2668	2N2668	PNP-Ge
2N2669	2N2669	2N2669	PNP-Ge
2N2670	2N2670	2N2670	PNP-Ge
2N2679		2N3001	SCR
2N2680		2N3002	SCR
2N2681		2N3003	SCR
2N2683		2N3001	SCR
2N2684		2N3002	SCR
2N2685		2N3003	SCR
2N2687		2N3005	SCR
2N2688		2N3006	SCR
2N2689		2N3007	SCR
2N2690		2N3008	SCR
2N2811	CTI	2N4301	NPN-Si
2N2812	CTI	2N4301	NPN-Si
2N2813	CTI	2N4301	NPN-Si
2N2814	CTI	2N4301	NPN-Si
2N2815	CTI	2N4002	NPN-Si
2N2816	CTI	2N4002	NPN-Si
2N2817	CTI	2N6324	NPN-Si
2N2818	CTI	2N6324	NPN-Si
2N2819	CTI	2N4002	NPN-Si
2N2820	CTI	2N4002	NPN-Si
2N2821	CTI	2N6324	NPN-Si
2N2822	CTI	2N6324	NPN-Si
2N2823	CTI	2N4002	NPN-Si
2N2824	CTI	2N4002	NPN-Si
2N2825	CTI	2N6324	NPN-Si
2N2828	CTI	2N3998	NPN-Si
2N2829	CTI	2N3998	NPN-Si
2N2832		2N1908	PNP-Si
2N2835		2N2564	PNP-Si
2N2836		TI3029	PNP-Si
2N2866	CTI	2N3998	NPN-Si
2N2867	CTI	2N3999	NPN-Si
2N2869		TI3030	PNP-Si
2N2870		TI3030	PNP-Si
2N2875	CTI	2N3998	NPN-Si
2N2877	CTI	2N3998	NPN-Si
2N2878	CTI	2N3998	NPN-Si
2N2879	CTI	2N3998	NPN-Si
2N2880	2N2880	2N2880	NPN-Si
2N2881	CTI	2N5333	PNP-Si
2N2882	CTI	2N5333	PNP-Si
2N2890	CTI	2N4000	NPN-Si
2N2891	CTI	2N4000	NPN-Si
2N2892	CTI	2N5004	NPN-Si

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CROSS-REFERENCE GUIDE

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N2893	CTI	2N5004	NPN-Si	2N3144		CTI	NPN-Si
2N2983	CTI	2N3418	NPN-Si	2N4145		CTI	NPN-Si
2N2984	CTI	2N3418	NPN-Si	2N3146	2N3146	2N3146	PNP-Ge
2N2985	CTI	2N3418	NPN-Si	2N3147	2N3147	2N3147	PNP-Ge
2N2986	CTI	2N3418	NPN-Si	2N3149		CTI	NPN-Si
2N2987	2N2987	2N2987	NPN-Si	2N3150		CTI	NPN-Si
2N2988	2N2988	2N2988	NPN-Si	2N3151		CTI	NPN-Si
2N2989	2N2989	2N2989	NPN-Si	2N3163		2N3789	PNP-Si
2N2990	2N2990	2N2990	NPN-Si	2N3164		CTI	PNP-Si
2N2991	2N2991	2N2991	NPN-Si	2N3165		CTI	PNP-Si
2N2992	2N2992	2N2992	NPN-Si	2N3166		CTI	PNP-Si
2N2993	2N2993	2N2993	NPN-Si	2N3167		CTI	PNP-Si
2N2994	2N2994	2N2994	NPN-Si	2N3168		CTI	PNP-Si
2N3001	2N3001	2N3001	SCR	2N3169		CTI	PNP-Si
2N3002	2N3002	2N3002	SCR	2N3170		CTI	PNP-Si
2N3003	2N3003	2N3003	SCR	2N3171		2N3789	PNP-Si
2N3004	2N3004	2N3004	SCR	2N3172		2N3789	PNP-Si
2N3005	2N3005	TIC44	SCR	2N3173		2N3790	PNP-Si
2N3006	2N3006	TIC45	SCR	2N3174		2N3790	PNP-Si
2N3007	2N3007	TIC46	SCR	2N3175		CTI	PNP-Si
2N3008	2N3008	TIC47	SCR	2N3176		CTI	PNP-Si
2N3021	2N3021	2N3789	PNP-Si	2N3177		CTI	PNP-Si
2N3022	2N3022	2N3789	PNP-Si	2N3178		CTI	PNP-Si
2N3023	2N3023	2N3789	PNP-Si	2N3179		CTI	PNP-Si
2N3024	2N3024	2N3791	PNP-Si	2N3180		CTI	PNP-Si
2N3025	2N3025	2N3791	PNP-Si	2N3181		CTI	PNP-Si
2N3026	2N3026	2N3791	PNP-Si	2N3182		CTI	PNP-Si
2N3027		TIC44	SCR	2N3183		2N3789	PNP-Si
2N3028		TIC45	SCR	2N3184		2N3789	PNP-Si
2N3029		TIC46	SCR	2N3185		2N3790	PNP-Si
2N3030		TIC44	SCR	2N3186		2N3790	PNP-Si
2N3031		TIC45	SCR	2N3187		CTI	PNP-Si
2N3032		TIC46	SCR	2N3188		CTI	PNP-Si
2N3054		TIP31A	NPN-Si	2N3189		CTI	PNP-Si
2N3055	2N3055	TIP3055	NPN-Si	2N3190		CTI	PNP-Si
2N3074		CTI	PNP-Ge	2N3191		CTI	NPN-Si
2N3075		CTI	PNP-Ge	2N3192		CTI	NPN-Si
2N3076		CTI	NPN-Si	2N3193		CTI	NPN-Si
2N3079		CTI	NPN-Si	2N3194		CTI	NPN-Si
2N3080		CTI	NPN-Si	2N3195		2N3789	PNP-Si
2N3125		2N3146	PNP-Ge	2N3196		2N3789	PNP-Si
2N3126		2N3146	PNP-Ge	2N3197		2N3790	PNP-Si
2N3132		TI3031	PNP-Ge	2N3198		2N3790	PNP-Si
2N3138		CTI	NPN-Si	2N3199		CTI	PNP-Si
2N3139		CTI	NPN-Si	2N3200		CTI	NPN-Si
2N3140		CTI	NPN-Si	2N3201		CTI	NPN-Si
2N3141		CTI	NPN-Si	2N3202		CTI	NPN-Si
2N3142		CTI	NPN-Si	2N3203		CTI	NPN-Si
2N3143		CTI	NPN-Si	2N3204		CTI	NPN-Si

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CROSS-REFERENCE GUIDE

2

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N3205		CTI	NPN-Si	2N3445		2N3713	NPN-Si
2N3206		CTI	NPN-Si	2N3446		2N3714	NPN-Si
2N3207		CTI	NPN-Si	2N3447		2N3715	NPN-Si
2N3208		CTI	NPN-Si	2N3448		2N3716	NPN-Si
2N3220		CTI	NPN-Si	2N3469		CTI	NPN-Si
2N3221		CTI	NPN-Si	2N3470		CTI	NPN-Si
2N3222		CTI	NPN-Si	2N3471		CTI	NPN-Si
2N3223		CTI	NPN-Si	2N3472		CTI	NPN-Si
2N3226		2N3713	NPN-Si	2N3473		CTI	NPN-Si
2N3228		TIC106B	SCR	2N3474		CTI	NPN-Si
2N3230		CTI	NPN-Si	2N3475		CTI	NPN-Si
2N3231		CTI	NPN-Si	2N3476		CTI	NPN-Si
2N3232		CTI	NPN-Si	2N3487		CTI	NPN-Si
2N3233		CTI	NPN-Si	2N3488		CTI	NPN-Si
2N3234		CTI	NPN-Si	2N3489		CTI	NPN-Si
2N3235		CTI	NPN-Si	2N3490		CTI	NPN-Si
2N3236		CTI	NPN-Si	2N3491		CTI	NPN-Si
2N3237		CTI	NPN-Si	2N3492		CTI	NPN-Si
2N3238		CTI	NPN-Si	2N3525		2N1599	SCR
2N3239		CTI	NPN-Si	2N3528		2N1597	SCR
2N3240		CTI	NPN-Si	2N3551	2N3551	2N3551	NPN-Si
2N3255		2N3001	SCR	2N3552	2N3552	2N3552	NPN-Si
2N3256		2N3002	SCR	2N3555		TIC39Y	SCR
2N3258		2N3004	SCR	2N3556		TIC39F	SCR
2N3259		2N3005	SCR	2N3557		TIC39A	SCR
2N3260		CTI	NPN-Si	2N3558		TIC39B	SCR
2N3263	2N3263	CTI	NPN-Si	2N3559		TIC39Y	SCR
2N3264	2N3264	CTI	NPN-Si	2N3560		TIC39Y	SCR
2N3265	2N3265	CTI	NPN-Si	2N3561		TIC39A	SCR
2N3266	2N3266	CTI	NPN-Si	2N3562		TIC39B	SCR
2N3273		TIC106A	SCR	2N3583	2N3583	2N3583	NPN-Si
2N3274		TIC106B	SCR	2N3584	2N3584	2N3584	NPN-Si
2N3275		TIC106C	SCR	2N3585	2N3585	2N3585	NPN-Si
2N3297		CTI	NPN-Si	2N3589	CTI	CTI	NPN-Si
2N3327		CTI	NPN-Si	2N3590	CTI	CTI	NPN-Si
2N3418	2N3418	2N3418	NPN-Si	2N3591	CTI	CTI	NPN-Si
2N3419	2N3419	2N3419	NPN-Si	2N3592	CTI	CTI	NPN-Si
2N3420	2N3420	2N3420	NPN-Si	2N3593	CTI	CTI	NPN-Si
2N3421	2N3421	2N3421	NPN-Si	2N3594	CTI	CTI	NPN-Si
2N3429		CTI	NPN-Si	2N3595	CTI	CTI	NPN-Si
2N3430		CTI	NPN-Si	2N3596	CTI	CTI	NPN-Si
2N3431		CTI	NPN-Si	2N3597	CTI	2N4002	NPN-Si
2N3432		CTI	NPN-Si	2N3598	CTI	2N4002	NPN-Si
2N3433		CTI	NPN-Si	2N3599	CTI	2N4003	NPN-Si
2N3434		CTI	NPN-Si	2N3611		TI3027	PNP-Ge
2N3439	2N3439	CTI	NPN-Si	2N3612		TI3028	PNP-Ge
2N3440	2N3440	CTI	NPN-Si	2N3613		TI3027	PNP-Ge
2N3441		CTI	NPN-Si	2N3614		TI3028	PNP-Ge
2N3442		CTI	NPN-Si	2N3615		TI3021	PNP-Ge

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CROSS-REFERENCE GUIDE

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N3616		2N3146	PNP-Ge	2N3846	2N3846	2N3846	NPN-Si
2N3617		T13030	PNP-Ge	2N3847	2N3847	2N3847	NPN-Si
2N3618		2N3146	PNP-Ge	2N3848	2N3848	2N3848	NPN-Si
2N3660		2N5333	PNP-Si	2N3849	2N3849	2N3849	NPN-Si
2N3661		2N5333	PNP-Si	2N3850		2N5938	NPN-Si
2N3667		2N3713	NPN-Si	2N3851		2N5938	NPN-Si
2N3675		2N3420	NPN-Si	2N3852		2N5938	NPN-Si
2N3676		2N3421	NPN-Si	2N3853		2N5938	NPN-Si
2N3713	2N3713	2N3713	NPN-Si	2N3861		2N4240	NPN-Si
2N3714	2N3714	2N3714	NPN-Si	2N3863		2N3715	NPN-Si
2N3715	2N3715	2N3715	NPN-Si	2N3864		2N3716	NPN-Si
2N3716	2N3716	2N3716	NPN-Si	2N3865	CTI	CTI	NPN-Si
2N3719	2N3719	2N3719	PNP-Si	2N3878	CTI	TIP41A	NPN-Si
2N3720	2N3720	2N3720	PNP-Si	2N3879	CTI	TIP41C	NPN-Si
2N3730	CTI	CTI	PNP-Ge	2N3902	2N3902	2N3902	NPN-Si
2N3731	CTI	CTI	PNP-Ge	2N3916		2N3583	NPN-Si
2N3732	CTI	CTI	PNP-Ge	2N3917		2N3583	NPN-Si
2N3738		2N3584	NPN-Si	2N3918	CTI	TIP33	NPN-Si
2N3739		2N3585	NPN-Si	2N3919	CTI	TIP33	NPN-Si
2N3740	CTI	TIP30A	PNP-Si	2N3920	CTI	TIP33	NPN-Si
2N3741	CTI	TIP30B	PNP-Si	2N3996	2N3996	2N3996	NPN-Si
2N3743	CTI	CTI	PNP-Si	2N3997	2N3997	2N3997	NPN-Si
2N3744		2N3996	NPN-Si	2N3998	2N3998	2N3998	NPN-Si
2N3745		2N3997	NPN-Si	2N3999	2N3999	2N3999	NPN-Si
2N3746	CTI	CTI	NPN-Si	2N4000	2N4000	2N4000	NPN-Si
2N3747	CTI	CTI	NPN-Si	2N4001	2N4001	2N4001	NPN-Si
2N3748	CTI	CTI	NPN-Si	2N4002	2N4002	2N4002	NPN-Si
2N3749	CTI	CTI	NPN-Si	2N4003	2N4003	2N4003	NPN-Si
2N3750		2N5938	NPN-Si	2N4004	2N4004	2N4004	NPN-Si
2N3751	CTI	CTI	NPN-Si	2N4005	2N4005	2N4005	NPN-Si
2N3752	CTI	CTI	NPN-Si	2N4063		2N3440	NPN-Si
2N3766	CTI	TIP29A	NPN-Si	2N4064		2N3440	NPN-Si
2N3767	CTI	TIP29B	NPN-Si	2N4070		CTI	NPN-Si
2N3771	2N3771	2N3771	NPN-Si	2N4071		CTI	NPN-Si
2N3772	2N3772	2N2772	NPN-Si	2N4075		2N4998	NPN-Si
2N3773	CTI	CTI	NPN-Si	2N4076		2N4998	NPN-Si
2N3774		2N3719	PNP-Si	2N4096		TIC39F	SCR
2N3775		2N5333	PNP-Si	2N4097		TIC39A	SCR
2N3776		2N5333	PNP-Si	2N4108		2N3006	SCR
2N3777		2N5333	PNP-Si	2N4109		2N3007	SCR
2N3778		2N5333	PNP-Si	2N4111		TIP3055	NPN-Si
2N3779		2N5333	PNP-Si	2N4112		TIP3055	NPN-Si
2N3780		2N5333	PNP-Si	2N4113		TIP33B	NPN-Si
2N3781		2N5333	PNP-Si	2N4114		TIP33B	NPN-Si
2N3782		2N5333	PNP-Si	2N4115		CTI	NPN-Si
2N3788	CTI	TIP53	NPN-Si	2N4116		CTI	NPN-Si
2N3789	2N3789	2N3789	PNP-Si	2N4130		TIP35B	NPN-Si
2N3790	2N3790	2N3790	PNP-Si	2N4131		TIP35C	NPN-Si
2N3791	2N3791	2N3791	PNP-Si	2N4150		2N4300	NPN-Si
2N3792	2N3792	2N3792	PNP-Si				

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CROSS-REFERENCE GUIDE

2

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N4152		TIC116F	SCR	2N4201		TIC106E	SCR
2N4153		TIC116A	SCR	2N4202		CTI	SCR
2N4154		TIC116B	SCR	2N4210		2N4002	NPN-Si
2N4155		TIC116C	SCR	2N4211		2N4003	NPN-Si
2N4156		TIC116D	SCR	2N4212		TIC39Y	SCR
2N4157		TIC116E	SCR	2N4213		TIC39F	SCR
2N4158		TIC116M	SCR	2N4214		TIC39A	SCR
2N4159		TIC116F	SCR	2N4215		TIC39B	SCR
2N4160		TIC116F	SCR	2N4216		TIC39B	SCR
2N4161		TIC116A	SCR	2N4217		TIC39C	SCR
2N4162		TIC116B	SCR	2N4218		TIC39C	SCR
2N4163		TIC116C	SCR	2N4219		TIC39D	SCR
2N4164		TIC116D	SCR	2N4231		TIP31	NPN-Si
2N4165		TIC116E	SCR	2N4232		TIP31A	NPN-Si
2N4166		TIC116M	SCR	2N4233		TIP31B	NPN-Si
2N4167		TIC116F	SCR	2N4234		TIP30	PNP-Si
2N4168		TIC116F	SCR	2N4235		TIP30A	PNP-Si
2N4169		TIC116A	SCR	2N4236		TIP30B	PNP-Si
2N4170		TIC116B	SCR	2N4240	2N4240	TIP48	NPN-Si
2N4171		TIC116C	SCR	2N4241		T13027	PNP-Ge
2N4172		TIC116D	SCR	2N4242		T13029	PNP-Ge
2N4173		TIC116E	SCR	2N4243		T13028	PNP-Ge
2N4174		TIC116M	SCR	2N4244		T13027	PNP-Ge
2N4175		TIC116F	SCR	2N4245		T13030	PNP-Ge
2N4176		TIC116F	SCR	2N4246		T13028	PNP-Ge
2N4177		TIC116A	SCR	2N4247		T13027	PNP-Ge
2N4178		TIC116B	SCR	2N4271		2N657	NPN-Si
2N4179		TIC116C	SCR	2N4272		2N657	NPN-Si
2N4180		TIC116D	SCR	2N4273	CTI	CTI	NPN-Si
2N4181		TIC116E	SCR	2N4296		TIP47	NPN-Si
2N4182		TIC116M	SCR	2N4297		TIP47	NPN-Si
2N4183		TIC116F	SCR	2N4298		TIP49	NPN-Si
2N4184		TIC116F	SCR	2N4299		TIP49	NPN-Si
2N4185		TIC116A	SCR	2N4300	2N4300	2N4300	NPN-Si
2N4186		TIC116B	SCR	2N4301	2N4301	2N4301	NPN-Si
2N4187		TIC116C	SCR	2N4305	CTI	2N5154	NPN-Si
2N4188		TIC116D	SCR	2N4307	CTI	2N5154	NPN-Si
2N4189		TIC116E	SCR	2N4309	CTI	2N5154	NPN-Si
2N4190		TIC116M	SCR	2N4311	CTI	2N5154	NPN-Si
2N4191		TIC116F	SCR	2N4316		TIC116A	SCR
2N4192		TIC116F	SCR	2N4317		TIC116B	SCR
2N4193		TIC116A	SCR	2N4318		TIC116C	SCR
2N4194		TIC116B	SCR	2N4319		TIC116D	SCR
2N4195		TIC116C	SCR	2N4322*		2N3001	SCR
2N4196		TIC116D	SCR	2N4333*		TIC39F	SCR
2N4197		TIC116E	SCR	2N4334*		TIC39A	SCR
2N4198		TIC116M	SCR	2N4335*		TIC39B	SCR
2N4199		TIC106C	SCR	2N4337*		TIC39C	SCR
2N4200		TIC106D	SCR	2N4346		T13031	PNP-Ge

* Asterisk denotes 2N numbers not JEDEC registered through December 1970.
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CROSS-REFERENCE GUIDE

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N4347	CTI	2N3716	NPN-Si	2N5006		2N6128	NPN-Si
2N4348	CTI	2N3716	NPN-Si	2N5007		2N6127	PNP-Si
2N4387	CTI	TIP30	PNP-Si	2N5008		2N6128	NPN-Si
2N4388	CTI	TIP30A	PNP-Si	2N5009		2N6127	PNP-Si
2N4395		2N3713	NPN-Si	2N5010	CTI	2N3439	NPN-Si
2N4396		2N3713	NPN-Si	2N5011	CTI	2N3439	NPN-Si
2N4398	2N4398	2N4398	PNP-Si	2N5012	CTI	2N3439	NPN-Si
2N4399	2N4399	2N4399	PNP-Si	2N5013		2N3439	NPN-Si
2N4441		TIC116F	SCR	2N5014		2N3439	NPN-Si
2N4442		TIC116B	SCR	2N5015		2N3439	NPN-Si
2N4443		TIC116D	SCR	2N5034		TIP33	NPN-Si
2N4444		TIC116M	SCR	2N5035		TIP33	NPN-Si
2N4862		CTI	NPN-Si	2N5036		TIP33A	NPN-Si
2N4863	CTI	2N5148	NPN-Si	2N5037		TIP33A	NPN-Si
2N4864	CTI	CTI	NPN-Si	2N5038	2N5038	2N5038	NPN-Si
2N4865		CTI	NPN-Si	2N5039	2N5039	2N5039	NPN-Si
2N4866		CTI	NPN-Si	2N5048		2N6128	NPN-Si
2N4877		CTI	NPN-Si	2N5049		2N6128	NPN-Si
2N4898	CTI	TIP30	PNP-Si	2N5050	CTI	TIP47	NPN-Si
2N4899	CTI	TIP30A	PNP-Si	2N5051	CTI	TIP47	NPN-Si
2N4900	CTI	TIP30B	PNP-Si	2N5052	CTI	CTI	NPN-Si
2N4901	2N4901	TIP34	PNP-Si	2N5060	2N5060	TIC60	SCR
2N4902	2N4902	TIP34A	PNP-Si	2N5061	2N5061	TIC61	SCR
2N4903	2N4903	TIP34B	PNP-Si	2N5062	2N5062	TIC62	SCR
2N4904	2N4904	TIP34	PNP-Si	2N5063	2N5063	TIC63	SCR
2N4905	2N4905	TIP34A	PNP-Si	2N5064	2N5064	TIC64	SCR
2N4906	2N4906	TIP34B	PNP-Si	2N5067	2N5067	TIP33	NPN-Si
2N4907	CTI	TIP34	PNP-Si	2N5068	2N5068	TIP33A	NPN-Si
2N4908	CTI	TIP34A	PNP-Si	2N5069	2N5069	TIP33B	NPN-Si
2N4910	CTI	TIP33	NPN-Si	2N5147	2N5147	2N5147	PNP-Si
2N4911	CTI	TIP33A	NPN-Si	2N5148	2N5148	2N5148	NPN-Si
2N4912	CTI	TIP33B	NPN-Si	2N5149	2N5149	2N5149	PNP-Si
2N4913	2N4913	TIP33	NPN-Si	2N5150	2N5150	2N5150	NPN-Si
2N4914	2N4914	TIP33A	NPN-Si	2N5151	2N5151	2N5151	PNP-Si
2N4915	2N4915	TIP33B	NPN-Si	2N5152	2N5152	2N5152	NPN-Si
2N4918		TIP30	PNP-Si	2N5153	2N5153	2N5153	PNP-Si
2N4919		TIP30A	PNP-Si	2N5154	2N5154	2N5154	NPN-Si
2N4920		TIP30B	PNP-Si	2N5157	2N5157	2N5157	NPN-Si
2N4921		TIP29	NPN-Si	2N5190		TIP31	NPN-Si
2N4922		TIP29A	NPN-Si	2N5191		TIP31A	NPN-Si
2N4923		TIP29B	NPN-Si	2N5192		TIP31B	NPN-Si
2N4998	2N4998	2N4998	NPN-Si	2N5193		TIP32	PNP-Si
2N4999	2N4999	2N4999	NPN-Si	2N5194		TIP32A	PNP-Si
2N5000	2N5000	2N5000	NPN-Si	2N5195		TIP32B	PNP-Si
2N5001	2N5001	2N5001	NPN-Si	2N5202	CTI	CTI	NPN-Si
2N5002	2N5002	2N5002	NPN-Si	2N5237	CTI	CTI	NPN-Si
2N5003	2N5003	2N5003	PNP-Si	2N5238	CTI	CTI	NPN-Si
2N5004	2N5004	2N5004	NPN-Si	2N5239	CTI	CTI	NPN-Si
2N5005	2N5005	2N5005	PNP-Si	2N5240	CTI	CTI	NPN-Si

2

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2

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N5241	2N5241	2N5241	NPN-Si	2N5349	CTI	CTI	NPN-Si
2N5273		TIC263B	TRIAC	2N5384	2N5384	2N5384	PNP-Si
2N5274		TIC263D	TRIAC	2N5385	2N5385	2N5385	PNP-Si
2N5275		TIC263M	TRIAC	2N5386	2N5386	2N5386	PNP-Si
2N5279	CTI	2N3439	NPN-Si	2N5387	2N5387	2N5387	NPN-Si
2N5280	CTI	2N3439	NPN-Si	2N5388	2N5388	2N5388	NPN-Si
2N5284	CTI	2N5002	NPN-Si	2N5389	2N5389	2N5389	NPN-Si
2N5285	CTI	2N5004	NPN-Si	2N5390	2N5390	2N5390	NPN-Si
2N5286	CTI	2N5003	PNP-Si	2N5404	CTI	2N5153	PNP-Si
2N5287	CTI	2N5005	PNP-Si	2N5405	CTI	2N5153	PNP-Si
2N5288	CTI	2N6128	NPN-Si	2N5406	CTI	2N5153	PNP-Si
2N5289	CTI	2N6128	NPN-Si	2N5407	CTI	2N5153	PNP-Si
2N5290	CTI	2N6127	PNP-Si	2N5408	CTI	2N5005	PNP-Si
2N5291	CTI	2N6127	PNP-Si	2N5409	CTI	2N5005	PNP-Si
2N5293		TIP31B	NPN-Si	2N5410	CTI	2N5005	PNP-Si
2N5294		TIP31B	NPN-Si	2N5411	CTI	2N5005	PNP-Si
2N5295		TIP31	NPN-Si	2N5412	CTI	CTI	NPN-Si
2N5296		TIP31	NPN-Si	2N5427	CTI	TIP31B	NPN-Si
2N5297		TIP31A	NPN-Si	2N5428	CTI	TIP31B	NPN-Si
2N5298		TIP31A	NPN-Si	2N5429	CTI	TIP31C	NPN-Si
2N5301	2N5301	2N5301	NPN-Si	2N5230	CTI	TIP31C	NPN-Si
2N5302	2N5302	2N5302	NPN-Si	2N5466	CTI	TIP54	NPN-Si
2N5303	2N5303	2N5303	NPN-Si	2N5467	CTI	TIP54	NPN-Si
2N5312	CTI	2N6127	PNP-Si	2N5468	CTI	TIP530	NPN-Si
2N5313	CTI	2N6128	NPN-Si	2N5469	CTI	TIP530	NPN-Si
2N5314	CTI	2N6127	PNP-Si	2N5477	CTI	CTI	NPN-Si
2N5315	CTI	2N6128	NPN-Si	2N5478	CTI	CTI	NPN-Si
2N5316	CTI	2N6127	PNP-Si	2N5479	CTI	CTI	NPN-Si
2N5317	CTI	2N6128	NPN-Si	2N5480	CTI	CTI	NPN-Si
2N5318	CTI	2N6127	PNP-Si	2N5489	CTI	T1XP547	NPN-Si
2N5319	CTI	2N6128	NPN-Si	2N5490		TIP41	NPN-Si
2N5326	CTI	CTI	NPN-Si	2N5491		TIP41	NPN-Si
2N5327	CTI	CTI	NPN-Si	2N5492		TIP41A	NPN-Si
2N5328	CTI	CTI	NPN-Si	2N5493		TIP41A	NPN-Si
2N5329	CTI	CTI	NPN-Si	2N5494		TIP41	NPN-Si
2N5330	CTI	CTI	NPN-Si	2N5495		TIP41	NPN-Si
2N5331	CTI	CTI	NPN-Si	2N5496		TIP41B	NPN-Si
2N5333	2N5333	2N5333	NPN-Si	2N5497		TIP41B	NPN-Si
2N5334	CTI	CTI	NPN-Si	2N5529	CTI	2N5938	NPN-Si
2N5335	CTI	CTI	NPN-Si	2N5530	CTI	2N5938	NPN-Si
2N5336	CTI	2N5152	NPN-Si	2N5531	CTI	CTI	NPN-Si
2N5337	CTI	2N5154	NPN-Si	2N5532	CTI	2N5938	NPN-Si
2N5338	CTI	2N5152	NPN-Si	2N5533	CTI	2N5938	NPN-Si
2N5339	CTI	2N5154	NPN-Si	2N5534	CTI	2N5938	NPN-Si
2N5344	CTI	CTI	PNP-Si	2N5535	CTI	2N5939	NPN-Si
2N5345	CTI	CTI	PNP-Si	2N5536	CTI	2N5939	NPN-Si
2N5346	CTI	CTI	NPN-Si	2N5537	CTI	2N5939	NPN-Si
2N5347	CTI	CTI	NPN-Si	2N5538	CTI	2N5939	NPN-Si
2N5348	CTI	CTI	NPN-Si	2N5539	CTI	2N4002	NPN-Si

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CROSS-REFERENCE GUIDE

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N5540	CTI	2N5389	NPN-Si	2N5632	CTI	2N5885	NPN-Si
2N5541	CTI	2N3421	NPN-Si	2N5633	CTI	2N5885	NPN-Si
2N5542	CTI	2N4301	NPN-Si	2N5634	CTI	2N5885	NPN-Si
2N5552	CTI	CTI	NPN-Si	2N5655		TIP47	NPN-Si
2N5553*	CTI	CTI	NPN-Si	2N5656		TIP48	NPN-Si
2N5554*	CTI	CTI	NPN-Si	2N5657		TIP49	NPN-Si
2N5559	CTI	CTI	NPN-Si	2N5658	CTI	2N3997	NPN-Si
2N5560	CTI	2N4002	NPN-Si	2N5659	CTI	2N3997	NPN-Si
2N5567		TIC236B	TRIAC	2N5660	CTI	CTI	NPN-Si
2N5568		TIC236D	TRIAC	2N5661	CTI	CTI	NPN-Si
2N5569		TIC236B	TRIAC	2N5662	CTI	CTI	NPN-Si
2N5570		TIC236D	TRIAC	2N5663	CTI	CTI	NPN-Si
2N5571		TIC246B	TRIAC	2N5664	CTI	CTI	NPN-Si
2N5572		TIC246D	TRIAC	2N5665	CTI	CTI	NPN-Si
2N5573		TIC246B	TRIAC	2N5666	CTI	CTI	NPN-Si
2N5574		TIC246D	TRIAC	2N5667	CTI	CTI	NPN-Si
2N5597		TIP30A	PNP-Si	2N5671	2N5671	2N5671	NPN-Si
2N5598		TIP31A	NPN-Si	2N5672	2N5672	2N5672	NPN-Si
2N5599		TIP30B	PNP-Si	2N5675	CTI	2N5333	PNP-Si
2N5600	CTI	TIP31B	NPN-Si	2N5676	CTI	2N5384	PNP-Si
2N5601	CTI	TIP30B	PNP-Si	2N5677	CTI	2N5386	PNP-Si
2N5602	CTI	TIP31B	NPN-Si	2N5678	CTI	CTI	PNP-Si
2N5603	CTI	TIP30C	PNP-Si	2N5679	CTI	2N5333	PNP-Si
2N5604	CTI	TIP31C	NPN-Si	2N5680	CTI	2N5333	PNP-Si
2N5605	CTI	TIP42A	PNP-Si	2N5681	CTI	2N2990	NPN-Si
2N5606	CTI	CTI	NPN-Si	2N5682	CTI	2N2990	NPN-Si
2N5607	CTI	TIP42B	PNP-Si	2N5683	2N5683	2N5683	PNP-Si
2N5608	CTI	CTI	NPN-Si	2N5684	2N5684	2N5684	PNP-Si
2N5609	CTI	TIP42C	PNP-Si	2N5685	2N5685	2N5685	NPN-Si
2N5611		TIP42C	PNP-Si	2N5686	2N5686	2N5686	NPN-Si
2N5613		2N3791	PNP-Si	2N5692	CTI	CTI	PNP-Ge
2N5614		TIP33A	NPN-Si	2N5693	CTI	CTI	PNP-Ge
2N5615		2N3792	PNP-Si	2N5694	CTI	CTI	PNP-Ge
2N5616		TIP33B	NPN-Si	2N5695	CTI	CTI	PNP-Ge
2N5617		2N3792	PNP-Si	2N5696	CTI	CTI	PNP-Ge
2N5618		TIP33B	NPN-Si	2N5719		2N3002	SCR
2N5619		2N3792	PNP-Si	2N5720		2N3003	SCR
2N5620		TIP33C	NPN-Si	2N5721		2N3004	SCR
2N5621		2N3791	PNP-Si	2N5722		CTI	SCR
2N5622		TIP35A	NPN-Si	2N5724		TIC39F	SCR
2N5623		2N3792	PNP-Si	2N5725		TIC39A	SCR
2N5624		TIP35B	NPN-Si	2N5726		TIC39B	SCR
2N5625		2N5884	PNP-Si	2N5727		TIC39C	SCR
2N5626		TIP35B	NPN-Si	2N5729	CTI	2N3420	NPN-Si
2N5627		2N5884	PNP-Si	2N5730	CTI	2N5004	NPN-Si
2N5628	CTI	CTI	NPN-Si	2N5731	CTI	2N6128	NPN-Si
2N5629	CTI	2N5885	NPN-Si	2N5732		TIP35C	NPN-Si
2N5630	CTI	2N5885	NPN-Si	2N5734		2N5885	NPN-Si
2N5631	CTI	2N5885	NPN-Si	2N5737	CTI	2N3791	PNP-Si

* Asterisk denotes 2N numbers not JEDEC registered through December 1970.

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CROSS-REFERENCE GUIDE

TI DIRECT				TI DIRECT			
TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	REPLACEMENT	FOR NEW DESIGN	CLASS
2N5738	CTI	2N3792	PNP-Si	2N5888	CTI	CTI	PNP-Ge
2N5739	CTI	CTI	PNP-Si	2N5889	CTI	CTI	PNP-Ge
2N5740	CTI	CTI	PNP-Si	2N5900	CTI	CTI	PNP-Ge
2N5741	CTI	2N5883	PNP-Si	2N5901	CTI	CTI	PNP-Ge
2N5742	CTI	2N5884	PNP-Si	2N5926	CTI	CTI	NPN-Si
2N5743	CTI	CTI	PNP-Si	2N5927	CTI	CTI	NPN-Si
2N5744	CTI	CTI	PNP-Si	2N5928	CTI	CTI	NPN-Si
2N5745	CTI	2N5883	PNP-Si	2N5929	CTI	CTI	NPN-Si
2N5758	2N5758	2N5758	NPN-Si	2N5930	CTI	CTI	NPN-Si
2N5759	2N5759	2N5759	NPN-Si	2N5931	CTI	CTI	NPN-Si
2N5760	2N5760	2N5760	NPN-Si	2N5932	CTI	CTI	NPN-Si
2N5781	CTI	CTI	PNP-Si	2N5933	CTI	CTI	NPN-Si
2N5782	CTI	CTI	PNP-Si	2N5934	CTI	CTI	NPN-Si
2N5783	CTI	CTI	PNP-Si	2N5935	CTI	CTI	NPN-Si
2N5784	CTI	CTI	NPN-Si	2N5936	CTI	CTI	NPN-Si
2N5785	CTI	CTI	NPN-Si	2N5937	CTI	CTI	NPN-Si
2N5786	CTI	CTI	NPN-Si	2N5938	2N5938	CTI	NPN-Si
2N5787		TIC44	SCR	2N5939	2N5939	CTI	NPN-Si
2N5788		TIC45	SCR	2N5940	2N5940	CTI	NPN-Si
2N5791		CTI	SCR	2N5954	CTI	TIP41A	NPN-Si
2N5792		TIC39D	SCR	2N5955	CTI	TIP41A	NPN-Si
2N5804	CTI	TIP52	NPN-Si	2N5956	CTI	TIP41	NPN-Si
2N5805	CTI	TIP54	NPN-Si	2N5957	CTI	CTI	NPN-Si
2N5838		TIP52	NPN-Si	2N5958	CTI	CTI	NPN-Si
2N5839		TIP52	NPN-Si	2N5959	CTI	CTI	NPN-Si
2N5840		TIP54	NPN-Si	2N5960	CTI	CTI	NPN-Si
2N5853	CTI	2N5386	PNP-Si	2N5966	CTI	CTI	NPN-Si
2N5854	CTI	2N4301	NPN-Si	2N5967	CTI	CTI	NPN-Si
2N5867	2N5867	2N5867	PNP-Si	2N5968	CTI	CTI	NPN-Si
2N5868	2N5868	2N5868	PNP-Si	2N5969	CTI	CTI	NPN-Si
2N5869	2N5869	2N5869	NPN-Si	2N5970	CTI	CTI	NPN-Si
2N5870	2N5870	2N5870	NPN-Si	2N5971	CTI	CTI	NPN-Si
2N5871	2N5871	2N5871	PNP-Si	2N5972	CTI	CTI	NPN-Si
2N5872	2N5872	2N5872	PNP-Si	2N5973	CTI	CTI	NPN-Si
2N5873	2N5873	2N5873	NPN-Si	2N5974	CTI	TIP34	PNP-Si
2N5874	2N5874	2N5874	NPN-Si	2N5975	CTI	TIP34A	PNP-Si
2N5875	2N5875	2N5875	PNP-Si	2N5976	CTI	TIP34B	PNP-Si
2N5876	2N5876	2N5876	PNP-Si	2N5977	CTI	TIP33	NPN-Si
2N5877	2N5877	2N5877	NPN-Si	2N5978	CTI	TIP33A	NPN-Si
2N5878	2N5878	2N5878	NPN-Si	2N5979	CTI	TIP33B	NPN-Si
2N5879	2N5879	2N5879	PNP-Si	2N5980	CTI	TIP34	PNP-Si
2N5880	2N5880	2N5880	PNP-Si	2N5981	CTI	TIP34A	PNP-Si
2N5881	2N5881	2N5881	NPN-Si	2N5982	CTI	TIP34B	PNP-Si
2N5882	2N5882	2N5882	NPN-Si	2N5983	CTI	TIP33	NPN-Si
2N5883	2N5883	2N5883	PNP-Si	2N5984	CTI	TIP33A	NPN-Si
2N5884	2N5884	2N5884	PNP-Si	2N5985	CTI	TIP33B	NPN-Si
2N5885	2N5885	2N5885	NPN-Si	2N5986	CTI	TIP36	PNP-Si
2N5886	2N5886	2N5886	NPN-Si	2N5987	CTI	TIP36A	PNP-Si
2N5887	CTI	CTI	PNP-Ge	2N5988	CTI	TIP36B	PNP-Si

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CROSS-REFERENCE GUIDE

TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS
2N5989		TIP35	NPN-Si	2N6125		TIP32A	PNP-Si
2N5990		TIP35A	NPN-Si	2N6126		TIP32B	PNP-Si
2N5991		TIP35B	NPN-Si	2N6127	2N6127	2N6127	PNP-Si
2N6021		TIP32B	PNP-Si	2N6128	2N6128	2N6128	NPN-Si
2N6022		TIP32B	PNP-Si	2N6129		TIP41	NPN-Si
2N6023		TIP32	PNP-Si	2N6130		TIP41A	NPN-Si
2N6024		TIP32	PNP-Si	2N6131		TIP41B	NPN-Si
2N6025		TIP32A	PNP-Si	2N6132		TIP42	PNP-Si
2N6026		TIP32A	PNP-Si	2N6133		TIP42A	PNP-Si
2N6032	CTI	CTI	NPN-Si	2N6134		TIP42B	PNP-Si
2N6033	CTI	CTI	NPN-Si	2N6139		TIC236B	TRIAC
2N6046	CTI	2N4002	NPN-Si	2N6140		TIC236D	TRIAC
2N6047	CTI	2N4002	NPN-Si	2N6141		CTI	TRIAC
2N6048	CTI	2N4002	NPN-Si	2N6142		TIC236B	TRIAC
2N6049	CTI	CTI	PNP-Si	2N6143		TIC236D	TRIAC
2N6060	CTI	2N4002	NPN-Si	2N6144		CTI	TRIAC
2N6061	CTI	2N4002	NPN-Si	2N6148		TIC236B	TRIAC
2N6062	CTI	2N4002	NPN-Si	2N6149		TIC236D	TRIAC
2N6063	CTI	2N4002	NPN-Si	2N6150		CTI	TRIAC
2N6064	CTI	CTI	PNP-Ge	2N6154		TIC236B	TRIAC
2N6065	CTI	CTI	PNP-Ge	2N6155		TIC236D	TRIAC
2N6066	CTI	CTI	PNP-Ge	2N6156		CTI	TRIAC
2N6068		TIC226B	TRIAC	2N6157		TIC263B	TRIAC
2N6069		TIC226B	TRIAC	2N6158		TIC263D	TRIAC
2N6070		TIC226A	TRIAC	2N6159		TIC263M	TRIAC
2N6071		TIC226B	TRIAC	2N6160		TIC263B	TRIAC
2N6072		TIC226D	TRIAC	2N6161		TIC263D	TRIAC
2N6073		TIC226D	TRIAC	2N6162		TIC263M	TRIAC
2N6074		TIC226M	TRIAC	2N6175		TIP47	NPN-Si
2N6075		TIC226M	TRIAC	2N6176		TIP48	NPN-Si
2N6077	CTI	CTI	NPN-Si	2N6177		TIP49	NPN-Si
2N6078	CTI	CTI	NPN-Si	2N6178		TIP29B	NPN-Si
2N6079	CTI	CTI	NPN-Si	2N6179		TIP29A	NPN-Si
2N6098		TIP31A	NPN-Si	2N6180		TIP30B	PNP-Si
2N6099		TIP31A	NPN-Si	2N6181		TIP30A	PNP-Si
2N6100		TIP41B	NPN-Si	2N6182	CTI	2N5003	PNP-Si
2N6101		TIP41B	NPN-Si	2N6183	CTI	2N5005	PNP-Si
2N6102		TIP41	NPN-Si	2N6184	CTI	2N5003	PNP-Si
2N6103		TIP41	NPN-Si	2N6185	CTI	2N5003	PNP-Si
2N6106		TIP32B	PNP-Si	2N6186	CTI	2N5003	PNP-Si
2N6107		TIP32B	PNP-Si	2N6187	CTI	2N5005	PNP-Si
2N6108		TIP32A	PNP-Si	2N6188	CTI	2N5003	PNP-Si
2N6109		TIP32A	PNP-Si	2N6189	CTI	2N5005	PNP-Si
2N6110		TIP32	PNP-Si	2N6233	CTI	CTI	NPN-Si
2N6111		TIP32	PNP-Si	2N6234	CTI	CTI	NPN-Si
2N6121		TIP31	NPN-Si	2N6235	CTI	CTI	NPN-Si
2N6122		TIP31A	NPN-Si	2N6236		TIC106Y	SCR
2N6123		TIP31B	NPN-Si	2N6237		TIC106F	SCR
2N6124		TIP32	PNP-Si	2N6238		TIC106A	SCR

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CROSS-REFERENCE GUIDE

TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS	TYPE	TI DIRECT REPLACEMENT	FOR NEW DESIGN	CLASS
2N6239		TIC106B	SCR	2N6288		TIP41	NPN-Si
2N6240		TIC106D	SCR	2N6289		TIP41	NPN-Si
2N6241		CTI	SCR	2N6290		TIP41	NPN-Si
2N6246	CTI	2N5879	PNP-Si	2N6291		TIP41	NPN-Si
2N6247	CTI	2N5880	PNP-Si	2N6292		TIP41B	NPN-Si
2N6248	CTI	CTI	PNP-Si	2N6293		TIP41B	NPN-Si
2N6249	CTI	CTI	NPN-Si	2N6322	2N6322	2N6322	NPN-Si
2N6250	CTI	CTI	NPN-Si	2N6323	2N6323	2N6323	NPN-Si
2N6251	CTI	CTI	NPN-Si	2N6324	2N6324	2N6324	NPN-Si
2N6253	CTI	2N3713	NPN-Si	2N6325	2N6325	2N6325	NPN-Si
2N6254	CTI	2N3713	NPN-Si	2N6326	2N6326	2N6326	NPN-Si
2N6257	CTI	CTI	NPN-Si	2N6327	2N6327	2N6327	NPN-Si
2N6258	CTI	CTI	NPN-Si	2N6328	2N6328	2N6328	NPN-Si
2N6259	CTI	CTI	NPN-Si	2N6329	2N6329	2N6329	PNP-Si
2N6260*	CTI	CTI	NPN-Si	2N6330	2N6330	2N6330	PNP-Si
2N6261*	CTI	CTI	NPN-Si	2N6331	2N6331	2N6331	PNP-Si
2N6262	CTI	2N5885	NPN-Si	2N6332	2N6332	2N6332	SCR
2N6263	CTI	CTI	NPN-Si	2N6333	2N6333	2N6333	SCR
2N6264	CTI	CTI	NPN-Si	2N6334	2N6334	2N6334	SCR
2N6270	2N6270	2N6270	NPN-Si	2N6335	2N6335	2N6335	SCR
2N6271	2N6271	2N6271	NPN-Si	2N6336	2N6336	2N6336	SCR
2N6272	2N6272	2N6272	NPN-Si	2N6337	2N6337	2N6337	SCR
2N6273	2N6273	2N6273	NPN-Si				

* Asterisk denotes 2N numbers not JEDEC registered through December 1970.
CTI—Contact Texas Instruments.

KEY TO MANUFACTURERS

ECC—Electronic Control Corporation

FSC—Fairchild Semiconductor Corporation

GE—General Electric Company

MOTA—Motorola Semiconductor Products, Incorporated

RCA—Radio Corporation of America

SOD—Solitron Devices, Incorporated

TEC—Transitron Electronic Corporation

UNI—Unitrode Corporation

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
40250	RCA	TIP31	NPN-Si	40531	RCA	TIC205A	TRIAC
40251	RCA	2N5881	NPN-Si	40532	RCA	TIC205B	TRIAC
40310	RCA	TIP31	NPN-Si	40533	RCA	TIC106B	SCR
40312	RCA	TIP31A	NPN-Si	40534	RCA	TIC205A	TRIAC
40313	RCA	TIP48	NPN-Si	40535	RCA	TIC205B	TRIAC
40316	RCA	TIP31	NPN-Si	40536	RCA	TIC205D	TRIAC
40318	RCA	TIP48	NPN-Si	40553	RCA	TIC116B	SCR
40322	RCA	TIP48	NPN-Si	40554	RCA	TIC106D	SCR
40324	RCA	TIP31	NPN-Si	40575	RCA	TIC246B	TRIAC
40325	RCA	2N5877	NPN-Si	40576	RCA	TIC246D	TRIAC
40328	RCA	TIP48	NPN-Si	40613	RCA	TIP31	NPN-Si
40363	RCA	2N5877	NPN-Si	40618	RCA	TIP31	NPN-Si
40364	RCA	TIP31A	NPN-Si	40621	RCA	TIP31	NPN-Si
40369	RCA	2N3713	NPN-Si	40622	RCA	TIP31	NPN-Si
40372	RCA	TIP31A	NPN-Si	40624	RCA	TIP41	NPN-Si
40374	RCA	TIP47	NPN-Si	40627	RCA	TIP41A	NPN-Si
40375	RCA	TIP31A	NPN-Si	40629	RCA	TIP31	NPN-Si
40378	RCA	TIC106B	SCR	40630	RCA	TIP31	NPN-Si
40379	RCA	TIC116D	SCR	40631	RCA	TIP31	NPN-Si
40411	RCA	2N5878	NPN-Si	40632	RCA	TIP41A	NPN-Si
40429	RCA	TIC226B	TRIAC	40633	RCA	TIP33A	NPN-Si
40430	RCA	TIC226D	TRIAC	40636	RCA	2N5878	NPN-Si
40431	RCA	TIC226B	TRIAC	40638	RCA	TIC226B	TRIAC
40432	RCA	TIC226D	TRIAC	40654	RCA	TIC116B	SCR
40433	RCA	TIP48	NPN-Si	40655	RCA	TIC116D	SCR
40464	RCA	2N3715	NPN-Si	40656	RCA	TIC116B	SCR
40465	RCA	2N3715	NPN-Si	40657	RCA	TIC116D	SCR
40466	RCA	2N3715	NPN-Si	40658	RCA	TIC116B	SCR
40485	RCA	TIC226B	TRIAC	40659	RCA	TIC116D	SCR
40486	RCA	TIC226D	TRIAC	40664	RCA	TIC216D	TRIAC
40502	RCA	TIC226B	TRIAC	40667	RCA	TIC216D	TRIAC
40503	RCA	TIC226D	TRIAC	40668	RCA	TIC226B	TRIAC
40504	RCA	TIC106B	SCR	40669	RCA	TIC226D	TRIAC
40505	RCA	TIC106D	SCR	40684	RCA	TIC205A	TRIAC
40507	RCA	TIC106B	SCR	40685	RCA	TIC205B	TRIAC
40508	RCA	TIC116D	SCR	40686	RCA	TIC205D	TRIAC
40509	RCA	TIC226B	TRIAC	40691	RCA	TIC215B	TRIAC
40511	RCA	TIC226B	TRIAC	40692	RCA	TIC205D	TRIAC
40512	RCA	TIC226D	TRIAC	40693	RCA	TIC205A	TRIAC
40513	RCA	TIP33	NPN-Si	40694	RCA	TIC205B	TRIAC
40514	RCA	TIP33	NPN-Si	40696	RCA	TIC205A	TRIAC
40526	RCA	TIC205B	TRIAC	40697	RCA	TIC205B	TRIAC
40529	RCA	TIC205B	TRIAC	40698	RCA	TIC205D	TRIAC

CROSS-REFERENCE GUIDE

2

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
40711	RCA	TIC246B	TRIAC	40803	RCA	TIC246D	TRIAC
40712	RCA	TIC246D	TRIAC	40804	RCA	TIC253M	TRIAC
40713	RCA	TIC246B	TRIAC	40807	RCA	TIC253M	TRIAC
40714	RCA	TIC246D	TRIAC	40810	RCA	2N1595	SCR
40715	RCA	TIC246B	TRIAC	40811	RCA	2N1597	SCR
40716	RCA	TIC246D	TRIAC	40812	RCA	2N1599	SCR
40717	RCA	TIC236B	TRIAC	40816	RCA	TIP41	NPN-Si
40718	RCA	TIC236D	TRIAC	40829	RCA	TIP32B	PNP-Si
40719	RCA	TIC236B	TRIAC	40830	RCA	TIP32A	PNP-Si
40720	RCA	TIC236D	TRIAC	40831	RCA	TIP32	PNP-Si
40721	RCA	TIC226B	TRIAC	40840	RCA	TIP52†	NPN-Si
40722	RCA	TIC226D	TRIAC	40850	RCA	TIP48	NPN-Si
40723	RCA	TIC216D	TRIAC	40851	RCA	TIP49	NPN-Si
40725	RCA	TIC226B	TRIAC	40852	RCA	TIP53†	NPN-Si
40726	RCA	TIC216D	TRIAC	40853	RCA	TIP53†	NPN-Si
40727	RCA	TIC226B	TRIAC	40867	RCA	TIC116B	SCR
40728	RCA	TIC226D	TRIAC	40868	RCA	TIC116B	SCR
40729	RCA	TIC226B	TRIAC	40869	RCA	TIC116D	SCR
40731	RCA	TIC205B	TRIAC	40872	RCA	TIP32C	PNP-Si
40733	RCA	TIC226B	TRIAC	40874	RCA	TIP32B	PNP-Si
40737	RCA	TIC116A	SCR	40876	RCA	TIP32A	PNP-Si
40738	RCA	TIC116B	SCR	40884	RCA	TIP41A	NPN-Si
40739	RCA	TIC126D	SCR	A01001	ECC	TIC206B	TRIAC
40740	RCA	TIC126M	SCR	A01002	ECC	TIC206B	TRIAC
40741	RCA	TIC116A	SCR	A01003	ECC	TIC206D	TRIAC
40742	RCA	TIC116B	SCR	A01004	ECC	TIC206D	TRIAC
40743	RCA	TIC126D	SCR	A01021	ECC	TIC216B	TRIAC
40744	RCA	TIC126M	SCR	A01022	ECC	TIC216D	TRIAC
40745	RCA	TIC116A	SCR	A01061	ECC	TIC226B	TRIAC
40746	RCA	TIC116B	SCR	A01062	ECC	TIC226D	TRIAC
40747	RCA	TIC126D	SCR	A01101	ECC	TIC236B	TRIAC
40748	RCA	TIC126M	SCR	A01102	ECC	TIC236D	TRIAC
40761	RCA	TIC215B	TRIAC	A01141	ECC	TIC246B	TRIAC
40773	RCA	TIC205B	TRIAC	A01142	ECC	TIC246D	TRIAC
40774	RCA	TIC205D	TRIAC	A01181	ECC	TIC253B	TRIAC
40775	RCA	TIC216B	TRIAC	A01182	ECC	TIC253D	TRIAC
40776	RCA	TIC226D	TRIAC	A03001	ECC	TIC206B	TRIAC
40778	RCA	TIC226D	TRIAC	A03002	ECC	TIC206B	TRIAC
40779	RCA	TIC236B	TRIAC	A03003	ECC	TIC206D	TRIAC
40780	RCA	TIC236D	TRIAC	A03004	ECC	TIC206D	TRIAC
40781	RCA	TIC236B	TRIAC	AA100	UNI	2N3002	SCR
40782	RCA	TIC236D	TRIAC	AA101	UNI	2N3003	SCR
40783	RCA	TIC246B	TRIAC	AA103	UNI	2N1598	SCR
40784	RCA	TIC246D	TRIAC	AA107	UNI	2N3002	SCR
40785	RCA	TIC246B	TRIAC	AA108	UNI	TIC39A	SCR
40786	RCA	TIC246D	TRIAC	AA110	UNI	2N1598	SCR
40797	RCA	TIC253M	TRIAC	AA114	UNI	2N3002	SCR
40798	RCA	TIC253M	TRIAC	AA115	UNI	2N3007	SCR
40799	RCA	TIC236B	TRIAC	AA117	UNI	2N1598	SCR
40802	RCA	TIC246B	TRIAC	AD100	UNI	TIC39F	SCR

Refer to page 2-17 for key to manufacturers.

† Contact Texas Instruments for direct replacement.

CROSS-REFERENCE GUIDE

2

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
AD101	UNI	TIC39A	SCR	B04025	ECC	TIC106D	SCR
AD103	UNI	TIC106C	SCR	B04026	ECC	TIC106D	SCR
AD107	UNI	TIC39F	SCR	B05001	ECC	TIC116B	SCR
AD108	UNI	TIC39A	SCR	B05002	ECC	TIC116B	SCR
AD110	UNI	2N1598	SCR	B05003	ECC	TIC116D	SCR
AD111	UNI	TIC106D	SCR	B05004	ECC	TIC116D	SCR
AD114	UNI	TIC39F	SCR	B05005	ECC	TIC116M	SCR
AD115	UNI	TIC39A	SCR	B05006	ECC	TIC116M	SCR
AD117	UNI	2N1598	SCR	B05021	ECC	TIC126B	SCR
AD118	UNI	TIC106D	SCR	B05022	ECC	TIC126B	SCR
B01021	ECC	TIC106B	SCR	B05023	ECC	TIC126D	SCR
B01022	ECC	TIC106B	SCR	B05024	ECC	TIC126D	SCR
B01023	ECC	TIC106B	SCR	B05025	ECC	TIC126M	SCR
B01024	ECC	TIC106D	SCR	B05026	ECC	TIC126M	SCR
B01025	ECC	TIC106D	SCR	B05041	ECC	TIC126B	SCR
B01026	ECC	TIC106D	SCR	B05042	ECC	TIC126B	SCR
B01051	ECC	TIC116B	SCR	B05043	ECC	TIC126D	SCR
B01052	ECC	TIC116B	SCR	B05044	ECC	TIC126D	SCR
B01053	ECC	TIC116D	SCR	B05045	ECC	TIC126M	SCR
B01054	ECC	TIC116D	SCR	B05046	ECC	TIC126M	SCR
B01055	ECC	TIC116M	SCR	B150	UNI	2N3005	SCR
B01056	ECC	TIC116M	SCR	B151	UNI	2N3006	SCR
B01071	ECC	TIC126B	SCR	B152	UNI	2N3007	SCR
B01072	ECC	TIC126B	SCR	BA150*	UNI	2N3005	SCR
B01073	ECC	TIC126D	SCR	BA151*	UNI	2N3006	SCR
B01074	ECC	TIC126D	SCR	BA152*	UNI	2N3007	SCR
B01075	ECC	TIC126M	SCR	BD100*	UNI	2N3005	SCR
B01076	ECC	TIC126M	SCR	BD101*	UNI	2N3006	SCR
B01091	ECC	TIC126B	SCR	BD102*	UNI	2N3007	SCR
B01092	ECC	TIC126B	SCR	BTD0105	TEC	TIC205A	TRIAC
B01093	ECC	TIC126D	SCR	BTD0110	TEC	TIC205A	TRIAC
B01094	ECC	TIC126D	SCR	BTD0120	TEC	TIC205B	TRIAC
B01095	ECC	TIC126M	SCR	BTD0130	TEC	TIC205D	TRIAC
B01096	ECC	TIC126M	SCR	BTD0140	TEC	TIC205D	TRIAC
B03001	ECC	TIC106B	SCR	BTD0150	TEC	CTI	TRIAC
B03002	ECC	TIC106B	SCR	BTD0160	TEC	CTI	TRIAC
B03003	ECC	TIC106B	SCR	BTD0205	TEC	TIC205A	TRIAC
B03004	ECC	TIC106D	SCR	BTD0210	TEC	TIC205A	TRIAC
B03005	ECC	TIC106D	SCR	BTD0220	TEC	TIC205B	TRIAC
B03006	ECC	TIC106D	SCR	BTD0230	TEC	TIC205D	TRIAC
B04001	ECC	TIC39B	SCR	BTD0240	TEC	TIC205D	TRIAC
B04002	ECC	TIC39B	SCR	BTD0250	TEC	CTI	TRIAC
B04003	ECC	TIC39B	SCR	BTD0260	TEC	CTI	TRIAC
B04004	ECC	TIC39D	SCR	BTR0205	TEC	TIC206A	TRIAC
B04005	ECC	TIC39D	SCR	BTR0210	TEC	TIC206A	TRIAC
B04006	ECC	TIC39D	SCR	BTR0220	TEC	TIC206B	TRIAC
B04021	ECC	TIC106B	SCR	BTR0230	TEC	TIC206D	TRIAC
B04022	ECC	TIC106B	SCR	BTR0240	TEC	TIC206D	TRIAC
B04023	ECC	TIC106B	SCR	BTR0250	TEC	CTI	TRIAC
B04024	ECC	TIC106D	SCR	BTR0260	TEC	CTI	TRIAC

Refer to page 2-17 for key to manufacturers.

*These are the designations of the indicated manufacturer and should not be confused with Pro Electron designations.

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CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
BTR0305	TEC	TIC206A	TRIAC	BTU0410	TEC	TIC226B	TRIAC
BTR0310	TEC	TIC206A	TRIAC	BTU0420	TEC	TIC226B	TRIAC
BTR0320	TEC	TIC206B	TRIAC	BTU0430	TEC	TIC226D	TRIAC
BTR0330	TEC	TIC206D	TRIAC	BTU0440	TEC	TIC226D	TRIAC
BTR0340	TEC	TIC206D	TRIAC	BTU0450	TEC	CTI	TRIAC
BTR0350	TEC	CTI	TRIAC	BTU0460	TEC	CTI	TRIAC
BTR0360	TEC	CTI	TRIAC	BTU0505	TEC	TIC236B	TRIAC
BTR0405	TEC	TIC206A	TRIAC	BTU0510	TEC	TIC236B	TRIAC
BTR0410	TEC	TIC206A	TRIAC	BTU0520	TEC	TIC236B	TRIAC
BTR0420	TEC	TIC206B	TRIAC	BTU0530	TEC	TIC236D	TRIAC
BTR0430	TEC	TIC206D	TRIAC	BTU0540	TEC	TIC236D	TRIAC
BTR0440	TEC	TIC205D	TRIAC	BTU0560	TEC	CTI	TRIAC
BTR0450	TEC	CTI	TRIAC	BTU0605	TEC	TIC246B	TRIAC
BTR0460	TEC	CTI	TRIAC	BTU0610	TEC	TIC246B	TRIAC
BTS0205	TEC	TIC216A	TRIAC	BTU0620	TEC	TIC246B	TRIAC
BTS0210	TEC	TIC216A	TRIAC	BTU0630	TEC	TIC246D	TRIAC
BTS0220	TEC	TIC216B	TRIAC	BTU0640	TEC	TIC246D	TRIAC
BTS0230	TEC	TIC216D	TRIAC	BTU0650	TEC	CTI	TRIAC
BTS0240	TEC	TIC216D	TRIAC	BTU0660	TEC	CTI	TRIAC
BTS0250	TEC	CTI	TRIAC	C5A	GE	2N1596	SCR
BTS0260	TEC	CTI	TRIAC	C5B	GE	2N1597	SCR
BTS0305	TEC	TIC226B	TRIAC	C5D	GE	2N1599	SCR
BTS0310	TEC	TIC226B	TRIAC	C5F	GE	2N1595	SCR
BTS0320	TEC	TIC226B	TRIAC	C5G	GE	2N1597	SCR
BTS0330	TEC	TIC226D	TRIAC	C5H	GE	2N1598	SCR
BTS0340	TEC	TIC226D	TRIAC	C5U	GE	2N1595	SCR
BTS0350	TEC	CTI	TRIAC	C6A	GE	2N1596	SCR
BTS0360	TEC	CTI	TRIAC	C6B	GE	2N1597	SCR
BTS0405	TEC	TIC226B	TRIAC	C6F	GE	2N1595	SCR
BTS0410	TEC	TIC226B	TRIAC	C6G	GE	2N1597	SCR
BTS0420	TEC	TIC226B	TRIAC	C6U	GE	2N1595	SCR
BTS0430	TEC	TIC226D	TRIAC	C10A	GE	TIC116A	SCR
BTS0440	TEC	TIC226D	TRIAC	C10B	GE	TIC116B	SCR
BTS0450	TEC	CTI	TRIAC	C10C	GE	TIC116C	SCR
BTS0460	TEC	CTI	TRIAC	C10D	GE	TIC116D	SCR
BTS0505	TEC	TIC236B	TRIAC	C10F	GE	TIC116F	SCR
BTS0510	TEC	TIC236B	TRIAC	C10G	GE	TIC116B	SCR
BTS0520	TEC	TIC236B	TRIAC	C10H	GE	TIC116C	SCR
BTS0530	TEC	TIC236D	TRIAC	C10U	GE	TIC116F	SCR
BTS0540	TEC	TIC236D	TRIAC	C11A	GE	TIC116A	SCR
BTS0550	TEC	CTI	TRIAC	C11B	GE	TIC116B	SCR
BTS0560	TEC	CTI	TRIAC	C11C	GE	TIC116C	SCR
BTU0305	TEC	TIC226B	TRIAC	C11D	GE	TIC116D	SCR
BTU0310	TEC	TIC226B	TRIAC	C11E	GE	TIC116E	SCR
BTU0320	TEC	TIC226B	TRIAC	C11F	GE	TIC116F	SCR
BTU0330	TEC	TIC226D	TRIAC	C11G	GE	TIC116B	SCR
BTU0340	TEC	TIC226D	TRIAC	C11H	GE	TIC116C	SCR
BTU0350	TEC	CTI	TRIAC	C11M	GE	TIC116M	SCR
BTU0360	TEC	CTI	TRIAC	C11U	GE	TIC116F	SCR
BTU0405	TEC	TIC226B	TRIAC	C12A	GE	TIC116A	SCR

Refer to page 2-17 for key to manufacturers.

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CROSS-REFERENCE GUIDE

2

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
C12B	GE	TIC116B	SCR	C122E	GE	TIC116E	SCR
C12C	GE	TIC116C	SCR	C122F	GE	TIC116F	SCR
C12D	GE	TIC116D	SCR	C220A	GE	TIC126A	SCR
C12F	GE	TIC116F	SCR	C220B	GE	TIC126B	SCR
C12G	GE	TIC116B	SCR	C220C	GE	TIC126C	SCR
C12H	GE	TIC116C	SCR	C220D	GE	TIC126D	SCR
C12U	GE	TIC116F	SCR	C220E	GE	TIC126E	SCR
C15A	GE	TIC116A	SCR	C220F	GE	TIC126F	SCR
C15B	GE	TIC116B	SCR	C220U	GE	TIC126F	SCR
C15C	GE	TIC116C	SCR	C222A	GE	TIC126A	SCR
C15D	GE	TIC116D	SCR	C222B	GE	TIC126B	SCR
C15E	GE	TIC116E	SCR	C222C	GE	TIC126C	SCR
C15F	GE	TIC116F	SCR	C222D	GE	TIC126D	SCR
C15G	GE	TIC116B	SCR	C222E	GE	TIC126E	SCR
C15M	GE	TIC116M	SCR	C222F	GE	TIC126F	SCR
C15U	GE	TIC116F	SCR	C222U	GE	TIC126F	SCR
C20A	GE	TIC116A	SCR	C611A	GE	2N1596	SCR
C20B	GE	TIC116B	SCR	C611B	GE	2N1597	SCR
C20C	GE	TIC116C	SCR	C611F	GE	2N1595	SCR
C20D	GE	TIC116D	SCR	C611G	GE	2N1597	SCR
C20F	GE	TIC116F	SCR	C611U	GE	2N1595	SCR
C20U	GE	TIC116F	SCR	CB200	UNI	2N3005	SCR
C22A	GE	TIC116A	SCR	CB201	UNI	2N3006	SCR
C22B	GE	TIC116B	SCR	CB202	UNI	2N3007	SCR
C22C	GE	TIC116C	SCR	CB203	UNI	2N3008	SCR
C22D	GE	TIC116D	SCR	CD200	UNI	TIC39Y	SCR
C22F	GE	TIC116F	SCR	CD201	UNI	TIC39A	SCR
C22U	GE	TIC116F	SCR	CD202	UNI	TIC39A	SCR
C103A	GE	TIC46	SCR	CD203	UNI	TIC39B	SCR
C103B	GE	TIC47	SCR	CM100	UNI	TIC106A	SCR
C103Y	GE	TIC44	SCR	CM101	UNI	TIC106A	SCR
C103YY	GE	TIC45	SCR	CM102	UNI	TIC106B	SCR
C106A	GE	TIC106A	SCR	CM103	UNI	TIC106C	SCR
C106B	GE	TIC106B	SCR	CM104	UNI	TIC106D	SCR
C106C	GE	TIC106C	SCR	CM106	UNI	TIC106A	SCR
C106D	GE	TIC106D	SCR	CM107	UNI	TIC106A	SCR
C106F	GE	TIC106F	SCR	CM108	UNI	TIC106B	SCR
C106Q	GE	TIC106Y	SCR	CM109	UNI	TIC106C	SCR
C106Y	GE	TIC106Y	SCR	CM110	UNI	TIC106D	SCR
C107A	GE	TIC106A	SCR	D40D1	GE	TIP29	NPN-Si
C107B	GE	TIC106B	SCR	D40D2	GE	TIP29	NPN-Si
C107C	GE	TIC106C	SCR	D40D4	GE	TIP29	NPN-Si
C107D	GE	TIC106D	SCR	D40D5	GE	TIP29	NPN-Si
C107F	GE	TIC106F	SCR	D40D7	GE	TIP29A	NPN-Si
C107Q	GE	TIC106Y	SCR	D40D8	GE	TIP29A	NPN-Si
C107Y	GE	TIC106Y	SCR	D40D10	GE	TIP29B	NPN-Si
C122A	GE	TIC116A	SCR	D40D11	GE	TIP29B	NPN-Si
C122B	GE	TIC116B	SCR	D40N1	GE	TIP47	NPN-Si
C122C	GE	TIC116C	SCR	D40N2	GE	TIP47	NPN-Si
C122D	GE	TIC116D	SCR	D40N3	GE	TIP48	NPN-Si

Refer to page 2-17 for key to manufacturers.

CROSS-REFERENCE GUIDE

2

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
D40N4	GE	TIP48	NPN-Si	D44H8	GE	TIP41A	NPN-Si
D40P1	GE	TIP47	NPN-Si	D44H10	GE	TIP41B	NPN-Si
D40P3	GE	TIP47	NPN-Si	D44H11	GE	TIP41B	NPN-Si
D40P5	GE	TIP47	NPN-Si	D44R1	GE	TIP47	NPN-Si
D41D1	GE	TIP30	PNP-Si	D44R2	GE	TIP47	NPN-Si
D41D2	GE	TIP30	PNP-Si	D44R3	GE	TIP48	NPN-Si
D41D4	GE	TIP30	PNP-Si	D44R4	GE	TIP48	NPN-Si
D41D5	GE	TIP30	PNP-Si	D45C1	GE	TIP32	PNP-Si
D41D7	GE	TIP30A	PNP-Si	D45C2	GE	TIP32	PNP-Si
D41D8	GE	TIP30A	PNP-Si	D45C3	GE	TIP32	PNP-Si
D41D10	GE	TIP30B	PNP-Si	D45C4	GE	TIP32	PNP-Si
D41D11	GE	TIP30B	PNP-Si	D45C5	GE	TIP32	PNP-Si
D42C1	GE	TIP31	NPN-Si	D45C6	GE	TIP32	PNP-Si
D42C2	GE	TIP31	NPN-Si	D45C7	GE	TIP32A	PNP-Si
D42C3	GE	TIP31	NPN-Si	D45C8	GE	TIP32A	PNP-Si
D42C4	GE	TIP31	NPN-Si	D45C9	GE	TIP32A	PNP-Si
D42C5	GE	TIP31	NPN-Si	D45C10	GE	TIP32B	PNP-Si
D42C6	GE	TIP31	NPN-Si	D45C11	GE	TIP32B	PNP-Si
D42C7	GE	TIP31A	NPN-Si	D45H1	GE	TIP42	PNP-Si
D42C8	GE	TIP31A	NPN-Si	D45H2	GE	TIP42	PNP-Si
D42C9	GE	TIP31A	NPN-Si	D45H4	GE	TIP42	PNP-Si
D42C10	GE	TIP31B	NPN-Si	D45H5	GE	TIP42	PNP-Si
D42C11	GE	TIP31B	NPN-Si	D45H7	GE	TIP42A	PNP-Si
D43C1	GE	TIP32	PNP-Si	D45H8	GE	TIP42A	PNP-Si
D43C2	GE	TIP32	PNP-Si	D45H10	GE	TIP42B	PNP-Si
D43C3	GE	TIP32	PNP-Si	D45H11	GE	TIP42B	PNP-Si
D43C4	GE	TIP32	PNP-Si	FT1869	FSC	TIC39Y	SCR
D43C5	GE	TIP32	PNP-Si	FT2009	FSC	TIC39Y	SCR
D43C6	GE	TIP32	PNP-Si	FT2010	FSC	TIC39Y	SCR
D43C7	GE	TIP32A	PNP-Si	GA200	UNI	TIC45	SCR
D43C8	GE	TIP32A	PNP-Si	GA200A	UNI	TIC45	SCR
D43C9	GE	TIP32A	PNP-Si	GA201	UNI	TIC39A	SCR
D43C10	GE	TIP32B	PNP-Si	GA201A	UNI	TIC39A	SCR
D43C11	GE	TIP32B	PNP-Si	GA300	UNI	TIC45	SCR
D44C1	GE	TIP31	NPN-Si	GA300A	UNI	TIC45	SCR
D44C2	GE	TIP31	NPN-Si	GA301	UNI	TIC39A	SCR
D44C3	GE	TIP31	NPN-Si	GA301A	UNI	TIC39A	SCR
D44C4	GE	TIP31	NPN-Si	GB200	UNI	TIC116A	SCR
D44C5	GE	TIP31	NPN-Si	GB200A	UNI	TIC116A	SCR
D44C6	GE	TIP31	NPN-Si	GB300	UNI	TIC106A	SCR
D44C7	GE	TIP31A	NPN-Si	GB300A	UNI	TIC106A	SCR
D44C8	GE	TIP31A	NPN-Si	HR878	UNI	2N3006	SCR
D44C9	GE	TIP31A	NPN-Si	HR878A	UNI	2N3002	SCR
D44C10	GE	TIP31B	NPN-Si	HR879A	UNI	TIC39A	SCR
D44C11	GE	TIP31B	NPN-Si	HR879B	UNI	TIC39A	SCR
D44H1	GE	TIP41	NPN-Si	HR3028	UNI	TIC46	SCR
D44H2	GE	TIP41	NPN-Si	HR3029	UNI	TIC39A	SCR
D44H4	GE	TIP41	NPN-Si	HR3031	UNI	TIC46	SCR
D44H5	GE	TIP41	NPN-Si	HR3032	UNI	TIC39A	SCR
D44H7	GE	TIP41A	NPN-Si	MAC1-1	MOTA	TIC226B	TRIAC

Refer to page 2-17 for key to manufacturers.

CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
MAC1-2	MOTA	TIC226B	TRIAC	MAC7-4	MOTA	TIC226B	TRIAC
MAC1-3	MOTA	TIC226B	TRIAC	MAC7-5	MOTA	TIC226D	TRIAC
MAC1-4	MOTA	TIC226B	TRIAC	MAC7-6	MOTA	TIC226D	TRIAC
MAC1-5	MOTA	TIC226D	TRIAC	MAC7-7	MOTA	CTI	TRIAC
MAC1-6	MOTA	TIC226D	TRIAC	MAC7-8	MOTA	CTI	TRIAC
MAC1-7	MOTA	CTI	TRIAC	MAC8-1	MOTA	TIC226B	TRIAC
MAC1-8	MOTA	CTI	TRIAC	MAC8-2	MOTA	TIC226B	TRIAC
MAC2-1	MOTA	TIC226B	TRIAC	MAC8-3	MOTA	TIC226B	TRIAC
MAC2-2	MOTA	TIC226B	TRIAC	MAC8-4	MOTA	TIC226B	TRIAC
MAC2-3	MOTA	TIC226B	TRIAC	MAC8-5	MOTA	TIC226D	TRIAC
MAC2-4	MOTA	TIC226B	TRIAC	MAC8-6	MOTA	TIC226D	TRIAC
MAC2-5	MOTA	TIC226D	TRIAC	MAC8-7	MOTA	CTI	TRIAC
MAC2-6	MOTA	TIC226D	TRIAC	MAC8-8	MOTA	CTI	TRIAC
MAC2-7	MOTA	CTI	TRIAC	MAC9-1	MOTA	TIC226B	TRIAC
MAC2-8	MOTA	CTI	TRIAC	MAC9-2	MOTA	TIC226B	TRIAC
MAC3-1	MOTA	TIC226B	TRIAC	MAC9-3	MOTA	TIC226B	TRIAC
MAC3-2	MOTA	TIC226B	TRIAC	MAC9-4	MOTA	TIC226B	TRIAC
MAC3-3	MOTA	TIC226B	TRIAC	MAC9-5	MOTA	TIC226D	TRIAC
MAC3-4	MOTA	TIC226B	TRIAC	MAC9-6	MOTA	TIC226D	TRIAC
MAC3-5	MOTA	TIC226D	TRIAC	MAC9-7	MOTA	CTI	TRIAC
MAC3-6	MOTA	TIC226D	TRIAC	MAC9-8	MOTA	CTI	TRIAC
MAC3-7	MOTA	CTI	TRIAC	MAC10-1	MOTA	TIC226B	TRIAC
MAC3-8	MOTA	CTI	TRIAC	MAC10-2	MOTA	TIC226B	TRIAC
MAC4-1	MOTA	TIC226B	TRIAC	MAC10-3	MOTA	TIC226B	TRIAC
MAC4-2	MOTA	TIC226B	TRIAC	MAC10-4	MOTA	TIC226B	TRIAC
MAC4-3	MOTA	TIC226B	TRIAC	MAC10-5	MOTA	TIC226D	TRIAC
MAC4-4	MOTA	TIC226B	TRIAC	MAC10-6	MOTA	TIC226D	TRIAC
MAC4-5	MOTA	TIC226D	TRIAC	MAC10-7	MOTA	CTI	TRIAC
MAC4-6	MOTA	TIC226D	TRIAC	MAC10-8	MOTA	CTI	TRIAC
MAC4-7	MOTA	CTI	TRIAC	MAC11-1	MOTA	TIC226B	TRIAC
MAC4-8	MOTA	CTI	TRIAC	MAC11-2	MOTA	TIC226B	TRIAC
MAC5-1	MOTA	TIC226B	TRIAC	MAC11-3	MOTA	TIC226B	TRIAC
MAC5-2	MOTA	TIC226B	TRIAC	MAC11-4	MOTA	TIC226B	TRIAC
MAC5-3	MOTA	TIC226B	TRIAC	MAC11-5	MOTA	TIC226D	TRIAC
MAC5-4	MOTA	TIC226B	TRIAC	MAC11-6	MOTA	TIC226D	TRIAC
MAC5-5	MOTA	TIC226D	TRIAC	MAC11-7	MOTA	CTI	TRIAC
MAC5-6	MOTA	TIC226D	TRIAC	MAC11-8	MOTA	CTI	TRIAC
MAC5-7	MOTA	CTI	TRIAC	MAC35-1	MOTA	TIC263B	TRIAC
MAC5-8	MOTA	CTI	TRIAC	MAC35-2	MOTA	TIC263B	TRIAC
MAC6-1	MOTA	TIC226B	TRIAC	MAC35-3	MOTA	TIC263B	TRIAC
MAC6-2	MOTA	TIC226B	TRIAC	MAC35-4	MOTA	TIC263B	TRIAC
MAC6-3	MOTA	TIC226B	TRIAC	MAC35-5	MOTA	TIC263D	TRIAC
MAC6-4	MOTA	TIC226B	TRIAC	MAC35-6	MOTA	TIC263D	TRIAC
MAC6-5	MOTA	TIC226D	TRIAC	MAC35-7	MOTA	TIC263E	TRIAC
MAC6-6	MOTA	TIC226D	TRIAC	MAC36-1	MOTA	TIC263B	TRIAC
MAC6-7	MOTA	CTI	TRIAC	MAC36-2	MOTA	TIC263B	TRIAC
MAC6-8	MOTA	CTI	TRIAC	MAC36-3	MOTA	TIC263B	TRIAC
MAC7-1	MOTA	TIC226B	TRIAC	MAC36-4	MOTA	TIC263B	TRIAC
MAC7-2	MOTA	TIC226B	TRIAC	MAC36-5	MOTA	TIC263D	TRIAC
MAC7-3	MOTA	TIC226B	TRIAC	MAC36-6	MOTA	TIC263D	TRIAC

Refer to page 2-17 for key to manufacturers.

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CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
MAC36-7	MOTA	TIC263E	TRIAC
MAC37-1	MOTA	TIC263B	TRIAC
MAC37-2	MOTA	TIC263B	TRIAC
MAC37-3	MOTA	TIC263B	TRIAC
MAC37-4	MOTA	TIC263B	TRIAC
MAC37-5	MOTA	TIC263D	TRIAC
MAC37-6	MOTA	TIC263D	TRIAC
MAC37-7	MOTA	TIC263E	TRIAC
MAC38-1	MOTA	TIC263B	TRIAC
MAC38-2	MOTA	TIC263B	TRIAC
MAC38-3	MOTA	TIC263B	TRIAC
MAC38-4	MOTA	TIC263B	TRIAC
MAC38-5	MOTA	TIC263D	TRIAC
MAC38-6	MOTA	TIC263D	TRIAC
MAC38-7	MOTA	TIC263E	TRIAC
MAC77-1	MOTA	TIC206A	TRIAC
MAC77-2	MOTA	TIC206A	TRIAC
MAC77-3	MOTA	TIC206A	TRIAC
MAC77-4	MOTA	TIC206B	TRIAC
MAC77-5	MOTA	TIC206D	TRIAC
MAC77-6	MOTA	TIC206D	TRIAC
MAC77-7	MOTA	CTI	TRIAC
MAC77-8	MOTA	CTI	TRIAC
MCR101	MOTA	TIC44	SCR
MCR102	MOTA	TIC44	SCR
MCR103	MOTA	TIC45	SCR
MCR104	MOTA	TIC46	SCR
MCR106-1	MOTA	TIC106Y	SCR
MCR106-2	MOTA	TIC106A	SCR
MCR106-3	MOTA	TIC106A	SCR
MCR106-4	MOTA	TIC106B	SCR
MCR115	MOTA	TIC47	SCR
MCR120	MOTA	TIC47	SCR
MCR406-1	MOTA	TIC106Y	SCR
MCR406-2	MOTA	TIC106A	SCR
MCR406-3	MOTA	TIC106A	SCR
MCR406-4	MOTA	TIC106B	SCR
MCR407-1	MOTA	TIC106Y	SCR
MCR407-2	MOTA	TIC106A	SCR
MCR407-3	MOTA	TIC106A	SCR
MCR407-4	MOTA	TIC106B	SCR
MCR2315-1	MOTA	TIC116F	SCR
MCR2315-2	MOTA	TIC116F	SCR
MCR2315-3	MOTA	TIC116A	SCR
MCR2315-4	MOTA	TIC116B	SCR
MCR2315-5	MOTA	TIC116D	SCR
MCR2315-6	MOTA	TIC116D	SCR
MCR3000-1	MOTA	TIC116F	SCR
MCR3000-2	MOTA	TIC116F	SCR
MCR3000-3	MOTA	TIC116A	SCR

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
MCR3000-4	MOTA	TIC116B	SCR
MCR3000-5	MOTA	TIC116D	SCR
MCR3000-6	MOTA	TIC116D	SCR
MCR3000-7	MOTA	TIC116E	SCR
MCR3000-8	MOTA	TIC116M	SCR
MJ400	MOTA	TIP49	NPN-Si
MJ413	MOTA	TIP54	NPN-Si
MJ423	MOTA	TIP54	NPN-Si
MJ431	MOTA	TIP54	NPN-Si
MJ450	MOTA	TIP32	PNP-Si
MJ480	MOTA	2N3713	NPN-Si
MJ481	MOTA	2N3714	NPN-Si
MJ490	MOTA	TIP34	PNP-Si
MJ491	MOTA	TIP34	PNP-Si
MJ500	MOTA	TIP42	PNP-Si
MJ501	MOTA	TIP42A	PNP-Si
MJ802	MOTA	2N3716	NPN-Si
MJ900	MOTA	2N3789	PNP-Si
MJ901	MOTA	2N3790	PNP-Si
MJ1000	MOTA	2N3713	NPN-Si
MJ1001	MOTA	2N3714	NPN-Si
MJ1800	MOTA	TIP51	NPN-Si
MJ2249	MOTA	TIP31A	NPN-Si
MJ2250	MOTA	TIP31B	NPN-Si
MJ2251	MOTA	TIP47	NPN-Si
MJ2252	MOTA	TIP48	NPN-Si
MJ2253	MOTA	TIP32	PNP-Si
MJ2254	MOTA	TIP32B	PNP-Si
MJ2267	MOTA	2N3789	PNP-Si
MJ2268	MOTA	2N3790	PNP-Si
MJ2500	MOTA	TIP145	PNP-Si
MJ2501	MOTA	TIP146	PNP-Si
MJ2840	MOTA	TIP41A	NPN-Si
MJ2841	MOTA	TIP41B	NPN-Si
MJ2901	MOTA	2N3055	NPN-Si
MJ2940	MOTA	TIP41A	NPN-Si
MJ2941	MOTA	TIP41B	NPN-Si
MJ3000	MOTA	TIP140	NPN-Si
MJ3001	MOTA	TIP141	NPN-Si
MJ3010	MOTA	TIP51	NPN-Si
MJ3011	MOTA	TIP53	NPN-Si
MJ3029	MOTA	TIP51	NPN-Si
MJ3030	MOTA	TIP53	NPN-Si
MJ3101	MOTA	TIP31	NPN-Si
MJ3201	MOTA	TIP47	NPN-Si
MJ3202	MOTA	TIP48	NPN-Si
MJ3701	MOTA	TIP32	PNP-Si
MJ3771	MOTA	2N5301	NPN-Si
MJ3772	MOTA	2N5301	NPN-Si
MJ3801	MOTA	TIP33B	NPN-Si

Refer to page 2-17 for key to manufacturers.

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CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
MJ3802	MOTA	TIP33B	NPN-Si	MJE1101	MOTA	TIP120	NPN-Si
MJ4000	MOTA	TIP120	NPN-Si	MJE1102	MOTA	TIP121	NPN-Si
MJ4001	MOTA	TIP121	NPN-Si	MJE1103	MOTA	TIP121	NPN-Si
MJ4010	MOTA	TIP125	PNP-Si	MJE1290	MOTA	TIP34	PNP-Si
MJ4011	MOTA	TIP126	PNP-Si	MJE1291	MOTA	TIP34A	PNP-Si
MJ4030	MOTA	TIP145	PNP-Si	MJE1660	MOTA	TIP33	NPN-Si
MJ4031	MOTA	TIP146	PNP-Si	MJE1661	MOTA	TIP33A	NPN-Si
MJ4032	MOTA	TIP147	PNP-Si	MJE2010	MOTA	TIP34	PNP-Si
MJ4033	MOTA	TIP145	PNP-Si	MJE2011	MOTA	TIP34A	PNP-Si
MJ4034	MOTA	TIP146	PNP-Si	MJE2020	MOTA	TIP33	NPN-Si
MJ4035	MOTA	TIP147	PNP-Si	MJE2021	MOTA	TIP33A	NPN-Si
MJ4101	MOTA	TIP31	NPN-Si	MJE2360	MOTA	TIP54	NPN-Si
MJ4502	MOTA	2N4399	PNP-Si	MJE2361	MOTA	TIP54	NPN-Si
MJ6700	MOTA	TIP41	NPN-Si	MJE2370	MOTA	TIP34	PNP-Si
MJ6701	MOTA	TIP41A	NPN-Si	MJE2371	MOTA	TIP34A	PNP-Si
MJ7000	MOTA	2N5303	NPN-Si	MJE2480	MOTA	TIP33	NPN-Si
MJ7200	MOTA	CTI	NPN-Si	MJE2481	MOTA	TIP33A	NPN-Si
MJ7201	MOTA	CTI	NPN-Si	MJE2482	MOTA	TIP33	NPN-Si
MJ8100	MOTA	CTI	PNP-Si	MJE2483	MOTA	TIP33A	NPN-Si
MJ8101	MOTA	CTI	PNP-Si	MJE2490	MOTA	TIP34	PNP-Si
MJ8400	MOTA	CTI	NPN-Si	MJE2491	MOTA	TIP34A	NPN-Si
MJ9000	MOTA	CTI	NPN-Si	MJE2520	MOTA	TIP33	NPN-Si
MJE101	MOTA	TIP34	PNP-Si	MJE2521	MOTA	TIP33A	NPN-Si
MJE102	MOTA	TIP34A	PNP-Si	MJE2522	MOTA	TIP33	NPN-Si
MJE103	MOTA	TIP34A	PNP-Si	MJE2523	MOTA	TIP33A	NPN-Si
MJE104	MOTA	TIP34B	PNP-Si	MJE2801	MOTA	TIP41A	NPN-Si
MJE105	MOTA	TIP34A	PNP-Si	MJE2901	MOTA	TIP42A	PNP-Si
MJE201	MOTA	TIP33	NPN-Si	MJE2955	MOTA	TIP2955	PNP-Si
MJE202	MOTA	TIP33A	NPN-Si	MJE3050	MOTA	TIP33A	NPN-Si
MJE203	MOTA	TIP33A	NPN-Si	MJE3055	MOTA	TIP3055	NPN-Si
MJE204	MOTA	TIP33B	NPN-Si	MJE3370	MOTA	TIP32	PNP-Si
MJE205	MOTA	TIP33A	NPN-Si	MJE3371	MOTA	TIP32	PNP-Si
MJE340	MOTA	TIP48	NPN-Si	MJE3439	MOTA	TIP51	NPN-Si
MJE370	MOTA	TIP32	PNP-Si	MJE3440	MOTA	TIP52	NPN-Si
MJE371	MOTA	TIP32	PNP-Si	MJE3520	MOTA	TIP33	NPN-Si
MJE520	MOTA	TIP31	NPN-Si	MJE3521	MOTA	TIP33	NPN-Si
MJE521	MOTA	TIP31	NPN-Si	MJE3738	MOTA	TIP51	NPN-Si
MJE700	MOTA	TIP110	NPN-Si	MJE3739	MOTA	TIP52	NPN-Si
MJE701	MOTA	TIP115	PNP-Si	MJE3740	MOTA	TIP34A	PNP-Si
MJE702	MOTA	TIP116	PNP-Si	MJE3741	MOTA	TIP34B	PNP-Si
MJE703	MOTA	TIP116	PNP-Si	Q2001P	ECC	TIC215B	TRIAC
MJE800	MOTA	TIP110	NPN-Si	Q2001PS	ECC	TIC215B	TRIAC
MJE801	MOTA	TIP110	NPN-Si	Q2001PST	ECC	TIC215B	TRIAC
MJE802	MOTA	TIP111	NPN-Si	Q2001PT	ECC	TIC215B	TRIAC
MJE803	MOTA	TIP111	NPN-Si	Q2003P	ECC	TIC226B	TRIAC
MJE1090	MOTA	TIP125	PNP-Si	Q2003PT	ECC	TIC226B	TRIAC
MJE1091	MOTA	TIP125	PNP-Si	Q2004	ECC	TIC226B	TRIAC
MJE1092	MOTA	TIP126	PNP-Si	Q2004A	ECC	TIC226B	TRIAC
MJE1093	MOTA	TIP126	PNP-Si	Q2004B	ECC	TIC226B	TRIAC
MJE1100	MOTA	TIP120	NPN-Si	Q2004T	ECC	TIC226B	TRIAC

Refer to page 2-17 for key to manufacturers.

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CROSS-REFERENCE GUIDE

2

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
Q2004TA	ECC	TIC226B	TRIAC	Q5006A	ECC	TIC253E	TRIAC
Q2004TB	ECC	TIC226B	TRIAC	Q5006B	ECC	TIC253E	TRIAC
Q2006	ECC	TIC226B	TRIAC	Q5006TA	ECC	TIC253E	TRIAC
Q2006A	ECC	TIC226B	TRIAC	Q5006TB	ECC	TIC253E	TRIAC
Q2006B	ECC	TIC226B	TRIAC	Q5008	ECC	TIC253E	TRIAC
Q2006T	ECC	TIC226B	TRIAC	Q5008A	ECC	TIC253E	TRIAC
Q2006TA	ECC	TIC226B	TRIAC	Q5008B	ECC	TIC253E	TRIAC
Q2006TB	ECC	TIC226B	TRIAC	Q5008T	ECC	TIC253E	TRIAC
Q2008A	ECC	TIC236B	TRIAC	Q5008TA	ECC	TIC253E	TRIAC
Q2008B	ECC	TIC236B	TRIAC	Q5008TB	ECC	TIC253E	TRIAC
Q2008TA	ECC	TIC236B	TRIAC	Q6015	ECC	TIC253M	TRIAC
Q2008TB	ECC	TIC236B	TRIAC	Q6015A	ECC	TIC253M	TRIAC
Q2010	ECC	TIC246B	TRIAC	Q6015T	ECC	TIC253M	TRIAC
Q2010A	ECC	TIC246B	TRIAC	Q6015TA	ECC	TIC253M	TRIAC
Q2010B	ECC	TIC246B	TRIAC	Q6015TB	ECC	TIC253M	TRIAC
Q2010T	ECC	TIC236B	TRIAC	RTA0101	TEC	2N3005	SCR
Q2010TA	ECC	TIC236B	TRIAC	RTA0103	TEC	2N3005	SCR
Q2010TB	ECC	TIC246B	TRIAC	RTA0106	TEC	2N3006	SCR
Q2015	ECC	TIC253B	TRIAC	RTA0110	TEC	TIC39A	SCR
Q2015A	ECC	TIC253B	TRIAC	RTA0115	TEC	2N3008	SCR
Q2015B	ECC	TIC253B	TRIAC	RTA0120	TEC	2N3008	SCR
Q2015T	ECC	TIC253B	TRIAC	RTB0101	TEC	2N3005	SCR
Q2015TA	ECC	TIC253B	TRIAC	RTB0103	TEC	2N3005	SCR
Q2015TB	ECC	TIC253B	TRIAC	RTB0106	TEC	2N3006	SCR
Q2025	ECC	TIC253B	TRIAC	RTB0110	TEC	TIC39A	SCR
Q2025C	ECC	TIC253B	TRIAC	RTB0115	TEC	2N3008	SCR
Q2025D	ECC	TIC263B	TRIAC	RTB0120	TEC	2N3008	SCR
Q4004	ECC	TIC226D	TRIAC	RTB0125	TEC	2N1598	SCR
Q4004A	ECC	TIC226D	TRIAC	RTB0130	TEC	2N1598	SCR
Q4004B	ECC	TIC226D	TRIAC	RTB0201	TEC	2N3005	SCR
Q4004T	ECC	TIC226D	TRIAC	RTB0203	TEC	2N3005	SCR
Q4004TB	ECC	TIC226D	TRIAC	RTB0206	TEC	2N3006	SCR
Q4006A	ECC	TIC226D	TRIAC	RTB0210	TEC	TIC39A	SCR
Q4008A	ECC	TIC246D	TRIAC	RTB0215	TEC	2N3008	SCR
Q4008B	ECC	TIC246D	TRIAC	RTB0220	TEC	2N3008	SCR
Q4008TA	ECC	TIC246D	TRIAC	RTB0225	TEC	2N1598	SCR
Q4008TB	ECC	TIC246D	TRIAC	RTB0230	TEC	2N1598	SCR
Q4010	ECC	TIC246D	TRIAC	RTB0301	TEC	2N3005	SCR
Q4010A	ECC	TIC246D	TRIAC	RTB0303	TEC	2N3005	SCR
Q4010B	ECC	TIC246D	TRIAC	RTB0306	TEC	2N3006	SCR
Q4010T	ECC	TIC246D	TRIAC	RTB0310	TEC	TIC39A	SCR
Q4010TA	ECC	TIC246D	TRIAC	RTB0315	TEC	2N3008	SCR
Q4010TB	ECC	TIC246D	TRIAC	RTB0320	TEC	2N3008	SCR
Q4025	ECC	TIC263D	TRIAC	RTB0325	TEC	2N1598	SCR
Q4025C	ECC	TIC263D	TRIAC	RTB0330	TEC	2N1598	SCR
Q4025D	ECC	TIC263D	TRIAC	RTB0401	TEC	2N3001	SCR
Q5004	ECC	TIC216D	TRIAC	RTB0403	TEC	2N3001	SCR
Q5004A	ECC	TIC216D	TRIAC	RTB0406	TEC	2N3002	SCR
Q5004B	ECC	TIC216D	TRIAC	RTB0410	TEC	TIC39A	SCR

Refer to page 2-17 for key to manufacturers.

CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
RTB0415	TEC	2N3004	SCR	RTC0430	TEC	2N1598	SCR
RTB0420	TEC	2N3008	SCR	RTC0501	TEC	2N3001	SCR
RTB0425	TEC	2N1598	SCR	RTC0503	TEC	2N3001	SCR
RTB0430	TEC	2N1598	SCR	RTC0506	TEC	2N3002	SCR
RTB0501	TEC	2N3001	SCR	RTC0510	TEC	2N3003	SCR
RTB0503	TEC	2N3005	SCR	RTC0515	TEC	2N3004	SCR
RTB0506	TEC	2N3002	SCR	RTC0520	TEC	2N3004	SCR
RTB0510	TEC	TIC39A	SCR	RTC0525	TEC	2N1598	SCR
RTB0515	TEC	2N3004	SCR	RTC0530	TEC	2N1598	SCR
RTB0520	TEC	2N3004	SCR	RTC0601	TEC	2N3001	SCR
RTB0525	TEC	2N1598	SCR	RTC0603	TEC	2N3001	SCR
RTB0530	TEC	2N1598	SCR	RTC0606	TEC	2N3002	SCR
RTB0601	TEC	2N3001	SCR	RTC0610	TEC	2N3003	SCR
RTB0603	TEC	2N3001	SCR	RTC0615	TEC	2N3004	SCR
RTB0606	TEC	2N3002	SCR	RTC0620	TEC	2N3004	SCR
RTB0608	TEC	2N3002	SCR	RTD0101	TEC	TIC39Y	SCR
RTB0610	TEC	TIC39A	SCR	RTD0103	TEC	TIC39Y	SCR
RTB0615	TEC	2N3004	SCR	RTD0106	TEC	TIC39F	SCR
RTB0620	TEC	2N3004	SCR	RTD0110	TEC	TIC39A	SCR
RTC0101	TEC	2N3005	SCR	RTD0115	TEC	TIC39B	SCR
RTC0103	TEC	2N3005	SCR	RTD0120	TEC	2N1598	SCR
RTC0106	TEC	2N3006	SCR	RTD0125	TEC	2N1597	SCR
RTC0110	TEC	2N3007	SCR	RTD0130	TEC	2N1598	SCR
RTC0115	TEC	2N3004	SCR	RTD0135	TEC	2N1599	SCR
RTC0120	TEC	2N3004	SCR	RTD0140	TEC	TIC106D	SCR
RTC0125	TEC	2N1598	SCR	RTD0201	TEC	TIC39Y	SCR
RTC0130	TEC	2N1598	SCR	RTD0203	TEC	TIC39Y	SCR
RTC0201	TEC	2N3005	SCR	RTD0206	TEC	TIC39F	SCR
RTC0203	TEC	2N3005	SCR	RTD0210	TEC	TIC39A	SCR
RTC0206	TEC	2N3006	SCR	RTD0215	TEC	TIC39B	SCR
RTC0210	TEC	2N3009	SCR	RTD0220	TEC	TIC39B	SCR
RTC0215	TEC	2N3008	SCR	RTD0225	TEC	2N1598	SCR
RTC0220	TEC	TIC116B	SCR	RTD0230	TEC	2N1598	SCR
RTC0225	TEC	2N1598	SCR	RTD0235	TEC	2N1599	SCR
RTC0230	TEC	2N1598	SCR	RTD0240	TEC	TIC106D	SCR
RTC0301	TEC	2N3005	SCR	RTD0301	TEC	TIC39Y	SCR
RTC0303	TEC	2N3005	SCR	RTD0303	TEC	TIC39Y	SCR
RTC0306	TEC	2N3006	SCR	RTD0306	TEC	TIC39F	SCR
RTC0310	TEC	2N3007	SCR	RTD0310	TEC	TIC39A	SCR
RTC0315	TEC	2N3008	SCR	RTD0315	TEC	TIC39B	SCR
RTC0320	TEC	2N3008	SCR	RTD0320	TEC	TIC39B	SCR
RTC0325	TEC	2N1598	SCR	RTD0325	TEC	2N1598	SCR
RTC0330	TEC	2N1598	SCR	RTD0330	TEC	2N1598	SCR
RTC0401	TEC	2N3001	SCR	RTD0335	TEC	2N1599	SCR
RTC0403	TEC	2N3001	SCR	RTD0340	TEC	TIC106D	SCR
RTC0406	TEC	2N3002	SCR	RTD0401	TEC	TIC39Y	SCR
RTC0410	TEC	2N3003	SCR	RTD0403	TEC	TIC39Y	SCR
RTC0415	TEC	2N3008	SCR	RTD0406	TEC	TIC39F	SCR
RTC0420	TEC	2N3008	SCR	RTD0410	TEC	TIC39A	SCR
RTC0425	TEC	2N1598	SCR	RTD0415	TEC	TIC39B	SCR

Refer to page 2-17 for key to manufacturers.

CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
RTD0420	TEC	TIC39B	SCR	RTF0340	TEC	TIC39D	SCR
RTD0425	TEC	2N1598	SCR	RTF0401	TEC	TIC39Y	SCR
RTD0430	TEC	2N1598	SCR	RTF0403	TEC	TIC39Y	SCR
RTD0435	TEC	2N1599	SCR	RTF0406	TEC	TIC39A	SCR
RTD0440	TEC	TIC106D	SCR	RTF0410	TEC	TIC39A	SCR
RTD0501	TEC	TIC39Y	SCR	RTF0415	TEC	TIC39B	SCR
RTD0503	TEC	TIC39Y	SCR	RTF0420	TEC	TIC39B	SCR
RTD0506	TEC	TIC39F	SCR	RTF0425	TEC	TIC39C	SCR
RTD0510	TEC	TIC39A	SCR	RTF0430	TEC	TIC39C	SCR
RTD0515	TEC	TIC39B	SCR	RTF0435	TEC	TIC39D	SCR
RTD0520	TEC	TIC39B	SCR	RTF0440	TEC	TIC39D	SCR
RTD0525	TEC	2N1598	SCR	RTF0501	TEC	TIC39Y	SCR
RTD0530	TEC	2N1598	SCR	RTF0503	TEC	TIC39Y	SCR
RTD0535	TEC	2N1599	SCR	RTF0506	TEC	TIC39A	SCR
RTD0540	TEC	TIC106D	SCR	RTF0510	TEC	TIC39A	SCR
RTD0601	TEC	TIC39Y	SCR	RTF0515	TEC	TIC39B	SCR
RTD0603	TEC	TIC39Y	SCR	RTF0520	TEC	TIC39B	SCR
RTD0606	TEC	TIC39F	SCR	RTF0525	TEC	TIC39C	SCR
RTD0610	TEC	TIC39A	SCR	RTF0530	TEC	TIC39C	SCR
RTD0615	TEC	TIC39B	SCR	RTF0535	TEC	TIC39D	SCR
RTD0620	TEC	TIC39B	SCR	RTF0540	TEC	TIC39D	SCR
RTF0101	TEC	TIC39Y	SCR	RTF0601	TEC	TIC39Y	SCR
RTF0103	TEC	TIC39Y	SCR	RTF0603	TEC	TIC39Y	SCR
RTF0106	TEC	TIC39A	SCR	RTF0606	TEC	TIC39A	SCR
RTF0110	TEC	TIC39A	SCR	RTF0610	TEC	TIC39A	SCR
RTF0115	TEC	TIC39B	SCR	RTF0615	TEC	TIC39B	SCR
RTF0120	TEC	TIC39B	SCR	RTF0620	TEC	TIC39B	SCR
RTF0125	TEC	TIC39C	SCR	RTN0102	TEC	TIC116F	SCR
RTF0130	TEC	TIC39C	SCR	RTN0105	TEC	TIC116F	SCR
RTF0135	TEC	TIC39D	SCR	RTN0110	TEC	TIC116A	SCR
RTF0140	TEC	TIC39D	SCR	RTN0120	TEC	TIC116B	SCR
RTF0201	TEC	TIC39Y	SCR	RTN0130	TEC	TIC116C	SCR
RTF0203	TEC	TIC39Y	SCR	RTN0140	TEC	TIC116D	SCR
RTF0206	TEC	TIC39A	SCR	RTN0150	TEC	TIC116E	SCR
RTF0210	TEC	TIC39A	SCR	RTN0160	TEC	TIC116M	SCR
RTF0215	TEC	TIC39B	SCR	RTN0202	TEC	TIC126F	SCR
RTF0220	TEC	TIC39B	SCR	RTN0205	TEC	TIC126F	SCR
RTF0225	TEC	TIC39C	SCR	RTN0210	TEC	TIC126A	SCR
RTF0230	TEC	TIC39C	SCR	RTN0220	TEC	TIC126B	SCR
RTF0235	TEC	TIC39D	SCR	RTN0230	TEC	TIC126C	SCR
RTF0240	TEC	TIC39D	SCR	RTN0240	TEC	TIC126D	SCR
RTF0301	TEC	TIC39Y	SCR	RTN0250	TEC	TIC126E	SCR
RTF0303	TEC	TIC39Y	SCR	RTN0260	TEC	TIC126M	SCR
RTF0306	TEC	TIC39A	SCR	RTN0302	TEC	TIC126F	SCR
RTF0310	TEC	TIC39A	SCR	RTN0305	TEC	TIC126F	SCR
RTF0315	TEC	TIC39B	SCR	RTN0310	TEC	TIC126A	SCR
RTF0320	TEC	TIC39B	SCR	RTN0320	TEC	TIC126B	SCR
RTF0325	TEC	TIC39C	SCR	RTN0330	TEC	TIC126C	SCR
RTF0330	TEC	TIC39C	SCR	RTN0340	TEC	TIC126D	SCR
RTF0335	TEC	TIC39D	SCR	RTN0350	TEC	TIC126E	SCR

Refer to page 2-17 for key to manufacturers.

CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
RTN0360	TEC	TIC126M	SCR	RTR0405	TEC	TIC106F	SCR
RTN0402	TEC	TIC126F	SCR	RTR0410	TEC	TIC106A	SCR
RTN0405	TEC	TIC126F	SCR	RTR0420	TEC	TIC106B	SCR
RTN0410	TEC	TIC126A	SCR	RTR0430	TEC	TIC106C	SCR
RTN0420	TEC	TIC126B	SCR	RTR0440	TEC	TIC106D	SCR
RTN0430	TEC	TIC126C	SCR	RTR0450	TEC	CTI	SCR
RTN0440	TEC	TIC126D	SCR	RTR0460	TEC	CTI	SCR
RTN0450	TEC	TIC126E	SCR	RTR0502	TEC	TIC106F	SCR
RTN0460	TEC	TIC126M	SCR	RTR0505	TEC	TIC106F	SCR
RTN0502	TEC	TIC126F	SCR	RTR0510	TEC	TIC106A	SCR
RTN0505	TEC	TIC126F	SCR	RTR0520	TEC	TIC106B	SCR
RTN0510	TEC	TIC126A	SCR	RTR0530	TEC	TIC106C	SCR
RTN0520	TEC	TIC126B	SCR	RTR0540	TEC	TIC106D	SCR
RTN0530	TEC	TIC126C	SCR	RTR0550	TEC	CTI	SCR
RTN0540	TEC	TIC126D	SCR	RTR0560	TEC	CTI	SCR
RTN0550	TEC	TIC126E	SCR	RTS0102	TEC	TIC106F	SCR
RTN0560	TEC	TIC126M	SCR	RTS0105	TEC	TIC106F	SCR
RTN0602	TEC	TIC126F	SCR	RTS0110	TEC	TIC106A	SCR
RTN0605	TEC	TIC126F	SCR	RTS0120	TEC	TIC106B	SCR
RTN0610	TEC	TIC126A	SCR	RTS0130	TEC	TIC106C	SCR
RTN0620	TEC	TIC126B	SCR	RTS0140	TEC	TIC106D	SCR
RTN0630	TEC	TIC126C	SCR	RTS0150	TEC	CTI	SCR
RTN0640	TEC	TIC126D	SCR	RTS0160	TEC	CTI	SCR
RTN0650	TEC	TIC126E	SCR	RTS0202	TEC	TIC106F	SCR
RTN0660	TEC	TIC126M	SCR	RTS0205	TEC	TIC106F	SCR
RTR0102	TEC	TIC106F	SCR	RTS0210	TEC	TIC106A	SCR
RTR0105	TEC	TIC106F	SCR	RTS0220	TEC	TIC106B	SCR
RTR0110	TEC	TIC106A	SCR	RTS0230	TEC	TIC106C	SCR
RTR0120	TEC	TIC106B	SCR	RTS0240	TEC	TIC106D	SCR
RTR0130	TEC	TIC106C	SCR	RTS0250	TEC	CTI	SCR
RTR0140	TEC	TIC106D	SCR	RTS0260	TEC	CTI	SCR
RTR0150	TEC	CTI	SCR	RTS0302	TEC	TIC106F	SCR
RTR0160	TEC	CTI	SCR	RTS0305	TEC	TIC106F	SCR
RTR0202	TEC	TIC106F	SCR	RTS0310	TEC	TIC106A	SCR
RTR0205	TEC	TIC106F	SCR	RTS0320	TEC	TIC106B	SCR
RTR0210	TEC	TIC106A	SCR	RTS0330	TEC	TIC106C	SCR
RTR0220	TEC	TIC106B	SCR	RTS0340	TEC	TIC106D	SCR
RTR0230	TEC	TIC106C	SCR	RTS0350	TEC	CTI	SCR
RTR0240	TEC	TIC106D	SCR	RTS0360	TEC	CTI	SCR
RTR0250	TEC	CTI	SCR	RTS0402	TEC	TIC106F	SCR
RTR0260	TEC	CTI	SCR	RTS0405	TEC	TIC106F	SCR
RTR0302	TEC	TIC106F	SCR	RTS0410	TEC	TIC106A	SCR
RTR0305	TEC	TIC106F	SCR	RTS0420	TEC	TIC106B	SCR
RTR0310	TEC	TIC106A	SCR	RTS0430	TEC	TIC106C	SCR
RTR0320	TEC	TIC106B	SCR	RTS0440	TEC	TIC106D	SCR
RTR0330	TEC	TIC106C	SCR	RTS0450	TEC	CTI	SCR
RTR0340	TEC	TIC106D	SCR	RTS0460	TEC	CTI	SCR
RTR0350	TEC	CTI	SCR	RTT0102	TEC	TIC116F	SCR
RTR0360	TEC	CTI	SCR	RTT0105	TEC	TIC116F	SCR
RTR0402	TEC	TIC106F	SCR	RTT0110	TEC	TIC116A	SCR

Refer to page 2-17 for key to manufacturers.

CTI—Contact Texas Instruments.

CROSS-REFERENCE GUIDE

2

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
RTT0120	TEC	TIC116B	SCR	RTU0140	TEC	TIC126D	SCR
RTT0130	TEC	TIC116C	SCR	RTU0150	TEC	TIC126E	SCR
RTT0140	TEC	TIC116D	SCR	RTU0160	TEC	TIC126M	SCR
RTT0150	TEC	TIC116E	SCR	RTU0202	TEC	TIC126F	SCR
RTT0160	TEC	TIC116M	SCR	RTU0205	TEC	TIC126F	SCR
RTT0202	TEC	TIC116F	SCR	RTU0210	TEC	TIC126A	SCR
RTT0205	TEC	TIC116F	SCR	RTU0220	TEC	TIC126B	SCR
RTT0210	TEC	TIC116A	SCR	RTU0230	TEC	TIC126C	SCR
RTT0220	TEC	TIC116B	SCR	RTU0240	TEC	TIC126D	SCR
RTT0230	TEC	TIC116C	SCR	RTU0250	TEC	TIC126E	SCR
RTT0240	TEC	TIC116D	SCR	RTU0260	TEC	TIC126M	SCR
RTT0250	TEC	TIC116E	SCR	RTU0302	TEC	TIC126F	SCR
RTT0260	TEC	TIC116M	SCR	RTU0305	TEC	TIC126F	SCR
RTT0302	TEC	TIC116F	SCR	RTU0310	TEC	TIC126A	SCR
RTT0305	TEC	TIC116F	SCR	RTU0320	TEC	TIC126B	SCR
RTT0310	TEC	TIC116A	SCR	RTU0330	TEC	TIC126C	SCR
RTT0320	TEC	TIC116B	SCR	RTU0340	TEC	TIC126D	SCR
RTT0330	TEC	TIC116C	SCR	RTU0350	TEC	TIC126E	SCR
RTT0340	TEC	TIC116D	SCR	RTU0360	TEC	TIC126M	SCR
RTT0350	TEC	TIC116E	SCR	RTU0402	TEC	TIC126F	SCR
RTT0360	TEC	TIC116M	SCR	RTU0405	TEC	TIC126F	SCR
RTT0402	TEC	TIC116F	SCR	RTU0410	TEC	TIC126A	SCR
RTT0405	TEC	TIC116F	SCR	RTU0420	TEC	TIC126B	SCR
RTT0410	TEC	TIC116A	SCR	RTU0430	TEC	TIC126C	SCR
RTT0420	TEC	TIC116B	SCR	RTU0440	TEC	TIC126D	SCR
RTT0430	TEC	TIC116C	SCR	RTU0450	TEC	TIC126E	SCR
RTT0440	TEC	TIC116D	SCR	RTU0460	TEC	TIC126M	SCR
RTT0450	TEC	TIC116E	SCR	RTU0502	TEC	TIC126F	SCR
RTT0460	TEC	TIC116M	SCR	RTU0505	TEC	TIC126F	SCR
RTT0502	TEC	TIC116F	SCR	RTU0510	TEC	TIC126A	SCR
RTT0505	TEC	TIC116F	SCR	RTU0520	TEC	TIC126B	SCR
RTT0510	TEC	TIC116A	SCR	RTU0530	TEC	TIC126C	SCR
RTT0520	TEC	TIC116B	SCR	RTU0540	TEC	TIC126D	SCR
RTT0530	TEC	TIC116C	SCR	RTU0550	TEC	TIC126E	SCR
RTT0540	TEC	TIC116D	SCR	RTU0560	TEC	TIC126M	SCR
RTT0550	TEC	TIC116E	SCR	RTU0602	TEC	TIC126F	SCR
RTT0560	TEC	TIC116M	SCR	RTU0605	TEC	TIC126F	SCR
RTT0602	TEC	TIC116F	SCR	RTU0610	TEC	TIC126A	SCR
RTT0605	TEC	TIC116F	SCR	RTU0620	TEC	TIC126B	SCR
RTT0610	TEC	TIC116A	SCR	RTU0630	TEC	TIC126C	SCR
RTT0620	TEC	TIC116B	SCR	RTU0640	TEC	TIC126D	SCR
RTT0630	TEC	TIC116C	SCR	RTU0650	TEC	TIC126E	SCR
RTT0640	TEC	TIC116D	SCR	RTU0660	TEC	TIC126M	SCR
RTT0650	TEC	TIC116E	SCR	SC60B	GE	TIC263B	TRIAC
RTT0660	TEC	TIC116M	SCR	SC60D	GE	TIC263D	TRIAC
RTU0102	TEC	TIC126F	SCR	SC60E	GE	TIC263E	TRIAC
RTU0105	TEC	TIC126F	SCR	SC61B	GE	TIC263B	TRIAC
RTU0110	TEC	TIC126A	SCR	SC61D	GE	TIC263D	TRIAC
RTU0120	TEC	TIC126B	SCR	SC61E	GE	TIC263E	TRIAC
RTU0130	TEC	TIC126C	SCR	SC141B	GE	TIC226B	TRIAC

Refer to page 2-17 for key to manufacturers.

CROSS-REFERENCE GUIDE

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
SC141D	GE	TIC226D	TRIAC	SDT3510	SOD	TIP32A	PNP-Si
SC141E	GE	TIC226D	TRIAC	SDT3511	SOD	TIP32B	PNP-Si
SC146B	GE	TIC226B	TRIAC	SDT3512	SOD	TIP32C	PNP-Si
SC146D	GE	TIC226D	TRIAC	SDT3513	SOD	TIP32	PNP-Si
SC146E	GE	TIC226D	TRIAC	SDT3514	SOD	TIP32A	PNP-Si
SC240B	GE	TIC226B	TRIAC	SDT3515	SOD	TIP32B	PNP-Si
SC240D	GE	TIC226D	TRIAC	SDT3516	SOD	TIP32C	PNP-Si
SC240E	GE	TIC226D	TRIAC	SDT3575	SOD	TIP30	PNP-Si
SC241B	GE	TIC226B	TRIAC	SDT3576	SOD	TIP30A	PNP-Si
SC241D	GE	TIC226D	TRIAC	SDT3577	SOD	TIP30B	PNP-Si
SC241E	GE	TIC226D	TRIAC	SDT3578	SOD	TIP30	PNP-Si
SC245B	GE	TIC226B	TRIAC	SDT3579	SOD	TIP30A	PNP-Si
SC245D	GE	TIC226D	TRIAC	SDT3701	SOD	TIP42	PNP-Si
SC245E	GE	TIC226D	TRIAC	SDT3702	SOD	TIP42A	PNP-Si
SC246B	GE	TIC226B	TRIAC	SDT3703	SOD	TIP42	PNP-Si
SC246D	GE	TIC226D	TRIAC	SDT3704	SOD	TIP42A	PNP-Si
SC246E	GE	TIC226D	TRIAC	SDT3705	SOD	TIP42B	PNP-Si
SC250B	GE	TIC236B	TRIAC	SDT3706	SOD	TIP42	PNP-Si
SC250D	GE	TIC236D	TRIAC	SDT3707	SOD	TIP42	PNP-Si
SC250E	GE	TIC236D	TRIAC	SDT3708	SOD	TIP42A	PNP-Si
SC251B	GE	TIC236B	TRIAC	SDT3709	SOD	TIP42	PNP-Si
SC251D	GE	TIC236D	TRIAC	SDT3710	SOD	TIP42	PNP-Si
SC251E	GE	TIC236D	TRIAC	SDT3711	SOD	TIP42A	PNP-Si
SCC321	FSC	TIP35A	NPN-Si	SDT3712	SOD	TIP42	PNP-Si
SCC421	FSC	TIP36A	PNP-Si	SDT3713	SOD	TIP42A	PNP-Si
SCD321	FSC	TIP33B	NPN-Si	SDT3714	SOD	TIP42A	PNP-Si
SCD421	FSC	TIP36B	PNP-Si	SDT3715	SOD	TIP42	PNP-Si
SCE321	FSC	TIP33C	NPN-Si	SDT3716	SOD	TIP42	PNP-Si
SCE421	FSC	TIP36C	PNP-Si	SDT3717	SOD	TIP42A	PNP-Si
SDI345	FSC	TIP41	NPN-Si	SDT3718	SOD	TIP42B	PNP-Si
SDI445	FSC	TIP42	PNP-Si	SDT3719	SOD	TIP42C	PNP-Si
SDJ345	FSC	TIP41	NPN-Si	SDT3720	SOD	TIP42	PNP-Si
SDJ445	FSC	TIP42	PNP-Si	SDT3721	SOD	TIP42	PNP-Si
SDK345	FSC	TIP41	NPN-Si	SDT3722	SOD	TIP42A	PNP-Si
SDK445	FSC	TIP42	PNP-Si	SDT3723	SOD	TIP42B	PNP-Si
SDL345	FSC	TIP41A	NPN-Si	SDT3724	SOD	TIP42C	PNP-Si
SDL445	FSC	TIP42A	PNP-Si	SDT3725	SOD	TIP42	PNP-Si
SDM345	FSC	TIP41	NPN-Si	SDT3726	SOD	TIP42	PNP-Si
SDM445	FSC	TIP42	PNP-Si	SDT3727	SOD	TIP42A	PNP-Si
SDN345	FSC	TIP41A	NPN-Si	SDT3728	SOD	TIP42B	PNP-Si
SDN445	FSC	TIP42A	PNP-Si	SDT3729	SOD	TIP42	PNP-Si
SDO345	FSC	TIP41B	NPN-Si	SDT3730	SOD	TIP42A	PNP-Si
SDO445	FSC	TIP42B	PNP-Si	SDT3731	SOD	TIP42A	PNP-Si
SDP345	FSC	TIP41C	NPN-Si	SDT3732	SOD	TIP42C	PNP-Si
SDP445	FSC	TIP42C	PNP-Si	SDT3733	SOD	TIP42	PNP-Si
SDT402	SOD	TIP54	NPN-Si	SDT3750	SOD	TIP34	PNP-Si
SDT410	SOD	TIP51	NPN-Si	SDT3751	SOD	TIP34A	PNP-Si
SDT411	SOD	TIP52	NPN-Si	SDT3752	SOD	TIP34	PNP-Si
SDT423	SOD	TIP54	NPN-Si	SDT3753	SOD	TIP34A	PNP-Si
SDT3509	SOD	TIP32	PNP-Si	SDT3754	SOD	TIP34B	PNP-Si

Refer to page 2-17 for key to manufacturers.

CROSS-REFERENCE GUIDE

2

TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS	TYPE	MANUFACTURER	FOR NEW DESIGN	CLASS
SDT3755	SOD	TIP34C	PNP-Si	SDT7602	SOD	TIP33A	NPN-Si
SDT3756	SOD	TIP34	PNP-Si	SDT7603	SOD	TIP33B	NPN-Si
SDT3757	SOD	TIP34	PNP-Si	SDT7607	SOD	TIP33	NPN-Si
SDT3758	SOD	TIP34A	PNP-Si	SDT7608	SOD	TIP33A	NPN-Si
SDT3759	SOD	TIP34B	PNP-Si	SDT7609	SOD	TIP33B	NPN-Si
SDT3760	SOD	TIP34C	PNP-Si	SDT7731	SOD	2N5301	NPN-Si
SDT3761	SOD	TIP34	PNP-Si	SDT7732	SOD	2N5301	NPN-Si
SDT3762	SOD	TIP34	PNP-Si	SDT7733	SOD	2N5301	NPN-Si
SDT3763	SOD	TIP34A	PNP-Si	SDT7734	SOD	2N5301	NPN-Si
SDT3764	SOD	TIP34B	PNP-Si	SDT9201	SOD	TIP35	NPN-Si
SDT3765	SOD	TIP34C	PNP-Si	SDT9202	SOD	TIP35B	NPN-Si
SDT3766	SOD	TIP34	PNP-Si	SDT9203	SOD	TIP35C	NPN-Si
SDT3825	SOD	TIP34	PNP-Si	SDT9204	SOD	2N5301	NPN-Si
SDT3826	SOD	TIP34B	PNP-Si	SDT9205	SOD	TIP35	NPN-Si
SDT3827	SOD	TIP34	PNP-Si	SDT9206	SOD	TIP35A	NPN-Si
SDT3875	SOD	TIP36	PNP-Si	SDT9207	SOD	TIP35B	NPN-Si
SDT3876	SOD	TIP36A	PNP-Si	SDT9208	SOD	TIP35C	NPN-Si
SDT3877	SOD	TIP36	PNP-Si	SDT9209	SOD	2N5301	NPN-Si
SDT5901	SOD	TIP41	NPN-Si	SDT9210	SOD	TIP35	NPN-Si
SDT5902	SOD	TIP41A	NPN-Si	SDT9801	SOD	TIP35	NPN-Si
SDT5903	SOD	TIP41B	NPN-Si	SDT9802	SOD	TIP35A	NPN-Si
SDT5904	SOD	TIP41C	NPN-Si	SDT9803	SOD	TIP35B	NPN-Si
SDT7601	SOD	TIP33	NPN-Si	SDT9804	SOD	TIP35C	NPN-Si

Refer to page 2-17 for key to manufacturers.

Product Selection Guides

PRODUCT SELECTION GUIDE

HIGH-RELIABILITY SILICON POWER TRANSISTORS

DEVICE TYPE	POLARITY	I _C		V _{CEO}		h _{FE} @ I _C V _{CE}				V _{CE(sat)}		P _T		PACKAGE
		CONTINUOUS	A	V	MIN	MAX	A	V	V	A	T _C = 25°C	T _C = 100°C		
2N497	NPN	0.5		60	12	36	0.2	10	5	0.2		4	2.3	I(TO-5)
2N497A	NPN	0.5		60	12	36	0.2	10	5	0.2		5	2.8	I(TO-5)
2N656	NPN	0.5		60	30	90	0.2	10	5	0.2		4	2.3	I(TO-5)
2N656A	NPN	0.5		60	30	90	0.2	10	5	0.2		5	2.8	I(TO-5)
2N498	NPN	0.5		100	12	36	0.2	10	5	0.2		4	2.3	I(TO-5)
2N498A	NPN	0.5		100	12	36	0.2	10	5	0.2		5	2.8	I(TO-5)
2N657	NPN	0.5		100	30	90	0.2	10	5	0.2		4	2.3	I(TO-5)
2N657A	NPN	0.5		100	30	90	0.2	10	5	0.2		5	2.8	I(TO-5)
2N1714	NPN	1		60	20	60	0.2	5	2	0.2			15	I(TO-5)
2N1716	NPN	1		60	40	120	0.2	5	2	0.2			15	I(TO-5)
2N2987	NPN	1		80	25	75	0.2	5	0.8	0.2			15	I(TO-5)
2N2989	NPN	1		80	60	120	0.2	5	0.8	0.2			15	I(TO-5)
2N4000	NPN	1		80	30	120	0.5	2	0.3	0.5			15	I(TO-5)
2N1715	NPN	1		100	20	60	0.2	5	2	0.2			15	I(TO-5)
2N1717	NPN	1		100	40	120	0.2	5	2	0.2			15	I(TO-5)
2N2988	NPN	1		100	25	75	0.2	5	0.8	0.2			15	I(TO-5)
2N2990	NPN	1		100	60	120	0.2	5	0.8	0.2			15	I(TO-5)
2N4001	NPN	1		100	30	120	0.5	2	0.3	0.5			15	I(TO-5)
2N3583	NPN	1		175	40	200	0.5	10	0.5	1	35	20	5B(TO-66)	
T1486	NPN	1.5		60	20	80	0.2	5	2	0.2			15	I(TO-5)
T1487	NPN	1.5		60	20	80	0.2	5	2	0.2			15	S
TIP541†	NPN	2		45	40	200	1	4	0.3	1			4	PPP(TO-39)
2N5333	PNP	2		80	30	120	1	4	0.45	1			15	I(TO-5)
2N1047	NPN	2		80	12	36	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N1047A	NPN	2		80	12	36	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N1049	NPN	2		80	30	90	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N1049A	NPN	2		80	30	90	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N1049B	NPN	2		80	30	90	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N2150	NPN	2		80	20	60	1	5	1	1			30	DD(TO-111)
2N2151	NPN	2		80	40	120	1	5	1	1			30	DD(TO-111)
2N4300	NPN	2		80	30	120	1	2	0.3	1			15	I(TO-5)
2N4998	NPN	2		80	30	90	1	5	0.85	2	35	20	YYYY(TO-59)	
2N5000	NPN	2		80	70	200	1	5	0.85	2	35	20	YYYY(TO-59)	
2N5148	NPN	2		80	30	90	1	5	0.85	2	7	4	PPP(TO-39)	
2N5150	NPN	2		80	70	200	1	5	0.85	2	7	4	PPP(TO-39)	
2N4999	PNP	2		80	30	90	1	5	0.85	2	35	20	YYYY(TO-59)	
2N5001	PNP	2		80	70	200	1	5	0.85	2	35	20	YYYY(TO-59)	
2N5147	PNP	2		80	30	90	1	5	0.85	2	7	4	PPP(TO-39)	
2N5149	PNP	2		80	70	200	1	5	0.85	2	7	4	PPP(TO-39)	
2N5152	NPN	2		80	30	90	2.5	5	0.75	2.5	11.7	6.7	PPP(TO-39)	
2N5154	NPN	2		80	70	200	2.5	5	0.75	2.5	11.7	6.7	PPP(TO-39)	
2N1048	NPN	2		120	12	36	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N1048A	NPN	2		120	12	36	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N1048B	NPN	2		120	12	36	0.5	10	7.5	0.5	40	23	F(TO-57)	
2N1050	NPN	2		120	30	90	0.5	10	7.5	0.5	40	23	F(TO-57)	

† Radiation tolerant

PRODUCT SELECTION GUIDE

HIGH-RELIABILITY SILICON POWER TRANSISTORS

DEVICE TYPE	POLARITY	I _C	V _{CEO}	h _{FE}		@ I _C		V _{CE(sat)}		P _T T _C = 25°C	P _T T _C = 100°C	PACKAGE
		CONTINUOUS		MIN	MAX	A	V	MAX @ I _C	A			
TIP503	NPN	2	120	40	200	1	4	0.6	1		20	5B(TO-66)
TIP505	NPN	2	120	40	200	1	4	0.6	1		20	YYYY(TO-59)
TIP504	NPN	2	150	40	200	1	4	0.6	1		20	5B(TO-66)
TIP506	NPN	2	150	40	200	1	4	0.6	1		20	YYYY(TO-59)
TIP507	PNP	2	150	30	120	1	4	1.5	2		20	YYYY(TO-59)
TIP508	PNP	2	150	30	120	1	4	1.5	2		4	PPP(TO-39)
TIP521	PNP	2	200	20	100	1	4	2.5	2		20	YYYY(TO-59)
TIP522	PNP	2	200	20	100	1	4	2.5	2		4	PPP(TO-39)
2N3584	NPN	2	250	8	80	1	2	0.75	1	35	20	5B(TO-66)
2N3585	NPN	2	300	8	80	1	2	0.75	1	35	20	5B(TO-66)
2N4240	NPN	2	300	10	100	0.75	2	1	0.75	35	20	5B(TO-66)
2N3902	NPN	2.5	400	30	90	1	5	0.8	1	100§	67	K(TO-3)
2N3021	PNP	3	30	20	60	1	2	1.5	3	25	12.5	K(TO-3)
2N3024	PNP	3	30	50	180	1	2	1	3	25	12.5	K(TO-3)
TIP501	NPN	3	40	25	180	1	1.5	0.75	1	6	3.4	PPP(TO-39)
2N3719	PNP	3	40	25	180	1	1.5	0.75	1	6	3.4	I(TO-5)
2N3022	PNP	3	45	20	60	1	2	1.5	3	25	12.5	K(TO-3)
2N3025	PNP	3	45	50	180	1	2	1	3	25	12.5	K(TO-3)
TIP502	NPN	3	60	25	180	1	1.5	0.75	1	6	3.4	PPP(TO-39)
2N3720	PNP	3	60	25	180	1	1.5	0.75	1	6	3.4	I(TO-5)
2N3023	PNP	3	60	20	60	1	2	1.5	3	25	12.5	K(TO-3)
2N3026	PNP	3	60	50	180	1	2	1	3	25	12.5	K(TO-3)
2N3418	NPN	3	60	10	60	1	2	0.25	1		15	I(TO-5)
2N3420	NPN	3	60	15	120	1	2	0.25	1		15	I(TO-5)
2N389	NPN	3	60‡	12	60	1	15	5	1		85	D(TO-53)
2N389A	NPN	3	60‡	12	60	1	15	5	1		85	D(TO-53)
2N3419	NPN	3	80	10	60	1	2	0.25	1		15	I(TO-5)
2N3421	NPN	3	80	15	120	1	2	0.25	1		15	I(TO-5)
2N424	NPN	3	80‡	12	60	1	15	5	1		85	D(TO-53)
2N424A	NPN	3	80‡	12	60	1	15	5	1		85	D(TO-53)
TIP529	NPN	3	300	25	125	1.5	4	2.5	3		67	N(TO-61)
TIP530	NPN	3	300	25	125	1.5	4	2.5	3		20	5B(TO-66)
2N5157	NPN	3.5	500	30	90	1	5	0.8	1	100§	67	K(TO-3)
2N5938	NPN	4	50	30	150	1	3	0.75	3		20	ZZZZ
TIP509	NPN	4	120	40	200	2	4	0.6	2		30	K(TO-3)
TIP511	NPN	4	120	40	200	2	4	0.6	2		30	N(TO-61)
TIP510	NPN	4	150	40	200	2	4	0.6	2		30	K(TO-3)
TIP512	NPN	4	150	40	200	2	4	0.6	2		30	N(TO-61)
2N4913	NPN	5	40	25	100	2.5	2	0.75	2.5	87	50	K(TO-3)
2N4914	NPN	5	60	25	100	2.5	2	0.75	2.5	87	50	K(TO-3)
2N2880	NPN	5	70	40	120	1	2	0.25	1		30	DD(TO-111)
2N5385	PNP	5	80	20	80	2	4	0.6	2		30	DD(TO-111)
2N1722	NPN	5	80	20	90	2	15	1	2		50	D(TO-53)
2N1723	NPN	5	80	50	150	2	15	1	2		50	D(TO-53)
2N1724	NPN	5	80	20	90	2	15	1	2		50	N(TO-61)
2N1725	NPN	5	80	50	150	2	15	1	2		50	N(TO-61)

‡V_{CE}R
§T_C = 75°C

PRODUCT SELECTION GUIDE

HIGH-RELIABILITY SILICON POWER TRANSISTORS

DEVICE TYPE	POLARITY	I _C	V _{CEO}	h _{FE} @ I _C		V _{CE}		V _{CE(sat)}		P _T	P _T	PACKAGE	
		CONTINUOUS	V	MIN	MAX	A	V	MAX @ I _C	A	T _C = 25°C	T _C = 100°C		
		A	V			A	V	V	A	W	W		
2N3996	NPN	5	80	40	120	1	2	0.25	1		30	BB(TO-111)	
2N3997	NPN	5	80	80	240	1	2	0.25	1		30	BB(TO-111)	
2N3998	NPN	5	80	40	120	1	2	0.25	1		30	DD(TO-111)	
2N3999	NPN	5	80	80	240	1	2	0.25	1		30	DD(TO-111)	
2N4915	NPN	5	80	25	100	2.5	2	0.75	2.5	87	50	K(TO-3)	
2N5384	PNP	5	80	20	80	2	4	0.6	2		30	BB(TO-111)	
2N5002	NPN	5	80	30	90	2.5	5	0.75	2.5	58	33.3	YYYY(TO-59)	
2N5004	NPN	5	80	70	200	2.5	5	0.75	2.5	58	33.3	YYYY(TO-59)	
2N5003	PNP	5	80	30	90	2.5	5	0.75	2.5	58	33.3	YYYY(TO-59)	
2N5005	PNP	5	80	70	200	2.5	5	0.75	2.5	58	33.3	YYYY(TO-59)	
2N5151	PNP	5	80	30	90	2.5	5	0.75	2.5	11.7	6.7	PPP(TO-39)	
2N5153	PNP	5	80	70	200	2.5	5	0.75	2.5	11.7	6.7	PPP(TO-39)	
2N1722A	NPN	5	120	30	90	2	15	0.6	2		50	D(TO-53)	
2N1724A	NPN	5	120	30	90	2	15	0.6	2		50	N(TO-61)	
TIP513	PNP	5	150	30	150	2.5	4	1	2.5		30	YYYY(TO-59)	
TIP514	PNP	5	150	30	150	2.5	4	1	2.5		20	5B(TO-66)	
TIP523	PNP	5	200	20	100	2.5	4	1.5	2.5		30	YYYY(TO-59)	
TIP524	PNP	5	200	20	100	2.5	4	1.5	2.5		6	PPP(TO-39)	
TIP525	NPN	5	200	30	150	2.5	4	1.2	2.5		60	K(TO-3)	
TIP526	NPN	5	200	30	150	2.5	4	1.2	2.5		60	N(TO-61)	
TIP544	PNP	6	100	25	100	3	2	1	3	150	85	K(TO-3)	
2N5758	NPN	6	100	25	100	3	2	1	3	150	85	K(TO-3)	
TIP545	PNP	6	120	20	80	3	2	1	3	150	85	K(TO-3)	
2N5759	NPN	6	120	20	80	3	2	1	3	150	85	K(TO-3)	
TIP546	PNP	6	140	15	60	3	2	1	3	150	85	K(TO-3)	
2N5760	NPN	6	140	15	60	3	2	1	3	150	85	K(TO-3)	
T11135	NPN	7.5	50	30	120	2	4	1	2	80#	50	N(TO-61)	
T11136	NPN	7.5	50	15	60	2	4	1	2	80#	50	N(TO-61)	
T11155	NPN	7.5	50	20	80	5	4	2.5	5	80#	50	N(TO-61)	
T11156	NPN	7.5	50	10	40	5	4	2.5	5	80#	50	N(TO-61)	
T11133	NPN	7.5	75	30	120	2	4	1	2	80#	50	N(TO-61)	
T11134	NPN	7.5	75	15	60	2	4	1	2	80#	50	N(TO-61)	
T11153	NPN	7.5	75	20	80	5	4	2.5	5	80#	50	N(TO-61)	
T11154	NPN	7.5	75	10	40	5	4	2.5	5	80#	50	N(TO-61)	
T11131	NPN	7.5	100	30	120	2	4	1	2	80#	50	N(TO-61)	
T11132	NPN	7.5	100	15	60	2	4	1	2	80#	50	N(TO-61)	
T11151	NPN	7.5	100	20	80	5	4	2.5	5	80#	50	N(TO-61)	
T11152	NPN	7.5	100	10	40	5	4	2.5	5	80#	50	N(TO-61)	
2N5387	NPN	7.5	200	25	100	2	5	2	5		100	N(TO-61)	
TIP535	NPN	7.5	200	20	100	5	4	1.2	5		100	K(TO-3)	
2N5388	NPN	7.5	250	25	100	2	5	2	5		100	N(TO-61)	
TIP536	NPN	7.5	300	20	100	5	4	1.2	5		100	K(TO-3)	
2N5389	NPN	7.5	300	25	100	2	5	2	5		100	N(TO-61)	
TIP537	NPN	7.5	400	20	100	5	4	1.2	5		100	K(TO-3)	
TIP519	PNP	8	150	30	150	4	4	1	4		50	K(TO-3)	
TIP520	PNP	8	150	30	150	4	4	1	4		50	N(TO-61)	
TIP527	PNP	8	200	20	100	4	4	1.5	4		60	K(TO-3)	

3

#T_C = 55°C

PRODUCT SELECTION GUIDE

HIGH-RELIABILITY SILICON POWER TRANSISTORS

DEVICE TYPE	POLARITY	I _C		V _{CEO}		h _{FE} @ I _C		V _{CE(sat)}		P _T		PACKAGE
		CONTINUOUS						MAX @ I _C		T _C = 25°C	T _C = 100°C	
		A	V	MIN	MAX	A	V	V	A	W	W	
TIP528	PNP	8	200	20	100	4	4	1.5	4		60	N(TO-61)
TIP542†	NPN	10	45	40	200	5	4	0.8	10		40	YYYY(TO-59)
2N3789	PNP	10	60	25	90	1	2	1	4	150	85	K(TO-3)
2N3713	NPN	10	60	25	75	1	2	1	5	150	85	K(TO-3)
2N3715	NPN	10	60	50	150	1	2	1	5	150	85	K(TO-3)
2N3791	PNP	10	60	50	180	1	2	1	5	150	85	K(TO-3)
TIP543†	NPN	10	65	40	200	5	4	0.8	10		40	YYYY(TO-59)
2N5940	NPN	10	70	40	200	5	4	1	10		40	CC(TO-111)
2N3790	PNP	10	80	25	90	1	2	1	4	150	85	K(TO-3)
2N3792	PNP	10	80	50	180	1	2	1	5	150	85	K(TO-3)
2N5939	NPN	10	80	40	200	5	4	1	10		40	CC(TO-111)
2N6127	PNP	10	80	30	120	5	5	0.9	5	100†	67	N(TO-61)
2N6128	NPN	10	80	30	120	5	5	0.9	5	100†	67	N(TO-61)
2N3714	NPN	10	80	25	75	1	2	1	5	150	85	K(TO-3)
2N3716	NPN	10	80	50	150	1	2	1	5	150	85	K(TO-3)
2N4301	NPN	10	80	30	120	5	4	0.4	5		50	N(TO-61)
2N3551	NPN	12	60	20	90	10	2	1	10		40	DDD
2N3552	NPN	12	80	20	90	10	2	1	10		40	DDD
2N5386	PNP	12	80	20	80	6	4	0.6	6		50	N(TO-61)
TIP515	NPN	12	120	40	200	6	4	0.8	6		80	K(TO-3)
TIP517	NPN	12	120	40	200	6	4	0.8	6		80	N(TO-61)
TIP516	NPN	12	150	40	200	6	4	0.8	6		80	K(TO-3)
TIP518	NPN	12	150	40	200	6	4	0.8	6		80	N(TO-61)
TIP538	NPN	15	200	20	100	7.5	4	0.75	7.5		125	K(TO-3)
TIP539	NPN	15	300	20	100	7.5	4	0.75	7.5		125	K(TO-3)
TIP531	NPN	15	300	20	120	7.5	4	1.5	15		150	K(TO-3)
TIP533	NPN	15	300	20	120	7.5	4	1.5	15		150	P(TO-63)
TIP540	NPN	15	400	20	100	7.5	4	0.75	7.5		125	K(TO-3)
TIP532	NPN	15	400	20	120	7.5	4	1.5	15		150	K(TO-3)
TIP534	NPN	15	400	20	120	7.5	4	1.5	15		150	P(TO-63)
2N1936	NPN	20	60	10	50	10	3	0.75	10		150	P(TO-63)
2N5039	NPN	20	75	20	100	10	5	2.5	20	140	80	K(TO-3)
2N1937	NPN	20	80	10	50	10	3	0.75	10		150	P(TO-63)
2N5303	NPN	20	80	15	60	10	2	1.5	15	200	114	K(TO-3)
2N4004	NPN	20	80	30	150	10	4	1	20		40	QQ
2N5038	NPN	20	90	20	100	12	5	2.5	20	140	80	K(TO-3)
2N4005	NPN	20	100	30	150	10	4	1	20		40	QQ
2N3846	NPN	20	200	10	60	10	3	0.75	10		150	P(TO-63)
2N3847	NPN	20	300	10	60	10	3	0.75	10		150	P(TO-63)
2N3263	NPN	25	60	20	55	15	2	1	20	83.3	66.7	QQ
2N3265	NPN	25	60	20	55	15	2	1	20	125	100	P(TO-63)
2N3264	NPN	25	90	20	80	15	3	1.6	20	83.3	66.7	QQ
2N3266	NPN	25	90	20	80	15	3	1.6	20	125	100	P(TO-63)
2N4398	PNP	30	40	15	60	15	4	1	15	200	114	K(TO-3)
2N5301	NPN	30	40	15	60	15	2	2	20	200	114	K(TO-3)
2N4399	PNP	30	60	15	60	15	4	1	15	200	114	K(TO-3)

† Radiation tolerant

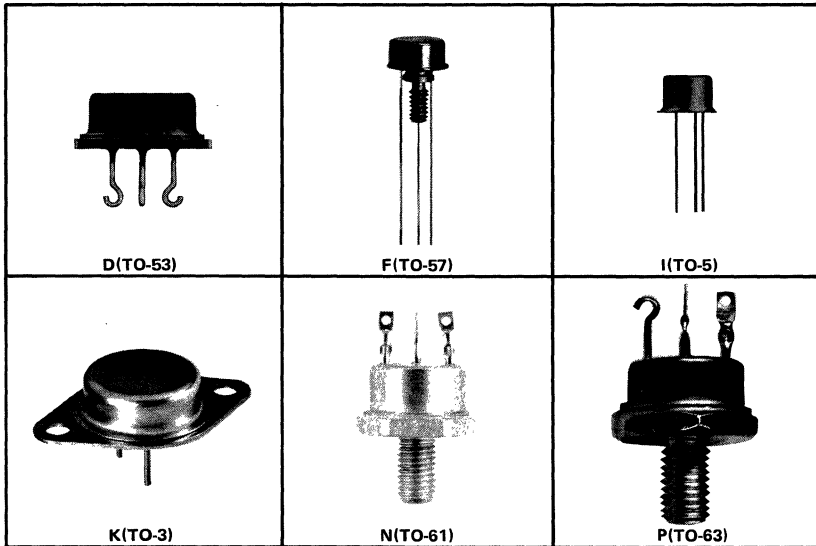
‡ T_C = 50°C

PRODUCT SELECTION GUIDE

HIGH-RELIABILITY SILICON POWER TRANSISTORS

DEVICE TYPE	POLARITY	I _C CONTINUOUS	V _{CEO}	h _{FE} @ I _C V _{CE}				V _{CE(sat)} MAX @ I _C		P _T T _C = 25°C		P _T T _C = 100°C		PACKAGE
				MIN		MAX		V	A	W		W		
				A	V	A	V	V	A					
2N5302	NPN	30	60	15	60	15	2	2	20	200		114	K(TO-3)	
2N4002	NPN	30	80	20	80	15	4	1.2	30			100	P(TO-63)	
2N6270	NPN	30	80	20	100	15	4	1	15			150	K(TO-3)	
2N6272	NPN	30	80	20	100	15	4	1	15			150	P(TO-63)	
2N4003	NPN	30	100	20	80	15	4	1.2	30			100	P(TO-63)	
2N6271	NPN	30	100	20	100	15	4	1	15			150	K(TO-3)	
2N6273	NPN	30	100	20	100	15	4	1	15			150	P(TO-63)	
2N6322	NPN	30	200	40	150	5	5	1.5	20			200	K(TO-3)	
2N6323	NPN	30	200	40	150	5	5	1.5	20			200	P(TO-63)	
2N6324	NPN	30	300	30	150	5	5	1.5	20			200	K(TO-3)	
2N6325	NPN	30	300	30	150	5	5	1.5	20			200	P(TO-63)	
2N5685	NPN	50	60	15	60	25	2	1	25	300		171	K(TO-3)	
2N5683	PNP	50	60	15	60	25	2	1	25	300		171	K(TO-3)	
2N5684	PNP	50	80	15	60	25	2	1	25	300		171	K(TO-3)	
2N5686	NPN	50	80	15	60	25	2	1	25	300		171	K(TO-3)	
T1XP547	NPN	100	60	15	100	50	4	1.5	50			200	5E(TO-114)	
T1XP548	NPN	100	80	15	100	50	4	1.5	50			200	5E(TO-114)	
T1XP549	NPN	100	100	15	100	50	4	1.5	50			200	5E(TO-114)	

3



PRODUCT SELECTION GUIDE
HIGH-RELIABILITY SILICON POWER TRANSISTORS

 <p>S</p>	 <p>BB(TO-111)</p>	 <p>CC(TO-111)</p>
 <p>DD(TO-111)</p>	 <p>QQ</p>	 <p>DDD</p>
 <p>PPP(TO-39)</p>	 <p>YYYYY(TO-59)</p>	 <p>5B(TO-66)</p>
 <p>ZZZZ</p>	 <p>5E(TO-114)</p>	

3

PRODUCT SELECTION GUIDE GERMANIUM POWER TRANSISTORS

DEVICE TYPE	I _C CONTINUOUS	V _{CEO}	h _{FE} @ I _C		V _{CE}		V _{CE(sat)} MAX @ I _C		P _T T _C = 25°C	PACKAGE
			MIN	MAX	A	V	V	A	W	
	A	V								
2N2659	3	30	30	90	0.5	0.5	0.2	0.5	15	I(TO-5)
2N2662	3	30	30	90	0.5	0.5	0.2	0.5	15	C
2N2665	3	30	50	150	0.5	0.5	0.2	0.5	15	I(TO-5)
2N2668	3	30	50	150	0.5	0.5	0.2	0.5	15	C
2N1038	3	40	20	60	1	0.5	0.25	1	20	I(TO-5)
2N2552	3	40	20	60	1	0.5	0.25	1	20	C
2N2556	3	40	20	60	1	0.5	0.25	1	20	B
2N2660	3	40	30	90	0.5	0.5	0.2	0.5	15	I(TO-5)
2N2663	3	40	30	90	0.5	0.5	0.2	0.5	15	C
2N2666	3	40	50	150	0.5	0.5	0.2	0.5	15	I(TO-5)
2N2669	3	40	50	150	0.5	0.5	0.2	0.5	15	C
2N2661	3	50	30	90	0.5	0.5	0.2	0.5	15	I(TO-5)
2N2664	3	50	30	90	0.5	0.5	0.2	0.5	15	C
2N2667	3	50	50	150	0.5	0.5	0.2	0.5	15	I(TO-5)
2N2670	3	50	50	150	0.5	0.5	0.2	0.5	15	C
2N1039	3	60	20	60	1	0.5	0.25	1	20	I(TO-5)
2N2553	3	60	20	60	1	0.5	0.25	1	20	C
2N2557	3	60	20	60	1	0.5	0.25	1	20	B
2N1040	3	80	20	60	1	0.5	0.25	1	20	I(TO-5)
2N2554	3	80	20	60	1	0.5	0.25	1	20	C
2N2558	3	80	20	60	1	0.5	0.25	1	20	B
2N1041	3	100	20	60	1	0.5	0.25	1	20	I(TO-5)
2N2555	3	100	20	60	1	0.5	0.25	1	20	C
2N2559	3	100	20	60	1	0.5	0.25	1	20	B
2N1042	3.5	30	20	60	3	1	0.75	3	20	B
2N2560	3.5	30	20	60	3	1	0.75	3	20	C
2N2564	3.5	30	20	60	3	1	0.75	3	20	I(TO-5)
2N1043	3.5	40	20	60	3	1	0.75	3	20	B
2N2561	3.5	40	20	60	3	1	0.75	3	20	C
2N2565	3.5	40	20	60	3	1	0.75	3	20	I(TO-5)
2N1044	3.5	50	20	60	3	1	0.75	3	20	B
2N2562	3.5	50	20	60	3	1	0.75	3	20	C
2N2566	3.5	50	20	60	3	1	0.75	3	20	I(TO-5)
2N1045	3.5	60	20	60	3	1	0.75	3	20	B
2N2563	3.5	60	20	60	3	1	0.75	3	20	C
2N2567	3.5	60	20	60	3	1	0.75	3	20	I(TO-5)
2N1529	5	20	20	40	3	2	1.5	3	106	K(TO-3)
2N1534	5	20	35	70	3	2	1.2	3	106	K(TO-3)
2N1539	5	20	50	100	3	2	0.3	3	106	K(TO-3)
2N1544	5	20	75	150	3	2	0.2	3	106	K(TO-3)
2N1530	5	30	20	40	3	2	1.5	3	106	K(TO-3)
2N1535	5	30	35	70	3	2	1.2	3	106	K(TO-3)
2N1540	5	30	50	100	3	2	0.3	3	106	K(TO-3)
2N1545	5	30	75	150	3	2	0.2	3	106	K(TO-3)
2N1531	5	40	20	40	3	2	1.5	3	106	K(TO-3)
2N1536	5	40	35	70	3	2	1.2	3	106	K(TO-3)

3

PRODUCT SELECTION GUIDE

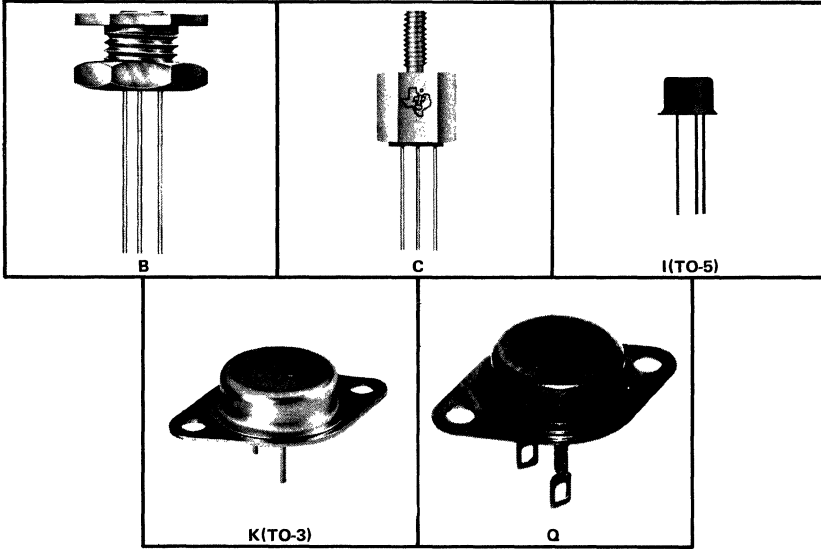
GERMANIUM POWER TRANSISTORS

DEVICE TYPE	I _C CONTINUOUS		V _{CEO}	h _{FE} @ I _C		V _{CE}	V _{CE(sat)} MAX @ I _C		P _T T _C = 25°C	PACKAGE
	A	V		MIN	MAX		A	V	V	
	2N1541	5	40	50	100	3	2	0.3	3	
2N1546	5	40	75	150	3	2	0.2	3	106	K(TO-3)
2N1532	5	50	20	40	3	2	1.5	3	106	K(TO-3)
2N1537	5	50	35	70	3	2	1.2	3	106	K(TO-3)
2N1542	5	50	50	100	3	2	0.3	3	106	K(TO-3)
2N1547	5	50	75	150	3	2	0.2	3	106	K(TO-3)
2N1533	5	60	20	40	3	2	1.5	3	106	K(TO-3)
2N1538	5	60	35	70	3	2	1.2	3	106	K(TO-3)
2N1543	5	60	50	100	3	2	0.3	3	106	K(TO-3)
2N1548	5	60	75	150	3	2	0.2	3	106	K(TO-3)
2N250A	7	25	25	100	3	1.5	0.7	3	90	K(TO-3)
2N251A	7	35	25	100	3	1.5	0.7	3	90	K(TO-3)
2N456A	7	30	30	90	5	1.5	0.5	5	150	K(TO-3)
2N456B	7	30	30	90	5	1.5	0.5	5	150	K(TO-3)
2N457A	7	40	30	90	5	1.5	0.5	5	150	K(TO-3)
2N457B	7	40	30	90	5	1.5	0.5	5	150	K(TO-3)
TI3027	7	40	40	250	3	2	0.5	3	106	K(TO-3)
2N458A	7	45	30	90	5	1.5	0.5	5	150	K(TO-3)
2N458B	7	45	30	90	5	1.5	0.5	5	150	K(TO-3)
TI3028	7	50	40	250	3	2	0.5	3	106	K(TO-3)
2N1021	7	50	30	90	5	1.5	0.5	5	150	K(TO-3)
2N1021A	7	50	30	90	5	1.5	0.5	5	150	K(TO-3)
2N1022	7	55	30	90	5	1.5	0.5	5	150	K(TO-3)
2N1022A	7	55	30	90	5	1.5	0.5	5	150	K(TO-3)
TI3029	7	55	40	250	3	2	0.5	3	106	K(TO-3)
TI3030	7	60	40	250	3	2	0.5	3	106	K(TO-3)
TI3031	7	65	40	250	3	2	0.5	3	106	K(TO-3)
2N1046	12	50	60	200	5	1.5	0.4	5	50 [†]	K(TO-3)
2N3146	15	65	30	90	5	1.5	0.5	10	150	K(TO-3)
2N3147	15	75	30	90	5	1.5	0.5	10	150	K(TO-3)
2N1907	20	40	30	170	10	1.5	0.4	5	60 [‡]	K(TO-3)
2N1908	20	50	30	170	10	1.5	0.4	5	60 [‡]	K(TO-3)
2N511	25	30	20	60	10	2	0.5	10	150	Q
2N512	25	30	20	60	15	2	1	15	150	Q
2N513	25	30	20	60	20	2	1.5	20	150	Q
2N514	25	30	20	60	25	2	2	25	150	Q
2N511A	25	40	20	60	10	2	0.5	10	150	Q
2N512A	25	40	20	60	15	2	1	15	150	Q
2N513A	25	40	20	60	20	2	1.5	20	150	Q
2N514A	25	40	20	60	25	2	2	25	150	Q
2N511B	25	45	20	60	10	2	0.5	10	150	Q
2N512B	25	45	20	60	15	2	1	15	150	Q
2N513B	25	45	20	60	20	2	1.5	20	150	Q
2N514B	25	45	20	60	25	2	2	25	150	Q

[†]T_C = 75°C

[‡]T_C = 70°C

PRODUCT SELECTION GUIDE GERMANIUM POWER TRANSISTORS



3

PRODUCT SELECTION GUIDE

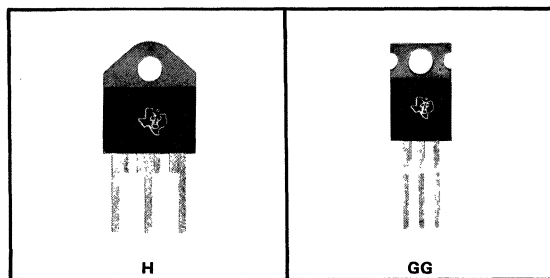
ECONOMY SILICON POWER TRANSISTORS

plastic single-diffused silicon power transistors

TYPE NO.		I _C CONTINUOUS	V _{CEO}	h _{FE}		@		V _{CE(sat)} MAX @ I _C		P _T 25°C	PACKAGE
NPN	PNP			A	V	MIN	MAX	I _C	V _{CE}	V	
TIP29	TIP30	1	40	15	75	1	4	0.7	1	30	GG
TIP29A	TIP30A	1	60	15	75	1	4	0.7	1	30	
TIP29B	TIP30B	1	80	15	75	1	4	0.7	1	30	
TIP29C	TIP30C	1	100	15	75	1	4	0.7	1	30	
TIP31	TIP32	3	40	10	50	3	4	1.2	3	40	
TIP31A	TIP32A	3	60	10	50	3	4	1.2	3	40	
TIP31B	TIP32B	3	80	10	50	3	4	1.2	3	40	
TIP31C	TIP32C	3	100	10	50	3	4	1.2	3	40	
TIP41	TIP42	6	40	15	75	3	4	1.5	6	65	
TIP41A	TIP42A	6	60	15	75	3	4	1.5	6	65	
TIP41B	TIP42B	6	80	15	75	3	4	1.5	6	65	
TIP41C	TIP42C	6	100	15	75	3	4	1.5	6	65	
TIP3055	TIP2955	15	60	20	70	4	4	3	10	90	H
TIP33	TIP34	10	40	20	100	3	4	4	10	80	
TIP33A	TIP34A	10	60	20	100	3	4	4	10	80	
TIP33B	TIP34B	10	80	20	100	3	4	4	10	80	
TIP33C	TIP34C	10	100	20	100	3	4	4	10	80	
TIP35	TIP36	25	40	10	50	15	4	4	25	125	
TIP35A	TIP36A	25	60	10	50	15	4	4	25	125	
TIP35B	TIP36B	25	80	10	50	15	4	4	25	125	
TIP35C	TIP36C	25	100	10	50	15	4	4	25	125	

plastic high-voltage power transistors

TIP47		1	250	30	150	0.3	10	1	1	40	GG
TIP48		1	300	30	150	0.3	10	1	1	40	
TIP49		1	350	30	150	0.3	10	1	1	40	
TIP50		1	400	30	150	0.3	10	1	1	40	
TIP51		3	250	30	150	0.3	10	1.5	3	100	H
TIP52		3	300	30	150	0.3	10	1.5	3	100	
TIP53		3	350	30	150	0.3	10	1.5	3	100	
TIP54		3	400	30	150	0.3	10	1.5	3	100	



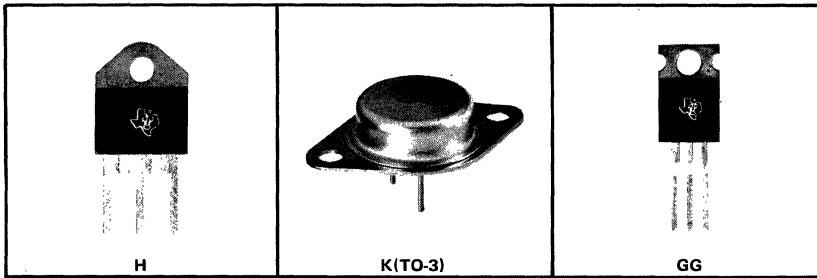
PRODUCT SELECTION GUIDE

ECONOMY SILICON POWER TRANSISTORS

power darlings

TYPE NO.		I_C	V_{CE0}	h_{FE}	@ I_C	V_{CE}	$V_{CE(sat)}$	@ I_C	I_B	P_T	PACKAGE
NPN	PNP	A	V	MIN	A	V	MAX V	A	mA	W	
TIP110	TIP115	2	60	1000	1	4	2.5	2	8	50	GG
TIP111	TIP116	2	80	1000	1	4	2.5	2	8	50	
TIP112	TIP117	2	100	1000	1	4	2.5	2	8	50	
TIP120	TIP125	5	60	1000	3	3	2	3	12	65	GG
TIP121	TIP126	5	80	1000	3	3	2	3	12	65	
TIP122	TIP127	5	100	1000	3	3	2	3	12	65	
TIP140	TIP145	10	60	1000	5	4	2	5	10	125	H
TIP141	TIP146	10	80	1000	5	4	2	5	10	125	
TIP142	TIP147	10	100	1000	5	4	2	5	10	125	
TIP640	TIP645	10	60	1000	5	4	2	5	10	175	K (TO-3)
TIP641	TIP646	10	80	1000	5	4	2	5	10	175	
TIP642	TIP647	10	100	1000	5	4	2	5	10	175	

$^{\dagger}T_C = 25^{\circ}C$



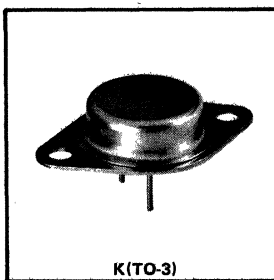
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PRODUCT SELECTION GUIDE

ECONOMY SILICON POWER TRANSISTORS

power transistors in TO-3 hermetic cases

TYPE NO.		I _C CONTINUOUS	V _{CEO}	hFE		β		V _{CE(sat)} MAX @ I _C		P _T 25°C	PACKAGE
NPN	PNP			MIN	MAX	I _C	V _{CE}	V	A	W	
		A	V			A	V	V	A		
2N5067	2N4901	5	40	20	80	1	2	1.5	5	87.5	K (TO-3)
2N5068	2N4902	5	60	20	80	1	2	1.5	5	87.5	
2N5069	2N4903	5	80	20	80	1	2	1.5	5	87.5	
2N4913	2N4904	5	40	25	100	2.5	2	1.5	5	87.5	
2N4914	2N4905	5	60	25	100	2.5	2	1.5	5	87.5	
2N4915	2N4906	5	80	25	100	2.5	2	1.5	5	87.5	
2N5869	2N5867	5	60	20	100	1.5	4	2	3	87.5	
2N5870	2N5868	5	80	20	100	1.5	4	2	3	87.5	
2N5873	2N5871	7	60	20	100	2.5	4	2	5	115	
2N5874	2N5872	7	80	20	100	2.5	4	2	5	115	
2N5877	2N5875	10	60	20	100	4	4	3	8	150	
2N5878	2N5876	10	80	20	100	4	4	3	8	150	
2N3713	2N3789	10	60	25	75	1	2	4	10	150	
2N3714	2N3790	10	80	25	75	1	2	4	10	150	
2N3715	2N3791	10	60	50	150	1	2	4	10	150	
2N3716	2N3792	10	80	50	150	1	2	4	10	150	
2N3055		15	60	20	70	4	4	8	10	115	
2N5881	2N5879	15	60	20	100	6	4	4	12	160	
2N5882	2N5880	15	80	20	100	6	4	4	12	160	
2N5885	2N5883	25	60	20	100	10	4	4	20	200	
2N5886	2N5884	25	80	20	100	10	4	4	20	200	
2N6326	2N6329	30	60	12		15	4	3	30	200	
2N6327	2N6330	30	80	12		15	4	3	30	200	
2N6328	2N6331	30	100	12		15	4	3	30	200	
2N3771		30	40	15	60	15	4	4	30	150	
2N3772		20	60	15	60	10	4	4	20	150	



K(TO-3)

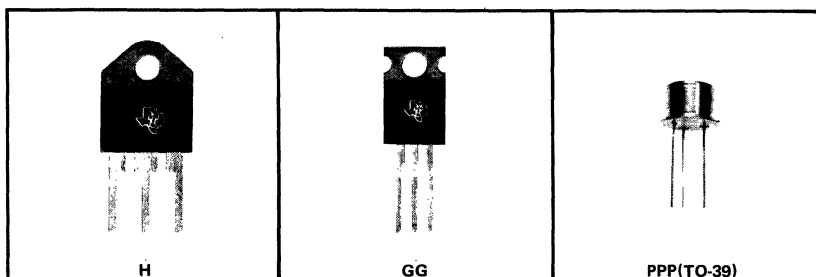
PRODUCT SELECTION GUIDE

ECONOMY THYRISTORS

plastic triacs

TYPE NO.	I _T (RMS)	V _{DRM}	I _{TSM}	I _{GT} MAX I, II, III†	I _{GT} MAX IV†	V _{GT} MAX I, II, III†	V _{GT} MAX IV	V _{TM} MAX @	I _{TM}	I _H MAX	PACKAGE
	A	V	A	mA	mA	V	V	V	A	mA	
TIC205A	2	100	20	5	10	2	2	1.9	2.8	30	PPP (TO-39)
TIC205B	2	200	20	5	10	2	2	1.9	2.8	30	
TIC205D	2	400	20	5	10	2	2	1.9	2.8	30	
TIC206A	3	100	20	5	10	2	2	2.2	4.2	30	GG
TIC206B	3	200	20	5	10	2	2	2.2	4.2	30	
TIC206D	3	400	20	5	10	2	2	2.2	4.2	30	
TIC215A	3	100	20	5	10	2.2	3	2	4.2	30	PPP (TO-39)
TIC215B	3	200	20	5	10	2.2	3	2	4.2	30	
TIC215D	3	400	20	5	10	2.2	3	2	4.2	30	
TIC216A	6	100	60	5	10	2.2	3	1.7	8.4	30	GG
TIC216B	6	200	60	5	10	2.2	3	1.7	8.4	30	
TIC216D	6	400	60	5	10	2.2	3	1.7	8.4	30	
TIC226B	8	200	70	50		2.5		2.1	12	60	GG
TIC226D	8	400	70	50		2.5		2.1	12	60	
TIC236B	12	200	100	50		2.5		2.1	17	50	GG
TIC236D	12	400	100	50		2.5		2.1	17	50	
TIC246B	16	200	125	50		2.5		1.7	22.5	50	GG
TIC246D	16	400	125	50		2.5		1.7	22.5	50	
TIC253B	20	200	150	50		2.5		1.7	28.2	50	H
TIC253D	20	400	150	50		2.5		1.7	28.2	50	
TIC253E	20	500	150	50		2.5		1.7	28.2	50	
TIC253M	20	600	150	50		2.5		1.7	28.2	50	
TIC263B	25	200	175	50		2.5		1.7	35.2	50	H
TIC263D	25	400	175	50		2.5		1.7	35.2	50	
TIC263E	25	500	175	50		2.5		1.7	35.2	50	
TIC263M	25	600	175	50		2.5		1.7	35.2	50	

† Roman numerals designate the V_G, V_S quadrants as explained on page 1-19.



PRODUCT SELECTION GUIDE

ECONOMY THYRISTORS

economy SCR's

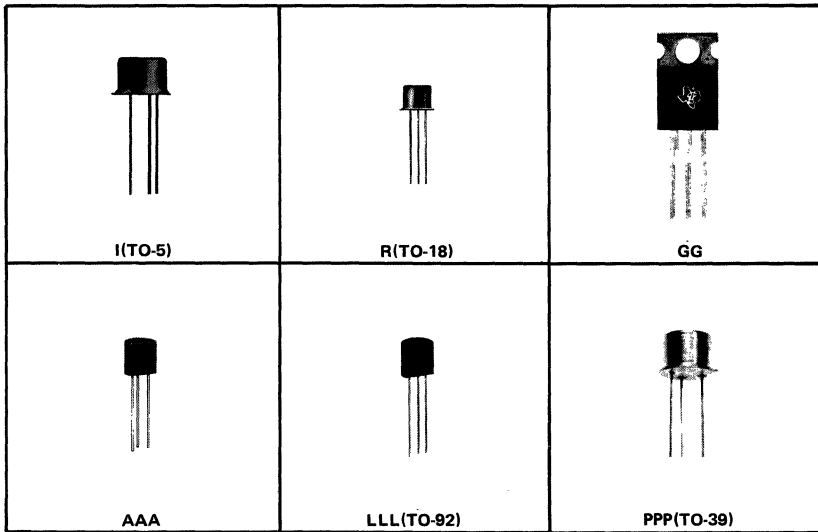
TYPE NO.	I_T	V_{DRM}	I_{TSM}	$I_{GT\ MAX}$	$V_{GT\ MAX}$	$I_H\ MAX$	$V_T\ MAX @$	I_T	PACKAGE
	A	V	A	mA	V	mA	V	A	
2N3001	0.35	30	6	0.02	0.7	3	1.2	0.35	R (TO-18)
2N3002	0.35	60	6	0.02	0.7	3	1.2	0.35	
2N3003	0.35	100	6	0.02	0.7	3	1.2	0.35	
2N3004	0.35	200	6	0.02	0.7	3	1.2	0.35	
2N3005	0.35	30	6	0.2	0.8	5	1.2	0.35	
2N3006	0.35	60	6	0.2	0.8	5	1.2	0.35	
2N3007	0.35	100	6	0.2	0.8	5	1.2	0.35	
2N3008	0.35	200	6	0.2	0.8	5	1.2	0.35	
TIC44	0.6	30	6	0.2	0.8	5	1.4	0.3	AAA
TIC45	0.6	60	6	0.2	0.8	5	1.4	0.3	
TIC46	0.6	100	6	0.2	0.8	5	1.4	0.3	
TIC47	0.6	200	6	0.2	0.8	5	1.4	0.3	
TIC60	0.8	30	6	0.2	0.8	5	1.7	1.2	LLL (TO-92)
TIC61	0.8	60	6	0.2	0.8	5	1.7	1.2	
TIC62	0.8	100	6	0.2	0.8	5	1.7	1.2	
TIC63	0.8	150	6	0.2	0.8	5	1.7	1.2	
TIC64	0.8	200	6	0.2	0.8	5	1.7	1.2	
2N5060	0.8	30	6	0.2	0.8	5	1.7	1.2	
2N5061	0.8	60	6	0.2	0.8	5	1.7	1.2	
2N5062	0.8	100	6	0.2	0.8	5	1.7	1.2	
2N5063	0.8	150	6	0.2	0.8	5	1.7	1.2	
2N5064	0.8	200	6	0.2	0.8	5	1.7	1.2	
2N1595	1	50	15	10	3	25	2	1	I (TO-5)
2N1596	1	100	15	10	3	25	2	1	
2N1597	1	200	15	10	3	25	2	1	
2N1598	1	300	15	10	3	25	2	1	
2N1599	1	400	15	10	3	25	2	1	
TI145A0	1.6	50	30	25	3.5	25	2	1	I (TO-5)
TI145A1	1.6	100	30	25	3.5	25	2	1	
TI145A2	1.6	200	30	25	3.5	25	2	1	
TI145A3	1.6	300	30	25	3.5	25	2	1	
TI145A4	1.6	400	30	25	3.5	25	2	1	
TIC39Y	2	30	20	0.2	1	5	1.75	2	PPP (TO-39)
TIC39F	2	50	20	0.2	1	5	1.75	2	
TIC39A	2	100	20	0.2	1	5	1.75	2	
TIC39B	2	200	20	0.2	1	5	1.75	2	
TIC39C	2	300	20	0.2	1	5	1.75	2	
TIC39D	2	400	20	0.2	1	5	1.75	2	

PRODUCT SELECTION GUIDE

ECONOMY THYRISTORS

economy SCR's

TYPE NO.	I_T	V_{DRM}	I_{TSM}	$I_{GT\ MAX}$	$V_{GT\ MAX}$	$I_H\ MAX$	$V_T\ MAX @$	I_T	PACKAGE
	A	V	A	mA	V	mA	V	A	
2N6332	2	30	20	0.2	0.7	5	1.75	2	PPP (TO-39)
2N6333	2	50	20	0.2	0.7	5	1.75	2	
2N6334	2	100	20	0.2	0.7	5	1.75	2	
2N6335	2	200	20	0.2	0.7	5	1.75	2	
2N6336	2	300	20	0.2	0.7	5	1.75	2	
2N6337	2	400	20	0.2	0.7	5	1.75	2	
TIC106Y	5	30	30	0.2	1	5	1.7	5	GG
TIC106F	5	50	30	0.2	1	5	1.7	5	
TIC106A	5	100	30	0.2	1	5	1.7	5	
TIC106B	5	200	30	0.2	1	5	1.7	5	
TIC106C	5	300	30	0.2	1	5	1.7	5	
TIC106D	5	400	30	0.2	1	5	1.7	5	
TIC116F	8	50	80	20	1.5	40	1.7	8	GG
TIC116A	8	100	80	20	1.5	40	1.7	8	
TIC116B	8	200	80	20	1.5	40	1.7	8	
TIC116C	8	300	80	20	1.5	40	1.7	8	
TIC116D	8	400	80	20	1.5	40	1.7	8	
TIC116E	8	500	80	20	1.5	40	1.7	8	
TIC116M	8	600	80	20	1.5	40	1.7	8	
TIC126F	12	50	100	20	1.5	40	1.4	12	GG
TIC126A	12	100	100	20	1.5	40	1.4	12	
TIC126B	12	200	100	20	1.5	40	1.4	12	
TIC126C	12	300	100	20	1.5	40	1.4	12	
TIC126D	12	400	100	20	1.5	40	1.4	12	
TIC126E	12	500	100	20	1.5	40	1.4	12	
TIC126M	12	600	100	20	1.5	40	1.4	12	



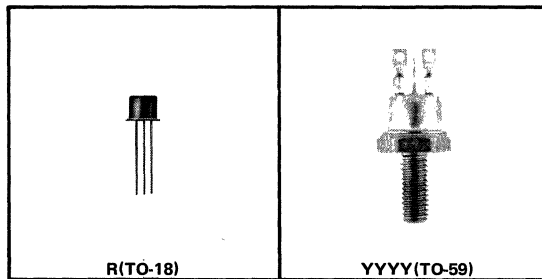
PRODUCT SELECTION GUIDE

RADIATION-TOLERANT SCR'S

radiation-tolerant SCR's

DEVICE TYPE	I _T	V _D	I _H MAX	I _{GT} MAX	V _T		1 X 10 ¹⁴ n/cm ² POST IRRADIATION			PACKAGE
					MAX	@ I _T	I _{GT} MAX	MAX	V _T @ I _T	
					V	A	mA	V	A	
TIC35	0.4	15	4	0.02	1.6	1	5	1.6	1	R(TO-18)
TIC36	0.4	30	4	0.02	1.6	1	5	1.6	1	R(TO-18)
TIC67	20	60	20	20	1.5	20	40	1.5	20	YYYY(TO-59)
TIC68	20	80	20	20	1.5	20	40	1.5	20	YYYY(TO-59)

3



**Alpha-Numeric Index
to
Data Sheets**

ALPHA-NUMERIC INDEX

ALL TYPES

TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE
2N389	5-11	2N1533	6-41
2N424	5-11	2N1534	6-41
2N456A	6-1	2N1535	6-41
2N456B	6-5	2N1536	6-41
2N457A	6-1	2N1537	6-41
2N457B	6-5	2N1538	6-41
2N458A	6-1	2N1539	6-41
2N458B	6-5	2N1540	6-41
2N497	5-13	2N1541	6-41
2N498	5-13	2N1542	6-41
2N511	6-11	2N1543	6-41
2N511A	6-11	2N1544	6-41
2N511B	6-11	2N1545	6-41
2N512	6-15	2N1546	6-41
2N512A	6-15	2N1547	6-41
2N512B	6-15	2N1548	6-41
2N656	5-13	2N1595	7-1
2N657	5-13	2N1596	7-1
2N1021	6-1	2N1597	7-1
2N1021A	6-5	2N1598	7-1
2N1022	6-1	2N1599	7-1
2N1022A	6-5	2N1714	5-23
2N1038	6-19	2N1715	5-23
2N1039	6-19	2N1716	5-23
2N1040	6-19	2N1717	5-23
2N1041	6-19	2N1718	5-23
2N1042	6-27	2N1719	5-23
2N1043	6-27	2N1720	5-23
2N1044	6-27	2N1721	5-23
2N1045	6-27	2N1722	5-31
2N1046	6-35	2N1722A	5-39
2N1047	5-15	2N1723	5-41
2N1047A	5-15	2N1724	5-31
2N1047B	5-15	2N1724A	5-39
2N1048	5-15	2N1725	5-41
2N1048A	5-15	2N1907	6-49
2N1048B	5-15	8N1908	6-49
8N1049	5-15	2N1936	5-43
2N1049A	5-15	2N1937	5-43
2N1049B	5-15	2N2150	5-51
2N1050	5-15	2N2151	5-51
2N1050A	5-15	2N2552	6-19
2N1050B	5-15	2N2553	6-19
2N1529	6-41	2N2554	6-19
2N1530	6-41	2N2555	6-19
2N1531	6-41	2N2556	6-19
2N1532	6-41	2N2557	6-19

ALPHA-NUMERIC INDEX

TYPE NO.	SEC. PAGE
2N2558	6-19
2N2559	6-19
2N2560	6-27
2N2561	6-27
2N2562	6-27
2N2563	6-27
2N2564	6-27
2N2565	6-27
2N2566	6-27
2N2567	6-27
2N2659	6-57
2N2660	6-57
2N2661	6-57
2N2662	6-57
2N2663	6-57
2N2664	6-57
2N2665	6-57
2N2666	6-57
2N2667	6-57
2N2668	6-57
2N2669	6-57
2N2670	6-57
2N2880	5-57
2N2987	5-63
2N2988	5-63
2N2989	5-63
2N2990	5-63
2N2991	5-63
2N2992	5-63
2N2993	5-63
2N2994	5-63
2N3001	7-5
2N3002	7-5
2N3003	7-5
2N3004	7-5
2N3005	7-11
2N3006	7-11
2N3007	7-11
2N3008	7-11
2N3021	5-71
2N3022	5-71
2N3023	5-71
2N3024	5-71
2N3025	5-71
2N3026	5-71
2N3055	5-75
2N3146	6-65
2N3147	6-65
2N3263	5-77

TYPE NO.	SEC. PAGE
2N3264	5-77
2N3265	5-77
2N3266	5-77
2N3418	5-81
2N3419	5-81
2N3420	5-81
2N3421	5-81
2N3439	5-87
2N3440	5-87
2N3551	5-91
2N3552	5-91
2N3583	5-95
2N3584	5-95
2N3585	5-95
2N3713	5-99
2N3714	5-99
2N3715	5-99
2N3716	5-99
2N3719	5-105
2N3720	5-105
2N3771	5-109
2N3772	5-109
2N3789	5-111
2N3790	5-111
2N3791	5-111
2N3792	5-111
2N3846	5-117
2N3847	5-117
2N3902	5-123
2N3996	5-127
2N3997	5-127
2N3998	5-127
2N3999	5-127
2N4000	5-133
2N4001	5-133
2N4002	5-139
2N4003	5-139
2N4004	5-145
2N4005	5-145
2N4240	5-95
2N4300	5-151
2N4301	5-157
2N4398	5-163
2N4399	5-163
2N4901	5-167
2N4902	5-167
2N4903	5-167
2N4904	5-171
2N4905	5-171

4

ALPHA-NUMERIC INDEX

TYPE NO.	SEC.-PAGE
2N4906	5-171
2N4913	5-175
2N4914	5-175
2N4915	5-175
2N4998	5-181
2N4999	5-185
2N5000	5-181
2N5001	5-185
2N5002	5-189
2N5003	5-193
2N5004	5-189
2N5005	5-193
2N5038	5-197
2N5039	5-197
2N5060	7-19
2N5061	7-19
2N5062	7-19
2N5063	7-19
2N5064	7-19
2N5067	5-199
2N5068	5-199
2N5069	5-199
2N5147	5-185
2N5148	5-181
2N5149	5-185
2N5150	5-181
2N5151	5-193
2N5152	5-189
2N5153	5-193
2N5154	5-189
2N5157	5-203
2N5241	5-207
2N5301	5-211
2N5302	5-211
2N5303	5-211
2N5333	5-217
2N5384	5-223
2N5385	5-223
2N5386	5-227
2N5387	5-231
2N5388	5-231
2N5389	5-231
2N5390	5-237
2N5671	5-243
2N5672	5-243
2N5683	5-247
2N5684	5-247
2N5685	5-249
2N5686	5-249

TYPE NO.	SEC.-PAGE
2N5758	5-251
2N5759	5-251
2N5760	5-251
2N5867	5-253
2N5868	5-253
2N5869	5-255
2N5870	5-255
2N5871	5-257
2N5872	5-257
2N5873	5-259
2N5874	5-259
2N5875	5-261
2N5876	5-261
2N5877	5-263
2N5878	5-263
2N5879	5-265
2N5880	5-265
2N5881	5-267
2N5882	5-267
2N5883	5-269
2N5884	5-269
2N5885	5-271
2N5886	5-271
2N5938	5-273
2N5939	5-279
2N5940	5-279
2N6127	5-285
2N6128	5-289
2N6270	5-293
2N6271	5-293
2N6272	5-293
2N6273	5-293
2N6322	5-297
2N6323	5-297
2N6324	5-297
2N6325	5-297
2N6326	5-301
2N6327	5-301
2N6328	5-301
2N6329	5-305
2N6330	5-305
2N6331	5-305
2N6332	7-23
2N6333	7-23
2N6334	7-23
2N6335	7-23
2N6336	7-23
2N6337	7-23
T1145A0	7-25

ALPHA-NUMERIC INDEX

TYPE NO.	SEC.-PAGE
TI145A1	7-25
TI145A2	7-25
TI145A3	7-25
TI145A4	7-25
TI156	6-67
TI156L	6-67
TI159	6-69
TI160	6-69
TI161	6-69
TI162	6-69
TI486	5-309
TI487	5-309
TI1131	5-315
TI1132	5-315
TI1133	5-315
TI1134	5-315
TI1135	5-315
TI1136	5-315
TI1151	5-317
TI1152	5-317
TI1153	5-317
TI1154	5-317
TI1155	5-317
TI1156	5-317
TI3027	6-73
TI3028	6-73
TI3029	6-77
TI3030	6-77
TI3031	6-77
TIC35	7-27
TIC36	7-27
TIC39	7-35
TIC44	7-37
TIC45	7-37
TIC46	7-37
TIC47	7-37
TIC60	7-19
TIC61	7-19
TIC62	7-19
TIC63	7-19
TIC64	7-19
TIC67	7-43
TIC68	7-43
TIC106	7-45
TIC116	7-51
TIC126	7-51
TIC205	7-57
TIC206	7-57
TIC215	7-59

TYPE NO.	SEC.-PAGE
TIC216	7-59
TIC226B	7-61
TIC226D	7-61
TIC236	7-65
TIC246	7-65
TIC253	7-67
TIC263	7-67
TIP29	5-319
TIP29A	5-319
TIP29B	5-319
TIP29C	5-319
TIP30	5-323
TIP30A	5-323
TIP30B	5-323
TIP30C	5-323
TIP31	5-327
TIP31A	5-327
TIP31B	5-327
TIP31C	5-327
TIP32	5-331
TIP32A	5-331
TIP32B	5-331
TIP32C	5-331
TIP33	5-335
TIP33A	5-335
TIP33B	5-335
TIP33C	5-335
TIP34	5-339
TIP34A	5-339
TIP34B	5-339
TIP34C	5-339
TIP35	5-343
TIP35A	5-343
TIP35B	5-343
TIP35C	5-343
TIP36	5-347
TIP36A	5-347
TIP36B	5-347
TIP36C	5-347
TIP41	5-351
TIP41A	5-351
TIP41B	5-351
TIP41C	5-351
TIP42	5-355
TIP42A	5-355
TIP42B	5-355
TIP42C	5-355
TIP47	5-359
TIP48	5-359

4

ALPHA-NUMERIC INDEX

TYPE NO.	SEC.-PAGE
TIP49	5-359
TIP50	5-359
TIP51	5-363
TIP52	5-363
TIP53	5-363
TIP54	5-363
TIP110	5-367
TIP111	5-367
TIP112	5-367
TIP115	5-371
TIP116	5-371
TIP117	5-371
TIP120	5-375
TIP121	5-375
TIP122	5-375
TIP125	5-379
TIP126	5-379
TIP127	5-379
TIP140	5-383
TIP141	5-383
TIP142	5-383
TIP145	5-387
TIP146	5-387
TIP147	5-387
TIP501	5-391
TIP502	5-391
TIP503	5-395
TIP504	5-395
TIP505	5-395
TIP506	5-395
TIP507	5-397
TIP508	5-397
TIP509	5-399
TIP510	5-399
TIP511	5-399
TIP512	5-399
TIP513	5-401
TIP514	5-401
TIP515	5-403
TIP516	5-403
TIP517	5-403
TIP518	5-403
TIP519	5-405
TIP520	5-405
TIP521	5-407
TIP522	5-407
TIP523	5-409

TYPE NO.	SEC.-PAGE
TIP524	5-409
TIP525	5-411
TIP526	5-411
TIP527	5-413
TIP528	5-413
TIP529	5-415
TIP530	5-415
TIP531	5-417
TIP532	5-417
TIP533	5-417
TIP534	5-417
TIP535	5-419
TIP536	5-419
TIP537	5-419
TIP538	5-421
TIP539	5-421
TIP540	5-421
TIP541	5-423
TIP542	5-425
TIP543	5-427
TIP544	5-429
TIP545	5-429
TIP546	5-429
TIP640	5-433
TIP641	5-433
TIP642	5-433
TIP645	5-437
TIP646	5-437
TIP647	5-437
TIP2955	5-441
TIP3055	5-445
TIXH601	9-3
TIXH602	9-5
TIXH603	9-7
TIXH604	9-7
TIXH701	9-9
TIXH702	9-11
TIXH703	9-13
TIXH704	9-15
TIXH801	9-17
TIXH802	9-17
TIXH803	9-19
TIXH804	9-19
TIXH805	9-21
TIXH806	9-25
TIXP547	5-431
TIXP548	5-431
TIXP549	5-431

ALPHA-NUMERIC INDEX

SILICON POWER TRANSISTORS

TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE
2N389	5-11	2N3024	5-71	2N4399	5-163	2N5685	5-249
2N424	5-11	2N3025	5-71	2N4901	5-167	2N5686	5-249
2N497	5-13	2N3026	5-71	2N4902	5-167	2N5758	5-251
2N498	5-13	2N3055	5-75	2N4903	5-167	2N5759	5-251
2N656	5-13	2N3263	5-77	2N4904	5-171	2N5760	5-251
2N657	5-13	2N3264	5-77	2N4905	5-171	2N5867	5-253
2N1047	5-15	2N3265	5-77	2N4906	5-171	2N5868	5-253
2N1047A	5-15	2N3266	5-77	2N4913	5-175	2N5869	5-255
2N1047B	5-15	2N3418	5-81	2N4914	5-175	2N5870	5-255
2N1048	5-15	2N3419	5-81	2N4915	5-175	2N5871	5-257
2N1048A	5-15	2N3420	5-81	2N4998	5-181	2N5872	5-257
2N1048B	5-15	2N3421	5-81	2N4999	5-185	2N5873	5-259
2N1049	5-15	2N3439	5-87	2N5000	5-181	2N5874	5-259
2N1049A	5-15	2N3440	5-87	2N5001	5-185	2N5875	5-261
2N1049B	5-15	2N3551	5-91	2N5002	5-189	2N5876	5-261
2N1050	5-15	2N3552	5-91	2N5003	5-193	2N5877	5-263
2N1050A	5-15	2N3583	5-95	2N5004	5-189	2N5878	5-263
2N1050B	5-15	2N3584	5-95	2N5005	5-193	2N5879	5-265
2N1714	5-23	2N3585	5-95	2N5038	5-197	2N5880	5-265
2N1715	5-23	2N3713	5-99	2N5039	5-197	2N5881	5-267
2N1716	5-23	2N3714	5-99	2N5067	5-199	2N5882	5-267
2N1717	5-23	2N3715	5-99	2N5068	5-199	2N5883	5-269
2N1718	5-23	2N3716	5-99	2N5069	5-199	2N5884	5-269
2N1719	5-23	2N3719	5-105	2N5147	5-185	2N5885	5-271
2N1720	5-23	2N3720	5-105	2N5148	5-181	2N5886	5-271
2N1721	5-23	2N3771	5-109	2N5149	5-185	2N5938	5-273
2N1722	5-31	2N3772	5-109	2N5150	5-181	2N5939	5-279
2N1722A	5-39	2N3789	5-111	2N5151	5-193	2N5940	5-279
2N1723	5-41	2N3790	5-111	2N5152	5-189	2N6127	5-285
2N1724	5-31	2N3791	5-111	2N5153	5-193	2N6128	5-289
2N1724A	5-39	2N3792	5-111	2N5154	5-189	2N6270	5-293
2N1725	5-41	2N3846	5-117	2N5157	5-203	2N6271	5-293
2N1936	5-43	2N3847	5-117	2N5241	5-207	2N6272	5-293
2N1937	5-43	2N3902	5-123	2N5301	5-211	2N6273	5-293
2N2150	5-51	2N3996	5-127	2N5302	5-211	2N6322	5-297
2N2151	5-51	2N3997	5-127	2N5303	5-211	2N6323	5-297
2N2880	5-57	2N3998	5-127	2N5333	5-217	2N6324	5-297
2N2987	5-63	2N3999	5-127	2N5384	5-223	2N6325	5-297
2N2988	5-63	2N4000	5-133	2N5385	5-223	2N6326	5-301
2N2989	5-63	2N4001	5-133	2N5386	5-227	2N6327	5-301
2N2990	5-63	2N4002	5-139	2N5387	5-231	2N6328	5-301
2N2991	5-63	2N4003	5-139	2N5388	5-231	2N6329	5-305
2N2992	5-63	2N4004	5-145	2N5389	5-231	2N6330	5-305
2N2993	5-63	2N4005	5-145	2N5390	5-237	2N6331	5-305
2N2994	5-63	2N4240	5-95	2N5671	5-243	TI486	5-309
2N3021	5-71	2N4300	5-151	2N5672	5-243	TI487	5-309
2N3022	5-71	2N4301	5-157	2N5683	5-247	TI1131	5-315
2N3023	5-71	2N4398	5-163	2N5684	5-247	TI1132	5-315

4

ALPHA-NUMERIC INDEX

TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE
T11134	5-315	TIP35	5-343	TIP125	5-379	TIP525	5-411
T11135	5-315	TIP35A	5-343	TIP126	5-379	TIP526	5-411
T11136	5-315	TIP35B	5-343	TIP127	5-379	TIP527	5-413
T11151	5-317	TIP35C	5-343	TIP140	5-383	TIP528	5-413
T11152	5-317	TIP36	5-347	TIP141	5-383	TIP529	5-415
T11153	5-317	TIP36A	5-347	TIP142	5-383	TIP530	5-415
T11154	5-317	TIP36B	5-347	TIP145	5-387	TIP531	5-417
T11155	5-317	TIP36C	5-347	TIP146	5-387	TIP532	5-417
T11156	5-317	TIP41	5-351	TIP147	5-387	TIP533	5-417
TIP29	5-319	TIP41A	5-351	TIP501	5-391	TIP534	5-417
TIP29A	5-319	TIP41B	5-351	TIP502	5-391	TIP535	5-419
TIP29B	5-319	TIP41C	5-351	TIP503	5-395	TIP536	5-419
TIP29C	5-319	TIP42	5-355	TIP504	5-395	TIP537	5-419
TIP30	5-323	TIP42A	5-355	TIP505	5-395	TIP538	5-421
TIP30A	5-323	TIP42B	5-355	TIP506	5-395	TIP539	5-421
TIP30B	5-323	TIP42C	5-355	TIP507	5-397	TIP540	5-421
TIP30C	5-323	TIP47	5-359	TIP508	5-397	TIP541	5-423
TIP31	5-327	TIP48	5-359	TIP509	5-399	TIP542	5-425
TIP31A	5-327	TIP49	5-359	TIP510	5-399	TIP543	5-427
TIP31B	5-327	TIP50	5-359	TIP511	5-399	TIP544	5-429
TIP31C	5-327	TIP51	5-363	TIP512	5-399	TIP545	5-429
TIP32	5-331	TIP52	5-363	TIP513	5-401	TIP546	5-429
TIP32A	5-331	TIP53	5-363	TIP514	5-401	TIP640	5-433
TIP32B	5-331	TIP54	5-363	TIP515	5-403	TIP641	5-433
TIP32C	5-331	TIP110	5-367	TIP516	5-403	TIP642	5-433
TIP33	5-335	TIP111	5-367	TIP517	5-403	TIP645	5-437
TIP33A	5-335	TIP112	5-367	TIP518	5-403	TIP646	5-437
TIP33B	5-335	TIP115	5-371	TIP519	5-405	TIP647	5-437
TIP33C	5-335	TIP116	5-371	TIP520	5-405	TIP2955	5-441
TIP34	5-339	TIP117	5-371	TIP521	5-407	TIP3055	5-445
TIP34A	5-339	TIP120	5-375	TIP522	5-407	TIXP547	5-431
TIP34B	5-339	TIP121	5-375	TIP523	5-409	TIXP548	5-431
TIP34C	5-339	TIP122	5-375	TIP524	5-409	TIXP549	5-431

4

ALPHA-NUMERIC INDEX

GERMANIUM POWER TRANSISTORS

TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE
2N456A	6-1	2N1044	6-27	2N1548	6-41	2N2662	6-57
2N456B	6-5	2N1045	6-27	2N1907	6-49	2N2663	6-57
2N457A	6-1	2N1046	6-35	2N1908	6-49	2N2664	6-57
2N457B	6-5	2N1529	6-41	2N2552	6-19	2N2665	6-57
2N458A	6-1	2N1530	6-41	2N2553	6-19	2N2666	6-57
2N458B	6-5	2N1531	6-41	2N2554	6-19	2N2667	6-57
2N511	6-11	2N1532	6-41	2N2555	6-19	2N2668	6-57
2N511A	6-11	2N1533	6-41	2N2556	6-19	2N2669	6-57
2N511B	6-11	2N1534	6-41	2N2557	6-19	2N2670	6-57
2N512	6-15	2N1535	6-41	2N2558	6-19	2N3146	6-65
2N512A	6-15	2N1536	6-41	2N2559	6-19	2N3147	6-65
2N512B	6-15	2N1537	6-41	2N2560	6-27	TI156	6-67
2N1021	6-1	2N1538	6-41	2N2561	6-27	TI156L	6-67
2N1021A	6-5	2N1539	6-41	2N2562	6-27	TI159	6-69
2N1022	6-1	2N1540	6-41	2N2563	6-27	TI160	6-69
2N1022A	6-5	2N1541	6-41	2N2564	6-27	TI161	6-69
2N1038	6-19	2N1542	6-41	2N2565	6-27	TI162	6-69
2N1039	6-19	2N1543	6-41	2N2566	6-27	TI3027	6-73
2N1040	6-19	2N1544	6-41	2N2567	6-27	TI3028	6-73
2N1041	6-19	2N1545	6-41	2N2659	6-57	TI3029	6-77
2N1042	6-27	2N1546	6-41	2N2660	6-57	TI3030	6-77
2N1043	6-27	2N1547	6-41	2N2661	6-57	TI3031	6-77

THYRISTORS

TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE
2N1595	7-1	2N5061	7-19	TI145A4	7-25	TIC68	7-43
2N1596	7-1	2N5062	7-19	TIC35	7-27	TIC106	7-45
2N1597	7-1	2N5063	7-19	TIC36	7-27	TIC116	7-51
2N1598	7-1	2N5064	7-19	TIC39	7-35	TIC126	7-51
2N1599	7-1	2N6332	7-23	TIC44	7-37	TIC205	7-57
2N3001	7-5	2N6333	7-23	TIC45	7-37	TIC206	7-57
2N3002	7-5	2N6334	7-23	TIC46	7-37	TIC215	7-59
2N3003	7-5	2N6335	7-23	TIC47	7-37	TIC216	7-59
2N3004	7-5	2N6336	7-23	TIC60	7-19	TIC226B	7-61
2N3005	7-11	2N6337	7-23	TIC61	7-19	TIC226D	7-61
2N3006	7-11	TI145A0	7-25	TIC62	7-19	TIC236	7-65
2N3007	7-11	TI145A1	7-25	TIC63	7-19	TIC246	7-65
2N3008	7-11	TI145A2	7-25	TIC64	7-19	TIC253	7-67
2N5060	7-19	TI145A3	7-25	TIC67	7-43	TIC263	7-67

POWER FUNCTIONS

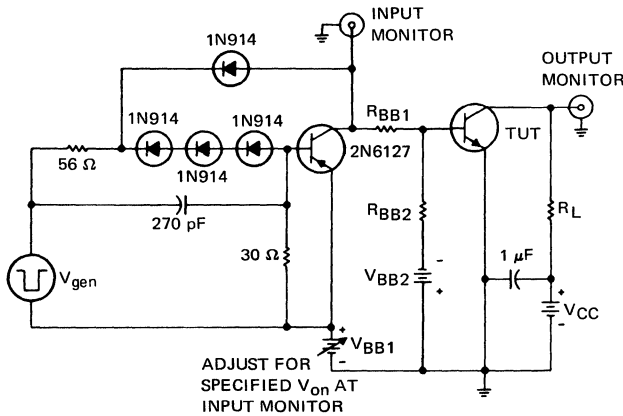
TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE	TYPE NO.	SEC.-PAGE
TIXH601	9-3	TIXH701	9-9	TIXH801	9-17	TIXH804	9-19
TIXH602	9-5	TIXH702	9-11	TIXH802	9-17	TIXH805	9-21
TIXH603	9-7	TIXH703	9-13	TIXH803	9-19	TIXH806	9-25
TIXH604	9-7	TIXH704	9-15				

Silicon Power Data Sheets

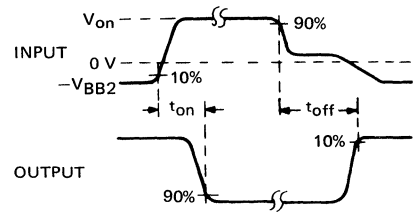


SILICON POWER TRANSISTORS STANDARD TEST CIRCUITS

The circuits shown below are used to test many of the silicon power transistors manufactured by Texas Instruments. They are taken from the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.



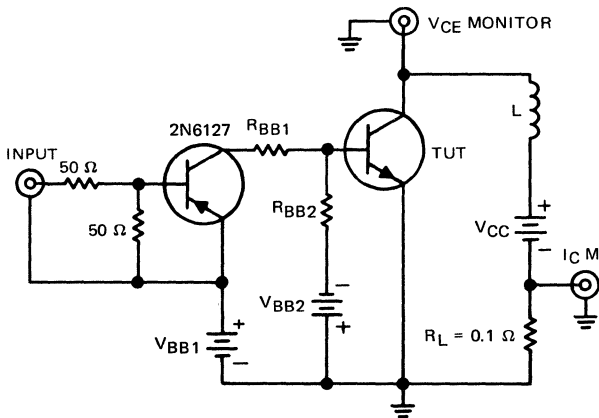
TEST CIRCUIT



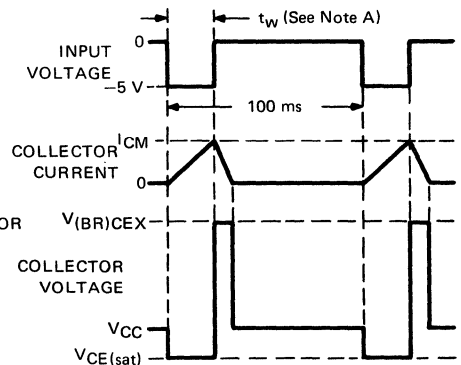
VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 5\text{ }\mu\text{s}$, duty cycle $\leq 5\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10\text{ ns}$, $R_{in} \geq 1\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.
 F. Circuit shown is for testing n-p-n transistors. For p-p-n transistors, all voltage supplies and waveforms are reversed and the driver transistor is type 2N6128.

FIGURE 1—SWITCHING TIMES



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. Input pulse width is increased until the peak collector current reaches the specified value of I_{CM} .
 B. Circuit shown is for testing n-p-n transistors. For p-p-n transistors, all voltage supplies and waveforms are reversed and the driver transistor is type 2N6128.

FIGURE 2—INDUCTIVE LOAD SWITCHING

5

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS
BULLETIN NO. DL-S-718870, JANUARY 1971
REVISED SEPTEMBER 1971

This data sheet identifies those standard hardware kits which are supplied with each device. At additional cost, nonstandard hardware items will be supplied.

The mounting hardware assembly drawings of Section A (Figures 1 through 8) specify the individual hardware items that are included in each mounting hardware kit. Section A also references the package outlines for which each kit is designed and shows the typical thermal resistance associated with the mounting hardware.

Section B contains mechanical drawings of the individual hardware items that are referenced in Figures 1 through 8.

DIRECTORY

OUTLINE	KIT
TO-3	7
TO-5	1
TO-33	1
TO-39	1
TO-53	4
TO-57	3
TO-59	8
TO-60	8
TO-61 Unisolated	5
TO-63	6
TO-111 Unisolated	2
TO-111 Isolated	8

Texas Instruments reserves the right to substitute similar parts at any time in order to expedite delivery or improve design.

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

SECTION A — MOUNTING HARDWARE ASSEMBLY DRAWINGS

MOUNTING KIT 1
for
TO-5, TO-33, AND TO-39
PACKAGE OUTLINES

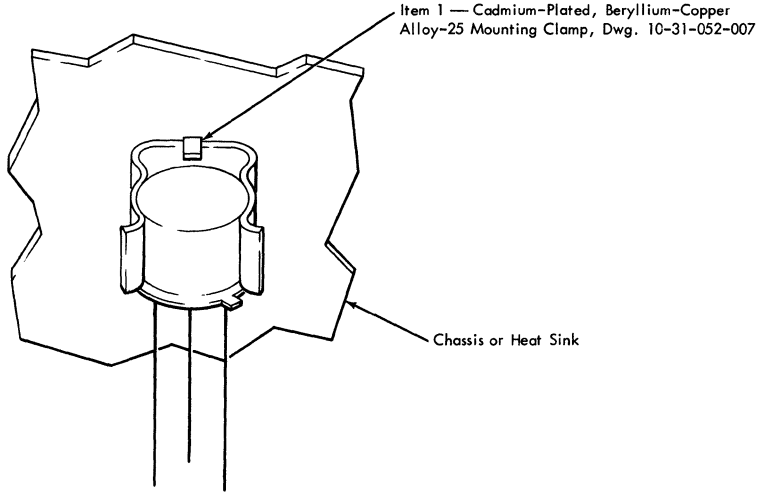
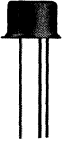


FIGURE 1

MOUNTING KIT 2
for
TO-111 AND OTHER
7/16-INCH STUD PACKAGE OUTLINES
(INSULATION REQUIRED)

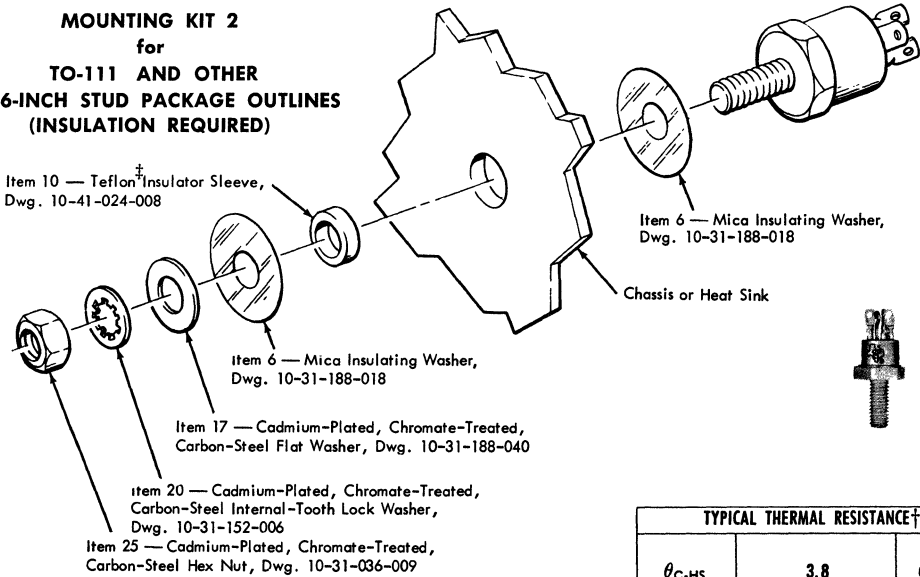


FIGURE 2

TYPICAL THERMAL RESISTANCE†		
θ_{C-HS}	3.8	deg/W

† θ_{C-HS} is the thermal resistance from the mounting base of the semiconductor-device case to the mounting surface of the heat sink. The heat sink used to determine this value was a smooth, flat, copper plate, with the thermocouple mounted 0.05 inch below the mounting surface in an area beneath the device. The device was mounted directly to a clean, dry, heat-sink surface, without the use of a thermal compound and a torque of ten inch-pounds was applied to the stud or each of the mounting screws.

‡ Trademark of E. I. duPont

5

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

SECTION A — MOUNTING HARDWARE ASSEMBLY DRAWINGS

MOUNTING KIT 3 for TO-57 PACKAGE OUTLINE

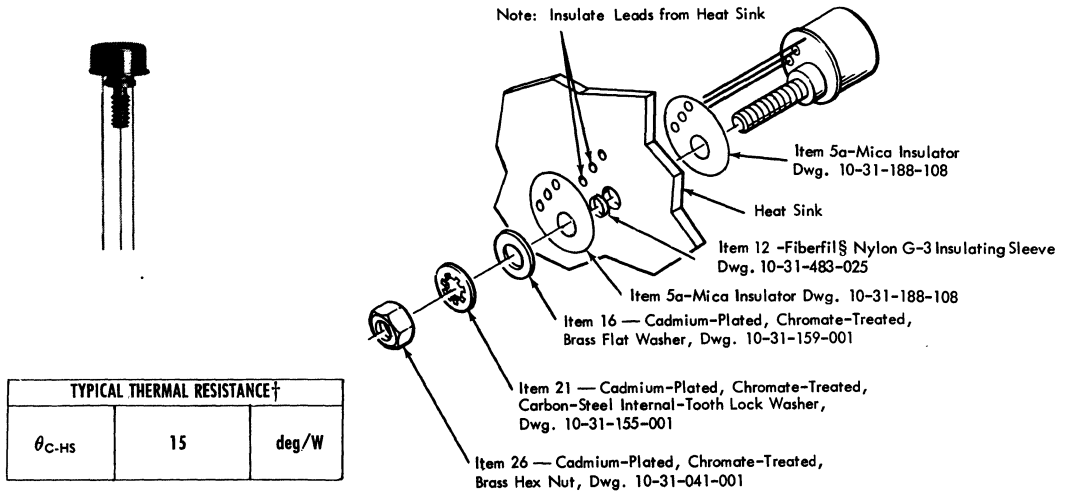


FIGURE 3

MOUNTING KIT 4 for TO-53 PACKAGE OUTLINE

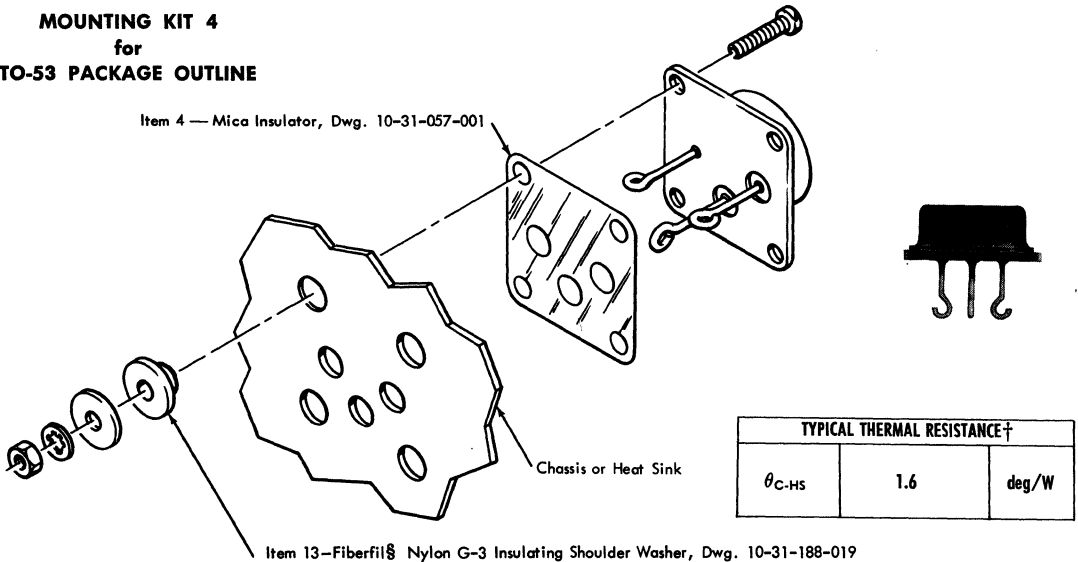


FIGURE 4

† θ_{C-HS} is the thermal resistance from the mounting base of the semiconductor-device case to the mounting surface of the heat sink. The heat sink used to determine this value was a smooth, flat, copper plate, with the thermocouple mounted 0.05 inch below the mounting surface in an area beneath the device. The device was mounted directly to a clean, dry, heat-sink surface, without the use of a thermal compound and a torque of ten inch-pounds was applied to the stud or each of the mounting screws.

§Trademark of Cedar Plastics

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

SECTION A — MOUNTING HARDWARE ASSEMBLY DRAWINGS

MOUNTING KIT 5 for TO-61 PACKAGE OUTLINE

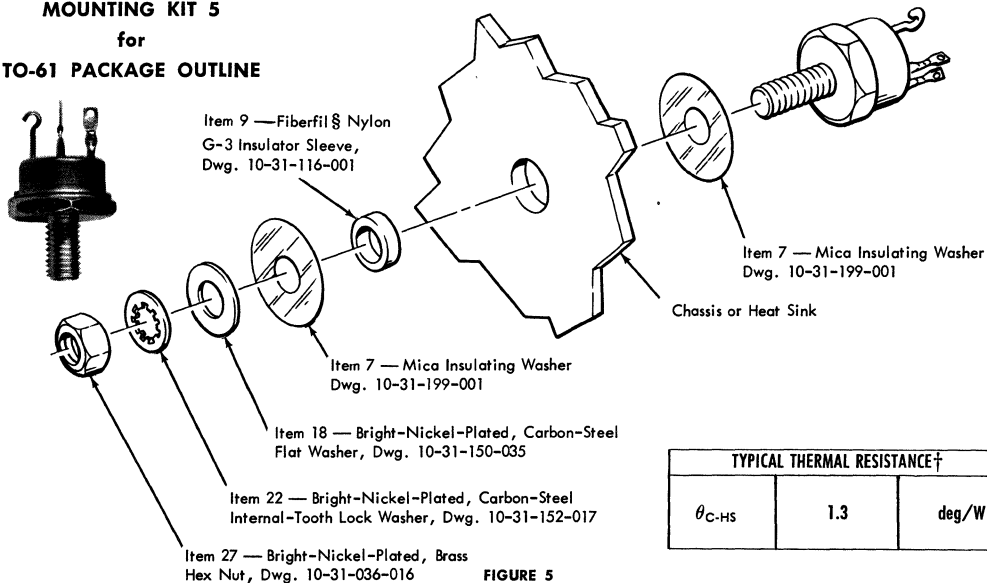


FIGURE 5

MOUNTING KIT 6 for TO-63 PACKAGE OUTLINE

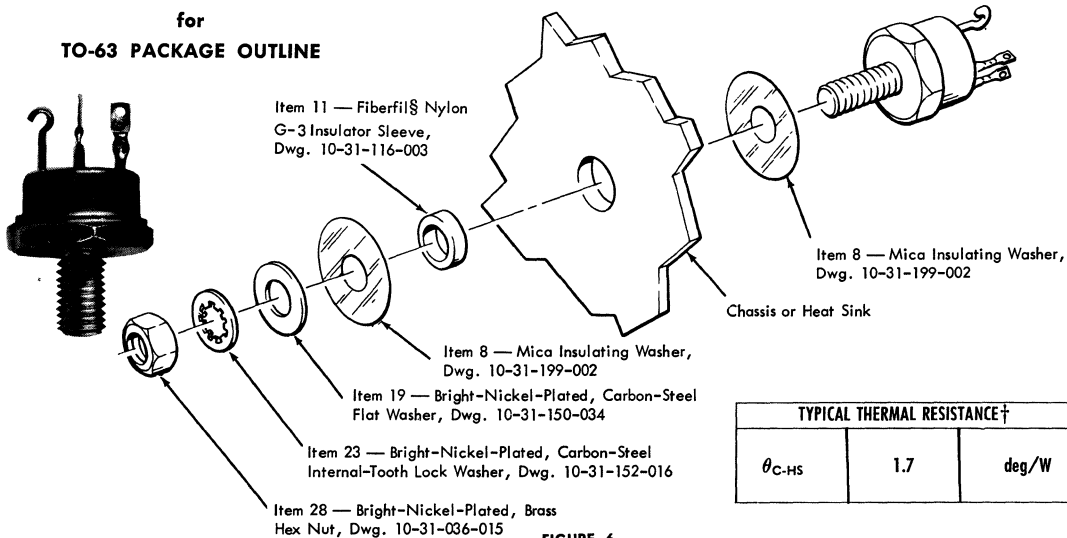


FIGURE 6

† θ_{C-HS} is the thermal resistance from the mounting base of the semiconductor-device case to the mounting surface of the heat sink. The heat sink used to determine this value was a smooth, flat, copper plate, with the thermocouple mounted 0.05 inch below the mounting surface in an area beneath the device. The device was mounted directly to a clean, dry, heat-sink surface, without the use of a thermal compound and a torque of ten inch-pounds was applied to the stud or each of the mounting screws.

§Trademark of Cedar Plastics

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

SECTION A — MOUNTING HARDWARE ASSEMBLY DRAWINGS

MOUNTING KIT 7
for
TO-3 PACKAGE OUTLINE

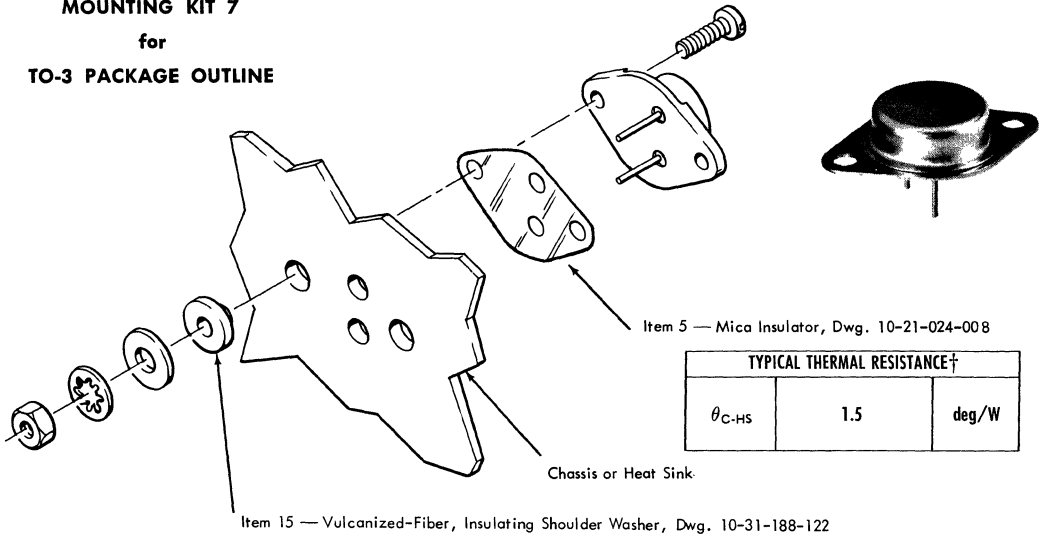


FIGURE 7

MOUNTING KIT 8
for
TO-59, TO-60, TO-111, AND OTHER
7/16-INCH STUD PACKAGE OUTLINES
(NO INSULATION REQUIRED)

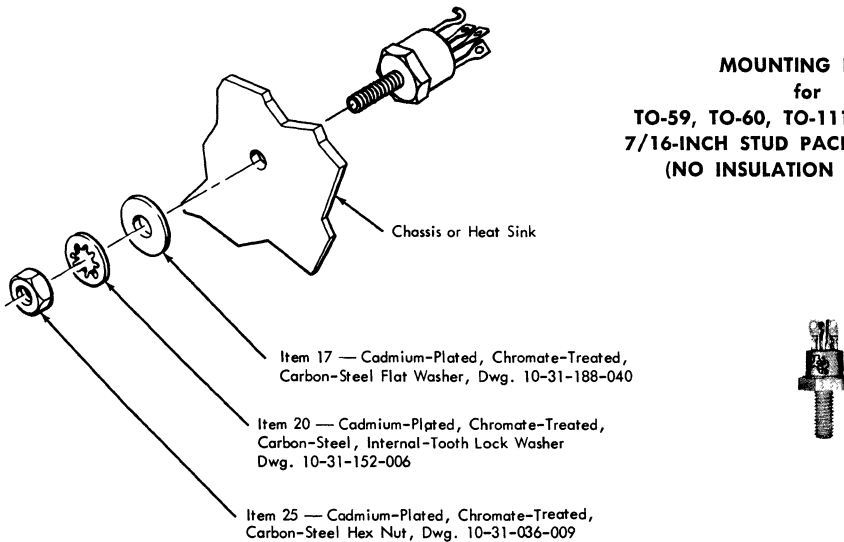
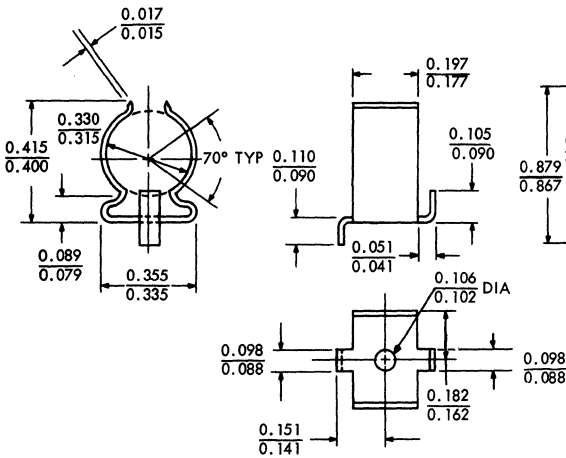


FIGURE 8

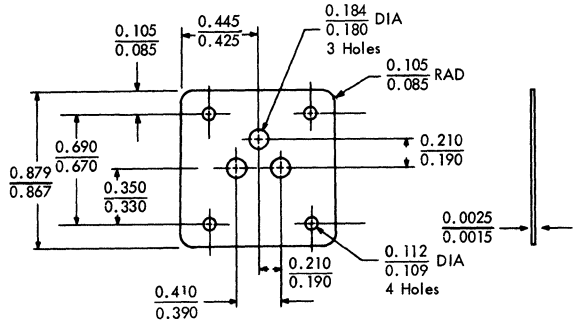
† θ_{C-HS} is the thermal resistance from the mounting base of the semiconductor-device case to the mounting surface of the heat sink. The heat sink used to determine this value was a smooth, flat, copper plate, with the thermocouple mounted 0.05 inch below the mounting surface in an area beneath the device. The device was mounted directly to a clean, dry, heat-sink surface, without the use of a thermal compound and a torque of ten inch-pounds was applied to the stud or each of the mounting screws.

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

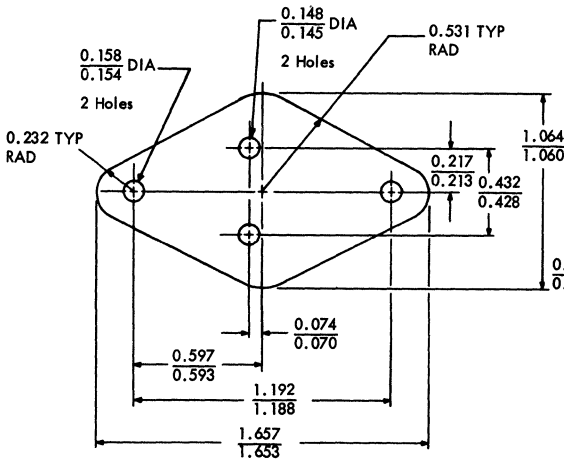
SECTION B — MECHANICAL DRAWINGS OF HARDWARE ITEMS †



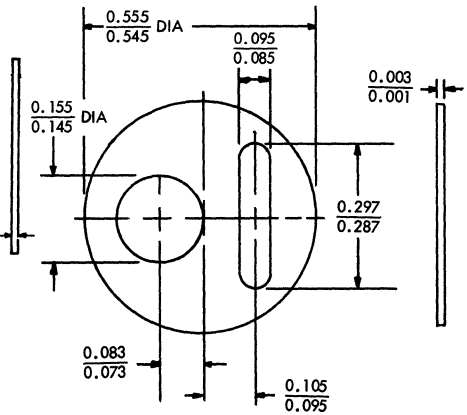
MOUNTING CLAMP
Item 1



INSULATOR
Item 4



INSULATOR
Item 5

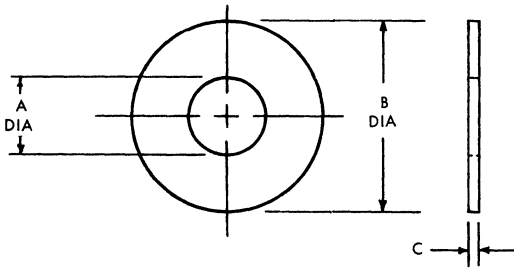


INSULATING WASHER
Item 5a

† All dimensions are in inches unless otherwise specified.

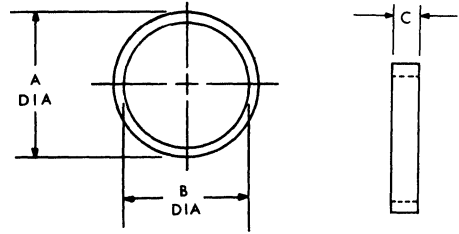
STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

SECTION B — MECHANICAL DRAWINGS OF HARDWARE ITEMS †



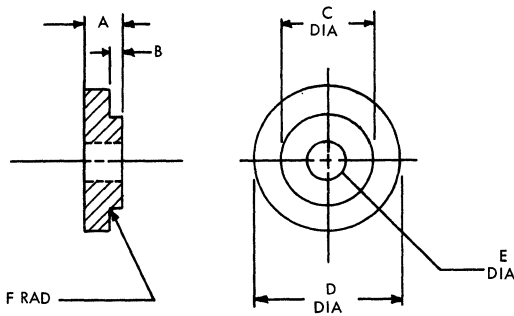
Item	A	B	C
6	0.205	0.536	0.005
	0.195	0.526	0.001
7	0.270	0.885	0.0025
	0.260	0.865	0.0015
8	0.333	1.055	0.0035
	0.323	1.035	0.0015

INSULATING WASHER
Item 6 thru 8



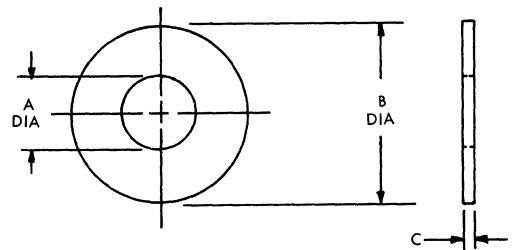
Item	A	B	C
9	0.340	0.270	0.072
	0.330	0.260	0.052
10	0.271	0.203	0.050
	0.251	0.191	0.035
11	0.405	0.333	0.072
	0.395	0.323	0.052
12	0.209	0.145	0.036
	0.199	0.135	0.026

INSULATING SLEEVE
Item 9 thru 12



Item	A	B	C	D	E	F
13	0.100	0.040	0.200	0.344	0.115	0.016 MAX
	0.080	0.020	0.190	0.280	0.111	
15	0.105	0.045	0.250	0.391	0.172	NA
	0.075	0.015	0.230	0.359	0.140	

INSULATING SHOULDER WASHER
Items 13 and 15



Item	A	B	C
16	0.150	0.285	0.014
	0.142	0.275	0.009
17	0.208	0.505	0.051
	0.198	0.495	0.041
18	0.276	0.635	0.069
	0.255	0.615	0.034
19	0.323	0.760	0.080
	0.302	0.740	0.051

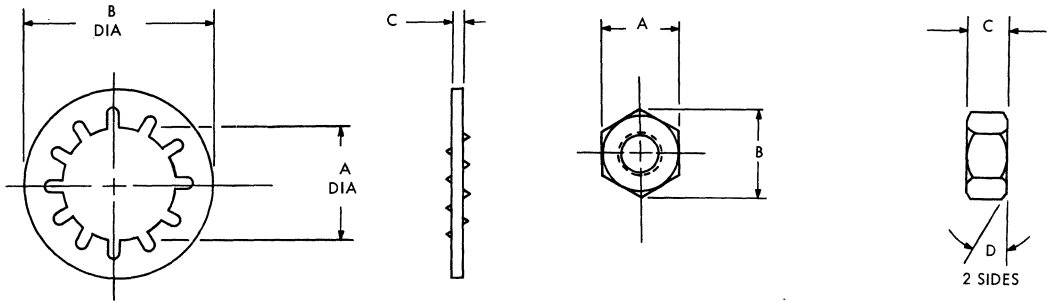
FLAT WASHER
Item 16 thru 19

† All dimensions are in inches unless otherwise specified.

5

STANDARD MOUNTING HARDWARE FOR POWER TRANSISTORS

SECTION B — MECHANICAL DRAWINGS OF HARDWARE ITEMS †



Item	A	B	C
20	0.204	0.381	0.025
	0.195	0.365	0.020
21	0.150	0.295	0.031
	0.142	0.275	0.015
22	0.267	0.478	0.027
	0.256	0.466	0.023
23	0.332	0.607	0.032
	0.320	0.594	0.028

INTERNAL TOOTH LOCK WASHER
Item 20 thru 23

Item	Thread	A	B	C	D
25	10-32	0.375	0.433	0.130	30°
	UNF-2B	0.362	0.413	0.117	
26	6-32	0.250	0.289	0.098	30°
	UNC-2B	0.241	0.275	0.087	
27	1/4-28	0.438	0.506	0.193	30°
	UNF-2B	0.423	0.488	0.178	
28	5/16-24	0.563	0.650	0.225	30°
	UNF-2B	0.545	0.629	0.208	

HEXAGONAL NUT
Item 25 thru 28

† All dimensions are in inches unless otherwise specified.

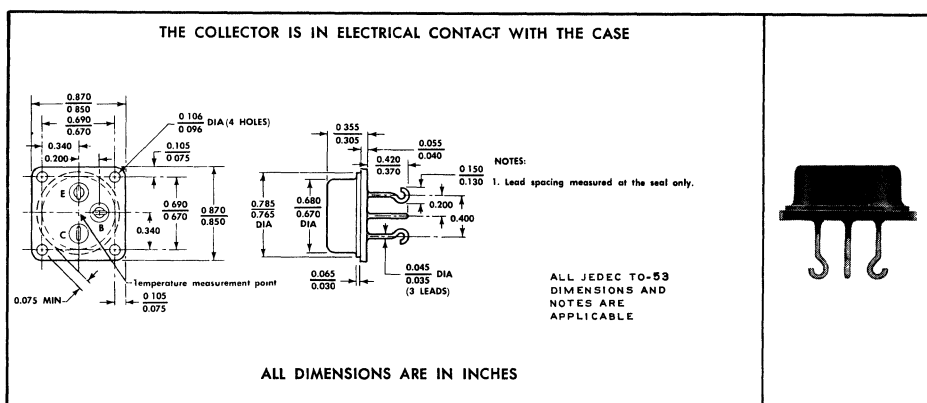
TYPES 2N389 and 2N424 N-P-N MESA SILICON POWER TRANSISTORS

TYPES 2N389, 2N424
BULLETIN NO. D.L.S. 65962, AUGUST 1958
REVISED SEPTEMBER 1965

85 watts at 25°C with infinite heat sink
Minimum beta of 8 at -55°C
-65°C to 200°C operating and storage range

mechanical data

The transistors are in hermetically-sealed welded packages.



5

maximum ratings

Collector voltage referred to emitter at 25°C (Breakdown voltages are indicated below)
Total dissipation at 25°C (case temperature)* 85 W
Total dissipation at 100°C (case temperature)* 45 W
Junction temperature (maximum range) -65°C to 200°C

* Derate 0.485 W/°C increase in case temperature within range of 25°C to 200°C

maximum and minimum design characteristics at T_c = 25°C (except as indicated)

PARAMETER	TEST CONDITIONS	2N389		2N424		UNIT
		MIN	MAX	MIN	MAX	
BV _{CEB} Breakdown Voltage	I _c = 10 mA, R _{BE} = 33 Ω	60		80		V
BV _{EBO} Breakdown Voltage	I _E = 10 mA, I _C = 0	10		10		V
I _{CEB} Collector Cutoff Current	V _{CE} = 60 V, R _{BE} = 33 Ω, T _C = 100°C		10		10	mA
V _{BE} Base-Emitter Voltage†	I _C = 1.5 A, V _{CE} = 15 V		8			V
	I _C = 0.75 A, V _{CE} = 15 V				8	
r _{CS} Saturation Resistance†	I _C = 1 A, I _B = 0.2 A		5		10	Ω
h _{FE} Transfer Ratio†	I _C = 1 A, V _{CE} = 15 V	12	60	12	60	
	I _C = 1 A, V _{CE} = 15 V, T _C = -55°C	8		8		

† This parameter must be measured using pulse techniques. PW = 300 μsec, Duty Cycle ≤ 2%.

TYPES 2N497, 2N498, 2N656, 2N657 N-P-N DIFFUSED JUNCTION SILICON TRANSISTORS

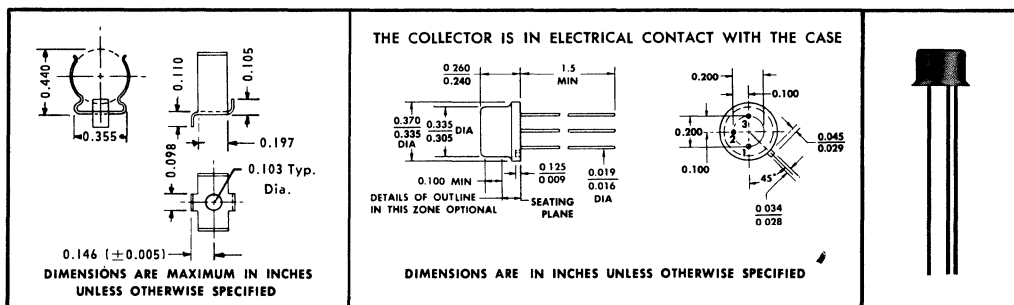
TYPES 2N497, 2N498, 2N656, 2N657
BULLETIN NO. DL-571945, AUGUST 1968
REVISED SEPTEMBER 1971

4 watts at 25°C with infinite heat sink
10-Ohm saturation resistance (typical)
-65°C to +200°C operating and storage range

mechanical data

The transistor is contained in a JEDEC TO-5 outline welded package with glass-to-metal hermetic seal between case and leads. Approximate weight is 1.0 gram.

The noninsulated mounting clip (TI P/N 10-31-052-007) is provided with each transistor. It is suitable for applications where thermal dissipation to a heat sink is desired. Material: beryllium copper, cadmium plated—gold irridated.



maximum ratings

Collector Voltage referred to base or emitter at 25°C (Breakdown voltages are indicated below)
Collector Dissipation at 25°C. (case temperature)* 4 W
Junction Temperature (maximum range) -65°C to +200°C

*Derate 22.8 mW/°C increase in case temperature within range of 25°C to 200°C

maximum and minimum design characteristics at T_j = 25°C

PARAMETER	TEST CONDITIONS	2N497		2N498		2N656		2N657		unit
		min.	max.	min.	max.	min.	max.	min.	max.	
BV _{CS0} Breakdown Voltage	I _c = 100 μA I _e = 0	60	100	60	100	60	100	60	100	V
BV _{CE0} Breakdown Voltage	I _c = 250 μA I _s = 0	60	100	60	100	60	100	60	100	V
BV _{ES0} Breakdown Voltage	I _E = 250 μA I _c = 0	8	8	8	8	8	8	8	8	V
I _{CS0} Collector Cutoff Current	V _{CB} = 30V I _e = 0		10		10		10		10	μA
h _{FE} Current Transfer Ratio†	V _{CE} = 10V I _c = 200mA	12	36	12	36	30	90	30	90	—
h _{IE} Input Impedance‡	V _{CE} = 10V I _s = 8mA		500		500		500		500	ohm
R _{CS} Saturation Resistance‡	I _c = 200 mA I _s = 40mA		25		25		25		25	ohm

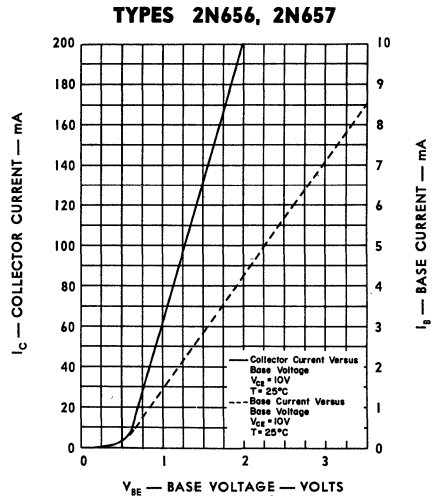
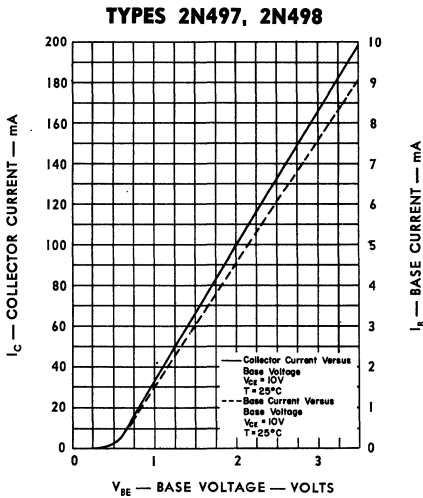
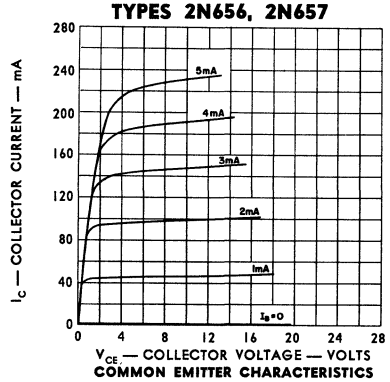
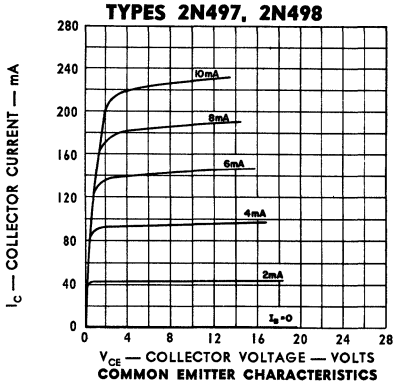
† Semiautomatic testing is facilitated by using pulse techniques to measure these parameters. A 300-microsecond pulse (approximately 2% duty cycle) is utilized. Thus, the unit can be tested under maximum current conditions without a significant increase in junction temperature, even though no heat sink is used. The parameter values obtained in this manner are particularly pertinent for switching circuit design and, in general, indicate the true capabilities of the device.



TYPES 2N497, 2N498, 2N656, 2N657

N-P-N DIFFUSED JUNCTION SILICON TRANSISTORS

TYPICAL CHARACTERISTICS (AS INDICATED)



typical design characteristics at $T_j = 25^\circ C$

PARAMETER	TEST CONDITIONS	2N497-98	2N656-57	unit
h_{ie} Input Impedance @ 1kc	$V_C = 30V$ $I_C = 30$ mA	250	350	ohm
h_{fe} Forward Current Gain @ 1kc	$V_C = 30V$ $I_C = 30$ mA	30	60	—
h_{re} Reverse Voltage Gain @ 1kc	$V_C = 30V$ $I_C = 30$ mA	200	400	—
h_{oe} Output Admittance @ 1kc	$V_C = 30V$ $I_C = 30$ mA	70	90	μ mho
h_{fc} Forward Current Gain @ 2 megacycles	$V_C = 30V$ $I_C = 30$ mA	9	6	—
I_{E0} Emitter Cutoff Current	$V_{EB} = 5V$ $I_C = 0$	0.1	0.1	μA
I_{C0} Collector Cutoff Current @ 150°C	$V_{CB} = 30V$ $I_E = 0$	60	60	μA

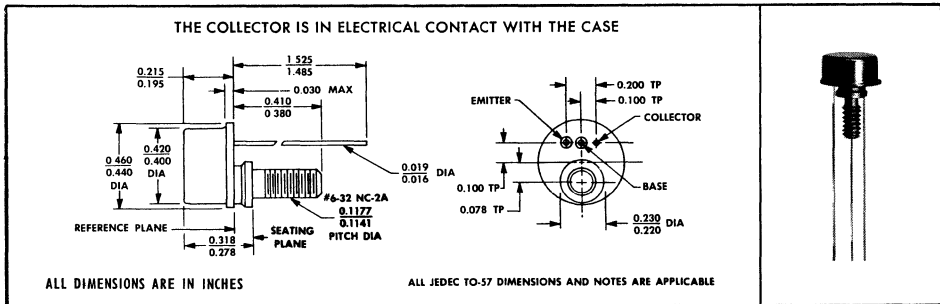
TYPES 2N1047 THRU 2N1050 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

 TYPES 2N1047 THRU 2N1050, 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B
 BULLETIN NO. DLS-6810610, DECEMBER 1968

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Dissipation Capability in excess of 22 W
at $V_{CE} = 40 \text{ V}$, $T_c = 100^\circ\text{C}$
- Typical $V_{CE(sat)}$ of 0.15 V at $I_c = 500 \text{ mA}$
- Typical f_T of 50 MHz at $V_{CE} = 10 \text{ V}$, $I_c = 100 \text{ mA}$

*mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N1047 2N1049	2N1048 2N1050	2N1047A 2N1049A	2N1048A 2N1050A	2N1047B 2N1049B	2N1048B 2N1050B	UNIT
Collector-Base Voltage	80*	120*	80*	120*	80*	120*	V
Collector-Emitter Voltage (See Note 1)	80	120	80*	120*	80*	120*	V
Emitter-Base Voltage	6*	6*	10*	10*	10*	10*	V
Continuous Collector Current	2† 0.5*		2† 0.5*		2† 0.75*		A
Peak Collector Current (See Note 2)	8		8		8		A
Continuous Base Current	0.5		0.5*		0.5*		A
Continuous Emitter Current	2		2		2† 0.75*		A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 10						
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	40*						W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	1*						W
Operating Collector Junction Temperature	200*						°C
Storage Temperature Range	-65 to 200*						°C
Lead Temperature 1/8 Inch from Case for 10 Sec.	230		230*		230*		°C

NOTES: 1. These values apply when the base-emitter diode is open-circuited.

2. This value applies for $I_p \leq 0.3 \text{ ms}$, duty cycle $\leq 10\%$.

3. Derate linearly to 200°C case temperature at the rate of 228 mW/deg.

4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/deg.

*Indicates JEDEC registered data

†Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

TYPES 2N1047 THRU 2N1050, 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N1047		2N1048		2N1049		2N1050		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80		120		80		120		V
* I_{CBO} Collector Cutoff Current	$V_{CB} = 30 \text{ V}$, $I_E = 0$ $V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	15		15		15		15		μA
* I_{CEV} Collector Cutoff Current	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$ $V_{CE} = 120 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	250		250		250		250		μA
* I_{EBO} Emitter Cutoff Current	$V_{EB} = 6 \text{ V}$, $I_C = 0$	250		250		250		250		μA
* h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6 $V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, $T_C = -55^\circ\text{C}$, See Notes 5 and 6	12	36	12	36	30	90	30	90	
* V_{BE} Base-Emitter Voltage	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	6		6		6		6		V
* $V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	7.5		7.5		7.5		7.5		V

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N1047A		2N1048A		2N1049A		2N1050A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80		120		80		120		V
I_{CBO} Collector Cutoff Current	$V_{CB} = 3 \text{ V}$, $I_E = 0$	15		15		15		15		μA
	$V_{CB} = 30 \text{ V}$, $I_E = 0$	15		15		15		15		
	$V_{CB} = 80 \text{ V}$, $I_E = 0$	350		350		350		350		
	$V_{CB} = 120 \text{ V}$, $I_E = 0$	350		350		350		350		
	$V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	350		350		350		350		
I_{CEV} Collector Cutoff Current	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	250		250		250		250		μA
	$V_{CE} = 120 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	250		250		250		250		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 3 \text{ V}$, $I_C = 0$	250		250		250		250		μA
	$V_{EB} = 10 \text{ V}$, $I_C = 0$	250		250		250		250		
$V_{EB(f1)}$ Emitter-Base Floating Potential	$V_{CB} = 80 \text{ V}$, $I_E = 0$	0.5		0.5		0.5		0.5		V
	$V_{CB} = 120 \text{ V}$, $I_E = 0$	0.5		0.5		0.5		0.5		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	12	36	12	36	30	90	30	90	
	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, $T_C = -55^\circ\text{C}$, See Notes 5 and 6	8		8		20		20		
V_{BE} Base-Emitter Voltage	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	6		6		6		6		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	7.5		7.5		7.5		7.5		V
f_{hfo} Common-Emitter Beta-Cutoff Frequency	$V_{CE} = 30 \text{ V}$, $I_C = 30 \text{ mA}$	75		75		75		75		kHz

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*Indicates JEDEC registered data

TYPES 2N1047 THRU 2N1050, 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N1047B		2N1048B		2N1049B		2N1050B		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_E = 0$, See Note 5	80*		120*		80*		120*		V
I_{CBO} Collector Cutoff Current	$V_{CB} = 3 \text{ V}$, $I_E = 0$	10* 5†		10* 5†		10* 5†		10* 5†		μA
	$V_{CB} = 30 \text{ V}$, $I_E = 0$	15*		15*		15*		15*		
	$V_{CB} = 80 \text{ V}$, $I_E = 0$	50*				50*				
	$V_{CB} = 120 \text{ V}$, $I_E = 0$			100* 50†				100* 50†		
	$V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	200*		200*		200*		200*		
I_{CEV} Collector Cutoff Current	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	250* 50†				250* 50†				μA
	$V_{CE} = 120 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			250* 50†				250* 50†		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 3 \text{ V}$, $I_C = 0$	10* 4†		10* 4†		10* 4†		10* 4†		μA
	$V_{EB} = 10 \text{ V}$, $I_C = 0$	10*		10*		10*		10*		
$V_{EB(f)}$ Emitter-Base Floating Potential	$V_{CB} = 80 \text{ V}$, $I_E = 0$	0.5*				0.5*				V
	$V_{CB} = 120 \text{ V}$, $I_E = 0$			0.5*				0.5*		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	12*	36*	12*	36*	30*	90*	30*	90*	
	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, $T_C = -55^\circ\text{C}$, See Notes 5 and 6	8*		8*		20*		20*		
V_{BE} Base-Emitter Voltage	$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	1.6*		1.6*		1.6*		1.6*		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	2*		2*		2*		2*		V
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$, $f = 12 \text{ MHz}$	1*		1*		1*		1*		
f_{htc} Common-Emitter Beta-Cutoff Frequency	$V_{CE} = 30 \text{ V}$, $I_C = 30 \text{ mA}$	125*		125*		125*		125*		kHz

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER	ALL TYPES	UNIT
	MAX	
θ_{J-C} Junction-to-Case Thermal Resistance	4.375	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	175	

*Indicates JEDEC registered data

†Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

TYPES 2N1047 THRU 2N1050, 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS‡	2N1049	2N1050	UNIT
		2N1049A	2N1050A	
		TYP		
t_{on} Turn-On Time	$I_C = 500 \text{ mA}$, $I_{B(1)} = 50 \text{ mA}$, $I_{B(2)} = -50 \text{ mA}$,	0.225		μs
t_{off} Turn-Off Time	$V_{BE(off)} = -4.1 \text{ V}$, $R_L = 100 \Omega$, See Figure 1	3		

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

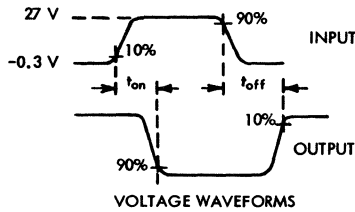
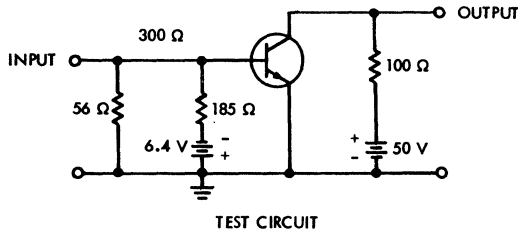


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_m \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive type.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPES 2N1047 THRU 2N1050 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

2N1047, 2N1047A, 2N1047B
2N1048, 2N1048A, 2N1048B

2N1049, 2N1049A, 2N1049B
2N1050, 2N1050A, 2N1050B

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

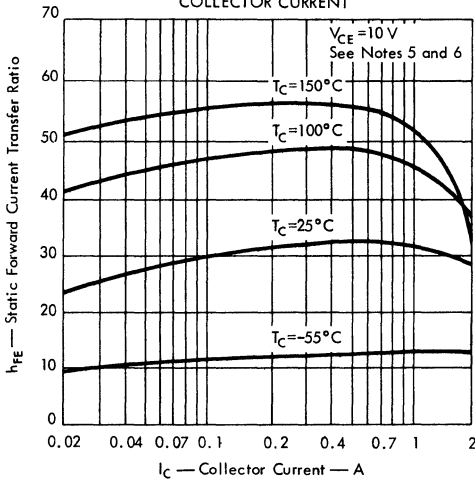


FIGURE 2

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

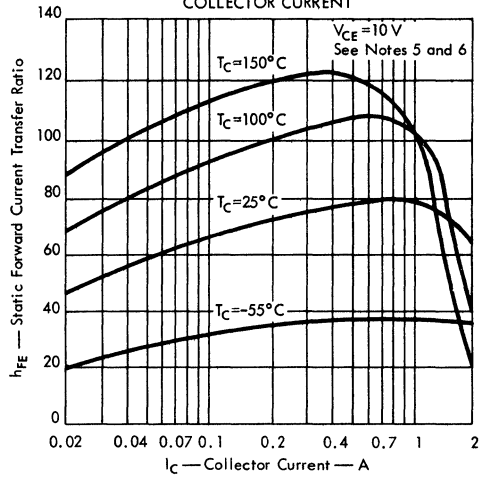


FIGURE 3

BASE-EMITTER VOLTAGE
vs
CASE TEMPERATURE

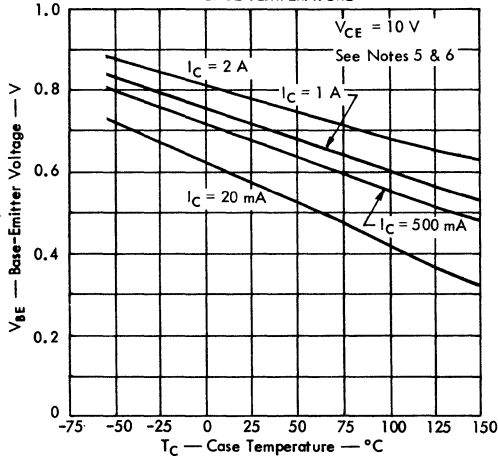


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE

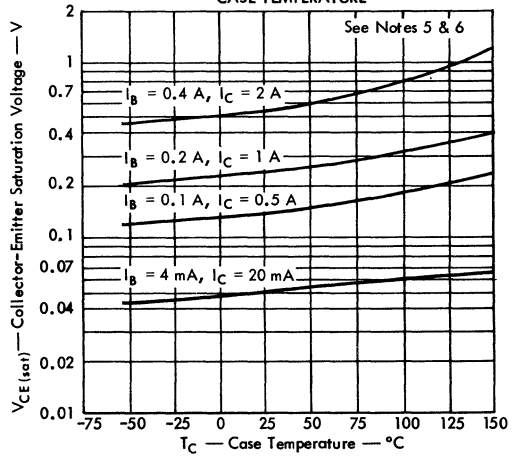


FIGURE 5

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

5

TYPES 2N1047 THRU 2N1050, 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

NORMALIZED COLLECTOR-EMITTER BREAKDOWN VOLTAGE
vs
BASE-EMITTER RESISTANCE

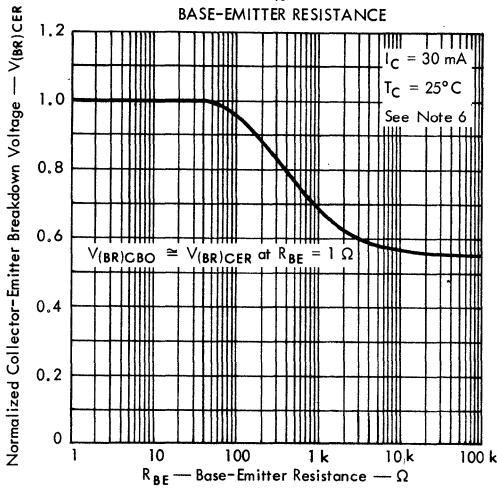


FIGURE 6

COMMON-BASE OPEN-CIRCUIT
INPUT AND OUTPUT CAPACITANCE
vs
REVERSE BIAS VOLTAGE

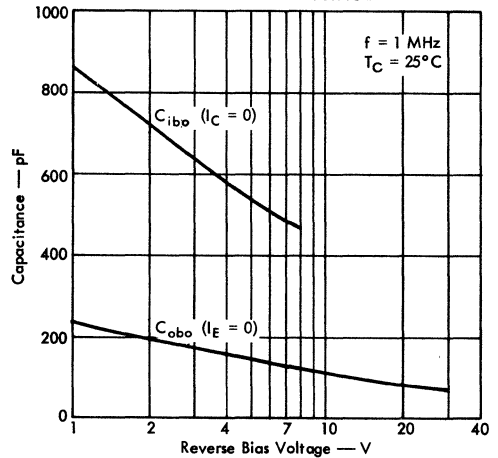


FIGURE 7

2N1047, 2N1047A, 2N1047B
2N1048, 2N1048A, 2N1048B
SMALL-SIGNAL COMMON-EMITTER
FORWARD CURRENT TRANSFER RATIO
vs
FREQUENCY

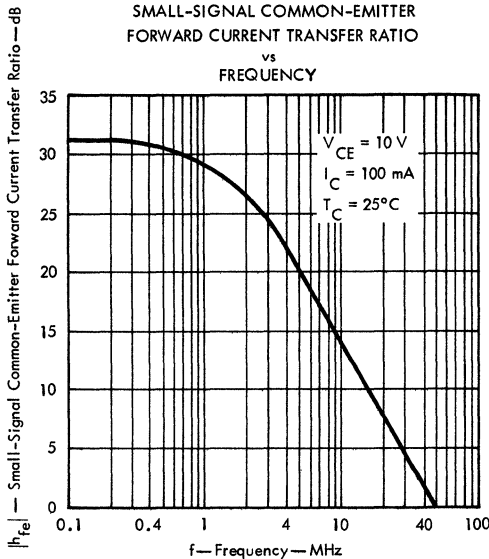


FIGURE 8

2N1049, 2N1049A, 2N1049B
2N1050, 2N1050A, 2N1050B
SMALL-SIGNAL COMMON-EMITTER
FORWARD CURRENT TRANSFER RATIO
vs
FREQUENCY

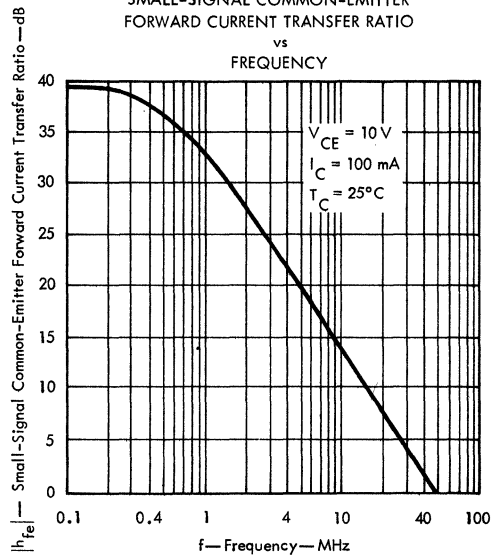


FIGURE 9

TYPES 2N1047 THRU 2N1050, 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGION

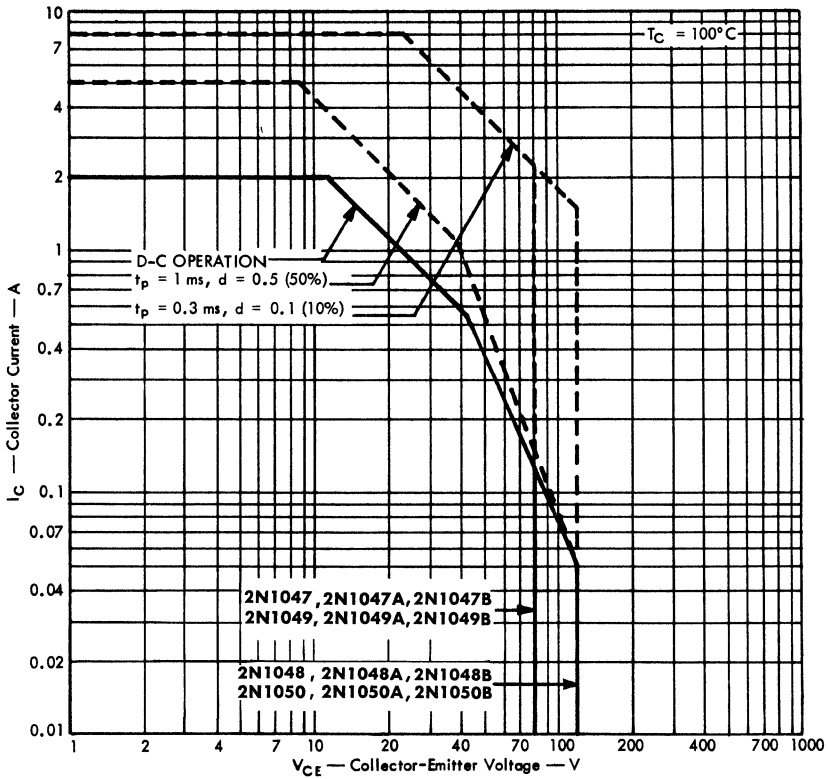


FIGURE 10

5

TYPES 2N1047 THRU 2N1050, 2N1047A THRU 2N1050A, 2N1047B THRU 2N1050B N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

5 THERMAL INFORMATION

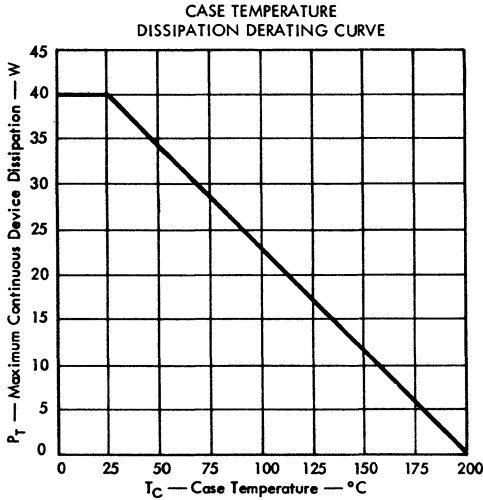


FIGURE 11

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	4.375	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	171	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 12	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 4 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

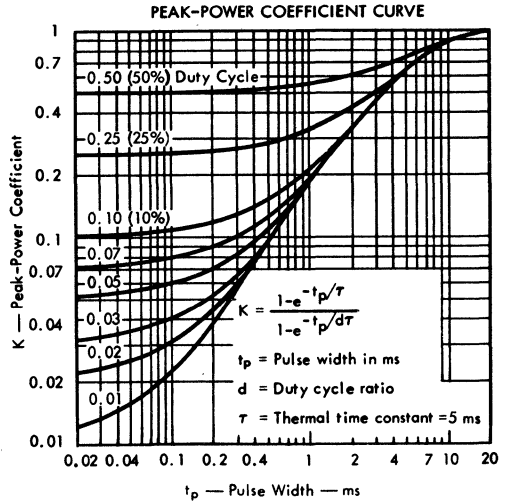


FIGURE 12

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C}, \text{ as in figure 11}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 12, Peak-Power Coefficient

$$K = 0.11 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(4) + (0.11) 4.375} = 170 \text{ W}$$

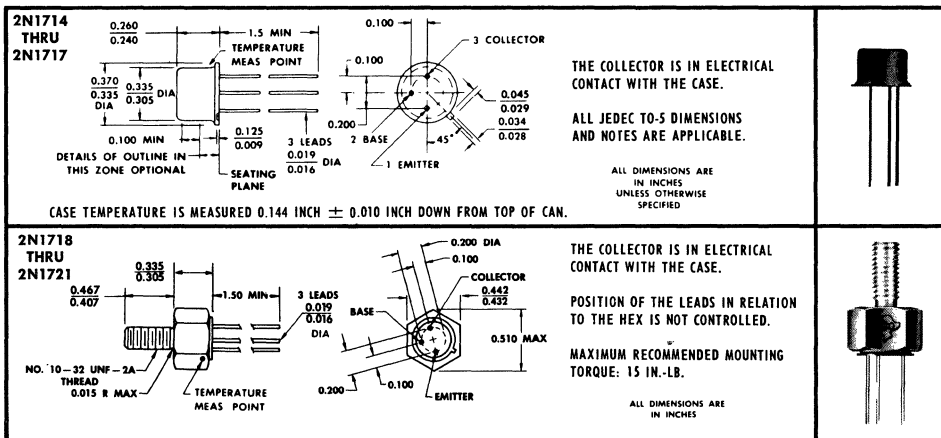
TYPES 2N1714 THRU 2N1721 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPES 2N1714 THRU 2N1721
BULLETIN NO. DL-5 6810483, NOVEMBER 1968

HIGH-FREQUENCY INTERMEDIATE-POWER TRANSISTORS

- 15 Watts at 100°C Case Temperature
- Typ $V_{CE(sat)}$ of 0.2 V at 200 mA
- Typ V_{BE} of 0.8 V at 200 mA
- Typ f_T of 50 MHz at 10 V, 100 mA

***mechanical data**



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N1714 2N1716	2N1715 2N1717	2N1718 2N1720	2N1719 2N1721
Collector-Base Voltage	90 V*	150 V*	90 V*	150 V*
Collector-Emitter Voltage (See Note 1)	60 V*	100 V*	60 V*	100 V*
Emitter-Base Voltage	← 6 V* →			
Continuous Collector Current	← { 1 A† } →			
Peak Collector Current (See Note 2)	← { 0.75 A* } →			
Continuous Emitter Current	← { 1.5 A† } →			
Safe Operating Region at (or below) 100°C Case Temperature	← { 1 A* } →			
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← { 1A† } →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← { 0.75 A* } →			
Operating Collector Junction Temperature	← See Figure 10 →			
Storage Temperature Range	← { 15 W† } →			
	← { 10 W* } →			
	← { 1 W† } →			
	← { 0.8 W* } →			
	← { 200°C† } →			
	← { 175°C* } →			
	← -65°C to 200°C* →			

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. For operation above 100°C case temperature refer to Dissipation Derating Curve, figure 13.
 4. For operation above 25°C free-air temperature refer to Dissipation Derating Curves, figures 11 and 12.

*Indicates JEDEC registered data
 †Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

5

TYPES 2N1714 THRU 2N1721

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N1714	2N1715	2N1716	2N1717	UNIT		
		2N1718	2N1719	2N1720	2N1721			
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	60	100	60	100		V	
I_{CBO} Collector Cutoff Current	$V_{CB} = 3 \text{ V}$, $I_E = 0$	1	1	1	1		μA	
I_{CEO} Collector Cutoff Current	$V_{CE} = 50 \text{ V}$, $I_B = 0$	50		50			μA	
	$V_{CE} = 90 \text{ V}$, $I_B = 0$		50		50			
I_{CES} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$	2	2	2	2		μA	
	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$	50		50				
	$V_{CE} = 150 \text{ V}$, $V_{BE} = 0$		50		50			
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$, $T_C = 170^\circ\text{C}$	500	500	500	500			
I_{EBO} Emitter Cutoff Current	$V_{EB} = 3 \text{ V}$, $I_C = 0$	10	10	10	10		μA	
	$V_{EB} = 6 \text{ V}$, $I_C = 0$	10	10	10	10			
$V_{EB(1)}$ Emitter-Base Floating Potential	$V_{CB} = 60 \text{ V}$, $I_E = 0$	1		1			V	
	$V_{CB} = 100 \text{ V}$, $I_E = 0$		2		2			
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 10 \text{ mA}$, See Note 5	10	10	20	20			
	$V_{CE} = 5 \text{ V}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6	20	60	20	60	40		120
	$V_{CE} = 5 \text{ V}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6 $T_C = -55^\circ\text{C}$	10	10	20	20			
V_{BE} Base-Emitter Voltage	$I_B = 20 \text{ mA}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6	1.6	1.6	1.6	1.6		V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 20 \text{ mA}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6	2	2	2	2		V	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$, $f = 16 \text{ MHz}$	1	1	1	1			
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	50	50	50	50		pF	

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	2N1714, 2N1715	2N1718, 2N1719	UNIT
	2N1716, 2N1717	2N1720, 2N1721	
		MAX	MAX
θ_{J-C} Junction-to-Case Thermal Resistance	6.67† 7.5*	6.67† 7.5*	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	175† 187.5*	75*	

* Indicates JEDEC registered data

† Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

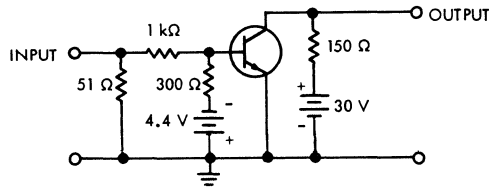
TYPES 2N1714 THRU 2N1721 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

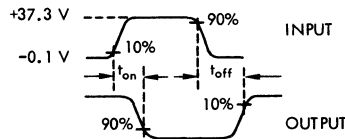
PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 200 \text{ mA}$, $I_{B(1)} = 20 \text{ mA}$, $I_{B(2)} = -20 \text{ mA}$,	0.14	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -3.4 \text{ V}$, $R_L = 150 \Omega$, See Figure 1	2.6	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPES 2N1714 THRU 2N1721

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

2N1714, 2N1715, 2N1718, 2N1719
 STATIC FORWARD CURRENT TRANSFER RATIO
 vs
 COLLECTOR CURRENT

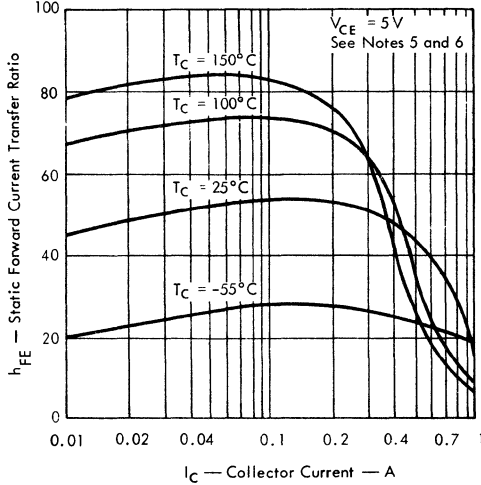


FIGURE 2

2N1716, 2N1717, 2N1720, 2N1721
 STATIC FORWARD CURRENT TRANSFER RATIO
 vs
 COLLECTOR CURRENT

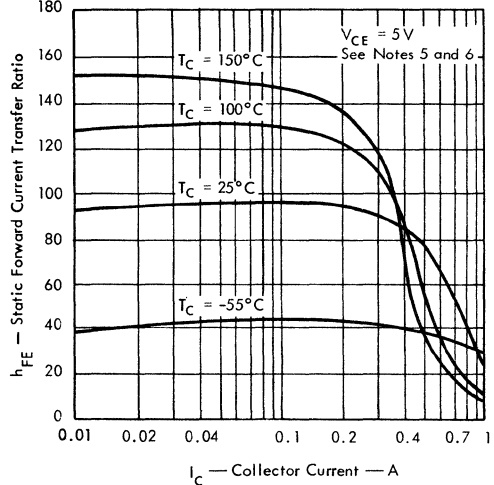


FIGURE 3

BASE-EMITTER VOLTAGE
 vs
 CASE TEMPERATURE

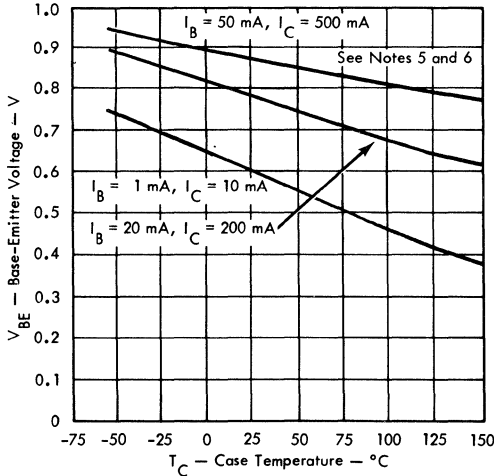


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE
 vs
 CASE TEMPERATURE

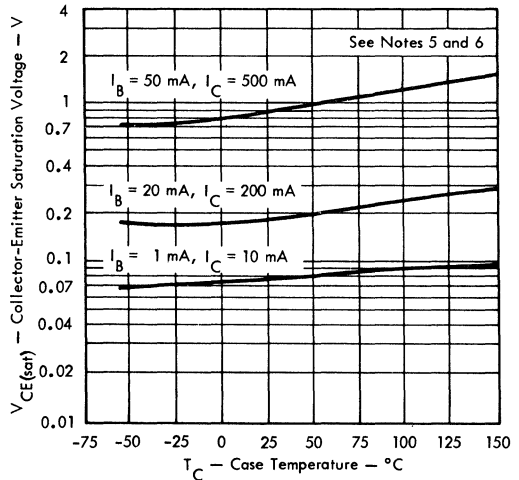


FIGURE 5

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

5

TYPES 2N1714 THRU 2N1721

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

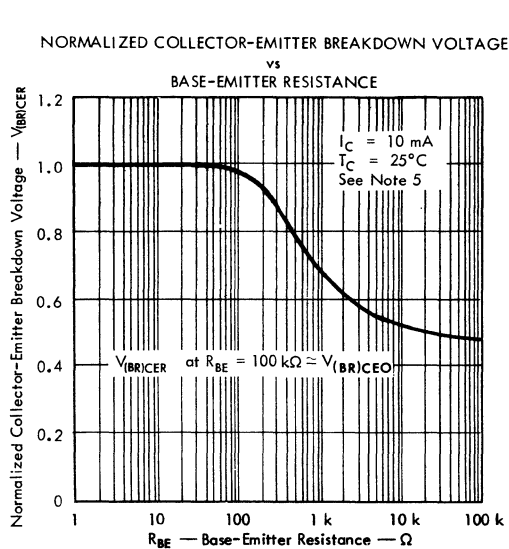


FIGURE 6

2N1714, 2N1715,
2N1718, 2N1719

SMALL-SIGNAL COMMON-EMITTER
FORWARD CURRENT TRANSFER RATIO

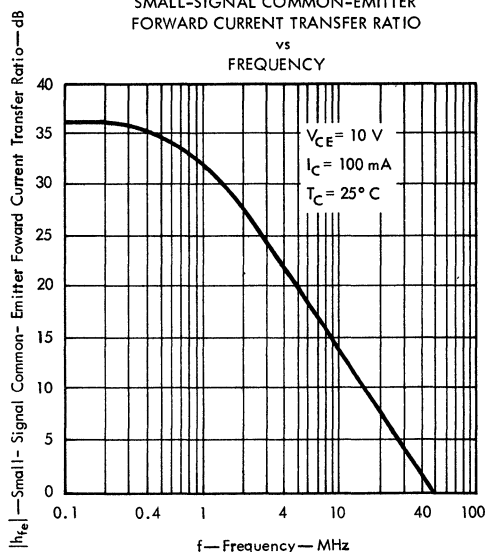


FIGURE 8

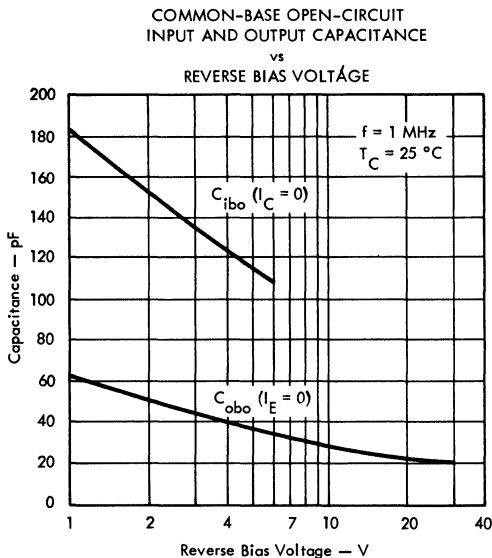


FIGURE 7

2N1716, 2N1717,
2N1720, 2N1721

SMALL-SIGNAL COMMON-EMITTER
FORWARD CURRENT TRANSFER RATIO

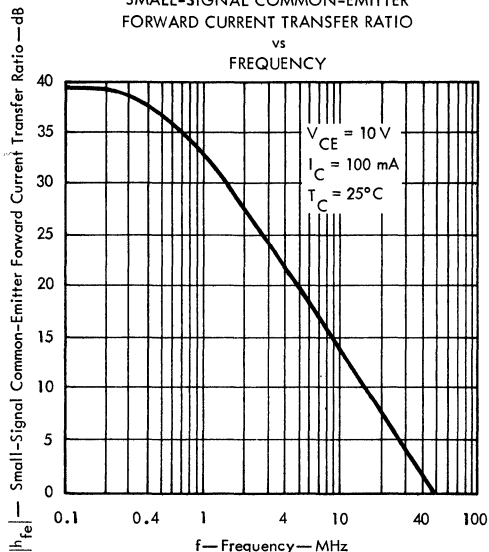


FIGURE 9

NOTE 5: This parameter must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

5

TYPES 2N1714 THRU 2N1721

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGION

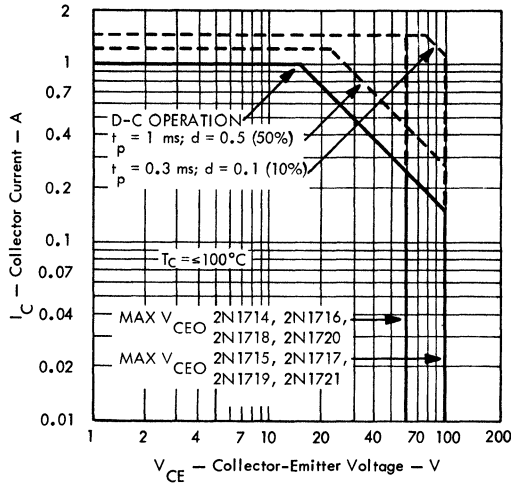


FIGURE 10

THERMAL INFORMATION

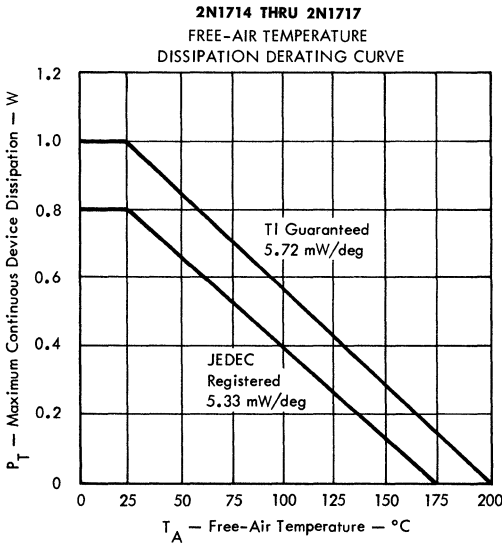


FIGURE 11

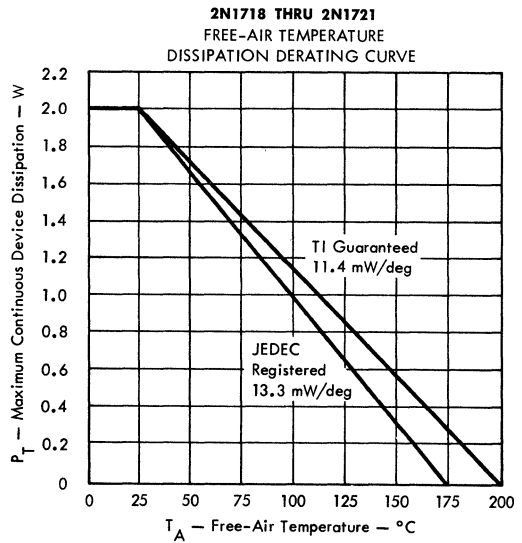


FIGURE 12

TYPES 2N1714 THRU 2N1721

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

THERMAL INFORMATION

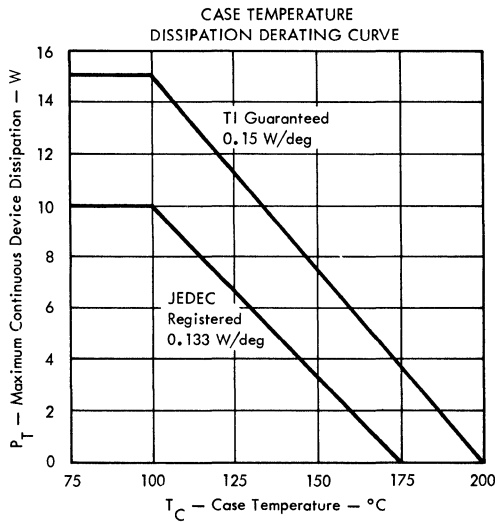


FIGURE 13

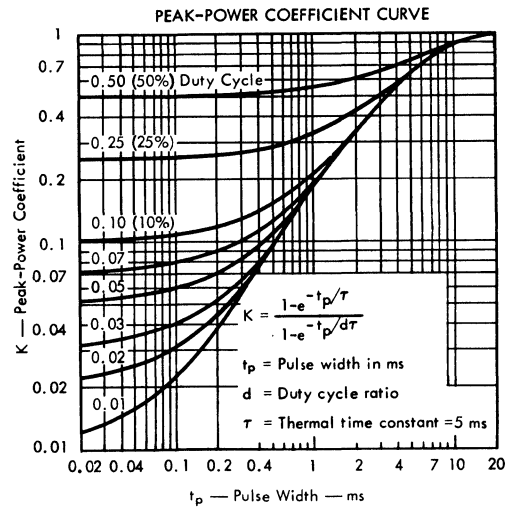


FIGURE 14

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE		UNIT
		2N1714 THRU 2N1717	2N1718 THRU 2N1721	
$P_{T(av)}$	Average Power Dissipation			W
$P_{T(max)}$	Peak Power Dissipation			W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	75	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	6.67	6.67	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168	68	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance			deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance			deg/W
T_A	Free-Air Temperature			°C
T_C	Case Temperature			°C
$T_{J(av)}$	Average Junction Temperature	≤ 200		°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200		°C
K	Peak-Power Coefficient	See Figure 14		
t_p	Pulse Width			ms
t_x	Pulse Period			ms
d	Duty-Cycle Ratio (t_p/t_x)			

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C-HS} + \theta_{HS-A} = 7$ deg/W (from information supplied with heat sink.)

$T_{J(av)}$ (design limit) = 200°C

$T_A = 50^\circ\text{C}$

$d = 10\%$ (0.1)

$t_p = 0.1$ ms

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \quad \text{for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C} \text{ as in Figure 13}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \quad \text{for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \quad \text{for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \quad \text{for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 14, Peak-Power Coefficient

$K = 0.11$ and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + 0.11(6.67)} = 105 \text{ W}$$

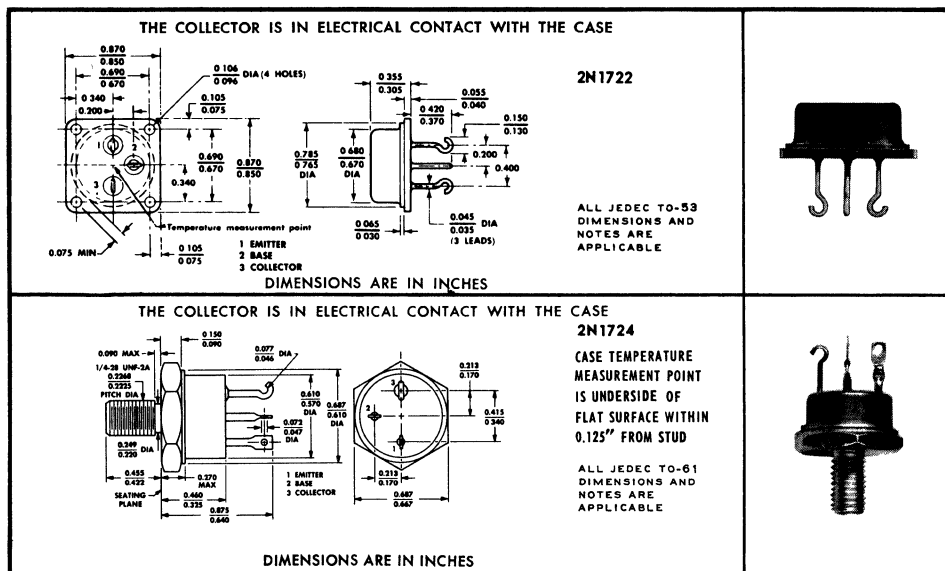
TYPES 2N1722, 2N1724 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS

- 50 Watts at 100°C Case Temperature
- Minimum f_T of 10 Megacycles
- Maximum R_{CS} of 0.5 Ohm at 2 Amperes I_C
- Maximum V_{BE} of 2 Volts at 2 Amperes I_C

mechanical data

TYPES 2N1722, 2N1724
BULLETIN NO. DL-S-691315, APRIL 1961
REVISED DECEMBER 1969



absolute maximum ratings at 25°C ambient temperature (unless otherwise noted)

Collector-Emitter Voltage (See Note 1)	80 v
Emitter-Base Voltage	10 v
Collector Current, Continuous	5 a
Collector Current, Peak (See Note 2)	7.5 a
Total Device Dissipation at 100°C Case Temperature (See Note 3)	50 w
Total Device Dissipation at 25°C Ambient Temperature (See Note 4)	3 w
Collector Junction Operating Temperature	+ 175°C
Storage Temperature Range	- 65°C to + 200°C

- Note 1** This is the voltage at which $|h_{FE}|$ approaches one when the emitter-base diode is open-circuited. Maximum allowable collector-emitter voltage shall be derated with increasing collector current as shown in the maximum V_{CE} curve which appears with the collector characteristics. Average power dissipation shall not exceed the maximum ratings for this device.
- Note 2** Maximum peak collector current may be allowed if maximum junction temperature is not exceeded. See Figure 2, "Junction Temperature Response vs Pulse Width and Duty Cycle."
- Note 3** Derate linearly to 175°C case temperature at the rate of 0.67 w/C°.
- Note 4** Derate linearly to 175°C ambient temperature at the rate of 20 mw/C°.
- Note 5** For correct measurement of I_{CES} , the base must be shorted to the emitter. The current meter must not be placed in the base-emitter short-circuit loop. I_{CES} may be used in place of I_{CBO} for circuit-stability calculations.
- Note 6** For typical BV_{CER} at finite values of R_{BE} , refer to BV_{CER} vs R_{BE} curve. Peak collector-emitter voltage of 120 v may be allowed in the cutoff-current region if the emitter-base diode is short-circuited.
- Note 7** Heat-sinking sufficient to limit case temperature to 40°C or less over a 10-second measurement period must be used for this test.
- Note 8** DC collector current should not be applied longer than 5 seconds to maintain case temperature less than 40°C without a heat sink.
- Note 9** To obtain f_T , the $|h_{fe}|$ response with frequency is extrapolated at 6 db/octave to $|h_{fe}| = 1$ from $f = 10$ mc. The product of $f_T \times 1$ has been referred to as the gain-bandwidth product.

TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

electrical characteristics at 25°C ambient temperature (unless otherwise noted)

Parameter	Test Conditions	Min	Max	Unit
I_{CES} Collector Reverse Current	$V_{CE} = 60 \text{ v}, V_{BE} = 0$ (See note 5)		1	ma
I_{CES} Collector Reverse Current	$V_{CE} = 60 \text{ v}, V_{BE} = 0,$ $T_C = +150^\circ\text{C}$ (See note 5)		2	ma
I_{CES} Collector Reverse Current	$V_{CE} = 120 \text{ v}, V_{BE} = 0,$ $T_C = +150^\circ\text{C}$ (See note 5)		10	ma
I_{EBO} Emitter Reverse Current	$V_{EB} = 10 \text{ v}, I_C = 0$		10	ma
* BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ ma}, I_B = 0$ (See notes 6 & 7)	80		v
* h_{FE} DC Forward Current Transfer Ratio	$V_{CE} = 15 \text{ v}, I_C = 2 \text{ a}$	20	90	
* h_{FE} DC Forward Current Transfer Ratio	$V_{CE} = 15 \text{ v}, I_C = 2 \text{ a},$ $T_A = -55^\circ\text{C}$	12		
* h_{FE} DC Forward Current Transfer Ratio	$V_{CE} = 15 \text{ v}, I_C = 100 \text{ ma}$	20		
* V_{BE} Base-Emitter Voltage	$I_B = 200 \text{ ma}, I_C = 2 \text{ a}$		2.0	v
* $V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 200 \text{ ma}, I_C = 2 \text{ a}$		1.0	v
$ h_{fe} $ AC Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 15 \text{ v}, I_C = 500 \text{ ma},$ $f = 10 \text{ mc}$ (See note 8)	1.0		
C_{ob} Common-Base Output Capacitance	$V_{CB} = 15 \text{ v}, I_E = 0, f = 1 \text{ mc}$		550	pf

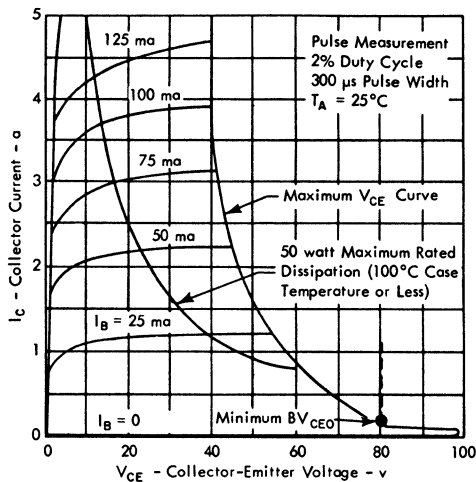
thermal characteristics

θ_{J-C} Thermal Resistance, Junction to Case (Bottom, Center of Case)	1.5	$^\circ\text{C}/\text{w}$
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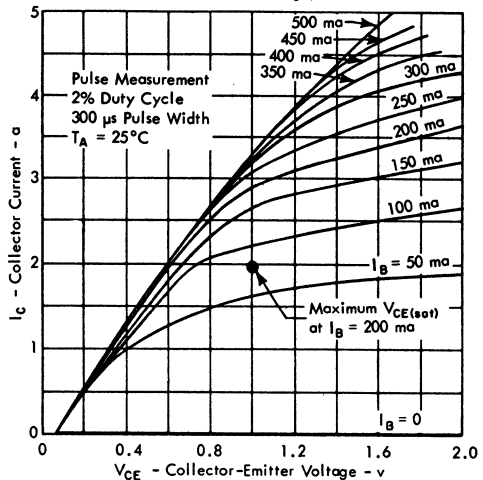
*Semi-automatic testing is facilitated by using pulse techniques to measure these parameters. A 300 μsec pulse (approximately 2% duty cycle) is utilized.

TYPICAL CHARACTERISTICS

COMMON-EMITTER COLLECTOR CHARACTERISTICS

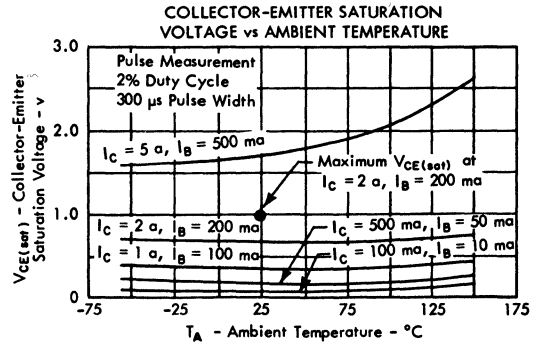
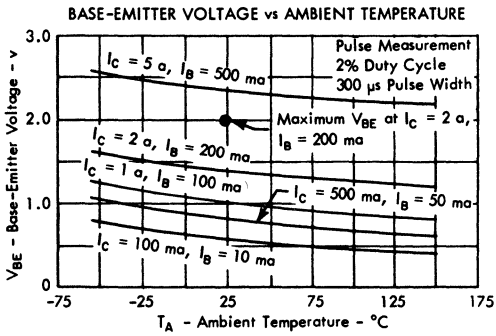
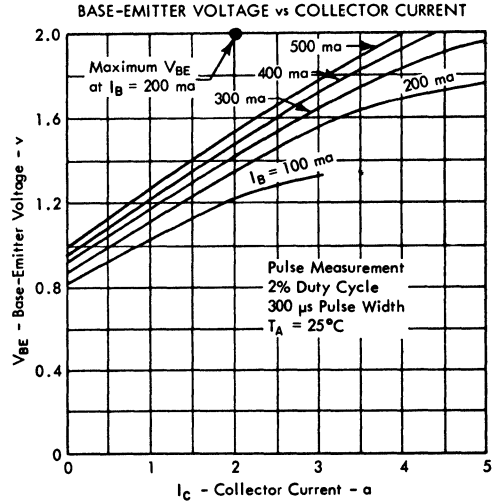
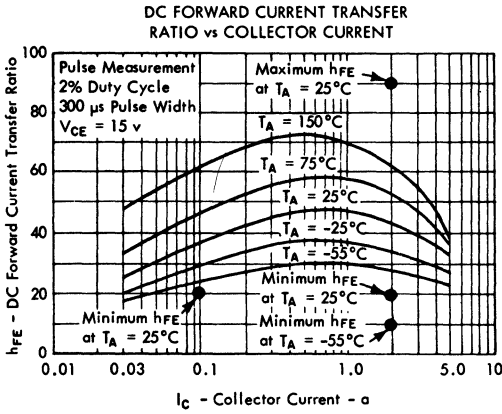


COMMON-EMITTER COLLECTOR CHARACTERISTICS (Low - Voltage)



TYPES 2N1722, 2N1724 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL CHARACTERISTICS

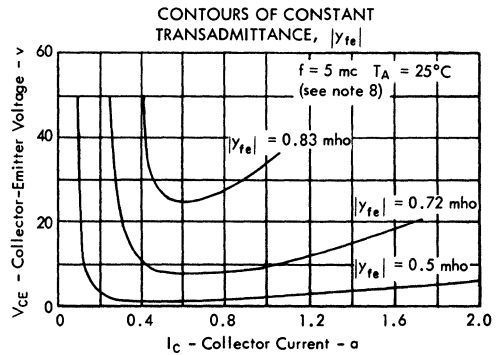
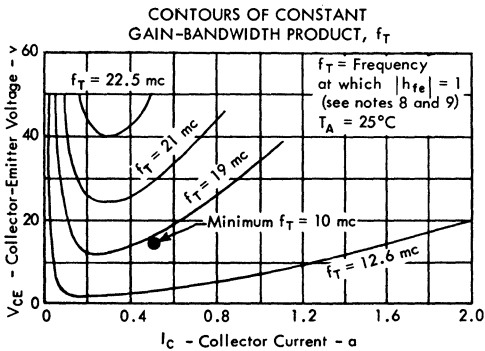
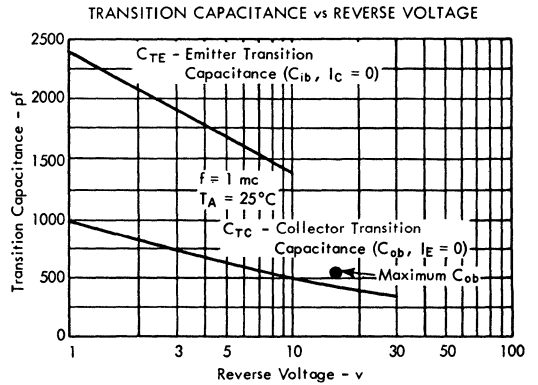
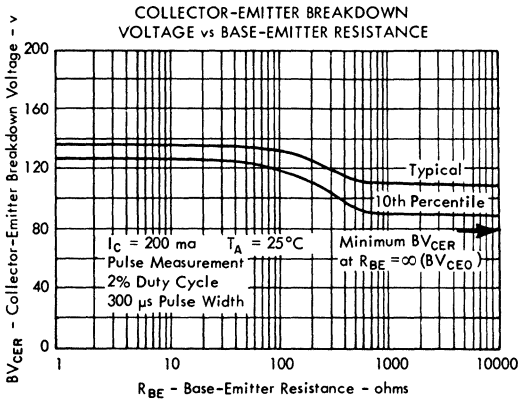


TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

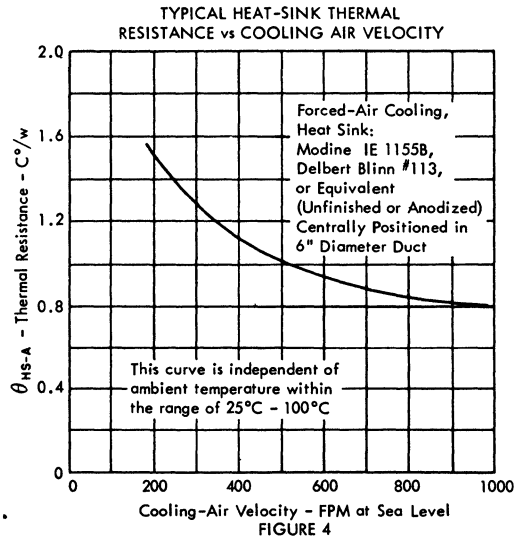
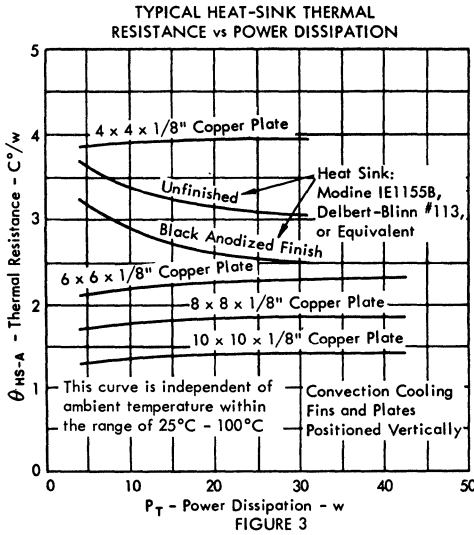
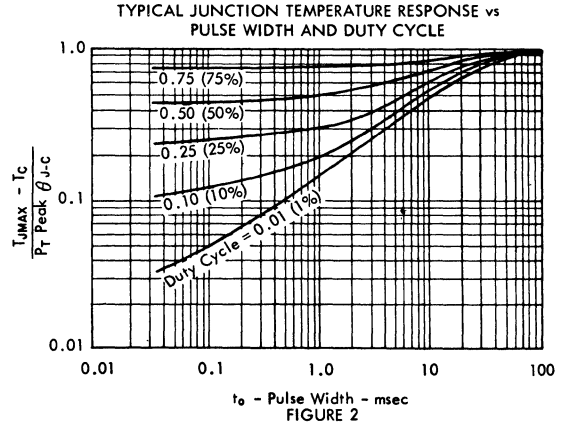
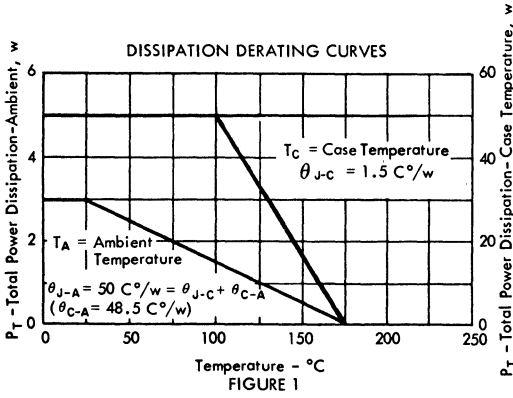
TYPICAL CHARACTERISTICS

5



TYPES 2N1722, 2N1724 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

THERMAL INFORMATION



5

TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

THERMAL INFORMATION

TABLE I

Mounting Conditions	2N1722 mounted with four 2-56 screws at 4 in-lb torque 2N1724 mounted at 30 in.-lb. torque			
	Unfinished Alum. or Copper	Alum. or Copper with .0025" mica ins.	Anodized Aluminum	Anodized Alum. with DC-200 Oil
θ_{C-HS} - contact thermal resistance $^{\circ}\text{C}/\text{w}$	0.15	0.45	0.40	0.28

Symbol	Definition	Unit
P_T	DC or average total power dissipation	w
$P_{T\text{peak}}$	Peak total power dissipation (pulsed operation)	w
θ_{HS-A}	Heat-sink-to-ambient thermal resistance	$^{\circ}\text{C}/\text{w}$
θ_{C-HS}	Case-to-heat-sink (contact) thermal resistance	$^{\circ}\text{C}/\text{w}$
θ_{J-C}	Junction-to-case thermal resistance	$^{\circ}\text{C}/\text{w}$
θ_{J-A}	Junction-to-ambient thermal resistance (no heat sink)	$^{\circ}\text{C}/\text{w}$
θ_{C-A}	Case-to-ambient thermal resistance (no heat sink)	$^{\circ}\text{C}/\text{w}$
T_A	Ambient temperature	$^{\circ}\text{C}$
T_{HS}	Heat-sink mounting surface temperature	$^{\circ}\text{C}$
T_C	Case temperature (transistor mounting surface)	$^{\circ}\text{C}$
$T_{J\text{max}}$	Maximum junction temperature	$^{\circ}\text{C}$
t_o	Pulse width	msec

$$T_{J\text{max}} = T_A + P_{T\text{peak}} \times \text{duty cycle} \times \theta_{C-A} + \left[\frac{T_{J\text{max}} - T_C}{P_{T\text{peak}} \theta_{J-C}} \right] P_{T\text{peak}} \theta_{J-C}$$

Note that the ambient-to-transistor case temperature rise remains constant at a value proportional to average power dissipation throughout the pulse width and duty cycle range shown in Figure 2. Values for θ_{HS-A} taken from Figures 3 and 4 are used in the example problems. However, the curves in Figures 1 and 2 may be used for any heat sink provided its thermal resistance is known. Under no circumstances should peak power dissipation exceed the value indicated by the maximum V_{CE} curve on the collector characteristics.

Example 1, Find $T_{J\text{max}}$

Operating Conditions

Heat sink = Modine IE11558, Delbert Blinn 113, or equivalent, anodized finish, convection cooling

$t_o = 1$ msec

duty cycle = 0.10 (10%)

$P_{T\text{peak}} = 50$ w

$T_A = 50^{\circ}\text{C}$

$$T_{J\text{max}} = T_A + P_{T\text{peak}} \times \text{duty cycle} \times (\theta_{C-HS} + \theta_{HS-A}) + \left[\frac{T_{J\text{max}} - T_C}{P_{T\text{peak}} \theta_{J-C}} \right] P_{T\text{peak}} \theta_{J-C}$$

From Figure 1, $\theta_{J-C} = 1.5^{\circ}\text{C}/\text{w}$

From Figure 3, $\theta_{HS-A} = 3.15^{\circ}\text{C}/\text{w}$ ($P_T = P_{T\text{peak}} \times \text{duty cycle}$)

From Table 1, $\theta_{C-HS} = 0.40^{\circ}\text{C}/\text{w}$

$$\text{From Figure 2, } \left[\frac{T_{J\text{max}} - T_C}{P_{T\text{peak}} \theta_{J-C}} \right] = 0.20$$

then

$$\begin{aligned} T_{J\text{max}} &= 50^{\circ}\text{C} + 50\text{w} \times 0.10 \times (3.15 + 0.40)^{\circ}\text{C}/\text{w} + 0.20 \times 50\text{w} \times 1.5^{\circ}\text{C}/\text{w} \\ &= 50 + 17.7 + 15 \\ &= 82.7^{\circ}\text{C} \end{aligned}$$

Example 2, Find $P_{T\text{peak}}$

Operating Conditions

heat sink = none

$t_o = 10$ msec

duty cycle = 0.01 (1%)

$T_{J\text{max}}$ (design limit) = 175°C

$T_A = 25^{\circ}\text{C}$

$$T_{J\text{max}} = T_A + P_{T\text{peak}} \times \text{duty cycle} \times \theta_{C-A} + \left[\frac{T_{J\text{max}} - T_C}{P_{T\text{peak}} \theta_{J-C}} \right] P_{T\text{peak}} \theta_{J-C}$$

From Figure 1, $\theta_{C-A} = 48.5^{\circ}\text{C}/\text{w}$

From Figure 1, $\theta_{J-C} = 1.5^{\circ}\text{C}/\text{w}$

$$\text{From Figure 2, } \left[\frac{T_{J\text{max}} - T_C}{P_{T\text{peak}} \theta_{J-C}} \right] = 0.50$$

then

$$\begin{aligned} 175^{\circ}\text{C} &= 25^{\circ}\text{C} + P_{T\text{peak}} \times 0.01 \times 48.5^{\circ}\text{C}/\text{w} + 0.50 \times P_{T\text{peak}} \times 1.5^{\circ}\text{C}/\text{w} \\ P_{T\text{peak}} &= \frac{150}{0.485 + 0.75} \approx 121 \text{ watts} \end{aligned}$$

For steady-state power dissipation or pulsed dissipation with $t_o < 100$ μsec , maximum junction temperature may be considered equal to the ambient temperature plus the product of average power dissipation and total junction-to-ambient thermal resistance. Under these pulse conditions, the junction-to-case temperature gradient varies so slightly with instantaneous power dissipation that average dissipation may be used in thermal calculations. When a heat sink is used, junction-to-ambient thermal resistance may be broken down into three quantities: θ_{J-C} , θ_{C-HS} , and θ_{HS-A} . Thermal performance can then be calculated using the following equation:

$$T_{J\text{max}} = T_A + P_T(\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A})$$

Or, if no heat sink is used,

$$T_{J\text{max}} = T_A + P_T \theta_{J-A}$$

θ_{J-C} , θ_{J-A} , and θ_{C-A} are shown in Figure 1. To minimize contact thermal resistance, θ_{C-HS} , the heat sink mounting surface should be as smooth as possible. θ_{C-HS} for several surface and mounting conditions is given in Table 1. These figures represent maximum values encountered on surfaces equivalent to those of most commercially available heat sinks. Note that in some cases, as with the anodized aluminum finish, θ_{C-HS} can be reduced substantially by the application of a film of silicone grease between transistor and heat sink.

As t_o exceeds 100 μsec during pulsed operation, the instantaneous variation of the junction-to-case temperature gradient increases sharply. Therefore, maximum rather than average junction temperature must be considered. Figure 2 shows the ratio of maximum instantaneous case-to-junction temperature rise at any pulse width and duty cycle to the rise which would occur at 100% duty cycle. Use of this curve is best explained by the equations below and by the example problems. Provided the other operating conditions are known, $T_{J\text{max}}$ or $P_{T\text{peak}}$ may be found using the relation

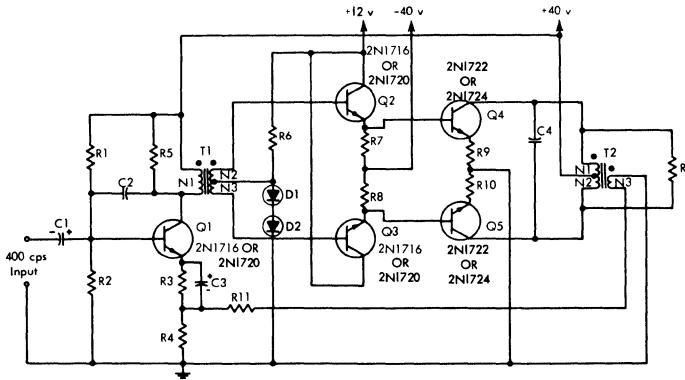
$$T_{J\text{max}} = T_A + P_{T\text{peak}} \times \text{duty cycle} \times (\theta_{C-HS} + \theta_{HS-A}) + \left[\frac{T_{J\text{max}} - T_C}{P_{T\text{peak}} \theta_{J-C}} \right] P_{T\text{peak}} \theta_{J-C}$$

Or, if no heat sink is used,

TYPES 2N1722, 2N1724 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL APPLICATION DATA, $T_A = -55^\circ\text{C}$ TO 125°C

35 watt, 400 cps SERVO AMPLIFIER



Circuit Characteristics at 35 w

Power Output:

Power Gain - 45 db min.

Voltage Amplification -

36.5 \pm 1.5 db

Circuit Input Resistance - 700 Ω

min.

Total Harmonic Distortion - 5%

R_L - 68, 35 w
R1 - 4.32 K, 1/2 w
R2 - 3.32 K, 1/2 w
R3 - 1.00 K, 1 w
R4 - 33.2, 1/2 w

R5 - 2.21 K, 1/2 w
R6 - 390, 1/2 w
R7 & R8 - 2.00 K, 1 w
R9 & R10 - 1.00, 2 w
R11 - 1.00 K, 1/2 w

C1 - 40 μf , 25 v
C2 - 500 pf, 100 v
C3 - 1000 μf , 25 v
C4 - 2.0 μf , 100 v
D1 & D2 - TI 1N538
Q1, Q2, & Q3 - TI 2N1716
OR TI 2N1720
Q4 & Q5 - TI 2N1722
OR TI 2N1724

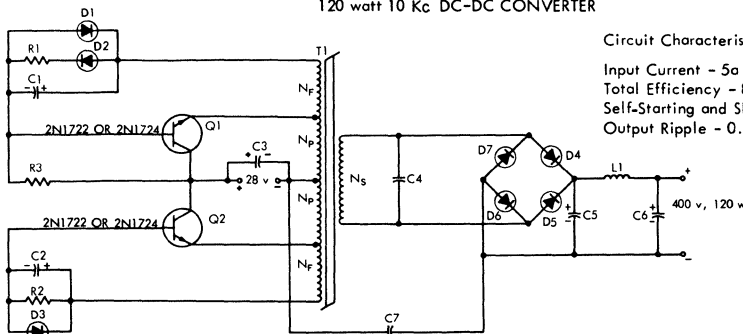
T1: N1 = 755 T, #30 AWG; N2 = N3 = 330 T, #28 AWG Bifilar Wound.

Core - Magnetic Metals 75E1 SL14 or equivalent - 1 x 1 interleaved.

T2: N1 = N2 = 100 T, #20 AWG Bifilar Wound; N3 = 67 T, #28 AWG. Core - Magnetic Metals 100 E1 SL14 or equivalent - Butt Joint.

- NOTES:
1. All Resistance Values in ohms - 5% Tolerance
 2. Resistor Wattage Ratings at 125°C Ambient
 3. Capacitor Voltage Ratings at 125°C Ambient
 4. Q1 on Heat Sink with $\theta_{C-HS} + \theta_{HS-A} \leq 40^\circ\text{C}/\text{w}$
 5. Q2 and Q3 on same Heat Sink. $\theta_{C-HS} + \theta_{HS-A} \leq 40^\circ\text{C}/\text{w}$ each. h_{FE} 's matched within 10%.
 6. Q4 and Q5 on Heat Sinks with $\theta_{C-HS} + \theta_{HS-A} \leq 1.5^\circ\text{C}/\text{w}$. h_{FE} 's matched within 10%.

120 watt 10 Kc DC-DC CONVERTER



Circuit Characteristics at 120 w Power Output:

Input Current - 5a

Total Efficiency - 85%

Self-Starting and Short-Circuit Protected

Output Ripple - 0.6 v max.

Q1 & Q2 - TI 2N1722
OR TI 2N1724
D1 - D3 - TI 1N645
D4 - D7 - TI 1N1096
C1 & C2 - 22 μf , 15 v
C3 - 100 μf , 35 v
C4 - 510 pf, 500 v

C5 - 0.1 μf , 500 v
C6 - 3 μf , 500 v
C7 - 0.01 μf , 500 v
L1 - 15 μH
R1 - 2.74, 2 w
R2 - 3.32, 2 w
R3 - 511, 2 w

T1: Np = 18 T #16 AWG
Ns = 290 T #25 AWG
Nf = 3 T #22 AWG
Core: Toroid, Magnetic Metals Inc. 51026-ID or equivalent.

- NOTES:
1. All Resistance Values in ohms, 5% Tolerance.
 2. All Resistor Wattage Ratings at 125°C Ambient.
 3. Capacitor Voltage Ratings at 125°C Ambient.
 4. Q1 and Q2 on Same Heat Sink, $\theta_{C-HS} + \theta_{HS-A} \leq 4^\circ\text{C}/\text{w}$ each.

TYPES 2N1722, 2N1724 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL APPLICATION DATA, $T_A = -55^\circ\text{C}$ TO 125°C

30-volt, 0 - 2.5-a VOLTAGE REGULATOR

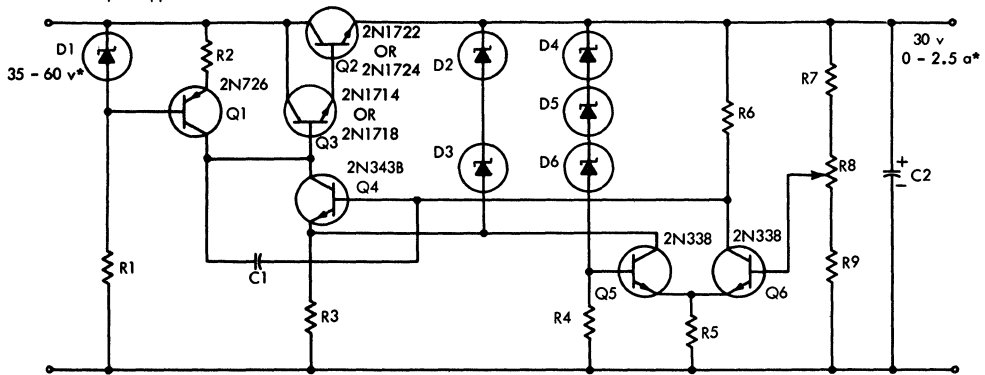
Circuit Characteristics:

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} \Big|_{\Delta V_{IN} = 0} = \text{Output Resistance} \leq 0.007 \text{ ohm}$$

$$100 \times \frac{\Delta V_{OUT}}{\Delta V_{IN}} \Big|_{\Delta I_{OUT} = 0} = \text{Input Regulation} \leq 0.05\% \text{ at } I_{OUT} = 2.0 \text{ a}$$

$$100 \times \frac{\Delta V_{OUT}/V_{OUT}}{\Delta T_A} \Big|_{\Delta V_{IN} = 0} = \text{Output Voltage Temperature Coefficient} \leq 0.007\%/^\circ\text{C} \text{ at } I_{OUT} = 2.0 \text{ a, } V_{IN} = 45 \text{ v}$$

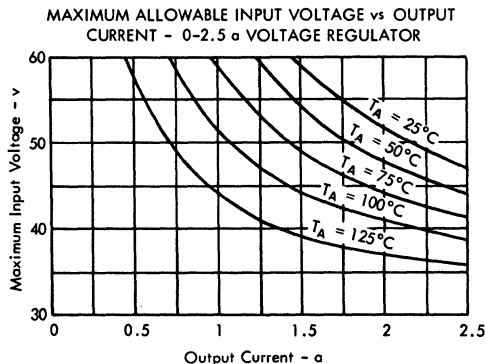
$$\frac{\text{Input Ripple}}{\text{Output Ripple}} = \text{Ripple Reduction} \geq 10,000$$



Q1 - TI 2N726	Q4 - TI 2N343B	C1 - 0.01 μf , 50 v	R4 - 2.43 K, 1/4 w (Wirewound)
Q2 - TI 2N1722 OR TI 2N1724	Q5 & Q6 - TI 2N338	C2 - 100 μf , 50 v	R5 - 35.7 K, 1/4 w
Q3 - TI 2N1714 OR TI 2N1718	D1 - TI 1N746	R1 - 5.11 K, 1/2 w	R6 - 35.7 K, 1/4 w
	D2 & D3 - TI 1N751	R2 - 681, 1/4 w	R7 & R9 - 3.57 K, 1/4 w (Wirewound)
	D4 - D6 - TI 1N752A	R3 - 2.00 K, 1/4 w	R8 - 200, 1/4 w (Wirewound)

- NOTES:
- All Resistor Values in ohms, 5% Tolerance.
 - Resistor Wattage Ratings at 125°C Ambient.
 - Capacitor Voltage Ratings at 125°C Ambient.
 - Q2 and Q3 on Same Heat Sink: Q2: $\theta_{C-HS} + \theta_{HS-A} \leq 2^\circ\text{C}/\text{w}$
Q3: $\theta_{C-HS} + \theta_{HS-A} \leq 22^\circ\text{C}/\text{w}$
 - Q5 and Q6 on Same Heat Sink: Each, $\theta_{C-HS} + \theta_{HS-A} \leq 80^\circ\text{C}/\text{w}$

*See Voltage - Current Derating Curves Below



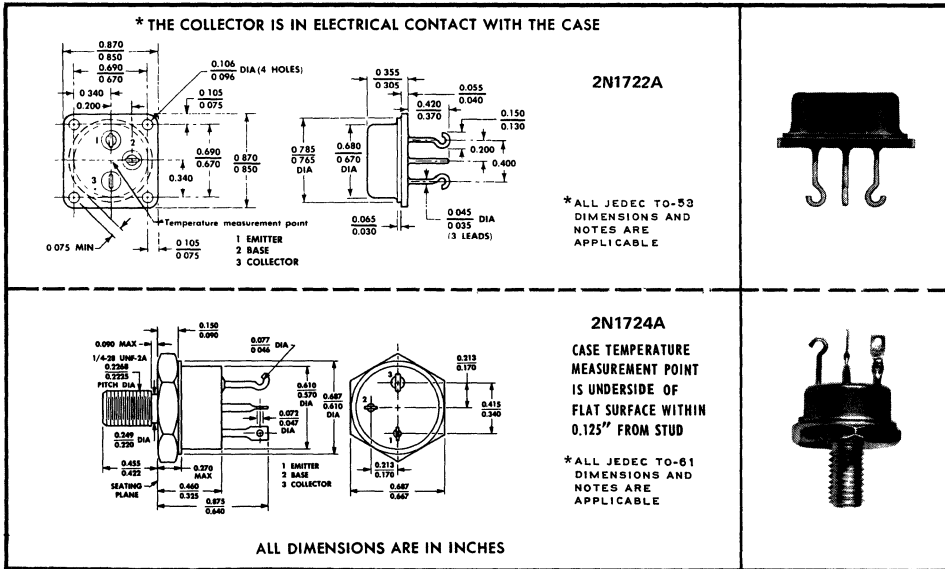
TYPES 2N1722A, 2N1724A N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPES 2N1722A, 2N1724A
BULLETIN NO. DL-S-714268, AUGUST 1963
REVISED SEPTEMBER 1971

- 50 Watts at 100°C Case Temperature
- Maximum r_{CS} of 0.3 Ohm at 2 Amperes I_C
- Maximum V_{BE} of 2 Volts at 5 Amperes I_C
- Minimum f_T of 10 Megahertz

*mechanical data

The transistors are in hermetically sealed welded packages with glass-to-metal seal between case and leads.



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	180 V
Collector-Emitter Voltage (See Note 1)	120 V
Emitter-Base Voltage	10 V
Collector Current, Continuous	5 A
Collector Current, Peak	7.5 A
Emitter Current, Continuous	6 A
Base Current, Continuous	1 A
Safe Continuous Operating Region at (or below) 100°C Case Temperature	See Figure 1
Collector Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	3 W
Collector Power Dissipation at (or below) 100°C Case Temperature (See Note 3)	50 W
Operating Collector Junction Temperature	175°C
Storage Temperature Range	-65°C to +200°C

- NOTES: 1. This value applies when base-emitter diode is open-circuited.
 2. Derate linearly to 175°C free-air temperature at the rate of 20 mW/°C.
 3. Derate linearly to 175°C case temperature at the rate of 0.67 W/°C.

*JEDEC registered data



TYPES 2N1722A, 2N1724A

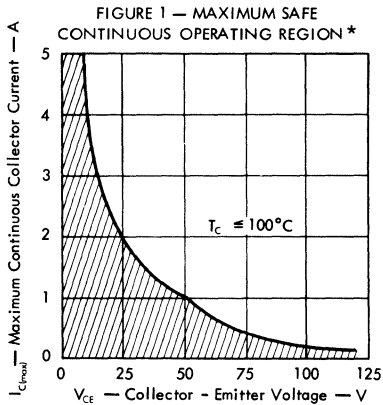
N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Notes 4 and 7	120		V
I_{CBO} Collector Cutoff Current	$V_{CB} = 3 \text{ V}$, $I_E = 0$		0.1	mA
I_{CES} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$, See Note 5		0.1	mA
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$, See Note 5		1.0	
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$, See Note 5		2.0	
	$V_{CE} = 180 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$, See Note 5		10	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 9 \text{ V}$, $I_C = 0$		0.5	mA
	$V_{EB} = 10 \text{ V}$, $I_C = 0$		10	
V_{EBf} Emitter-Base Floating Potential	$V_{CB} = 180 \text{ V}$, $I_E = 0$		1.0	V
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 15 \text{ V}$, $I_C = 100 \text{ mA}$, See Note 4		30	
	$V_{CE} = 15 \text{ V}$, $I_C = 2 \text{ A}$, See Note 4		30 90	
	$V_{CE} = 15 \text{ V}$, $I_C = 2 \text{ A}$, $T_C = -55^\circ\text{C}$, See Note 4		18	
	$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$, See Note 4		20	
V_{BE} Base-Emitter Voltage	$I_B = 200 \text{ mA}$, $I_C = 2 \text{ A}$, See Note 4		1.2	V
	$I_B = 500 \text{ mA}$, $I_C = 5 \text{ A}$, See Note 4		2.0	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 200 \text{ mA}$, $I_C = 2 \text{ A}$, See Note 4		0.6	V
	$I_B = 200 \text{ mA}$, $I_C = 2 \text{ A}$, $T_C = -55^\circ\text{C}$, See Note 4		0.8	
	$I_B = 500 \text{ mA}$, $I_C = 5 \text{ A}$, See Note 4		1.5	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 15 \text{ V}$, $I_C = 500 \text{ mA}$, $f = 10 \text{ MHz}$, See Note 6		1.0	
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 15 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$		550	pF

*thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.5	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	50	°C/W



- NOTES: 4. These parameters must be measured using pulse techniques. $PW = 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.
5. For correct measurement of I_{CES} , the base must be shorted to the emitter. The current meter must not be placed in the base-emitter, short-circuit loop. I_{CES} may be used in place of I_{CBO} for circuit-stability calculations.
6. If tested without a heat sink, DC collector current must not be applied longer than 5 seconds.
7. Other pulse widths or duty cycles may be used for the measurement of collector-emitter breakdown voltage with results similar to those obtained using the conditions specified in Note 4, providing that collector current is limited to 200 mA and case temperature is limited to less than 40°C over a 5 second (or less) measurement period.

*JEDEC registered data

TYPES 2N1723, 2N1725 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

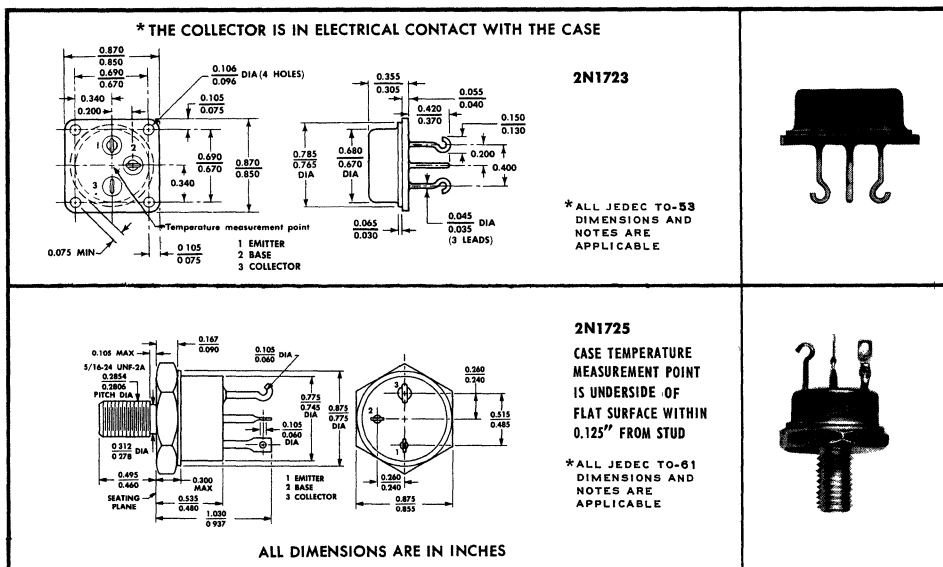
TYPES 2N1723, 2N1725
BULLETIN NO. DL-S-653710, JUNE 1963
REVISED OCTOBER 1965

High-Frequency Power Transistors

50 Watts at 100°C Case Temperature
Maximum R_{CS} of 0.5 Ohm at 2 Amperes I_C
Maximum V_{BE} of 2 Volts at 2 Amperes I_C
Minimum f_T of 10 Megacycles

mechanical data

The transistors are in a hermetically sealed welded package with glass-to-metal seal between case and leads.



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	120 v
Collector-Emitter Voltage (See Note 1)	80 v
Emitter-Base Voltage	10 v
Collector Current, Continuous	5 a
Emitter Current, Continuous	5 a
Safe Continuous Operating Region at 100°C Case Temperature	See Fig. 1
Continuous Collector Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	3 w
Continuous Collector Dissipation at (or below) 100°C Case Temperature (See Note 3)	50 w
Operating Collector Junction Temperature	175°C
Storage Temperature Range	-65° to 200°C

- NOTES: 1. This value applies when base-emitter diode is open circuited.
 2. Derate linearly to 175°C free-air temperature at the rate of 20 mw/°C.
 3. Derate linearly to 175°C case temperature at the rate of 0.67 w/°C.
 4. These parameters are measured using pulse techniques. PW = 300 μsec, Duty Cycle ≤ 2%.
 5. If tested without a heat sink, DC collector current must not be applied longer than 5 seconds.

*Indicates JEDEC registered data.



TYPES 2N1723, 2N1725

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = 0.20$ a, $I_B = 0$, (See Note 4)	80	—	v
I_{CBO} Collector Cutoff Current	$V_{CB} = 3$ v, $I_E = 0$	—	0.1	ma
I_{CES} Collector Cutoff Current	$V_{CE} = 30$ v, $V_{BE} = 0$	—	0.1	ma
	$V_{CE} = 60$ v, $V_{BE} = 0$	—	1.0	ma
	$V_{CE} = 60$ v, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	—	2.0	ma
	$V_{CE} = 120$ v, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	—	10	ma
I_{EBO} Emitter Cutoff Current	$V_{EB} = 3$ v, $I_C = 0$	—	0.5	ma
	$V_{EB} = 9$ v, $I_C = 0$	—	0.5	ma
	$V_{EB} = 10$ v, $I_C = 0$	—	10	ma
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 15$ v, $I_C = 2$ a, (See Note 4)	50	150	—
	$V_{CE} = 15$ v, $I_C = 2$ a, $T_A = -55^\circ\text{C}$, (See Note 4)	25	—	—
	$V_{CE} = 15$ v, $I_C = 0.1$ a, (See Note 4)	50	—	—
V_{BE} Base-Emitter Voltage	$I_B = 0.20$ a, $I_C = 2.0$ a, (See Note 4)	—	2.0	v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.20$ a, $I_C = 2.0$ a, (See Note 4)	—	1.0	v
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 15$ v, $I_C = 0.50$ a, $f = 10$ mc, (See Note 5)	1.0	—	—
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 15$ v, $I_E = 0$, $f = 1.0$ mc	—	550	pf

*thermal characteristics

PARAMETER	MIN	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	—	1.5	$^\circ\text{C}/\text{w}$
θ_{J-A} Junction-to-Free-Air Thermal Resistance	—	50	$^\circ\text{C}/\text{w}$

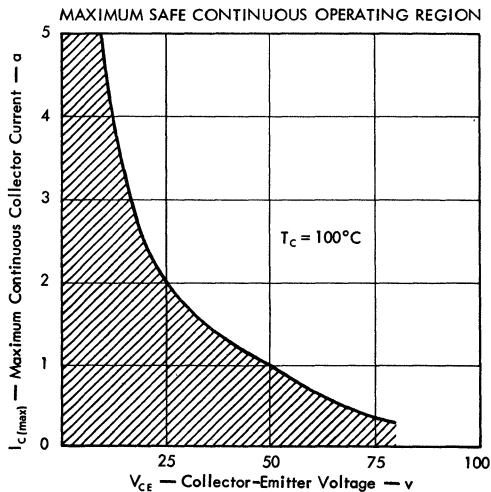


Figure 1

*Indicates JEDEC registered data.

TYPES 2N1936, 2N1937 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

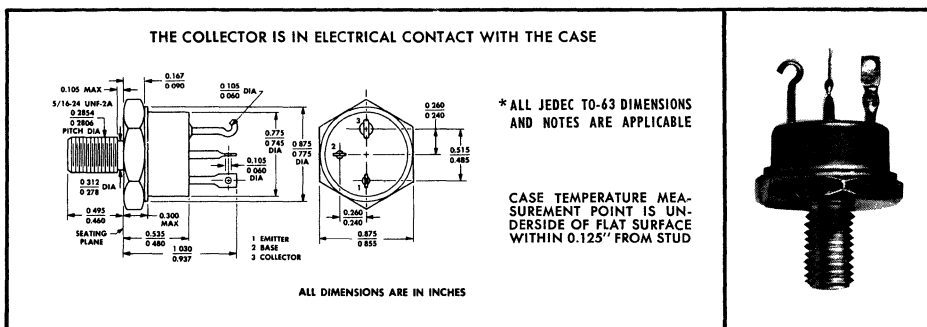
TYPES 2N1936, 2N1937
BULLETIN NO. DL-5 644380, FEBRUARY 1964

HIGH-FREQUENCY POWER TRANSISTORS

- **High Power Dissipation:** 150 watts at $T_c = 100^\circ \text{C}$
- **Low Thermal Resistance:** $0.5^\circ \text{C}/\text{w max}$
- **Low Saturation Voltage:** $V_{CE} = 0.75 \text{ v max @ } I_C = 10 \text{ a}$
- **High f_T :** 18 mc min at 10 v, 1 a

mechanical data

Stress effects caused by the difference in thermal coefficients of expansion between the silicon wafer and copper header are minimized by the use of a molybdenum platform brazed to the header. The wafer is mounted to the molybdenum platform by means of a special high-temperature gold alloy in an oxygen-free atmosphere, thus eliminating flux. Final encapsulation of the device is carried out in an ultra-clean, controlled atmosphere dry-box utilizing extremely-high-reliability techniques.



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N1936	2N1937
* Collector-Base Voltage	← 125 v →	
* Collector-Emitter Voltage (See Note 1)	60 v	80 v
* Emitter-Base Voltage	← 6 v →	
* Collector Current, Continuous	← 20 a →	
* Base Current, Continuous	← 10 a →	
* Emitter Current, Continuous	← { 25 a [†] } (20 a*) →	
* Safe Continuous Operation Region at 100°C Case Temperature	See Figure 5	
* Total Device Dissipation at (or below) 100°C Case Temperature (See Note 2)	← 150 w →	
* Operating Case Temperature Range	← -65°C to +175°C →	
* Storage Temperature Range	← -65°C to +200°C →	

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 175°C case temperature at the rate of 2 w/°C.

*Indicates JEDEC registered data.

†Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

TYPES 2N1936, 2N1937

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYPE	MIN	MAX	UNIT
BV _{CEO}	Collector-Emitter Breakdown Voltage	I _C = 200 ma, I _B = 0, (See Note 3)	2N1936	60*		v
			2N1937	80*		
I _{CEO}	Collector Cutoff Current	V _{CE} = 50 v, I _B = 0			15*	ma
I _{CEX}	Collector Cutoff Current	V _{CE} = 120 v, V _{BE} = -1 v			10*	ma
		V _{CE} = 60 v, V _{BE} = -1 v, T _C = 150°C	2N1936		10*	
		V _{CE} = 80 v, V _{BE} = -1 v, T _C = 150°C	2N1937		10*	
I _{EBO}	Emitter Cutoff Current	V _{EB} = 6 v, I _C = 0			1.0*	ma
h _{FE}	Static Forward Current Transfer Ratio	V _{CE} = 3 v, I _C = 1 a, (See Note 3)		12*	75*	
		V _{CE} = 3 v, I _C = 10 a, (See Note 3)		7*, 10†	50*	
		V _{CE} = 3 v, I _C = 10 a, T _C = -55°C, (See Note 3)		6		
		V _{CE} = 10 v, I _C = 10 a, (See Note 3)		10*	50*	
		V _{CE} = 10 v, I _C = 10 a, T _C = -55°C, (See Note 3)		6*		
V _{BE}	Base-Emitter Voltage	V _{CE} = 3 v, I _C = 10 a, (See Notes 3 and 4)			1.25*	v
		I _B = 1.6 a, I _C = 10 a, (See Notes 3 and 4)			1.50*	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	I _B = 1.6 a, I _C = 10 a, (See Notes 3 and 4)			0.75*	v
h _{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 v, I _C = 1 a, f = 1 kc		15*	90*	
h _{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 v, I _C = 1 a, f = 1 mc		4.0*		
h _{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 v, I _C = 1 a, f = 4.5 mc		4.0		
C _{ob}	Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 v, I _E = 0, f = 1 mc			1800*	pf

NOTES: 3. These parameters must be measured using pulse techniques.

PW = 300 μsecs, Duty Cycle ≤ 2%.*

4. V_{CE} and V_{BE} measurements are made with voltage sensing contacts that are separated from the current carrying contacts.

*Indicates JEDEC registered data.

†Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

TYPES 2N1936, 2N1937 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

thermal characteristics

PARAMETER	MIN	MAX	UNIT
* θ_{J-C} Junction-to-Case Thermal Resistance		0.5	$^{\circ}\text{C}/\text{w}$
θ_{J-A} Junction-to-Free-Air Thermal Resistance		37.5	$^{\circ}\text{C}/\text{w}$

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS [†]	TYP	MAX	UNIT
t_d Delay Time	$I_C = 10 \text{ a}$,	70		nsec
t_r Rise Time	$I_{B(1)} = 1.6 \text{ a}$, $I_{B(2)} = -1.6 \text{ a}$,	40		nsec
t_s Storage Time	$V_{BE(\text{off})} = -6 \text{ v}$, $R_L = 2.7 \Omega$,	5.0		μsec
t_f Fall Time	See Figure 1	0.4		μsec
t_{off} Turn-off Time		5.4	10	μsec

^{††}Voltage and current values shown are nominal; exact values vary slightly with device parameters.

*Indicates JEDEC registered data.

PARAMETER MEASUREMENT INFORMATION

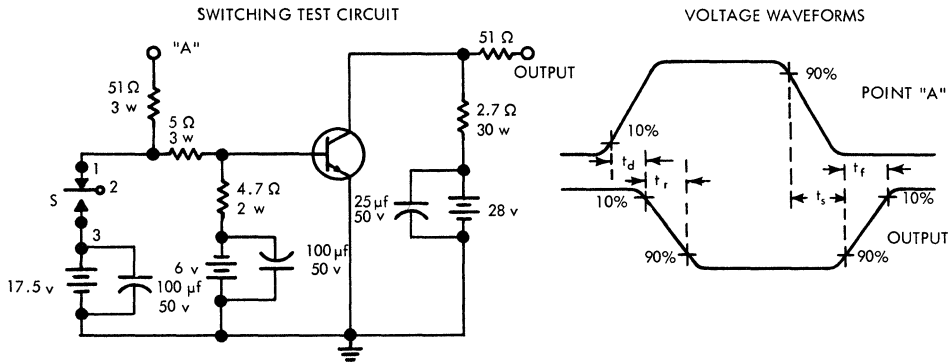


FIGURE 1

NOTES: 5. Relay S is a make-before-break relay with mercury-wetted contacts that is driven by an input pulse with the following characteristics:
Amplitude = 80v, PRR = 20 PPS, PW = 6 msec.

6. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ nsec}$, $C_{in} \leq 20 \text{ pf}$, $R_{in} \geq 1 \text{ M}\Omega$.

5

TYPES 2N1936, 2N1937

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

THERMAL INFORMATION

TABLE I

HEAT SINK		θ_{HS-A}
TYPE	DIMENSIONS	
Bright Copper	4" x 4" x 1/8"	3.8 C°/w
	6" x 6" x 1/8"	2.2 C°/w
	8" x 8" x 1/8"	1.8 C°/w
	10" x 10" x 1/8"	1.4 C°/w
Bright Aluminum	4" x 4" x 1/8"	6.5 C°/w
	6" x 6" x 1/8"	4.5 C°/w
	8" x 8" x 1/8"	3.5 C°/w
	10" x 10" x 1/8"	2.8 C°/w
Delbert Blinn #113 or Modine 1E1155B Unfinished (or Equivalent)		3.7 C°/w
Delbert Blinn #113 or Modine 1E1155B, Black Anodized (or Equivalent)		3.2 C°/w

θ_{HS-A} are typical values based on convection cooling with plates and fins mounted in a vertical position.

[†]This value applies with the transistor mounted in the center of the heat sink with 40 inch-pounds of torque applied to transistor stud.

The PEAK-POWER-COEFFICIENT CURVE (See Figure 4), shows the ratio of maximum instantaneous junction-to-case temperature rise at any pulse width and duty cycle to the rise which occurs at 100% duty cycle. Use of this curve is best explained by the equations and examples below. See Table II for a definition of terms.

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-A}}$$

Example A — Find $P_{T(avg)}$ (design limit)

OPERATING CONDITIONS:

Heat Sink = 4" x 4" x 1/8" copper,

$\theta_{HS-A} = 3.8 \text{ C}^\circ/\text{w}$

$T_{J(avg)}$ (design limit) = 175°C

$T_A = 30 \text{ C}^\circ$

$d = 100\%$ (1.0)

with DC-11 silicone grease, $\theta_{C-HS} = 0.45 \text{ C}^\circ/\text{w}$

Example B — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

Heat Sink = 8" x 8" x 1/8" copper,

$\theta_{HS-A} = 1.8 \text{ C}^\circ/\text{w}$

with DC-11 silicone grease, $\theta_{C-HS} = 0.45 \text{ C}^\circ/\text{w}$

$T_{J(max)}$ (design limit) = 175°C

$T_A = 35 \text{ C}^\circ$

$d = 5\%$ (0.05)

$t_w = 1 \text{ msec}$

TABLE II

SYMBOL	DEFINITION	UNIT	VALUE
$P_{T(avg)}$	Average Power Dissipation	w	
$P_{T(max)}$	Peak Power Dissipation	w	
θ_{J-C}	Junction-to-Case Thermal Resistance	C°/w	0.5
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	C°/w	37.5
θ_{C-A}	Case-to-Free-Air Thermal Resistance	C°/w	37.0
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance	C°/w	0.65
	Typical with Dry Stud		
	Typical with DC-11 Silicone Grease (or Equivalent)	C°/w	0.45
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance	C°/w	See Table I
T_A	Free-Air Temperature	°C	
$T_{J(max)}$	Peak Junction Temperature	°C	≤ 175
$T_{J(avg)}$	Average Junction Temperature	°C	≤ 175
T_C	Case Temperature	°C	
K	Peak-Power Coefficient		See Figure 4
t_w	Pulse Width	msec	
t_p	Pulse Period	msec	
d	Duty Cycle Ratio (t_w/t_p)		

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d \theta_{C-A} + K \theta_{J-C}}$$

Solution:

By use of equation No. 1

$$P_{T(avg)} = \frac{T_{J(max)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}}$$

$$P_{T(avg)} = \frac{175 - 30}{0.5 + 0.45 + 3.8} = 30.5 \text{ w}$$

Solution:

From Figure 4, Peak-Power Coefficient

$K = 0.12$ and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}}$$

$$P_{T(max)} = \frac{175 - 35}{0.05(0.45 + 1.8) + 0.12(0.5)} = 811 \text{ w}$$

TYPES 2N1936, 2N1937

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

THERMAL CHARACTERISTICS

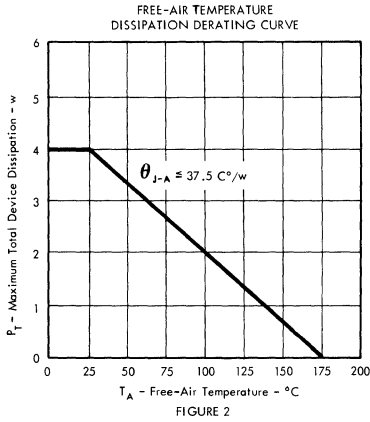


FIGURE 2

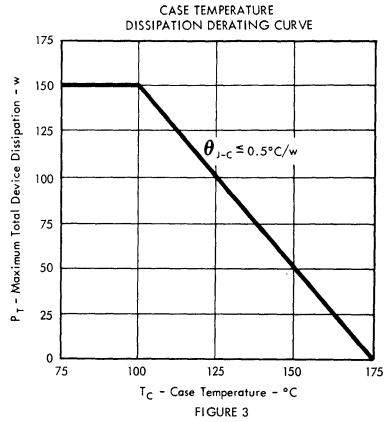


FIGURE 3

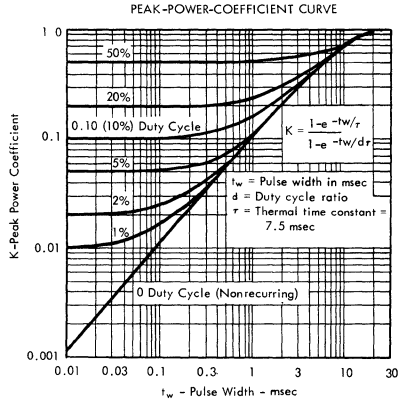


FIGURE 4

* MAXIMUM SAFE CONTINUOUS OPERATING REGION

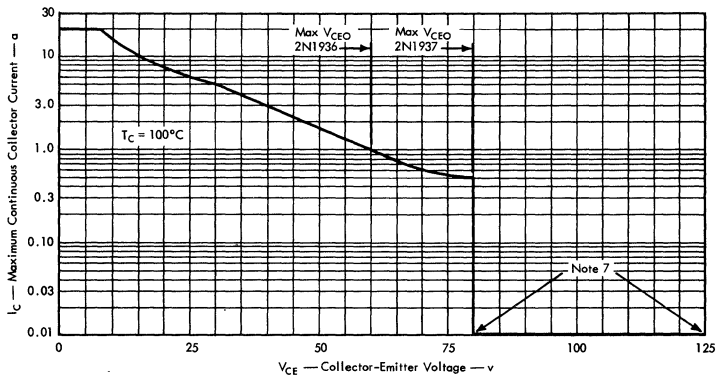


FIGURE 5

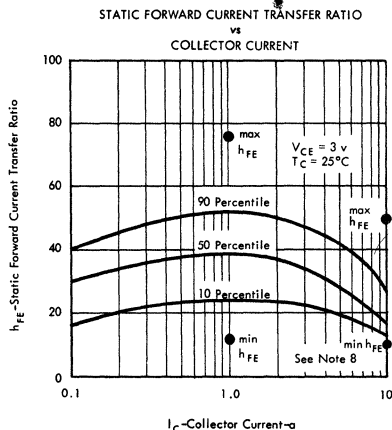
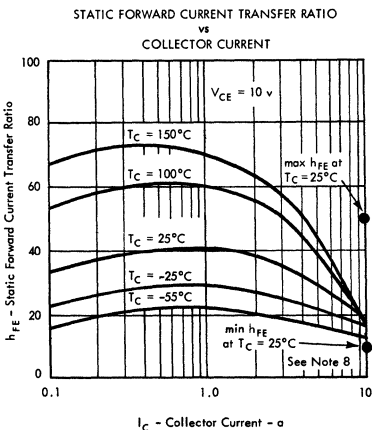
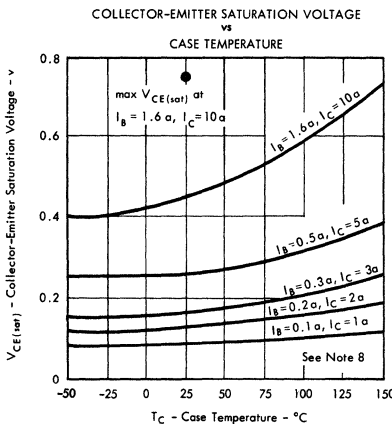
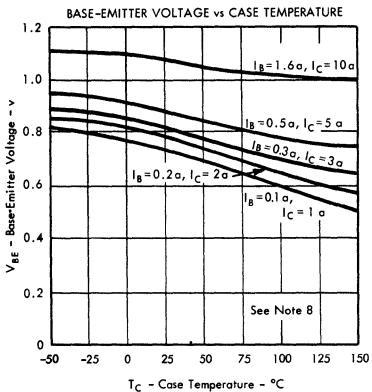
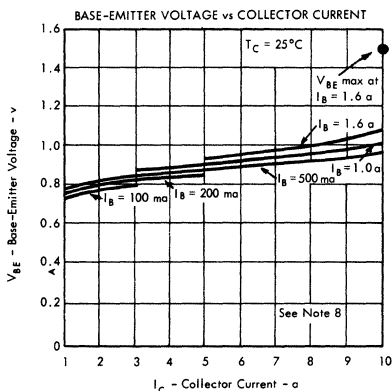
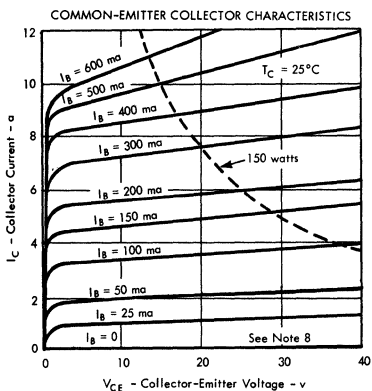
Note 7: Operation in this region is permissible only when the base is reverse-voltage-biased with respect to the emitter.

5

TYPES 2N1936, 2N1937

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL CHARACTERISTICS



Note 8: These characteristics were measured using pulse techniques. $PW \leq 300 \mu sec$, Duty Cycle 2%.

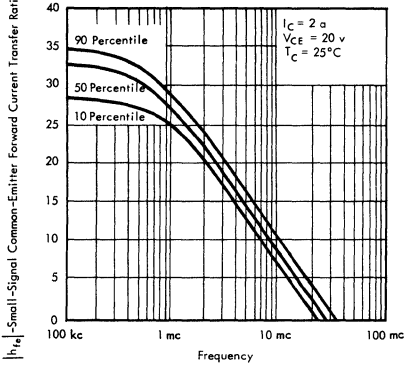
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TYPES 2N1936, 2N1937

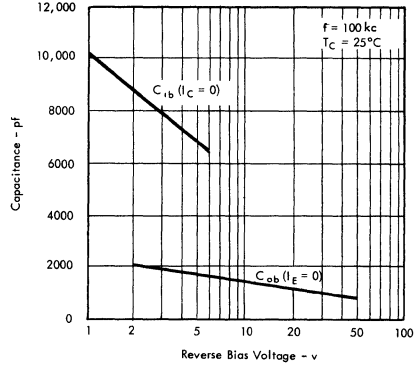
N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL CHARACTERISTICS

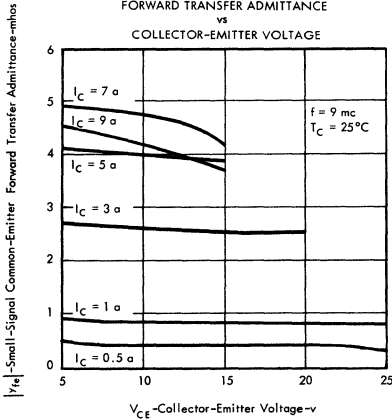
SMALL-SIGNAL COMMON-EMITTER FORWARD CURRENT TRANSFER RATIO
vs
FREQUENCY



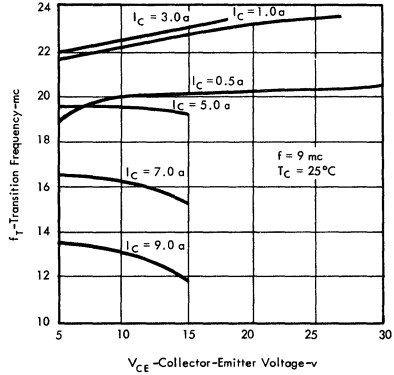
COMMON-BASE OPEN-CIRCUIT INPUT AND OUTPUT CAPACITANCE
vs
REVERSE BIAS VOLTAGE



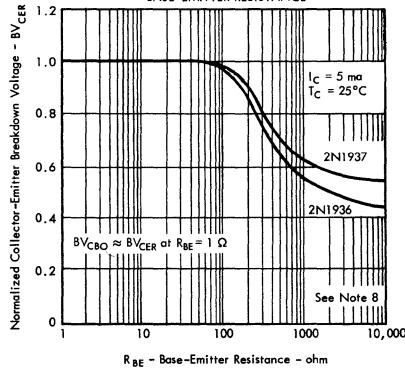
SMALL-SIGNAL COMMON-EMITTER
FORWARD TRANSFER ADMITTANCE
vs
COLLECTOR-EMITTER VOLTAGE



TRANSITION FREQUENCY vs COLLECTOR-EMITTER VOLTAGE



NORMALIZED COLLECTOR-EMITTER BREAKDOWN VOLTAGE
vs
BASE-EMITTER RESISTANCE



NOTE 8: These characteristics were measured using pulse techniques. PW = 300 μ sec, Duty Cycle \leq 2%.

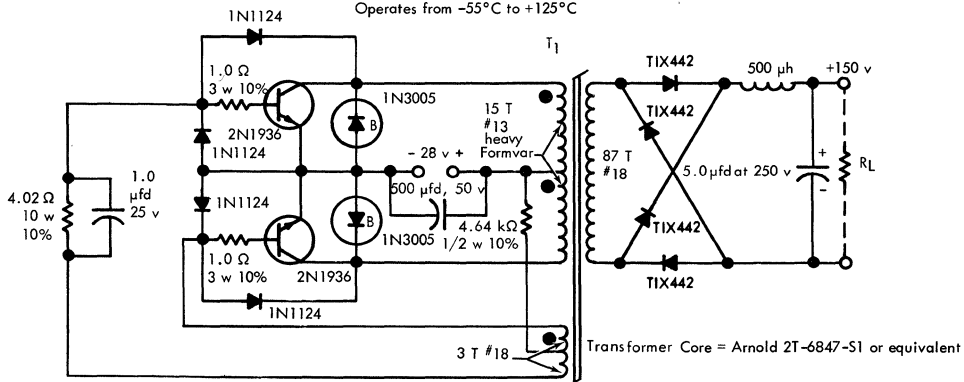
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TYPES 2N1936, 2N1937

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL APPLICATION DATA

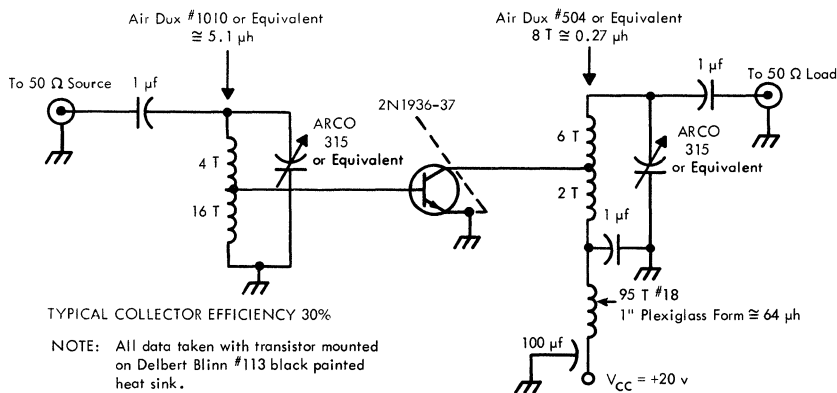
FIGURE A — 225 WATT 10 kc DC-DC CONVERTER
Operates from -55°C to $+125^{\circ}\text{C}$



NOTE: Minimum usable $h_{FE} = 10$ at $V_{CE} = 3\text{v}$, $I_C = 10\text{a}$, $T_A = 25^{\circ}\text{C}$
Both transistors use heat sinks, $\theta_{C-HS} + \theta_{HS-A} \leq 2^{\circ}\text{C}/\text{w}$
each. All diodes must have adequate heat sinks.

TYPICAL PERFORMANCE AT $T_A = 25^{\circ}\text{C}$
Efficiency = 80%
Output ripple 1.0 volt

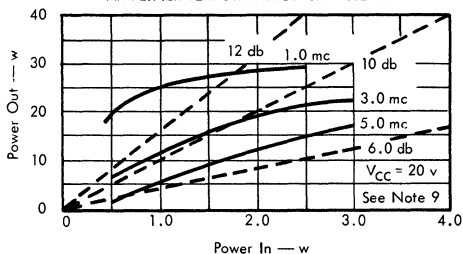
FIGURE B — 3 mc POWER AMPLIFIER



TYPICAL COLLECTOR EFFICIENCY 30%

NOTE: All data taken with transistor mounted on Delbert Blinn #113 black painted heat sink.

TYPICAL ONE-STAGE COMMON-EMITTER
AMPLIFIER PERFORMANCE CAPABILITY



NOTE 9: This data was taken in amplifiers with configuration similar to Fig. B with component values optimized at each frequency.

TYPES 2N2150, 2N2151

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPES 2N2150, 2N2151
 BULLETIN NO. DL-S-7110369, OCTOBER 1968
 REVISED SEPTEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Dissipation Capability of 30 W at 40 V, $T_c = 100^\circ\text{C}$
- Typ $V_{CE(sat)}$ of 0.2 V at 1 A

***mechanical data**

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE

3 - COLLECTOR
0.175 NOM
(SEE NOTES A & B)

120° NOM
3 PLACES
(SEE NOTE C)

1 - EMITTER

2 - BASE

**ALL JEDEC TO-111
DIMENSIONS AND
NOTES ARE
APPLICABLE**

NOTES:

- A. Position of terminals with respect to hexagon is not controlled.
- B. Terminals located on true position within 0.030 inch relative to diameter of can.
- C. This dimension applies to the location of the center line of the terminals.
- D. The case temperature may be measured anywhere on the seating plane within 0.125 inch of the stud.
- E. All dimensions are in inches unless otherwise specified.

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

*Collector-Base Voltage	125 V
*Collector-Emitter Voltage (See Note 1)	80 V
*Emitter-Base Voltage	8 V
*Continuous Collector Current	1 A
Peak Collector Current (See Note 2)	8 A
*Continuous Base Current	1 A
*Continuous Emitter Current	2 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 8
*Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	30 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W
*Operating Collector Junction Temperature Range	-65°C to 175°C
*Storage Temperature Range	-65°C to 200°C
*Terminal Temperature 1/8 Inch from Case for 10 Seconds	230°C

- NOTES:**
1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 175°C case temperature at the rate of 0.4 W/deg.
 4. Derate linearly to 175°C free-air temperature at the rate of 13.3 mW/deg.

*Indicates JEDEC registered data



TYPES 2N2150, 2N2151

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N2150		2N2151		UNIT	
		MIN	MAX	MIN	MAX		
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 50 \text{ mA}, I_B = 0$, See Note 5	80		80		V	
I_{CEO} Collector Cutoff Current	$V_{CE} = 80 \text{ V}, I_B = 0$		50		50	μA	
I_{CES} Collector Cutoff Current	$V_{CE} = 120 \text{ V}, V_{BE} = 0$		5		5	μA	
	$V_{CE} = 120 \text{ V}, V_{BE} = 0, T_C = 150^\circ\text{C}$		50		50	μA	
I_{CEV} Collector Cutoff Current	$V_{CE} = 120 \text{ V}, V_{BE} = -1 \text{ V}$		5		5	μA	
	$V_{CE} = 120 \text{ V}, V_{BE} = -1 \text{ V}, T_C = 150^\circ\text{C}$		50		50	μA	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 8 \text{ V}, I_C = 0$		2		2	μA	
	$V_{EB} = 8 \text{ V}, I_C = 0, T_C = 150^\circ\text{C}$		20		20	μA	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}, I_C = 1 \text{ A}$	See Notes 5 and 6	20	60	40	120	
	$V_{CE} = 5 \text{ V}, I_C = 500 \text{ mA}$		20	60	40	120	
	$V_{CE} = 5 \text{ V}, I_C = 100 \text{ mA}$		20		40		
	$V_{CE} = 5 \text{ V}, I_C = 500 \text{ mA}, T_C = -55^\circ\text{C}$		10		20		
V_{BE} Base-Emitter Voltage	$V_{CE} = 5 \text{ V}, I_C = 1 \text{ A}$	See Notes 5 and 6		1.6		1.6	V
	$I_B = 100 \text{ mA}, I_C = 1 \text{ A}$			1.8		1.8	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}, I_C = 1 \text{ A}$	See Notes 5 and 6		1		1	V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 30 \text{ V}, I_C = 100 \text{ mA}, f = 1 \text{ kHz}$		20	80	40	160	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 30 \text{ V}, I_C = 100 \text{ mA}, f = 10 \text{ MHz}$		1	10	1	10	
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 20 \text{ V}, I_E = 0, f = 1 \text{ MHz}$			160		160	pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
* θ_{J-C} Junction-to-Case Thermal Resistance	2.5	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	75	

*Indicates JEDEC registered data

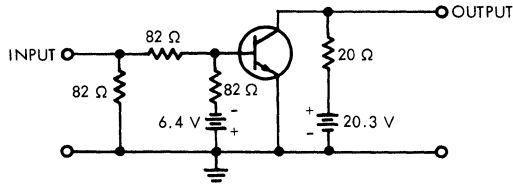
TYPES 2N2150, 2N2151 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

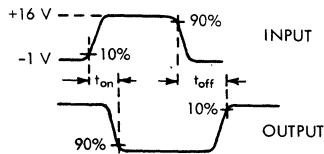
PARAMETER	TEST CONDITIONS†	2N2151	UNIT
		TYP	
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_{B(1)} = 100 \text{ mA}$, $I_{B(2)} = -100 \text{ mA}$,	130	ns
t_{off} Turn-Off Time	$V_{BE(off)} = -3.7 \text{ V}$, $R_L = 20 \Omega$, See Figure 1	1100	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

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TYPES 2N2150, 2N2151

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

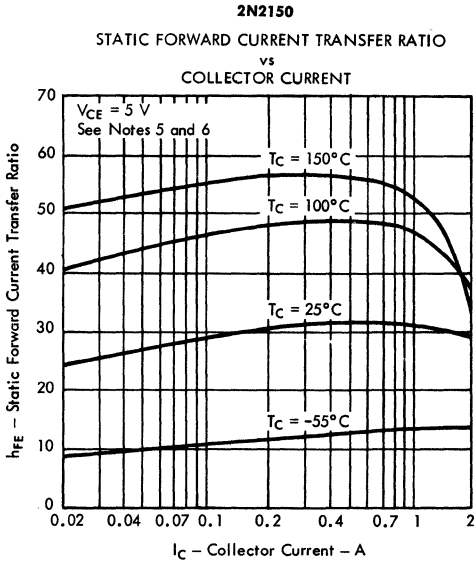


FIGURE 2

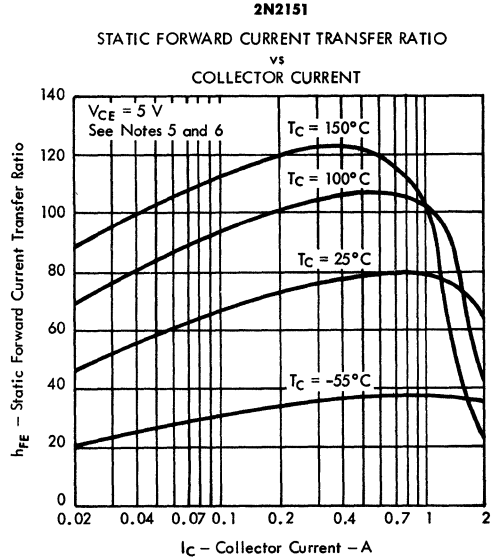


FIGURE 3

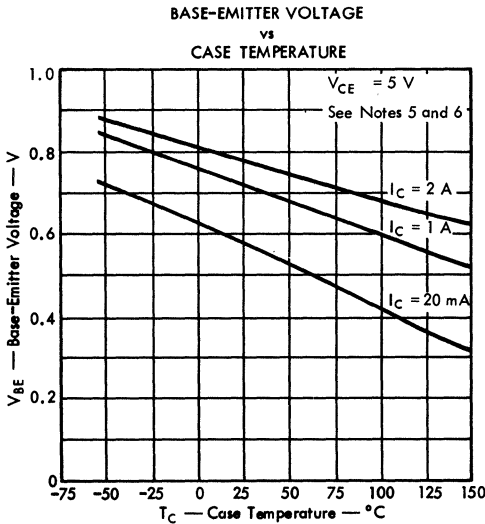


FIGURE 4

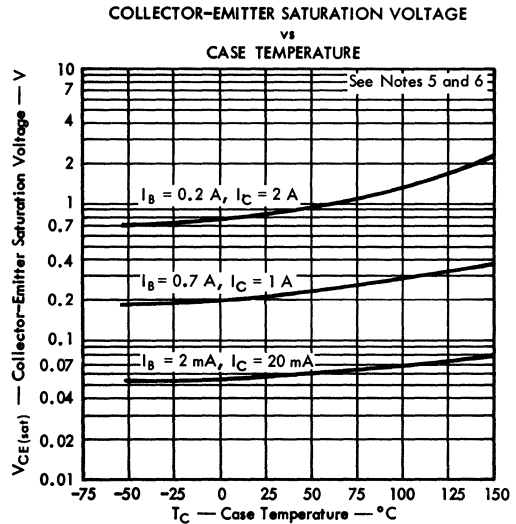


FIGURE 5

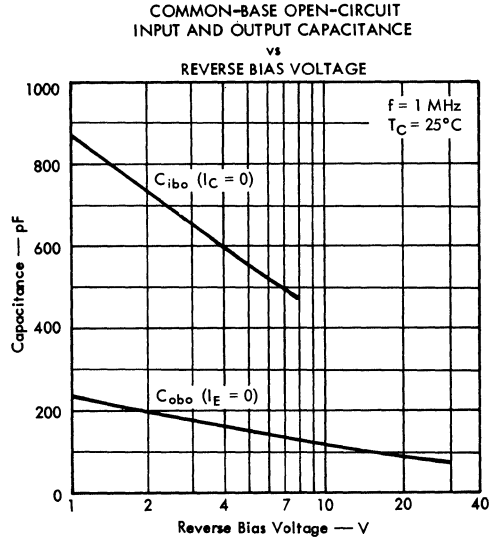
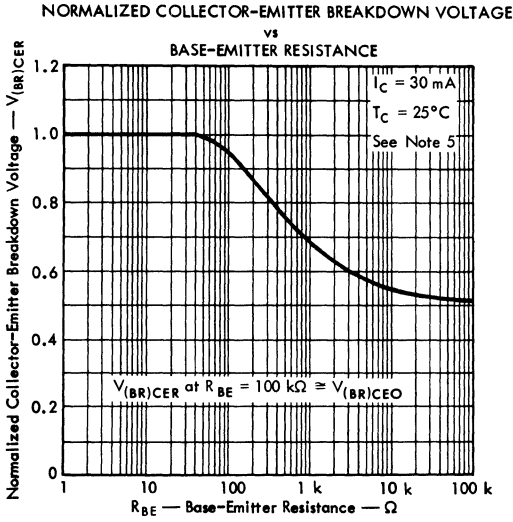
NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N2150, 2N2151

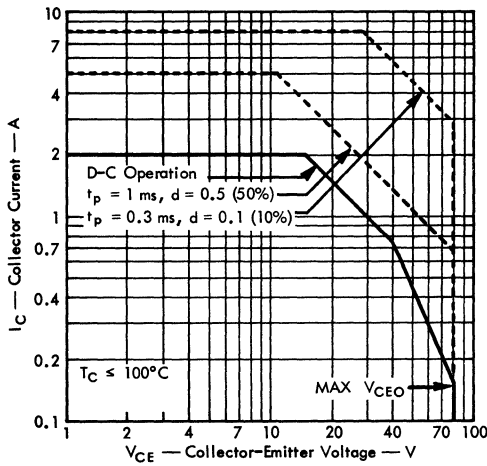
N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS



NOTE 5: This parameter must be measured using pulse techniques: $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

MAXIMUM SAFE OPERATING REGION



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TYPES 2N2150, 2N2151

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

THERMAL INFORMATION

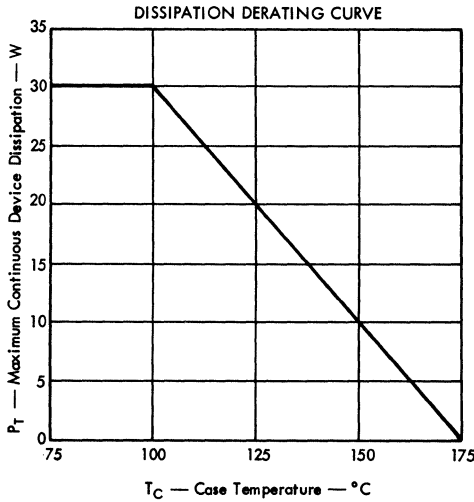


FIGURE 9

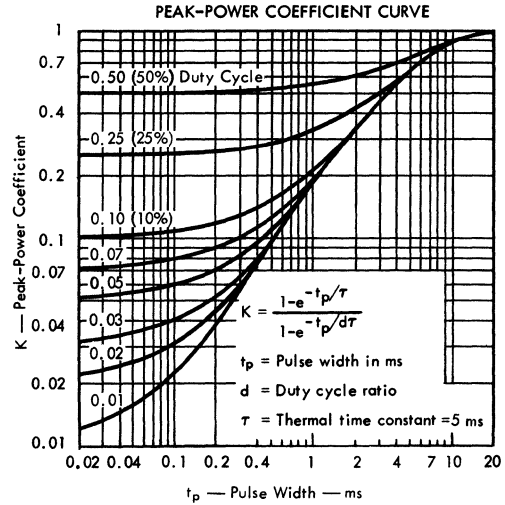


FIGURE 10

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	75	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	2.5	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	72.5	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 175	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 175	°C
K	Peak-Power Coefficient	See Figure 10	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 175^\circ\text{C} \text{ as in figure 9}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 175^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 175^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 175^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C-HS} + \theta_{HS-A} = 4 \text{ deg/W}$ (From information supplied with heat sink.)

$T_{J(av)}$ (design limit) = 175°C

$T_A = 50^\circ\text{C}$

d = 10% (0.1)

$t_p = 0.1 \text{ ms}$

Solution:

From figure 10, Peak-Power Coefficient

$K = 0.11$ and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{175 - 50}{0.1(4) + (0.11)2.5} = 185 \text{ W}$$

TYPE 2N2880

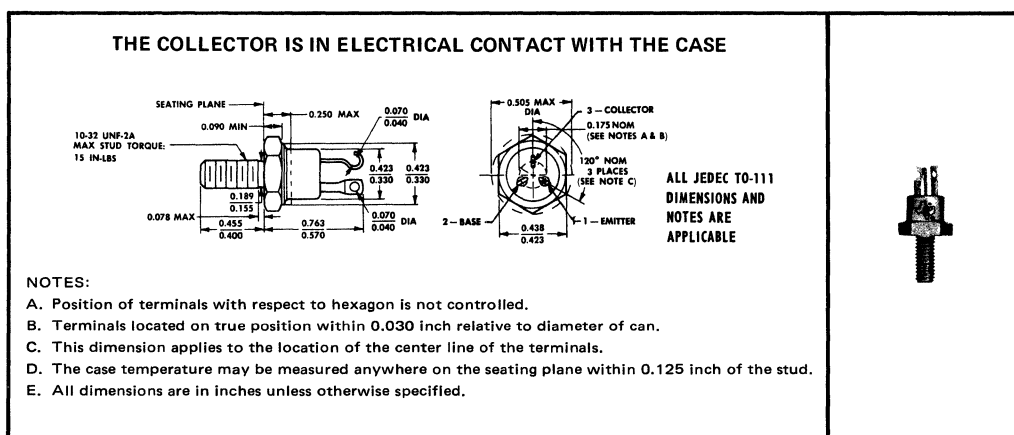
N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPE 2N2880
BULLETIN NO. D.L.S. 6911246, DECEMBER 1969

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 30 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.25 V at $I_C = 1$ A
- Max t_r of 80 ns at $I_C = 1$ A
- Min f_T of 50 MHz at 10 V, 1 A

*mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

*Collector-Base Voltage	100 V
*Collector-Emitter Voltage (See Note 1)	80 V
*Emitter-Base Voltage	8 V
*Continuous Collector Current	5 A
*Continuous Base Current	0.5 A
*Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7
*Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	30 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W
*Operating Collector Junction Temperature Range	-65°C to 200°C
*Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	230°C

- NOTES:
1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 1$ ms, duty cycle $\leq 50\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.3 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C.

*JEDEC registered data

TYPE 2N2880

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

* electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10 \mu A, I_E = 0$		100		V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 10 \text{ mA}, I_B = 0$	See Note 5	80		V
		$I_C = 100 \text{ mA}, I_B = 0$		70		
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10 \mu A, I_C = 0$		8		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 60 \text{ V}, I_E = 0$			0.1	μA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 50 \text{ V}, I_B = 0$			100	μA
I_{CEV}	Collector Cutoff Current	$V_{CE} = 100 \text{ V}, V_{BE} = -0.5 \text{ V}$			10	μA
		$V_{CE} = 60 \text{ V}, V_{BE} = -0.5 \text{ V}, T_C = 150^\circ C$			50	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}, I_C = 0$			0.1	μA
		$V_{EB} = 8 \text{ V}, I_C = 0$			10	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}, I_C = 10 \text{ mA}$	See Notes 5 and 6		30	
		$V_{CE} = 2 \text{ V}, I_C = 1 \text{ A}$		40	120	
		$V_{CE} = 5 \text{ V}, I_C = 5 \text{ A}$		15		
		$V_{CE} = 2 \text{ V}, I_C = 1 \text{ A}, T_C = -55^\circ C$		10		
V_{BE}	Base-Emitter Voltage	$I_B = 100 \text{ mA}, I_C = 1 \text{ A}$	See Notes 5 and 6		1.2	V
		$V_{CE} = 2 \text{ V}, I_C = 1 \text{ A}$			1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}, I_C = 1 \text{ A}$	See Notes 5 and 6		0.25	V
		$I_B = 500 \text{ mA}, I_C = 5 \text{ A}$			2	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}, I_C = 50 \text{ mA}, f = 1 \text{ kHz}$		40	140	
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}, I_C = 1 \text{ A}, f = 10 \text{ MHz}$		5		
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}, I_E = 0, f = 1 \text{ MHz}$			150	pF

NOTES: 5. These parameters must be measured using pulse techniques, $t_p = 330 \mu s$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	3.33	$^\circ C/W$
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	87.5	

*JEDEC registered data

TYPE 2N2880

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MAX	UNIT
t_r Rise Time	$V_{CC} = 25\text{ V}, I_C = 1\text{ A}^\dagger$, See Figure 1	80	ns
t_s Storage Time		60	ns
t_f Fall Time		80	ns

[†]This value of on-state collector current is nominal. Actual value will vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION

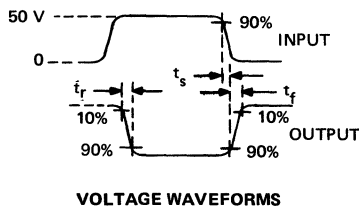
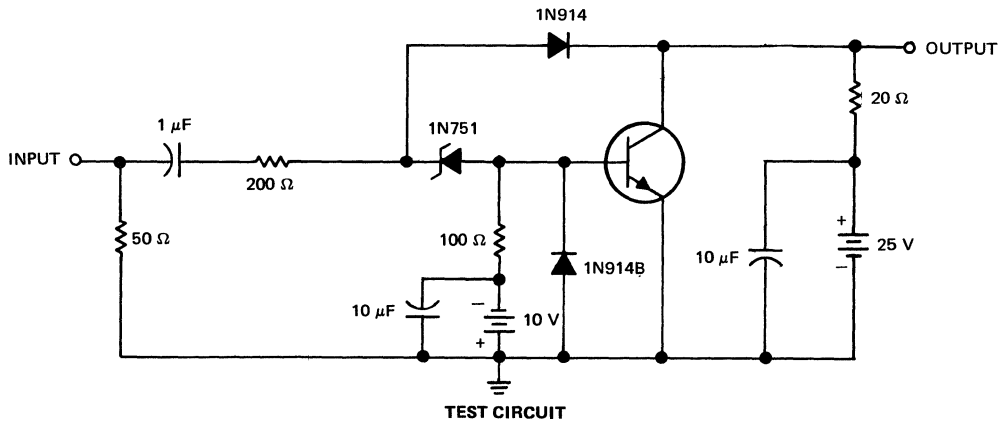


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 1.5\text{ k}\Omega$, $t_p = 10\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 1\text{ M}\Omega$, $C_{in} \leq 15\text{ pF}$.
 - Resistors must be noninductive types.

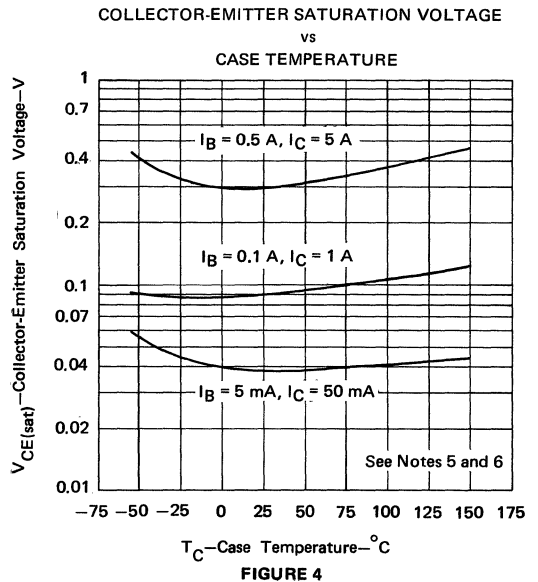
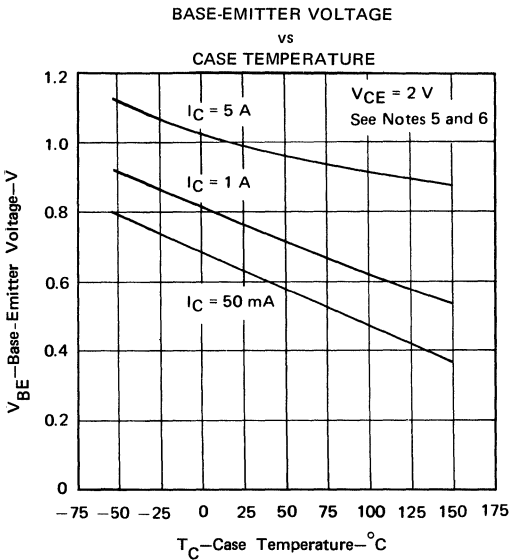
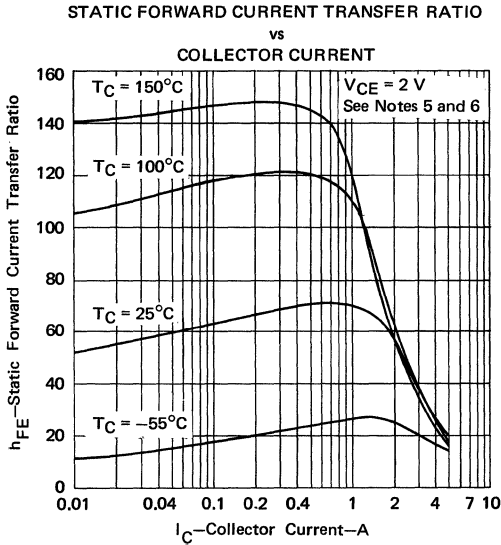
*JEDEC registered data

TYPE 2N2880

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

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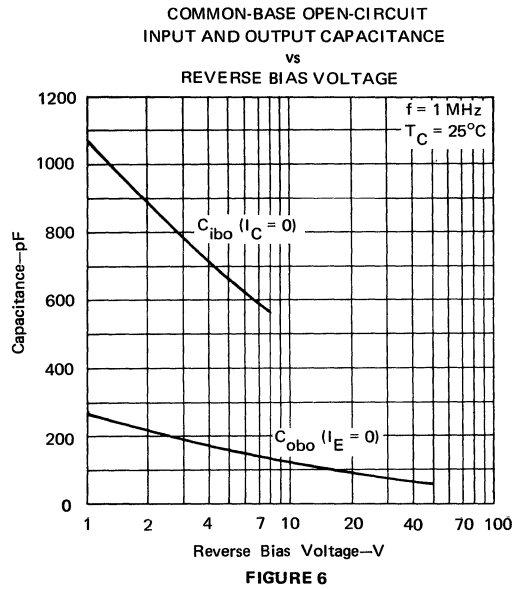
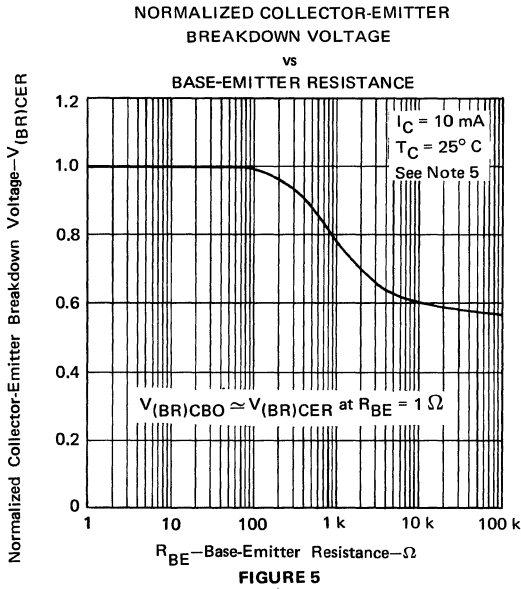


- NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 330 \mu s$, duty cycle $\leq 2\%$.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPE 2N2880

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

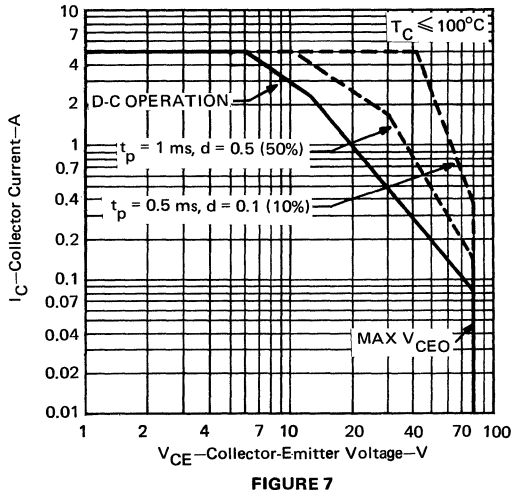
TYPICAL CHARACTERISTICS



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NOTE 5: These parameters must be measured using pulse techniques. $t_p = 330 \mu s$, duty cycle $\leq 2\%$.

*MAXIMUM SAFE OPERATING REGION



*JEDEC registered data

TYPE 2N2880

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

THERMAL INFORMATION

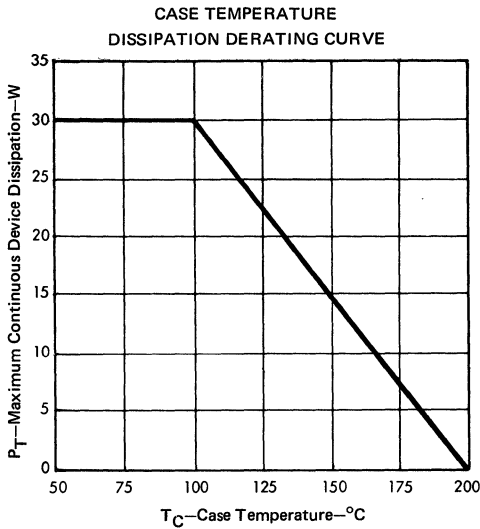


FIGURE 8

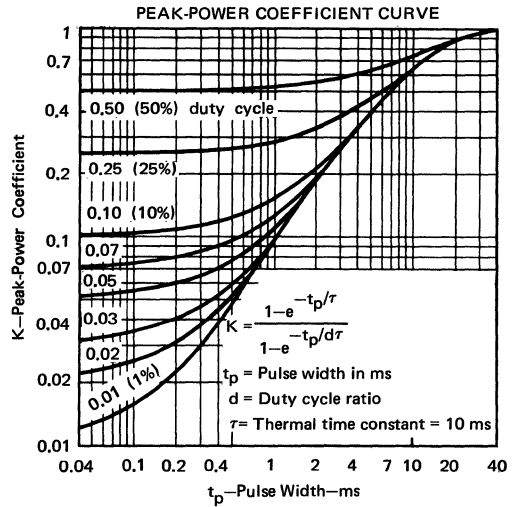


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	87.5	°C/W
θ_{J-C}	Junction-to-Case Thermal Resistance	3.33	°C/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	84.17	°C/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		°C/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		°C/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Equation No. 1—Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C < 200^\circ\text{C} \text{ as in Figure 8}$$

Equation No. 2—Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3—Application: Peak-power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4—Application: Peak-power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Example—Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C-HS} + \theta_{HS-A} = 3.8^\circ\text{C/W}$ (From information supplied with heat sink.)

$T_{J(av)}$ (design limit) = 200°C
 $T_A = 50^\circ\text{C}$
 $d = 10\%$ (0.1)
 $t_p = 0.1$ ms

Solution:

From Figure 9, Peak-Power Coefficient

$K = 0.103$ and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(3.8) + 0.103(3.33)} = 207 \text{ W}$$

TYPES 2N2987 THRU 2N2994 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPES 2N2987 THRU 2N2994
BULLETIN NO. DL-5-6810508, DECEMBER 1968

HIGH-FREQUENCY INTERMEDIATE-POWER TRANSISTORS

- 15 Watts at 100°C Case Temperature
- Typ $V_{CE(sat)}$ of 0.2 V at 200 mA
- Typ V_{BE} of 0.8 V at 200 mA
- Typ f_T of 50 MHz at 10 V, 100 mA

* mechanical data

<p>2N2987 THRU 2N2990</p>	<p>THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE</p> <p>ALL JEDEC TO-5 DIMENSIONS AND NOTES ARE APPLICABLE</p> <p>ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED</p>	
<p>2N2991 THRU 2N2994</p>	<p>THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE</p> <p>POSITION OF THE LEADS IN RELATION TO THE HEX IS NOT CONTROLLED</p> <p>MAXIMUM RECOMMENDED MOUNTING TORQUE: 15 IN.-LB.</p> <p>ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED</p>	

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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N2987	2N2988	2N2991	2N2992
	2N2989	2N2990	2N2993	2N2994
* Collector-Base Voltage	95 V	155 V	95 V	155 V
* Collector-Emitter Voltage (See Note 1)	80 V	100 V	80 V	100 V
* Emitter-Base Voltage	← 7 V →			
* Continuous Collector Current	← 1 A →			
* Peak Collector Current (See Note 2)	← 1.5 A →			
* Continuous Base Current	← 0.2 A →			
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 10			
* Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 15 W →			
* Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1 W →		← 2 W →	
* Operating Case Temperature Range	← -65°C to 200°C →			
* Storage Temperature Range	← -65°C to 200°C →			
* Lead Temperature 1/8 Inch from Case for 10 Seconds	← 230°C →			

- NOTES: 1. This value applies between 1 mA and 30 mA collector current when the base-emitter diode is open-circuited.
 2. This value applies for $t_{on} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 150 mW/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/deg for the 2N2987 through 2N2990 and 11.4 mW/deg for the 2N2991 through 2N2994.

*Indicates JEDEC registered data

TYPES 2N2987 THRU 2N2994

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N2987	2N2988	2N2989	2N2990	UNIT
		2N2991	2N2992	2N2993	2N2994	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80	100	80	100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = 50 \text{ V}$, $I_B = 0$	0.1		0.1		μA
	$V_{CE} = 90 \text{ V}$, $I_B = 0$		0.1		0.1	
I_{CEV} Collector Cutoff Current	$V_{CE} = 90 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	25		25		nA
	$V_{CE} = 150 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		25		25	
	$V_{CE} = 90 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 175^\circ\text{C}$	15		15		μA
	$V_{CE} = 150 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 175^\circ\text{C}$		15		15	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 7 \text{ V}$, $I_C = 0$	25	25	25	25	nA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ mA}$	20	20	40	40	
	$V_{CE} = 5 \text{ V}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6	25 75	25 75	60 120	60 120	
	$V_{CE} = 5 \text{ V}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	20	20	40	40	
	$V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$, See Notes 5 and 6	25	25	50	50	
	$V_{CE} = 5 \text{ V}$, $I_C = 200 \text{ mA}$, $T_C = -55^\circ\text{C}$, See Notes 5 and 6	10	10	20	20	
V_{BE} Base-Emitter Voltage	$V_{CE} = 5 \text{ V}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6	0.9	0.9	0.9	0.9	V
	$I_B = 20 \text{ mA}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6	1	1	1	1	
	$I_B = 50 \text{ mA}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	1.4	1.4	1.4	1.4	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 20 \text{ mA}$, $I_C = 200 \text{ mA}$, See Notes 5 and 6	0.8	0.8	0.8	0.8	V
	$I_B = 50 \text{ mA}$, $I_C = 500 \text{ mA}$, See Notes 5 and 6	3	3	3	3	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$, $f = 1 \text{ kHz}$	25 85	25 85	50 170	50 170	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$, $f = 30 \text{ MHz}$	1	1	1	1	
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	50	50	50	50	pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*Indicates JEDEC registered data

thermal characteristics

PARAMETER	2N2987 THRU 2N2990	2N2991 THRU 2N2994	UNIT
	MAX	MAX	
θ_{J-C} Junction-to-Case Thermal Resistance	6.67	6.67	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	175	87.5	

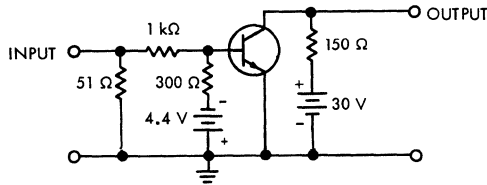
TYPES 2N2987 THRU 2N2994 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

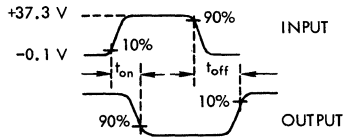
PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 200 \text{ mA}$, $I_{B(1)} = 20 \text{ mA}$, $I_{B(2)} = -20 \text{ mA}$,	0.14	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -3.4 \text{ V}$, $R_L = 150 \Omega$, See Figure 1	2.6	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

- NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPES 2N2987 THRU 2N2994

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

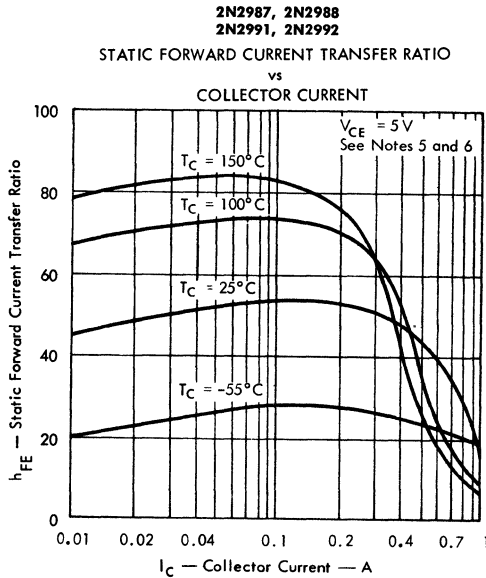


FIGURE 2

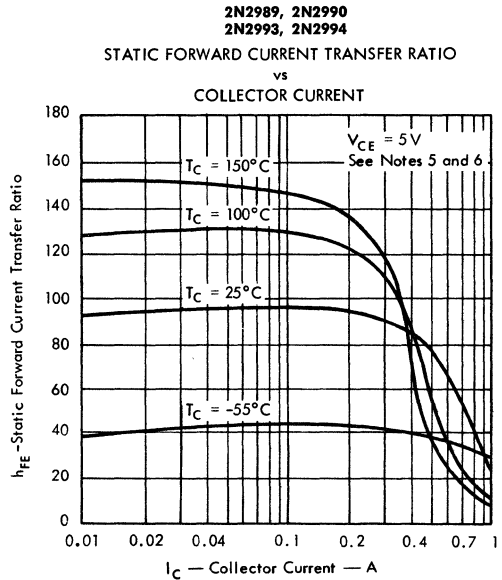


FIGURE 3

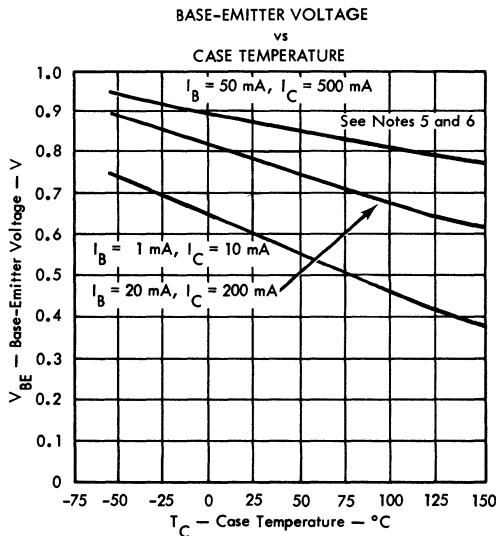


FIGURE 4

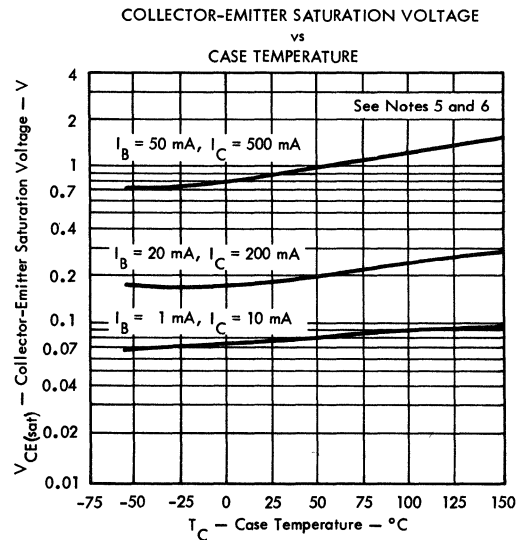


FIGURE 5

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300\ \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N2987 THRU 2N2994 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

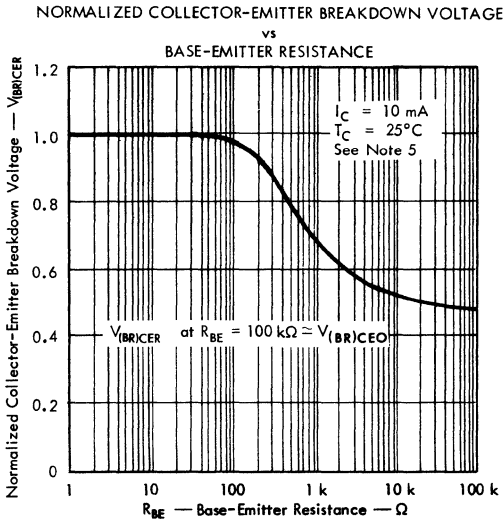


FIGURE 6

2N2987, 2N2988
2N2991, 2N2992

SMALL-SIGNAL COMMON-EMITTER
FORWARD CURRENT TRANSFER RATIO
vs
FREQUENCY

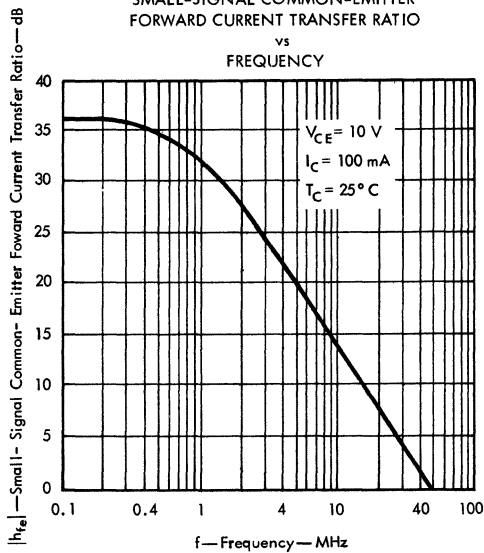


FIGURE 8

NOTE 5: This parameter must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

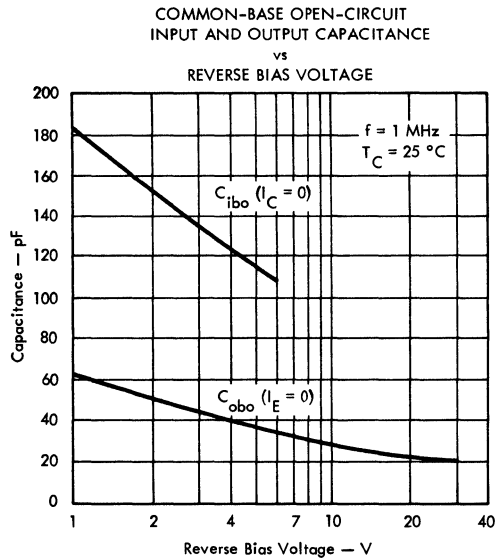


FIGURE 7

2N2989, 2N2990
2N2993, 2N2994

SMALL-SIGNAL COMMON-EMITTER
FORWARD CURRENT TRANSFER RATIO
vs
FREQUENCY

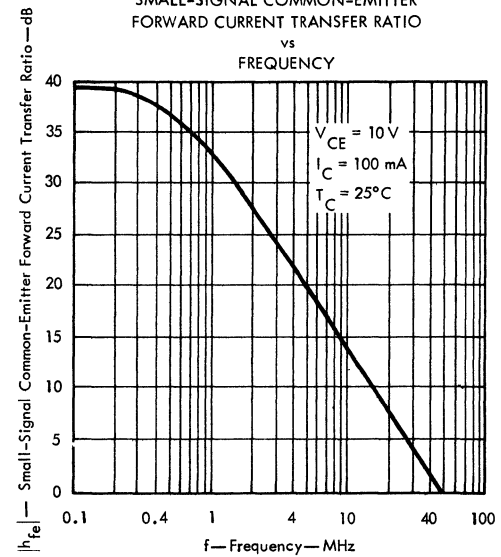


FIGURE 9

TYPES 2N2987 THRU 2N2994 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGION

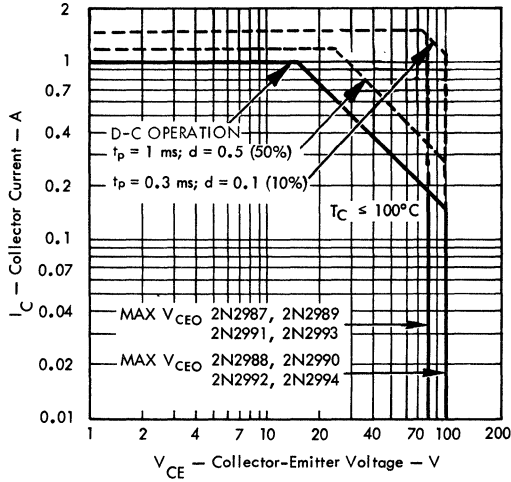


FIGURE 10

THERMAL INFORMATION

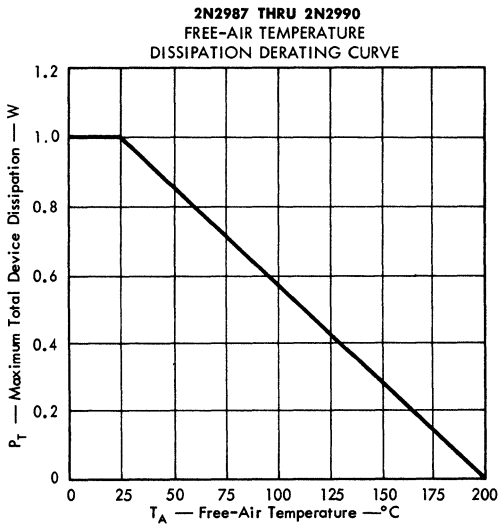


FIGURE 11

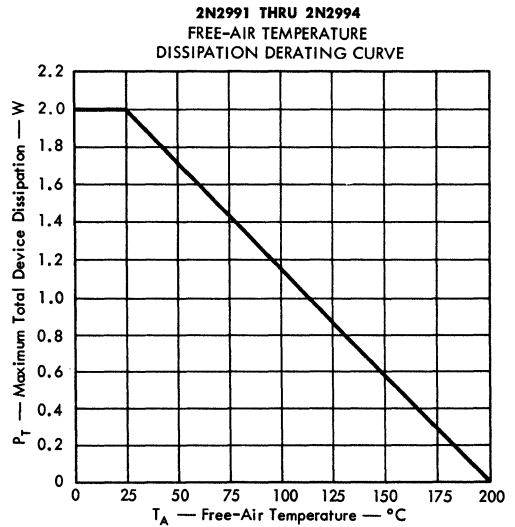


FIGURE 12

TYPES 2N2987 THRU 2N2994 N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

THERMAL INFORMATION

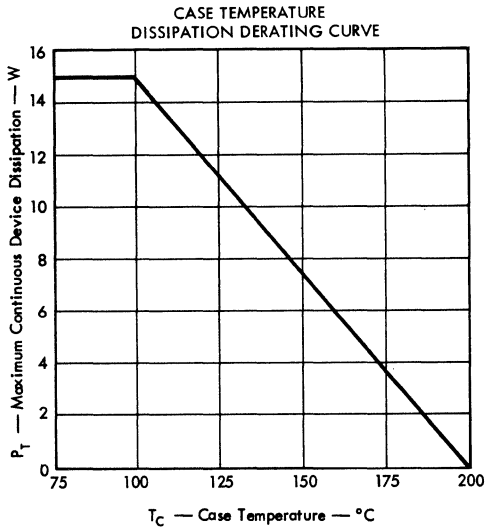


FIGURE 13

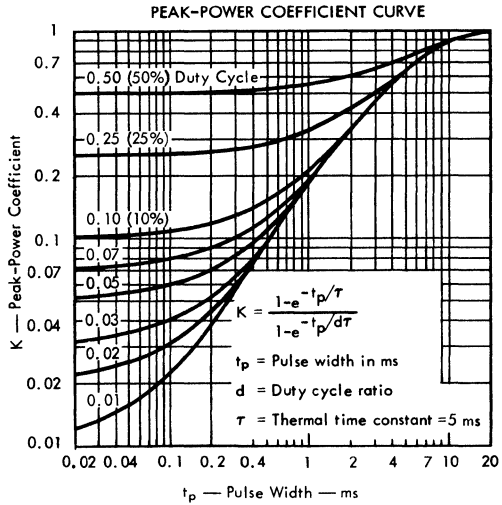


FIGURE 14

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE		UNIT
		2N2987 THRU 2N2990	2N2991 THRU 2N2994	
$P_{T(av)}$	Average Power Dissipation			W
$P_{T(max)}$	Peak Power Dissipation			W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	87.5	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	6.67	6.67	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168	81	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance			deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance			deg/W
T_A	Free-Air Temperature			°C
T_C	Case Temperature			°C
$T_{J(av)}$	Average Junction Temperature	≤ 200		°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200		°C
K	Peak-Power Coefficient	See Figure 14		
t_p	Pulse Width			ms
t_x	Pulse Period			ms
d	Duty-Cycle Ratio (t_p/t_x)			

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C} \text{ as in figure 13}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 7 \text{ deg/W (from information supplied with heat sink)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Solution:

From Figure 14, Peak-Power Coefficient

$$K = 0.11 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + 0.11(6.67)} = 105 \text{ W}$$

TYPES 2N3021 THRU 2N3026 P-N-P SILICON POWER TRANSISTORS

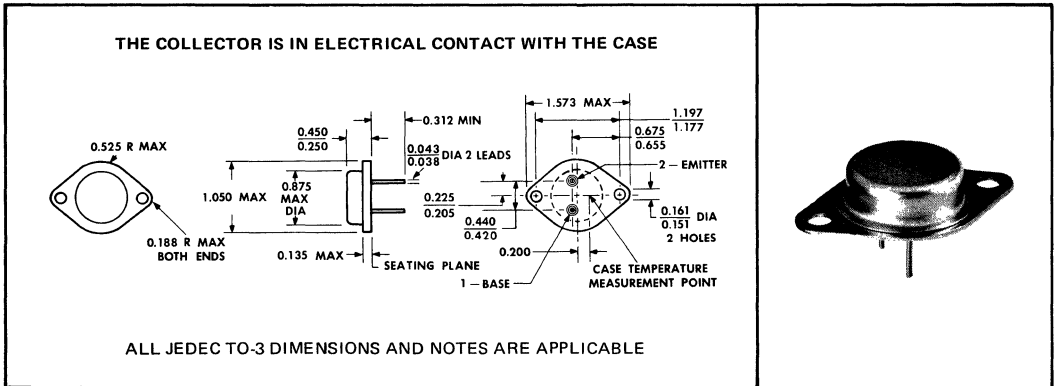
FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Max t_{off} 400 ns at $I_C = 1$ A
- 3-A Rated Continuous Collector Current
- 25 Watts at 25°C Case Temperature
- Min f_T of 60 MHz at 15 V, 0.5 A

*mechanical data

TYPES 2N3021 THRU 2N3026
BULLETIN NO. DL-S-7111596, DECEMBER 1971

5



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3021	2N3022	2N3023	2N3024	2N3025	2N3026
Collector-Base Voltage	-30 V	-45 V	-60 V	-30 V	-45 V	-60 V
Collector-Emitter Voltage (See Note 1)	-30 V	-45 V	-60 V	-30 V	-45 V	-60 V
Emitter-Base Voltage	-4 V	-4 V	-4 V	-4 V	-4 V	-4 V
Continuous Collector Current	← -3 A →					
Continuous Base Current	← -0.5 A →					
Safe Operating Areas at (or below) 25°C Case Temperature	See Figures 3 thru 5					
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 25 W →					
Operating Collector Junction Temperature Range	-65°C to 175°C					
Storage Temperature Range	-65°C to 175°C					
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 250°C →					

NOTES: 1. These values apply when the base-emitter diode is open-circuited.
2. For operation above 25°C case temperature, refer to Dissipation Derating Curve, Figure 6.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N3021 THRU 2N3026

P-N-P SILICON POWER TRANSISTORS

*electrical characteristics of 2N3021, 2N3022, 2N3023 at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		2N3021	2N3022	2N3023	UNIT
			MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage		See Note 3	-30			V
				-45		
					-60	
I_{CEV} Collector Cutoff Current			-0.2			mA
				-0.2		
					-0.2	
			-2			
				-2		
I_{EBO} Emitter Cutoff Current			-1	-1	-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 V, I_C = 1 A,$	See Notes 3 and 4	20 60	20 60	20 60	
V_{BE} Base-Emitter Voltage	$I_C = -3 A, I_B = -0.3 A,$	See Notes 3 and 4	-1.5	-1.5	-1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_C = -3 A, I_B = -0.3 A,$	See Notes 3 and 4	-1.5	-1.5	-1.5	V
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -15 V, I_C = -0.5 A, f = 30 MHz$		2	2	2	

*electrical characteristics of 2N3024, 2N3025, 2N3026 at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		2N3024	2N3025	2N3026	UNIT
			MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage		See Note 3	-30			V
				-45		
					-60	
I_{CEV} Collector Cutoff Current			-0.2			mA
				-0.2		
					-0.2	
			-2			
				-2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -4 V, I_C = 0$		-1	-1	-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 V, I_C = 1 A,$	See Notes 3 and 4	50 180	50 180	50 180	
V_{BE} Base-Emitter Voltage	$I_C = -3 A, I_B = -0.3 A,$	See Notes 3 and 4	-1.5	-1.5	-1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_C = -3 A, I_B = -0.3 A,$	See Notes 3 and 4	-1	-1	-1	V
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -15 V, I_C = -0.5 A, f = 30 MHz$		2	2	2	

NOTES: 3. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

TYPES 2N3021 THRU 2N3026 P-N-P SILICON POWER TRANSISTORS

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = -1 \text{ A}$, $R_L = 12 \Omega$, $I_B(1) = -0.1 \text{ A}$, See Figure 1	100	ns
t_s Storage Time	$I_C = -1 \text{ A}$, $I_B(1) = -0.1 \text{ A}$, $I_B(2) = 0.1 \text{ A}$	325	
t_f Fall Time	$R_L = 12 \Omega$, See Figure 2	75	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION

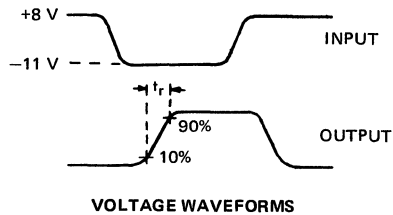
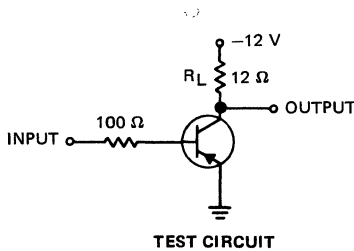


FIGURE 1—RISE TIME

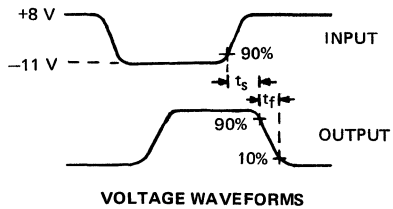
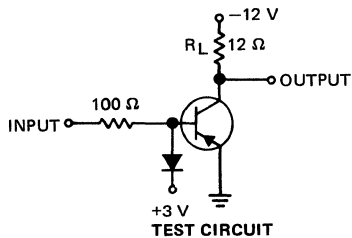


FIGURE 2—STORAGE AND FALL TIMES

- NOTES: a. The input waveforms are supplied by a generator with the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 10 \mu\text{s}$, $Z_{out} = 50 \Omega$, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5 \text{ ns}$, $R_{in} \geq 10 \text{ k}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

* JEDEC registered data

TYPES 2N3021 THRU 2N3026 P-N-P SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

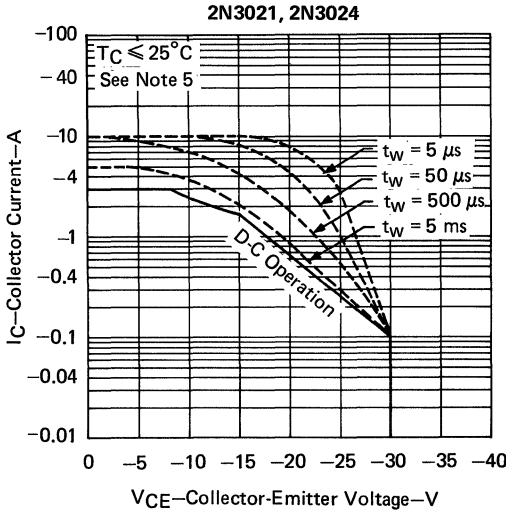


FIGURE 3

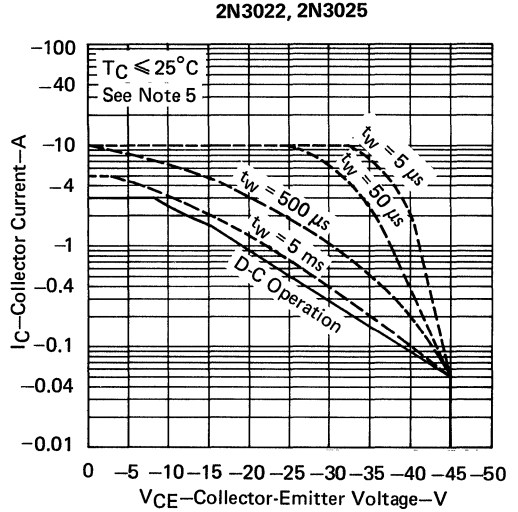


FIGURE 4

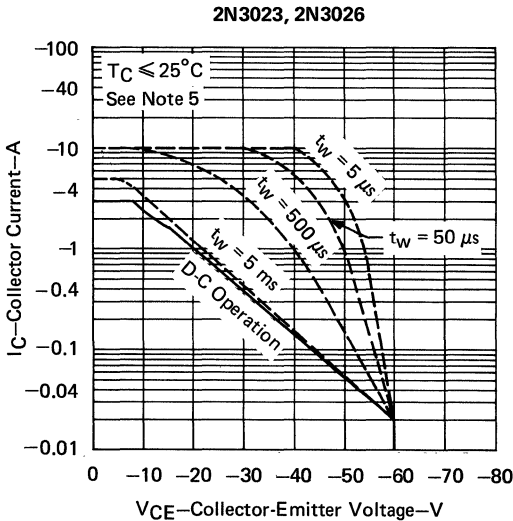


FIGURE 5

NOTE 5: Areas defined by dashed lines apply for nonrepetitive-pulse operation. The pulse may be repeated after the device has regained thermal equilibrium.

THERMAL INFORMATION

CASE TEMPERATURE DISSIPATION DERATING CURVE

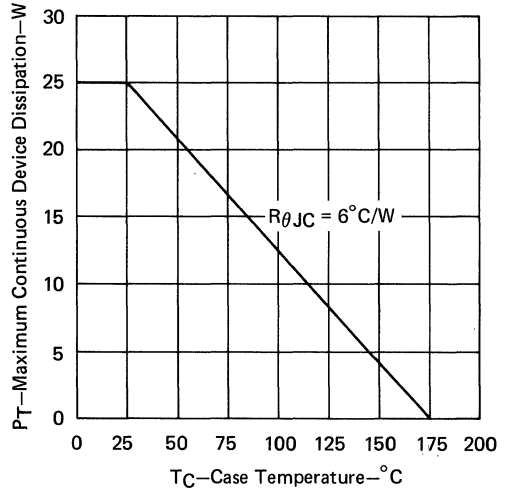


FIGURE 6

TYPE 2N3055

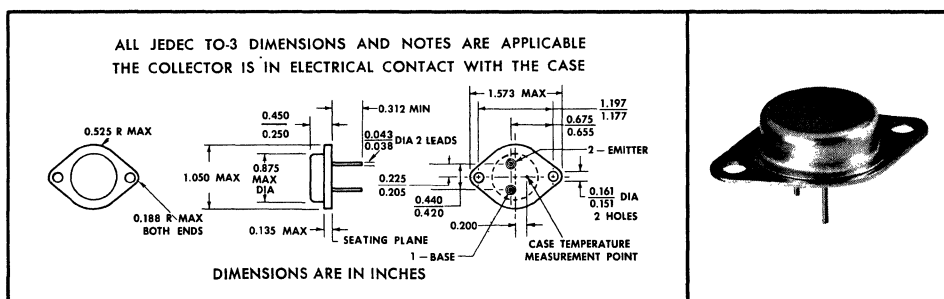
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

TYPE 2N3055
 BULLETIN NO. DL-S-719659, AUGUST 1967
 REVISED DECEMBER 1971

FOR POWER-AMPLIFIER APPLICATIONS

- 115 W at 25°C Case Temperature
- Max I_C of 15 A
- Min f_{hfe} of 20 kHz

***mechanical data**



5

***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 1)	70 V
Emitter-Base Voltage	7 V
Continuous Collector Current	15 A
Continuous Base Current	7 A
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	115 W
Operating Case Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/2 Inch from Case for 10 Seconds	235°C

NOTES: 1. This value applies when the base-emitter resistance $R_{BE} = 100 \Omega$.

2. Derate linearly to 200°C case temperature at the rate of 0.66 W/deg.

*Indicates JEDEC registered data

TYPE 2N3055

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 4	60		V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $R_{BE} = 100 \Omega$	70		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$		0.7	mA
I_{CEV}	Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		5	mA
		$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		30	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 7 \text{ V}$, $I_C = 0$		5	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, See Notes 3 and 4	20	70	
		$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 3 and 4	5		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, See Notes 3 and 4		1.8	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 400 \text{ mA}$, $I_C = 4 \text{ A}$, See Notes 3 and 4		1.1	V
		$I_B = 3.3 \text{ A}$, $I_C = 10 \text{ A}$, See Notes 3 and 4		8	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	15	60	
f_{hfe}	Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Note 5	10		kHz

NOTES: 3. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

5. f_{hfe} is the frequency at which the magnitude of the small-signal forward current transfer ratio is 0.707 of its low-frequency value. For this device, the reference measurement is made at 1 kHz.

*Indicates JEDEC registered data

thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	1.52	deg/W

PRINTED IN U.S.A.

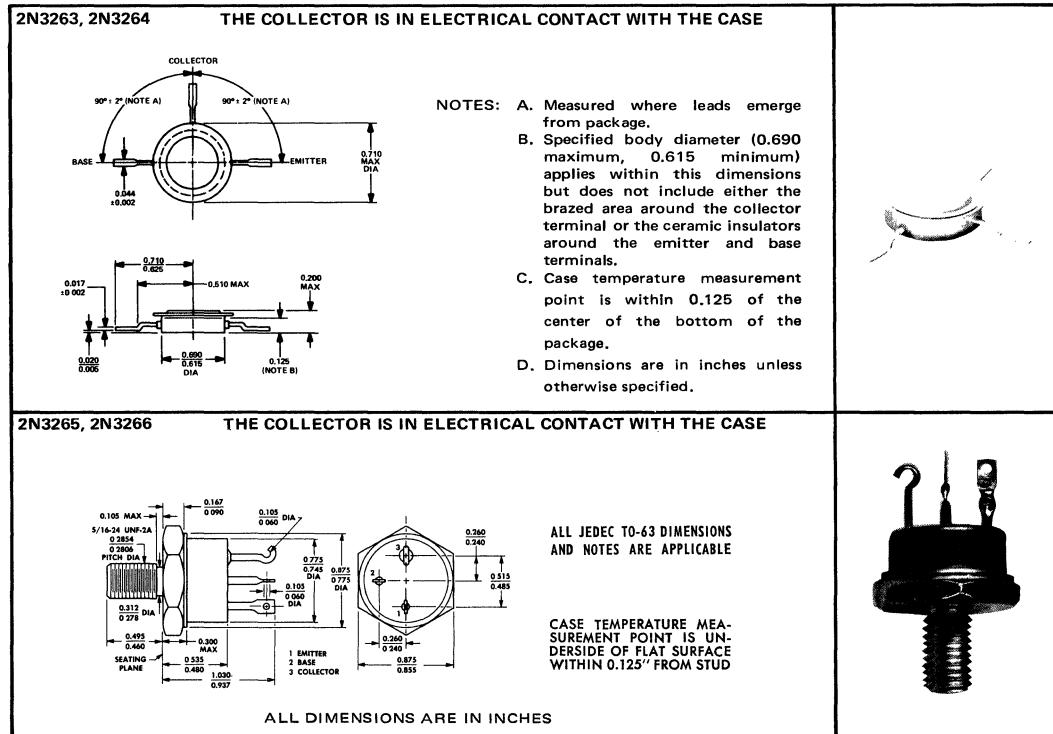
1271

TYPES 2N3263, 2N3264, 2N3265, 2N3266 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED SWITCHING APPLICATIONS

• Min $f_T = 20$ MHz

*mechanical data



TYPES 2N3263, 2N3264, 2N3265, 2N3266
BULLETIN NO. DLS-711502, JUNE 1971
REVISED SEPTEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3263	2N3264	2N3265	2N3266
* Collector-Emitter Voltage ($V_{BE} = -1.5$ V, See Note 1)	150 V	120 V	150 V	120 V
* Collector-Emitter Voltage (Base Open, See Note 1)	90 V	60 V	90 V	60 V
* Emitter-Base Voltage	← 7 V →			
* Continuous Collector Current	← 25 A →			
* Continuous Base Current	← 10 A →			
* Safe Operating Area at Specified Temperatures	← See Figures 6 and 7 →			
* Continuous Device Dissipation at (or below) 75°C Case Temperature (See Note 2)	83.3 W	83.3 W	125 W	125 W
* Continuous Device Dissipation at 100°C Case Temperature (See Note 2)	66.7 W	66.7 W	100 W	100 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	1.2 W	1.2 W	4 W	4 W
* Unclamped Inductive Load Energy (See Note 4)	← 2 mJ →			
* Operating Collector Junction Temperature Range	← -65°C to 200°C →			
* Storage Temperature Range	← -65°C to 200°C →			
Lead or Terminal Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

NOTES:

- These values apply only when the collector-emitter voltage is applied with the transistor in the off-state with the base-emitter diode reverse-biased or open-circuited, as specified. In operation, the limitations of Figure 6 or 7, as applicable, must be observed.
- For operation above 75°C case temperature, refer to Dissipation Derating Curve, Figure 8.
- For operation above 25°C free-air temperature refer to Dissipation Derating Curve, Figure 9.
- This rating is based on the capability of the transistor to operate safely in the circuit of Figure 5. $L = 40 \mu\text{H}$, $R_{BB2} = 20 \Omega$, $V_{BB2} = 6$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N3263, 2N3264, 2N3265, 2N3266

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3263		2N3264		UNIT
		2N3265	MIN	MAX	MIN	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 5	90			60	V
I_{CEV} Collector Cutoff Current	$V_{CE} = 120 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			20		mA
	$V_{CE} = 150 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		20			
	$V_{CE} = 120 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 125^\circ\text{C}$				20	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 7 \text{ V}$, $I_C = 0$	5			15	mA
	$V_{CE} = 3 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6				20	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	20	55			
	$V_{BE} = 2 \text{ A}$, $I_C = 20 \text{ A}$, See Notes 5 and 6	1.8			2.2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 2 \text{ A}$, $I_C = 20 \text{ A}$, See Notes 5 and 6		1		1.6	V
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 3 \text{ A}$, $f = 5 \text{ MHz}$	4			4	

5

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	2N3263		2N3264		UNIT
		2N3265	MAX	MAX	MAX	
t_r Rise Time	$I_C = 15 \text{ A}$, $I_B(1) = 1.2 \text{ A}$, $I_B(2) = -1.2 \text{ A}$, $V_{BE(off)} = -6.3 \text{ V}$, $R_L = 2 \Omega$, See Figure 4	0.5			0.5	μs
t_s Storage Time		1.5			1.5	
t_f Fall Time		0.5			0.5	
t_{on} Turn-On Time		0.5			0.5	
t_{off} Turn-Off Time		2			2	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

TYPICAL CHARACTERISTICS

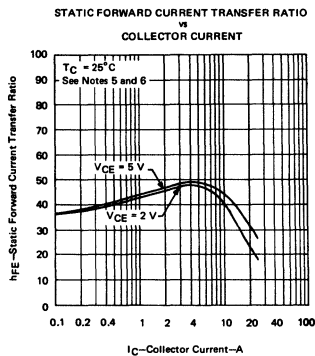


FIGURE 1

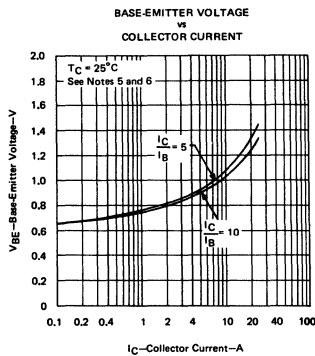


FIGURE 2

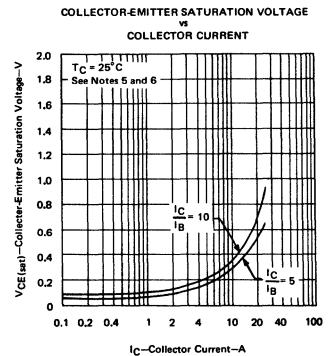


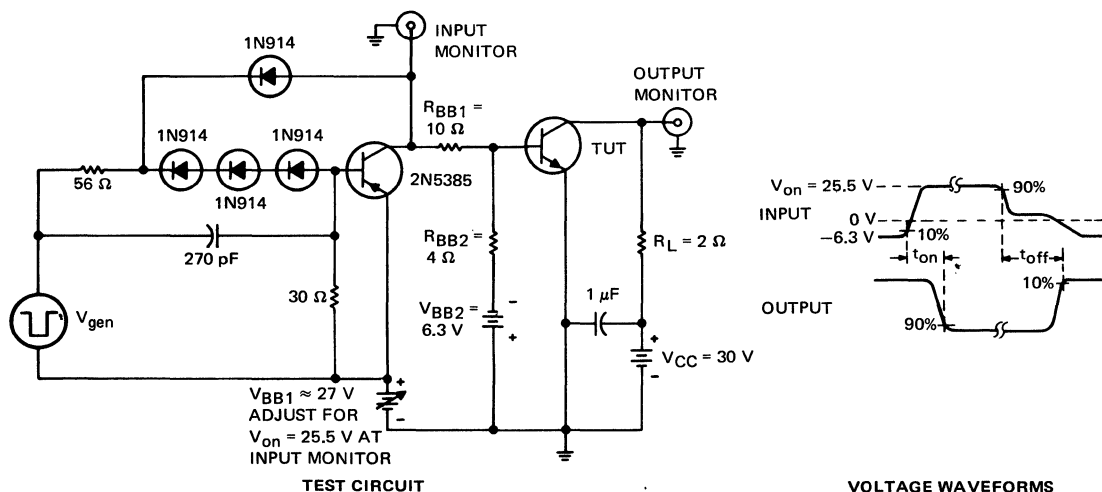
FIGURE 3

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N3263, 2N3264, 2N3265, 2N3266 N-P-N SILICON POWER TRANSISTORS

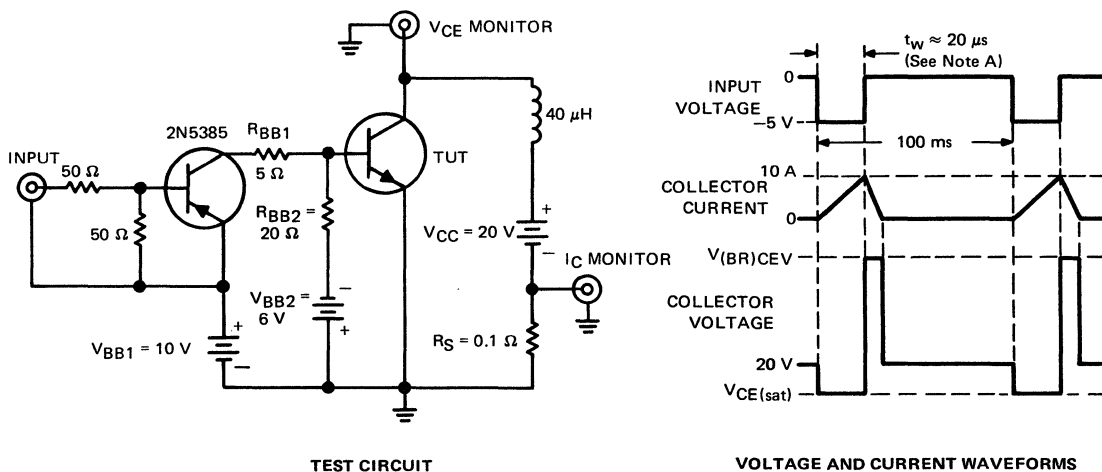
PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - D. Resistors must be noninductive types.
 - E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 4

INDUCTIVE LOAD SWITCHING



NOTE A: Input pulse width is increased until $I_{CM} = 10\text{ A}$.

FIGURE 5

TYPES 2N3263, 2N3264, 2N3265, 2N3266 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREA

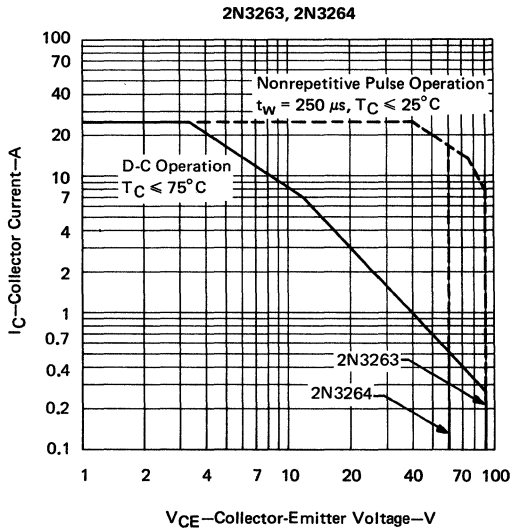


FIGURE 6

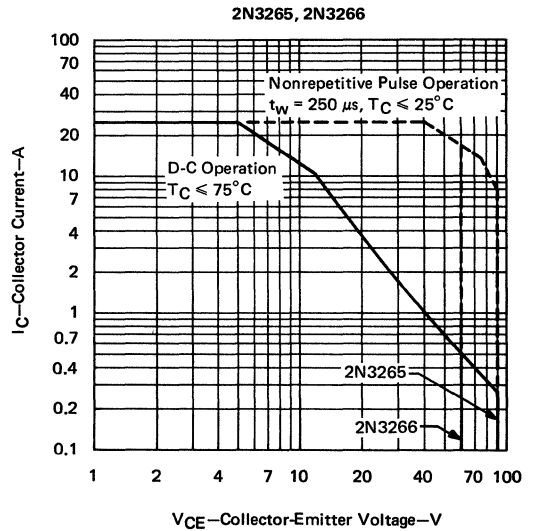


FIGURE 7

THERMAL INFORMATION

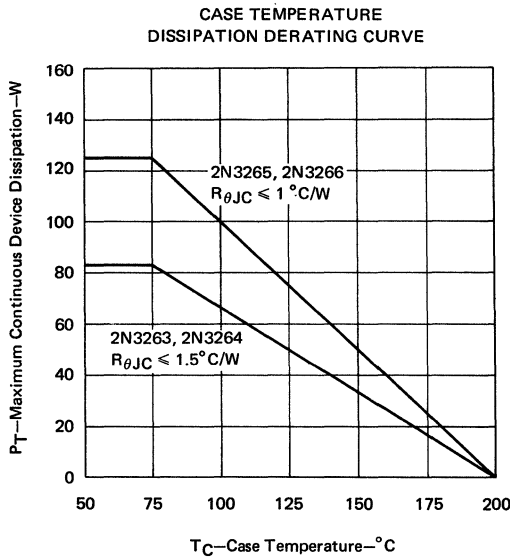


FIGURE 8

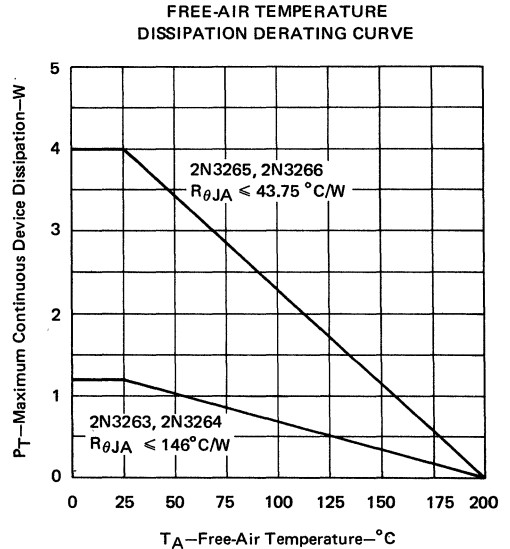


FIGURE 9

TYPES 2N3418, 2N3419, 2N3420, 2N3421 N-P-N EPITAXIAL PLANAR SILICON MEDIUM-POWER TRANSISTORS

TYPES 2N3418, 2N3419, 2N3420, 2N3421
BULLETIN NO. DL-5 685521, JUNE 1964
REVISED MAY 1968

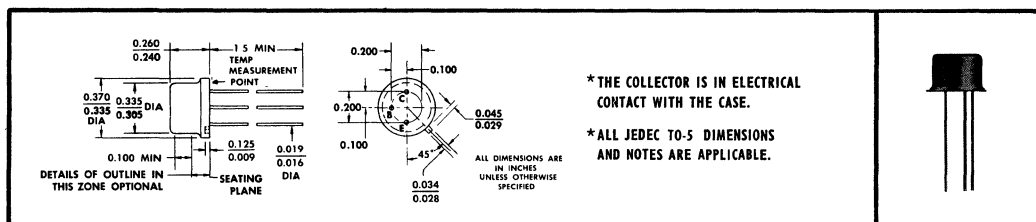
HIGH-FREQUENCY MEDIUM-POWER TRANSISTORS

Formerly TIX3033, TIX3034, TIX3035, TIX3036

- High-Power Dissipation in TO-5 Package: 15 watts at $T_c = 100^\circ\text{C}$
- Low-Leakage Current: $0.5 \mu\text{a}$ at max voltage
- Low-Saturation Voltage: $V_{CE(sat)} = 0.25 \text{ v max}$ at $I_c = 1 \text{ a}$
- High f_T : 40 Mc min at 10 v, 100 ma

mechanical data

These transistors are in precision welded, hermetically sealed enclosures. Extreme cleanliness during the assembly process prevents sealed-in contamination. The approximate unit weight is 1.8 grams.



5

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3418	2N3419
	2N3420	2N3421
Collector-Base Voltage	85 v	125 v
Collector-Emitter Voltage (See Note 1)	60 v	80 v
Emitter-Base Voltage	← 8 v →	← 8 v →
Collector Current, Continuous	← 3 a →	← 3 a →
Collector Current, Peak (See Note 2)	← 5 a →	← 5 a →
Base Current	← 1 a →	← 1 a →
Safe Operating Region	See Figures 8 and 9	
Total Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 15 w →	← 15 w →
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1 w →	← 1 w →
Operating Case Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 230°C →	← 230°C →

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $PW \leq 1 \text{ msec}$, Duty Cycle $\leq 50\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.15 w/C°.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.72 mw/C°.

*Indicates JEDEC registered data.

TYPES 2N3418, 2N3419, 2N3420, 2N3421

N-P-N EPITAXIAL PLANAR SILICON MEDIUM-POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3418		2N3419		2N3420		2N3421		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = 50 \text{ ma}$, $I_B = 0$, See Note 5	60		80		60		80		v
I_{CEX} Collector Cutoff Current	$V_{CE} = 80 \text{ v}$, $V_{BE} = -0.5 \text{ v}$	0.5				0.5				μa
	$V_{CE} = 120 \text{ v}$, $V_{BE} = -0.5 \text{ v}$			0.5				0.5		μa
	$V_{CE} = 80 \text{ v}$, $V_{BE} = -0.5 \text{ v}$, $T_C = 150^\circ\text{C}$	50				50				μa
	$V_{CE} = 120 \text{ v}$, $V_{BE} = -0.5 \text{ v}$, $T_C = 150^\circ\text{C}$			50				50		μa
I_{EBO} Emitter Cutoff Current	$V_{EB} = 6 \text{ v}$, $I_C = 0$	500		500		500		500		na
	$V_{EB} = 8 \text{ v}$, $I_C = 0$	10		10		10		10		μa
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ v}$, $I_C = 100 \text{ ma}$, See Notes 5 and 6	20		20		40		40		
	$V_{CE} = 2 \text{ v}$, $I_C = 1 \text{ a}$, See Notes 5 and 6	20	60	20	60	40	120	40	120	
	$V_{CE} = 2 \text{ v}$, $I_C = 2 \text{ a}$, See Notes 5 and 6	15		15		30		30		
	$V_{CE} = 5 \text{ v}$, $I_C = 5 \text{ a}$, See Notes 5 and 6	10		10		15		15		
	$V_{CE} = 2 \text{ v}$, $I_C = 1 \text{ a}$, $T_C = -55^\circ\text{C}$ See Notes 5 and 6	10		10		10		10		
V_{BE} Base-Emitter Voltage	$I_B = 100 \text{ ma}$, $I_C = 1 \text{ a}$, See Notes 5 and 6	0.6	1.2	0.6	1.2	0.6	1.2	0.6	1.2	v
	$I_B = 200 \text{ ma}$, $I_C = 2 \text{ a}$, See Notes 5 and 6	0.7	1.4	0.7	1.4	0.7	1.4	0.7	1.4	v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ ma}$, $I_C = 1 \text{ a}$, See Notes 5 and 6	0.25		0.25		0.25		0.25		v
	$I_B = 200 \text{ ma}$, $I_C = 2 \text{ a}$, See Notes 5 and 6	0.5		0.5		0.5		0.5		v
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ v}$, $I_C = 100 \text{ ma}$, $f = 20 \text{ Mc}$	2		2		2		2		
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ v}$, $I_E = 0$, $f = 1 \text{ Mc}$	150		150		150		150		pf

NOTES: 5. These parameters must be measured using pulse techniques. $PW = 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts located 0.25 in. from the header of the transistor. Voltage-sensing contacts are separate from current-carrying contacts.

*switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS†	TYP	MAX	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ a}$, $I_{B(1)} = 100 \text{ ma}$, $I_{B(2)} = -100 \text{ ma}$,	165	300	nsec
t_{off} Turn-Off Time	$V_{BE(off)} = -3.7 \text{ v}$, $R_L = 20 \Omega$, See Figure 10	540	1200	
t_{on} Turn-On Time	$I_C = 2 \text{ a}$, $I_{B(1)} = 200 \text{ ma}$, $I_{B(2)} = -200 \text{ ma}$,	200		
t_{off} Turn-Off Time	$V_{BE(off)} = -4.7 \text{ v}$, $R_L = 20 \Omega$, See Figure 10	350		

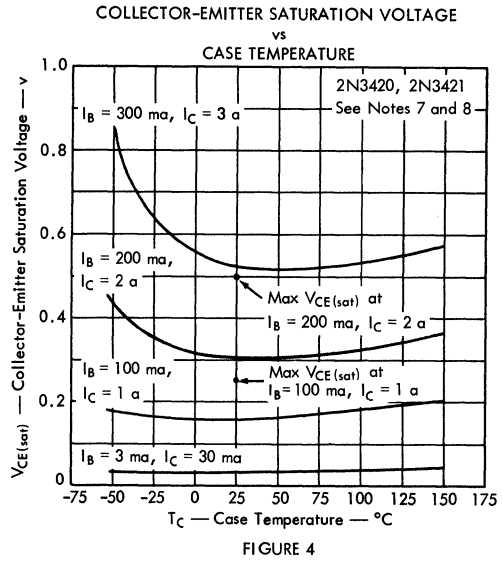
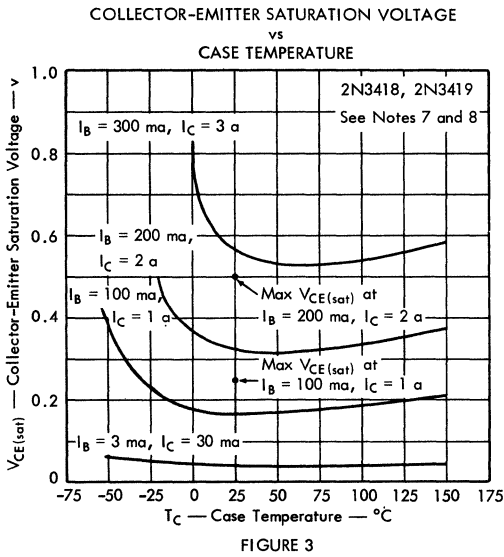
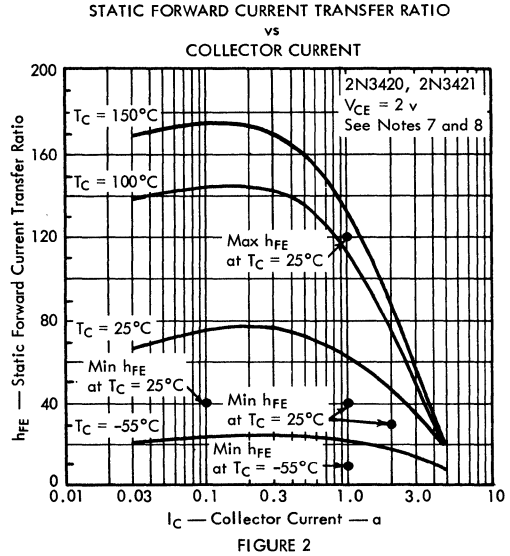
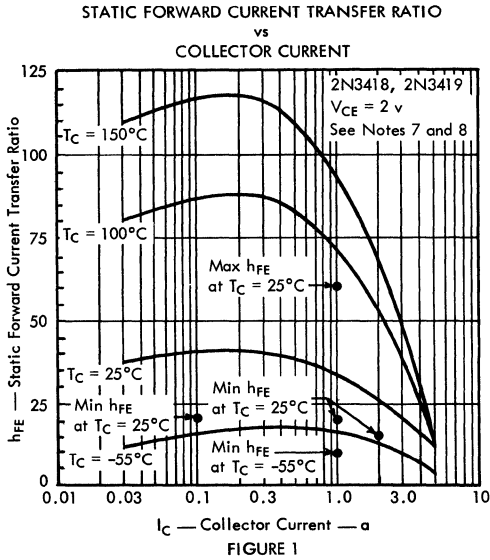
†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*Indicates JEDEC registered data

TYPES 2N3418, 2N3419, 2N3420, 2N3421

N-P-N EPITAXIAL PLANAR SILICON MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS



NOTES: 7. These parameters were measured using pulse techniques. $PW = 300 \mu\text{sec}$. Duty Cycle $\leq 2\%$.

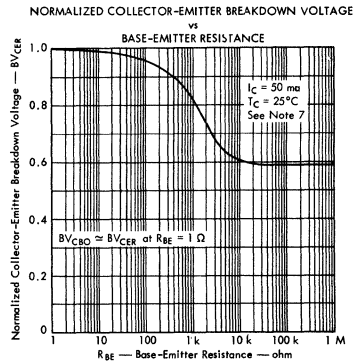
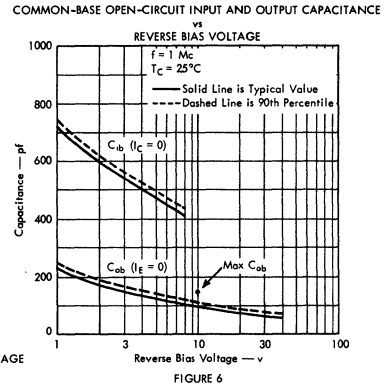
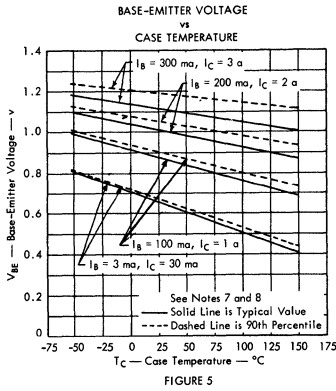
8. Separate voltage-sensing and current-carrying contacts were used.

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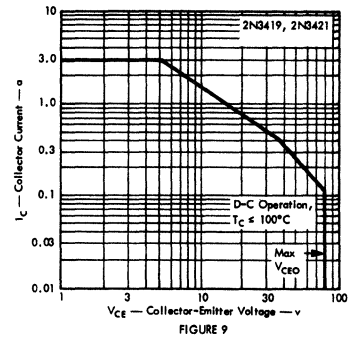
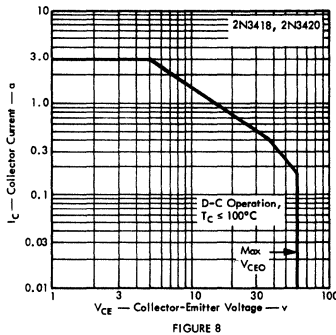
TYPES 2N3418, 2N3419, 2N3420, 2N3421

N-P-N EPITAXIAL PLANAR SILICON MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

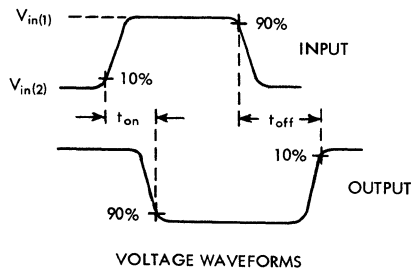
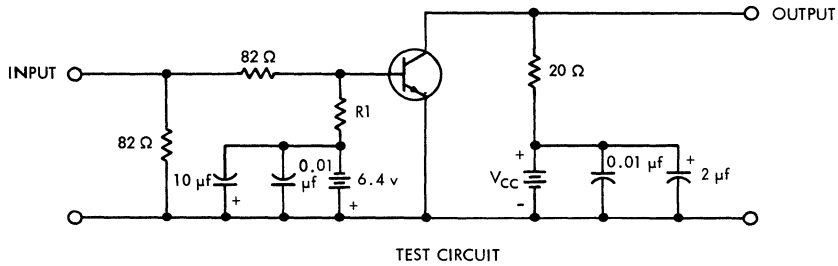


MAXIMUM SAFE OPERATING REGION



TYPES 2N3418, 2N3419, 2N3420, 2N3421 N-P-N EPITAXIAL PLANAR SILICON MEDIUM-POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



Nominal I_C	R1	V _{CC}	V _{in(1)}	V _{in(2)}
1 a	82 Ω	20.3 v	+16.0 v	-1.0 v
2 a	41 Ω	40.5 v	+32.0 v	-1.3 v

CIRCUIT CONDITIONS

FIGURE 10

- NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ nsec, $t_f \leq 15$ nsec, $Z_{out} = 50 \Omega$, $PW = 2 \mu\text{sec}$, Duty Cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ nsec, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5$ pf.
- c. Resistors must be non-inductive types.

TYPES 2N3418, 2N3419, 2N3420, 2N3421 N-P-N EPITAXIAL PLANAR SILICON MEDIUM-POWER TRANSISTORS

THERMAL INFORMATION

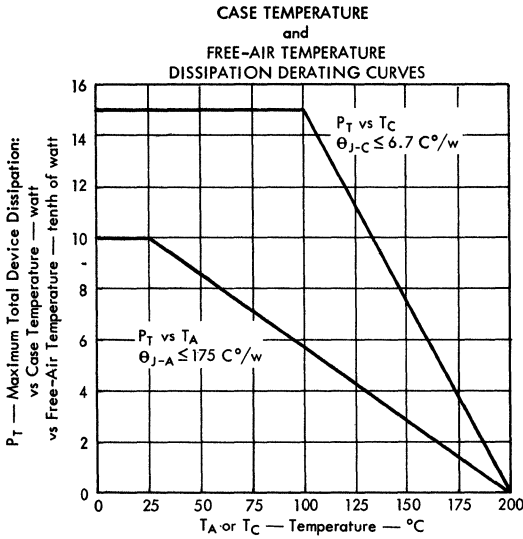


FIGURE 11

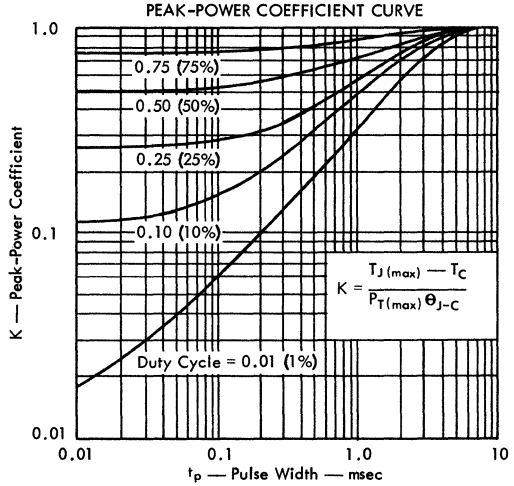


FIGURE 12

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		w
$P_{T(max)}$	Peak Power Dissipation		w
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	$^{\circ}\text{C}/\text{w}$
θ_{J-C}	Junction-to-Case Thermal Resistance	6.67	$^{\circ}\text{C}/\text{w}$
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168.33	$^{\circ}\text{C}/\text{w}$
θ_{C-HS}	Case-to-Heat Sink Thermal Resistance		$^{\circ}\text{C}/\text{w}$
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		$^{\circ}\text{C}/\text{w}$
T_A	Free-Air Temperature		$^{\circ}\text{C}$
T_C	Case Temperature		$^{\circ}\text{C}$
$T_{J(av)}$	Average Junction Temperature	≤ 200	$^{\circ}\text{C}$
$T_{J(max)}$	Peak Junction Temperature	≤ 200	$^{\circ}\text{C}$
K	Peak-Power Coefficient	See Figure 12	
t_p	Pulse Width		msec
t_x	Pulse Period		msec
d	Duty Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C-HS} + \theta_{HS-A} = 7^{\circ}\text{C}/\text{w}$ (From information supplied with heat sink.)

$T_{J(av)}$ (design limit) = 200°C

$T_A = 50^{\circ}\text{C}$

$d = 10\%$ (0.1)

$t_p = 0.1$ msec

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^{\circ}\text{C} \leq T_C \leq 200^{\circ}\text{C}, \text{ as in Figure 11}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^{\circ}\text{C} \leq T_A \leq 200^{\circ}\text{C}, \text{ as in Figure 11}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}} \text{ for } 100^{\circ}\text{C} \leq T_C \leq 200^{\circ}\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d \theta_{C-A} + K \theta_{J-C}} \text{ for } 25^{\circ}\text{C} \leq T_A \leq 200^{\circ}\text{C}$$

Solution:

From Figure 12, Peak-Power Coefficient

$K = 0.155$ and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}}$$

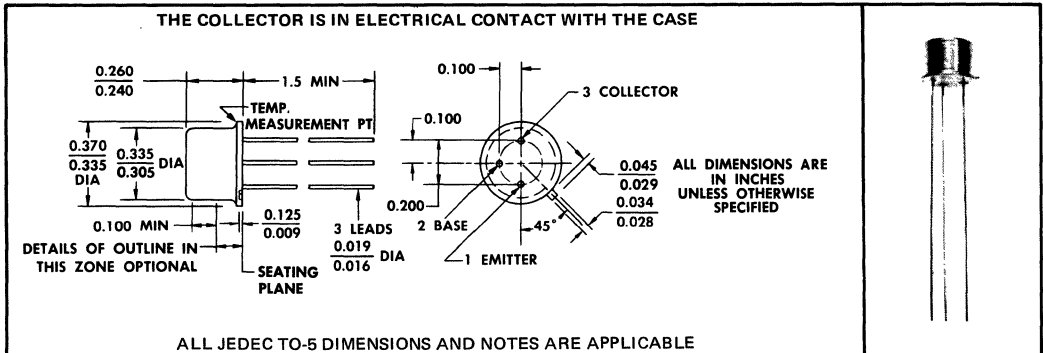
$$P_{T(max)} = \frac{200 - 50}{0.1(7) + 0.155(6.67)} = 86 \text{ w}$$

TYPES 2N3439, 2N3440 N-P-N SILICON POWER TRANSISTORS

HIGH-VOLTAGE POWER TRANSISTORS DESIGNED FOR INDUSTRIAL AND MILITARY APPLICATIONS

- Min $V_{(BR)CEO}$ of 350 V (2N3439)
- Max $V_{CE(sat)}$ of 0.5 V at $I_C = 50$ mA
- Min f_T of 15 MHz at 10 V, 20 mA
- 1 A Continuous Collector Current
- 5 W at $T_C = 25^\circ\text{C}$

*mechanical data



TYPES 2N3439, 2N3440
BULLETIN NO. DL-S-7111476, MAY 1971

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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3439	2N3440
* Collector-Base Voltage	450 V	300 V
* Collector-Emitter Voltage (See Note 1)	350 V	250 V
* Emitter-Base Voltage	← 7 V →	
* Continuous Collector Current	← 1 A →	
Peak Collector Current (See Note 2)	← 1.5 A →	
* Continuous Base Current	← 0.5 A →	
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 5	
* Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 5 W →	
* Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1 W →	
Operating Collector Junction Temperature Range	-65°C to 200°C	
* Storage Temperature Range	-65°C to 200°C	
* Lead Temperature 1/16 Inch from Case for 10 Seconds	← 255°C →	

- NOTES: 1. These values apply between 0 and 50 mA collector current when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 28.6 mW/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.71 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N3439, 2N3440

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	2N3439		2N3440		UNIT
		MIN	MAX	MIN	MAX	
V _{(BR)CBO} Collector-Base Breakdown Voltage	I _C = 500 μA, I _E = 0	450		300		V
*V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = 50 mA, I _B = 0, See Note 5	350		250		V
*I _{CBO} Collector Cutoff Current	V _{CB} = 360 V, I _E = 0		20			μA
	V _{CB} = 250 V, I _E = 0			20		
*I _{EBO} Emitter Cutoff Current	V _{EB} = 6 V, I _C = 0		20	20		μA
*h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 20 mA, See Note 5	40	160	40	160	
*V _{BE} Base-Emitter Voltage	I _B = 4 mA, I _C = 50 mA, See Note 5		1.3	1.3		V
*V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 4 mA, I _C = 50 mA, See Note 5		0.5	0.5		V
*h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 5 mA, f = 1 kHz	25		25		
* h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 20 mA, f = 5 MHz	3		3		
*C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 1 MHz		10	10		pF
*C _{iBo} Common-Base Open-Circuit Input Capacitance	V _{EB} = 5 V, I _C = 0, f = 1 MHz		75	75		pF
*h _{ie(real)} Real Part of Small-Signal Common-Emitter Input Impedance	V _{CE} = 10 V, I _C = 5 mA, f = 1 MHz	300		300		Ω

NOTE 5: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

thermal characteristics

PARAMETER	MAX	UNIT
R _{θJC} Junction-to-Case Thermal Resistance	35	°C/W
R _{θJA} Junction-to-Free-Air Thermal Resistance	175	

switching characteristics at 25°C case temperature

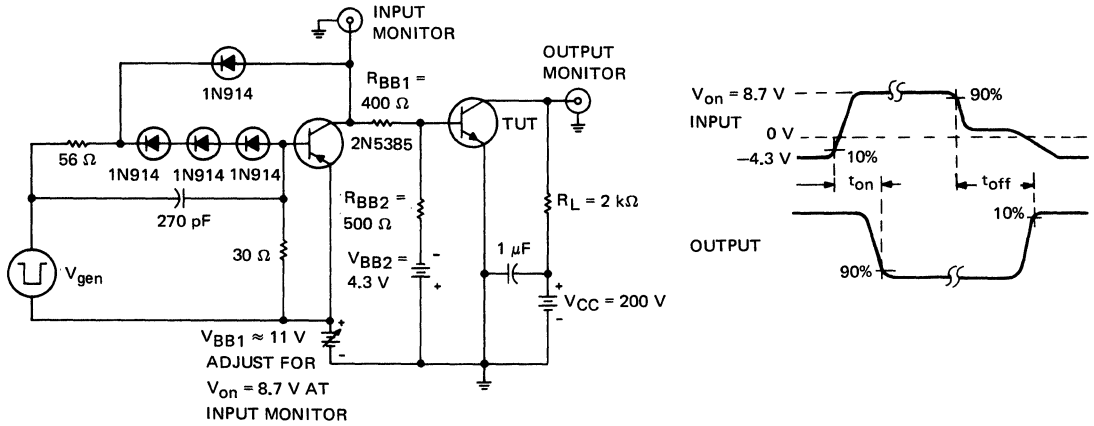
PARAMETER	TEST CONDITIONS†	TYP	UNIT
t _{on} Turn-On Time	I _C = 100 mA, I _{B(1)} = 10 mA, I _{B(2)} = -10 mA, V _{BE(off)} = -4.3 V, R _L = 2 kΩ, See Figure 1	0.3	μs
t _{off} Turn-Off Time		2.9	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

TYPES 2N3439, 2N3440 N-P-N SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. V_{gen} is a -30 V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

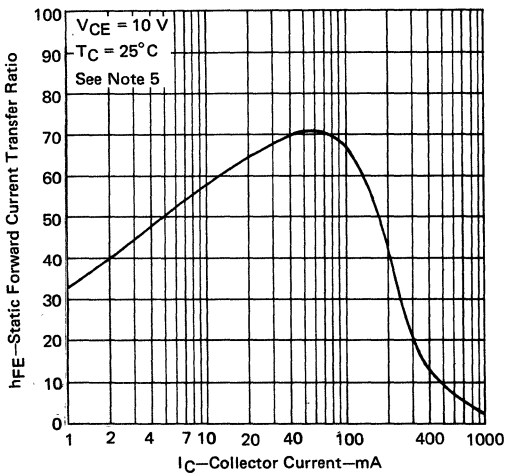


FIGURE 2

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE

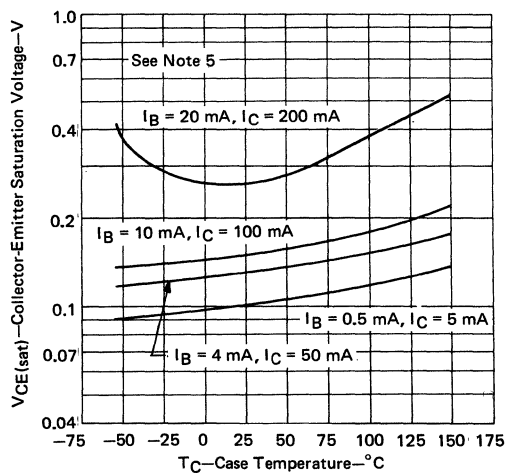


FIGURE 3

NOTE 5: These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

TYPES 2N3439, 2N3440 N-P-N SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

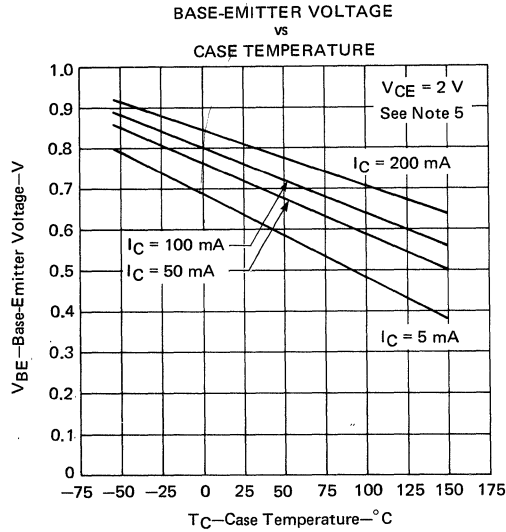


FIGURE 4

NOTE 5: These parameters must be measured using pulse techniques. $t_w = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

MAXIMUM SAFE OPERATING AREA

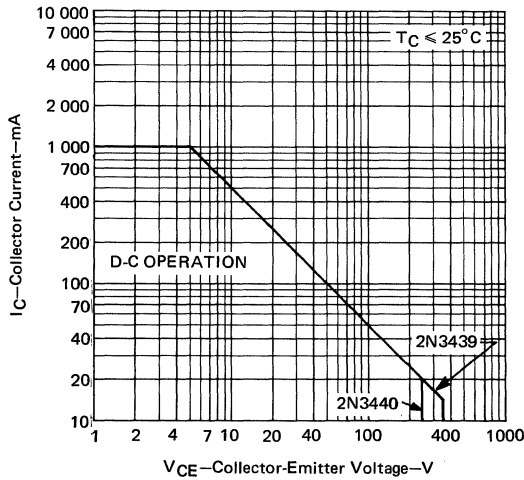


FIGURE 5

TYPES 2N3551, 2N3552 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

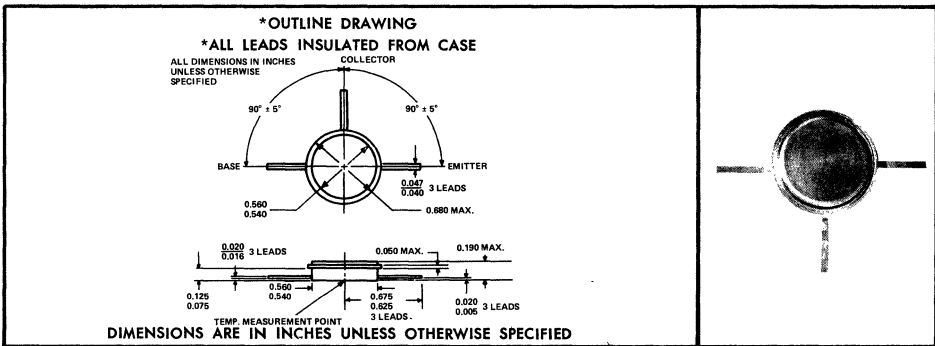
TYPES 2N3551, 2N3552
 BULLETIN NO. DL-S-715883, AUGUST 1964
 REVISED DECEMBER 1971

HIGH-SPEED POWER SWITCH, ISOLATED COLLECTOR FORMERLY TIX210, TIX211

- 40 Watts at 100°C Case Temperature
- Maximum r_{CS} of 0.1 Ohm at 10 Amperes I_C
- Maximum V_{BE} of 1.4 Volts at 10 Amperes I_C
- Maximum t_{on} of 300 nsec

mechanical data

These transistors are in precision welded, hermetically sealed enclosures. Extreme cleanliness during the assembly process prevents sealed-in contamination. The approximate unit weight is 3.8 grams.



* absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3551	2N3552
Collector-Base Voltage	115 v	140 v
Collector-Emitter Voltage (See Note 1)	60 v	80 v
Emitter-Base Voltage	← 7 v →	← 7 v →
Continuous Collector Current	← 12 a →	← 12 a →
Continuous Base Current	← 5 a →	← 5 a →
Continuous Emitter Current	← -12 a →	← -12 a →
Safe Operating Region at 100°C		
Case Temperature	See Figures 3 and 4	
Continuous Device Dissipation at (or below) 25°C		
Free-Air Temperature (See Note 2)	← 1.2 w →	← 1.2 w →
Continuous Device Dissipation at (or below) 100°C		
Case Temperature (See Note 3)	← 40 w →	← 40 w →
Operating Collector Junction Temperature	← 175°C →	← 175°C →
Operating Case Temperature Range	← -65°C to + 175°C →	← -65°C to + 175°C →
Storage Temperature Range	← -65°C to + 200°C →	← -65°C to + 200°C →
Lead Temperature 1/16 Inch from Case for 12 Seconds	← 235°C →	← 235°C →

NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. Derate linearly to 175°C free-air temperature at the rate of 8 mw/°C.
 3. Derate linearly to 175°C case temperature at the rate of 0.53 w/°C.

*JEDEC registered data

TYPES 2N3551, 2N3552

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3551		2N3552		UNIT
		MIN	MAX	MIN	MAX	
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = 10 \text{ ma}$, $I_E = 0$, See Note 4	115		140		v
BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ ma}$, $I_B = 0$, See Note 4	60		80		v
I_{CEV} Collector Cutoff Current	$V_{CE} = 110 \text{ v}$, $V_{BE} = -1.5 \text{ v}$		10			ma
	$V_{CE} = 135 \text{ v}$, $V_{BE} = -1.5 \text{ v}$				10	
	$V_{CE} = 60 \text{ v}$, $V_{BE} = -1.5 \text{ v}$, $T_C = 150^\circ\text{C}$		10			
	$V_{CE} = 80 \text{ v}$, $V_{BE} = -1.5 \text{ v}$, $T_C = 150^\circ\text{C}$				10	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ v}$, $I_C = 0$		0.1		0.1	ma
	$V_{EB} = 7 \text{ v}$, $I_C = 0$		1		1	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ v}$, $I_C = 5 \text{ a}$, See Note 4	25		25		
	$V_{CE} = 2 \text{ v}$, $I_C = 10 \text{ a}$, See Note 4	20	90	20	90	
	$V_{CE} = 2 \text{ v}$, $I_C = 10 \text{ a}$, $T_C = -55^\circ\text{C}$, See Note 4	10		10		
V_{BE} Base-Emitter Voltage	$I_B = 0.5 \text{ a}$, $I_C = 5 \text{ a}$, See Note 4		1.2		1.2	v
	$I_B = 1 \text{ a}$, $I_C = 10 \text{ a}$, See Note 4		1.4		1.4	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ a}$, $I_C = 5 \text{ a}$, See Note 4		0.5		0.5	v
	$I_B = 1 \text{ a}$, $I_C = 10 \text{ a}$, See Note 4		1.0		1.0	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ v}$, $I_C = 3 \text{ a}$, $f = 10 \text{ Mc}$	4		4		
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ v}$, $I_E = 0$, $f = 1 \text{ Mc}$		850		850	pf

NOTE 4: These parameters must be measured using pulse techniques. PW = 300 μsec , Duty Cycle $\leq 2\%$.

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	1.875	$^\circ\text{C}/\text{w}$
θ_{J-A} Junction-to-Free-Air Thermal Resistance	125	$^\circ\text{C}/\text{w}$

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = 10 \text{ a}$, $I_{B(1)} = 1 \text{ a}$, $I_{B(2)} = -1 \text{ a}$ $V_{BE(off)} = -6 \text{ v}$, $R_L = 2.4\Omega$, See Figure 1	0.3	μsec
t_{off} Turn-Off Time		2.5	μsec

†Voltage and current values shown are nominal; exact values vary slightly with device parameters.

*JEDEC Registered Data

TYPES 2N3551, 2N3552 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

PARAMETER MEASUREMENT INFORMATION

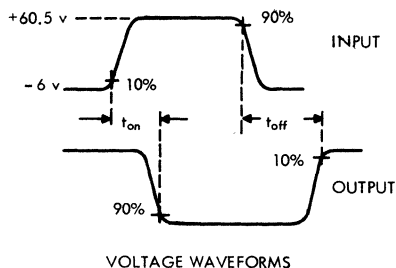
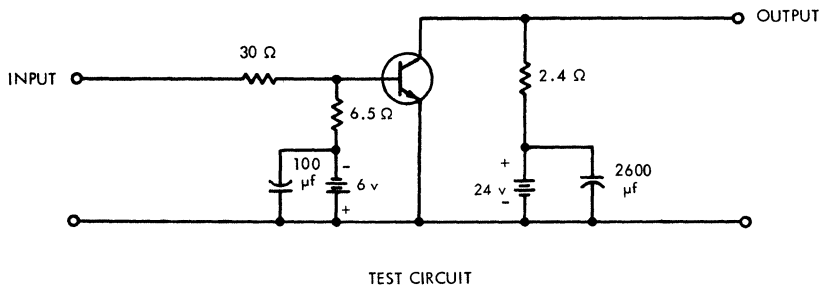


FIGURE 1

- NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 20$ nsec, $t_f \leq 20$ nsec, $Z_{out} = 1500 \Omega$, $PW = 5 \mu\text{sec}$,
Duty Cycle $\leq 0.5\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5$ nsec, $R_{in} \geq 1 \text{ M}\Omega$, $C_{in} \leq 5$ pf.
- c. Resistors must be noninductive types.

TYPES 2N3551, 2N3552

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

THERMAL INFORMATION

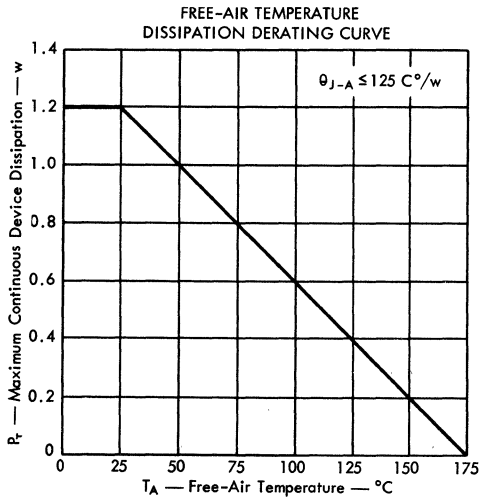


FIGURE 1

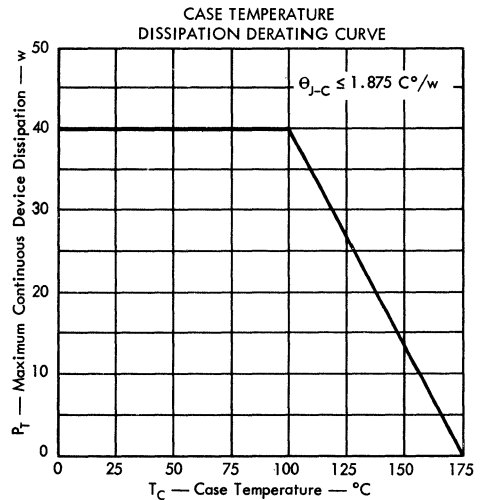


FIGURE 2

MAXIMUM SAFE OPERATING REGIONS

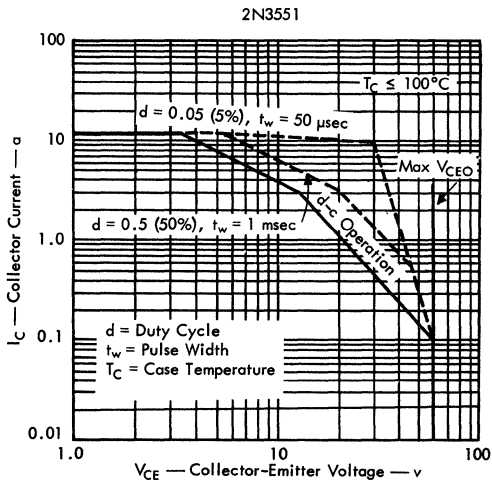


FIGURE 3

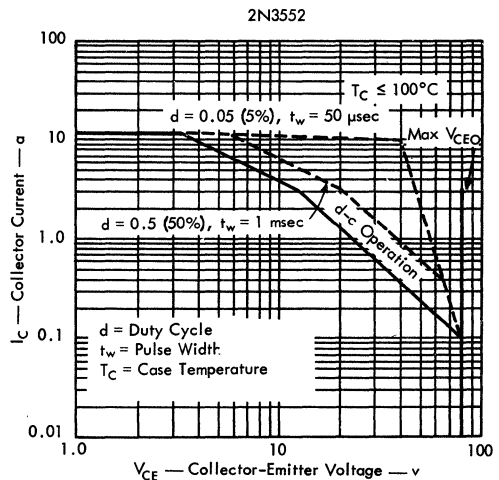


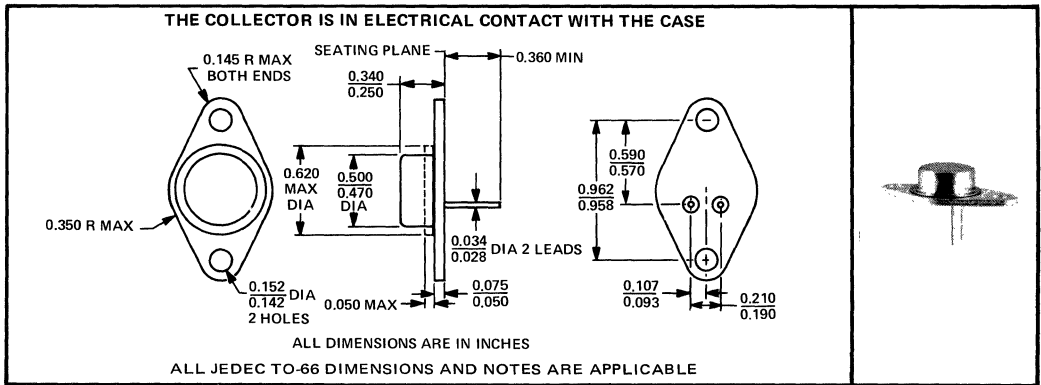
FIGURE 4

TYPES 2N3583, 2N3584, 2N3585, 2N4240 N-P-N SILICON POWER TRANSISTORS

HIGH-VOLTAGE POWER TRANSISTORS DESIGNED FOR INDUSTRIAL AND MILITARY APPLICATIONS

- Min $V_{(BR)CEO}$ of 300 V (2N3585, 2N4240)
- Typ $V_{CE(sat)}$ of 0.25 V at $I_B = 125$ mA, $I_C = 1$ A
- Typ t_{on} of 0.2 μs , at 750 mA, 200 V (2N4240)
- Min f_T of 15 MHz at 10 V, 200 mA (2N4240)
- 35 W at 25°C Case Temperature

***mechanical data**



TYPES 2N3583, 2N3584, 2N3585, 2N4240
 BULLETIN NO. DL-5711489, AUGUST 1971
 REVISED DECEMBER 1971

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3583	2N3584	2N3585	2N4240
Collector-Base Voltage	250 V*	375 V*	500 V*	500 V*
Collector-Emitter Voltage (See Note 1)	175 V*	250 V*	300 V*	300 V*
Emitter-Base Voltage	← 6 V* →			
Continuous Collector Current	1 A*	2 A*	2 A*	2 A*
Peak Collector Current (See Note 2)	5 A*	5 A*	5 A*	5 A*
Continuous Base Current	← 1 A* →			
Safe Operating Area at 100°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 35 W* →			
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	← 20 W* →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Operating Collector Junction Temperature Range	← -65°C to 200°C* →			
Storage Temperature Range	← -65°C to 200°C* →			
Terminal Temperature 1/32 Inch from Case for 10 Seconds	← 235°C* →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.2 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N3583, 2N3584, 2N3585, 2N4240

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3583		2N3584		2N3585		2N4240		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = 200 mA, I _B = 0, See Note 5	175		250		300		300		V
I _{CEO} Collector Cutoff Current	V _{CE} = 150 V, I _B = 0		10							mA
I _{CEV} Collector Cutoff Current	V _{CE} = 225 V, V _{BE} = -1.5 V		1							mA
	V _{CE} = 340 V, V _{BE} = -1.5 V				1					
	V _{CE} = 450 V, V _{BE} = -1.5 V						1		2	
	V _{CE} = 225 V, V _{BE} = -1.5 V, T _C = 150°C		3							
I _{EBO} Emitter Cutoff Current	V _{CE} = 300 V, V _{BE} = -1.5 V, T _C = 150°C				3		3		5	mA
	V _{EB} = 6 V, I _C = 0		5		0.5		0.5		0.5	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 0.5 A	40	200							
	V _{CE} = 10 V, I _C = 1 A	10								
	V _{CE} = 2 V, I _C = 1 A			8	80	8	80			
	V _{CE} = 2 V, I _C = 0.75 A							10	100	
V _{BE} Base-Emitter Voltage	I _B = 75 mA, I _C = 0.75 A								1.8	V
	I _B = 0.1 A, I _C = 1 A				1.4		1.4			
	V _{CE} = 10 V, I _C = 1 A		1.4							
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 75 mA, I _C = 0.75 A								1	V
	I _B = 125 mA, I _C = 1 A		5		0.75		0.75			
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 30 V, I _C = 0.1 A, f = 1 kHz	25	350							
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 0.2 A, f = 5 MHz	2		2		2		3		

NOTES: 5. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

thermal characteristics

PARAMETER	MAX	UNIT
R _{θJC} Junction-to-Case Thermal Resistance	5	°C/W
R _{θJA} Junction-to-Free-Air Thermal Resistance	87.5	

TYPES 2N3583, 2N3584, 2N3585, 2N4240 N-P-N SILICON POWER TRANSISTORS

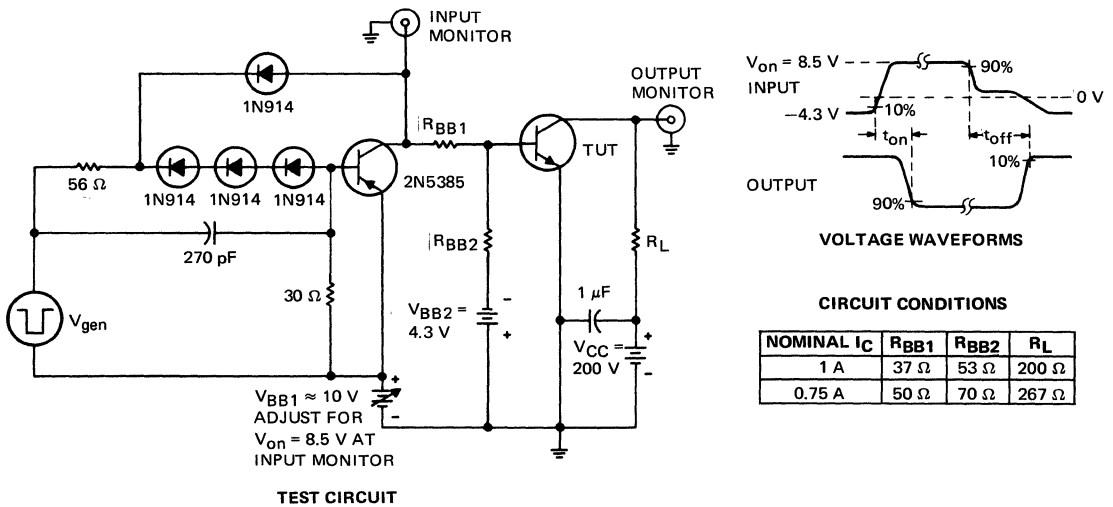
*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS‡	2N3584		2N4240		UNIT
		TYP	MAX	TYP	MAX	
t_r Rise Time	$I_C = 1 \text{ A}, \quad I_B(1) = 100 \text{ mA}, \quad I_B(2) = -100 \text{ mA},$ $V_{BE(off)} = -4.3 \text{ V}, \quad R_L = 200 \Omega,$ See Figure 1	1	3			μs
t_s Storage Time		1.5	4			
t_f Fall Time		1	3			
t_r Rise Time	$I_C = 0.75 \text{ A}, \quad I_B(1) = 75 \text{ mA}, \quad I_B(2) = -75 \text{ mA},$ $V_{BE(off)} = -4.3 \text{ V}, \quad R_L = 267 \Omega,$ See Figure 1			0.15	0.5	μs
t_s Storage Time				2.5	6	
t_f Fall Time				0.5	3	

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- V_{gen} is a -30-V pulse (from 0 V) into a 50- Ω termination.
 - The V_{gen} waveform is supplied by a generator with following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPES 2N3583, 2N3584, 2N3585, 2N4240

N-P-N SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

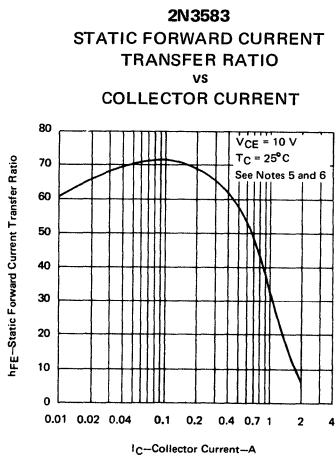


FIGURE 2

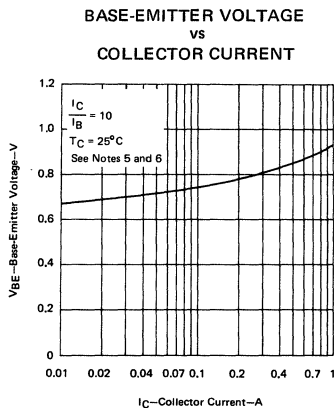


FIGURE 3

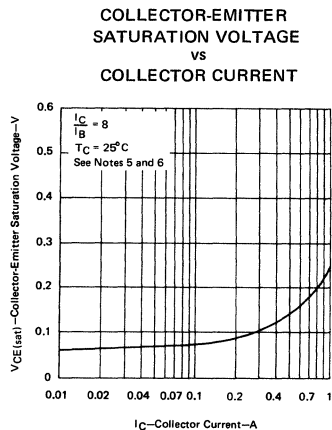


FIGURE 4

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

MAXIMUM SAFE OPERATING AREA

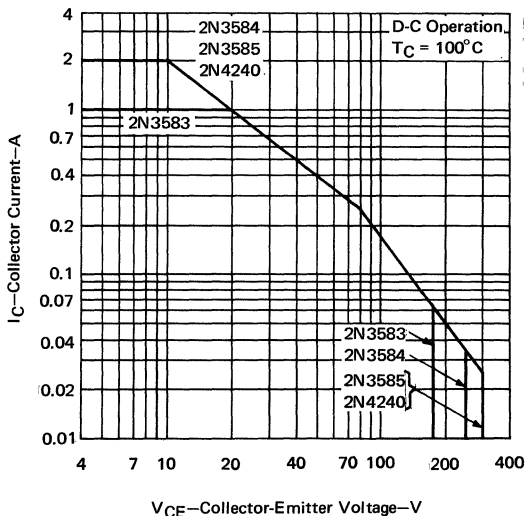


FIGURE 5

THERMAL INFORMATION

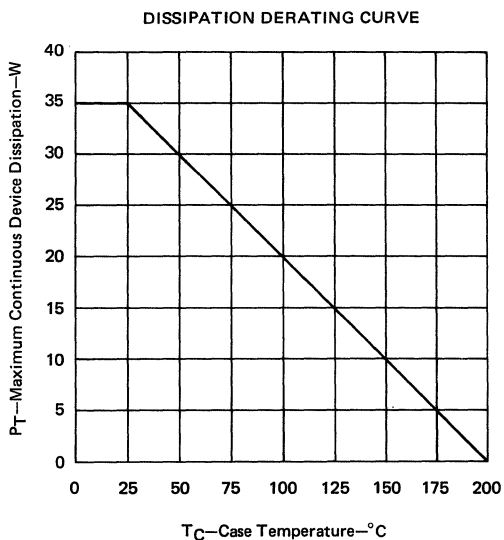


FIGURE 6

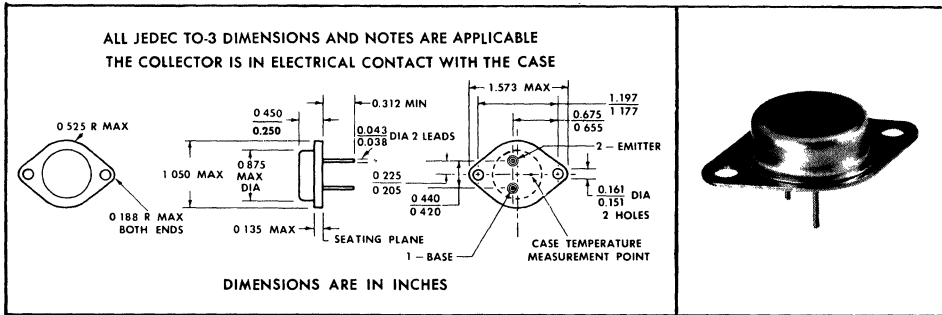
TYPES 2N3713, 2N3714, 2N3715, 2N3716 N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPES 2N3713, 2N3714, 2N3715, 2N3716
BULLETIN NO. DL-5 6810691, FEBRUARY 1968

FOR POWER-AMPLIFIER AND SWITCHING APPLICATIONS

- 150 W at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_{hfe} of 30 kHz
- Min f_T of 4 MHz

***mechanical data**



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3713	2N3714	2N3715	2N3716
*Collector-Base Voltage	80 V	100 V	80 V	100 V
*Collector-Emitter Voltage (See Note 1)	60 V	80 V	60 V	80 V
*Emitter-Base Voltage	← 7 V →			
*Continuous Collector Current	← 10 A →			
Peak Collector Current (See Note 2)	← 15 A →			
*Continuous Base Current	← 4 A →			
*Safe Operating Region at (or below) 25°C Case Temperature	See Figures 8 and 9			
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →			
*Operating Collector Junction Temperature Range	← -65°C to 200°C →			
*Storage Temperature Range	← -65°C to 200°C →			
Lead Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p = 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.855 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

TYPES 2N3713, 2N3714, 2N3715, 2N3716

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3713		2N3714		2N3715		2N3716		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}, I_B = 0$, See Note 5	60		80		60		80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}, I_B = 0$	0.7				0.7				mA
	$V_{CE} = 40 \text{ V}, I_B = 0$			0.7				0.7		
I_{CEV} Collector Cutoff Current	$V_{CE} = 80 \text{ V}, V_{BE} = -1.5 \text{ V}$	1				1				mA
	$V_{CE} = 100 \text{ V}, V_{BE} = -1.5 \text{ V}$			1				1		
	$V_{CE} = 60 \text{ V}, V_{BE} = -1.5 \text{ V}, T_C = 150^\circ\text{C}$	10				10				mA
	$V_{CE} = 80 \text{ V}, V_{BE} = -1.5 \text{ V}, T_C = 150^\circ\text{C}$			10				10		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 7 \text{ V}, I_C = 0$	1		1		1		1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}, I_C = 1 \text{ A}$, See Notes 5 and 6	25	75	25	75	50	150	50	150	
	$V_{CE} = 2 \text{ V}, I_C = 3 \text{ A}$, See Notes 5 and 6	15		15		30		30		
	$V_{CE} = 4 \text{ V}, I_C = 10 \text{ A}$, See Notes 5 and 6	5		5		5		5		
V_{BE} Base-Emitter Voltage	$V_{CE} = 2 \text{ V}, I_C = 5 \text{ A}$, See Notes 5 and 6	2		2		1.8		1.8		V
	$V_{CE} = 4 \text{ V}, I_C = 10 \text{ A}$, See Notes 5 and 6	4		4		4		4		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}, I_C = 5 \text{ A}$, See Notes 5 and 6	1		1		0.8		0.8		V
	$I_B = 2 \text{ A}, I_C = 10 \text{ A}$, See Notes 5 and 6	4		4		4		4		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}, I_C = 0.5 \text{ A}, f = 1 \text{ kHz}$	25	250	25	250	25	250	25	250	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}, I_C = 0.5 \text{ A}, f = 1 \text{ MHz}$	4		4		4		4		
f_{hfe} Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = 10 \text{ V}, I_C = 0.5 \text{ A}$	30		30		30		30		kHz
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}, I_E = 0, f = 100 \text{ kHz}$	250		250		250		250		pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	1.17	deg/W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	43.7	

*Indicates JEDEC registered data

TYPES 2N3713, 2N3714, 2N3715, 2N3716

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_{B(1)} = 100 \text{ mA}$, $I_{B(2)} = -100 \text{ mA}$,	450	ns
t_{off} Turn-Off Time	$V_{BE(off)} = -3.7 \text{ V}$, $R_L = 20 \Omega$, See Figure 1	350	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

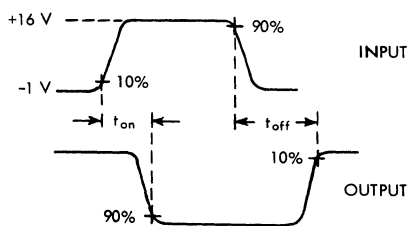
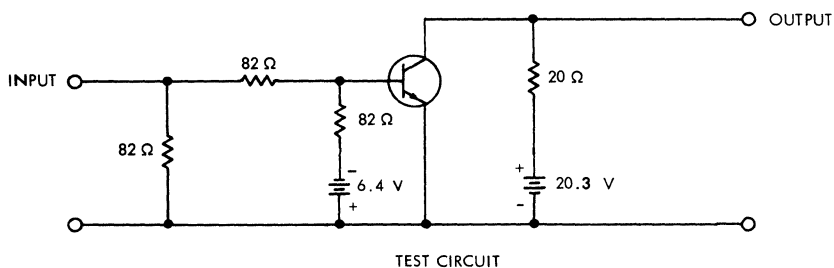


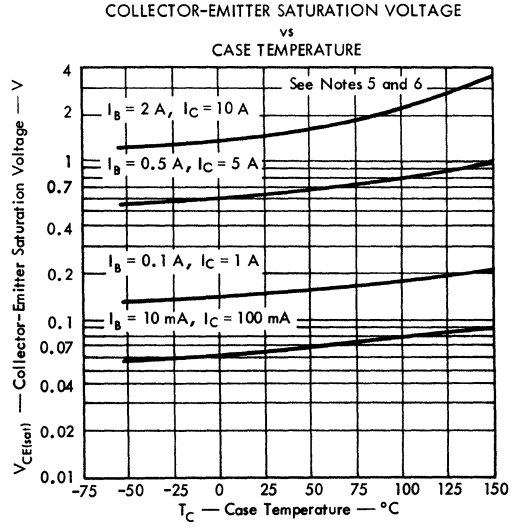
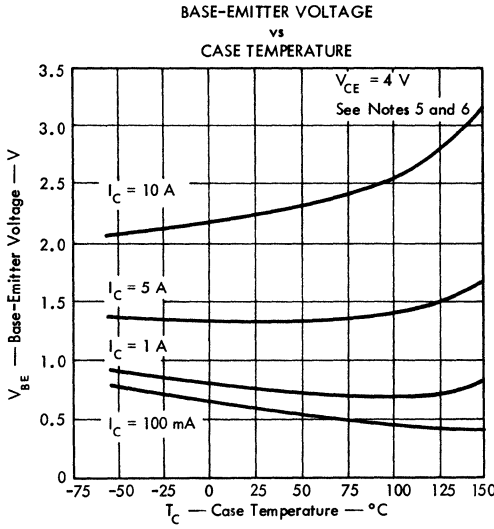
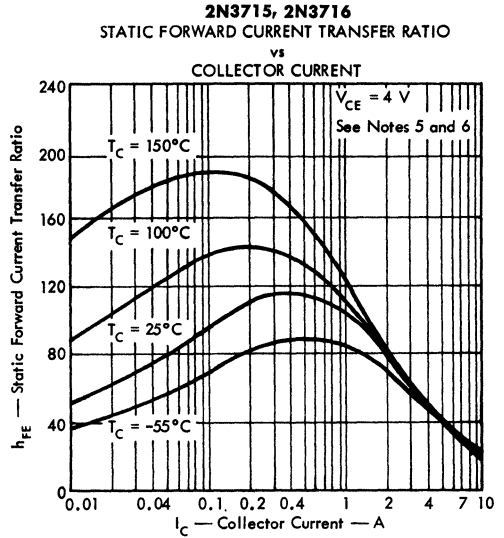
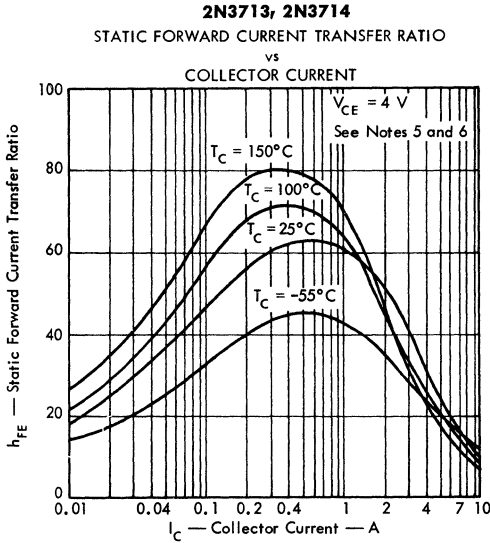
FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPES 2N3713, 2N3714, 2N3715, 2N3716

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS



NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N3713, 2N3714, 2N3715, 2N3716

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

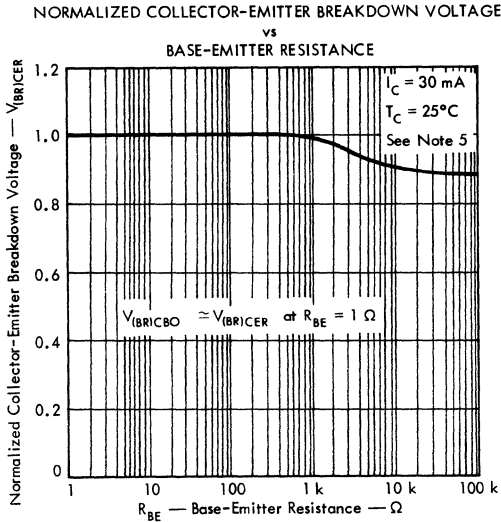


FIGURE 6

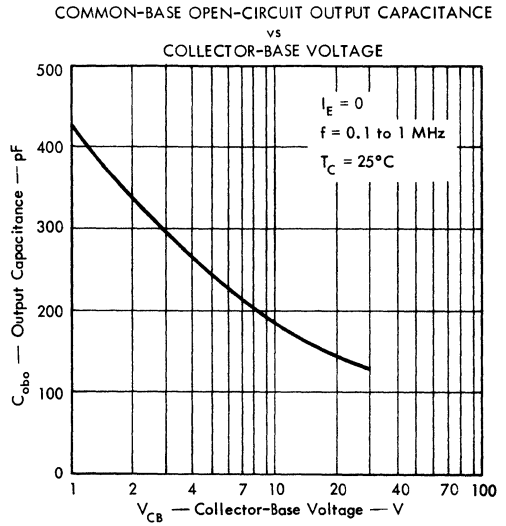


FIGURE 7

MAXIMUM SAFE OPERATING REGIONS

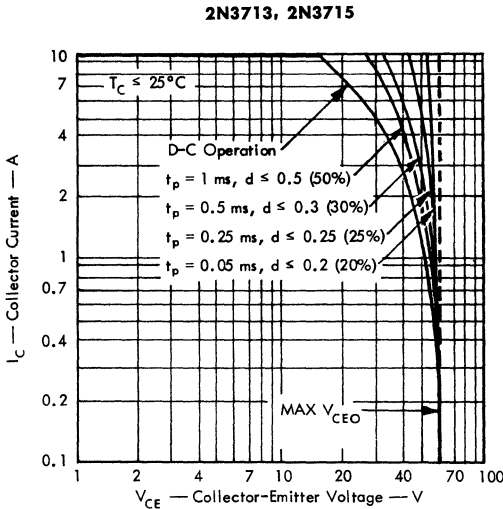


FIGURE 8

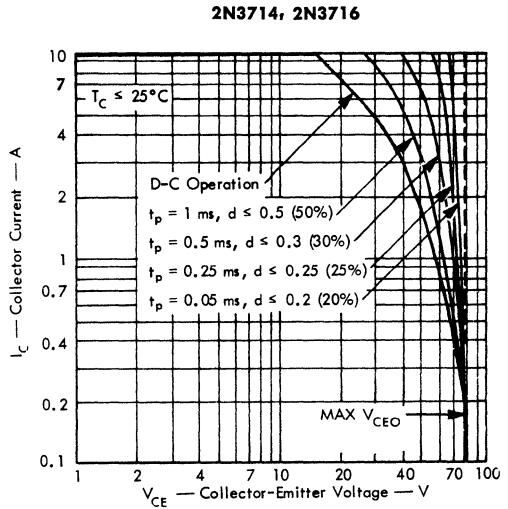


FIGURE 9

NOTES: 5. This parameter must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

TYPES 2N3713, 2N3714, 2N3715, 2N3716

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

THERMAL INFORMATION

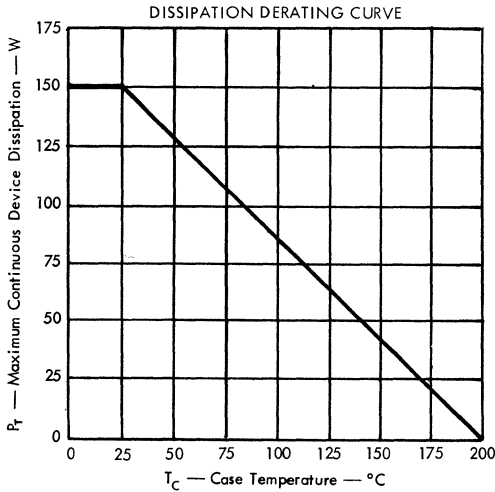


FIGURE 10

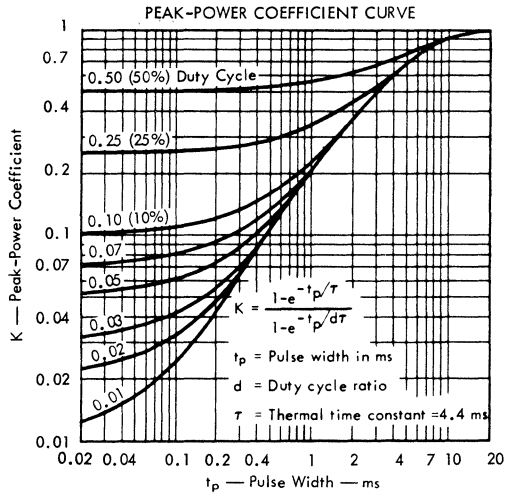


FIGURE 11

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	43.7	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	1.17	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	42.5	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 11	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 2.25 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C, as in figure 10.}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From figure 11, Peak-Power Coefficient

$$K = 0.11 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(2.25) + 0.11(1.17)} = 424 \text{ W}$$

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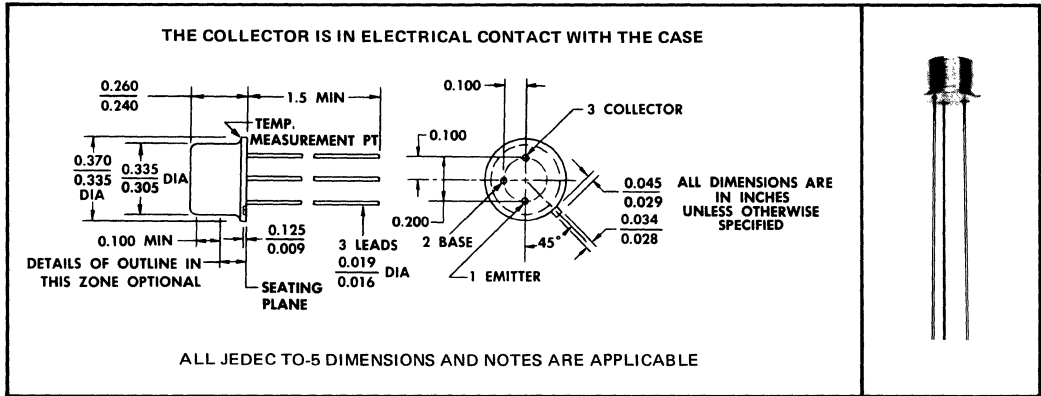
971

TYPES 2N3719, 2N3720 P-N-P SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP501, TIP502

- Max t_{off} of 0.4 μ s at $I_C = 1$ A
- 3-A Rated Continuous Collector Current
- 6 Watts at 25°C Case Temperature
- Min f_T of 60 MHz at 10 V, 0.5 A

*mechanical data



TYPES 2N3719, 2N3720
BULLETIN NO. DLS-7111606, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3719	2N3720
*Collector-Base Voltage	-40 V	-60 V
*Collector-Emitter Voltage (See Note 1)	-40 V	-60 V
*Emitter-Base Voltage	-4 V	-4 V
*Continuous Collector Current	← -3 A →	
*Peak Collector Current (See Note 2)	← -10 A →	
*Continuous Base Current	← -0.5 A →	
*Safe Operating Areas at (or below) 25°C Case Temperature	See Figures 3 and 4	
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 6 W →	
*Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1 W →	
*Operating Collector Junction Temperature Range	-65°C to 200°C	
*Storage Temperature Range	-65°C to 200°C	
*Lead Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.5$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 34.3 mW/°C or refer to Dissipation Derating Curve, Figure 5.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.71 mW/°C or refer to Dissipation Derating Curve, Figure 6.
- *JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N3719, 2N3720

P-N-P SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3719		2N3720		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -20 \text{ mA}$, $I_B = 0$, See Note 5	-40		-60		V
I_{CEV} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 2 \text{ V}$	-10				μA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 2 \text{ V}$			-10		μA
	$V_{CE} = -40 \text{ V}$, $V_{BE} = 2 \text{ V}$, $T_C = 150^\circ\text{C}$			-1		mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 2 \text{ V}$, $T_C = 150^\circ\text{C}$				-1	mA
I_{CBO} Collector Cutoff Current	$V_{CB} = -40 \text{ V}$, $I_E = 0$			-10		μA
	$V_{CB} = -60 \text{ V}$, $I_E = 0$				-10	μA
I_{EBO} Emitter Cutoff Current	$V_{EB} = -4 \text{ V}$, $I_C = 0$			-1	-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ V}$, $I_C = -0.5 \text{ A}$	20		20		
	$V_{CE} = -1.5 \text{ V}$, $I_C = -1 \text{ A}$	25	180	25	180	
	$V_{CE} = -1.5 \text{ V}$, $I_C = -1 \text{ A}$, $T_C = -40^\circ\text{C}$	15		15		
V_{BE} Base-Emitter Voltage	$I_B = -100 \text{ mA}$, $I_C = -1 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C			-1.5	-1.5	V
	$I_B = -300 \text{ mA}$, $I_C = -3 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C			-2.3	-2.3	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -100 \text{ mA}$, $I_C = -1 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C			-0.75	-0.75	V
	$I_B = -300 \text{ mA}$, $I_C = -3 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C			-1.5	-1.5	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 30 \text{ MHz}$	2		2		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 100 \text{ kHz}$		120		120	pF
C_{ibo} Common-Base Open-Circuit Input Capacitance	$V_{EB} = -0.5 \text{ V}$, $I_C = 0$, $f = 100 \text{ kHz}$		1000		1000	pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

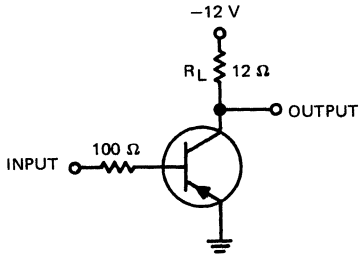
PARAMETER	TEST CONDITIONS [†]	MAX	UNIT
t_{on} Turn-On Time	$I_C = -1 \text{ A}$, $R_L = 12 \Omega$, $I_B(1) = -0.1 \text{ A}$, See Figure 1, $V_{BE(off)} = 4 \text{ V}$	0.1	μs
t_{off} Turn-Off Time	$I_C = -1 \text{ A}$, $R_L = 12 \Omega$, $I_B(1) = -0.1 \text{ A}$, See Figure 2, $I_B(2) = 0.1 \text{ A}$	0.4	

[†] Voltage and current values shown are nominal exact values vary slightly with transistor parameters.

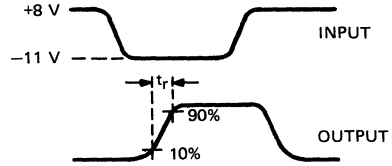
*JEDEC registered data

TYPES 2N3719, 2N3720 P-N-P SILICON POWER TRANSISTORS

*PARAMETER MEASUREMENT INFORMATION

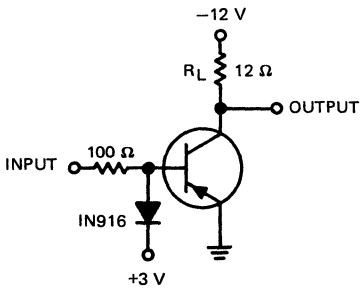


TEST CIRCUIT

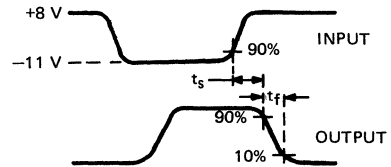


VOLTAGE WAVEFORMS

FIGURE 1—TURN-ON TIME



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2—TURN-OFF TIME

- NOTES: a. The input waveforms are supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_{out} = 50 \Omega$, $t_w = 10 \mu$ s, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5$ ns, $R_{in} \geq 10$ k Ω , $C_{in} \leq 11.5$ pF.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

*JEDEC registered data

TYPES 2N3719, 2N3720

P-N-P SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

2N3719

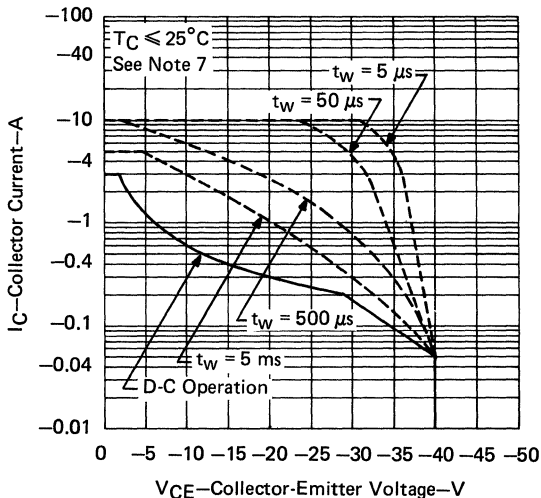


FIGURE 3

2N3720

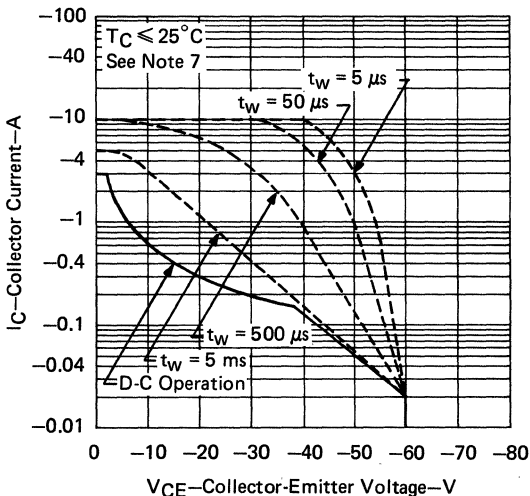


FIGURE 4

NOTE 7: Areas defined by dashed lines apply for nonrepetitive-pulse operation. The pulse may be repeated after the device has regained thermal equilibrium.

THERMAL INFORMATION

CASE TEMPERATURE DISSIPATION DERATING CURVE

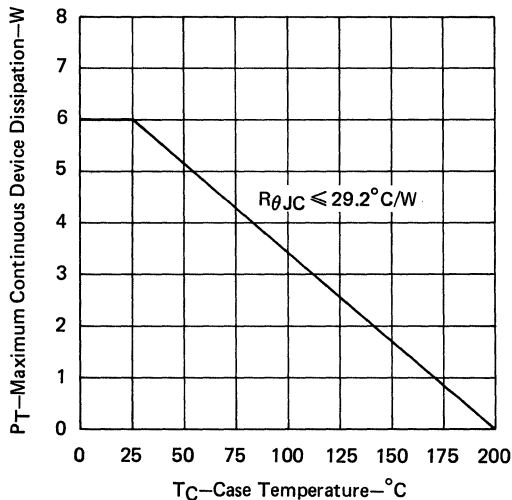


FIGURE 5

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

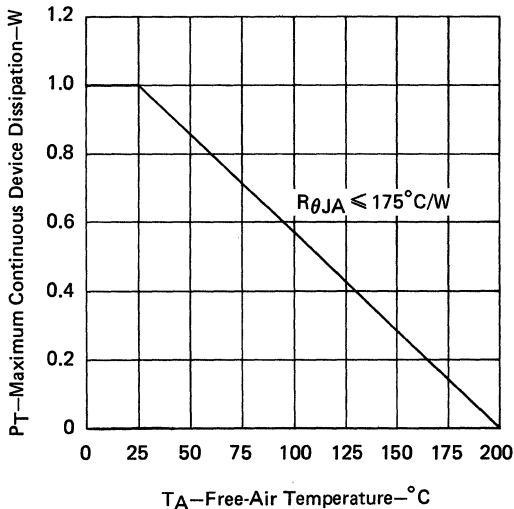


FIGURE 6

TYPES 2N3771, 2N3772

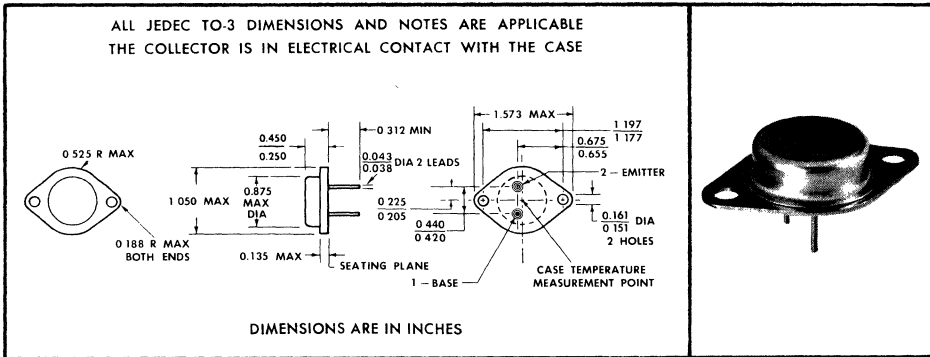
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR UNTUNED POWER-AMPLIFIER APPLICATIONS

150 W at 25°C Case Temperature
30-A Rated Continuous Collector Current (2N3771)
20-A Rated Continuous Collector Current (2N3772)

TYPES 2N3771, 2N3772
BULLETIN NO. DLS-7110299, DECEMBER 1971

***mechanical data**



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3771	2N3772
Collector-Base Voltage	50 V*	100 V*
Collector-Emitter Voltage (See Note 1)	50 V*	100 V* 80 V*
Collector-Emitter Voltage (See Note 2)	40 V*	60 V*
Emitter-Base Voltage	5 V*	7 V*
Continuous Collector Current	30 A*	20 A*
Peak Collector Current (See Note 3)	← 30 A* →	
Continuous Base Current	7.5 A*	5 A*
Peak Base Current	← 15 A* →	
Safe Operating Region	See Figure 1*	
Continuous Dissipation at (or below) 25°C Case Temperature (See Note 4)	← 150 W* →	
Operating Collector Junction Temperature Range	-65°C to 200°C*	
Storage Temperature Range	-65°C to 200°C*	
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 235°C* →	

- NOTES: 1. These values apply when the base-emitter voltage $V_{BE} = -1.5$ V.
2. These values apply when the base-emitter diode is open-circuited.
3. This value applies for a nonrepetitive pulse of any duration for the 2N3771, or of 500-ms maximum duration for the 2N3772.
4. Derate linearly to 200°C case temperature at the rate of 0.855 W/deg see figure 2.

*Indicates JEDEC registered data
†Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

TYPES 2N3771, 2N3772

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3771		2N3772		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 5	40		60		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	10				mA
	$V_{CE} = 50 \text{ V}$, $I_B = 0$			10		
I_{CBO} Collector Cutoff Current	$V_{CB} = 50 \text{ V}$, $I_E = 0$	2				mA
	$V_{CB} = 100 \text{ V}$, $I_E = 0$			5		
I_{CEV} Collector Cutoff Current	$V_{CE} = 50 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	2				mA
	$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			5		
	$V_{CE} = 30 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	10		10		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	5				mA
	$V_{EB} = 7 \text{ V}$, $I_C = 0$			5		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 5 and 6			15	60	
	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6					
	$V_{CE} = 4 \text{ V}$, $I_C = 20 \text{ A}$, See Notes 5 and 6			5		
	$V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$, See Notes 5 and 6	5				
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 5 and 6			2.2		V
	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	2.7				
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1 \text{ A}$, $I_C = 10 \text{ A}$, See Notes 5 and 6			1.4		V
	$I_B = 1.5 \text{ A}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	2				
	$I_B = 4 \text{ A}$, $I_C = 20 \text{ A}$, See Notes 5 and 6			4		
	$I_B = 6 \text{ A}$, $I_C = 30 \text{ A}$, See Notes 5 and 6	4				
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	40		40		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, $f = 50 \text{ kHz}$	4		4		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*Indicates JEDEC registered data

MAXIMUM SAFE OPERATING REGION

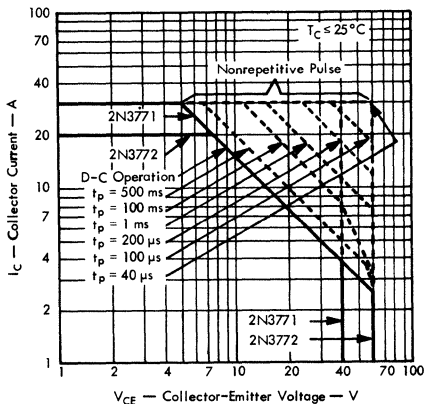


FIGURE 1

THERMAL INFORMATION

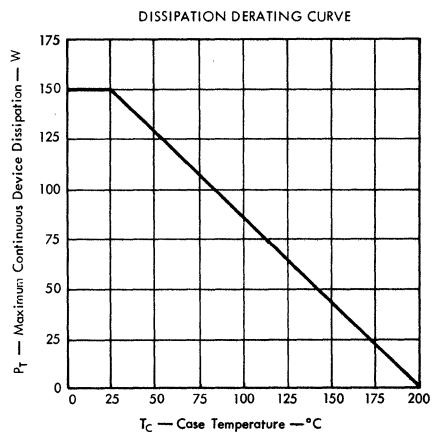


FIGURE 2

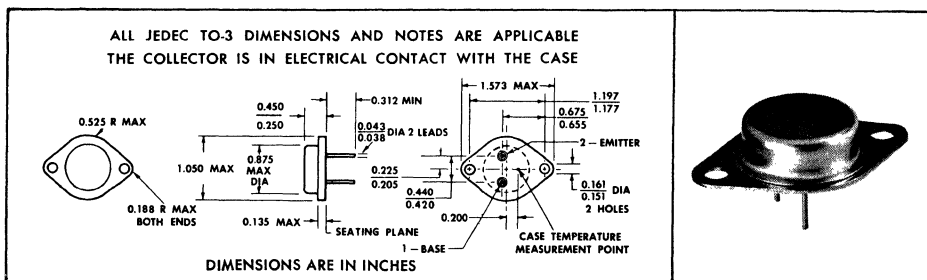
TYPES 2N3789, 2N3790, 2N3791, 2N3792 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N3713 THRU 2N3716

- 150 Watts at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_T of 4 MHz at 10 V, 500 mA
- Min f_{hfe} of 30 kHz at 10 V, 500 mA

TYPES 2N3789, 2N3790, 2N3791, 2N3792
BULLETIN NO. D.L.S. 6810050, NOVEMBER 1968

***mechanical data**



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3789	2N3790
*Collector-Base Voltage	-60 V	-80 V
*Collector-Emitter Voltage (See Note 1)	-60 V	-80 V
*Emitter-Base Voltage	← -7 V →	
*Continuous Collector Current	← -10 A →	
Peak Collector Current (See Note 2)	← -15 A →	
*Continuous Base Current	← -4 A →	
*Safe Operating Region at (or below) 25°C Case Temperature	See Figures 6 and 7	
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →	
*Operating Collector Junction Temperature Range	-65°C to 200°C	
*Storage Temperature Range	-65°C to 200°C	
Lead Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_D = 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.855 W/deg.
4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

TYPES 2N3789, 2N3790, 2N3791, 2N3792

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3789	2N3790	2N3791	2N3792	UNIT
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ mA}$, $I_B = 0$, See Note 5	-60	-80	-60	-80	V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-10		-10		mA
	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-10		-10	
I_{CEV} Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 1.5 \text{ V}$	-1		-1		mA
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 1.5 \text{ V}$		-1		-1	
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	-5		-5		
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		-5		-5	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -7 \text{ V}$, $I_C = 0$	-5	-5	-5	-5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 5 and 6	25 90	25 90	50 180	50 180	
	$V_{CE} = -2 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 5 and 6	15	15	30	30	
	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$, See Notes 5 and 6	4	4	4	4	
V_{BE} Base-Emitter Voltage	$V_{CE} = -2 \text{ V}$, $I_C = -5 \text{ A}$, See Notes 5 and 6	-2	-2	-1.8	-1.8	V
	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$, See Notes 5 and 6	-4	-4	-4	-4	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.4 \text{ A}$, $I_C = -4 \text{ A}$, See Notes 5 and 6	-1	-1			V
	$I_B = -0.5 \text{ A}$, $I_C = -5 \text{ A}$, See Notes 5 and 6			-1	-1	
	$I_B = -2 \text{ A}$, $I_C = -10 \text{ A}$, See Notes 5 and 6	-4	-4	-4	-4	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ kHz}$	25 250	25 250	25 250	25 250	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ MHz}$	4	4	4	4	
f_{hfe} Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, See Note 7	30	30	30	30	kHz
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 100 \text{ kHz}$	500	500	500	500	pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

7. f_{hfe} is the frequency at which the magnitude of the small-signal forward current transfer ratio is 0.707 of its low-frequency value. For this device, the reference measurement is made at 1 kHz.

*Indicates JEDEC registered data

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	1.17	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	43.7	

TYPES 2N3789, 2N3790, 2N3791, 2N3792 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -1 \text{ A}$, $I_{B(1)} = -100 \text{ mA}$, $I_{B(2)} = 100 \text{ mA}$,	0.35	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 3.7 \text{ V}$, $R_L = 20 \Omega$, See Figure 1	0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

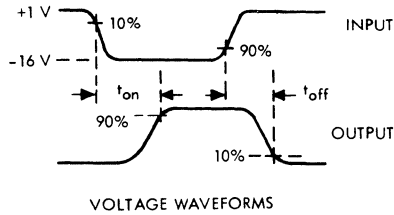
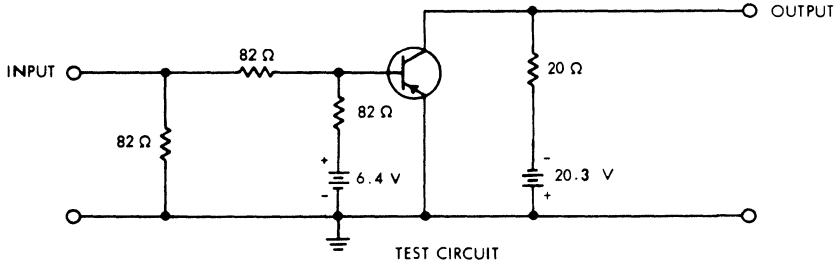


FIGURE 1

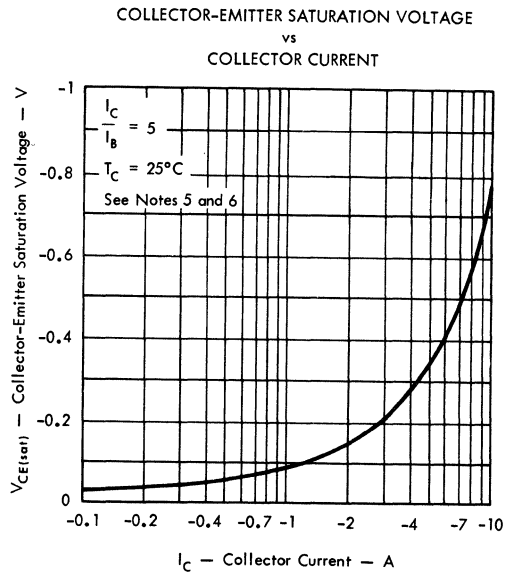
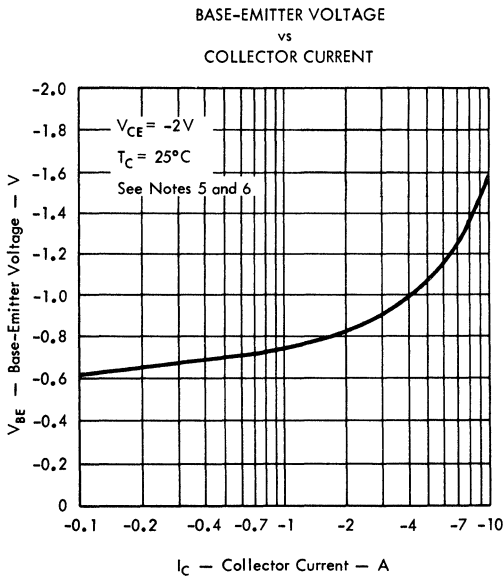
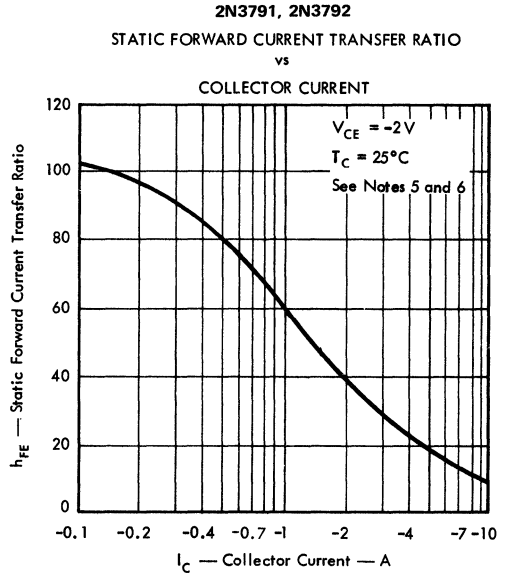
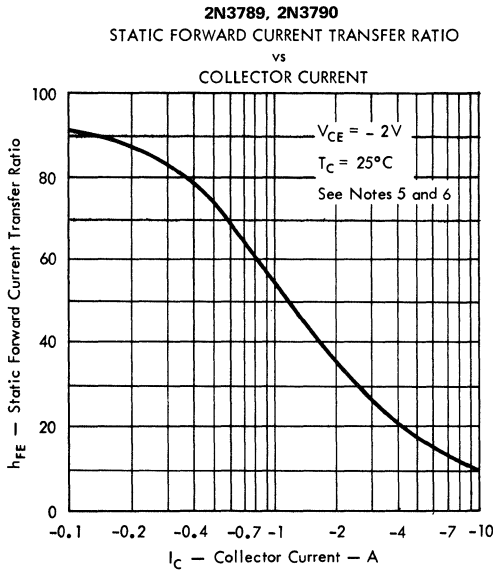
- NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPES 2N3789, 2N3790, 2N3791, 2N3792

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS



NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N3789, 2N3790, 2N3791, 2N3792 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGIONS

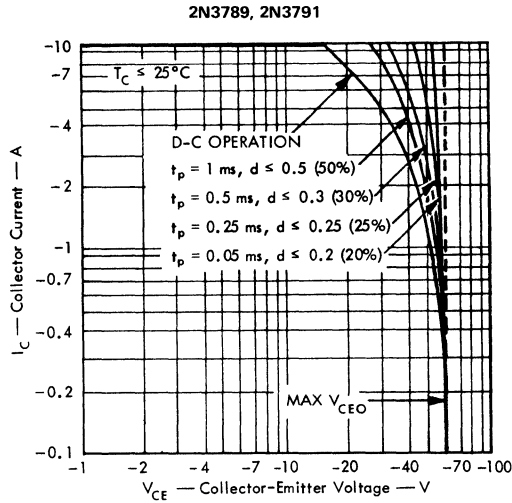


FIGURE 6

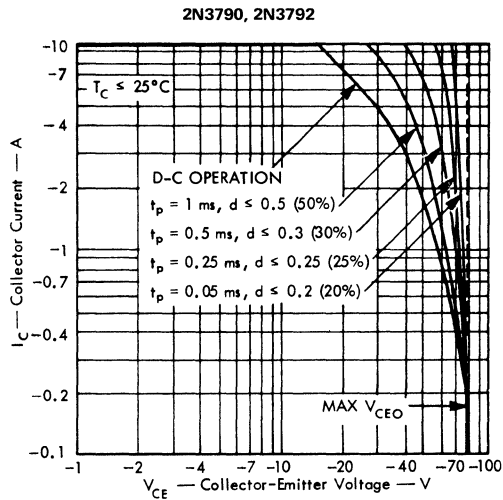


FIGURE 7

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TYPES 2N3789, 2N3790, 2N3791, 2N3792 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

THERMAL INFORMATION

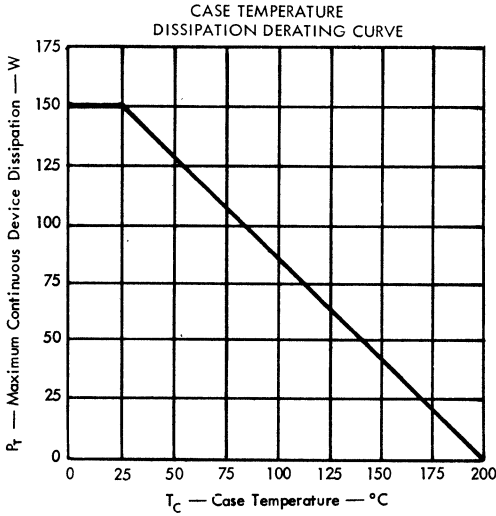


FIGURE 8

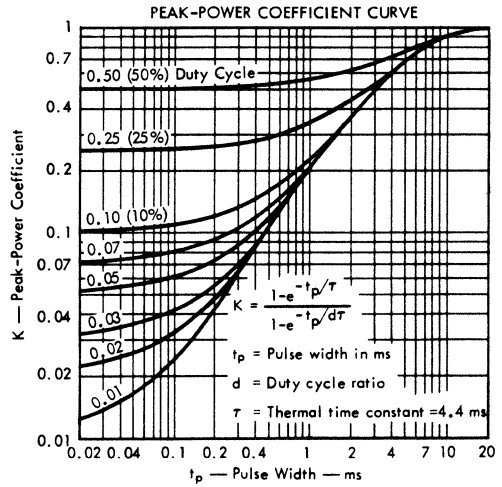


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	43.7	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	1.17	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	42.5	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 2.25 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C, as in Figure 8.}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.11 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(2.25) + 0.11(1.17)} = 424 \text{ W}$$

TYPES 2N3846, 2N3847

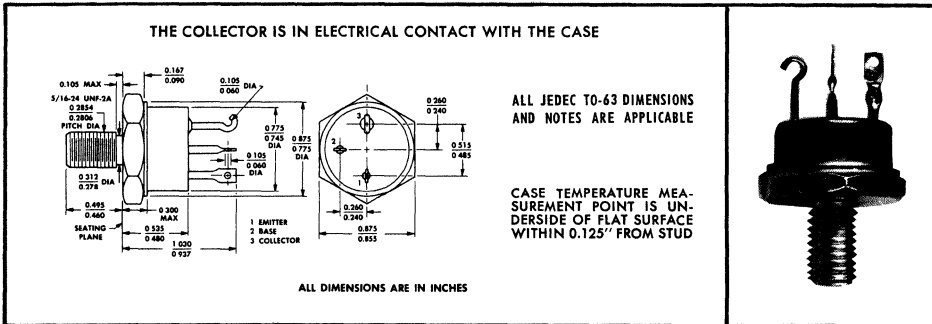
N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPES 2N3846, 2N3847
BULLETIN NO. DL-S-6810980, DECEMBER 1968

FOR POWER-AMPLIFIER APPLICATIONS

- 150 Watts at 100°C Case Temperature
- 200 V, 300 V Rated Collector-Emitter Voltages
- Max $V_{CE(sat)}$ of 0.75 V at 10 A I_c
- Max Thermal Resistance of 0.5 deg/W
- Min f_T of 10 MHz at 10 V, 1 A

***mechanical data**



5

***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

	2N3846	2N3847
Collector-Base Voltage	300 V	400 V
Collector-Emitter Voltage (See Note 1)	200 V	300 V
Emitter-Base Voltage	← 10 V →	← 10 V →
Continuous Collector Current	← 20 A →	← 20 A →
Continuous Base Current	← 10 A →	← 10 A →
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 2)	← 150 W →	← 150 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	← 4 W →	← 4 W →
Operating Case Temperature Range	-65°C to 175°C	
Storage Temperature Range	-65°C to 200°C	
Terminal Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →	← 260°C →

NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. Derate linearly to 175°C case temperature at the rate of 2 W/deg.
 3. Derate linearly to 175°C free-air temperature at the rate of 26.6 mW/deg.

*Indicates JEDEC registered data

TYPES 2N3846, 2N3847

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3846		2N3847		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 4	200		300		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 200 \text{ V}$, $I_B = 0$	5				mA
	$V_{CE} = 300 \text{ V}$, $I_B = 0$			5		
I_{CES} Collector Cutoff Current	$V_{CE} = 300 \text{ V}$, $V_{BE} = 0$	2				mA
	$V_{CE} = 400 \text{ V}$, $V_{BE} = 0$			2		
	$V_{CE} = 300 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	10				
	$V_{CE} = 400 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$			10		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 10 \text{ V}$, $I_C = 0$	250		250		μA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 3 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 4 and 5	40	200	40	200	
	$V_{CE} = 3 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 4 and 5	10	60	10	60	
	$V_{CE} = 3 \text{ V}$, $I_C = 10 \text{ A}$, $T_C = -55^\circ\text{C}$, See Notes 4 and 5	10		10		
V_{BE} Base-Emitter Voltage	$V_{CE} = 3 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 4 and 5	1.2		1.2		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1.6 \text{ A}$, $I_C = 10 \text{ A}$, See Notes 4 and 5	0.75		0.75		V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ A}$, $f = 1 \text{ kHz}$	50	250	50	250	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ MHz}$	10		10		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	750		750		pF

NOTES: 4. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance		0.5	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance		37.5	

*Indicates JEDEC registered data

TYPES 2N3846, 2N3847

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C \approx 10 \text{ A}$, $I_{B(1)} = 2 \text{ A}$, $I_{B(2)} = -2 \text{ A}$,	4	μS
t_{off} Turn-Off Time	$V_{BE(off)} \approx -7.5 \text{ V}$, $R_L = 15 \Omega$, See Figure 1	7	

† Base-emitter voltage and collector current values shown are nominal; exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION

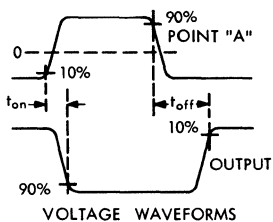
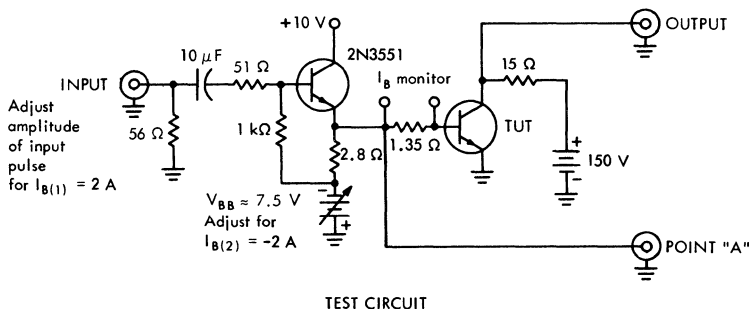


FIGURE 1

- NOTES: a. The waveform at point "A" has the following characteristics: $t_r \leq 100 \text{ ns}$, $t_f \leq 100 \text{ ns}$, $t_p = 20 \mu\text{s}$, duty cycle $\leq 0.2\%$.
 b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5 \text{ ns}$, $R_{in} \geq 1 \text{ M}\Omega$, $C_{in} \leq 5 \text{ pF}$.
 c. Resistors must be noninductive types.
 d. The d-c power supplies may require additional bypassing in order to minimize ringing.

*Indicates JEDEC registered data

TYPES 2N3846, 2N3847

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

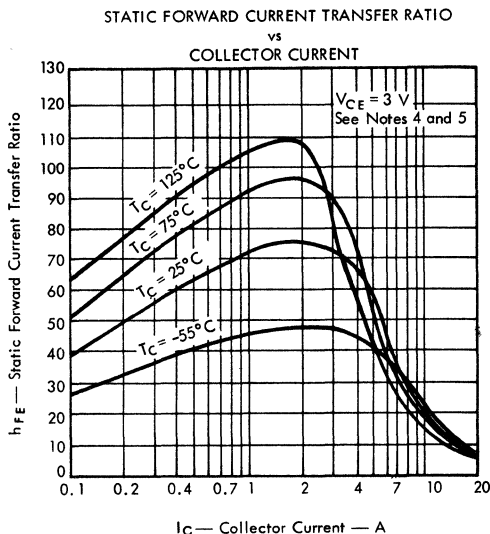


FIGURE 2

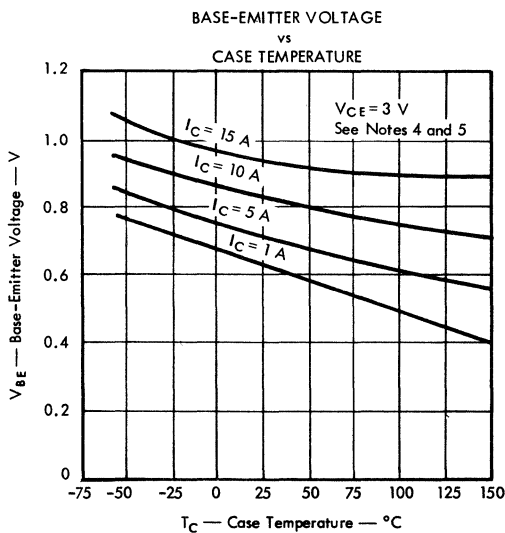


FIGURE 3

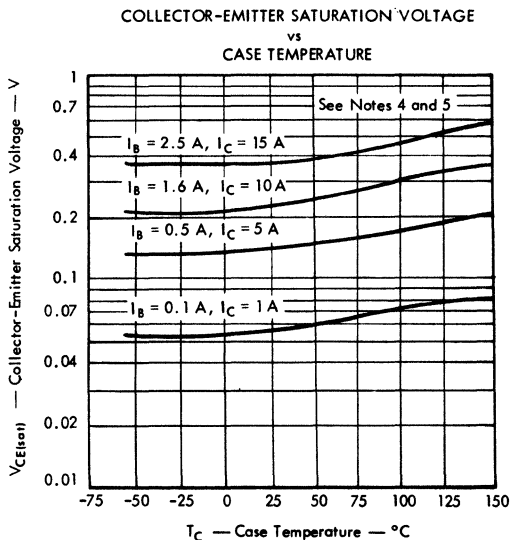


FIGURE 4

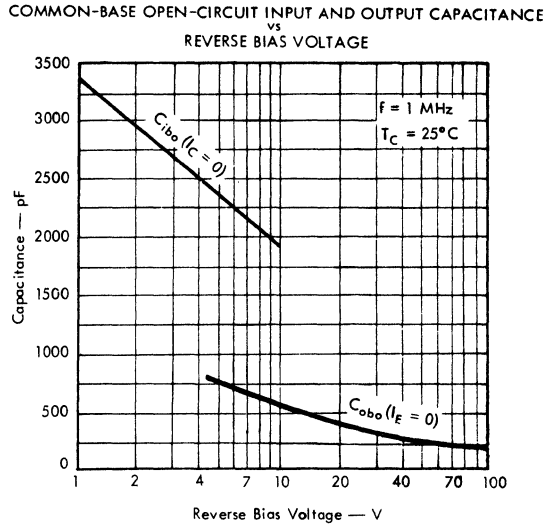
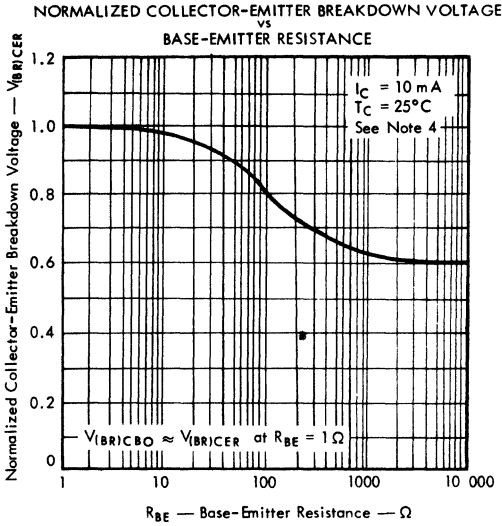
NOTES: 4. These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

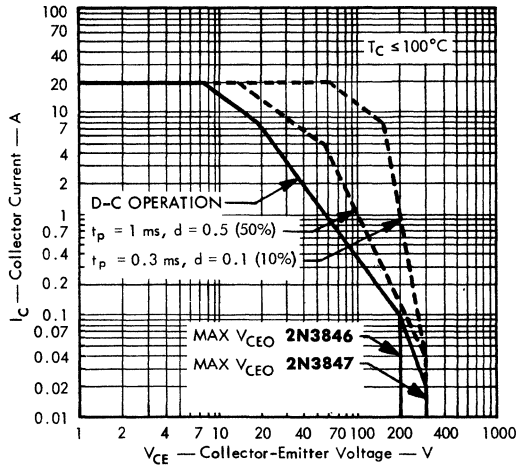
TYPES 2N3846, 2N3847

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS



MAXIMUM SAFE OPERATING REGION



NOTES: 4. This parameter must be measured using pulse techniques: $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

TYPES 2N3846, 2N3847

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

THEMAL INFORMATION

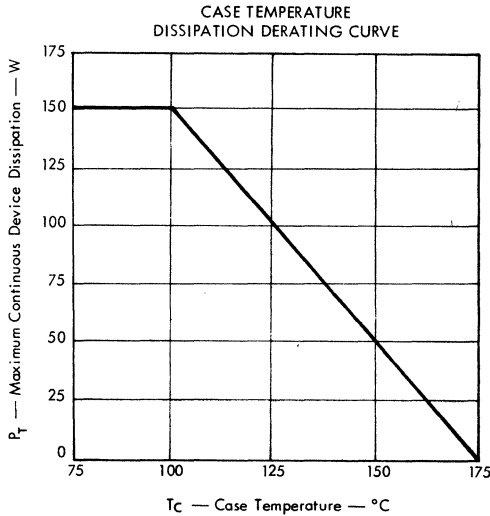


FIGURE 8

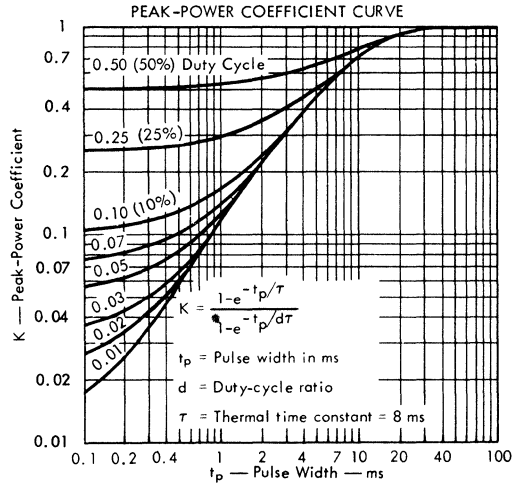


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	37.5	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	0.5	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	37	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 175	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 175	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \quad \text{for } 100^\circ\text{C} \leq T_C \leq 175^\circ\text{C} \quad \text{as in Figure 8}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \quad \text{for } 25^\circ\text{C} \leq T_A \leq 175^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \quad \text{for } 100^\circ\text{C} \leq T_C \leq 175^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \quad \text{for } 25^\circ\text{C} \leq T_A \leq 175^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 2.5 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 175^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.105 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

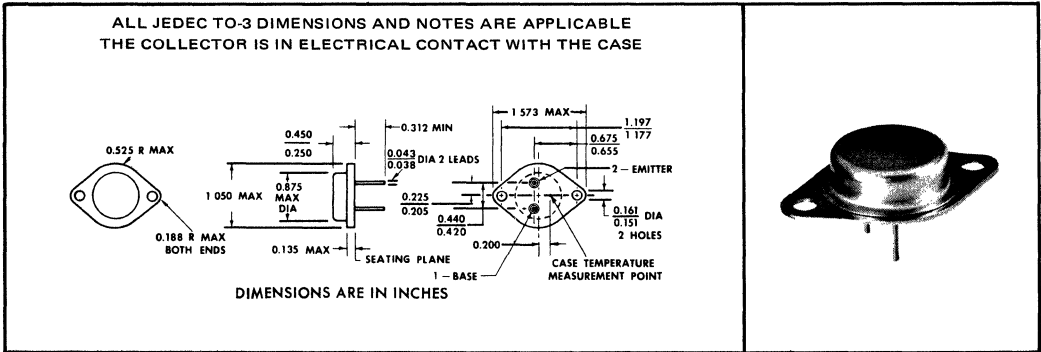
$$P_{T(max)} = \frac{175 - 50}{0.1(2.5) + 0.105(0.5)} = 413 \text{ W}$$

TYPE 2N3902 N-P-N SILICON POWER TRANSISTOR

**HIGH VOLTAGE, HIGH FORWARD AND REVERSE ENERGY
DESIGNED FOR INDUSTRIAL AND MILITARY APPLICATIONS**

- 100 W at 75°C Case Temperature
- 400 V Collector-Emitter Off-State Voltage
- Min $V_{(BR)CEO}$ of 325 V
- Max t_{off} of 1.7 μs at $I_C = 1 A$
- Typ $V_{CE(sat)}$ of 0.25 V at $I_C = 2.5 A$
- Typ f_T of 5 MHz at 10 V, 0.2 A

***mechanical data**



TYPE 2N3902
BULLETIN NO. DL-S-711473, APRIL 1971
REVISED DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

* Collector-Emitter Voltage (See Note 1)	400 V
* Emitter-Base Voltage	5 V
* Continuous Collector Current	2.5 A
* Continuous Base Current	1 A
Safe Operating Area at (or below) 75°C Case Temperature	See Figure 6
* Continuous Device Dissipation at (or below) 75°C Case Temperature (See Note 2)	100 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	4 W
Unclamped Inductive Load Energy (See Note 4)	180 mJ
* Operating Collector Junction Temperature Range	-65°C to 150°C
* Storage Temperature Range	-65°C to 200°C
* Terminal Temperature 1/16 Inch from Case for 10 Seconds	300°C

NOTES: 1. This value applies only when the collector-emitter voltage is applied with the transistor in the off-state and the base-emitter diode is open-circuited or reverse-biased. In operation, the limitations of Figure 7 must be observed.
 2. Derate linearly to 150°C case temperature at the rate of 1.33 W/°C.
 3. Derate linearly to 150°C free-air temperature at the rate of 32 mW/°C.
 4. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 40 \text{ mH}$, $R_{BB2} = 3 \text{ k}\Omega$, $V_{BB2} = 1.5 \text{ V}$, $R_S = 0.1 \Omega$, $V_{CC} = 50 \text{ V}$. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPE 2N3902

N-P-N SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 100 \text{ mA}$, $I_B = 0$, See Note 5	325			V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 400 \text{ V}$, $I_B = 0$		0.25		mA
I_{CEV}	Collector Cutoff Current	$V_{CE} = 400 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		0.25		mA
I_{EBO}	Emitter Cutoff Current	$V_{CE} = 400 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 125^\circ\text{C}$		0.5		mA
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		5		mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 5 and 6	30		90	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6	10			
V_{BE}	Base-Emitter Voltage	$I_B = 0.5 \text{ A}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6		1	2	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.1 \text{ A}$, $I_C = 1 \text{ A}$, See Notes 5 and 6		0.2	0.8	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6		0.25	2.5	V
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ MHz}$		5		
f_{hfe}	Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = 12 \text{ V}$, $I_C = 0.2 \text{ A}$, See Note 7	40			kHz

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.
7. f_{hfe} is the frequency at which the magnitude of the small-signal forward current transfer ratio is 0.707 of its low-frequency value. For this device, the reference measurement is made at 1 kHz.

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	0.75	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	31.25	

*switching characteristics at 25°C case temperature

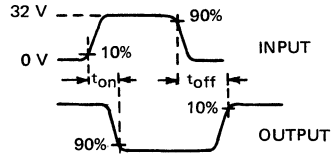
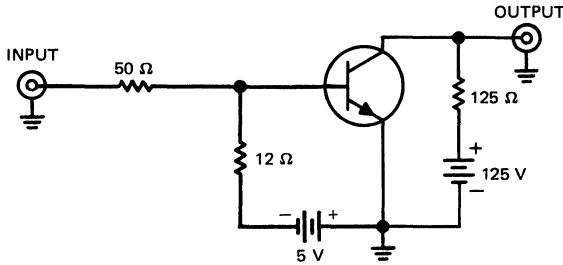
PARAMETER		TEST CONDITIONS†	MAX	UNIT
t_r	Rise Time	$I_C = 1 \text{ A}$, $I_B(1) = 0.1 \text{ A}$, $I_B(2) = -0.1 \text{ A}$, $V_{BE(off)} = -5 \text{ V}$, $R_L = 125 \Omega$, See Figure 1	0.8	μs
t_s	Storage Time		0.9	
t_f	Fall Time		0.8	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

TYPE 2N3902 N-P-N SILICON POWER TRANSISTOR

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

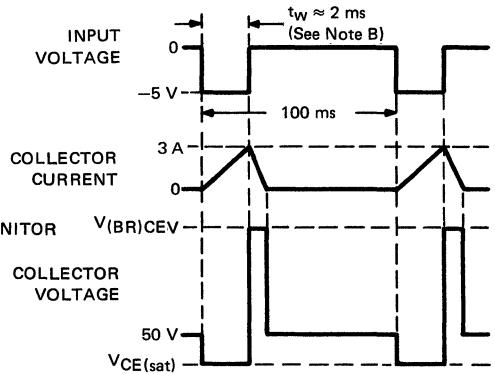
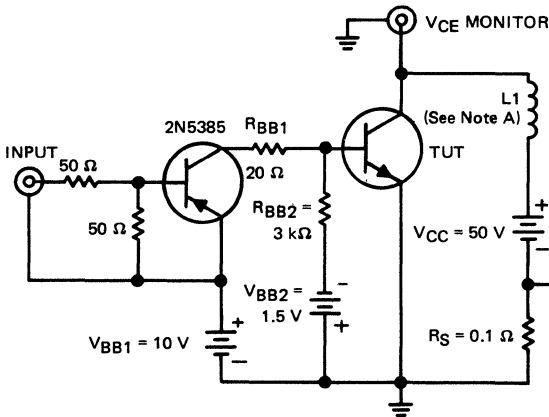
VOLTAGE WAVEFORMS

5

- NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 20$ ns, $t_f \leq 20$ ns, $Z_{out} = 50 \Omega$, $t_w = 5 \mu$ s, duty cycle $\leq 5\%$.
 B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 20$ ns, $R_{in} \geq 100$ k Ω , $C_{in} \leq 50$ pF.
 C. Resistors must be noninductive types.
 D. The d-c power supply may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. L1 is a 40-mH inductor.
 B. Input pulse width is increased until $I_{CM} = 3$ A.

FIGURE 2

TYPE 2N3902

N-P-N SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO VS COLLECTOR CURRENT

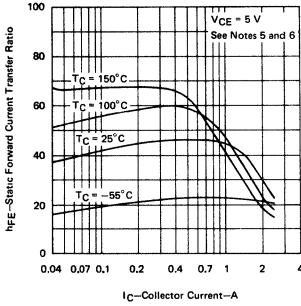


FIGURE 3

BASE-EMITTER VOLTAGE VS CASE TEMPERATURE

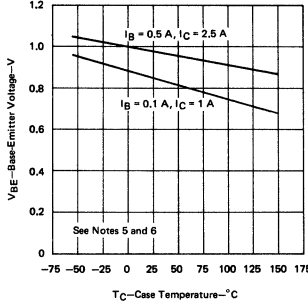


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE VS CASE TEMPERATURE

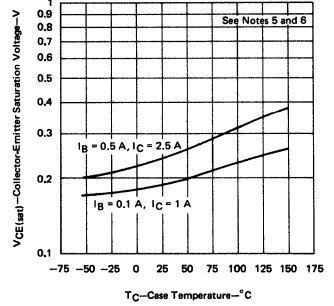


FIGURE 5

- NOTES: 5. These parameters must be measured using pulse techniques, $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

MAXIMUM SAFE OPERATING AREA

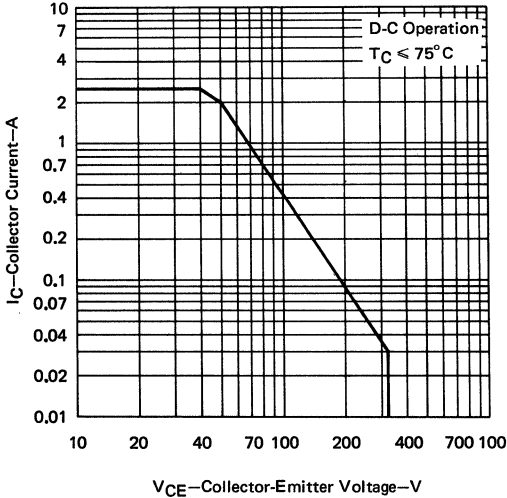


FIGURE 6

THERMAL INFORMATION

DISSIPATION DERATING CURVE

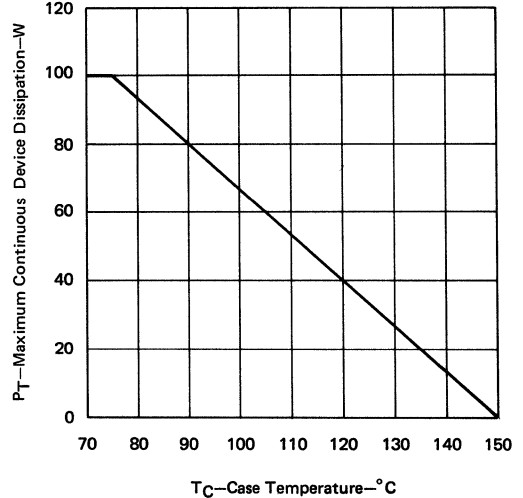


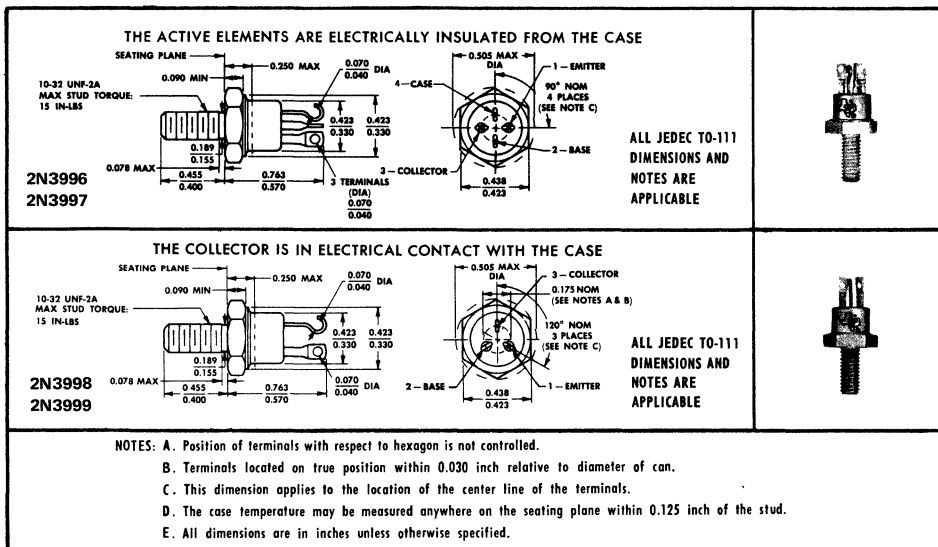
FIGURE 7

TYPES 2N3996, 2N3997, 2N3998, 2N3999 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

FOR HIGH-SPEED POWER SWITCHING APPLICATIONS

- 30 W at 100°C Case Temperature
- Isolated-Stud Package (2N3996, 2N3997)
- Max $V_{CE(sat)}$ of 0.25 V at 1 A I_C
- Max t_{on} of 300 ns at 1 A I_C
- Min f_T of 40 MHz

*mechanical data



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 1)	80 V
Emitter-Base Voltage	8 V
Continuous Collector Current	5 A
Peak Collector Current (See Note 2)	10 A
Continuous Base Current	1 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 8
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	30 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 1$ ms, duty cycle $\leq 50\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.3 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/deg.

*Indicates JEDEC registered data.

TYPES 2N3996, 2N3997, 2N3998, 2N3999
 BULLETIN NO. DLS-718257, MARCH 1966
 REVISED SEPTEMBER 1971

5

TYPES 2N3996, 2N3997, 2N3998, 2N3999

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

* electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3996 2N3998		2N3997 2N3999		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 50 \text{ mA}$, $I_B = 0$, See Note 5	80		80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $I_B = 0$	10		10		μA
I_{CES} Collector Cutoff Current	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$	5		5		μA
	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	50		50		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	0.5		0.5		μA
	$V_{EB} = 8 \text{ V}$, $I_C = 0$	10		10		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 50 \text{ mA}$	30		60		
	$V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$, See Note 5	40 120		80 240		
	$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$, See Note 5	15		20		
	$V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$, $T_C = -55^\circ\text{C}$, See Note 5	10		20		
V_{BE} Base-Emitter Voltage	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$, See Note 5	0.6 1.2		0.6 1.2		V
	$I_B = 500 \text{ mA}$, $I_C = 5 \text{ A}$, See Note 5	1.6		1.6		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$, See Note 5	0.25		0.25		V
	$I_B = 500 \text{ mA}$, $I_C = 5 \text{ A}$, See Note 5	2		2		
$ h_{re} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 10 \text{ MHz}$	4		4		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	150		150		pF

NOTE 5: This parameter must be measured using pulse techniques: $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

* thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	3.33	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	87.5	deg/W

* switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	2N3996 2N3998	2N3997 2N3999	UNIT
		MAX	MAX	
t_{on} Turn-On Time	$I_C = 1 \text{ R}$, $I_{B(1)} = 100 \text{ mA}$, $I_{B(2)} = -100 \text{ mA}$, $V_{BE(off)} = -3.7 \text{ V}$, $R_L = 20 \Omega$, See Figure 1	0.3	0.3	μs
t_{off} Turn-Off Time		1.5	2	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

* Indicates JEDEC registered data.

TYPES 2N3996, 2N3997, 2N3998, 2N3999 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

*PARAMETER MEASUREMENT INFORMATION

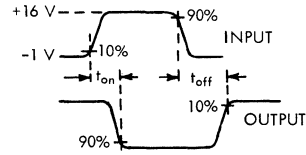
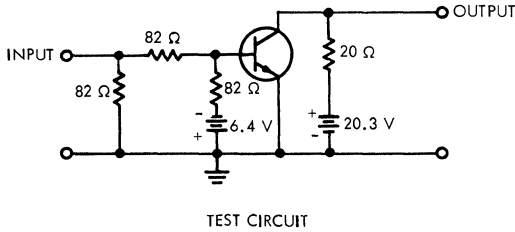


FIGURE 1

- NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50 \Omega$, $t_p = 2 \mu$ s, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPICAL CHARACTERISTICS

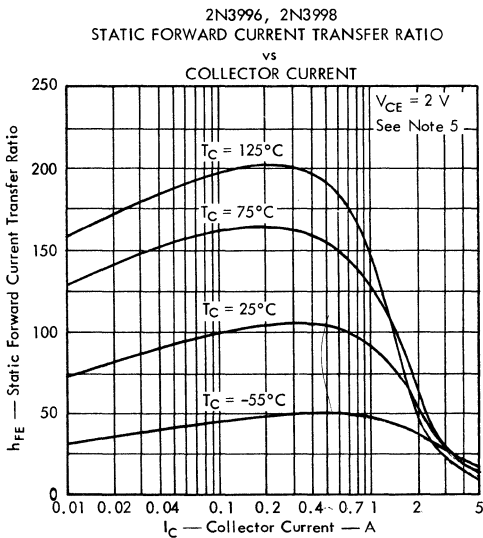


FIGURE 2

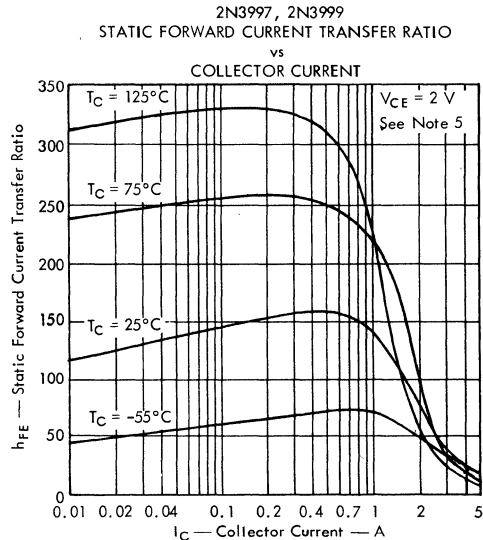


FIGURE 3

NOTE 5: This parameter must be measured using pulse techniques: $t_p = 300 \mu$ s, duty cycle $\leq 2\%$.
*Indicates JEDEC registered data.

TYPES 2N3996, 2N3997, 2N3998, 2N3999

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

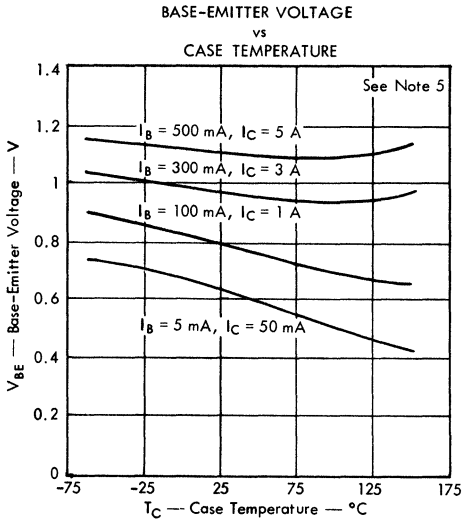


FIGURE 4

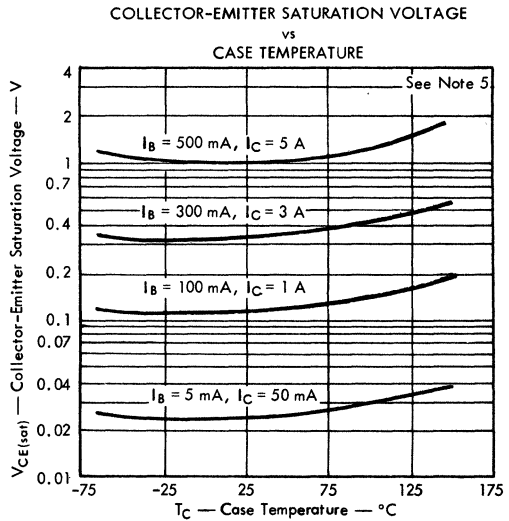


FIGURE 5

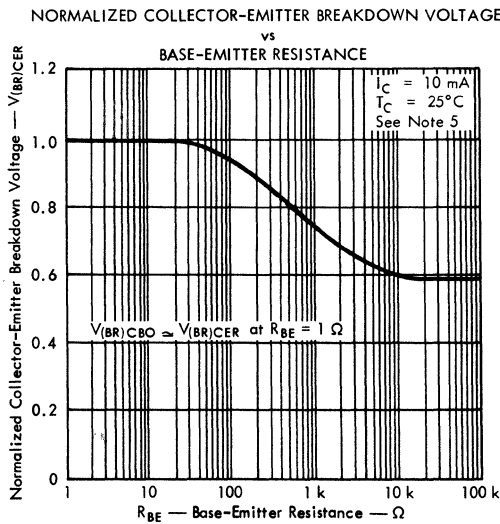


FIGURE 6

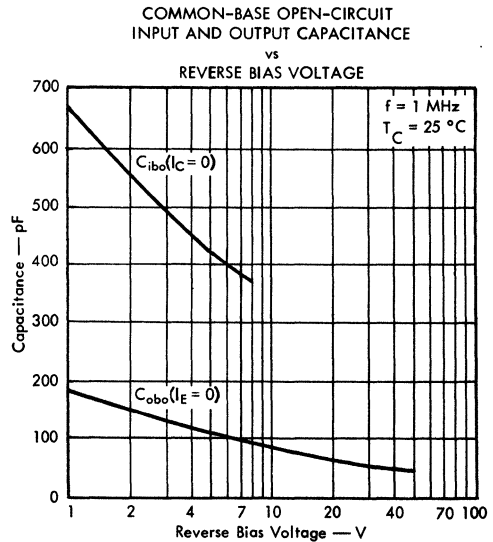


FIGURE 7

NOTE 5: This parameter must be measured using pulse techniques: $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

TYPES 2N3996, 2N3997, 2N3998, 2N3999 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGION

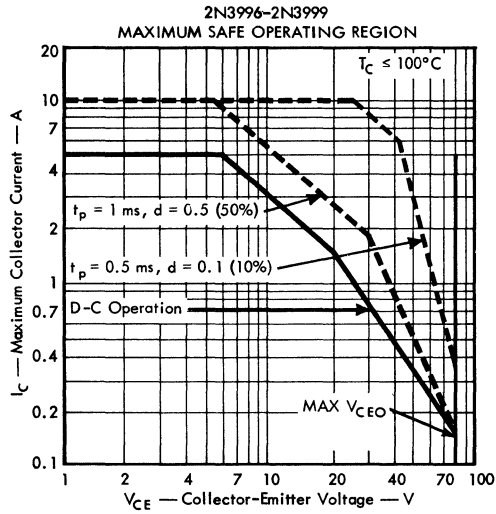


FIGURE 8

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TYPES 2N3996, 2N3997, 2N3998, 2N3999

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

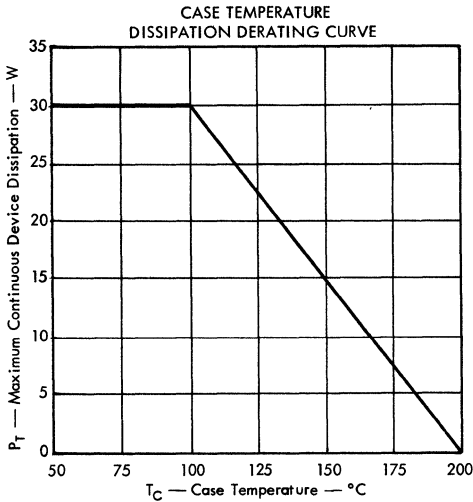


FIGURE 9

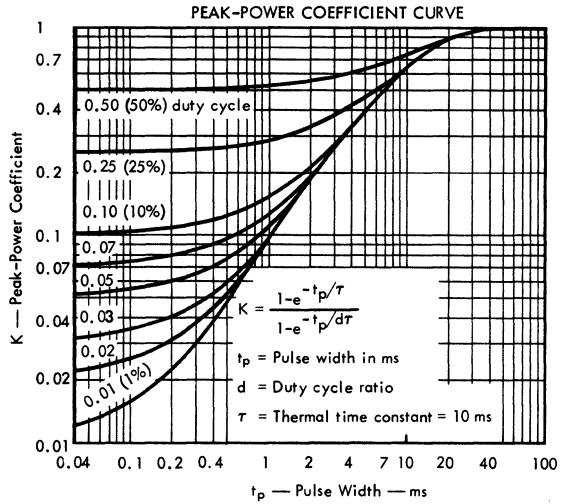


FIGURE 10

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	87.5	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	3.33	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	84.17	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 10	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 7 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 10, Peak-Power Coefficient

$$K = 0.103 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + (0.103)3.33} = 143 \text{ W}$$

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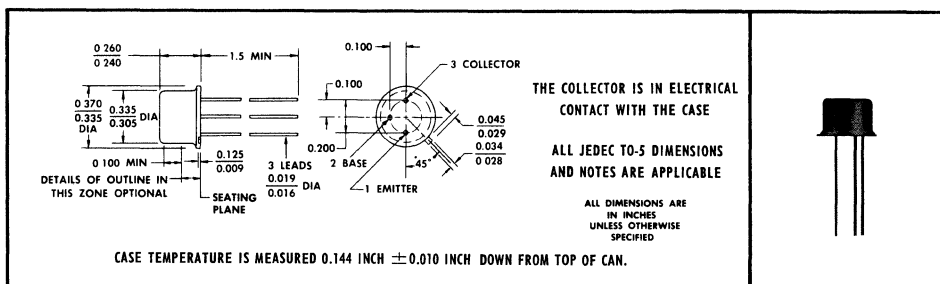
TYPES 2N4000, 2N4001 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPES 2N4000, 2N4001
BULLETIN NO. DL-5 568214, MARCH 1966

FOR HIGH-SPEED POWER SWITCHING APPLICATIONS

- 15 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.3 V at 0.5 A I_C
- Max t_{on} of 300 ns at 0.5 A I_C
- Min f_T of 40 MHz

*mechanical data



5

* absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4000	2N4001
Collector-Base Voltage	100 V	120 V
Collector-Emitter Voltage (See Note 1)	80 V	100 V
Emitter-Base Voltage	← 8 V →	← 8 V →
Continuous Collector Current	← 1 A →	← 1 A →
Peak Collector Current (See Note 2)	← 3 A →	← 3 A →
Continuous Base Current	← 0.5 A →	← 0.5 A →
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 8	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 15 W →	← 15 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1 W →	← 1 W →
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead Temperature 1/16 Inch from Case for 10 Seconds	← 230°C →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 1$ ms, duty cycle $\leq 50\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.15 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.72 mW/°C.

* JEDEC registered data

TYPES 2N4000, 2N4001

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4000		2N4001		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $I_B = 0$	10				μA
	$V_{CE} = 80 \text{ V}$, $I_B = 0$			10		
I_{CES} Collector Cutoff Current	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$	2				μA
	$V_{CE} = 110 \text{ V}$, $V_{BE} = 0$			2		
	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	50				
	$V_{CE} = 110 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$			50		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	500		500		nA
	$V_{EB} = 8 \text{ V}$, $I_C = 0$	10		10		μA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 50 \text{ mA}$	10		20		
	$V_{CE} = 2 \text{ V}$, $I_C = 0.5 \text{ A}$, See Note 5	30	120	40	120	
	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, See Note 5	10		20		
	$V_{CE} = 2 \text{ V}$, $I_C = 0.5 \text{ A}$, $T_C = -55^\circ\text{C}$, See Note 5	10		15		
V_{BE} Base-Emitter Voltage	$I_B = 50 \text{ mA}$, $I_C = 0.5 \text{ A}$, See Note 5	1		1		V
	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$, See Note 5	1.2		1.2		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 50 \text{ mA}$, $I_C = 0.5 \text{ A}$, See Note 5	0.3		0.3		V
	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$, See Note 5	0.5		0.5		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 20 \text{ MHz}$	2		2		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	60		60		pF

NOTE 5: These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

*thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	6.67	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	175	

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = 0.5 \text{ A}$, $I_{B(1)} = 50 \text{ mA}$, $I_{B(2)} = -50 \text{ mA}$,	0.3	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -4 \text{ V}$, $R_L = 20 \Omega$, See Figure 1	2	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

TYPES 2N4000, 2N4001 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION

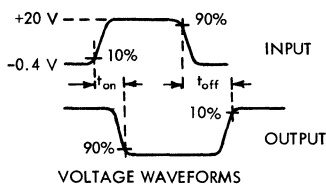
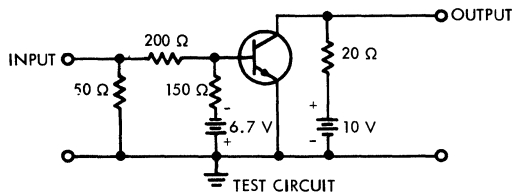


FIGURE 1

- NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 5 \text{ pF}$.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPES 2N4000, 2N4001

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

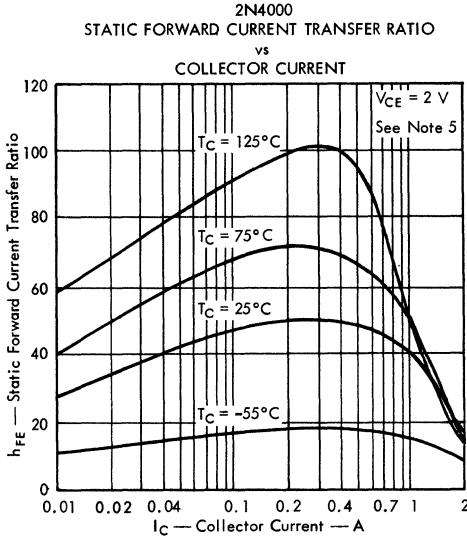


FIGURE 2

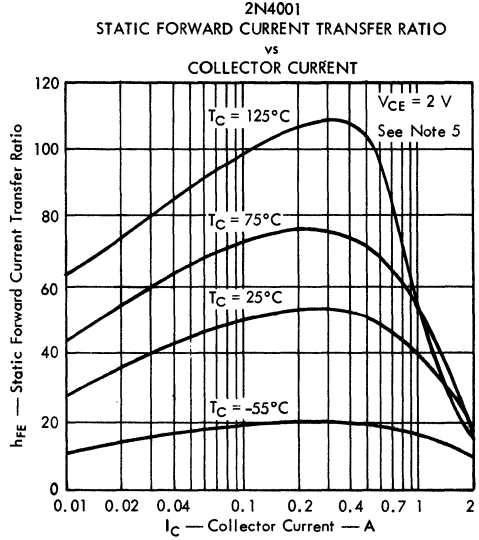


FIGURE 3

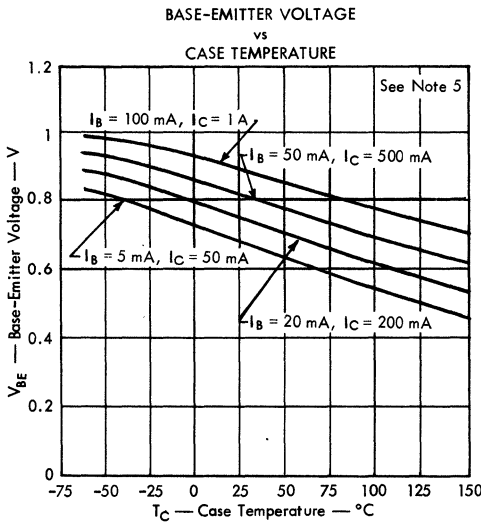


FIGURE 4

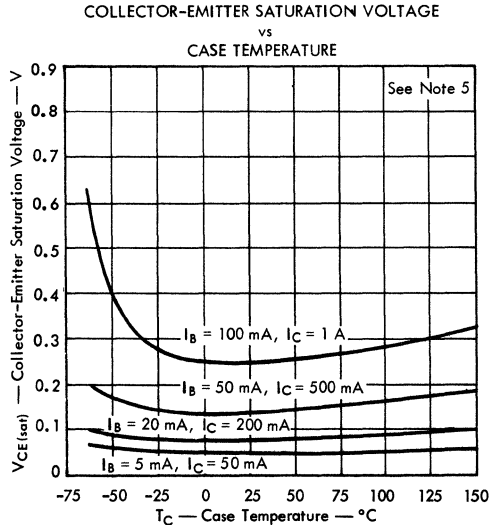


FIGURE 5

NOTE 5: These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

TYPES 2N4000, 2N4001 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

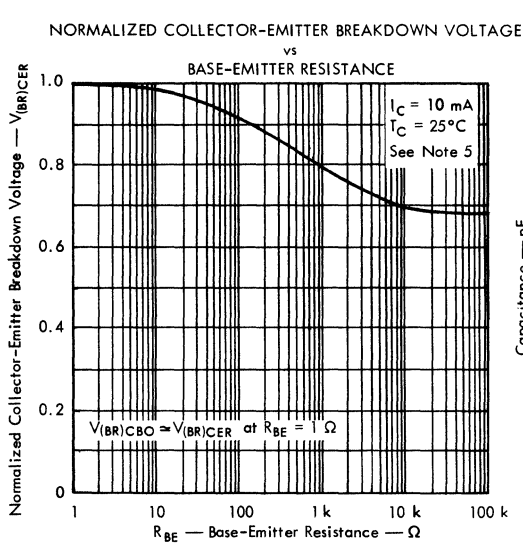


FIGURE 6

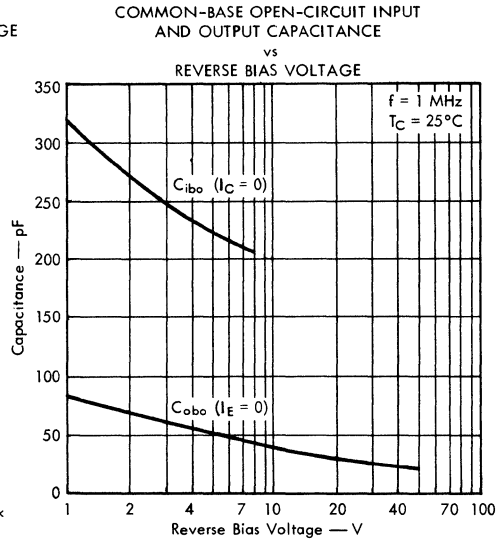


FIGURE 7

NOTE 5: These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

MAXIMUM SAFE OPERATING REGION

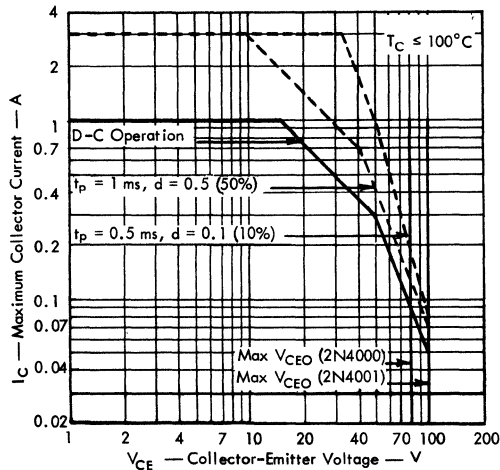


FIGURE 8

TYPES 2N4000, 2N4001

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

THERMAL INFORMATION

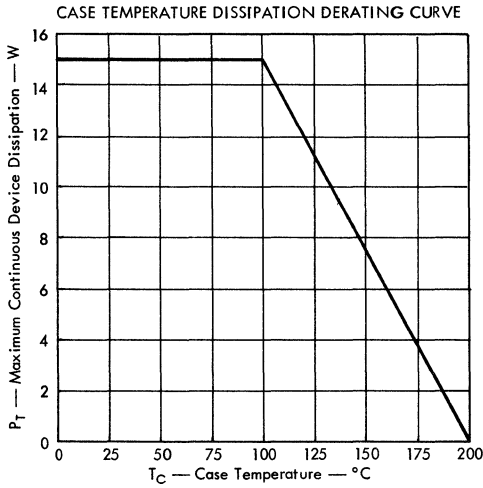


FIGURE 9

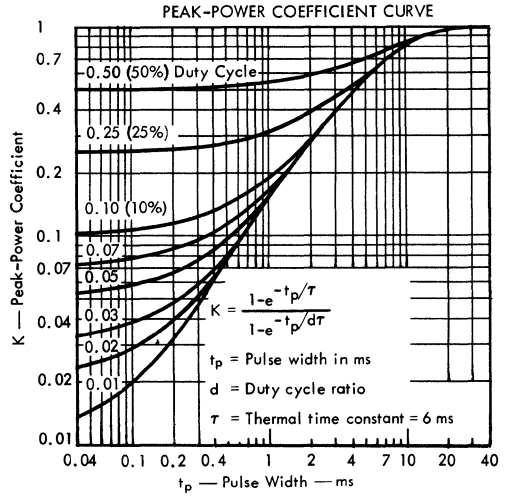


FIGURE 10

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	6.67	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168.33	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 10	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 7 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 1 \text{ ms}$$

Solution:

From Figure 10, Peak-Power Coefficient

$$K = 0.19 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + (0.19)(6.67)} = 76 \text{ W}$$

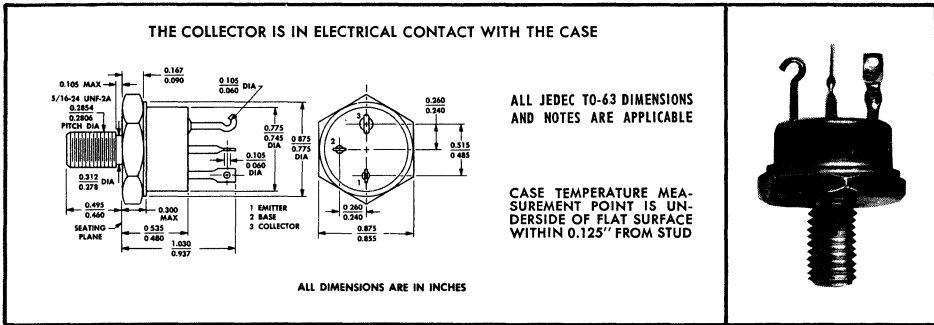
TYPES 2N4002, 2N4003 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPES 2N4002, 2N4003
BULLETIN NO. DI-5-688606, MAY 1966
REVISED MAY 1968

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 30-A Rated Continuous Collector Current
- 100 Watts at 100°C Case Temperature
- Maximum $V_{CE(sat)}$ of 1.2 V at 30 A
- Maximum V_{BE} of 1.8 V at 30 A
- Maximum t_{on} of 1 μs at 15 A

***mechanical data**



***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

	2N4002	2N4003
Collector-Base Voltage	100 V	120 V
Collector-Emitter Voltage (See Note 1)	80 V	100 V
Emitter-Base Voltage	← 8 V →	
Continuous Collector Current	← 30 A →	
Peak Collector Current (See Note 2)	← 40 A →	
Continuous Base Current	← 10 A →	
Continuous Emitter Current	← 30 A →	
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 100 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →	
Operating Collector Junction Temperature Range	← -65°C to 200°C →	
Storage Temperature Range	← -65°C to 200°C →	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 230°C →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data.

TYPES 2N4002, 2N4003

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4002		2N4003		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$	2				mA
	$V_{CE} = 50 \text{ V}$, $I_B = 0$			2		
I_{CES} Collector Cutoff Current	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$	1				mA
	$V_{CE} = 110 \text{ V}$, $V_{BE} = 0$			1		
	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	2				
	$V_{CE} = 110 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$			2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	100		100		μA
	$V_{EB} = 8 \text{ V}$, $I_C = 0$	50		50		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$, See Notes 5 and 6	10		10		
	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	20	80	20	80	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$, See Notes 5 and 6	1.8		1.8		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 4 \text{ A}$, $I_C = 30 \text{ A}$, See Notes 5 and 6	1.2		1.2		V
h_{fo} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	30		30		
$ h_{fo} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 10 \text{ MHz}$	3		3		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	1	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	43.7	deg/W

*Indicates JEDEC registered data.

TYPES 2N4002, 2N4003 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = 15 \text{ A}$, $I_{B(1)} = 1.5 \text{ A}$, $I_{B(2)} = -1.5 \text{ A}$,	1	μs
t_{off} Turn-Off Time	$V_{BE (off)} = -2 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	3	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION

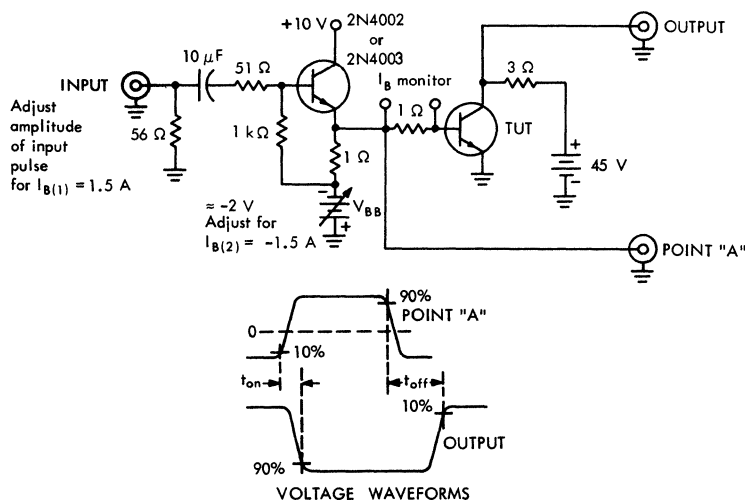


FIGURE 1

- NOTES: a. The input waveform at point "A" has the following characteristics: $t_r \leq 100 \text{ ns}$, $t_f \leq 100 \text{ ns}$, $t_p = 20 \mu\text{s}$, duty cycle $\leq 0.2\%$.
 b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5 \text{ ns}$, $R_{in} \geq 1 \text{ M}\Omega$, $C_{in} \leq 5 \text{ pF}$.
 c. Resistors must be noninductive types.
 d. The d-c power supplies may require additional bypassing in order to minimize ringing.

*Indicates JEDEC registered data.

5

TYPES 2N4002, 2N4003 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

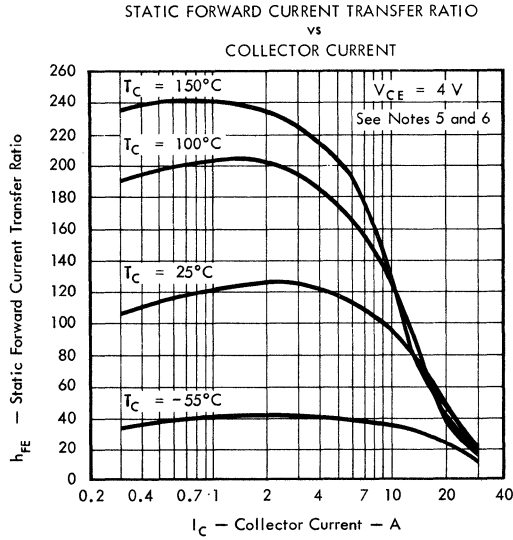


FIGURE 2

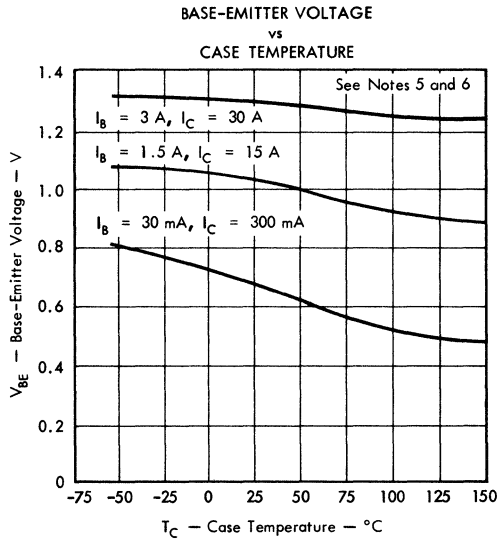


FIGURE 3

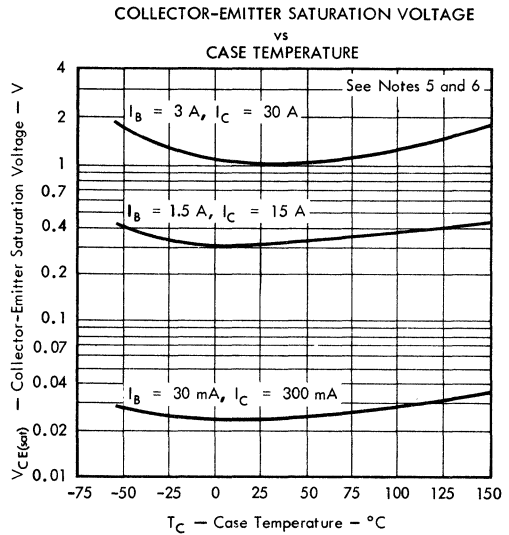


FIGURE 4

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N4002, 2N4003 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

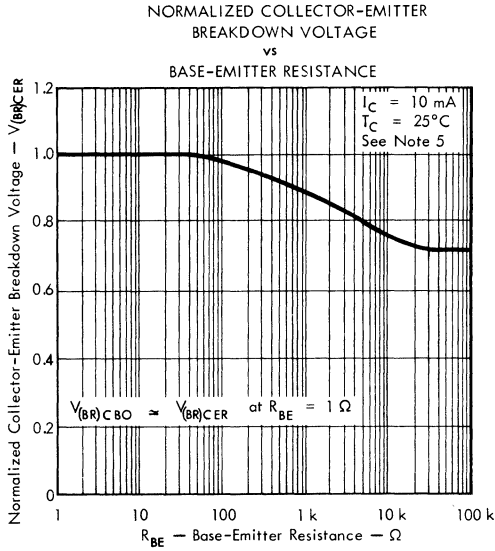


FIGURE 5

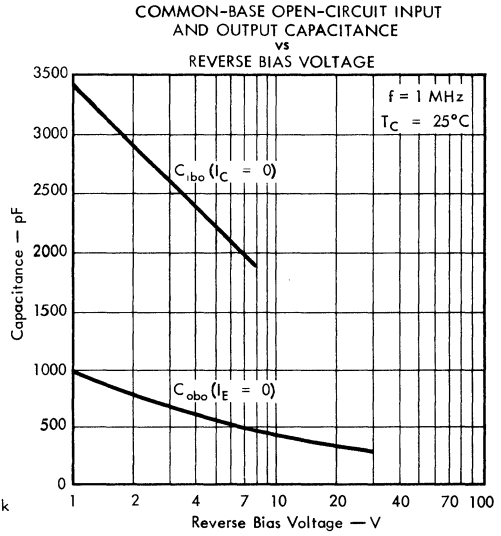


FIGURE 6

NOTE 5: These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

MAXIMUM SAFE OPERATING REGION

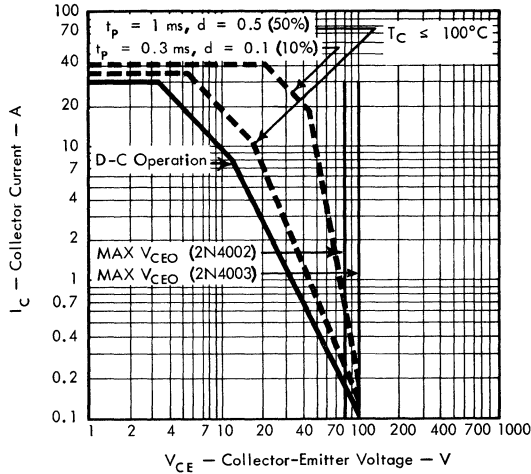


FIGURE 7

5

TYPES 2N4002, 2N4003 N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

THERMAL INFORMATION

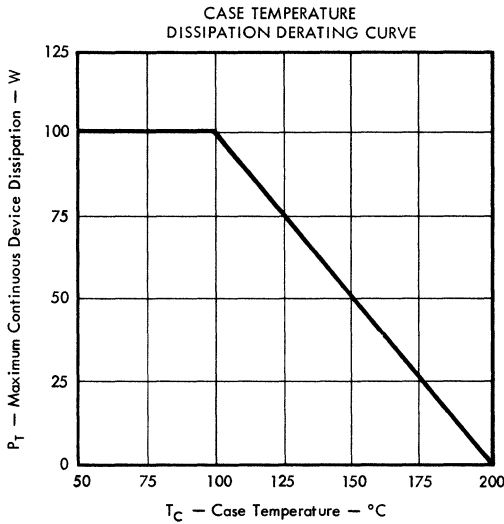


FIGURE 8

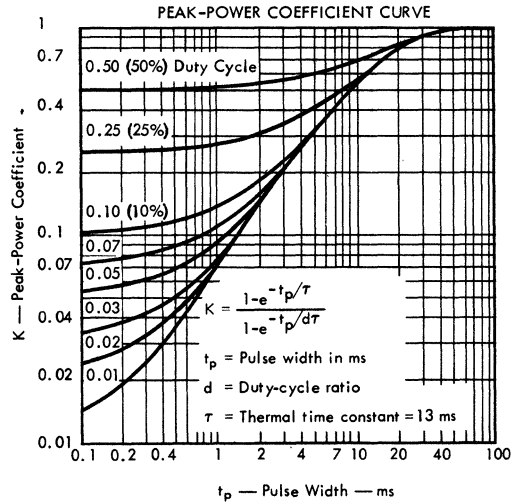


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(avg)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	43.7	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	1	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	42.7	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		$^{\circ}C$
T_C	Case Temperature		$^{\circ}C$
$T_{J(avg)}$	Average Junction Temperature	≤ 200	$^{\circ}C$
$T_{J(max)}$	Peak Junction Temperature	≤ 200	$^{\circ}C$
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^{\circ}C \leq T_C \leq 200^{\circ}C, \text{ as in Figure 8}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-A}} \text{ for } 25^{\circ}C \leq T_A \leq 200^{\circ}C$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^{\circ}C \leq T_C \leq 200^{\circ}C$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^{\circ}C \leq T_A \leq 200^{\circ}C$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 2.5 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(avg)} \text{ (design limit)} = 200^{\circ}C$$

$$T_A = 50^{\circ}C$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.1 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(2.5) + 0.1(1)} = 428 \text{ W}$$

TYPES 2N4004, 2N4005

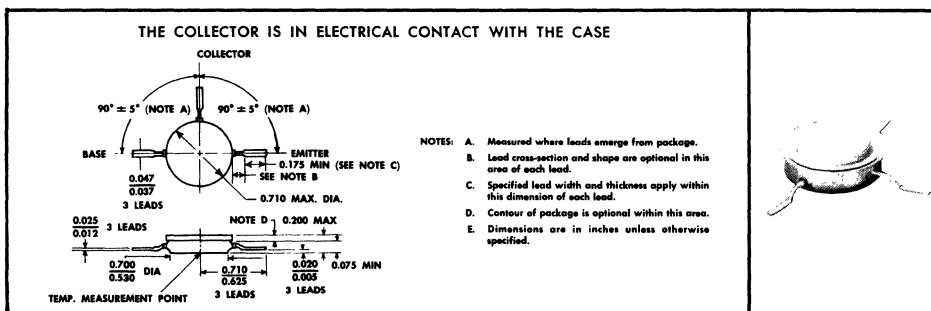
N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPES 2N4004, 2N4005
BULLETIN NO. DL-5 668607, SEPTEMBER 1966

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 20 A Rated Collector Current
- 40 Watts at 100°C Case Temperature
- Maximum $V_{CE(sat)}$ of 1 V at 20 A
- Maximum V_{BE} of 1.6 V at 20 A
- Maximum t_{on} of 1 μ s at 10 A

***mechanical data**



5

***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

	2N4004	2N4005
Collector-Base Voltage	100 V	120 V
Collector-Emitter Voltage (See Note 1)	80 V	100 V
Emitter-Base Voltage	← 8 V →	← 8 V →
Continuous Collector Current	← 20 A →	← 20 A →
Peak Collector Current (See Note 2)	← 30 A →	← 30 A →
Continuous Base Current	← 10 A →	← 10 A →
Continuous Emitter Current	← 20 A →	← 20 A →
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 40 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1.2 W →	
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead Temperature $\frac{1}{16}$ Inch from Case for 10 Seconds	← 230°C →	

- NOTES:
1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.4 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 6.87 mW/deg.

*Indicates JEDEC registered data.

TYPES 2N4004, 2N4005

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4004		2N4005		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$		2			mA
	$V_{CE} = 50 \text{ V}$, $I_B = 0$				2	
I_{CES} Collector Cutoff Current	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$		1			mA
	$V_{CE} = 110 \text{ V}$, $V_{BE} = 0$				1	
	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		2			
	$V_{CE} = 110 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$				2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		100		100	μA
	$V_{EB} = 8 \text{ V}$, $I_C = 0$		50		50	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 20 \text{ A}$, See Notes 5 and 6	15		15		
	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 5 and 6	30	150	30	150	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 20 \text{ A}$, See Notes 5 and 6		1.6		1.6	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 3 \text{ A}$, $I_C = 20 \text{ A}$, See Notes 5 and 6		1		1	V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	30		30		
$ h_{fo} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 10 \text{ MHz}$	3		3		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts. The voltage-sensing contacts are separate from current-carrying contacts.

*thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance		2.5	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance		146	deg/W

*Indicates JEDEC registered data.

TYPES 2N4004, 2N4005

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

* switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = 10 \text{ A}$, $I_{B(1)} = 0.8 \text{ A}$, $I_{B(2)} = -0.8 \text{ A}$,	1	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -1 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	4	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION

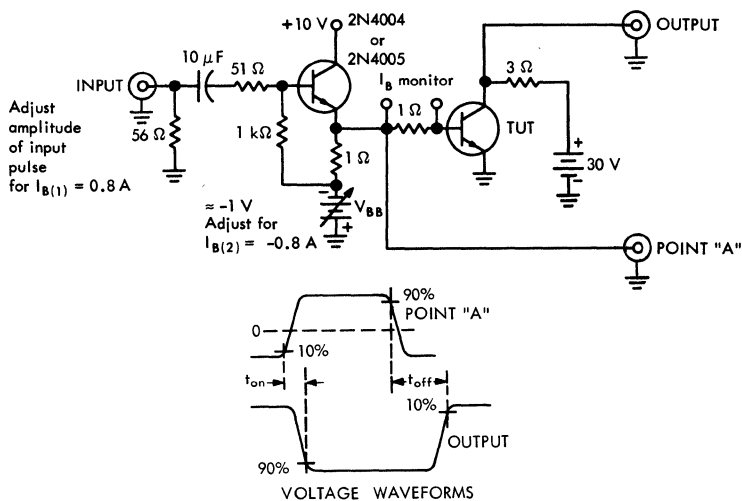


FIGURE 1

- NOTES: a. The input waveform at point "A" has the following characteristics: $t_r \leq 100 \text{ ns}$, $t_f \leq 100 \text{ ns}$, $t_p = 20 \mu\text{s}$, duty cycle $\leq 0.2\%$.
 b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5 \text{ ns}$, $R_{in} \geq 1 \text{ M}\Omega$, $C_{in} \leq 5 \text{ pF}$.
 c. Resistors must be noninductive types.
 d. The d-c power supplies may require additional bypassing in order to minimize ringing.

*Indicates JEDEC registered data.

5

TYPES 2N4004, 2N4005

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

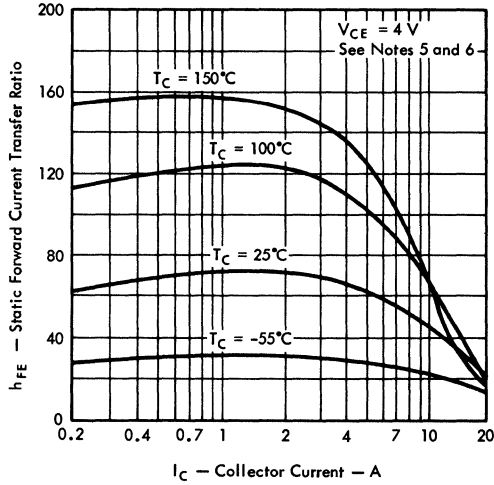


FIGURE 2

BASE-EMITTER VOLTAGE
vs
CASE TEMPERATURE

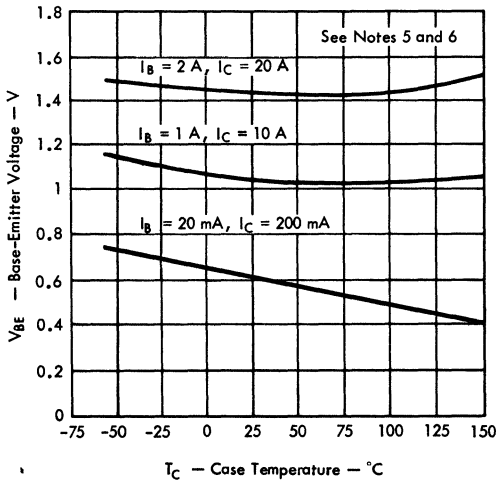


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE

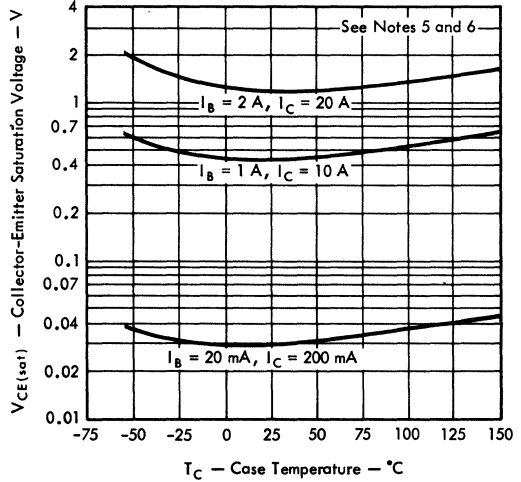
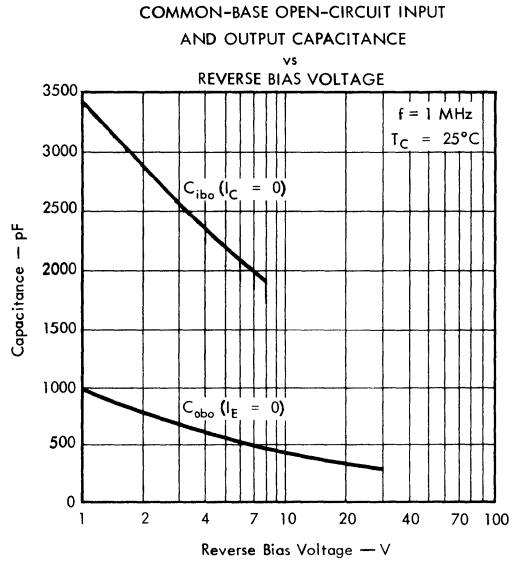
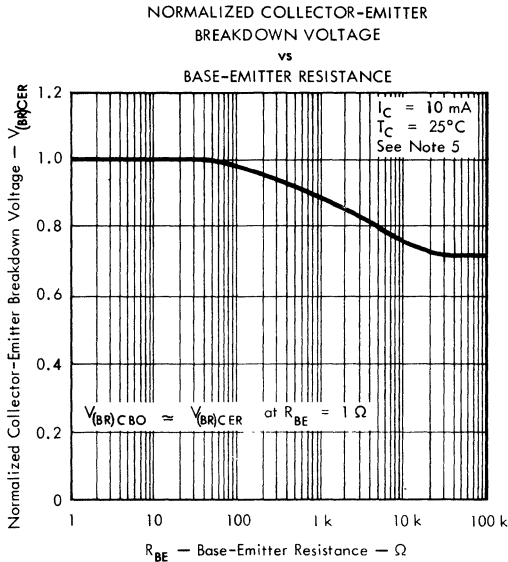


FIGURE 4

TYPES 2N4004, 2N4005

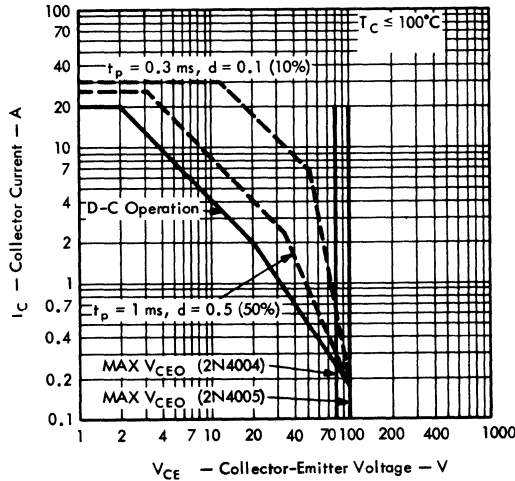
N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS



NOTE 5: These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

MAXIMUM SAFE OPERATING REGION



5

TYPES 2N4004, 2N4005

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTORS

THERMAL INFORMATION

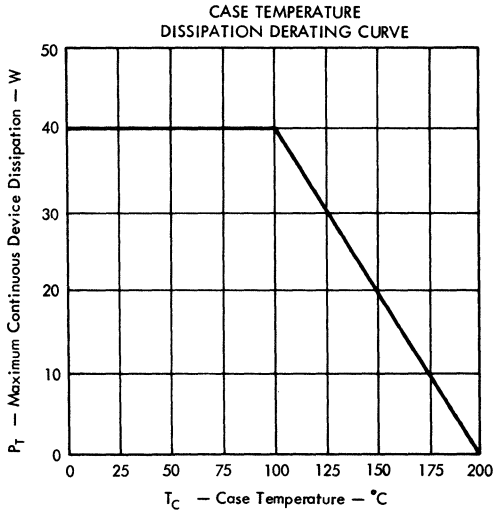


FIGURE 8

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(avg)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	146	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	2.5	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	143.5	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(avg)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 2.5 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(avg)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

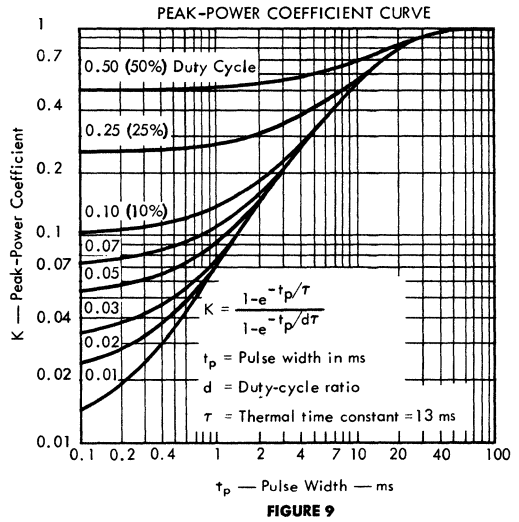


FIGURE 9

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}, \text{ as in Figure 8}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.1 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(2.5) + 0.1(2.5)} = 300 \text{ W}$$

TYPE 2N4300

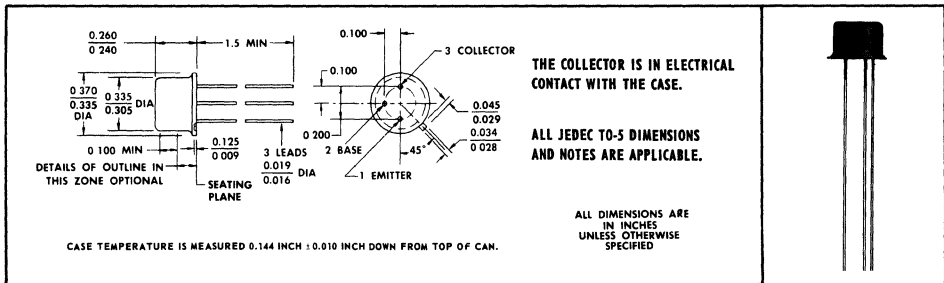
N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPE 2N4300
BULLETIN NO. DL-5-668562, MAY 1966

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 15 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.3 V at 1 A I_C
- Typ t_{on} of 130 ns at 1 A I_C
- Min f_T of 30 MHz

***mechanical data**



***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 1)	80 V
Emitter-Base Voltage	8 V
Continuous Collector Current	2 A
Peak Collector Current (See Note 2)	4 A
Continuous Base Current	1 A
Continuous Emitter Current	3 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	15 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	1 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.15 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.72 mW/deg.

*Indicates JEDEC registered data.

TYPE 2N4300

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$		1	μA
I_{CES} Collector Cutoff Current	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$		10	μA
	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		75	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		0.5	μA
	$V_{EB} = 8 \text{ V}$, $I_C = 0$		10	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 5 and 6	30	120	
	$V_{CE} = 2 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 5 and 6	15		
V_{BE} Base-Emitter Voltage	$V_{CE} = 2 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 5 and 6		1.2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$, See Notes 5 and 6		0.3	V
	$I_B = 200 \text{ mA}$, $I_C = 2 \text{ A}$, See Notes 5 and 6		0.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	30		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 15 \text{ MHz}$	2		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	6.66	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	175	

*Indicates JEDEC registered data.

TYPE 2N4300

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_{B(1)} = 100 \text{ mA}$, $I_{B(2)} = -100 \text{ mA}$	0.13	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -3.7 \text{ V}$, $R_L = 20 \Omega$, See Figure 1		

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

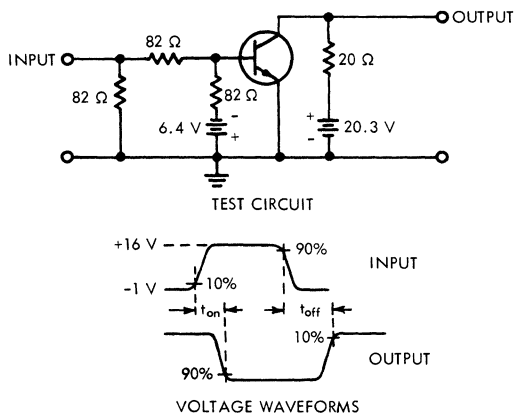


FIGURE 1

- NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 2 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPE 2N4300

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

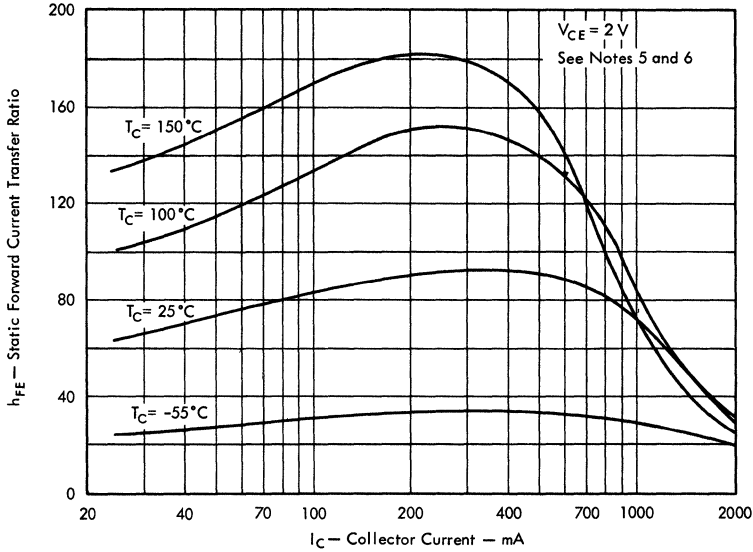


FIGURE 2

BASE-EMITTER VOLTAGE
vs
CASE TEMPERATURE

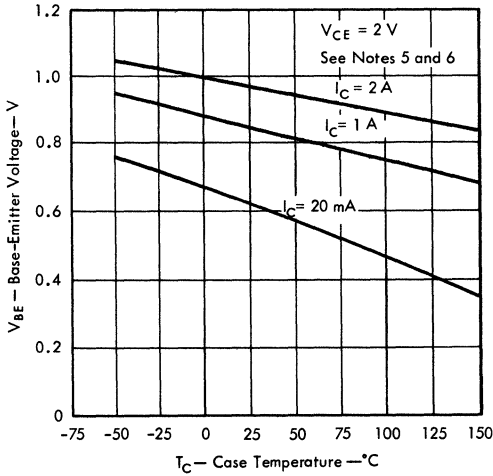


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE

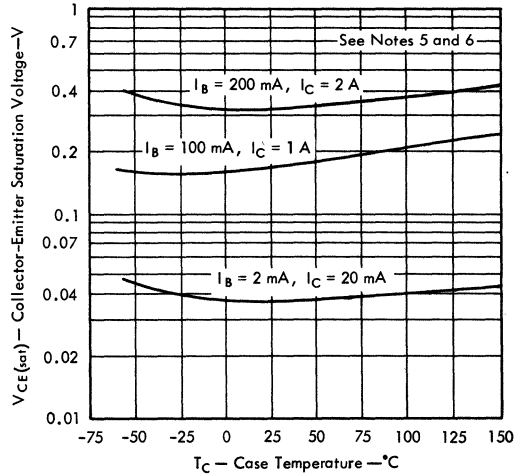


FIGURE 4

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPE 2N4300

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

NORMALIZED COLLECTOR - EMITTER BREAKDOWN VOLTAGE
vs
BASE - EMITTER RESISTANCE

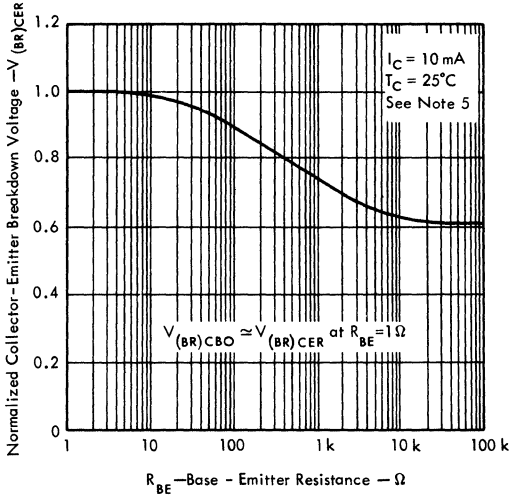


FIGURE 5

COMMON-BASE OPEN-CIRCUIT INPUT
AND OUTPUT CAPACITANCE
vs
REVERSE BIAS VOLTAGE

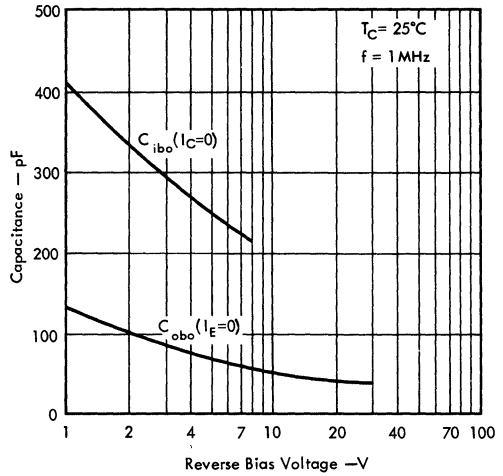


FIGURE 6

NOTE 5: These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

MAXIMUM SAFE OPERATING REGION

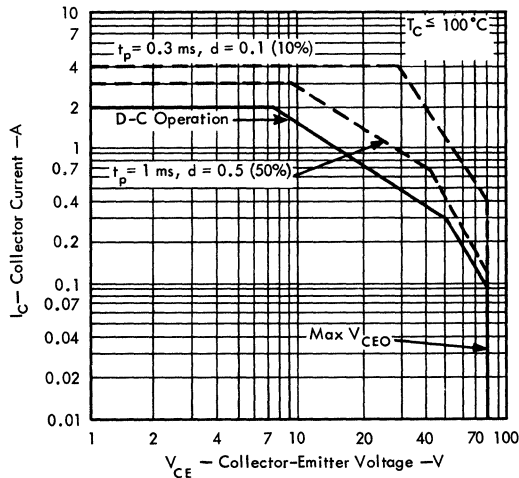


FIGURE 7

5

TYPE 2N4300

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

THERMAL INFORMATION

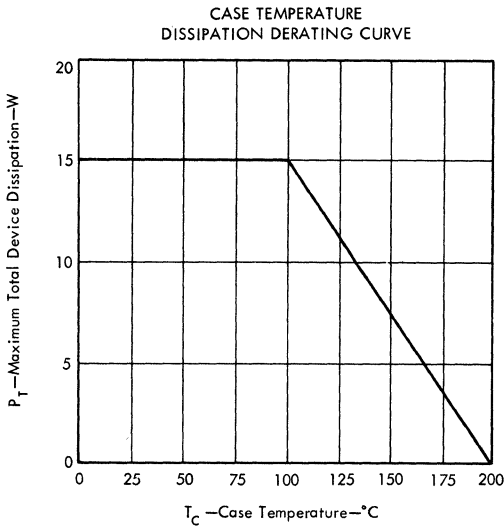


FIGURE 8

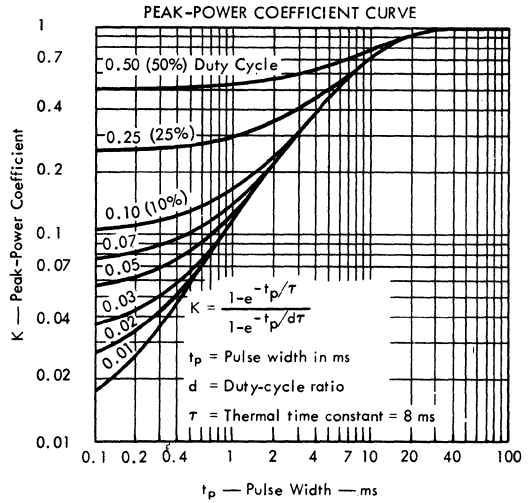


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	6.66	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \quad \text{for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C} \quad \text{as in Figure 8}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \quad \text{for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \quad \text{for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \quad \text{for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)
OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 7 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.105 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + 0.105(6.66)} = 107 \text{ W}$$

TYPE 2N4301

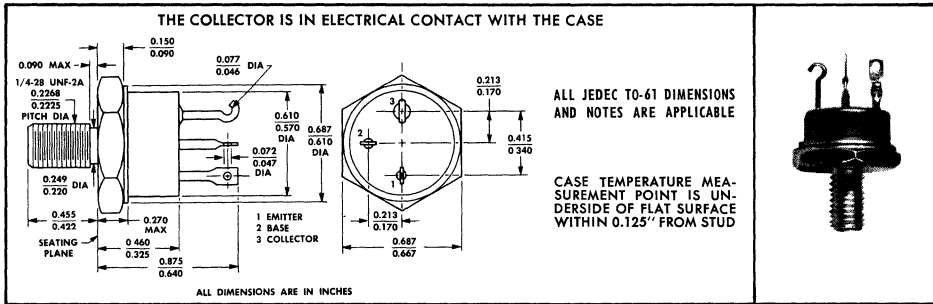
N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPE 2N4301
BULLETIN NO. DL-5 668510, MAY 1966

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 50 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.4 V at 5 A I_C
- Typ t_{on} of 150 ns at 5 A I_C
- Min f_T of 40 MHz

***mechanical data**



***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 1)	80 V
Emitter-Base Voltage	8 V
Continuous Collector Current	10 A
Peak Collector Current (See Note 2)	20 A
Continuous Base Current	4 A
Continuous Emitter Current	10 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	50 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	3.5 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	230°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 20 mW/deg.

*Indicates JEDEC registered data.



TYPE 2N4301

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	80		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$		10	μA
I_{CES}	Collector Cutoff Current	$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$		10	μA
		$V_{CE} = 90 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		500	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		5	μA
		$V_{EB} = 8 \text{ V}$, $I_C = 0$		50	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 5 and 6	30	120	
		$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 5 and 6	15		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 5 and 6		1.2	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$, See Notes 5 and 6		0.4	V
		$I_B = 1.3 \text{ A}$, $I_C = 10 \text{ A}$, See Notes 5 and 6		1	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	30		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 20 \text{ MHz}$	2		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	2	deg/W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	50	

*Indicates JEDEC registered data.

TYPE 2N4301

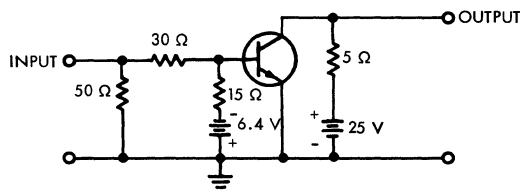
N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

switching characteristics at 25°C case temperature

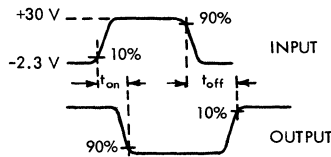
PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 5 \text{ A}$, $I_{B(1)} = 500 \text{ mA}$, $I_{B(2)} = -500 \text{ mA}$,	0.15	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -5 \text{ V}$, $R_L = 5 \Omega$, See Figure 1	1.5	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.

b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.

c. Resistors must be noninductive types.

d. The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPE 2N4301

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

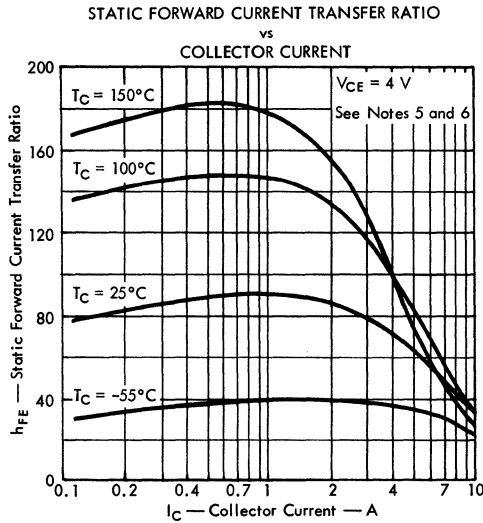


FIGURE 2

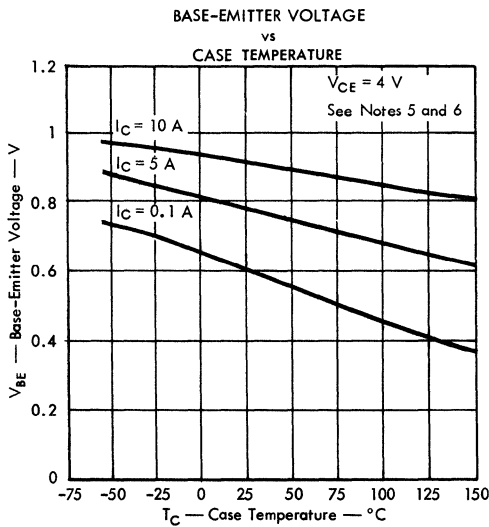


FIGURE 3

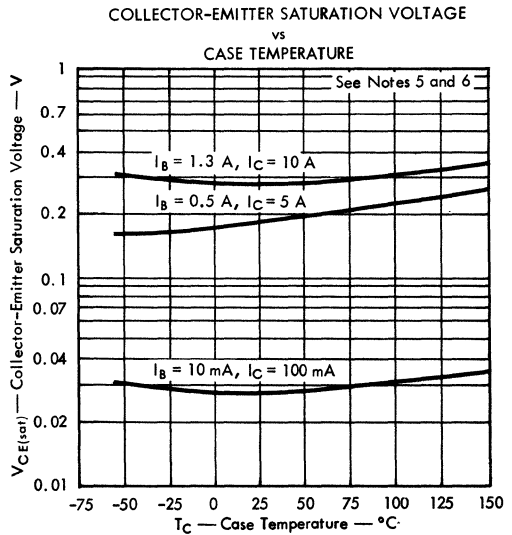


FIGURE 4

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPE 2N4301

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

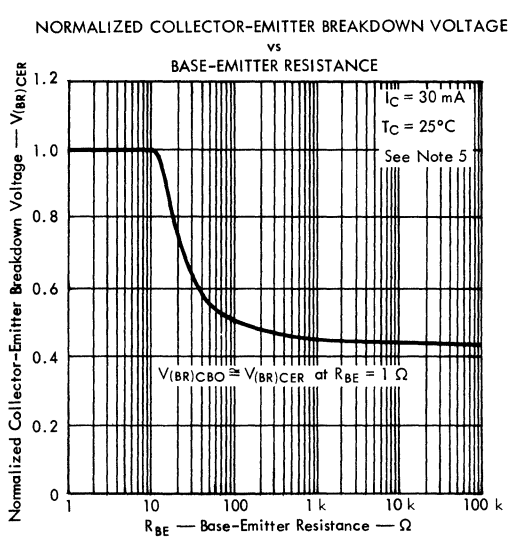


FIGURE 5

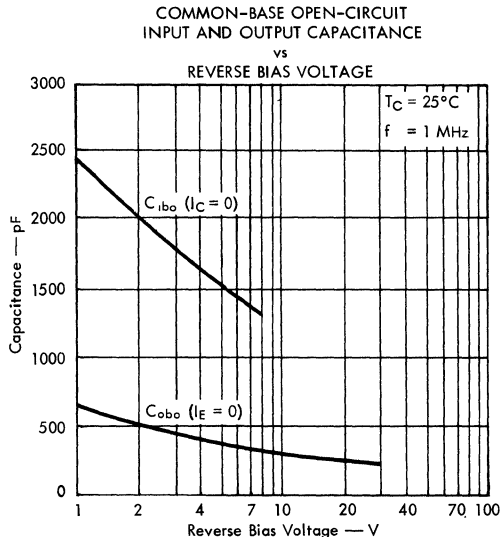


FIGURE 6

5

MAXIMUM SAFE OPERATING REGION

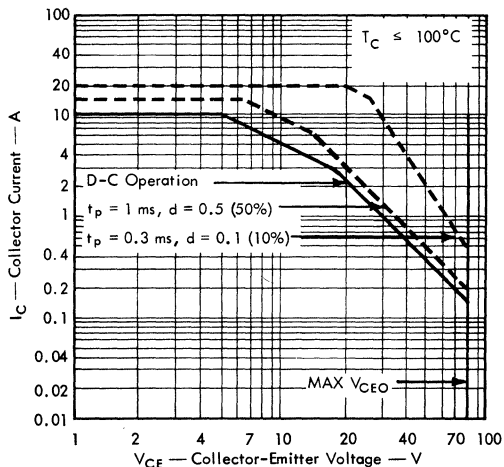


FIGURE 7

TYPE 2N4301

N-P-N EPITAXIAL PLANAR SILICON POWER TRANSISTOR

THERMAL INFORMATION

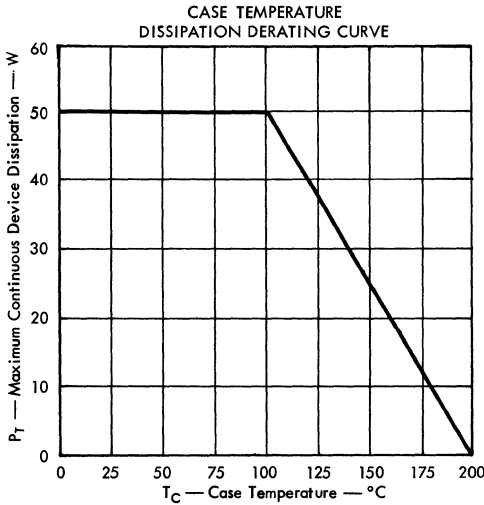


FIGURE 8

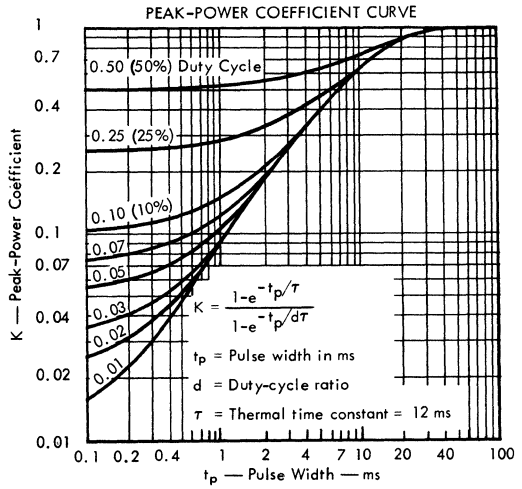


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	50	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	2	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	48	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 1.3 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d \theta_{C-A} + K \theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.101 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(1.3) + 0.101(2)} = 450 \text{ W}$$

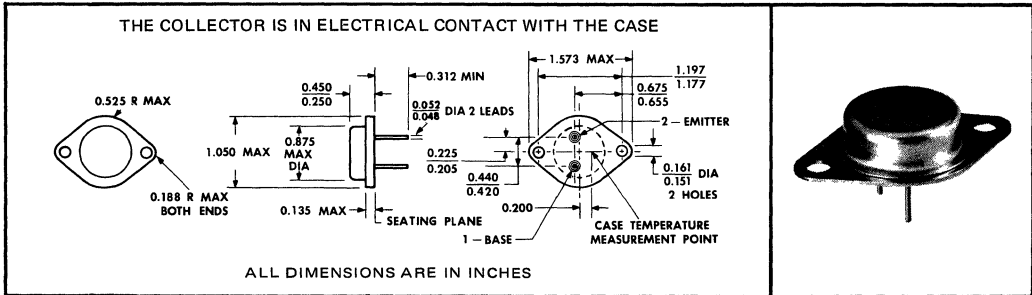
TYPES 2N4398, 2N4399 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5301, 2N5302

- 200 Watts at 25°C Case Temperature
- 30 A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 1 A

***mechanical data**

The case outline is the same as JEDEC TO-3 except for lead diameter.



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4398	2N4399
*Collector-Base Voltage	-40 V	-60 V
*Collector-Emitter Voltage (See Note 1)	-40 V	-60 V
*Collector-Emitter Voltage (See Note 2)	-40 V	-60 V
*Emitter-Base Voltage	← -5 V →	← -5 V →
*Continuous Collector Current	← -30 A →	← -30 A →
*Peak Collector Current (See Note 3)	← -50 A →	← -50 A →
*Continuous Base Current	← -7.5 A →	← -7.5 A →
*Peak Base Current (See Note 3)	← -15 A →	← -15 A →
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 2	
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 4)	← 200 W →	← 200 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 5)	← 5 W →	← 5 W →
*Operating Collector Junction Temperature Range	-65°C to 200°C	-65°C to 200°C
*Storage Temperature Range	-65°C to 200°C	-65°C to 200°C
*Lead Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →	← 235°C →

- NOTES: 1. These values apply when the base-emitter voltage $V_{BE} = 1.5$ V.
 2. These values apply when the base-emitter diode is open-circuited.
 3. This value applies for $t_D \leq 0.3$ ms, duty cycle $\leq 10\%$.
 4. Derate linearly to 200°C case temperature at the rate of 1.15 W/deg.
 5. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/deg.

*Indicates JEDEC registered data

TYPES 2N4398, 2N4399
BULLETIN NO. DL-S-6911059, JANUARY 1969

TYPES 2N4398, 2N4399

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4398		2N4399		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ mA}$, $I_B = 0$ See Note 6	-40		-60		V
I_{CBO} Collector Cutoff Current	$V_{CB} = -40 \text{ V}$, $I_E = 0$	-1				mA
	$V_{CB} = -60 \text{ V}$, $I_E = 0$			-1		
I_{CEO} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$			-5		mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$				-5	
I_{CEV} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 1.5 \text{ V}$			-5		mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 1.5 \text{ V}$				-5	
	$V_{CE} = -30 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ \text{C}$			-10	-10	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$			-5	-5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ V}$, $I_C = -1 \text{ A}$			40	40	
	$V_{CE} = -4 \text{ V}$, $I_C = -15 \text{ A}$			15	60	
	$V_{CE} = -4 \text{ V}$, $I_C = -30 \text{ A}$			5	5	
V_{BE} Base-Emitter Voltage	$I_B = -1.5 \text{ A}$, $I_C = -15 \text{ A}$			-1.85	-1.85	V
	$V_{CE} = -2 \text{ V}$, $I_C = -15 \text{ A}$			-1.7	-1.7	
	$V_{CE} = -4 \text{ V}$, $I_C = -30 \text{ A}$			-3	-3	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -1 \text{ A}$, $I_C = -10 \text{ A}$			-0.75	-0.75	V
	$I_B = -1.5 \text{ A}$, $I_C = -15 \text{ A}$			-1	-1	
	$I_B = -6 \text{ A}$, $I_C = -30 \text{ A}$			-4	-4	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$			40	40	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ MHz}$			4	4	

NOTES: 6. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	0.875	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	35	

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_r Rise Time	$I_C = -10 \text{ A}$, $I_{B(1)} = -1 \text{ A}$, $V_{BE(off)} = 2 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	0.4	μs
t_s Storage Time	$I_C = -10 \text{ A}$, $I_{B(1)} = -1 \text{ A}$, $I_{B(2)} = 1 \text{ A}$,	1.5	
t_f Fall Time	$R_L = 3 \Omega$, See Figure 2	0.6	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

* Indicates JEDEC registered data

TYPES 2N4398, 2N4399 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*PARAMETER MEASUREMENT INFORMATION

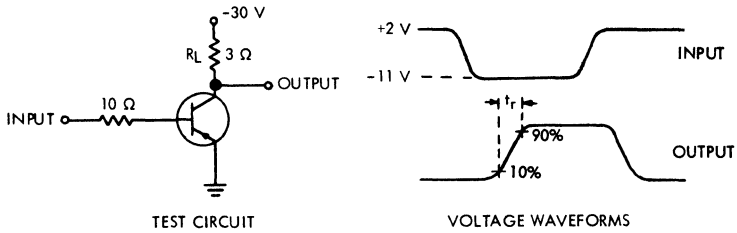


FIGURE 1 — RISE TIME

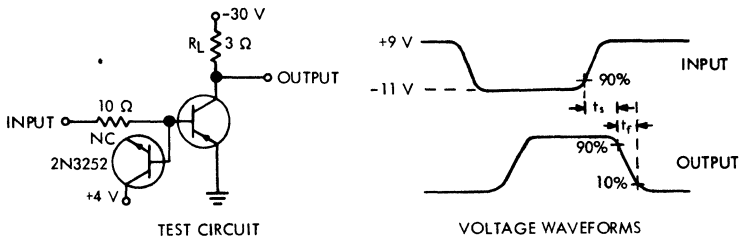


FIGURE 2 — STORAGE AND FALL TIMES

- NOTES:**
- a. The input waveforms have the following characteristics: $t_r \leq 20$ ns, $t_f \leq 20$ ns, $t_p = 10$ μ s to 100 μ s, duty cycle $\leq 2\%$.
 - b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 20$ ns, $R_{in} \geq 10$ k Ω , $C_{in} \leq 11.5$ pF.
 - c. Resistors must be noninductive types.
 - d. The d-c power supplies may require additional bypassing in order to minimize ringing.

*Indicates JEDEC registered data

MAXIMUM SAFE OPERATING REGION

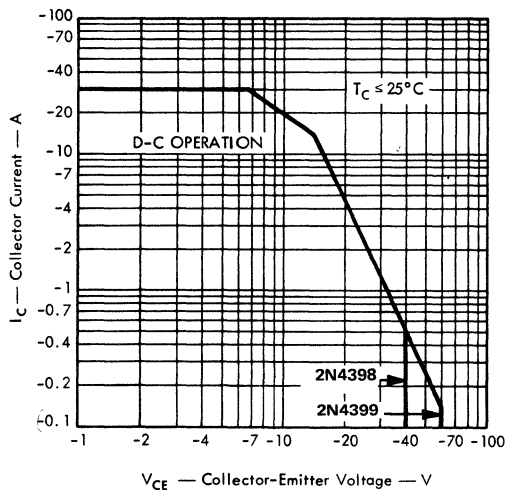


FIGURE 3

TYPES 2N4398, 2N4399

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

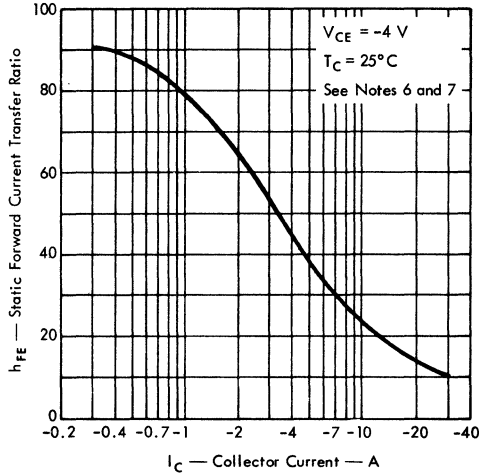


FIGURE 4

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

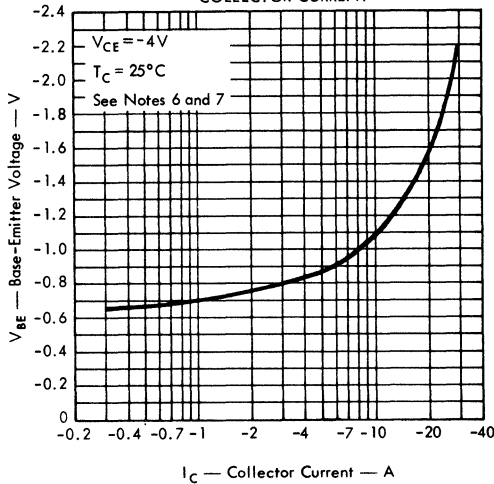


FIGURE 5

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

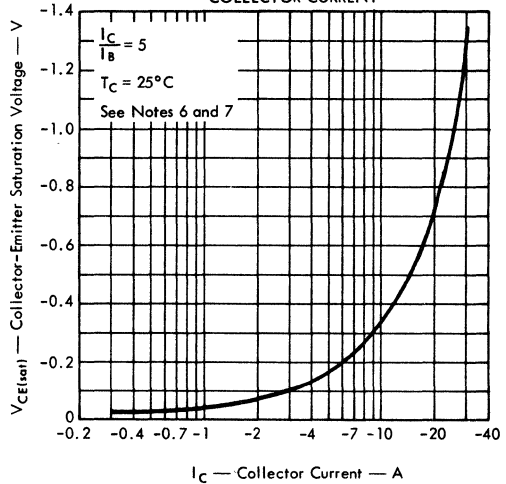


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

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169

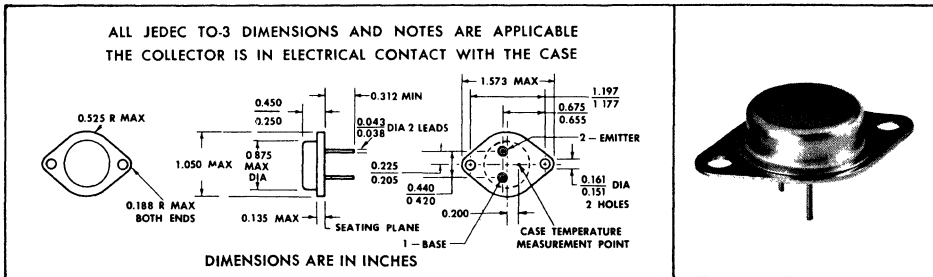
TYPES 2N4901, 2N4902, 2N4903 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND SWITCHING APPLICATIONS

- 87.5 W at 25°C Case Temperature
- 5 A Rated Collector Current
- Min f_T of 4 MHz at 10 V, 1 A

TYPES 2N4901, 2N4902, 2N4903
BULLETIN NO. DLS-6810048, NOVEMBER 1968

***mechanical data**



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4901	2N4902	2N4903
*Collector-Base Voltage	-40 V	-60 V	-80 V
*Collector-Emitter Voltage (See Note 1)	-40 V	-60 V	-80 V
*Emitter-Base Voltage	-5 V	-5 V	-5 V
*Continuous Collector Current	←	-5 A	→
Peak Collector Current (See Note 2)	←	-15 A	→
*Continuous Base Current	←	-1 A	→
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 2 →		
*Continuous Device Dissipation at (or below) 25°C	← 87.5 W →		
Case Temperature (See Note 3)	← 87.5 W →		
Free-Air Temperature (See Note 4)	← 4 W →		
*Operating Collector Junction Temperature Range	← -65°C to 200°C →		
*Storage Temperature Range	← -65°C to 200°C →		
*Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

TYPES 2N4901, 2N4902, 2N4903

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4901	2N4902	2N4903	UNIT
		MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ mA}, I_B = 0$, See Note 5	-40	-60	-80	V
I_{CEO} Collector Cutoff Current	$V_{CE} = -40 \text{ V}, I_B = 0$	-1			mA
	$V_{CE} = -60 \text{ V}, I_B = 0$		-1		
	$V_{CE} = -80 \text{ V}, I_B = 0$			-1	
I_{CEV} Collector Cutoff Current	$V_{CE} = -40 \text{ V}, V_{BE} = 1.5 \text{ V}$	-0.1			mA
	$V_{CE} = -60 \text{ V}, V_{BE} = 1.5 \text{ V}$		-0.1		
	$V_{CE} = -80 \text{ V}, V_{BE} = 1.5 \text{ V}$			-0.1	
	$V_{CE} = -40 \text{ V}, V_{BE} = 1.5 \text{ V}, T_C = 150^\circ\text{C}$	-2			
	$V_{CE} = -60 \text{ V}, V_{BE} = 1.5 \text{ V}, T_C = 150^\circ\text{C}$		-2		
	$V_{CE} = -80 \text{ V}, V_{BE} = 1.5 \text{ V}, T_C = 150^\circ\text{C}$			-2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}, I_C = 0$	-1	-1	-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ V}, I_C = -1 \text{ A}$, See Notes 5 and 6	20 80	20 80	20 80	
	$V_{CE} = -2 \text{ V}, I_C = -5 \text{ A}$, See Notes 5 and 6	7	7	7	
V_{BE} Base-Emitter Voltage	$V_{CE} = -2 \text{ V}, I_C = -1 \text{ A}$, See Notes 5 and 6	-1.2	-1.2	-1.2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.1 \text{ A}, I_C = -1 \text{ A}$, See Notes 5 and 6	-0.4	-0.4	-0.4	V
	$I_B = -1 \text{ A}, I_C = -5 \text{ A}$, See Notes 5 and 6	-1.5	-1.5	-1.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}, I_C = -0.5 \text{ A}, f = 1 \text{ kHz}$	20	20	20	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}, I_C = -1 \text{ A}, f = 1 \text{ MHz}$	4	4	4	

NOTES: 5. These parameters must be measured using pulse techniques: $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*Indicates JEDEC registered data

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	2	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	43.7	

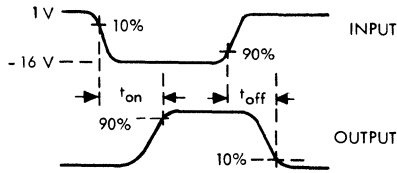
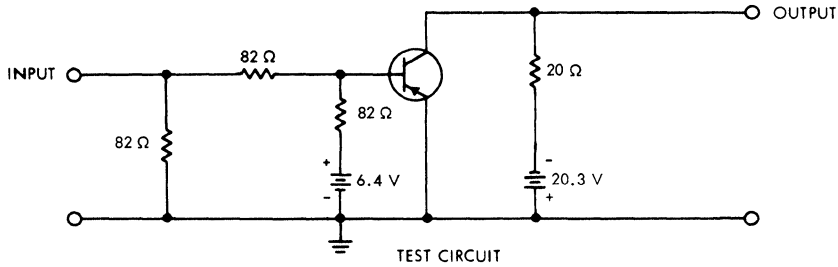
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -1 \text{ A}, I_{B(1)} = -0.1 \text{ A}, I_{B(2)} = 0.1 \text{ A}$,	0.35	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 3.7 \text{ V}, R_L = 20 \Omega$, See Figure 1	0.8	

†Voltage and current values shown are nominal; exact values vary slightly with device parameters.

TYPES 2N4901, 2N4902, 2N4903 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50 \Omega$, $t_p = 10 \mu s$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10 M\Omega$, $C_{in} \leq 11.5$ pF.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

MAXIMUM SAFE OPERATING REGION

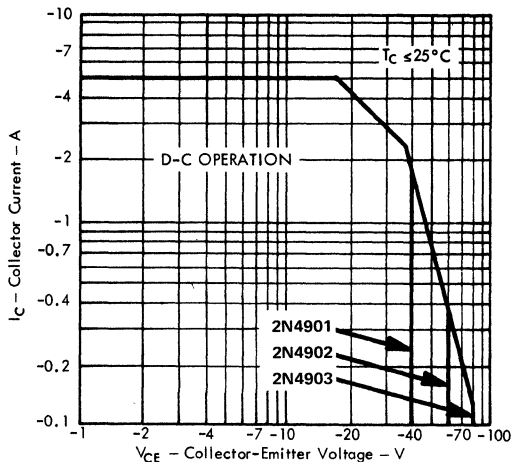
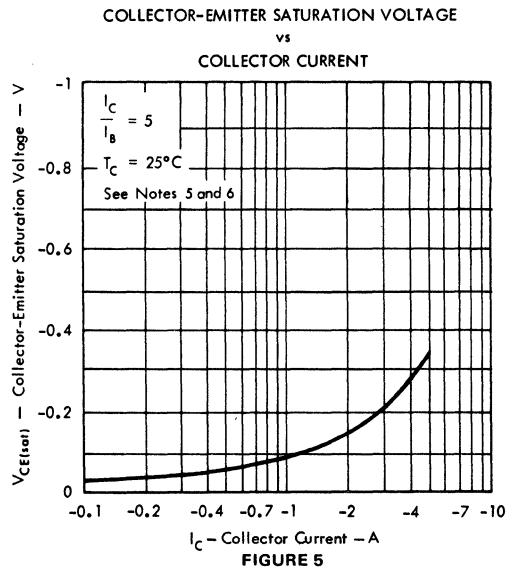
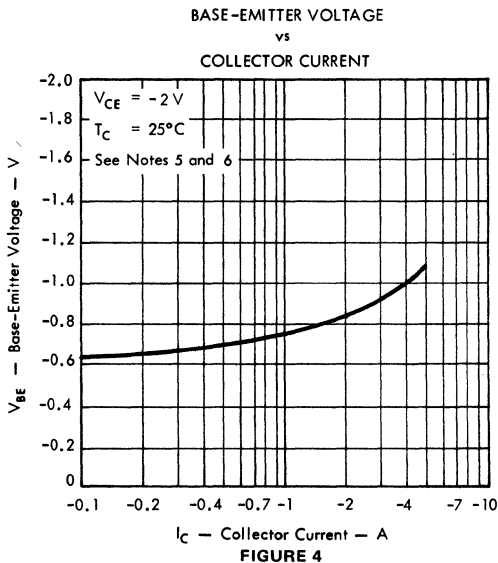
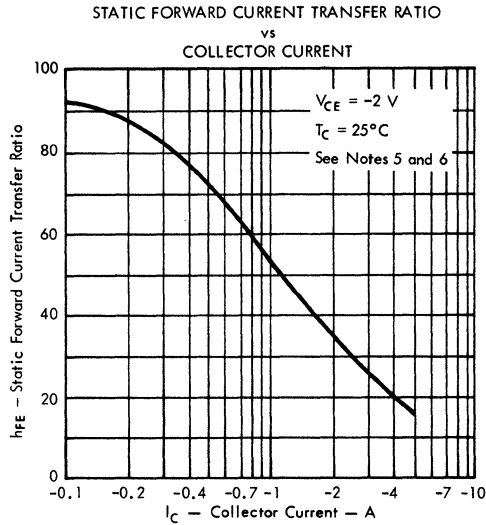


FIGURE 2

TYPES 2N4901, 2N4902, 2N4903

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS



NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

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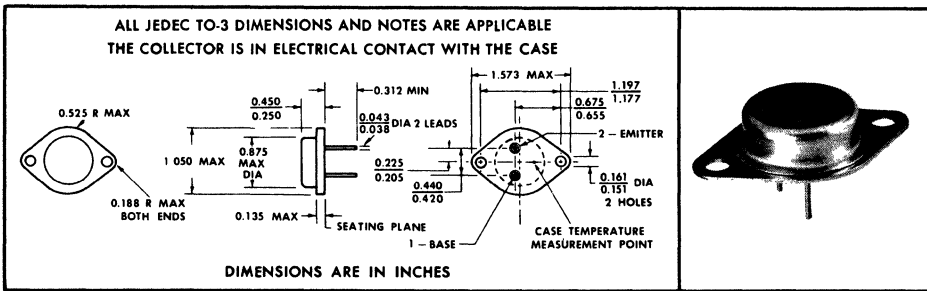
TYPES 2N4904, 2N4905, 2N4906 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPES 2N4904, 2N4905, 2N4906
BULLETIN NO. D.L.S. 6810049, NOVEMBER 1968

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N4913, 2N4914, 2N4915**

- 87.5 W at 25°C Case Temperature
- 5 A Rated Collector Current
- Min f_T of 4 MHz at 10 V, 500 mA

***mechanical data**



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4904	2N4905	2N4906
*Collector-Base Voltage	-40 V	-60 V	-80 V
*Collector-Emitter Voltage (See Note 1)	-40 V	-80 V	-80 V
*Emitter-Base Voltage	← -5 V →		→
*Continuous Collector Current	← -5 A →		→
Peak Collector Current (See Note 2)	← -15 A →		→
*Continuous Base Current	← -1 A →		→
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 2 →		
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 87.5 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →		
*Operating Collector Junction Temperature Range	← -65°C to 200°C →		
*Storage Temperature Range	← -65°C to 200°C →		
*Lead Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →		

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

TYPES 2N4904, 2N4905, 2N4906

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4904	2N4905	2N4906	UNIT
		MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ mA}$, $I_B = 0$, See Note 5	-40	-60	-80	V
I_{CEO} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$	-1			mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$	-1			
	$V_{CE} = -80 \text{ V}$, $I_B = 0$	-1			
I_{CEV} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 1.5 \text{ V}$	-0.1			mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 1.5 \text{ V}$	-0.1			
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 1.5 \text{ V}$	-0.1			
	$V_{CE} = -40 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	-2			
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	-2			
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	-2			
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1	-1	-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ V}$, $I_C = -2.5 \text{ A}$, See Notes 5 and 6	25 100	25 100	25 100	
	$V_{CE} = -2 \text{ V}$, $I_C = -5 \text{ A}$, See Notes 5 and 6	7	7	7	
V_{BE} Base-Emitter Voltage	$V_{CE} = -2 \text{ V}$, $I_C = -2.5 \text{ A}$, See Notes 5 and 6	-1.4	-1.4	-1.4	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.25 \text{ A}$, $I_C = -2.5 \text{ A}$, See Notes 5 and 6	-1	-1	-1	V
	$I_B = -1 \text{ A}$, $I_C = -5 \text{ A}$, See Notes 5 and 6	-1.5	-1.5	-1.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ kHz}$	40	40	40	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ MHz}$	4	4	4	

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

* Indicates JEDEC registered data

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	2	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	43.7	

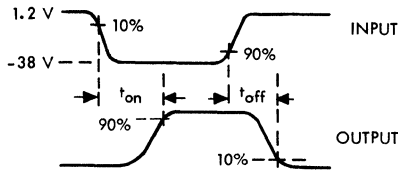
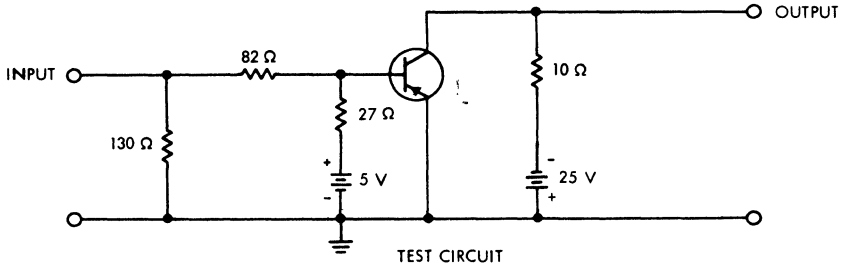
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -2.5 \text{ A}$, $I_{B(1)} = -250 \text{ mA}$, $I_{B(2)} = 250 \text{ mA}$, $V_{BE(off)} = 4.1 \text{ V}$, $R_L = 10 \Omega$, See Figure 1	0.4	μs
t_{off} Turn-Off Time		0.7	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES 2N4904, 2N4905, 2N4906 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50 \Omega$, $t_p = 10 \mu s$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

MAXIMUM SAFE OPERATING REGION

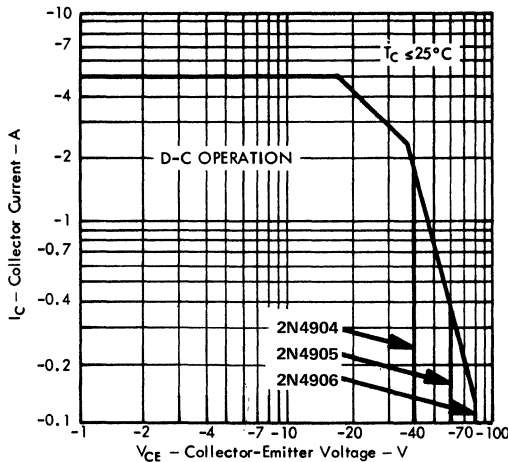
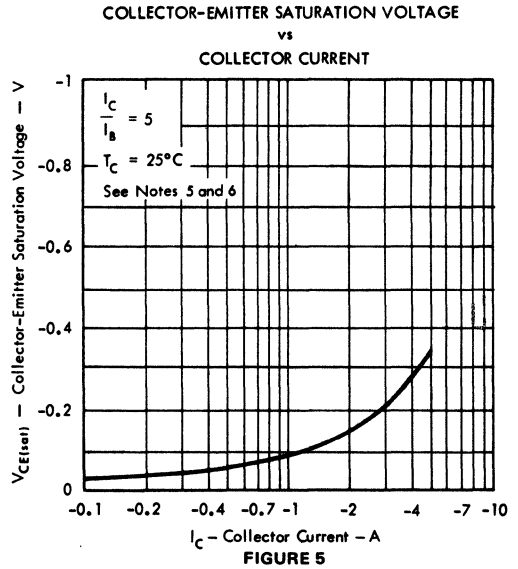
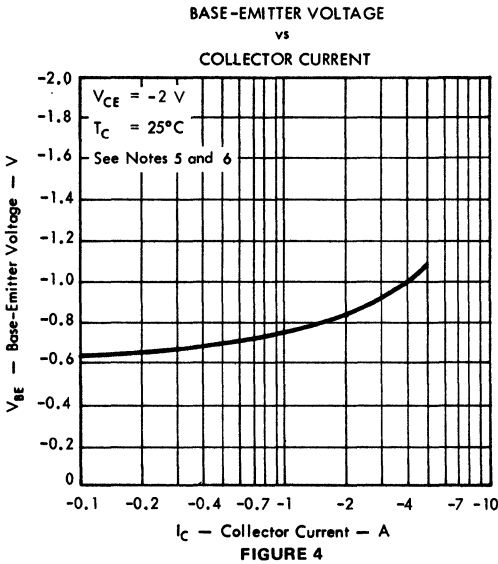
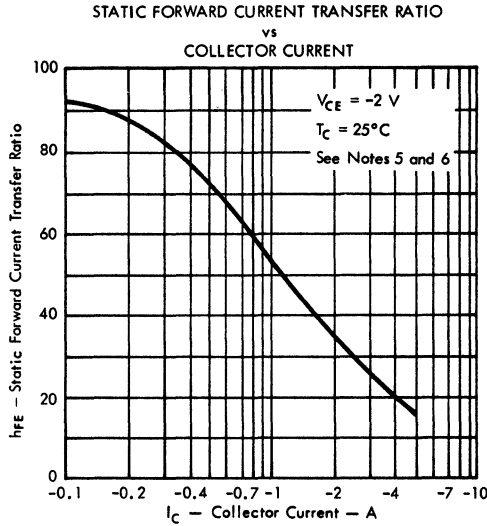


FIGURE 2

TYPES 2N4904, 2N4905, 2N4906

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS



NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

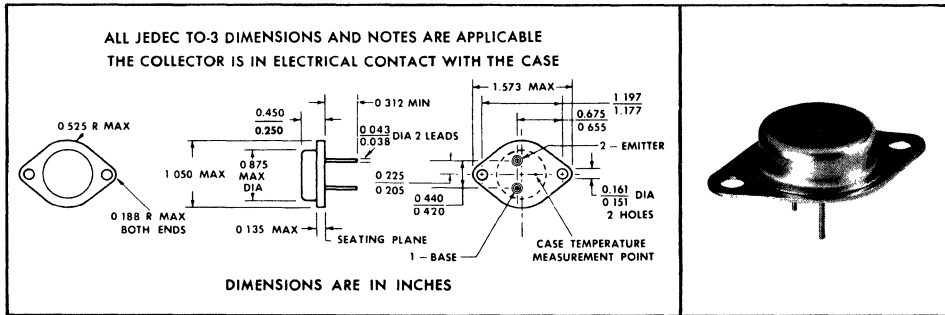
TYPES 2N4913, 2N4914, 2N4915 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPES 2N4913, 2N4914, 2N4915
BULLETIN NO. DL-5 681 0999, NOVEMBER 1968

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N4904 THRU 2N4906**

- 87.5 W at 25°C Case Temperature
- 5 A Rated Collector Current
- Min f_T of 4 MHz at 10 V, 1 A

***mechanical data**



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4913	2N4914	2N4915
*Collector-Base Voltage	40 V	60 V	80 V
*Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V
*Emitter-Base Voltage	←	5 V	→
*Continuous Collector Current	←	5 A	→
Peak Collector Current (See Note 2)	←	15 A	→
*Continuous Base Current	←	1 A	→
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 6 →		
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 87.5 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →		
*Operating Collector Junction Temperature Range	← -65°C to 200°C →		
*Storage Temperature Range	← -65°C to 200°C →		
*Lead Temperature 1/8 Inch from Case for 10 Seconds	← 235°C →		

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p = 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/deg.

*Indicates JEDEC registered data

TYPES 2N4913, 2N4914, 2N4915

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4913		2N4914		2N4915		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 5	40		60		80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$	1						mA
	$V_{CE} = 60 \text{ V}$, $I_B = 0$			1				
	$V_{CE} = 80 \text{ V}$, $I_B = 0$					1		
I_{CEV} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	0.1						mA
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			0.1				
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$					0.1		
	$V_{CE} = 40 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	2						
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$			2				
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$					2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1		1		1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6	25	100	25	100	25	100	
	$V_{CE} = 2 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 5 and 6	7		7		7		
V_{BE} Base-Emitter Voltage	$V_{CE} = 2 \text{ V}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6	1.4		1.4		1.4		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.25 \text{ A}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6	0.75		0.75		0.75		V
	$I_B = 1 \text{ A}$, $I_C = 5 \text{ A}$, See Notes 5 and 6	1.5		1.5		1.5		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		
h_{fo} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ MHz}$	4		4		4		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	2	deg/W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	43.7	

*Indicates JEDEC registered data

TYPES 2N4913, 2N4914, 2N4915

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 2.5 \text{ A}$, $I_{B(1)} = 250 \text{ mA}$, $I_{B(2)} = -250 \text{ mA}$	0.6	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -4.1 \text{ V}$, $R_L = 10 \Omega$, See Figure 1	1.2	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

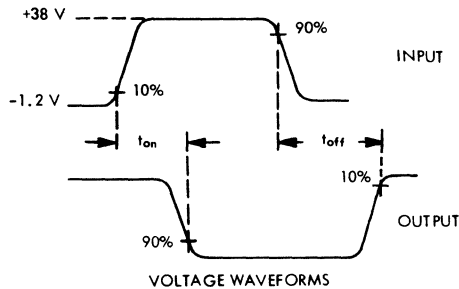
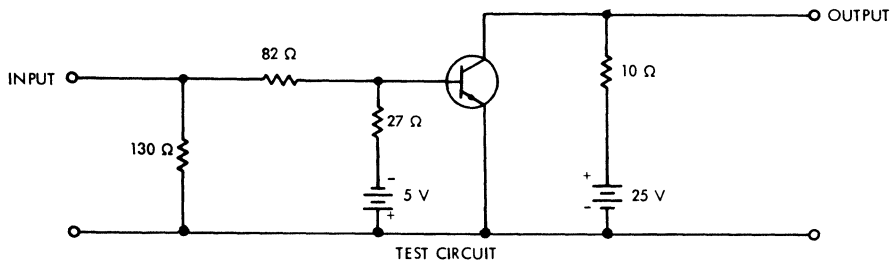


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPES 2N4913, 2N4914, 2N4915

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

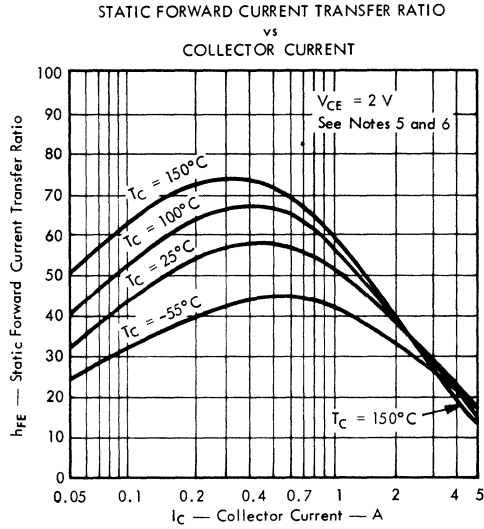


FIGURE 2

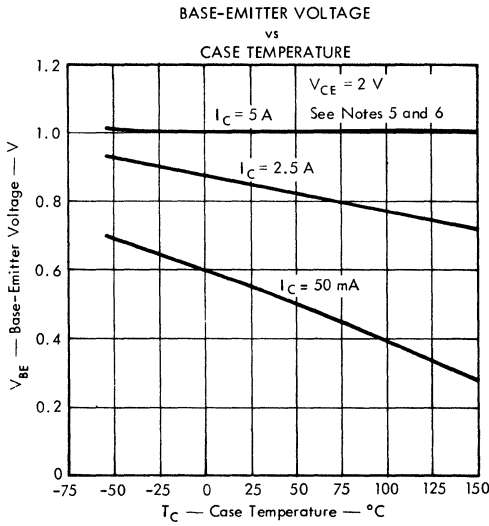


FIGURE 3

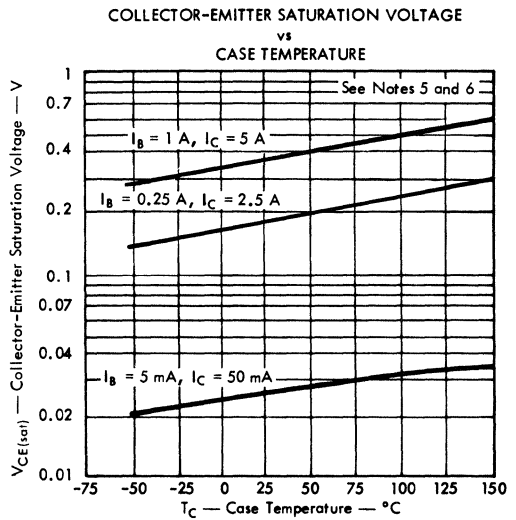


FIGURE 4

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N4913, 2N4914, 2N4915 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

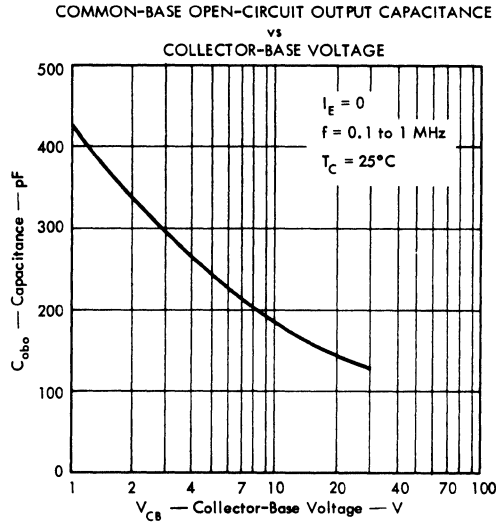


FIGURE 5

MAXIMUM SAFE OPERATING REGION

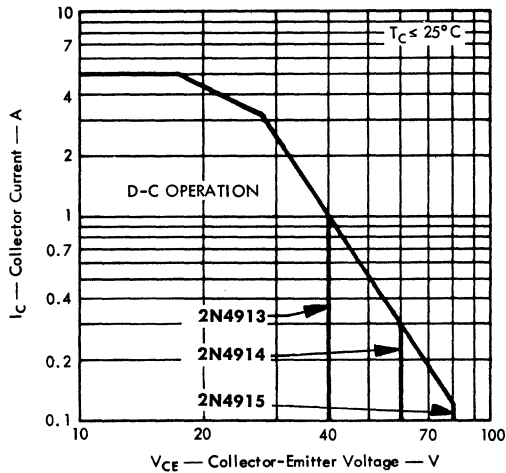


FIGURE 6

5

TYPES 2N4913, 2N4914, 2N4915

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

THERMAL INFORMATION

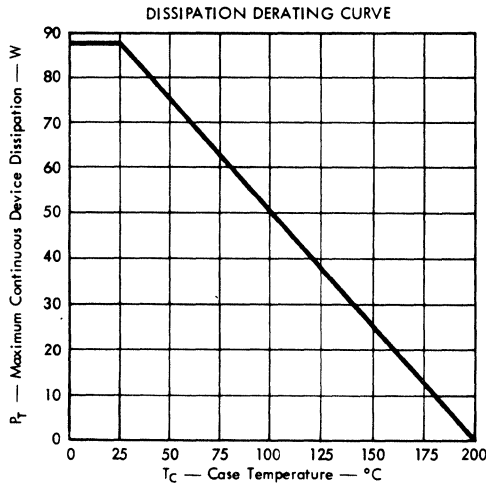


FIGURE 7

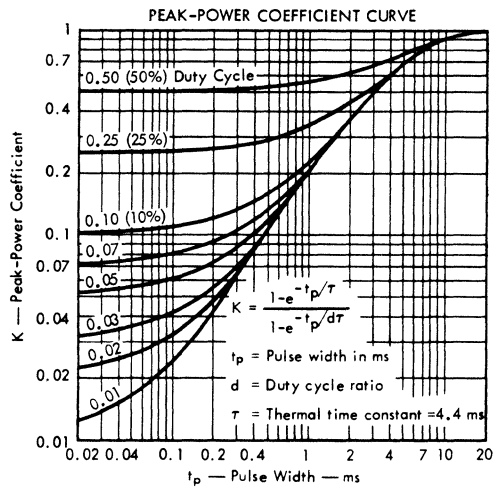


FIGURE 8

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	43.7	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	2	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	41.7	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 8	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C-HS} + \theta_{HS-A} = 2.25$ deg/W (From information supplied with heat sink.)

$T_{J(av)}$ (design limit) = 200°C

$T_A = 50^\circ\text{C}$

d = 10% (0.1)

$t_p = 0.1$ ms

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C}, \text{ as in figure 7.}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From figure 8, Peak-Power Coefficient

$$K = 0.11 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(2.25) + 0.11(2)} = 337 \text{ W}$$

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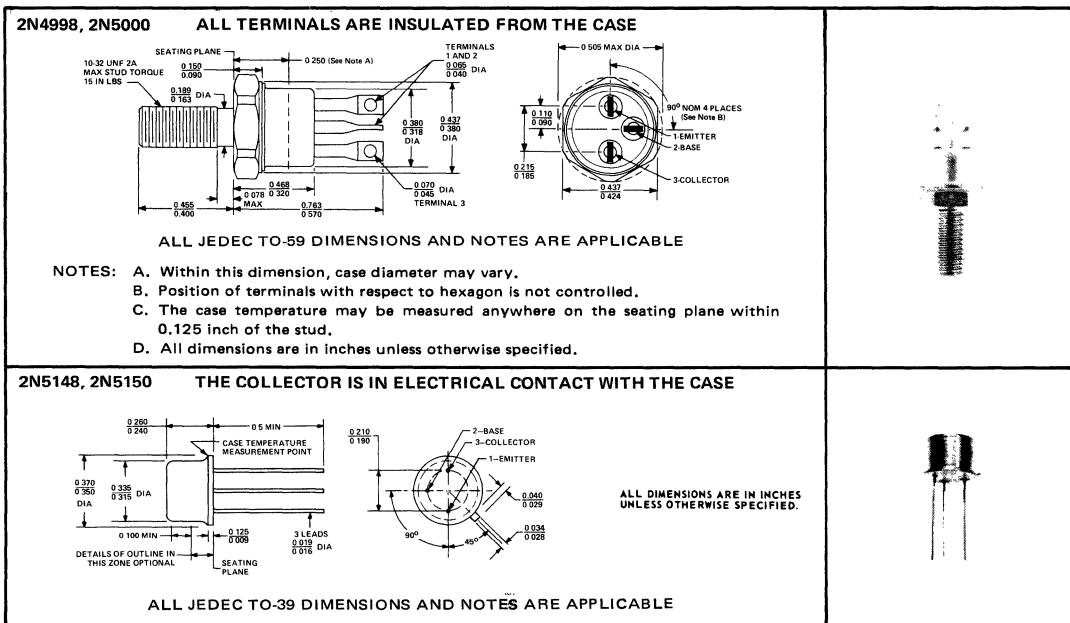
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TYPES 2N4998, 2N5000, 2N5148, 2N5150 N-P-N SILICON POWER TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- For Complementary Use With 2N4999, 2N5001, 2N5147, and 2N5149
- 6 mJ Reverse Energy Rating with $I_C = 5$ A and 4 V Reverse Bias

*mechanical data



TYPES 2N4998, 2N5000, 2N5148, 2N5150
BULLETIN NO. DL-S-711497, JUNE 1971
REVISED NOVEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4998	2N5148	2N5000	2N5150
Collector-Base Voltage	← 100 V* →			
Collector-Emitter Voltage (See Note 1)	← 80 V* →			
Emitter-Base Voltage	← 6 V* →			
Continuous Collector Current	2 A*	2 A*		
Peak Collector Current (See Note 2)	5 A*	5 A*		
Continuous Base Current	1 A*	1 A*		
Safe Operating Areas	See Figures 7* and 8			
Continuous Device Dissipation at 50°C Case Temperature (See Note 3)	30 W*	6 W*		
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	20 W	4 W		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W	1 W*		
Unclamped Inductive Load Energy (See Note 5)	← 6 mJ →			
Operating Collector Junction Temperature Range	-65°C to 200°C*			
Storage Temperature Range	-65°C to 200°C*			
Lead or Terminal Temperature 1/8 Inch from Case for 60 Seconds	← 300°C* →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_W \leq 8.3$ ms, duty cycle $\leq 1\%$.
3. For operation above (or below) 50°C case temperature, refer to Dissipation Derating Curves Figures 9 and 10.
4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C for 2N4998 and 2N5000, 5.7 mW/°C for 2N5148 and 2N5150.
5. This rating is based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*†. $L = 0.48$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 4$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = 5$ A, Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

†This circuit appears on page 5-1 of this data book.

TYPES 2N4998, 2N5000, 2N5148, 2N5150

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4998		2N5000		UNIT
		2N5148		2N5150		
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 100 \text{ mA}$, $I_B = 0$, See Note 6	80		80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$	50		50		μA
I_{CES} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$	1		1		μA
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$	1		1		mA
I_{CEV} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = -2 \text{ V}$, $T_C = 150^\circ\text{C}$	500		500		μA
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1		1		μA
	$V_{EB} = 6 \text{ V}$, $I_C = 0$	1		1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 50 \text{ mA}$	20		50		
	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$	30	90	70	200	
	$V_{CE} = 5 \text{ V}$, $I_C = 2 \text{ A}$	15		30		
	$V_{CE} = 5 \text{ V}$, $I_C = 3 \text{ A}$	5		15		
	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $T_C = -55^\circ\text{C}$	15		35		
V_{BE} Base-Emitter Voltage	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$		1.2		1.2	V
	$I_B = 200 \text{ mA}$, $I_C = 2 \text{ A}$		1.5		1.5	
	$V_{CE} = 5 \text{ V}$, $I_C = 2 \text{ A}$		1.5		1.5	
	$V_{CE} = 5 \text{ V}$, $I_C = 3 \text{ A}$		3		3	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$		0.46		0.46	V
	$I_B = 200 \text{ mA}$, $I_C = 2 \text{ A}$		0.85		0.85	
	$I_B = 600 \text{ mA}$, $I_C = 3 \text{ A}$		5		5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.1 \text{ A}$, $f = 1 \text{ kHz}$	20		50		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 20 \text{ MHz}$	2.5		3		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	70		70		pF

NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 1\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

thermal characteristics

PARAMETER		2N4998		2N5148		UNIT
		2N5000		2N5150		
		MAX	MAX	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance		5		25		$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance		87.5		175		

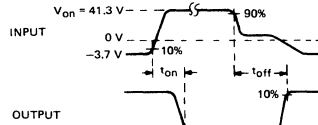
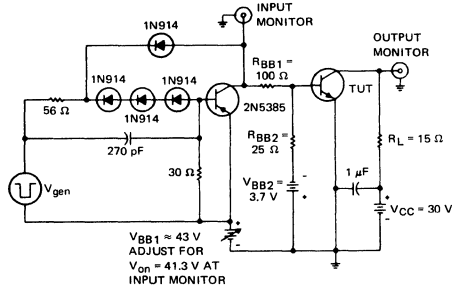
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	ALL TYPES		UNIT
		TYP		
t_{on} Turn-On Time	$I_C = 2 \text{ A}$, $I_B(1) = 200 \text{ mA}$, $I_B(2) = -200 \text{ mA}$,	0.1		μs
t_{off} Turn-Off Time	$V_{BE(off)} = -3.7 \text{ V}$, $R_L = 15 \Omega$, See Figure 1	1.1		

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES 2N4998, 2N5000, 2N5148, 2N5150 N-P-N SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPICAL CHARACTERISTICS

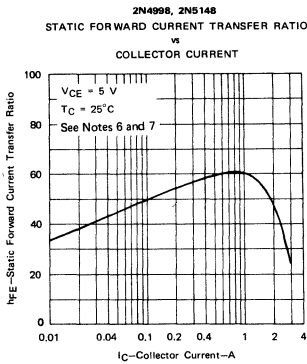


FIGURE 2

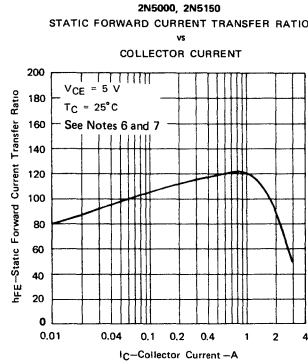


FIGURE 3

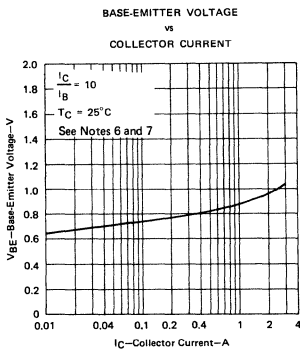


FIGURE 4

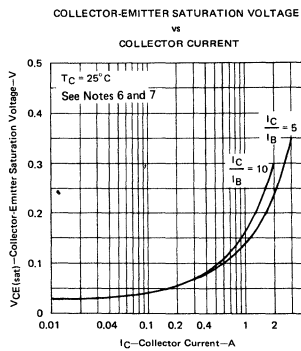


FIGURE 5

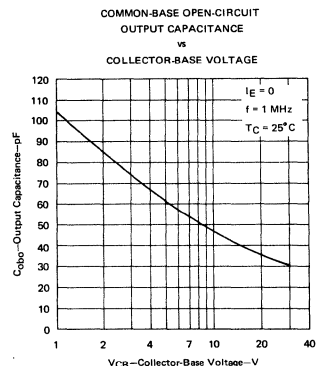


FIGURE 6

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 1\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N4998, 2N5000, 2N5148, 2N5150 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

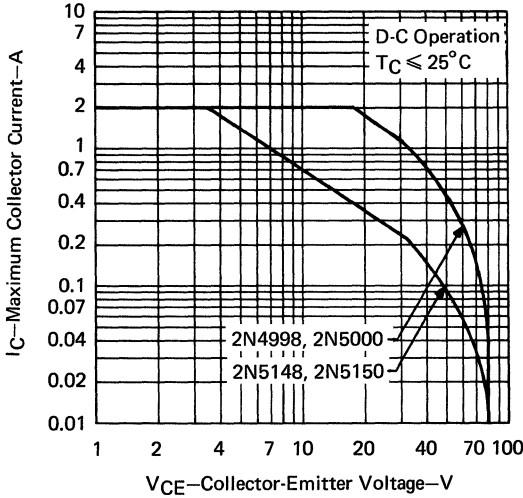


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

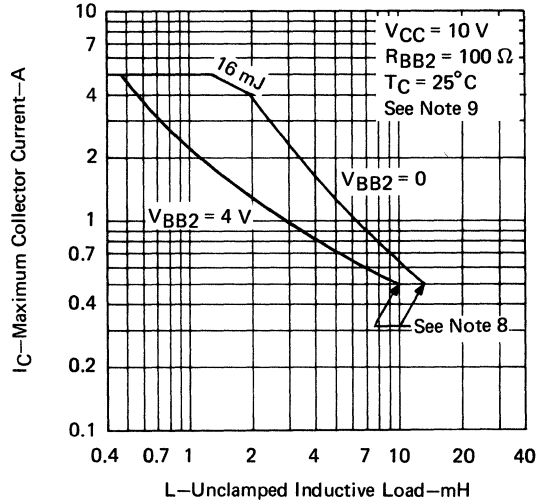


FIGURE 8

NOTES: 8. Above these points the safe operating areas have not been defined.

9. These curves are based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $R_{BB1} = 10 \cdot V_{BB1} / I_C$, $V_{BB1} = 10 \text{ V}$, $R_L = 0.1 \Omega$. Energy $\approx I_C^2 L / 2$.

[†]This circuit appears on page 5-1 of this data book.

THERMAL CHARACTERISTICS

2N4998, 2N5000
DISSIPATION DERATING CURVE

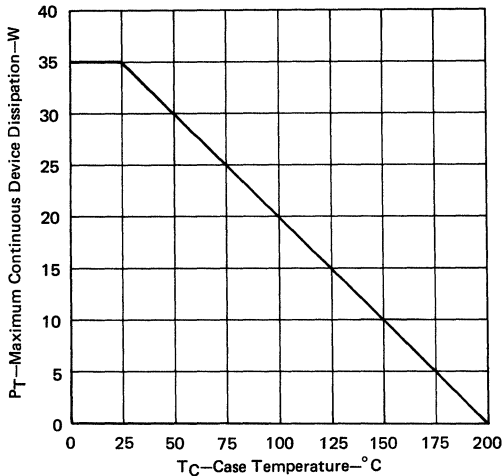


FIGURE 9

2N5148, 2N5150
DISSIPATION DERATING CURVE

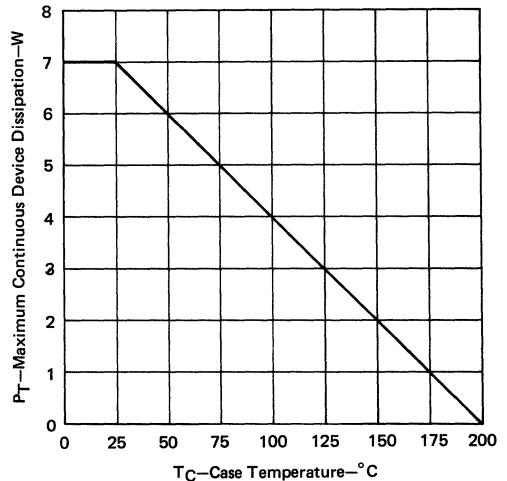


FIGURE 10

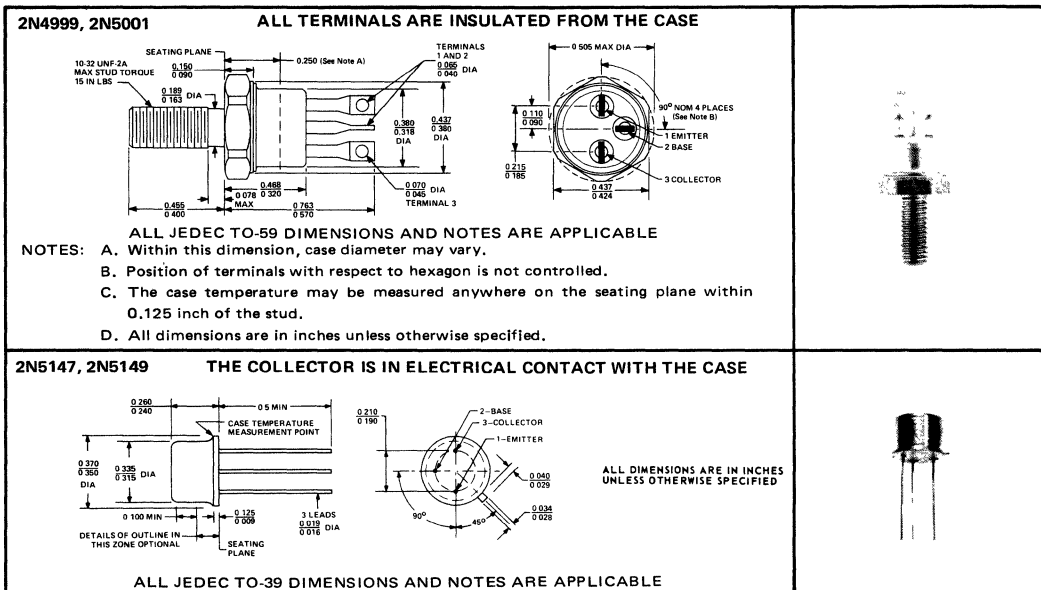
TYPES 2N4999, 2N5001, 2N5147, 2N5149 P-N-P SILICON POWER TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- For Complementary Use With 2N4998, 2N5000, 2N5148, and 2N5150
- 6 mJ Reverse Energy Rating with $I_C = 5$ A and 4 V Reverse Bias

*mechanical data

TYPES 2N4999, 2N5001, 2N5147, 2N5149
BULLETIN NO. DL-S-711493, SEPTEMBER 1971
REVISED NOVEMBER 1971



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N4999	2N5147	2N5001	2N5149
Collector-Base Voltage	← -100 V* →			
Collector-Emitter Voltage (See Note 1)	← -80 V* →			
Emitter-Base Voltage	← -5.5 V* →			
Continuous Collector Current	-2 A*	-2 A*		
Peak Collector Current (See Note 2)	-5 A*	-5 A*		
Continuous Base Current	-1 A*	-1 A*		
Safe Operating Areas	See Figures 7* and 8			
Continuous Device Dissipation at 50°C Case Temperature (See Note 3)	30 W*	6 W*		
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	20 W	4 W		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W	1 W*		
Unclamped Inductive Load Energy (See Note 5)	← 6 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 200°C* →			
Storage Temperature Range	← -65°C to 200°C* →			
Lead or Terminal Temperature 1/8 Inch from Case for 60 Seconds	← 300°C* →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 8.3$ ms, duty cycle $\leq 1\%$.
 3. For operation above (or below) 50°C case temperature, refer to Dissipation Derating Curves Figures 9 and 10.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C for 2N4999 and 2N5001, 5.7 mW/°C for 2N5147 and 2N5149.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*[†]. $L = 0.48$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 4$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = 5$ A. Energy $\approx I_C^2 L/2$.

* JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

[†] This circuit appears on page 5-1 of this data book.

TYPES 2N4999, 2N5001, 2N5147, 2N5149

P-N-P SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N4999	2N5001	UNIT
		2N5147	2N5149	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -100 \text{ mA}$, $I_B = 0$, See Note 6	-80	-80	V
I_{CEO} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$	-50	-50	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$ $V_{CE} = -100 \text{ V}$, $V_{BE} = 0$	-1	-1	μA
I_{CEV} Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 2 \text{ V}$, $T_C = 150^\circ\text{C}$	-500	-500	μA
I_{EBO} Emitter Cutoff Current	$V_{EB} = -4 \text{ V}$, $I_C = 0$	-1	-1	μA
	$V_{EB} = -5.5 \text{ V}$, $I_C = 0$	-1	-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -50 \text{ mA}$	20	50	
	$V_{CE} = -5 \text{ V}$, $I_C = -1 \text{ A}$	30	90	
	$V_{CE} = -5 \text{ V}$, $I_C = -2 \text{ A}$	15	30	
	$V_{CE} = -5 \text{ V}$, $I_C = -3 \text{ A}$	5	15	
	$V_{CE} = -5 \text{ V}$, $I_C = -1 \text{ A}$, $T_C = -55^\circ\text{C}$	15	35	
V_{BE} Base-Emitter Voltage	$I_B = -100 \text{ mA}$, $I_C = -1 \text{ A}$	-1.2	-1.2	V
	$I_B = -200 \text{ mA}$, $I_C = -2 \text{ A}$	-1.5	-1.5	
	$V_{CE} = -5 \text{ V}$, $I_C = -2 \text{ A}$	-1.5	-1.5	
	$V_{CE} = -5 \text{ V}$, $I_C = -3 \text{ A}$	-3	-3	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -100 \text{ mA}$, $I_C = -1 \text{ A}$	-0.46	-0.46	V
	$I_B = -200 \text{ mA}$, $I_C = -2 \text{ A}$	-0.85	-0.85	
	$I_B = -600 \text{ mA}$, $I_C = -3 \text{ A}$	-5	-5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.1 \text{ A}$, $f = 1 \text{ kHz}$	20	50	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 20 \text{ MHz}$	2.5	3	
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	120	120	pF

NOTES: 6. This parameter must be measured using pulse techniques: $t_w = 300 \mu\text{s}$, duty cycle $\leq 1\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

thermal characteristics

PARAMETER		2N4999	2N5147	UNIT
		2N5001	2N5149	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance		5	25	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance		87.5	175	

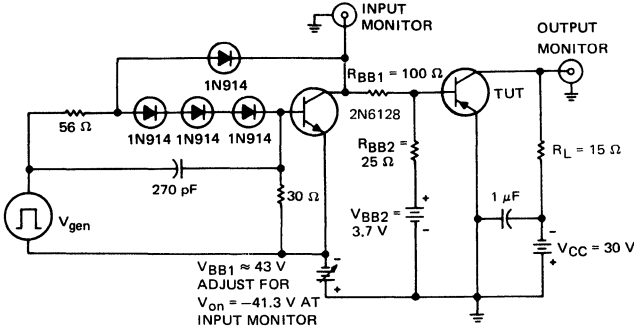
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	ALL TYPES	UNIT
		TYP	
t_{on} Turn-On Time	$I_C = -2 \text{ A}$, $I_B(1) = -200 \text{ mA}$, $I_B(2) = 200 \text{ mA}$, $V_{BE(off)} = 3.7 \text{ V}$, $R_L = 15 \Omega$, See Figure 1	0.2	μs
t_{off} Turn-Off Time		0.4	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

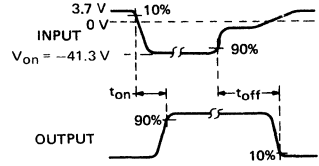
TYPES 2N4999, 2N5001, 2N5147, 2N5149 P-N-P SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50 \Omega$, $t_w = 20 \mu s$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.



VOLTAGE WAVEFORMS

FIGURE 1

TYPICAL CHARACTERISTICS

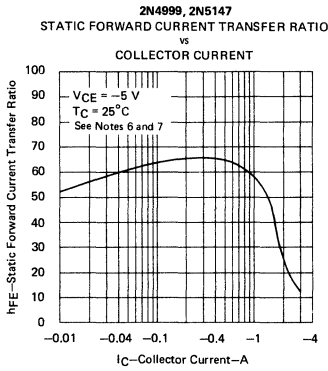


FIGURE 2

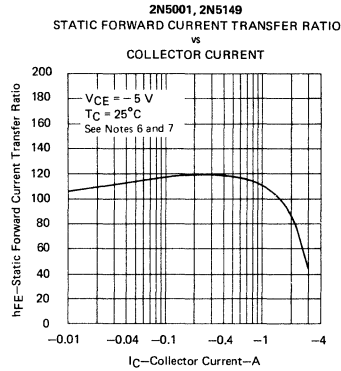


FIGURE 3

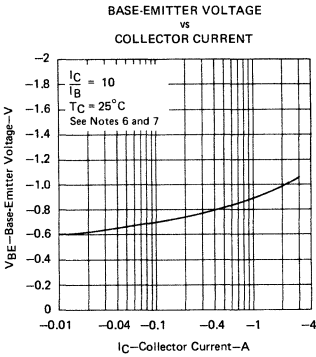


FIGURE 4

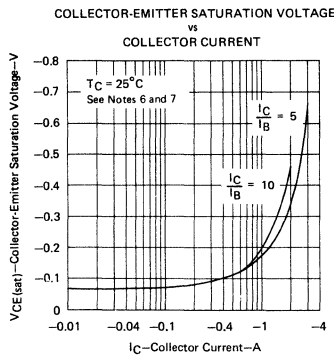


FIGURE 5

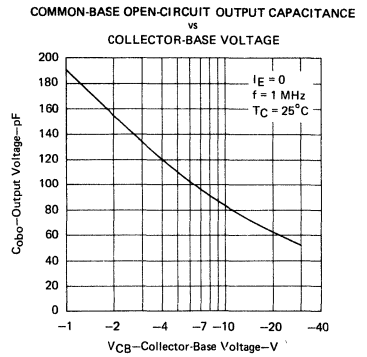


FIGURE 6

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 1\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N4999, 2N5001, 2N5147, 2N5149

P-N-P SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

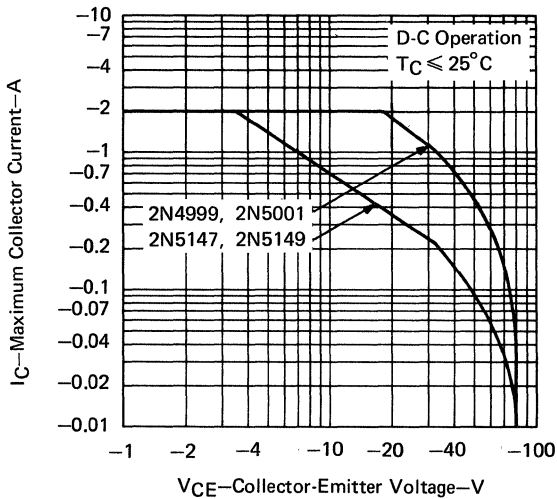


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

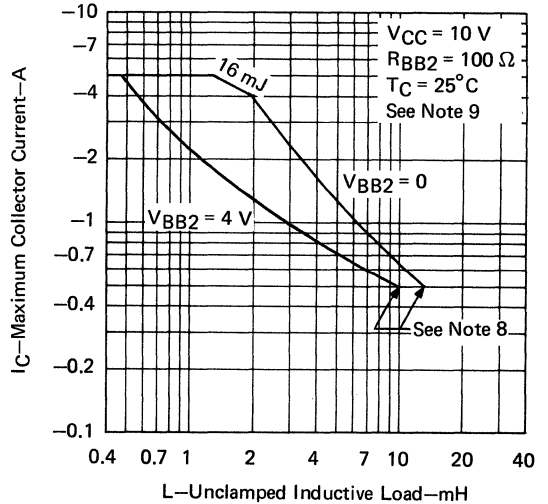


FIGURE 8

NOTES: 8. Above these points the safe operating areas have not been defined.

9. These curves are based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $R_{BB1} = 10 \cdot V_{BB1} / I_C$. $V_{BB1} = 10\text{ V}$, $R_L = 0.1\ \Omega$. Energy $\approx I_C^2 L / 2$.

[†]This circuit appears on page 5-1 of this data book.

THERMAL CHARACTERISTICS

2N4999, 2N5001

DISSIPATION DERATING CURVE

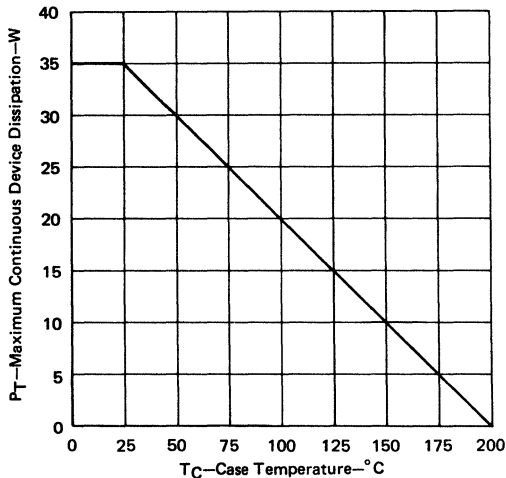


FIGURE 9

2N5147, 2N5149

DISSIPATION DERATING CURVE

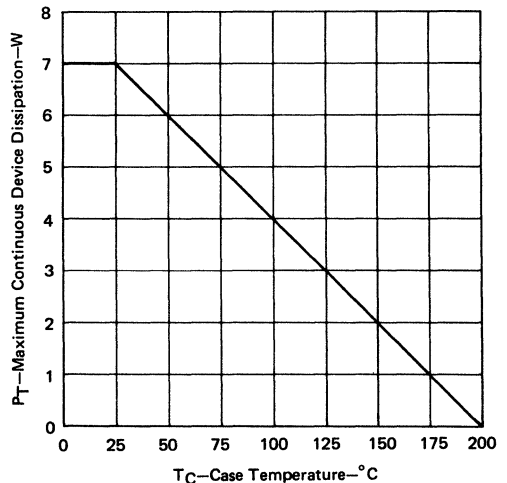


FIGURE 10

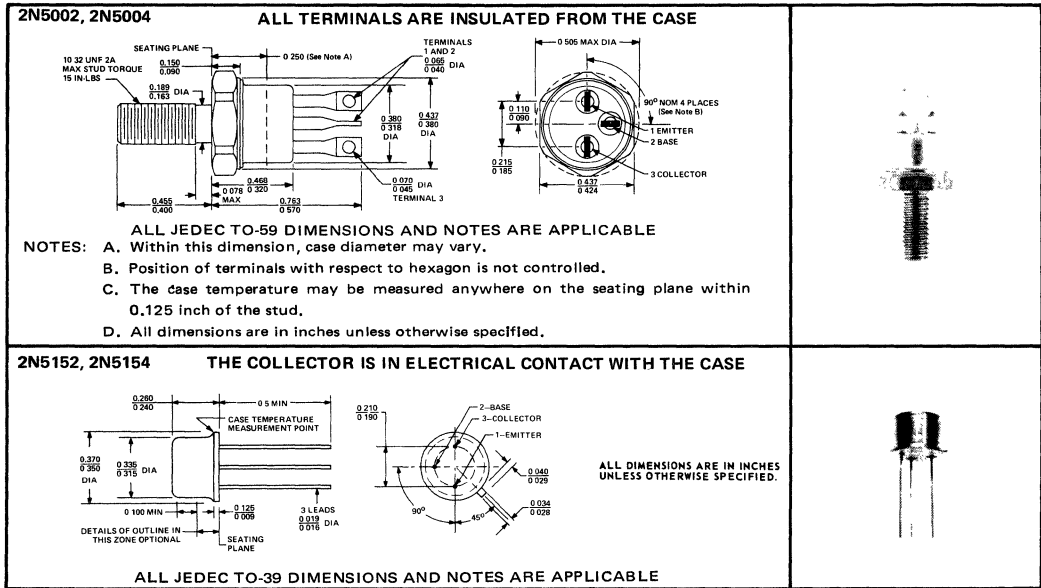
TYPES 2N5002, 2N5004, 2N5152, 2N5154 N-P-N SILICON POWER TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- For Complementary Use with 2N5003, 2N5005, 2N5151, and 2N5153
- 15 mJ Reverse Energy Rating with $I_C = 10$ A and 4 V Reverse Bias

TYPES 2N5002, 2N5004, 2N5152, 2N5154
BULLETIN NO. DL-S-711488, JUNE 1971
REVISED NOVEMBER 1971

*mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5002	2N5152
	2N5004	2N5154
Collector-Base Voltage	← 100 V* →	
Collector-Emitter Voltage (See Note 1)	← 80 V* →	
Emitter-Base Voltage	← 6 V* →	
Continuous Collector Current	5 A*	2 A*
Peak Collector Current (See Note 2)	10 A*	10 A
Continuous Base Current	2 A*	1 A*
Safe Operating Areas	See Figures 7* and 8	
Continuous Device Dissipation at 50°C Case Temperature (See Note 3)	50 W*	10 W*
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	33.3 W	6.7 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)		1 W*
Unclamped Inductive Load Energy (See Note 5)	← 15 mJ →	
Operating Collector Junction Temperature Range	← -65°C to 200°C* →	
Storage Temperature Range	← -65°C to 200°C* →	
Lead or Terminal Temperature 1/8 Inch from Case for 60 Seconds	← 300°C* →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 8.3$ ms, duty cycle $\leq 1\%$.
 3. For operation above (or below) 50°C case temperature, refer to Dissipation Derating Curves, Figure 9 and 10.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*¹. $L = 0.3$ mH, $R_{BB1} = 10$ Ω, $R_{BB2} = 100$ Ω, $V_{BB1} = 10$ V, $V_{BB2} = 4$ V, $R_L = 0.1$ Ω, $V_{CC} = 10$ V, $I_{CM} = 10$ A. Energy $\approx I_C^2 L/2$.

* JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

[†] This circuit appears on page 5-1 of this data book.

TYPES 2N5002, 2N5004, 2N5152, 2N5154

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5002		2N5004		UNIT	
		2N5152		2N5154			
		MIN	MAX	MIN	MAX		
V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = 100 mA, I _B = 0, See Note 6	80		80		V	
I _{CEO} Collector Cutoff Current	V _{CE} = 40 V, I _B = 0		50		50	μA	
I _{CES} Collector Cutoff Current	V _{CE} = 60 V, V _{BE} = 0		1		1	μA	
	V _{CE} = 100 V, V _{BE} = 0		1		1	mA	
I _{CEV} Collector Cutoff Current	V _{CE} = 60 V, V _{BE} = -2 V, T _C = 150°C		500		500	μA	
I _{EBO} Emitter Cutoff Current	V _{EB} = 5 V, I _C = 0		1		1	μA	
	V _{EB} = 6 V, I _C = 0		1		1	mA	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 5 V, I _B = 50 mA		20		50		
	V _{CE} = 5 V, I _C = 2.5 A	See Notes 6 and 7	30	90	70		200
	V _{CE} = 5 V, I _C = 5 A		20		40		
	V _{CE} = 5 V, I _C = 2.5 A, T _C = -55°C		15		35		
V _{BE} Base-Emitter Voltage	I _B = 250 mA, I _C = 2.5 A		See Notes 6 and 7	1.45		1.45	V
I _B = 500 mA, I _C = 5 A	2.2			2.2			
V _{CE} = 5 V, I _C = 2.5 A	1.45			1.45			
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 250 mA, I _C = 2.5 A	See Notes 6 and 7	0.75		0.75	V	
	I _B = 500 mA, I _C = 5 A		1.5		1.5		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 5 V, I _C = 0.1 A, f = 1 kHz		20		50		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 5 V, I _C = 0.5 A, f = 20 MHz		3		3.5		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 V, I _B = 0, f = 1 MHz		250		250	pF	

NOTES: 6. These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 1%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

thermal characteristics

PARAMETER	TEST CONDITIONS	2N5002	2N5152	UNIT
		2N5004	2N5154	
		MAX	MAX	
R _{θJC} Junction-to-Case Thermal Resistance		3	15	°C/W

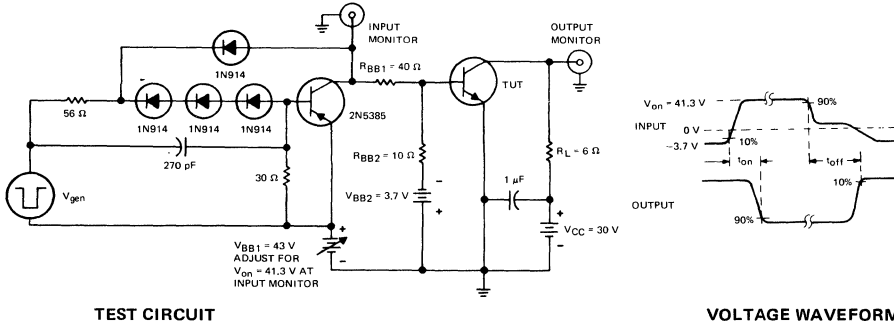
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	ALL TYPES		UNIT
		TYP		
t _{on} Turn-On Time	I _C = 5 A, I _{B(1)} = 500 mA, I _{B(2)} = -500 mA,	0.5		μs
t _{off} Turn-Off Time	V _{BE(off)} = -3.7 V, R _L = 6 Ω, See Figure 1	1.3		

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES 2N5002, 2N5004, 2N5152, 2N5154 N-P-N SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. V_{gen} is a -30 V pulse (from 0 V) into a $50\ \Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\ \Omega$, $t_w = 20\ \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPICAL CHARACTERISTICS

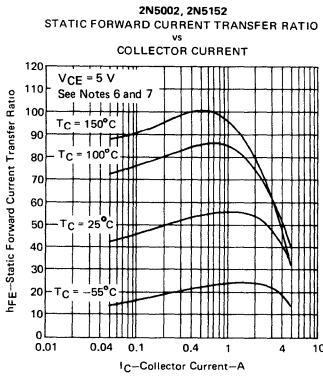


FIGURE 2

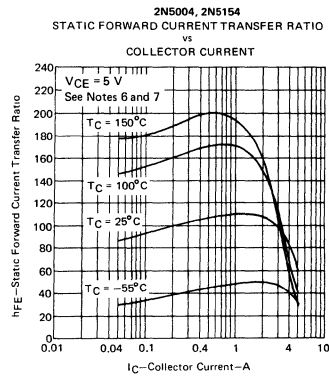


FIGURE 3

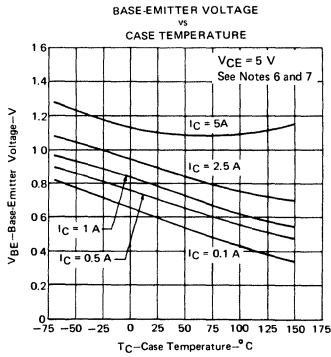


FIGURE 4

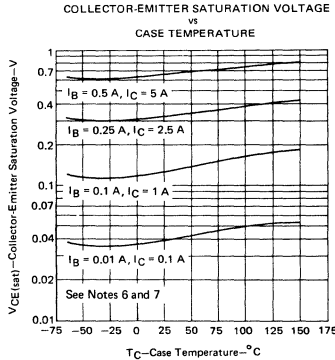


FIGURE 5

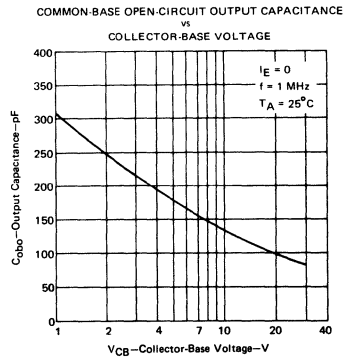


FIGURE 6

- NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300\ \mu\text{s}$, duty cycle $\leq 1\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N5002, 2N5004, 2N5152, 2N5154 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

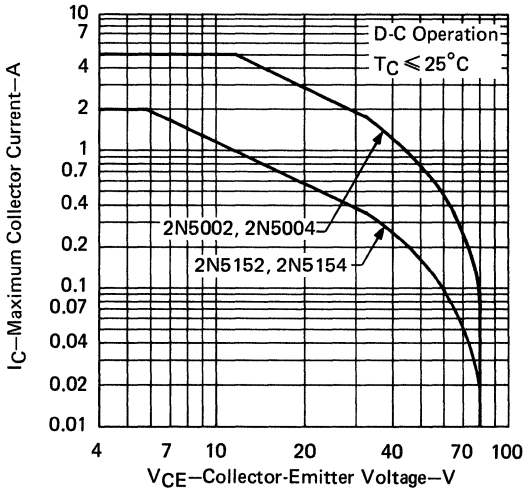


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

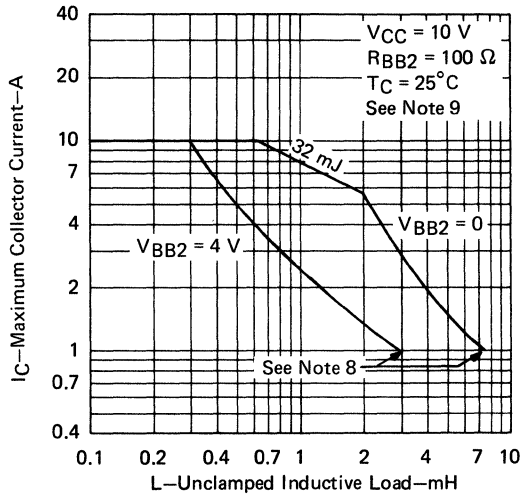


FIGURE 8

- NOTES: 8. Above these points the safe operating areas have not been defined.
9. These curves are based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $R_{BB1} = 10 \cdot V_{BB1} / I_C$, $V_{BB1} = 10 \text{ V}$, $R_L = 0.1 \Omega$. Energy $\approx I_C^2 L / 2$.

[†]This circuit appears on page 5-1 of this data book.

THERMAL CHARACTERISTICS

2N5002, 2N5004
DISSIPATION DERATING CURVE

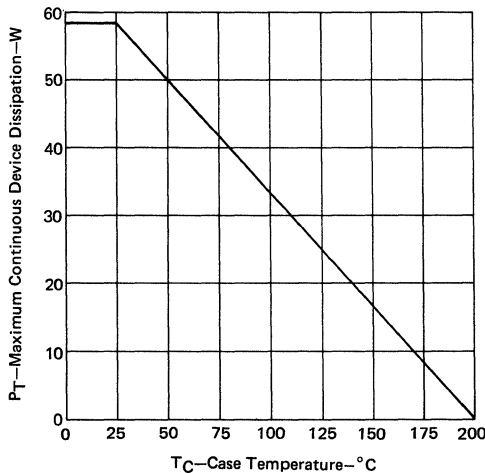


FIGURE 9

2N5152, 2N5154
DISSIPATION DERATING CURVE

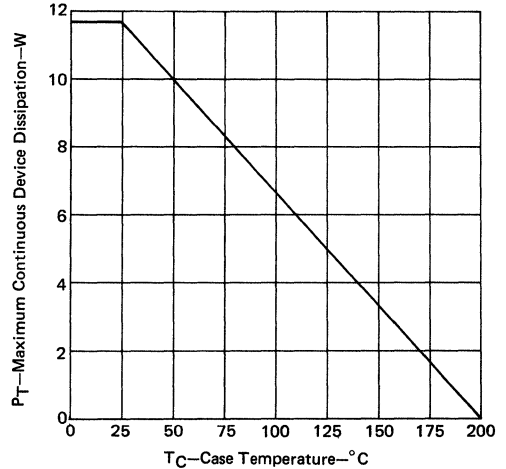


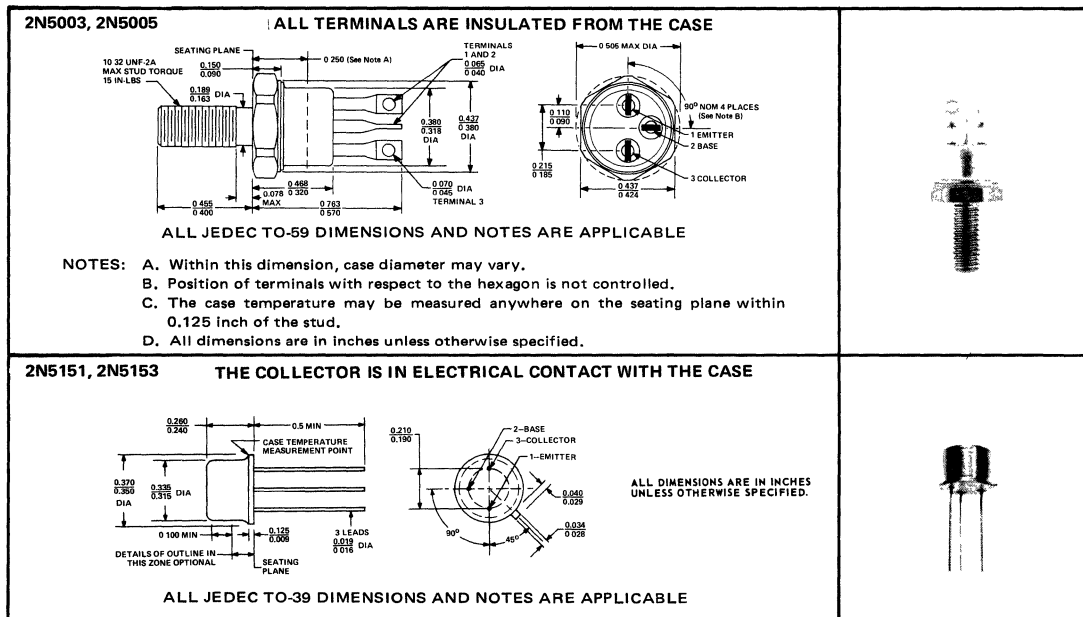
FIGURE 10

TYPES 2N5003, 2N5005, 2N5151, 2N5153 P-N-P SILICON POWER TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- For Complementary Use With 2N5002, 2N5004, 2N5152, 2N5154
- 15 mJ Reverse Energy Rating with $I_C = 10$ A and 4 V Reverse Bias

*mechanical data



TYPES 2N5003, 2N5005, 2N5151, 2N5153
BULLETIN NO. DLS-711491, JUNE 1971
REVISED NOVEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5003	2N5151	2N5005	2N5153
Collector-Base Voltage	← -100 V* →			
Collector-Emitter Voltage (See Note 1)	← -80 V* →			
Emitter-Base Voltage	← -5.5 V* →			
Continuous Collector Current	-5 A*	-5 A*		
Peak Collector Current (See Note 2)	-10 A*	-10 A*		
Continuous Base Current	-2 A*	-2.5 A*		
Safe Operating Areas	See Figures 7* and 8			
Continuous Device Dissipation at 50°C Case Temperature (See Note 3)	50 W*		10 W*	
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	33.3 W		6.7 W	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	1 W*			
Unclamped Inductive Load Energy (See Note 5)	← 15 mJ →			
Operating Collector Junction Temperature Range	-65°C to 200°C*			
Storage Temperature Range	-65°C to 200°C*			
Lead or Terminal Temperature 1/8 Inch from Case for 60 Seconds	← 300°C* →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leq 8.3$ ms, duty cycle $\leq 1\%$.
3. For operation above (or below) 50°C case temperature, refer to Dissipation Derating Curves, Figures 9 and 10.
4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/°C.
5. This rating is based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*†. $L = 0.3$ mH, $R_{BB1} = 10 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 4$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = 10$ A. Energy $\approx I_C^2 L/2$.

* JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

† This circuit appears on page 5-1 of this data book.

TYPES 2N5003, 2N5005, 2N5151, 2N5153

P-N-P SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5003		2N5005		UNIT
		2N5151	2N5153	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -100 \text{ mA}$, $I_B = 0$, See Note 6	-80	-80			V
I_{CEO} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$	-50	-50			μA
I_{CES} Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$	-1	-1			μA
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$	-1	-1			mA
I_{CEV} Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 2 \text{ V}$, $T_C = 150^\circ\text{C}$	-500	-500			μA
I_{EBO} Emitter Cutoff Current	$V_{EB} = -4 \text{ V}$, $I_C = 0$	-1	-1			μA
	$V_{EB} = -5.5 \text{ V}$, $I_C = 0$	-1	-1			mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -50 \text{ mA}$	20	50			
	$V_{CE} = -5 \text{ V}$, $I_C = -2.5 \text{ A}$	30	90	70	200	
	$V_{CE} = -5 \text{ V}$, $I_C = -5 \text{ A}$	20	40			
	$V_{CE} = -5 \text{ V}$, $I_C = -2.5 \text{ A}$, $T_C = -55^\circ\text{C}$	15	35			
V_{BE} Base-Emitter Voltage	$I_B = -250 \text{ mA}$, $I_C = -2.5 \text{ A}$	-1.45	-1.45			V
	$I_B = -500 \text{ mA}$, $I_C = -5 \text{ A}$	-2.2	-2.2			
	$V_{CE} = -5 \text{ V}$, $I_C = -2.5 \text{ A}$	-1.45	-1.45			
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -250 \text{ mA}$, $I_C = -2.5 \text{ A}$	-0.75	-0.75			V
	$I_B = -500 \text{ mA}$, $I_C = -5 \text{ A}$	-1.5	-1.5			
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.1 \text{ A}$, $f = 1 \text{ kHz}$	20	50			
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 20 \text{ MHz}$	3	3.5			
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	250	250			pF

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 1\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

thermal characteristics

PARAMETER		2N5003	2N5151	UNIT
		2N5005	2N5153	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance		3	15	$^\circ\text{C}/\text{W}$

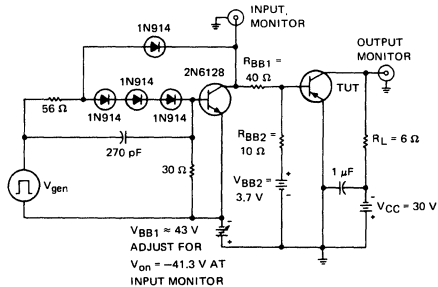
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	ALL TYPES	UNIT
		TYP	
t_{on} Turn-On Time	$I_C = -5 \text{ A}$, $I_{B(1)} = -500 \text{ mA}$, $I_{B(2)} = 500 \text{ mA}$,	0.5	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 3.7 \text{ V}$, $R_L = 6 \Omega$, See Figure 1	1.3	

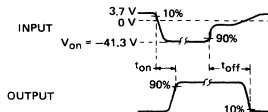
† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES 2N5003, 2N5005, 2N5151, 2N5153 P-N-P SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50 \Omega$, $t_w = 20 \mu$ s, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPICAL CHARACTERISTICS

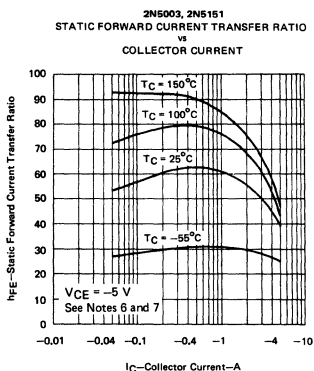


FIGURE 2

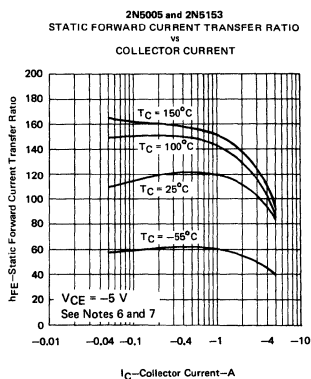


FIGURE 3

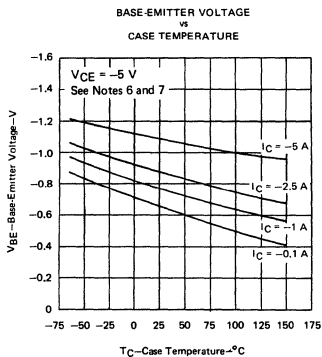


FIGURE 4

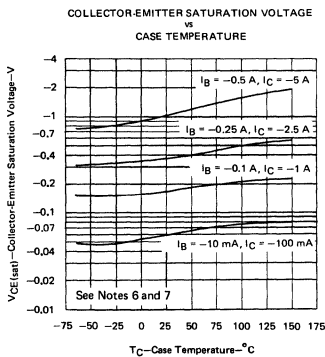


FIGURE 5

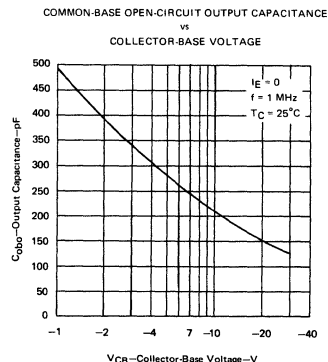


FIGURE 6

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu$ s, duty cycle $\leq 1\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

5

TYPES 2N5003, 2N5005, 2N5151, 2N5153

P-N-P SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

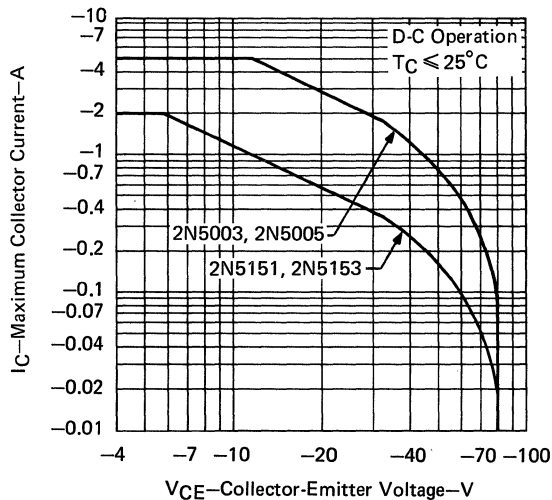


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

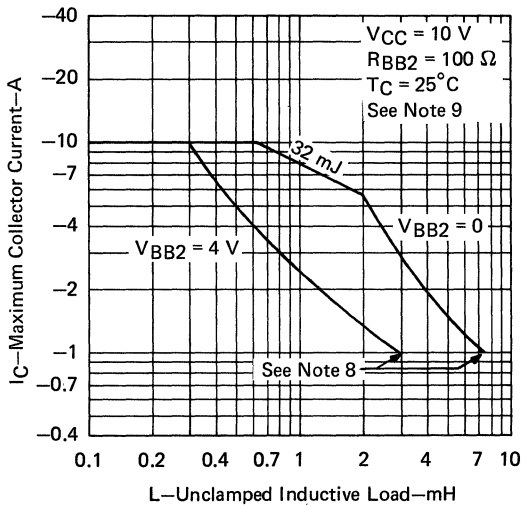


FIGURE 8

NOTES: 8. Above these points the safe operating areas have not been defined.

9. These curves are based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $R_{BB1} = 10 \cdot V_{BB1}/I_C$, $V_{BB1} = 10 \text{ V}$, $R_L = 0.1 \Omega$. Energy $\approx I_C^2 L/2$.

[†]This circuit appears on page 5-1 of this data book.

THERMAL INFORMATION

2N5003, 2N5005
DISSIPATION DERATING CURVE

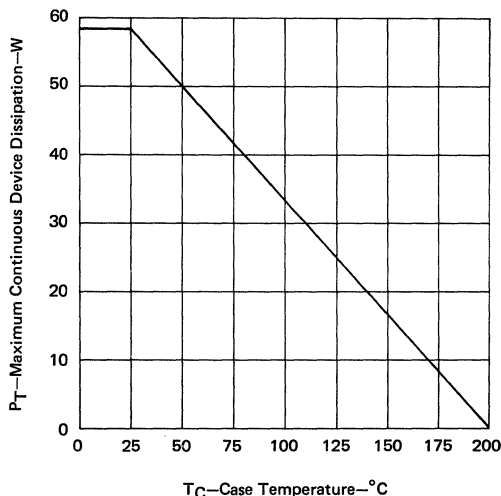


FIGURE 9

2N5151, 2N5153
DISSIPATION DERATING CURVE

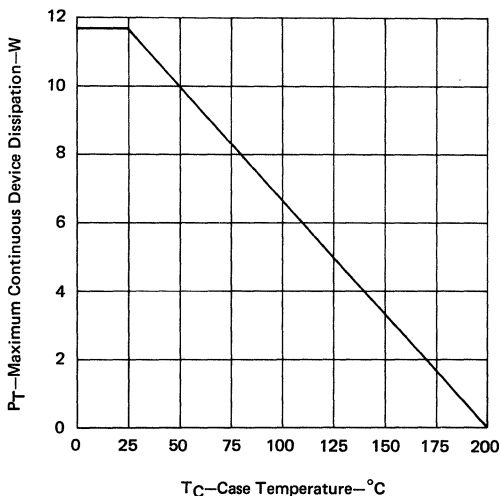


FIGURE 10

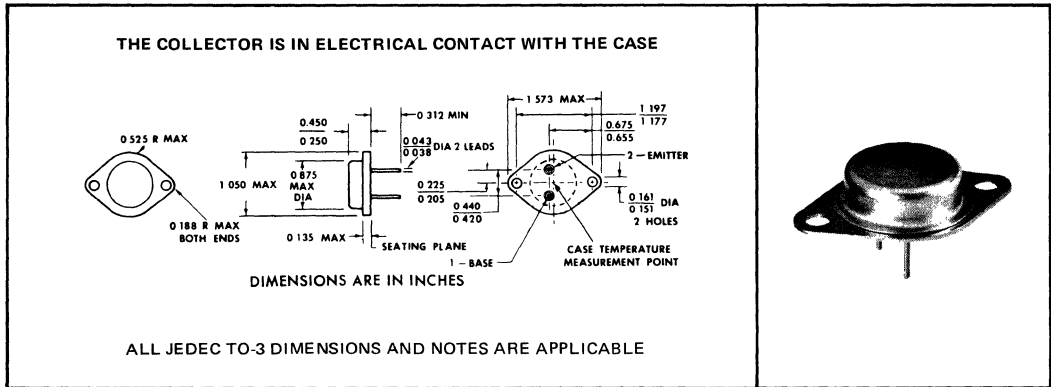
TYPES 2N5038, 2N5039 N-P-N SILICON POWER TRANSISTORS

TYPES 2N5038, 2N5039
BULLETIN NO. DL-S-7111501, JUNE 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED SWITCHING APPLICATIONS

- Min $V_{(BR)CEO}$ of 90 V (2N5038)
- Min f_T of 60 MHz at 10 V, 2 A
- 20-A Rated Continuous Collector Current

***mechanical data**



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5038	2N5039
*Collector-Emitter Voltage ($V_{BE} = -1.5$ V, See Note 1)	150 V	120 V
Collector-Emitter Voltage (Base Open, See Note 1)	90 V	75 V
*Emitter-Base Voltage	7 V	7 V
*Continuous Collector Current	← 20 A →	← 20 A →
*Peak Collector Current (See Note 2)	← 30 A →	← 30 A →
*Continuous Base Current	← 5 A →	← 5 A →
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 140 W →	← 140 W →
*Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 80 W →	← 80 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	← 5 W →
*Operating Collector Junction Temperature Range	-65°C to 200°C	-65°C to 200°C
*Storage Temperature Range	-65°C to 200°C	-65°C to 200°C
Terminal Temperature 1/32 Inch from Case for 10 Seconds	← 230°C →	← 230°C →

- NOTES: 1. These values apply only when the collector-emitter voltage is applied with the transistor in the off-state with the base-emitter diode reverse-biased or open-circuited, as specified.
2. This value applies for $t_w \leq 10$ ms, duty cycle $\leq 50\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.8 W/°C.
4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N5038, 2N5039

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5038		2N5039		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 5	90		75		V
I_{CEV} Collector Cutoff Current	$V_{CE} = 140 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	50				mA
	$V_{CE} = 110 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			50		
	$V_{CE} = 85 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$			10		
	$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	10				
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	5		15		mA
	$V_{EB} = 7 \text{ V}$, $I_C = 0$	50		50		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 5 and 6			20	100	
	$V_{CE} = 5 \text{ V}$, $I_C = 12 \text{ A}$, See Notes 5 and 6	20	100			
V_{BE} Base-Emitter Voltage	$I_B = 5 \text{ A}$, $I_C = 20 \text{ A}$, See Notes 5 and 6	3.3		3.3		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 5 \text{ A}$, $I_C = 20 \text{ A}$, See Notes 5 and 6	2.5		2.5		V
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 2 \text{ A}$, $f = 5 \text{ MHz}$	12		12		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

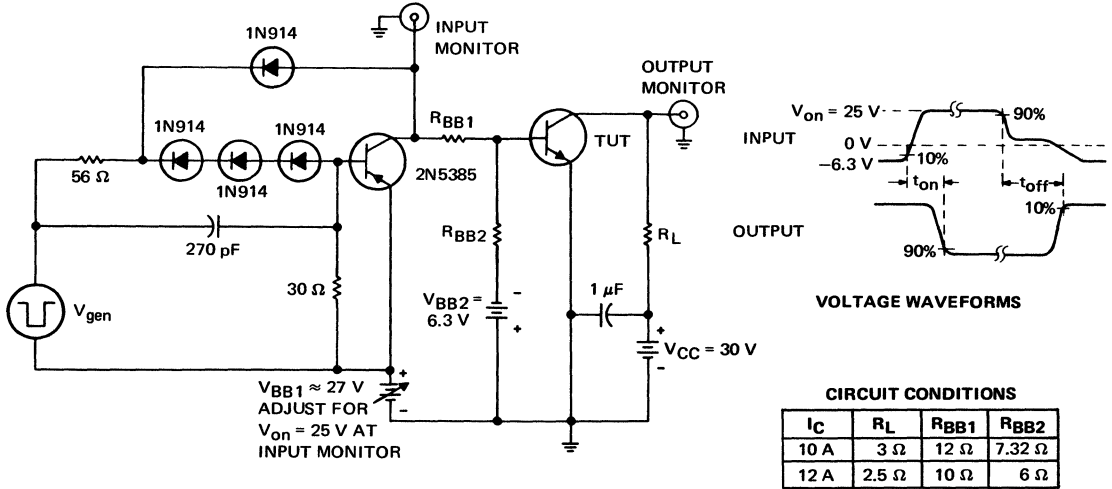
*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_r Rise Time	2N5038 $I_C = 12 \text{ A}$, $I_B(1) = 1.2 \text{ A}$, $I_B(2) = -1.2 \text{ A}$, $V_{BE(off)} = -6.3 \text{ V}$, $R_L = 2.5 \Omega$, See Figure 1	0.5	μs
t_s Storage Time	2N5039 $I_C = 10 \text{ A}$, $I_B(1) = 1 \text{ A}$, $I_B(2) = -1 \text{ A}$, $V_{BE(off)} = -6.3 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	1.5	
t_f Fall Time		0.5	
t_{on} Turn-On Time		0.5	
t_{off} Turn-Off Time		2	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

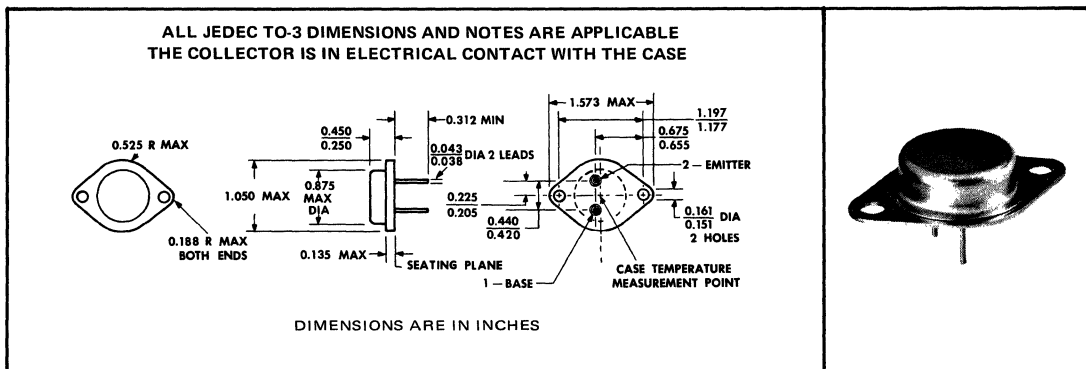
FIGURE 1

TYPES 2N5067, 2N5068, 2N5069 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N4901 THRU 2N4903

- 87.5 W at 25°C Case Temperature
- 5-A Rated Collector Current
- Min f_T of 4 MHz at 10 V, 1 A
- 62.5 mJ Reverse Energy Rating

***mechanical data**



TYPES 2N5067, 2N5068, 2N5069
BULLETIN NO. DL-S-7211663, JANUARY 1972



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5067	2N5068	2N5069
*Collector-Base Voltage	40 V	60 V	80 V
*Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V
*Emitter-Base Voltage	5 V	5 V	5 V
*Continuous Collector Current	← 5 A →		
Peak Collector Current (See Note 2)	← 15 A →		
*Continuous Base Current	← 1 A →		
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 6 and 7 →		
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 87.5 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →		
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →		
*Operating Collector Junction Temperature Range	← -65°C to 200°C →		
*Storage Temperature Range	← -65°C to 200°C →		
*Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 W/°C or refer to Dissipation Derating Curve, Figure 8.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.9 mW/°C or refer to Dissipation Derating Curve, Figure 9.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 5. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L/2$.
- *JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N5067, 2N5068, 2N5069

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5067	2N5068	2N5069	UNIT	
		MIN	MAX	MIN		MAX
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 6	40	60	80	V	
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$	1			mA	
	$V_{CE} = 60 \text{ V}$, $I_B = 0$		1			
	$V_{CE} = 80 \text{ V}$, $I_B = 0$			1		
I_{CEV} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	1			mA	
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		1			
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			1		
	$V_{CE} = 40 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	2				
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		2			
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$			2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1	1	1	mA	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 6 and 7	20	80	20	80	
	$V_{CE} = 2 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 6 and 7	7	7	7	7	
V_{BE} Base-Emitter Voltage	$V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 6 and 7	1.2	1.2	1.2	V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.1 \text{ A}$, $I_C = 1 \text{ A}$, See Notes 6 and 7	0.4	0.4	0.4	V	
	$I_B = 1 \text{ A}$, $I_C = 5 \text{ A}$, See Notes 6 and 7	1.5	1.5	1.5		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	20	20	20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ MHz}$	4	4	4		

*JEDEC registered data

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_{B(1)} = 100 \text{ mA}$, $I_{B(2)} = -100 \text{ mA}$	0.5	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -4.3 \text{ V}$, $R_L = 30 \Omega$, See Figure 4	2	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPICAL CHARACTERISTICS

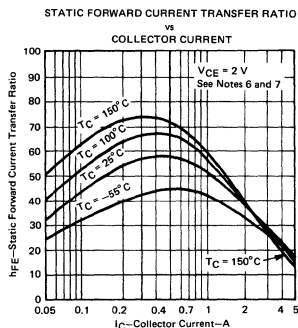


FIGURE 1

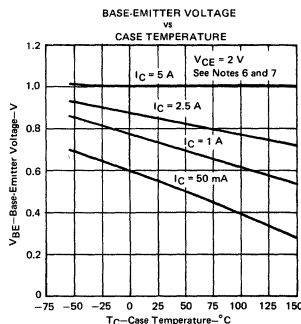


FIGURE 2

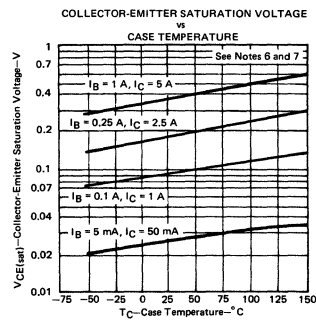
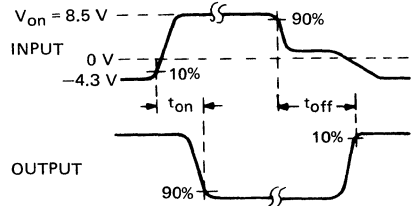
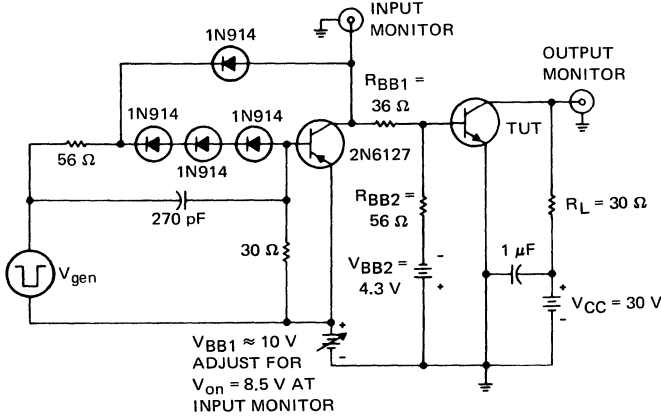


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N5067, 2N5068, 2N5069 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



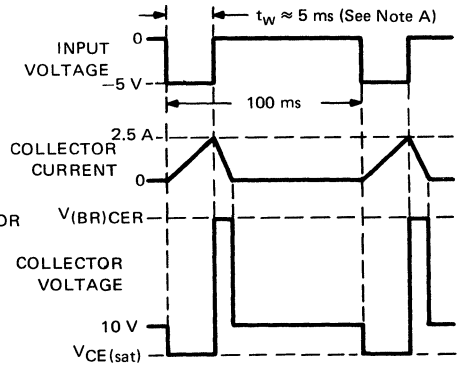
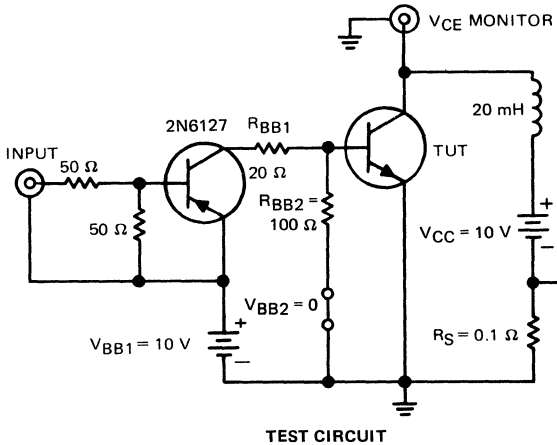
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES:
- A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - D. Resistors must be noninductive types.
 - E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 4

INDUCTIVE LOAD SWITCHING



- NOTE: A. Input pulse width is increased until $I_{CM} = 2.5\text{ A}$.

FIGURE 5

TYPES 2N5067, 2N5068, 2N5069 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

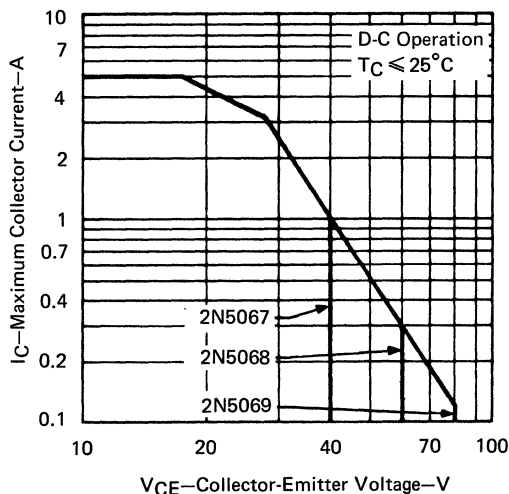


FIGURE 6

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

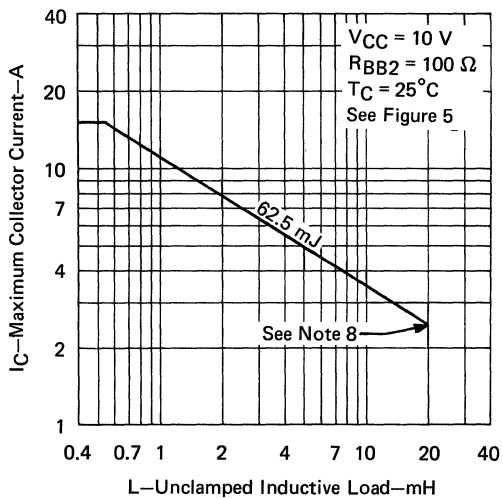


FIGURE 7

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

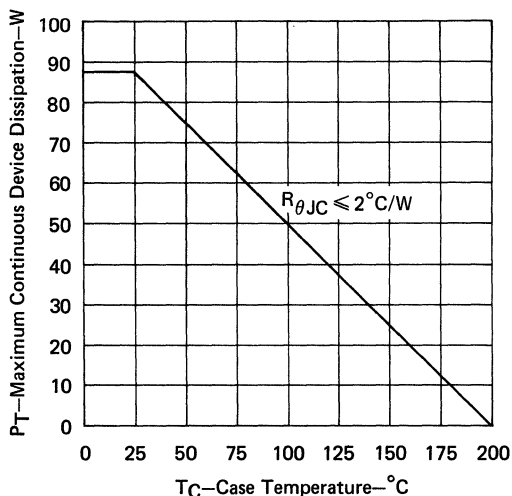


FIGURE 8

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

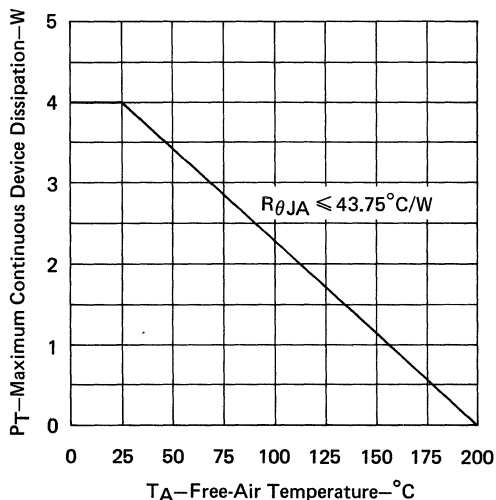


FIGURE 9

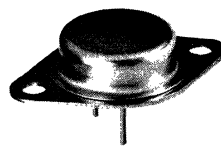
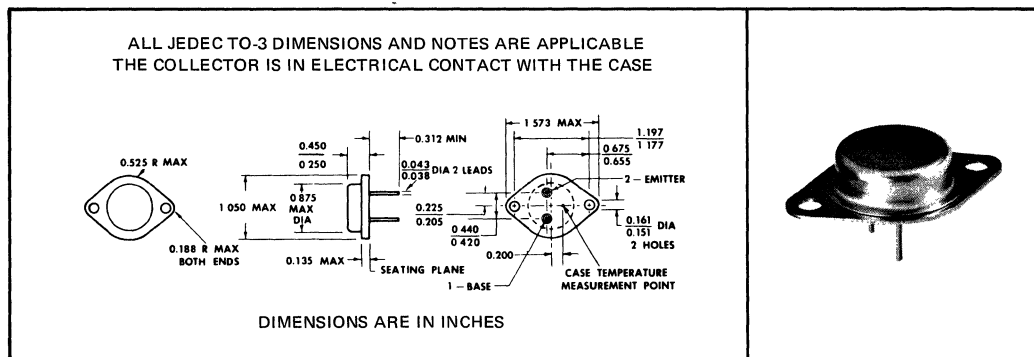
TYPE 2N5157 N-P-N SILICON POWER TRANSISTOR

TYPE 2N5157
BULLETIN NO. DL-S-7111483, MAY 1971

HIGH VOLTAGE, HIGH FORWARD AND REVERSE ENERGY DESIGNED FOR INDUSTRIAL AND MILITARY APPLICATIONS

- 100 W at 75°C Case Temperature
- 700 V Collector-Emitter Off-State Voltage
- Min $V_{(BR)CEO}$ of 400 V
- Max t_{off} of 1.7 μ s at $I_C = 1$ A
- Typ $V_{CE(sat)}$ of 0.3 V at $I_C = 3.5$ A
- Typ f_T of 5 MHz at 12 V, 0.2 A

*mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

* Collector-Emitter Voltage ($V_{BE} = -1.5$ V, See Note 1)	700 V
* Collector-Emitter Voltage (Base Open, See Note 1)	500 V
* Emitter-Base Voltage	6 V
* Continuous Collector Current	3.5 A
* Continuous Base Current	2 A
Safe Operating Area at (or below) 75°C Case Temperature	See Figure 6
* Continuous Device Dissipation at (or below) 75°C Case Temperature (See Note 2)	100 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	4 W
Unclamped Inductive Load Energy (See Note 4)	180 mJ
* Operating Collector Junction Temperature Range	-65°C to 150°C
* Storage Temperature Range	-65°C to 200°C
* Terminal Temperature 1/16 Inch from Case for 10 Seconds	300°C

- NOTES: 1. These values apply only when the collector-emitter voltage is applied with the transistor in the off-state with the base-emitter diode reverse-biased or open-circuited, as specified. In operation, the limitations of Figure 6 must be observed.
2. Derate linearly to 150°C case temperature at the rate of 1.33 W/°C.
3. Derate linearly to 150°C free-air temperature at the rate of 32 mW/°C.
4. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2, condition 1. $L = 40$ mH, $R_{BB2} = 3$ k Ω , $V_{BB2} = 1.5$ V, $R_S = 0.1$ Ω , $V_{CC} = 50$ V. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPE 2N5157

N-P-N SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 100 \text{ mA}$, $I_B = 0$, See Note 5	400			V
$V_{(BR)CER}$ Collector-Emitter Breakdown Voltage	$I_{CM} = 3.5 \text{ A}$, $R_{BE} = 10 \Omega$, See Figure 2 (Condition 2)	500			V
I_{CEO} Collector Cutoff Current	$V_{CE} = 500 \text{ V}$, $I_B = 0$			0.25	mA
I_{CEV} Collector Cutoff Current	$V_{CE} = 700 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			0.5	mA
	$V_{CE} = 400 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 125^\circ\text{C}$			0.5	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 6 \text{ V}$, $I_C = 0$			5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$	See Notes 5 and 6	30	90	
	$V_{CE} = 5 \text{ V}$, $I_C = 2.5 \text{ A}$		10		
	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $T_C = -55^\circ\text{C}$		10		
V_{BE} Base-Emitter Voltage	$I_B = 0.7 \text{ A}$, $I_C = 3.5 \text{ A}$, See Notes 5 and 6		1.1	2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.1 \text{ A}$, $I_C = 1 \text{ A}$	See Notes 5 and 6	0.2	0.8	V
	$I_B = 0.7 \text{ A}$, $I_C = 3.5 \text{ A}$		0.3	2.5	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 12 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ MHz}$	2.8	5		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 20 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$	100	150		pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	0.75	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	31.25	

*switching characteristics at 25°C case temperature

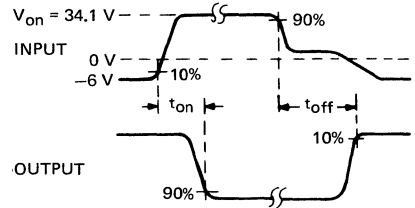
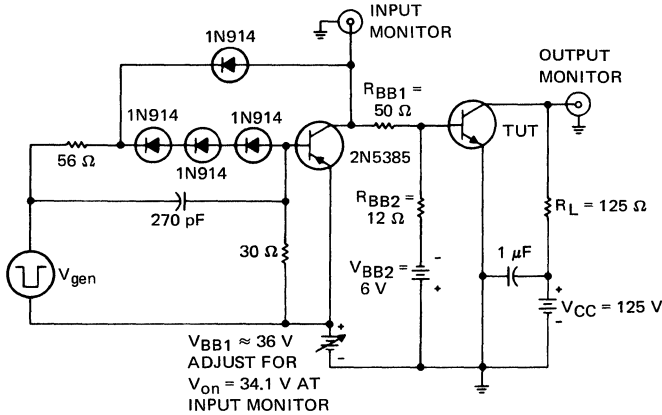
PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_B(1) = 0.1 \text{ A}$, $I_B(2) = -0.5 \text{ A}$,	0.8	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -6 \text{ V}$, $R_L = 125 \Omega$, See Figure 1	1.7	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

* JEDEC registered data

TYPE 2N5157 N-P-N SILICON POWER TRANSISTOR

PARAMETER MEASUREMENT INFORMATION



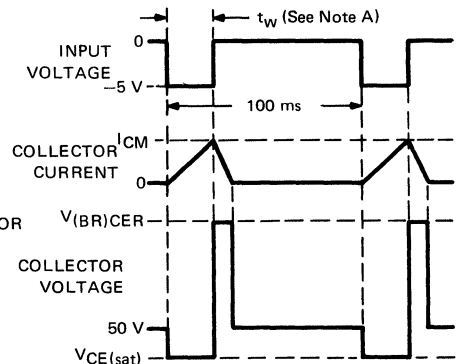
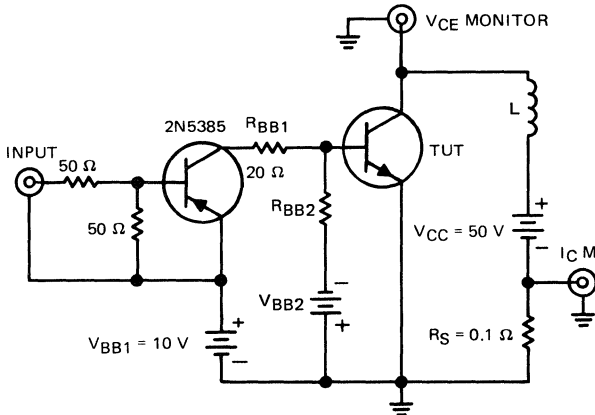
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 5\text{ }\mu\text{s}$, duty cycle $\leq 5\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10\text{ ns}$, $R_{in} \geq 1\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



CONDITION	R_{BB2}	V_{BB2}	L	I_{CM}	t_w
1	$3\text{ k}\Omega$	1.5 V	40 mH	3 A	$\approx 2.4\text{ ms}$
2	$10\text{ }\Omega$	0 V	10 mH	3.5 A	$\approx 0.7\text{ ms}$

TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until the peak collector current reaches the specified value of I_{CM} .

FIGURE 2

TYPE 2N5157

N-P-N SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO VS COLLECTOR CURRENT

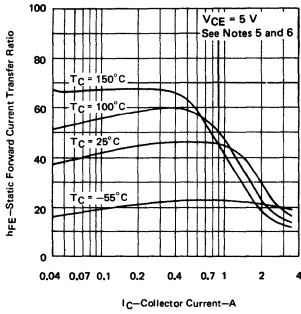


FIGURE 3

BASE-EMITTER VOLTAGE VS CASE TEMPERATURE

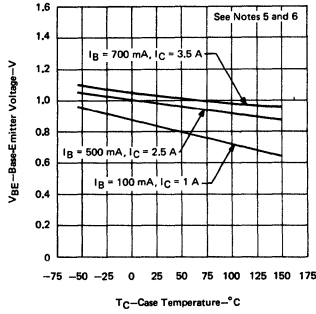


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE VS CASE TEMPERATURE

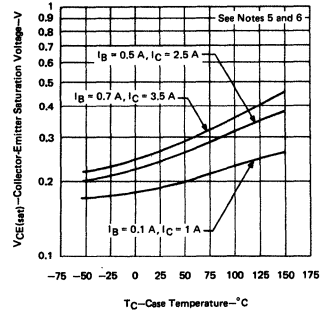


FIGURE 5

5

- NOTES: 5. These parameters must be measured using pulse techniques, $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

MAXIMUM SAFE OPERATING AREA

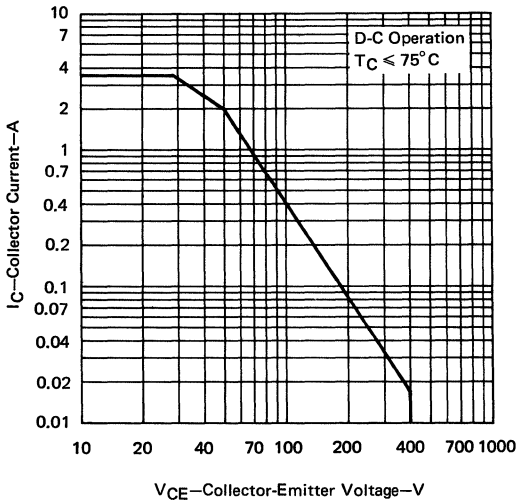


FIGURE 6

THERMAL INFORMATION

DISSIPATION DERATING CURVE

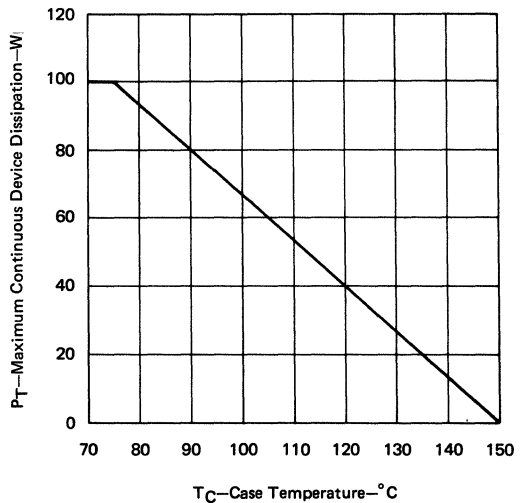


FIGURE 7

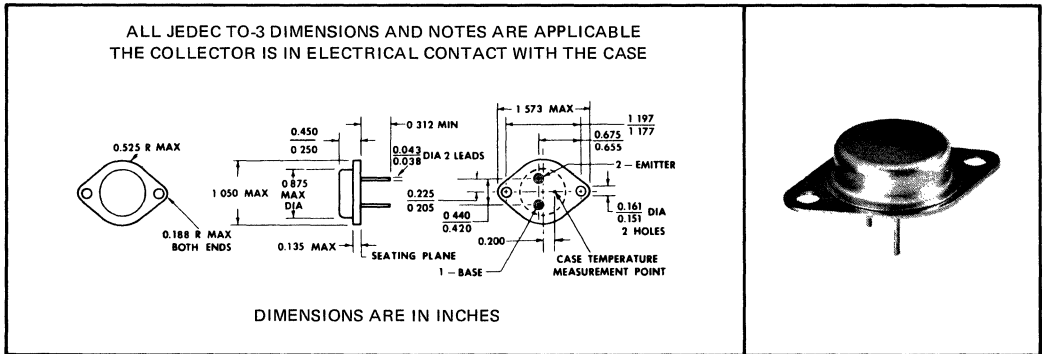
TYPE 2N5241 N-P-N SILICON POWER TRANSISTOR

TYPE 2N5241
BULLETIN NO. DL-S-7111482, MAY 1971

**HIGH VOLTAGE, HIGH FORWARD AND REVERSE ENERGY
DESIGNED FOR INDUSTRIAL AND MILITARY APPLICATIONS**

- 125 W at 62.5°C Case Temperature
- 400 V Collector-Emitter Off-State Voltage
- Min $V_{(BR)CEO}$ of 325 V
- Max t_{off} of 1.7 μs at $I_C = 2.5 A$
- Typ $V_{CE(sat)}$ of 0.35 V at $I_C = 5 A$
- Typ f_T of 5 MHz at 12 V, 0.2 A

***mechanical data**



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

*Collector-Emitter Voltage (See Note 1)	400 V
*Emitter-Base Voltage	5 V
*Continuous Collector Current	5 A
*Continuous Base Current	2 A
Safe Operating Area at (or below) 62.5°C Case Temperature	See Figure 6
*Continuous Device Dissipation at (or below) 62.5°C Case Temperature (See Note 2)	125 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	4 W
Unclamped Inductive Load Energy (See Note 4)	180 mJ
*Operating Collector Junction Temperature Range	-65°C to 150°C
*Storage Temperature Range	-65°C to 200°C
*Terminal Temperature 1/16 Inch from Case for 10 Seconds	300°C

NOTES: 1. This value applies only when the collector-emitter voltage is applied with the transistor in the off-state with the base-emitter diode reverse-biased or open-circuited. In operation, the limitations of Figure 6 must be observed.

2. Derate linearly to 150°C case temperature at the rate 1.43 W/°C.

3. Derate linearly to 150°C free-air temperature at the rate 32 mW/°C.

4. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. L = 40 mH, $R_{BB2} = 3 k\Omega$, $V_{BB2} = 1.5 V$, $R_S = 0.1 \Omega$, $V_{CC} = 50 V$. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPE 2N5241

N-P-N SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 100 \text{ mA}$, $I_B = 0$, See Note 5	325			V
I_{CEO} Collector Cutoff Current	$V_{CE} = 400 \text{ V}$, $I_B = 0$		2.5		mA
I_{CEV} Collector Cutoff Current	$V_{CE} = 400 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		0.5		mA
I_{EBO} Emitter Cutoff Current	$V_{CE} = 400 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 125^\circ\text{C}$		5		mA
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		2		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 2.5 \text{ A}$ $V_{CE} = 5 \text{ V}$, $I_C = 3.5 \text{ A}$	See Notes 5 and 6	15 10	35	
V_{BE} Base-Emitter Voltage	$I_B = 0.5 \text{ A}$, $I_C = 2.5 \text{ A}$ $I_B = 1 \text{ A}$, $I_C = 5 \text{ A}$	See Notes 5 and 6	1 1.2	1.5 2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 2.5 \text{ A}$ $I_B = 1 \text{ A}$, $I_C = 5 \text{ A}$	See Notes 5 and 6	0.25 0.35	0.7 2.5	V
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 12 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ MHz}$	2.5	5		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

5

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	0.7	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	31.25	

*switching characteristics at 25°C case temperature

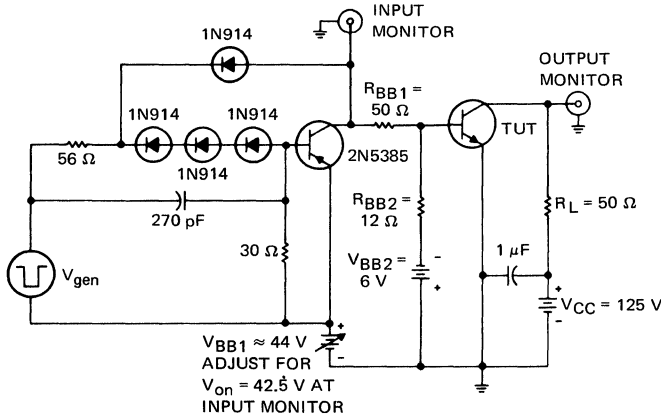
PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = 2.5 \text{ A}$, $I_{B(1)} = 0.25 \text{ A}$, $I_{B(2)} = -0.5 \text{ A}$	0.8	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -6 \text{ V}$, $R_L = 50 \Omega$, See Figure 1	1.7	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

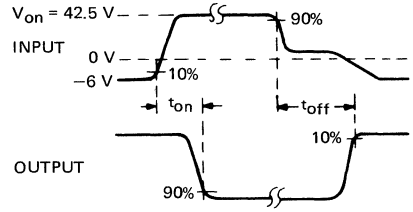
*JEDEC registered data.

TYPE 2N5241 N-P-N SILICON POWER TRANSISTOR

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

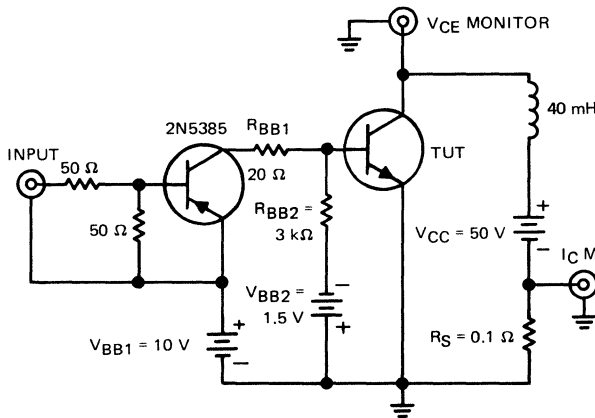


VOLTAGE WAVEFORMS

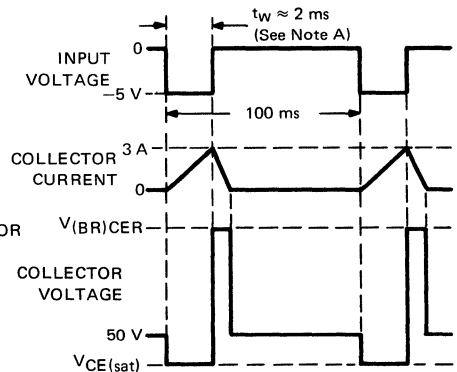
- NOTES:**
- A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 5\text{ }\mu\text{s}$, duty cycle $\leq 5\%$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10\text{ ns}$, $R_{in} \geq 1\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - D. Resistors must be noninductive types.
 - E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = 3\text{ A}$.

FIGURE 2

TYPE 2N5241

N-P-N SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO VS COLLECTOR CURRENT

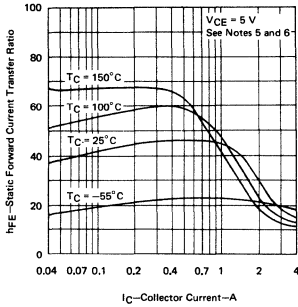


FIGURE 3

BASE-EMITTER VOLTAGE VS CASE TEMPERATURE

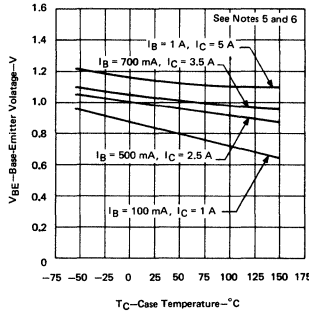


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE VS CASE TEMPERATURE

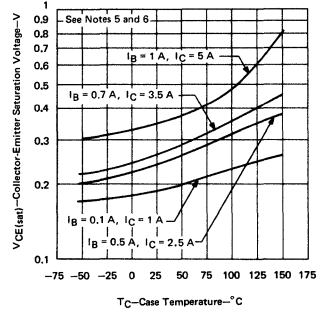


FIGURE 5

NOTES: 5. These parameters must be measured using pulse techniques. $t_{w} = 300 \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

MAXIMUM SAFE OPERATING AREA

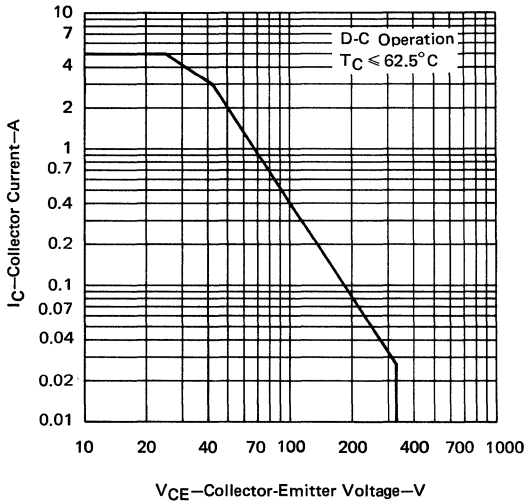


FIGURE 6

THERMAL INFORMATION

DISSIPATION DERATING CURVE

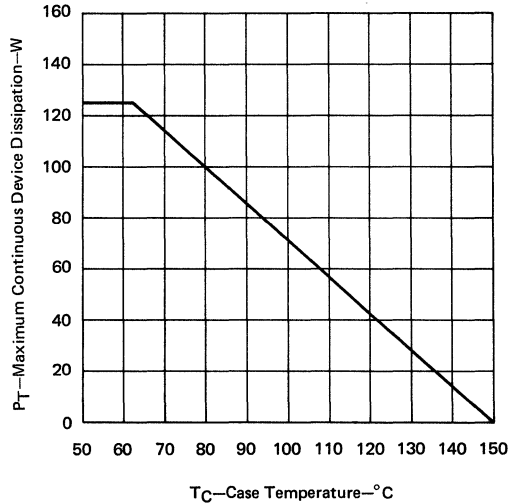


FIGURE 7

TYPES 2N5301, 2N5302, 2N5303 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
2N5301, 2N5302 DESIGNED FOR COMPLEMENTARY USE WITH 2N4398, 2N4399

200 W at 25°C Case Temperature

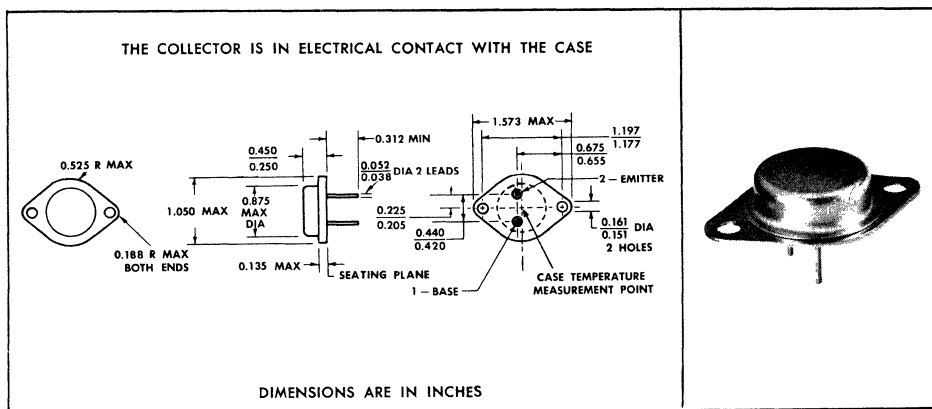
30-A Rated Continuous Collector Current (2N5301, 2N5302)

20-A Rated Continuous Collector Current (2N5303)

Min f_T of 2 MHz at 10 V, 1 A

***mechanical data**

The case outline is the same as JEDEC TO-3 except for lead diameter.



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5301	2N5302	2N5303
*Collector-Base Voltage	40 V	60 V	80 V
*Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V
*Emitter-Base Voltage	5 V	5 V	5 V
*Continuous Collector Current	30 A	30 A	20 A
*Peak Collector Current (See Note 2)	← 50 A →		
*Continuous Base Current	← 7.5 A →		
Safe Operating Region at (or below) 25°C Case Temperature	See Figures 7 and 8		
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 200 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →		
*Operating Collector Junction Temperature Range	-65°C to 200°C		
*Storage Temperature Range	-65°C to 200°C		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 1.14 W/deg.
4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/deg.
*Indicates JEDEC registered data

TYPES 2N5301, 2N5302, 2N5303
BULLETIN NO. DL-S-711086 FEBRUARY 1969
REVISED SEPTEMBER 1971



TYPES 2N5301, 2N5302, 2N5303

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5301	2N5302	2N5303	UNIT
		MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 5	40	60	80	V
I_{CBO} Collector Cutoff Current	$V_{CB} = 40 \text{ V}$, $I_E = 0$	1			mA
	$V_{CB} = 60 \text{ V}$, $I_E = 0$		1		
	$V_{CB} = 80 \text{ V}$, $I_E = 0$			1	
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$	5			mA
	$V_{CE} = 60 \text{ V}$, $I_B = 0$		5		
	$V_{CE} = 80 \text{ V}$, $I_B = 0$			5	
I_{CEV} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	1			mA
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		1		
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			1	
	$V_{CE} = 40 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	10			
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		10		
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$			10	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	5	5	5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$	40	40	40	
	$V_{CE} = 2 \text{ V}$, $I_C = 10 \text{ A}$			15 60	
	$V_{CE} = 2 \text{ V}$, $I_C = 15 \text{ A}$	15 60	15 60		
	$V_{CE} = 2 \text{ V}$, $I_C = 20 \text{ A}$			5	
	$V_{CE} = 2 \text{ V}$, $I_C = 30 \text{ A}$	5	5		
V_{BE} Base-Emitter Voltage	$I_B = 1 \text{ A}$, $I_C = 10 \text{ A}$	1.7	1.7	1.7	V
	$I_B = 1.5 \text{ A}$, $I_C = 15 \text{ A}$	1.8	1.8	2	
	$I_B = 2 \text{ A}$, $I_C = 20 \text{ A}$	2.5	2.5		
	$I_B = 4 \text{ A}$, $I_C = 20 \text{ A}$			2.5	
	$V_{CE} = 2 \text{ V}$, $I_C = 10 \text{ A}$			1.5	
	$V_{CE} = 2 \text{ V}$, $I_C = 15 \text{ A}$	1.7	1.7		
	$V_{CE} = 4 \text{ V}$, $I_C = 20 \text{ A}$			2.5	
	$V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$	3	3		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1 \text{ A}$, $I_C = 10 \text{ A}$	0.75	0.75	1	V
	$I_B = 1.5 \text{ A}$, $I_C = 15 \text{ A}$			1.5	
	$I_B = 2 \text{ A}$, $I_C = 20 \text{ A}$	2	2		
	$I_B = 4 \text{ A}$, $I_C = 20 \text{ A}$			2	
	$I_B = 6 \text{ A}$, $I_C = 30 \text{ A}$	3	3		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	40	40	40	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ MHz}$	2	2	2	

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*Indicates JEDEC registered data

TYPES 2N5301, 2N5302, 2N5303

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	0.875	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	35	

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_r Rise Time	$I_C = 10 \text{ A}$, $I_{B(1)} = 1 \text{ A}$, $V_{BE(off)} = -2 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	1	μs
t_s Storage Time	$I_C = 10 \text{ A}$, $I_{B(1)} = 1 \text{ A}$, $I_{B(2)} = -1 \text{ A}$,	2	
t_f Fall Time	$R_L = 3 \Omega$, See Figure 2	1	

† Voltage and current values shown are nominal, exact values vary slightly with transistor parameters.

*PARAMETER MEASUREMENT INFORMATION

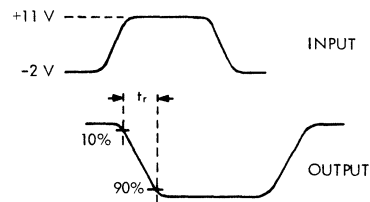
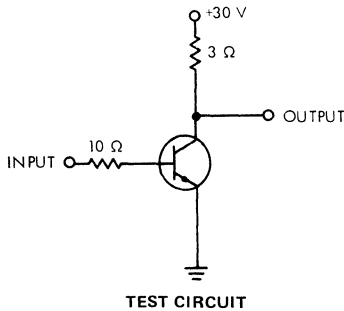


FIGURE 1 – RISE TIME

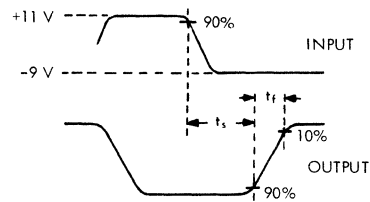
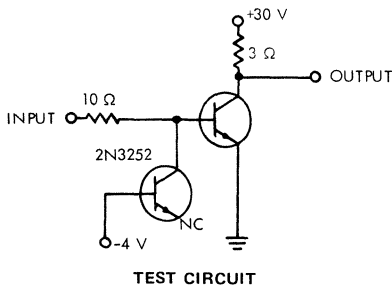


FIGURE 2 – STORAGE AND FALL TIMES

- NOTES: a. The input waveforms are supplied by a generator with the following characteristics: $t_r \leq 20 \text{ ns}$, $t_f \leq 20 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$ to $100 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 20 \text{ ns}$, $R_{in} \geq 10 \text{ k}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

*Indicates JEDEC registered data

TYPES 2N5301, 2N5302, 2N5303

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

5

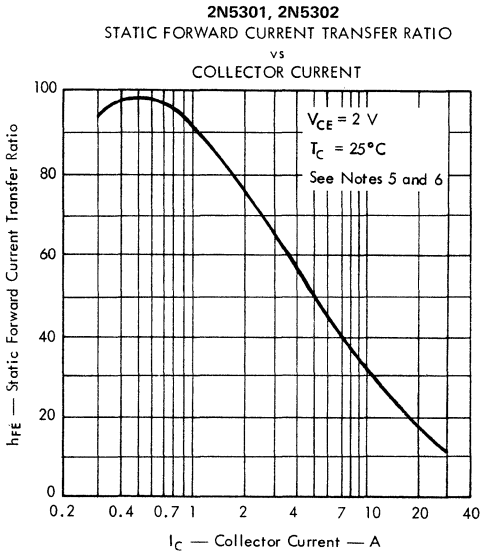


FIGURE 3

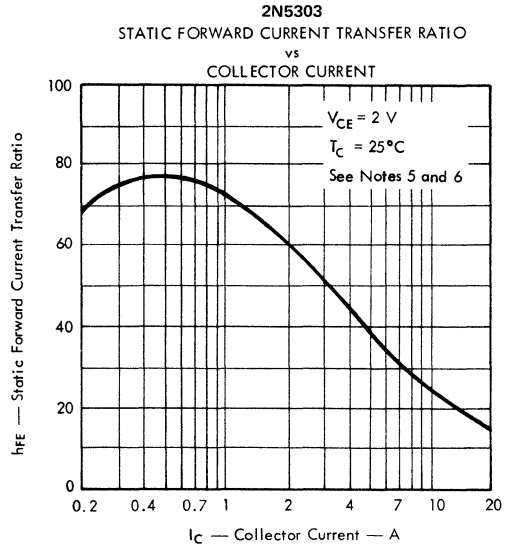


FIGURE 4

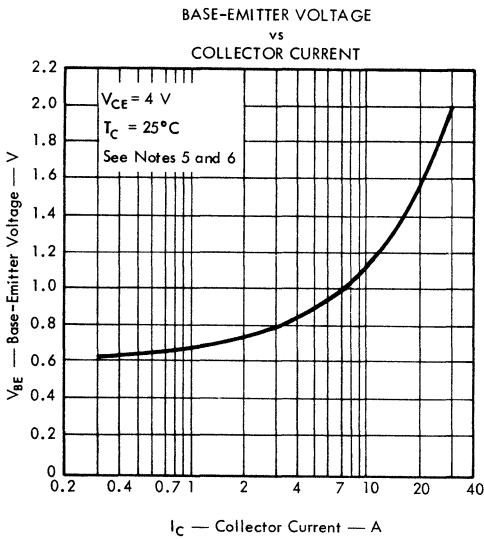


FIGURE 5

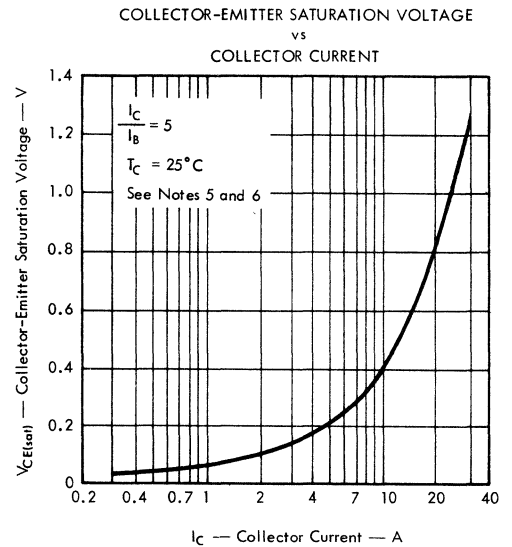


FIGURE 6

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N5301, 2N5302, 2N5303 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGIONS

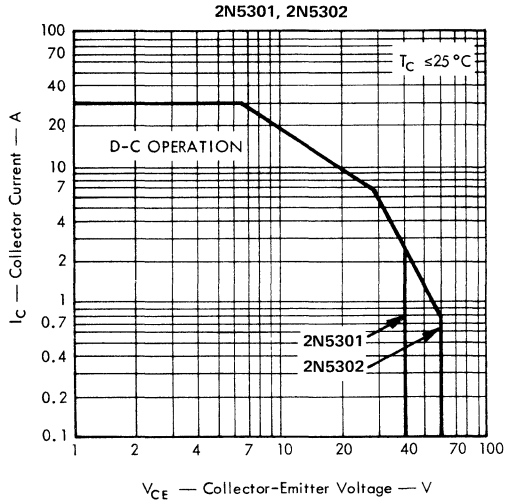


FIGURE 7

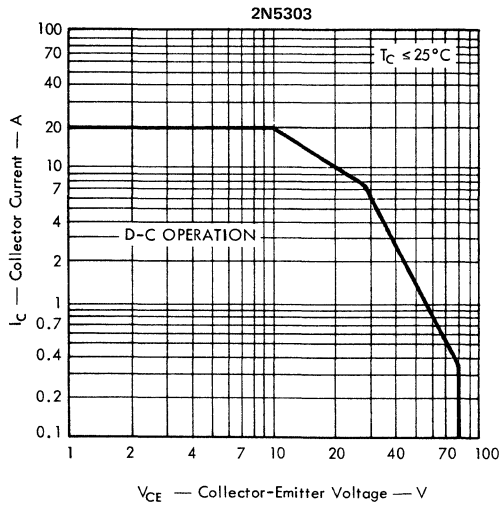


FIGURE 8

5

TYPES 2N5301, 2N5302, 2N5303

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

THEMAL INFORMATION

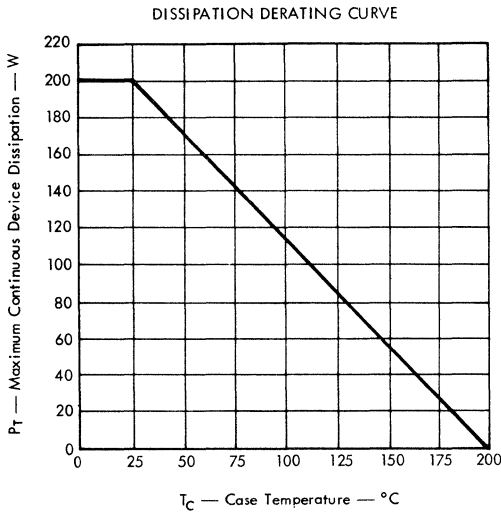


FIGURE 9

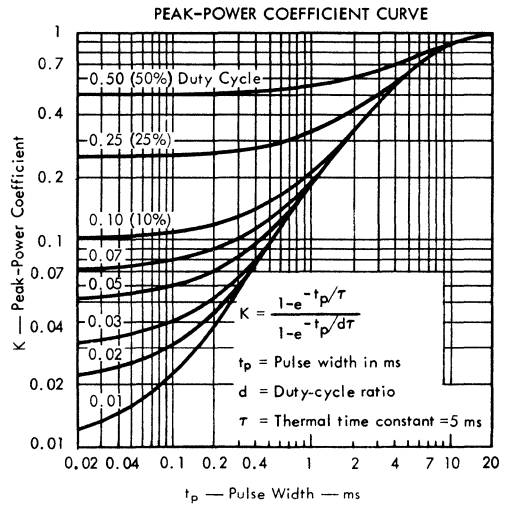


FIGURE 10

5

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	35	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	0.875	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	34.125	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 10	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C} \text{ as in Figure 9}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$\theta_{C-HS} + \theta_{HS-A} = 2.25 \text{ deg/W}$ (From information supplied with heat sink.)

$T_{J(av)}$ (design limit) = 200°C

$T_A = 50^\circ\text{C}$

$d = 10\%$ (0.1)

$t_p = 0.1 \text{ ms}$

Solution:

From Figure 10, Peak-Power Coefficient

$K = 0.109$ and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(2.25) + 0.109(0.875)} = 469 \text{ W}$$

TYPE 2N5333

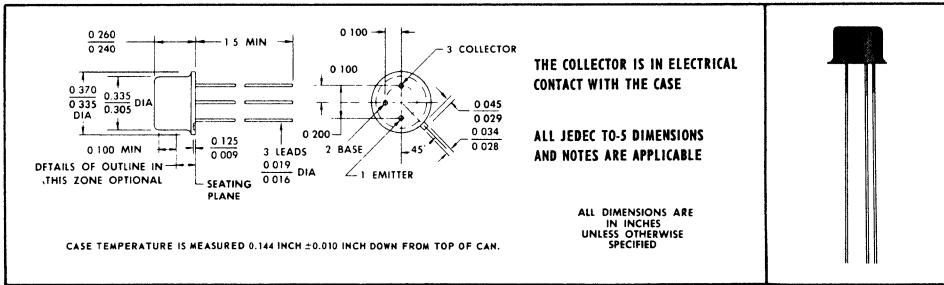
P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPE 2N5333
BULLETIN NO. DL-5 689281, MARCH 1968

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N4300**

- 15 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.45 V at 1 A I_C
- Typ t_{on} of 150 ns at 1 A I_C
- Min f_T of 30 MHz

***mechanical data**



5

***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector-Base Voltage	-100 V
Collector-Emitter Voltage (See Note 1)	-80 V
Emitter-Base Voltage	-6 V
Continuous Collector Current	-2 A
Peak Collector Current (See Note 2)	-5 A
Continuous Base Current	-1 A
Continuous Emitter Current	-3 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	15 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	1 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Lead Temperature $\frac{1}{16}$ Inch from Case for 10 Seconds	260°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_D \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.15 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.72 mW/deg.

*JEDEC registered data

TYPE 2N5333

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-80		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-50	μA
I_{CES}	Collector Cutoff Current	$V_{CE} = -90 \text{ V}$, $V_{BE} = 0$		-10	μA
		$V_{CE} = -50 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-500	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = -4 \text{ V}$, $I_C = 0$		-1	μA
		$V_{EB} = -6 \text{ V}$, $I_C = 0$		-100	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 5 and 6	30	120	
		$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 5 and 6	10		
V_{BE}	Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 5 and 6		-1.5	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -0.1 \text{ A}$, $I_C = -1 \text{ A}$, See Notes 5 and 6		-0.45	V
		$I_B = -0.4 \text{ A}$, $I_C = -2 \text{ A}$, See Notes 5 and 6		-1	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$	30		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 15 \text{ MHz}$	2		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER		MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance	6.66	deg/W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	

*JEDEC registered data

5

TYPE 2N5333

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -1 \text{ A}$, $I_{B(1)} = -0.1 \text{ A}$, $I_{B(2)} = 0.1 \text{ A}$,	150	ns
t_{off} Turn-Off Time	$V_{BE(off)} = 3.7 \text{ V}$, $R_L = 20 \Omega$, See Figure 1	450	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

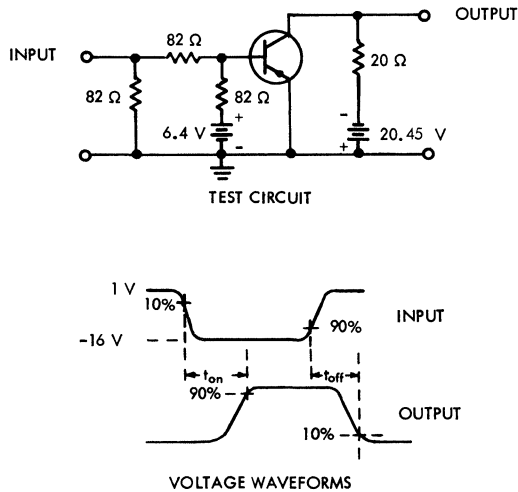


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 2 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPE 2N5333

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

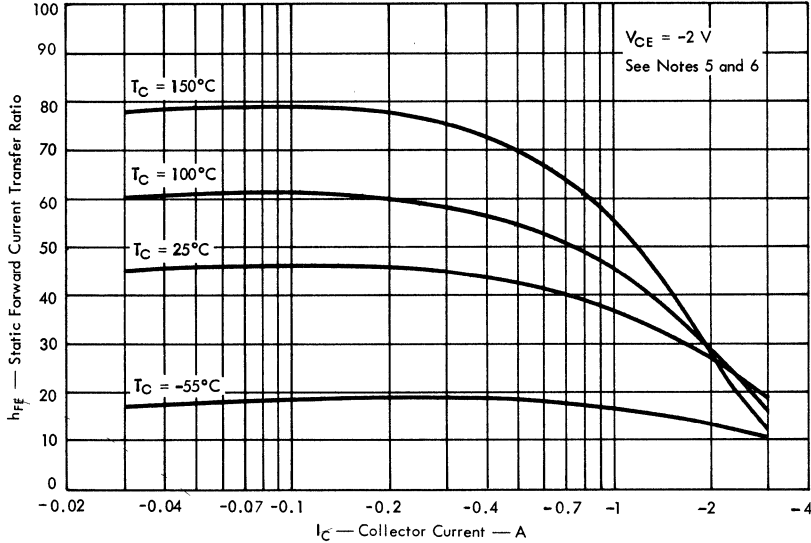


FIGURE 2

BASE-EMITTER VOLTAGE
vs
CASE TEMPERATURE

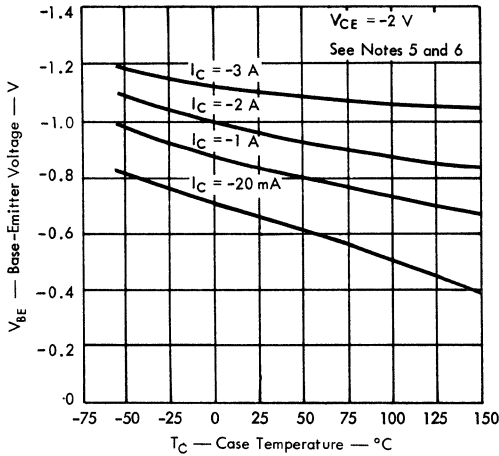


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE

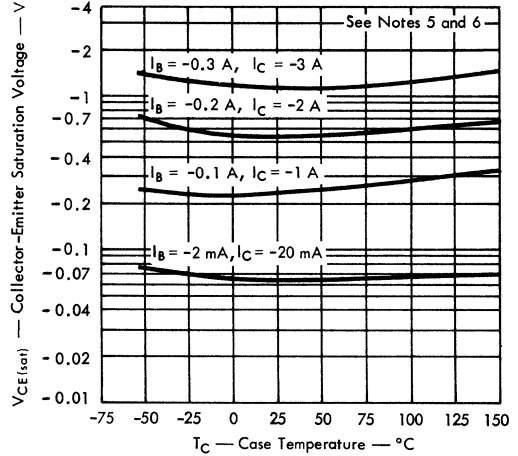


FIGURE 4

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPE 2N5333

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

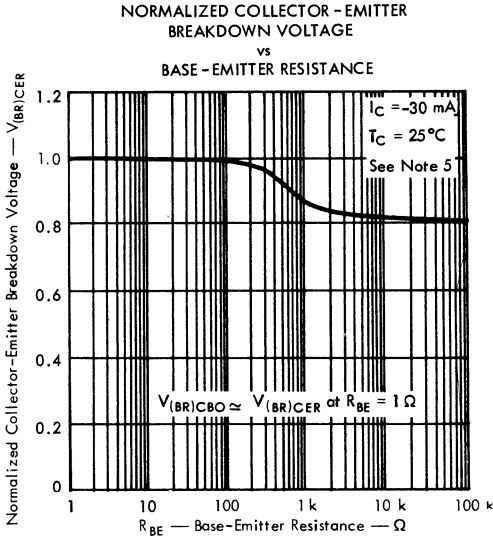


FIGURE 5

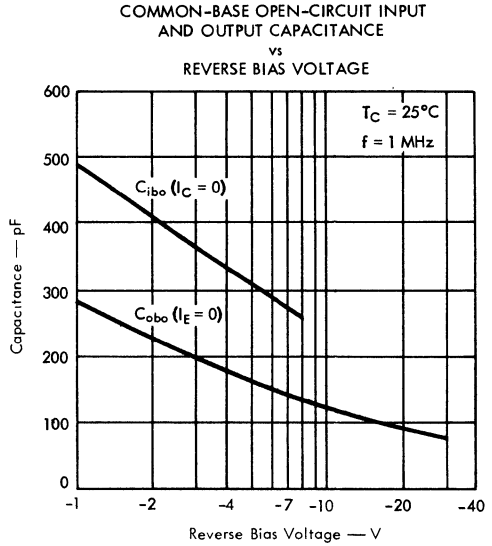


FIGURE 6

NOTE 5: These parameters must be measured using pulse techniques. $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

MAXIMUM SAFE OPERATING REGION

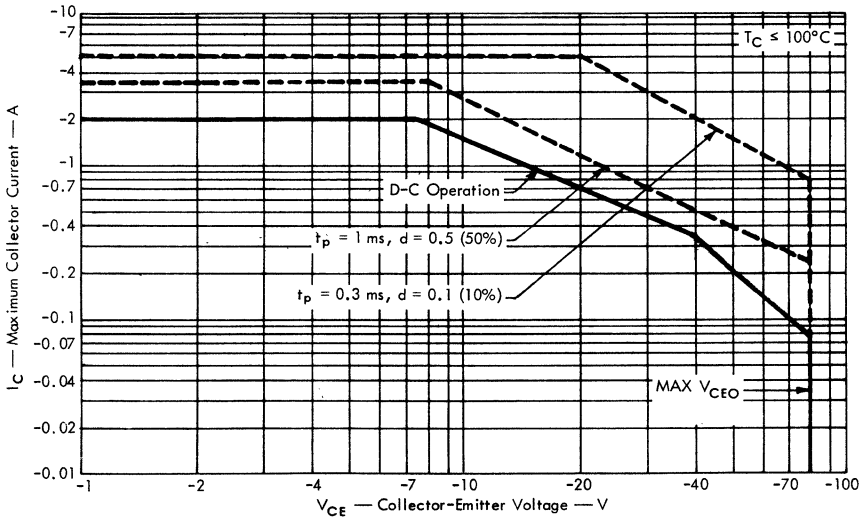


FIGURE 7

5

TYPE 2N5333

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

THERMAL INFORMATION

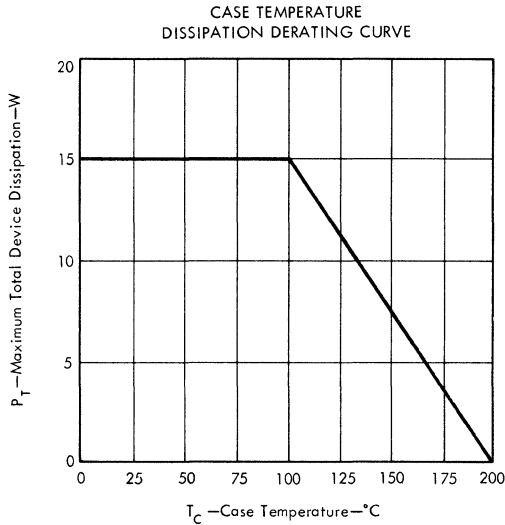


FIGURE 8

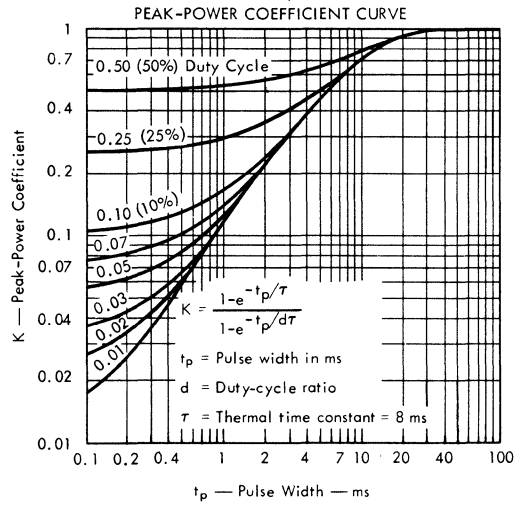


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	6.66	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)
OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 7 \text{ deg/W (From information supplied with heat sink.)}$$

$$\begin{aligned} T_{J(av)} \text{ (design limit)} &= 200^\circ\text{C} \\ T_A &= 50^\circ\text{C} \\ d &= 10\% (0.1) \\ t_p &= 0.1 \text{ ms} \end{aligned}$$

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C} \text{ as in Figure 8}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.105 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + 0.105(6.66)} = 107 \text{ W}$$

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TYPES 2N5384, 2N5385

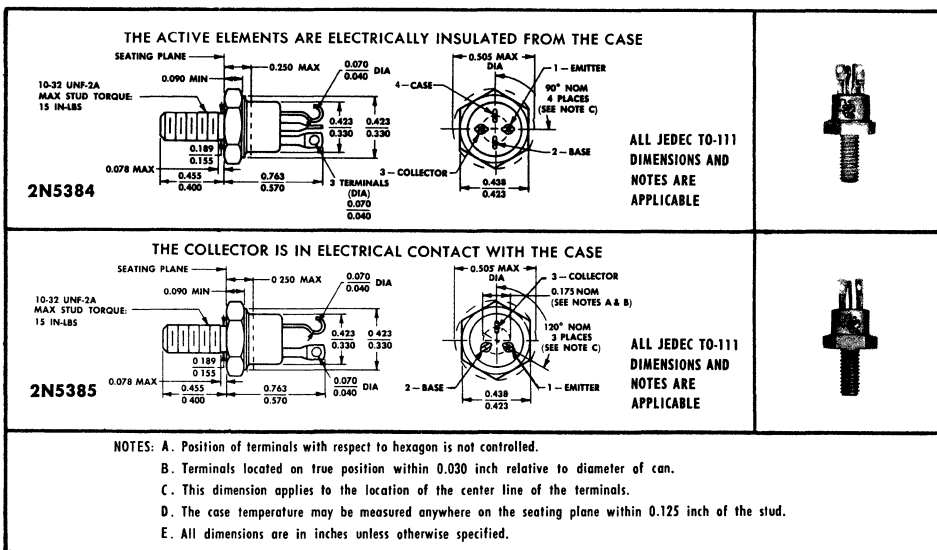
P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTORS

TYPES 2N5384, 2N5385
BULLETIN NO. DLS-689279, MARCH 1968

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N3996 AND 2N3998**

- 30 W at 100°C Case Temperature
- Typ t_{on} of 160 ns at 2 A I_c
- Max $V_{CE(sat)}$ of 0.6 V at 2 A I_c
- Min f_T of 30 MHz

***mechanical data**



5

***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector-Base Voltage	-100 V
Collector-Emitter Voltage (See Note 1)	-80 V
Emitter-Base Voltage	-6 V
Continuous Collector Current	-5 A
Peak Collector Current (See Note 2)	-12 A
Continuous Base Current	-1 A
Continuous Emitter Current	-6 A
Safe Operating Region at (or below) 100°C Case Temperature.	See Figure 2
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	30 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $I_B \leq 0.3$ ms, duty cycle $\leq 10\%$.

3. Derate linearly to 200°C case temperature at the rate of 0.3 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/deg.

*Indicates JEDEC registered data

TYPES 2N5384, 2N5385

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-50	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -90 \text{ V}$, $V_{BE} = 0$		-10	μA
	$V_{CE} = -50 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-500	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -4 \text{ V}$, $I_C = 0$		-1	μA
	$V_{EB} = -6 \text{ V}$, $I_C = 0$		-100	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 5 and 6	20	80	
	$V_{CE} = -4 \text{ V}$, $I_C = -5 \text{ A}$, See Notes 5 and 6	10		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -5 \text{ A}$, See Notes 5 and 6		-1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.2 \text{ A}$, $I_C = -2 \text{ A}$, See Notes 5 and 6		-0.6	V
	$I_B = -1 \text{ A}$, $I_C = -5 \text{ A}$, See Notes 5 and 6		-1.4	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$	20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 15 \text{ MHz}$	2		

NOTES: 5. These parameters must be measured using pulse techniques. $I_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	3.33	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	87.5	

*Indicates JEDEC registered data

TYPES 2N5384, 2N5385 P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -2\text{ A}$, $I_{B(1)} = -150\text{ mA}$, $I_{B(2)} = 150\text{ mA}$,	160	ns
t_{off} Turn-Off Time	$V_{BE(off)} = 2.8\text{ V}$, $R_L = 15\ \Omega$, See Figure 1	550	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

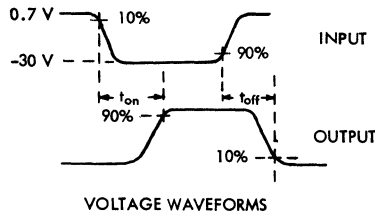
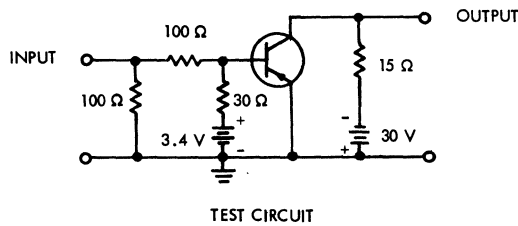


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\ \Omega$, $t_p = 5\ \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPES 2N5384, 2N5385

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGION

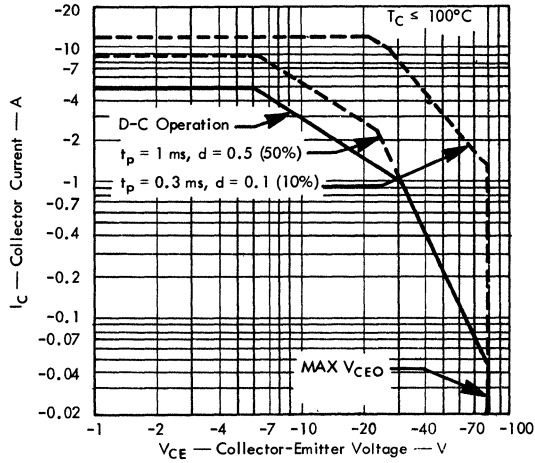


FIGURE 2

THERMAL CHARACTERISTICS

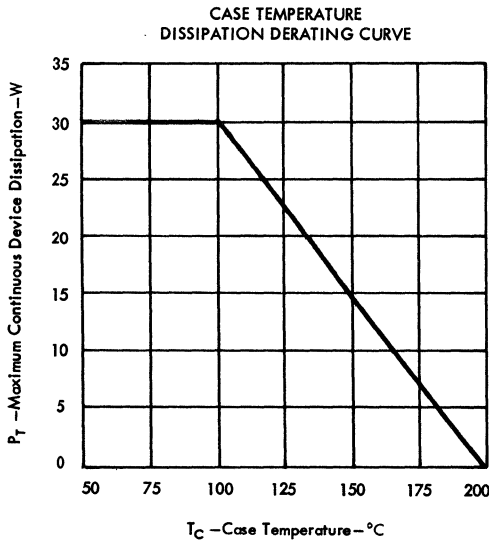


FIGURE 3

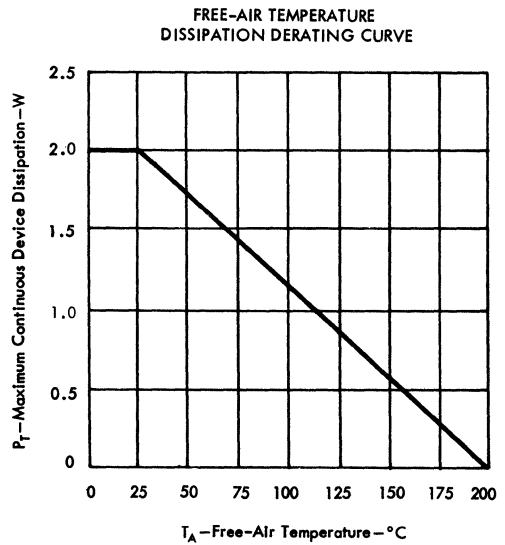


FIGURE 4

TYPE 2N5386

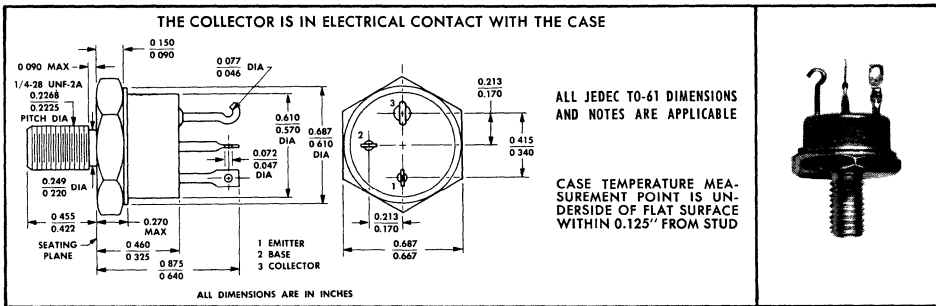
P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

TYPE 2N5386
BULLETIN NO. DL-5 689280, MARCH 1968

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N4301**

- 50 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.6 V at 6 A I_C
- Typ t_{on} of 230 ns at 6 A I_C
- Min f_T of 30 MHz at 10 V, 1 A

***mechanical data**



***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector-Base Voltage	-100 V
Collector-Emitter Voltage (See Note 1)	-80 V
Emitter-Base Voltage	-6 V
Continuous Collector Current	-12 A
Peak Collector Current (See Note 2)	-25 A
Continuous Base Current	-4 A
Continuous Emitter Current	-13 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 2
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	50 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	3.5 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	260°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 20 mW/deg.

*Indicates JEDEC registered data

TYPE 2N5386

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-50	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -90 \text{ V}$, $V_{BE} = 0$		-10	μA
	$V_{CE} = -50 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-500	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -4 \text{ V}$, $I_C = 0$		-5	μA
	$V_{EB} = -6 \text{ V}$, $I_C = 0$		-100	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -6 \text{ A}$, See Notes 5 and 6	20	80	
	$V_{CE} = -4 \text{ V}$, $I_C = -12 \text{ A}$, See Notes 5 and 6	10		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -12 \text{ A}$, See Notes 5 and 6		-1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.6 \text{ A}$, $I_C = -6 \text{ A}$, See Notes 5 and 6		-0.6	V
	$I_B = -2.4 \text{ A}$, $I_C = -12 \text{ A}$, See Notes 5 and 6		-1.4	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$	20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 15 \text{ MHz}$	2		

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	2	deg / W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	50	

*Indicates JEDEC registered data

TYPE 2N5386

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -6 \text{ A}, I_{B(1)} = -400 \text{ mA}, I_{B(2)} = 400 \text{ mA},$ $V_{BE(off)} = 3.6 \text{ V}, R_L = 5 \Omega,$ See Figure 1	230	ns
t_{off} Turn-Off Time		750	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

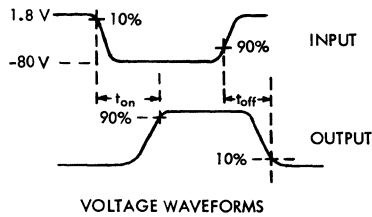
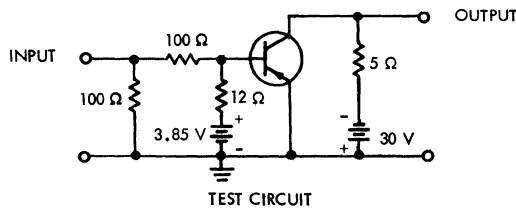


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}, t_f \leq 15 \text{ ns}, Z_{out} = 1.5 \text{ k}\Omega, t_p = 5 \mu\text{s},$ duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}, R_{in} \geq 10 \text{ M}\Omega, C_{in} \leq 11.5 \text{ pF}.$
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPE 2N5386

P-N-P EPITAXIAL PLANAR SILICON POWER TRANSISTOR

MAXIMUM SAFE OPERATING REGION

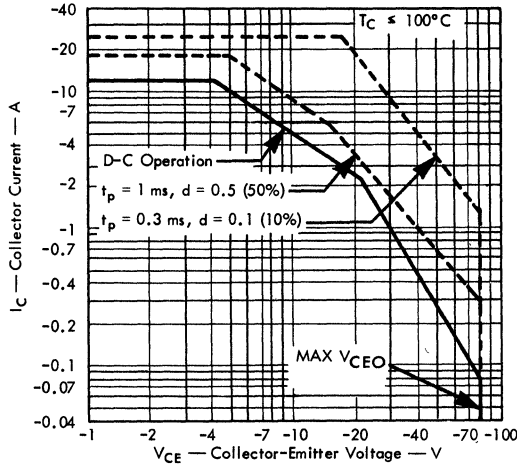


FIGURE 2

THERMAL CHARACTERISTICS

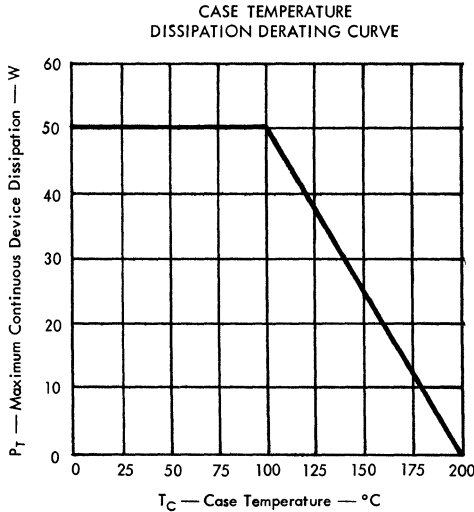


FIGURE 3

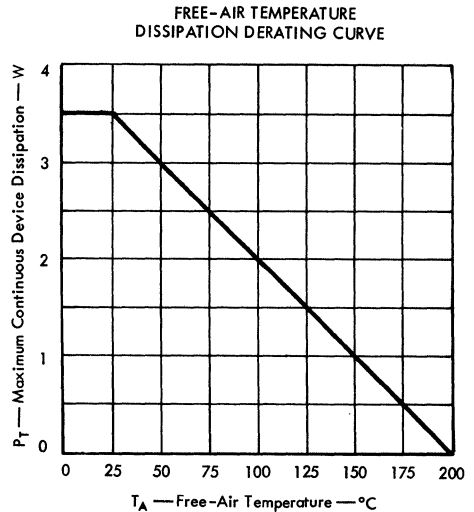


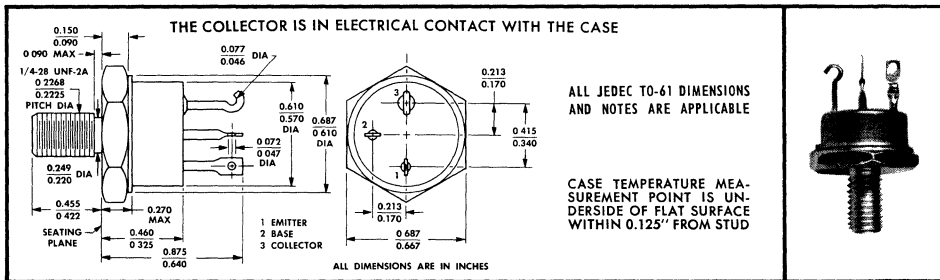
FIGURE 4

TYPES 2N5387, 2N5388, 2N5389 N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER APPLICATIONS

- 200 V, 250 V, 300 V Rated Collector-Emitter Voltages
- 100 Watts at 100°C Case Temperature
- Typ t_{on} of 300 ns at 2 A I_C
- Min f_T of 15 MHz at 10 V, 1 A

*mechanical data



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5387	2N5388	2N5389
Collector-Base Voltage	200 V	250 V	300 V
Collector-Emitter Voltage (See Note 1)	200 V	250 V	300 V
Emitter-Base Voltage	← 10 V →		
Continuous Collector Current	← 7.5 A →		
Peak Collector Current (See Note 2)	← 10 A →		
Continuous Base Current	← 3 A →		
Continuous Emitter Current	← 8 A →		
Safe Operating Region at (or below) 100°C Case Temperature	← See Figure 6 →		
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 100 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →		
Operating Collector Junction Temperature Range	← -65°C to 200°C →		
Storage Temperature Range	← -65°C to 200°C →		
Terminal Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →		

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1 W/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 20 mW/deg.

*Indicates JEDEC registered data



TYPES 2N5387, 2N5388, 2N5389

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5387		2N5388		2N5389		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	200		250		300		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 180 \text{ V}$, $I_B = 0$		30					mA
	$V_{CE} = 225 \text{ V}$, $I_B = 0$				30			
	$V_{CE} = 270 \text{ V}$, $I_B = 0$					30		
I_{CES} Collector Cutoff Current	$V_{CE} = 180 \text{ V}$, $V_{BE} = 0$		1					mA
	$V_{CE} = 225 \text{ V}$, $V_{BE} = 0$				1			
	$V_{CE} = 270 \text{ V}$, $V_{BE} = 0$					1		
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		10					
	$V_{CE} = 125 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$				10			
I_{EBO} Emitter Cutoff Current	$V_{EB} = 8 \text{ V}$, $I_C = 0$		0.1		0.1		0.1	mA
	$V_{EB} = 10 \text{ V}$, $I_C = 0$		1		1		1	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 5 and 6	25	100	25	100	25	100	
	$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 5 and 6	15		15		15		
	$V_{CE} = 5 \text{ V}$, $I_C = 7 \text{ A}$, See Notes 5 and 6	5		5		5		
V_{BE} Base-Emitter Voltage	$V_{CE} = 5 \text{ V}$, $I_C = 7 \text{ A}$, See Notes 5 and 6		2.5		2.5		2.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1 \text{ A}$, $I_C = 5 \text{ A}$, See Notes 5 and 6		2		2		2	V
	$I_B = 1.4 \text{ A}$, $I_C = 7 \text{ A}$, See Notes 5 and 6		2.2		2.2		2.2	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$		20		20		20	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 10 \text{ MHz}$		1.5		1.5		1.5	

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	1	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	50	

*Indicates JEDEC registered data

TYPES 2N5387, 2N5388, 2N5389

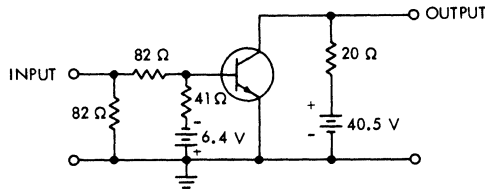
N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

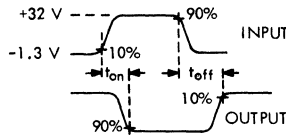
PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 2\text{ A}$, $I_{B(1)} = 200\text{ mA}$, $I_{B(2)} = -200\text{ mA}$	0.3	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -4.7\text{ V}$, $R_L = 20\ \Omega$, See Figure 1	1	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\ \Omega$, $t_p = 10\ \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPES 2N5387, 2N5388, 2N5389

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

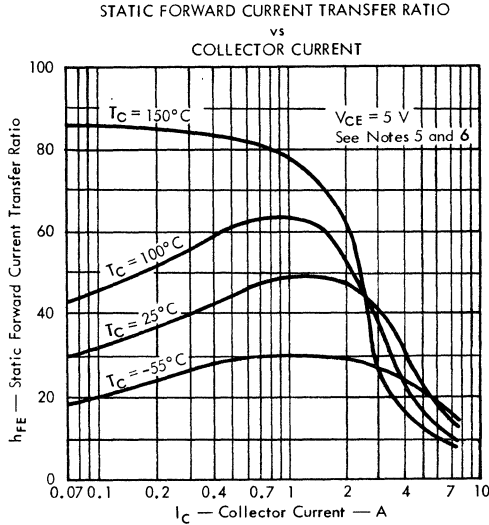


FIGURE 2

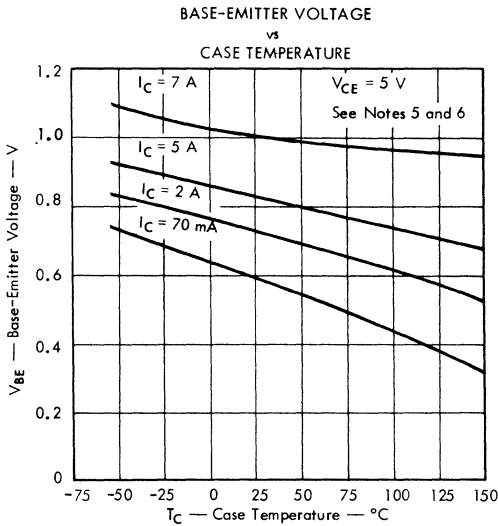


FIGURE 3

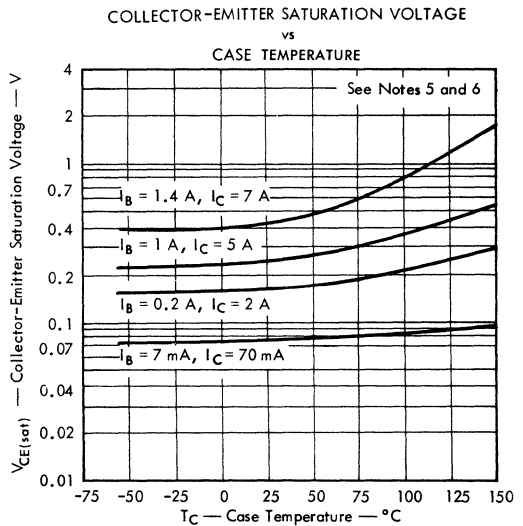


FIGURE 4

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N5387, 2N5388, 2N5389 N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

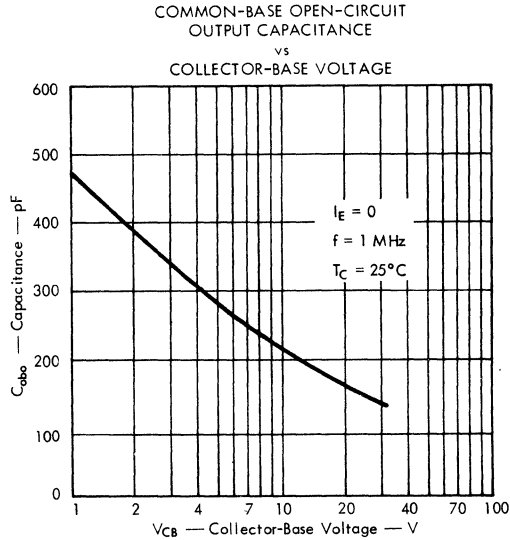


FIGURE 5

MAXIMUM SAFE OPERATING REGION

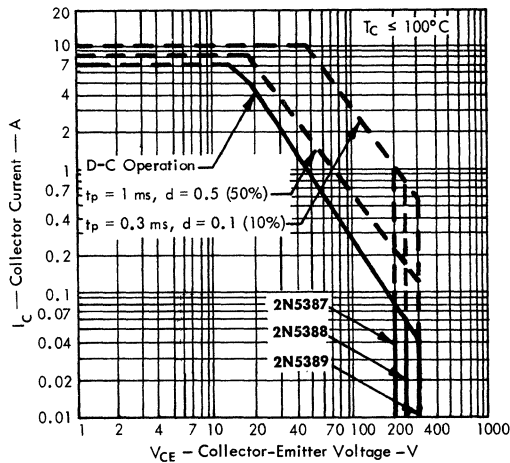


FIGURE 6

TYPES 2N5387, 2N5388, 2N5389

N-P-N TRIPLE-DIFFUSED MESA SILICON POWER TRANSISTORS

5 THERMAL INFORMATION

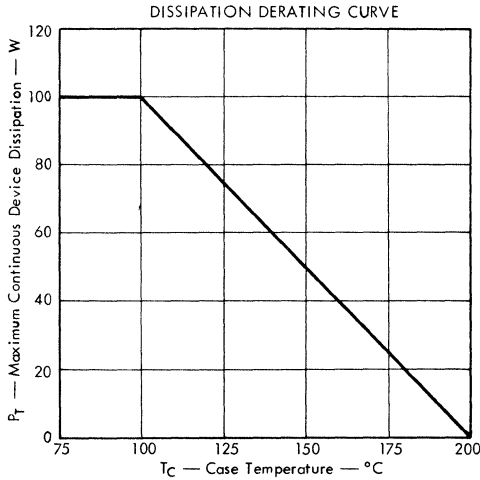


FIGURE 7

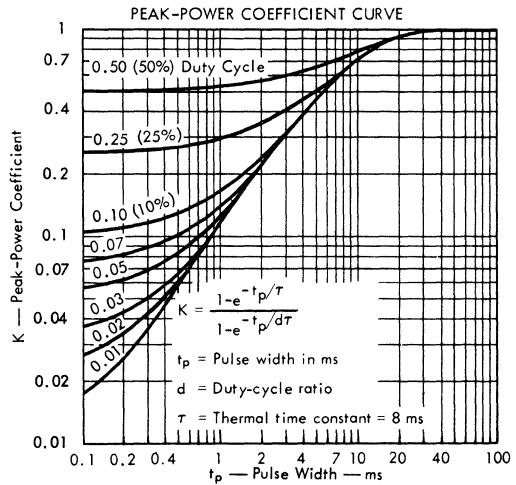


FIGURE 8

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	50	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	1	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	49	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 8	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 4 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C} \text{ as in Figure 7}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Solution:

From Figure 8, Peak-Power Coefficient

$$K = 0.105 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(4) + 0.105(1)} = 296 \text{ W}$$

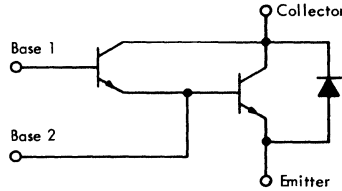
TYPE 2N5390

N-P-N DARLINGTON-CONNECTED PLANAR SILICON POWER TRANSISTOR

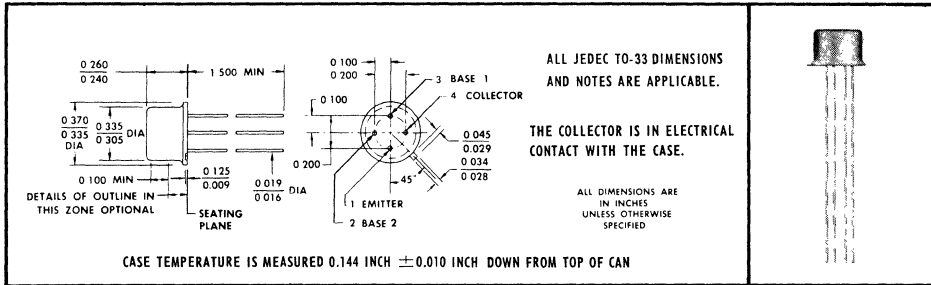
TYPE 2N5390
BULLETIN NO. DL-5 6810670, JULY 1968

- Very High Gain — 1000 Min at 5 A
- High-Speed Switching — 0.3 μ s Typ t_{on}

***device schematic**



***mechanical data**



5

***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector — Base-1 Voltage	120 V
Collector — Emitter Voltage (See Note 1)	80 V
Emitter — Base-1 Voltage	15 V
Continuous Collector Current	2 A
Peak Collector Current (See Note 2)	5 A
Commutating-Diode Current (See Note 3)	-2 A
Continuous Base-One Current	0.1 A
Continuous Base-Two Terminal Current	1 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 7
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 4)	15 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 5)	1 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/8 Inch from Case for 10 Seconds	300°C

- NOTES: 1. This value applies when both base terminals are open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. This applies to the total collector-terminal current when the collector is at negative potential with respect to the emitter.
 4. Derate linearly to 200°C case temperature at the rate of 150 mW/deg.
 5. Derate linearly to 200°C free-air temperature at the rate of 5.71 mW/deg.

*Indicates JEDEC registered data

TYPE 2N5390

N-P-N DARLINGTON-CONNECTED PLANAR SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_{B1} = I_{B2} = 0$, See Note 6	80		V
I_{CES} Collector Cutoff Current	$V_{CE} = 120 \text{ V}$, $V_{B1-E} = V_{B2-E} = 0$		10	μA
	$V_{CE} = 80 \text{ V}$, $V_{B1-E} = V_{B2-E} = 0$, $T_C = 150^\circ\text{C}$		1	mA
I_{EB10} Emitter Cutoff Current	$V_{EB1} = 15 \text{ V}$, $I_C = 0$, $I_{B2} = 0$		10	μA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $I_{B2} = 0$, See Notes 6 and 7		1000	
	$V_{CE} = 5 \text{ V}$, $I_C = 2 \text{ A}$, $I_{B2} = 0$, See Notes 6 and 7	2000	20 000	
	$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$, $I_{B2} = 0$, See Notes 6 and 7	1000		
V_{B1-E} Base-One Emitter Voltage	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $I_{B2} = 0$, See Notes 6 and 7		1.8	V
	$V_{CE} = 5 \text{ V}$, $I_C = 2 \text{ A}$, $I_{B2} = 0$, See Notes 6 and 7	1.1	2.2	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_{B1} = 2 \text{ mA}$, $I_C = 2 \text{ A}$, $I_{B2} = 0$, See Notes 6 and 7		1.4	V
	$I_{B1} = 10 \text{ mA}$, $I_C = 5 \text{ A}$, $I_{B2} = 0$, See Notes 6 and 7		2.5	
$ h_{fo} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $I_{B2} = 0$, $f = 20 \text{ MHz}$		2	
C_{ob10} Common-Base-One Open-Circuit Output Capacitance	$V_{CB1} = 10 \text{ V}$, $I_E = 0$, $I_{B2} = 0$, $f = 1 \text{ MHz}$		100	pF

NOTES: 6. These parameters must be measured using pulse techniques. $I_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*Indicates JEDEC registered data

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	6.67	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	175	deg/W

TYPE 2N5390

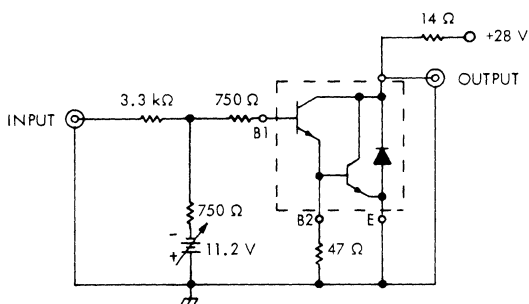
N-P-N DARLINGTON-CONNECTED PLANAR SILICON POWER TRANSISTOR

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 2 \text{ A}$, $I_{B1(1)} = 4 \text{ mA}$, $I_{B1(2)} = -8 \text{ mA}$,	0.3	μS
t_{off} Turn-Off Time	$V_{B1-E(off)} = -10 \text{ V}$, $R_L = 14 \Omega$, See Figure 1	1.5	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

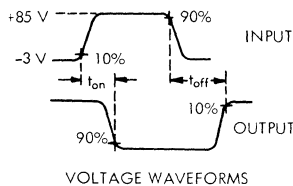


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 1500 \Omega$, $t_p = 5 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.

5

TYPE 2N5390

N-P-N DARLINGTON-CONNECTED PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

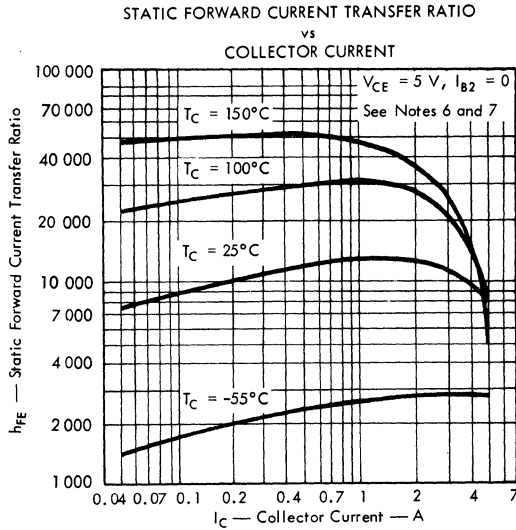


FIGURE 2

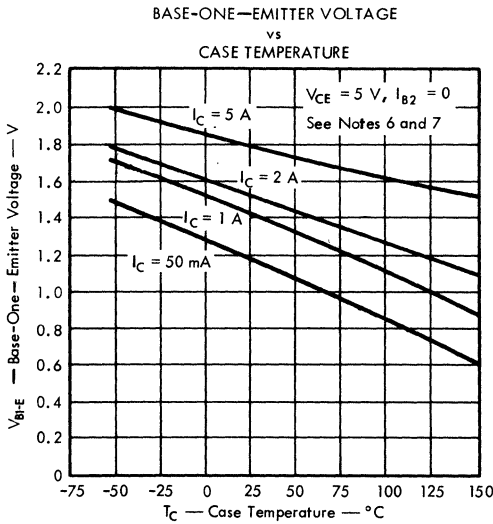


FIGURE 3

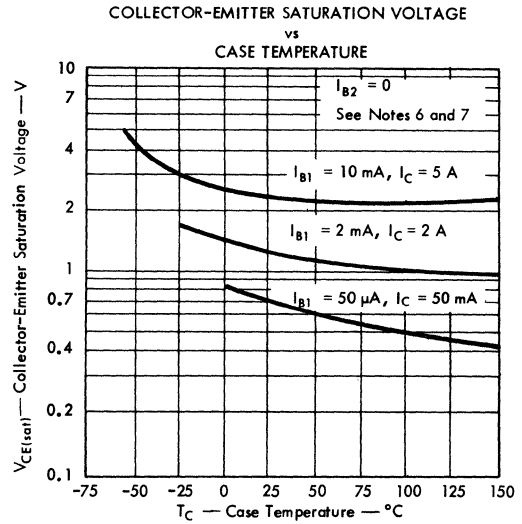


FIGURE 4

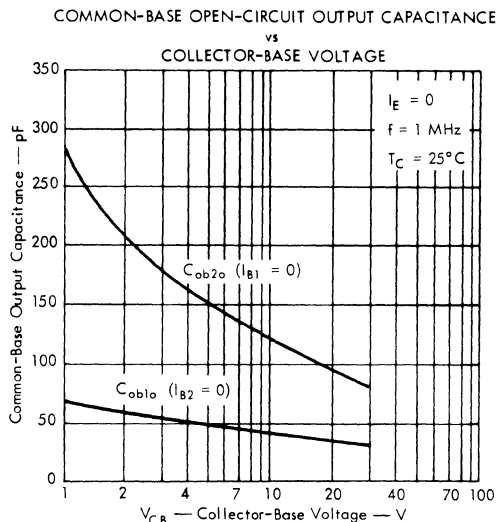
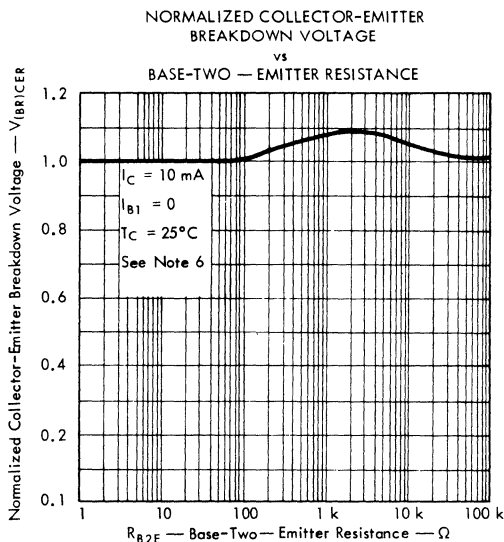
NOTES: 6. These parameters must be measured using pulse techniques. $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

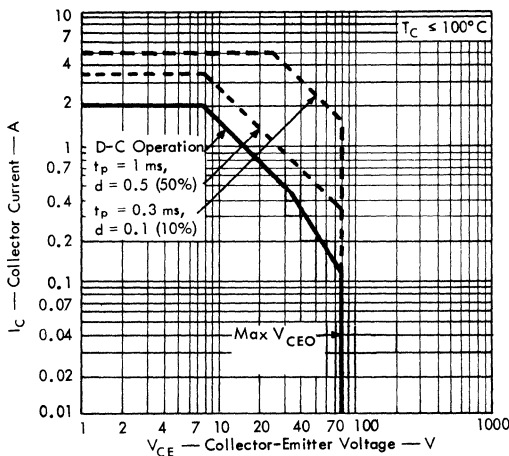
TYPE 2N5390

N-P-N DARLINGTON-CONNECTED PLANAR SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS



MAXIMUM SAFE OPERATING REGION



NOTE 6: This parameter must be measured using pulse techniques: $t_p = 300 \mu s$, duty cycle $\leq 2\%$.

TYPE 2N5390

N-P-N DARLINGTON-CONNECTED PLANAR SILICON POWER TRANSISTOR

THERMAL INFORMATION

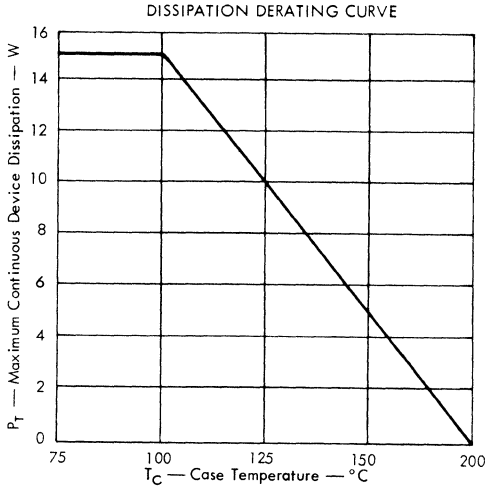


FIGURE 8

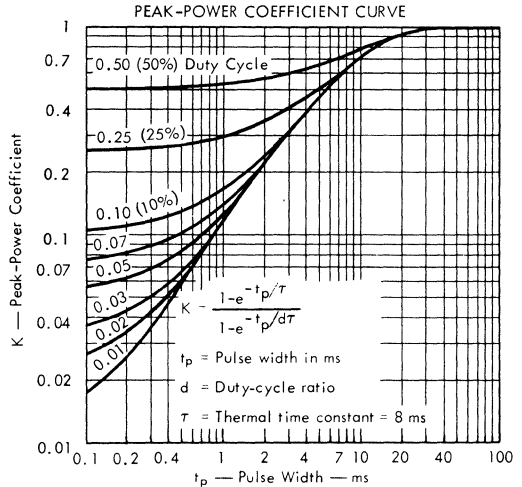


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	6.67	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 200	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200	°C
K	Peak-Power Coefficient	See Figure 9	
t_p	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_p/t_x)		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C} \text{ as in figure 8}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 7 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Solution:

From figure 9, Peak-Power Coefficient

$$K = 0.105 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + 0.105(6.67)} = 107 \text{ W}$$

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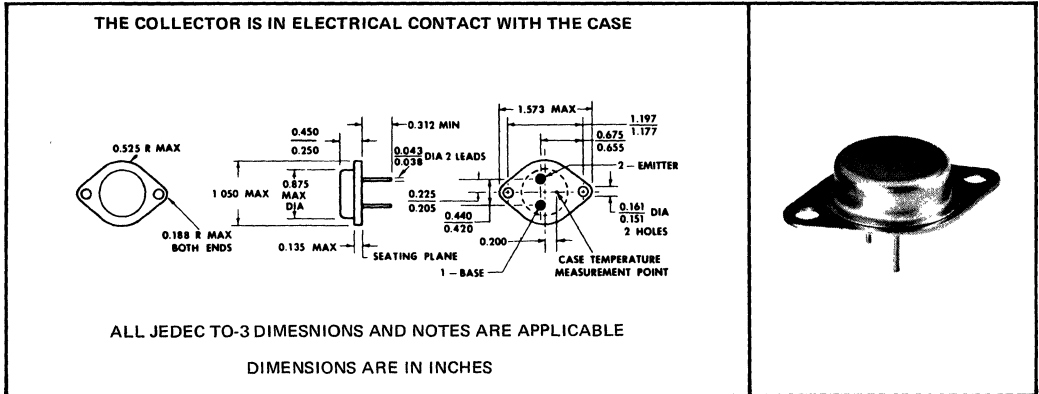
971

TYPES 2N5671, 2N5672 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED SWITCHING APPLICATIONS

- 20 mJ Reverse Energy Rating
- Min $V_{(BR)CEO}$ of 120 V (2N5672)
- Min f_T of 50 MHz at 10 V, 2 A
- 30-A Rated Continuous Collector Current

*mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5671	2N5672
Collector-Emitter Voltage ($V_{BE} = -1.5$ V, See Note 1)	120 V*	150 V*
Collector-Emitter Voltage (Base Open, See Note 1)	90 V	120 V
Emitter-Base Voltage	7 V*	7 V*
Continuous Collector Current	← 30 A* →	
Continuous Base Current	← 10 A* →	
Safe Operating Area at Specified Temperatures	See Figure 6	
Continuous Device Dissipation at (or below) 25°C Case Temperature (see Note 3)	← 140 W* →	
Continuous Device Dissipation at 100°C Case Temperature (see Note 3)	← 80 W* →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (see Note 4)	← 5 W →	
Unclamped Inductive Load Energy (see Note 5)	← 20 mJ* →	
Operating Collector Junction Temperature Range	-65°C to 200°C*	
Storage Temperature Range	-65°C to 200°C*	
Terminal Temperature 1/32 Inch from Case for 10 Seconds	← 230°C* →	

- NOTES: 1. These values apply only when the collector-emitter voltage is applied with the transistor in the off-state with the base-emitter diode reverse-biased or open-circuited, as specified. In operation, the limitations of Figure 6 must be observed.
2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.8 W/°C or refer to Dissipation Derating Curve, Figure 7.
4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C or refer to Dissipation Derating Curve, Figure 8.
5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 5, condition 1. $L = 180 \mu\text{H}$, $R_{BB2} = 20 \Omega$, $V_{BB2} = 4$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V, Energy = $I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N5671, 2N5672
BULLETIN NO. DL-S-7111500, DECEMBER 1971



TYPES 2N5671, 2N5672

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5671		2N5672		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 6	90		120		V
$V_{(BR)CEV}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, See Figure 5 (Condition 2)	120		150		V
I_{CEV} Collector Cutoff Current	$V_{CE} = 110 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		12			mA
	$V_{CE} = 135 \text{ V}$, $V_{BE} = -1.5 \text{ V}$				10	
	$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		15		10	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 7 \text{ V}$, $I_C = 0$		10		10	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 6 and 7	20	100	20	100	
V_{BE} Base-Emitter Voltage	$I_B = 1.2 \text{ A}$, $I_C = 15 \text{ A}$, See Notes 6 and 7		1.5		1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1.2 \text{ A}$, $I_C = 15 \text{ A}$, See Notes 6 and 7		0.75		0.75	V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 2 \text{ A}$, $f = 5 \text{ MHz}$	10		10		

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MAX	UNIT
t_r Rise Time	$I_C \approx 15 \text{ A}$, $I_B(1) = 1.2 \text{ A}$, $I_B(2) \approx -1.2 \text{ A}$, $V_{BE(off)} = -6 \text{ V}$, $R_L = 2 \Omega$, See Figure 4	0.5	μs
t_s Storage Time		1.5	
t_f Fall Time		0.5	

*JEDEC registered data

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
VS
COLLECTOR CURRENT

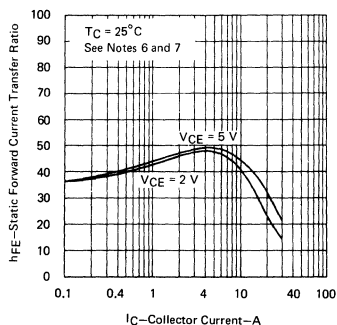


FIGURE 1

BASE-EMITTER VOLTAGE
VS
COLLECTOR CURRENT

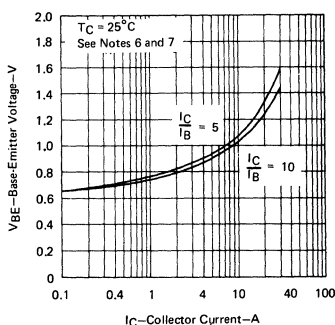


FIGURE 2

COLLECTOR-EMITTER SATURATION VOLTAGE
VS
COLLECTOR CURRENT

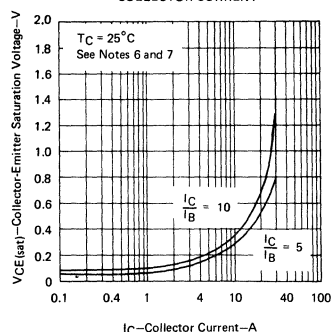


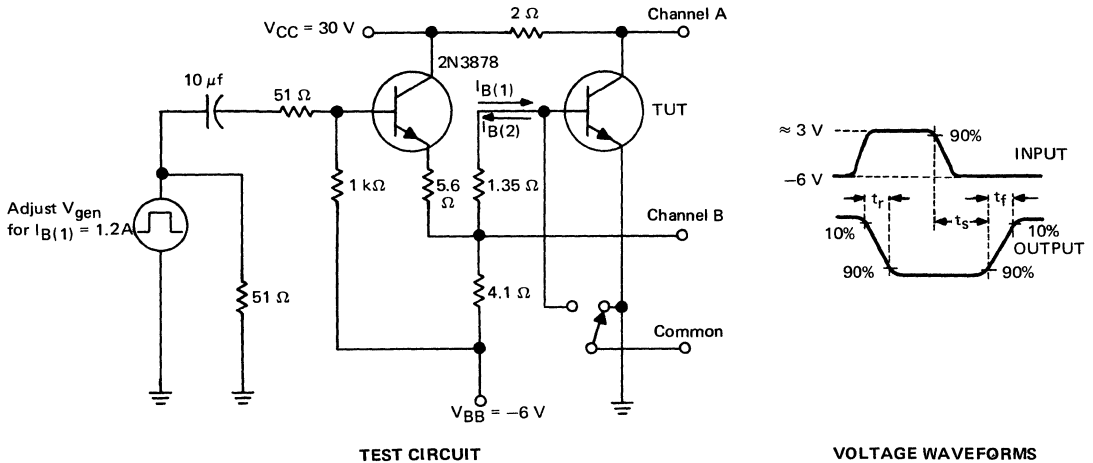
FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N5671, 2N5672 N-P-N SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 20$ ns, $t_f \leq 20$ ns, $t_w = 5$ μ s, duty cycle = 0.2%.
 B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 C. Resistor must be noninductive types.
 D. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 4

INDUCTIVE LOAD SWITCHING

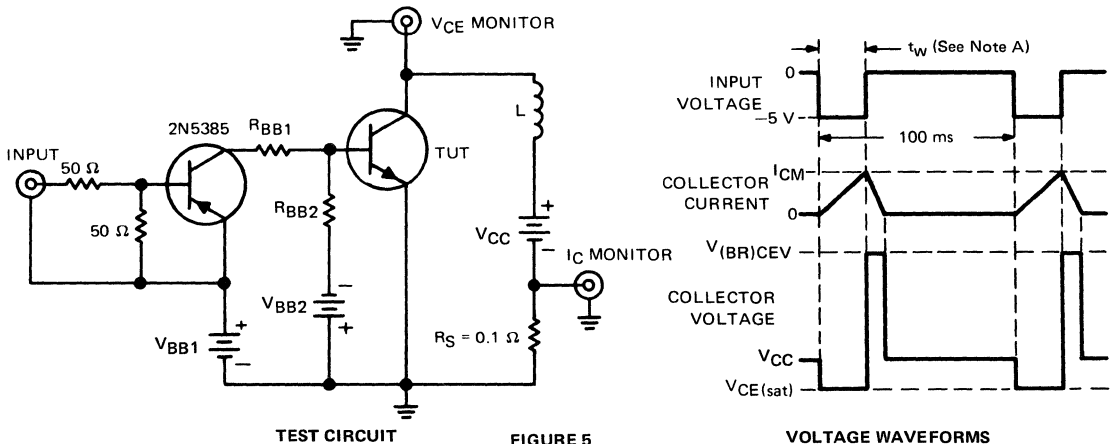


FIGURE 5

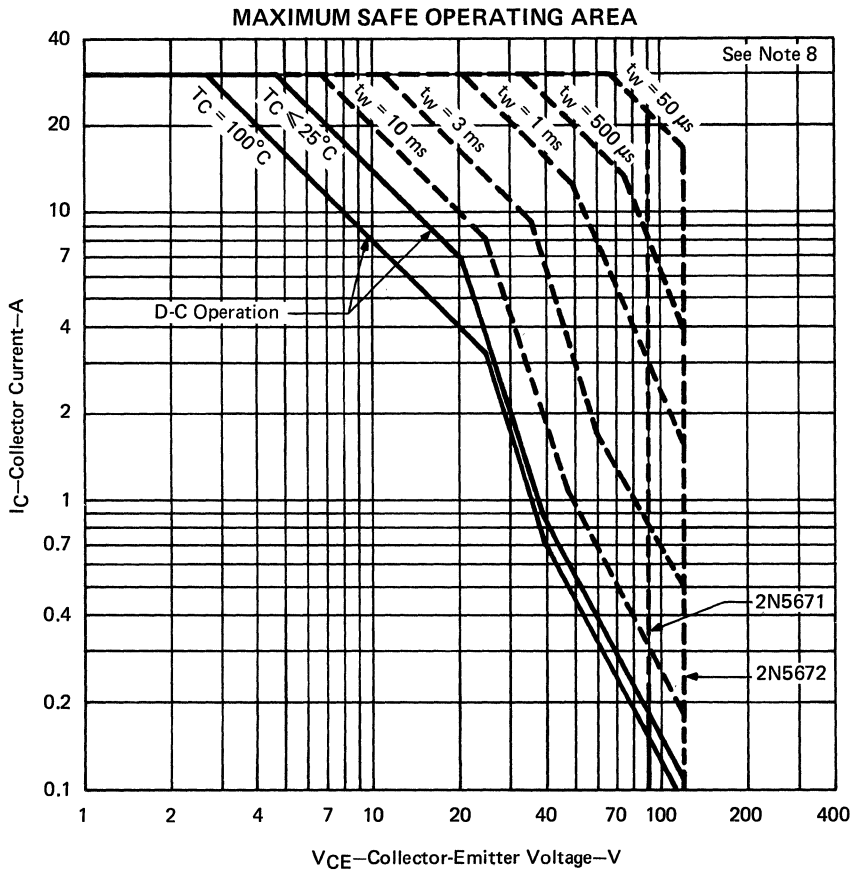
CIRCUIT CONDITIONS

CONDITION	R_{BB1}	R_{BB2}	V_{BB1}	V_{BB2}	V_{CC}	I_{CM}	L	t_w	DUTY CYCLE
1	8.2 Ω	20 Ω	10 V	4 V	10 V	15 A	0.18 mH†	0.3 ms	5%
2	110 Ω	50 Ω	6 V	1.5 V	50 V	0.2 A	2 mH	8 ms	50%

NOTE A: Input pulse width is increased until $I_C = I_{CM}$. † $Q = 86$ at 1.4 MHz.

TYPES 2N5671, 2N5672

N-P-N SILICON POWER TRANSISTORS



NOTE 8: Areas defined by dashed lines apply for nonrepetitive-pulse operation at $T_C \leq 25^\circ\text{C}$. The pulse may be repeated after the device has regained thermal equilibrium.

FIGURE 6

THERMAL INFORMATION

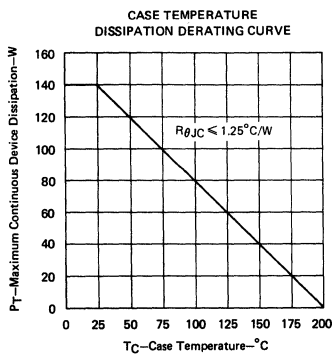


FIGURE 7

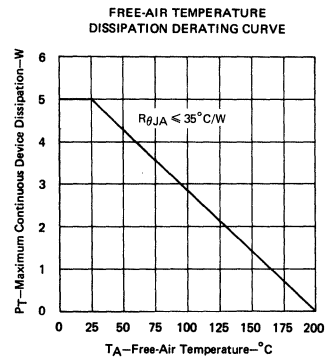


FIGURE 8

TYPES 2N5683, 2N5684

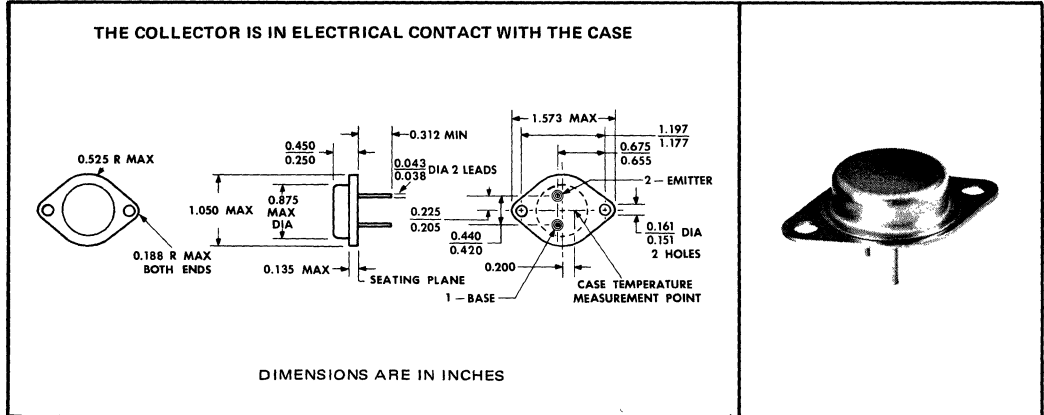
P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5685, 2N5686

- 300 Watts at 25°C Case Temperature
- 50-A Rated Continuous Collector Current
- Min f_T of 2 MHz at 10 V, 5 A

***mechanical data**

The case outline falls within JEDEC-TO-3 except for lead diameter.



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5683	2N5684
*Collector-Base Voltage	-60 V	-80 V
*Collector-Emitter Voltage (See Note 1)	-60 V	-80 V
*Emitter-Base Voltage	-5 V	-5 V
*Continuous Collector Current	←-50 A	←-50 A
*Continuous Base Current	←-15 A	←-15 A
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	←-300 W	←-300 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	←-5 W	←-5 W
*Operating Collector Junction Temperature Range	-65°C to 200°C	-65°C to 200°C
*Storage Temperature Range	-65°C to 200°C	-65°C to 200°C
*Terminal Temperature 1/16 Inch from Case for 10 Seconds	←-235°C	←-235°C

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. Derate linearly to 200°C case temperature at the rate of 1.715 W/°C or refer to Dissipation Derating Curve, Figure 1.
 3. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C or refer to Dissipation Derating Curve, Figure 2.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N5683, 2N5684
BULLETIN NO. D.L.S-7111990, DECEMBER 1971



TYPES 2N5683, 2N5684

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5683		2N5684		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ mA}$, $I_B = 0$, See Note 6	-60		-80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$		-1			mA
	$V_{CE} = -40 \text{ V}$, $I_B = 0$				-1	
I_{CEV} Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 1.5 \text{ V}$		-2			mA
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 1.5 \text{ V}$				-2	
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		-10			
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$				-10	
I_{CBO} Collector Cutoff Current	$V_{CB} = -60 \text{ V}$, $I_E = 0$		-2			mA
	$V_{CB} = -80 \text{ V}$, $I_E = 0$				-2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$		-5		-5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ V}$, $I_C = -25 \text{ A}$	15	60	15	60	
	$V_{CE} = -5 \text{ V}$, $I_C = -50 \text{ A}$	5		5		
V_{BE} Base-Emitter Voltage	$I_B = -2.5 \text{ A}$, $I_C = -25 \text{ A}$		-2		-2	V
	$V_{CE} = -2 \text{ V}$, $I_C = -25 \text{ A}$		-2		-2	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -2.5 \text{ A}$, $I_C = -25 \text{ A}$		-1		-1	V
	$I_B = -10 \text{ A}$, $I_C = -50 \text{ A}$		-5		-5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -10 \text{ A}$, $f = 1 \text{ kHz}$	15		15		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -5 \text{ A}$, $f = 1 \text{ MHz}$	2		2		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 0.1 \text{ MHz}$	2000		2000		pF

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

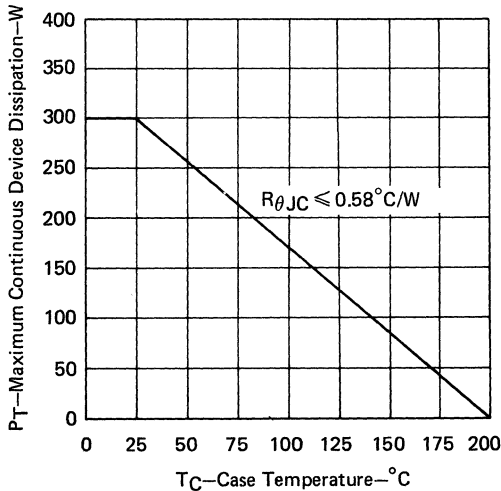


FIGURE 1

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

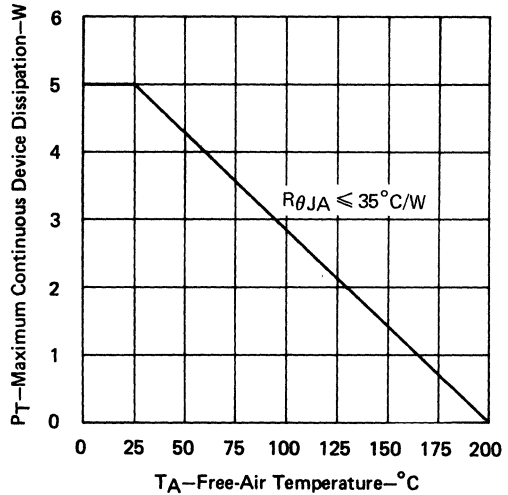


FIGURE 2

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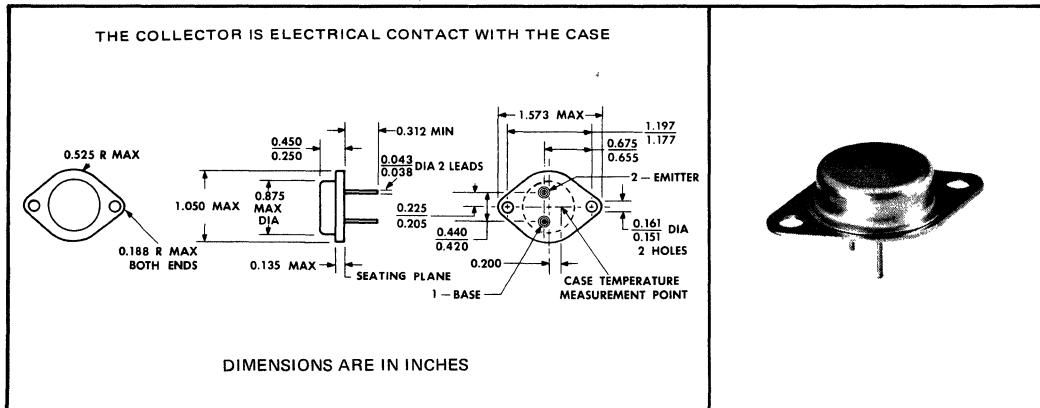
TYPES 2N5685, 2N5686 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5683, 2N5684

- 300 Watts at 25°C Case Temperature
- 50-A Rated Continuous Collector Current
- Min f_T of 2 MHz at 10 V, 5 A

***mechanical data**

The case outline falls within JEDEC-TO-3 except for lead diameter.



TYPES 2N5685, 2N5686
BULLETIN NO. DL-S-7111591, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5685	2N5686
*Collector-Base Voltage	60 V	80 V
*Collector-Emitter Voltage (See Note 1)	60 V	80 V
*Emitter-Base Voltage	5 V	5 V
*Continuous Collector Current	← 50 A →	
*Continuous Base Current	← 15 A →	
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 300 W →	
*Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	← 5 W →	
*Operating Collector Junction Temperature Range	-65°C to 200°C	
*Storage Temperature Range	-65°C to 200°C	
*Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →	

NOTES: 1. These values apply when the base-emitter diode is open-circuited.
2. Derate linearly to 200°C case temperature at the rate of 1.715 W/°C or refer to Dissipation Derating Curve, Figure 1.
3. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C or refer to Dissipation Derating Curve, Figure 2.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N5685, 2N5686

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

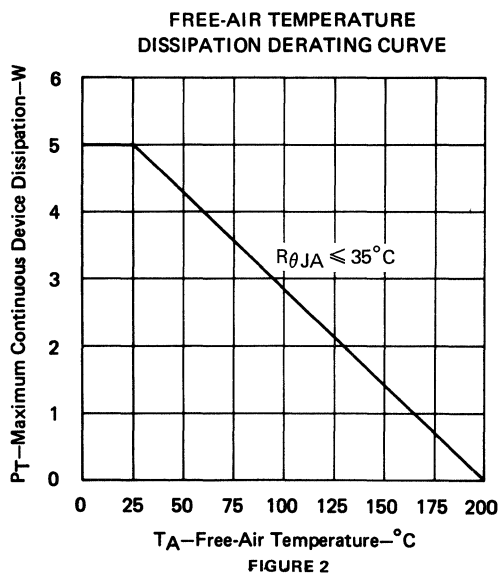
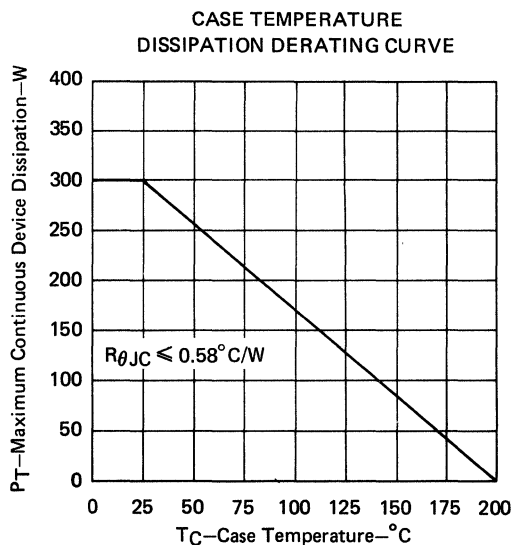
*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5685		2N5686		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 6	60		80		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$ $V_{CE} = 40 \text{ V}$, $I_B = 0$		1		1	mA
I_{CEV} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		2			mA
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$				2	
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		10			
	$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$				10	
I_{CBO} Collector Cutoff Current	$V_{CB} = 60 \text{ V}$, $I_E = 0$		2			mA
	$V_{CB} = 80 \text{ V}$, $I_E = 0$				2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		5		5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 25 \text{ A}$	15	60	15	60	
	$V_{CE} = 5 \text{ V}$, $I_C = 50 \text{ A}$	5		5		
V_{BE} Base-Emitter Voltage	$I_B = 2.5 \text{ A}$, $I_C = 25 \text{ A}$		2		2	V
	$V_{CE} = 2 \text{ V}$, $I_C = 25 \text{ A}$		2		2	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 2.5 \text{ A}$, $I_C = 25 \text{ A}$		1		1	V
	$I_B = 10 \text{ A}$, $I_C = 50 \text{ A}$		5		5	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 10 \text{ A}$, $f = 1 \text{ kHz}$	15		15		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ A}$, $f = 1 \text{ MHz}$	2		2		
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 0.1 \text{ MHz}$		1200		1200	pF

NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

THERMAL INFORMATION



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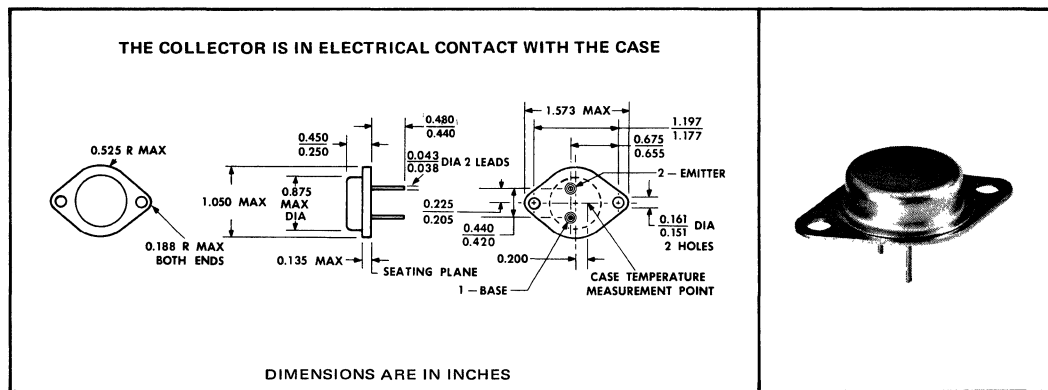
TYPES 2N5758, 2N5759, 2N5760 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
RECOMMENDED FOR COMPLEMENTARY USE WITH TIP544, TIP545, TIP546

- 150 W at 25°C Case Temperature
- 6-A Rated Continuous Collector Current
- Min f_T of 1 MHz at 20 V, 0.5 A

***mechanical data**

The case outline falls within JEDEC TO-3.



TYPES 2N5758, 2N5759, 2N5760
BULLETIN NO. DLS-7211804, JANUARY 1972

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5758	2N5759	2N5760
*Collector-Base Voltage	100 V	120 V	140 V
*Collector-Emitter Voltage (See Note 1)	100 V	120 V	140 V
*Emitter-Base Voltage	7 V	7 V	7 V
*Continuous Collector Current	← 6 A →		
*Peak Collector Current (See Note 2)	← 10 A →		
*Continuous Base Current	← 4 A →		
*Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →		
*Operating Collector Junction Temperature Range	-65°C to 200°C		
*Storage Temperature Range	-65°C to 200°C		
*Terminal Temperature 1/16 Inch from Case for 10 Seconds.	← 235°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.857 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N5758, 2N5759, 2N5760

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5758		2N5759		2N5760		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 5	100		120		140		V
I_{CBO} Collector Cutoff Current	$V_{CB} = 100 \text{ V}$, $I_E = 0$	1						mA
	$V_{CB} = 120 \text{ V}$, $I_E = 0$			1				
	$V_{CB} = 140 \text{ V}$, $I_E = 0$					1		
I_{CEO} Collector Cutoff Current	$V_{CE} = 50 \text{ V}$, $I_B = 0$	1						mA
	$V_{CE} = 60 \text{ V}$, $I_B = 0$			1				
	$V_{CE} = 70 \text{ V}$, $I_B = 0$					1		
I_{CEV} Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	1						mA
	$V_{CE} = 120 \text{ V}$, $V_{BE} = -1.5 \text{ V}$			1				
	$V_{CE} = 140 \text{ V}$, $V_{BE} = -1.5 \text{ V}$					1		
	$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	5						
	$V_{CE} = 120 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$			5				
$V_{CE} = 140 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$					5			
I_{EBO} Emitter Cutoff Current	$V_{EB} = 7 \text{ V}$, $I_C = 0$	1		1	1	1	1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 2 \text{ V}$, $I_C = 3 \text{ A}$	25 100		20 80	15 60			
	$V_{CE} = 2 \text{ V}$, $I_C = 6 \text{ A}$	5		5	5			
V_{BE} Base-Emitter Voltage	$V_{CE} = 2 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 5 and 6	1.5		1.5	1.5			V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.3 \text{ A}$, $I_C = 3 \text{ A}$	1		1	1			V
	$I_B = 1.2 \text{ A}$, $I_C = 6 \text{ A}$	2		2	2			
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 2 \text{ A}$, $f = 1 \text{ kHz}$	15		15	15			
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 20 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 0.5 \text{ MHz}$	2		2	2			
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 0.1 \text{ MHz}$	300		300	300			pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from device body.

*JEDEC registered data

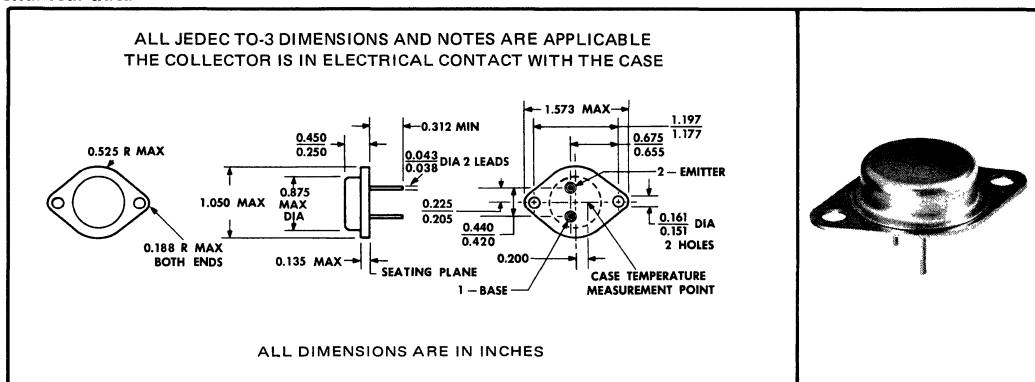
TYPES 2N5867, 2N5868 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5869, 2N5870

- 87.5 Watts at 25°C Case Temperature
- 5-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 0.25 A
- 62.5-mJ Reverse Energy Rating

TYPES 2N5867, 2N5868
BULLETIN NO. DL-S-7111592, DECEMBER 1971

***mechanical data**



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5867	2N5868
Collector-Base Voltage	-60 V*	-80 V*
Collector-Emitter Voltage (See Note 1)	-60 V*	-80 V*
Emitter-Base Voltage	-5 V*	-5 V*
Continuous Collector Current		
Peak Collector Current (See Note 2)		
Continuous Base Current		
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)		
Unclamped Inductive Load Energy (See Note 5)		
Operating Collector Junction Temperature Range	-65°C to 200°C*	
Storage Temperature Range	-65°C to 200°C*	
Terminal Temperature 1/16 Inch from Case for 10 Seconds		

NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 mW/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $L = 20$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = -2.5$ A, Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

[†]Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

[‡]This circuit appears on page 5-1 of this data book.

TYPES 2N5867, 2N5868

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

* electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5867		2N5868		UNIT
		MIN	MAX	MIN	MAX	
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = -100 mA, I _B = 0, See Note 6	-60		-80		V
I _{CEO} Collector Cutoff Current	V _{CE} = -30 V, I _B = 0 V _{CE} = -40 V, I _B = 0	-0.5		-0.5		mA
I _{CEV} Collector Cutoff Current	V _{CE} = -60 V, V _{BE} = 1.5 V	-0.1				mA
	V _{CE} = -80 V, V _{BE} = 1.5 V			-0.1		
	V _{CE} = -60 V, V _{BE} = 1.5 V, T _C = 150°C V _{CE} = -80 V, V _{BE} = 1.5 V, T _C = 150°C			-2		
I _{CBO} Collector Cutoff Current	V _{CB} = -60 V, I _E = 0 V _{CB} = -80 V, I _E = 0	-0.1		-0.1		mA
I _{EBO} Emitter Cutoff Current	V _{EB} = -5 V, I _C = 0	-1		-1		mA
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -300 mA	35		35		
	V _{CE} = -4 V, I _C = -1.5 A	20	100	20	100	
	V _{CE} = -4 V, I _C = -3 A	5		5		
V _{BE} Base-Emitter Voltage	I _B = -200 mA, I _C = -2 A			-1.6		V
	V _{CE} = -4 V, I _C = -3 A			-2		
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = -200 mA, I _C = -2 A			-1		V
	I _B = -0.6 A, I _C = -3 A			-2		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -0.25 A, f = 1 kHz	20		20		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -10 V, I _C = -0.25 A, f = 1 MHz	4		4		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = -10 V, I _E = 0, f = 1 MHz	200		200		pF

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

* switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = -1.5 A, I _B (1) = -0.15 A, I _B (2) = 0.15 A, V _{BE(off)} = 5 V, R _L = 20 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

* JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡ V_{BB1} = 25 V, V_{BB2} = 5 V, V_{CC} = 30 V, V_{on} = -23 V, R_{BB1} = 73 Ω, R_{BB2} = 39 Ω.

‡ This circuit appears on page 5-1 of this data book.

MAXIMUM SAFE OPERATING AREA

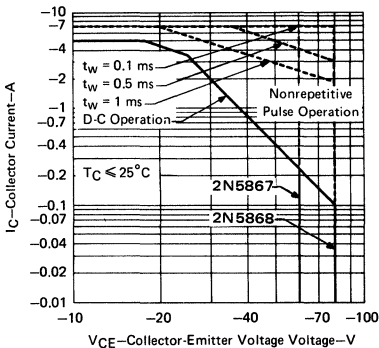


FIGURE 1

THERMAL CHARACTERISTICS

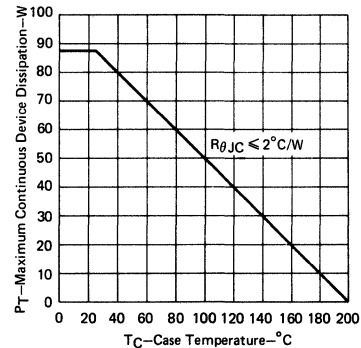


FIGURE 2

TYPES 2N5869, 2N5870

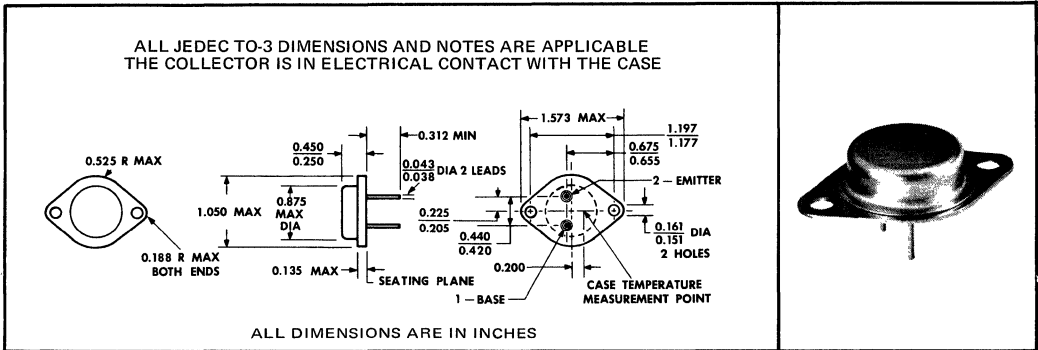
N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

 TYPES 2N5869, 2N5870
 BULLETIN NO. DLS-7111622, DECEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
 DESIGNED FOR COMPLEMENTARY USE WITH 2N5867, 2N5868

- 87.5 Watts at 25°C Case Temperature
- 5-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 0.25 A
- 62.5-mJ Reverse Energy Rating

*mechanical data


5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5869	2N5870
Collector-Base Voltage	60 V*	80 V*
Collector-Emitter Voltage (See Note 1)	60 V*	80 V*
Emitter-Base Voltage	5 V*	5 V*
Continuous Collector Current		
Peak Collector Current (See Note 2)		
Continuous Base Current		
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)		
Unclamped Inductive Load Energy (See Note 5)		
Operating Collector Junction Temperature Range		
Storage Temperature Range		
Terminal Temperature 1/16 Inch from Case for 10 Seconds		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 mW/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $L = 20$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = 2.5$ A. Energy $\approx I_C^2 L / 2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

[†]Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

[‡]This circuit appears on page 5-1 of this data book.

TYPES 2N5869, 2N5870

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5869		2N5870		UNIT
		MIN	MAX	MIN	MAX	
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = 100 mA, I _B = 0, See Note 6	60		80		V
I _{CEO} Collector Cutoff Current	V _{CE} = 30 V, I _B = 0 V _{CE} = 40 V, I _B = 0	0.5		0.5		mA
I _{CEV} Collector Cutoff Current	V _{CE} = 60 V, V _{BE} = -1.5 V	0.1				mA
	V _{CE} = 80 V, V _{BE} = -1.5 V			0.1		
	V _{CE} = 60 V, V _{BE} = -1.5 V, T _C = 150°C V _{CE} = 80 V, V _{BE} = -1.5 V, T _C = 150°C	2		2		
I _{CBO} Collector Cutoff Current	V _{CB} = 60 V, I _E = 0	0.1				mA
	V _{CB} = 80 V, I _E = 0			0.1		
I _{EBO} Emitter Cutoff Current	V _{EB} = 5 V, I _C = 0	1		1		mA
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 300 mA	35		35		
	V _{CE} = 4 V, I _C = 1.5 A	20	100	20	100	
	V _{CE} = 4 V, I _C = 3 A	5		5		
V _{BE} Base-Emitter Voltage	I _B = 200 mA, I _C = 2 A	1.6		1.6		V
	V _{CE} = 4 V, I _C = 3 A	2		2		
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 200 mA, I _C = 2 A	1		1		V
	I _B = 0.6 A, I _C = 3 A	2		2		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 0.25 A, f = 1 kHz	20		20		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 0.25 A, f = 1 MHz	4		4		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 1 MHz	150		150		pF

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = 1.5 A, I _{B(1)} = 0.15 A, I _{B(2)} = -0.15 A, V _{BE(off)} = -5 V, R _L = 20 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡ V_{BB1} = 25 V, V_{BB2} = 5 V, V_{CC} = 30 V, V_{on} = 23 V, R_{BB1} = 73 Ω, R_{BB2} = 39 Ω.

‡This circuit appears on page 5-1 of this data book.

MAXIMUM SAFE OPERATING AREA

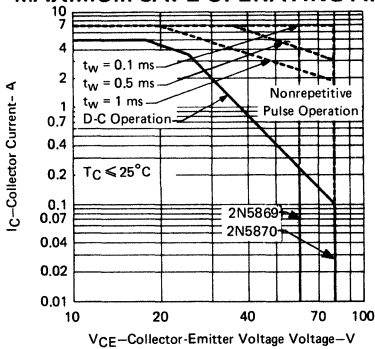


FIGURE 1

THERMAL CHARACTERISTICS

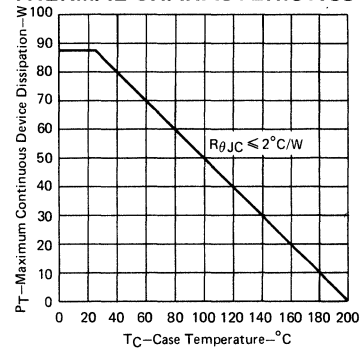


FIGURE 2

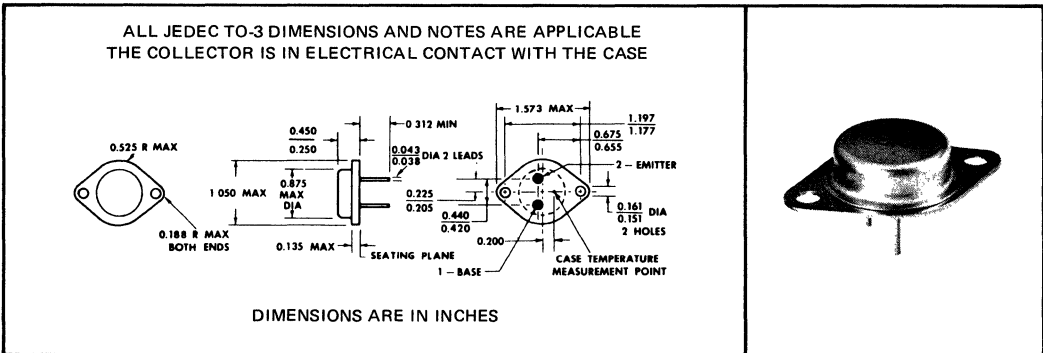
TYPES 2N5871, 2N5872

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5873, 2N5874

- 115 Watts at 25°C Case Temperature
- 7-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 0.25 A
- 62.5-mJ Reverse Energy Rating

*mechanical data



TYPES 2N5871, 2N5872
BULLETIN NO. DL-S-7111597, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5871	2N5872
Collector-Base Voltage	-60 V*	-80 V*
Collector-Emitter Voltage (See Note 1)	-60 V*	-80 V*
Emitter-Base Voltage	-5 V*	-5 V*
Continuous Collector Current	← { -7 A† } → ← { -5 A* } →	
Peak Collector Current (See Note 2)	← -10 A →	
Continuous Base Current	← -1.5 A* →	
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 115 W* →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →	
Operating Collector Junction Temperature Range	-65°C to 200°C*	
Storage Temperature Range	-65°C to 200°C*	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 250°C* →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.66 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. † L = 20 mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = -2.5$ A. Energy $\approx I_C^2 L / 2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.
 †Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.
 ‡This circuit appears on page 5-1 of this data book.

TYPES 2N5871, 2N5872

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5871		2N5872		UNIT
		MIN	MAX	MIN	MAX	
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = -0.1 A, I _B = 0, See Note 6	-60		-80		V
ICEO Collector Cutoff Current	VCE = -30 V, I _B = 0		-0.5			mA
	VCE = -40 V, I _B = 0				-0.5	
ICEV Collector Cutoff Current	VCE = -60 V, VBE = 1.5 V		-0.25			mA
	VCE = -80 V, VBE = 1.5 V				-0.25	
	VCE = -60 V, VBE = 1.5 V, T _C = 150°C		-2			
	VCE = -80 V, VBE = 1.5 V, T _C = 150°C				-2	
ICBO Collector Cutoff Current	VCB = -60 V, I _E = 0		-0.25			mA
	VCB = -80 V, I _E = 0				-0.25	
IEBO Emitter Cutoff Current	VEB = -5 V, I _C = 0		-1		-1	mA
	VCE = -4 V, I _C = -0.5 A		35		35	
hFE Static Forward Current Transfer Ratio	VCE = -4 V, I _C = -2.5 A	See Notes 6 and 7	20	100	20	100
	VCE = -4 V, I _C = -5 A		5		5	
	I _B = -0.4 A, I _C = -4 A					
VBE Base-Emitter Voltage	I _B = -0.4 A, I _C = -4 A	See Notes 6 and 7		-1.6		-1.6
	VCE = -4 V, I _C = -5 A			-2		-2
VCE(sat) Collector-Emitter Saturation Voltage	I _B = -0.4 A, I _C = -4 A	See Notes 6 and 7		-1		-1
	I _B = -1 A, I _C = -5 A			-2		-2
hfe Small-Signal Common-Emitter Forward Current Transfer Ratio	VCE = -4 V, I _C = -0.5 A, f = 1 kHz		20		20	
hfe Small-Signal Common-Emitter Forward Current Transfer Ratio	VCE = -10 V, I _C = -0.25 A, f = 1 MHz		4		4	
Cobo Common-Base Open-Circuit Output Capacitance	VCB = -10 V, I _E = 0, f = 1 MHz		300		300	pF

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = -2.5 A, I _B (1) = -0.25 A, I _B (2) = 0.25 A, VBE(off) = 4.6 V, R _L = 12 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[‡] V_{BB1} = 24 V, V_{BB2} = 4.6 V, V_{CC} = 30 V, V_{on} = 22.5 V, R_{BB1} = 43 Ω, R_{BB2} = 22 Ω.

‡ This circuit appears on page 5-1 of this data book.

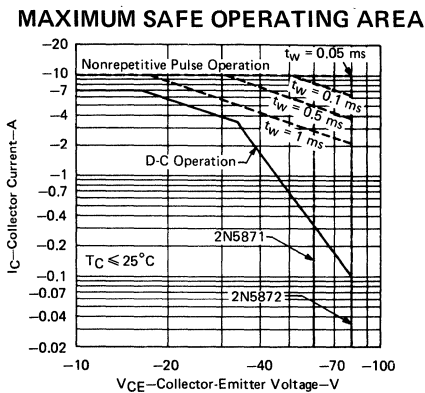


FIGURE 1

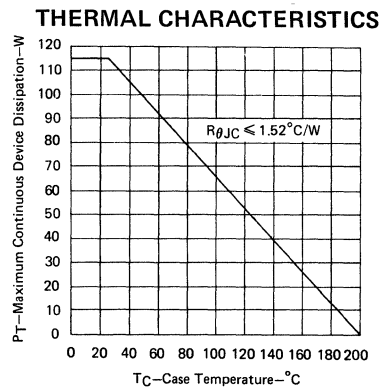


FIGURE 2

TYPES 2N5873, 2N5874

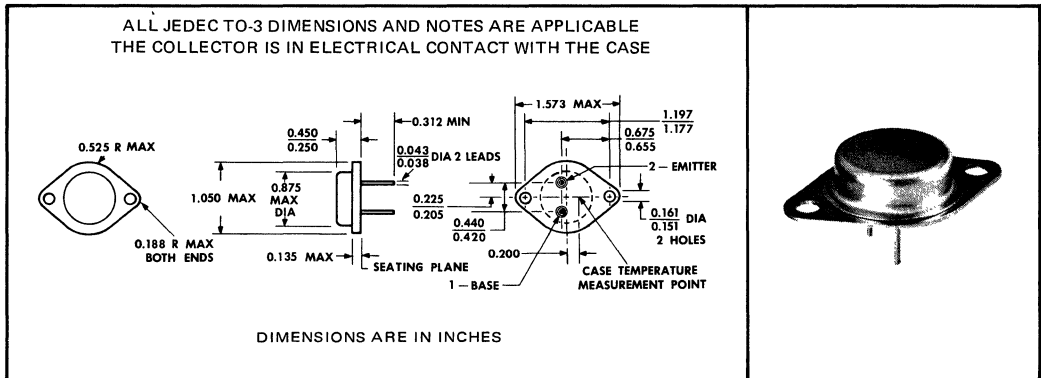
N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

 TYPES 2N5873, 2N5874
 BULLETIN NO. DL-S-7111623, DECEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
 DESIGNED FOR COMPLEMENTARY USE WITH 2N5871, 2N5872

- 115 Watts at 25°C Case Temperature
- 7-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 0.25 A
- 62.5-mJ Reverse Energy Rating

*mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5873	2N5874	
Collector-Base Voltage	60 V*	80 V*	
Collector-Emitter Voltage (See Note 1)	60 V*	80 V*	
Emitter-Base Voltage	5 V*	5 V*	
Continuous Collector Current			
Peak Collector Current (See Note 2)			
Continuous Base Current			
Safe Operating Area at (or below) 25°C Case Temperature			See Figure 1
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)			115 W*
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)			5 W
Unclamped Inductive Load Energy (See Note 5)			62.5 mJ
Operating Collector Junction Temperature Range			-65°C to 200°C*
Storage Temperature Range			-65°C to 200°C*
Terminal Temperature 1/16 Inch from Case for 10 Seconds			250°C*

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.66 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡ L = 20 mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = 2.5$ A. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

†Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

‡This circuit appears on page 5-1 of this data book.

TYPES 2N5873, 2N5874

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5873		2N5874		UNIT
		MIN	MAX	MIN	MAX	
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = 0.1 A, I _B = 0, See Note 6	60		80		V
I _{CEO} Collector Cutoff Current	V _{CE} = 30 V, I _B = 0 V _{CE} = 40 V, I _B = 0	0.5		0.5		mA
I _{CEV} Collector Cutoff Current	V _{CE} = 60 V, V _{BE} = -1.5 V	0.25				mA
	V _{CE} = 80 V, V _{BE} = -1.5 V			0.25		
	V _{CE} = 60 V, V _{BE} = -1.5 V, T _C = 150°C V _{CE} = 80 V, V _{BE} = -1.5 V, T _C = 150°C	2		2		
I _{CBO} Collector Cutoff Current	V _{CB} = 60 V, I _E = 0	0.25				mA
	V _{CB} = 80 V, I _E = 0			0.25		
I _{EBO} Emitter Cutoff Current	V _{EB} = 5 V, I _C = 0	1		1		mA
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 0.5 A	35		35		
	V _{CE} = 4 V, I _C = 2.5 A	20		20		
	V _{CE} = 4 V, I _C = 5 A	5		5		
V _{BE} Base-Emitter Voltage	I _B = 0.4 A, I _C = 4 A	1.6		1.6		V
	V _{CE} = 4 V, I _C = 5 A	2		2		
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 0.4 A, I _C = 4 A	1		1		V
	I _B = 1 A, I _C = 5 A	2		2		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 0.5 A, f = 1 kHz	20		20		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 0.25 A, f = 1 MHz	4		4		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 1 MHz	200		200		pF

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = 2.5 A, I _{B(1)} = 0.25 A, I _{B(2)} = -0.25 A, V _{BE(off)} = -4.6 V, R _L = 12 Ω, See Note 8	0.7		μs
t _s Storage Time		1		
t _f Fall Time		0.8		

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*‡. V_{BB1} = 24 V, V_{BB2} = 4.6 V, V_{CC} = 30 V, V_{on} = 22.5 V, R_{BB1} = 43 Ω, R_{BB2} = 22 Ω.

‡This circuit appears on page 5-1 of this data book.

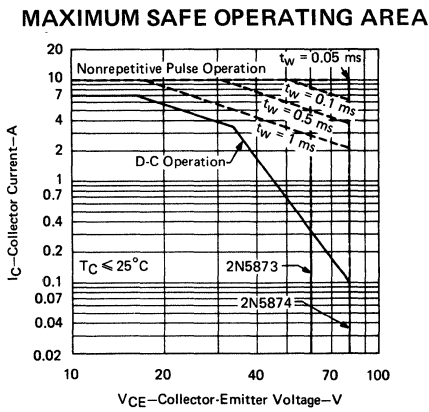


FIGURE 1

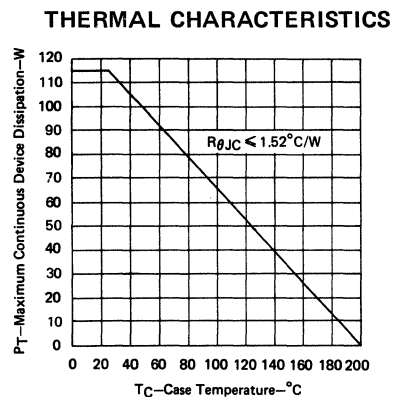


FIGURE 2

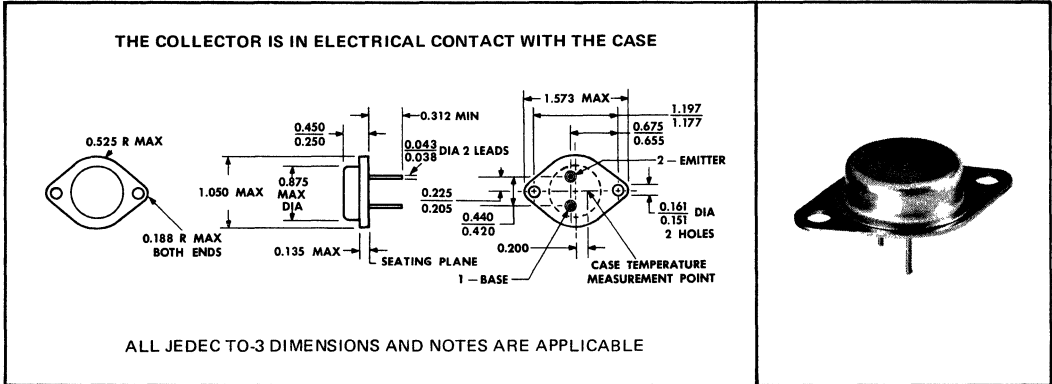
TYPES 2N5875, 2N5876

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5877, 2N5878**

- 150 Watts at 25°C Case Temperature
- 10-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 0.5 A
- 62.5-mJ Reverse Energy Rating

***mechanical data**



TYPES 2N5875, 2N5876
BULLETIN NO. DL-S-7111608, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5875	2N5876
Collector-Base Voltage	-60 V*	-80 V*
Collector-Emitter Voltage (See Note 1)	-60 V*	-80 V*
Emitter-Base Voltage	-5 V*	-5 V*
Continuous Collector Current		
Peak Collector Current (See Note 2)	← -15 A →	
Continuous Base Current	← -2 A* →	
Safe Operating Area at (or below) 25°C Case Temperature	← See Figure 1 →	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W* →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →	
Operating Collector Junction Temperature Range	-65°C to 200°C*	
Storage Temperature Range	-65°C to 200°C*	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 250°C* →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.857 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $L = 20$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = -2.5$ A. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.
[†]Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.
[‡]This circuit appears on page 5-1 of this data book.

TYPES 2N5875, 2N5876

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5875		2N5876		UNIT	
		MIN	MAX	MIN	MAX		
V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = -0.2 A, I _B = 0, See Note 6	-60		-80		V	
I _{CEO} Collector Cutoff Current	V _{CE} = -30 V, I _B = 0 V _{CE} = -40 V, I _B = 0		-1		-1	mA	
I _{CEV} Collector Cutoff Current	V _{CE} = -60 V, V _{BE} = 1.5 V		-0.5			mA	
	V _{CE} = -80 V, V _{BE} = 1.5 V				-0.5		
	V _{CE} = -60 V, V _{BE} = 1.5 V, T _C = 150°C V _{CE} = -80 V, V _{BE} = 1.5 V, T _C = 150°C				-5		
I _{CBO} Collector Cutoff Current	V _{CB} = -60 V, I _E = 0		-0.5			mA	
	V _{CB} = -80 V, I _E = 0				-0.5		
I _{EBO} Emitter Cutoff Current	V _{EB} = -5 V, I _C = 0		-1		-1	mA	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -1 A		35		35		
	V _{CE} = -4 V, I _C = -4 A	See Notes 6 and 7	20	100	20		100
	V _{CE} = -4 V, I _C = -8 A		5		5		
V _{BE} Base-Emitter Voltage	I _B = -0.5 A, I _C = -5 A	See Notes 6 and 7		-1.6		-1.6	V
	V _{CE} = -4 V, I _C = -8 A			-2.5		-2.5	
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = -0.5 A, I _C = -5 A	See Notes 6 and 7		-1		-1	V
	I _B = -1.6 A, I _C = -8 A			-3		-3	
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -1 A, f = 1 kHz		20		20		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -10 V, I _C = -0.5 A, f = 1 MHz		4		4		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = -10 V, I _E = 0, f = 1 MHz		500		500	pF	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = -4 A, I _B (1) = -0.4 A, I _B (2) = 0.4 A, V _{BE(off)} = 5 V, R _L = 7.5 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡V_{BB1} = 24 V, V_{BB2} = 5 V, V_{CC} = 30 V, V_{on} = -22 V, R_{BB1} = 26 Ω, R_{BB2} = 15 Ω.

‡ This circuit appears on page 5-1 of this data book.

MAXIMUM SAFE OPERATION AREAS

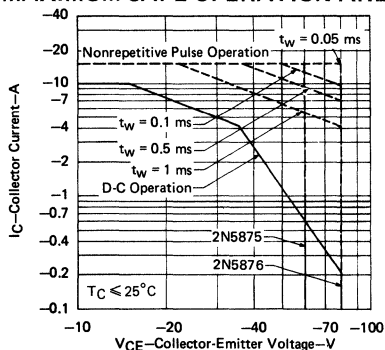


FIGURE 1

THERMAL CHARACTERISTICS

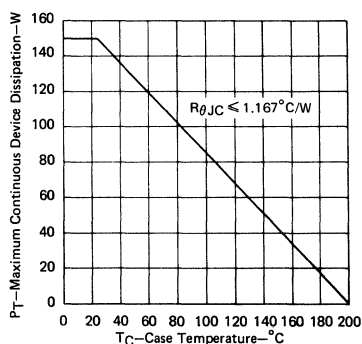


FIGURE 2

TYPES 2N5877, 2N5878

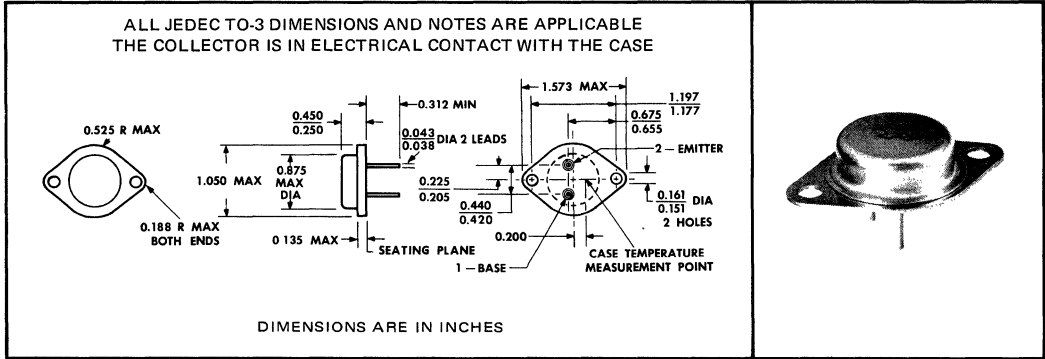
N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPES 2N5877, 2N5878
BULLETIN NO. DL-S-7111624, DECEMBER 1971

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5875, 2N5876**

- 150 Watts at 25°C Case Temperature
- 10-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 0.5 A
- 62.5-mJ Reverse Energy Rating

*mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5877	2N5878
Collector-Base Voltage	60 V*	80 V*
Collector-Emitter Voltage (See Note 1)	60 V*	80 V*
Emitter-Base Voltage	5 V*	5 V*
Continuous Collector Current		
Peak Collector Current (See Note 2)	← 15 A →	
Continuous Base Current	← 2 A* →	
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W* →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →	
Operating Collector Junction Temperature Range	← -65°C to 200°C* →	
Storage Temperature Range	← -65°C to 200°C* →	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 250°C* →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.857 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[‡] $L = 20$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = 2.5$ A. Energy $\approx I_C^2 L/2$.

* JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.
 † Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.
 ‡ This circuit appears on page 5-1 of this data book.

TYPES 2N5877, 2N5878

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5877		2N5878		UNIT	
		MIN	MAX	MIN	MAX		
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = 0.2 A, I _B = 0, See Note 6	60		80		V	
I _{CEO} Collector Cutoff Current	V _{CE} = 30 V, I _B = 0 V _{CE} = 40 V, I _B = 0		1		1	mA	
I _{CEV} Collector Cutoff Current	V _{CE} = 60 V, V _{BE} = -1.5 V		0.5			mA	
	V _{CE} = 80 V, V _{BE} = -1.5 V				0.5		
	V _{CE} = 60 V, V _{BE} = -1.5 V, T _C = 150°C V _{CE} = 80 V, V _{BE} = -1.5 V, T _C = 150°C		5		5		
I _{CBO} Collector Cutoff Current	V _{CB} = 60 V, I _E = 0		0.5			mA	
	V _{CB} = 80 V, I _E = 0				0.5		
I _{EBO} Emitter Cutoff Current	V _{EB} = 5 V, I _C = 0		1		1	mA	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 1 A		35		35		
	V _{CE} = 4 V, I _C = 4 A	See Notes 6 and 7	20	100	20		100
	V _{CE} = 4 V, I _C = 8 A		5		5		
V _{BE} Base-Emitter Voltage	I _B = 0.5 A, I _C = 5 A	See Notes 6 and 7		1.6		1.6	V
	V _{CE} = 4 V, I _C = 8 A			2.5		2.5	
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 0.5 A, I _C = 5 A	See Notes 6 and 7		1		1	V
	I _B = 1.6 A, I _C = 8 A			3		3	
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 1 A, f = 1 kHz		20		20		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 0.5 A, f = 1 MHz		4		4		
Cobo Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 1 MHz		300		300	pF	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

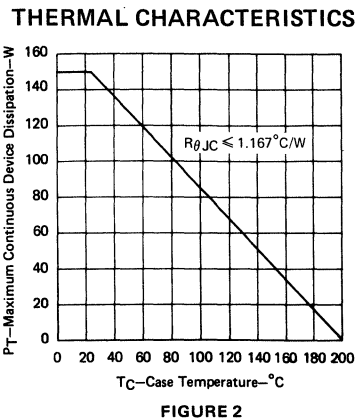
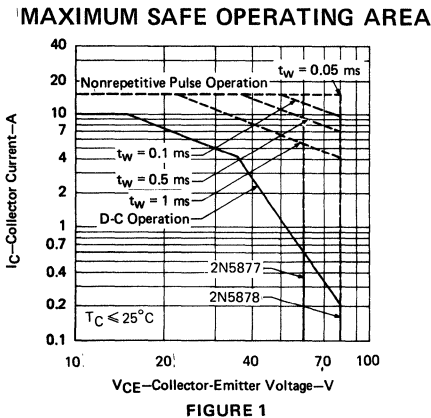
PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = 4 A, I _{B(1)} = 0.4 A, I _{B(2)} = -0.4 A, V _{BE(off)} = -5 V, R _L = 7.5 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡ V_{BB1} = 24 V, V_{BB2} = 5 V, V_{CC} = 30 V, V_{on} = 22 V, R_{BB1} = 26 Ω, R_{BB2} = 15 Ω.

‡ This circuit appears on page 5-1 of this data book.



TYPES 2N5879, 2N5880

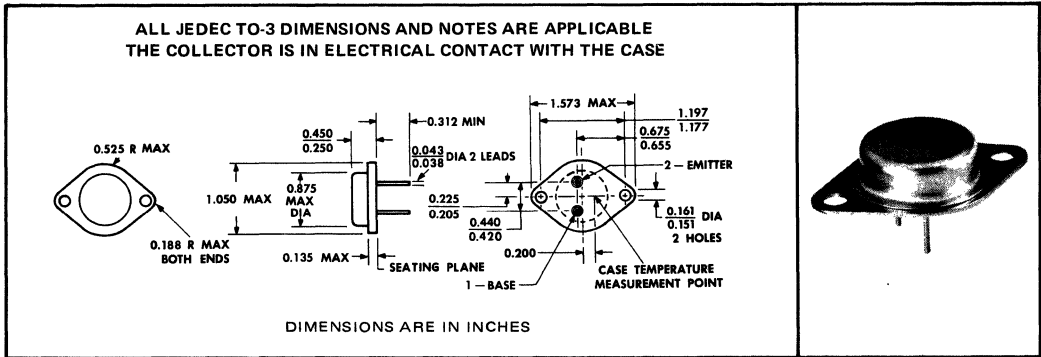
P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPES 2N5879, 2N5880
BULLETIN NO. DLS-7111609, DECEMBER 1971

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5881, 2N5882**

- 160 Watts at 25°C Case Temperature
- 15-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 1 A
- 90 mJ-Reverse Energy Rating

*mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5879	2N5880
Collector-Base Voltage	-60 V*	-80 V*
Collector-Emitter Voltage (See Note 1)	-60 V*	-80 V*
Emitter-Base Voltage	-5 V*	-5 V*
Continuous Collector Current		
Peak Collector Current (See Note 2)		
Continuous Base Current		
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)		
Unclamped Inductive Load Energy (See Note 5)		
Operating Collector Junction Temperature Range		
Storage Temperature Range		
Terminal Temperature 1/16 Inch from Case for 10 Seconds		

NOTES: 1. These values apply when the base-emitter diode is open-circuited.

2. This value applies for $t_W \leq 1$ ms, duty cycle $\leq 10\%$.

3. Derate linearly to 200°C case temperature at the rate of 0.915 W/°C.

4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.

5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $L = 20$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = -3$ A. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

[†]Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

[‡]This circuit appears on page 5-1 of this data book.

TYPES 2N5879, 2N5880

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5875		2N5876		UNIT	
		MIN	MAX	MIN	MAX		
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = -0.2 A, I _B = 0, See Note 6	-60		-80		V	
I _{CEO} Collector Cutoff Current	V _{CE} = -30 V, I _B = 0 V _{CE} = -40 V, I _B = 0		-1		-1	mA	
I _{CEV} Collector Cutoff Current	V _{CE} = -60 V, V _{BE} = 1.5 V		-0.5			mA	
	V _{CE} = -80 V, V _{BE} = 1.5 V				-0.5		
	V _{CE} = -60 V, V _{BE} = 1.5 V, T _C = 150°C V _{CE} = -80 V, V _{BE} = 1.5 V, T _C = 150°C		-5		-5		
I _{CBO} Collector Cutoff Current	V _{CB} = -60 V, I _E = 0		-0.5			mA	
	V _{CB} = -80 V, I _E = 0				-0.5		
I _{EBO} Emitter Cutoff Current	V _{EB} = -5 V, I _C = 0		-1		-1	mA	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -2 A		35		35		
	V _{CE} = -4 V, I _C = -6 A	See Notes 6 and 7	20	100	20		100
	V _{CE} = -4 V, I _C = -12 A		5	5			
V _{BE} Base-Emitter Voltage	I _B = -0.7 A, I _C = -7 A	See Notes 6 and 7	-1.6		-1.6	V	
	V _{CE} = -4 V, I _C = -12 A		-2.5		-2.5		
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = -0.7 A, I _C = -7 A	See Notes 6 and 7	-1		-1	V	
	I _B = -2.4 A, I _C = -12 A		-4		-4		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -2 A, f = 1 kHz		20		20		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -10 V, I _C = -1 A, f = 1 MHz		4		4		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = -10 V, I _E = 0, f = 1 MHz		600		600	pF	

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = -6 A, I _B (1) = -0.6 A, I _B (2) = 0.6 A, V _{BE(off)} = 5 V, R _L = 5 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡ V_{BB1} = 23 V, V_{BB2} = 5 V, V_{CC} = 30 V, V_{on} = -20.5 V, R_{BB1} = 16 Ω, R_{BB2} = 10 Ω.

‡ This circuit appears on page 5-1 of this data book.

MAXIMUM SAFE OPERATING AREA

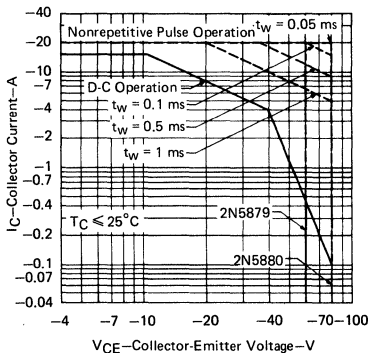


FIGURE 1

THERMAL CHARACTERISTICS

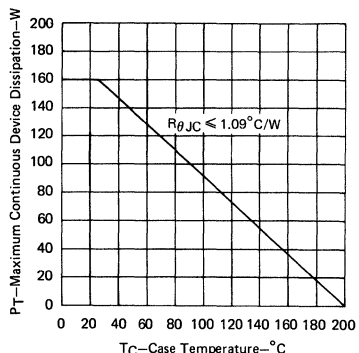


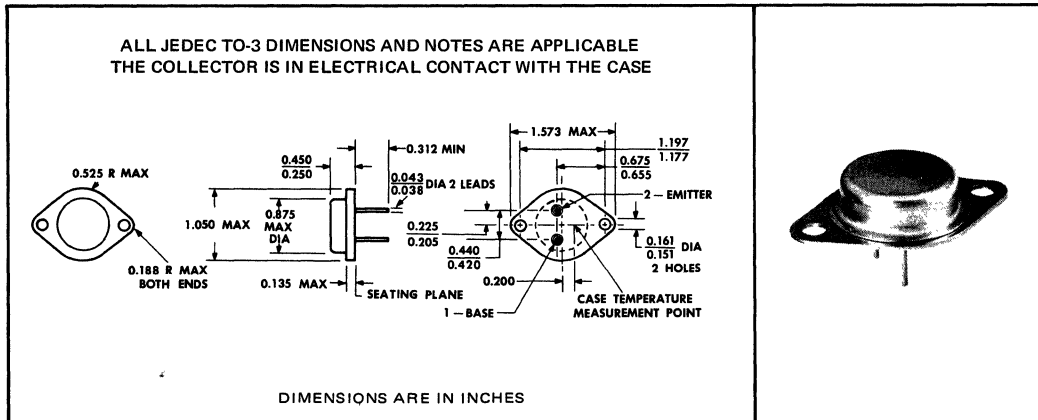
FIGURE 2

TYPES 2N5881, 2N5882 N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5879, 2N5880**

- 160 Watts at 25°C Case Temperature
- 15-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 1 A
- 90-mJ Reverse Energy Rating

***mechanical data**



TYPES 2N5881, 2N5882
BULLETIN NO. DL-S-7111625, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5881	2N5882
Collector-Base Voltage	60 V*	80 V*
Collector-Emitter Voltage (See Note 1)	60 V*	80 V*
Emitter-Base Voltage	5 V*	5 V*
Continuous Collector Current		
Peak Collector Current (See Note 2)		
Continuous Base Current		
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)		
Unclamped Inductive Load Energy (See Note 5)		
Operating Collector Junction Temperature Range		
Storage Temperature Range		
Terminal Temperature 1/16 Inch from Case for 10 Seconds		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.915 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $L = 20$ mH, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 10$ V, $I_{CM} = 3$ A. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

[†]Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

[‡]This circuit appears on page 5-1 of this data book.

TYPES 2N5881, 2N5882

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5881		2N5882		UNIT	
		MIN	MAX	MIN	MAX		
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = 0.2 A, I _B = 0, See Note 6	60		80		V	
I _{CEO} Collector Cutoff Current	V _{CE} = 30 V, I _B = 0 V _{CE} = 40 V, I _B = 0		1		1	mA	
I _{CEV} Collector Cutoff Current	V _{CE} = 60 V, V _{BE} = -1.5 V		0.5			mA	
	V _{CE} = 80 V, V _{BE} = -1.5 V				0.5		
	V _{CE} = 60 V, V _{BE} = -1.5 V, T _C = 150°C			5			
	V _{CE} = 80 V, V _{BE} = -1.5 V, T _C = 150°C				5		
I _{CBO} Collector Cutoff Current	V _{CB} = 60 V, I _E = 0		0.5			mA	
	V _{CB} = 80 V, I _E = 0				0.5		
I _{EBO} Emitter Cutoff Current	V _{EB} = 5 V, I _C = 0		1		1	mA	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 2 A		35		35		
	V _{CE} = 4 V, I _C = 6 A	See Notes 6 and 7	20	100	20		100
	V _{CE} = 4 V, I _C = 12 A		5		5		
V _{BE} Base-Emitter Voltage	I _B = 0.7 A, I _C = 7 A	See Notes 6 and 7	1.6		1.6	V	
	V _{CE} = 4 V, I _C = 12 A		2.5		2.5		
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 0.7 A, I _C = 7 A	See Notes 6 and 7	1		1	V	
	I _B = 2.4 A, I _C = 12 A		4		4		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 2 A, f = 1 kHz		20		20		
h _{fe1} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 1 A, f = 1 MHz		4		4		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 1 MHz		400		400	pF	

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = 6 A, I _{B(1)} = 0.6 A, I _{B(2)} = -0.6 A, V _{BE(off)} = -5 V, R _L = 5 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

* JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistor*. † V_{BB1} = 23 V, V_{BB2} = 5 V, V_{CC} = 30 V, V_{on} = 20.5 V, R_{BB1} = 16 Ω, R_{BB2} = 10 Ω.

‡ This circuit appears on page 5-1 of this data book.

MAXIMUM SAFE OPERATING AREA

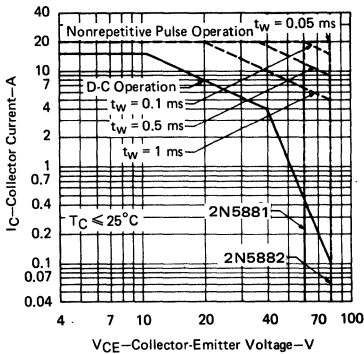


FIGURE 1

THERMAL CHARACTERISTICS

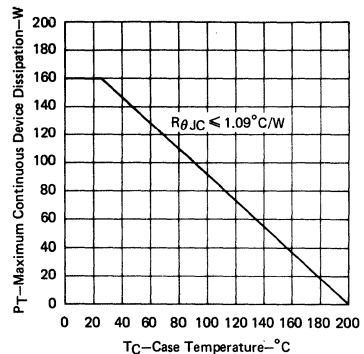


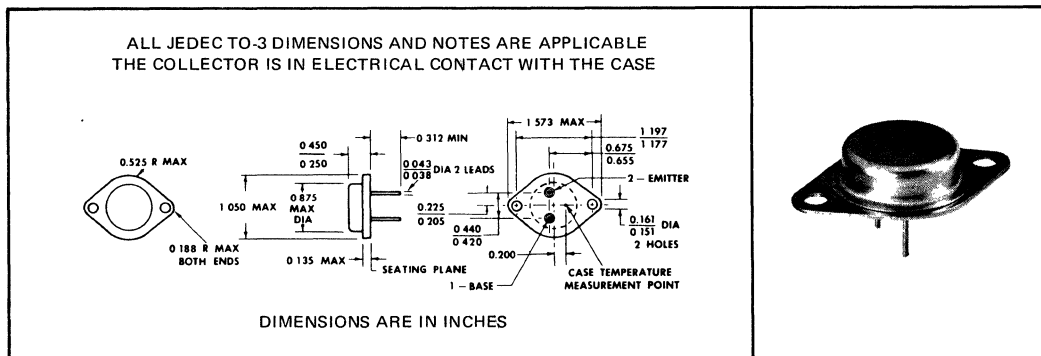
FIGURE 2

TYPES 2N5883, 2N5884 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5885, 2N5886

- 200 Watts at 25°C Case Temperature
- 25-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 1 A
- 90-mJ Reverse Energy Rating

*mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5883	2N5884
Collector-Base Voltage	-60 V*	-80 V*
Collector-Emitter Voltage (See Note 1)	-60 V*	-80 V*
Emitter-Base Voltage	-5 V*	-5 V*
Continuous Collector Current	← { -25 A † } →	
Peak Collector Current (See Note 2)	← -30 A →	
Continuous Base Current	← -6 A* →	
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 200 W* →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	
Unclamped Inductive Load Energy (See Note 5)	← 90 mJ →	
Operating Collector Junction Temperature Range	-65°C to 200°C*	
Storage Temperature Range	-65°C to 200°C*	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 250°C* →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1.14 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡ L = 20 mH, R_{BB1} = 20 Ω, R_{BB2} = 100 Ω, V_{BB1} = 10 V, V_{BB2} = 0 V, R_L = 0.1 Ω, V_{CC} = 10 V, I_{CM} = -3 A, Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

†Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

‡This circuit appears on page 5-1 of this data book.

TYPES 2N5883, 2N5884
BULLETIN NO. DL-S-7111610, DECEMBER 1971

5

TYPES 2N5883, 2N5884

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5883		2N5884		UNIT
		MIN	MAX	MIN	MAX	
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = -0.2 A, I _B = 0, See Note 6	-60		-80		V
I _{CEO} Collector Cutoff Current	V _{CE} = -30 V, I _B = 0		-2			mA
	V _{CE} = -40 V, I _B = 0				-2	
I _{CEV} Collector Cutoff Current	V _{CE} = -60 V, V _{BE} = 1.5 V		-1			mA
	V _{CE} = -80 V, V _{BE} = 1.5 V				-1	
	V _{CE} = -60 V, V _{BE} = 1.5 V, T _C = 150°C		-10			
	V _{CE} = -80 V, V _{BE} = 1.5 V, T _C = 150°C				-10	
I _{CBO} Collector Cutoff Current	V _{CB} = -60 V, I _E = 0		-1			mA
	V _{CB} = -80 V, I _E = 0				-1	
I _{EBO} Emitter Cutoff Current	V _{EB} = -5 V, I _C = 0		-1		-1	mA
	V _{EB} = -4 V, I _C = -3 A					
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -10 A	See Notes 6 and 7	20	100	20	100
	V _{CE} = -4 V, I _C = -20 A		5		5	
	I _B = -1.5 A, I _C = -15 A			-1.8		-1.8
V _{BE} Base-Emitter Voltage	V _{CE} = -4 V, I _C = -20 A	See Notes 6 and 7		-2.5		-2.5
	I _B = -1.5 A, I _C = -15 A			-1		-1
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = -1.5 A, I _C = -15 A	See Notes 6 and 7		-1		-1
	I _B = -4 A, I _C = -20 A			-4		-4
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -4 V, I _C = -3 A, f = 1 kHz		20		20	
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -10 V, I _C = -1 A, f = 1 MHz		4		4	
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = -10 V, I _E = 0, f = 1 MHz		800		800	pF

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = -10 A, I _{B(1)} = -1 A, I _{B(2)} = 1 A V _{BE(off)} = 4 V, R _L = 3 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡: V_{BB1} = 25 V, V_{BB2} = 4 V, V_{CC} = 30 V, V_{on} = -23 V, R_{BB1} = 11 Ω, R_{BB2} = 5 Ω.

‡ This circuit appears on page 5-1 of this data book.

MAXIMUM SAFE OPERATING AREA

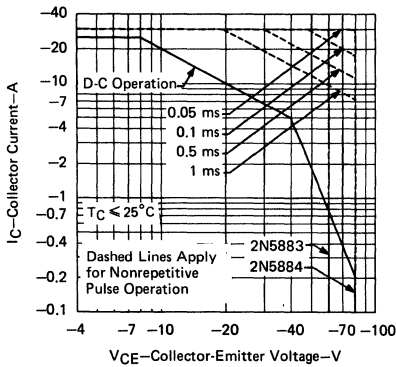


FIGURE 1

THERMAL CHARACTERISTICS

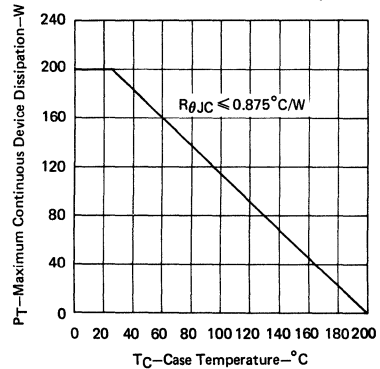


FIGURE 2

TYPES 2N5885, 2N5886

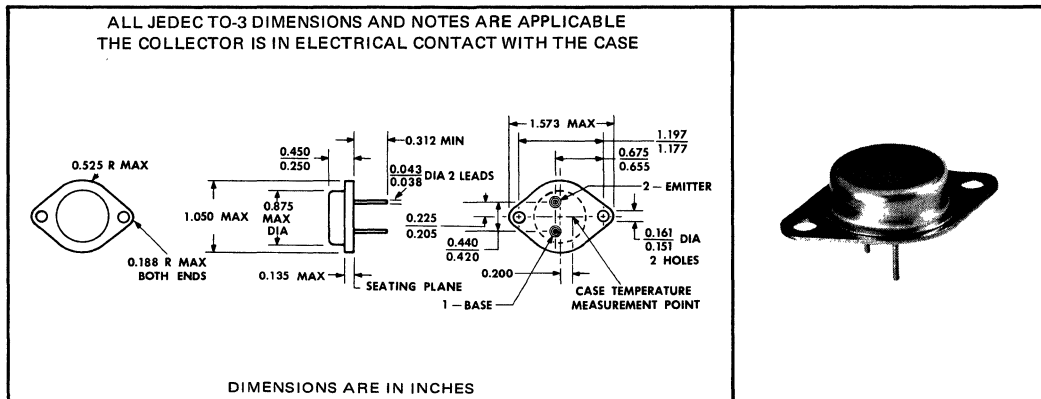
N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPES 2N5885, 2N5886
BULLETIN NO. DL-S-7111626, DECEMBER 1971

**FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N5883, 2N5884**

- 200 Watts at 25°C Case Temperature
- 25-A Rated Continuous Collector Current
- Min f_T of 4 MHz at 10 V, 1 A
- 90-mJ Reverse Energy Rating

***mechanical data**



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5885	2N5886
Collector-Base Voltage	60 V*	80 V*
Collector-Emitter Voltage (See Note 1)	60 V*	80 V*
Emitter-Base Voltage	5 V*	5 V*
Continuous Collector Current	← $\left. \begin{matrix} 25 \text{ A}^\dagger \\ 20 \text{ A}^* \end{matrix} \right\} \rightarrow$	
Peak Collector Current (See Note 2)	← 30 A →	
Continuous Base Current	← 6 A* →	
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 200 W* →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	
Unclamped Inductive Load Energy (See Note 5)	← 90 mJ →	
Operating Collector Junction Temperature Range	← -65°C to 200°C* →	
Storage Temperature Range	← -65°C to 200°C* →	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 250°C* →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1.14 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.
 5. This rating is based on the capability of the transistors to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. † L = 20 mH, R_{BB1} = 20 Ω, R_{BB2} = 100 Ω, V_{BB1} = 10 V, V_{BB2} = 0 V, R_L = 0.1 Ω, V_{CC} = 10 V, I_{CM} = 3 A. Energy $\approx I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

†Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

‡This circuit appears on page 5-1 of this data book.

TYPES 2N5885, 2N5886

N-P-N SINGLE-DIFFUSED SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5885		2N5886		UNIT	
		MIN	MAX	MIN	MAX		
V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = 0.2 A, I _B = 0, See Note 6	60		80		V	
I _{CEO} Collector Cutoff Current	V _{CE} = 30 V, I _B = 0 V _{CE} = 40 V, I _B = 0		2		2	mA	
I _{CEV} Collector Cutoff Current	V _{CE} = 60 V, V _{BE} = -1.5 V		1			mA	
	V _{CE} = 80 V, V _{BE} = -1.5 V				1		
	V _{CE} = 60 V, V _{BE} = -1.5 V, T _C = 150°C V _{CE} = 80 V, V _{BE} = -1.5 V, T _C = 150°C		10		10		
I _{CBO} Collector Cutoff Current	V _{CB} = 60 V, I _E = 0		1			mA	
	V _{CB} = 80 V, I _E = 0				1		
I _{EBO} Emitter Cutoff Current	V _{EB} = 5 V, I _C = 0		1		1	mA	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 3 A		35		35		
	V _{CE} = 4 V, I _C = 10 A	See Notes 6 and 7	20	100	20		100
	V _{CE} = 4 V, I _C = 20 A		5		5		
V _{BE} Base-Emitter Voltage	I _B = 1.5 A, I _C = 15 A	See Notes 6 and 7		1.8		1.8	V
	V _{CE} = 4 V, I _C = 20 A			2.5		2.5	
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 1.5 A, I _C = 15 A	See Notes 6 and 7		1		1	V
	I _B = 4 A, I _C = 20 A			4		4	
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 3 A, f = 1 kHz		20		20		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 10 V, I _C = 1 A, f = 1 MHz		4		4		
C _{obo} Common-Base Open-Circuit Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 1 MHz		500		500	pF	

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
t _r Rise Time	I _C = 10 A, I _B (1) = 1 A, I _B (2) = -1 A, V _{BE(off)} = -4 V, R _L = 3 Ω, See Note 8		0.7	μs
t _s Storage Time			1	
t _f Fall Time			0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

* JEDEC registered data.

NOTE 8: These characteristics are measured in the circuit of clause 3.3.13.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. ‡ V_{BB1} = 25 V, V_{BB2} = 4 V, V_{CC} = 30 V, V_{on} = 23 V, R_{BB1} = 11 Ω, R_{BB2} = 5 Ω.

‡ This circuit appears on page 5-1 of this data book.

MAXIMUM SAFE OPERATING AREA

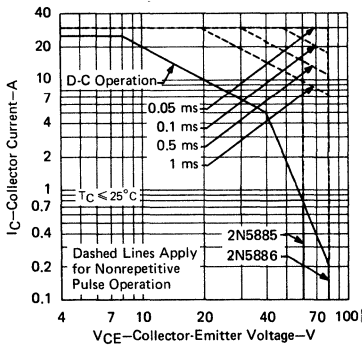


FIGURE 1

THERMAL CHARACTERISTICS

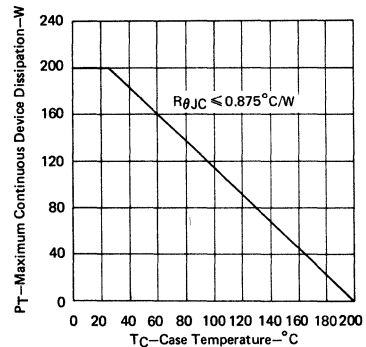


FIGURE 2

TYPE 2N5938 N-P-N SILICON POWER TRANSISTOR

TYPE 2N5938
BULLETIN NO. DL-S-7011339, JUNE 1970

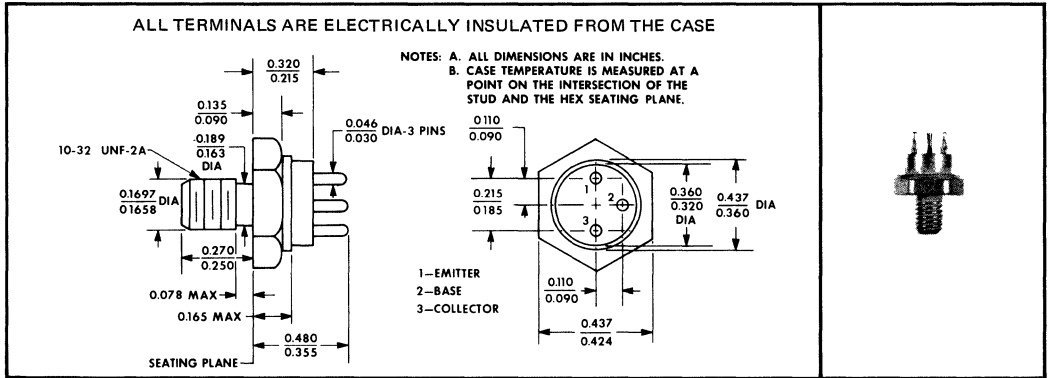
RADIATION-TOLERANT TRANSISTOR FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Min h_{FE} of 10 at 3 V, 1 A after 1×10^{14} Fast Neutrons/cm²
- 20 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.4 V at $I_C = 1$ A
- Min f_T of 150 MHz at 5 V, 1 A

description

The 2N5938 transistor offers a significant advance in radiation-resistant-device technology. Unique construction techniques produce transistors which maintain useful characteristics after fast-neutron radiation fluences through 10^{14} n/cm².

*mechanical data



5

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	60 V
Collector-Emitter Voltage (See Note 1)	50 V
Emitter-Base Voltage	4 V
Continuous Collector Current	3 A
Peak Collector Current (See Note 2)	5 A
Continuous Base Current	1 A
Continuous Emitter Current	4 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 6
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	20 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2.5 W
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	230°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 10$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.2 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 14.3 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPE 2N5938

N-P-N SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 10 \text{ mA}$, $I_B = 0$, See Note 5	50		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$		500	μA
I_{CES}	Collector Cutoff Current	$V_{CE} = 55 \text{ V}$, $V_{BE} = 0$		100	μA
		$V_{CE} = 30 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		200	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 2 \text{ V}$, $I_C = 0$		10	μA
		$V_{EB} = 4 \text{ V}$, $I_C = 0$		100	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 5 and 6	30	150	
		$V_{CE} = 3 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 5 and 6	20		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 3 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 5 and 6		1.4	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.1 \text{ A}$, $I_C = 1 \text{ A}$, See Notes 5 and 6		0.4	V
		$I_B = 0.3 \text{ A}$, $I_C = 3 \text{ A}$, See Notes 5 and 6		0.75	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	20		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 30 \text{ MHz}$	5		
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$		80	pF

*post-irradiation electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	RADIATION FLUENCE†	MIN	MAX	UNIT
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 5 and 6	$1 \times 10^{14} \text{ n/cm}^2$	10		

*thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	5	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	70	

*JEDEC registered data

†Radiation is fast neutrons (n) at $E \geq 10 \text{ keV}$ (reactor spectrum).

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPE 2N5938 N-P-N SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

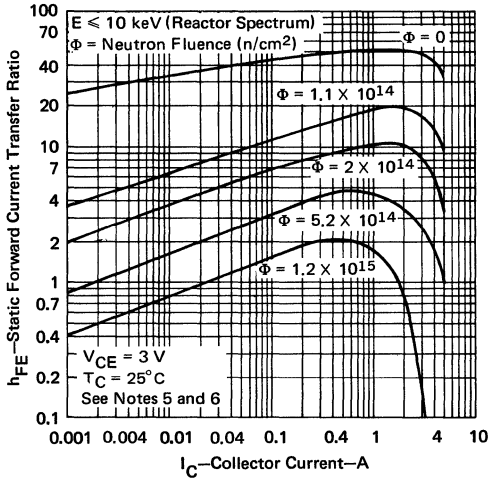


FIGURE 1

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

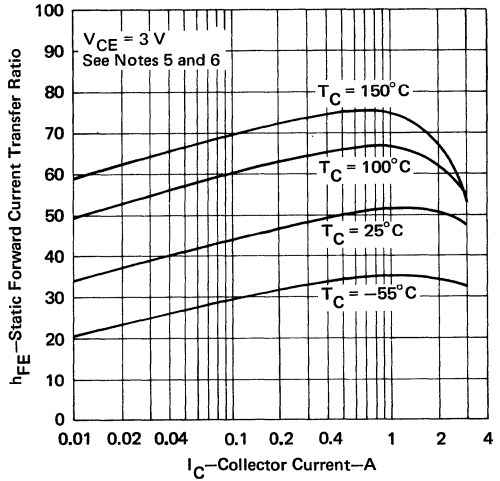


FIGURE 2

BASE-EMITTER VOLTAGE
vs
CASE TEMPERATURE

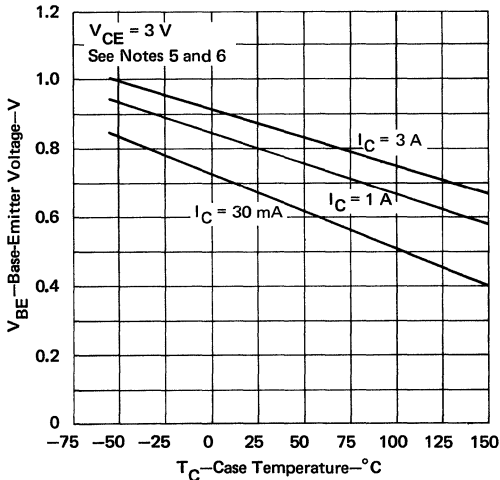


FIGURE 3

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE

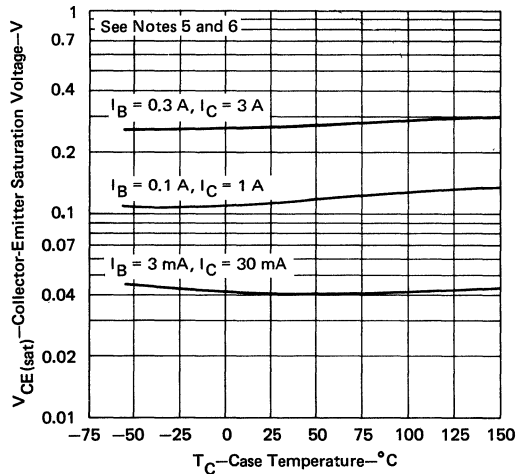


FIGURE 4

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

5

TYPE 2N5938 N-P-N SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

COMMON-BASE OPEN-CIRCUIT INPUT
AND OUTPUT CAPACITANCE
vs
REVERSE BIAS VOLTAGE

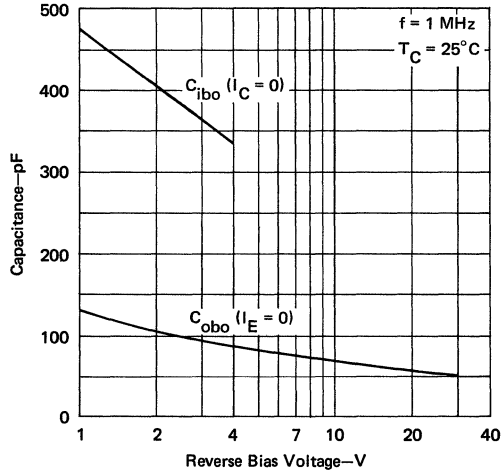


FIGURE 5

MAXIMUM SAFE OPERATING REGION

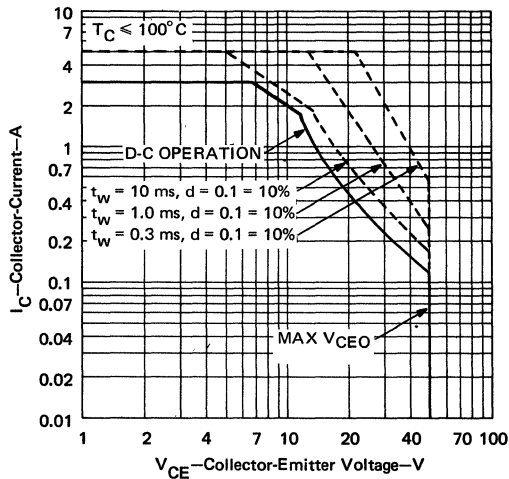


FIGURE 6

TYPE 2N5938 N-P-N SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

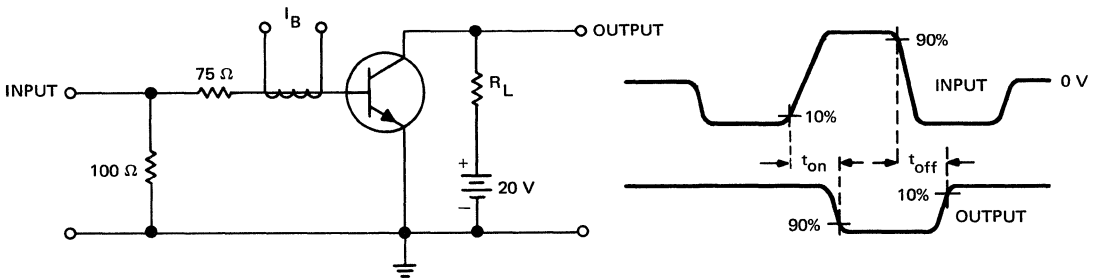
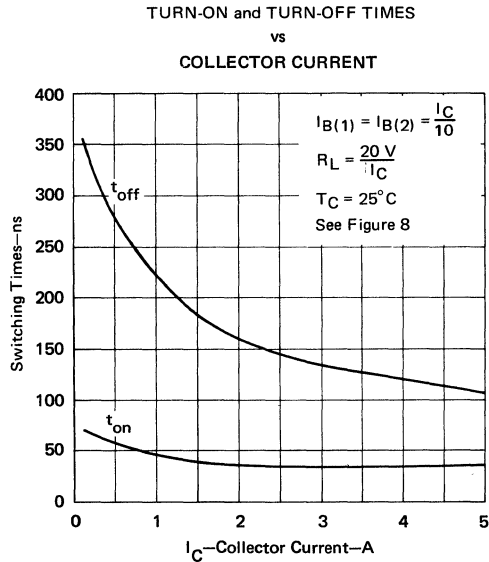


FIGURE 8—TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR FIGURE 7

- NOTES:
- Adjust the input voltage for the desired values of $I_{B(1)}$ and $I_{B(2)}$.
 - The input voltage is supplied by two generators connected in parallel. Each generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{OUT} = 50 \Omega$, duty cycle $\leq 1\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPE 2N5938 N-P-N SILICON POWER TRANSISTOR

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

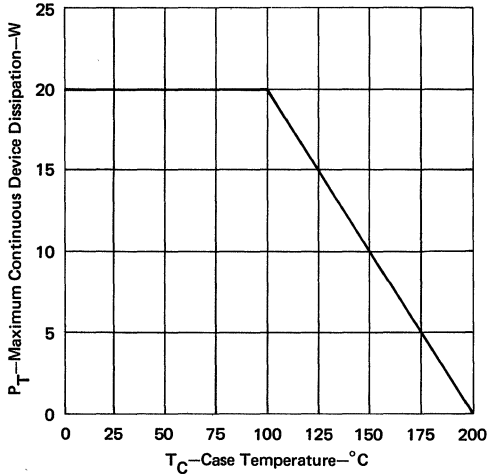


FIGURE 9

PEAK-POWER COEFFICIENT CURVE

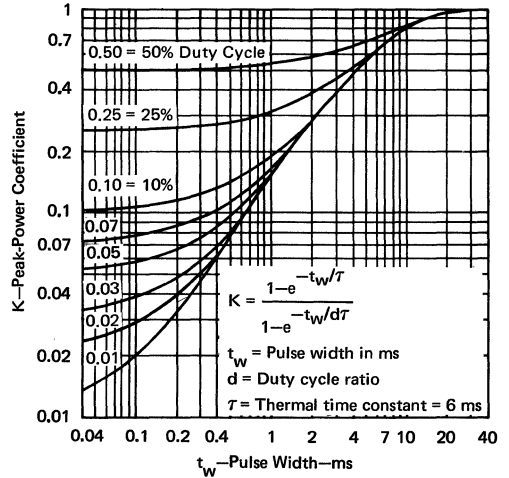


FIGURE 10

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_T(av)$	Average Power Dissipation		W
$P_T(max)$	Peak Power Dissipation		W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	70	$^{\circ}C/W$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	5	$^{\circ}C/W$
$R_{\theta CA}$	Case-to-Free-Air Thermal Resistance	65	$^{\circ}C/W$
$R_{\theta CHS}$	Case-to-Heat-Sink Thermal Resistance		$^{\circ}C/W$
$R_{\theta HSA}$	Heat-Sink-to-Free-Air Thermal Resistance		$^{\circ}C/W$
T_A	Free-Air Temperature		$^{\circ}C$
T_C	Case Temperature		$^{\circ}C$
$T_J(av)$	Average Junction Temperature	≤ 200	$^{\circ}C$
$T_J(max)$	Peak Junction Temperature	≤ 200	$^{\circ}C$
K	Peak-Power Coefficient	See Figure 10	
t_w	Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_w/t_x)		

Equation No. 1—Application: d-c power dissipation, heat sink used.

$$P_T(av) = \frac{T_J(av) - T_A}{R_{\theta JC} + R_{\theta CHS} + R_{\theta HSA}} \quad \text{for } 100^{\circ}C \leq T_C \leq 200^{\circ}C \quad \text{as in Figure 9}$$

Equation No. 2—Application: d-c power dissipation, no heat sink used.

$$P_T(av) = \frac{T_J(av) - T_A}{R_{\theta JA}} \quad \text{for } 25^{\circ}C \leq T_A \leq 200^{\circ}C$$

Equation No. 3—Application: Peak power dissipation, heat sink used.

$$P_T(max) = \frac{T_J(max) - T_A}{d(R_{\theta CHS} + R_{\theta HSA}) + K \cdot R_{\theta JC}} \quad \text{for } 100^{\circ}C \leq T_C \leq 200^{\circ}C$$

Equation No. 4—Application: Peak-power dissipation, no heat sink used.

$$P_T(max) = \frac{T_J(max) - T_A}{d \cdot R_{\theta CA} + K \cdot R_{\theta JC}} \quad \text{for } 25^{\circ}C \leq T_A \leq 200^{\circ}C$$

Example—Find $P_T(max)$ (design limit)

OPERATING CONDITIONS:

$R_{\theta CHS} + R_{\theta HSA} = 4^{\circ}C/W$ (From information supplied with heat sink.)

$T_J(av)$ (design limit) = $200^{\circ}C$

$T_A = 50^{\circ}C$

$d = 10\% = 0.1$

$t_w = 0.6$ ms

Solution:

From Figure 10, Peak-Power Coefficient

$K = 0.151$ and by use of equation No. 3

$$P_T(max) = \frac{T_J(max) - T_A}{d(R_{\theta CHS} + R_{\theta HSA}) + K \cdot R_{\theta JC}}$$

$$P_T(max) = \frac{200 - 50}{0.1(4) + 0.151(5)} \text{ W} = 130 \text{ W}$$

TYPES 2N5939, 2N5940 N-P-N SILICON POWER TRANSISTORS

TYPES 2N5939, 2N5940
BULLETIN NO. DL-S-7011423, DECEMBER 1970

RADIATION-TOLERANT TRANSISTORS

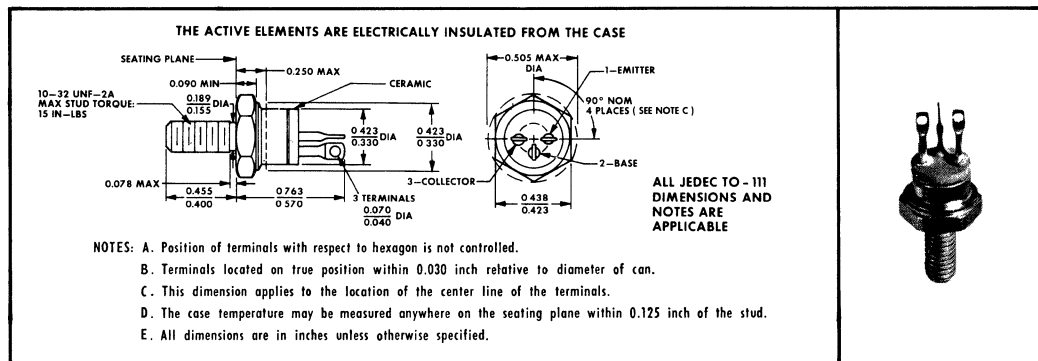
FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Formerly TIXP39, TIXP40
- Min h_{FE} of 10 at 4 V, 5 A after 1×10^{14} Fast Neutrons/cm²
- Max $V_{CE(sat)}$ of 1 V at $I_C = 10$ A
- 40 Watts at 100°C Case Temperature
- Min f_T of 120 MHz at 5 V, 1 A

description

The 2N5939, 2N5940 transistors offer a significant advance in radiation-resistant-device technology. Unique construction techniques produce transistors which maintain useful characteristics after fast-neutron radiation fluences through 10^{14} n/cm²

*mechanical data



5



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5939	2N5940
Collector-Base Voltage	80 V	70 V
Collector-Emitter Voltage (See Note 1)	80 V	70 V
Emitter-Base Voltage	← 5 V →	
Continuous Collector Current	← 10 A →	
Peak Collector Current (See Note 2)	← 20 A →	
Continuous Base Current	← 4 A →	
Continuous Emitter Current	← 12 A →	
Safe Operating Region	See Figure 7	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 40 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →	
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 230°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.4 W/°C.
4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at time of publication.

TYPES 2N5939, 2N5940

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N5939		2N5940		UNIT
		MIN	MAX	MIN	MAX	
V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = 30 mA, I _B = 0, See Note 5	80		70		V
I _{CEO} Collector Cutoff Current	V _{CE} = 50 V, I _B = 0	2				mA
	V _{CE} = 40 V, I _B = 0			2		
I _{CES} Collector Cutoff Current	V _{CE} = 75 V, V _{BE} = 0	500				μA
	V _{CE} = 65 V, V _{BE} = 0			500		
	V _{CE} = 40 V, V _{BE} = 0, T _C = 150°C	2				mA
	V _{CE} = 35 V, V _{BE} = 0, T _C = 150°C			2		
I _{EBO} Emitter Cutoff Current	V _{EB} = 3 V, I _C = 0	200		200		μA
	V _{EB} = 5 V, I _C = 0	1		1		mA
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 5 A	40	200	40	200	
	V _{CE} = 4 V, I _C = 10 A					
V _{BE} Base-Emitter Voltage	V _{CE} = 4 V, I _C = 5 A	1.2		1.2		V
	V _{CE} = 4 V, I _C = 10 A	1.6		1.6		
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 0.5 A, I _C = 5 A	0.6		0.6		V
	I _B = 1 A, I _C = 10 A	1		1		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 5 V, I _C = 1 A, f = 1 kHz	30		30		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 5 V, I _C = 1 A, f = 20 MHz	6		6		

*post-irradiation electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	RADIATION FLUENCE†	MIN	MAX	UNIT
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 5 A, See Notes 5 and 6	1 X 10 ¹⁴ n/cm ²	10		

† Radiation is fast neutrons (n) at E ≥ 10 keV (reactor spectrum).

*thermal characteristics

PARAMETER	MAX	UNIT
R _{θJC} Junction-to-Case Thermal Resistance	2.5	°C/W
R _{θJA} Junction-to-Free-Air Thermal Resistance	87.5	

NOTES: 5. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

*JEDEC registered data.

TYPES 2N5939, 2N5940

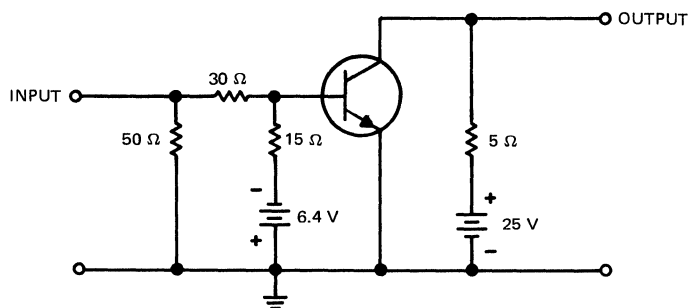
N-P-N SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

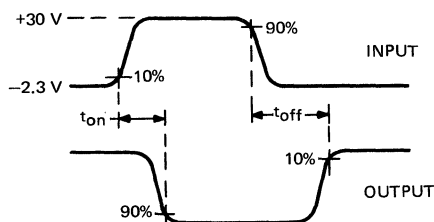
PARAMETER	TEST CONDITIONS‡	TYP	UNIT
t_{on} Turn-On Time	$I_C = 5\text{ A}$, $I_B(1) = 500\text{ mA}$, $I_B(2) = -500\text{ mA}$, $V_{BE(off)} = -5\text{ V}$, $R_L = 5\ \Omega$, See Figure 1	135	ns
t_{off} Turn-Off Time		800	

‡ Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\ \Omega$, $t_w = 10\ \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

5

TYPES 2N5939, 2N5940

N-P-N SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs

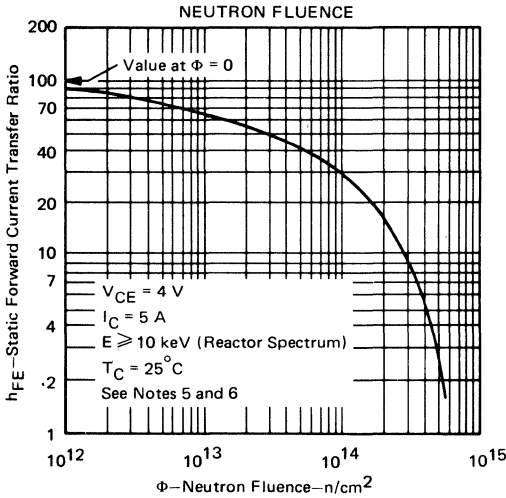


FIGURE 2

STATIC FORWARD CURRENT TRANSFER RATIO
vs

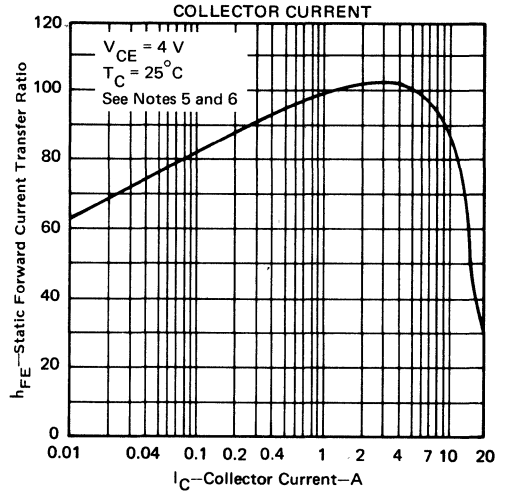


FIGURE 3

BASE-EMITTER VOLTAGE
vs

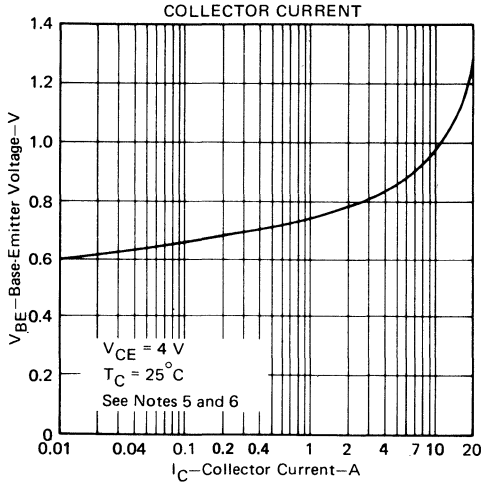


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE
vs

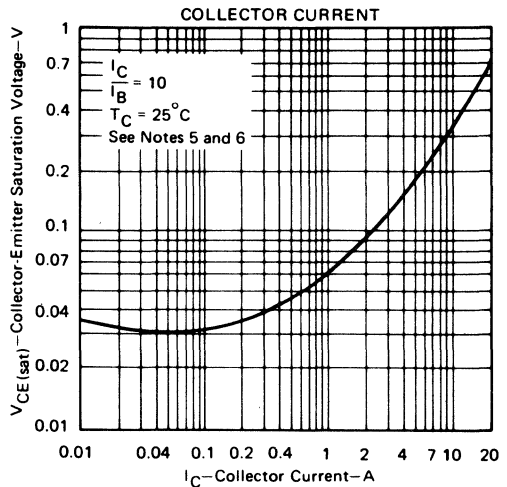


FIGURE 5

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES 2N5939, 2N5940 N-P-N SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

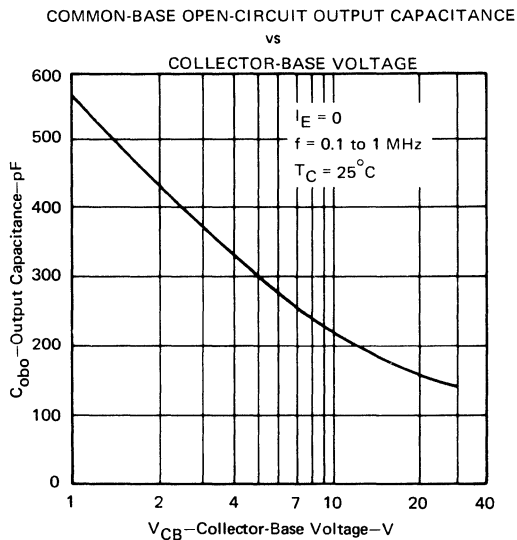


FIGURE 6

5

MAXIMUM SAFE OPERATING AREA

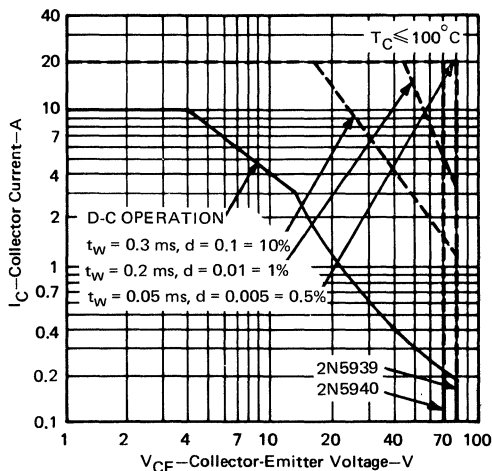


FIGURE 7

TYPES 2N5939, 2N5940

N-P-N SILICON POWER TRANSISTORS

THERMAL INFORMATION

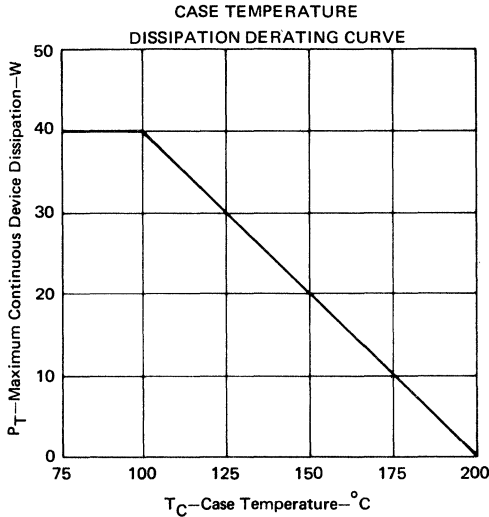


FIGURE 8

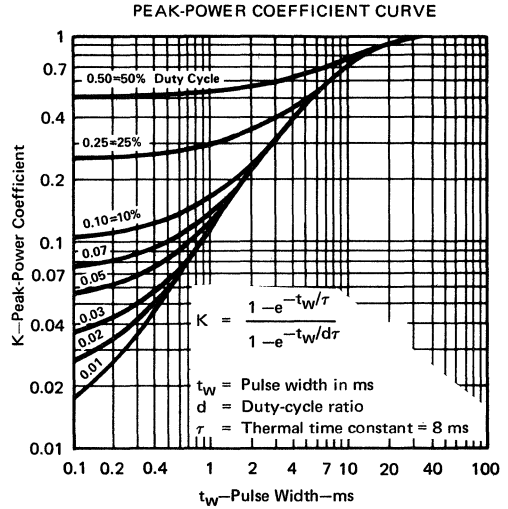


FIGURE 9

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	87.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	2.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta CA}$	Case-to-Free-Air Thermal Resistance	85.0	$^{\circ}\text{C}/\text{W}$
$R_{\theta CHS}$	Case-to-Heat-Sink Thermal Resistance		$^{\circ}\text{C}/\text{W}$
$R_{\theta HSA}$	Heat-Sink-to-Free-Air Thermal Resistance		$^{\circ}\text{C}/\text{W}$
T_A	Free-Air Temperature		$^{\circ}\text{C}$
T_C	Case Temperature		$^{\circ}\text{C}$
$T_{J(av)}$	Average Junction Temperature	≤ 200	$^{\circ}\text{C}$
$T_{J(max)}$	Peak Junction Temperature	≤ 200	$^{\circ}\text{C}$
K	Peak-Power Coefficient	See Figure 9	
t_w	Average Pulse Width		ms
t_x	Pulse Period		ms
d	Duty-Cycle Ratio (t_w/t_x)		

Equation No. 1—Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{R_{\theta JC} + R_{\theta CHS} + R_{\theta HSA}} \quad \text{for } 100^{\circ}\text{C} \leq T_C \leq 200^{\circ}\text{C} \quad \text{as in Figure 8}$$

Equation No. 2—Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{R_{\theta JA}} \quad \text{for } 25^{\circ}\text{C} \leq T_A \leq 200^{\circ}\text{C}$$

Equation No. 3—Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(R_{\theta CHS} + R_{\theta HSA}) + K \cdot R_{\theta JC}} \quad \text{for } 100^{\circ}\text{C} \leq T_C \leq 200^{\circ}\text{C}$$

Equation No. 4—Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d \cdot R_{\theta CA} + K \cdot R_{\theta JC}} \quad \text{for } 25^{\circ}\text{C} \leq T_A \leq 200^{\circ}\text{C}$$

Example—Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$R_{\theta CHS} + R_{\theta HSA} = 3^{\circ}\text{C}/\text{W} \quad (\text{From information supplied with heat sink.})$$

$$T_{J(av)} \text{ (design limit)} = 200^{\circ}\text{C}$$

$$T_A = 50^{\circ}\text{C}$$

$$d = 10\% = 0.1$$

$$t_w = 0.1 \text{ ms}$$

Solution:

From Figure 9, Peak-Power Coefficient

$$K = 0.105 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(R_{\theta CHS} + R_{\theta HSA}) + K \cdot R_{\theta JC}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(3) + 0.105(2.5)} \text{ W} = 267 \text{ W}$$

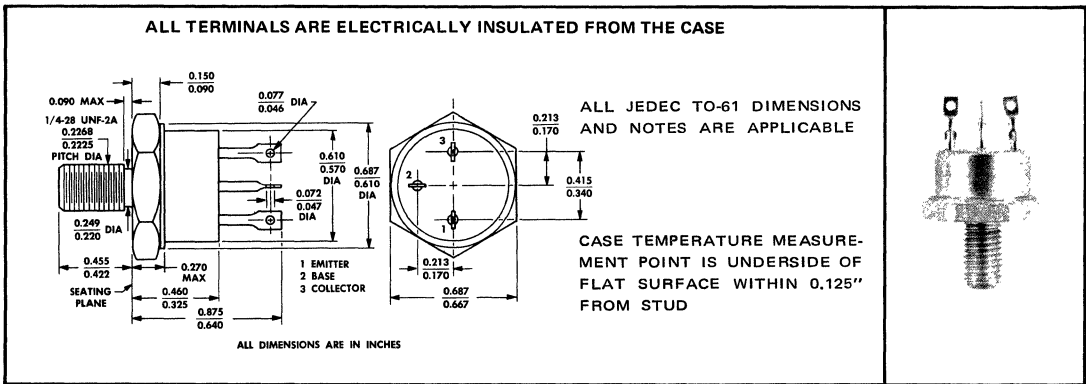
TYPE 2N6127 P-N-P SILICON POWER TRANSISTOR

TYPE 2N6127
BULLETIN NO. D.L.S-711484, JUNE 1971
REVISED NOVEMBER 1971

HIGH-FREQUENCY, HIGH-POWER TRANSISTOR WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- 40 mJ Reverse Energy Rating with $I_C = 20$ A and 4 V Reverse Bias
- Isolated Stud Package
- 100 W at 50°C Case Temperature
- Min f_T of 40 MHz at -5 V, -2 A
- Designed for Complementary Use with 2N6128

***mechanical data**



5

***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

Collector-Base Voltage	-100 V
Collector-Emitter Voltage (See Note 1)	-80 V
Emitter-Base Voltage	-5 V
Continuous Collector Current	-10 A
Peak Collector Current (See Note 2)	-20 A
Continuous Base Current	-3 A
Safe Operating Areas	See Figures 6 and 7
Continuous Device Dissipation at (or below) 50°C Case Temperature (See Note 3)	100 W
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	67 W
Unclamped Inductive Load Energy ($V_{BE(off)} = 0$, See Note 4)	50 mJ
Unclamped Inductive Load Energy ($V_{BE(off)} = 4$ V, See Note 4)	40 mJ
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/8 Inch from Case for 60 Seconds	300°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_{WV} \leq 0.3$ ms, duty cycle ≤ 10 %.
 3. Derate linearly to 200°C case temperature at the rate of 0.67 W/°C.
 4. These ratings are based on the capability of the transistor to operate safely in the circuit of Figure 2.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPE 2N6127

P-N-P SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT	
$V_{(BR)CEO}$	Collector-Emmitter Breakdown Voltage	$I_C = -200 \text{ mA}$, $I_B = 0$, See Note 5	-80		V	
I_{CEO}	Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-100	μA	
I_{CES}	Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$		-10	μA	
		$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$		-1	mA	
		$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-500	μA	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = -4 \text{ V}$, $I_C = 0$		-10	μA	
		$V_{EB} = -5 \text{ V}$, $I_C = 0$		-1	mA	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -100 \text{ mA}$	See Notes 5 and 6	20		
		$V_{CE} = -5 \text{ V}$, $I_C = -5 \text{ A}$		30		120
		$V_{CE} = -5 \text{ V}$, $I_C = -10 \text{ A}$		15		
		$V_{CE} = -5 \text{ V}$, $I_C = -5 \text{ A}$, $T_C = -55^\circ\text{C}$		12		
V_{BE}	Base-Emmitter Voltage	$I_B = -0.5 \text{ A}$, $I_C = -5 \text{ A}$	See Notes 5 and 6	-1.8	V	
		$V_{CE} = -5 \text{ V}$, $I_C = -5 \text{ A}$		-1.8		
		$V_{CE} = -5 \text{ V}$, $I_C = -10 \text{ A}$		-2.2		
$V_{CE(sat)}$	Collector-Emmitter Saturation Voltage	$I_B = -0.5 \text{ A}$, $I_C = -5 \text{ A}$	See Notes 5 and 6	-0.9	V	
		$I_B = -1 \text{ A}$, $I_C = -10 \text{ A}$		-2.2		
h_{fe}	Small-Signal Common-Emmitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 1 \text{ kHz}$	20			
$ h_{fe} $	Small-Signal Common-Emmitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -2 \text{ A}$, $f = 20 \text{ MHz}$	2			
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$		500	pF	

NOTES: 5. These parameters must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction to Case Thermal Resistance	1.5	$^\circ\text{C/W}$

switching characteristics at 25°C case temperature

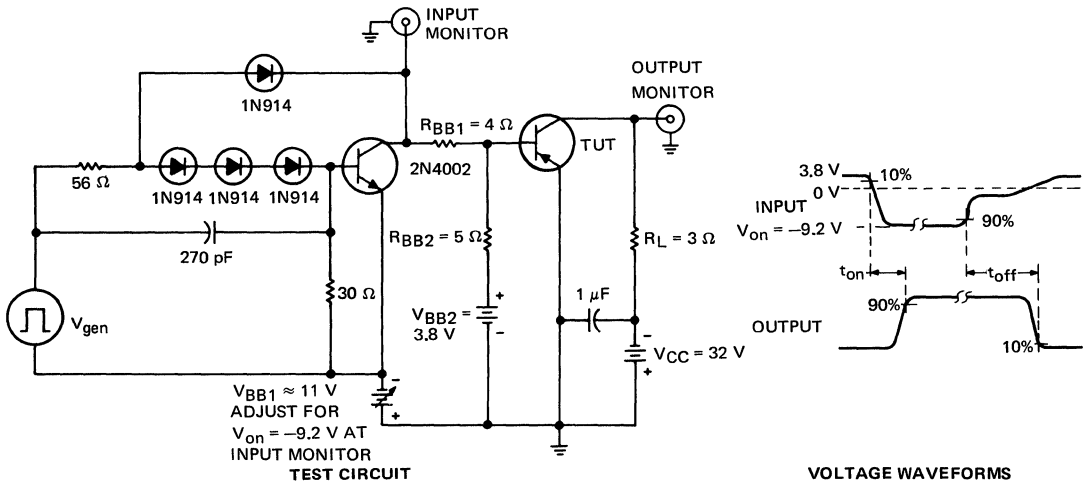
PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -10 \text{ A}$, $I_B(1) = -1 \text{ A}$, $I_B(2) = 1 \text{ A}$	0.45	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 3.8 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	0.5	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

TYPE 2N6127 P-N-P SILICON POWER TRANSISTOR

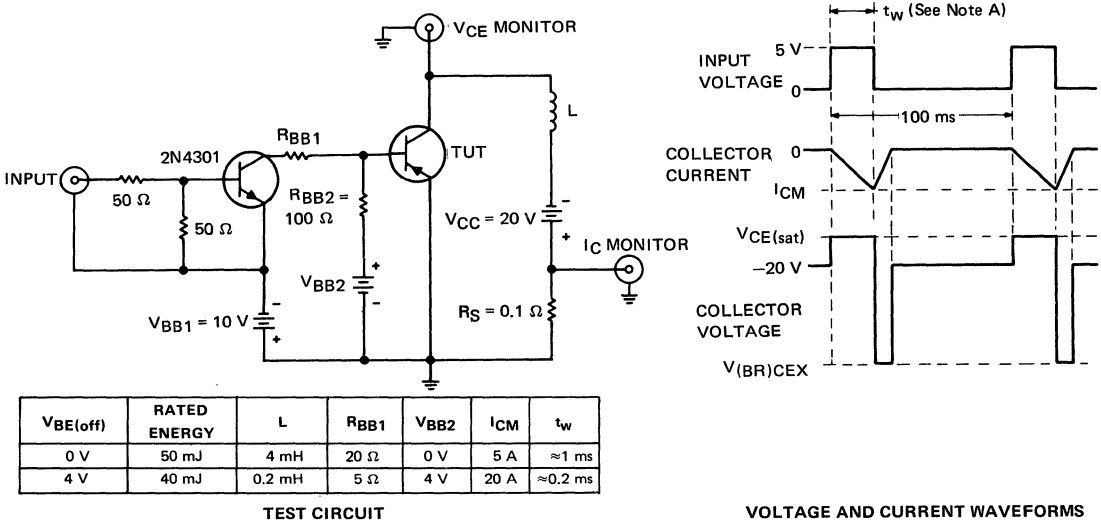
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



NOTE A: Input pulse width is increased until the collector current reaches the specified peak value of I_{CM} .

FIGURE 2

TYPE 2N6127

P-N-P SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

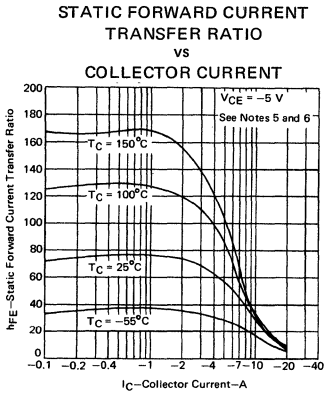


FIGURE 3

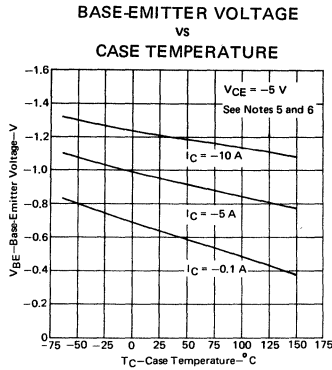


FIGURE 4

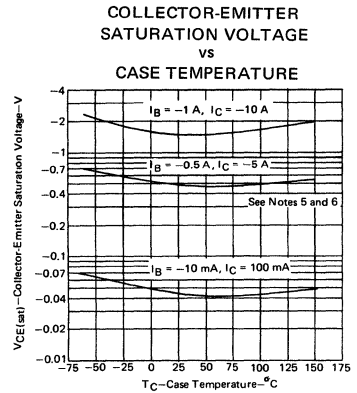


FIGURE 5

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

MAXIMUM SAFE OPERATING AREAS

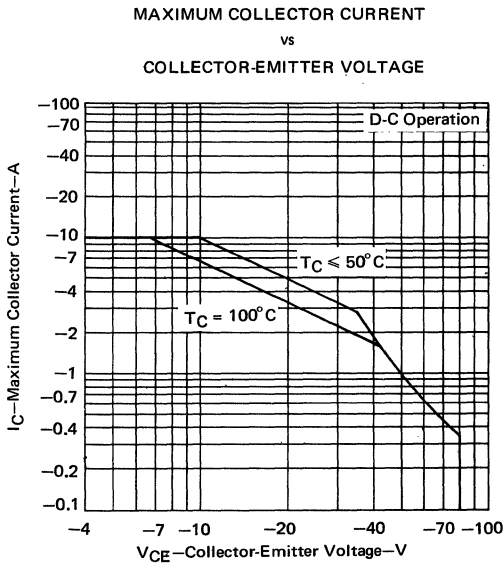


FIGURE 6

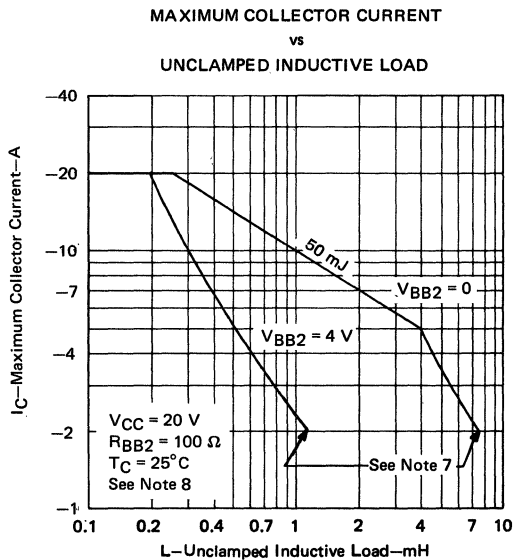


FIGURE 7

NOTES: 7. Above these points the safe operating areas have not been defined.

8. This curve is based on the capability of the transistor to operate safely in the circuit of Figure 2 with $R_{BB1} \approx 10 \cdot V_{BB1}/I_C$.

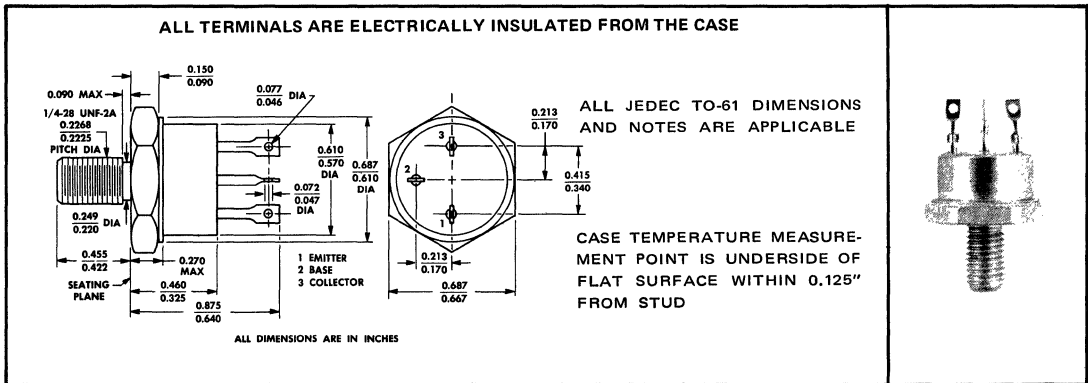
TYPE 2N6128 N-P-N SILICON POWER TRANSISTOR

TYPE 2N6128
BULLETIN NO. DL-S-711485, JUNE 1971
REVISED NOVEMBER 1971

HIGH-FREQUENCY, HIGH-POWER TRANSISTOR WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- 40 mJ Reverse Energy Rating with $I_C = 20$ A and 4 V Reverse Bias
- Isolated Stud Package
- 100 W at 50°C Case Temperature
- Min f_T of 50 MHz at 5 V, 2 A
- Designed for Complementary Use with 2N6127

*mechanical data



5

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 1)	80 V
Emitter-Base Voltage	6 V
Continuous Collector Current	10 A
Peak Collector Current (See Note 2)	20 A
Continuous Base Current	3 A
Safe Operating Areas	See Figures 6 and 7
Continuous Device Dissipation at (or below) 50°C Case Temperature (See Note 3)	100 W
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	67 W
Unclamped Inductive Load Energy ($V_{BE(off)} = 0$, See Note 4)	50 mJ
Unclamped Inductive Load Energy ($V_{BE(off)} = -4$ V, See Note 4)	40 mJ
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/8 Inch from Case for 60 Seconds	300°C

- NOTES: 1. This value applies when the base-emitter-diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.67 W/°C.
 4. These ratings are based on the capability of the transistor to operate safely in the circuit of Figure 2.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPE 2N6128

N-P-N SILICON POWER TRANSISTOR

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$	See Note 5	80		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$			100	μA
I_{CES}	Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$			10	μA
		$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$			1	mA
		$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$			500	μA
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$			10	μA
		$V_{EB} = 6 \text{ V}$, $I_C = 0$			1	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 100 \text{ mA}$	See Notes 5 and 6		20	
		$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$		30	120	
		$V_{CE} = 5 \text{ V}$, $I_C = 10 \text{ A}$		15		
		$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$, $T_C = -55^\circ\text{C}$		12		
V_{BE}	Base-Emitter Voltage	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$	See Notes 5 and 6		1.8	V
		$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$		1.8		
		$V_{CE} = 5 \text{ V}$, $I_C = 10 \text{ A}$		2.2		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$	See Notes 5 and 6		0.9	V
		$I_B = 1 \text{ A}$, $I_C = 10 \text{ A}$		2.2		
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.2 \text{ A}$	$f = 1 \text{ kHz}$	20		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 2 \text{ A}$	$f = 20 \text{ MHz}$	2.5		
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$	$f = 1 \text{ MHz}$		275	pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction to Case Thermal Resistance	1.5	$^\circ\text{C/W}$

switching characteristics at 25°C case temperature

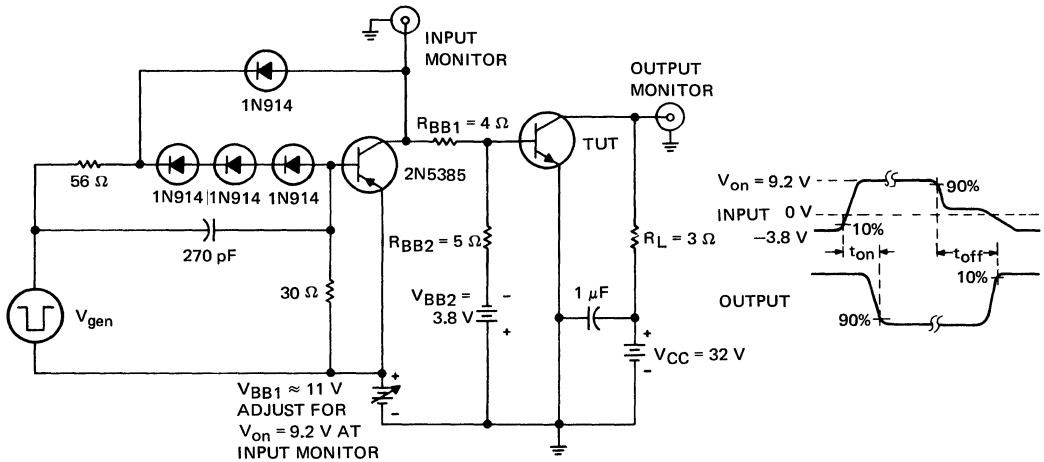
PARAMETER		TEST CONDITIONS†		TYP	UNIT
t_{on}	Turn-On Time	$I_C = 10 \text{ A}$, $I_B(1) = 1 \text{ A}$, $I_B(2) = -1 \text{ A}$		0.5	μs
t_{off}	Turn-Off Time	$V_{BE(off)} = -3.8 \text{ V}$, $R_L = 3 \Omega$	See Figure 1	1.3	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

TYPE 2N6128 N-P-N SILICON POWER TRANSISTOR

PARAMETER MEASUREMENT INFORMATION



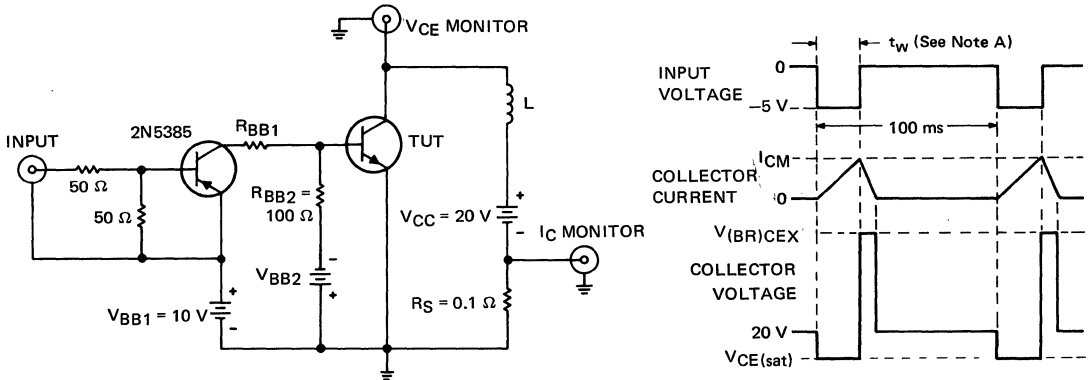
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



$V_{BE(off)}$	RATED ENERGY	L	R_{BB1}	V_{BB2}	I_{CM}	t_w
0 V	50 mJ	4 mH	20 Ω	0 V	5 A	$\approx 1\text{ ms}$
-4 V	40 mJ	0.2 mH	5 Ω	4 V	20 A	$\approx 0.2\text{ ms}$

TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until the collector current reaches the specified peak value of I_{CM} .

FIGURE 2

TYPE 2N6128 N-P-N SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

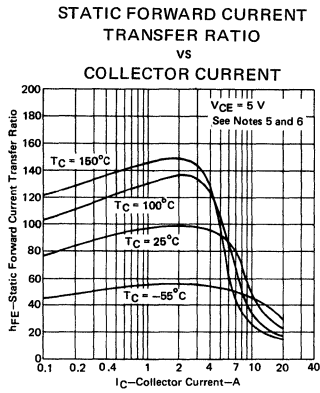


FIGURE 3

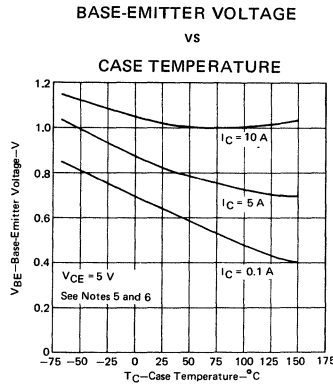


FIGURE 4

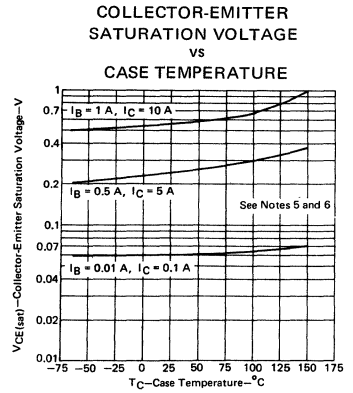


FIGURE 5

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

MAXIMUM SAFE OPERATING AREAS

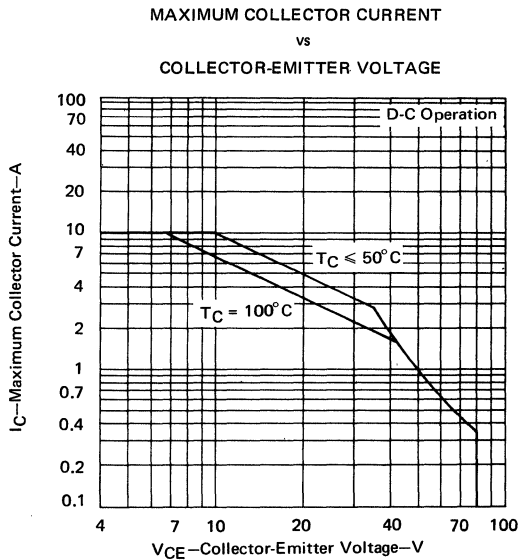


FIGURE 6

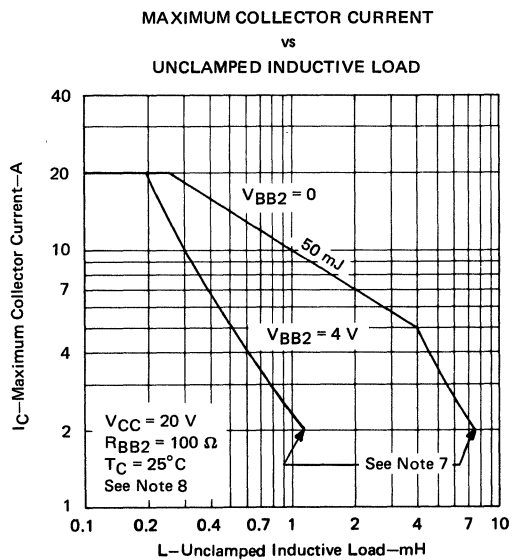


FIGURE 7

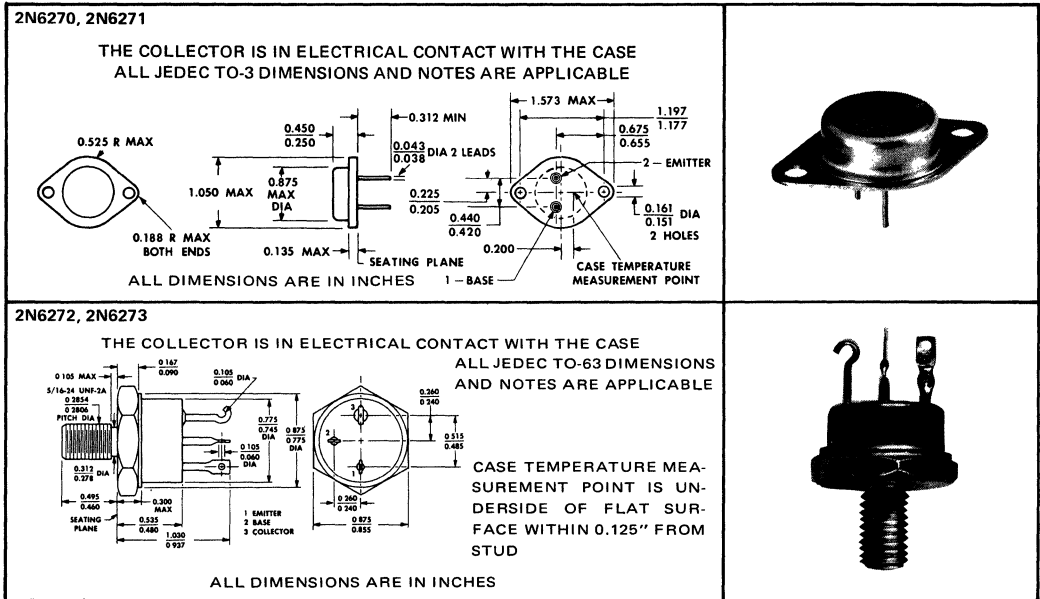
- NOTES: 7. Above these points the safe operating areas have not been defined.
8. This curve is based on the capability of the transistor to operate safely in the circuit of Figure 2 with $R_{BB1} \approx 10 \cdot V_{BB1}/I_C$.

TYPES 2N6270, 2N6271, 2N6272, 2N6273 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED SWITCHING APPLICATIONS

- 100-mJ Reverse-Energy Rating
- 30-A Rated Continuous Collector Current
- 150 Watts at 100°C Case Temperature
- Min f_T of 75 MHz at 10 V, 1 A

*mechanical data



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N6270	2N6271
Collector-Base Voltage	100 V	120 V
Collector-Emitter Voltage (See Note 1)	80 V	100 V
Emitter-Base Voltage	8 V	8 V
Continuous Collector Current	← 30 A →	← 30 A →
Peak Collector Current (See Note 2)	← 40 A →	← 40 A →
Continuous Base Current	← 10 A →	← 10 A →
Safe Operating Areas	See Figures 6 and 7	
Unclamped Inductive Load Energy (See Note 3 and Figure 7)	← 100 mJ →	← 100 mJ →
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 4)	← 150 W →	← 150 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 5)	← 5 W →	← 5 W →
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 5. $L = 1$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V, Energy $\approx I_C^2 L/2$.
 4. For operation above 100°C case temperature, refer to Dissipation Derating Curve, Figure 8.
 5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 9.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication..

TYPES 2N6270, 2N6271, 2N6272, 2N6273
BULLETIN NO. DL-S-711531, NOVEMBER 1971



TYPES 2N6270, 2N6271, 2N6272, 2N6273

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N6270		2N6271		UNIT
		2N6272	MIN	MAX	MIN	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	80			100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$ $V_{CE} = 50 \text{ V}$, $I_B = 0$		1		1	mA
I_{CES} Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$ $V_{CE} = 120 \text{ V}$, $V_{BE} = 0$ $V_{CE} = 60 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		1		1	mA
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$ $V_{EB} = 8 \text{ V}$, $I_C = 0$		0.1		0.1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 6 and 7 $V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$, See Notes 6 and 7	20	100	20	100	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$, See Notes 6 and 7		2.2		2.2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1.5 \text{ A}$, $I_C = 15 \text{ A}$, See Notes 6 and 7 $I_B = 6 \text{ A}$, $I_C = 30 \text{ A}$, See Notes 6 and 7		1		1	V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	30		30		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 5 \text{ MHz}$	15		15		

*JEDEC registered data

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	2N6270		2N6271		UNIT
		2N6272	TYP	TYP	TYP	
t_{on} Turn-On Time	$I_C = 15 \text{ A}$, $I_B(1) = 1.2 \text{ A}$, $I_B(2) = -1.2 \text{ A}$,		0.5		0.5	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -6.3 \text{ V}$, $R_L = 2 \Omega$, See Figure 1		1.3		1.3	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPICAL CHARACTERISTICS

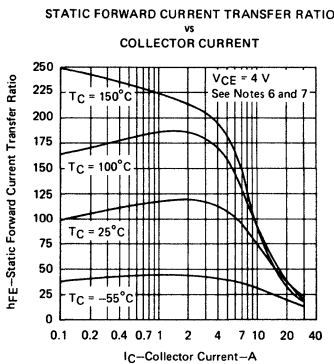


FIGURE 1

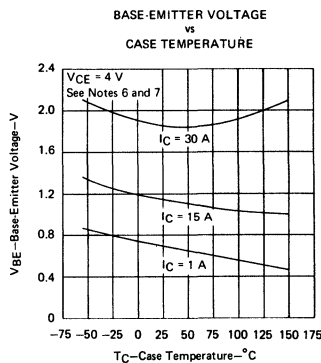


FIGURE 2

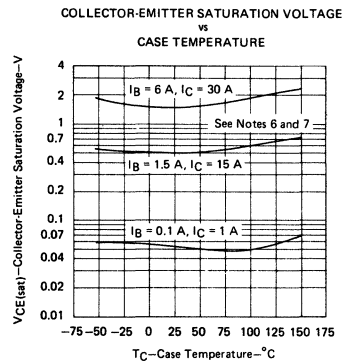


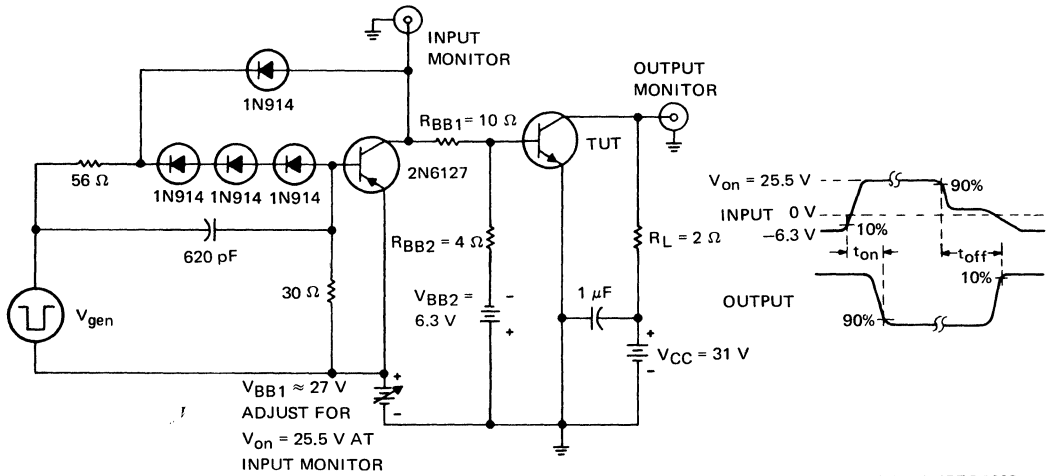
FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N6270, 2N6271, 2N6272, 2N6273 N-P-N SILICON POWER TRANSISTORS

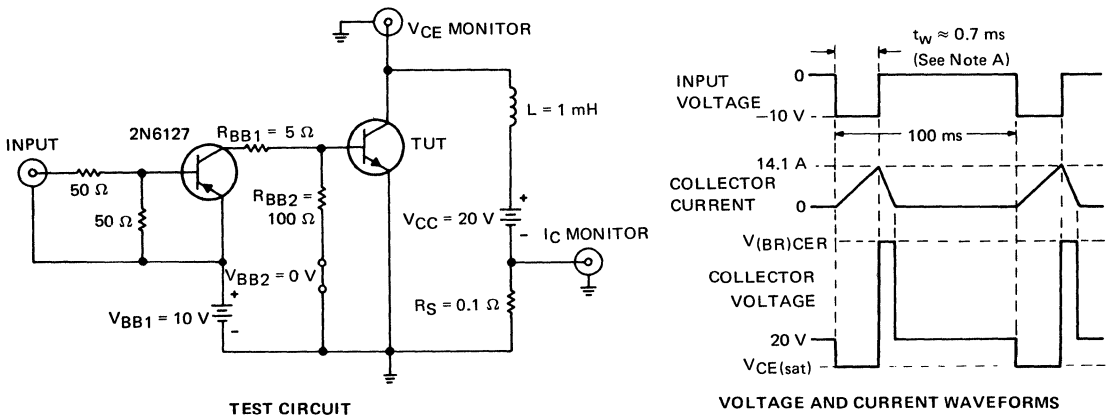
PARAMETER MEASUREMENT INFORMATION



- NOTES:**
- A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - D. Resistors must be noninductive types.
 - E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 4

INDUCTIVE LOAD SWITCHING



NOTE A: Input pulse width is increased until $I_{CM} = 14.1\text{ A}$.

FIGURE 5

TYPES 2N6270, 2N6271, 2N6272, 2N6273 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

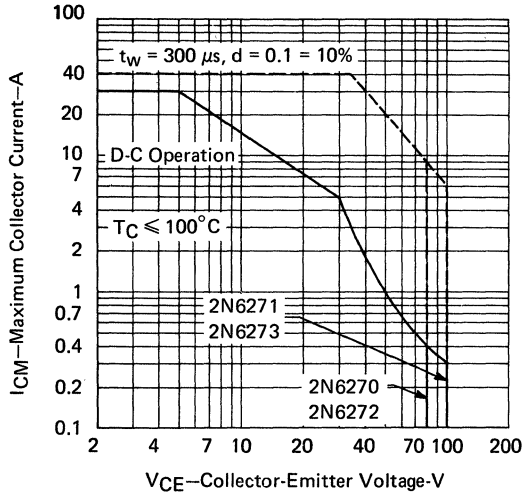


FIGURE 6

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

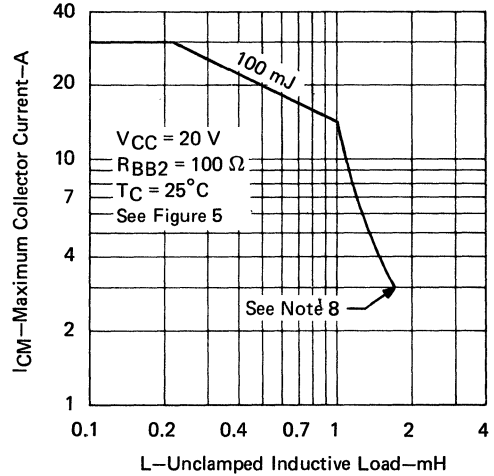


FIGURE 7

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

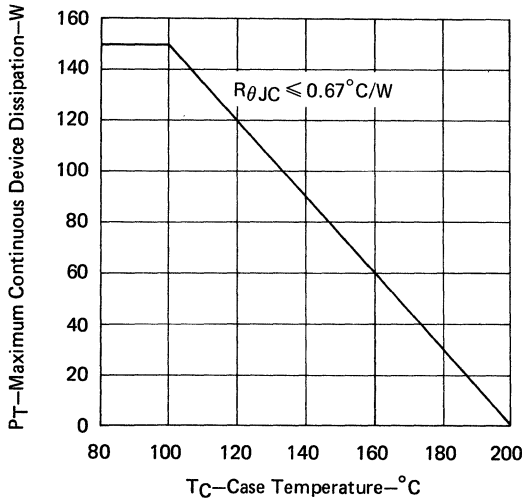


FIGURE 8

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

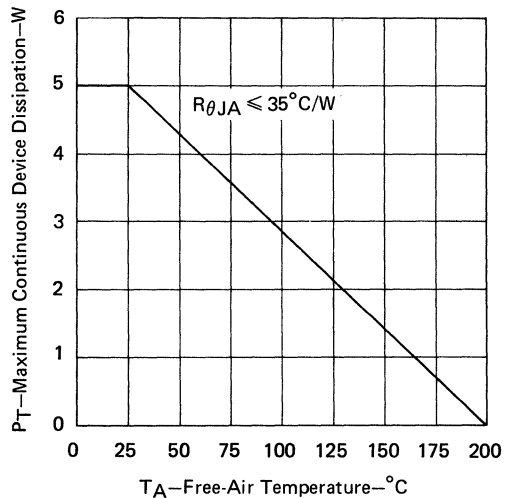


FIGURE 9

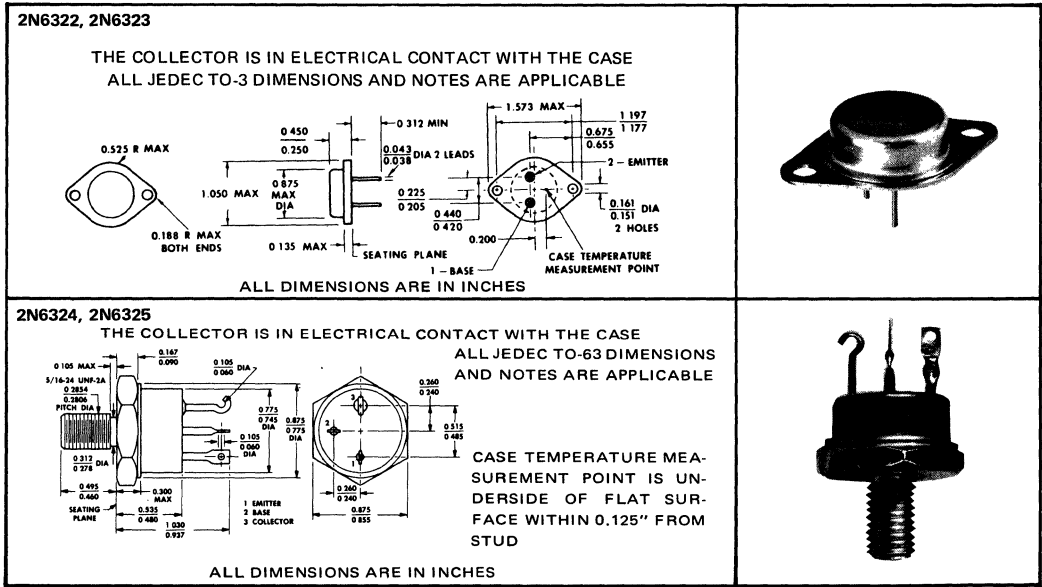
TYPES 2N6322 THRU 2N6325 N-P-N SILICON POWER TRANSISTORS

TYPES 2N6322 THRU 2N6325
BULLETIN NO. DLS-7211989, JANUARY 1972

HIGH VOLTAGE, HIGH FORWARD AND REVERSE ENERGY
DESIGNED FOR INDUSTRIAL AND MILITARY APPLICATIONS

- 100-mJ Reverse-Energy Rating
- 30-A Rated Continuous Collector Current
- 200 Watts at 100°C Case Temperature
- Min $V(BR)_{CEO}$ of 300 V (2N6323, 2N6325)

*mechanical data



*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N6322	2N6323
Collector-Base Voltage	300 V	400 V
Collector-Emitter Voltage (See Note 1)	200 V	300 V
Emitter-Base Voltage	5 V	5 V
Continuous Collector Current	← 30 A →	← 30 A →
Peak Collector Current (See Note 2)	← 40 A →	← 40 A →
Continuous Base Current	← 10 A →	← 10 A →
Safe Operating Areas	See Figures 6 and 7	
Unclamped Inductive Load Energy (See Note 3 and Figure 7)	← 100 mJ →	← 100 mJ →
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 4)	← 200 W →	← 200 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 5)	← 5 W →	← 5 W →
Operating Collector Junction Temperature Range	-65°C to 200°C	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 230°C →	← 230°C →

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 5. $L = 30$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V, Energy $\approx I_C^2 L/2$.
 4. For operation above 100°C case temperature, refer to Dissipation Derating Curve, Figure 8.
 5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 9.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication..

TYPES 2N6322 THRU 2N6325

N-P-N SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N6322		2N6323		UNIT	
		2N6324	2N6325	MIN	MAX		
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	200	300			V	
I_{CEO} Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $I_B = 0$ $V_{CE} = 150 \text{ V}$, $I_B = 0$	5		5		mA	
I_{CES} Collector Cutoff Current	$V_{CE} = 300 \text{ V}$, $V_{BE} = 0$ $V_{CE} = 400 \text{ V}$, $V_{BE} = 0$ $V_{CE} = 200 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	2		2		mA	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	5		5		mA	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$ $V_{CE} = 5 \text{ V}$, $I_C = 20 \text{ A}$ $V_{CE} = 5 \text{ V}$, $I_C = 30 \text{ A}$	See Notes 6 and 7		40	150	30	150
V_{BE} Base-Emitter Voltage	$V_{CE} = 5 \text{ V}$, $I_C = 30 \text{ A}$, See Notes 6 and 7	2.5		2.5		V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$ $I_B = 2 \text{ A}$, $I_C = 20 \text{ A}$ $I_B = 6 \text{ A}$, $I_C = 30 \text{ A}$	See Notes 6 and 7		0.5	0.5	1.5	1.5
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	35		30			
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 5 \text{ MHz}$	2		2			

*JEDEC registered data

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 20 \text{ A}$, $I_B(1) = 2 \text{ A}$, $I_B(2) = -2 \text{ A}$, $V_{BE(off)} \approx -3 \text{ V}$, $R_L = 2 \Omega$, See Figure 4	0.8	μs
t_{off} Turn-Off Time		3	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

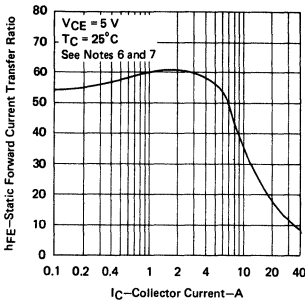


FIGURE 1

BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT

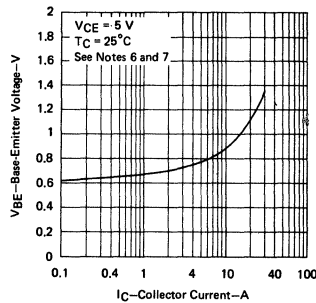


FIGURE 2

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

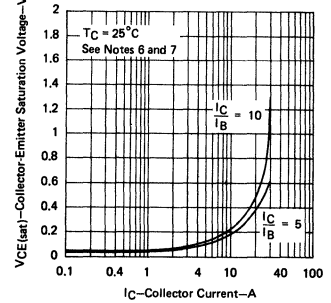


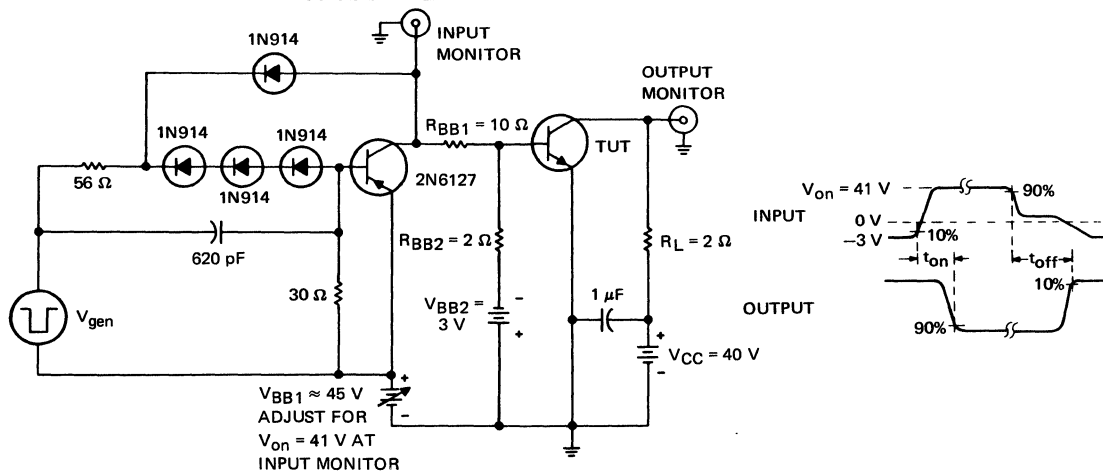
FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES 2N6322 THRU 2N6325 N-P-N SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



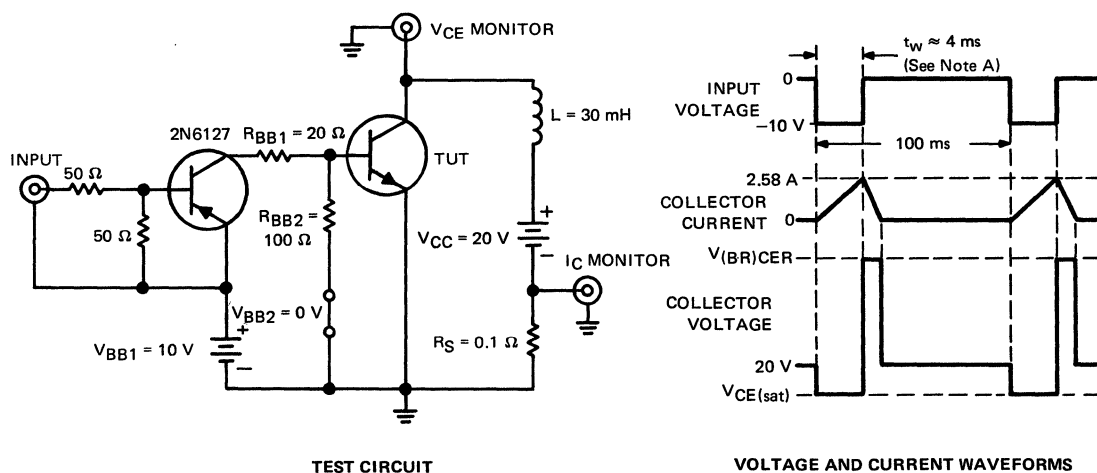
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES:
- V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 4

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = 2.58\text{ A}$.

FIGURE 5

TYPES 2N6322 THRU 2N6325 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

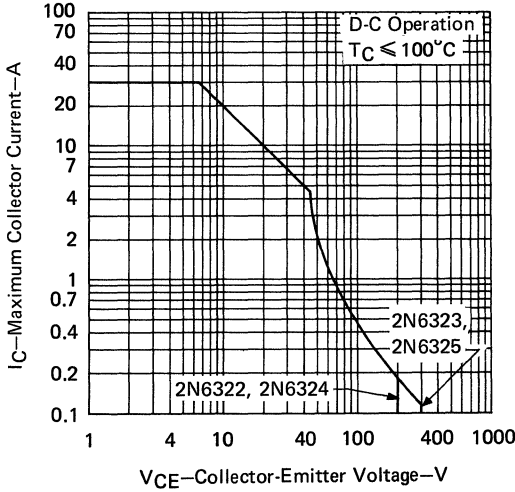


FIGURE 6

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

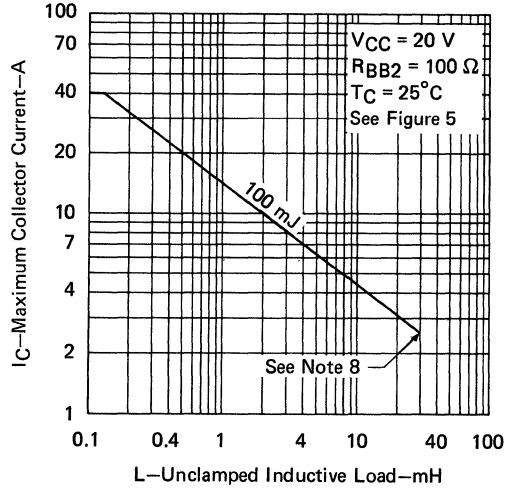


FIGURE 7

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

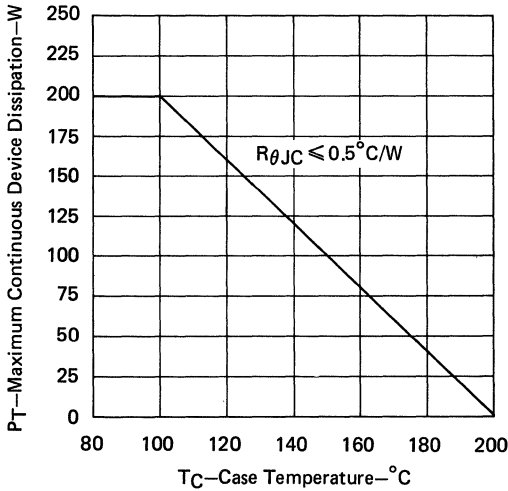


FIGURE 8

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

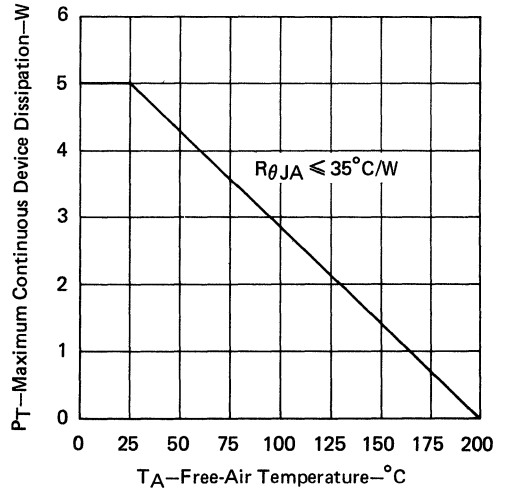


FIGURE 9

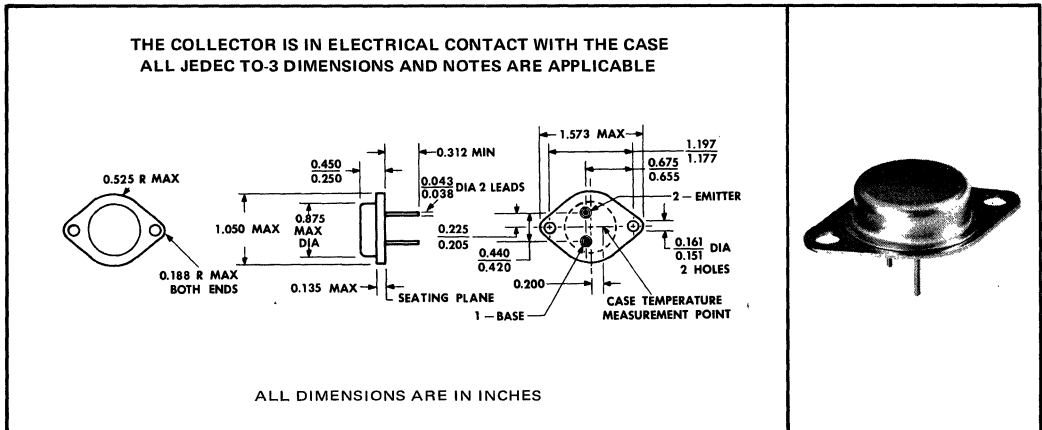
TYPES 2N6326, 2N6327, 2N6328 N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPES 2N6326, 2N6327, 2N6328
BULLETIN NO. DL-S-7211655, JANUARY 1972

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N6329, 2N6330, 2N6331

- 200 W at 25°C Case Temperature
- 30-A Rated Collector Current
- 200-mJ Reverse Energy Rating
- High SOA Capability, 20 V and 10 A

*mechanical data



5

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N6326	2N6327	2N6328
Collector-Base Voltage	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	60 V	80 V	100 V
Emitter-Base Voltage	5 V	5 V	5 V
Continuous Collector Current	← 30 A →		
Peak Collector Current (See Note 2)	← 40 A →		
Continuous Base Current	← 10 A →		
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 3 and 4 →		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 200 W →		
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	← 114 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →		
Unclamped Inductive Load Energy (See Note 5)	← 200 mJ →		
Operating Collector Junction Temperature Range	← -65°C to 200°C →		
Storage Temperature Range	← -65°C to 200°C →		
Terminal Temperature 1/8 Inch from Case for 10 Seconds	← 250°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_{W} \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1.14 W/°C or refer to Dissipation Derating Curve, Figure 5.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C or refer to Dissipation Derating Curve, Figure 6.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L / 2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N6326, 2N6327, 2N6328

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N6326		2N6327		2N6328		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	60		80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$		1					mA
	$V_{CE} = 40 \text{ V}$, $I_B = 0$				1			
	$V_{CE} = 50 \text{ V}$, $I_B = 0$					1		
I_{CES} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$		0.5					mA
	$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$				0.5			
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$					0.5		
	$V_{CE} = 30 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		5					
	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$				5			
	$V_{CE} = 50 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$					5		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$,		0.5		0.5		0.5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$		25		25		25	
	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$		12		12		12	
	$V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$		6	30	6	30	6	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$		2		2		2	V
	$V_{CE} = 4 \text{ V}$, $I_C = 30 \text{ A}$		4		4		4	
$V_{CE(sat)}$ Collector-Emitter Voltage	$I_B = 2 \text{ A}$, $I_C = 15 \text{ A}$		1.5		1.5		1.5	V
	$I_B = 7.5 \text{ A}$, $I_C = 30 \text{ A}$		3		3		3	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$		30		30		30	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ MHz}$		3		3		3	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

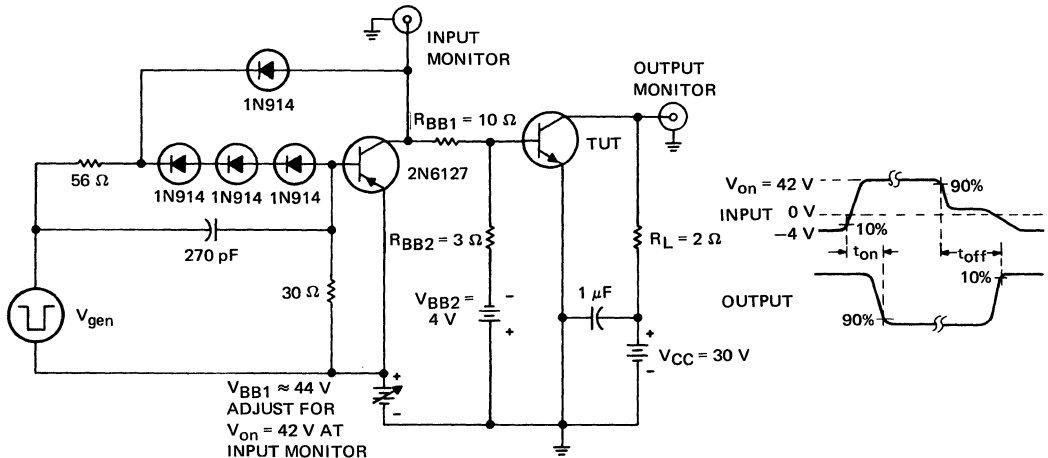
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS [†]	TYP	UNIT
t_{on} Turn-On Time	$I_C = 15 \text{ A}$, $I_B(1) = 2 \text{ A}$, $I_B(2) = -2 \text{ A}$,	0.6	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -4 \text{ V}$, $R_L = 2 \Omega$, See Figure 1	0.9	

[†]Voltage and current values shown are nominal, exact values vary slightly with transistor parameters.

TYPES 2N6326, 2N6327, 2N6328 N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



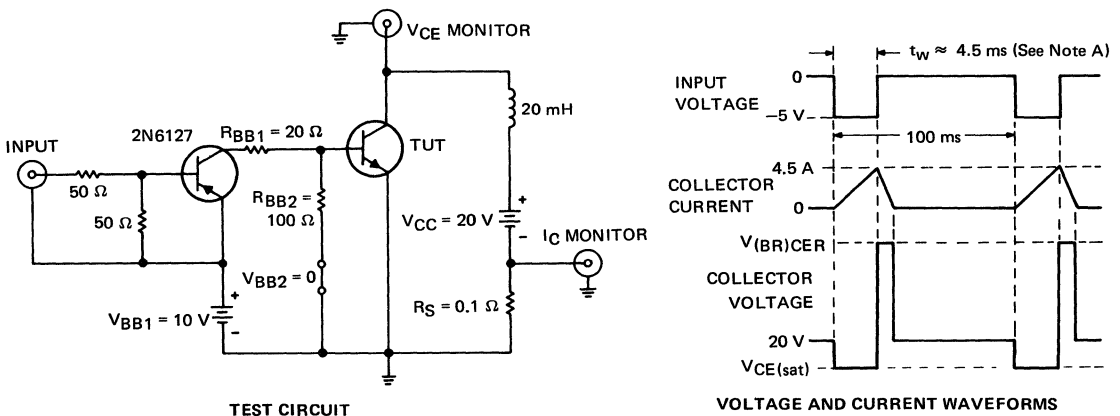
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = 4.5\text{ A}$.

FIGURE 2

TYPES 2N6326, 2N6327, 2N6328

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

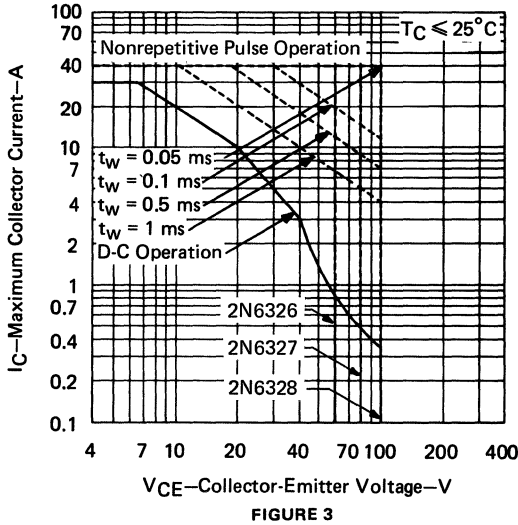


FIGURE 3

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

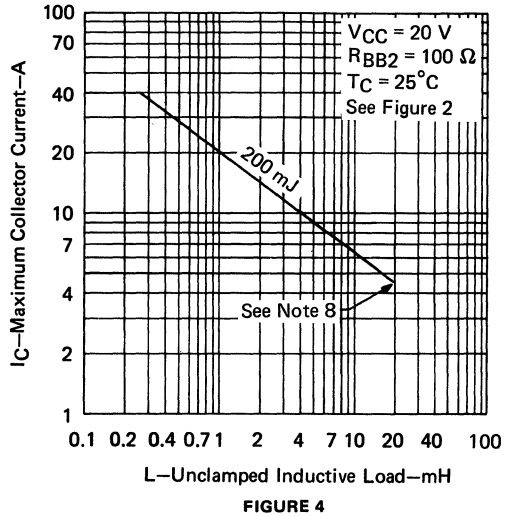


FIGURE 4

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

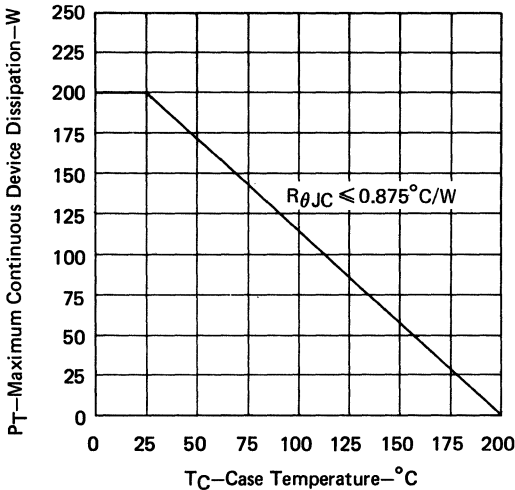


FIGURE 5

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

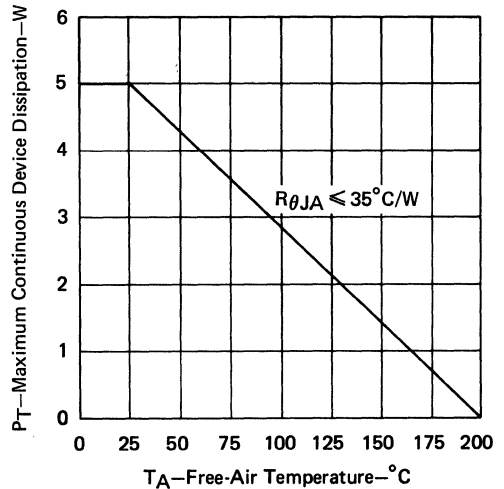


FIGURE 6

TYPES 2N6329, 2N6330, 2N6331 P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

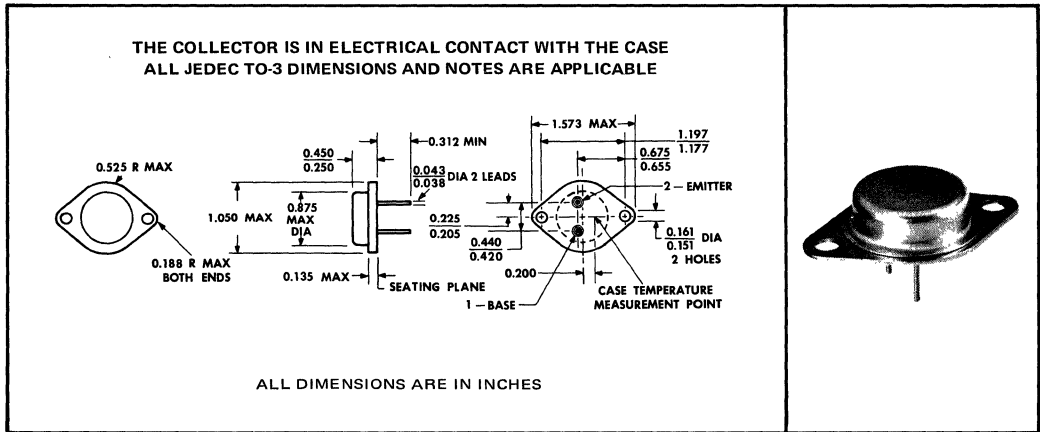
FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N6326, 2N6327, 2N6328

- 200 W at 25°C Case Temperature
- 30-A Rated Collector Current
- 200-mJ Reverse Energy Rating
- High SOA Capability, 20 V and 10 A

TYPES 2N6329, 2N6330, 2N6331
BULLETIN NO. DL-57211654, JANUARY 1972

5

***mechanical data**



***absolute maximum ratings at 25°C case temperature (unless otherwise noted)**

	2N6329	2N6330	2N6331
Collector-Base Voltage	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-60 V	-80 V	-100 V
Emitter-Base Voltage	-5 V	-5 V	-5 V
Continuous Collector Current	← -30 A →		
Peak Collector Current (See Note 2)	← -40 A →		
Continuous Base Current	← -10 A →		
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 3 and 4 →		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 200 W →		
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	← 114 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →		
Unclamped Inductive Load Energy (See Note 5)	← 200 mJ →		
Operating Collector Junction Temperature Range	← -65°C to 200°C →		
Storage Temperature Range	← -65°C to 200°C →		
Terminal Temperature 1/8 Inch from Case for 10 Seconds	← 250°C →		

- NOTES: 1. These value apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 1$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1.14 W/°C or refer to Dissipation Derating Curve, Figure 5.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C or refer to Dissipation Derating Curve, Figure 6.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L / 2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N6329, 2N6330, 2N6331

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N6329	2N6330	2N6331	UNIT
		MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-60	-80	-100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-1			mA
	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-1		
	$V_{CE} = -50 \text{ V}$, $I_B = 0$			-1	
I_{CES} Collector Cutoff Current	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$	-0.5			mA
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 0$		-0.5		
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$			-0.5	
	$V_{CE} = -30 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	-5			
	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-5		
	$V_{CE} = -50 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$			-5	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$,	-0.5	-0.5	-0.5	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -5 \text{ A}$	25	25	25	
	$V_{CE} = -4 \text{ V}$, $I_C = -15 \text{ A}$	12	12	12	
	$V_{CE} = -4 \text{ V}$, $I_C = -30 \text{ A}$	6 30	6 30	6 30	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -15 \text{ A}$	-2	-2	-2	V
	$V_{CE} = -4 \text{ V}$, $I_C = -30 \text{ A}$	-4	-4	-4	
$V_{CE(sat)}$ Collector-Emitter Voltage	$I_B = -2 \text{ A}$, $I_C = -15 \text{ A}$	-1.5	-1.5	-1.5	V
	$I_B = -7.5 \text{ A}$, $I_C = -30 \text{ A}$	-3	-3	-3	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$	30	30	30	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ MHz}$	3	3	3	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

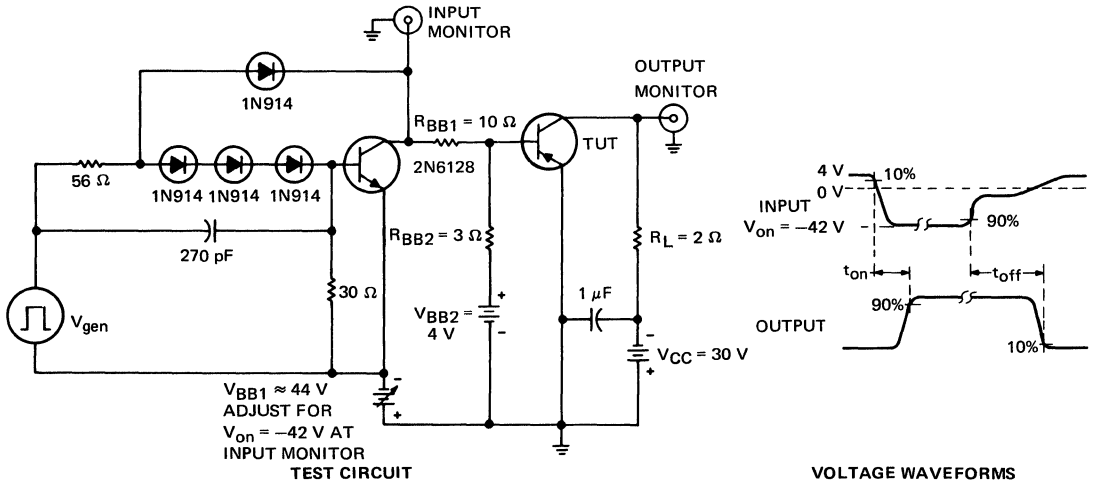
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -15 \text{ A}$, $I_{B(1)} = -2 \text{ A}$, $I_{B(2)} = 2 \text{ A}$,	0.6	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 4 \text{ V}$, $R_L = 2 \Omega$, See Figure 1	0.9	

†Voltage and current values shown are nominal, exact values vary slightly with transistor parameters.

TYPES 2N6329, 2N6330, 2N6331 P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

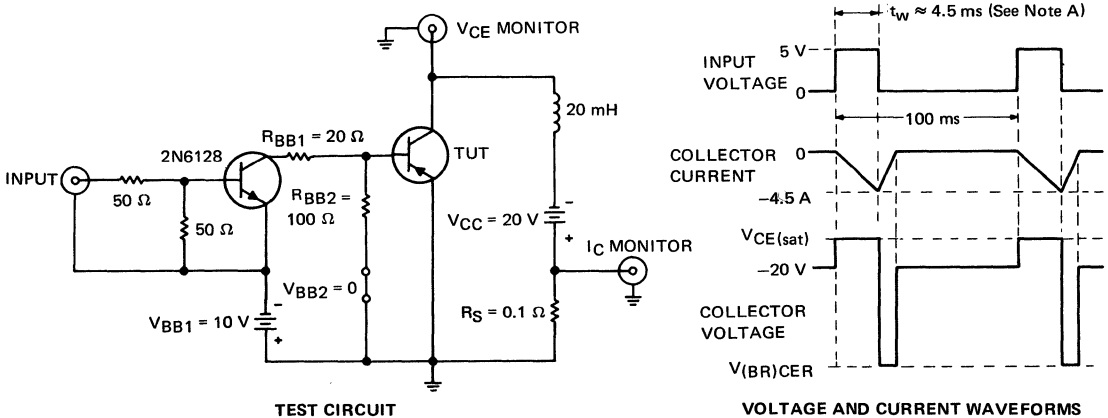
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



NOTE A: Input pulse width is increased until $I_{CM} = -4.5$ A.

FIGURE 2

TYPES 2N6329, 2N6330, 2N6331

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

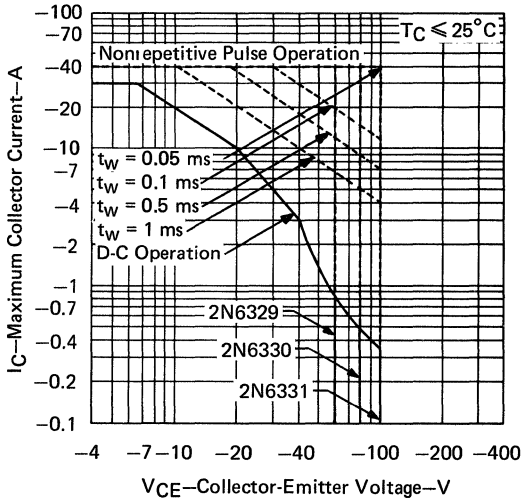


FIGURE 3

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

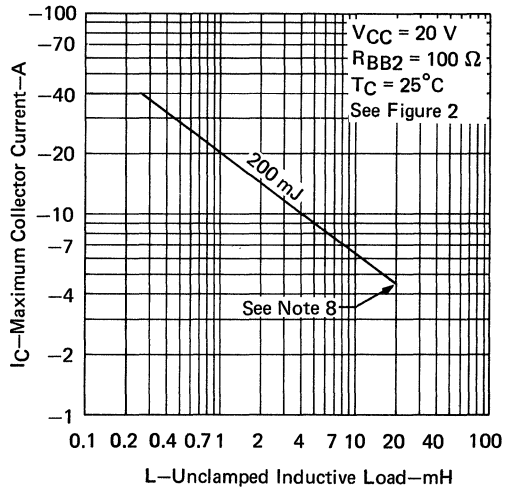


FIGURE 4

NOTE 8: Above this point the safe operating area has not been defined:

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

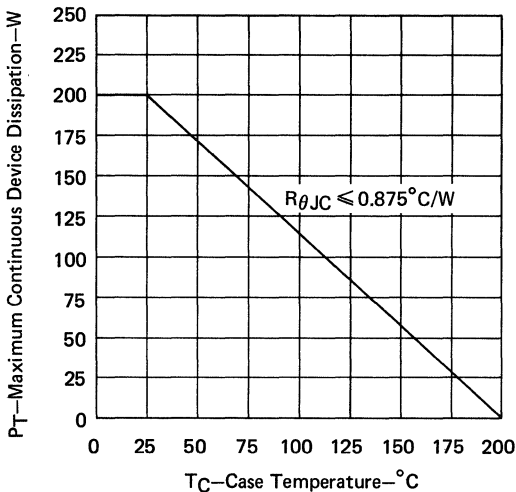


FIGURE 5

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

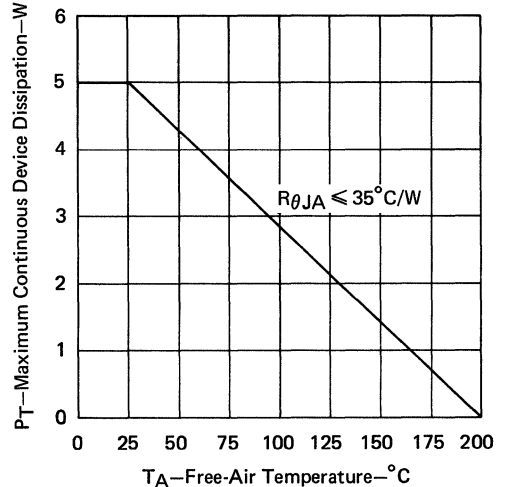


FIGURE 6

TYPES TI486, TI487

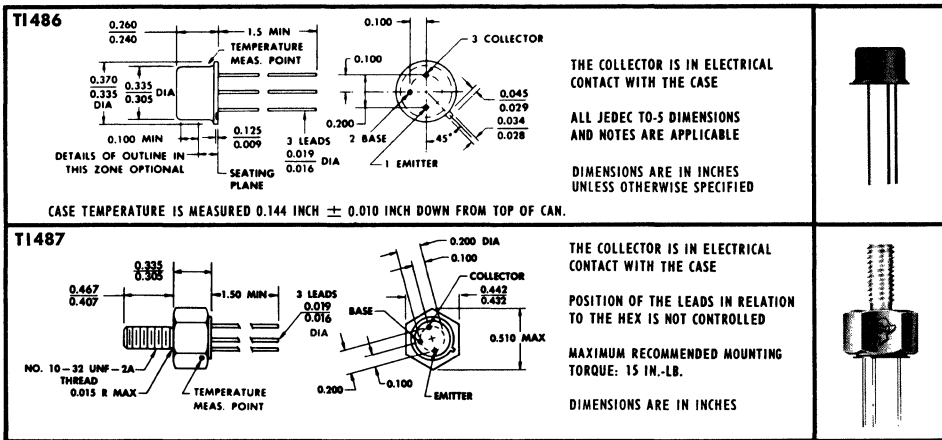
N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPES TI 486, TI 487
BULLETIN NO. DL-5 6910496, JANUARY 1969

HIGH-FREQUENCY INTERMEDIATE-POWER TRANSISTORS

- 15 Watts at 100°C Case Temperature
- Typ $V_{CE(sat)}$ of 0.2 V at 200 mA
- Typ V_{BE} of 0.8 V at 200 mA
- Typ f_T of 50 MHz at 10 V, 100 mA

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TI486	TI487
Collector-Base Voltage	← 80 V	→ 80 V
Collector-Emitter Voltage (See Note 1)	← 60 V	→ 60 V
Emitter-Base Voltage	← 6 V	→ 6 V
Continuous Collector Current	← 1 A	→ 1 A
Peak Collector Current (See Note 2)	← 1.5 A	→ 1.5 A
Safe Operating Region at (or below) 100°C Case Temperature	See Figure 8	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 15 W	→ 15 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	1 W	2 W
Operating Case Temperature Range	← -65°C to 200°C →	
Storage Temperature Range	← -65°C to 200°C →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 150 mW/deg.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/deg for the TI486 and 11.4 mW/deg for the TI487.

TYPES TI486, TI487

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100 \mu A, I_E = 0$	80			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}, I_B = 0,$ See Note 5	60			V
I_{CES}	Collector Cutoff Current	$V_{CE} = 60 \text{ V}, V_{BE} = 0$			3	μA
		$V_{CE} = 60 \text{ V}, V_{BE} = 0,$ $T_C = 150^\circ C$			300	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 6 \text{ V}, I_C = 0$			20	μA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}, I_C = 200 \text{ mA},$ See Notes 5 and 6	20		80	
V_{BE}	Base-Emitter Voltage	$I_B = 20 \text{ mA}, I_C = 200 \text{ mA},$ See Notes 5 and 6		0.8	2	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 20 \text{ mA}, I_C = 200 \text{ mA},$ See Notes 5 and 6		0.2	2	V
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}, I_C = 100 \text{ mA}, f = 10 \text{ MHz}$		5		
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}, I_E = 0,$ $f = 1 \text{ MHz}$		30		pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300 \mu s,$ duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		TI486	TI487	UNIT
		MAX	MAX	
θ_{J-C}	Junction-to-Case Thermal Resistance	6.67	6.67	deg/W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	87.5	

TYPES TI486, TI487

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 200 \text{ mA}$, $I_{B(1)} = 20 \text{ mA}$, $I_{B(2)} = -20 \text{ mA}$,	0.14	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -3.4 \text{ V}$, $R_L = 150 \Omega$, See Figure 1	2.6	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

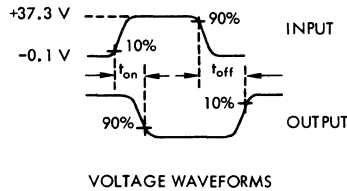
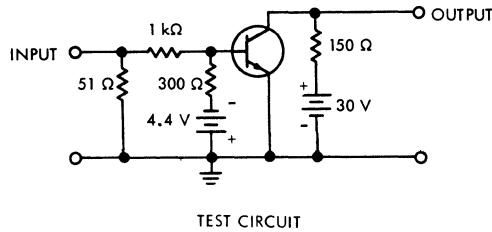


FIGURE 1

- NOTES:
- The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPES TI486, TI487

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

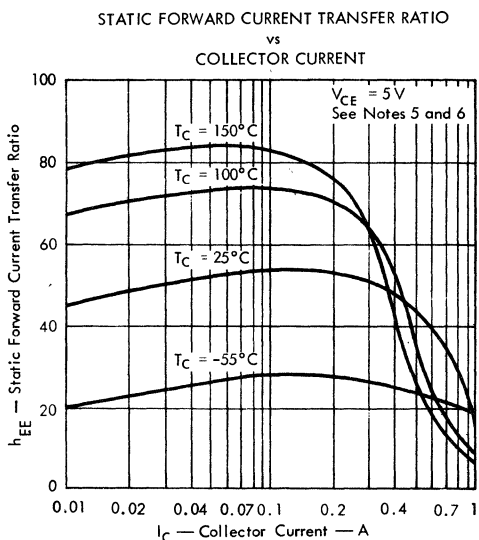


FIGURE 2

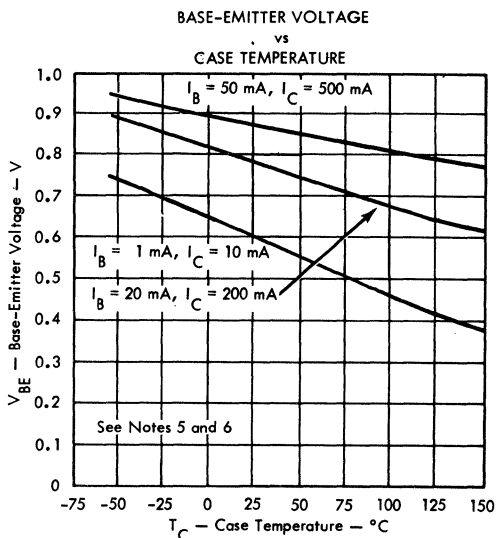


FIGURE 3

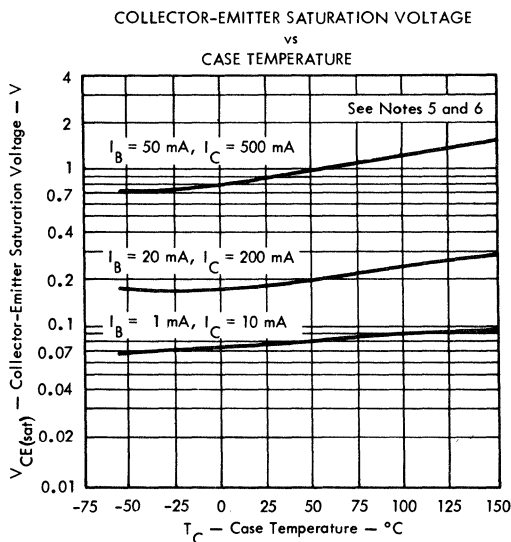


FIGURE 4

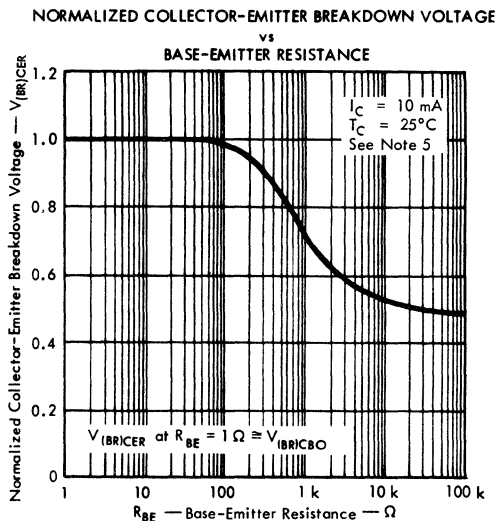


FIGURE 5

NOTES: 5. These parameters must be measured using pulse techniques. $t_p = 300\ \mu s$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TYPES TI486, TI487

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

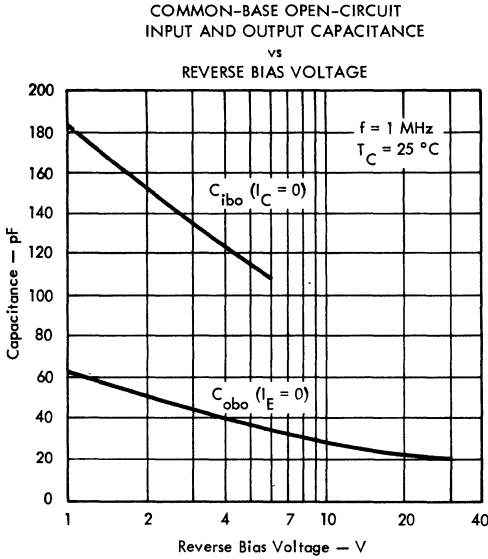


FIGURE 6

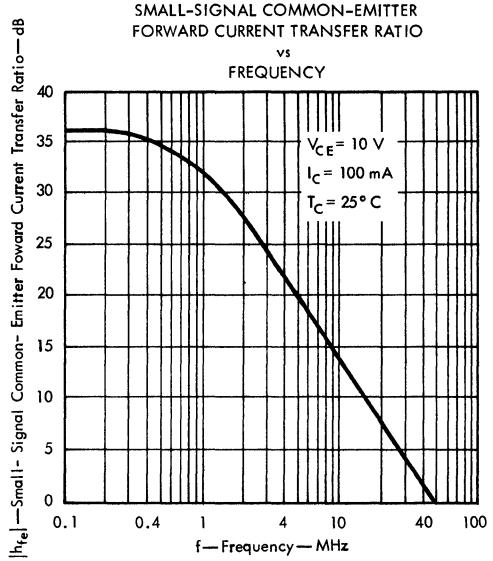


FIGURE 7

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MAXIMUM SAFE OPERATING REGION

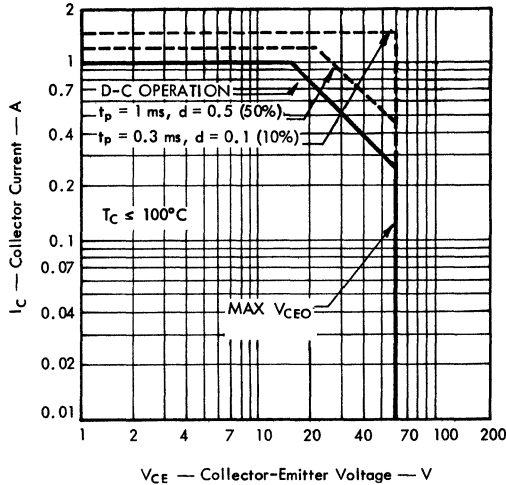


FIGURE 8

TYPES TI486, TI487

N-P-N TRIPLE-DIFFUSED PLANAR SILICON POWER TRANSISTORS

THERMAL INFORMATION

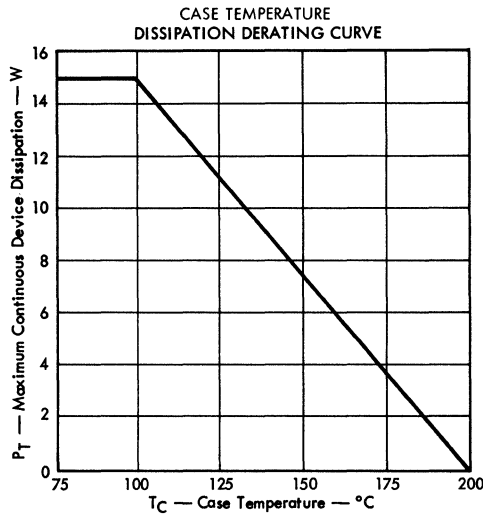


FIGURE 9

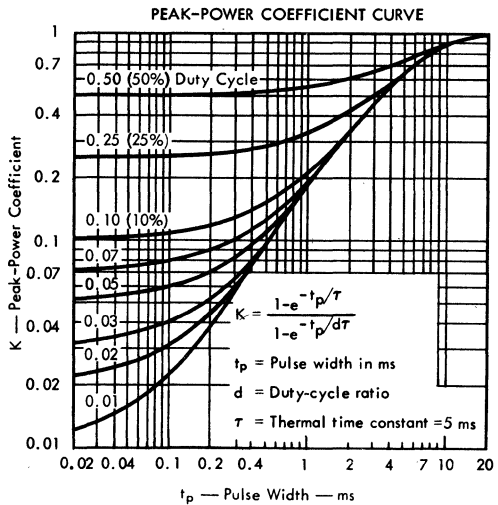


FIGURE 10

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE		UNIT
		TI 486	TI 487	
$P_{T(av)}$	Average Power Dissipation			W
$P_{T(max)}$	Peak Power Dissipation			W
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	175	87.5	deg/W
θ_{J-C}	Junction-to-Case Thermal Resistance	6.67	6.67	deg/W
θ_{C-A}	Case-to-Free-Air Thermal Resistance	168	81	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance			deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance			deg/W
T_A	Free-Air Temperature			°C
T_C	Case Temperature			°C
$T_{J(av)}$	Average Junction Temperature	≤ 200		°C
$T_{J(max)}$	Peak Junction Temperature	≤ 200		°C
K	Peak-Power Coefficient	See Figure 10		
t_p	Pulse Width			ms
t_x	Pulse Period			ms
d	Duty-Cycle Ratio (t_p/t_x)			

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \text{ as in Figure 9 for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-A}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \text{ for } 100^\circ\text{C} \leq T_C \leq 200^\circ\text{C}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}} \text{ for } 25^\circ\text{C} \leq T_A \leq 200^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 7 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 200^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 0.1 \text{ ms}$$

Solution:

From Figure 10, Peak-Power Coefficient

$$K = 0.11 \text{ and by use of equation No. 3}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{200 - 50}{0.1(7) + 0.11(6.67)} = 105 \text{ W}$$

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971

TYPES TI1131, TI1132, TI1133, TI1134, TI1135, TI1136 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

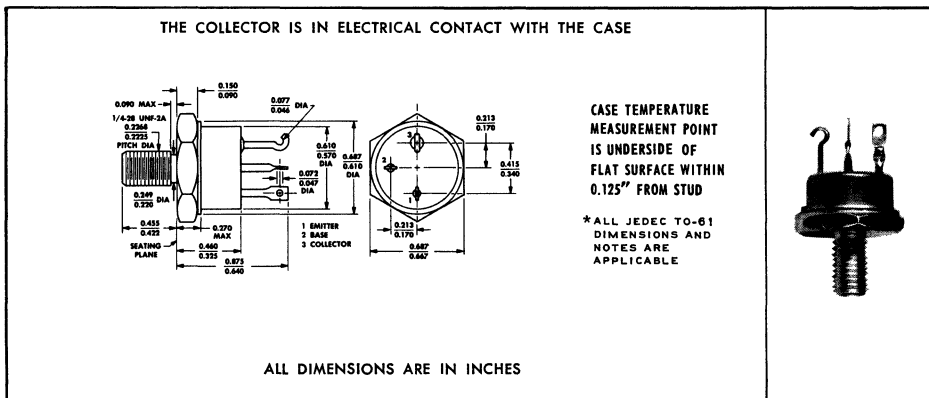
TYPES TI1131, TI1132, TI1133, TI1134, TI1135, TI1136
BULLETIN NO. DL-5 654635, DECEMBER 1963
REVISED OCTOBER 1965

HIGH-VOLTAGE, HIGH-FREQUENCY POWER TRANSISTORS FOR INDUSTRIAL APPLICATIONS

- 80 Watts at 55°C Case Temperature
- Maximum r_{CS} of 0.5 Ohm at 2 Amperes I_C
- Maximum V_{BE} of 2 Volts at 2 Amperes I_C
- Minimum f_T of 7.5 Megacycles

mechanical data

The transistors are in hermetically-sealed welded packages.



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TI1131 TI1132	TI1133 TI1134	TI1135 TI1136
Collector-Base Voltage	200 v	150 v	100 v
Collector-Emitter Voltage (See Note 1)	100 v	75 v	50 v
Emitter-Base Voltage	←	8 v	→
Collector Current, Continuous	←	7.5 a	→
Emitter Current, Continuous	←	7.5 a	→
Safe Continuous Operating Region at (or below) 55°C Case Temperature	See Figure 1		
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	←	3 w	→
Total Device Dissipation at (or below) 55°C Case Temperature (See Note 3)	←	80 w	→
Operating Collector Junction Temperature	←	175°C	→
Storage Temperature Range	-65°C to +200°C		

- NOTES: 1. This value applies when base-emitter diode is open-circuited.
 2. Derate linearly to 175°C free-air temperature at the rate of 20 mw/°C.
 3. Derate linearly to 175°C case temperature at the rate of 0.67 w/°C.

TYPES TI 1131, TI 1132, TI 1133, TI 1134, TI 1135, TI 1136

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	MAX	UNIT
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = 10 \text{ ma}$, $I_E = 0$	TI1131, TI1132	200		v
		TI1133, TI1134	150		v
		TI1135, TI1136	100		v
BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = 0.2 \text{ a}$, $I_B = 0$, (See Note 4)	TI1131, TI1132	100		v
		TI1133, TI1134	75		v
		TI1135, TI1136	50		v
I_{CES} Collector Cutoff Current	$V_{CE} = 30 \text{ v}$, $V_{BE} = 0$	All		100	μa
	$V_{CE} = 100 \text{ v}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	TI1131, TI1132		10	ma
	$V_{CE} = 75 \text{ v}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	TI1133, TI1134		10	ma
	$V_{CE} = 50 \text{ v}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	TI1135, TI1136		10	ma
I_{EBO} Emitter Cutoff Current	$V_{EB} = 8 \text{ v}$, $I_C = 0$	All		1.0	ma
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ v}$, $I_C = 2.0 \text{ a}$, (See Note 4)	TI1131, TI1133 TI1135	30	120	
		TI1132, TI1134 TI1136	15	60	
V_{BE} Base-Emitter Voltage	$I_B = 0.20 \text{ a}$, $I_C = 2.0 \text{ a}$, (See Note 4)	All		2.0	v
$r_{CE(sat)}$ Static Collector-Emitter Saturation Resistance	$I_B = 0.20 \text{ a}$, $I_C = 2.0 \text{ a}$, (See Note 4)	All		0.5	ohm
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 15 \text{ v}$, $I_C = 0.5 \text{ a}$, $f = 7.5 \text{ mc}$, (See Note 5)	All	1.0		
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 15 \text{ v}$, $I_E = 0$, $f = 1.0 \text{ mc}$	All		550	pf

NOTES: 4. These parameters must be measured using pulse techniques. $PW = 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.
5. If tested without a heat sink, DC collector current must not be applied longer than 5 seconds.

thermal characteristics

PARAMETER	TYPE	MIN	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	All		1.5	$^\circ\text{C}/\text{w}$
θ_{J-A} Junction-to-Free-Air Thermal Resistance	All		50	$^\circ\text{C}/\text{w}$

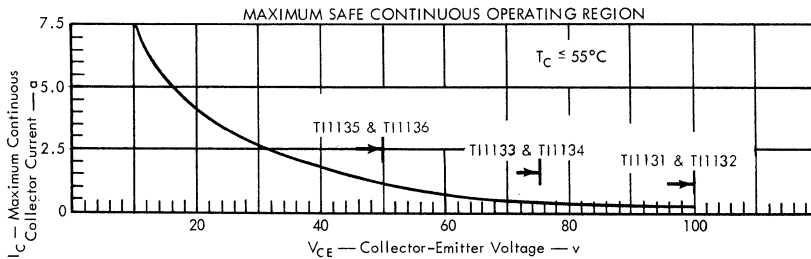


Figure 1

TYPES TI 1151, TI 1152, TI 1153, TI 1154, TI 1155, TI 1156 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

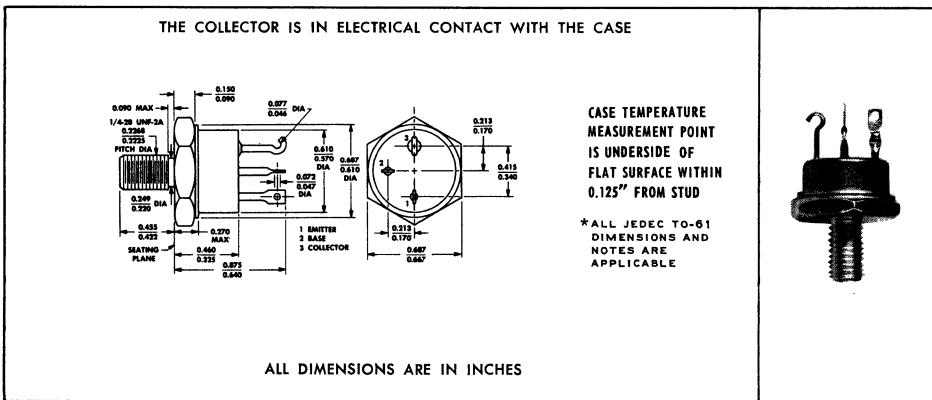
HIGH-VOLTAGE, HIGH-FREQUENCY POWER TRANSISTORS FOR INDUSTRIAL APPLICATIONS

- 80 Watts at 55°C Case Temperature
- Maximum r_{CS} of 0.5 Ohm at 5 Amperes I_C
- Maximum V_{BE} of 2 Volts at 5 Amperes I_C
- Minimum f_T of 7.5 Megacycles

TYPES TI 1151, TI 1152, TI 1153, TI 1154, TI 1155, TI 1156
BULLETIN NO. DLS-654637, DECEMBER 1963
REVISED OCTOBER 1965

mechanical data

The transistors are in hermetically-sealed welded packages.



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TI1151 TI1152	TI1153 TI1154	TI1155 TI1156
Collector-Base Voltage	200 v	150 v	100 v
Collector-Emitter Voltage (See Note 1)	100 v	75 v	50 v
Emitter-Base Voltage	←	8 v	→
Collector Current, Continuous	←	7.5 a	→
Emitter Current, Continuous	←	7.5 a	→
Safe Continuous Operating Region at (or below) 55°C Case Temperature	See Figure 1		
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	←	3 w	→
Total Device Dissipation at (or below) 55°C Case Temperature (See Note 3)	←	80 w	→
Operating Collector Junction Temperature	←	175°C	→
Storage Temperature Range	-65°C to +200°C		

- NOTES: 1. This value applies when base-emitter diode is open-circuited.
 2. Derate linearly to 175°C free-air temperature at the rate of 20 mw/°C.
 3. Derate linearly to 175°C case temperature at the rate of 0.67 w/°C.

TYPES TI 1151, TI 1152, TI 1153, TI 1154, TI 1155, TI 1156

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	MAX	UNIT
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = 10 \text{ ma}$, $I_E = 0$	TI1151, TI1152	200		v
		TI1153, TI1154	150		v
		TI1155, TI1156	100		v
BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = 0.2 \text{ a}$, $I_B = 0$, (See Note 4)	TI1151, TI1152	100		v
		TI1153, TI1154	75		v
		TI1155, TI1156	50		v
I_{CES} Collector Cutoff Current	$V_{CE} = 30 \text{ v}$, $V_{BE} = 0$	All		100	μa
	$V_{CE} = 100 \text{ v}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	TI1151, TI1152		10	ma
	$V_{CE} = 75 \text{ v}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	TI1153, TI1154		10	ma
	$V_{CE} = 50 \text{ v}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	TI1155, TI1156		10	ma
I_{EBO} Emitter Cutoff Current	$V_{EB} = 8 \text{ v}$, $I_C = 0$	All		1.0	ma
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ v}$, $I_C = 5.0 \text{ a}$, (See Note 4)	TI1151, TI1153 TI1155	20	80	
		TI1152, TI1154 TI1156	10	40	
V_{BE} Base-Emitter Voltage	$I_B = 0.50 \text{ a}$, $I_C = 5.0 \text{ a}$, (See Note 4)	All		2.0	v
$r_{CE(sat)}$ Static Collector-Emitter Saturation Resistance	$I_B = 0.50 \text{ a}$, $I_C = 5.0 \text{ a}$, (See Note 4)	All		0.5	ohm
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 15 \text{ v}$, $I_C = 0.5 \text{ a}$, $f = 7.5 \text{ mc}$, (See Note 5)	All	1.0		
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 15 \text{ v}$, $I_E = 0$, $f = 1.0 \text{ mc}$	All		550	pf

NOTES: 4. These parameters must be measured using pulse techniques. $PW = 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.
5. If tested without a heat sink, DC collector current must not be applied longer than 5 seconds.

thermal characteristics

PARAMETER	TYPE	MIN	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	All		1.5	$^\circ\text{C}/\text{w}$
θ_{J-A} Junction-to-Free-Air Thermal Resistance	All		50	$^\circ\text{C}/\text{w}$

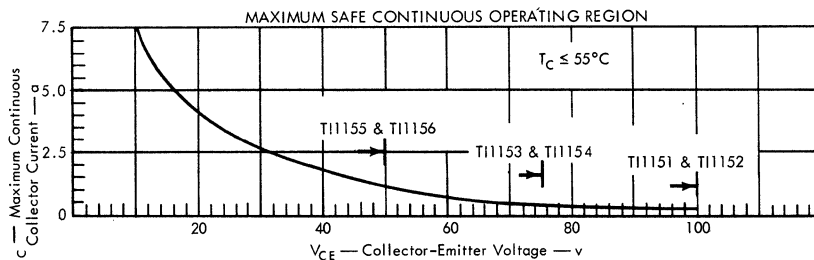


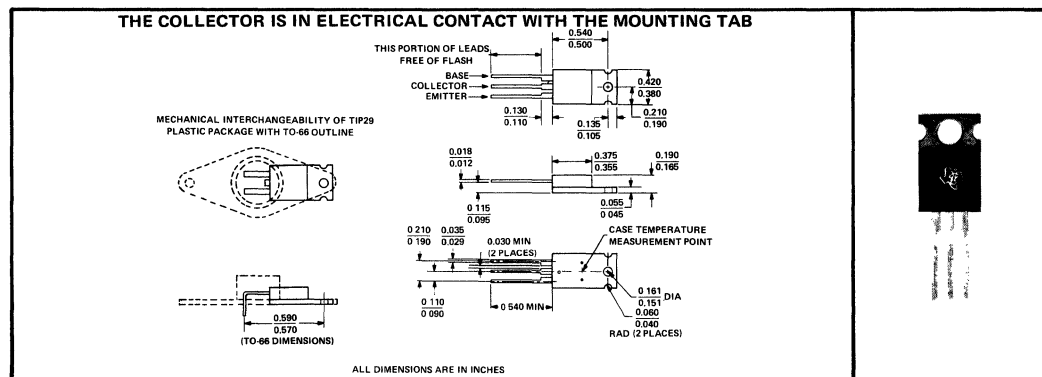
Figure 1

TYPES TIP29, TIP29A, TIP29B, TIP29C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP30, TIP30A, TIP30B, TIP30C

- 30 W at 25°C Case Temperature
- 1 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 200 mA

mechanical data



TYPES TIP29, TIP29A, TIP29B, TIP29C
BULLETIN NO. DL-S-7011371, OCTOBER 1970
REPLACES BULLETIN NO. DL-S-6810954, JULY 1968

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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP29	TIP29A	TIP29B	TIP29C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	← 5 V →			
Continuous Collector Current	← 1 A →			
Peak Collector Current (See Note 2)	← 3 A →			
Continuous Base Current	← 0.4 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 30 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Unclamped Inductive Load Energy (See Note 5)	← 32 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES:
1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of $0.24 \text{ W}/^\circ\text{C}$.
 4. Derate linearly to 150°C free-air temperature at the rate of $16 \text{ mW}/^\circ\text{C}$.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP29, TIP29A, TIP29B, TIP29C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP29		TIP29A		TIP29B		TIP29C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	40		60		80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$		0.3		0.3					mA
	$V_{CE} = 60 \text{ V}$, $I_B = 0$						0.3		0.3	
I_{CES} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$		0.2							mA
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$				0.2					
	$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$						0.2			
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$							0.2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		1		1		1		1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 0.2 \text{ A}$, See Notes 6 and 7	40		40		40		40		
	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 6 and 7	15	75	15	75	15	75	15	75	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 6 and 7		1.3		1.3		1.3		1.3	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 125 \text{ mA}$, $I_C = 1 \text{ A}$, See Notes 6 and 7		0.7		0.7		0.7		0.7	V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	4.17	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	

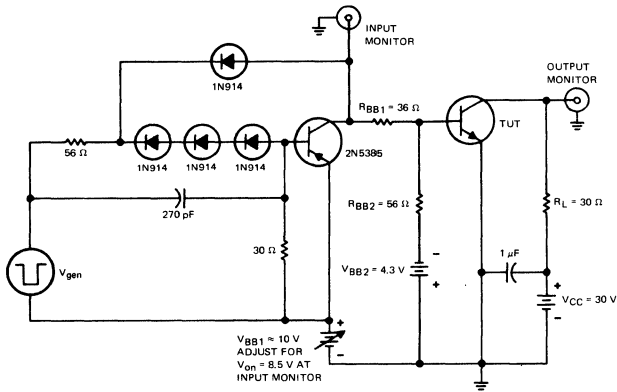
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_B(1) = 100 \text{ mA}$, $I_B(2) = -100 \text{ mA}$, $V_{BE(off)} = -4.3 \text{ V}$, $R_L = 30 \Omega$, See Figure 1	0.5	μs
t_{off} Turn-Off Time		2	

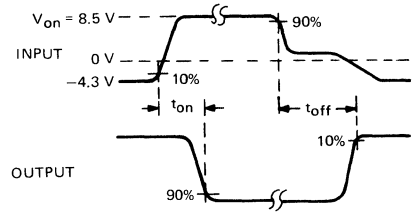
† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP29, TIP29A, TIP29B, TIP29C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

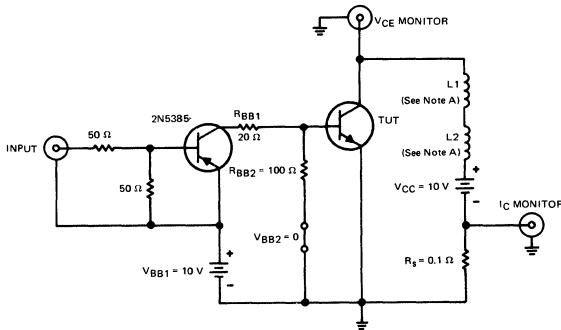


VOLTAGE WAVEFORMS

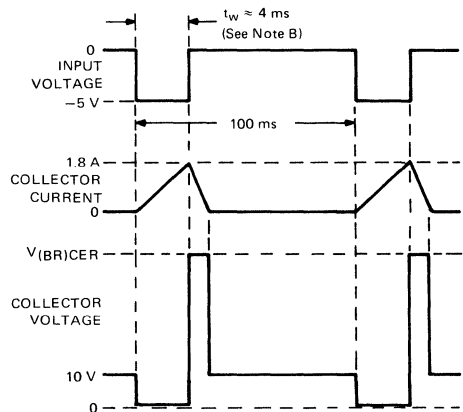
- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. L_1 and L_2 are 10 mH , $0.11\text{ }\Omega$, Chicago Standard Transformer Corporation C-2688, or equivalent.
 B. Input pulse width is increased until $I_{CM} = 1.8\text{ A}$.

FIGURE 2

TYPES TIP29, TIP29A, TIP29B, TIP29C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS
 STATIC FORWARD CURRENT TRANSFER RATIO
 vs
 COLLECTOR CURRENT

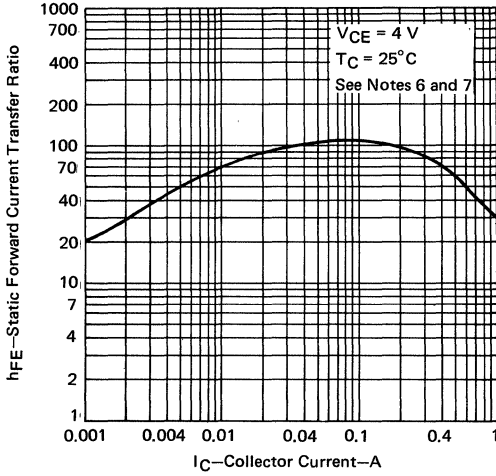


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

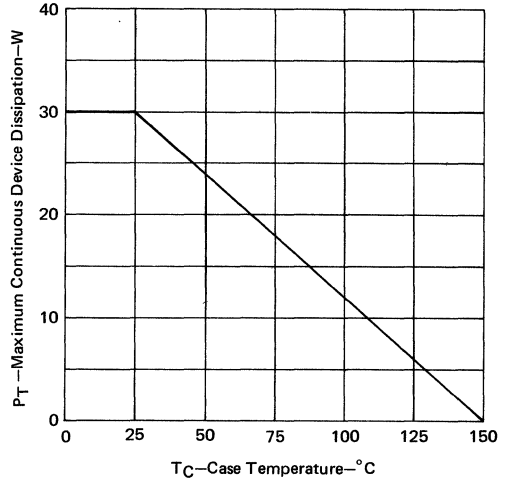


FIGURE 4

MAXIMUM SAFE OPERATING REGION

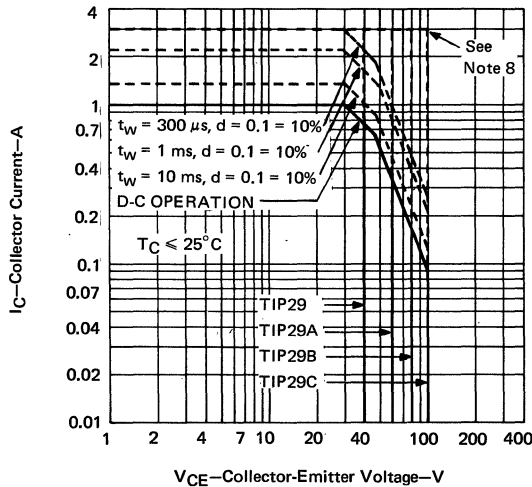


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

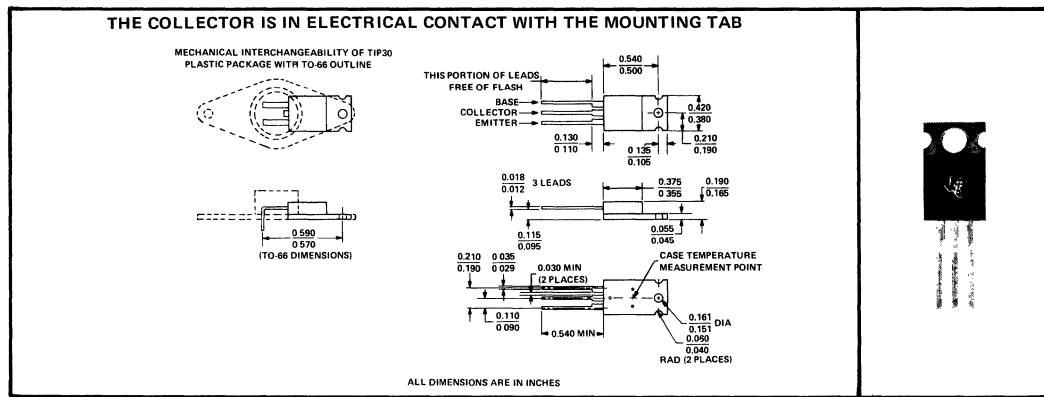
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TYPES TIP30, TIP30A, TIP30B, TIP30C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP29, TIP29A, TIP29B, TIP29C

- 30 W at 25°C Case Temperature
- 1 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 200 mA

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP30	TIP30A	TIP30B	TIP30C
Collector-Base Voltage	-40 V	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V	-80 V	-100 V
Emitter-Base Voltage	←		-5 V	→
Continuous Collector Current	←		-1 A	→
Peak Collector Current (See Note 2)	←		-3 A	→
Continuous Base Current	←		-0.4 A	→
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	←		30 W	→
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	←		2 W	→
Unclamped Inductive Load Energy (See Note 5)	←		32 mJ	→
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 150°C case temperature at the rate of 0.24 W/°C.
4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C.
5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L / 2$.

TYPES TIP30, TIP30A, TIP30B, TIP30C
BULLETIN NO. DLS-7011401, DECEMBER 1970
REPLACES BULLETIN NO. DLS-6810956, JULY 1968

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TYPES TIP30, TIP30A, TIP30B, TIP30C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP30		TIP30A		TIP30B		TIP30C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-40		-60		-80		-100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.3		-0.3						mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$					-0.3		-0.3		
I_{CES} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$	-0.2								mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$			-0.2						
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 0$					-0.2				
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$							-0.2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1		-1		-1		-1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -0.2 \text{ A}$, See Notes 6 and 7	40		40		40		40		
	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 6 and 7	15	75	15	75	15	75	15	75	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 6 and 7	-1.3		-1.3		-1.3		-1.3		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -125 \text{ mA}$, $I_C = -1 \text{ A}$, See Notes 6 and 7	-0.7		-0.7		-0.7		-0.7		V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	4.17	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	

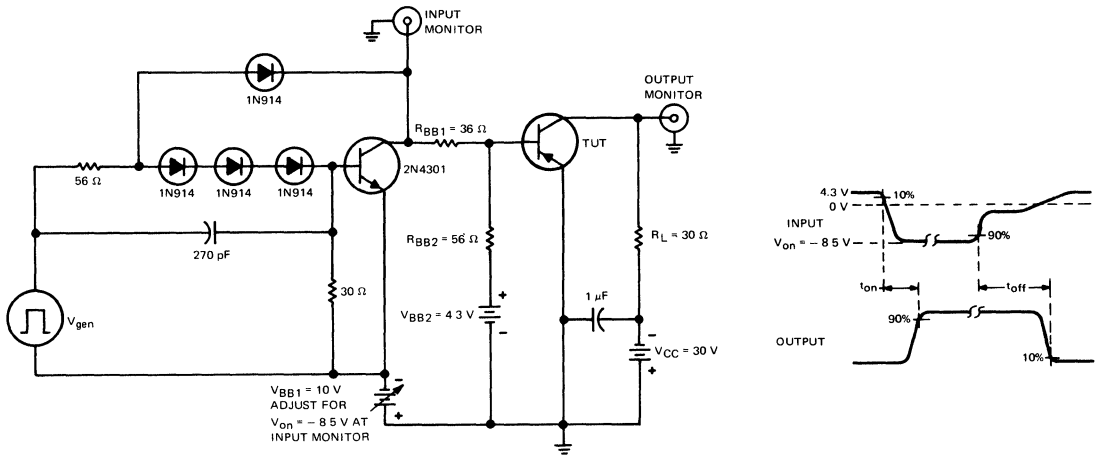
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -1 \text{ A}$, $I_{B(1)} = -100 \text{ mA}$, $I_{B(2)} = 100 \text{ mA}$, $V_{BE(off)} = 4.3 \text{ V}$, $R_L = 30 \Omega$, See Figure 1	0.3	μs
t_{off} Turn-Off Time		1.0	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP30, TIP30A, TIP30B, TIP30C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



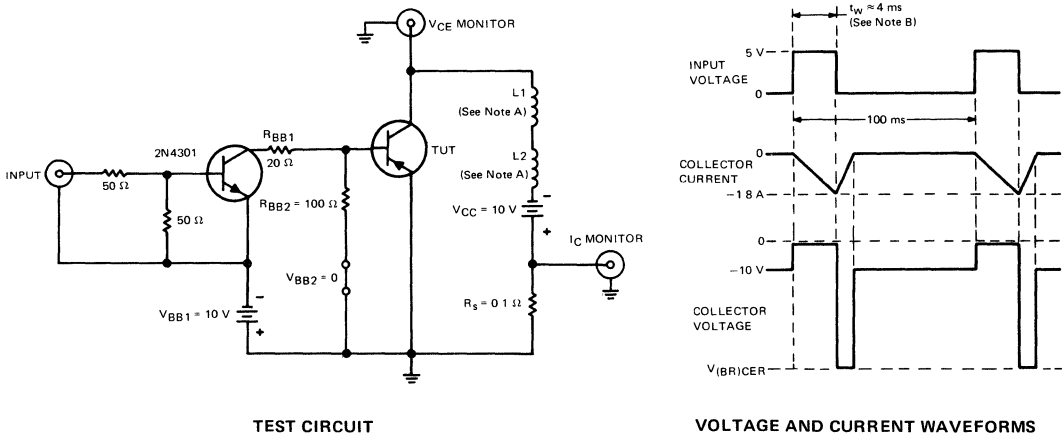
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES:
- V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 - The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

- NOTES:
- L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
 - Input pulse width is increased until $I_{CM} = -1.8$ A.

FIGURE 2

TYPES TIP30, TIP30A, TIP30B, TIP30C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

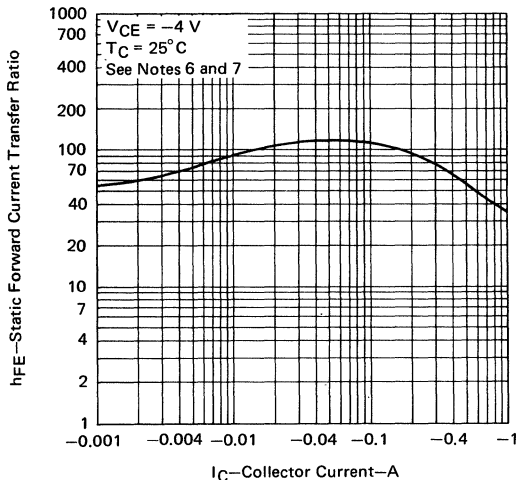


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

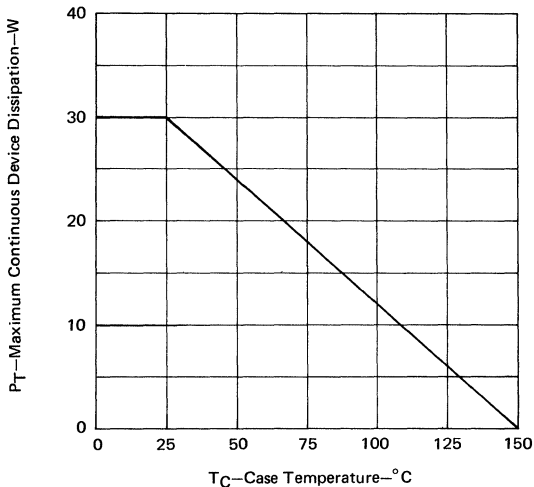


FIGURE 4

MAXIMUM SAFE OPERATING REGION

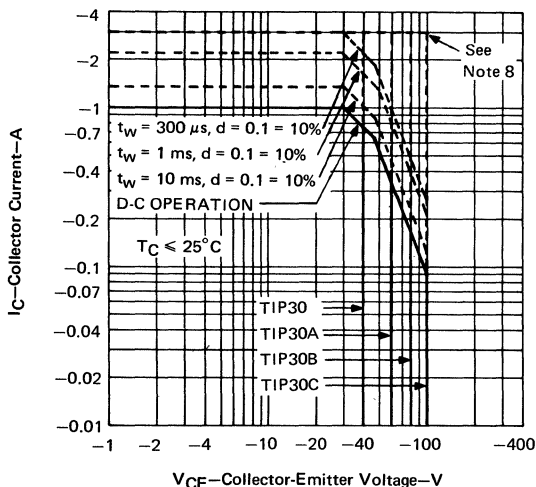


FIGURE 5

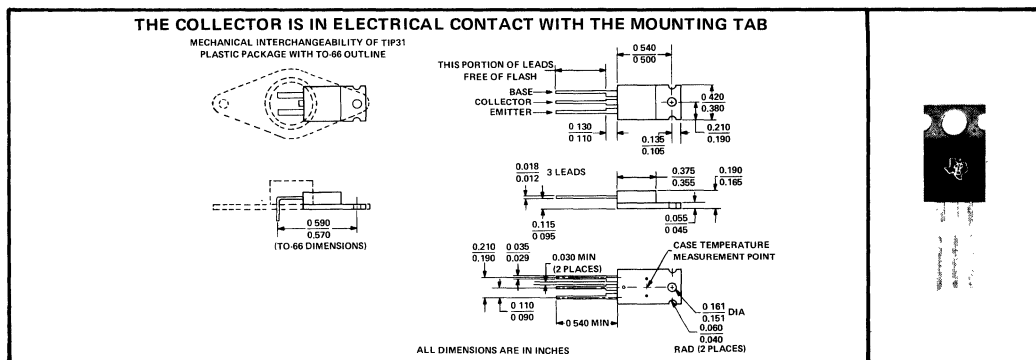
NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

TYPES TIP31, TIP31A, TIP31B, TIP31C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP32, TIP32A, TIP32B, TIP32C

- 40 W at 25°C Case Temperature
- 3 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP31	TIP31A	TIP31B	TIP31C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	← 5 V →			
Continuous Collector Current	← 3 A →			
Peak Collector Current (See Note 2)	← 5 A →			
Continuous Base Current	← 1 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 40 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Unclamped Inductive Load Energy (See Note 5)	← 32 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.32W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L / 2$.

TYPES TIP31, TIP31A, TIP31B, TIP31C
BULLETIN NO. DL-S-7011402, DECEMBER 1970
REPLACES BULLETIN NO. DL-S-6810953, JULY 1968

5

TYPES TIP31, TIP31A, TIP31B, TIP31C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP31		TIP31A		TIP31B		TIP31C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	40		60		80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	0.3		0.3						mA
	$V_{CE} = 60 \text{ V}$, $I_B = 0$					0.3		0.3		
I_{CES} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$	0.2								mA
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$			0.2						
	$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$					0.2				
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$							0.2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1		1		1		1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 6 and 7	25		25		25		25		
	$V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	10	50	10	50	10	50	10	50	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	1.8		1.8		1.8		1.8		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 375 \text{ mA}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	1.2		1.2		1.2		1.2		V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3.125	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	

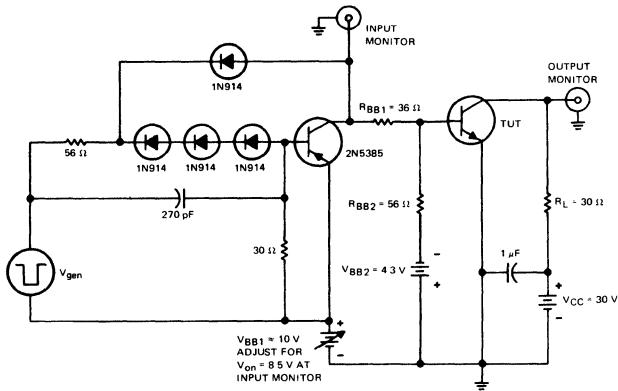
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_{B(1)} = 100 \text{ mA}$, $I_{B(2)} = -100 \text{ mA}$, $V_{BE(off)} = -4.3 \text{ V}$, $R_L = 30 \Omega$, See Figure 1	0.5	μs
t_{off} Turn-Off Time		2	

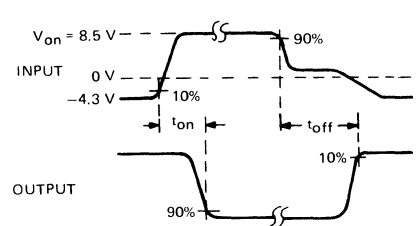
†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP31, TIP31A, TIP31B, TIP31C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

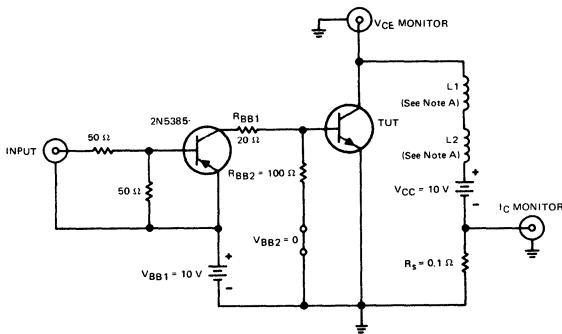


VOLTAGE WAVEFORMS

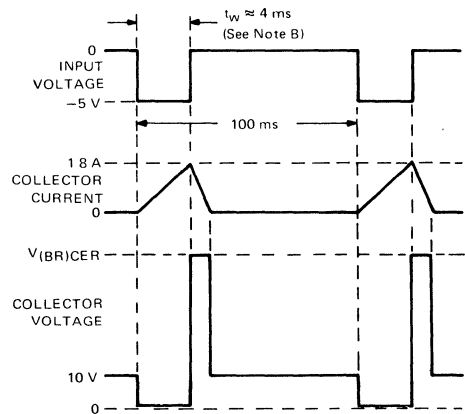
- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. L_1 and L_2 are 10 mH , $0.11\text{ }\Omega$, Chicago Standard Transformer Corporation C-2688, or equivalent.
 B. Input pulse width is increased until $I_{CM} = 1.8\text{ A}$.

FIGURE 2

TYPES TIP31, TIP31A, TIP31B, TIP31C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

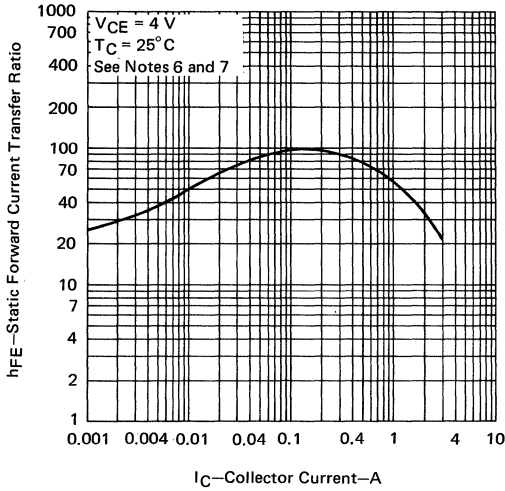


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

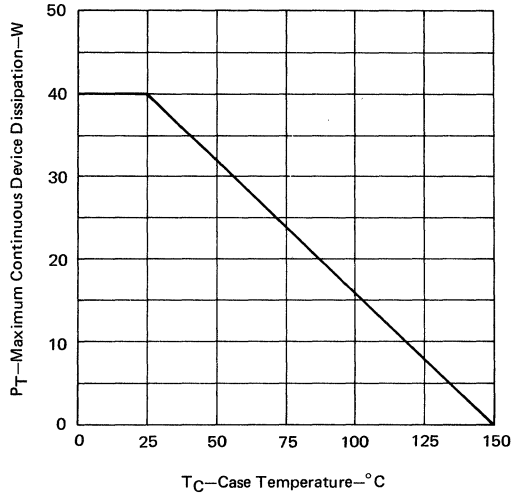


FIGURE 4

MAXIMUM SAFE OPERATING REGION

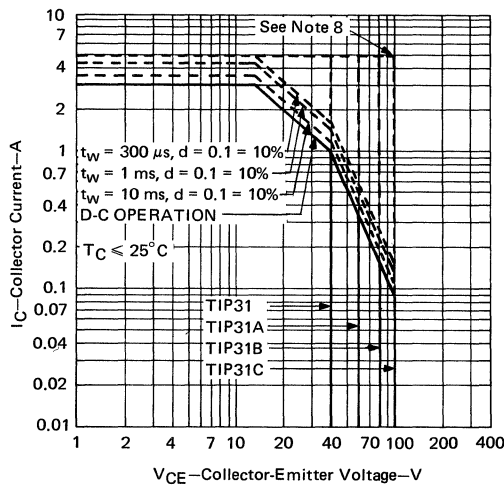


FIGURE 5

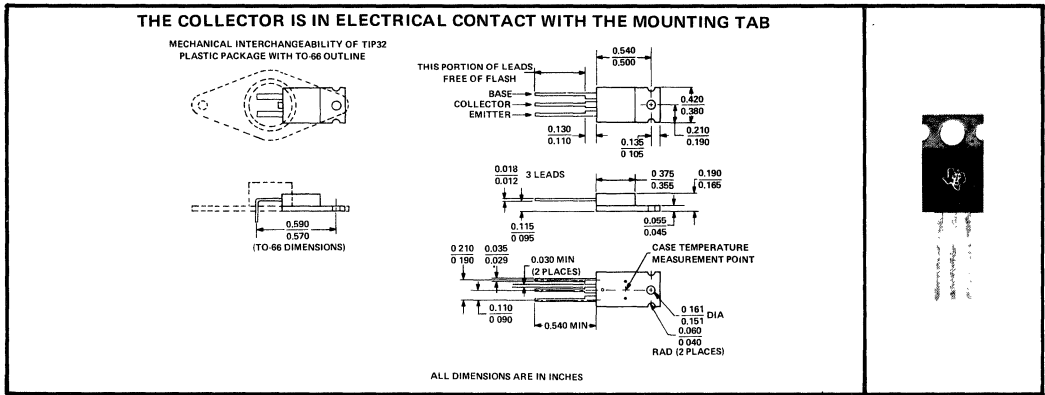
NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

TYPES TIP32, TIP32A, TIP32B, TIP32C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP31, TIP31A, TIP31B, TIP31C

- 40 W at 25°C Case Temperature
- 3 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP32	TIP32A	TIP32B	TIP32C
Collector-Base Voltage	-40 V	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V	-80 V	-100 V
Emitter-Base Voltage	← -5 V →			
Continuous Collector Current	← -3 A →			
Peak Collector Current (See Note 2)	← -5 A →			
Continuous Base Current	← -1 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 40 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Unclamped Inductive Load Energy (See Note 5)	← 32 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.32 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP32, TIP32A, TIP32B, TIP32C
BULLETIN NO. DL-S-7011403, DECEMBER 1970
REPLACES BULLETIN NO. DL-S-6810952, JULY 1968

5

TYPES TIP32, TIP32A, TIP32B, TIP32C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP32		TIP32A		TIP32B		TIP32C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-40		-60		-80		-100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.3		-0.3						mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$					-0.3		-0.3		
I_{CES} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$	-0.2								mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$			-0.2						
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 0$					-0.2				
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$							-0.2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1		-1		-1		-1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 6 and 7	25		25		25		25		
	$V_{CE} = -4 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	10	50	10	50	10	50	10	50	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	-1.8		-1.8		-1.8		-1.8		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -375 \text{ mA}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	-1.2		-1.2		-1.2		-1.2		V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3.125	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	

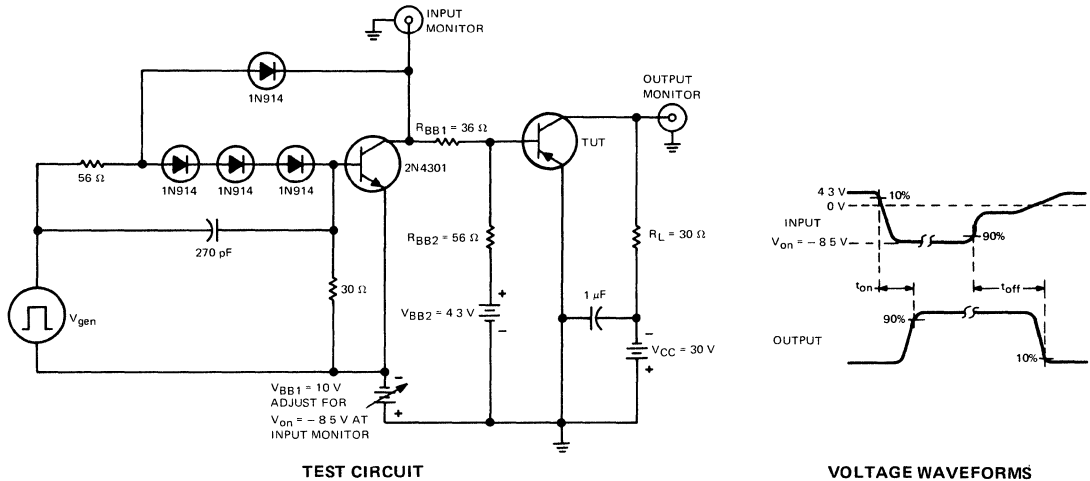
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -1 \text{ A}$, $I_{B(1)} = -100 \text{ mA}$, $I_{B(2)} = 100 \text{ mA}$, $V_{BE(off)} = 4.3 \text{ V}$, $R_L = 30 \Omega$, See Figure 1	0.3	μs
t_{off} Turn-Off Time		1.0	

† Voltages and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP32, TIP32A, TIP32B, TIP32C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

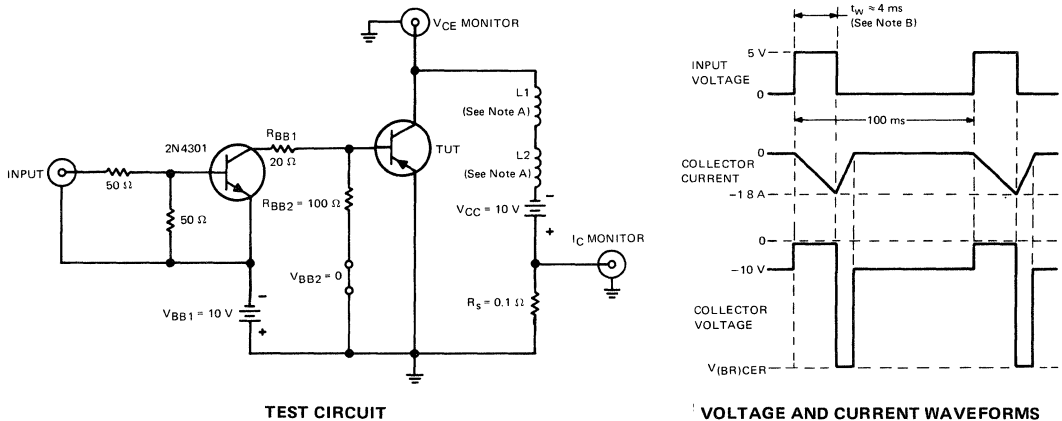
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



- NOTES: A. L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
 B. Input pulse width is increased until $I_{CM} = -1.8$ A.

FIGURE 2

TYPES TIP32, TIP32A, TIP32B, TIP32C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

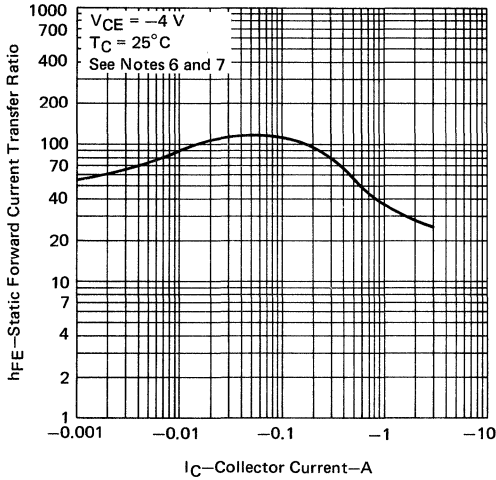


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

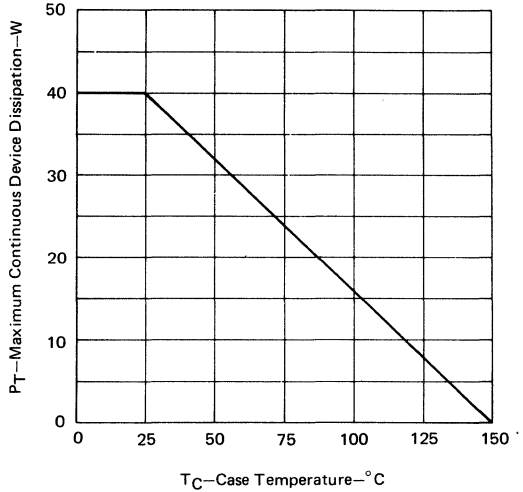


FIGURE 4

MAXIMUM SAFE OPERATING REGION

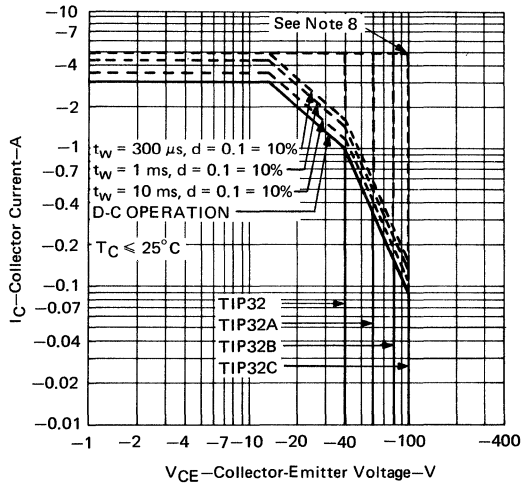


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

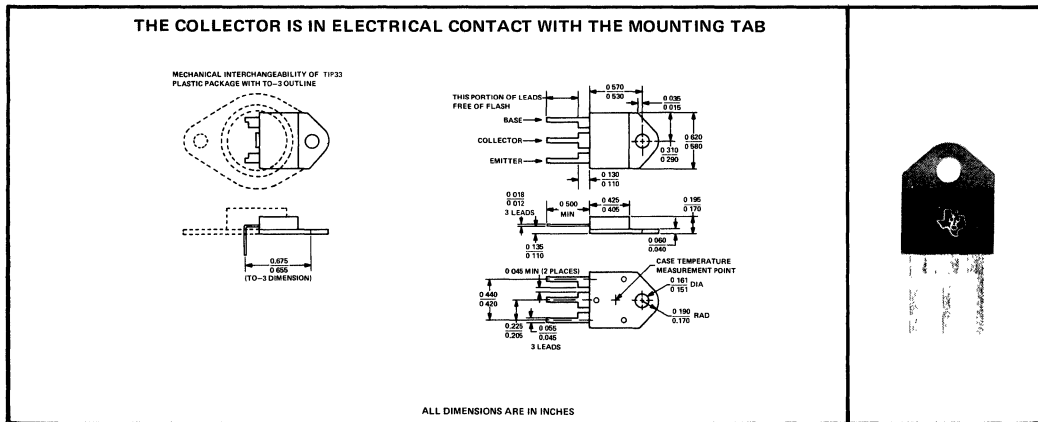
TYPES TIP33, TIP33A, TIP33B, TIP33C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP34, TIP34A, TIP34B, TIP34C

- 80 W at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

TYPES TIP33, TIP33A, TIP33B, TIP33C
BULLETIN NO. DL-S-7011404, DECEMBER 1970
REPLACES BULLETIN NO. DL-S-6810957, JULY 1968

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP33	TIP33A	TIP33B	TIP33C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	←———— 5 V —————→			
Continuous Collector Current	←———— 10 A —————→			
Peak Collector Current (See Note 2)	←———— 15 A —————→			
Continuous Base Current	←———— 3 A —————→			
Safe Operating Region at (or below) 25°C Case Temperature Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	←———— See Figure 5 —————→			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	←———— 80 W —————→			
Unclamped Inductive Load Energy (See Note 5)	←———— 62.5 mJ —————→			
Operating Collector Junction Temperature Range	←———— -65°C to 150°C —————→			
Storage Temperature Range	←———— -65°C to 150°C —————→			
Lead Temperature 1/8 Inch from Case for 10 Seconds	←———— 260°C —————→			

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.64 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx |I_C|^2 L / 2$.

TYPES TIP33, TIP33A, TIP33B, TIP33C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP33		TIP33A		TIP33B		TIP33C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	40		60		80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	0.7		0.7						mA
	$V_{CE} = 60 \text{ V}$, $I_B = 0$					0.7		0.7		
I_{CES} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$	0.4								mA
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$			0.4						
	$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$					0.4				
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$							0.4		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1		1		1		1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 6 and 7	40		40		40		40		
	$V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	20	100	20	100	20	100	20	100	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	1.6		1.6		1.6		1.6		V
	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 6 and 7	3		3		3		3		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.3 \text{ A}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	1		1		1		1		V
	$I_B = 2.5 \text{ A}$, $I_C = 10 \text{ A}$, See Notes 6 and 7	4		4		4		4		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.56	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35.7	

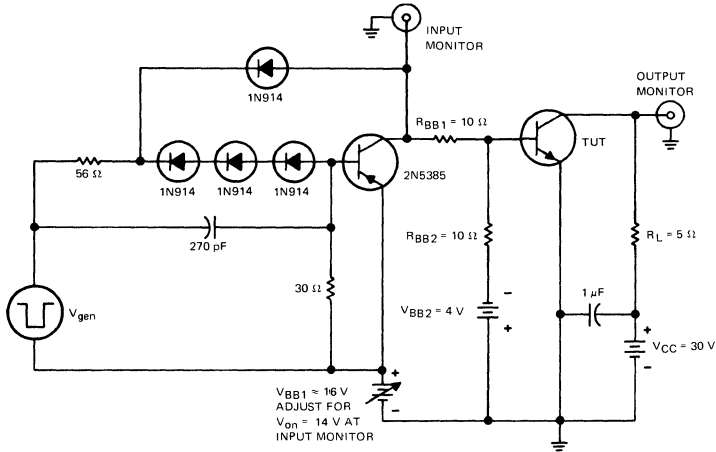
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 6 \text{ A}$, $V_{BE(off)} = -4 \text{ V}$, $I_B(1) = 0.6 \text{ A}$, $R_L = 5 \Omega$, $I_B(2) = -0.6 \text{ A}$, See Figure 1	0.6	μs
t_{off} Turn-Off Time		1	

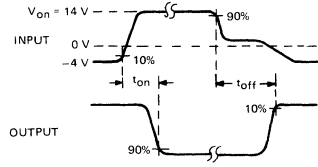
† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP33, TIP33A, TIP33B, TIP33C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

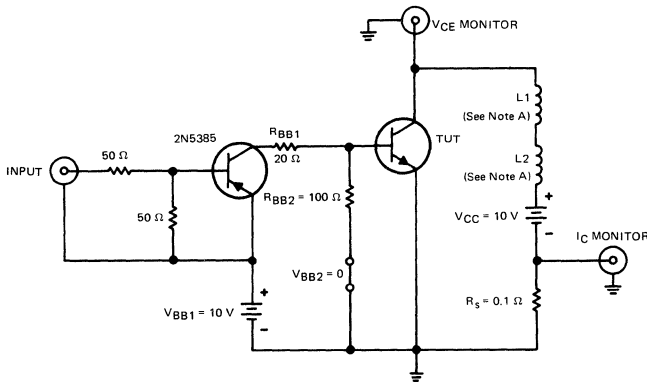


VOLTAGE WAVEFORMS

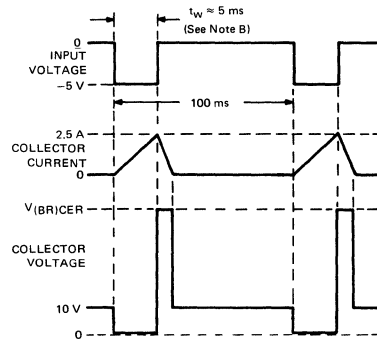
- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. L_1 and L_2 are 10 mH , $0.11\text{ }\Omega$, Chicago Standard Transformer Corporation C-2688, or equivalent.
 B. Input pulse width is increased until $I_{CM} = 2.5\text{ A}$.

FIGURE 2

TYPES TIP33, TIP33A, TIP33B, TIP33C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

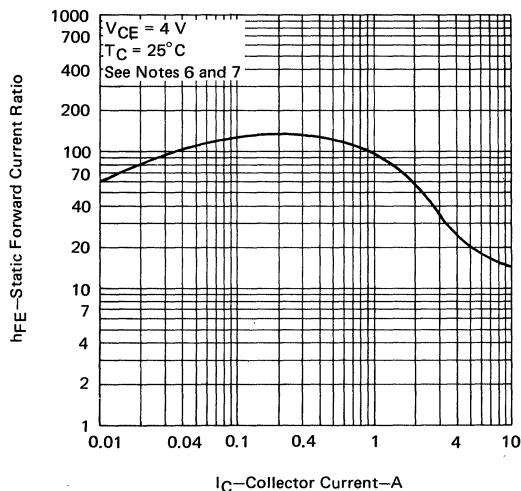


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

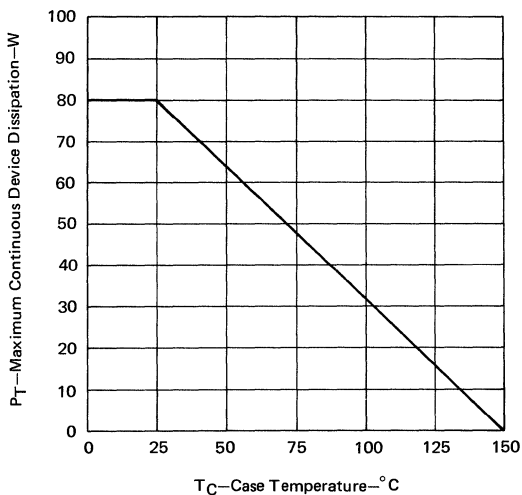


FIGURE 4

MAXIMUM SAFE OPERATING REGION

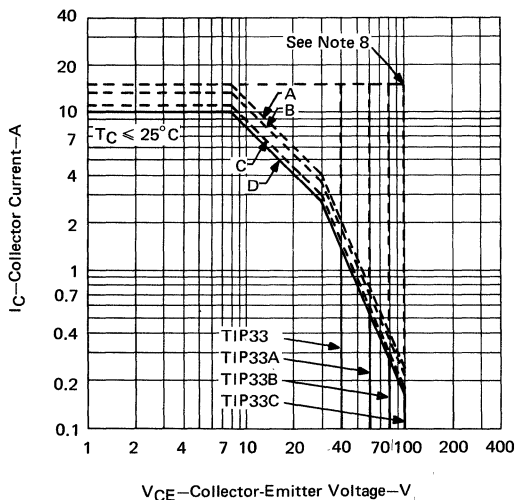


FIGURE 5

KEY FOR FIGURE 5

CURVE	CONDITIONS
A	$t_w = 300 \mu s$, $d = 0.1 = 10\%$
B	$t_w = 1 \text{ ms}$, $d = 0.1 = 10\%$
C	$t_w = 10 \text{ ms}$, $d = 0.1 = 10\%$
D	D-C OPERATION

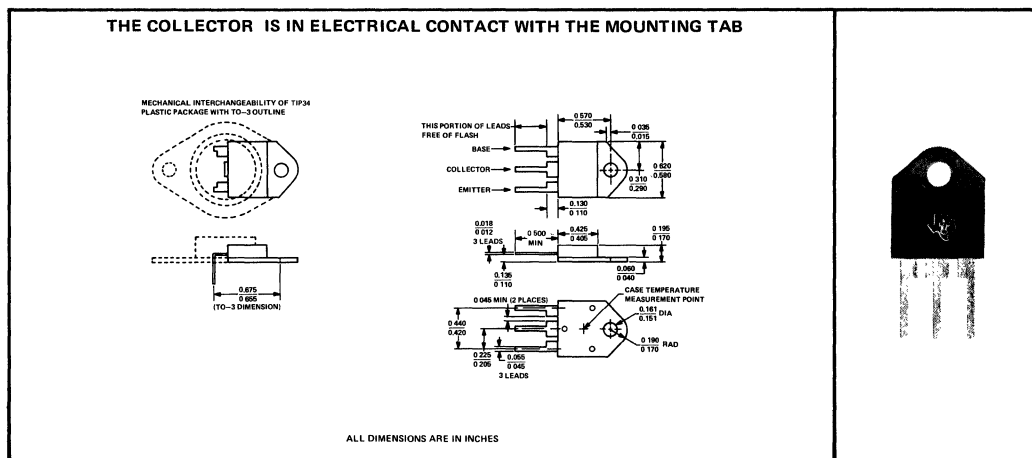
NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

TYPES TIP34, TIP34A, TIP34B, TIP34C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP33, TIP33A, TIP33B, TIP33C

- 80 W at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP34	TIP34A	TIP34B	TIP34C
Collector-Base Voltage	-40 V	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V	-80 V	-100 V
Emitter-Base Voltage	← -5 V →			
Continuous Collector Current	← -10 A →			
Peak Collector Current (See Note 2)	← -15 A →			
Continuous Base Current	← -3 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 80 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →			
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_{W} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.64 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx 1/2 I_C^2 L/2$.

TYPES TIP34, TIP34A, TIP34B, TIP34C
BULLETIN NO. DL-S-7011405, DECEMBER 1970
REPLACES BULLETIN NO. DLS-6810958, JULY 1968

5

TYPES TIP34, TIP34A, TIP34B, TIP34C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP34		TIP34A		TIP34B		TIP34C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-40		-60		-80		-100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.7		-0.7						mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$					-0.7		-0.7		
I_{CES} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$	-0.4								mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$			-0.4						
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 0$					-0.4				
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$							-0.4		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1		-1		-1		-1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 6 and 7	40		40		40		40		
	$V_{CE} = -4 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	20 100		20 100		20 100		20 100		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	-1.6		-1.6		-1.6		-1.6		V
	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$, See Notes 6 and 7	-3		-3		-3		-3		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.3 \text{ A}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	-1		-1		-1		-1		V
	$I_B = -2.5 \text{ A}$, $I_C = -10 \text{ A}$, See Notes 6 and 7	-4		-4		-4		-4		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.56	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35.7	

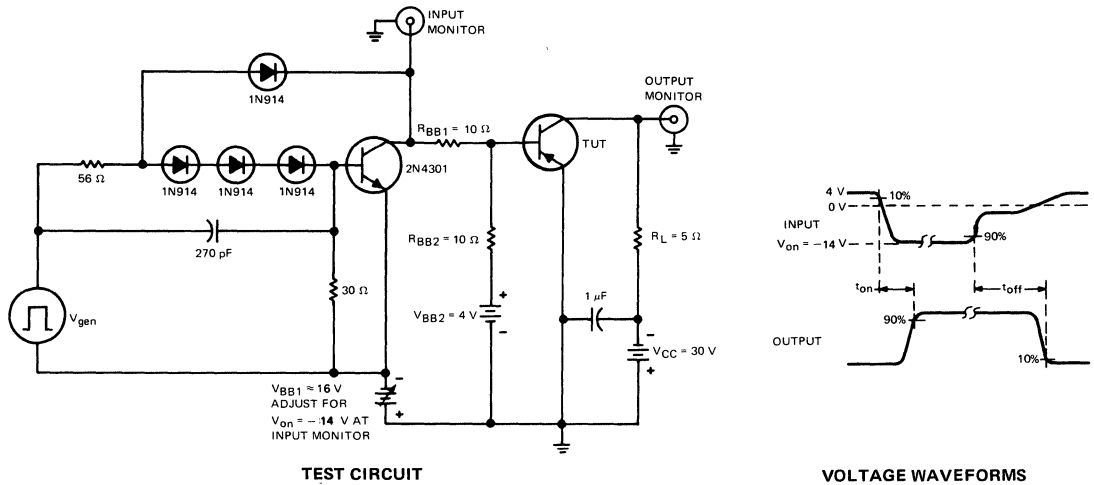
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS [†]			TYP	UNIT
t_{on} Turn-On Time	$I_C = -6 \text{ A}$, $V_{BE(off)} = 4 \text{ V}$,	$I_B(1) = -0.6 \text{ A}$, $R_L = 5 \Omega$,	$I_B(2) = 0.6 \text{ A}$, See Figure 1	0.4	μs
t_{off} Turn-Off Time				0.7	

[†] Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP34, TIP34A, TIP34B, TIP34C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

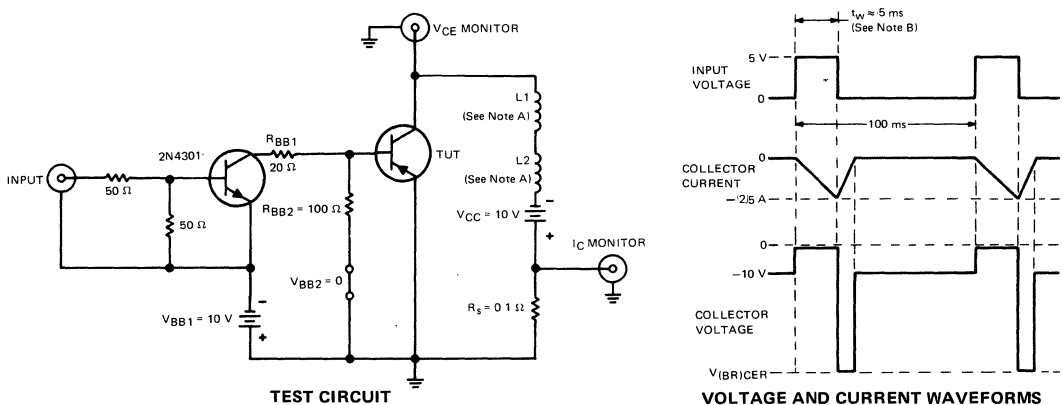
PARAMETER MEASUREMENT INFORMATION



- NOTES:
- V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 - The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



- NOTES:
- L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
 - Input pulse width is increased until $I_{CM} = -2.5$ A.

FIGURE 2

TYPES TIP34, TIP34A, TIP34B, TIP34C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
VS
COLLECTOR CURRENT

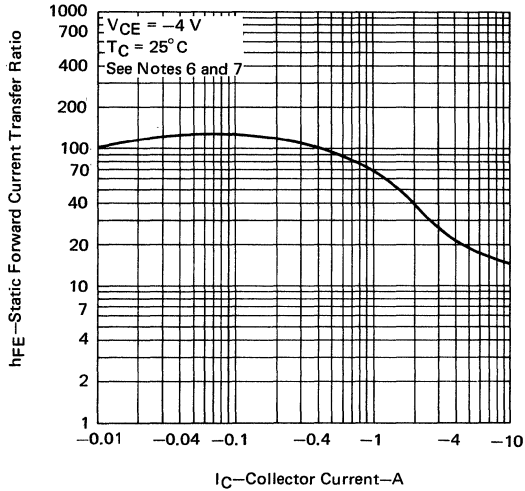


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

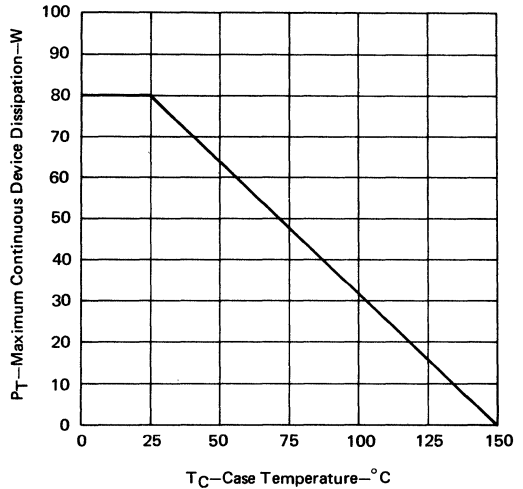


FIGURE 4

MAXIMUM SAFE OPERATING REGION

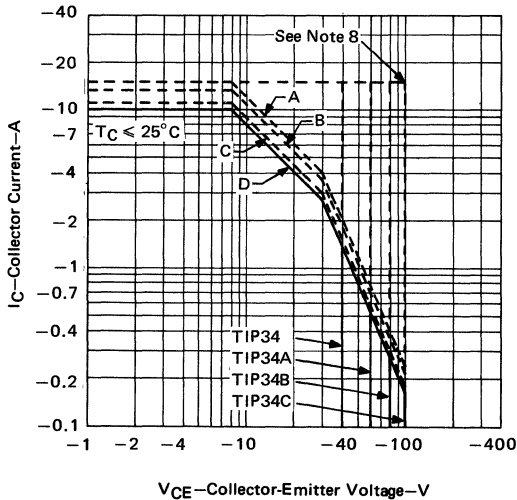


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

KEY FOR FIGURE 5

CURVE	CONDITIONS
A	$t_w = 300 \mu s$, $d = 0.1 = 10\%$
B	$t_w = 1 \text{ ms}$, $d = 0.1 = 10\%$
C	$t_w = 10 \text{ ms}$, $d = 0.1 = 10\%$
D	D-C OPERATION

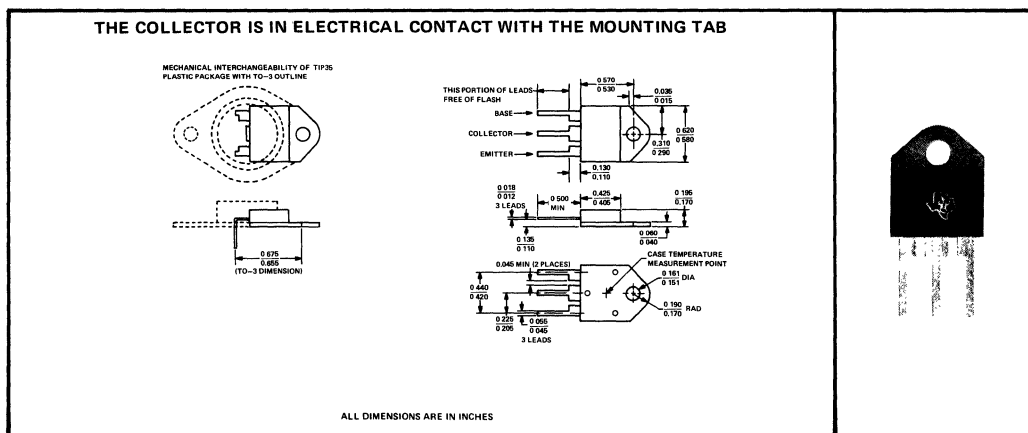
TYPES TIP35, TIP35A, TIP35B, TIP35C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP36, TIP36A, TIP36B, TIP36C

- 125 W at 25°C Case Temperature
- 25 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 1 A

TYPES TIP35, TIP35A, TIP35B, TIP35C
BULLETIN NO. DLS-7011406, DECEMBER 1970
REPLACES BULLETIN NO. DLS-6810959, JULY 1968

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP35	TIP35A	TIP35B	TIP35C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	← 5 V →			
Continuous Collector Current	← 25 A →			
Peak Collector Current (See Note 2)	← 40 A →			
Continuous Base Current	← 5 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 125 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →			
Unclamped Inductive Load Energy (See Note 5)	← 90 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 1 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP35, TIP35A, TIP35B, TIP35C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP35		TIP35A		TIP35B		TIP35C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	40		60		80		100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	1		1						mA
	$V_{CE} = 60 \text{ V}$, $I_B = 0$					1		1		
I_{CES} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$	0.7								mA
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$			0.7						
	$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$					0.7				
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$							0.7		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		1		1		1		1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1.5 \text{ A}$, See Notes 6 and 7	25		25		25		25		
	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 6 and 7	10	50	10	50	10	50	10	50	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 6 and 7		2		2		2		2	V
	$V_{CE} = 4 \text{ V}$, $I_C = 25 \text{ A}$, See Notes 6 and 7		4		4		4		4	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 1.5 \text{ A}$, $I_C = 15 \text{ A}$, See Notes 6 and 7		1.8		1.8		1.8		1.8	V
	$I_B = 5 \text{ A}$, $I_C = 25 \text{ A}$, See Notes 6 and 7		4		4		4		4	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	25		25		25		25		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35.7	

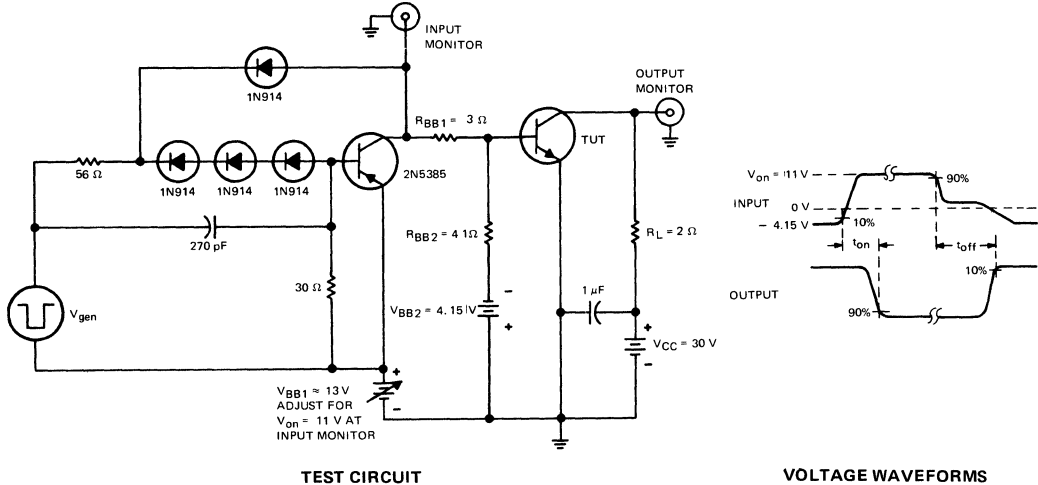
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 15 \text{ A}$, $I_{B(1)} = 1.5 \text{ A}$, $I_{B(2)} = -1.5 \text{ A}$, $V_{BE(off)} = -4.15 \text{ V}$, $R_L = 2 \Omega$, See Figure 1	1.2	μs
t_{off} Turn-Off Time		0.9	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP35, TIP35A, TIP35B, TIP35C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



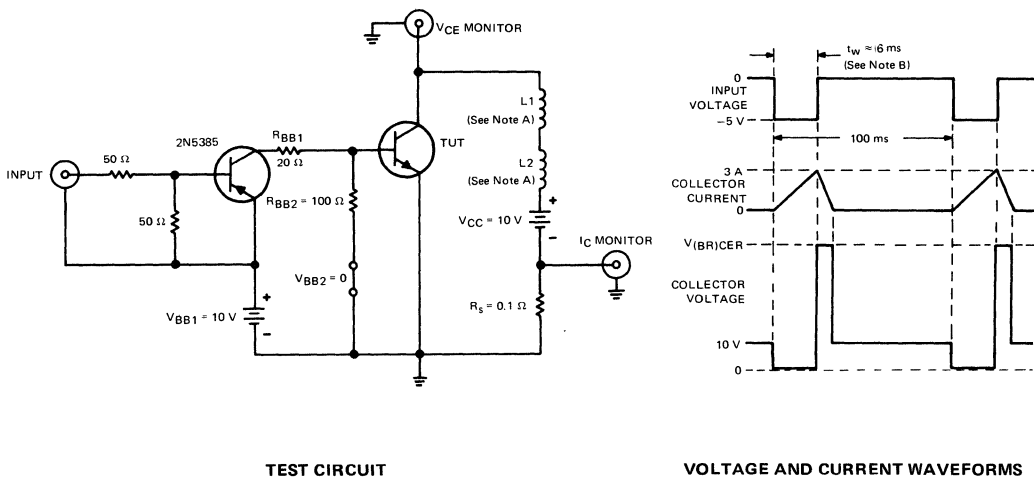
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES:
- V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

- NOTES:
- $L1$ and $L2$ are 10 mH , $0.11\text{ }\Omega$, Chicago Standard Transformer Corporation C-2688, or equivalent.
 - Input pulse width is increased until $I_{CM} = 3\text{ A}$.

FIGURE 2

TYPES TIP35, TIP35A, TIP35B, TIP35C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

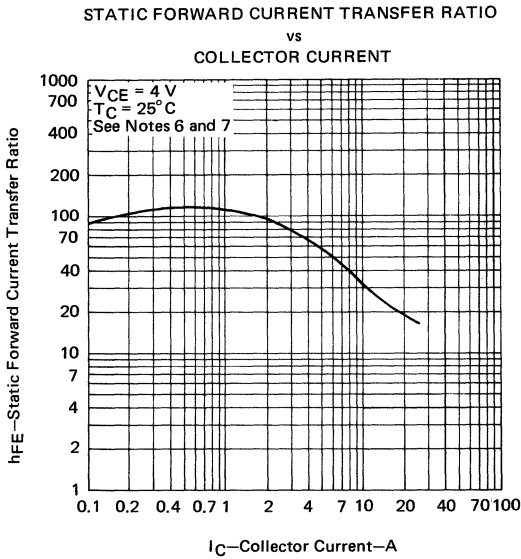


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

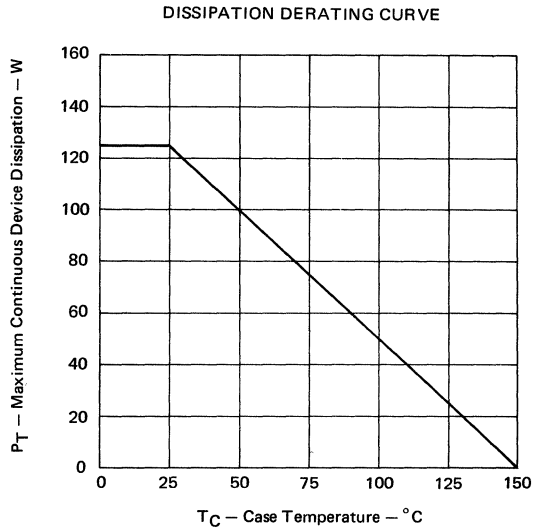


FIGURE 4

MAXIMUM SAFE OPERATING REGION

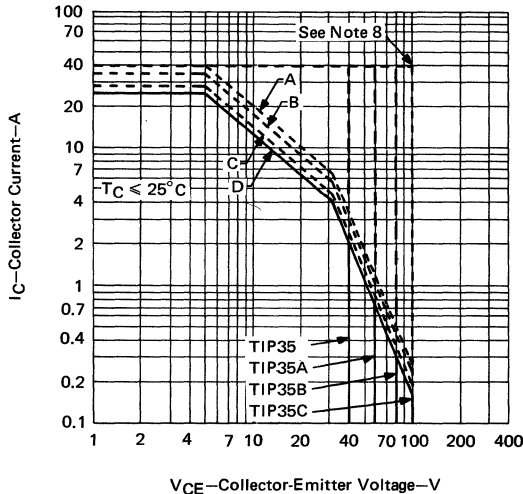


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

KEY FOR FIGURE 5

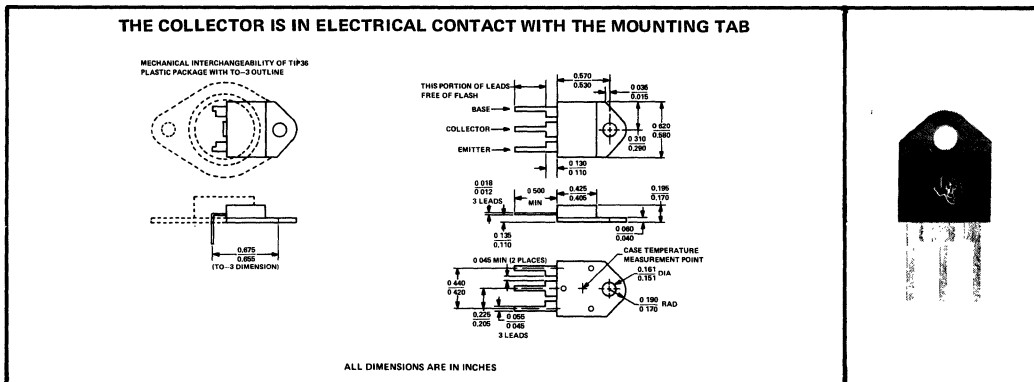
CURVE	CONDITIONS
A	$t_w = 300\ \mu\text{s}$, $d = 0.1 = 10\%$
B	$t_w = 1\ \text{ms}$, $d = 0.1 = 10\%$
C	$t_w = 10\ \text{ms}$, $d = 0.1 = 10\%$
D	D-C OPERATION

TYPES TIP36, TIP36A, TIP36B, TIP36C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP35, TIP35A, TIP35B, TIP35C

- 125 W at 25°C Case Temperature
- 25 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 1 A

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP36	TIP36A	TIP36B	TIP36C
Collector-Base Voltage	-40 V	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V	-80 V	-100 V
Emitter-Base Voltage	← -5 V →			
Continuous Collector Current	← -25 A →			
Peak Collector Current (See Note 2)	← -40 A →			
Continuous Base Current	← -5 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 125 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →			
Unclamped Inductive Load Energy (See Note 5)	← 90 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 1 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. L = 20 mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP36, TIP36A, TIP36B, TIP36C
BULLETIN NO.: DL-S-7011407, DECEMBER 1970
REPLACES BULLETIN NO.: DL-S-6810955, JULY 1968

5

TYPES TIP36, TIP36A, TIP36B, TIP36C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP36		TIP36A		TIP36B		TIP36C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-40		-60		-80		-100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-1		-1						mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$					-1		-1		
I_{CES} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$	-0.7								mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$			-0.7						
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 0$					-0.7				
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$							-0.7		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1		-1		-1		-1		mA
h_{FE} Static, Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1.5 \text{ A}$, See Notes 6 and 7	25		25		25		25		
	$V_{CE} = -4 \text{ V}$, $I_C = -15 \text{ A}$, See Notes 6 and 7	10	50	10	50	10	50	10	50	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -15 \text{ A}$, See Notes 6 and 7	-2		-2		-2		-2		V
	$V_{CE} = -4 \text{ V}$, $I_C = -25 \text{ A}$, See Notes 6 and 7	-4		-4		-4		-4		
$V_{CE(sat)}$ Collector-Emitter Voltage	$I_B = -1.5 \text{ A}$, $I_C = -15 \text{ A}$, See Notes 6 and 7	-1.8		-1.8		-1.8		-1.8		V
	$I_B = -5 \text{ A}$, $I_C = -25 \text{ A}$, See Notes 6 and 7	-4		-4		-4		-4		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$	25		25		25		25		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35.7	

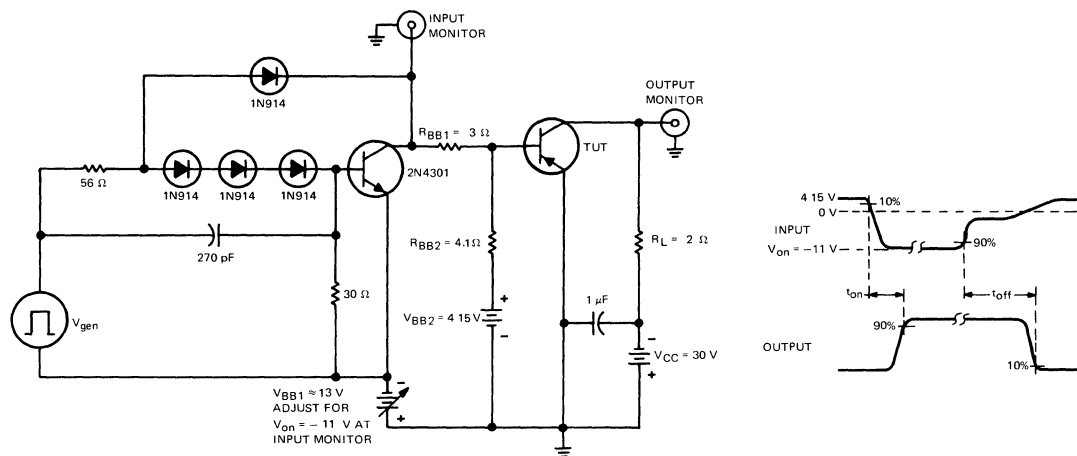
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -15 \text{ A}$, $I_{B(1)} = -1.5 \text{ A}$, $I_{B(2)} = 1.5 \text{ A}$, $V_{BE(off)} = 4.15 \text{ V}$, $R_L = 2 \Omega$, See Figure 1	1.1	μs
t_{off} Turn-Off Time		0.8	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP36, TIP36A, TIP36B, TIP36C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



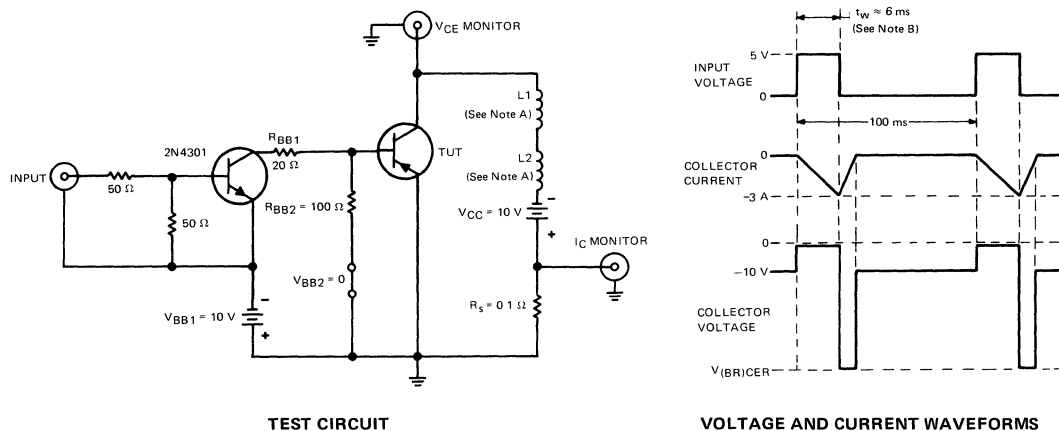
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES:
- V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 - The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

- NOTES:
- $L1$ and $L2$ are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
 - Input pulse width is increased until $I_{CM} = -3$ A.

FIGURE 2

TYPES TIP36, TIP36A, TIP36B, TIP36C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

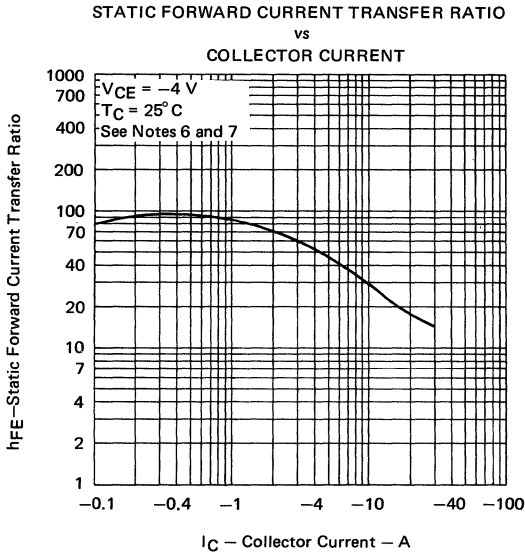


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

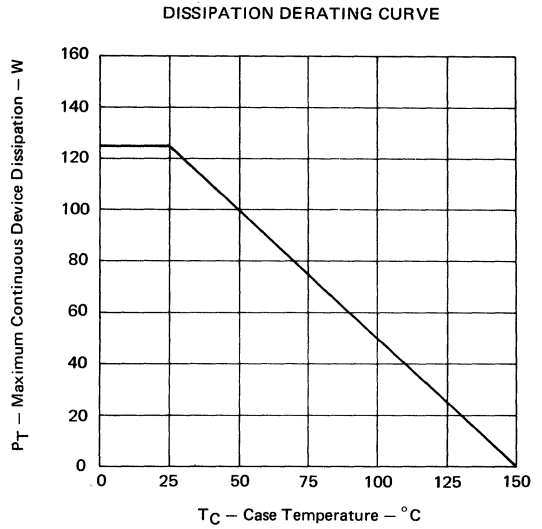


FIGURE 4

MAXIMUM SAFE OPERATING REGION

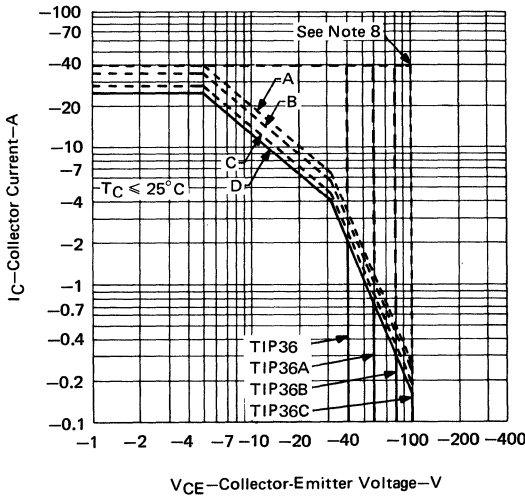


FIGURE 5

- NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

KEY FOR FIGURE 5

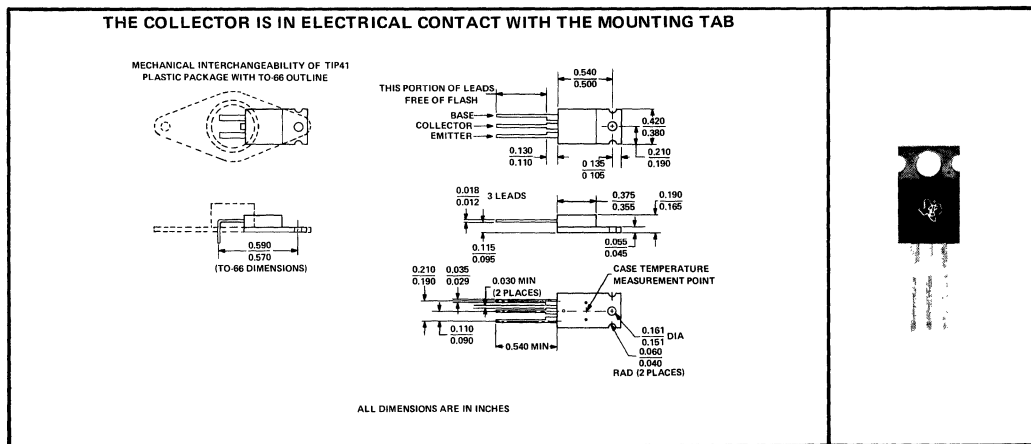
CURVE	CONDITIONS
A	$t_w = 300 \mu s$, $d = 0.1 = 10\%$
B	$t_w = 1 ms$, $d = 0.1 = 10\%$
C	$t_w = 10 ms$, $d = 0.1 = 10\%$
D	D-C OPERATION

TYPES TIP41, TIP41A, TIP41B, TIP41C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP42, TIP42A, TIP42B, TIP42C

- 65 W at 25°C Case Temperature
- 6 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

mechanical data



TYPES TIP41, TIP41A, TIP41B, TIP41C
BULLETIN NO. DLS-7011408, DECEMBER 1970

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP41	TIP41A	TIP41B	TIP41C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	← 5 V →			
Continuous Collector Current	← 6 A →			
Peak Collector Current (See Note 2)	← 10 A →			
Continuous Base Current	← 3 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 65 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.52 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP41, TIP41A, TIP41B, TIP41C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP41	TIP41A	TIP41B	TIP41C	UNIT
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	40	60	80	100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$ $V_{CE} = 60 \text{ V}$, $I_B = 0$	0.7	0.7	0.7	0.7	mA
I_{CES} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$	0.4				mA
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$		0.4			
	$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$			0.4		
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$				0.4	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1	1	1	1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 0.3 \text{ A}$, See Notes 6 and 7	30	30	30	30	
	$V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	15 75	15 75	15 75	15 75	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 6 \text{ A}$, See Notes 6 and 7	2	2	2	2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.6 \text{ A}$, $I_C = 6 \text{ A}$, See Notes 6 and 7	1.5	1.5	1.5	1.5	V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	20	20	20	20	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ MHz}$	3	3	3	3	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.92	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	

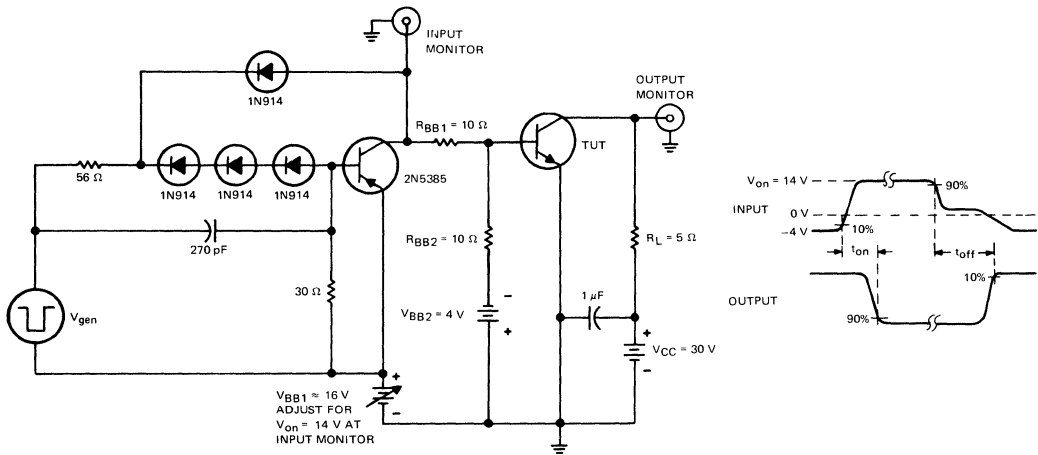
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 6 \text{ A}$, $I_B(1) = 0.6 \text{ A}$, $I_B(2) = -0.6 \text{ A}$, $V_{BE(off)} = -4 \text{ V}$, $R_L = 5 \Omega$, See Figure 1	0.6	μs
t_{off} Turn-Off Time		1	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP41, TIP41A, TIP41B, TIP41C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



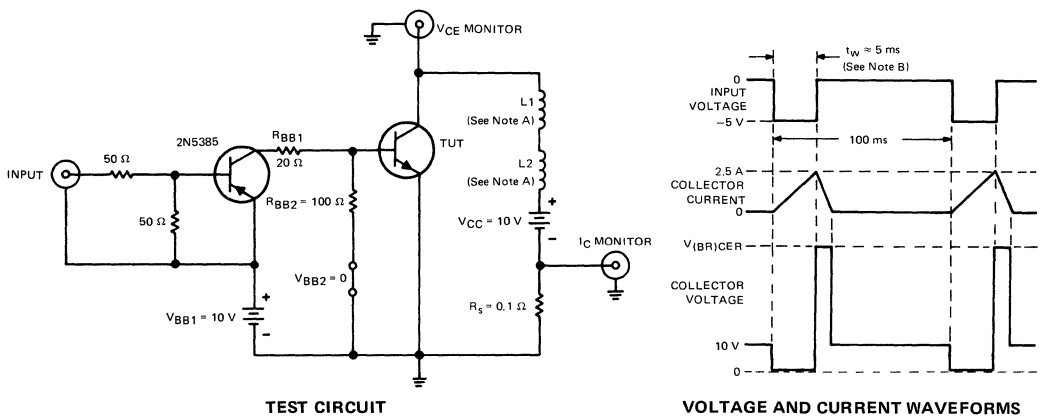
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES:
- V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - Resistors must be noninductive types.
 - The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

- NOTES:
- $L1$ and $L2$ are 10 mH , $0.11\text{ }\Omega$, Chicago Standard Transformer Corporation C-2688, or equivalent.
 - Input pulse width is increased until $I_{CM} = 2.5\text{ A}$.

FIGURE 2

TYPES TIP41, TIP41A, TIP41B, TIP41C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

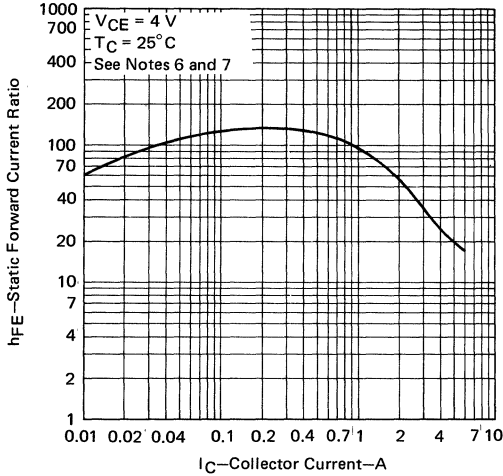


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

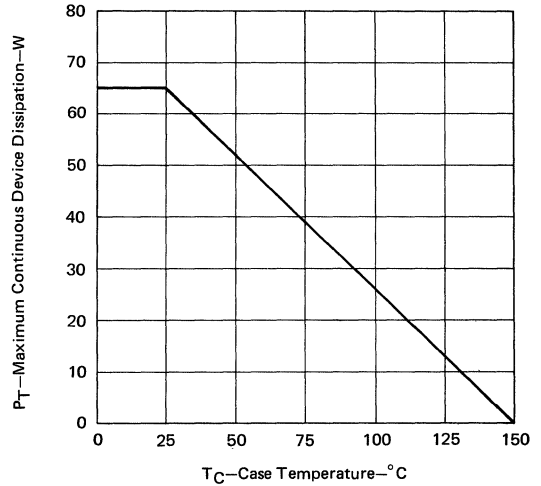


FIGURE 4

MAXIMUM SAFE OPERATING REGION

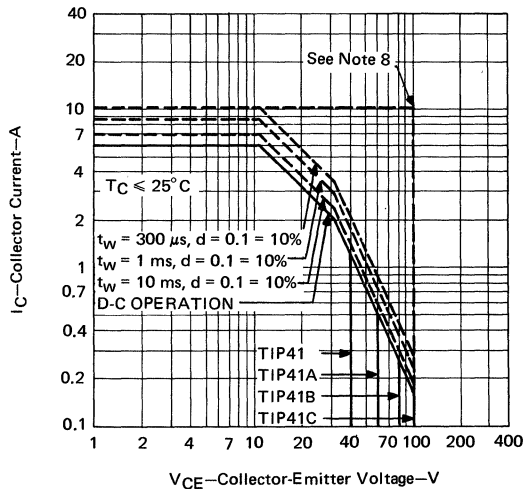


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

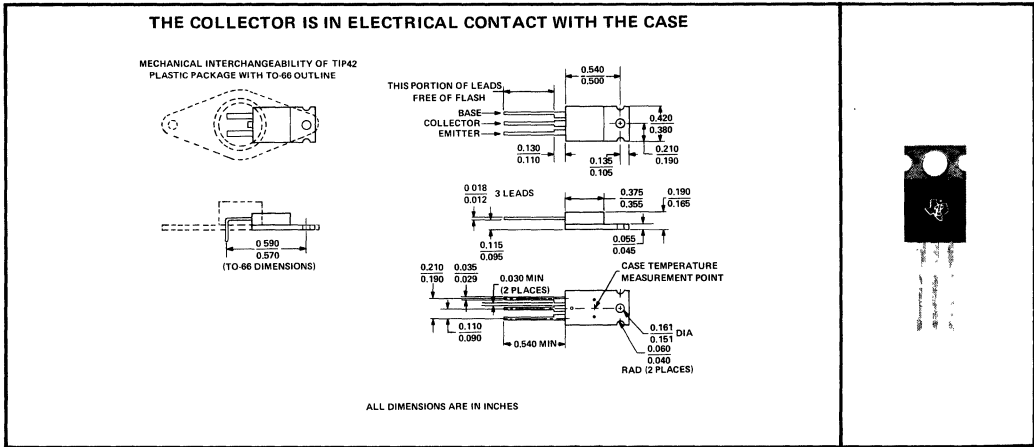
TYPES TIP42, TIP42A, TIP42B, TIP42C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP41, TIP41A, TIP41B, TIP41C

- 65 W at 25°C Case Temperature
- 6 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

TYPES TIP42, TIP42A, TIP42B, TIP42C
BULLETIN NO. DL-S-7011409, DECEMBER 1970

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP42	TIP42A	TIP42B	TIP42C
Collector-Base Voltage	-40 V	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V	-80 V	-100 V
Emitter-Base Voltage	← -5 V →			
Continuous Collector Current	← -6 A →			
Peak Collector Current (See Note 2)	← -10 A →			
Continuous Base Current	← -3 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 65 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.52 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx .1C^2L/2$.

TYPES TIP42, TIP42A, TIP42B, TIP42C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP42		TIP42A		TIP42B		TIP42C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-40		-60		-80		-100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.7		-0.7						mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$					-0.7		-0.7		
I_{CES} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$	-0.4								mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$			-0.4						
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 0$					-0.4				
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$							-0.4		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1		-1		-1		-1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -0.3 \text{ A}$, See Notes 6 and 7	30		30		30		30		
	$V_{CE} = -4 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	15	75	15	75	15	75	15	75	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -6 \text{ A}$, See Notes 6 and 7	-2		-2		-2		-2		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.6 \text{ A}$, $I_C = -6 \text{ A}$, See Notes 6 and 7	-1.5		-1.5		-1.5		-1.5		V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.92	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	

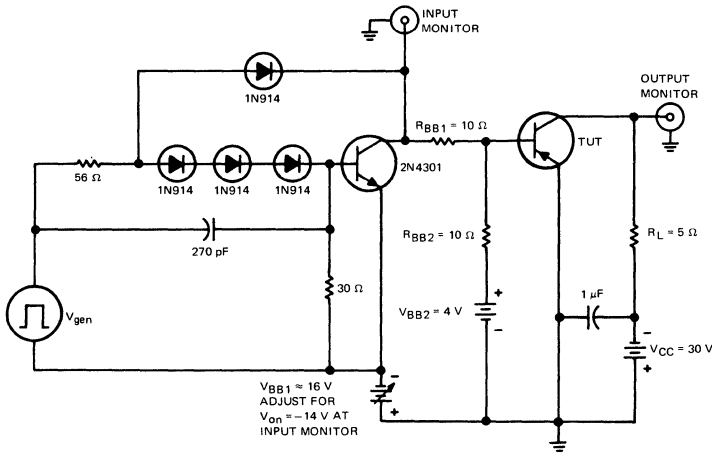
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -6 \text{ A}$, $I_B(1) = -0.6 \text{ A}$, $I_B(2) = 0.6 \text{ A}$, $V_{BE(off)} = 4 \text{ V}$, $R_L = 5 \Omega$, See Figure 1	0.4	μs
t_{off} Turn-Off Time		0.7	

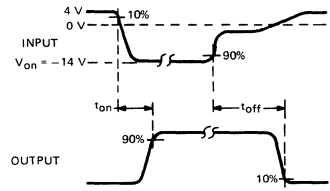
† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP42, TIP42A, TIP42B, TIP42C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



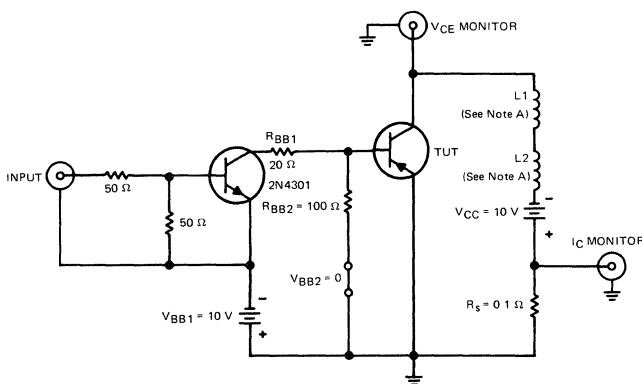
TEST CIRCUIT



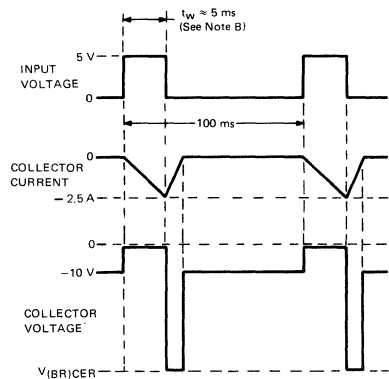
VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{OUT} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
 B. Input pulse width is increased until $I_{CM} = -2.5$ A.

FIGURE 2

TYPES TIP42, TIP42A, TIP42B, TIP42C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

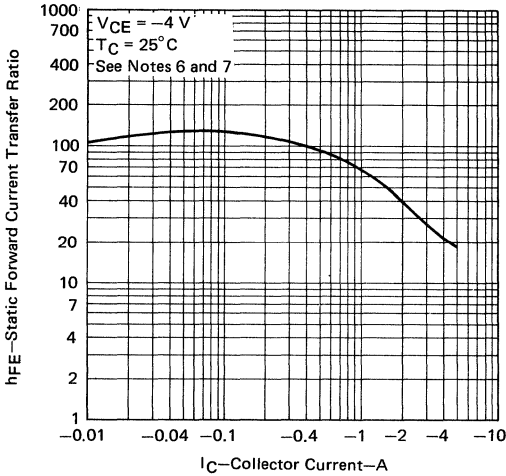


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

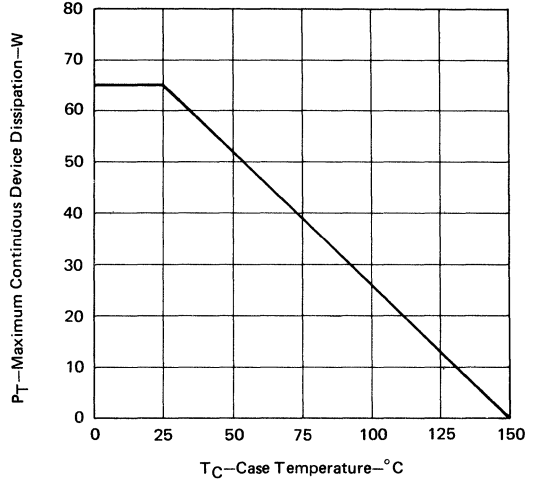


FIGURE 4

MAXIMUM SAFE OPERATING REGION

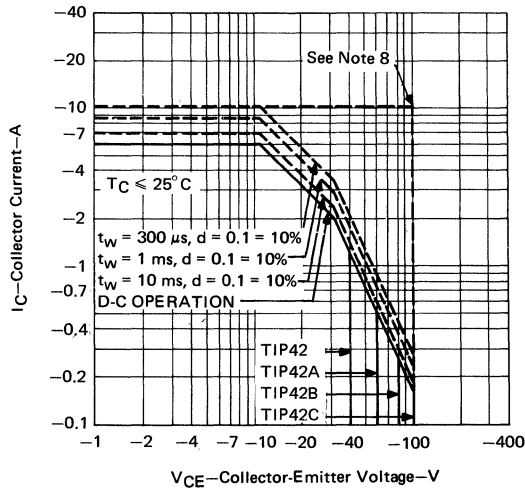


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

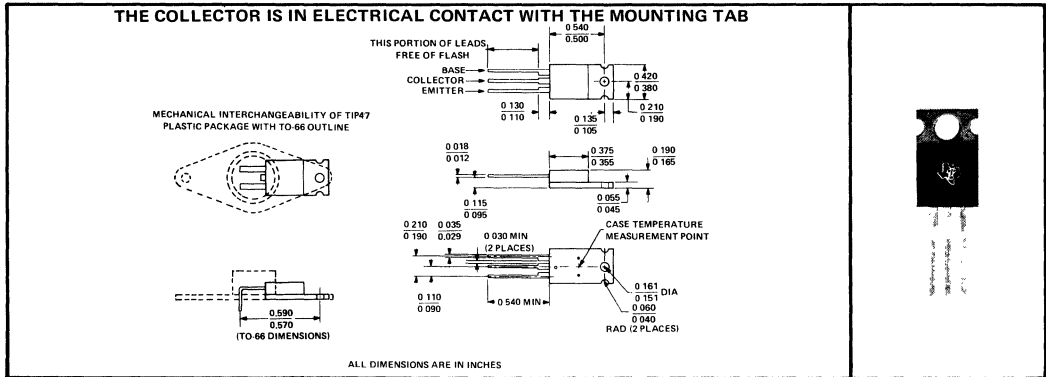
TYPES TIP47 THRU TIP50 N-P-N SILICON POWER TRANSISTORS

TYPES TIP47, TIP48, TIP49, TIP50
BULLETIN NO. DLS-7111593, DECEMBER 1971

**HIGH VOLTAGE, HIGH FORWARD AND REVERSE ENERGY
DESIGNED FOR INDUSTRIAL AND CONSUMER APPLICATION**

- 20 mJ Reverse-Energy Rating
- 250 V to 400 V Min $V_{(BR)CEO}$
- 40 W at 25°C Case Temperature
- 1-A Rated Collector Current
- 10 MHz Min f_T at 10 V, 0.2 A

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP47	TIP48	TIP49	TIP50
Collector-Base Voltage	350 V	400 V	450 V	500 V
Collector-Emitter Voltage (See Note 1)	250 V	300 V	350 V	400 V
Emitter-Base Voltage	5 V	5 V	5 V	5 V
Continuous Collector Current	1 A			
Peak Collector Current (See Note 2)	2 A			
Continuous Base Current	0.6 A			
Safe Operating Areas at (or below) 25°C Case Temperature	See Figures 6 and 7			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	40 W			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W			
Unclamped Inductive Load Energy (See Note 5)	20 mJ			
Operating Collector Junction Temperature Range	-65°C to 150°C			
Storage Temperature Range	-65°C to 150°C			
Terminal Temperature 1/8 Inch from Case for 10 Seconds	260°C			

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 1$ ms, duty cycle $\leq 10\%$.
 3. For operation above 25°C case temperature, refer to Dissipation Derating Curve, Figure 8.
 4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 9.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 5. $L = 100$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP47 THRU TIP50

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP47	TIP48	TIP49	TIP50	UNIT
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	250	300	350	400	V
I_{CEO} Collector Cutoff Current	$V_{CE} = 150 \text{ V}$, $I_B = 0$	1				mA
	$V_{CE} = 200 \text{ V}$, $I_B = 0$		1			
	$V_{CE} = 250 \text{ V}$, $I_B = 0$			1		
	$V_{CE} = 300 \text{ V}$, $I_B = 0$				1	
I_{CES} Collector Cutoff Current	$V_{CE} = 350 \text{ V}$, $V_{BE} = 0$	1				mA
	$V_{CE} = 400 \text{ V}$, $V_{BE} = 0$		1			
	$V_{CE} = 450 \text{ V}$, $V_{BE} = 0$			1		
	$V_{CE} = 500 \text{ V}$, $V_{BE} = 0$				1	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1	1	1	1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.3 \text{ A}$	30 150	30 150	30 150	30 150	
	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$	10	10	10	10	
V_{BE} Base-Emitter Voltage	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$	1.5	1.5	1.5	1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.2 \text{ A}$, $I_C = 1 \text{ A}$	1	1	1	1	V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ kHz}$	25	25	25	25	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 2 \text{ MHz}$	5	5	5	5	

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_B(1) = 100 \text{ mA}$, $I_B(2) = -100 \text{ mA}$	0.2	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -5 \text{ V}$, $R_L = 200 \Omega$, See Figure 4	2	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

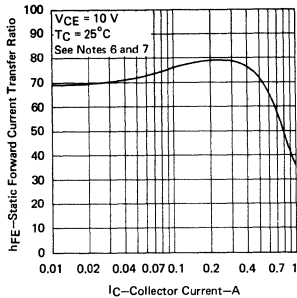


FIGURE 1

BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT

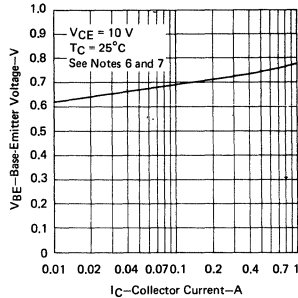


FIGURE 2

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

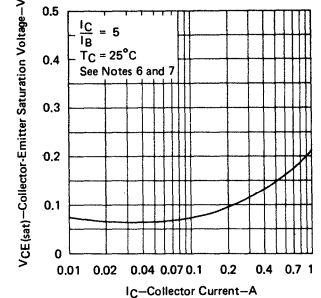


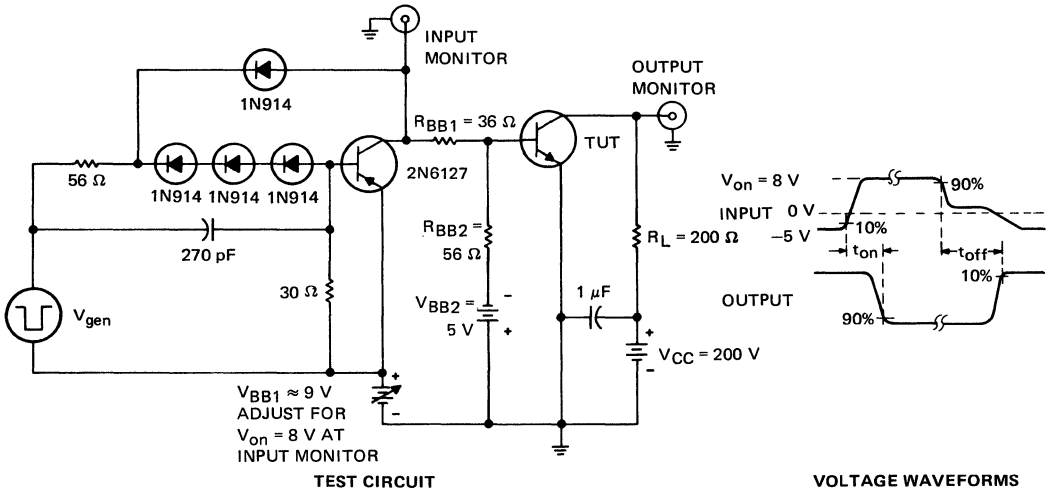
FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. $t_W = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP47 THRU TIP50 N-P-N SILICON POWER TRANSISTORS

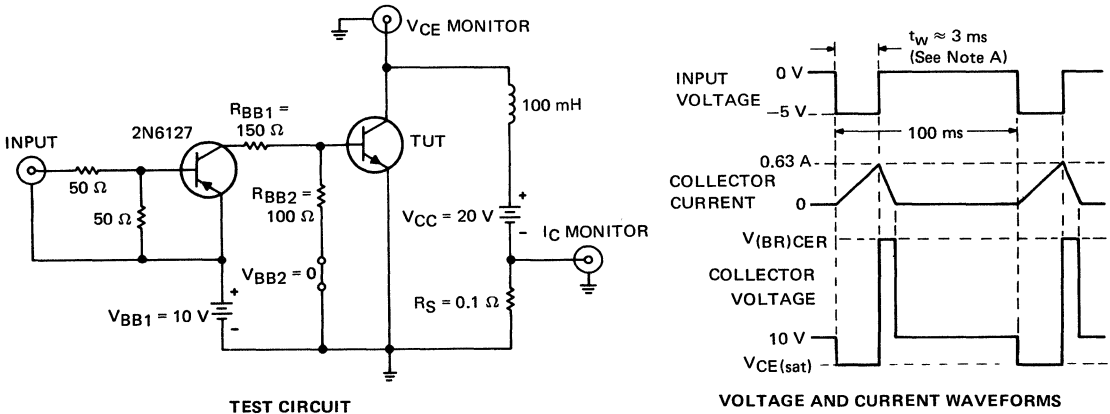
PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. V_{gen} is a -30 V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - B. The V_{gen} waveform is supplied by a generator with the following characteristics: $\tau_r \leq 15\text{ ns}$, $Z_{out} = 50\ \Omega$, $t_w = 20\ \mu\text{s}$, duty cycle $\leq 2\%$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $\tau_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - D. Resistors must be noninductive types.
 - E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 4

INDUCTIVE LOAD SWITCHING



NOTE A: Input pulse width is increased until $I_{CM} = 0.63\text{ A}$.

FIGURE 5

TYPES TIP47 THRU TIP50 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

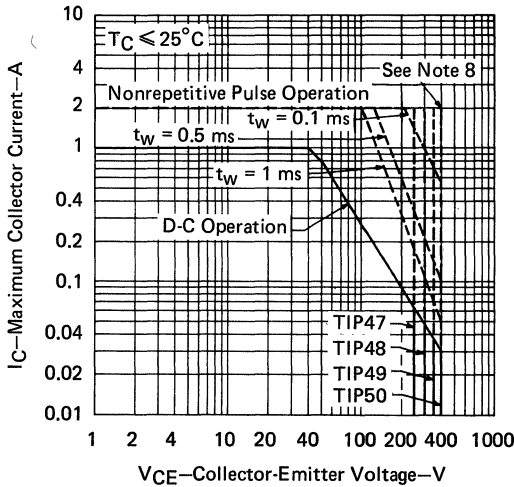


FIGURE 6

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

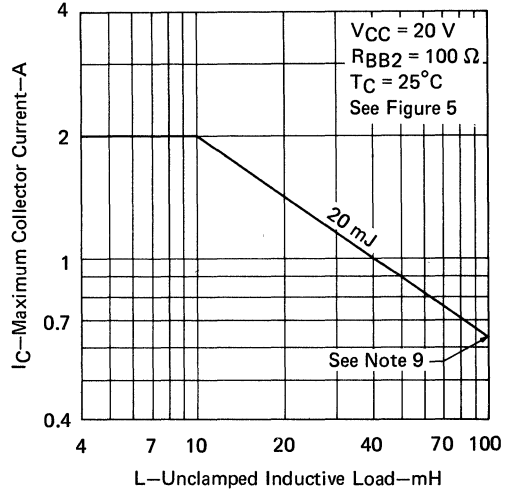


FIGURE 7

- NOTES: 8. This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.
9. Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

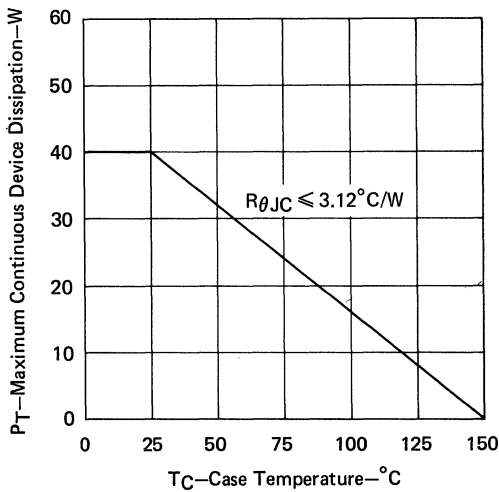


FIGURE 8

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

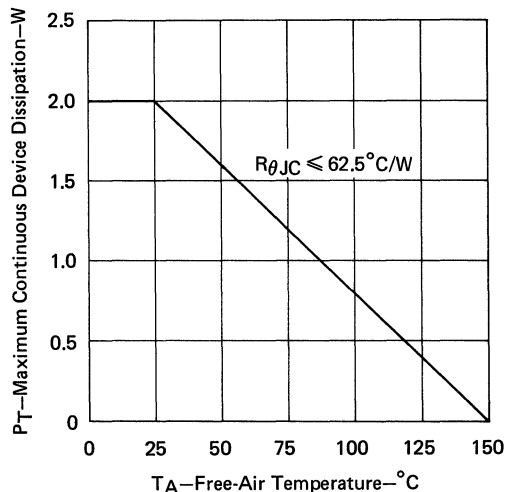


FIGURE 9

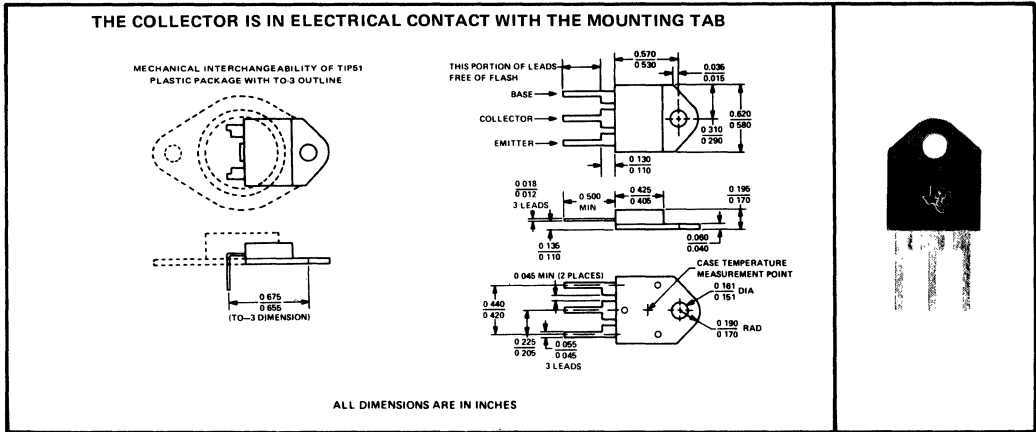
TYPES TIP51 THRU TIP54 N-P-N SILICON POWER TRANSISTORS

TYPES TIP51, TIP52, TIP53, TIP54
BULLETIN NO. DLS-711839, SEPTEMBER 1971

**HIGH VOLTAGE, HIGH FORWARD AND REVERSE ENERGY
DESIGNED FOR INDUSTRIAL AND CONSUMER APPLICATIONS**

- 100 mJ Reverse-Energy Rating
- 250 V to 400 V Min $V(BR)_{CEO}$
- 100 W at 25°C Case Temperature
- 5 A Peak Collector Current
- 2.5 MHz Min f_T at 10 V, 0.2 A

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP51	TIP52	TIP53	TIP54
Collector-Base Voltage	350 V	400 V	450 V	500 V
Collector-Emitter Voltage (See Note 1)	250 V	300 V	350 V	400 V
Emitter-Base Voltage	5 V	5 V	5 V	5 V
Continuous Collector Current	← 3 A →			
Peak Collector Current (See Note 2)	← 5 A →			
Continuous Base Current	← 0.6 A →			
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 6 and 7 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 100 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →			
Unclamped Inductive Load Energy (See Note 5)	← 100 mJ →			
Operating Collector Junction Temperature Range	← -65°C to 150°C →			
Storage Temperature Range	← -65°C to 150°C →			
Terminal Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. For operation above 25°C case temperature, refer to Dissipation Derating Curve, Figure 8.
 4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 9.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 5. $L = 30$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L / 2$.

TYPES TIP51 THRU TIP54 N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP51	TIP52	TIP53	TIP54	UNIT		
		MIN	MAX	MIN	MAX		MIN	MAX
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	250	300	350	400	V		
I_{CEO} Collector Cutoff Current	$V_{CE} = 150 \text{ V}$, $I_B = 0$	1				mA		
	$V_{CE} = 200 \text{ V}$, $I_B = 0$		1					
	$V_{CE} = 250 \text{ V}$, $I_B = 0$			1				
	$V_{CE} = 300 \text{ V}$, $I_B = 0$				1			
I_{CES} Collector Cutoff Current	$V_{CE} = 350 \text{ V}$, $V_{BE} = 0$	1				mA		
	$V_{CE} = 400 \text{ V}$, $V_{BE} = 0$		1					
	$V_{CE} = 450 \text{ V}$, $V_{BE} = 0$			1				
	$V_{CE} = 500 \text{ V}$, $V_{BE} = 0$				1			
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1	1	1	1	mA		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.3 \text{ A}$, See Notes 6 and 7	30	150	30	150	30	150	
	$V_{CE} = 10 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	10	10	10	10	10	10	
V_{BE} Base-Emitter Voltage	$V_{CE} = 10 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	1.5	1.5	1.5	1.5	V		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.6 \text{ A}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	1.5	1.5	1.5	1.5	V		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ kHz}$	30	30	30	30			
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.2 \text{ A}$, $f = 1 \text{ MHz}$	2.5	2.5	2.5	2.5			

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $I_B(1) = 100 \text{ mA}$, $I_B(2) = -100 \text{ mA}$, $V_{BE(off)} = -5 \text{ V}$, $R_L = 200 \Omega$, See Figure 4	0.25	μs
t_{off} Turn-Off Time		5	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPICAL CHARACTERISTICS

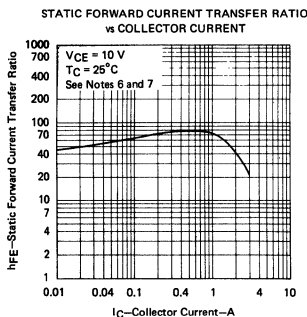


FIGURE 1

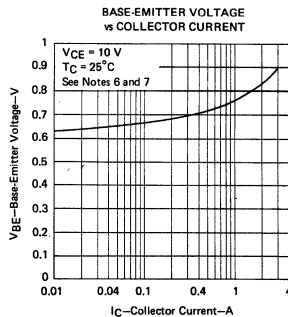


FIGURE 2

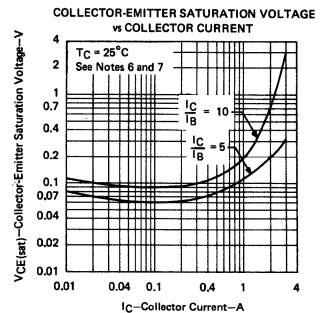


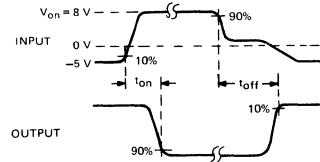
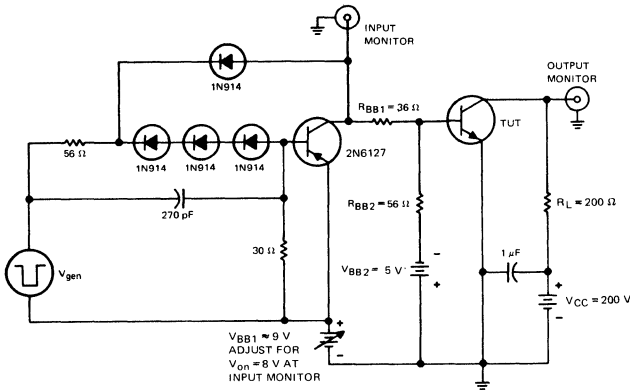
FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. $t_W = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP51 THRU TIP54 N-P-N SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



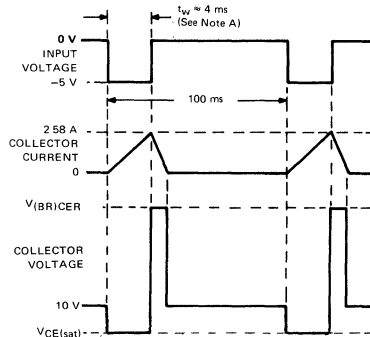
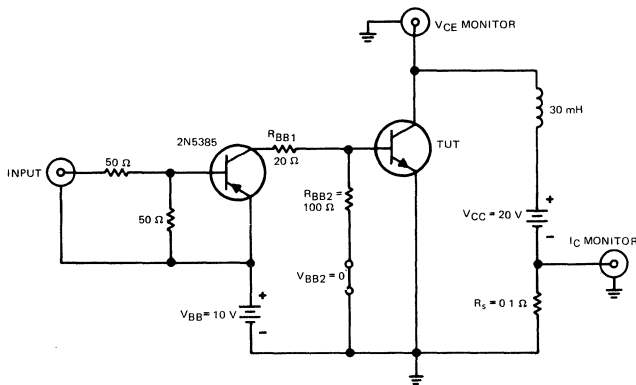
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. V_{gen} is a -30 V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 20\ \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 4

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = 2.58$ A.

FIGURE 5

TYPES TIP51 THRU TIP54 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

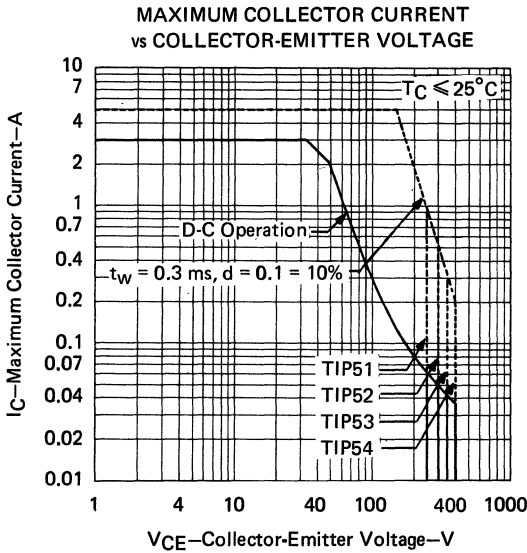


FIGURE 6

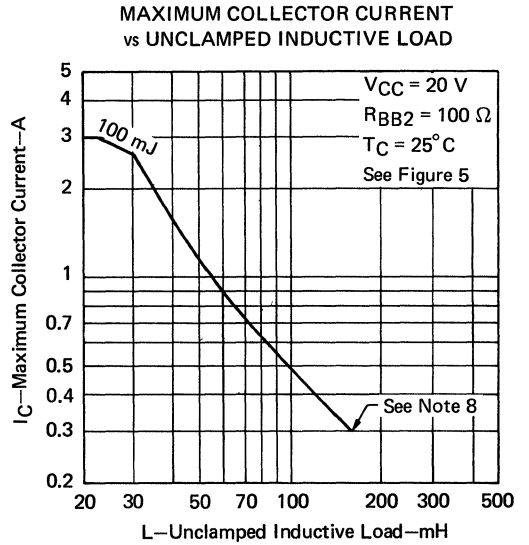


FIGURE 7

NOTE 8: Above this point, the safe operating area has not been defined.

THERMAL INFORMATION

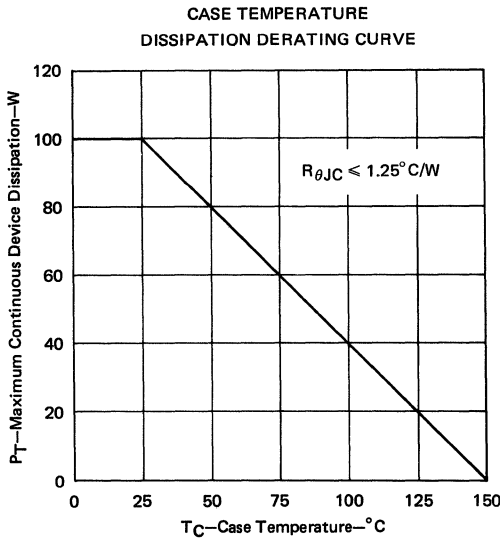


FIGURE 8

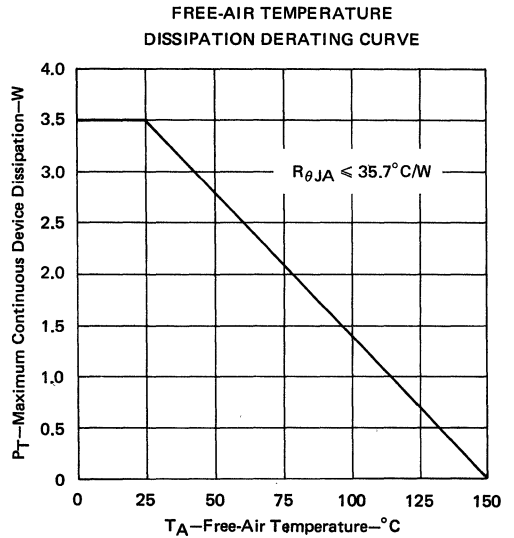


FIGURE 9

TYPES TIP110, TIP111, TIP112

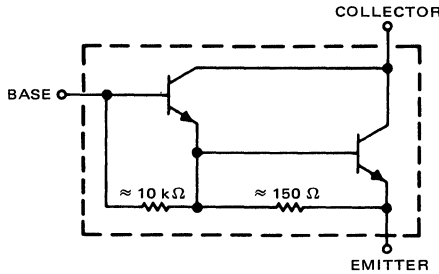
N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

SERIES TIP110, TIP111, TIP112
BULLETIN NO. DLS-7111646, DECEMBER 1971

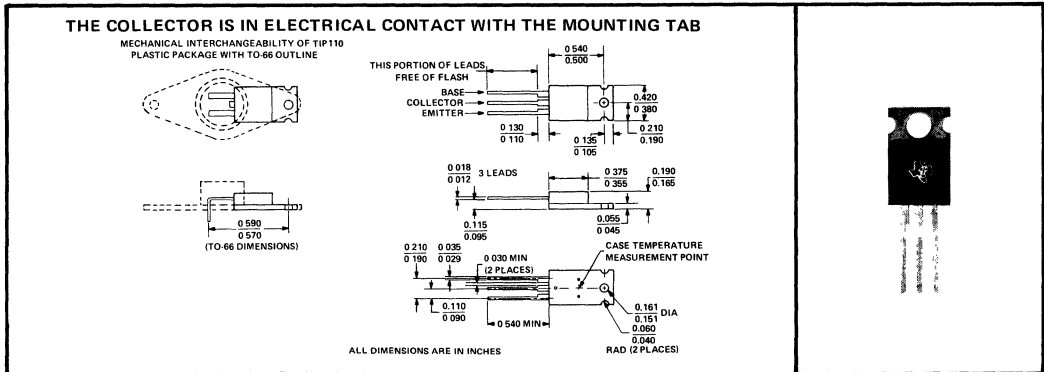
DESIGNED FOR COMPLEMENTARY USE WITH TIP115, TIP116, TIP117

- High SOA Capability, 40 V and 1.25 A
- 50 W at 25°C Case Temperature
- Min h_{FE} of 500 at 4 V, 2 A
- 2-A Rated Collector Current
- 25-mJ Reverse Energy Rating

device schematic



mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP110	TIP111	TIP112
Collector-Base Voltage	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	60 V	80 V	100 V
Emitter-Base Voltage	5 V	5 V	5 V
Continuous Collector Current	← 2 A →		
Peak Collector Current (See Note 2)	← 4 A →		
Continuous Base Current	← 50 mA →		
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 7 and 8 →		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 50 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →		
Unclamped Inductive Load Energy (See Note 5)	← 25 mJ →		
Operating Collector Junction Temperature Range	← -65°C to 150°C →		
Storage Temperature Range	← -65°C to 150°C →		
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →		

- NOTES:
1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.4 W/°C or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP110, TIP111, TIP112

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP110	TIP111	TIP112	UNIT	
		MIN MAX	MIN MAX	MIN MAX		
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	60	80	100	V	
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	2			mA	
	$V_{CE} = 40 \text{ V}$, $I_B = 0$		2			
	$V_{CE} = 50 \text{ V}$, $I_B = 0$			2		
I_{CBO} Collector Cutoff Current	$V_{CB} = 60 \text{ V}$, $I_E = 0$	1			mA	
	$V_{CB} = 80 \text{ V}$, $I_E = 0$		1			
	$V_{CB} = 100 \text{ V}$, $I_E = 0$			1		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	2	2	2	mA	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$	See Notes 6 and 7	1000	1000	1000	
	$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$		500	500	500	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 6 and 7	2.8	2.8	2.8	V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 8 \text{ mA}$, $I_C = 2 \text{ A}$, See Notes 6 and 7	2.5	2.5	2.5	V	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

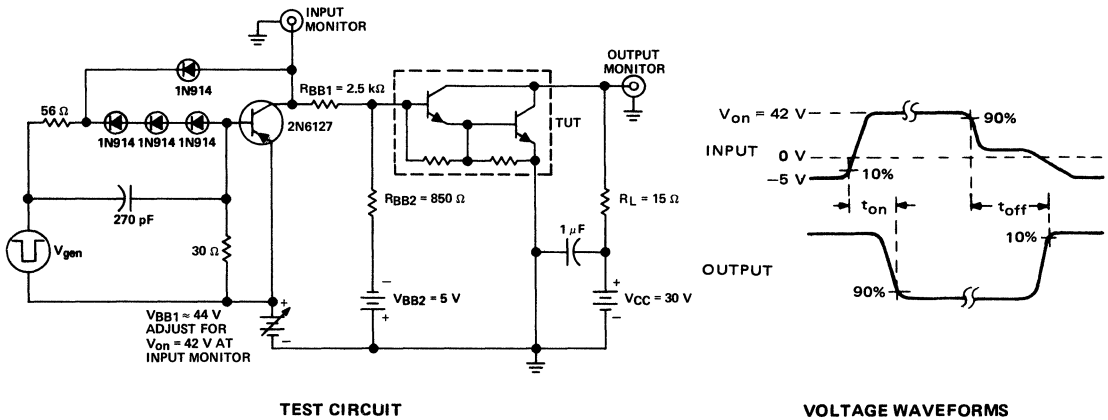
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switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 2 \text{ A}$, $I_{B(1)} = 8 \text{ mA}$, $I_{B(2)} = -8 \text{ mA}$, $V_{BE(off)} = -5 \text{ V}$, $R_L = 15 \Omega$, See Figure 1	2.6	μs
t_{off} Turn-Off Time		4.5	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.

B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.

C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.

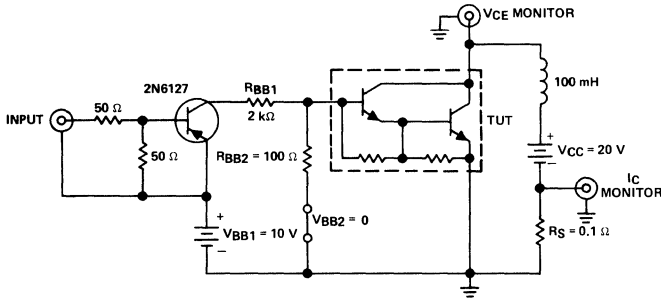
D. Resistors must be noninductive types.

E. The d-c power supplies may require additional bypassing in order to minimize ringing.

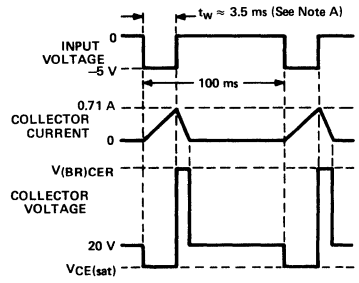
FIGURE 1

TYPES TIP110, TIP111, TIP112 N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = 0.71$ A.

FIGURE 2

TYPICAL CHARACTERISTICS

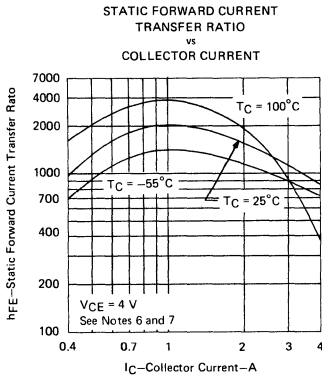


FIGURE 3

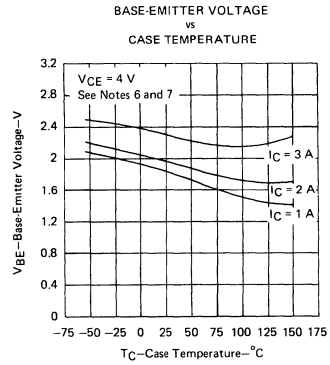


FIGURE 4

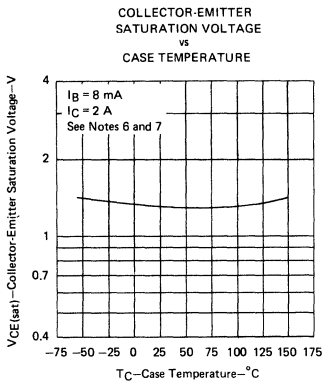


FIGURE 5

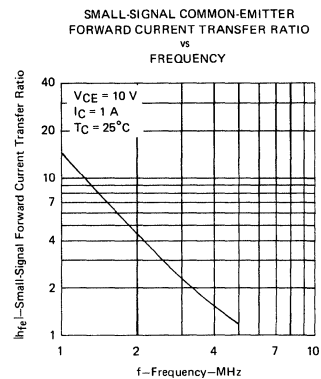


FIGURE 6

TYPES TIP110, TIP111, TIP112

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

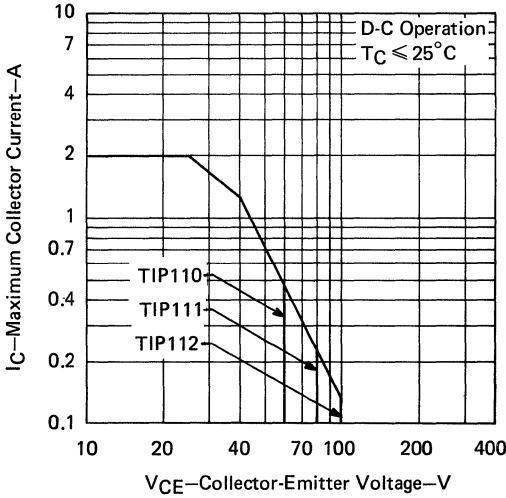


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

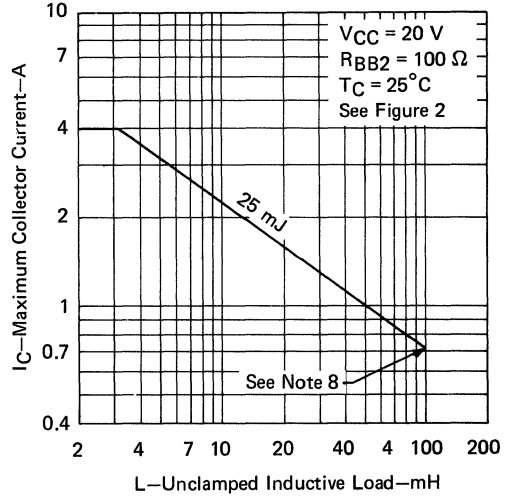


FIGURE 8

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

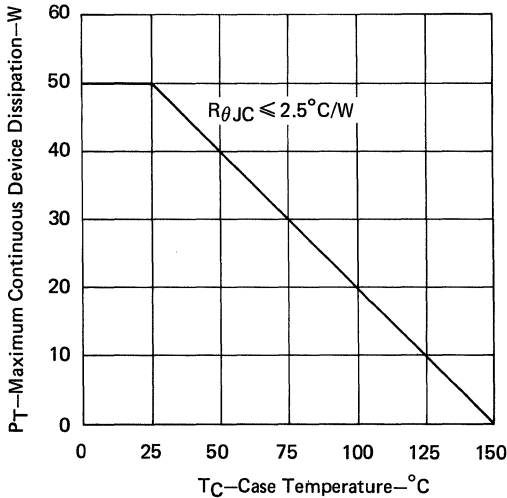


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

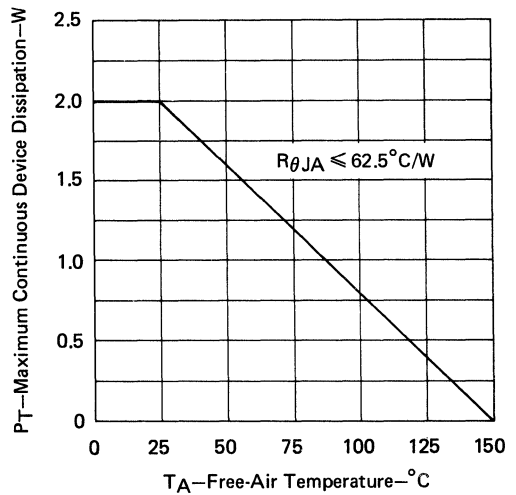


FIGURE 10

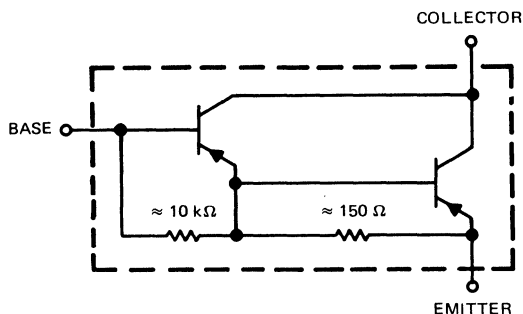
TYPES TIP115, TIP116, TIP117 P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

DESIGNED FOR COMPLEMENTARY USE WITH TIP110, TIP111, TIP112

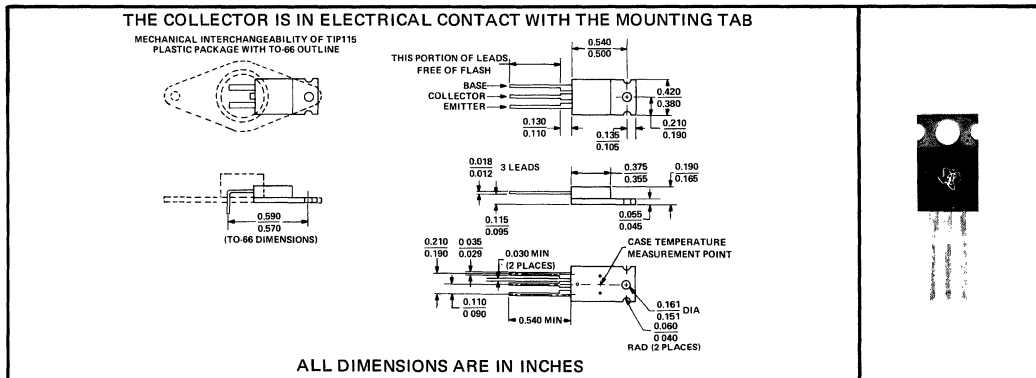
- High SOA Capability, 40 V and 1.25 A
- 50 W at 25°C Case Temperature
- 2-A Rated Collector Current
- Min h_{FE} of 500 at 4 V, 2 A
- 25-mJ Reverse Energy Rating

SERIES TIP115, TIP116, TIP117
BULLETIN NO. DLS-7111643, DECEMBER 1971

device schematic



mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP115	TIP116	TIP117
Collector-Base Voltage	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-60 V	-80 V	-100 V
Emitter-Base Voltage	-5 V	-5 V	-5 V
Continuous Collector Current	←-2 A→		
Peak Collector Current (See Note 2)	←-4 A→		
Continuous Base Current	←-50 mA→		
Safe Operating Areas at (or below) 25°C Case Temperature	←-See Figures 7 and 8→		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	←-50 W→		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	←-2 W→		
Unclamped Inductive Load Energy (See Note 5)	←-25 mJ→		
Operating Collector Junction Temperature Range	←-65°C to 150°C→		
Storage Temperature Range	←-65°C to 150°C→		
Lead Temperature 1/8 Inch from Case for 10 Seconds	←-260°C→		

- NOTES:
1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.4 W/°C or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP115, TIP116, TIP117

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP115	TIP116	TIP117	UNIT	
		MIN MAX	MIN MAX	MIN MAX		
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-60	-80	-100	V	
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-2			mA	
	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-2			
	$V_{CE} = -50 \text{ V}$, $I_B = 0$			-2		
I_{CBO} Collector Cutoff Current	$V_{CB} = -60 \text{ V}$, $I_E = 0$	-1			mA	
	$V_{CB} = -80 \text{ V}$, $I_E = 0$		-1			
	$V_{CB} = -100 \text{ V}$, $I_E = 0$			-1		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-2	-2	-2	mA	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$	See Notes 6 and 7	1000	1000	1000	
	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$		500	500	500	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 6 and 7	-2.8	-2.8	-2.8	V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -8 \text{ mA}$, $I_C = -2 \text{ A}$, See Notes 6 and 7	-2.5	-2.5	-2.5	V	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

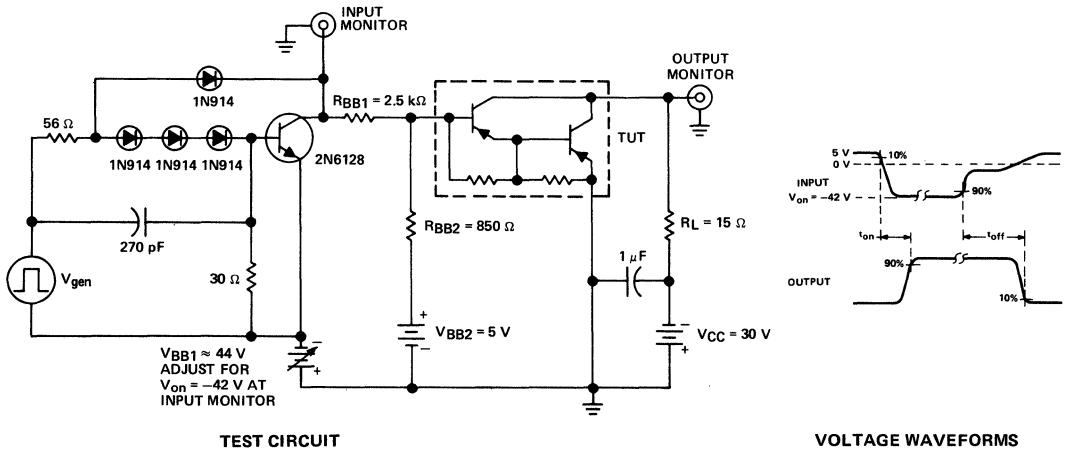
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switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -2 \text{ A}$, $I_B(1) = -8 \text{ mA}$, $I_B(2) = 8 \text{ mA}$,	2.6	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 5 \text{ V}$, $R_L = 15 \Omega$, See Figure 1	4.5	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.

B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.

C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.

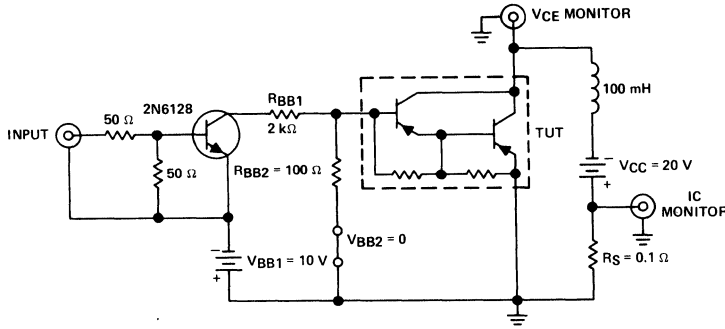
D. Resistors must be noninductive types.

E. The d-c power supplies may require additional bypassing in order to minimize ringing.

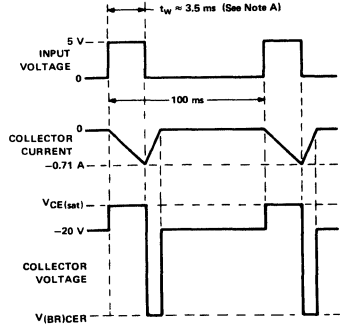
FIGURE 1

TYPES TIP115, TIP116, TIP117 P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = -0.71$ A.

FIGURE 2

TYPICAL CHARACTERISTICS

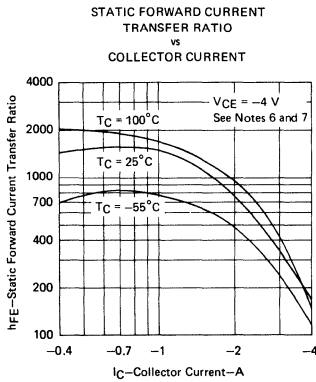


FIGURE 3

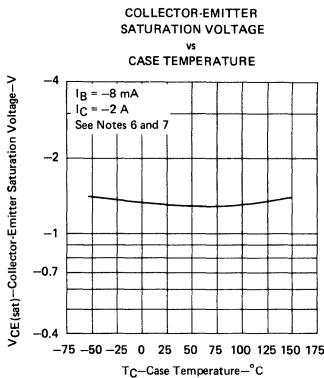


FIGURE 5

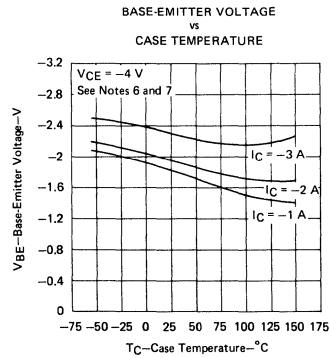


FIGURE 4

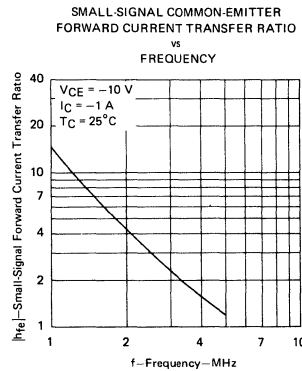


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP115, TIP116, TIP117

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

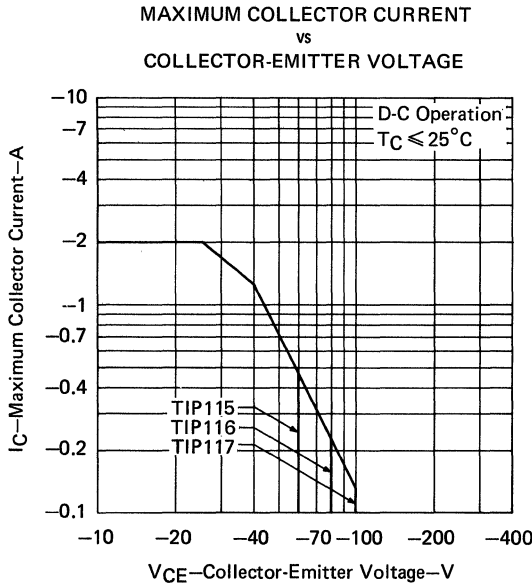


FIGURE 7

NOTE 8: Above this point the safe operating area has not been defined.

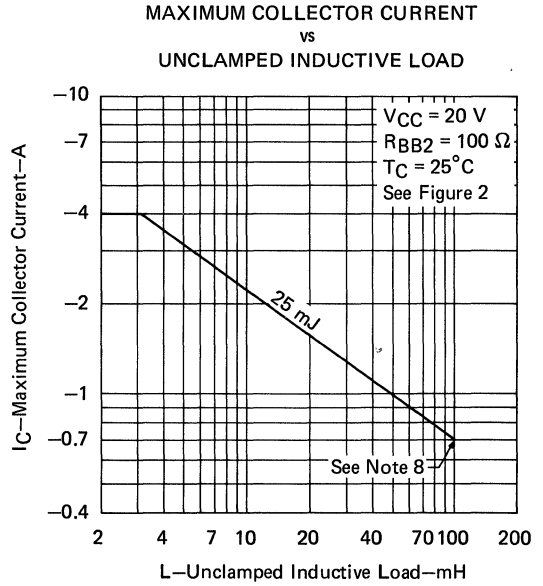


FIGURE 8

THERMAL INFORMATION

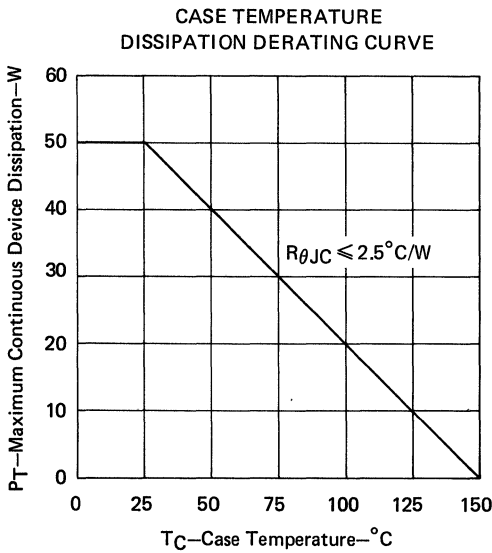


FIGURE 9

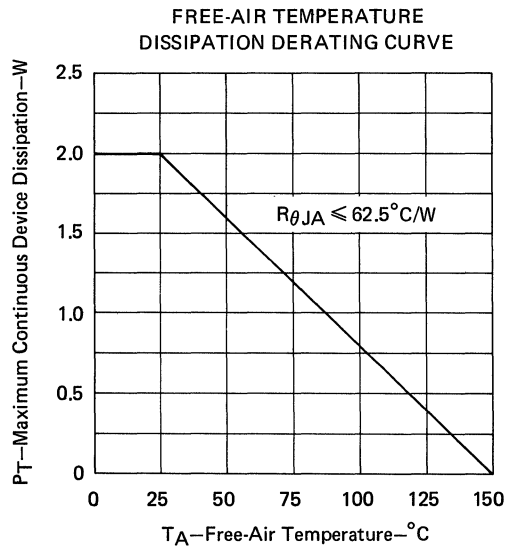


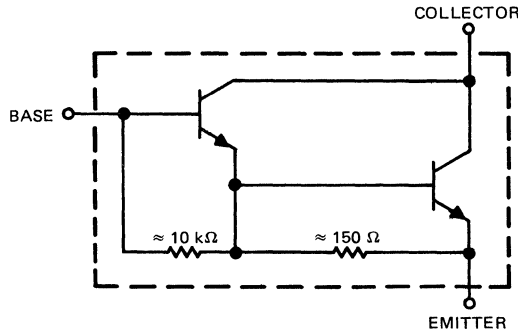
FIGURE 10

TYPES TIP120, TIP121, TIP122 N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

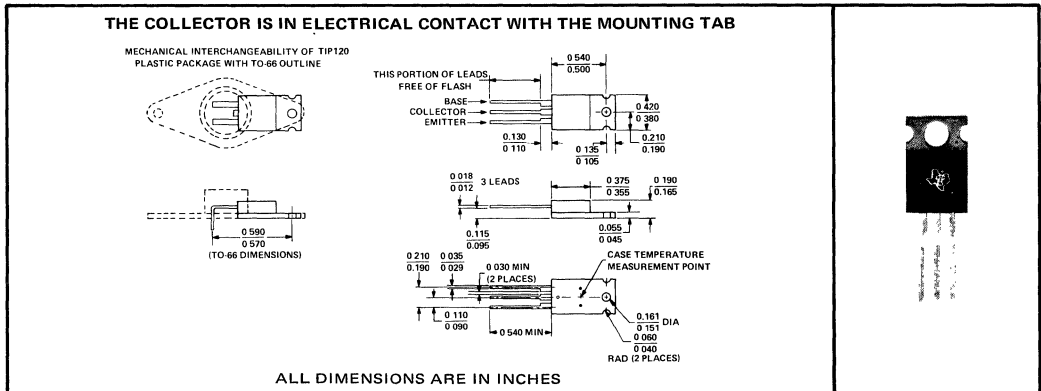
DESIGNED FOR COMPLEMENTARY USE WITH TIP125, TIP126, TIP127

- 65 W at 25°C Case Temperature
- 5 A Rated Collector Current
- Min h_{FE} of 1000 at 3 V, 3 A
- 50 mJ Reverse Energy Rating

device schematic



mechanical data



TYPES TIP120, TIP121, TIP122
BULLETIN NO. DLS-111588, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP120	TIP121	TIP122
Collector-Base Voltage	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	60 V	80 V	100 V
Emitter-Base Voltage	5 V	5 V	5 V
Continuous Collector Current	← 5 A →		
Peak Collector Current (See Note 2)	← 8 A →		
Continuous Base Current	← 0.1 A →		
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 7 and 8 →		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 65 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →		
Unclamped Inductive Load Energy (See Note 5)	← 50 mJ →		
Operating Collector Junction Temperature Range	← -65°C to 150°C →		
Storage Temperature Range	← -65°C to 150°C →		
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →		

- NOTES:
1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of $0.52 \text{ W}/^\circ\text{C}$ or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 150°C free-air temperature at the rate of $16 \text{ mW}/^\circ\text{C}$ or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100 \text{ mH}$, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0 \text{ V}$, $R_S = 0.1 \Omega$, $V_{CC} = 20 \text{ V}$. Energy $\approx I_C^2 L/2$.

TYPES TIP120, TIP121, TIP122

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP120	TIP121	TIP122	UNIT
		MIN	MAX	MIN	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	60	80	100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	0.5			mA
	$V_{CE} = 40 \text{ V}$, $I_B = 0$	0.5			
	$V_{CE} = 50 \text{ V}$, $I_B = 0$	0.5			
I_{CBO} Collector Cutoff Current	$V_{CB} = 60 \text{ V}$, $I_E = 0$	0.2			mA
	$V_{CB} = 80 \text{ V}$, $I_E = 0$	0.2			
	$V_{CB} = 100 \text{ V}$, $I_E = 0$	0.2			
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	2	2	2	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 3 \text{ V}$, $I_C = 0.5 \text{ A}$	1000	1000	1000	
	$V_{CE} = 3 \text{ V}$, $I_C = 3 \text{ A}$	1000	1000	1000	
V_{BE} Base-Emitter Voltage	$V_{CE} = 3 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 6 and 7	2.5	2.5	2.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 12 \text{ mA}$, $I_C = 3 \text{ A}$	2			V
	$I_B = 20 \text{ mA}$, $I_C = 5 \text{ A}$	4			

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

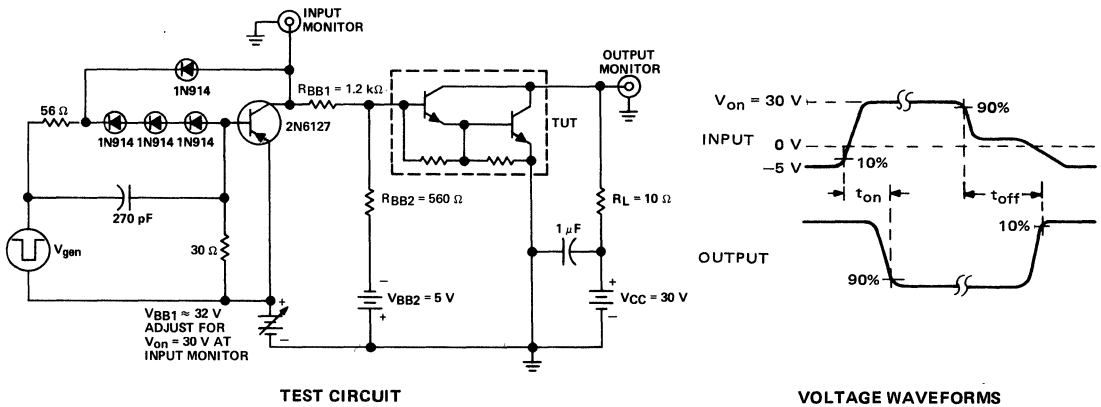
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 3 \text{ A}$, $I_{B(1)} = 12 \text{ mA}$, $I_{B(2)} = -12 \text{ mA}$	1.5	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -5 \text{ V}$, $R_L = 10 \Omega$, See Figure 1	8.5	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

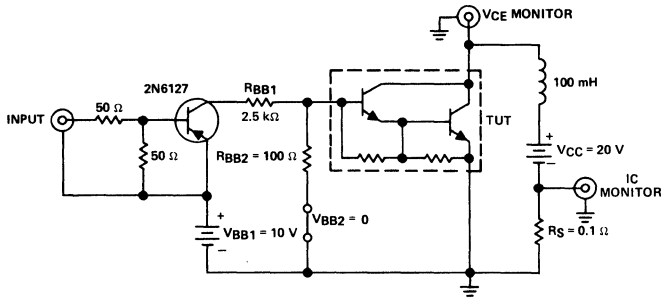


- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

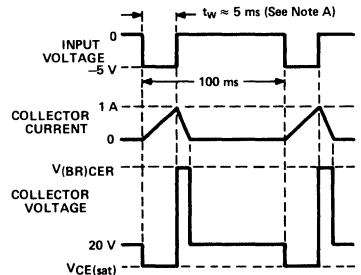
FIGURE 1

TYPES TIP120, TIP121, TIP122 N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = 1 \text{ A}$.

FIGURE 2

TYPICAL CHARACTERISTICS

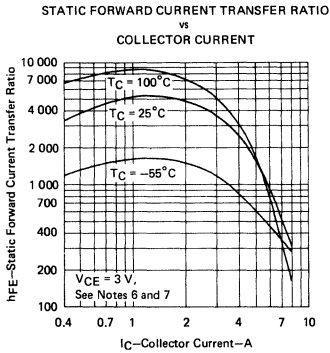


FIGURE 3

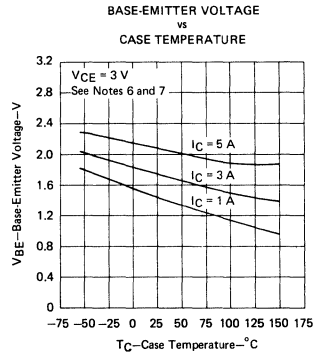


FIGURE 4

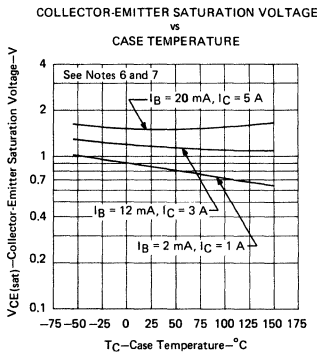


FIGURE 5

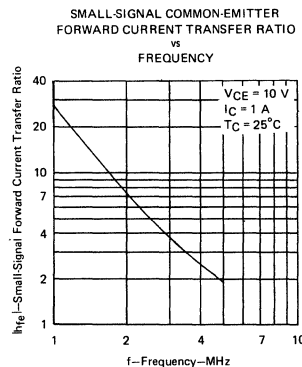


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP120, TIP121, TIP122

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

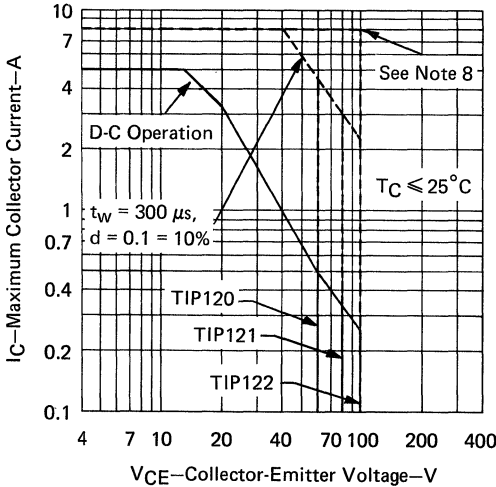


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

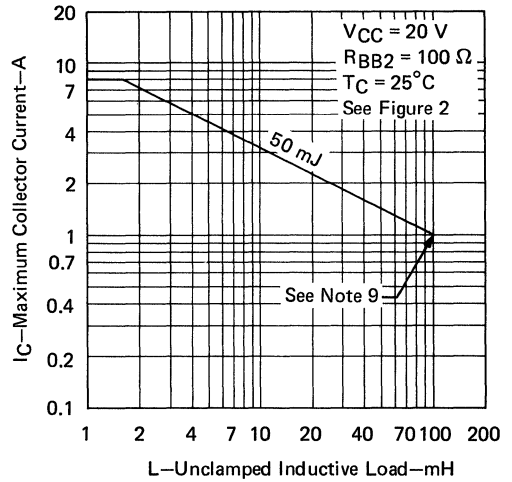


FIGURE 8

- NOTES: 8. This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.
9. Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

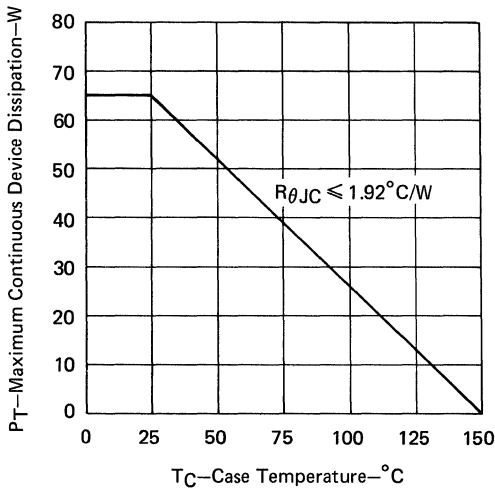


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

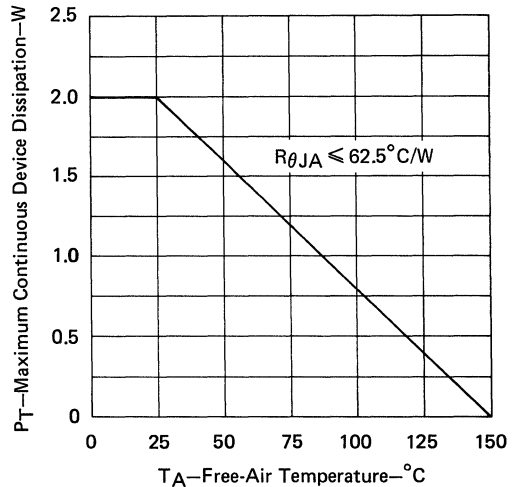


FIGURE 10

TYPES TIP125, TIP126, TIP127

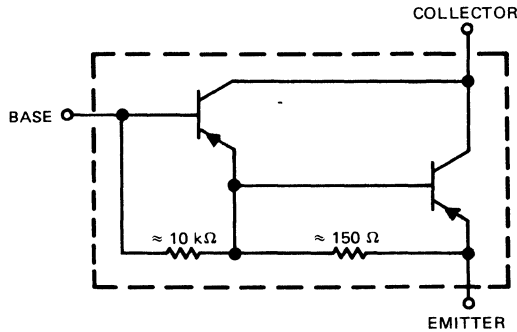
P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

DESIGNED FOR COMPLEMENTARY USE WITH TIP120, TIP121, TIP122

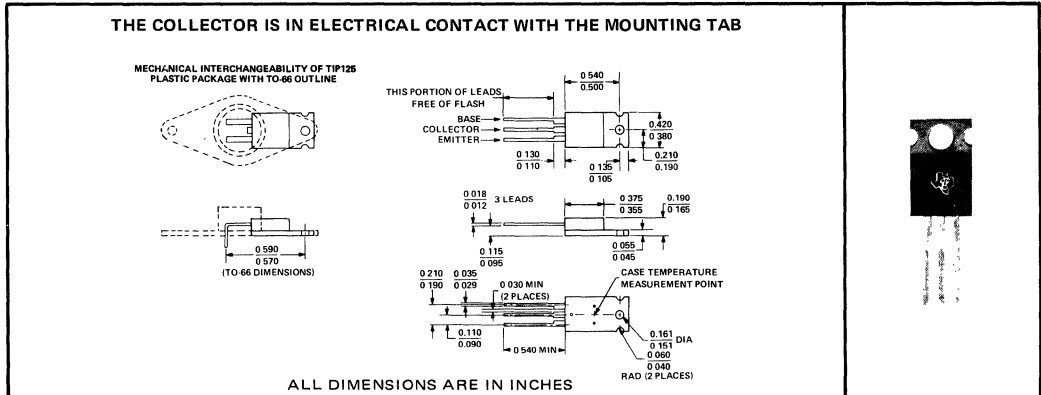
- 65 W at 25°C Case Temperature
- Min h_{FE} of 1000 at 3 V, 3 A
- 5 A Rated Collector Current
- 50 mJ Reverse Energy Rating

TYPES TIP125, TIP126, TIP127
BULLETIN NO. DL-S-7111611, DECEMBER 1971

device schematic



mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP125	TIP126	TIP127
Collector-Base Voltage	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-60 V	-80 V	-100 V
Emitter-Base Voltage	-5 V	-5 V	-5 V
Continuous Collector Current	← 5 A →		
Peak Collector Current (See Note 2)	← 8 A →		
Continuous Base Current	← 0.1 A →		
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 7 and 8 →		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 65 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →		
Unclamped Inductive Load Energy (See Note 5)	← 50 mJ →		
Operating Collector Junction Temperature Range	← -65°C to 150°C →		
Storage Temperature Range	← -65°C to 150°C →		
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_{W} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.52 W/°C or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L / 2$.

TYPES TIP125, TIP126, TIP127

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP125	TIP126	TIP127	UNIT
		MIN	MAX	MIN	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-60	-80	-100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.5			mA
	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-0.5		
	$V_{CE} = -50 \text{ V}$, $I_B = 0$			-0.5	
I_{CBO} Collector Cutoff Current	$V_{CB} = -60 \text{ V}$, $I_E = 0$	-0.2			mA
	$V_{CB} = -80 \text{ V}$, $I_E = 0$		-0.2		
	$V_{CB} = -100 \text{ V}$, $I_E = 0$			-0.2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-2	-2	-2	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -3 \text{ V}$, $I_C = -0.5 \text{ A}$	1000	1000	1000	
	$V_{CE} = -3 \text{ V}$, $I_C = -3 \text{ A}$	1000	1000	1000	
V_{BE} Base-Emitter Voltage	$V_{CE} = -3 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	-2.5	-2.5	-2.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -12 \text{ mA}$, $I_C = -3 \text{ A}$	-2	-2	-2	V
	$I_B = -20 \text{ mA}$, $I_C = -5 \text{ A}$	-4	-4	-4	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

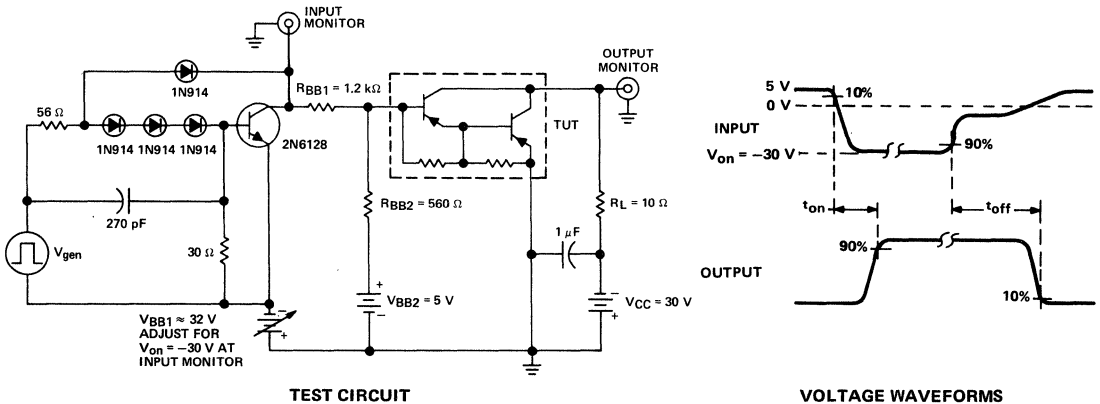
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -3 \text{ A}$, $I_{B(2)} = -12 \text{ mA}$, $I_{B(2)} = 12 \text{ mA}$,	1.5	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 5 \text{ V}$, $R_L = 10 \Omega$, See Figure 1	8.5	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

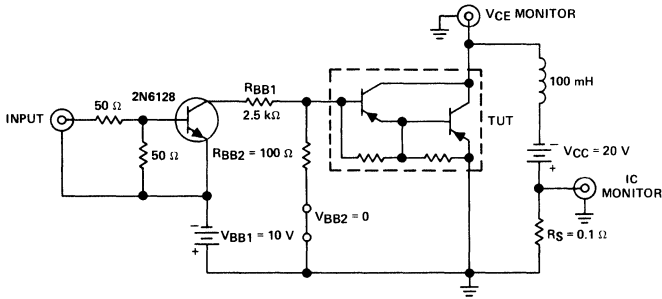


- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPES TIP125, TIP126, TIP127 P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

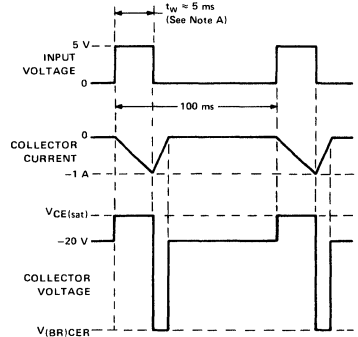
INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

NOTE A: Input pulse width is increased until $I_{CM} = -1$ A.

FIGURE 2



VOLTAGE AND CURRENT WAVEFORMS

TYPICAL CHARACTERISTICS

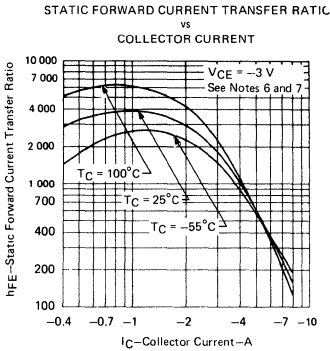


FIGURE 3

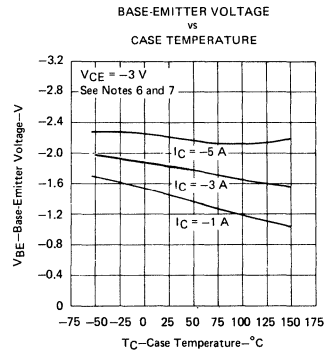


FIGURE 4

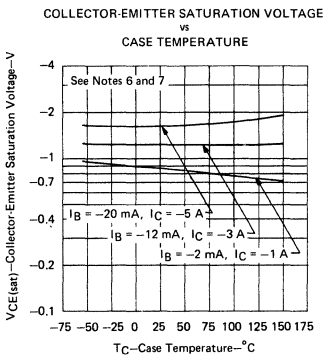


FIGURE 5

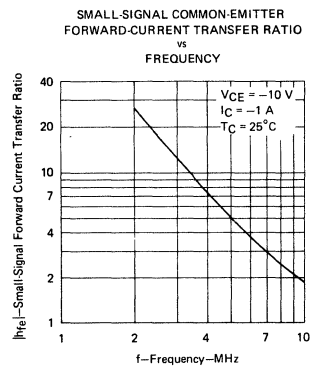


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

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TYPES TIP125, TIP126, TIP127

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

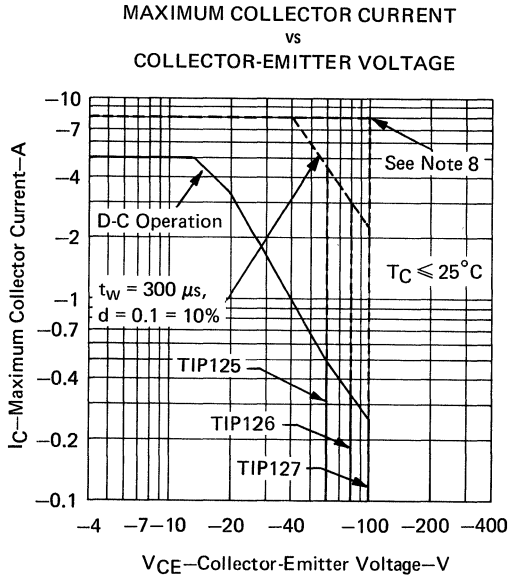


FIGURE 7

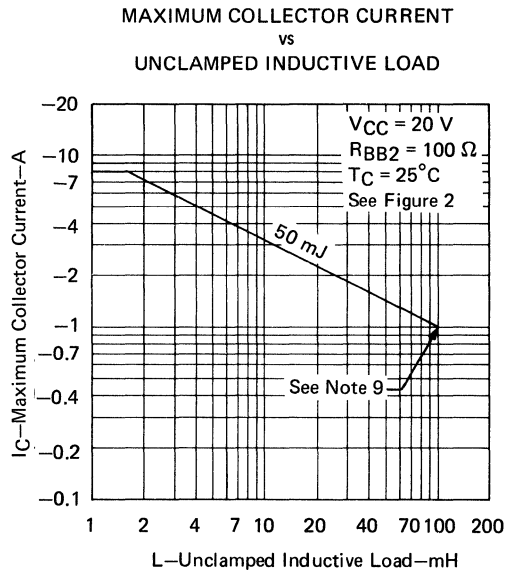


FIGURE 8

- NOTES: 8. These combinations of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.
9. Above this point the safe operating area has not been defined.

THERMAL INFORMATION

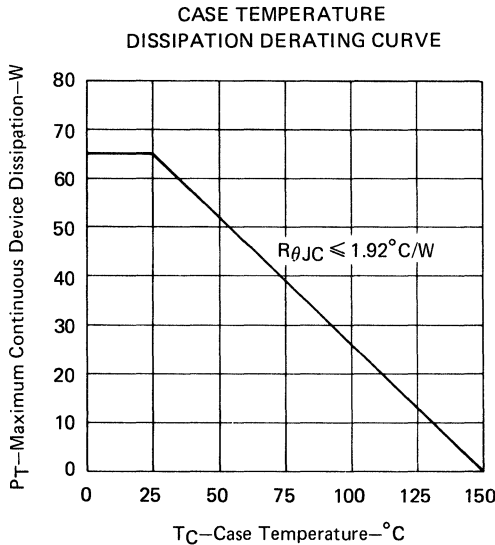


FIGURE 9

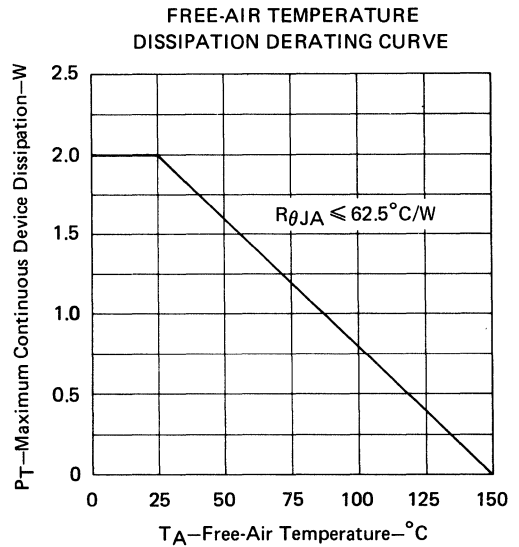


FIGURE 10

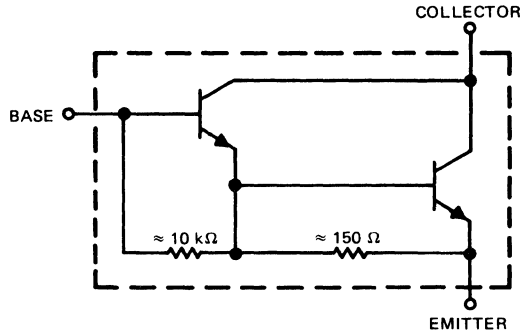
TYPES TIP140, TIP141, TIP142 N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

DESIGNED FOR COMPLEMENTARY USE WITH TIP145, TIP146, TIP147

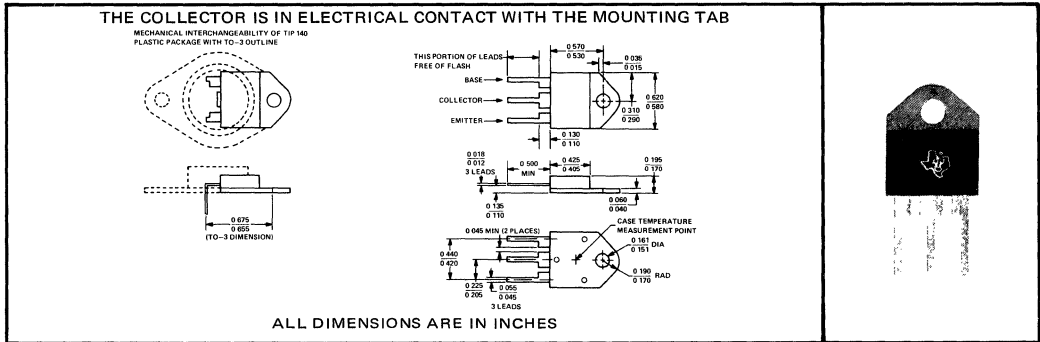
- 125 W at 25°C Case Temperature
- 10-A Rated Collector Current
- Min h_{FE} of 1000 at 4 V, 5 A
- 100-mJ Reverse Energy Rating

TYPES TIP140, TIP141, TIP142
BULLETIN NO. DL-57111639, DECEMBER 1971

device schematic



mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP140	TIP141	TIP142
Collector-Base Voltage	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	60 V	80 V	100 V
Emitter-Base Voltage	5 V	5 V	5 V
Continuous Collector Current	← 10 A →		
Peak Collector Current (See Note 2)	← 15 A →		
Continuous Base Current	← 0.5 A →		
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 7 and 8 →		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 125 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →		
Unclamped Inductive Load Energy (See Note 5)	← 100 mJ →		
Operating Collector Junction Temperature Range	← -65°C to 150°C →		
Storage Temperature Range	← -65°C to 150°C →		
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 1 W/°C or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP140, TIP141, TIP142

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP140	TIP141	TIP142	UNIT	
		MIN	MAX	MIN		MAX
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	60	80	100	V	
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	2			mA	
	$V_{CE} = 40 \text{ V}$, $I_B = 0$		2			
	$V_{CE} = 50 \text{ V}$, $I_B = 0$			2		
I_{CBO} Collector Cutoff Current	$V_{CB} = 60 \text{ V}$, $I_E = 0$	1			mA	
	$V_{CB} = 80 \text{ V}$, $I_E = 0$		1			
	$V_{CB} = 100 \text{ V}$, $I_E = 0$			1		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	2	2	2	mA	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$	See Notes 6 and 7	1000	1000	1000	
	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$		500	500	500	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 6 and 7	3	3	3	V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 10 \text{ mA}$, $I_C = 5 \text{ A}$	See Notes 6 and 7	2	2	2	V
	$I_B = 40 \text{ mA}$, $I_C = 10 \text{ A}$		3	3	3	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

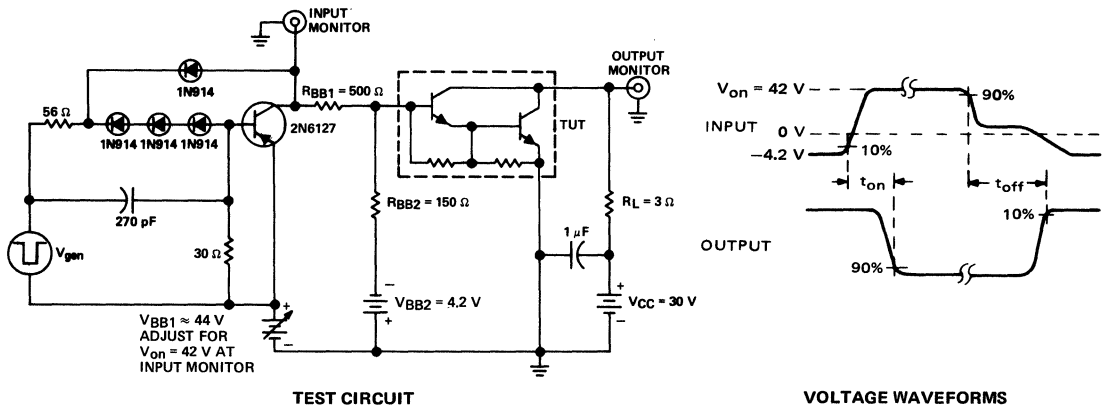
5

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 10 \text{ A}$, $I_B(1) = 40 \text{ mA}$, $I_B(2) = -40 \text{ mA}$, $V_{BE(off)} = -4.2 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	0.9	μs
t_{off} Turn-Off Time		11	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

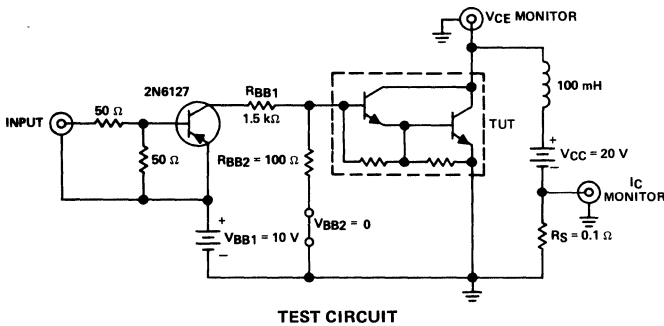


- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

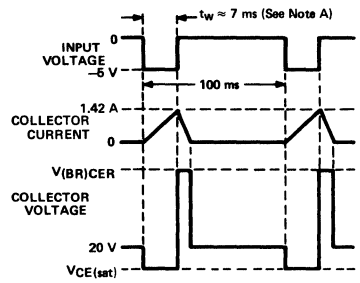
TYPES TIP140, TIP141, TIP142 N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

NOTE A: Input pulse width is increased until $I_{CM} = 1.42$ A.



VOLTAGE AND CURRENT WAVEFORMS

FIGURE 2

TYPICAL CHARACTERISTICS

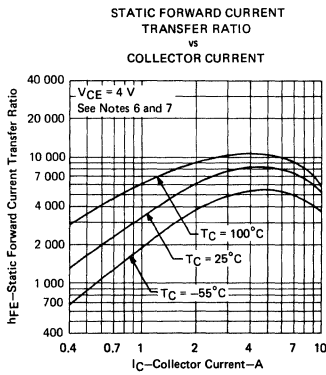


FIGURE 3

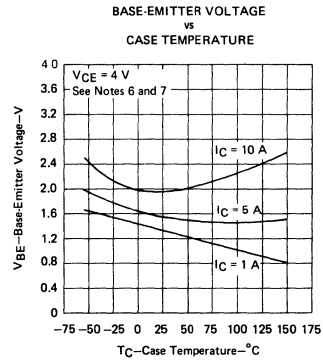


FIGURE 4

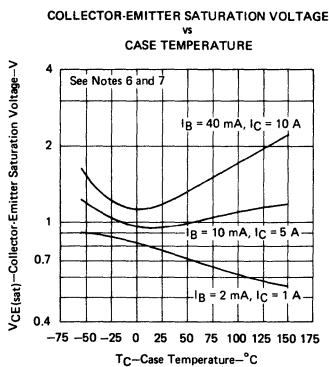


FIGURE 5

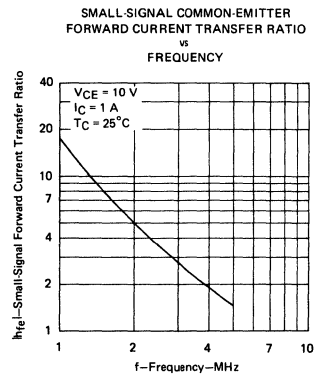


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP140, TIP141, TIP142

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

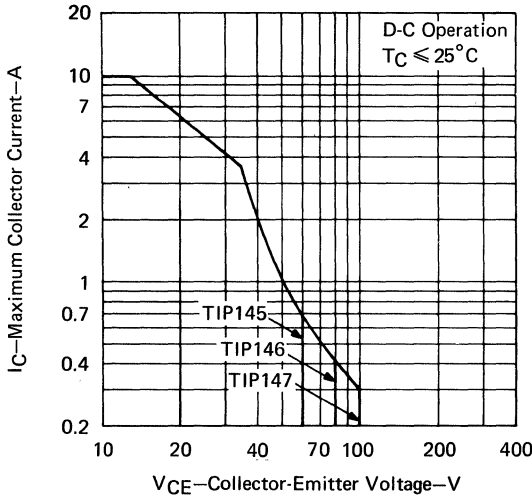


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

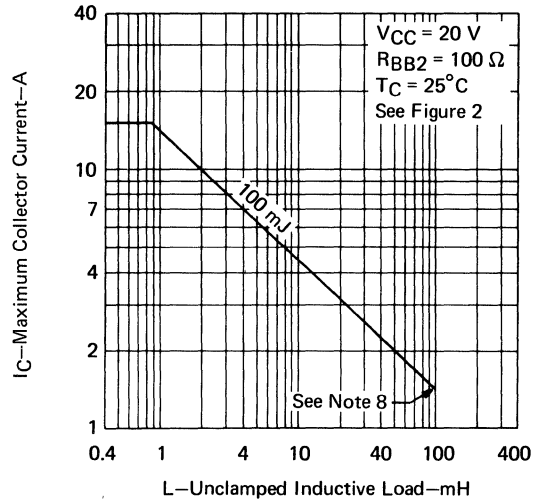


FIGURE 8

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

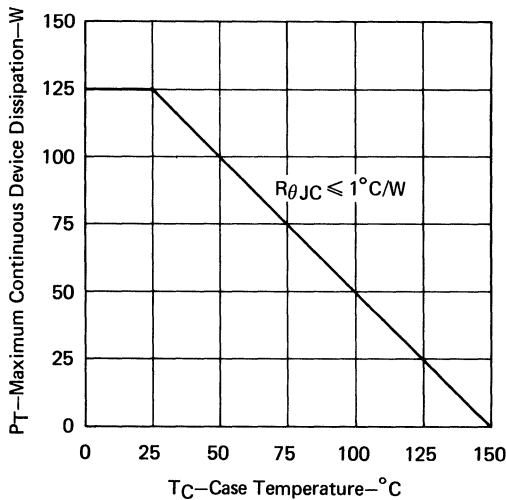


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

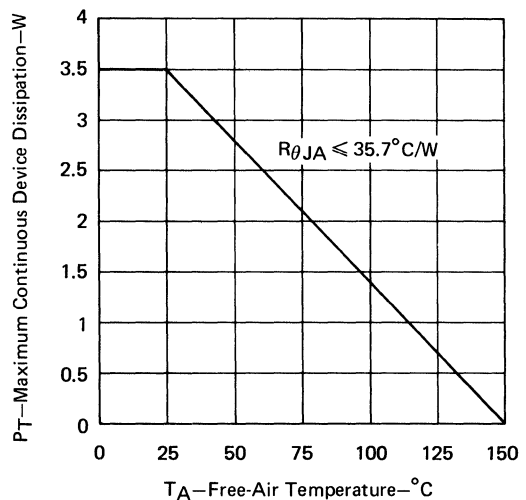


FIGURE 10

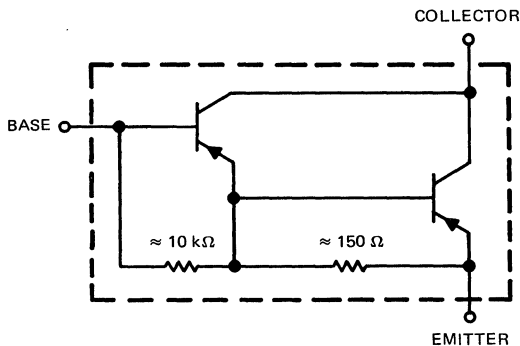
TYPES TIP145, TIP146, TIP147 P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

TYPES TIP145, TIP146, TIP147
BULLETIN NO. DL-S-711636, DECEMBER 1971

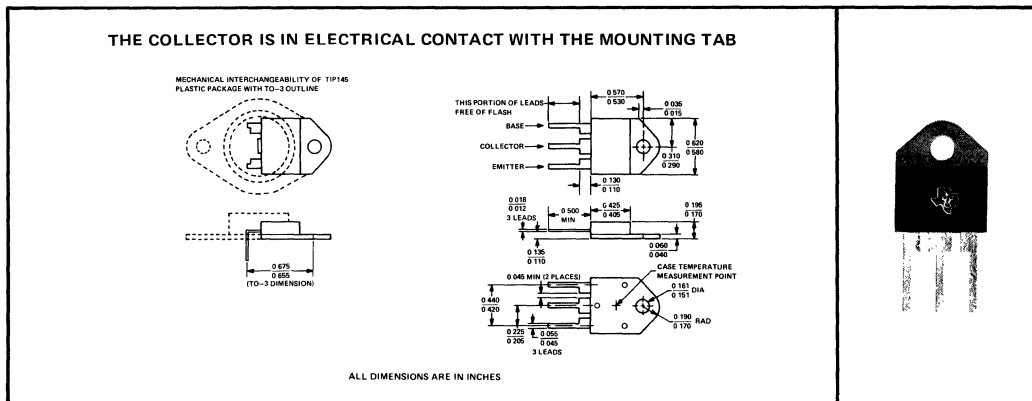
DESIGNED FOR COMPLEMENTARY USE WITH TIP140, TIP141, TIP142

- 125 W at 25°C Case Temperature
- 10-A Rated Collector Current
- Min h_{FE} of 1000 at 4 V, 5 A
- 100 mJ Reverse Energy Rating

device schematic



mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP145	TIP146	TIP147
Collector-Base Voltage	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-60 V	-80 V	-100 V
Emitter-Base Voltage	-5 V	-5 V	-5 V
Continuous Collector Current	← 10 A →	← 10 A →	← 10 A →
Peak Collector Current (See Note 2)	← 15 A →	← 15 A →	← 15 A →
Continuous Base Current	← 0.5 A →	← 0.5 A →	← 0.5 A →
Safe Operating Areas at (or below) 25°C Case Temperature	See Figures 7 and 8		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 125 W →	← 125 W →	← 125 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →	← 3.5 W →	← 3.5 W →
Unclamped Inductive Load Energy (See Note 5)	← 100 mJ →	← 100 mJ →	← 100 mJ →
Operating Collector Junction Temperature Range	← -65°C to 150°C →	← -65°C to 150°C →	← -65°C to 150°C →
Storage Temperature Range	← -65°C to 150°C →	← -65°C to 150°C →	← -65°C to 150°C →
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →	← 260°C →	← 260°C →

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_{W} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 1 W/°C or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L / 2$.

TYPES TIP145, TIP146, TIP147

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP145	TIP146	TIP147	UNIT	
		MIN	MAX	MIN		MAX
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-60	-80	-100	V	
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-2			mA	
	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-2			
	$V_{CE} = -50 \text{ V}$, $I_B = 0$			-2		
I_{CBO} Collector Cutoff Current	$V_{CB} = -60 \text{ V}$, $I_E = 0$	-1			mA	
	$V_{CB} = -80 \text{ V}$, $I_E = 0$		-1			
	$V_{CB} = -100 \text{ V}$, $I_E = 0$			-1		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-2	-2	-2	mA	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -5 \text{ A}$	See Notes 6 and 7	1000	1000	1000	
	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$		500	500	500	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$, See Notes 6 and 7	-3	-3	-3	V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -10 \text{ mA}$, $I_C = -5 \text{ A}$	See Notes 6 and 7	-2	-2	-2	V
	$I_B = -40 \text{ mA}$, $I_C = -10 \text{ A}$		-3	-3	-3	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

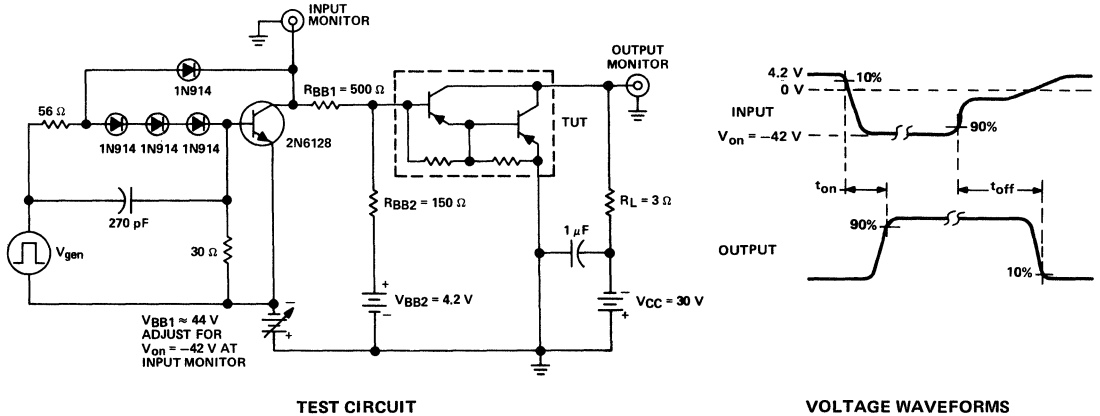
5

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -10 \text{ A}$, $I_{B(1)} = -40 \text{ mA}$, $I_{B(2)} = 40 \text{ mA}$,	0.9	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 4.2 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	11	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



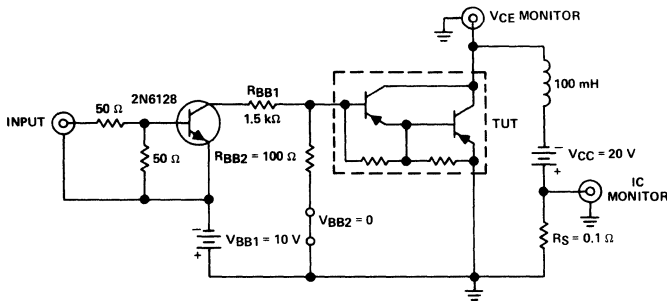
- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

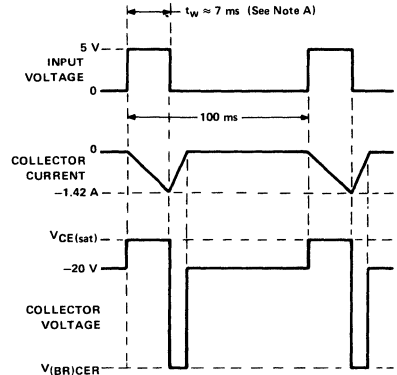
TYPES TIP145, TIP146, TIP147

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE A: Input pulse width is increased until $I_{CM} = -1.42$ A.

FIGURE 2

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

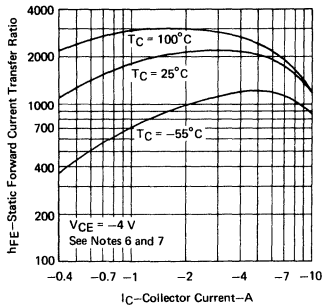


FIGURE 3

BASE-EMITTER VOLTAGE
vs
CASE TEMPERATURE

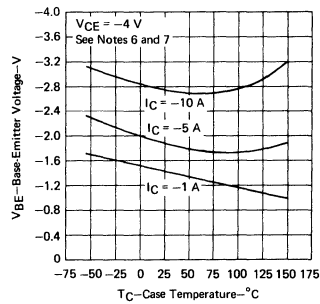


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE

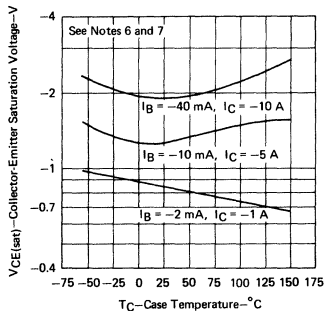


FIGURE 5

SMALL-SIGNAL COMMON-EMITTER
FORWARD CURRENT TRANSFER RATIO
vs
FREQUENCY

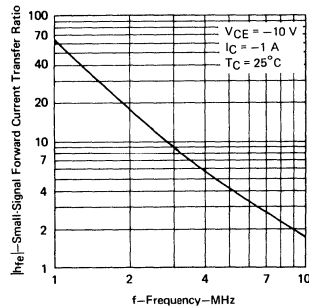


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP145, TIP146, TIP147 P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

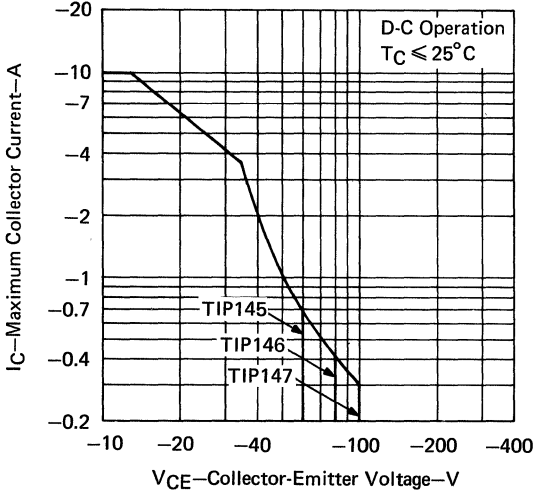


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

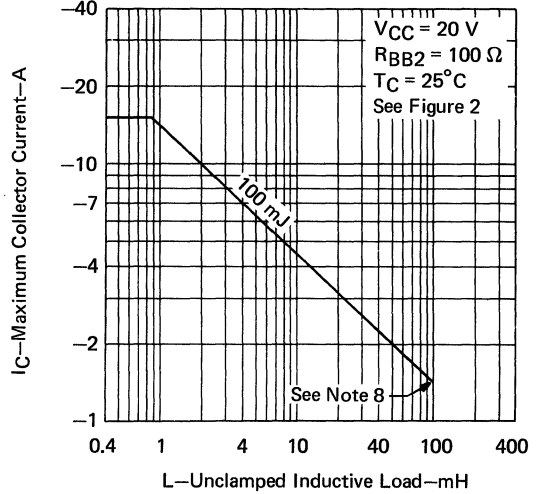


FIGURE 8

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

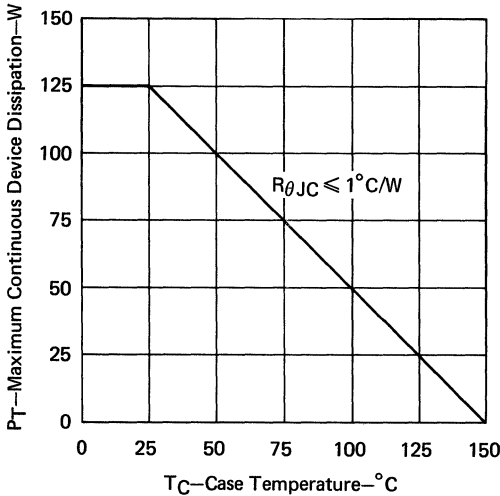


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

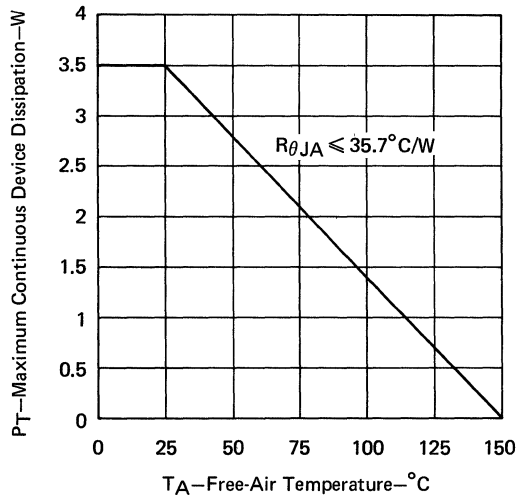


FIGURE 10

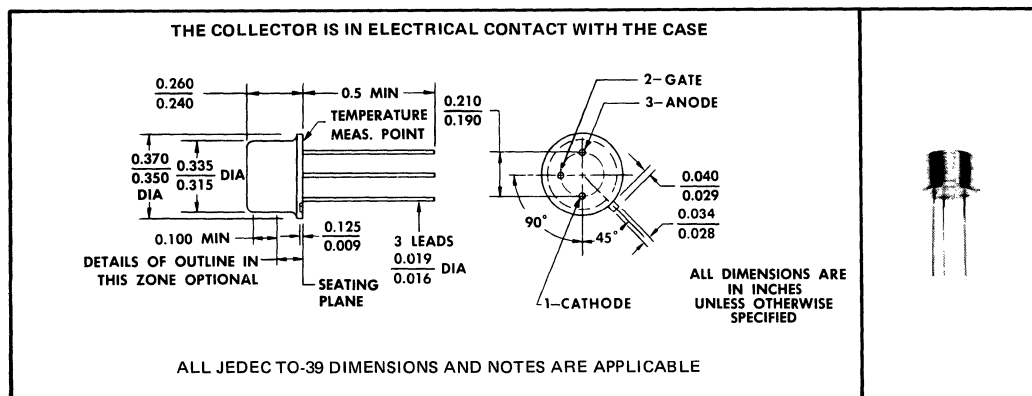
TYPES TIP501, TIP502 N-P-N SILICON POWER TRANSISTORS

TYPES TIP501, TIP502
BULLETIN NO. DL-57111607, DECEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH 2N3719, 2N3720

- Max t_{off} of 0.4 μs at $I_C = 1 A$
- 3-A Rated Continuous Collector Current
- 6 Watts at 25°C Case Temperature
- Min f_T of 60 MHz at 10 V, 0.5 A

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP501	TIP502
Collector-Base Voltage	40 V	60 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V
Emitter-Base Voltage	4 V	4 V
Continuous Collector Current	← 3 A →	
Peak Collector Current (See Note 2)	← 10 A →	
Continuous Base Current	← 0.5 A →	
Safe Operating Areas at (or below) 25°C Case Temperature	See Figures 3 and 4	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 6 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1 W →	
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.5$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 34.3 mW/°C or refer to Dissipation Derating Curve, Figure 5.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.71 mW/°C or refer to Dissipation Derating Curve, Figure 6.

TYPES TIP501, TIP502

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP501		TIP502		UNIT		
		MIN	MAX	MIN	MAX			
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 20 \text{ mA}$, $I_B = 0$, See Note 5	40		60		V		
I_{CEV} Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = -2 \text{ V}$		10			μA		
	$V_{CE} = 60 \text{ V}$, $V_{BE} = -2 \text{ V}$			10		μA		
	$V_{CE} = 40 \text{ V}$, $V_{BE} = -2 \text{ V}$, $T_C = 150^\circ\text{C}$		1			mA		
I_{CBO} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $V_{BE} = -2 \text{ V}$, $T_C = 150^\circ\text{C}$			1		mA		
	$V_{CB} = 40 \text{ V}$, $I_E = 0$		10			μA		
I_{EBO} Emitter Cutoff Current	$V_{CB} = 60 \text{ V}$, $I_E = 0$			10		μA		
	$V_{EB} = 4 \text{ V}$, $I_C = 0$		1	1		mA		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 1.5 \text{ V}$, $I_C = 0.5 \text{ A}$		20		20			
	$V_{CE} = 1.5 \text{ V}$, $I_C = 1 \text{ A}$	See Notes 5 and 6		25	180		25	180
	$V_{CE} = 1.5 \text{ V}$, $I_C = 1 \text{ A}$, $T_C = -40^\circ\text{C}$			15	15			
V_{BE} Base-Emitter Voltage	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C	See Notes 5 and 6		1.5	1.5	V		
	$I_B = 300 \text{ mA}$, $I_C = 3 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C			2.3	2.3			
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 100 \text{ mA}$, $I_C = 1 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C	See Notes 5 and 6		0.75	0.75	V		
	$I_B = 300 \text{ mA}$, $I_C = 3 \text{ A}$, $T_C = -40^\circ\text{C}$ to 100°C			1.5	1.5			
$ h_{fe} $ Small-Signal Common Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 30 \text{ MHz}$		2		2			
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 100 \text{ kHz}$ to 1 MHz		120		120	pF		
C_{ibo} Common-Base Open-Circuit Input Capacitance	$V_{EB} = 0.5 \text{ V}$, $I_C = 0$, $f = 100 \text{ kHz}$ to 1 MHz		1000		1000	pF		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

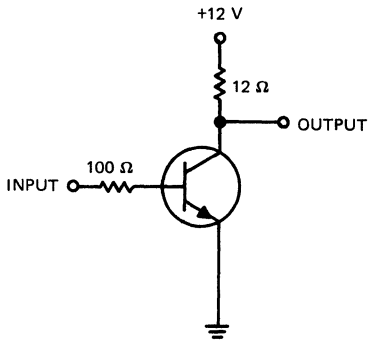
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	MAX	UNIT
t_{on} Turn-On Time	$I_C = 1 \text{ A}$, $R_L = 12 \Omega$, $I_{B(1)} = 0.1 \text{ A}$, See Figure 1, $V_{BE(off)} = -4 \text{ V}$,	0.1	μs
t_{off} Turn-Off Time	$I_C = 1 \text{ A}$, $R_L = 12 \Omega$, $I_{B(1)} = 0.1 \text{ A}$, See Figure 2, $I_{B(2)} = -0.1 \text{ A}$,	0.4	

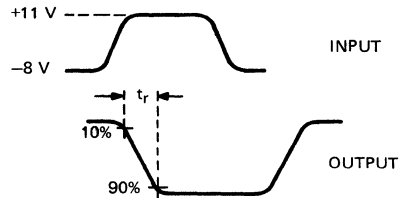
† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP501, TIP502 N-P-N SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



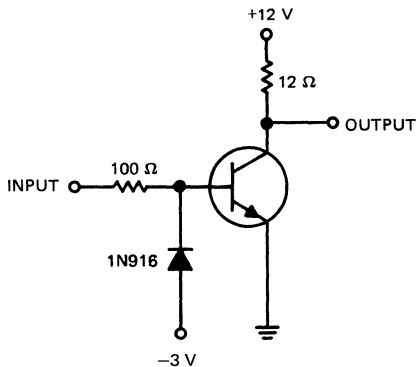
TEST CIRCUIT



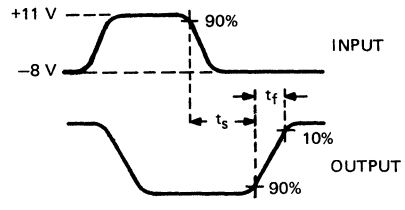
VOLTAGE WAVEFORMS

FIGURE 1—TURN-ON TIME

5



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2—TURN-OFF TIME

- NOTES: a. The input waveforms are supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_{out} = 50 \Omega$, $t_w = 10 \mu$ s, duty cycle $\leq 2\%$.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5$ ns, $R_{in} \geq 10$ k Ω , $C_{in} \leq 11.5$ pF.
- c. Resistors must be noninductive types.
- d. The d-c power supplies may require additional bypassing in order to minimize ringing.

TYPES TIP501, TIP502 N-P-N SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

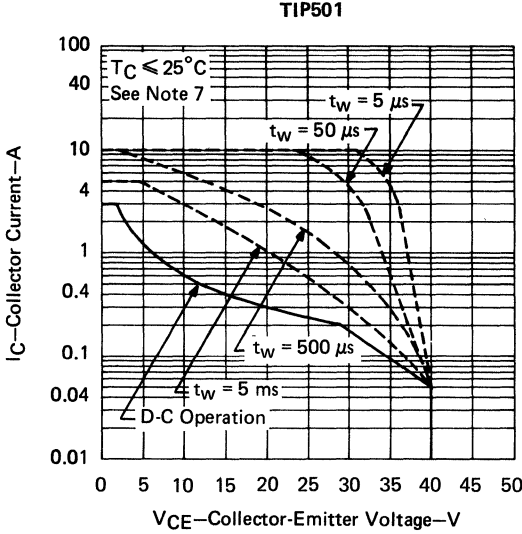


FIGURE 3

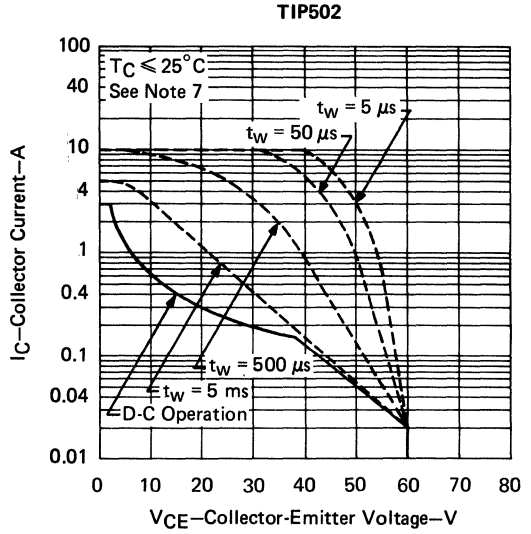


FIGURE 4

NOTE 7: Areas defined by dashed lines apply for nonrepetitive-pulse operation. The pulse may be repeated after the device has regained thermal equilibrium.

THERMAL INFORMATION

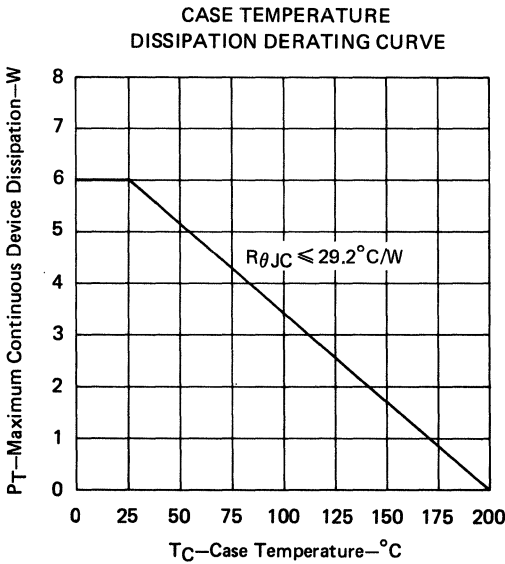


FIGURE 5

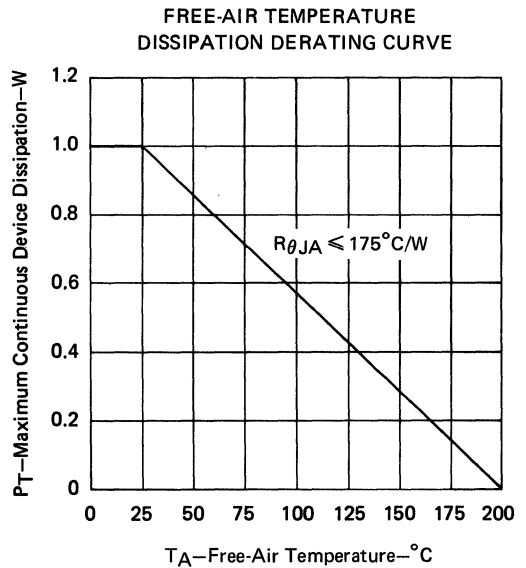


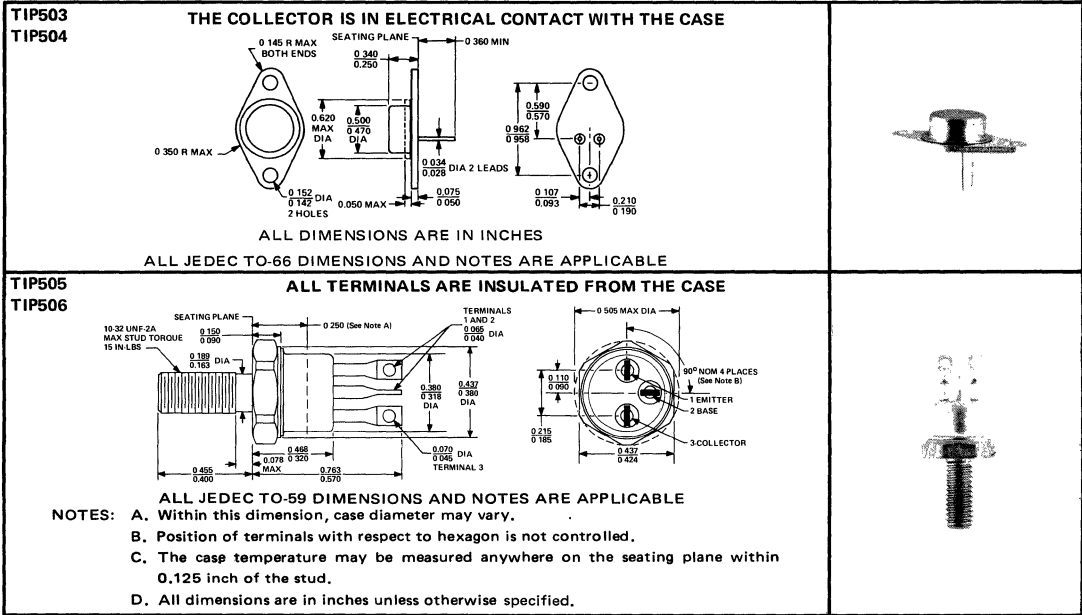
FIGURE 6

TYPES TIP503 THRU TIP506 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 120 V and 150 V Min $V(BR)_{CEO}$
- 2-A Rated Continuous Collector Current
- 20 Watts at 100°C Case Temperature
- Min f_T of 70 MHz at 5 V, 0.25 A

mechanical data



TYPES TIP503 THRU TIP506
BULLETIN NO. DL-57111598, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP503	TIP504	TIP505	TIP506
Collector-Base Voltage	130 V	160 V	120 V	150 V
Collector-Emitter Voltage (See Note 1)	120 V	150 V	6 V	6 V
Emitter-Base Voltage	6 V			
Continuous Collector Current	← 2 A →			
Peak Collector Current (See Note 2)	← 5 A →			
Continuous Base Current	← 1 A →			
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 20 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Operating Collector Junction Temperature Range	← -65°C to 200°C →			
Storage Temperature Range	← -65°C to 200°C →			
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →			

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_{WV} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.2 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C.

TYPES TIP503 THRU TIP506

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP503		TIP504		UNIT
		TIP505	TIP506	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	120	150			V
I_{CEO} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $I_B = 0$	50				μA
	$V_{CE} = 75 \text{ V}$, $I_B = 0$				50	
I_{CES} Collector Cutoff Current	$V_{CE} = 120 \text{ V}$, $V_{BE} = 0$	400				μA
	$V_{CE} = 150 \text{ V}$, $V_{BE} = 0$				400	
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	500				
	$V_{CE} = 75 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$				500	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 3 \text{ V}$, $I_C = 0$	20	20			μA
	$V_{EB} = 6 \text{ V}$, $I_C = 0$	200	200			
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 5 and 6	40	200	40	200	
	$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 5 and 6	20	20			
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 5 and 6	1.4	1.4			V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.1 \text{ A}$, $I_C = 1 \text{ A}$, See Notes 5 and 6	0.6	0.6			V
	$I_B = 0.2 \text{ A}$, $I_C = 2 \text{ A}$, See Notes 5 and 6	1.2	1.2			
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 250 \text{ mA}$, $f = 1 \text{ kHz}$	40	40			
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 250 \text{ mA}$, $f = 10 \text{ MHz}$	7	7			

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	5	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	87.5	

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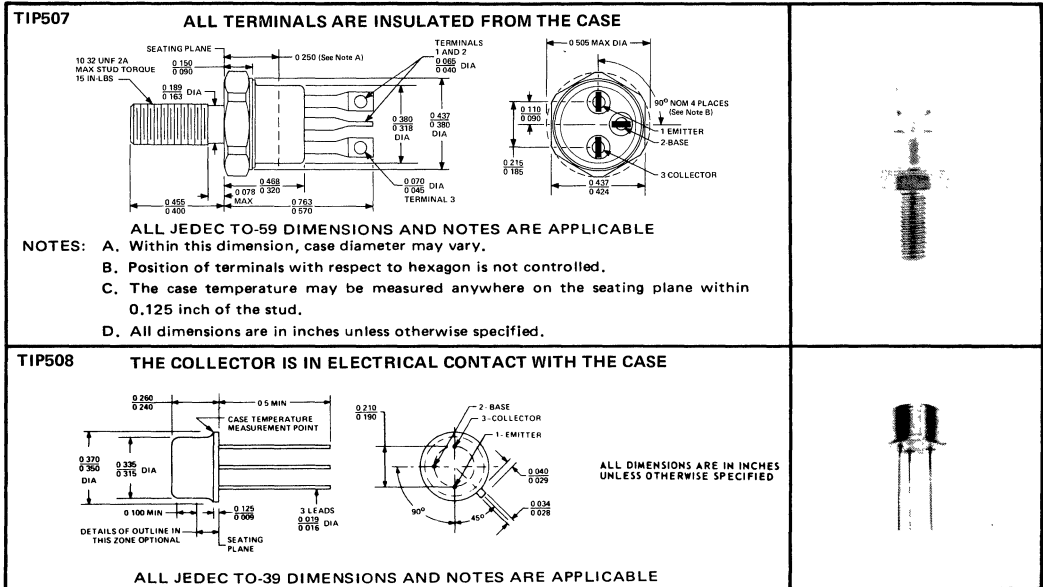
TYPES TIP507, TIP508 P-N-P SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 150 V Min $V(BR)_{CEO}$
- 2-A Rated Continuous Collector Current
- 20 Watts at 100°C Case Temperature (TIP507)
- 4 Watts at 100°C Case Temperature (TIP508)
- Min f_T of 50 MHz at 5 V, 0.2 A

TYPES TIP507, TIP508
BULLETIN NO. DL-S 711614, DECEMBER 1971

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP507	TIP508
Collector-Base Voltage	← -150 V →	← -150 V →
Collector-Emitter Voltage (See Note 1)	← -150 V →	← -150 V →
Emitter-Base Voltage	← -5 V →	← -5 V →
Continuous Collector Current	← -2 A →	← -2 A →
Peak Collector Current (See Note 2)	← -3 A →	← -3 A →
Continuous Base Current	← -0.6 A →	← -0.6 A →
Safe Operating Area at (or below) 100°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	20 W	4 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W	1 W
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_{tw} \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 200 mW/°C for TIP507 and 40 mW/°C for TIP508.
4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C for TIP507 and 5.7 mW/°C for TIP508.

TYPES TIP507, TIP508

P-N-P SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-150		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -75 \text{ V}$, $I_B = 0$		-200	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -150 \text{ V}$, $V_{BE} = 0$		-1	mA
	$V_{CE} = -75 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -2.5 \text{ V}$, $I_C = 0$		-100	μA
	$V_{EB} = -5 \text{ V}$, $I_C = 0$		-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 5 and 6	30	120	
	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 5 and 6	10		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 5 and 6		-1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.1 \text{ A}$, $I_C = -1 \text{ A}$, See Notes 5 and 6		-1	V
	$I_B = -0.4 \text{ A}$, $I_C = -2 \text{ A}$, See Notes 5 and 6		-1.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 1 \text{ kHz}$	30		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 5 \text{ MHz}$	10		

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

5

thermal characteristics

PARAMETER	TIP507	TIP508	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	5	25	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	87.5	175	

MAXIMUM SAFE OPERATING AREA

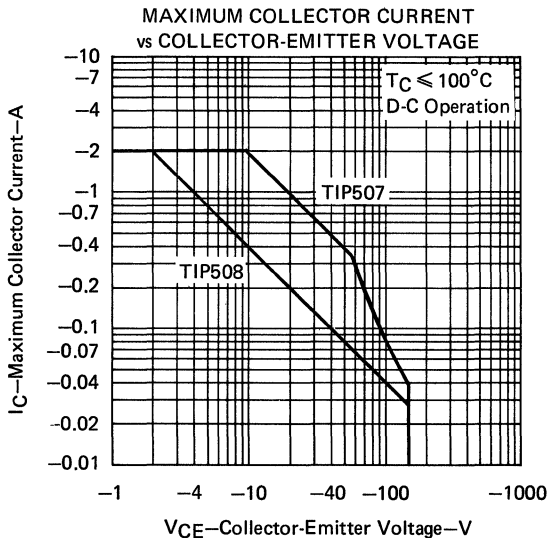


FIGURE 1

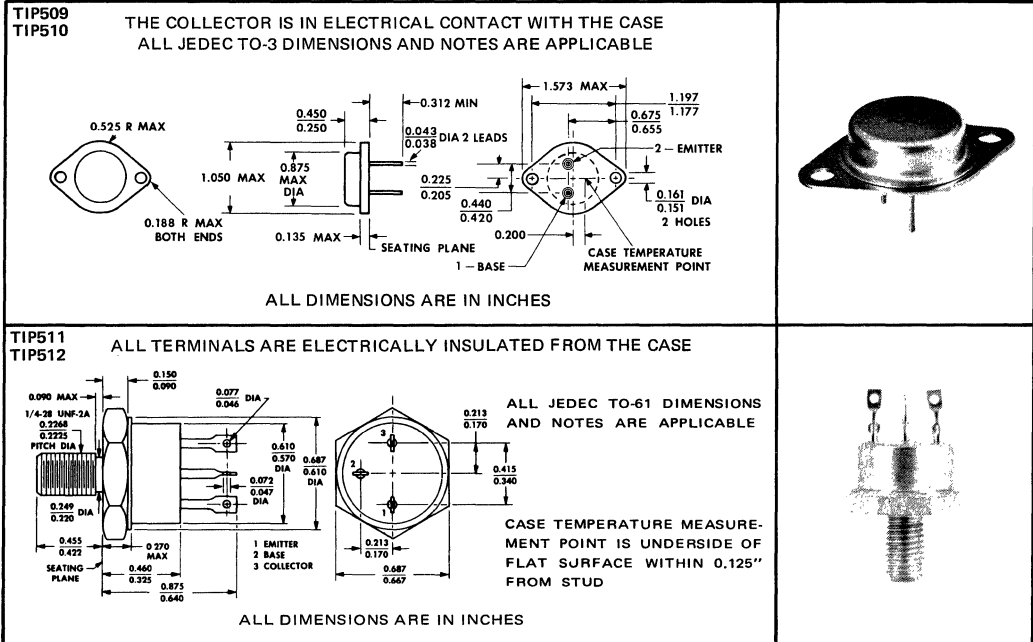
TYPES TIP509 THRU TIP512 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 120 V and 150 V Min $V_{(BR)CEO}$
- 4-A Rated Continuous Collector Current
- 30 Watts at 100°C Case Temperature
- Min f_T of 70 MHz at 5 V, 0.5 A

TYPES TIP509 THRU TIP512
BULLETIN NO. DLS-7111820, DECEMBER 1971

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP509	TIP510	TIP511	TIP512
Collector-Base Voltage	130 V	160 V	120 V	150 V
Collector-Emitter Voltage (See Note 1)	120 V	150 V	6 V	6 V
Emitter-Base Voltage	6 V	6 V	4 A	4 A
Continuous Collector Current	4 A	4 A	2 A	2 A
Peak Collector Current (See Note 2)	8 A	8 A	30 W	30 W
Continuous Base Current	2 A	2 A	4 W	4 W
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	30 W	30 W	-65°C to 200°C	-65°C to 200°C
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	4 W	4 W	-65°C to 200°C	-65°C to 200°C
Operating Collector Junction Temperature Range	-65°C to 200°C	-65°C to 200°C	300°C	300°C
Storage Temperature Range	-65°C to 200°C	-65°C to 200°C		
Terminal Temperature 1/16 Inch from Case for 10 Seconds	300°C	300°C		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.3 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.8 mW/°C.

TYPES TIP509 THRU TIP512

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP509	TIP510	UNIT		
		TIP511	TIP512			
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	120		150		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 60 \text{ V}$, $I_B = 0$ $V_{CE} = 75 \text{ V}$, $I_B = 0$		0.5		0.5	mA
I_{CES} Collector Cutoff Current	$V_{CE} = 120 \text{ V}$, $V_{BE} = 0$		1			mA
	$V_{CE} = 150 \text{ V}$, $V_{BE} = 0$				1	
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		1			
	$V_{CE} = 75 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$				1	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 3 \text{ V}$, $I_C = 0$		50		50	μA
	$V_{EB} = 6 \text{ V}$, $I_C = 0$		500		500	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 5 and 6	40	200	40	200	
	$V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, See Notes 5 and 6	25		25		
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, See Notes 5 and 6		1.4		1.4	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.2 \text{ A}$, $I_C = 2 \text{ A}$, See Notes 5 and 6		0.6		0.6	V
	$I_B = 0.4 \text{ A}$, $I_C = 4 \text{ A}$, See Notes 5 and 6		1.5		1.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	40		40		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 10 \text{ MHz}$	7		7		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3.33	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	43.75	

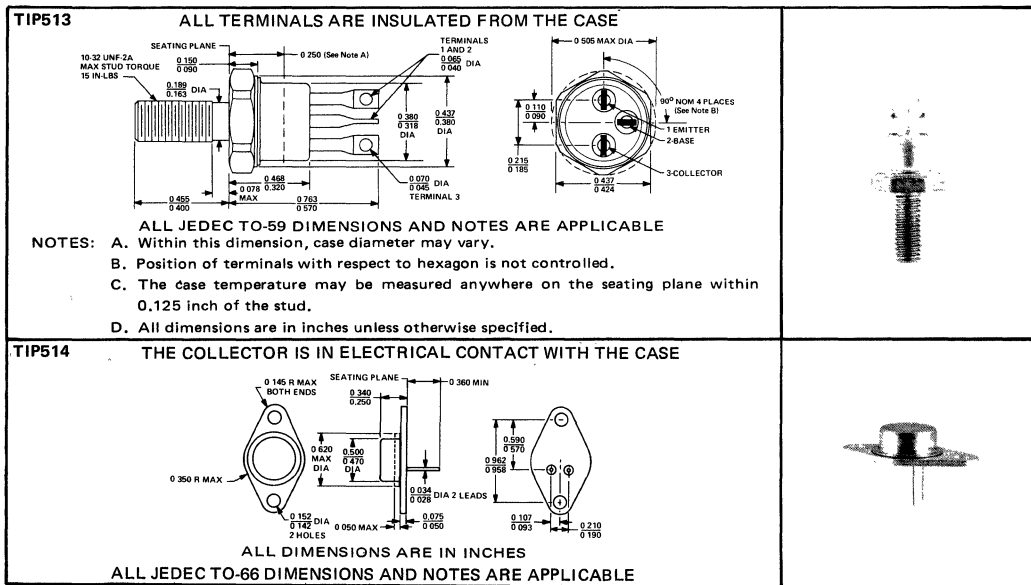
TYPES TIP513, TIP514 P-N-P SILICON POWER TRANSISTORS

TYPES TIP513, TIP514
BULLETIN NO. DL-S-7111615, DECEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 150 V Min $V_{(BR)CEO}$
- 5-A Rated Continuous Collector Current
- 30 Watts at 100°C Case Temperature (TIP513)
- 20 Watts at 100°C Case Temperature (TIP514)
- Min f_T of 40 MHz at 5 V, 0.5 A

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP513	TIP514
Collector-Base Voltage	← -150 V →	← -150 V →
Collector-Emitter Voltage (See Note 1)	← -150 V →	← -150 V →
Emitter-Base Voltage	← -5 V →	← -5 V →
Continuous Collector Current	← -5 A →	← -5 A →
Peak Collector Current (See Note 2)	← -7.5 A →	← -7.5 A →
Continuous Base Current	← -2 A →	← -2 A →
Safe Operating Area at (or below) 100°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	30 W	20 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W	2 W
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_{VV} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.3 W/°C for TIP513 and 0.2 W/°C for TIP514.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C.

TYPES TIP513, TIP514

P-N-P SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30$ mA, $I_B = 0$, See Note 5	-150		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -75$ V, $I_B = 0$		-300	μ A
I_{CES} Collector Cutoff Current	$V_{CE} = -150$ V, $V_{BE} = 0$		-1	mA
	$V_{CE} = -75$ V, $V_{BE} = 0$, $T_C = 150^\circ$ C		-2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -2.5$ V, $I_C = 0$		-100	μ A
	$V_{EB} = -5$ V, $I_C = 0$		-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4$ V, $I_C = -2.5$ A, See Notes 5 and 6	30	150	
	$V_{CE} = -4$ V, $I_C = -5$ A, See Notes 5 and 6	15		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4$ V, $I_C = -5$ A, See Notes 5 and 6		-2.2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.25$ A, $I_C = -2.5$ A, See Notes 5 and 6		-1	V
	$I_B = -0.5$ A, $I_C = -5$ A, See Notes 5 and 6		-2	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5$ V, $I_C = -0.5$ A, $f = 1$ kHz	30		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5$ V, $I_C = -0.5$ A, $f = 5$ MHz	8		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300$ μ s, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	TIP513	TIP514	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3.33	5	$^\circ$ C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	87.5	87.5	

MAXIMUM SAFE OPERATING AREA MAXIMUM COLLECTOR CURRENT vs COLLECTOR-EMITTER VOLTAGE

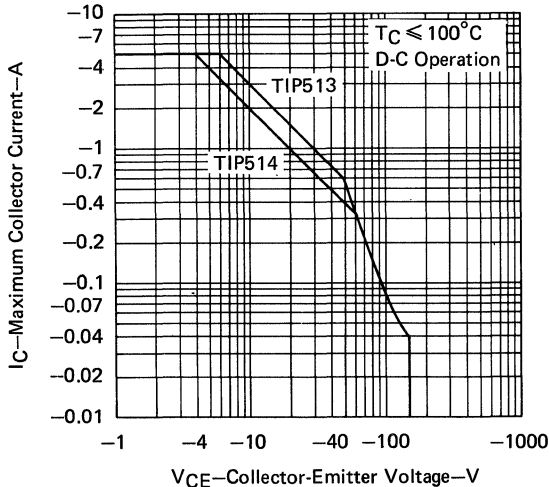


FIGURE 1

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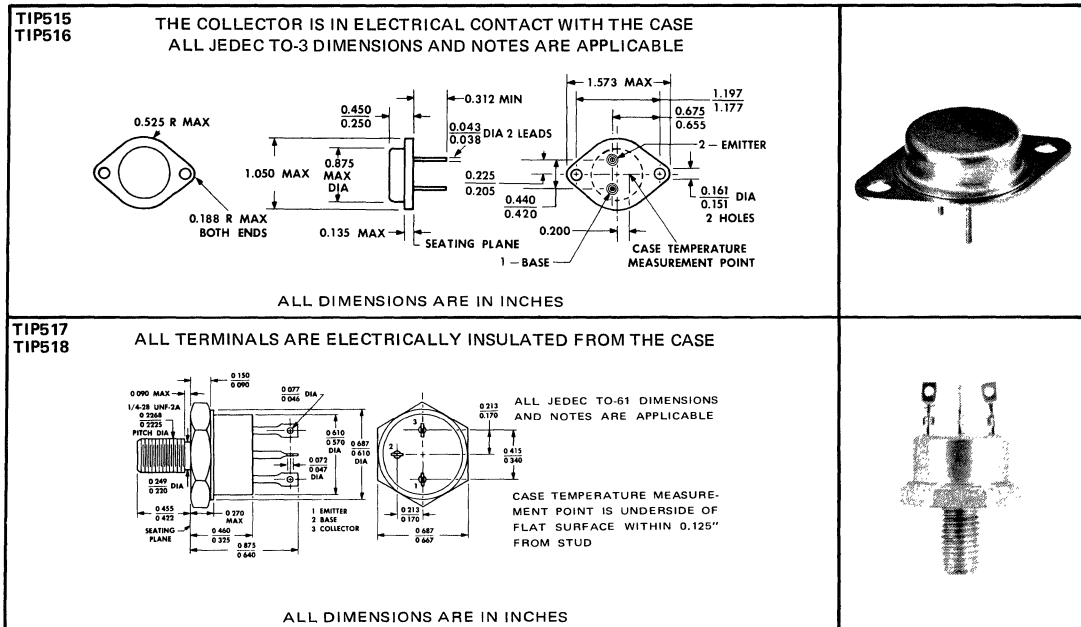
TYPES TIP515 THRU TIP518 N-P-N SILICON POWER TRANSISTORS

TYPES TIP515 THRU TIP518
BULLETIN NO. DL-S-7111603, DECEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 120 V and 150 V Min $V_{(BR)CEO}$
- 12-A Rated Continuous Collector Current
- 80 Watts at 100°C Case Temperature
- Min f_T of 70 MHz at 5 V, 1 A

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP515	TIP516	TIP517	TIP518
Collector-Base Voltage	130 V	160 V	130 V	160 V
Collector-Emitter Voltage (See Note 1)	120 V	150 V	120 V	150 V
Emitter-Base Voltage	6 V	6 V	6 V	6 V
Continuous Collector Current	← 12 A →			
Peak Collector Current (See Note 2)	← 25 A →			
Continuous Base Current	← 6 A →			
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	80 W	80 W	80 W	80 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	4 W	4 W	3.5 W	3.5 W
Operating Collector Junction Temperature Range	← -65°C to 200°C →			
Storage Temperature Range	← -65°C to 200°C →			
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →			

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.8 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.8 mW/°C for TIP515 and TIP516, 20 mW/°C for TIP517 and TIP518.

TYPES TIP515 THRU TIP518

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP515		TIP516		UNIT
		TIP517	TIP518	TIP517	TIP518	
		MIN	MAX	MIN	MAX	
V(BR)CEO Collector-Emitter Breakdown Voltage	I _C = 30 mA, I _B = 0, See Note 5	120		150		V
I _{CEO} Collector Cutoff Current	V _{CE} = 60 V, I _B = 0	1				mA
	V _{CE} = 75 V, I _B = 0			1		
I _{CES} Collector Cutoff Current	V _{CE} = 120 V, V _{BE} = 0	5				mA
	V _{CE} = 150 V, V _{BE} = 0			5		
	V _{CE} = 60 V, V _{BE} = 0, T _C = 150°C	5				
I _{EBO} Emitter Cutoff Current	V _{EB} = 3 V, I _C = 0	0.2		0.2		mA
	V _{EB} = 6 V, I _C = 0	2		2		
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 4 V, I _C = 6 A, See Notes 5 and 6	40	200	40	200	
	V _{CE} = 4 V, I _C = 12 A, See Notes 5 and 6	30		30		
V _{BE} Base-Emitter Voltage	V _{CE} = 4 V, I _C = 12 A, See Notes 5 and 6	1.4		1.4		V
V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = 0.6 A, I _C = 6 A, See Notes 5 and 6	0.8		0.8		V
	I _B = 1.2 A, I _C = 12 A, See Notes 5 and 6	1.5		1.5		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 5 V, I _C = 1 A, f = 1 kHz	40		40		
h _{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = 5 V, I _C = 1 A, f = 10 MHz	7		7		

NOTES: 5. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

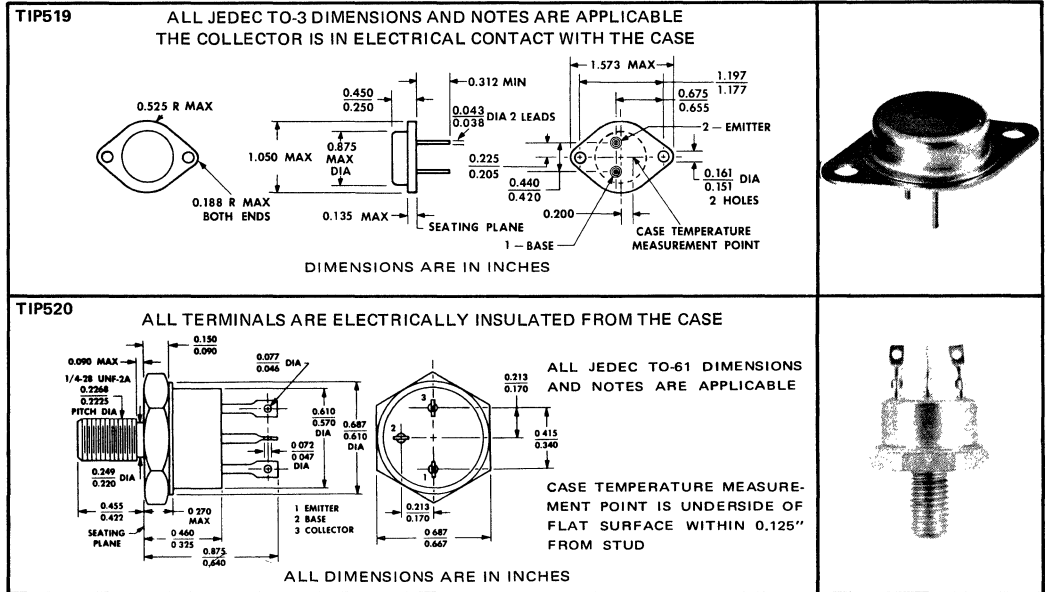
PARAMETER	TIP515	TIP517	UNIT
	TIP516	TIP518	
	MAX	MAX	
R _{θJC} Junction-to-Case Thermal Resistance	1.25	1.25	°C/W
R _{θJA} Junction-to-Free-Air Thermal Resistance	43.75	50	

TYPES TIP519, TIP520 P-N-P SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 150 V Min $V_{(BR)CEO}$
- 8-A Rated Continuous Collector Current
- 50 Watts at 100°C Case Temperature
- Min f_T of 40 MHz at 5 V, 1 A

mechanical data



TYPES TIP519, TIP520
BULLETIN NO. DL-S-711616, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP519	TIP520
Collector-Base Voltage	← 150 V →	← 150 V →
Collector-Emitter Voltage (See Note 1)	← 150 V →	← 150 V →
Emitter-Base Voltage	← 5 V →	← 5 V →
Continuous Collector Current	← 8 A →	← 8 A →
Peak Collector Current (See Note 2)	← 12 A →	← 12 A →
Continuous Base Current	← 3 A →	← 3 A →
Safe Operating Area at (or below) 100°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 50 W →	← 50 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	4 W	3.5 W
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.5 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.8 mW/°C for TIP519 and 20 mW/°C for TIP520.

TYPES TIP519, TIP520

P-N-P SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-150		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -75 \text{ V}$, $I_B = 0$		-500	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -150 \text{ V}$, $V_{BE} = 0$		-1	mA
	$V_{CE} = -75 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-3	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -2.5 \text{ V}$, $I_C = 0$		-100	μA
	$V_{EB} = -5 \text{ V}$, $I_C = 0$		-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -4 \text{ A}$, See Notes 5 and 6	30	150	
	$V_{CE} = -4 \text{ V}$, $I_C = -8 \text{ A}$, See Notes 5 and 6	10		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -8 \text{ A}$, See Notes 5 and 6		-2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.4 \text{ A}$, $I_C = -4 \text{ A}$, See Notes 5 and 6		-1	V
	$I_B = -1.6 \text{ A}$, $I_C = -8 \text{ A}$, See Notes 5 and 6		-2.2	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	30		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -1 \text{ A}$, $f = 5 \text{ MHz}$	8		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	TIP519	TIP520	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	2	2	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	43.8	50	

MAXIMUM SAFE OPERATING AREA

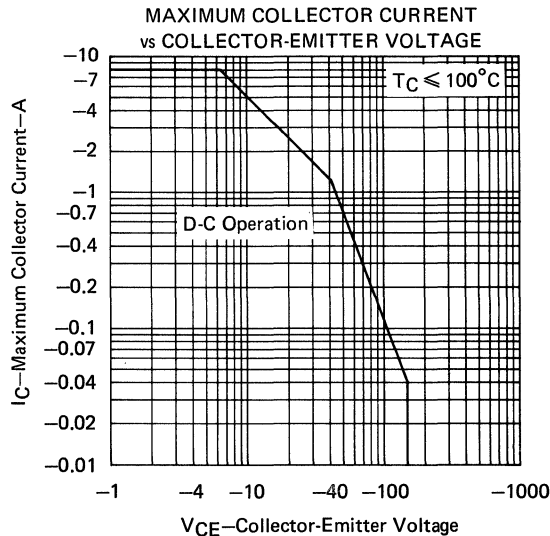


FIGURE 1

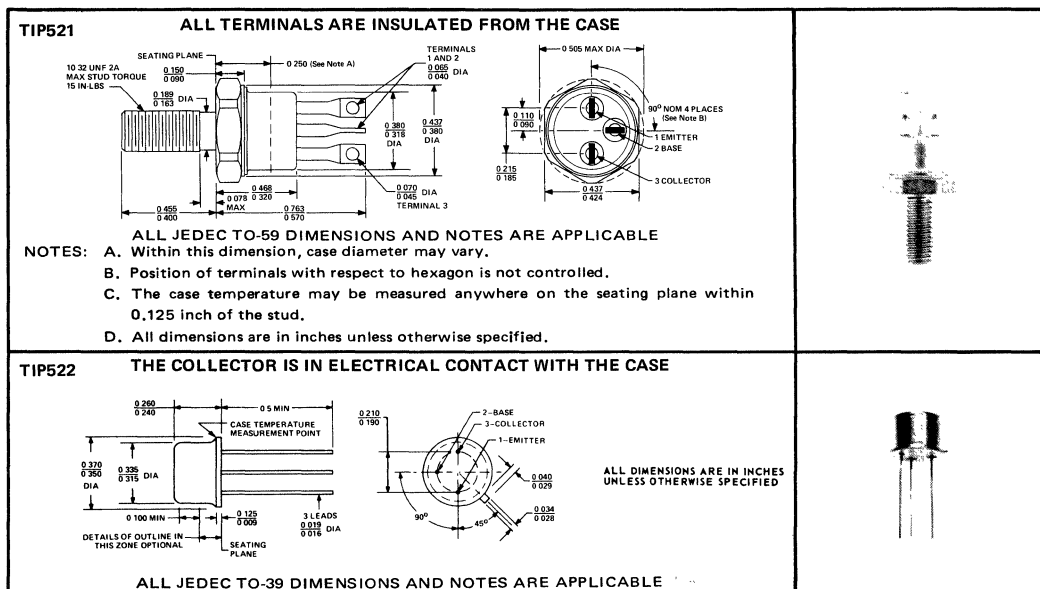
TYPES TIP521, TIP522 P-N-P SILICON POWER TRANSISTORS

TYPES TIP521, TIP522
BULLETIN NO. DL-S-7111617, DECEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 200 V Min $V_{(BR)CEO}$
- 2-A Rated Continuous Collector Current
- 20 Watts at 100°C Case Temperature (TIP521)
- 4 Watts at 100°C Case Temperature (TIP522)
- Min f_T of 50 MHz at 5 V, 0.2 A

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP521	TIP522
Collector-Base Voltage	← -200 V →	← -200 V →
Collector-Emitter Voltage (See Note 1)	← -200 V →	← -200 V →
Emitter-Base Voltage	← -5 V →	← -5 V →
Continuous Collector Current	← -2 A →	← -2 A →
Peak Collector Current (See Note 2)	← -3 A →	← -3 A →
Continuous Base Current	← -0.6 A →	← -0.6 A →
Safe Operating Area at (or below) 100°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	20 W	4 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W	1 W
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	← -300°C →	

- NOTES:** 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 200 mW/°C for TIP521 and 40 mW/°C for TIP522.
4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C for TIP521 and 5.7 mW/°C for TIP522.

TYPES TIP521, TIP522

P-N-P SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-200		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -100 \text{ V}$, $I_B = 0$		-200	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -200 \text{ V}$, $V_{BE} = 0$		-1	mA
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -2.5 \text{ V}$, $I_C = 0$		-100	μA
	$V_{EB} = -5 \text{ V}$, $I_C = 0$		-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 5 and 6	20	100	
	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 5 and 6	5		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -2 \text{ A}$, See Notes 5 and 6		-2.2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.1 \text{ A}$, $I_C = -1 \text{ A}$, See Notes 5 and 6		-1.5	V
	$I_B = -0.5 \text{ A}$, $I_C = -2 \text{ A}$, See Notes 5 and 6		-2.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 1 \text{ kHz}$	20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 5 \text{ MHz}$	10		

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	TIP521	TIP522	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	5	25	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	87.5	175	

MAXIMUM SAFE OPERATING AREA

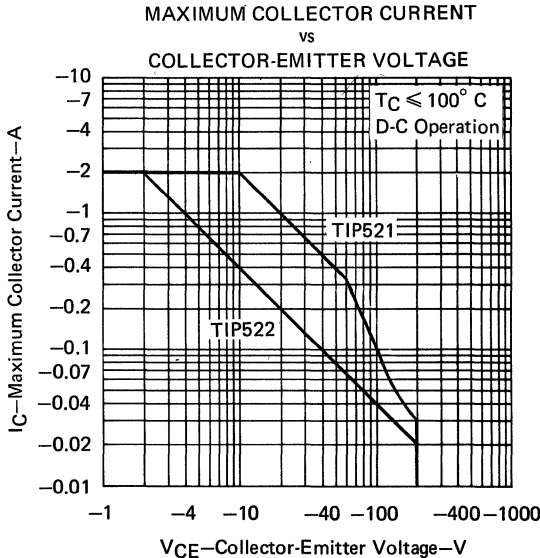


FIGURE 1

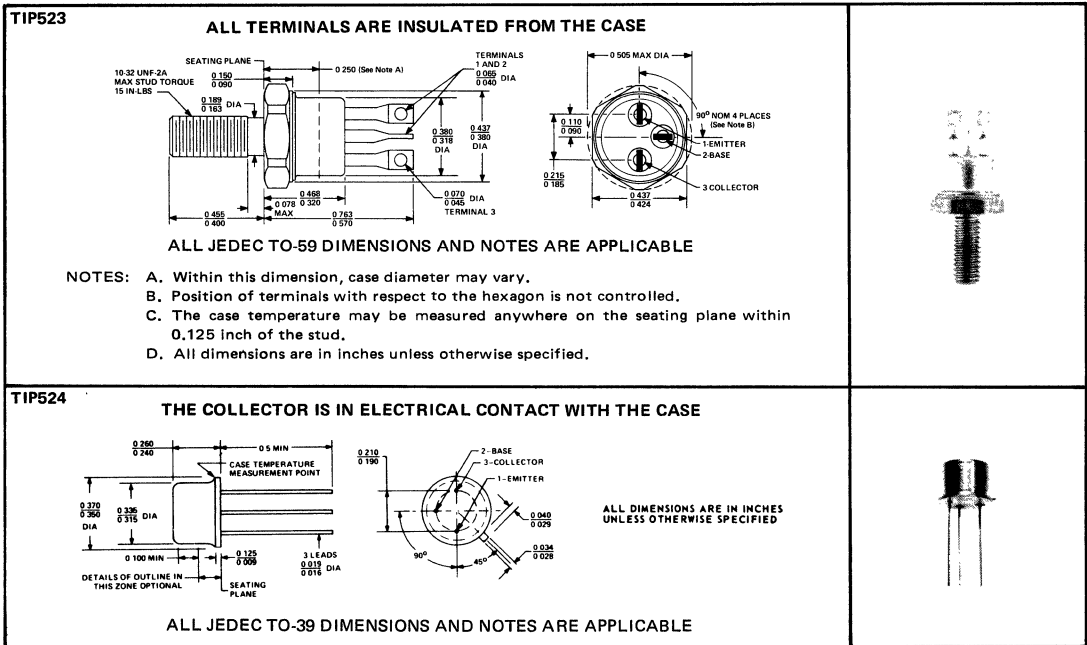
TYPES TIP523, TIP524 P-N-P SILICON POWER TRANSISTORS

TYPES TIP523, TIP524
BULLETIN NO. DL-S-7111618, DECEMBER 1971

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 200 V Min $V_{(BR)CEO}$
- 5-A Rated Continuous Collector Current
- 30 Watts at 100°C Case Temperature (TIP523)
- 6 Watts at 100°C Case Temperature (TIP524)
- Min f_T of 40 MHz at 5 V, 0.5 A

mechanical data



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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP523	TIP524
Collector-Base Voltage	← -200 V →	← -200 V →
Collector-Emitter Voltage (See Note 1)	← -200 V →	← -200 V →
Emitter-Base Voltage	← -5 V →	← -5 V →
Continuous Collector Current	← -5 A →	← -5 A →
Peak Collector Current (See Note 2)	← -7.5 A →	← -7.5 A →
Continuous Base Current	← -2 A →	← -2 A →
Safe Operating Area at (or below) 100°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	30 W	6 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W	1 W
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.3 mW/°C for TIP523 and 60 mW/°C for TIP524.
4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C for TIP523 and 5.7 mW/°C for TIP524.

TYPES TIP523, TIP524

P-N-P SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emmitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-200		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -100 \text{ V}$, $I_B = 0$		-300	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -200 \text{ V}$, $V_{BE} = 0$		-1	mA
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-2	
I_{EBO} Emmitter Cutoff Current	$V_{EB} = -2.5 \text{ V}$, $I_C = 0$		-100	μA
	$V_{EB} = -5 \text{ V}$, $I_C = 0$		-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -2.5 \text{ A}$, See Notes 5 and 6	20	100	
	$V_{CE} = -4 \text{ V}$, $I_C = -5 \text{ A}$, See Notes 5 and 6	5		
V_{BE} Base-Emmitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -5 \text{ A}$, See Notes 5 and 6		-2.2	V
$V_{CE(sat)}$ Collector-Emmitter Saturation Voltage	$I_B = -0.25 \text{ A}$, $I_C = -2.5 \text{ A}$, See Notes 5 and 6		-1.5	V
	$I_B = -1.25 \text{ A}$, $I_C = -5 \text{ A}$, See Notes 5 and 6		-2.5	
h_{fe} Small-Signal Common-Emmitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		
$ h_{fe} $ Small-Signal Common-Emmitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 5 \text{ MHz}$	8		

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

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thermal characteristics

PARAMETER	TIP523	TIP524	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3.33	16.7	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	87.5	175	

MAXIMUM SAFE OPERATING AREA

MAXIMUM COLLECTOR CURRENT
 vs
 COLLECTOR-EMITTER VOLTAGE

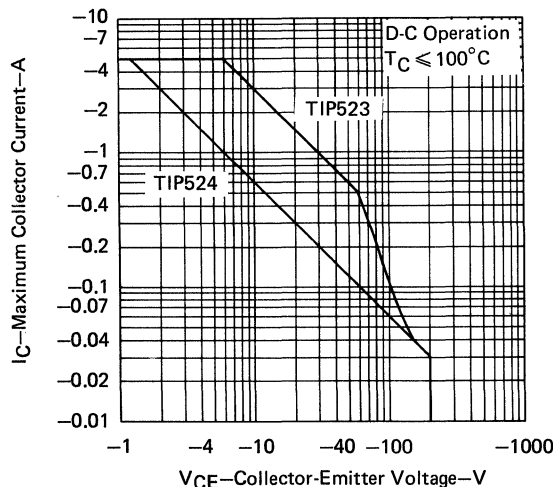


FIGURE 1

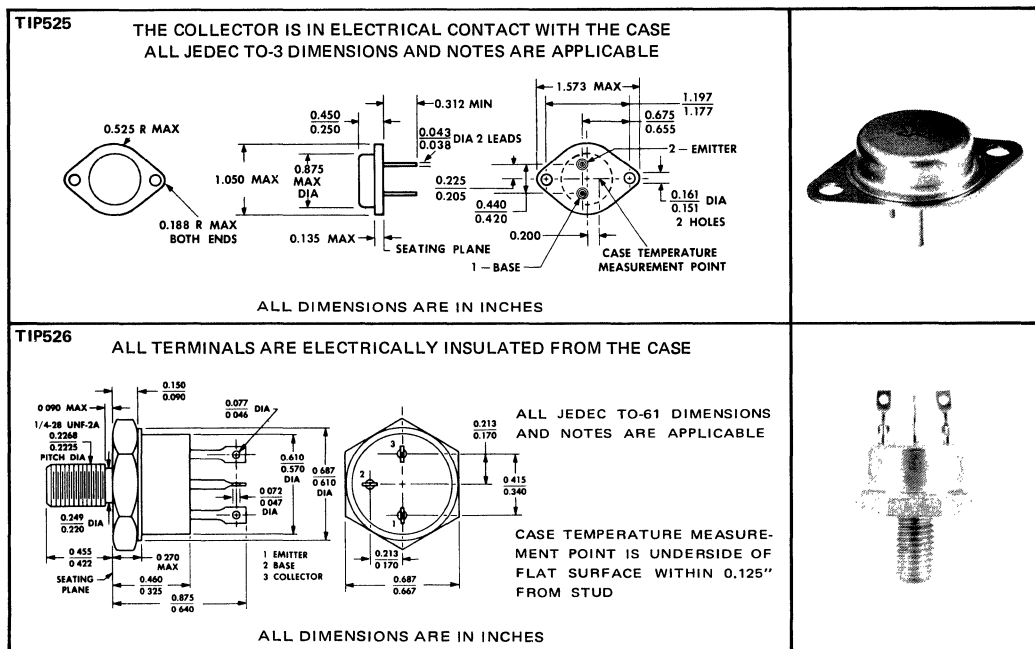
TYPES TIP525, TIP526 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 200 V Min $V_{(BR)CEO}$
- 5-A Rated Continuous Collector Current
- 60 Watts at 100°C Case Temperature
- Min f_T of 40 MHz at 5 V, 0.5 A

TYPES TIP525, TIP526
BULLETIN NO. DL-S-7111627, DECEMBER 1971

mechanical data



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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP525	TIP526
Collector-Base Voltage	← 250 V →	← 250 V →
Collector-Emitter Voltage (See Note 1)	← 200 V →	← 200 V →
Emitter-Base Voltage	← 6 V →	← 6 V →
Continuous Collector Current	← 5 A →	← 5 A →
Peak Collector Current (See Note 2)	← 10 A →	← 10 A →
Continuous Base Current	← 2 A →	← 2 A →
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 60 W →	← 60 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	4 W	3.5 W
Operating Collector Junction Temperature Range	← -65°C to 200°C →	← -65°C to 200°C →
Storage Temperature Range	← -65°C to 200°C →	← -65°C to 200°C →
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	← 300°C →

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.6 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.8 mW/°C for TIP525 and 20 mW/°C for TIP526.

TYPES TIP525, TIP526

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	200		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $I_B = 0$		500	μA
I_{CES} Collector Cutoff Current	$V_{CE} = 250 \text{ V}$, $V_{BE} = 0$		1	mA
	$V_{CE} = 125 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		2	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		100	μA
	$V_{EB} = 6 \text{ V}$, $I_C = 0$		1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6	30	150	
	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 5 and 6	20		
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 5 and 6		1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.25 \text{ A}$, $I_C = 2.5 \text{ A}$, See Notes 5 and 6		1.2	V
	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$, See Notes 5 and 6		2	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	30		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 5 \text{ MHz}$	8		

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- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	TIP525	TIP526	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.67	1.67	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	43.8	50	

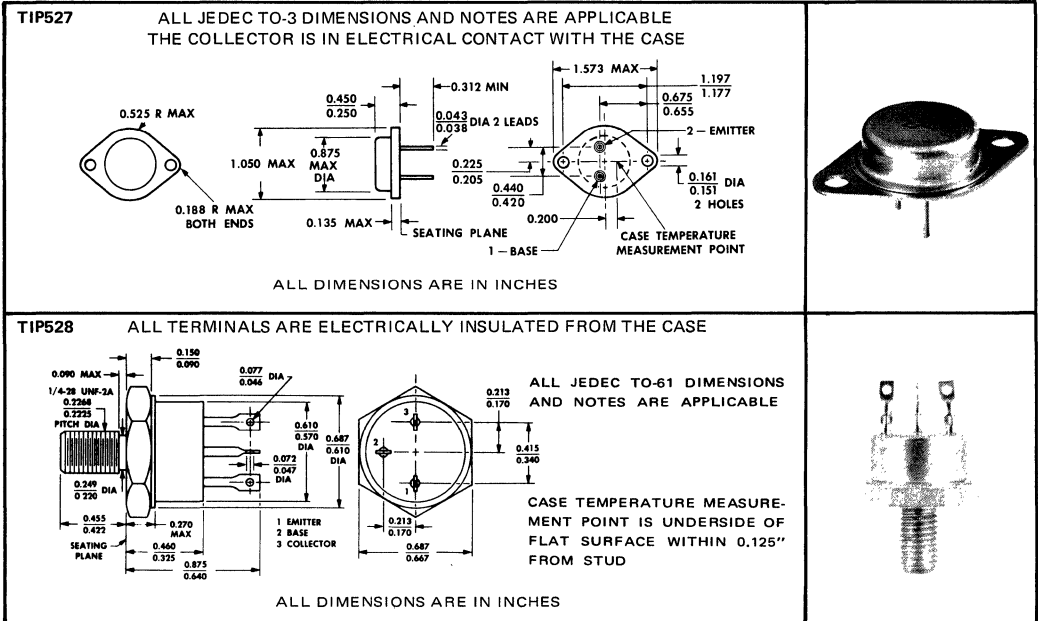
TYPES TIP527, TIP528 P-N-P SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 200 V Min $V(BR)_{CEO}$
- 8-A Rated Continuous Collector Current
- 60 Watts at 100°C Case Temperature
- Min f_T of 40 MHz at 5 V, 1 A

TYPES TIP527, TIP528
BULLETIN NO. DL-S-711619, DECEMBER 1971

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP527	TIP528
Collector-Base Voltage	← -200 V →	← -200 V →
Collector-Emitter Voltage (See Note 1)	← -200 V →	← -200 V →
Emitter-Base Voltage	← -5 V →	← -5 V →
Continuous Collector Current	← -8 A →	← -8 A →
Peak Collector Current (See Note 2)	← -12 A →	← -12 A →
Continuous Base Current	← -2 A →	← -2 A →
Safe Operating Area at (or below) 100°C Case Temperature	See Figure 1	
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 60 W →	← 60 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	4 W	3.5 W
Operating Collector Junction Temperature Range	← -65°C to 200°C →	
Storage Temperature Range	← -65°C to 200°C →	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

NOTES: 1. This value applies when the base-emitter diode is open-circuited.

2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.

3. Derate linearly to 200°C case temperature at the rate of 0.6 W/°C.

4. Derate linearly to 200°C free-air temperature at the rate of 22.8 mW/°C for TIP527 and 20 mW/°C for TIP528.

TYPES TIP527, TIP528

P-N-P SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-200		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -100 \text{ V}$, $I_B = 0$		-500	μA
I_{CES} Collector Cutoff Current	$V_{CE} = -200 \text{ V}$, $V_{BE} = 0$		-1	mA
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		-3	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -2.5 \text{ V}$, $I_C = 0$		-100	μA
	$V_{EB} = -5 \text{ V}$, $I_C = 0$		-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -4 \text{ A}$, See Notes 5 and 6	20	100	
	$V_{CE} = -4 \text{ V}$, $I_C = -8 \text{ A}$, See Notes 5 and 6	5		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -8 \text{ A}$, See Notes 5 and 6		-2.2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.4 \text{ A}$, $I_C = -4 \text{ A}$, See Notes 5 and 6		-1.5	V
	$I_B = -2 \text{ A}$, $I_C = -8 \text{ A}$, See Notes 5 and 6		-2.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$	20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -5 \text{ V}$, $I_C = -1 \text{ A}$, $f = 5 \text{ MHz}$	8		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

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thermal characteristics

PARAMETER	TIP527	TIP528	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.67	1.67	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	43.8	50	

MAXIMUM SAFE OPERATING AREA

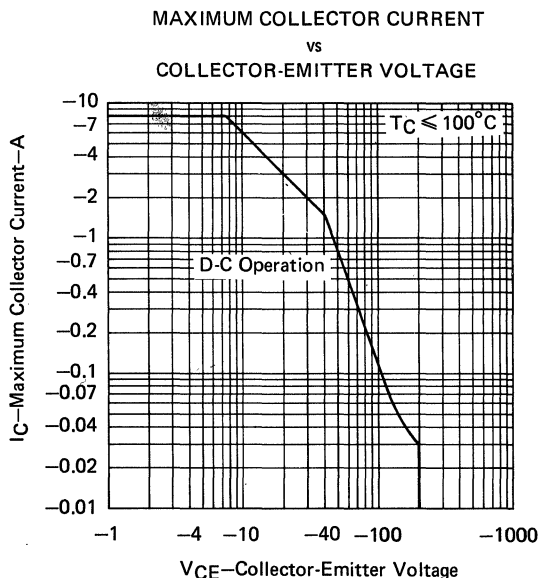


FIGURE 1

TYPES TIP529, TIP530 N-P-N SILICON POWER TRANSISTORS

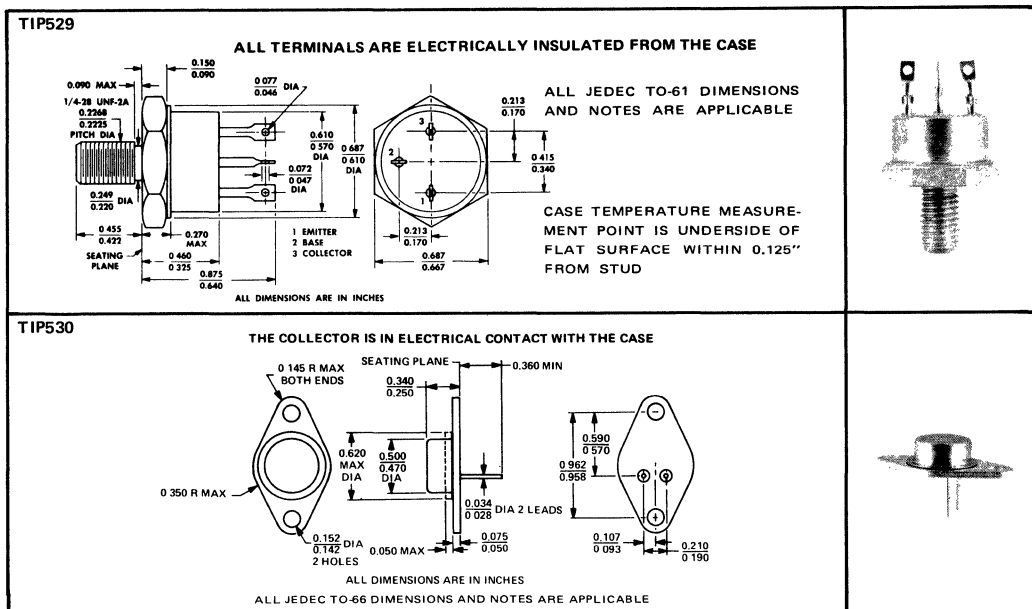
FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 300 V Min $V_{(BR)CEO}$
- 3-A Rated Continuous Collector Current
- 67 Watts at 100°C Case Temperature (TIP529)
- 20 Watts at 100°C Case Temperature (TIP530)
- Min f_T of 20 MHz at 5 V, 0.5 A

mechanical data

TYPES TIP529, TIP530
BULLETIN NO. DL-S-7111602, DECEMBER 1971

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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP529	TIP530
Collector-Base Voltage	← 400 V →	← 400 V →
Collector-Emitter Voltage (See Note 1)	← 300 V →	← 300 V →
Emitter-Base Voltage	← 6 V →	← 6 V →
Continuous Collector Current	← 3 A →	← 3 A →
Peak Collector Current (See Note 2)	← 10 A →	← 10 A →
Continuous Base Current	← 1.5 A →	← 1.5 A →
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	67 W	20 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	4 W	2 W
Operating Collector Junction Temperature Range	-65°C to 200°C	
Storage Temperature Range	-65°C to 200°C	
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.67 W/°C for TIP529 and 0.2 W/°C for TIP530.
 4. Derate linearly to 200°C free-air temperature at the rate of 22.8 mW/°C for TIP529 and 11.4 mW/°C for TIP530.

TYPES TIP529, TIP530

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	300		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 150 \text{ V}$, $I_B = 0$		100	μA
I_{CES}	Collector Cutoff Current	$V_{CE} = 400 \text{ V}$, $V_{BE} = 0$		100	μA
		$V_{CE} = 200 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		1	mA
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		100	μA
		$V_{EB} = 6 \text{ V}$, $I_C = 0$		1	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1.5 \text{ A}$, See Notes 5 and 6	25	125	
		$V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 5 and 6	8		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, See Notes 5 and 6		1.7	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.15 \text{ A}$, $I_C = 1.5 \text{ A}$, See Notes 5 and 6		1	V
		$I_B = 0.6 \text{ A}$, $I_C = 3 \text{ A}$, See Notes 5 and 6		2.5	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	25		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 5 \text{ MHz}$	4		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	TIP529	TIP530	UNIT
	MAX	MAX	
$R_{\theta JC}$	1.5	5	$^\circ\text{C/W}$
$R_{\theta JA}$	43.75	87.5	

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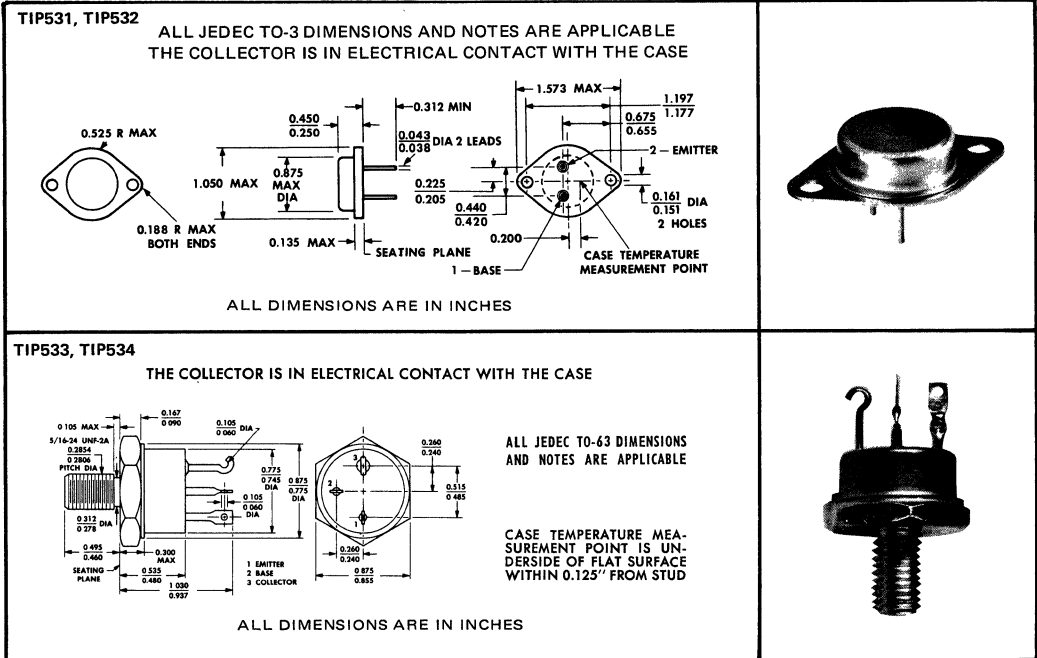
TYPES TIP531 THRU TIP534 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 300 V and 400 V Min $V(BR)_{CEO}$
- 15-A Rated Continuous Collector Current
- 150 Watts at 100°C Case Temperature
- Min f_T of 50 MHz at 10 V, 1 A

TYPES TIP531 THRU TIP534
BULLETIN NO. DL-S-7111648, DECEMBER 1971

mechanical data



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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP531	TIP532
Collector-Base Voltage	340 V	450 V
Collector-Emitter Voltage (See Note 1)	300 V	400 V
Emitter-Base Voltage	6 V	6 V
Continuous Collector Current	← 15 A →	← 15 A →
Peak Collector Current (See Note 2)	← 25 A →	← 25 A →
Continuous Base Current	← 4 A →	← 4 A →
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 150 W →	← 150 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 4 W →	← 4 W →
Operating Collector Junction Temperature Range	← -65°C to 175°C →	← -65°C to 175°C →
Storage Temperature Range	← -65°C to 200°C →	← -65°C to 200°C →
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →	← 300°C →

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_{W} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 175°C case temperature at the rate of 2 W/°C.
 4. Derate linearly to 175°C free-air temperature at the rate of 26.7 mW/°C.

TYPES TIP531 THRU TIP534

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP531		TIP532		UNIT
		TIP533		TIP534		
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 100 \text{ mA}$, $I_B = 0$, See Note 5	300		400		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 150 \text{ V}$, $I_B = 0$	2				mA
	$V_{CE} = 200 \text{ V}$, $I_B = 0$			2		
I_{CES} Collector Cutoff Current	$V_{CE} = 300 \text{ V}$, $V_{BE} = 0$	1				mA
	$V_{CE} = 400 \text{ V}$, $V_{BE} = 0$			1		
	$V_{CE} = 150 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	6				
	$V_{CE} = 200 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$			6		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 4 \text{ V}$, $I_C = 0$	0.5		0.5		mA
	$V_{EB} = 6 \text{ V}$, $I_C = 0$	10		10		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 7.5 \text{ A}$, See Notes 5 and 6	20	120	20	120	
	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	5		5		
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	1.5		1.5		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.75 \text{ A}$, $I_C = 7.5 \text{ A}$, See Notes 5 and 6	1.5		1.5		V
	$I_B = 4 \text{ A}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	2		2		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 5 \text{ MHz}$	10		10		

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	ALL TYPES	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	0.5	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	37.5	

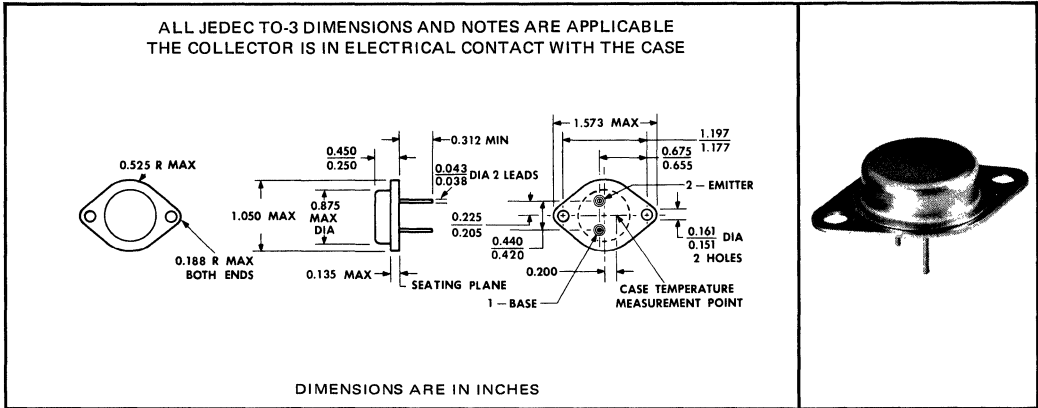
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TYPES TIP535, TIP536, TIP537 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 200 V, 300 V, 400 V Min V(BR)CEO
- 7.5-A Rated Continuous Collector Current
- 100 Watts at 100°C Case Temperature
- Min f_T of 10 MHz at 10 V, 1 A

mechanical data



TYPES TIP535, TIP536, TIP537
BULLETIN NO. DLS-7111613, DECEMBER 1971

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absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP535	TIP536	TIP537
Collector-Base Voltage	300 V	400 V	500 V
Collector-Emitter Voltage (See Note 1)	200 V	300 V	400 V
Emitter-Base Voltage	5 V	5 V	5 V
Continuous Collector Current	← 7.5 A →		
Peak Collector Current (See Note 2)	← 15 A →		
Continuous Base Current	← 3 A →		
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 100 W →		
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →		
Operating Collector Junction Temperature Range	← -65°C to 200°C →		
Storage Temperature Range	← -65°C to 200°C →		
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
2. This value applies for $t_{wv} \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 1 W/°C.
4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.

TYPES TIP535, TIP536, TIP537

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP535	TIP536	TIP537	UNIT
		MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	200	300	400	V
I_{CEO} Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $I_B = 0$	1			mA
	$V_{CE} = 150 \text{ V}$, $I_B = 0$		1		
	$V_{CE} = 200 \text{ V}$, $I_B = 0$			1	
I_{CES} Collector Cutoff Current	$V_{CE} = 300 \text{ V}$, $I_B = 0$	1			mA
	$V_{CE} = 400 \text{ V}$, $I_B = 0$		1		
	$V_{CE} = 500 \text{ V}$, $I_B = 0$			1	
	$V_{CE} = 150 \text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$	5			
	$V_{CE} = 200 \text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$		5		
	$V_{CE} = 250 \text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$			5	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 4 \text{ V}$, $I_C = 0$	0.5	0.5	0.5	mA
	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1	1	1	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$	20 100	20 100	20 100	V
	$V_{CE} = 4 \text{ V}$, $I_C = 7.5 \text{ A}$	5	5	5	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 7.5 \text{ A}$, See Notes 5 and 6	2	2	2	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$	1.2	1.2	1.2	V
	$I_B = 1.8 \text{ A}$, $I_C = 7.5 \text{ A}$	2.5	2.5	2.5	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	20	20	20	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 5 \text{ MHz}$	2	2	2	

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35	

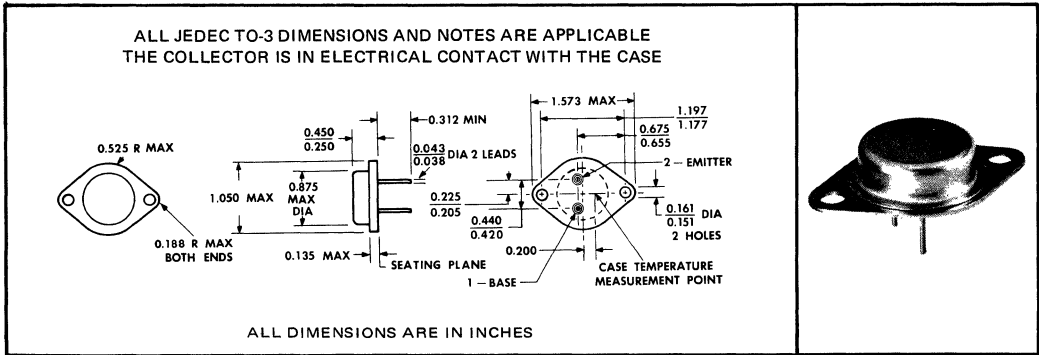
TYPES TIP538, TIP539, TIP540 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 200 V, 300 V, 400 V Min $V_{(BR)CEO}$
- 15-A Rated Continuous Collector Current
- 125 Watts at 100°C Case Temperature
- Min f_T of 10 MHz at 10 V, 1 A

TYPES TIP538, TIP539, TIP540
BULLETIN NO. DL-S7111647, DECEMBER 1971

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP538	TIP539	TIP540
Collector-Base Voltage	300 V	400 V	500 V
Collector-Emitter Voltage (See Note 1)	200 V	300 V	400 V
Emitter-Base Voltage	5 V	5 V	5 V
Continuous Collector Current	← 15 A →	← 15 A →	← 15 A →
Peak Collector Current (See Note 2)	← 25 A →	← 25 A →	← 25 A →
Continuous Base Current	← 5 A →	← 5 A →	← 5 A →
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	← 125 W →	← 125 W →	← 125 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	← 5 W →	← 5 W →
Operating Collector Junction Temperature Range	-65°C to 200°C		
Storage Temperature Range	-65°C to 200°C		
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 300°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1.25 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.

TYPES TIP538, TIP539, TIP540

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP538		TIP539		TIP540		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	200		300		400		V
I_{CEO} Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $I_B = 0$	2						mA
	$V_{CE} = 150 \text{ V}$, $I_B = 0$			2				
	$V_{CE} = 200 \text{ V}$, $I_B = 0$					2		
I_{CES} Collector Cutoff Current	$V_{CE} = 300 \text{ V}$, $I_B = 0$	1						mA
	$V_{CE} = 400 \text{ V}$, $I_B = 0$			1				
	$V_{CE} = 500 \text{ V}$, $I_B = 0$					1		
	$V_{CE} = 150 \text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$	10						
	$V_{CE} = 200 \text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$			10				
	$V_{CE} = 250 \text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$					10		
I_{EBO} Emitter Cutoff Current	$V_{EB} = 4 \text{ V}$, $I_C = 0$	0.5		0.5		0.5		mA
	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1		1		1		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 7.5 \text{ A}$	20	100	20	100	20	100	
	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$	5		5		5		
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 15 \text{ A}$, See Notes 5 and 6	2		2		2		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 0.75 \text{ A}$, $I_C = 7.5 \text{ A}$	0.75		0.75		0.75		V
	$I_B = 3.75 \text{ A}$, $I_C = 15 \text{ A}$	2.5		2.5		2.5		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $f = 5 \text{ MHz}$	2		2		2		

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	0.8	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35	$^\circ\text{C/W}$

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TYPE TIP541 N-P-N SILICON POWER TRANSISTORS

TYPE TIP541
BULLETIN NO. DL-S-7111600, DECEMBER 1971

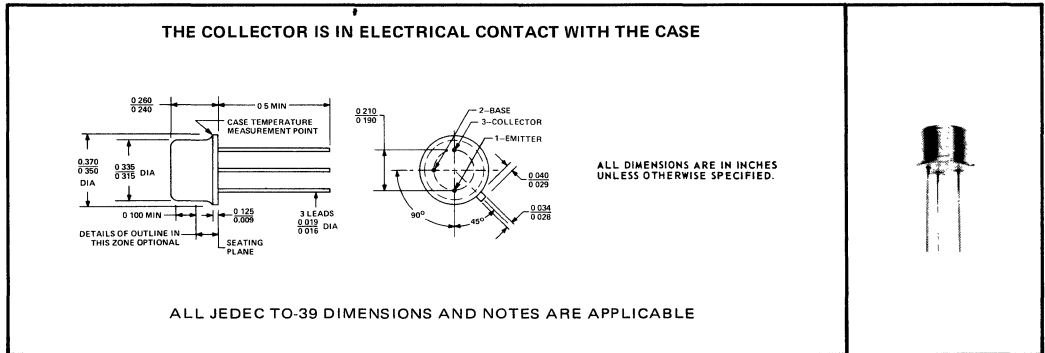
RADIATION-TOLERANT TRANSISTOR FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Min h_{FE} of 10 at 4 V, 2 A after 5×10^{14} Fast Neutrons/cm²
- 4 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.4 V at $I_C = 2$ A
- Min f_T of 150 MHz at 5 V, 0.5 A
- 1 mJ Reverse Energy Rating

description

The TIP541 transistor offers a significant advance in radiation-tolerant-device technology. Unique construction techniques produce transistors which maintain useful characteristics after fast-neutron radiation fluences through 5×10^{14} n/cm².

mechanical data



5



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	50 V
Collector-Emitter Voltage (See Note 1)	45 V
Emitter-Base Voltage	5 V
Continuous Collector Current	2 A
Peak Collector Current (See Note 2)	5 A
Continuous Base Current	1 A
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	4 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	1 W
Unclamped Inductive Load Energy (See Note 5)	1 mJ
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_{WV} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 40 mW/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. † L = 125 μ H, $R_{BB1} = 10 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 20$ V, $I_{CM} = 4$ A. Energy $\approx I_C^2 L/2$.

† This circuit appears on page 5-1 of this data book.

TYPE TIP541

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	45		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 20 \text{ V}$, $I_B = 0$		5	mA
I_{CES}	Collector Cutoff Current	$V_{CE} = 50 \text{ V}$, $V_{BE} = 0$		1	mA
		$V_{CE} = 25 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		2	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 4 \text{ V}$, $I_C = 0$		20	μA
		$V_{EB} = 5 \text{ V}$, $I_C = 0$		500	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Notes 6 and 7	40	200	
		$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 6 and 7	70		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 6 and 7	1.2		V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.1 \text{ A}$, $I_C = 1 \text{ A}$, See Notes 6 and 7		0.3	V
		$I_B = 0.2 \text{ A}$, $I_C = 2 \text{ A}$, See Notes 6 and 7		0.4	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$	40		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 10 \text{ MHz}$	15		

5

post-irradiation electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	RADIATION FLUENCE†	MIN	MAX	UNIT
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 2 \text{ A}$, See Notes 6 and 7	$5 \times 10^{14} \text{ n/cm}^2$	10		

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	175	

†Radiation is fast neutrons (n) at $E \geq 10 \text{ keV}$ (reactor spectrum).

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPE TIP542 N-P-N SILICON POWER TRANSISTOR

TYPE TIP542
BULLETIN NO. DL-5711599, DECEMBER 1971

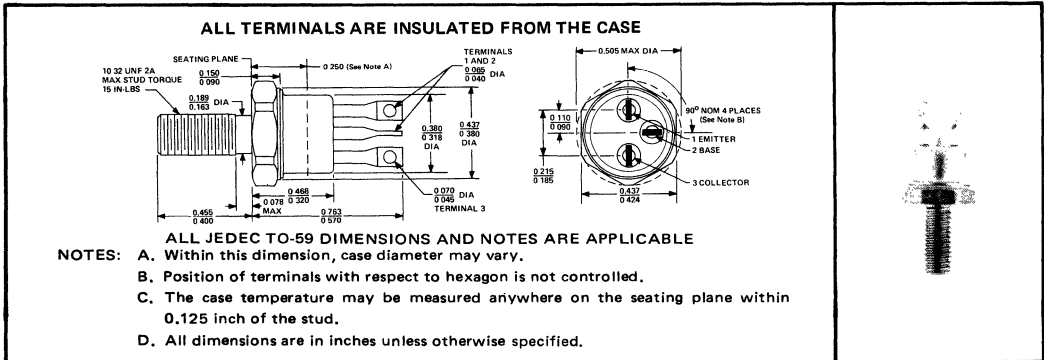
RADIATION-TOLERANT TRANSISTOR FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Min h_{FE} of 10 at 4 V, 8 A after 5×10^{14} Fast Neutrons/cm²
- 40 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.8 V at $I_C = 10$ A
- Min f_T of 150 MHz at 5 V, 1 A
- 4 mJ Reverse Energy Rating

description

The TIP542 transistor offers a significant advance in radiation-tolerant-device technology. Unique construction techniques produce transistors which maintain useful characteristics after fast-neutron radiation fluences through 5×10^{14} n/cm².

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	50 V
Collector-Emitter Voltage (See Note 1)	45 V
Emitter-Base Voltage	5 V
Continuous Collector Current	10 A
Peak Collector Current (See Note 2)	20 A
Continuous Base Current	5 A
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	40 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W
Unclamped Inductive Load Energy (See Note 5)	4 mJ
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	300°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_{sw} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.4 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. † $L = 125 \mu\text{H}$, $R_{BB1} = 5 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 20$ V, $I_{CM} = 8$ A, Energy $\approx I_C^2 L/2$.
- † This circuit appears on page 5-1 of this data book.

TYPE TIP542

N-P-N SILICON POWER TRANSISTOR

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	45		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 20 \text{ V}$, $I_B = 0$	5		mA
I_{CES}	Collector Cutoff Current	$V_{CE} = 50 \text{ V}$, $V_{BE} = 0$	2		mA
		$V_{CE} = 25 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	4		
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 4 \text{ V}$, $I_C = 0$	0.2		mA
		$V_{EB} = 5 \text{ V}$, $I_C = 0$	2		
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$	40	200	
		$V_{CE} = 4 \text{ V}$, $I_C = 8 \text{ A}$	70		
		$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$	70		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 6 and 7	1.4		V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$	0.5		V
		$I_B = 1 \text{ A}$, $I_C = 10 \text{ A}$	0.8		
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	35		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 10 \text{ MHz}$	15		

5

post-irradiation electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	RADIATION FLUENCE [†]	MIN	MAX	UNIT
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 8 \text{ A}$, See Notes 6 and 7	$5 \times 10^{14} \text{ n/cm}^2$	10		

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	2.5	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	87.5	

[†]Radiation is fast neutrons (n) at $E \geq 10 \text{ keV}$ (reactor spectrum).

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPE TIP543 N-P-N SILICON POWER TRANSISTOR

TYPE TIP543
BULLETIN NO. DL-S7111601, DECEMBER 1971

RADIATION-TOLERANT TRANSISTOR FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- Min h_{FE} of 10 at 4 V, 5 A after 2×10^{14} Fast Neutrons/cm²
- 40 W at 100°C Case Temperature
- Max $V_{CE(sat)}$ of 0.8 V at $I_C = 10$ A, $I_B = 1$ A
- Min f_T of 120 MHz at 5 V, 1 A
- 4 mJ Reverse Energy Rating

description

The TIP543 transistor offers a significant advance in radiation-tolerant-device technology. Unique construction techniques produce transistors which maintain useful characteristics after fast-neutron radiation fluences through 2×10^{14} n/cm².

mechanical data

ALL TERMINALS ARE INSULATED FROM THE CASE

ALL JEDEC TO-59 DIMENSIONS AND NOTES ARE APPLICABLE

NOTES: A. Within this dimension, case diameter may vary.
 B. Position of terminals with respect to hexagon is not controlled.
 C. The case temperature may be measured anywhere on the seating plane within 0.125 inch of the stud.
 D. All dimensions are in inches unless otherwise specified.

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	75 V
Collector-Emitter Voltage (See Note 1)	65 V
Emitter-Base Voltage	5 V
Continuous Collector Current	10 A
Peak Collector Current (See Note 2)	20 A
Continuous Base Current	5 A
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)	40 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W
Unclamped Inductive Load Energy (See Note 5)	4 mJ
Operating Collector Junction Temperature Range	-65°C to 200°C
Storage Temperature Range	-65°C to 200°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	300°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_W \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 0.4 W/°C.
 4. Derate linearly to 200°C free-air temperature at the rate of 11.4 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. † $L = 125 \mu\text{H}$, $R_{BB1} = 5 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10$ V, $V_{BB2} = 0$ V, $R_L = 0.1 \Omega$, $V_{CC} = 20$ V, $I_{CM} = 8$ A, Energy $\approx I_C^2 L/2$.

† This circuit appears on page 5-1 of this data book.

TYPE TIP543

N-P-N SILICON POWER TRANSISTOR

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	65		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $I_B = 0$		2	mA
I_{CES}	Collector Cutoff Current	$V_{CE} = 75 \text{ V}$, $V_{BE} = 0$		1	mA
		$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$		2	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 3 \text{ V}$, $I_C = 0$		0.2	mA
		$V_{EB} = 5 \text{ V}$, $I_C = 0$		1	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 6 and 7	40	200	
		$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 6 and 7	40		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 6 and 7		1.4	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.5 \text{ A}$, $I_C = 5 \text{ A}$, See Notes 6 and 7		0.5	V
		$I_B = 1 \text{ A}$, $I_C = 10 \text{ A}$, See Notes 6 and 7		0.8	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	40		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ A}$, $f = 10 \text{ MHz}$	12		

5

post-irradiation electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	RADIATION FLUENCE [†]	MIN	MAX	UNIT
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$, See Notes 6 and 7	$2 \times 10^{14} \text{ n/cm}^2$	10		

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	2.5	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	87.5	

[†]Radiation is fast neutrons (n) at $E \geq 10 \text{ keV}$ (reactor spectrum).

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

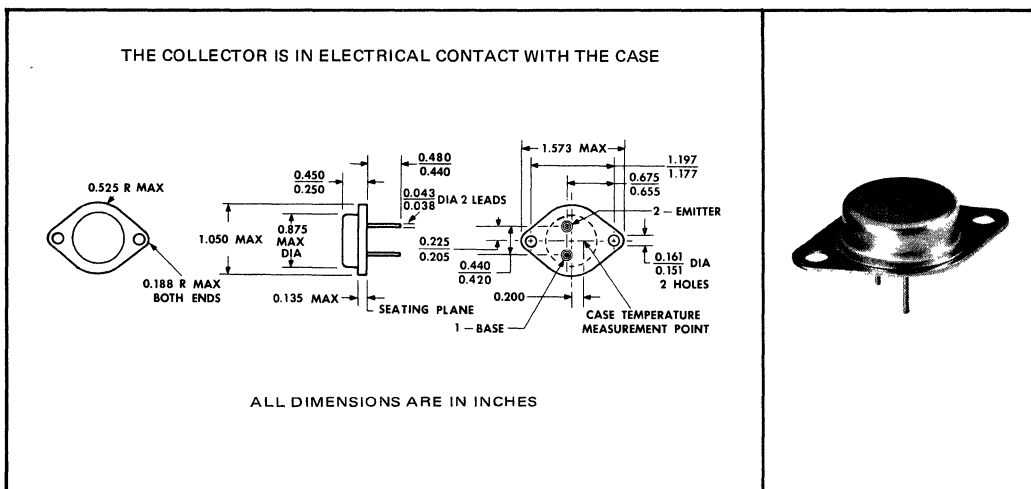
TYPES TIP544, TIP545, TIP546 P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
RECOMMENDED FOR COMPLEMENTARY USE WITH 2N5758, 2N5759, 2N5760

- 150 W at 25°C Case Temperature
- 6-A Rated Continuous Collector Current
- Min f_T of 1 MHz at 20 V, 0.5 A

mechanical data

The case outline falls within JEDEC TO-3.



TYPES TIP544, TIP545, TIP546
BULLETIN NO. DL-S-711605, DECEMBER 1971

5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP544	TIP545	TIP546
Collector-Base Voltage	-100 V	-120 V	-140 V
Collector-Emitter Voltage (See Note 1)	-100 V	-120 V	-140 V
Emitter-Base Voltage	-7 V	-7 V	-7 V
Continuous Collector Current	← -6 A →	← -6 A →	← -6 A →
Peak Collector Current (See Note 2)	← -10 A →	← -10 A →	← -10 A →
Continuous Base Current	← -4 A →	← -4 A →	← -4 A →
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W →	← 150 W →	← 150 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	← 5 W →	← 5 W →
Operating Collector Junction Temperature Range	← -65°C to 200°C →	← -65°C to 200°C →	← -65°C to 200°C →
Storage Temperature Range	← -65°C to 200°C →	← -65°C to 200°C →	← -65°C to 200°C →
Terminal Temperature 1/16 Inch from Case for 10 Seconds	← 235°C →	← 235°C →	← 235°C →

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 200°C case temperature at the rate of 0.857 W/°C.
4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C.

TYPES TIP544, TIP545, TIP546

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIP544	TIP545	TIP546	UNIT
		MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ mA}$, $I_B = 0$, See Note 5	-100	-120	-140	V
I_{CBO} Collector Cutoff Current	$V_{CB} = -100 \text{ V}$, $I_E = 0$	-1			mA
	$V_{CB} = -120 \text{ V}$, $I_E = 0$		-1		
	$V_{CB} = -140 \text{ V}$, $I_E = 0$			-1	
I_{CEO} Collector Cutoff Current	$V_{CE} = -50 \text{ V}$, $I_B = 0$	-5			mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$		-5		
	$V_{CE} = -70 \text{ V}$, $I_B = 0$			-5	
I_{CEV} Collector Cutoff Current	$V_{CE} = -100 \text{ V}$, $V_{BE} = 1.5 \text{ V}$	-1			mA
	$V_{CE} = -120 \text{ V}$, $V_{BE} = 1.5 \text{ V}$		-1		
	$V_{CE} = -140 \text{ V}$, $V_{BE} = 1.5 \text{ V}$			-1	
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	-5			
	$V_{CE} = -120 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$		-5		
$V_{CE} = -140 \text{ V}$, $V_{BE} = 1.5 \text{ V}$, $T_C = 150^\circ\text{C}$			-5		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -7 \text{ V}$, $I_C = 0$	-1	-1	-1	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ V}$, $I_C = -3 \text{ A}$	25 100	20 80	15 60	
	$V_{CE} = -2 \text{ V}$, $I_C = -6 \text{ A}$	5	5	5	
V_{BE} Base-Emitter Voltage	$V_{CE} = -2 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 5 and 6	-1.5	-1.5	-1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.3 \text{ A}$, $I_C = -3 \text{ A}$	-1	-1	-1	V
	$I_B = -1.2 \text{ A}$, $I_C = -6 \text{ A}$	-2	-2	-2	
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -2 \text{ A}$, $f = 1 \text{ kHz}$	15	15	15	
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -20 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 0.5 \text{ MHz}$	2	2	2	
C_{obo} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 0.1 \text{ to } 1 \text{ MHz}$	300	300	300	pF

NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

5

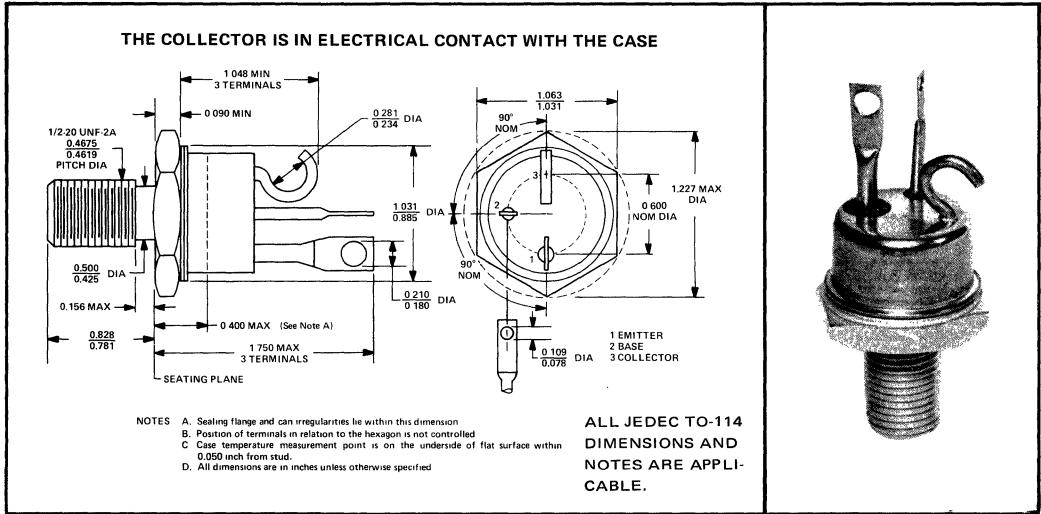
TYPES TIXP547, TIXP548, TIXP549 N-P-N SILICON POWER TRANSISTORS

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS

- 60 V, 80 V, and 100 V Min $V_{(BR)CEO}$
- 100-A Rated Continuous Collector Current
- 200 Watts at 100°C Case Temperature
- Min f_T of 3 MHz at 5 V, 5 A

TYPES TIXP547, TIXP548, TIXP549
BULLETIN NO. DLS-7111638, DECEMBER 1971

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage
Collector-Emitter Voltage (See Note 1)
Emitter-Base Voltage
Continuous Collector Current
Peak Collector Current (See Note 2)
Continuous Base Current
Safe Operating Area at (or below) 100°C Case Temperature
Continuous Device Dissipation at (or below) 100°C Case Temperature (See Note 3)
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)
Operating Collector Junction Temperature Range
Storage Temperature Range
Terminal Temperature 1/16 Inch from Case for 10 Seconds

TIXP547	TIXP548	TIXP549
80 V	100 V	120 V
60 V	80 V	100 V
5 V	5 V	5 V
← 100 A →		
← 150 A →		
← 25 A →		
← See Figure 1 →		
← 200 W →		
← 8.5 W →		
← -65°C to 200°C →		
← -65°C to 200°C →		
← 300°C →		

- NOTES:**
- These values apply when the base-emitter diode is open-circuited.
 - This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 - Derate linearly to 200°C case temperature at the rate of 2 W/°C.
 - Derate linearly to 200°C free-air temperature at the rate of 48.5 mW/°C.

TYPES TIXP547, TIXP548, TIXP549

N-P-N SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIXP547	TIXP548	TIXP549	UNIT	
		MIN	MAX	MIN		MAX
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 200 \text{ mA}$, $I_B = 0$, See Note 5	60	80	100	V	
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	10			mA	
	$V_{CE} = 40 \text{ V}$, $I_B = 0$	10				
	$V_{CE} = 50 \text{ V}$, $I_B = 0$	10				
I_{CES} Collector Cutoff Current	$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$	5			mA	
	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$	5				
	$V_{CE} = 120 \text{ V}$, $V_{BE} = 0$	5				
	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	25				
	$V_{CE} = 50 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	25				
	$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$, $T_C = 150^\circ\text{C}$	25				
I_{EBO} Emitter Cutoff Current	$V_{EB} = 4 \text{ V}$, $I_C = 0$	2	2	2	mA	
	$V_{EB} = 5 \text{ V}$, $I_C = 0$	5	5	5		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 50 \text{ A}$	15	100	15	100	
	$V_{CE} = 4 \text{ V}$, $I_C = 100 \text{ A}$	5	5	5	5	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 100 \text{ A}$, See Notes 5 and 6	4	4	4	V	
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 5 \text{ A}$, $I_C = 50 \text{ A}$	1.5	1.5	1.5	V	
	$I_B = 25 \text{ A}$, $I_C = 100 \text{ A}$, See Notes 5 and 6	3	3	3		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$, $f = 1 \text{ kHz}$	15	15	15		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ A}$, $f = 1 \text{ MHz}$	3	3	3		

NOTES: 5. These parameters must be measured using pulse techniques. $t_W = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	0.5	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	20.6	

MAXIMUM SAFE OPERATING AREA

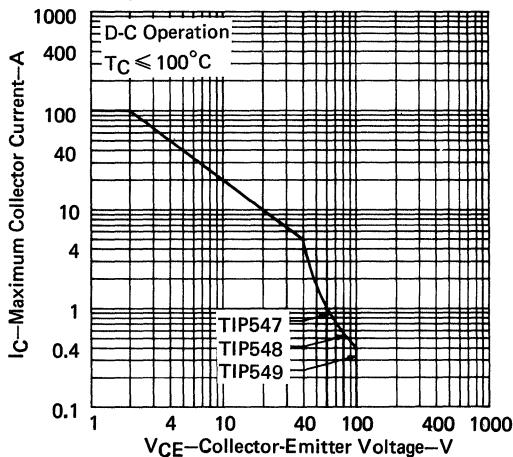


FIGURE 1

TYPES TIP640, TIP641, TIP642

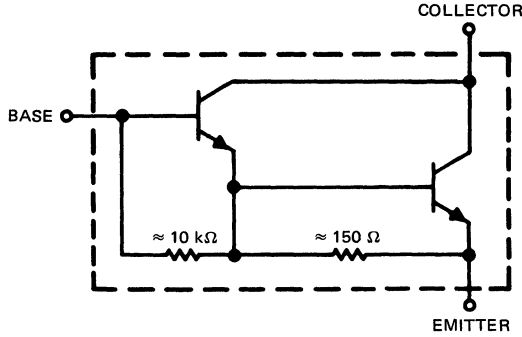
N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

DESIGNED FOR COMPLEMENTARY USE WITH TIP645, TIP646, TIP647

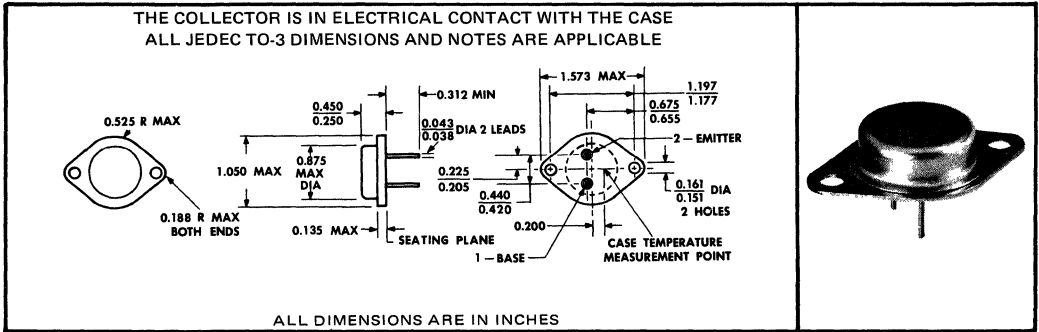
- 175 W at 25°C Case Temperature
- 10-A Rated Collector Current
- Min h_{FE} of 1000 at 4 V, 5 A
- 100-mJ Reverse Energy Rating

TYPES TIP640, TIP641, TIP642
BULLETIN NO. DLS-7111642, DECEMBER 1971

device schematic



mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP640	TIP641	TIP642
Collector-Base Voltage	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	60 V	80 V	100 V
Emitter-Base Voltage	5 V	5 V	5 V
Continuous Collector Current	← 10 A →	← 10 A →	← 10 A →
Peak Collector Current (See Note 2)	← 15 A →	← 15 A →	← 15 A →
Continuous Base Current	← 0.5 A →	← 0.5 A →	← 0.5 A →
Safe Operating Areas at (or below) 25°C Case Temperature	← See Figures 7 and 8 →		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 175 W →	← 175 W →	← 175 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	← 5 W →	← 5 W →
Unclamped Inductive Load Energy (See Note 5)	← 100 mJ →	← 100 mJ →	← 100 mJ →
Operating Collector Junction Temperature Range	← -65°C to 200°C →	← -65°C to 200°C →	← -65°C to 200°C →
Storage Temperature Range	← -65°C to 200°C →	← -65°C to 200°C →	← -65°C to 200°C →
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →	← 260°C →	← 260°C →

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_{sw} \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1 W/°C or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100$ mH, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 20$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP640, TIP641, TIP642

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP640	TIP641	TIP642	UNIT
		MIN	MAX	MIN	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	60	80	100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	2			mA
	$V_{CE} = 40 \text{ V}$, $I_B = 0$		2		
	$V_{CE} = 50 \text{ V}$, $I_B = 0$			2	
I_{CBO} Collector Cutoff Current	$V_{CB} = 60 \text{ V}$, $I_E = 0$	1			mA
	$V_{CB} = 80 \text{ V}$, $I_E = 0$		1		
	$V_{CB} = 100 \text{ V}$, $I_E = 0$			1	
I_{EBO} Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	2	2	2	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$	1000	1000	1000	
	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$	500	500	500	
V_{BE} Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 6 and 7	3	3	3	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 10 \text{ mA}$, $I_C = 5 \text{ A}$	2	2	2	V
	$I_B = 40 \text{ mA}$, $I_C = 10 \text{ A}$	3	3	3	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

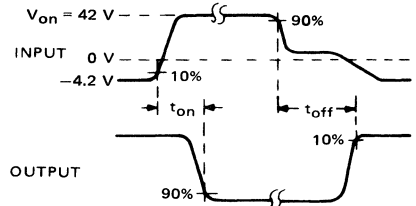
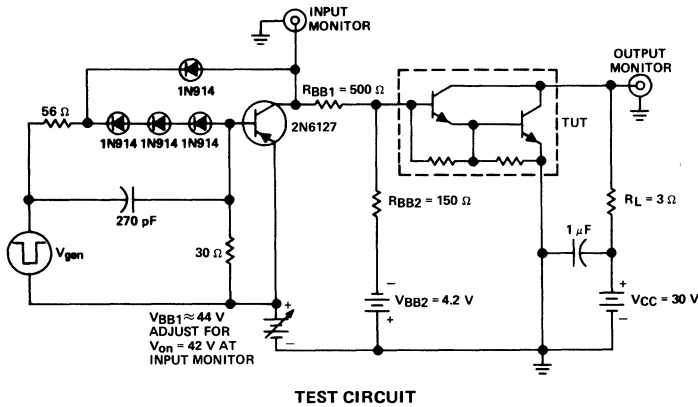
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 10 \text{ A}$, $I_B(1) = 40 \text{ mA}$, $I_B(2) = -40 \text{ mA}$,	0.9	μs
t_{off} Turn-Off Time	$V_{BE(off)} = -4.2 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	11	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

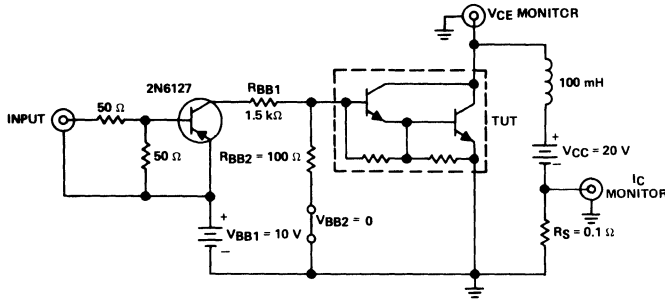


- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

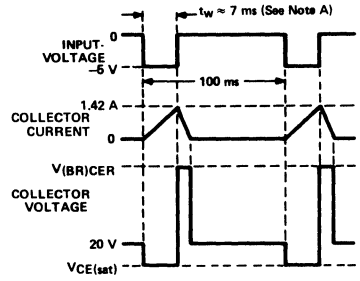
TYPES TIP640, TIP641, TIP642 N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

NOTE A: Input pulse width is increased until $I_{CM} = 1.42$ A.



VOLTAGE AND CURRENT WAVEFORMS

TYPICAL CHARACTERISTICS

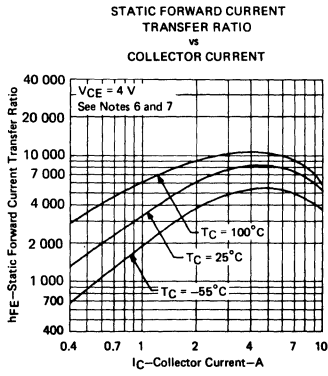


FIGURE 3

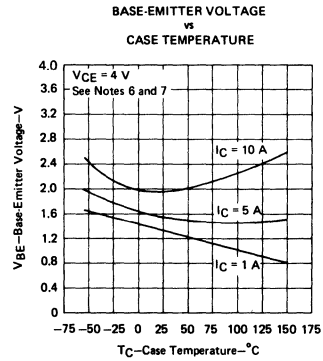


FIGURE 4

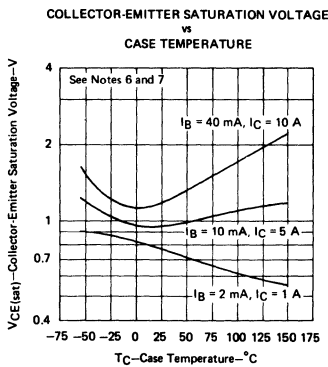


FIGURE 5

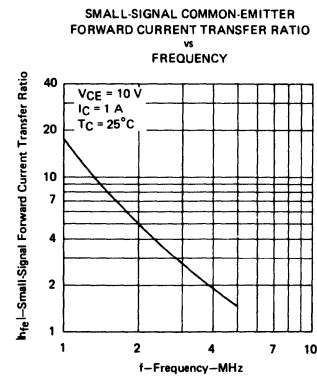


FIGURE 6

- NOTES: 6. These parameters must be measured using pulse techniques. $t_{pw} = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP640, TIP641, TIP642

N-P-N DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

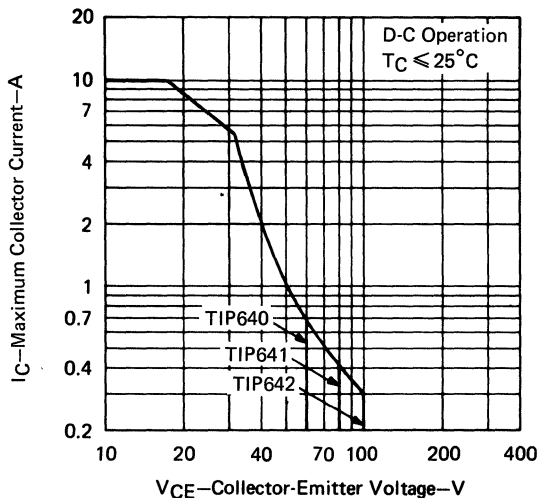


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

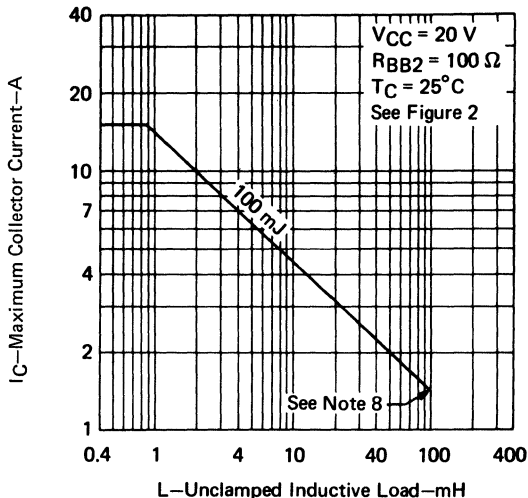


FIGURE 8

NOTE 8: Above this point the safe operating area has not been defined.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

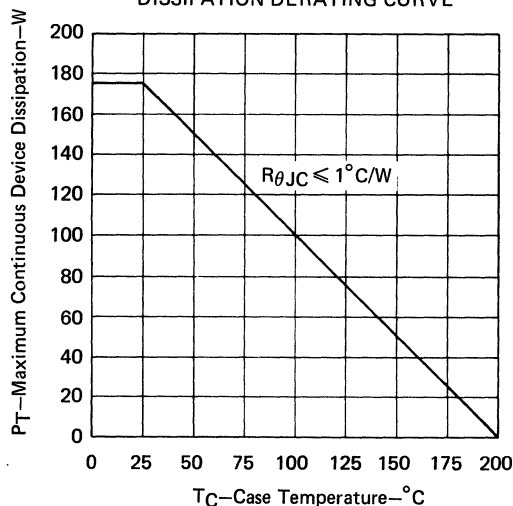


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

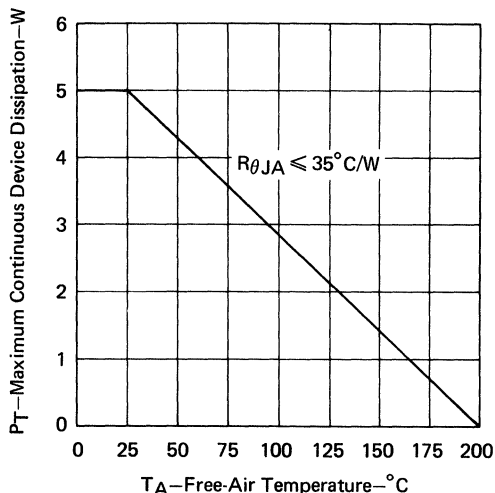


FIGURE 10

TYPES TIP645, TIP646, TIP647

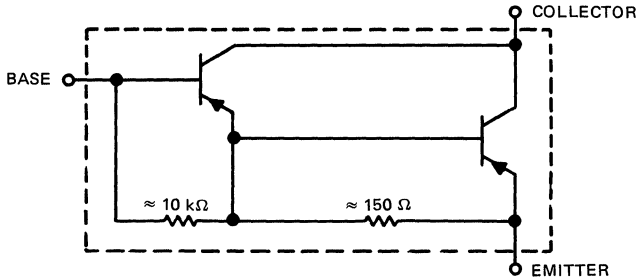
P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

DESIGNED FOR COMPLEMENTARY USE WITH TIP640, TIP641, TIP642

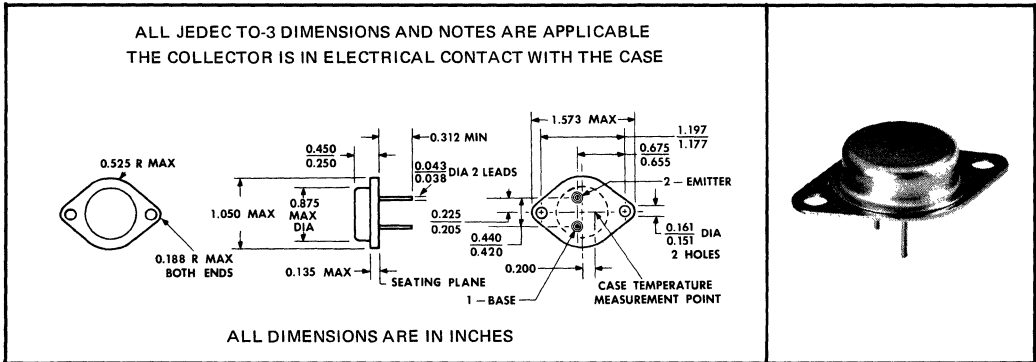
- 175 W at 25°C Case Temperature
- 10-A Rated Collector Current
- Min h_{FE} of 1000 at 4 V, 5 A
- 100 mJ Reverse Energy Rating

TYPES TIP645, TIP646, TIP647
BULLETIN NO. DL-S-7111637, DECEMBER 1971

device schematic



mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP645	TIP646	TIP647
Collector-Base Voltage	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-60 V	-80 V	-100 V
Emitter-Base Voltage	-5 V	-5 V	-5 V
Continuous Collector Current	← 10 A →	← 10 A →	← 10 A →
Peak Collector Current (See Note 2)	← 15 A →	← 15 A →	← 15 A →
Continuous Base Current	← 0.5 A →	← 0.5 A →	← 0.5 A →
Safe Operating Areas at (or below) 25°C Case Temperature	See Figures 7 and 8		
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 175 W →	← 175 W →	← 175 W →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 5 W →	← 5 W →	← 5 W →
Unclamped Inductive Load Energy (See Note 5)	← 100 mJ →	← 100 mJ →	← 100 mJ →
Operating Collector Junction Temperature Range	-65°C to 200°C		
Storage Temperature Range	-65°C to 200°C		
Terminal Temperature 1/8 Inch from Case to 10 Seconds	← 260°C →		

- NOTES: 1. These values apply when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 200°C case temperature at the rate of 1 W/°C or refer to Dissipation Derating Curve, Figure 9.
 4. Derate linearly to 200°C free-air temperature at the rate of 28.6 mW/°C or refer to Dissipation Derating Curve, Figure 10.
 5. This rating is based on the capability of the transistors to operate safely in the circuit of Figure 2. $L = 100$ mH, $R_{BB2} = 100$ Ω, $V_{BB2} = 0$ V, $R_S = 0.1$ Ω, $V_{CC} = 20$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP645, TIP646, TIP647

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP645	TIP646	TIP647	UNIT
		MIN MAX	MIN MAX	MIN MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-60	-80 *	-100	V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-2			mA
	$V_{CE} = -40 \text{ V}$, $I_B = 0$		-2		
	$V_{CE} = -50 \text{ V}$, $I_B = 0$			-2	
I_{CBO} Collector Cutoff Current	$V_{CB} = -60 \text{ V}$, $I_E = 0$	-1			mA
	$V_{CB} = -80 \text{ V}$, $I_E = 0$		-1		
	$V_{CB} = -100 \text{ V}$, $I_E = 0$			-1	
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-2	-2	-2	mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -5 \text{ A}$	1000	1000	1000	
	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$	500	500	500	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$, See Notes 6 and 7	-3	-3	-3	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -10 \text{ mA}$, $I_C = -5 \text{ A}$	-2	-2	-2	V
	$I_B = -40 \text{ mA}$, $I_C = -10 \text{ A}$	-3	-3	-3	

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

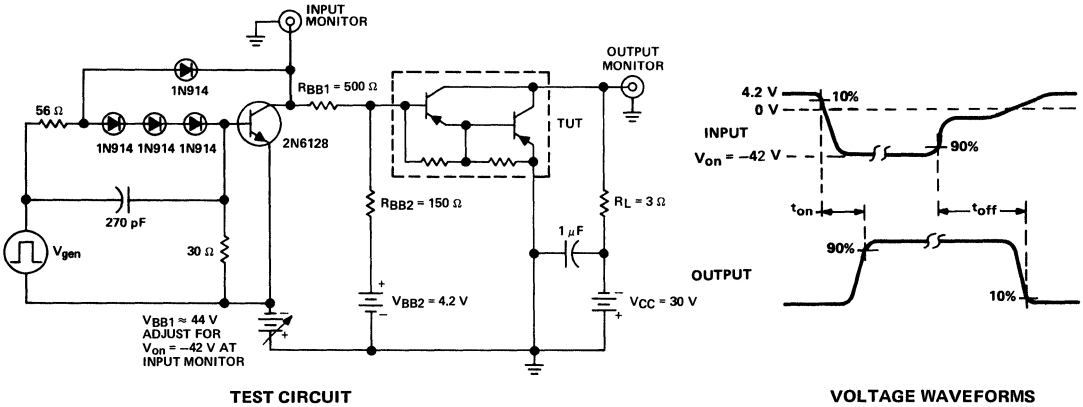
5

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -10 \text{ A}$, $I_B(1) = -40 \text{ mA}$, $I_B(2) = 40 \text{ mA}$,	0.9	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 4.2 \text{ V}$, $R_L = 3 \Omega$, See Figure 1	11	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



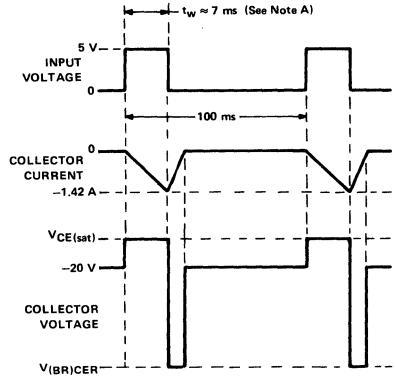
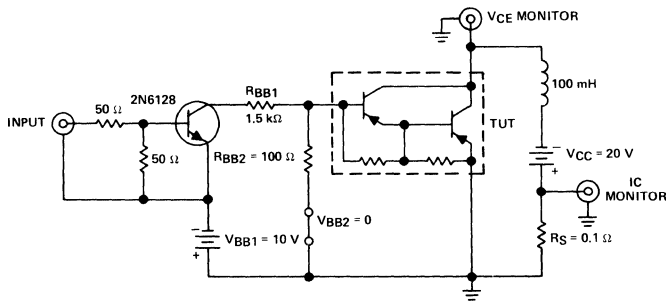
- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_w = 20 \mu\text{s}$, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPES TIP645, TIP646, TIP647

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

INDUCTIVE LOAD SWITCHING



NOTE A: Input pulse width is increased until $I_{CM} = -1.42$ A.

FIGURE 2

TYPICAL CHARACTERISTICS

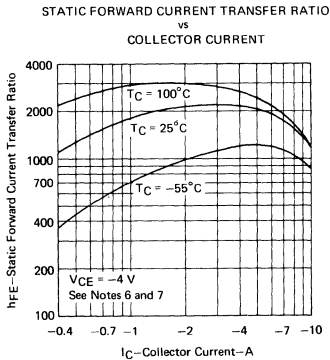


FIGURE 3

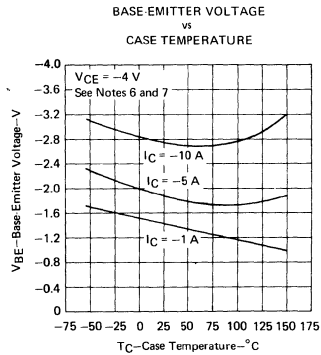


FIGURE 4

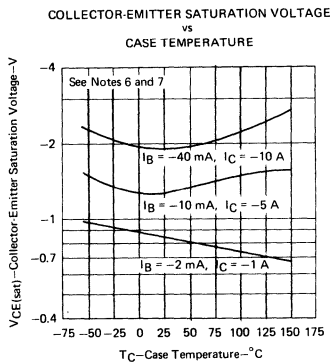


FIGURE 5

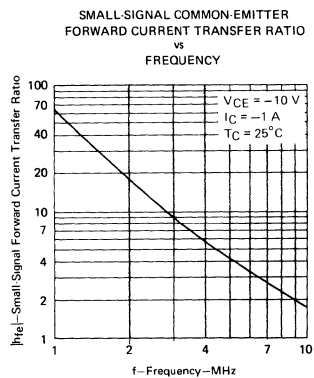


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques. $t_W = 300 \mu s$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

TYPES TIP645, TIP646, TIP647

P-N-P DARLINGTON-CONNECTED SILICON POWER TRANSISTORS

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

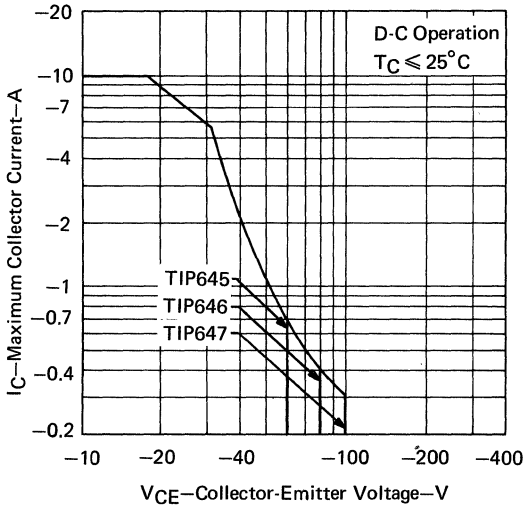


FIGURE 7

NOTE 8: Above this point the safe operating area has not been defined.

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

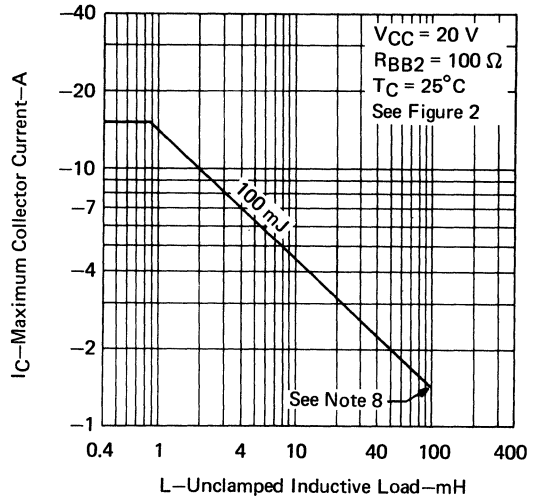


FIGURE 8

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE

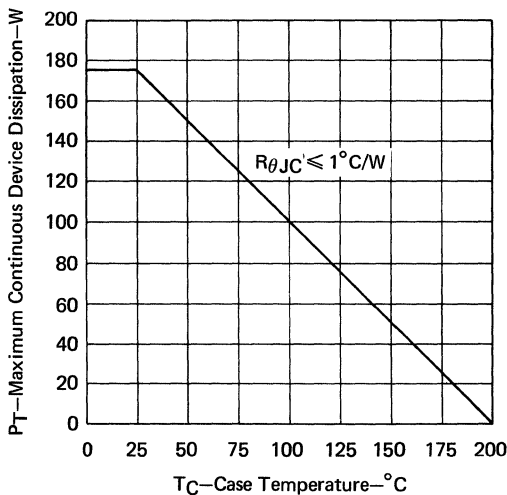


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

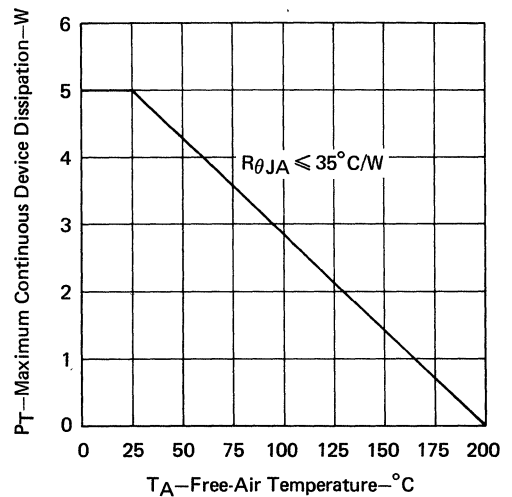


FIGURE 10

TYPE TIP2955

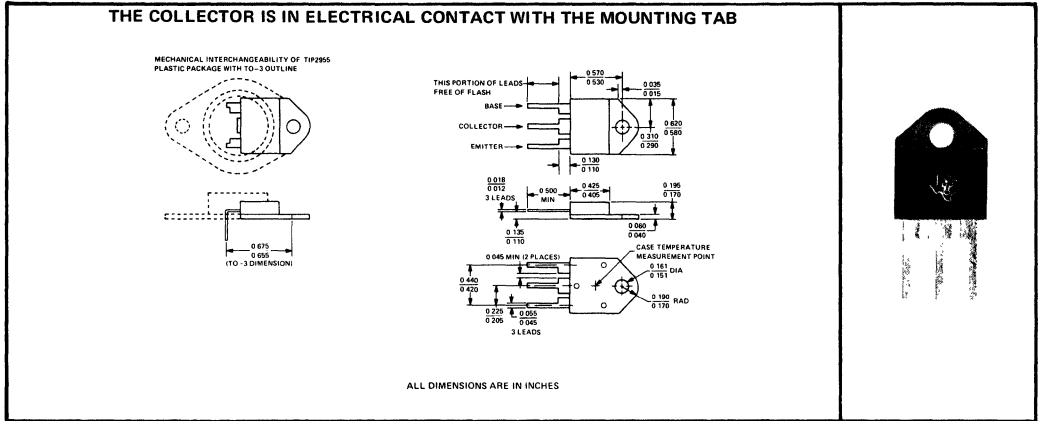
P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

TYPE TIP2955
BULLETIN NO. DLS-7211662, JANUARY 1972

**FOR POWER AMPLIFIER AND HIGH-SPEED SWITCHING APPLICATIONS
RECOMMENDED FOR COMPLEMENTARY USE WITH TIP3055**

- 90 Watts at 25°C Case Temperature
- 15 A Rated Collector Current
- 62.5 mJ Reverse Energy Rating

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	-100 V
Collector-Emitter Voltage (See Note 1)	-70 V
Emitter-Base Voltage	-7 V
Continuous Collector Current	-15 A
Continuous Base Current	-7 A
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 5
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	90 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	3.5 W
Unclamped Inductive Load Energy (See Note 4)	62.5 mJ
Operating Collector Junction Temperature Range	-65°C to 150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature 1/8 Inch from Case For 10 Seconds	260°C

- NOTES: 1. This value applies when the base-emitter resistance $R_{BE} = 100 \Omega$.
2. Derate linearly to 150°C case temperature at the rate of 0.72 W/°C.
3. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
4. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20 \text{ mH}$, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0 \text{ V}$, $R_S = 0.1 \Omega$, $V_{CC} = 10 \text{ V}$. Energy $\approx I_C^2 L / 2$.

TYPE TIP2955

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 5	-60		V
I_{CER} Collector Cutoff Current	$V_{CE} = -70 \text{ V}$, $R_{BE} = 100 \Omega$	-1		mA
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.7		mA
I_{CEV} Collector Cutoff Current	$V_{CE} = -100 \text{ V}$, $V_{BE} = 1.5 \text{ V}$	-5		mA
I_{EBO} Emitter Cutoff Current	$V_{EB} = -7 \text{ V}$, $I_C = 0$	-5		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -4 \text{ A}$, See Notes 5 and 6	20	70	
	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$, See Notes 5 and 6	5		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -4 \text{ A}$, See Notes 5 and 6	-1.8		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -400 \text{ mA}$, $I_C = -4 \text{ A}$, See Notes 5 and 6	-1.1		V
	$I_B = -3.3 \text{ A}$, $I_C = -10 \text{ A}$, See Notes 5 and 6	-3		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, $f = 1 \text{ kHz}$	15		
f_{hfe} Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Note 7	10		kHz

5

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.
7. f_{hfe} is the frequency at which the magnitude of the small-signal forward current transfer ratio is 0.707 of its low-frequency value. For this device, the reference measurement is made at 1 kHz.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.39	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35.7	

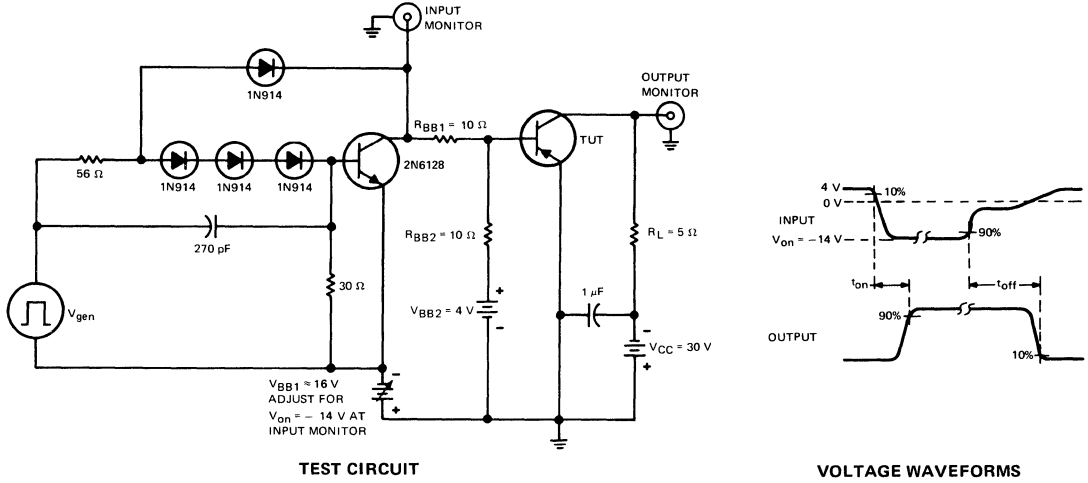
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -6 \text{ A}$, $I_B(1) = -0.6 \text{ A}$, $I_B(2) = 0.6 \text{ A}$,	0.4	μs
t_{off} Turn-Off Time	$V_{BE(off)} = 4 \text{ V}$, $R_L = 5 \Omega$, See Figure 1	0.7	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPE TIP2955 P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

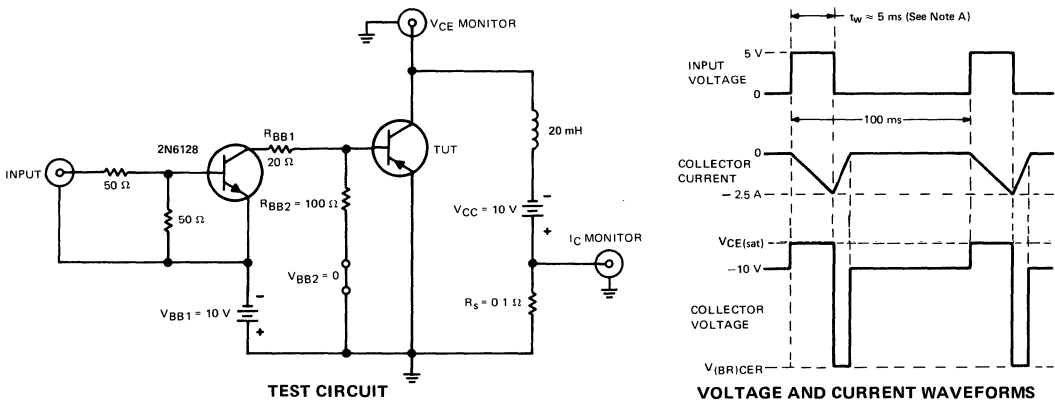
PARAMETER MEASUREMENT INFORMATION



- NOTES:**
- A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 - B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50 \Omega$, $t_w = 20 \mu$ s, duty cycle $\leq 2\%$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10 M\Omega$, $C_{in} \leq 11.5$ pF.
 - D. Resistors must be noninductive types.
 - E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



NOTE A: Input pulse width is increased until $I_{CM} = -2.5$ A.

FIGURE 2

TYPE TIP2955

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

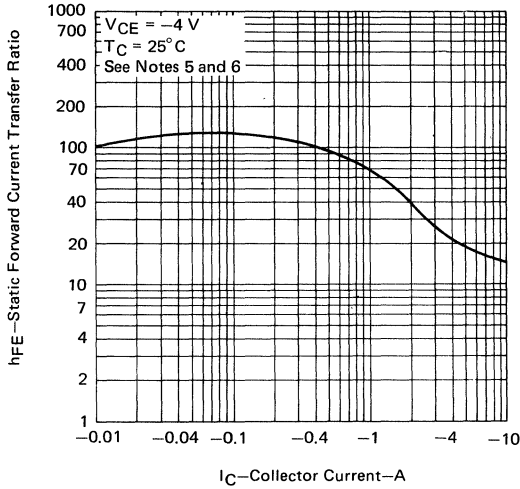


FIGURE 3

- NOTES: 5. These parameters must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

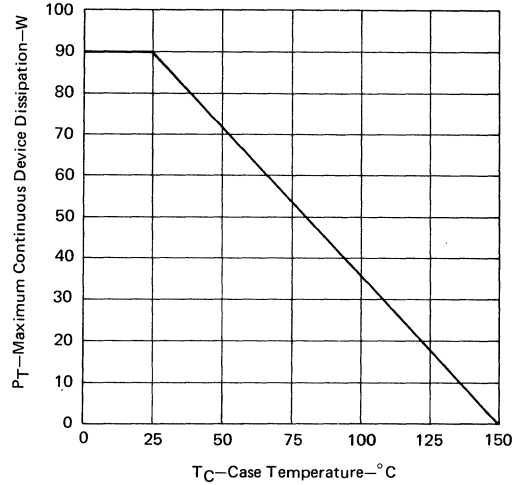


FIGURE 4

MAXIMUM SAFE OPERATING REGION

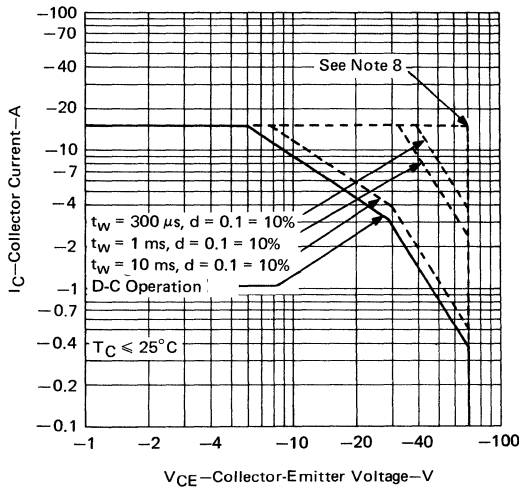


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

TYPE TIP3055

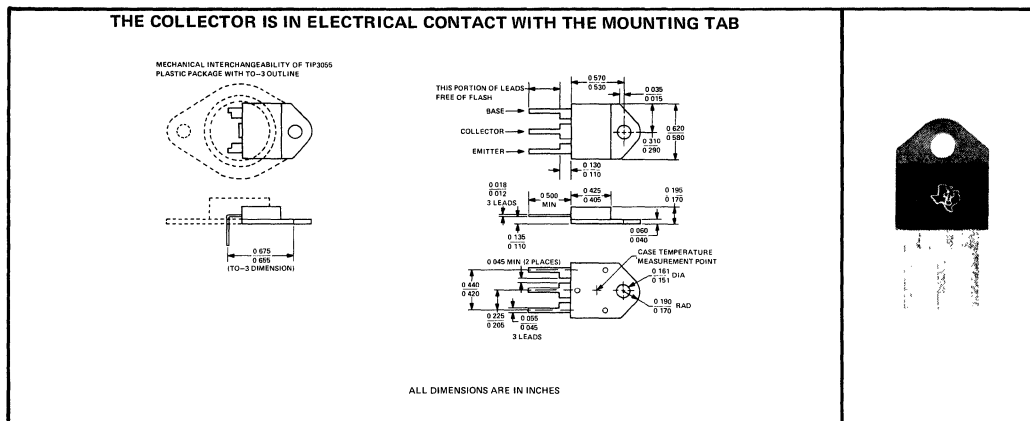
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

TYPE TIP3055
BULLETIN NO. DLS-7011410, DECEMBER 1970

FOR POWER AMPLIFIER AND HIGH-SPEED SWITCHING APPLICATIONS
PLASTIC-CASE REPLACEMENT FOR 2N3055

- 90 Watts at 25°C Case Temperature
- 15 A Rated Collector Current

mechanical data



5

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 1)	70 V
Emitter-Base Voltage	7 V
Continuous Collector Current	15 A
Continuous Base Current	7 A
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 5
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	90 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	3.5 W
Unclamped Inductive Load Energy (See Note 4)	62.5 mJ
Operating Collector Junction Temperature Range	-65°C to 150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature 1/8 Inch from Case For 10 Seconds	260°C

- NOTES: 1. This value applies when the base-emitter resistance $R_{BE} = 100 \Omega$.
2. Derate linearly to 150°C case temperature at the rate of 0.72 W/°C.
3. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
4. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20 \text{ mH}$, $R_{BB2} = 100 \Omega$, $V_{BB2} = 0 \text{ V}$, $R_S = 0.1 \Omega$, $V_{CC} = 10 \text{ V}$. Energy $\approx I_C^2 L / 2$.

TYPE TIP3055

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 5	60		V
I_{CER}	Collector Cutoff Current	$V_{CE} = 70 \text{ V}$, $R_{BE} = 100 \Omega$		1	mA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$		0.7	mA
I_{CEV}	Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$		5	mA
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 7 \text{ V}$, $I_C = 0$		5	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, See Notes 5 and 6	20	70	
		$V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, See Notes 5 and 6	5		
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, See Notes 5 and 6		1.8	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 400 \text{ mA}$, $I_C = 4 \text{ A}$, See Notes 5 and 6		1.1	V
		$I_B = 3.3 \text{ A}$, $I_C = 10 \text{ A}$, See Notes 5 and 6		3	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, $f = 1 \text{ kHz}$	15		
f_{hfe}	Small-Signal Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$, See Note 7	10		kHz

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
 7. f_{hfe} is the frequency at which the magnitude of the small-signal forward current transfer ratio is 0.707 of its low-frequency value. For this device, the reference measurement is made at 1 kHz.

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	1.39	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	35.7	

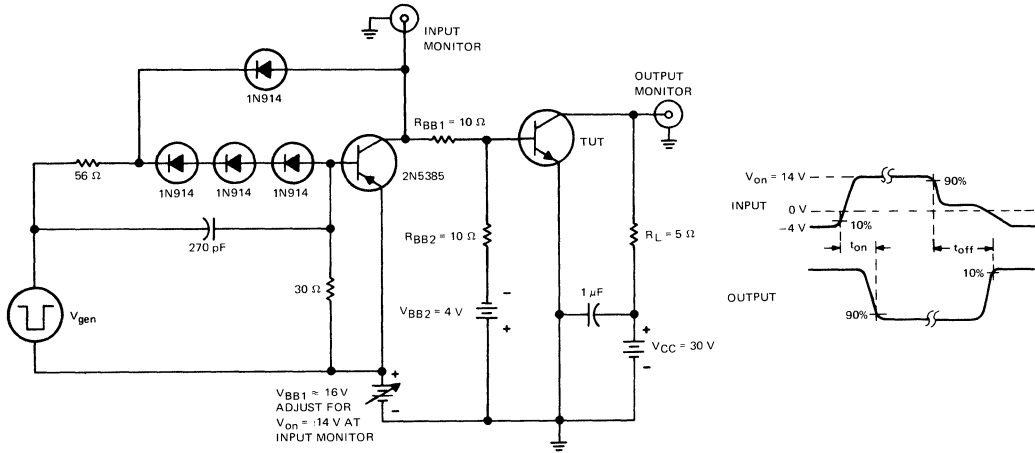
switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS†	TYP	UNIT
t_{on}	Turn-On Time	$I_C = 6 \text{ A}$, $I_{B(1)} = 0.6 \text{ A}$, $I_{B(2)} = -0.6 \text{ A}$,	0.6	μs
t_{off}	Turn-Off Time	$V_{BE(off)} = -4 \text{ V}$, $R_L = 5 \Omega$, See Figure 1	1	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPE TIP3055 N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

PARAMETER MEASUREMENT INFORMATION



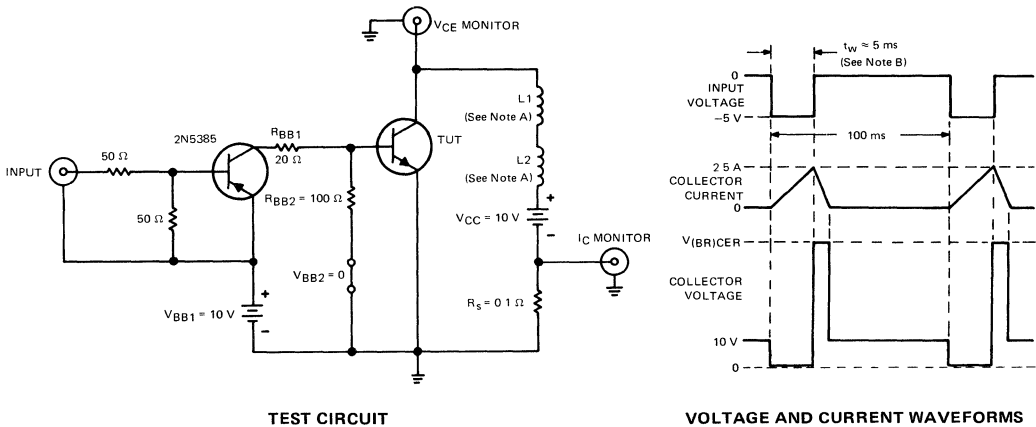
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES:**
- A. V_{gen} is a -30-V pulse (from 0 V) into a $50\text{-}\Omega$ termination.
 - B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $Z_{out} = 50\text{ }\Omega$, $t_w = 20\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 11.5\text{ pF}$.
 - D. Resistors must be noninductive types.
 - E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

- NOTES:**
- A. L1 and L2 are 10 mH , $0.11\text{ }\Omega$, Chicago Standard Transformer Corporation C-2688, or equivalent.
 - B. Input pulse width is increased until $I_{CM} = 2.5\text{ A}$.

FIGURE 2

TYPE TIP3055

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

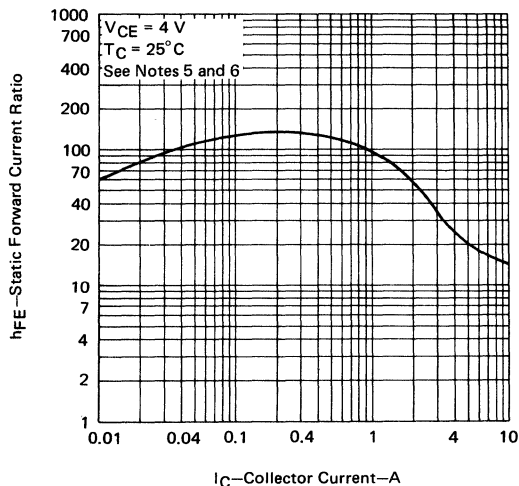


FIGURE 3

- NOTES: 5. These parameters must be measured using pulse techniques. $t_w = 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

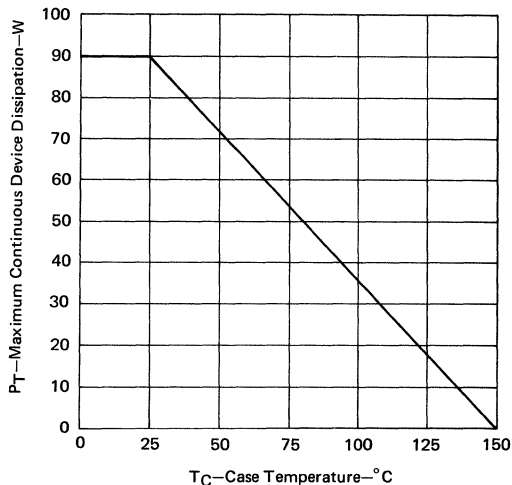


FIGURE 4

MAXIMUM SAFE OPERATING REGION

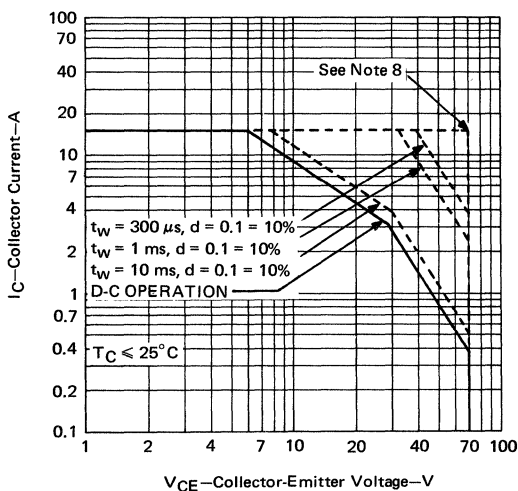


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

5

Germanium Power Data Sheets

TYPES 2N456A, 2N457A, 2N458A, 2N1021 AND 2N1022 P-N-P ALLOY -JUNCTION GERMANIUM POWER TRANSISTORS

CHOICE OF 40v, 60v, 80v, 100v, or 120v DEVICES

LOW I_{CO} HIGH BETA LOW R_{CS}

LOW THERMAL RESISTANCE

150 WATTS DISSIPATION

Designed specifically for High-Voltage Power Converters, High-Voltage Amplifiers and Switching Circuits. Featuring Low Distortion, Low Saturation Resistance and Fast Switching Times

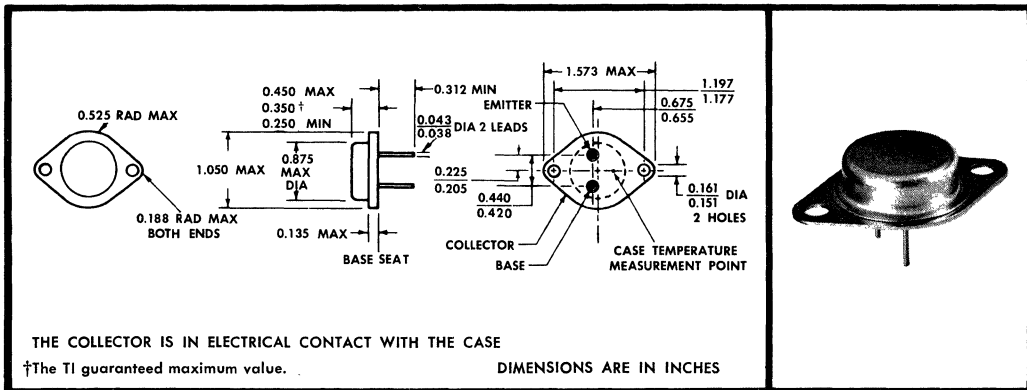
TYPES 2N456A, 2N457A, 2N1021, 2N1022
BULLETIN NO. DL-S-711419, MARCH 1961
REVISED SEPTEMBER 1971

mechanical data

The use of silver alloy to assemble the mounting base and the use of resistance welding to seal the can, provide a hermetically sealed enclosure. During the assembly process the absence of flux, combined with extreme cleanliness, prevents sealed-in contamination.

The mounting base provides an excellent heat path from the collector junction to a heat sink which must be in intimate contact to permit operation at maximum rated dissipation.

The transistors are in a JEDEC TO-3 case.



6

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N456A	2N457A	2N458A	2N1021	2N1022
Collector-Base Voltage	-40 v	-60 v	-80 v	-100 v	-120 v
Collector-Emitter Voltage (see Note 1)	-30 v	-40 v	-45 v	-50 v	-55 v
Emitter-Base Voltage	← -30 v →				
Collector Current	← -7 a →				
Base Current	← -3 a →				
Total Device Dissipation at (or below) 25°C Case Temperature (see Note 2)	← 150 w →				
Collector Junction Temperature	← 100°C →				
Storage Temperature Range	← -55°C to + 100°C →				

NOTES: 1. This value applies when the base-emitter diode is open circuited.
2. Derate linearly to + 100°C case temperature at the rate of 2w/°C.

TYPES 2N456A, 2N457A, 2N458A, 2N1021 AND 2N1022 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TYPE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CBO} Collector Reverse Current	2N456A	$V_{CB} = -40\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-1.0	-2.0	ma
		$V_{CB} = -20\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-0.2	-0.5	ma
		$V_{CB} = -40\text{ v}$ $I_E = 0, 71^\circ\text{C}$		-6.0	-10.0	ma
	2N457A	$V_{CB} = -60\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-1.0	-2.0	ma
		$V_{CB} = -30\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-0.2	-0.5	ma
		$V_{CB} = -60\text{ v}$ $I_E = 0, 71^\circ\text{C}$		-6.0	-10.0	ma
	2N458A	$V_{CB} = -80\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-1.0	-2.0	ma
		$V_{CB} = -40\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-0.2	-0.5	ma
		$V_{CB} = -80\text{ v}$ $I_E = 0, 71^\circ\text{C}$		-6.0	-10.0	ma
	2N1021	$V_{CB} = -100\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-1.0	-2.0	ma
		$V_{CB} = -50\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-0.2	-0.5	ma
		$V_{CB} = -100\text{ v}$ $I_E = 0, 71^\circ\text{C}$		-6.0	-10.0	ma
2N1022	$V_{CB} = -120\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-1.0	-2.0	ma	
	$V_{CB} = -60\text{ v}$ $I_E = 0, 25^\circ\text{C}$		-0.2	-0.5	ma	
	$V_{CB} = -120\text{ v}$ $I_E = 0, 71^\circ\text{C}$		-6.0	-10.0	ma	
I_{EBO} Emitter Reverse Current	All	$V_{EB} = -10\text{ v}$ $I_C = 0$		-0.2		ma
BV_{CBO} Collector-Base Breakdown Voltage	2N456A	$I_C = -2\text{ ma}$ $I_E = 0$	-40			v
	2N457A	$I_C = -2\text{ ma}$ $I_E = 0$	-60			v
	2N458A	$I_C = -2\text{ ma}$ $I_E = 0$	-80			v
	2N1021	$I_C = -2\text{ ma}$ $I_E = 0$	-100			v
	2N1022	$I_C = -2\text{ ma}$ $I_E = 0$	-120			v
BV_{CEO} Collector-Emitter Breakdown Voltage	2N456A	$I_C = -500\text{ ma}$ $I_B = 0$	-30	-40		v
	2N457A	$I_C = -500\text{ ma}$ $I_B = 0$	-40	-50		v
	2N458A	$I_C = -500\text{ ma}$ $I_B = 0$	-45	-55		v
	2N1021	$I_C = -500\text{ ma}$ $I_B = 0$	-50	-60		v
	2N1022	$I_C = -500\text{ ma}$ $I_B = 0$	-55	-60		v
BV_{CER} Collector-Emitter Breakdown Voltage	2N456A	$I_C = -200\text{ ma}$ $R_{BE} = 33\ \Omega$		-50		v
	2N457A	$I_C = -200\text{ ma}$ $R_{BE} = 33\ \Omega$		-60		v
	2N458A	$I_C = -200\text{ ma}$ $R_{BE} = 33\ \Omega$		-67		v
	2N1021	$I_C = -200\text{ ma}$ $R_{BE} = 33\ \Omega$		-73		v
	2N1022	$I_C = -200\text{ ma}$ $R_{BE} = 33\ \Omega$		-78		v
BV_{CES} Collector-Emitter Breakdown Voltage	2N456A	$I_C = -200\text{ ma}$ $V_{BE} = 0$	-50	-60		v
	2N457A	$I_C = -200\text{ ma}$ $V_{BE} = 0$	-60	-70		v
	2N458A	$I_C = -200\text{ ma}$ $V_{BE} = 0$	-65	-78		v
	2N1021	$I_C = -200\text{ ma}$ $V_{BE} = 0$	-70	-85		v
	2N1022	$I_C = -200\text{ ma}$ $V_{BE} = 0$	-75	-90		v
BV_{EBO} Emitter-Base Breakdown Voltage	All	$I_E = -2\text{ ma}$ $I_C = 0$	-30			v
h_{FE} DC Forward Current Transfer Ratio	All	$V_{CE} = -1.5\text{ v}$ $I_C = -7\text{ a}$	22	47		
		$V_{CE} = -1.5\text{ v}$ $I_C = -5\text{ a}$	30	60	90	
		$V_{CE} = -1.5\text{ v}$ $I_C = -3\text{ a}$	35	82		
		$V_{CE} = -1.5\text{ v}$ $I_C = -1\text{ a}$	40	120		

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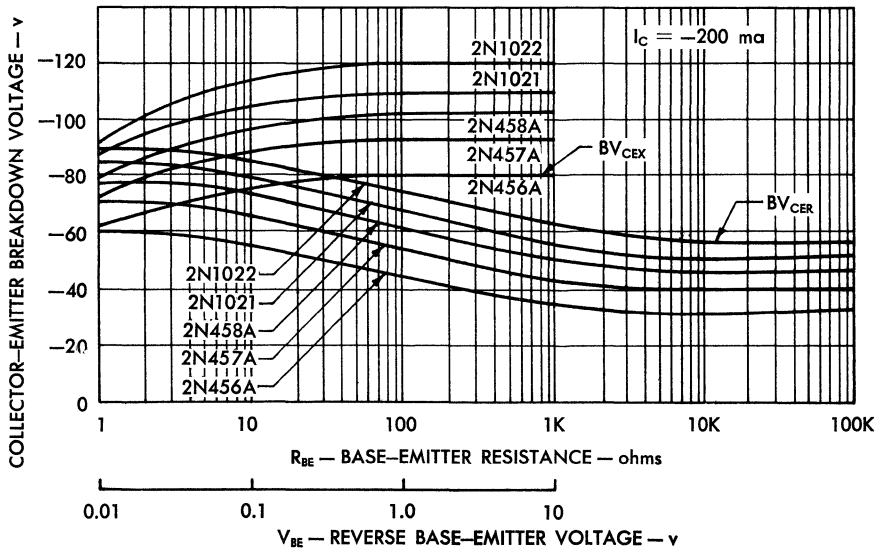
TYPES 2N456A, 2N457A, 2N458A, 2N1021 AND 2N1022 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TYPE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BE} Base-Emitter Voltage	All	$V_{CE} = -1.5 \text{ v}$ $I_C = -7 \text{ a}$		-1.2		v
		$V_{CE} = -1.5 \text{ v}$ $I_C = -5 \text{ a}$		-0.9	-1.5	v
		$V_{CE} = -1.5 \text{ v}$ $I_C = -3 \text{ a}$		-0.6		v
		$V_{CE} = -1.5 \text{ v}$ $I_C = -1 \text{ a}$		-0.35		v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	All	$I_B = -700 \text{ ma}$ $I_C = -7 \text{ a}$		-0.3		v
		$I_B = -500 \text{ ma}$ $I_C = -5 \text{ a}$		-0.2	-0.5	v
		$I_B = -300 \text{ ma}$ $I_C = -3 \text{ a}$		-0.1		v
		$I_B = -100 \text{ ma}$ $I_C = -1 \text{ a}$		-0.05		v
Y_{FE} DC Common-Emitter Forward Transfer Admittance	All	$V_{CE} = -1.5 \text{ v}$ $I_C = -7 \text{ a}$		5.7		mhos
		$V_{CE} = -1.5 \text{ v}$ $I_C = -5 \text{ a}$	3.3	5.5		mhos
		$V_{CE} = -1.5 \text{ v}$ $I_C = -3 \text{ a}$		4.8		mhos
		$V_{CE} = -1.5 \text{ v}$ $I_C = -1 \text{ a}$		3.0		mhos
h_{IE} DC Common-Emitter Input Impedance	All	$V_{CE} = -1.5 \text{ v}$ $I_C = -7 \text{ a}$		8		ohms
		$V_{CE} = -1.5 \text{ v}$ $I_C = -5 \text{ a}$		11	28	ohms
		$V_{CE} = -1.5 \text{ v}$ $I_C = -3 \text{ a}$		16		ohms
		$V_{CE} = -1.5 \text{ v}$ $I_C = -1 \text{ a}$		42		ohms
f_T Internal Cutoff Frequency (where $ h_{fe} = 1$)	All	$V_{CE} = -2 \text{ v}$ $I_C = -1 \text{ a}$	200	430		kc

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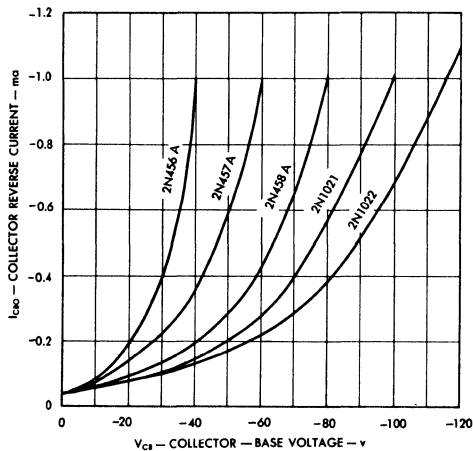
TYPICAL COMMON-EMITTER BREAKDOWN VOLTAGE CHARACTERISTICS



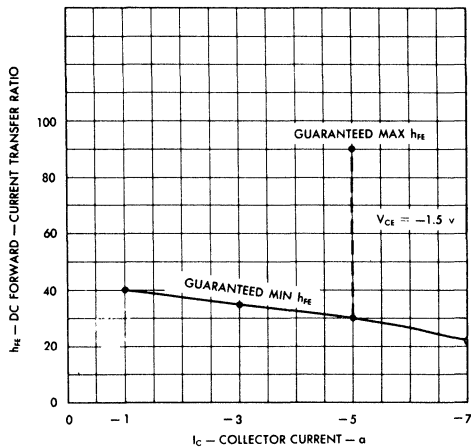
TYPES 2N456A, 2N457A, 2N458A, 2N1021 AND 2N1022 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

TYPICAL CHARACTERISTICS

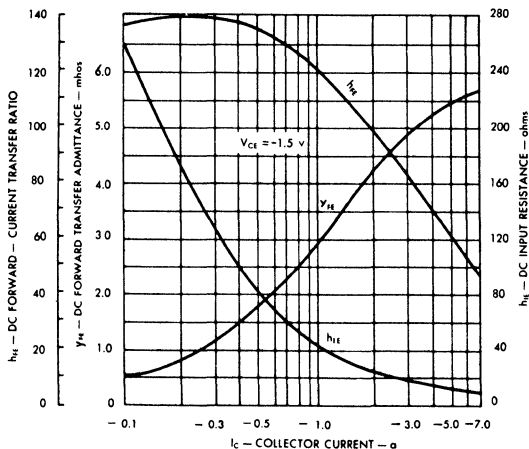
COLLECTOR REVERSE-CURRENT CHARACTERISTICS



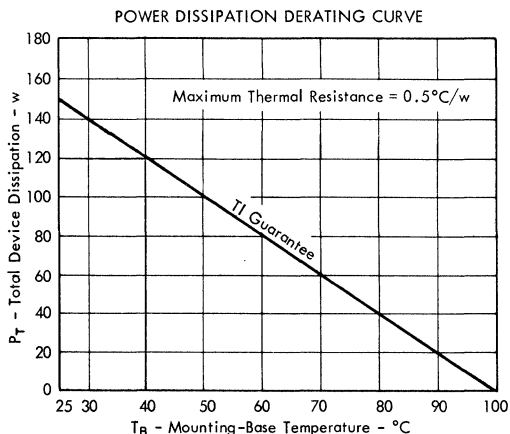
GUARANTEED COMMON-EMITTER DC FORWARD-CURRENT TRANSFER RATIO VS COLLECTOR CURRENT



COMMON-EMITTER DC FORWARD CURRENT TRANSFER RATIO, DC INPUT RESISTANCE, AND DC FORWARD TRANSFER ADMITTANCE VS COLLECTOR CURRENT



DISSIPATION DERATING



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TYPES 2N456B, 2N457B, 2N458B, 2N1021A AND 2N1022A P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

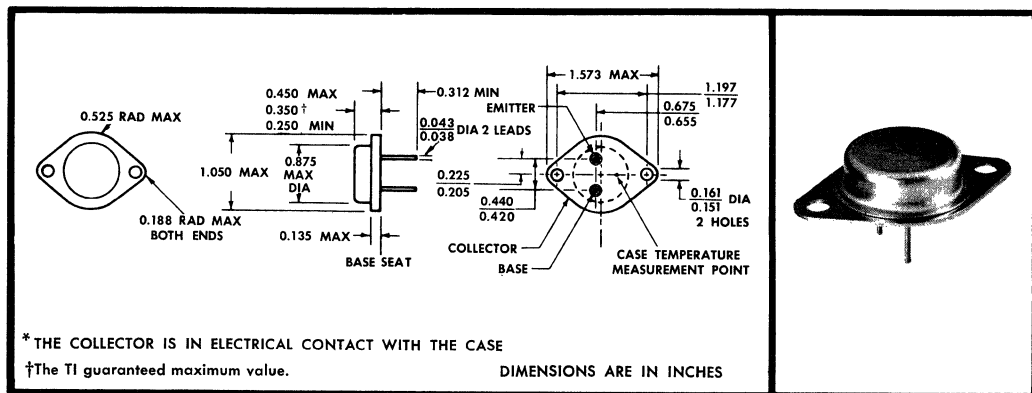
High-Power Transistors for Military and Industrial Applications

TYPES 2N456B, 2N457B, 2N458B, 2N1021A, AND 2N1022A
BULLETIN NO. DL-5 633454, FEBRUARY 1963

mechanical data

The use of silver alloy to assemble the mounting base and the use of resistance welding to seal the can, provide a hermetically sealed enclosure. During the assembly process the absence of flux, combined with extreme cleanliness, prevents sealed-in contamination. The mounting base provides an excellent heat path from the collector junction to a heat sink which must be in intimate contact to permit operation at maximum rated dissipation.

*The transistors are in a JEDEC TO-3 case.



6

* absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N456B	2N457B	2N458B	2N1021A	2N1022A
Collector-Base Voltage	40 v	60 v	80 v	100 v	120 v
Collector-Emitter Voltage (see Note 1)	30 v	40 v	45 v	50 v	55 v
Emitter-Base Voltage	←		30 v	→	
Collector Current	←		7 a	→	
Base Current	←		3 a	→	
Total Device Dissipation at (or below) 25°C Case Temperature (see Note 2)	←		150 w	→	
Collector Junction Temperature	←		100°C	→	
Storage Temperature Range	←		-55°C to +100°C	→	

*Indicates JEDEC registered data

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to +100°C case temperature at the rate of 2w/°C.

TYPES 2N456B, 2N457B, 2N458B, 2N1021A AND 2N1022A P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = -2 \text{ ma}$, $I_E = 0$	2N456B 2N457B 2N458B 2N1021A 2N1022A	-40 -60 -80 -100 -120			v
BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = -500 \text{ ma}$, $I_B = 0$ (see Note 3)	2N456B 2N457B 2N458B 2N1021A 2N1022A	-30* -40* -45* -50* -55*			v
BV_{CES} Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ ma}$, $V_{BE} = 0$ (see Note 3)	2N456B 2N457B 2N458B 2N1021A 2N1022A	-50* -60* -65* -70* -75*			v
BV_{CEX} Collector-Emitter Breakdown Voltage	$I_C = -2 \text{ ma}$, $V_{BE} = +0.2 \text{ v}$	2N456B 2N457B 2N458B 2N1021A 2N1022A	-40* -60* -80* -100* -120*			v
BV_{EBO} Emitter-Base Breakdown Voltage	$I_E = -2 \text{ ma}$, $I_C = 0$	All	-30			v
I_{CBO} Collector Cutoff Current	$V_{CB} = -20 \text{ v}$, $I_E = 0$ $V_{CB} = -40 \text{ v}$, $I_E = 0$ $V_{CB} = -40 \text{ v}$, $I_E = 0$, $T_C = 70^\circ\text{C}$	2N456B			-0.5* -2.0* -7.0*	ma
	$V_{CB} = -30 \text{ v}$, $I_E = 0$ $V_{CB} = -60 \text{ v}$, $I_E = 0$ $V_{CB} = -60 \text{ v}$, $I_E = 0$, $T_C = 70^\circ\text{C}$	2N457B			-0.5* -2.0* -7.0*	ma
	$V_{CB} = -40 \text{ v}$, $I_E = 0$ $V_{CB} = -80 \text{ v}$, $I_E = 0$ $V_{CB} = -80 \text{ v}$, $I_E = 0$, $T_C = 70^\circ\text{C}$	2N458B			-0.5* -2.0* -7.0*	ma
	$V_{CB} = -50 \text{ v}$, $I_E = 0$ $V_{CB} = -100 \text{ v}$, $I_E = 0$ $V_{CB} = -100 \text{ v}$, $I_E = 0$, $T_C = 70^\circ\text{C}$	2N1021A			-0.5* -2.0* -7.0*	ma
	$V_{CB} = -60 \text{ v}$, $I_E = 0$ $V_{CB} = -120 \text{ v}$, $I_E = 0$ $V_{CB} = -120 \text{ v}$, $I_E = 0$, $T_C = 70^\circ\text{C}$	2N1022A			-0.5* -2.0* -7.0*	ma
	I_{EBO} Emitter Cutoff Current	$V_{EB} = -30 \text{ v}$, $I_C = 0$	All			-2.0*
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ v}$, $I_C = -7 \text{ a}$ $V_{CE} = -1.5 \text{ v}$, $I_C = -5 \text{ a}$ $V_{CE} = -1.5 \text{ v}$, $I_C = -3 \text{ a}$ $V_{CE} = -1.5 \text{ v}$, $I_C = -1 \text{ a}$	All	22* 30* 35* 40*	45 55 60 100	90*	—
V_{BE} Base-Emitter Voltage	$V_{CE} = -1.5 \text{ v}$, $I_C = -7 \text{ a}$ $V_{CE} = -1.5 \text{ v}$, $I_C = -5 \text{ a}$ $V_{CE} = -1.5 \text{ v}$, $I_C = -3 \text{ a}$ $V_{CE} = -1.5 \text{ v}$, $I_C = -1 \text{ a}$	All		-1.2 -0.9 -0.7 -0.4	-1.5*	v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -700 \text{ ma}$, $I_C = -7 \text{ a}$ $I_B = -500 \text{ ma}$, $I_C = -5 \text{ a}$ $I_B = -300 \text{ ma}$, $I_C = -3 \text{ a}$ $I_B = -100 \text{ ma}$, $I_C = -1 \text{ a}$	All		-0.3 -0.2 -0.1 -.05	-0.5*	v
f_T Transition Frequency	$V_{CE} = -2 \text{ v}$, $I_C = -1 \text{ a}$ (see Note 4)	All	200*			kc

*Indicates JEDEC registered data.

NOTES: 3. If the transistor is tested without a heat sink, perform this test with a 100 msec current pulse and a duty cycle less than 2%.

4. To obtain f_T , the $|h_{fe}|$ response with frequency is extrapolated at the rate of -6 db/octave from $f = 100 \text{ kc}$ to the frequency at which $|h_{fe}| = 1$.

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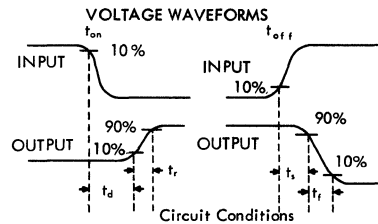
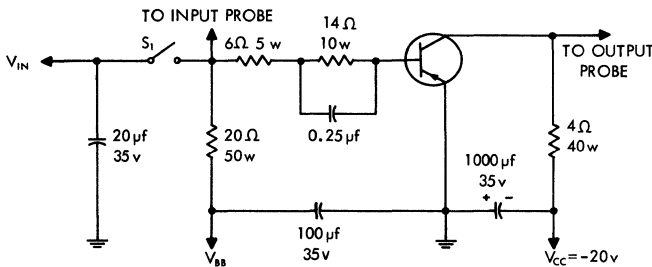
TYPES 2N456B, 2N457B, 2N458B, 2N1021A AND 2N1022A P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	2N456B, 2N457B, 2N458B, 2N1021A, 2N1022A			UNIT
		MIN	TYP	MAX	
t_d Delay Time	$I_C = -5 \text{ a}$, $I_{B(1)} = -0.5 \text{ a}$, $V_{BE(off)} = 9 \text{ v}$ $R_L = 4 \Omega$ (See Figure Below)		0.7		μSEC
t_r Rise Time			5		μSEC
t_s Storage Time			2		μSEC
t_f Fall Time			15		μSEC
t_T Total Switching Time			22.7		μSEC

†Voltage and current values shown are nominal; exact values vary slightly with device parameters.

PARAMETER MEASUREMENT INFORMATION



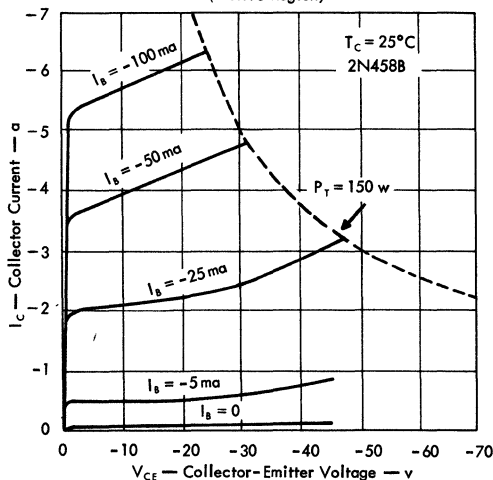
Test	V_{BB}	V_{IN}
Turn-On (t_d, t_r)	+9 v	-11 v
Turn-Off (t_s, t_f)	-21 v	+9 v

NOTES:

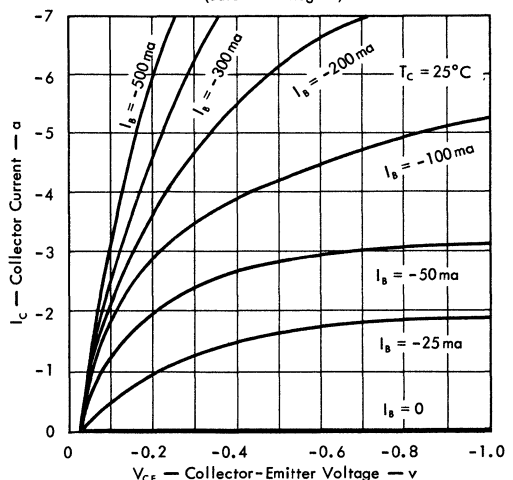
- Relay S_1 has mercury wetted contacts and provides rise times less than 1/10 of the switching times measured.
- Duty cycle of S_1 is such that the transistor is ON 4 msec and OFF 12 msec in both turn-on and turn-off tests.
- Waveforms monitored on scope with following characteristics: (a) Rise time 14 nsec max, (b) Input capacitance 11.5 pf max, (c) Input resistance 10 megohms min.
- All resistors 5% tolerance, noninductive type.

TYPICAL CHARACTERISTICS

COMMON-EMITTER COLLECTOR
CHARACTERISTICS
(Active Region)

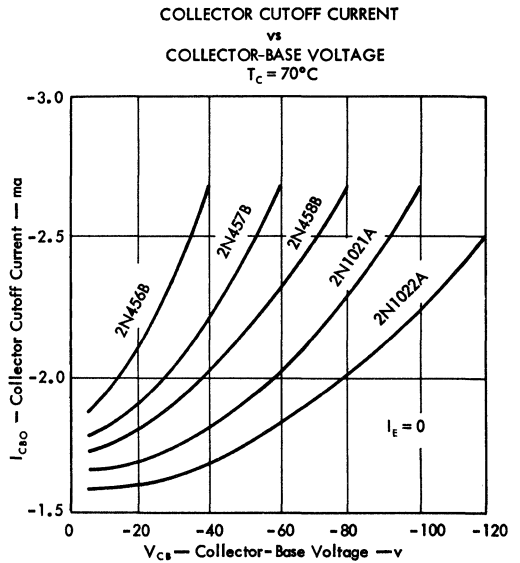
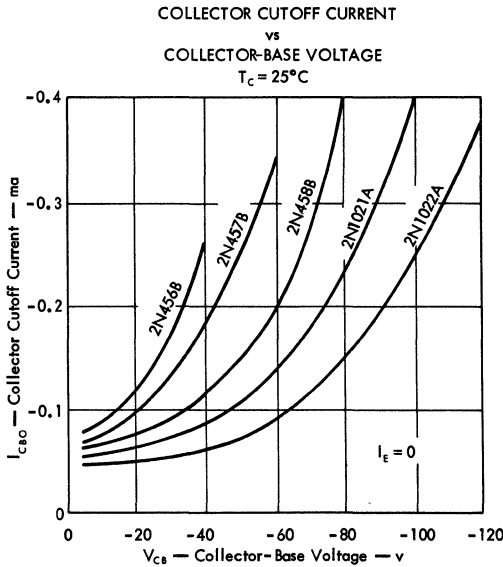
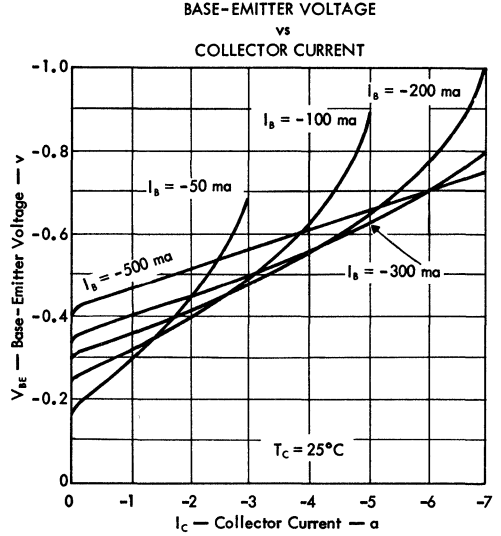
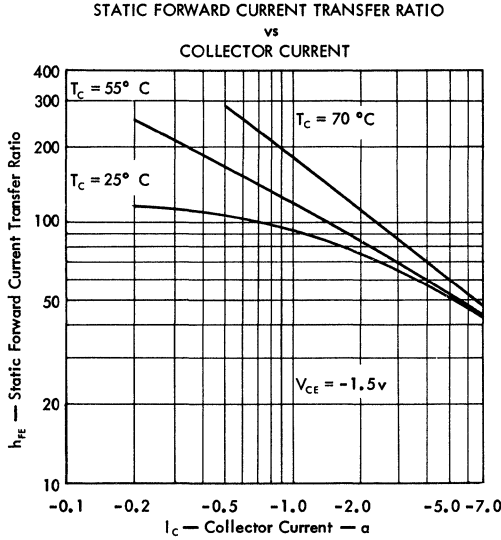


COMMON-EMITTER COLLECTOR
CHARACTERISTICS
(Saturation Region)



TYPES 2N456B, 2N457B, 2N458B, 2N1021A AND 2N1022A P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

TYPICAL CHARACTERISTICS



TYPES 2N456B, 2N457B, 2N458B, 2N1021A AND 2N1022A P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

THERMAL CHARACTERISTICS

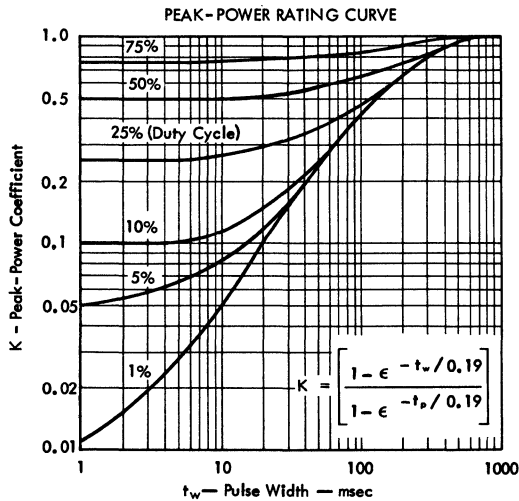
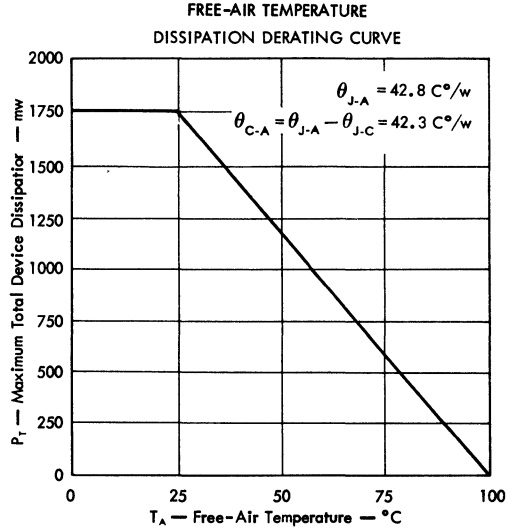
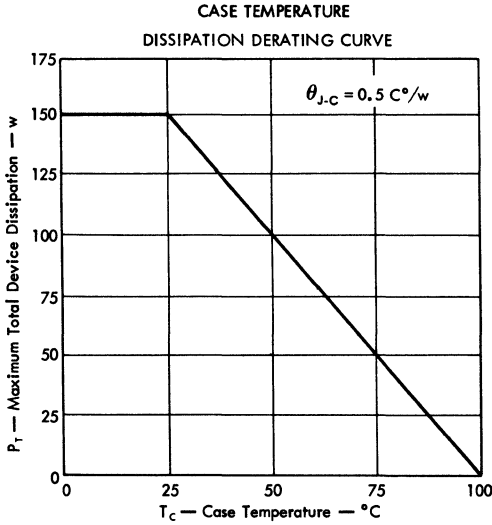


Figure 1

TYPES 2N456B, 2N457B, 2N458B, 2N1021A AND 2N1022A P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

THERMAL INFORMATION

TABLE I

HEAT SINK		$\dagger \theta_{HS-A}$
Type	Dimensions	
Bright Copper	4" x 4" x 1/8"	3.8 C°/w
	6" x 6" x 1/8"	2.2 C°/w
	8" x 8" x 1/8"	1.8 C°/w
	10" x 10" x 1/8"	1.4 C°/w
Bright Aluminum	4" x 4" x 1/8"	6.5 C°/w
	6" x 6" x 1/8"	4.5 C°/w
	8" x 8" x 1/8"	3.5 C°/w
	10" x 10" x 1/8"	2.8 C°/w
Delbert Blinn #113 or Modine 1E1155B, Unfinished (or Equivalents)		3.7 C°/w
Delbert Blinn #113 or Modine 1E1155B, Black Anodized (or Equivalents)		3.2 C°/w

$\dagger \theta_{HS-A}$ are typical values based on convection cooling; plates and fins mounted in vertical position.

\ddagger All transistors mounted in the center of the heat sink with two 6-32 screws at 6 inch-pounds of torque.

TABLE II

DEFINITION OF TERMS

Symbol	Definition	Unit	Value
P_T	Average Power Dissipation	w	
P_T	Peak Power Dissipation	w	
θ_{J-C}	Junction-to-Case Thermal Resistance	C°/w	0.5
θ_{J-A}	Junction-to-Ambient Thermal Resistance	C°/w	42.8
θ_{C-A}	Case-to-Ambient Thermal Resistance	C°/w	42.3
$\ddagger \theta_{C-HS}$	Case-to-Heat Sink Thermal Resistance — Typical w/o DC-11 Grease	C°/w	0.65
	Typical with DC-11 Grease		0.45
θ_{HS-A}	Heat-Sink Thermal Resistance	C°/w	^{see} Table I
T_A	Ambient Temperature	C°	
T_J	Average Junction Temperature	C°	
T_j	Peak Junction Temperature	C°	
T_c	Case Temperature	C°	
K	Peak-Power Coefficient		^{see} Fig. 1
t_w	Pulse Width	msec	
t_p	Pulse Period	msec	
d	Duty Cycle (t_w/t_p)		

The PEAK-POWER RATING CURVE shows the ratio of maximum instantaneous junction-to-case temperature rise at any pulse width and duty cycle to the rise which occurs at 100% duty cycle. Use of this curve is best explained by the equations and examples below. See Table II for a definition of terms.

Equation No. 1 — Application: D.C. power dissipation, heat sink used.

$$P_T = \frac{T_J - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}}$$

Equation No. 2 — Application: D.C. power dissipation, no heat sink used.

$$P_T = \frac{T_J - T_A}{\theta_{J-A}}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_T = \frac{T_j - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_T = \frac{T_j - T_A}{d \theta_{C-A} + K \theta_{J-C}}$$

Example A — Find $P_{T(max)}$

OPERATING CONDITIONS:

Heat Sink = 4" x 4" x 1/8" copper, $\theta_{HS-A} = 3.8$ C°/w

$T_{J(max)}$ (design limit) = 100 C°

$T_A = 30$ C°

d = 100% (1.0)

with DC-11 grease, $\theta_{C-HS} = 0.45$ C°/w

SOLUTION:

By use of equation No. 1

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}}$$

$$P_{T(max)} = \frac{100 - 30}{0.5 + 0.45 + 3.8} = 14.7 \text{ w}$$

Example B — Find $p_{T(max)}$

OPERATING CONDITIONS:

Heat Sink = 8" x 8" x 1/8" copper,

$\theta_{HS-A} = 1.8$ C°/w

with DC-11 grease, $\theta_{C-HS} = 0.45$ C°/w

$T_{j(max)}$ (design limit) = 100 C°

$T_A = 35$ C°

d = 5% (0.05)

$t_w = 40$ msec

SOLUTION:

From Figure 1, Peak-Power Coefficient,

K = 0.2, and by use of equation No. 3

$$P_{T(max)} = \frac{T_{j(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K \theta_{J-C}}$$

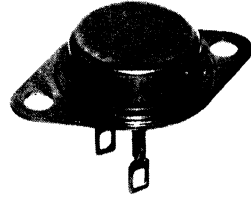
$$P_{T(max)} = \frac{100 - 35}{0.05(0.45 + 1.8) + 0.2(0.5)} = 306 \text{ w}$$

TYPES 2N511, 2N511A, AND 2N511B P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

TYPES 2N511, 2N511A, and 2N511B
BULLETIN NO. DL-5 611471, MARCH 1961

40, 60 or 80 VOLTS
10-AMP COLLECTOR CURRENT
150 -WATT DISSIPATION
LOW I_{CO} LOW V_{BE}
LOW THERMAL RESISTANCE

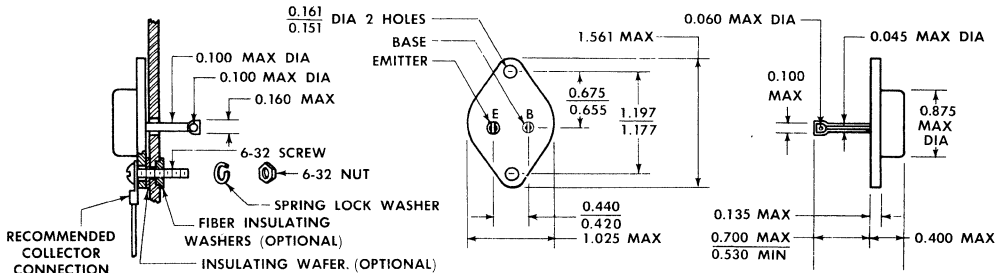
for
HIGH-POWER CONVERSION • HIGH-CURRENT SWITCHING
AUDIO AMPLIFIER OUTPUT STAGES



mechanical data

The use of high-temperature silver solder to assemble the mounting base and the use of projection weld to seal the can provide a hermetically sealed enclosure which can withstand up to 300 psi. During the assembly process the absence of flux and soft solder, combined with extra cleanliness, prevents sealed-in contamination.

The mounting base provides an excellent heat path from the collector junction, which is electrically attached to the mounting base, to a heat sink which must be tightly attached to permit operation at maximum rated dissipation. The approximate weight of the unit is 17.6 grams.



COLLECTOR IS COMMON TO CASE

absolute maximum ratings for all devices at 25°C mounting-base temperature

(unless otherwise noted)*

Collector Current	25a
Base Current	5a
Total Device Dissipation**	150w
Collector Junction Temperature	100°C
Storage Temperature Range	-55 to +100°C
Thermal Resistance	0.5 °C/w

* Maximum voltage ratings not specified because exceeding breakdown voltages will not permanently damage transistor characteristics so long as other maximum ratings are not exceeded.

**Derate at 2.0 w/°C.

6

TYPES 2N511, 2N511A, AND 2N511B

P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

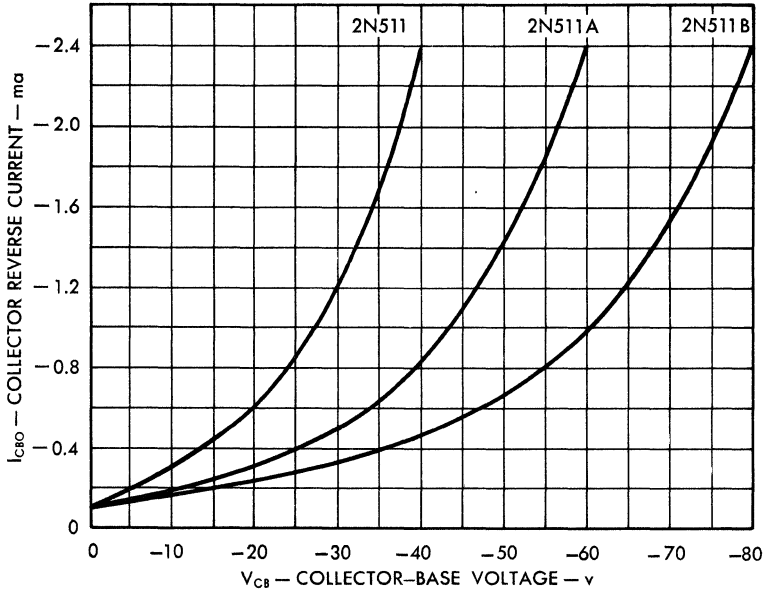
electrical characteristics at 25°C mounting-base temperature (unless otherwise noted)

PARAMETER	TYPE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CBO} Collector Reverse-Current, 71°	2N511	$V_{CB} = -40\text{ v}$ $I_E = 0$			-15.0	ma
	2N511A	$V_{CB} = -60\text{ v}$ $I_E = 0$			-15.0	ma
	2N511B	$V_{CB} = -80\text{ v}$ $I_E = 0$			-15.0	ma
I_{CBO} Collector Reverse-Current	2N511	$V_{CB} = -40\text{ v}$ $I_E = 0$		-2.4	-5.0	ma
		$V_{CB} = -20\text{ v}$ $I_E = 0$		-0.6	-2.0	ma
	2N511A	$V_{CB} = -60\text{ v}$ $I_E = 0$		-2.4	-5.0	ma
		$V_{CB} = -30\text{ v}$ $I_E = 0$		-0.5	-2.0	ma
	2N511B	$V_{CB} = -80\text{ v}$ $I_E = 0$		-2.4	-5.0	ma
		$V_{CB} = -40\text{ v}$ $I_E = 0$		-0.5	-2.0	ma
I_{EBO} Emitter Reverse-Current	All	$V_{EB} = -30\text{ v}$ $I_C = 0$		-1.5	-5.0	ma
	All	$V_{EB} = -15\text{ v}$ $I_C = 0$		-0.5		ma
BV_{CBO} Collector-Base Breakdown Voltage	2N511	$I_C = -5\text{ ma}$ $I_E = 0$	-40			v
	2N511A		-60			v
	2N511B		-80			v
BV_{CEO} Collector-Emitter Breakdown Voltage	2N511	$I_C = -500\text{ ma}$ $I_B = 0$	-30	-40		v
	2N511A		-40	-50		v
	2N511B		-45	-55		v
BV_{CES} Collector-Emitter Breakdown Voltage	2N511	$I_C = -300\text{ ma}$ $V_{BE} = 0$	-50	-60		v
	2N511A		-60	-70		v
	2N511B		-65	-80		v
BV_{CER} Collector-Emitter Breakdown Voltage	2N511	$I_C = -300\text{ ma}$ $R_{BE} = 100\text{ ohms}$		-45		v
	2N511A			-55		v
	2N511B			-65		v
BV_{EBO} Emitter-Base Breakdown Voltage	All	$I_E = -5\text{ ma}$ $I_C = 0$	-30	-60		v
h_{FE} DC Forward-Current Transfer Ratio	All	$V_{CE} = -2\text{ v}$ $I_C = -10\text{ a}$	20	25	60	—
V_{BE} Base-Emitter Voltage	All	$V_{CE} = -2\text{ v}$ $I_C = -10\text{ a}$			-2.0	v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	All	$I_B = -1.5\text{ a}$ $I_C = -10\text{ a}$		-0.25	-0.5	v
y_{FE} DC Common-Emitter Forward Transfer Admittance	All	$V_{CE} = -2\text{ v}$ $I_C = -10\text{ a}$	5			mhos
f_T Internal Cutoff Frequency (where $ h_{ie} = 1$)	All	$V_{CE} = -2\text{ v}$ $I_C = -1\text{ a}$		260		kc

TYPES 2N511, 2N511A, AND 2N511B P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

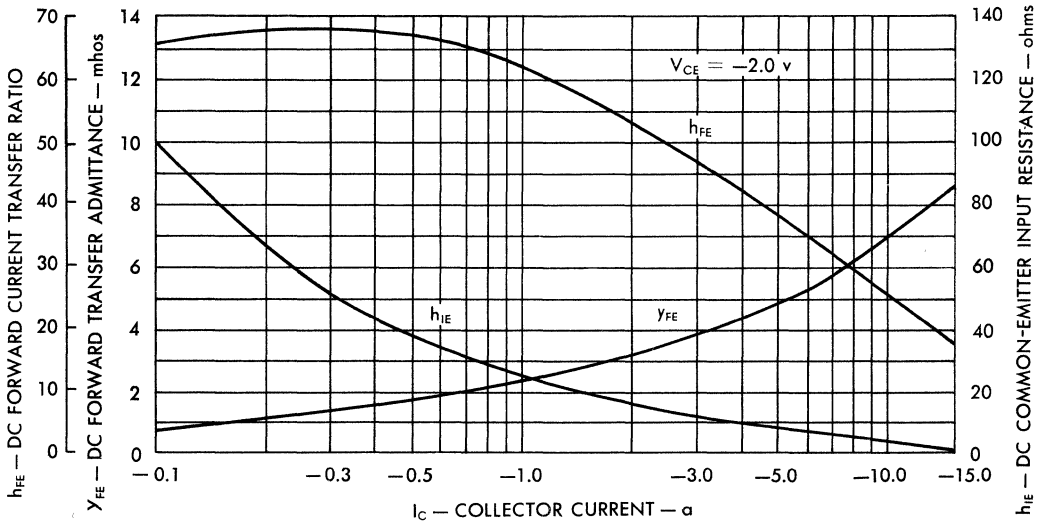
TYPICAL CHARACTERISTICS

COLLECTOR REVERSE-CURRENT CHARACTERISTICS



6

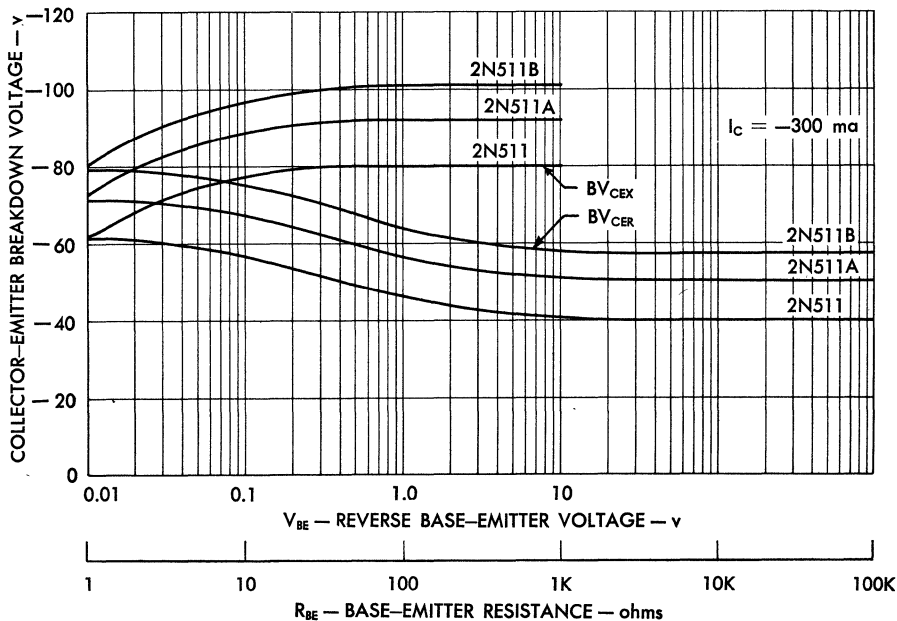
**COMMON-EMITTER DC FORWARD-CURRENT TRANSFER RATIO
DC FORWARD TRANSFER ADMITTANCE AND DC INPUT RESISTANCE
VS COLLECTOR CURRENT**



TYPES 2N511, 2N511A, AND 2N511B P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

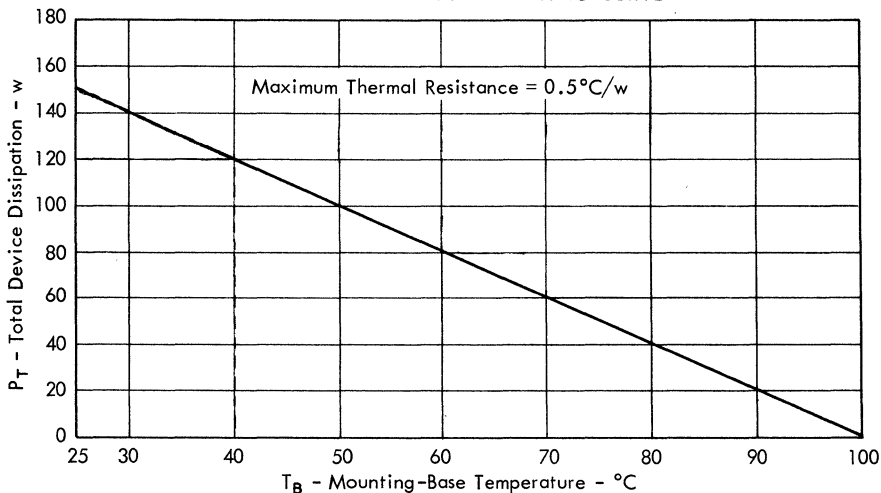
TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER BREAKDOWN VOLTAGE CHARACTERISTICS



THERMAL INFORMATION

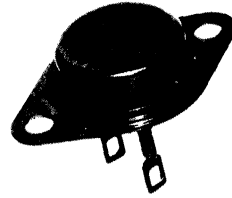
POWER DISSIPATION DERATING CURVE



TYPES 2N512, 2N512A, AND 2N512B P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

40, 60, or 80 VOLTS
15-Amp Collector Current
150-Watt Dissipation
LOW I_{CO} LOW V_{BE}
LOW THERMAL RESISTANCE
for

HIGH-POWER CONVERSION • HIGH-CURRENT SWITCHING
AUDIO AMPLIFIER OUTPUT STAGES

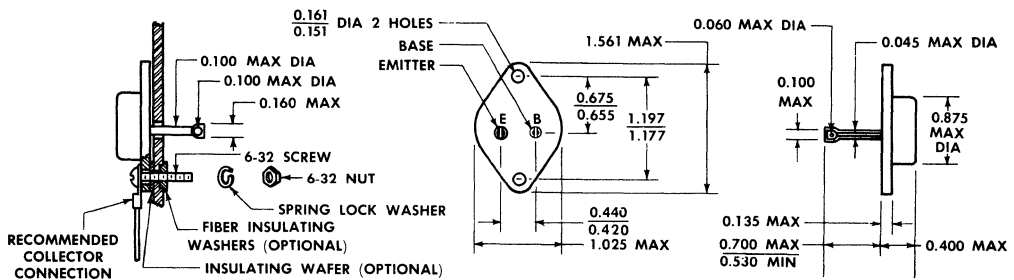


TYPES 2N512, 2N512A, and 2N512B
 BULLETIN NO. DL-5 611472, MARCH 1961

mechanical data

The use of high-temperature silver solder to assemble the mounting base and the use of projection weld to seal the can provide a hermetically sealed enclosure which can withstand up to 300 psi. During the assembly process the absence of flux and soft solder, combined with extra cleanliness, prevents sealed-in contamination.

The mounting base provides an excellent heat path from the collector junction, which is electrically attached to the mounting base, to a heat sink which must be tightly attached to permit operation at maximum rated dissipation. The approximate weight of the unit is 17.6 grams.



COLLECTOR IS COMMON TO CASE

absolute maximum ratings for all devices at 25°C mounting-base temperature

	(unless otherwise noted)*
Collector Current	25a
Base Current	5a
Total Device Dissipation**	150w
Collector Junction Temperature	100°C
Storage Temperature Range	-55 to +100°C
Thermal Resistance	0.5°C/w

*Maximum voltage ratings not specified because exceeding breakdown voltages will not permanently damage transistor characteristics so long as other maximum ratings are not exceeded.

**Derate at 2.0 w/°C.

6

TYPES 2N512, 2N512A, AND 2N512B

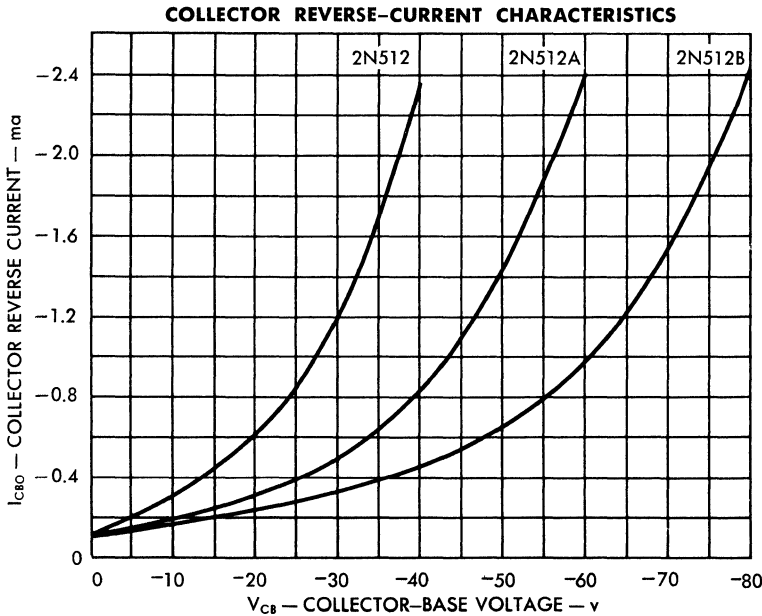
P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

electrical characteristics at 25°C mounting-base temperature (unless otherwise noted)

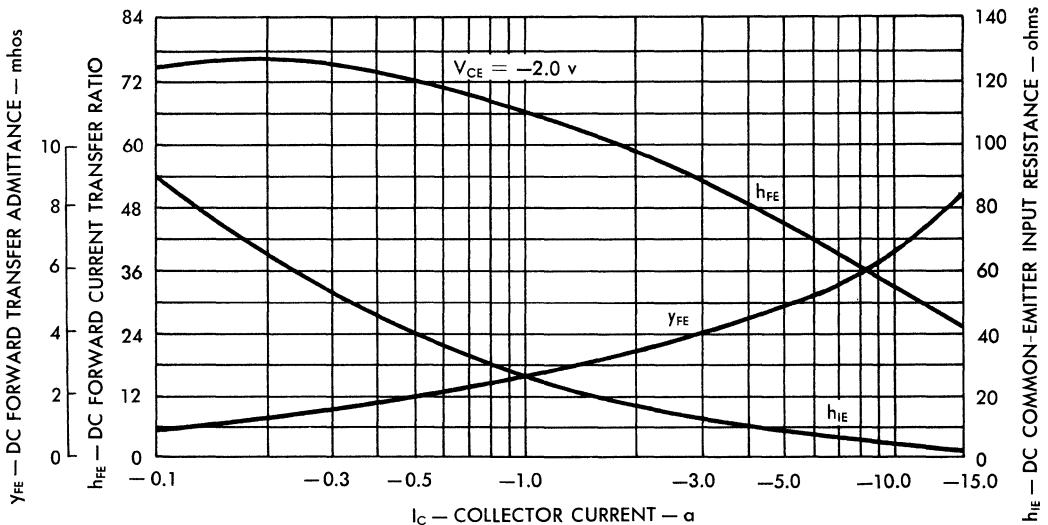
PARAMETER	TYPE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CBO} Collector Reverse-Current, 71°	2N512	$V_{CB} = -40\text{ v}$ $I_E = 0$			-15.0	ma
	2N512A	$V_{CB} = -60\text{ v}$ $I_E = 0$			-15.0	ma
	2N512B	$V_{CB} = -80\text{ v}$ $I_E = 0$			-15.0	ma
I_{CBO} Collector Reverse-Current	2N512	$V_{CB} = -40\text{ v}$ $I_E = 0$		-2.4	-5.0	ma
		$V_{CB} = -20\text{ v}$ $I_E = 0$		-0.6	-2.0	ma
	2N512A	$V_{CB} = -60\text{ v}$ $I_E = 0$		-2.4	-5.0	ma
		$V_{CB} = -30\text{ v}$ $I_E = 0$		-0.6	-2.0	ma
	2N512B	$V_{CB} = -80\text{ v}$ $I_E = 0$		-2.4	-5.0	ma
		$V_{CB} = -40\text{ v}$ $I_E = 0$		-0.6	-2.0	ma
I_{EBO} Emitter Reverse-Current	All	$V_{EB} = -30\text{ v}$ $I_C = 0$		-1.5	-5.0	ma
	All	$V_{EB} = -15\text{ v}$ $I_C = 0$		-0.5		ma
BV_{CBO} Collector-Base Breakdown Voltage	2N512	$I_C = -5\text{ ma}$ $I_E = 0$	-40			v
	2N512A		-60			v
	2N512B		-80			v
BV_{CEO} Collector-Emitter Breakdown Voltage	2N512	$I_C = -500\text{ ma}$ $I_B = 0$	-30	-40		v
	2N512A		-40	-50		v
	2N512B		-45	-55		v
BV_{CES} Collector-Emitter Breakdown Voltage	2N512	$I_C = -300\text{ ma}$ $V_{BE} = 0$	-50	-60		v
	2N512A		-60	-70		v
	2N512B		-65	-80		v
BV_{CER} Collector-Emitter Breakdown Voltage	2N512	$I_C = -300\text{ ma}$ $R_{BE} = 100\text{ ohms}$		-45		v
	2N512A			-55		v
	2N512B			-65		v
BV_{EBO} Emitter-Base Breakdown Voltage	All	$I_E = -5\text{ ma}$ $I_C = 0$	-30	-60		v
h_{FE} DC Forward Current Transfer Ratio	All	$V_{CE} = -2\text{ v}$ $I_C = -15\text{ a}$	20		60	—
V_{BE} Base-Emitter Voltage	All	$V_{CE} = -2\text{ v}$ $I_C = -15\text{ a}$			-2.0	v
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	All	$I_B = -2.25\text{ a}$ $I_C = -15\text{ a}$		-0.5	-1.0	v
γ_{FE} DC Common-Emitter Forward Transfer Admittance	All	$V_{CE} = -2\text{ v}$ $I_C = -15\text{ a}$	7.5			mhos
f_T Internal Cutoff Frequency (where $ h_{ie} = 1$)	All	$V_{CE} = -2\text{ v}$ $I_C = -1\text{ a}$		280		kc

TYPES 2N512, 2N512A, AND 2N512B P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

TYPICAL CHARACTERISTICS



**COMMON-EMITTER DC FORWARD-CURRENT TRANSFER RATIO,
DC FORWARD TRANSFER ADMITTANCE AND DC INPUT RESISTANCE
VS COLLECTOR CURRENT**



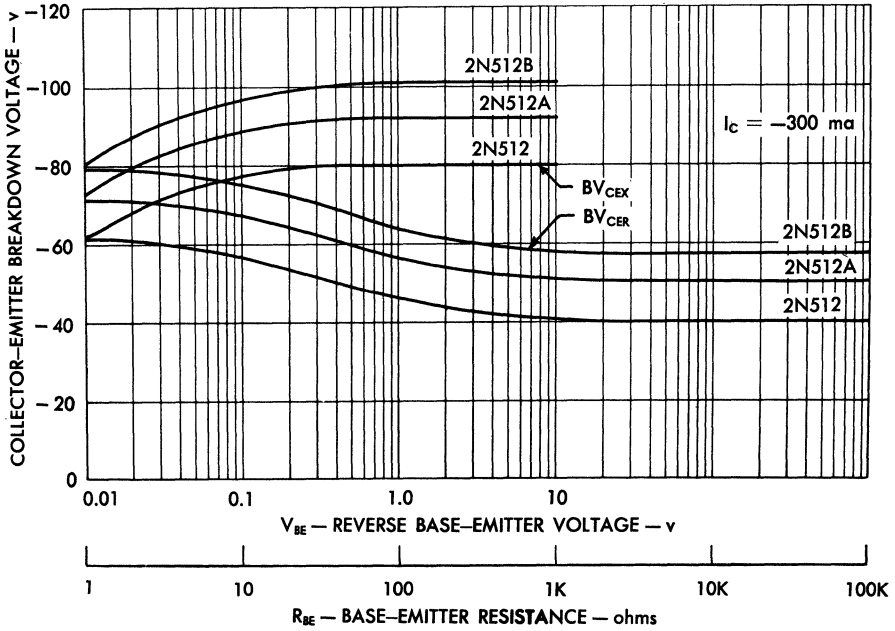
6

TYPES 2N512, 2N512A, AND 2N512B

P-N-P ALLOY-JUNCTION GERMANIUM HIGH-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

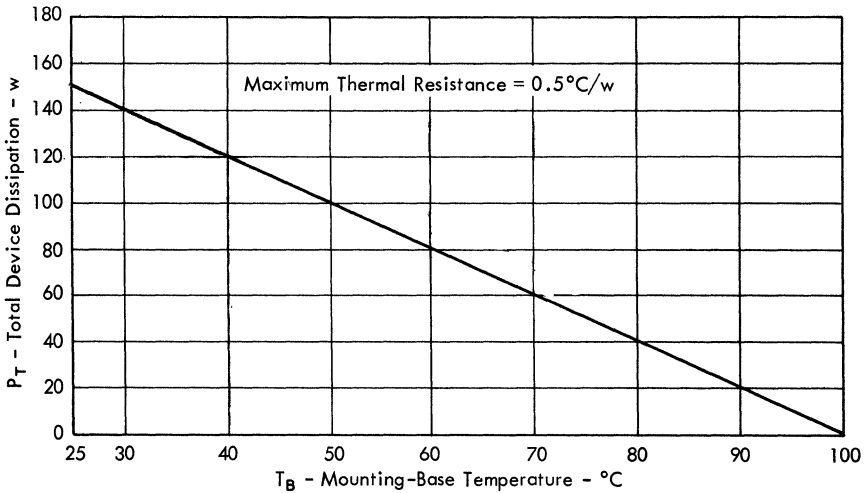
COLLECTOR-EMITTER BREAKDOWN VOLTAGE CHARACTERISTICS



6

THERMAL INFORMATION

POWER DISSIPATION DERATING CURVE



TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553, 2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

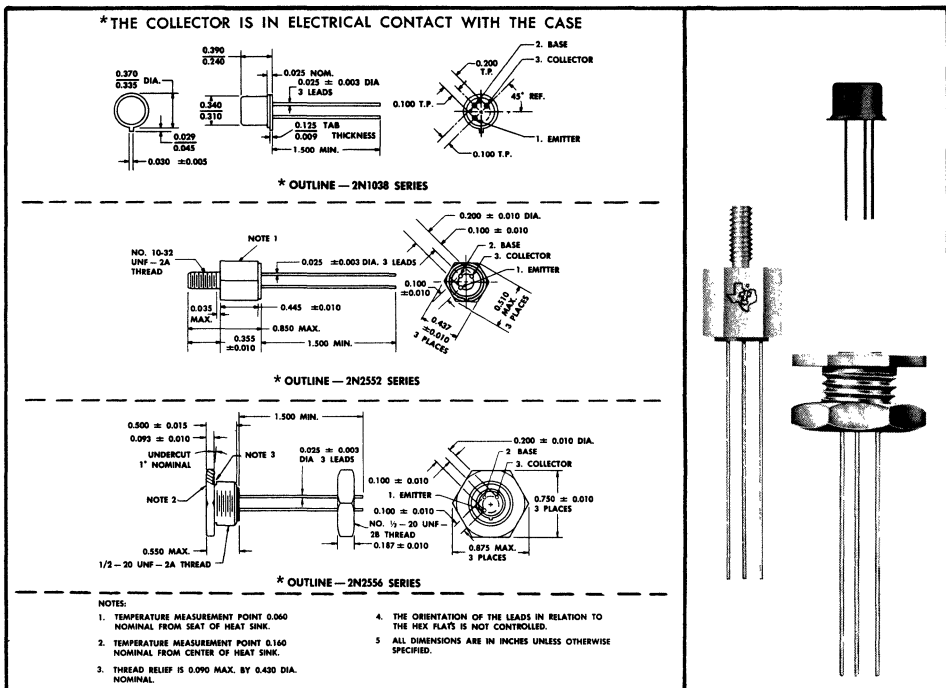
40-, 60-, 80-, or 100-VOLT UNITS
20 WATTS AT 25°C CASE TEMPERATURE
Choice of TO-5, Stud, or Hex Package
Guaranteed Beta at 1 amp and 50 ma I_c

Guaranteed I_{CEX} at 85°C
LOW r_{CS} • LOW I_{CBO} • LOW V_{BE}
for
RELAY DRIVERS • PULSE AMPLIFIERS
SERVO AMPLIFIERS • AUDIO AMPLIFIERS

TYPES 2N1038 THRU 2N1041, 2N2552 THRU 2N2559
BULLETIN NO. 68397, JULY 1963
REVISED FEBRUARY 1968

mechanical data

The transistors are in hermetically sealed, resistance-welded cases with glass-to-metal seals between case and leads. These devices are available in (1) a round TO-5 package weighing approximately 2.4 grams (2N1038 series), (2) a stud heat-sink package which weighs approximately 5.4 grams (2N2552 series) and (3) a hexagonal flanged-nut heat-sink package which weighs approximately 8.6 grams (2N2556 series). Mounting hardware available is shown on page 8.



*Indicates JEDEC Registered Data.

TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553, 2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N1038 2N2552 2N2556	2N1039 2N2553 2N2557	2N1040 2N2554 2N2558	2N1041 2N2555 2N2559
Collector-Base Voltage	40 v	60 v	80 v	100 v
Collector-Emitter Voltage (see Note 1)	40 v	60 v	80 v	100 v
Emitter-Base Voltage	←————— 20 v —————→			
Collector Current	←————— 3 a —————→			
Base Current	←————— 1 a —————→			
Total Device Dissipation at (or below) 25°C				
Case Temperature (see Note 2)	←————— 20 w —————→			
Operating Case Temperature Range	←————— -55°C to +100°C —————→			
Storage Temperature Range	←————— -55°C to +100°C —————→			

NOTES: 1. This value applies when base-emitter voltage $V_{BE} = +0.2$ v.

2. Derate linearly to +100°C case temperature at the rate of 267 mw/°C.

6

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
V_{CBO} Collector-Base Breakdown Voltage	$I_C = -650 \mu a, I_E = 0$	2N1038 2N2552 2N2556	-40			v
		2N1039 2N2553 2N2557	-60			
		2N1040 2N2554 2N2558	-80			
		2N1041 2N2555 2N2559	-100			
V_{CEO} Collector-Emitter Breakdown Voltage	$I_C = -100 ma, I_B = 0$	2N1038 2N2552 2N2556	-30			v
		2N1039 2N2553 2N2557	-40			
		2N1040 2N2554 2N2558	-50			
		2N1041 2N2555 2N2559	-60			

*Indicates JEDEC Registered Data.

**TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553,
2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559**
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
*I _{CBO} Collector Cutoff Current	V _{CB} = -20 v, I _E = 0	2N1038 2N2552 2N2556			-125	μa
	V _{CB} = -30 v, I _E = 0	2N1039 2N2553 2N2557				
	V _{CB} = -40 v, I _E = 0	2N1040 2N2554 2N2558				
	V _{CB} = -50 v, I _E = 0	2N1041 2N2555 2N2559				
*I _{CEO} Collector Cutoff Current	V _{CE} = -15 v, I _B = 0	2N1038 2N2552 2N2556			-25	ma
	V _{CE} = -20 v, I _B = 0	2N1039 2N2553 2N2557				
	V _{CE} = -25 v, I _B = 0	2N1040 2N2554 2N2558				
	V _{CE} = -30 v, I _B = 0	2N1041 2N2555 2N2559				
*I _{CEX} Collector Cutoff Current	V _{CE} = -40 v, V _{BE} = +0.2 v	2N1038 2N2552 2N2556			-650	μa
	V _{CE} = -60 v, V _{BE} = +0.2 v	2N1039 2N2553 2N2557				
	V _{CE} = -80 v, V _{BE} = +0.2 v	2N1040 2N2554 2N2558				
	V _{CE} = -100 v, V _{BE} = +0.2 v	2N1041 2N2555 2N2559				
*I _{CEX} Collector Cutoff Current	V _{CE} = -20 v, V _{BE} = +0.2 v T _C = +85°C	2N1038 2N2552 2N2556			-5	ma
	V _{CE} = -30 v, V _{BE} = +0.2 v T _C = +85°C	2N1039 2N2553 2N2557				
	V _{CE} = -40 v, V _{BE} = +0.2 v T _C = +85°C	2N1040 2N2554 2N2558				
	V _{CE} = -50 v, V _{BE} = +0.2 v T _C = +85°C	2N1041 2N2555 2N2559				
*I _{EBO} Emitter Cutoff Current	V _{EB} = -20 v, I _C = 0	All			-650	μa

*Indicates JEDEC Registered Data.

6

TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553, 2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
h_{IE} Static Common Emitter Input Impedance	$V_{CE} = -0.5 \text{ v}$, $I_C = -1 \text{ a}$ (see Note 3)	All			60	ohm
$^*h_{FE}$ Static Forward Current Transfer Ratio	$V_{CE} = -0.5 \text{ v}$, $I_C = -1 \text{ a}$ (see Note 3)	All	20		60	
	$V_{CE} = -0.5 \text{ v}$, $I_C = -50 \text{ ma}$	All	33		200	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -0.5 \text{ v}$, $I_C = -1 \text{ a}$ $T_C = -55^\circ\text{C}$ (See Note 3)	All	15		60	
	$V_{CE} = -0.5 \text{ v}$, $I_C = -1 \text{ a}$ $T_C = +85^\circ\text{C}$	All	20		75	
Y_{FE} Static Common-Emitter Forward Transfer Admittance	$V_{CE} = -0.5 \text{ v}$, $I_C = -1 \text{ a}$ (see Note 3)	All	1.0			mho
$^*V_{BE}$ Base-Emitter Voltage	$V_{CE} = -0.5 \text{ v}$, $I_C = -1 \text{ a}$ (see Note 3)	All			-1.0	v
V_{BE} Base-Emitter Voltage	$V_{CE} = -0.5 \text{ v}$, $I_C = -50 \text{ ma}$	All			-0.35	v
$^*V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -100 \text{ ma}$, $I_C = -1 \text{ a}$ (see Note 3)	All			-0.25	v
$^*h_{fe}$ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ v}$, $I_C = -0.5 \text{ a}$ $f = 1 \text{ kc}$	All	18		72	
$^* h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ v}$, $I_C = -0.5 \text{ a}$ $f = 112.5 \text{ kc}$	All	2.0			
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -6 \text{ v}$, $I_E = 0$ $f = 135 \text{ kc}$	All		100		pf

NOTES: 3. Measurements are made with voltage sensing contacts located 0.25 inch from header of transistor.
Voltage sensing contacts are separate from current carrying contacts.

*Indicates JEDEC Registered Data.

switching characteristics at 25°C case temperature

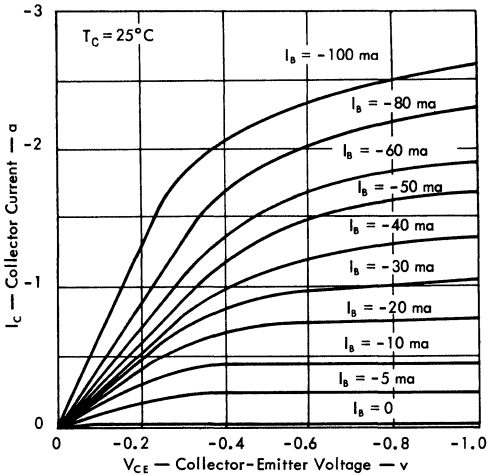
PARAMETER	TEST CONDITIONS†	TYPICAL	UNIT
t_d Delay Time	$I_C = -1 \text{ a}$ $V_{BE(off)} = 7.4 \text{ v}$ $R_L = 29 \Omega$ (See circuit on Page 8)	0.18	μsec
t_r Rise Time		0.47	μsec
t_s Storage Time		0.59	μsec
t_f Fall Time		1.21	μsec
t_T Total Switching Time		2.45	μsec

†Voltage and current values are nominal; exact values vary slightly with device parameters.

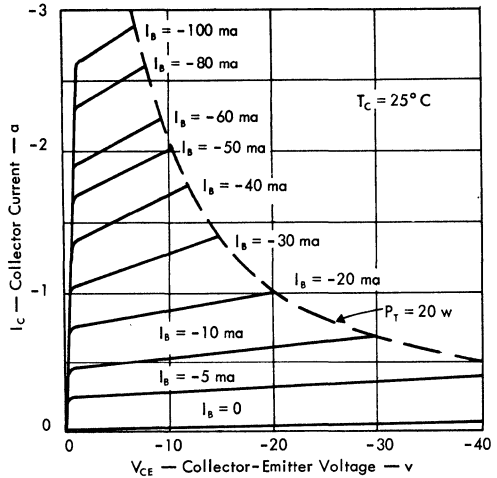
**TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553,
2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559**
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

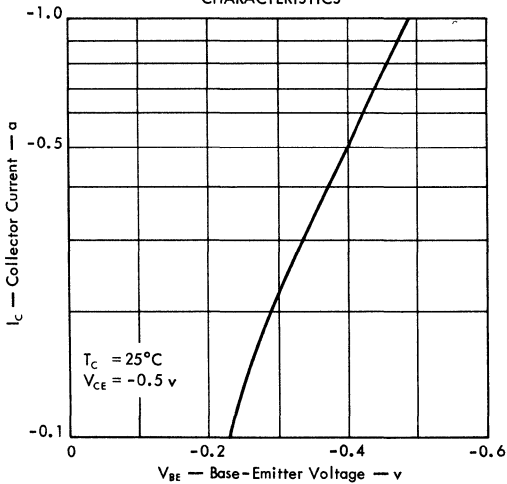
COMMON-EMITTER COLLECTOR
CHARACTERISTICS
(Low-Voltage Region)



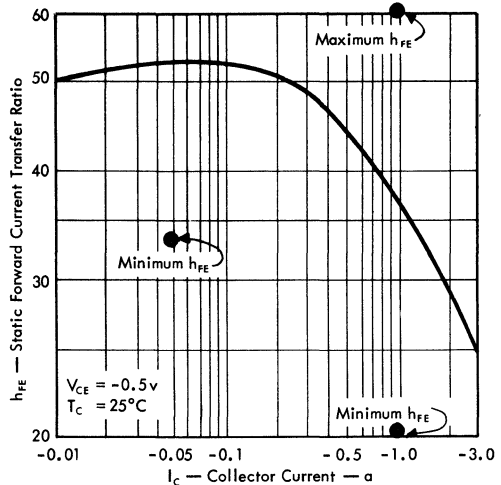
COMMON-EMITTER COLLECTOR
CHARACTERISTICS
(High-Voltage Region)



COMMON-EMITTER TRANSFER
CHARACTERISTICS

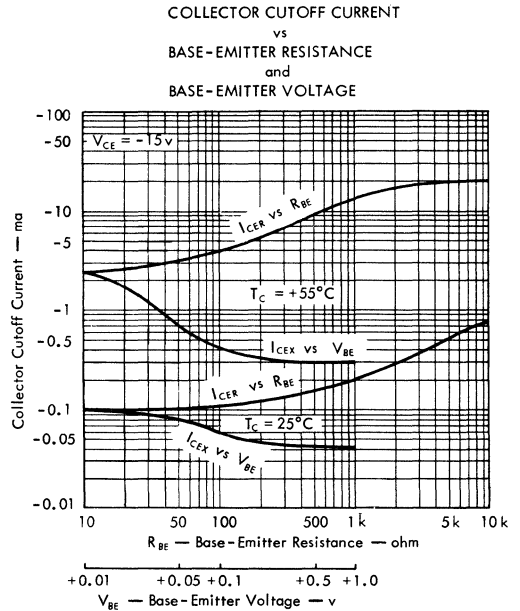
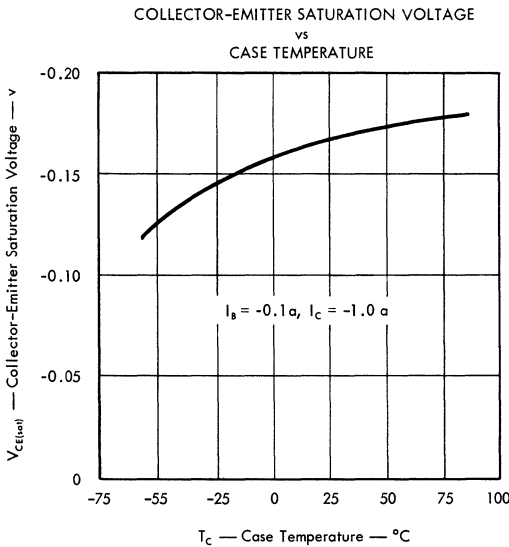
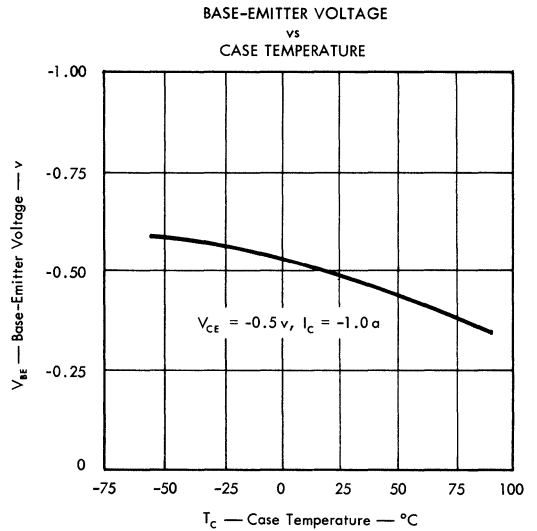
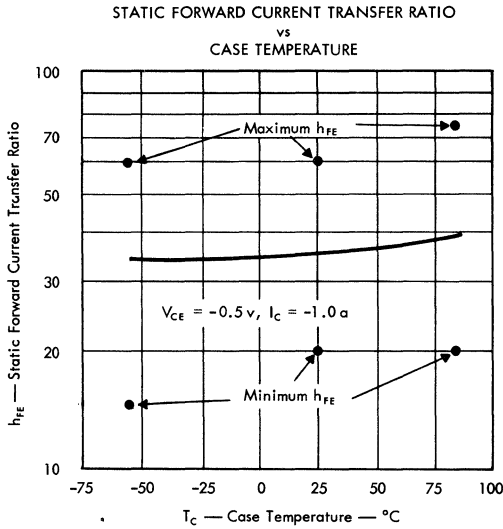


STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT



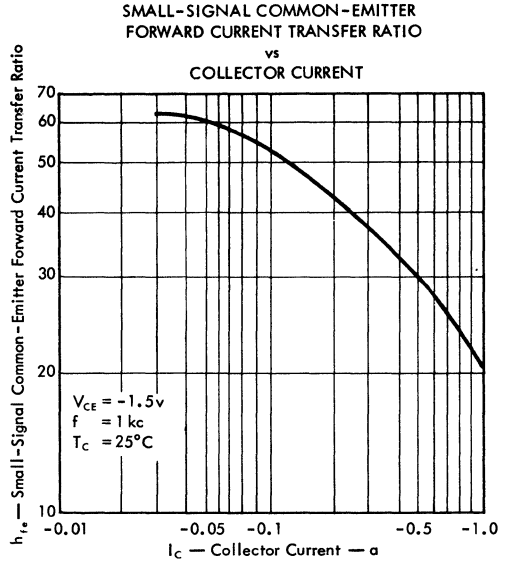
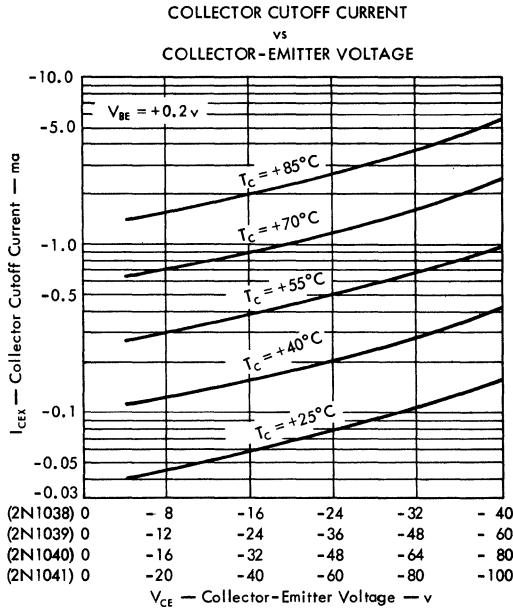
**TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553,
2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559**
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

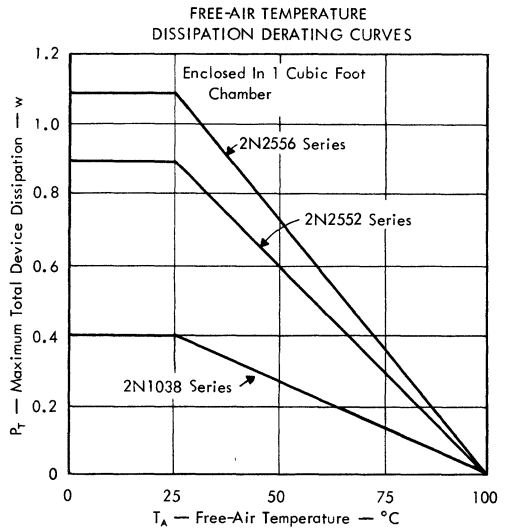
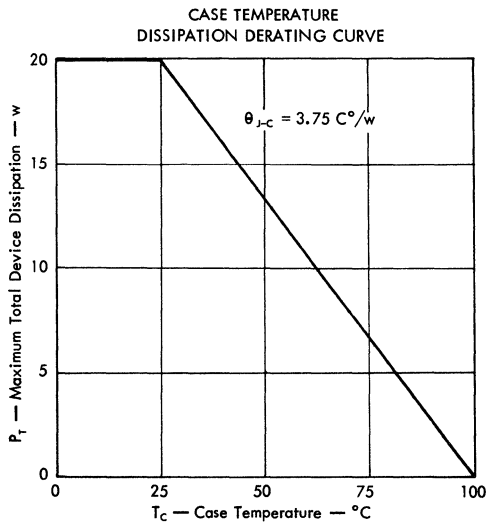


TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553, 2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS



THERMAL CHARACTERISTICS

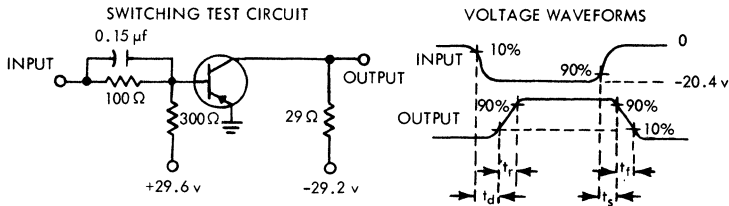


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TYPES 2N1038, 2N1039, 2N1040, 2N1041 • 2N2552, 2N2553, 2N2554, 2N2555 • 2N2556, 2N2557, 2N2558, 2N2559

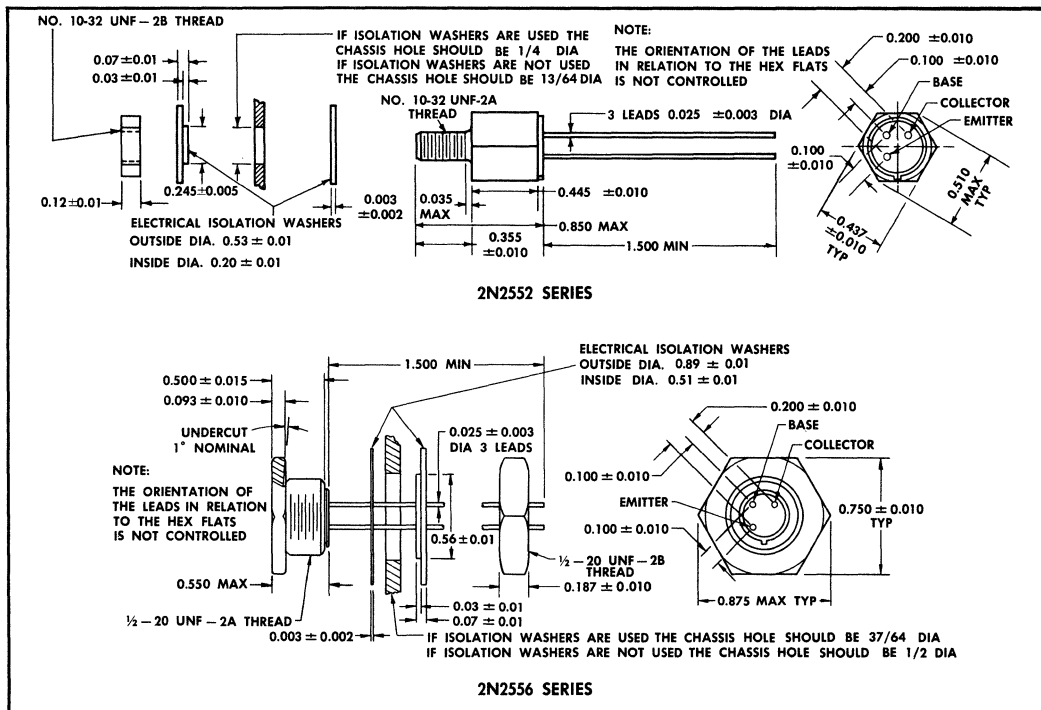
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



- NOTES: a. The input waveform has the following characteristics: $t_r \leq 10$ nsec, $t_f \leq 10$ nsec, $PW = 1.6$ msec, Duty Cycle = 10%.
- b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14$ nsec, $R_{in} \geq 10 M \Omega$, $C_{in} \leq 11.5$ pf.
- c. Resistors must be non-inductive types.

MOUNTING HARDWARE INFORMATION



PRINTED IN U.S.A.

971

TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561, 2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

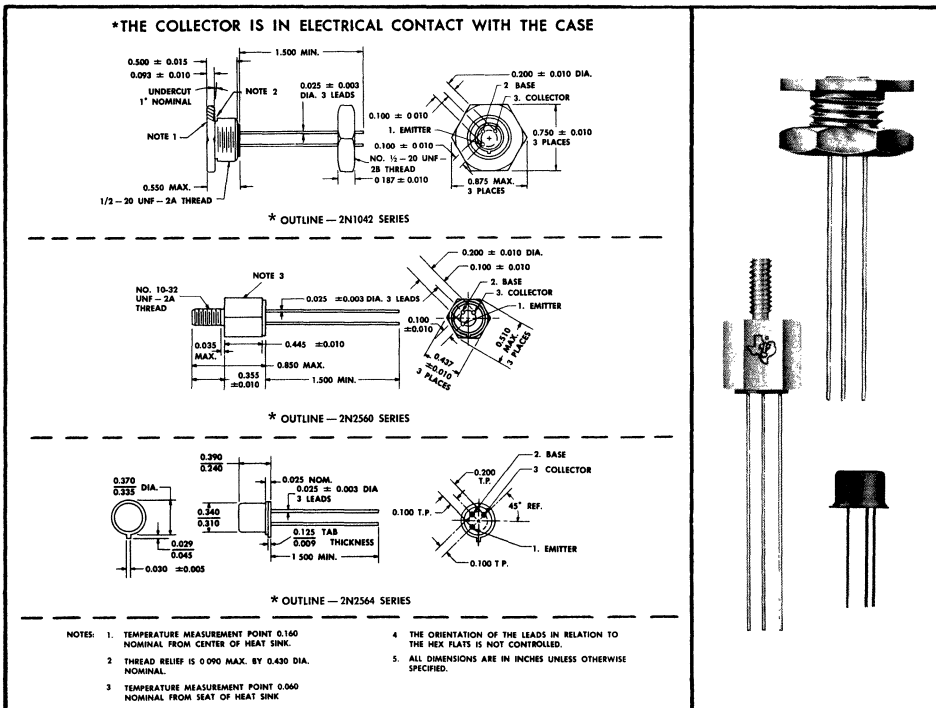
40-, 60-, 80-, or 100-VOLT UNITS
 20 WATTS AT 25°C CASE TEMPERATURE
 Choice of TO-5, Stud, or Hex Package
 Guaranteed Beta at 3 amps and 50 ma I_c

Guaranteed I_{CEX} at 85°C
 LOW r_{CS} • LOW I_{CBO} • LOW V_{BE}
 for
 RELAY DRIVERS • PULSE AMPLIFIERS
 SERVO AMPLIFIERS • AUDIO AMPLIFIERS

TYPES 2N1042 THRU 2N1045, 2N2560
 BULLETIN NO. DL-5 693398, JULY 1963
 REVISED JANUARY 1969

mechanical data

The transistors are in hermetically sealed, resistance-welded cases with glass-to-metal seals between case and leads. These devices are available in (1) a hexagonal flanged-nut heat-sink package which weighs approximately 8.6 grams (2N1042 series), (2) a stud heat-sink package which weighs approximately 5.4 grams (2N2560 series) and (3) a round TO-5 package weighing approximately 2.4 grams (2N2564 series). Mounting hardware available is shown on page 8.



*Indicates JEDEC Registered Data.

TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561, 2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N1042 2N2560 2N2564	2N1043 2N2561 2N2565	2N1044 2N2562 2N2566	2N1045 2N2563 2N2567
Collector-Base Voltage	40 v	60 v	80 v	100 v
Collector-Emitter Voltage (see Note 1)	40 v	60 v	80 v	100 v
Emitter-Base Voltage	←————— 20 v —————→			
Collector Current	←————— 3.5 a —————→			
Base Current	←————— 1 a —————→			
Total Device Dissipation at (or below) 25°C				
Case Temperature (see Note 2)	←————— 20 w —————→			
Operating Case Temperature Range	←————— - 55°C to + 100°C —————→			
Storage Temperature Range	←————— - 55°C to + 100°C —————→			

- NOTES: 1. This value applies when base-emitter voltage $V_{BE} = + 0.2$ v.
 2. Derate linearly to + 100°C case temperature at the rate of 267 mw/°C.

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
BV _{CBO} Collector-Base Breakdown Voltage	$I_C = - 650 \mu a, I_E = 0$	2N1042	- 40			v
		2N2560				
		2N2564				
		2N1043	- 60			
		2N2561				
		2N2565				
		2N1044	- 80			
		2N2562				
		2N2566				
		2N1045	- 100			
		2N2563				
		2N2567				
*BV _{CEO} Collector-Emitter Breakdown Voltage	$I_C = - 100 ma, I_B = 0$	2N1042	- 30			v
		2N2560				
		2N2564				
		2N1043	- 40			
		2N2561				
		2N2565				
		2N1044	- 50			
		2N2562				
		2N2566				
		2N1045	- 60			
		2N2563				
		2N2567				

*Indicates JEDEC Registered Data.

TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561, 2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
*I _{CBO} Collector Cutoff Current	V _{CB} = -20 v, I _E = 0	2N1042 2N2560 2N2564			-125	μa
	V _{CB} = -30 v, I _E = 0	2N1043 2N2561 2N2565				
	V _{CB} = -40 v, I _E = 0	2N1044 2N2562 2N2566				
	V _{CB} = -50 v, I _E = 0	2N1045 2N2563 2N2567				
*I _{CEO} Collector Cutoff Current	V _{CE} = -15 v, I _B = 0	2N1042 2N2560 2N2564			-25	ma
	V _{CE} = -20 v, I _B = 0	2N1043 2N2561 2N2565			-20	
	V _{CE} = -25 v, I _B = 0	2N1044 2N2562 2N2566			-20	
	V _{CE} = -30 v, I _B = 0	2N1045 2N2563 2N2567			-20	
*I _{CEX} Collector Cutoff Current	V _{CE} = -40 v, V _{BE} = +0.2 v	2N1042 2N2560 2N2564			-650	μa
	V _{CE} = -60 v, V _{BE} = +0.2 v	2N1043 2N2561 2N2565				
	V _{CE} = -80 v, V _{BE} = +0.2 v	2N1044 2N2562 2N2566				
	V _{CE} = -100 v, V _{BE} = +0.2 v	2N1045 2N2563 2N2567				
*I _{CEX} Collector Cutoff Current	V _{CE} = -20 v, V _{BE} = +0.2 v T _C = +85°C	2N1042 2N2560 2N2564			-5	ma
	V _{CE} = -30 v, V _{BE} = +0.2 v T _C = +85°C	2N1043 2N2561 2N2565				
	V _{CE} = -40 v, V _{BE} = +0.2 v T _C = +85°C	2N1044 2N2562 2N2566				
	V _{CE} = -50 v, V _{BE} = +0.2 v T _C = +85°C	2N1045 2N2563 2N2567				
*I _{EBO} Emitter Cutoff Current	V _{EB} = -20 v, I _C = 0	All			-650	μa

*Indicates JEDEC Registered Data.

6

TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561, 2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
h_{iE}	Static Common-Emitter Input Impedance	$V_{CE} = -1.0 \text{ v}$, $I_C = -3 \text{ a}$ (see Note 3)	All			30	ohm
* h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -1.0 \text{ v}$, $I_C = -3 \text{ a}$ (see Note 3)	All	20		60	
		$V_{CE} = -1.0 \text{ v}$, $I_C = -1 \text{ a}$ (see Note 3)	All			150	
		$V_{CE} = -0.5 \text{ v}$, $I_C = -50 \text{ ma}$	All	50			
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -1.0 \text{ v}$, $I_C = -3 \text{ a}$ $T_C = -55^\circ\text{C}$ (see Note 3)	All	15		60	
		$V_{CE} = -1.0 \text{ v}$, $I_C = -3 \text{ a}$ $T_C = +85^\circ\text{C}$ (see Note 3)	All	20		75	
Y_{FE}	Static Common-Emitter Forward Transfer Admittance	$V_{CE} = -1.0 \text{ v}$, $I_C = -3 \text{ a}$ (see Note 3)	All	2.0			mho
* V_{BE}	Base-Emitter Voltage	$V_{CE} = -1.0 \text{ v}$, $I_C = -3 \text{ a}$ (see Note 3)	All			-1.5	v
V_{BE}	Base-Emitter Voltage	$V_{CE} = -1.0 \text{ v}$, $I_C = -50 \text{ ma}$	All			-0.5	v
* $V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -0.3 \text{ a}$, $I_C = -3 \text{ a}$ (see Note 3)	All			-0.75	v
		$I_B = -100 \text{ ma}$, $I_C = -1 \text{ a}$ (see Note 3)	All			-0.25	
* h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ v}$, $I_C = -0.5 \text{ a}$ $f = 1 \text{ kc}$	All	25		100	
* $ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ v}$, $I_C = -0.5 \text{ a}$ $f = 125 \text{ kc}$	All	2.0			
C_{ob}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = -6 \text{ v}$, $I_E = 0$ $f = 135 \text{ kc}$	All		100		pf

NOTES: 3. Measurements are made with voltage sensing contacts located 0.25 inches from header of transistor.
Voltage sensing contacts are separate from current carrying contacts.

*Indicates JEDEC Registered Data.

switching characteristics at 25°C case temperature

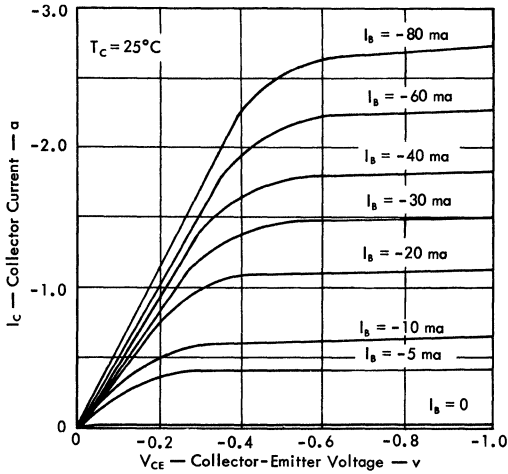
PARAMETER	TEST CONDITIONS †	TYPICAL	UNIT
t_{d} Delay Time	$I_C = -3 \text{ a}$ $V_{BE(off)} = 8.2 \text{ v}$ $R_L = 10 \Omega$ (See circuit on Page 8)	0.20	μsec
t_r Rise Time		0.48	μsec
t_s Storage Time		0.29	μsec
t_f Fall Time		2.15	μsec
t_T Total Switching Time		3.12	μsec

†Voltage and current values shown are nominal; exact values vary slightly with device parameters.

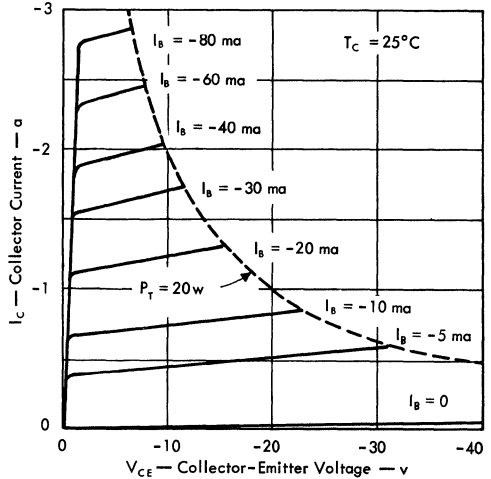
**TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561,
2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567**
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

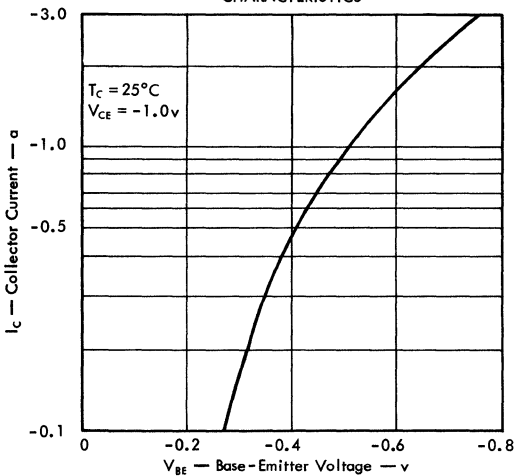
COMMON-EMITTER COLLECTOR
CHARACTERISTICS
(Low-Voltage Region)



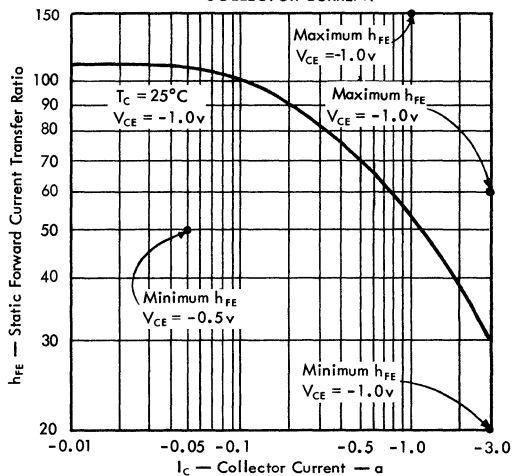
COMMON-EMITTER COLLECTOR
CHARACTERISTICS
(High-Voltage Region)



COMMON-EMITTER TRANSFER
CHARACTERISTICS



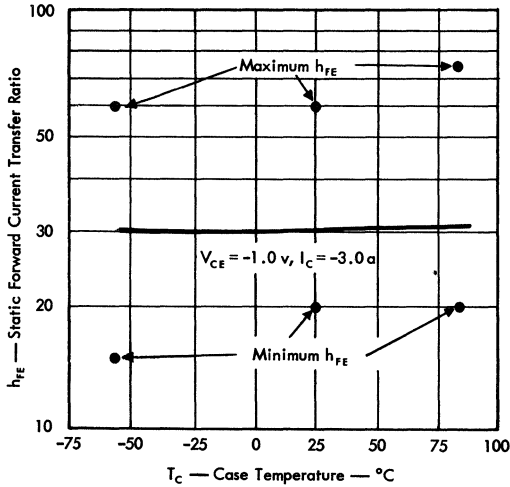
STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT



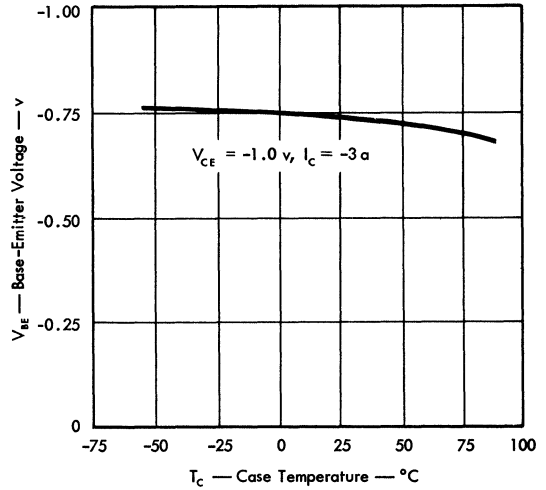
**TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561,
2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567**
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

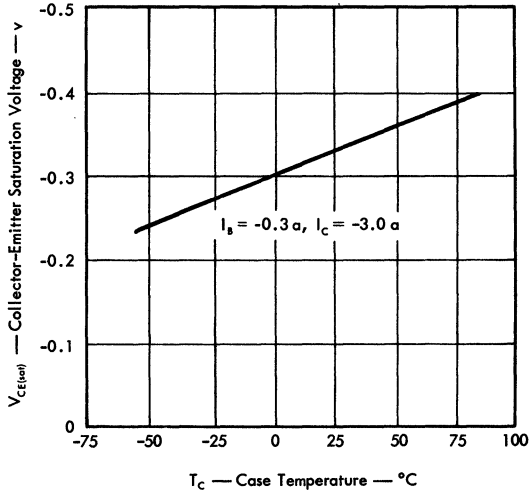
STATIC FORWARD CURRENT TRANSFER RATIO
vs
CASE TEMPERATURE



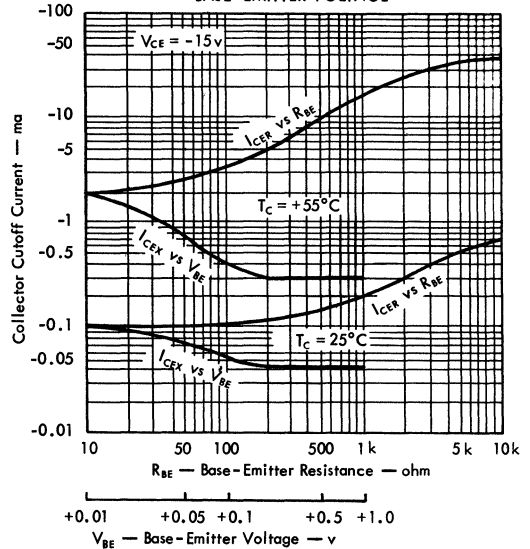
BASE-EMITTER VOLTAGE
vs
CASE TEMPERATURE



COLLECTOR-EMITTER SATURATION VOLTAGE
vs
CASE TEMPERATURE



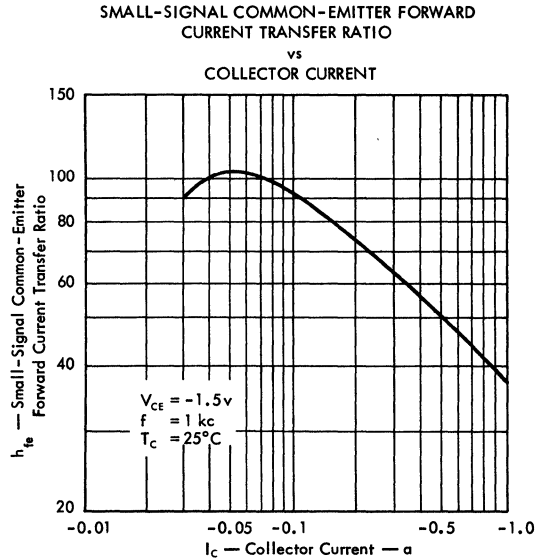
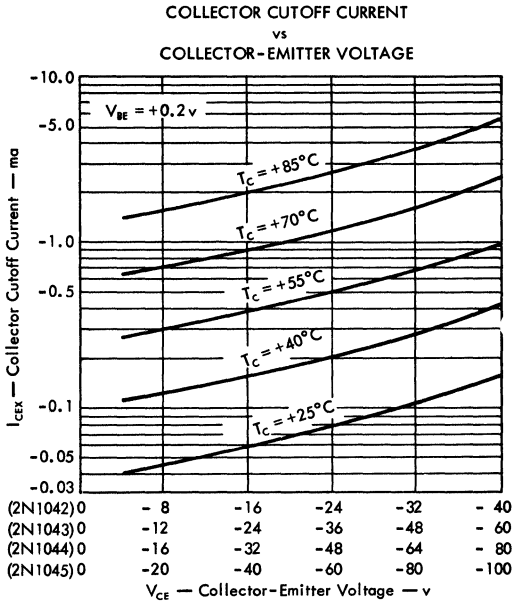
COLLECTOR CUTOFF CURRENT
vs
BASE-EMITTER RESISTANCE
and
BASE-EMITTER VOLTAGE



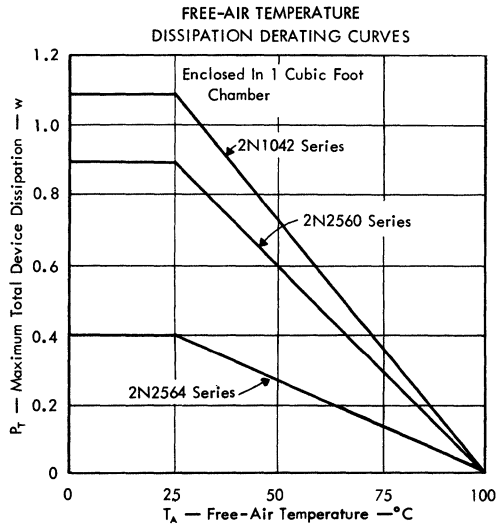
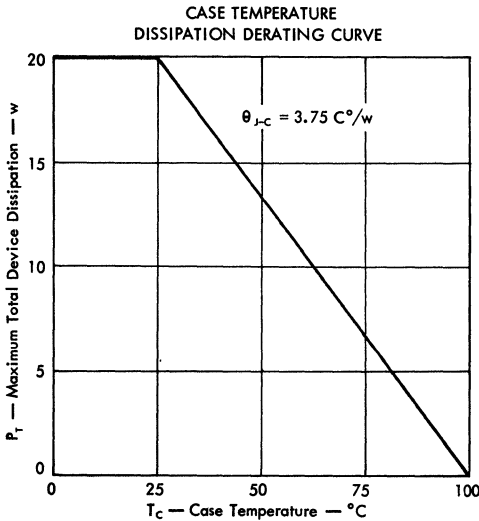
TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561, 2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS



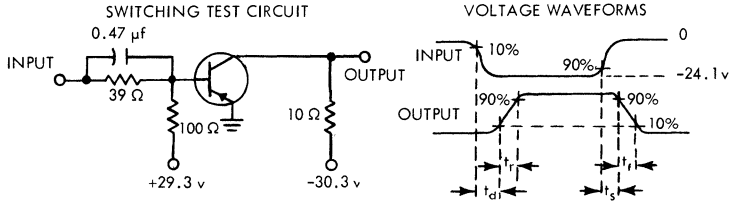
THERMAL CHARACTERISTICS



TYPES 2N1042, 2N1043, 2N1044, 2N1045 • 2N2560, 2N2561, 2N2562, 2N2563 • 2N2564, 2N2565, 2N2566, 2N2567

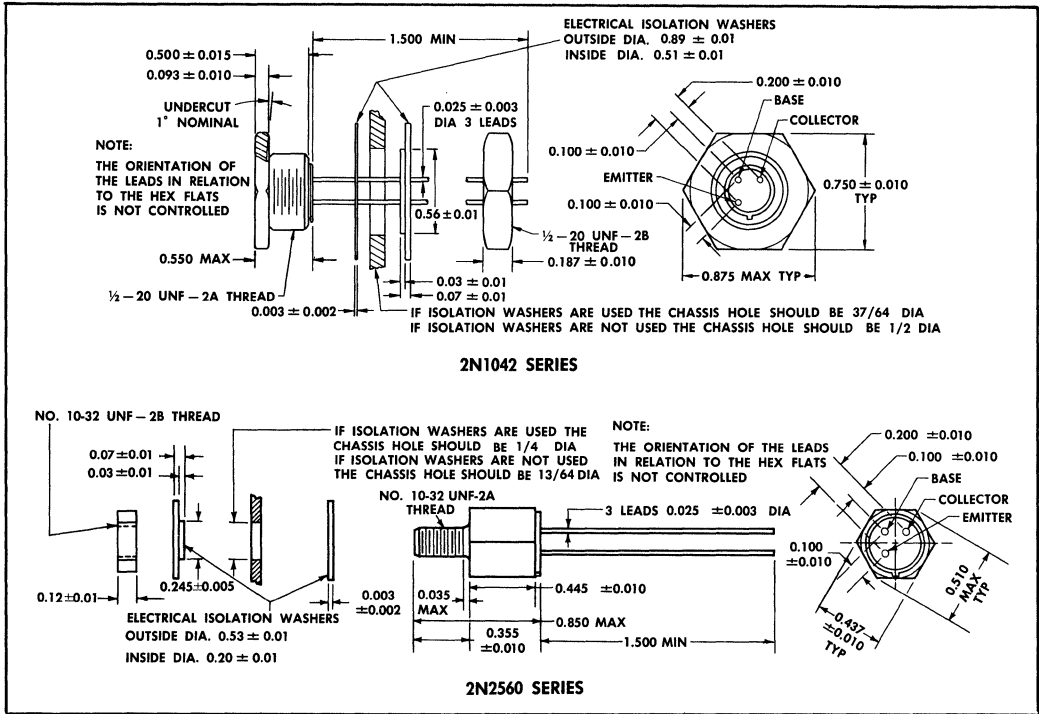
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION



- NOTES: a. The input waveform has the following characteristics: $t_r \leq 10$ nsec, $t_f \leq 10$ nsec, PW = 1.6 msec, Duty Cycle = 10%.
 b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14$ nsec, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pf.
 c. Resistors must be non-inductive types.

MOUNTING HARDWARE INFORMATION



TYPE 2N1046

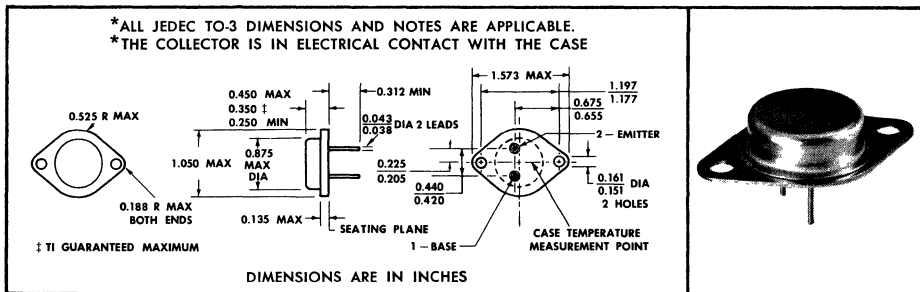
P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTOR

TYPE 2N1046
BULLETIN NO. DL-5 644551, APRIL 1964

HIGH-FREQUENCY POWER TRANSISTOR FOR MILITARY AND INDUSTRIAL APPLICATIONS

mechanical data

This transistor is in a precision-welded, hermetically sealed enclosure. The mounting base provides an excellent heat path from the collector junction to a heat sink. The mounting base and heat sink must be in intimate contact for maximum heat transfer. Extreme cleanliness during the assembly process prevents sealed-in contamination. The approximate weight of the unit is 18 grams.



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	100 v*
Collector-Emitter Voltage (See Note 1)	50 v*
Emitter-Base Voltage	{ 1.5 v* }
	{ 2.0 v† }
Continuous Collector Current	12 a*
Peak Collector Current (See Note 2)	20 a*
Base Current	3 a*
Safe Continuous Operating Region	See Figure 13*
Continuous Collector Dissipation at (or below) 75°C Case Temperature (See Note 3)	50 w
Continuous Collector Dissipation at (or below) 50°C Case Temperature (See Note 4)	50 w*
Peak Collector Power Dissipation at (or below) 25°C Case Temperature (See Notes 2 and 5)	600 w*
Operating Collector Junction Temperature	100°C*
Storage Temperature Range	{ -55°C to +100°C* }
	{ -55°C to +110°C† }
Lead Temperature, 1/8 inch ± 1/32 inch from case for 10 seconds	230°C*

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for a rectangular waveshape, pulse width ≤ 270 μsec, duty cycle ≤ 10%. See figure 12 for other allowable pulse width and duty cycle combinations.
 3. Derate linearly to 100°C case temperature at the rate of 2 w/°C.
 4. Derate linearly to 100°C case temperature at the rate of 1 w/°C. This corresponds to the JEDEC registered maximum value of thermal resistance, θ_{J-C}, 1.0 °C/w.
 5. Derate linearly to 100°C case temperature at the rate of 8 w/°C.

*Indicates JEDEC registered data. †Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

6

TYPE 2N1046

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTOR

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = -10 \text{ ma}, I_E = 0$	-100*	v
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ ma}, I_B = 0$, See Note 6	-50*	v
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = -2 \text{ ma}, I_C = 0$ $I_E = -10 \text{ ma}, I_C = 0$	-1.5* -2.0	v
I_{CBO}	Collector Cutoff Current	$V_{CB} = -3 \text{ v}, I_E = 0$	-0.3*	ma
		$V_{CB} = -75 \text{ v}, I_E = 0$	-2.0*	
		$V_{CB} = -75 \text{ v}, I_E = 0, T_C = +70^\circ\text{C}$	-12	
I_{CEX}	Collector Cutoff Current	$V_{CE} = -75 \text{ v}, V_{BE} = +0.2 \text{ v}$	-2.0	ma
I_{EBO}	Emitter Cutoff Current	$V_{EB} = -0.5 \text{ v}, I_C = 0$	-0.1*	ma
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ v}, I_C = -0.5 \text{ a}$, See Note 7	40* 60†	200†
		$V_{CE} = -1.5 \text{ v}, I_C = -5 \text{ a}$, See Note 7	40* 60†	
		$V_{CE} = -1.5 \text{ v}, I_C = -5 \text{ a}, T_C = -55^\circ\text{C}$, See Note 7	60	
		$V_{CE} = -1.5 \text{ v}, I_C = -5 \text{ a}, T_C = +70^\circ\text{C}$, See Note 7	40	
V_{BE}	Base-Emitter Voltage	$I_B = -50 \text{ ma}, I_C = -0.5 \text{ a}$, See Note 7	-0.4*	v
		$I_B = -500 \text{ ma}, I_C = -5 \text{ a}$, See Note 7	-0.7*	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -50 \text{ ma}, I_C = -0.5 \text{ a}$, See Note 7	-0.2*	v
		$I_B = -500 \text{ ma}, I_C = -5 \text{ a}$, See Note 7	-0.4*	
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -15 \text{ v}, I_C = -0.5 \text{ a}, f = 10 \text{ mc}$	1.0* 2.0†	

NOTES: 6. This parameter must be measured using pulse techniques. PW = 300 μsecs ; Duty Cycle $\leq 2\%$.

7. If these parameters are measured without a heat sink, d-c collector current must not be applied longer than 250 msec.

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYPICAL	UNIT
t_d Delay Time	$I_C = -5 \text{ a}, I_{B(1)} = -0.5 \text{ a}, I_{B(2)} = 0.5 \text{ a}$, $V_{BE(off)} = 2 \text{ v}, R_L = 4\Omega$, See Figure 1	0.1	μsec
t_r Rise Time		0.2	μsec
t_s Storage Time		2.0	μsec
t_f Fall Time		0.4	μsec
t_T Total Switching Time		2.7	μsec

†Voltage and current values are nominal; exact values vary slightly with device parameters.

PARAMETER MEASUREMENT INFORMATION

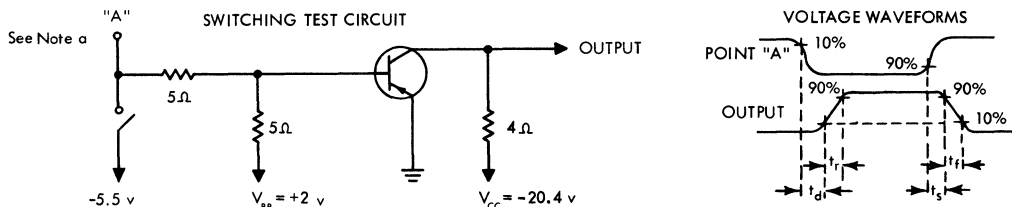


FIGURE 1

NOTES: (a) The pulse at point "A" has the following characteristics: $t_r \leq 20 \text{ nsec}$, $t_f \leq 20 \text{ nsec}$, PW = 5 μsec , duty cycle $\leq 5\%$.

(b) The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ nsec}$, $R_{in} \geq 1 \text{ M}\Omega$, $C_{in} \leq 20 \text{ pf}$.

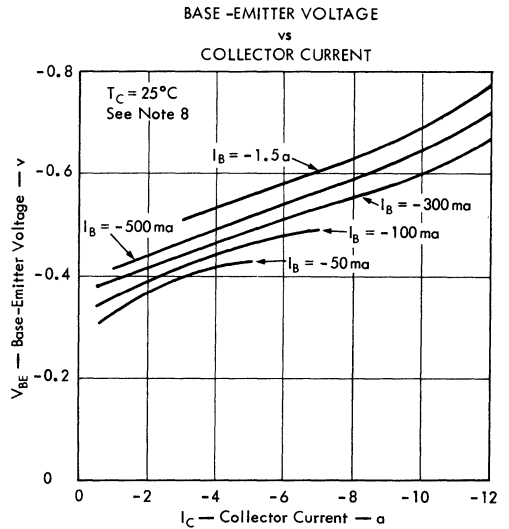
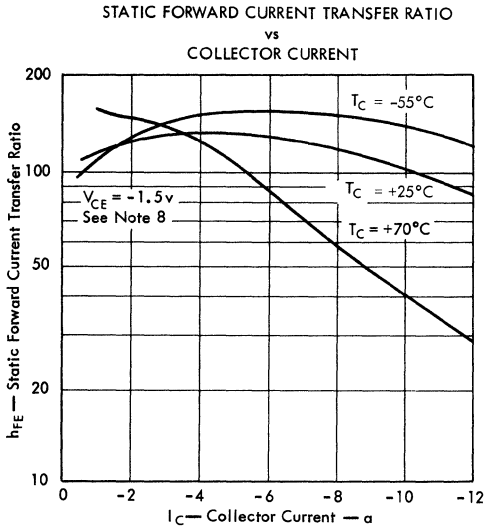
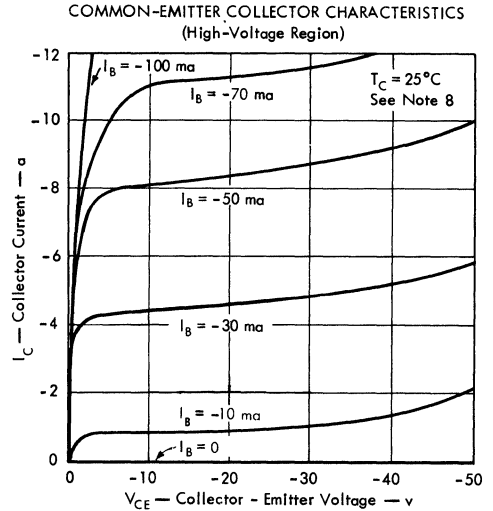
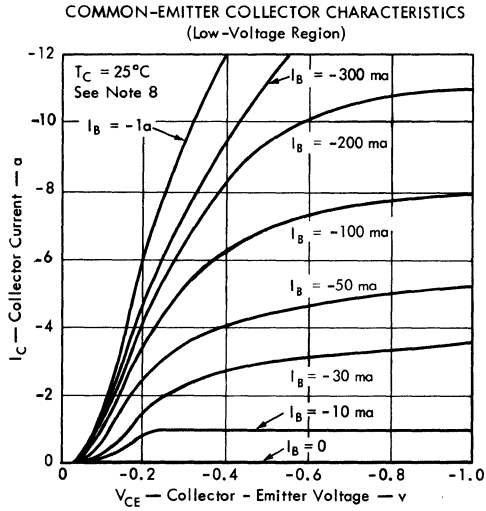
*Indicates JEDEC registered data.

†Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

TYPE 2N1046

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTOR

TYPICAL CHARACTERISTICS



NOTE 8: These characteristics were measured using pulse techniques. PW = 300 μ sec, Duty Cycle \leq 2%.

6

TYPE 2N1046

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTOR

TYPICAL CHARACTERISTICS

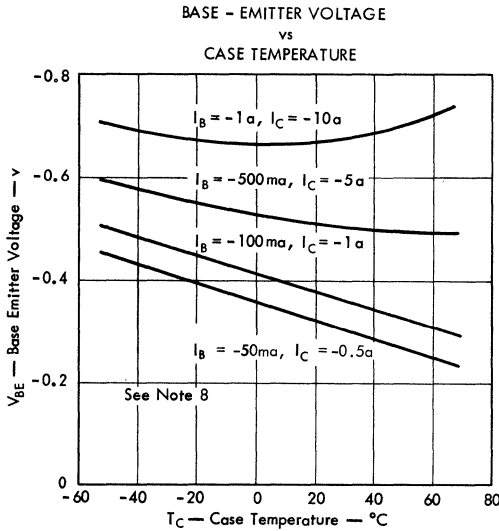


FIGURE 6

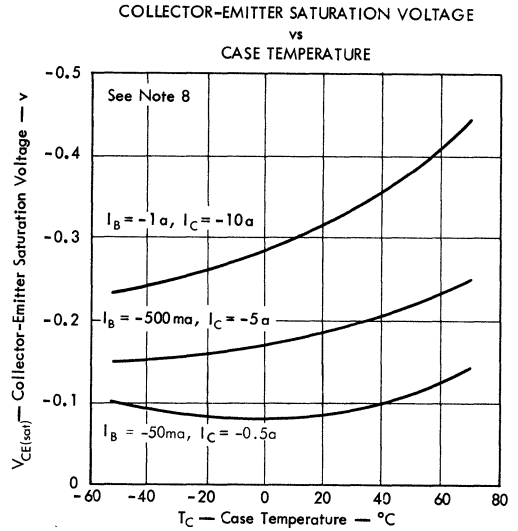


FIGURE 7

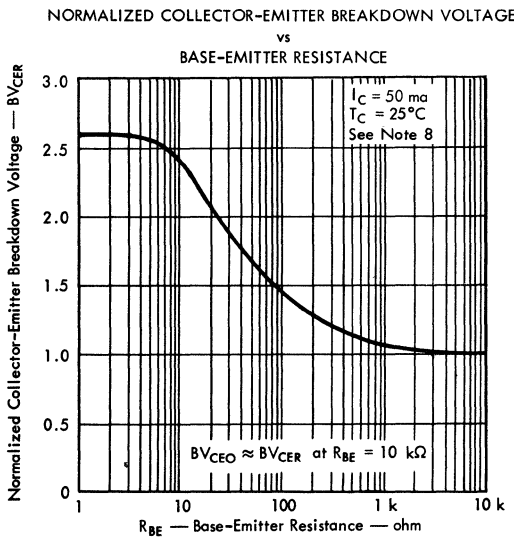


FIGURE 8

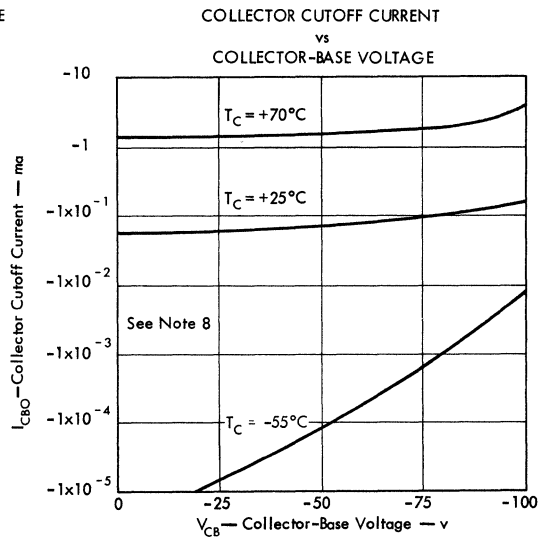


FIGURE 9

NOTE 8: These characteristics were measured using pulse techniques. PW = 300 μ sec, Duty Cycle \leq 2%.

TYPE 2N1046

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTOR

THERMAL CHARACTERISTICS

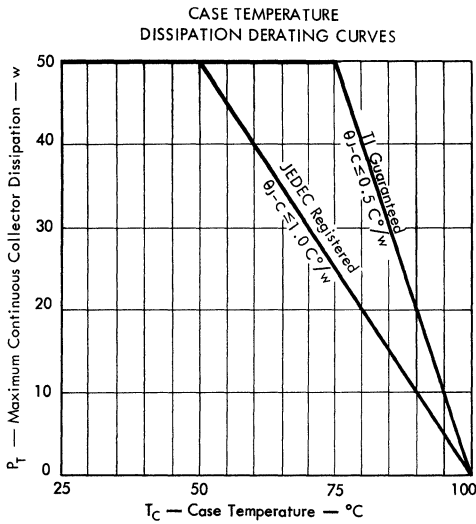


FIGURE 10

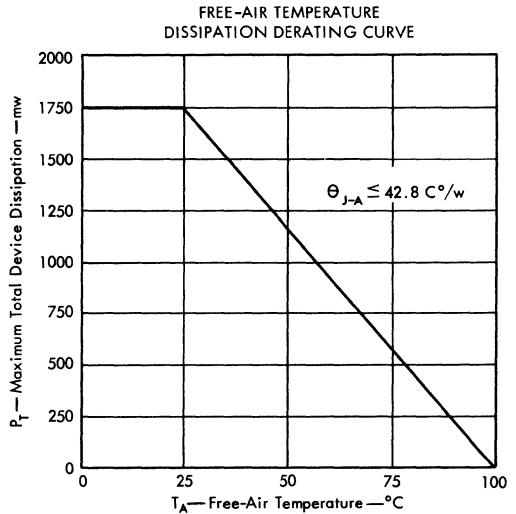


FIGURE 11

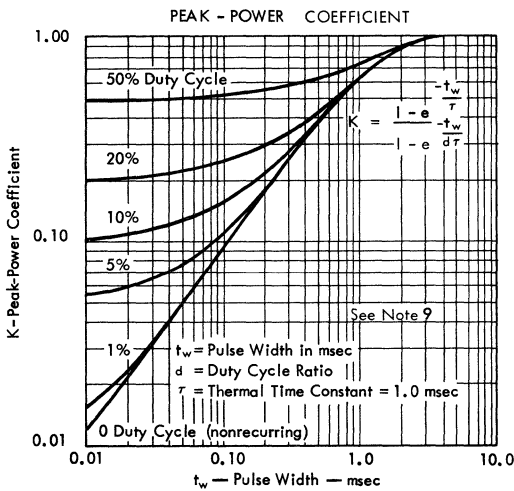


FIGURE 12

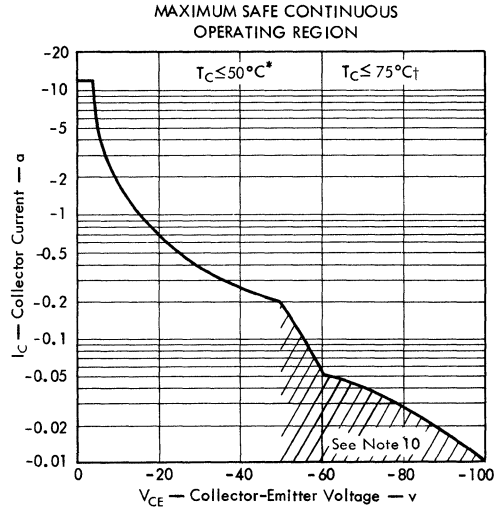


FIGURE 13

NOTES: 9. When $t_w > 3.0$ msec or $d > 0.5$ (50%), operation must be confined to the continuous operating region of Figure 13.

10. Operation in this region is permissible when base-emitter resistance $R_{BE} \leq 5 \Omega$

*Indicates JEDEC registered data.

†Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

TYPE 2N1046

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTOR

THERMAL INFORMATION

TABLE I

HEAT SINK		$\dagger\theta_{HS-A}$
Type	Dimensions	
Bright Copper	4" x 4" x 1/8"	3.8 C°/w
	6" x 6" x 1/8"	2.2 C°/w
	8" x 8" x 1/8"	1.8 C°/w
Bright Aluminum	10" x 10" x 1/8"	1.4 C°/w
	4" x 4" x 1/8"	6.5 C°/w
	6" x 6" x 1/8"	4.5 C°/w
Delbert Blinn #113 or Modine 1E1155B, Unfinished (or Equivalents)	8" x 8" x 1/8"	3.5 C°/w
	10" x 10" x 1/8"	2.8 C°/w
Delbert Blinn #113 or Modine 1E1155B, Black Anodized (or Equivalents)		3.2 C°/w

$\dagger\theta_{HS-A}$ are typical values based on convection cooling; plates and fins mounted in vertical position.

\ddagger All transistors mounted in the center of the heat sink with two 6-32 screws at 6 inch - pounds of torque.

TABLE II

SYMBOL	DEFINITION	UNIT	VALUE
$P_{T(avg)}$	Average Power Dissipation	w	
$P_{T(max)}$	Peak Power Dissipation	w	
θ_{J-C}	Junction-to-Case Thermal Resistance	C°/w	0.5
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	C°/w	42.8
θ_{C-A}	Case-to-Free-Air Thermal Resistance	C°/w	42.3
$\ddagger\theta_{C-HS}$	Case-to-Heat-Sink Thermal Resistance Typical with Dry Mounting Base	C°/w	0.65
	Typical with DC-11 Silicone Grease		0.45
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance	C°/w	see Table 1
T_A	Free-Air Temperature	°C	
$T_{J(avg)}$	Average Junction Temperature	°C	≤ 100
$T_{J(max)}$	Peak Junction Temperature	°C	≤ 100
T_C	Case Temperature	°C	
K	Peak-Power Coefficient		see Fig. 12
t_w	Pulse Width	msec	
t_p	Pulse Period	msec	
d	Duty Cycle Ratio (t_w/t_p)		

For d-c operation these transistors are voltage limited as well as thermally limited. Figure 10 or 11 and Figure 13 are recommended as a guide for selecting safe voltage and current combinations.

These transistors have a very low thermal resistance that may be fully utilized in a pulse-power application provided the pulse width is equal to (or less than) 3 milliseconds. If the power pulse is longer than 3 milliseconds, then the operating path is limited to the safe operating region described by Figure 10 or 11 and Figure 13.

The PEAK-POWER-COEFFICIENT CURVE shows the ratio of maximum instantaneous junction-to-case temperature rise for any pulse width and duty cycle to the rise which occurs at 100% duty cycle. Use of this curve is best explained by the equations and example below. See Table II for a definition of terms.

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_{T(avg)} = \frac{T_{J(avg)} - T_A}{\theta_{J-A}}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

Heat Sink = 8" x 8" x 1/8" copper,

$\theta_{HS-A} = 1.8$ C°/w

with DC-11 grease, $\theta_{C-HS} = 0.45$ C°/w

$T_{J(max)}$ (design limit) = 100°C

$T_A = 35$ °C

d = 20% (0.2)

$t_w = 0.1$ msec

SOLUTION:

From Figure 12, Peak-Power Coefficient,

K = 0.24, and by use of equation No. 3

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{100 - 35}{0.2(0.45 + 1.8) + 0.24(0.5)} = 114 \text{ w}$$

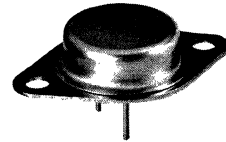
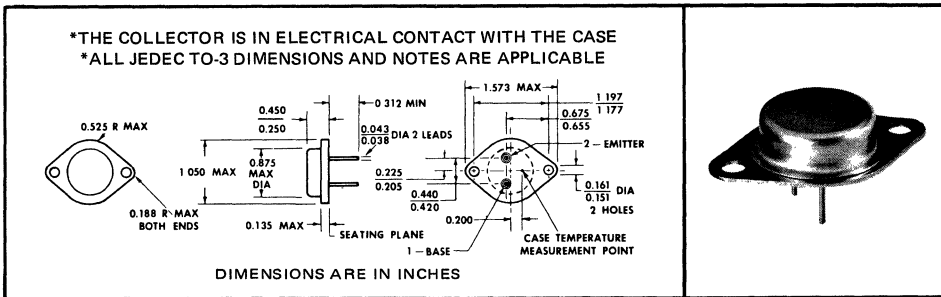
TYPES 2N1529 THRU 2N1548 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

TYPES 2N1529 THRU 2N1548
BULLETIN NO. DL-5 6810919, NOVEMBER, 1968

FOR HIGH-POWER SWITCHING AND AMPLIFIER APPLICATIONS

mechanical data

These transistors are in precision welded, hermetically sealed enclosures. The mounting base provides an excellent heat path from the collector junction to a heat sink. The mounting base and heat sink must be in intimate contact for maximum heat transfer. Extreme cleanliness and the absence of flux during the assembly process prevents sealed-in contamination.



6

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N1529	2N1530	2N1531	2N1532	2N1533
Collector-Base Voltage	-40 V*	-60 V*	-80 V*	-100 V*	-120 V*
Collector-Emitter Voltage (See Note 1)	-30 V*	-45 V*	-60 V*	-75 V*	-90 V*
Emitter-Base Voltage	-20 V*	-30 V*	-40 V*	-50 V*	-60 V*
Continuous Collector Current	←—————			-5 A*	—————→
Continuous Emitter Current	←—————			5 A*	—————→
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	←—————			106 W	—————→
Operating Collector Junction Temperature	←—————			{ 100°C* }	{ 110°C† } —————→
Storage Temperature Range	←—————			-65°C to 100°C*	—————→

NOTES: 1. This value applies when base-emitter diode is short-circuited.
2. Derate linearly to 110°C case temperature at the rate of 1.25 W/deg.

*Indicates JEDEC registered data
† This value is guaranteed by Texas Instruments in addition to the JEDEC registered value which is also shown.

TYPES 2N1529 THRU 2N1548

P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

2N1529 THRU 2N1533

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYPE	MIN	MAX	UNIT
*V _{(BR)CEO} Collector-Emmitter Breakdown Voltage	I _C = -500 mA, I _B = 0		2N1529 2N1530 2N1531 2N1532 2N1533	-20 -30 -40 -50 -60		V
*V _{(BR)CES} Collector-Emmitter Breakdown Voltage	I _C = -500 mA, V _{BE} = 0		2N1529 2N1530 2N1531 2N1532 2N1533	-30 -45 -60 -75 -90		V
*V _{(BR)EBO} Emmitter-Base Breakdown Voltage	I _E = -25 mA, I _C = 0		2N1529 2N1530 2N1531 2N1532 2N1533	-20 -30 -40 -50 -60		V
*I _{CBO} Collector Cutoff Current	V _{CB} = -2 V	I _E = 0	All		-200	μA
*I _{CBO} Collector Cutoff Current	V _{CB} = -25 V V _{CB} = -40 V V _{CB} = -55 V V _{CB} = -65 V V _{CB} = -80 V	I _E = 0	2N1529 2N1530 2N1531 2N1532 2N1533		-2	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -40 V V _{CB} = -60 V V _{CB} = -80 V V _{CB} = -100 V V _{CB} = -120 V	I _E = 0	2N1529 2N1530 2N1531 2N1532 2N1533		-20	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -15 V V _{CB} = -22.5 V V _{CB} = -30 V V _{CB} = -37.5 V V _{CB} = -45 V	I _E = 0, T _C = 90°C	2N1529 2N1530 2N1531 2N1532 2N1533		-20	mA
*I _{CEV} Collector Cutoff Current	V _{CE} = -40 V V _{CE} = -60 V V _{CE} = -80 V V _{CE} = -100 V V _{CE} = -120 V	V _{BE} = 1 V	2N1529 2N1530 2N1531 2N1532 2N1533		-20	mA
*I _{EBO} Emmitter Cutoff Current	V _{EB} = -12 V	I _C = 0	All		-0.5	mA
*h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -2 V	I _C = -3 A	All	20	40	
*g _{FE} Static Common-Emmitter Forward Transfer Conductance	V _{CE} = -2 V	I _C = -3 A	All	1.2		mho
*V _{BE} Base-Emmitter Voltage	I _B = -300 mA	I _C = -3 A	All		-1.7	V
*V _{CE(sat)} Collector-Emmitter Saturation Voltage	I _B = -300 mA	I _C = -3 A	All		-1.5	V
*f _{hfo} Common-Emmitter Forward Current Transfer Ratio Cutoff Frequency	V _{CE} = -2 V	I _C = -3 A	All	2		kHz
f _T Transition Frequency	V _{CE} = -2 V	I _C = -1 A, See Note 4	All	200		kHz

thermal characteristics

PARAMETER	TYPE	MAX	UNIT
*θ _{J-C} Junction-to-Case Thermal Resistance	All	0.8	deg/W

NOTE: 4. To obtain f_T, the |h_{re}| response with frequency is extrapolated at the rate of -6 dB/octave from f = 100 kHz to the frequency at which |h_{re}| = 1.

*Indicates JEDEC registered data

TYPES 2N1529 THRU 2N1548

P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

2N1534 THRU 2N1538

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYPE	MIN	MAX	UNIT
*V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = -500 mA, I _B = 0		2N1534 2N1535 2N1536 2N1537 2N1538	-20 -30 -40 -50 -60		V
*V _{(BR)CES} Collector-Emitter Breakdown Voltage	I _C = -500 mA, V _{BE} = 0		2N1534 2N1535 2N1536 2N1537 2N1538	-30 -45 -60 -75 -90		V
*V _{(BR)EBO} Emitter-Base Breakdown Voltage	I _E = -25 mA, I _C = 0		2N1534 2N1535 2N1536 2N1537 2N1538	-20 -30 -40 -50 -60		V
*I _{CBO} Collector Cutoff Current	V _{CB} = -2 V	I _E = 0	All		-200	μA
*I _{CBO} Collector Cutoff Current	V _{CB} = -25 V V _{CB} = -40 V V _{CB} = -55 V V _{CB} = -65 V V _{CB} = -80 V	I _E = 0	2N1534 2N1535 2N1536 2N1537 2N1538		-2	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -40 V V _{CB} = -60 V V _{CB} = -80 V V _{CB} = -100 V V _{CB} = -120 V	I _E = 0	2N1534 2N1535 2N1536 2N1537 2N1538		-20	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -15 V V _{CB} = -22.5 V V _{CB} = -30 V V _{CB} = -37.5 V V _{CB} = -45 V	I _E = 0, T _C = 90°C	2N1534 2N1535 2N1536 2N1537 2N1538		-20	mA
*I _{CEV} Collector Cutoff Current	V _{CE} = -40 V V _{CE} = -60 V V _{CE} = -80 V V _{CE} = -100 V V _{CE} = -120 V	V _{BE} = 1 V	2N1534 2N1535 2N1536 2N1537 2N1538		-20	mA
*I _{EBO} Emitter Cutoff Current	V _{EB} = -12 V	I _C = 0	All		-0.5	mA
*h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -2 V	I _C = -3 A	All	35	70	
*g _{FE} Static Common-Emitter Forward Transfer Conductance	V _{CE} = -2 V	I _C = -3 A	All	1.5		mho
*V _{BE} Base-Emitter Voltage	I _B = -300 mA	I _C = -3 A	All		-1.5	V
*V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = -300 mA	I _C = -3 A	All		-1.2	V
*f _{hfe} Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	V _{CE} = -2 V	I _C = -3 A	All	2		kHz
f _T Transition Frequency	V _{CE} = -2 V	I _C = -1 A, See Note 4	All	200		kHz

thermal characteristics

PARAMETER	TYPE	MAX	UNIT
*θ _{J-C} Junction-to-Case Thermal Resistance	All	0.8	deg/W

NOTE: 4. To obtain f_T, the |h_{re}| response with frequency is extrapolated at the rate of -6 dB/octave from f = 100 kHz to the frequency at which |h_{re}| = 1.

*Indicates JEDEC registered data

TYPES 2N1529 THRU 2N1548

P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

2N1539 THRU 2N1543

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYPE	MIN	MAX	UNIT
*V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = -500 mA, I _B = 0		2N1539 2N1540 2N1541 2N1542 2N1543	-20 -30 -40 -50 -60		V
*V _{(BR)CES} Collector-Emitter Breakdown Voltage	I _C = -500 mA, V _{BE} = 0		2N1539 2N1540 2N1541 2N1542 2N1543	-30 -45 -60 -75 -90		V
*V _{(BR)EBO} Emitter-Base Breakdown Voltage	I _E = -25 mA, I _C = 0		2N1539 2N1540 2N1541 2N1542 2N1543	-20 -30 -40 -50 -60		V
*I _{CBO} Collector Cutoff Current	V _{CB} = -2 V	I _E = 0	All		-200	μA
*I _{CBO} Collector Cutoff Current	V _{CB} = -25 V V _{CB} = -40 V V _{CB} = -55 V V _{CB} = -65 V V _{CB} = -80 V	I _E = 0	2N1539 2N1540 2N1541 2N1542 2N1543		-2	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -40 V V _{CB} = -60 V V _{CB} = -80 V V _{CB} = -100 V V _{CB} = -120 V	I _E = 0	2N1539 2N1540 2N1541 2N1542 2N1543		-20	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -15 V V _{CB} = -22.5 V V _{CB} = -30 V V _{CB} = -37.5 V V _{CB} = -45 V	I _E = 0, T _C = 90°C	2N1539 2N1540 2N1541 2N1542 2N1543		-20	mA
*I _{CEV} Collector Cutoff Current	V _{CE} = -40 V V _{CE} = -60 V V _{CE} = -80 V V _{CE} = -100 V V _{CE} = -120 V	V _{BE} = 1 V	2N1539 2N1540 2N1541 2N1542 2N1543		-20	mA
*I _{EBO} Emitter Cutoff Current	V _{EB} = -12 V	I _C = 0	All		-0.5	mA
*h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -2 V	I _C = -3 A	All	50	100	
*g _{FE} Static Common-Emitter Forward Transfer Conductance	V _{CE} = -2 V	I _C = -3 A	All	3		mho
*V _{BE} Base-Emitter Voltage	I _B = -300 mA	I _C = -3 A	All		-0.7	V
*V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = -300 mA	I _C = -3 A	All		-0.3	V
*f _{hfe} Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	V _{CE} = -2 V	I _C = -5 A	All	1		kHz
f _T Transition Frequency	V _{CE} = -2 V	I _C = -1 A, See Note 4	All	200		kHz

thermal characteristics

PARAMETER	TYPE	MAX	UNIT
*θ _{J-C} Junction-to-Case Thermal Resistance	All	0.8	deg/W

NOTE: 4. To obtain f_T, the |h_{re}| response with frequency is extrapolated at the rate of -6 dB/octave from f = 100 kHz to the frequency at which |h_{re}| = 1.

*Indicates JEDEC registered data

TYPES 2N1529 THRU 2N1548 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

2N1544 THRU 2N1548

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPE	MIN	MAX	UNIT
*V _{(BR)CEO} Collector-Emitter Breakdown Voltage	I _C = -500 mA, I _B = 0	2N1544 2N1545 2N1546 2N1547 2N1548	-20 -30 -40 -50 -60		V
*V _{(BR)CES} Collector-Emitter Breakdown Voltage	I _C = -500 mA, V _{BE} = 0	2N1544 2N1545 2N1546 2N1547 2N1548	-30 -45 -60 -75 -90		V
*V _{(BR)EBO} Emitter-Base Breakdown Voltage	I _E = -20 mA, I _C = 0	2N1544 2N1545 2N1546 2N1547 2N1548	-20 -30 -40 -50 -60		V
*I _{CBO} Collector Cutoff Current	V _{CB} = -2 V, I _E = 0	All		-200	μA
*I _{CBO} Collector Cutoff Current	V _{CB} = -25 V V _{CB} = -40 V V _{CB} = -55 V V _{CB} = -65 V V _{CB} = -80 V I _E = 0	2N1544 2N1545 2N1546 2N1547 2N1548		-2	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -40 V V _{CB} = -60 V V _{CB} = -80 V V _{CB} = -100 V V _{CB} = -120 V I _E = 0	2N1544 2N1545 2N1546 2N1547 2N1548		-20	mA
*I _{CBO} Collector Cutoff Current	V _{CB} = -15 V V _{CB} = -22.5 V V _{CB} = -30 V V _{CB} = -37.5 V V _{CB} = -45 V I _E = 0, T _C = 90°C	2N1544 2N1545 2N1546 2N1547 2N1548		-20	mA
*I _{CEV} Collector Cutoff Current	V _{CE} = -40 V V _{CE} = -60 V V _{CE} = -80 V V _{CE} = -100 V V _{CE} = -120 V V _{BE} = 1 V	2N1544 2N1545 2N1546 2N1547 2N1548		-20	mA
*I _{EBO} Emitter Cutoff Current	V _{EB} = -12 V, I _C = 0	All		-0.5	mA
*h _{FE} Static Forward Current Transfer Ratio	V _{CE} = -2 V, I _C = -3 A	All	75	150	
*g _{FE} Static Common-Emitter Forward Transfer Conductance	V _{CE} = -2 V, I _C = -3 A	All	4		mho
*V _{BE} Base-Emitter Voltage	I _B = -300 mA, I _C = -3 A	All		-0.6	V
*V _{CE(sat)} Collector-Emitter Saturation Voltage	I _B = -300 mA, I _C = -3 A	All		-0.2	V
*f _{hfo} Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	V _{CE} = -2 V, I _C = -5 A	All	1		kHz
f _T Transition Frequency	V _{CE} = -2 V, I _C = -1 A, See Note 4	All	200		kHz

thermal characteristics

PARAMETER	TYPE	MAX	UNIT
*θ _{J-C} Junction-to-Case Thermal Resistance	All	0.8	deg/W

NOTE: 4. To obtain f_T, the |h_{re}| response with frequency is extrapolated at the rate of -6 dB/octave from f = 100 kHz to the frequency at which |h_{re}| = 1.

*Indicates JEDEC registered data

TYPES 2N1529 THRU 2N1548

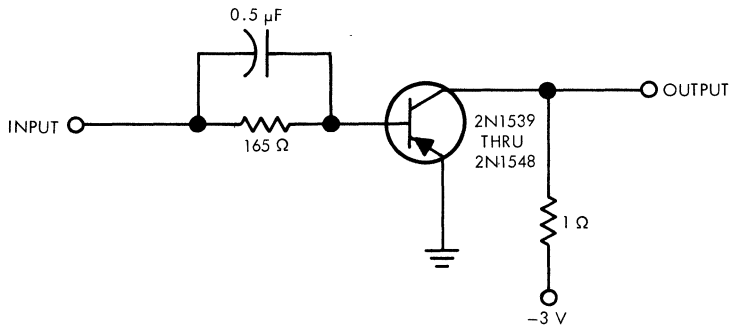
P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

2N1539 THRU 2N1548

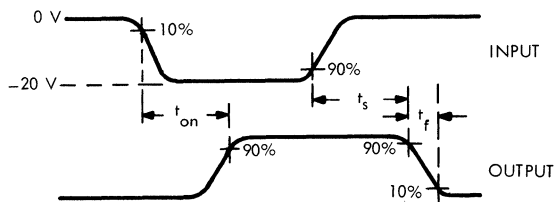
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{on} Turn-On Time	$I_C \approx 3 \text{ A}$, $R_L = 1 \Omega$, See Figure 1	5	μs
t_s Storage Time		3	μs
t_f Fall Time		5	μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: a. The input pulse is supplied by a generator with the following characteristics: $t_r \leq 0.1 \mu\text{s}$, $t_p = 50 \mu\text{s}$, duty cycle $\leq 10\%$.
 b. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 0.1 \mu\text{s}$, $R_{in} \geq 100 \text{ k}\Omega$, $C_{in} \leq 20 \text{ pF}$.

FIGURE 1

TYPES 2N1529 THRU 2N1548 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

THEMAL INFORMATION

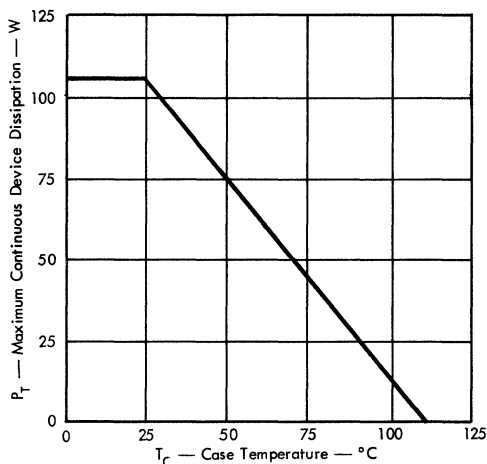


FIGURE 2

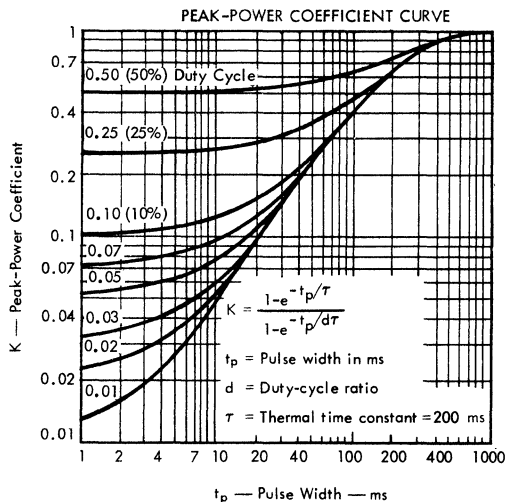


FIGURE 3

SYMBOL DEFINITION

SYMBOL	DEFINITION	VALUE	UNIT
$P_{T(av)}$	Average Power Dissipation		W
$P_{T(max)}$	Peak Power Dissipation		W
θ_{J-C}	Junction-to-Case Thermal Resistance	0.8	deg/W
θ_{C-HS}	Case-to-Heat-Sink Thermal Resistance		deg/W
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance		deg/W
T_A	Free-Air Temperature		°C
T_C	Case Temperature		°C
$T_{J(av)}$	Average Junction Temperature	≤ 110	°C
$T_{J(max)}$	Peak Junction Temperature	≤ 110	°C
K	Peak-Power Coefficient	See Figure 3	
t_p	Pulse Width		ms
d	Duty-Cycle Ratio		

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_{T(av)} = \frac{T_{J(av)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}} \quad \text{for } 25^\circ\text{C} \leq T_C \leq 110^\circ\text{C} \quad \text{as in Figure 2}$$

Equation No. 2 — Application: Peak power dissipation, heat sink used.

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}} \quad \text{for } 25^\circ\text{C} \leq T_C \leq 110^\circ\text{C}$$

Example — Find $P_{T(max)}$ (design limit)

OPERATING CONDITIONS:

$$\theta_{C-HS} + \theta_{HS-A} = 2.25 \text{ deg/W (From information supplied with heat sink.)}$$

$$T_{J(av)} \text{ (design limit)} = 110^\circ\text{C}$$

$$T_A = 50^\circ\text{C}$$

$$d = 10\% (0.1)$$

$$t_p = 10 \text{ ms}$$

Solution:

From Figure 3, Peak-Power Coefficient

$$K = 0.125 \text{ and by use of equation No. 2}$$

$$P_{T(max)} = \frac{T_{J(max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_{T(max)} = \frac{110 - 50}{0.1(2.25) + 0.125(0.8)} = 184 \text{ W}$$

6

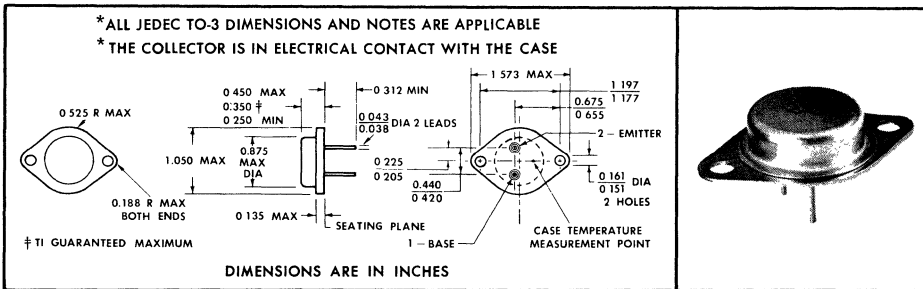
TYPES 2N1907, 2N1908 P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

TYPES 2N1907, 2N1908
BULLETIN NO. DL-5 644426, FEBRUARY 1964

HIGH-FREQUENCY POWER TRANSISTORS for MILITARY AND INDUSTRIAL APPLICATIONS

mechanical data

These transistors are in precision welded, hermetically sealed enclosures. The mounting base provides an excellent heat path from the collector junction to a heat sink. The mounting base and heat sink must be in intimate contact for maximum heat transfer. Extreme cleanliness during the assembly process prevents sealed-in contamination. The approximate weight of the unit is 18 grams.



6

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N1907	2N1908
Collector-Base Voltage	100 v*	130 v*
Collector-Emitter Voltage (See Note 1)	40 v	50 v
Emitter-Base Voltage	← { 1.5 v* } → ← { 2.0 v† } →	
Collector Current	← 20 a* →	
Base Current	← 3 a* →	
Safe Continuous Operating Region	See Figures 15 and 16	
Total Device Dissipation at (or below) 70°C Case Temperature (See Note 2)	← 60 w →	
Peak Collector Power Dissipation at (or below) 25°C		
Case Temperature (See Note 3)	800 w	1000 w
Operating Collector Junction Temperature	← 100°C* →	
Storage Temperature Range	{ -55°C to +100°C* } { -55°C to +110°C† }	

NOTES: 1. This value applies when the base-emitter diode is open-circuited.

2. Derate linearly to 100°C case temperature at the rate of 2 w/°C. This corresponds to the JEDEC registered maximum value of thermal resistance, θ_{J-C} , 0.5 °C/w.

3. These values apply for rectangular waveshape. See Figure 14 for allowable pulse width and duty cycle combinations. Derate linearly to 100°C case temperature.

*Indicates JEDEC registered data.

†Texas Instruments guarantees this value in addition to the JEDEC registered value which is also shown.

TYPES 2N1907, 2N1908

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N1907		2N1908		UNIT
		MIN	MAX	MIN	MAX	
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = -10 \text{ ma}$, $I_E = 0$	-100		-130		v
BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = -200 \text{ ma}$, $I_B = 0$, See Note 4	-40*		-50*		v
BV_{EBO} Emitter-Base Breakdown Voltage	$I_E = -2 \text{ ma}$, $I_C = 0$	-1.5		-1.5		v
	$I_E = -10 \text{ ma}$, $I_C = 0$	-2.0		-2.0		
I_{CBO} Collector Cutoff Current	$V_{CB} = -3 \text{ v}$, $I_E = 0$	-0.5*				ma
	$V_{CB} = -75 \text{ v}$, $I_E = 0$	-0.3†				
	$V_{CB} = -100 \text{ v}$, $I_E = 0$	-2.0				
	$V_{CB} = -100 \text{ v}$, $I_E = 0$	-10*				
	$V_{CB} = -75 \text{ v}$, $I_E = 0$, $T_C = +70^\circ\text{C}$	-12				
	$V_{CB} = -3 \text{ v}$, $I_E = 0$			-0.5*		
	$V_{CB} = -100 \text{ v}$, $I_E = 0$			-0.3†		
	$V_{CB} = -130 \text{ v}$, $I_E = 0$			-2.0		
I_{CEX} Collector Cutoff Current	$V_{CE} = -75 \text{ v}$, $V_{BE} = +0.2 \text{ v}$	-2.0				ma
	$V_{CE} = -100 \text{ v}$, $V_{BE} = +0.2 \text{ v}$			-2.0		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -0.5 \text{ v}$, $I_C = 0$	-0.2*		-0.2*		ma
	$V_{EB} = -1.5 \text{ v}$, $I_C = 0$	-0.1†		-0.1†		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ v}$, $I_C = -1 \text{ a}$, See Note 4	80		80		
	$V_{CE} = -1.5 \text{ v}$, $I_C = -5 \text{ a}$, See Note 4	90		90		
	$V_{CE} = -1.5 \text{ v}$, $I_C = -10 \text{ a}$, See Note 4	30	170	30	170	
	$V_{CE} = -1.5 \text{ v}$, $I_C = -15 \text{ a}$, See Note 4	20		20		
	$V_{CE} = -1.5 \text{ v}$, $I_C = -10 \text{ a}$, $T_C = -55^\circ\text{C}$, See Note 4	30		30		
	$V_{CE} = -1.5 \text{ v}$, $I_C = -10 \text{ a}$, $T_C = +70^\circ\text{C}$, See Note 4	15	100	15	100	
V_{BE} Base-Emitter Voltage	$I_B = -100 \text{ ma}$, $I_C = -1 \text{ a}$, See Note 4	-0.4		-0.4		v
	$I_B = -500 \text{ ma}$, $I_C = -5 \text{ a}$, See Note 4	-0.7		-0.7		
	$I_B = -1 \text{ a}$, $I_C = -10 \text{ a}$, See Note 4	-1.0		-1.0		
	$I_B = -1.5 \text{ a}$, $I_C = -15 \text{ a}$, See Note 4	-1.5		-1.5		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -100 \text{ ma}$, $I_C = -1 \text{ a}$, See Note 4	-0.2		-0.2		v
	$I_B = -500 \text{ ma}$, $I_C = -5 \text{ a}$, See Note 4	-0.4		-0.4		
	$I_B = -1 \text{ a}$, $I_C = -10 \text{ a}$, See Note 4	-0.7		-0.7		
	$I_B = -1.5 \text{ a}$, $I_C = -15 \text{ a}$, See Note 4	-1.0*		-1.0*		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -15 \text{ v}$, $I_C = -0.5 \text{ a}$, $f = 10 \text{ mc}$	1.0*		1.0*		
		2.0†		2.0†		

NOTE 4: If these parameters are measured without a heat sink, d-c collector current must not be applied longer than 250 msec.

*Indicates JEDEC registered data.

†Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

TYPES 2N1907, 2N1908

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS †	TYPICAL	UNIT
t_d Delay Time	$I_C = -10a, I_{B(1)} = -1.33a, I_{B(2)} = 1.33a,$ $V_{BE(off)} = 2\text{ v}, R_L = 2\ \Omega,$ See Figure 1	0.1	μsec
t_r Rise Time		0.8	μsec
t_s Storage Time		2.5	μsec
t_f Fall Time		1.0	μsec
t_T Total Switching Time		4.4	μsec

† Voltage and current values are nominal; exact values vary slightly with device parameters.

PARAMETER MEASUREMENT INFORMATION

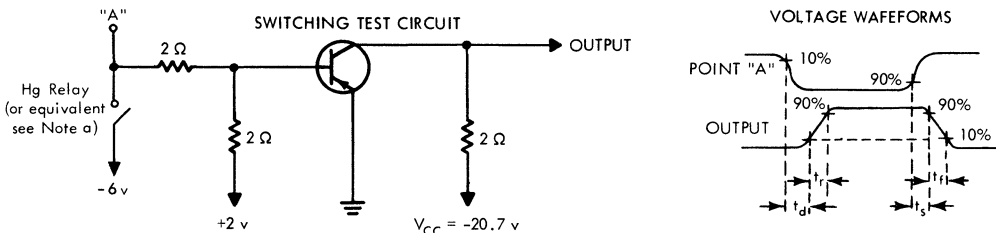


FIGURE 1

NOTES: a. The pulse at point "A" has the following characteristics: $t_r \leq 20\text{ nsec}$, $t_f \leq 20\text{ nsec}$, $PW \geq 50\ \mu\text{sec}$, duty cycle $\leq 5\%$.
 b. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15\text{ nsec}$, $R_{in} \geq 1\text{ M}\Omega$, $C_{in} \leq 20\text{ pf}$.

6

TYPICAL CHARACTERISTICS

COMMON-EMITTER COLLECTOR CHARACTERISTICS
(Low-Voltage Region)

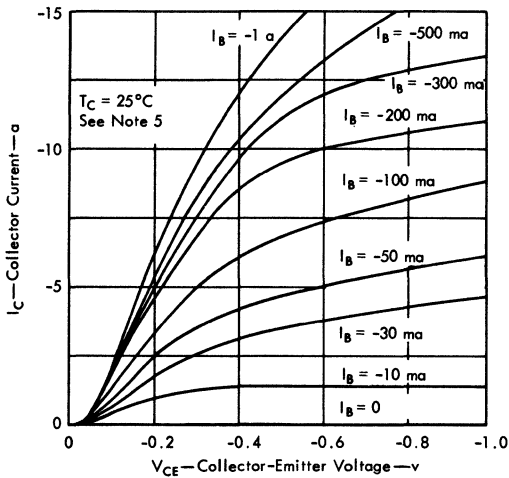


FIGURE 2

COMMON-EMITTER COLLECTOR CHARACTERISTICS
(High-Voltage Region)

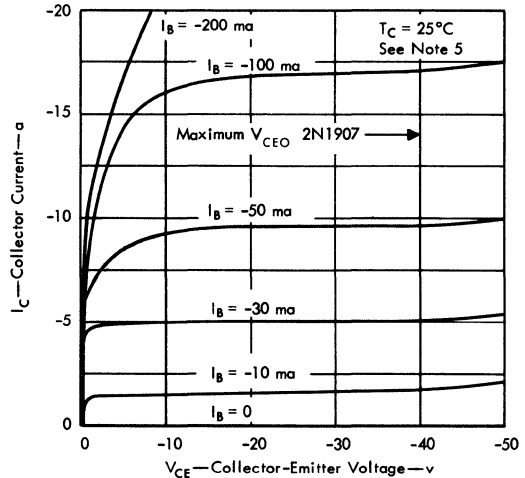


FIGURE 3

NOTE 5: These characteristics were measured using pulse techniques. $PW = 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

TYPES 2N1907, 2N1908

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

TYPICAL CHARACTERISTICS

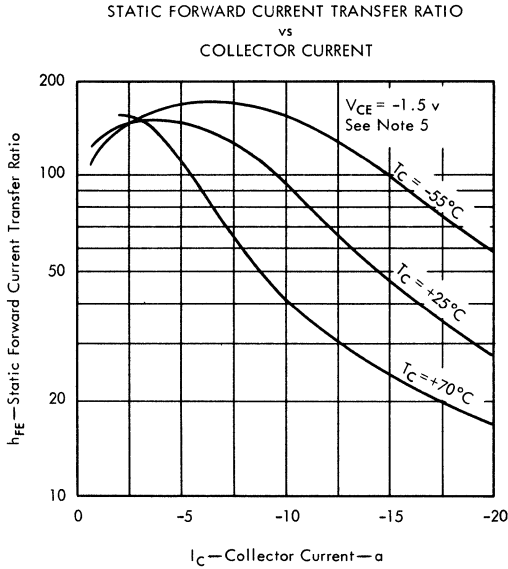


FIGURE 4

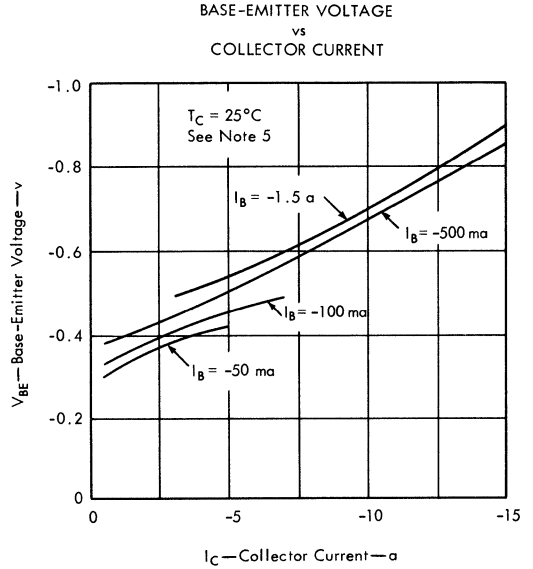


FIGURE 5

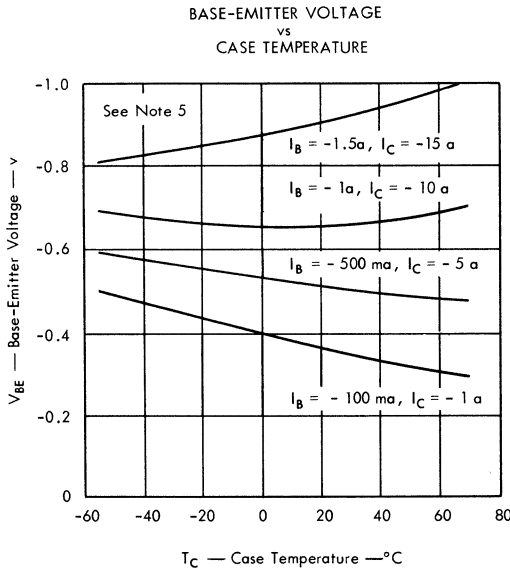


FIGURE 6

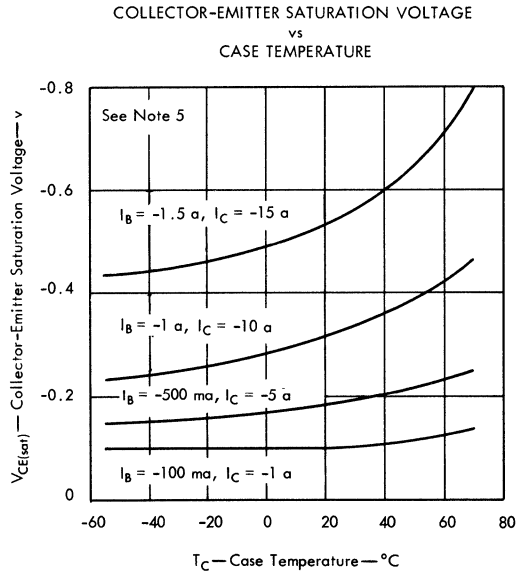


FIGURE 7

NOTE 5: These characteristics were measured using pulse techniques. $PW = 300 \mu sec.$, Duty Cycle $\leq 2\%$.

TYPES 2N1907, 2N1908 P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

TYPICAL CHARACTERISTICS

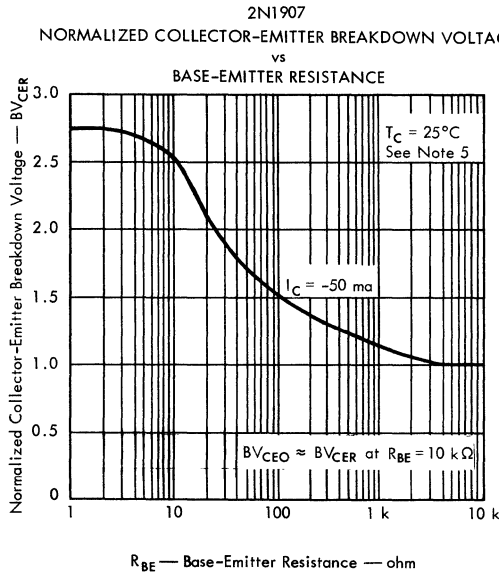


FIGURE 8

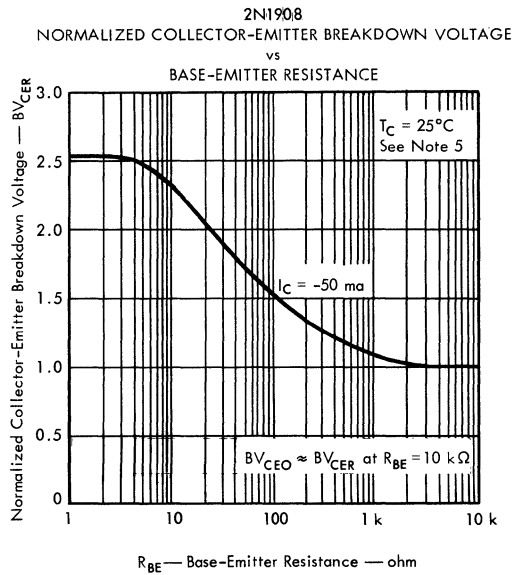


FIGURE 9

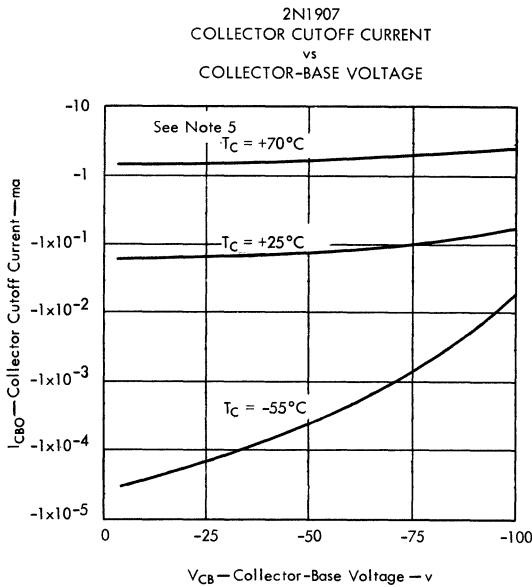


FIGURE 10

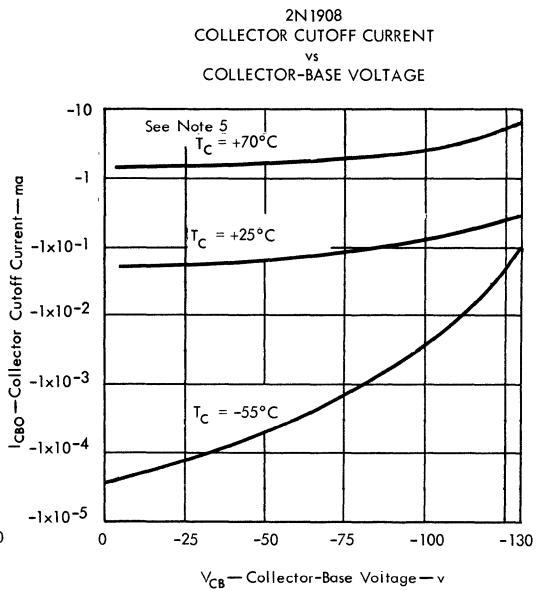


FIGURE 11

NOTE 5: These characteristics were measured using pulse techniques. $PW = 300 \mu\text{sec.}$, Duty Cycle $\leq 2\%$.

TYPES 2N1907, 2N1908

P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

THERMAL CHARACTERISTICS

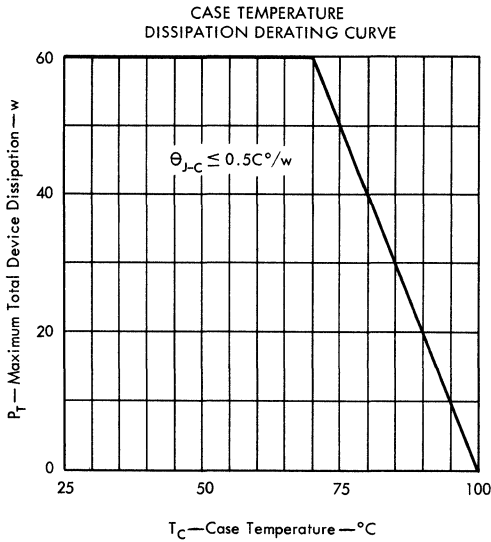


FIGURE 12

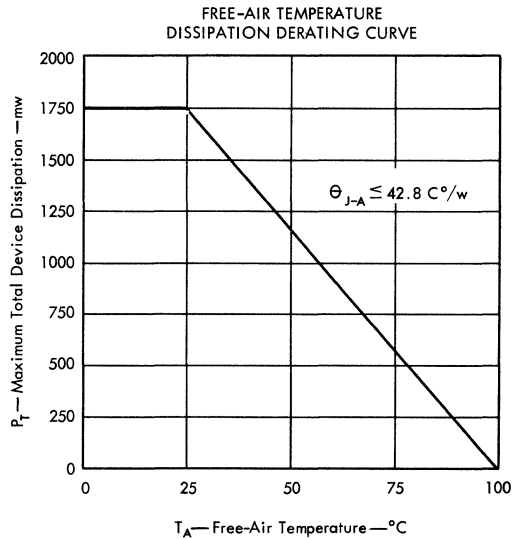


FIGURE 13

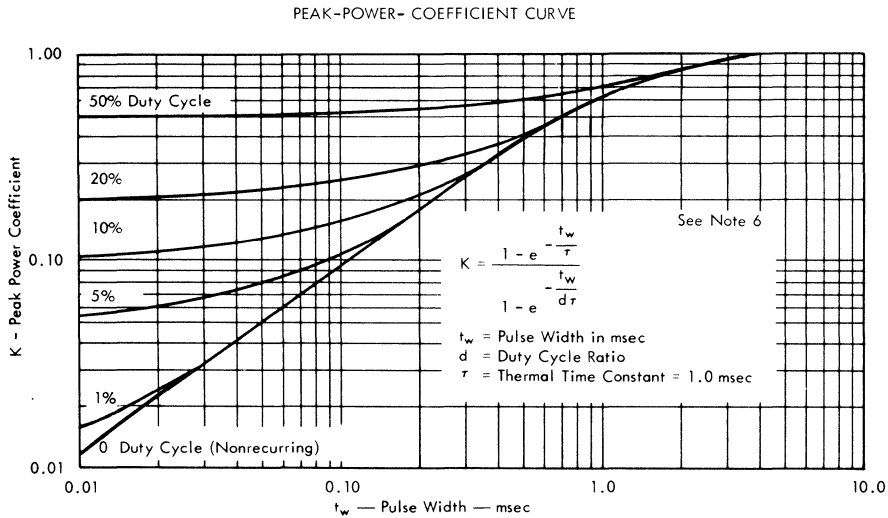


FIGURE 14

NOTE 6: When $t_w > 3.0$ msec or $d > 0.5$ (50%), operation must be confined to the continuous operating regions of Figure 15 or 16.

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TYPES 2N1907, 2N1908 P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

MAXIMUM SAFE OPERATING REGIONS

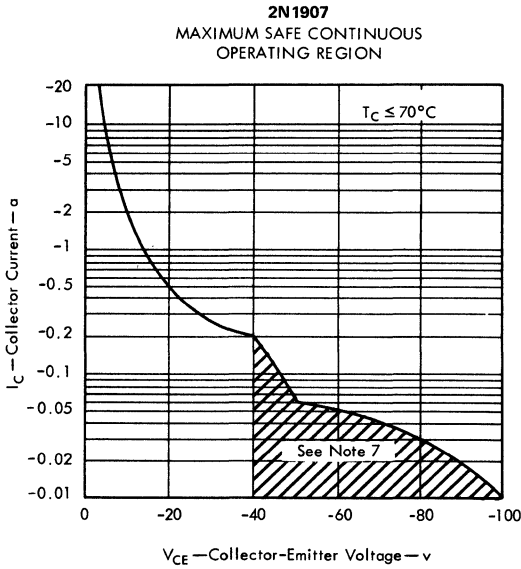


FIGURE 15

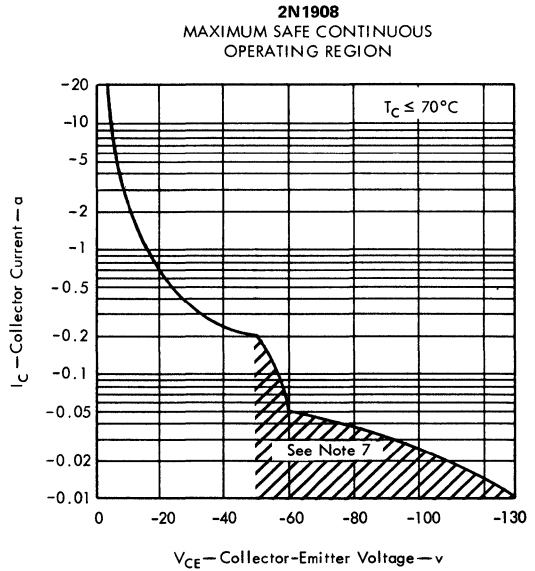


FIGURE 16

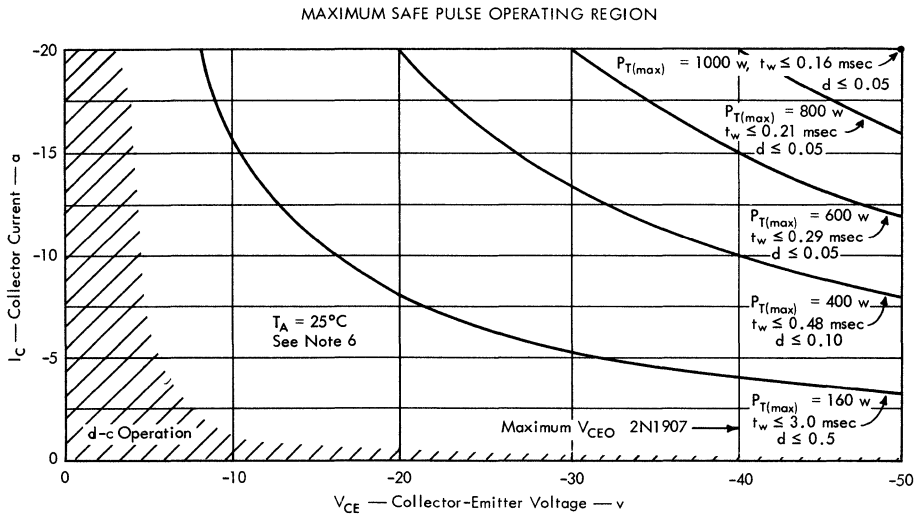


FIGURE 17

NOTES: 6. When $t_w \geq 3.0 \text{ msec}$ or $d \geq 0.5$ (50%), operation must be confined to the continuous operating regions of Figure 15 or 16.

7. Operation in this region is permissible when base-emitter resistance $R_{BE} \leq 5 \Omega$.

TYPES 2N1907, 2N1908 P-N-P ALLOY-DIFFUSED GERMANIUM POWER TRANSISTORS

THERMAL INFORMATION

TABLE I

HEAT SINK		$\dagger\theta_{HS-A}$
Type	Dimensions	
Bright Copper	4" x 4" x 1/8"	3.8 C°/w
	6" x 6" x 1/8"	2.2 C°/w
	8" x 8" x 1/8"	1.8 C°/w
	10" x 10" x 1/8"	1.4 C°/w
Bright Aluminum	4" x 4" x 1/8"	6.5 C°/w
	6" x 6" x 1/8"	4.5 C°/w
	8" x 8" x 1/8"	3.5 C°/w
	10" x 10" x 1/8"	2.8 C°/w
Delbert Blinn #113 or Modine 1E1155B, Unfinished (or Equivalents)		3.7 C°/w
Delbert Blinn #113 or Modine 1E1155B, Black Anodized (or Equivalents)		3.2 C°/w

$\dagger\theta_{HS-A}$ are typical values based on convection cooling; plates and fins mounted in vertical position.

\ddagger All transistors mounted in the center of the heat sink with two 6-32 screws at 6 inch - pounds of torque.

TABLE II

SYMBOL	DEFINITION	UNIT	VALUE
P_T (avg)	Average Power Dissipation	w	
P_T (max)	Peak Power Dissipation	w	
θ_{J-C}	Junction-to-Case Thermal Resistance	C°/w	0.5
θ_{J-A}	Junction-to-Free-Air Thermal Resistance	C°/w	42.8
θ_{C-A}	Case-to-Free-Air Thermal Resistance	C°/w	42.3
$\ddagger\theta_{C-HS}$	Case-to-Heat-Sink Thermal Resistance Typical With Dry Mounting Base	C°/w	0.65
	Typical with DC-11 Silicone Grease		0.45
θ_{HS-A}	Heat-Sink-to-Free-Air Thermal Resistance	C°/w	see Table I
T_A	Free-Air Temperature	C°	
T_J (avg)	Average Junction Temperature	C°	≤ 100
T_J (max)	Peak Junction Temperature	C°	≤ 100
T_C	Case Temperature	C°	
K	Peak-Power Coefficient		see Fig. 14
t_w	Pulse Width	msec	
t_p	Pulse Period	msec	
	Duty Cycle Ratio (t_w/t_p)		

For d-c operation, these transistors are voltage limited as well as thermally limited. Figure 12 and Figure 15 or 16 are recommended as a guide for selecting safe voltage and current combinations.

These transistors have a very low thermal resistance that may be fully utilized in a pulse-power application provided the pulse width is equal to (or less than) 3 milliseconds. If the power pulse is longer than 3 milliseconds, then the operating path is limited to the safe operating region described by Figure 12 and Figure 15 or 16.

The PEAK-POWER-COEFFICIENT CURVE shows the ratio of maximum instantaneous junction-to-case temperature rise for any pulse width and duty cycle to the rise which occurs at 100% duty cycle. Use of this curve is best explained by the equations and example below. See Table II for a definition of terms.

Equation No. 1 — Application: d-c power dissipation, heat sink used.

$$P_T \text{ (avg)} = \frac{T_J \text{ (avg)} - T_A}{\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A}}$$

Equation No. 2 — Application: d-c power dissipation, no heat sink used.

$$P_T \text{ (avg)} = \frac{T_J \text{ (avg)} - T_A}{\theta_{J-A}}$$

Equation No. 3 — Application: Peak power dissipation, heat sink used.

$$P_T \text{ (max)} = \frac{T_J \text{ (max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

Equation No. 4 — Application: Peak power dissipation, no heat sink used.

$$P_T \text{ (max)} = \frac{T_J \text{ (max)} - T_A}{d\theta_{C-A} + K\theta_{J-C}}$$

Example — Find P_T (max) (design limit)

OPERATING CONDITIONS:

Heat Sink = 8" x 8" x 1/8" copper,

$\theta_{HS-A} = 1.8$ C°/w

with DC-11 grease, $\theta_{C-HS} = 0.45$ C°/w

T_J (max) (design limit) = 100°C

$T_A = 35$ °C

$d = 20\%$ (0.2)

$t_w = 0.1$ msec

SOLUTION:

From Figure 14 Peak-Power Coefficient,

$K = 0.24$, and by use of equation No. 3

$$P_T \text{ (max)} = \frac{T_J \text{ (max)} - T_A}{d(\theta_{C-HS} + \theta_{HS-A}) + K\theta_{J-C}}$$

$$P_T \text{ (max)} = \frac{100 - 35}{0.2(0.45 + 1.8) + 0.24(0.5)} = 114 \text{ w}$$

TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPES 2N2659 THRU 2N2670
BULLETIN NO. DL-5 684128, AUGUST 1963
REVISED FEBRUARY 1968

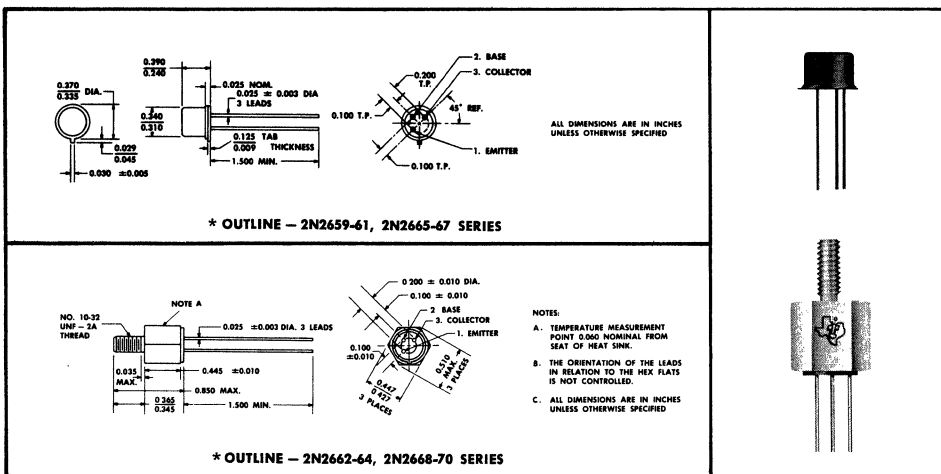
50-, 70-, or 90-VOLT UNITS
15 WATTS at 25°C CASE TEMPERATURE
Choice of TO-5 or Stud Package
Guaranteed Beta at 1 amp and 500 ma I_c

Guaranteed I_{CEX} at 85°C
LOW r_{CS} • LOW I_{CBO} • LOW V_{BE}
for
RELAY DRIVERS • PULSE AMPLIFIERS
SERVO AMPLIFIERS • AUDIO AMPLIFIERS

mechanical data

The transistors are in hermetically sealed, resistance-welded cases with glass-to-metal seals between case and leads. The 2N2659-2N2661 and 2N2665-2N2667 are in a round TO-5 package weighing approximately 2.4 grams. The 2N2662-2N2664 and 2N2668-2N2670 are in a stud package weighing approximately 5.4 grams.

*THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE



6

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N2659	2N2660	2N2661
Collector-Base Voltage	50 v	70 v	90 v
Collector-Emitter Voltage (See Note 1)	50 v	70 v	90 v
Emitter-Base Voltage	← 20 v →		
Collector Current	← 3 a →		
Base Current	← 1 a →		
Total Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 15 w →		
Operating Case Temperature Range	-55°C to 100°C		
Storage Temperature Range	-55°C to 100°C		

NOTES: 1. This value applies when base-emitter voltage $V_{BE} = +0.2$ v.
2. Derate linearly to 100°C case temperature at the rate of 200 mw/°C.

*Indicates JEDEC registered data.

TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TO-5 CASE	2N2659	2N2660	2N2661	UNIT
		STUD CASE	2N2662	2N2663	2N2664	
		MIN	MAX	MIN	MAX	
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = -600 \mu A, I_E = 0$		-50	-70	-90	v
* BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = -100 \text{ ma}, I_B = 0$, (See Note 3)		-30	-40	-50	v
* BV_{CES} Collector-Emitter Breakdown Voltage	$I_C = -50 \text{ ma}, V_{BE} = 0$, (See Note 3)		-50	-70	-90	v
I_{CBO} Collector Cutoff Current	$V_{CB} = -25 \text{ v}, I_E = 0$ $V_{CB} = -35 \text{ v}, I_E = 0$ $V_{CB} = -45 \text{ v}, I_E = 0$			-125		μA
* I_{CEO} Collector Cutoff Current	$V_{CE} = -15 \text{ v}, I_B = 0$ $V_{CE} = -20 \text{ v}, I_B = 0$ $V_{CE} = -25 \text{ v}, I_B = 0$			-20		ma
* I_{CEX} Collector Cutoff Current	$V_{CE} = -50 \text{ v}, V_{BE} = +0.2 \text{ v}$ $V_{CE} = -70 \text{ v}, V_{BE} = +0.2 \text{ v}$ $V_{CE} = -90 \text{ v}, V_{BE} = +0.2 \text{ v}$			-600		μA
* I_{CEX} Collector Cutoff Current	$V_{CE} = -25 \text{ v}, V_{BE} = +0.2 \text{ v}$ $V_{CE} = -35 \text{ v}, V_{BE} = +0.2 \text{ v}$ $V_{CE} = -45 \text{ v}, V_{BE} = +0.2 \text{ v}$			-125		μA
* I_{CEX} Collector Cutoff Current	$V_{CE} = -25 \text{ v}, V_{BE} = +0.2 \text{ v}, T_C = 85^\circ C$ $V_{CE} = -35 \text{ v}, V_{BE} = +0.2 \text{ v}, T_C = 85^\circ C$ $V_{CE} = -45 \text{ v}, V_{BE} = +0.2 \text{ v}, T_C = 85^\circ C$			-5		ma
* I_{EBO} Emitter Cutoff Current	$V_{EB} = -20 \text{ v}, I_C = 0$			-100		μA
* h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -0.5 \text{ v}, I_C = -1 \text{ a}$, (See Note 4) $V_{CE} = -0.5 \text{ v}, I_C = -500 \text{ ma}$, (See Note 4) $V_{CE} = -0.5 \text{ v}, I_C = -250 \text{ ma}$, (See Note 4)		15 30 90 125	15 30 90 125	15 30 90 125	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -0.5 \text{ v}, I_C = -500 \text{ ma}$, (See Note 4) $T_C = -55^\circ C$ $V_{CE} = -0.5 \text{ v}, I_C = -500 \text{ ma}$, (See Note 4) $T_C = +85^\circ C$		20 90 30 110	20 90 30 110	20 90 30 110	
* V_{BE} Base-Emitter Voltage	$V_{CE} = -0.5 \text{ v}, I_C = -500 \text{ ma}$, (See Note 4)			-0.6	-0.6	v
* $V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -50 \text{ ma}, I_C = -500 \text{ ma}$, (See Note 4) $I_B = -50 \text{ ma}, I_C = -500 \text{ ma}$, (See Note 4) $T_C = +85^\circ C$			-0.2 -0.25	-0.2 -0.25	v
* h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -3 \text{ v}, I_C = -100 \text{ ma}, f = 1 \text{ kc}$		30 120	30 120	30 120	
* h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -3 \text{ v}, I_C = -100 \text{ ma}, f = 140 \text{ kc}$		2.0	2.0	2.0	
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -3 \text{ v}, I_E = 0, f = 135 \text{ kc}$		100 (typical)	100 (typical)	100 (typical)	pf

NOTES: 3. These characteristics are measured by a 1/2 sine wave sweep method.

4. These measurements are made with voltage sensing contacts located 0.25 inches from header of transistor. Voltage sensing contacts are separate from current carrying contacts.

*Indicates JEDEC registered data.

TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TO-5 CASE	2N2665	2N2666	2N2667	UNIT
		STUD CASE	2N2668	2N2669	2N2670	
		MIN	MAX	MIN	MAX	
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = -600 \mu a, I_E = 0$		-50	-70	-90	v
* BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = -100 ma, I_B = 0$, (See Note 3)		-30	-40	-50	v
* BV_{CES} Collector-Emitter Breakdown Voltage	$I_C = -50 ma, V_{BE} = 0$, (See Note 3)		-50	-70	-90	v
I_{CBO} Collector Cutoff Current	$V_{CB} = -25 v, I_E = 0$ $V_{CB} = -35 v, I_E = 0$ $V_{CB} = -45 v, I_E = 0$		-125	-125	-125	μa
* I_{CEO} Collector Cutoff Current	$V_{CE} = -15 v, I_B = 0$ $V_{CE} = -20 v, I_B = 0$ $V_{CE} = -25 v, I_B = 0$		-20	-20	-20	ma
* I_{CEX} Collector Cutoff Current	$V_{CE} = -50 v, V_{BE} = +0.2 v$ $V_{CE} = -70 v, V_{BE} = +0.2 v$ $V_{CE} = -90 v, V_{BE} = +0.2 v$		-600	-600	-600	μa
* I_{CEX} Collector Cutoff Current	$V_{CE} = -25 v, V_{BE} = +0.2 v$ $V_{CE} = -35 v, V_{BE} = +0.2 v$ $V_{CE} = -45 v, V_{BE} = +0.2 v$		-125	-125	-125	μa
* I_{CEX} Collector Cutoff Current	$V_{CE} = -25 v, V_{BE} = +0.2 v, T_C = 85^\circ C$ $V_{CE} = -35 v, V_{BE} = +0.2 v, T_C = 85^\circ C$ $V_{CE} = -45 v, V_{BE} = +0.2 v, T_C = 85^\circ C$		-5	-5	-5	ma
* I_{EBO} Emitter Cutoff Current	$V_{EB} = -20 v, I_C = 0$		-100	-100	-100	μa
* h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -0.5 v, I_C = -1 a$, (See Note 4) $V_{CE} = -0.5 v, I_C = -500 ma$, (See Note 4) $V_{CE} = -0.5 v, I_C = -250 ma$, (See Note 4)		25 50 150 200	25 50 150 200	25 50 150 200	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -0.5 v, I_C = -500 ma$, (See Note 4) $T_C = -55^\circ C$, (See Note 4) $V_{CE} = -0.5 v, I_C = -500 ma$, (See Note 4) $T_C = +85^\circ C$, (See Note 4)		30 150 50 170	30 150 50 170	30 150 50 170	
* V_{BE} Base-Emitter Voltage	$V_{CE} = -0.5 v, I_C = -500 ma$, (See Note 4)		-0.6	-0.6	-0.6	v
* $V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -25 ma, I_C = -500 ma$, (See Note 4) $I_B = -25 ma, I_C = -500 ma$, (See Note 4) $T_C = +85^\circ C$, (See Note 4)		-0.2 -0.25	-0.2 -0.25	-0.2 -0.25	v
* h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -3 v, I_C = -100 ma, f = 1 kc$		50 200	50 200	50 200	
* $ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -3 v, I_C = -100 ma, f = 150 kc$		2.0	2.0	2.0	
C_{ob} Common-Base Open-Circuit Output Capacitance	$V_{CB} = -3 v, I_E = 0, f = 135 kc$		100 (typical)	100 (typical)	100 (typical)	pf

NOTES: 3. These characteristics are measured by a 1/2 sine wave sweep method.

4. These measurements are made with voltage sensing contacts located 0.25 inches from header of transistor. Voltage sensing contacts are separate from current carrying contacts.

*Indicates JEDEC registered data.

6

TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS †	TYPICAL	UNIT
t_d Delay Time	$I_C = -500 \text{ ma}$ $V_{BE}(\text{OFF}) = 7.4 \text{ v}$ $R_L = 60 \Omega$ (See Figure 1)	0.10	μSEC
t_r Rise Time		0.22	μSEC
t_s Storage Time		0.30	μSEC
t_f Fall Time		1.25	μSEC
t_T Total Switching Time		1.9	μSEC

† Voltage and current values are nominal, except values vary slightly with device parameters.

PARAMETER MEASUREMENT INFORMATION

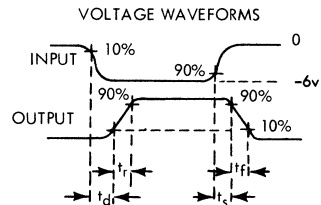
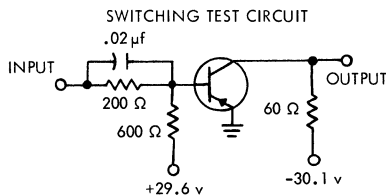
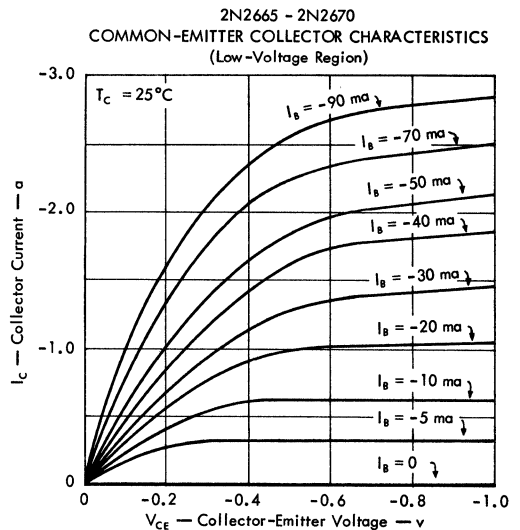
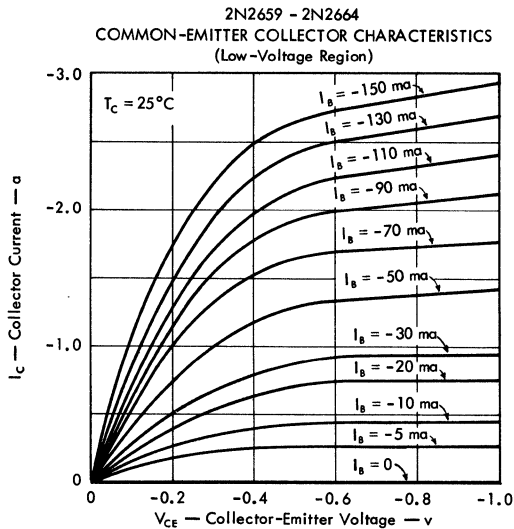


FIGURE 1

NOTES:

- (a) The input waveform has the following characteristics:
 $t_r \leq 10 \mu\text{sec}$, $t_f \leq 10 \mu\text{sec}$, $PW = 1.6 \text{ msec}$, Duty Cycle = 10%
- (b) Waveforms are monitored on an oscilloscope with the following characteristics:
 $t_r \leq 14 \mu\text{sec}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pf}$.
- (c) Resistors must be non-inductive types.

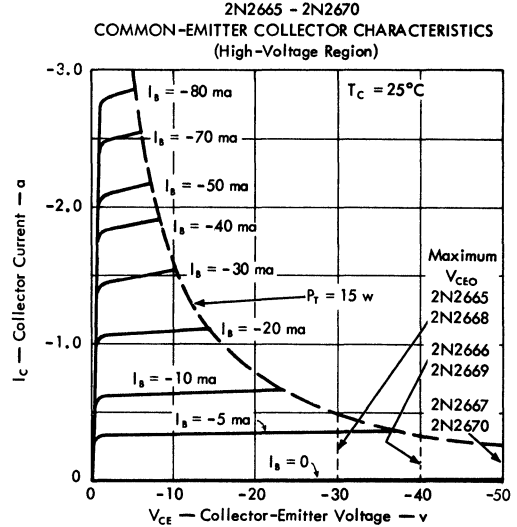
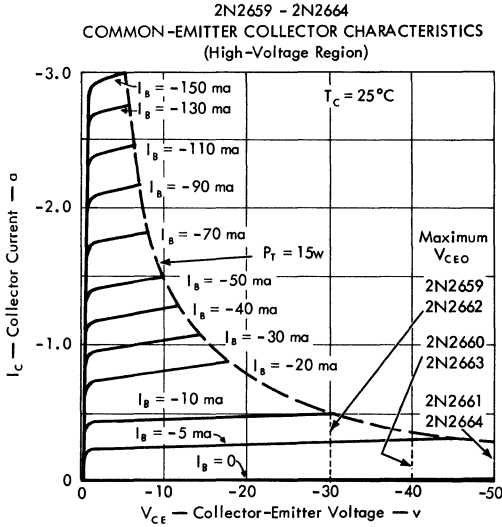
TYPICAL CHARACTERISTICS



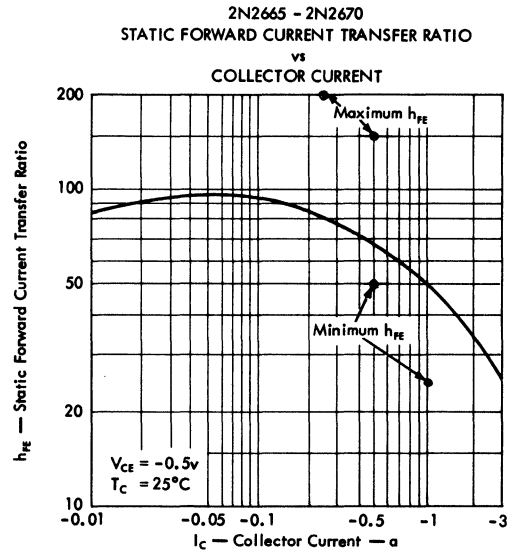
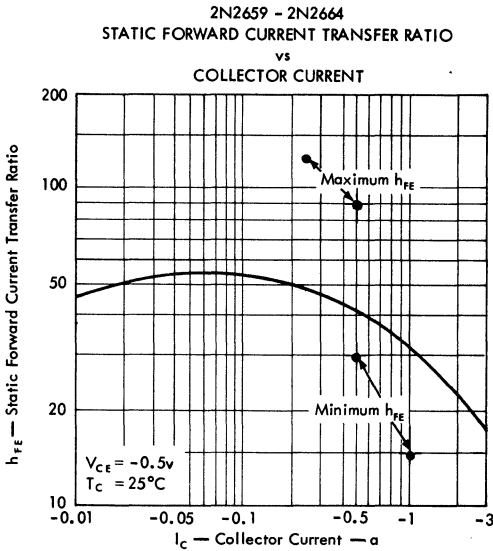
TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

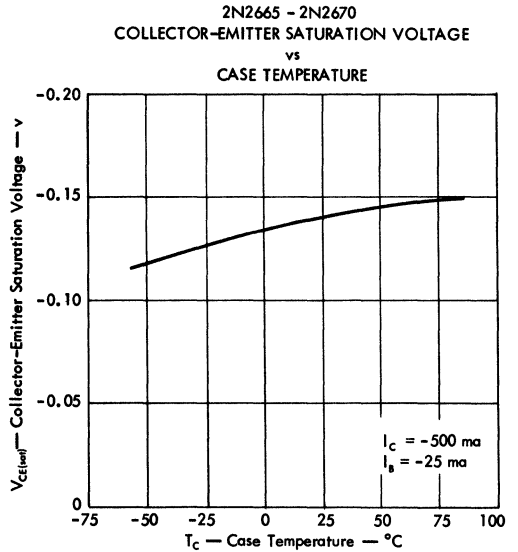
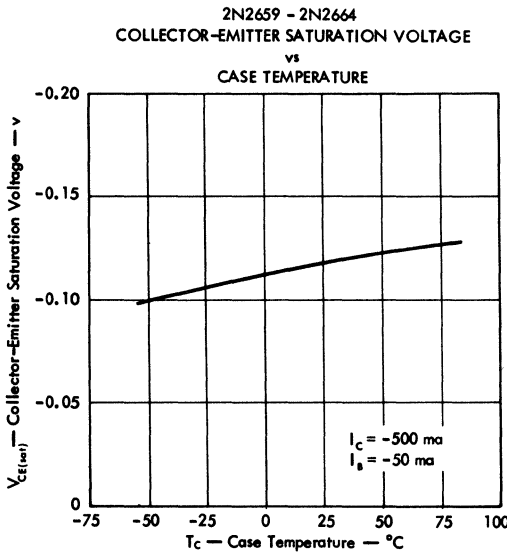
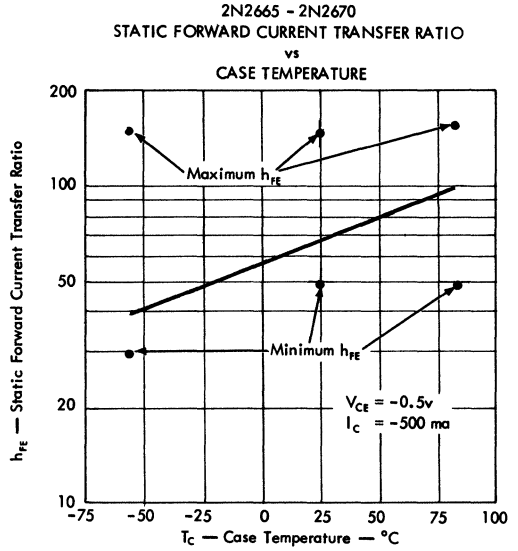
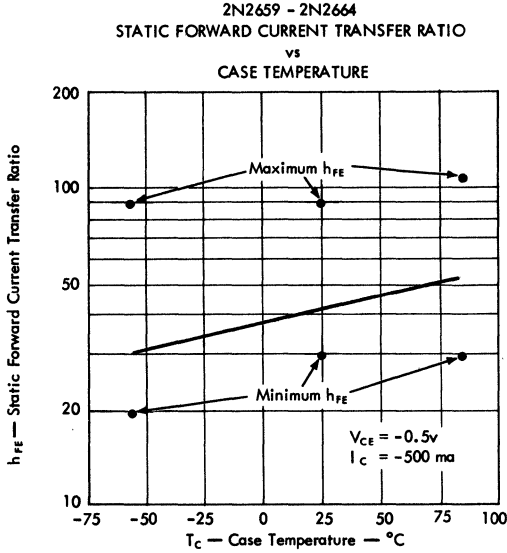


6



**TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664
 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670
 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS**

TYPICAL CHARACTERISTICS

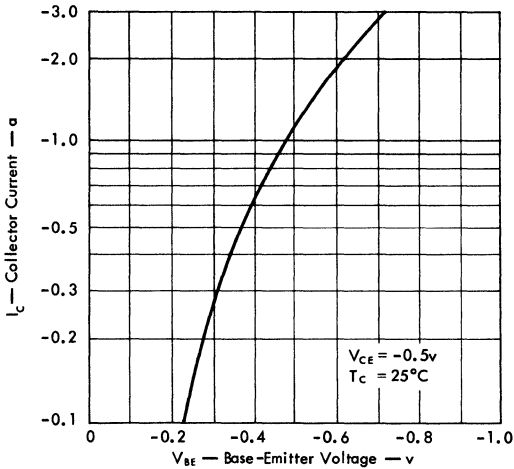


TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670

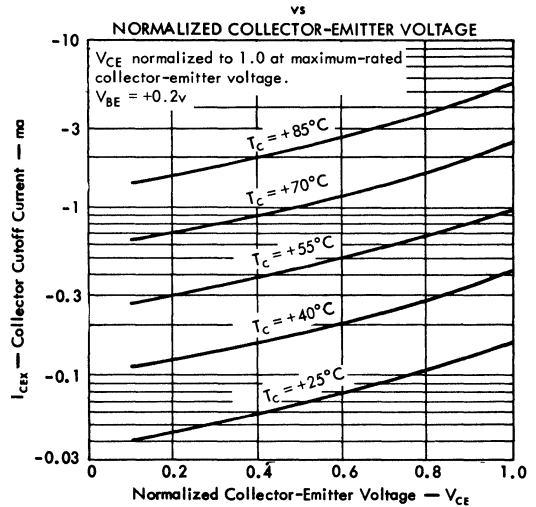
P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

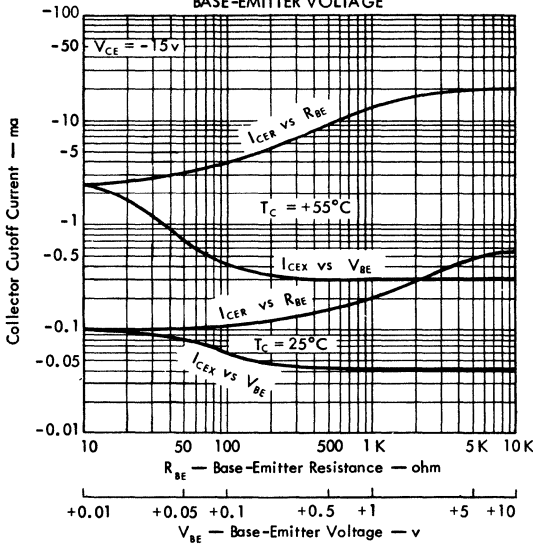
COMMON-EMITTER TRANSFER CHARACTERISTICS



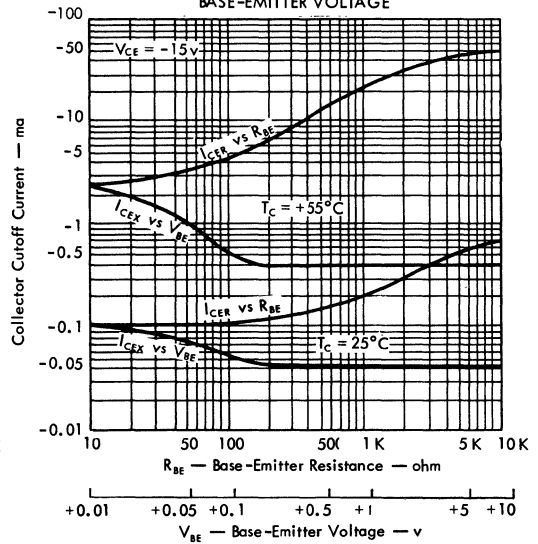
COLLECTOR CUTOFF CURRENT



2N2659 - 2N2664
COLLECTOR CUTOFF CURRENT
vs
BASE-EMITTER RESISTANCE
and
BASE-EMITTER VOLTAGE

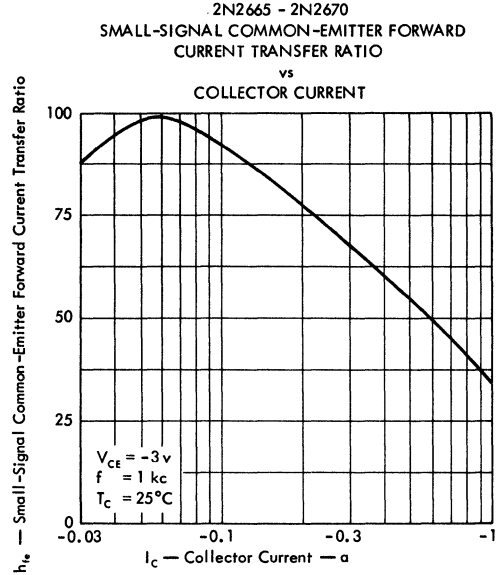
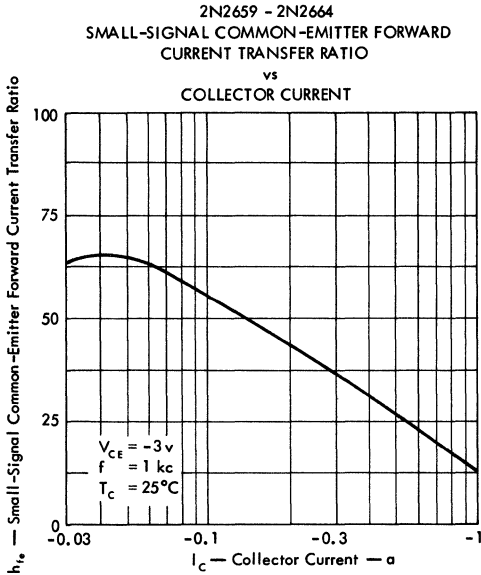


2N2665 - 2N2670
COLLECTOR CUTOFF CURRENT
vs
BASE-EMITTER RESISTANCE
and
BASE-EMITTER VOLTAGE

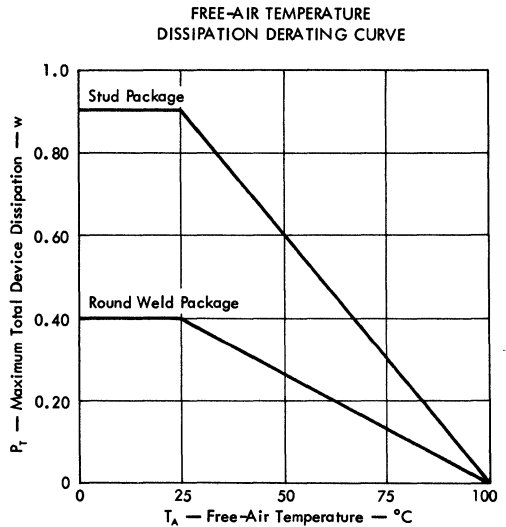
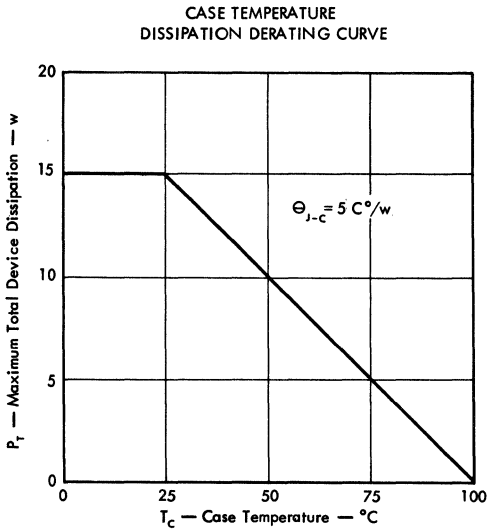


**TYPES 2N2659, 2N2660, 2N2661, 2N2662, 2N2663, 2N2664
 2N2665, 2N2666, 2N2667, 2N2668, 2N2669, 2N2670
 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS**

TYPICAL CHARACTERISTICS



THERMAL CHARACTERISTICS



TYPES 2N3146, 2N3147

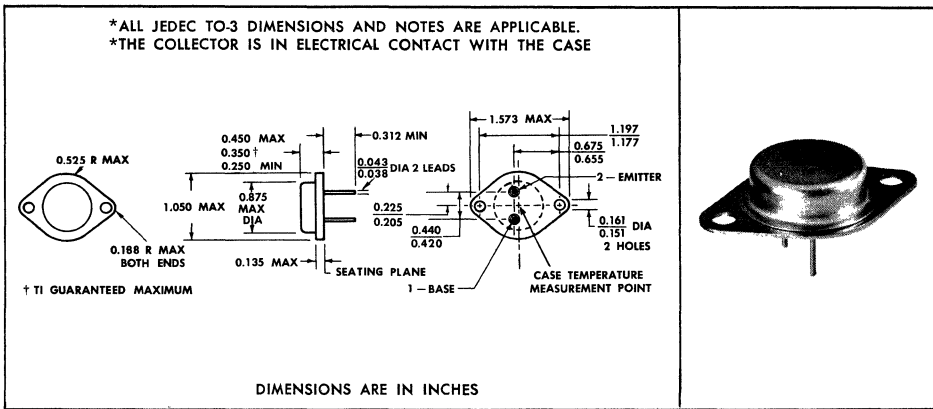
P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

HIGH-VOLTAGE HIGH-POWER TRANSISTORS for MILITARY AND INDUSTRIAL APPLICATIONS

TYPES 2N3146, 2N3147
BULLETIN NO. DL-5-684657, OCTOBER 1968

mechanical data

These transistors are in precision welded, hermetically sealed enclosures. The mounting base provides an excellent heat path from the collector junction to a heat sink. The mounting base and heat sink must be in intimate contact for maximum heat transfer. Extreme cleanliness and the absence of flux during the assembly process prevents sealed-in contamination.



6

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N3146	2N3147
Collector-Base Voltage	-150 V	-180 V
Collector-Emitter Voltage (See Note 1)	-140 V	-160 V
Emitter-Base Voltage	-60 V	-80 V
Continuous Collector Current	← -15 A →	
Peak Collector Current (See Note 2)	← -25 A →	
Continuous Base Current	← -3 A →	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 150 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 1.75 W →	
Operating Case Temperature Range	-65°C to 100°C	
Storage Temperature Range	-65°C to 100°C	
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 230°C →	

- NOTES: 1. These values apply when the base-emitter voltage $V_{BE} \geq 0.2$ V.
 2. This value applies for $t_p \leq 100$ ms, duty cycle $\leq 25\%$.
 3. Derate linearly to 100°C case temperature at the rate of 2 W/deg.
 4. Derate linearly to 100°C free-air temperature at the rate of 23.3 mW/deg.

*Indicates JEDEC registered data

TYPES 2N3146, 2N3147

P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

* electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	2N3146		2N3147		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -500 \text{ mA}, I_B = 0$	-65		-75		V
I_{CBO} Collector Cutoff Current	$V_{CB} = -150 \text{ V}, I_E = 0$		-10			mA
	$V_{CB} = -180 \text{ V}, I_E = 0$				-10	
I_{CEO} Collector Cutoff Current	$V_{CE} = -45 \text{ V}, I_B = 0$		-60			mA
	$V_{CE} = -50 \text{ V}, I_B = 0$				-60	
I_{CES} Collector Cutoff Current	$V_{CE} = -110 \text{ V}, V_{BE} = 0$		-5			mA
	$V_{CE} = -130 \text{ V}, V_{BE} = 0$				-5	
I_{CEV} Collector Cutoff Current	$V_{CE} = -100 \text{ V}, V_{BE} = 0.2 \text{ V}$		-1			mA
	$V_{CE} = -120 \text{ V}, V_{BE} = 0.2 \text{ V}$				-1	
	$V_{CE} = -140 \text{ V}, V_{BE} = 0.2 \text{ V}$		-10			
	$V_{CE} = -160 \text{ V}, V_{BE} = 0.2 \text{ V}$				-10	
	$V_{CE} = -80 \text{ V}, V_{BE} = 0.2 \text{ V}, T_C = 70^\circ \text{C}$		-5			
I_{EBO} Emitter Cutoff Current	$V_{EB} = -60 \text{ V}, I_C = 0$		-5			mA
	$V_{EB} = -80 \text{ V}, I_C = 0$				-5	
$V_{EB(FI)}$ Emitter-Base Floating Potential	$V_{CB} = -150 \text{ V}, I_E = 0$		-1			V
	$V_{CB} = -180 \text{ V}, I_E = 0$				-1	
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ V}, I_C = -1 \text{ A}$	40		40		
	$V_{CE} = -1.5 \text{ V}, I_C = -5 \text{ A}$	30	90	30	90	
	$V_{CE} = -1.5 \text{ V}, I_C = -10 \text{ A}$	25		25		
V_{BE} Base-Emitter Voltage	$V_{CE} = -1.5 \text{ V}, I_C = -5 \text{ A}$		-1.5		-1.5	V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.5 \text{ A}, I_C = -5 \text{ A}$		-0.4		-0.4	V
	$I_B = -1 \text{ A}, I_C = -10 \text{ A}$		-0.5		-0.5	
h_{fo} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ V}, I_C = -3 \text{ A}, f = 1 \text{ kHz}$	20	100	20	100	
h_{fc} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -1.5 \text{ V}, I_C = -3 \text{ A}, f = 100 \text{ kHz}$	2	5	2	5	

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	0.5	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	42.8	deg/W

*Indicates JEDEC registered data

TYPES T1156, T1156L

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

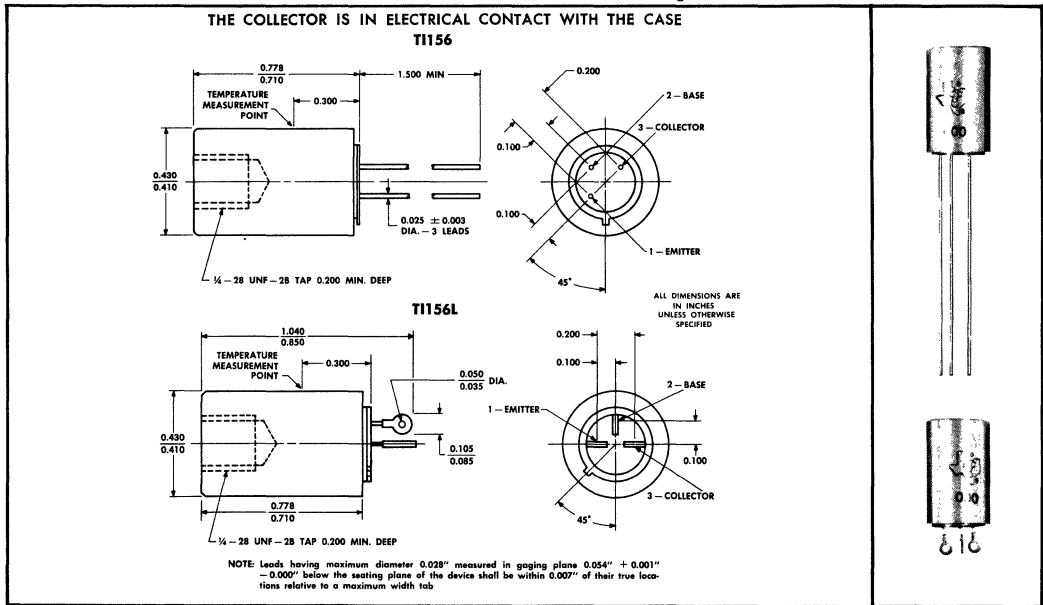
25 WATTS at 25°C CASE TEMPERATURE
for
RELAY DRIVERS • PULSE AMPLIFIERS • AUDIO AMPLIFIERS
and
DIRECT ELECTRICAL EQUIVALENTS of 2N156

TYPES T1156, T1156L
BULLETIN NO. DL-5-7111649, SEPTEMBER 1971
REPLACES BULLETIN NO. DL-5-694302, SEPTEMBER 1963

mechanical data

The transistors are in hermetically sealed welded cases with glass-to-metal seals between case and leads. Approximate weight: 5 grams.

The transistors are furnished with either wire leads (T1156) or with welded lugs (T1156L)



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Base Voltage	-30 V
Collector-Emitter Voltage (See Note 1)	-30 V
Emitter-Base Voltage	-15 V
Collector Current	-3 A
Base Current	-1 A
Total Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	25 W
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	1 W
Operating Case Temperature Range	-55°C to 100°C
Storage Temperature Range	-55°C to 100°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C case temperature at the rate of 333 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 13.3 mW/°C.

TYPES T1156, T1156L

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	WIRE LEAD	T1156		UNIT
		LUG	T1156L		
			MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -250 \text{ mA}$, $I_E = 0$, See Note 4		-30		V
I_{CBO} Collector Cutoff Current	$V_{CB} = -2 \text{ V}$, $I_E = 0$		-0.08		mA
	$V_{CB} = -30 \text{ V}$, $I_E = 0$		-0.65†		
	$V_{CB} = -30 \text{ V}$, $I_E = 0$, $T_C = 50^\circ\text{C}$		-1.6†		
	$V_{CB} = -30 \text{ V}$, $I_E = 0$, $T_C = 85^\circ\text{C}$		-8†		
I_{CES} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $V_{BE} = 0$		-1.5		mA
	$V_{CE} = -30 \text{ V}$, $V_{BE} = 0$, $T_C = 50^\circ\text{C}$		-5		
I_{CEV} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $V_{BE} = 0.5 \text{ V}$, $T_C = 85^\circ\text{C}$		-8†		mA
I_{EBO} Emitter Cutoff Current	$V_{EB} = -2 \text{ V}$, $I_C = 0$		-0.08		mA
	$V_{EB} = -15 \text{ V}$, $I_C = 0$		-0.5		
	$V_{EB} = -15 \text{ V}$, $I_C = 0$, $T_C = 50^\circ\text{C}$		-1		
	$V_{EB} = -15 \text{ V}$, $I_C = 0$, $T_C = 85^\circ\text{C}$		-5		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ V}$, $I_C = -1 \text{ A}$, See Note 5		15		
	$V_{CE} = -2 \text{ V}$, $I_C = -500 \text{ mA}$, See Note 5		25	75	
	$V_{CE} = -2 \text{ V}$, $I_C = -250 \text{ mA}$, See Note 5		30	100	
V_{BE} Base-Emitter Voltage	$V_{CE} = -2 \text{ V}$, $I_C = -500 \text{ mA}$, See Note 5		-0.6†		V
	$V_{CE} = -2 \text{ V}$, $I_C = -1 \text{ A}$, See Note 5		-1		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -100 \text{ mA}$, $I_C = -1 \text{ A}$, See Note 5		-0.25†		V
f_{hfe} Common-Emitter Forward Current Transfer Ratio Cutoff Frequency	$V_{CE} = -2 \text{ V}$, $I_C = -500 \text{ mA}$, $f = 1 \text{ kHz(ref)}$		6		kHz
f_T Transition Frequency	$V_{CE} = -2 \text{ V}$, $I_C = -250 \text{ mA}$, $f = 100 \text{ kHz}$, See Note 6		220		kHz

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	75	°C/W

NOTES: 4. These characteristics are measured by a half-sine-wave sweep method.

5. These measurements are made with voltage-sensing contacts located 0.25 inches from header of transistor. Voltage-sensing contacts are separate from current-carrying contacts.

6. To obtain f_T , the $|h_{fe}|$ response with frequency is extrapolated at the rate of -6 dB per octave from $f = 100 \text{ kHz}$ to the frequency at which $|h_{fe}| = 1$.

†These values surpass JEDEC registered values of the 2N156.

TYPES T1159, T1160, T1161, T1162 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

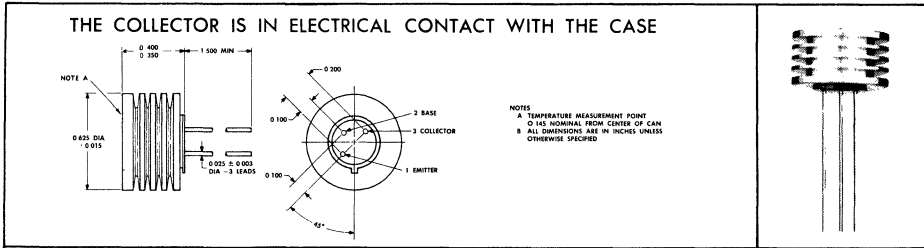
40, 60, 80 or 100 VOLT UNITS
20 WATTS AT 25°C CASE TEMPERATURE
1.4 WATTS IN FREE AIR
Guaranteed Beta at 1 amp and 50 ma I_C

Guaranteed I_{CEX} at 85°C
LOW r_{CS} • LOW I_{CO} • LOW V_{BE}
for
RELAY DRIVERS • PULSE AMPLIFIERS
SERVO AMPLIFIERS • AUDIO AMPLIFIERS

TYPES T1159, T1160, T1161, T1162
BULLETIN NO. DL-5 634413, DECEMBER 1963

mechanical data

The transistors are in hermetically-sealed welded cases with glass-to-metal seals between case and leads. Approximate weight: 4.8 grams.



6

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	T1159	T1160	T1161	T1162
Collector-Base Voltage	40 v	60 v	80 v	100 v
Collector-Emitter Voltage (See Note 1)	40 v	60 v	80 v	100 v
Emitter-Base Voltage	← 20 v →			
Collector Current	← 3 a →			
Base Current	← 1 a →			
Total Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 20 w →			
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	← 1.4 w →			
Operating Case Temperature Range	← -55°C to +100°C →			
Storage Temperature Range	← -55°C to +100°C →			
Lead Temperature, 1/16 Inch from Case for 10 Seconds	← 230°C →			

- NOTES: 1. This value applies when base-emitter voltage V_{BE} = + 0.2 v.
 2. Derate linearly to 100°C case temperature at the rate of 267 mw/°C.
 3. Derate linearly to 100°C free-air temperature at the rate of 18.7 mw/°C.

TYPES T1159, T1160, T1161, T1162

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

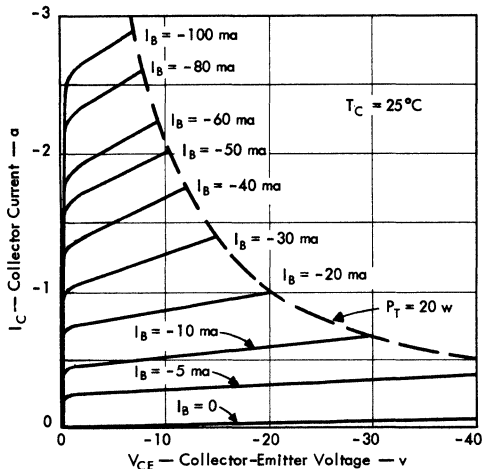
PARAMETER		TEST CONDITIONS	TYPE	MIN	MAX	UNIT
BV _{CB0}	Collector-Base Breakdown Voltage	I _C = -650 μa, I _E = 0	T1159	-40		v
			T1160	-60		
			T1161	-80		
			T1162	-100		
BV _{CEO}	Collector-Emitter Breakdown Voltage	I _C = -100 ma, I _B = 0	T1159	-30		v
			T1160	-40		
			T1161	-50		
			T1162	-60		
I _{CB0}	Collector Cutoff Current	V _{CB} = -20 v, I _E = 0	T1159		-125	μa
		V _{CB} = -30 v, I _E = 0	T1160			
		V _{CB} = -40 v, I _E = 0	T1161			
		V _{CB} = -50 v, I _E = 0	T1162			
I _{CEO}	Collector Cutoff Current	V _{CE} = -15 v, I _B = 0	T1159		-25	ma
		V _{CE} = -20 v, I _B = 0	T1160			
		V _{CE} = -25 v, I _B = 0	T1161			
		V _{CE} = -30 v, I _B = 0	T1162			
I _{CEX}	Collector Cutoff Current	V _{CE} = -40 v, V _{BE} = +0.2 v	T1159		-650	μa
		V _{CE} = -60 v, V _{BE} = +0.2 v	T1160			
		V _{CE} = -80 v, V _{BE} = +0.2 v	T1161			
		V _{CE} = -100 v, V _{BE} = +0.2 v	T1162			
I _{CEX}	Collector Cutoff Current	V _{CE} = -20 v, V _{BE} = +0.2 v, T _C = +85°C	T1159		-5	ma
		V _{CE} = -30 v, V _{BE} = +0.2 v, T _C = +85°C	T1160			
		V _{CE} = -40 v, V _{BE} = +0.2 v, T _C = +85°C	T1161			
		V _{CE} = -50 v, V _{BE} = +0.2 v, T _C = +85°C	T1162			
I _{EBO}	Emitter Cutoff Current	V _{EB} = -20 v, I _C = 0			-650	μa
h _{IE}	Static Common-Emitter Input Impedance	V _{CE} = -0.5 v, I _C = -1 a, (See Note 4)			60	ohm
h _{FE}	Static Forward Current Transfer Ratio	V _{CE} = -0.5 v, I _C = -1 a, (See Note 4)		20	60	
		V _{CE} = -0.5 v, I _C = -50 ma		33	200	
		V _{CE} = -0.5 v, I _C = -1 a, T _C = -55°C, (See Note 4)		15	60	
		V _{CE} = -0.5 v, I _C = -1 a, T _C = +85°C, (See Note 4)		20	75	
Y _{FE}	Static Common-Emitter Forward Transfer Admittance	V _{CE} = -0.5 v, I _C = -1 a, (See Note 4)		1.0		mho
V _{BE}	Base-Emitter Voltage	V _{CE} = -0.5 v, I _C = -1 a, (See Note 4)			-1.0	v
		V _{CE} = -0.5 v, I _C = -50 ma			-0.35	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	I _B = -100 ma, I _C = -1 a, (See Note 4)			-0.25	v
h _{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -1.5 v, I _C = -0.5 a, f = 1 kc		18	72	
h _{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V _{CE} = -1.5 v, I _C = -0.5 a, f = 112.5 kc		2.0		
C _{ob}	Common-Base Open-Circuit Output Capacitance	V _{CB} = -6 v, I _E = 0, f = 135 kc			100 (typical)	pf

NOTE 4: Measurements are made with voltage sensing contacts located 0.25 inches from header of transistor. Voltage sensing contacts are separate from current carrying contacts.

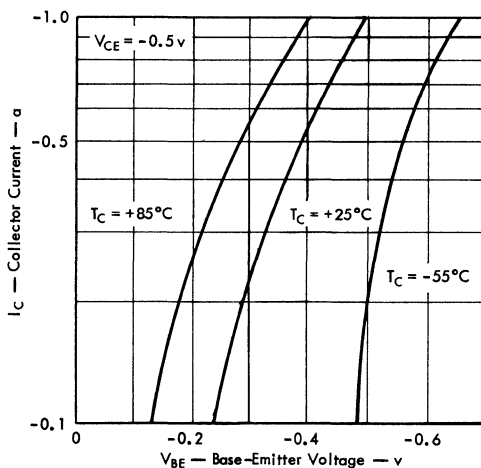
TYPES T1159, T1160, T1161, T1162 P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS

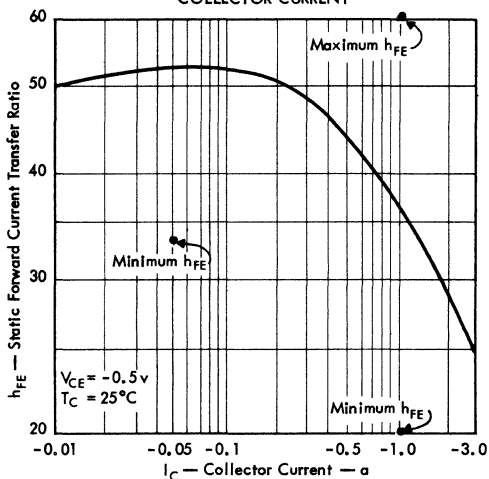
COMMON-EMITTER COLLECTOR
CHARACTERISTICS



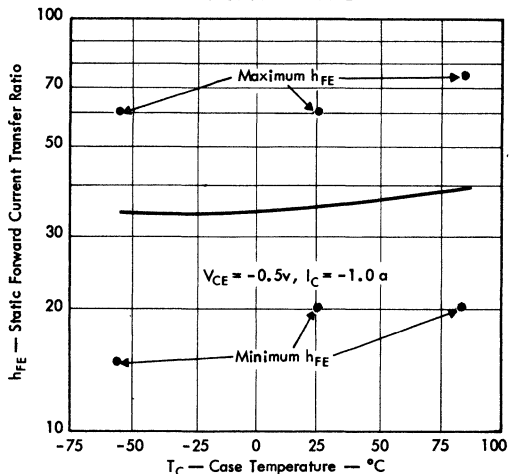
COMMON-EMITTER TRANSFER
CHARACTERISTICS



STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT



STATIC FORWARD CURRENT TRANSFER RATIO
vs
CASE TEMPERATURE

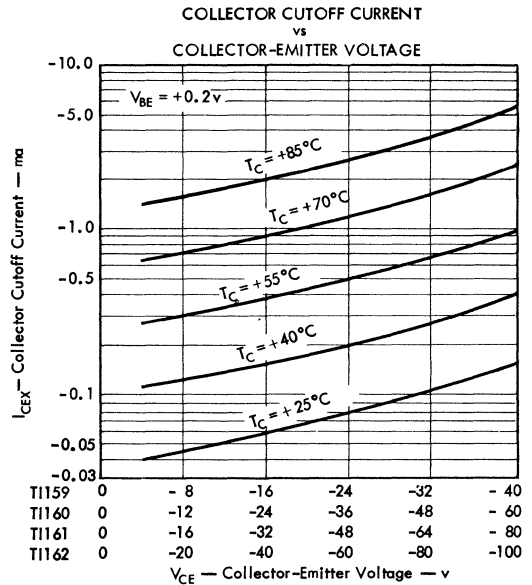
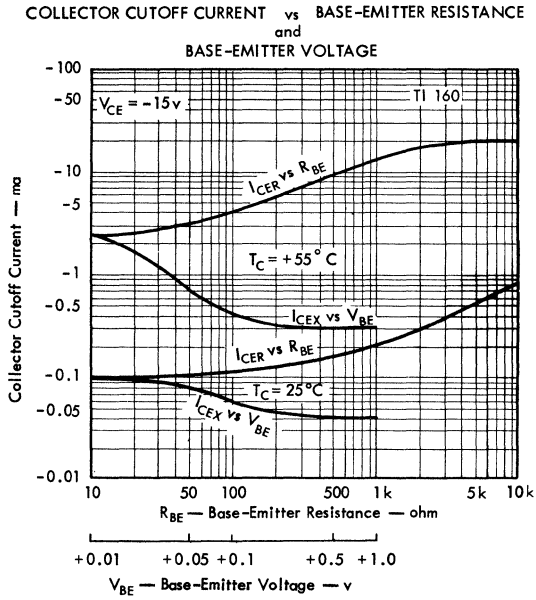


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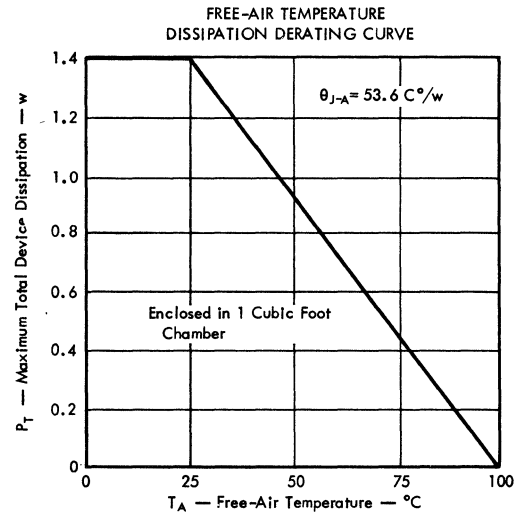
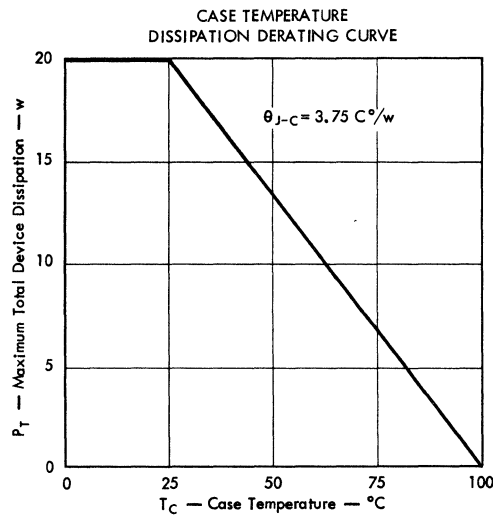
TYPES T1159, T1160, T1161, T1162

P-N-P ALLOY-JUNCTION GERMANIUM MEDIUM-POWER TRANSISTORS

TYPICAL CHARACTERISTICS



THERMAL CHARACTERISTICS



6

TYPES TI3027, TI3028

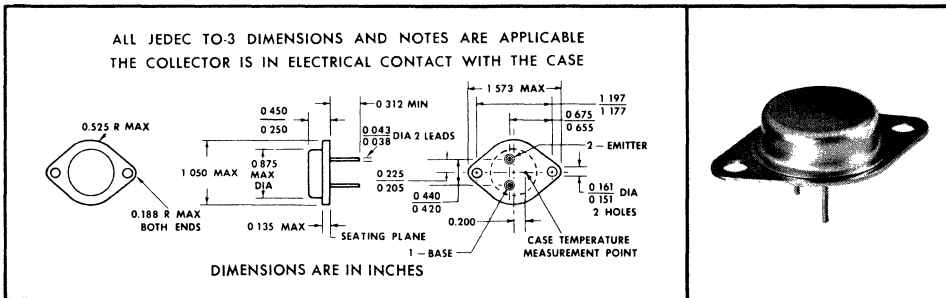
P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

HIGH-POWER TRANSISTORS for CONSUMER APPLICATIONS

TYPES TI3027, TI3028
 BULLETIN NO. DL-S 685053, APRIL 1964
 REVISED MAY 1969

mechanical data

These transistors are in a resistance-welded, hermetically sealed enclosure. The mounting base provides an excellent heat path from the collector junction to a heat sink. The entire mounting base must be in intimate contact with the heat sink for maximum heat transfer. A minimum torque of 10 inch-pounds applied to each of the mounting screws is recommended for mounting the device to the heat sink. Extreme cleanliness and the absence of flux during the assembly process prevents sealed-in contamination.



6

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TI3027	TI3028
Collector-Base Voltage	-45 v	-60 v
Collector-Emitter Voltage (See Note 1)	-40 v	-50 v
Emitter-Base Voltage	← -20 v →	← -20 v →
Continuous Collector Current	← -7 a →	← -7 a →
Continuous Base Current	← -3 a →	← -3 a →
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 106 w →	← 106 w →
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	← 2 w →	← 2 w →
Operating Case Temperature Range	← -65°C to +100°C →	← -65°C to +100°C →
Storage Temperature Range	← -65°C to +100°C →	← -65°C to +100°C →
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 230°C →	← 230°C →

- NOTES: 1. These values apply when the base-emitter resistance $R_{BE} \leq 68 \Omega$.
 2. Derate linearly to 110°C case temperature at the rate of 1.25 w/°C.
 3. Derate linearly to 110°C free-air temperature at the rate of 235 mw/°C.

TYPES TI3027, TI3028

P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TI3027		TI3028		UNIT
		MIN	MAX	MIN	MAX	
V_{CB0} Collector-Base Breakdown Voltage	$I_C = -5 \text{ ma}$, $I_E = 0$	-45		-60		v
V_{CER} Collector-Emitter Breakdown Voltage	$I_C = -600 \text{ ma}$, $R_{BE} = 68 \Omega$, See Note 4	-40		-50		v
I_{CBO} Collector Cutoff Current	$V_{CB} = -2 \text{ v}$, $I_E = 0$	-0.15		-0.15		ma
	$V_{CB} = -30 \text{ v}$, $I_E = 0$	-1				
	$V_{CB} = -40 \text{ v}$, $I_E = 0$			-1		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -20 \text{ v}$, $I_C = 0$	-1		-1		ma
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ v}$, $I_C = -1 \text{ a}$, See Note 4	70		70		
	$V_{CE} = -2 \text{ v}$, $I_C = -3 \text{ a}$, See Note 4	40	250	40	250	
V_{BE} Base-Emitter Voltage	$V_{CE} = -2 \text{ v}$, $I_C = -1 \text{ a}$, See Note 4	-0.5		-0.5		v
	$V_{CE} = -2 \text{ v}$, $I_C = -3 \text{ a}$, See Note 4	-1.0		-1.0		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -100 \text{ ma}$, $I_C = -1 \text{ a}$, See Note 4	-0.4		-0.4		v
	$I_B = -300 \text{ ma}$, $I_C = -3 \text{ a}$, See Note 4	-0.5		-0.5		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -2 \text{ v}$, $I_C = -1 \text{ a}$, $f = 100 \text{ kc}$	2		2		

NOTE 4: These parameters must be measured using pulse techniques. PW = 300 μsec , Duty Cycle $\leq 2\%$.

thermal characteristics

PARAMETER	TEST CONDITIONS	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	See notes in Thermal Characteristics section	0.8	$^{\circ}\text{C}/\text{w}$
θ_{J-HS} Junction-to-Heat-Sink Thermal Resistance		1.4	$^{\circ}\text{C}/\text{w}$
θ_{J-A} Junction-to-Free-Air Thermal Resistance		42.5	$^{\circ}\text{C}/\text{w}$

NUMERICAL SYSTEM FOR h_{FE} CODING

Upon request the transistors will be numerically coded to identify matched pairs. The transistors are in-house classified into 2-db (ratio 1.26 to 1) h_{FE} brackets and any two units within a bracket constitute a matched pair. A 10% tolerance is included in the bracket limits shown below to allow for test-set correlation.

No h_{FE} -bracket distribution is implied by this classification system.

BRACKET NUMBER	h_{FE} RANGE at $V_{CE} = -2 \text{ v}$, $I_C = -3 \text{ a}$
1	40 — 60
2	50 — 80
3	65 — 100
4	80 — 125
5	100 — 150
6	125 — 200
7	160 — 250

TYPES TI3027, TI3028 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

THERMAL CHARACTERISTICS

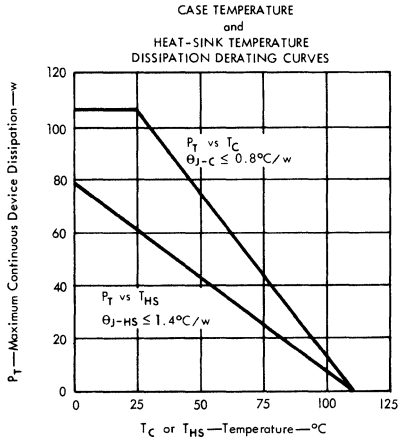


FIGURE 1

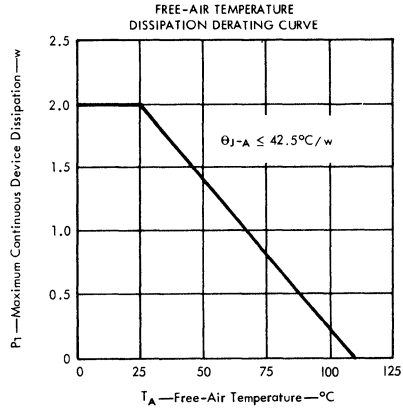


FIGURE 2

θ_{J-A} is the thermal resistance from the junction of the transistor to free-air. The curve shown above was determined by positioning the transistor in the center of a box 12 inches by 12 inches by 12 inches with the temperature measured two inches below the transistor.

θ_{J-C} is the thermal resistance from the junction of the transistor to the point on the mounting base of the transistor case specified on the outline drawing.

θ_{C-HS} is the thermal resistance from the mounting base of the transistor case to the mounting surface of the heat sink. The heat sink used to determine this value was a smooth, flat, copper plate, with the thermocouple mounted 0.05 inch below the mounting surface in an area beneath the center of the transistor. The transistor was mounted directly to a clean, dry, heat-sink surface, without the use of silicone grease, and a torque of ten inch-pounds was applied to each of the mounting screws.

θ_{J-HS} is the thermal resistance from the junction of the transistor to the mounting surface of the heat sink.

$$\theta_{J-HS} = \theta_{J-C} + \theta_{C-HS}$$

The dissipation levels shown above are verified statistically by operating-life tests.

6

TYPICAL CHARACTERISTICS

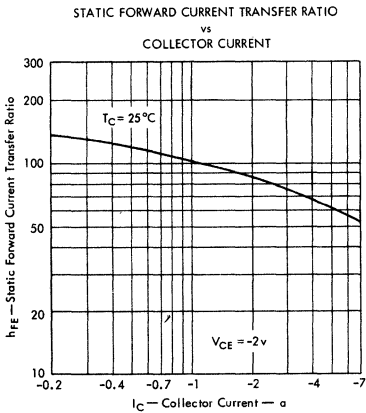


FIGURE 3

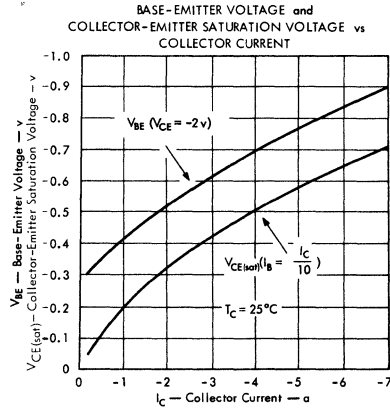


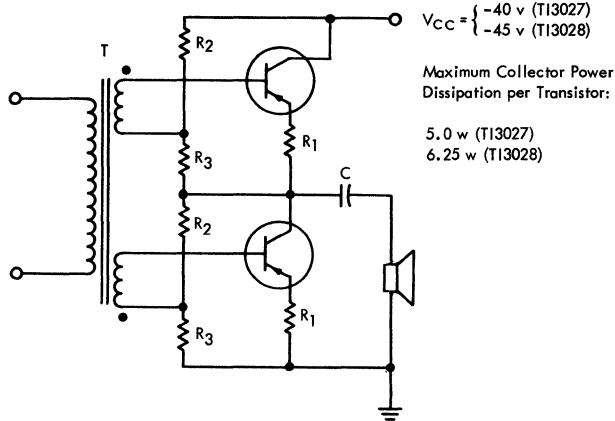
FIGURE 4

TYPES TI3027, TI3028

P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

TYPICAL APPLICATION DATA

CLASS B AUDIO AMPLIFIER



TYPICAL CIRCUIT PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $f = 1000 \text{ cps}$ (except where noted)

	TI3027	TI3028
Minimum RMS Power Output at 5% Total Harmonic Distortion	20 w	25 w
Minimum Power Gain	18 db	20 db
Frequency Response	20 to 20,000 cps	20 to 20,000 cps
D-C Collector Current with Zero Signal	-0.05 a	-0.05 a
D-C Collector Current with Maximum Signal	-1.25 a	-1.10 a
Peak Collector Current with Maximum Signal	-3.9 a	-3.5 a
Input Impedance, Base-to-Base	73 Ω	68 Ω

CIRCUIT COMPONENT INFORMATION

	TI3027	TI3028
R_1 :	0.56 Ω , 1 w	0.56 Ω , 1 w
R_2 :	125 Ω , 5 w	150 Ω , 5 w
R_3 :	1.1 Ω , 1/2 w	1.2 Ω , 1/2 w
Speaker Impedance:	8 Ω	8 Ω

All resistors $\pm 10\%$ tolerance

C: Selected to meet desired low-frequency response. Working voltage equals 40 v.

T: Driver transformer primary-winding impedance, current-carrying capacity, and d-c resistance are determined by large-signal characteristics of driver stage. Secondary windings are bifilar wound. The a-c impedance of each secondary winding equals 18 ohms for TI3027 and 17 ohms for TI3028.

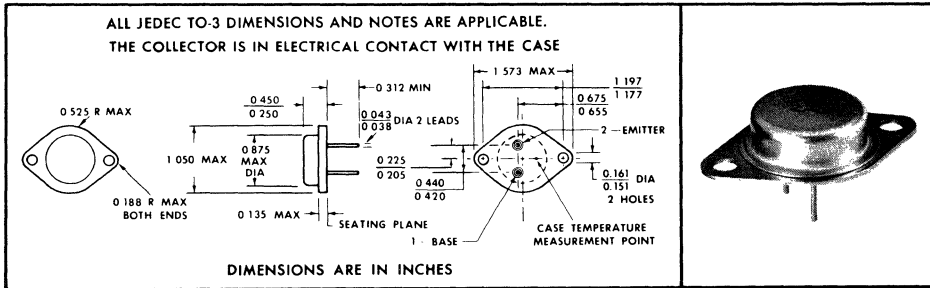
TYPES TI3029, TI3030, TI3031 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

TYPES TI3029, TI3030, TI3031
BULLETIN NO. DL-S-69505A, APRIL 1964
REVISED MAY 1969

HIGH-POWER TRANSISTORS for CONSUMER APPLICATIONS

mechanical data

These transistors are in a resistance-welded, hermetically sealed enclosure. The mounting base provides an excellent heat path from the collector junction to a heat sink. The entire mounting base must be in intimate contact with the heat sink for maximum heat transfer. A minimum torque of 10 inch-pounds applied to each of the mounting screws is recommended for mounting the device to the heat sink. Extreme cleanliness and the absence of flux during the assembly process prevents sealed-in contamination.



6

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TI3029	TI3030	TI3031
Collector-Base Voltage	-80 v	-100 v	-120 v
Collector-Emitter Voltage (See Note 1)	-55 v	-60 v	-65 v
Emitter-Base Voltage	←	-20 v	→
Continuous Collector Current	←	-7 a	→
Continuous Base Current	←	-3 a	→
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	←	106 w	→
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	←	2 w	→
Operating Case Temperature Range		-65°C to +100°C	
Storage Temperature Range		-65°C to +100°C	
Lead Temperature 1/8 Inch from Case for 10 Seconds	←	230°C	→

- NOTES: 1. These values apply when the base-emitter resistance $R_{BE} \leq 68 \Omega$.
2. Derate linearly to 110°C case temperature at the rate of 1.25 w/°C.
3. Derate linearly to 110°C free-air temperature at the rate of 23.5 mw/°C.

TYPES TI3029, TI3030, TI3031

P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TI3029		TI3030		TI3031		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
BV_{CBO} Collector-Base Breakdown Voltage	$I_C = -5 \text{ ma}, I_E = 0$	-80		-100		-120		v
BV_{CER} Collector-Emitter Breakdown Voltage	$I_C = -600 \text{ ma}, R_{BE} = 68 \Omega$, See Note 4	-55		-60		-65		v
I_{CBO} Collector Cutoff Current	$V_{CB} = -2 \text{ v}, I_E = 0$	-0.15		-0.15		-0.15		ma
	$V_{CB} = -50 \text{ v}, I_E = 0$	-1						
	$V_{CB} = -60 \text{ v}, I_E = 0$			-1				
	$V_{CB} = -70 \text{ v}, I_E = 0$					-1		
	$V_{CB} = -50 \text{ v}, I_E = 0, T_C = +70^\circ\text{C}$	-10						
	$V_{CB} = -60 \text{ v}, I_E = 0, T_C = +70^\circ\text{C}$			-10				
I_{EBO} Emitter Cutoff Current	$V_{EB} = -20 \text{ v}, I_C = 0$	-1		-1		-1		ma
	$V_{EB} = -70 \text{ v}, I_C = 0, T_C = +70^\circ\text{C}$					-10		
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -2 \text{ v}, I_C = -1 \text{ a}$, See Note 4	70		70		70		
	$V_{CE} = -2 \text{ v}, I_C = -3 \text{ a}$, See Note 4	40	250	40	250	40	250	
	$V_{CE} = -2 \text{ v}, I_C = -5 \text{ a}$, See Note 4	30		30		30		
V_{BE} Base-Emitter Voltage	$V_{CE} = -2 \text{ v}, I_C = -3 \text{ a}$, See Note 4	-1.0		-1.0		-1.0		v
	$V_{CE} = -2 \text{ v}, I_C = -5 \text{ a}$, See Note 4	-1.5		-1.5		-1.5		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -300 \text{ ma}, I_C = -3 \text{ a}$, See Note 4	-0.5		-0.5		-0.5		v
	$I_B = -500 \text{ ma}, I_C = -5 \text{ a}$, See Note 4	-0.7		-0.7		-0.7		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -2 \text{ v}, I_C = -1 \text{ a}, f = 100 \text{ kc}$	2		2		2		

NOTE 4: These parameters must be measured using pulse techniques. PW = 300 μsec , Duty Cycle $\leq 2\%$.

thermal characteristics

PARAMETER	TEST CONDITIONS	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	See notes in Thermal Characteristics section	0.8	$^\circ\text{C}/\text{w}$
θ_{J-HS} Junction-to-Heat-Sink Thermal Resistance		1.4	$^\circ\text{C}/\text{w}$
θ_{J-A} Junction-to-Free-Air Thermal Resistance		42.5	$^\circ\text{C}/\text{w}$

NUMERICAL SYSTEM FOR h_{FE} CODING

Upon request the transistors will be numerically coded to identify matched pairs. The transistors are in-house classified into 2-db (ratio 1.26 to 1) h_{FE} brackets and any two units within a bracket constitute a matched pair. A 10% tolerance is included in the bracket limits shown below to allow for test-set correlation.

No h_{FE} -bracket distribution is implied by this classification system.

BRACKET NUMBER	h_{FE} RANGE at $V_{CE} = -2 \text{ v}, I_C = -3 \text{ a}$
1	40 - 60
2	50 - 80
3	65 - 100
4	80 - 125
5	100 - 150
6	125 - 200
7	160 - 250

TYPES TI3029, TI3030, TI3031 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

THERMAL CHARACTERISTICS

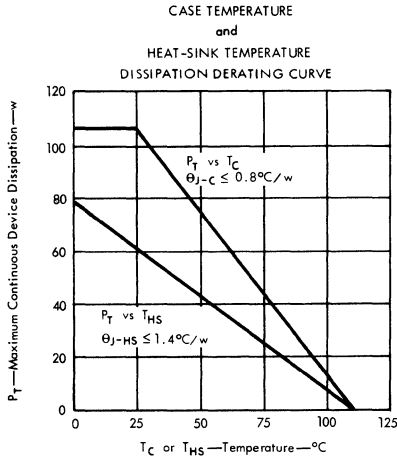


FIGURE 1

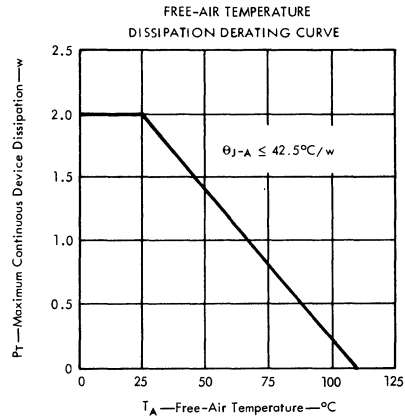


FIGURE 2

θ_{J-A} is the thermal resistance from the junction of the transistor to free-air. The curve shown above was determined by positioning the transistor in the center of a box 12 inches by 12 inches by 12 inches with the temperature measured two inches below the transistor.

θ_{J-C} is the thermal resistance from the junction of the transistor to the point on the mounting base of the transistor case specified on the outline drawing.

θ_{C-HS} is the thermal resistance from the mounting base of the transistor case to the mounting surface of the heat sink. The heat sink used to determine this value was a smooth, flat, copper plate, with the thermocouple mounted 0.05 inch below the mounting surface in an area beneath the center of the transistor. The transistor was mounted directly to a clean, dry, heat-sink surface, without the use of silicone grease, and a torque of ten inch-pounds was applied to each of the mounting screws.

θ_{J-HS} is the thermal resistance from the junction of the transistor to the mounting surface of the heat sink.

$$\theta_{J-HS} = \theta_{J-C} + \theta_{C-HS}$$

The dissipation levels shown above are verified statistically by operating-life tests.

TYPICAL CHARACTERISTICS

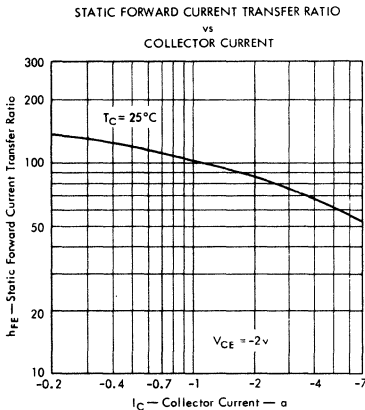


FIGURE 3

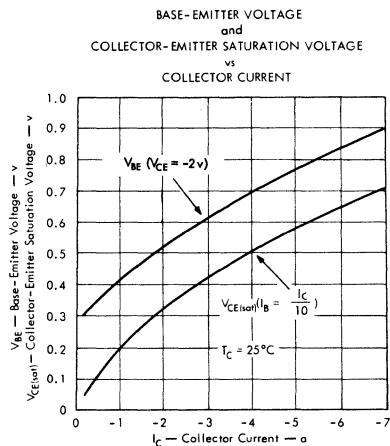


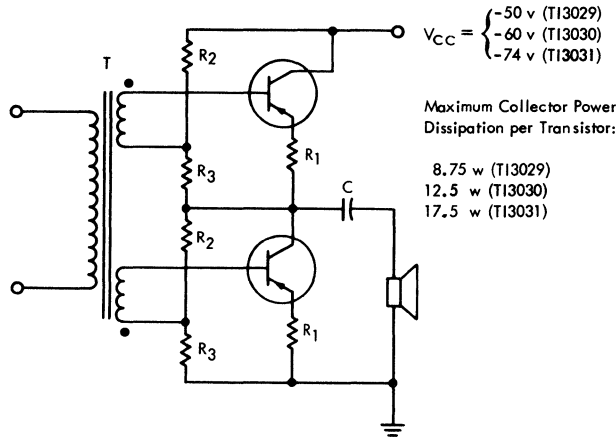
FIGURE 4

6

TYPES TI3029, TI3030, TI3031 P-N-P ALLOY-JUNCTION GERMANIUM POWER TRANSISTORS

TYPICAL APPLICATION DATA

CLASS B AUDIO AMPLIFIER



TYPICAL CIRCUIT PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $f = 1000$ cps (except where noted)

	TI3029	TI3030	TI3031
Minimum RMS Power Output at 5% Total Harmonic Distortion	35 w	50 w	70 w
Minimum Power Gain	26 db	25 db	20 db
Frequency Response	← 20 to 20,000 cps →		
D-C Collector Current with Zero Signal	-0.05 a	-0.05 a	-0.05 a
D-C Collector Current with Maximum Signal	-0.95 a	-1.10 a	-2.22 a
Peak Collector Current with Maximum Signal	-3.0 a	-3.5 a	-7.0 a
Input Impedance, Base-to-Base	88.5 Ω	74.5 Ω	69 Ω

CIRCUIT COMPONENT INFORMATION

	TI3029	TI3030	TI3031
R_1 :	0.27 Ω , 1/2 w	0.27 Ω , 1/2 w	0.47 Ω , 3 w
R_2 :	330 Ω , 2 w	250 Ω , 5 w	150 Ω , 10 w
R_3 :	2.2 Ω , 1/2 w	1.2 Ω , 1/2 w	0.56 Ω , 1/2 w

Speaker Impedance: 8 Ω 8 Ω 4 Ω

All resistors $\pm 10\%$ tolerance

C: Selected to meet desired low-frequency response. Working voltage should be greater than 85% of V_{CC} .

T: Driver transformer primary-winding impedance, current-carrying capacity, and d-c resistance are determined by large-signal characteristics of driver stage. Secondary windings are bifilar wound. The a-c impedance of each secondary winding equals one-fourth of base-to-base input impedance.

Thyristor Data Sheets

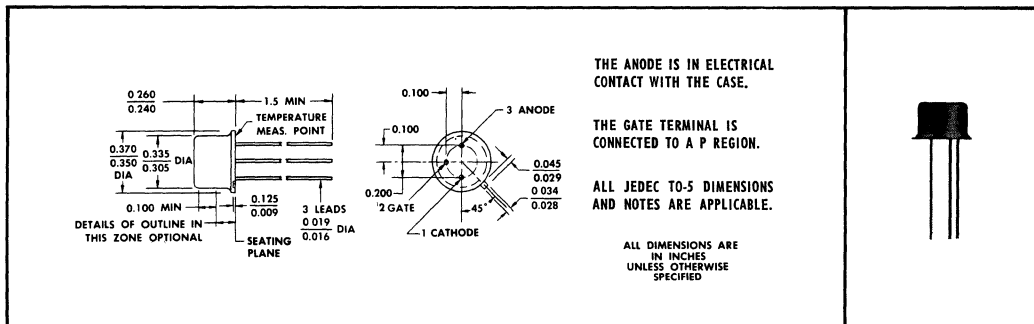
7

TYPES 2N1595 THRU 2N1599 P-N-P-N DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYRISTORS

1 AMP DC • 50 to 400 VOLTS

TYPES 2N1595 THRU 2N1599
BULLETIN NO. DLS-7111668, DECEMBER 1971
REPLACES BULLETIN NO. DLS-668697, JUNE 1966

***mechanical data**



***absolute maximum ratings over operating case temperature range (unless otherwise noted)**

	2N1595	2N1596	2N1597	2N1598	2N1599	UNIT
Static Off-State Voltage, V_D (See Note 1)	50	100	200	300	400	V
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	50	100	200	300	400	V
Static Reverse Voltage, V_R (See Note 1)	50	100	200	300	400	V
Repetitive Peak Reverse Voltage, V_{RRM} (See Note 1)	50	100	200	300	400	V
Continuous or RMS On-State Current at (or below) 80°C Case Temperature (See Note 2)	1					A
Average On-State Current (180° Conduction Angle) at (or below) 80°C Case Temperature (See Note 3)	1					A
Surge On-State Current (See Note 4)	15					A
Operating Case Temperature Range	-65 to 125					°C
Storage Temperature Range	-65 to 150					°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300					°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} \leq \infty$.
2. This value applies for continuous d-c operation with resistive load. Above 80°C derate according to Figure 1.
3. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 80°C derate according to Figure 1.
4. These values apply for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

7

TYPES 2N1595 THRU 2N1599

P-N-P-N DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
*I _D Static On-State Current	V _D = Rated V _D , I _G = 0, T _C = 125°C	1		mA
*I _R Static Reverse Current	V _R = Rated V _R , I _G = 0, T _C = 125°C	1		mA
*I _{GT} Gate Trigger Current	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 20 μs	10		mA
*V _{GT} Gate Trigger Voltage	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 20 μs	3		V
I _H Holding Current	R _L = 1 kΩ, I _G = 0	25		mA
*V _T On-State Voltage	I _T = 1 A, R _{GK} ≥ 1 kΩ	2		V

*JEDEC registered data

THERMAL INFORMATION

AVERAGE ON-STATE CURRENT DERATING CURVE

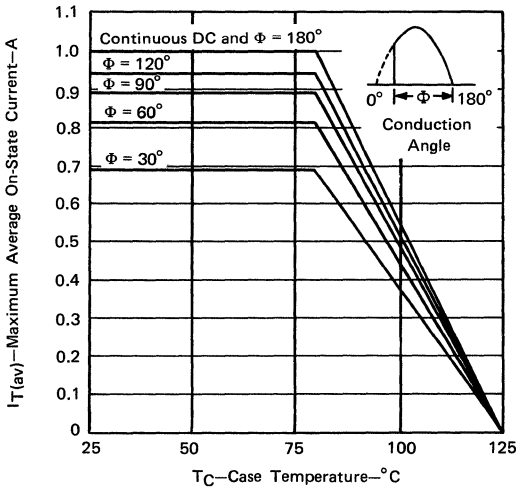


FIGURE 1

MAXIMUM AVERAGE ANODE POWER DISSIPATION vs AVERAGE ON-STATE CURRENT

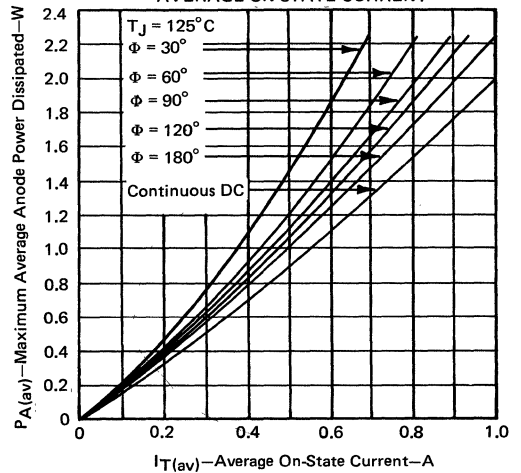


FIGURE 2

7

TYPES 2N1595 THRU 2N1599 P-N-P-N DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

STATIC OFF-STATE CURRENT
vs
CASE TEMPERATURE

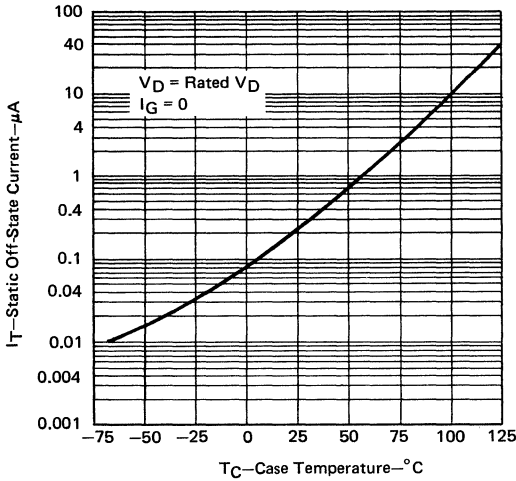


FIGURE 3

STATIC REVERSE CURRENT
vs
CASE TEMPERATURE

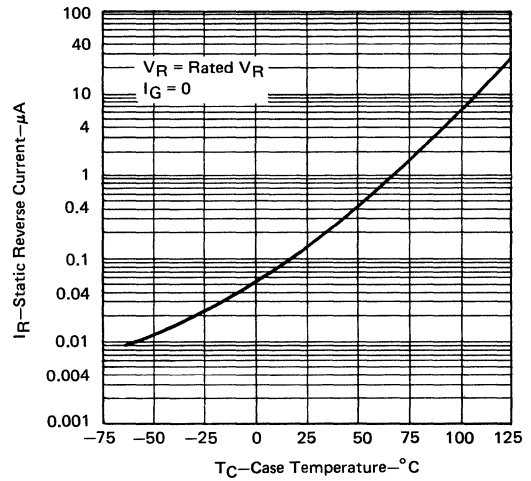


FIGURE 4

HOLDING CURRENT
vs
CASE TEMPERATURE

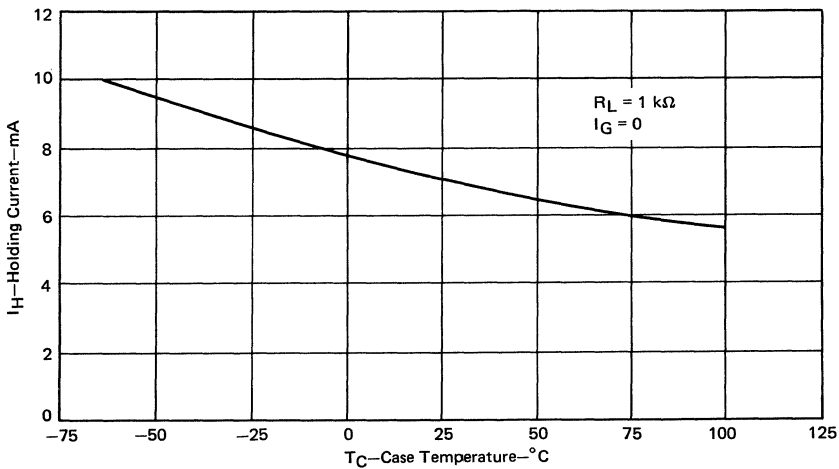


FIGURE 5

7

TYPES 2N1595 THRU 2N1599

P-N-P-N DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

GATE TRIGGER CURRENT
vs
CASE TEMPERATURE

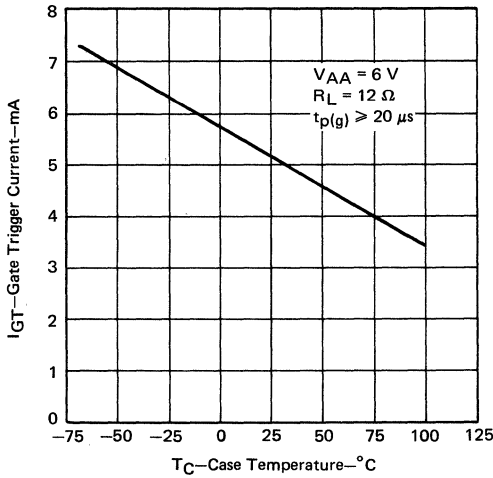


FIGURE 6

GATE TRIGGER VOLTAGE
vs
CASE TEMPERATURE

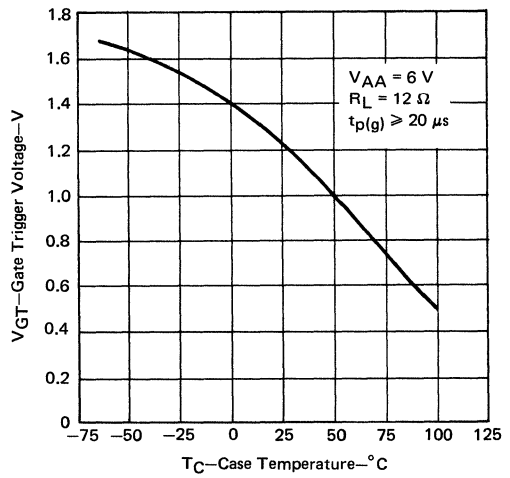


FIGURE 7

GATE VOLTAGE
vs
POSITIVE GATE CURRENT

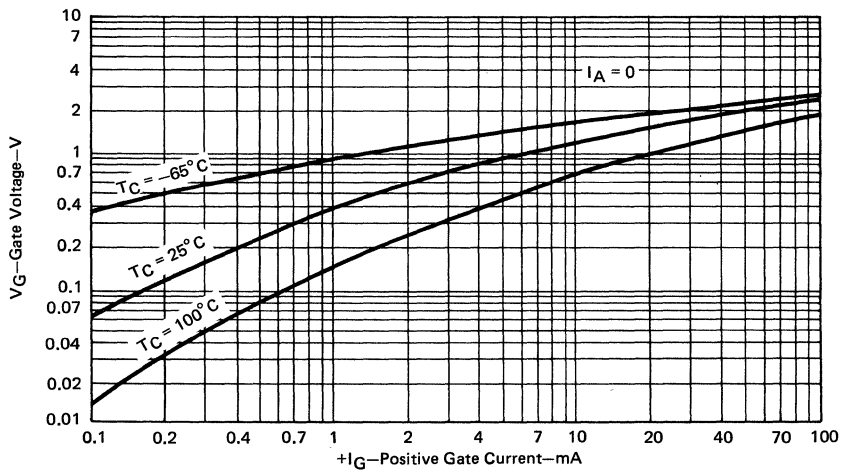


FIGURE 8

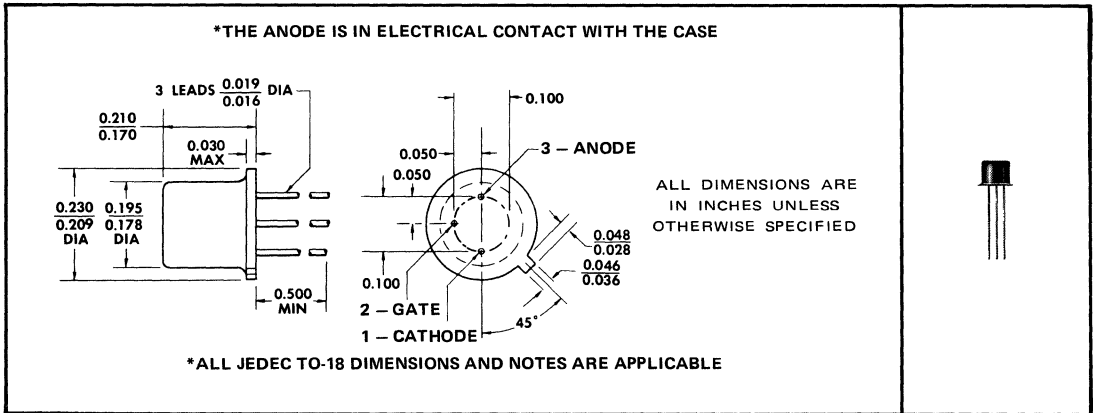
TYPES 2N3001, 2N3002, 2N3003, 2N3004 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

350 mA • 30 to 200 VOLTS • 20 μ A GATE SENSITIVITY
ALL PLANAR, OXIDE-PASSIVATED JUNCTIONS
NO SOLDER OR FLUXES

- High Operating Temperatures
- High Surge Current Capability
- Fast Switching Speeds
- Low Forward Voltage Drop

mechanical data

The devices are in a hermetically sealed welded case with a glass-to-metal seal between case and leads. Approximate weight is 0.35 grams.



TYPES 2N3001, 2N3002, 2N3003, 2N3004
 BULLETIN NO. DL-S-711164, DECEMBER 1971
 REPLACES DL-S-694260, AUGUST 1969

7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	2N3001	2N3002	2N3003	2N3004	UNIT
*Static Off-State Voltage, V_D (See Note 1)	30	60	100	200	V
*Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	30	60	100	200	V
*Static Reverse Voltage, V_R (See Note 2)	30	60	100	200	V
*Repetitive Peak Reverse Voltage, V_{RRM} (See Note 2)	30	60	100	200	V
*Continuous or RMS On-State Current at (or below) 55°C Free-Air Temperature (See Note 3)	350				mA
*Average On-State Current (180° Conduction Angle) at (or below) 55°C Free-Air Temperature (See Note 4)	250				mA
*Surge On-State Current (See Note 5)	6				A
Peak Negative Gate Voltage	8				V
*Peak Positive Gate Current (Pulse Width \leq 8 ms)	250				mA
*Average Gate Power Dissipation	100				mW
*Operating Free-Air Temperature Range	-65 to 150				°C
*Storage Temperature Range	-65 to 200				°C
*Lead Temperature 1/16 Inch from Case for 10 Seconds	300				°C

- NOTES:
1. These values apply when the gate-cathode resistance $R_{GK} \leq 1 \text{ k}\Omega$.
 2. These values apply when the gate-cathode resistance $R_{GK} \leq \infty$.
 3. This value applies for continuous d-c or single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C, derate according to Figure 1.
 4. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C, derate according to Figure 1.
 5. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 2N3001, 2N3002, 2N3003, 2N3004

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_D Static Off-State Current	$V_D = \text{Rated } V_D, R_{GK} = 1 \text{ k}\Omega$			0.1	μA
	$V_D = \text{Rated } V_D, R_{GK} = 1 \text{ k}\Omega, T_A = 150^\circ\text{C}$			100	
I_R Static Reverse Current	$V_R = \text{Rated } V_R, R_{GK} = \infty$			0.1	μA
	$V_R = \text{Rated } V_R, R_{GK} = \infty, T_A = 150^\circ\text{C}$			100	
I_G Gate Current	$V_G = -5 \text{ V}, I_A = 0$			-5	μA
I_{GT} Gate Trigger Current	$V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}$			5	μA
	$V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}, T_A = -65^\circ\text{C}$			20	
	$V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}$			0.9	
V_{GT} Gate Trigger Voltage	$V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}$			0.55	V
	$V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}, T_A = -65^\circ\text{C}$			0.7	
	$V_{AA} = 5 \text{ V}, R_L = 12 \Omega, t_{p(g)} \geq 10 \mu\text{s}, T_A = 150^\circ\text{C}$			0.2	
I_H Holding Current	$R_{GK} = 1 \text{ k}\Omega, R_L = 2 \text{ k}\Omega$			1.2	mA
	$R_{GK} = 1 \text{ k}\Omega, R_L = 2 \text{ k}\Omega, T_A = -65^\circ\text{C}$			3	
V_T On-State Voltage	$I_T = 350 \text{ mA}, R_{GK} \geq 1 \text{ k}\Omega, \text{ See Note 6}$			1.2	V
dv/dt Critical Rate of Rise of Off-State Voltage	$V_D = 1 \text{ V}$			400	V/ μs

NOTE 6: The initial instantaneous value is measured using pulse techniques. On-state pulse width = 300 μs , PRR = 100 pps.

*JEDEC registered data

switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	2N3004	UNIT
		TYPICAL	
t_{gt} Gate-Controlled Turn-On Time	$V_{AA} = 200 \text{ V}, R_L = 2.2 \text{ k}\Omega, R_G = 100 \Omega, V_{in} = 3 \text{ V}, \text{ See Figure 14}$	0.3	μs
t_q Circuit-Commutated Turn-Off Time	$V_{AA} = 50 \text{ V}, R_L = 140 \Omega, \text{ 1N645 between gate and cathode, See Figure 15}$	3.5	

thermal characteristics

PARAMETER	TYPICAL	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	75	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	275	

ON-STATE CURRENT DERATING CURVES

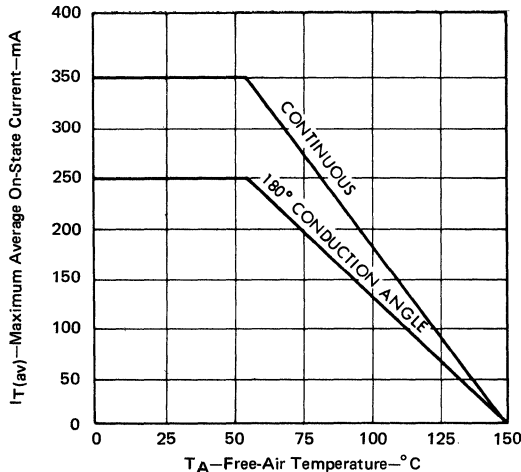
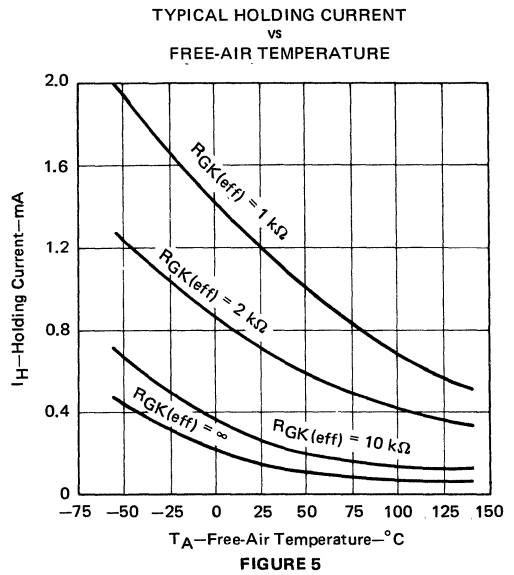
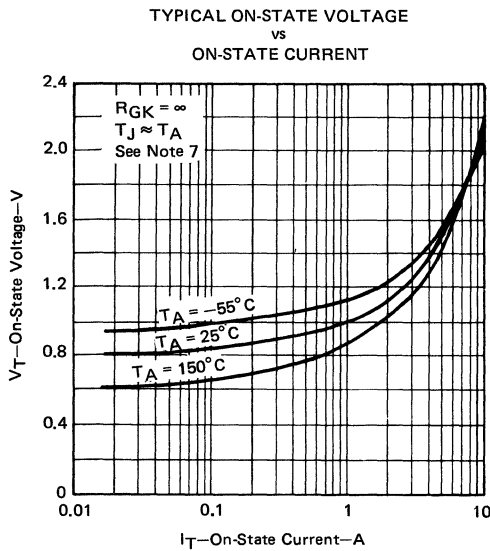
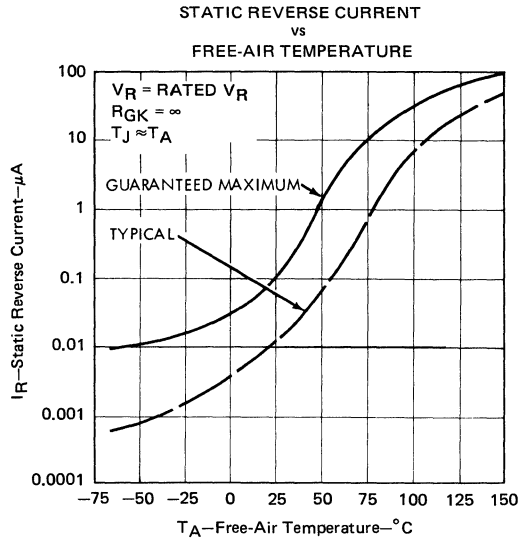
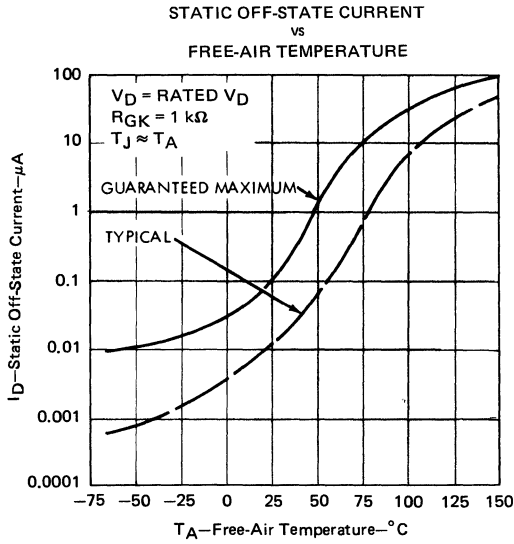


FIGURE 1

TYPES 2N3001, 2N3002, 2N3003, 2N3004

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

ANODE CHARACTERISTICS



NOTE 7: These parameters were measured using pulse techniques. $t_w = 300 \mu s$, PRR = 10 pps.

7

TYPES 2N3001, 2N3002, 2N3003, 2N3004

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

GATE CHARACTERISTICS

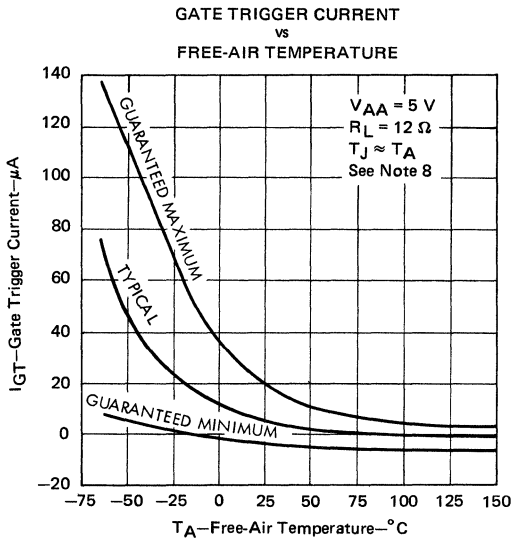


FIGURE 6

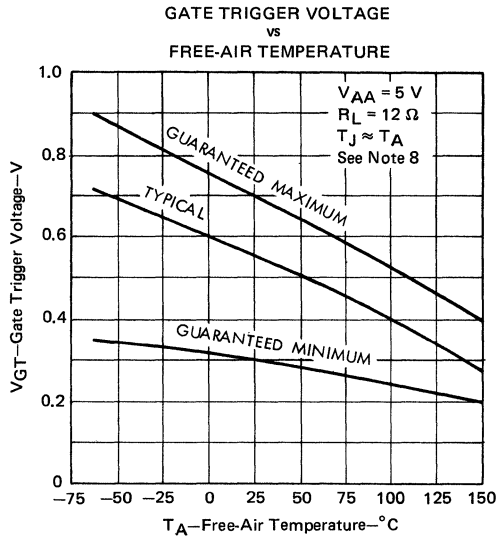


FIGURE 7

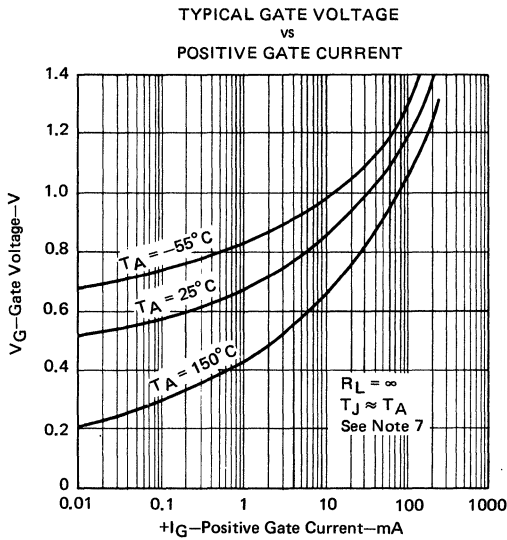


FIGURE 8

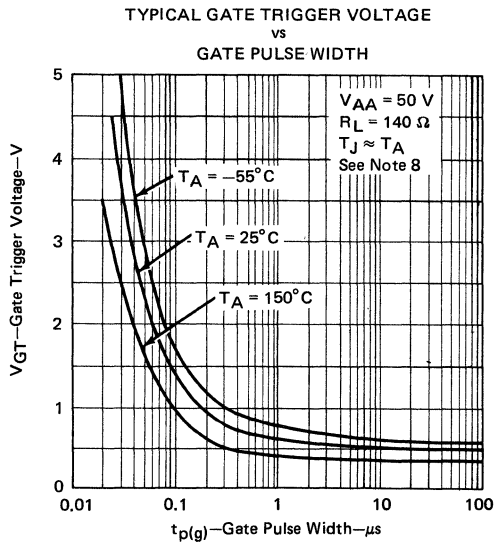


FIGURE 9

- NOTES: 7. These parameters were measured using pulse techniques. $t_w = 300 \mu s$, PRR = 10 pps.
8. These parameters were measured using single-pulse techniques. $t_w = 300 \mu s$, duty cycle = 0.

TYPES 2N3001, 2N3002, 2N3003, 2N3004 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL SWITCHING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

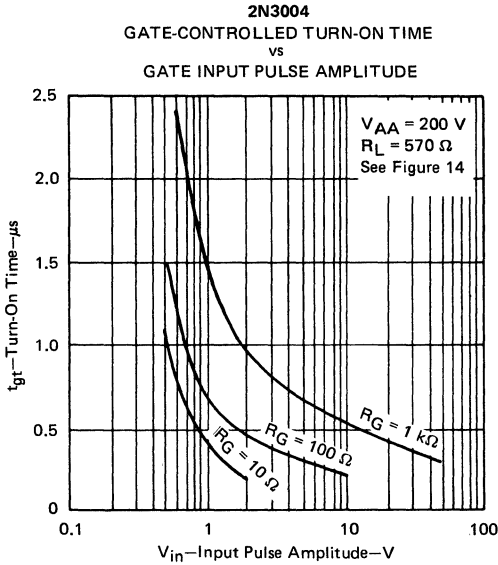


FIGURE 10

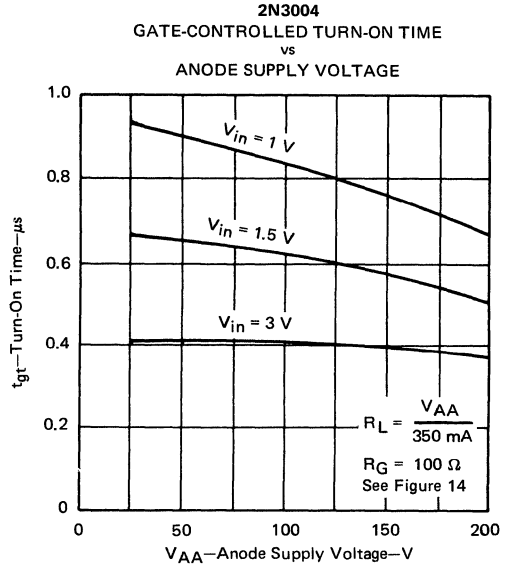


FIGURE 11

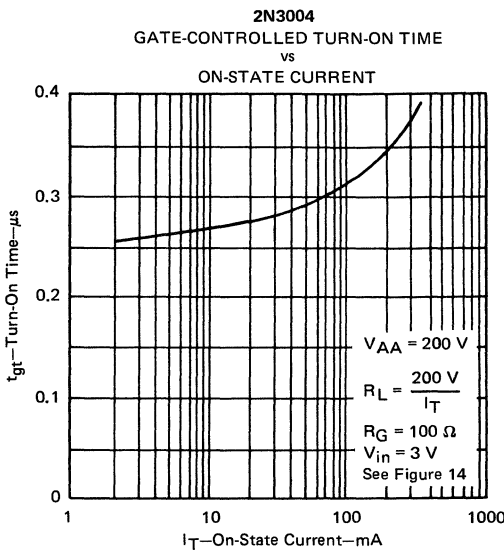


FIGURE 12

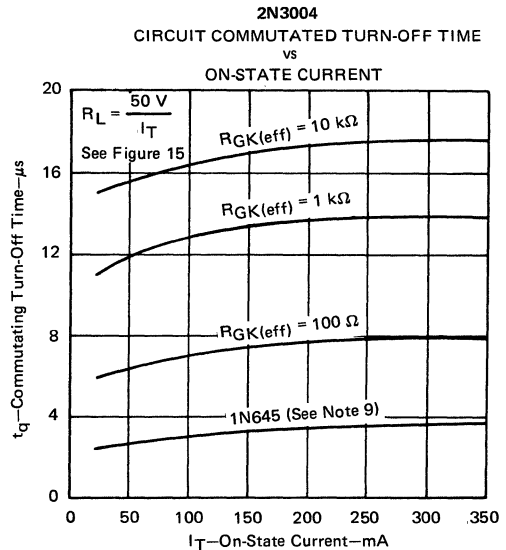


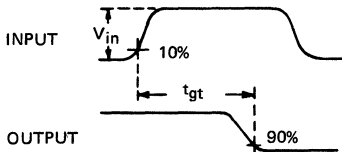
FIGURE 13

NOTE 9: The commutating turn-off time of the 2N3001 series thyristor is significantly affected by the source impedance of the gate firing circuit as shown in Figure 13. Faster turn-off times are achieved when this impedance is low. However, some circuits require the use of a high source impedance, even though fast turn-off is desired. In these applications, a diode may be used to by-pass the gate-cathode junction, as shown in the circuit in Figure 15. This diode improves commutating turn-off time by eliminating the effect of the gate-cathode recovery time.

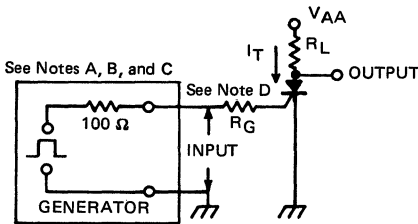
TYPES 2N3001, 2N3002, 2N3003, 2N3004

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

PARAMETER MEASUREMENT INFORMATION



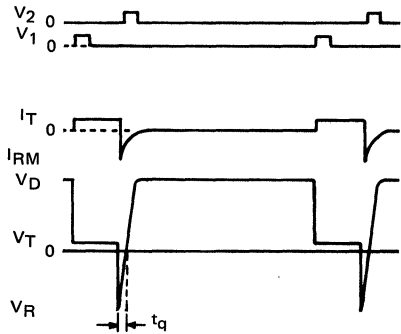
VOLTAGE WAVEFORMS



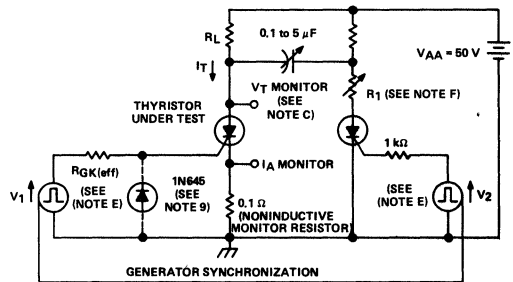
TEST CIRCUIT

FIGURE 14—TURN-ON TIME

- NOTES:
- A. V_{in} is measured with gate and cathode terminals connected as shown and anode terminal open.
 - B. The input waveform of Figure 14 has the following characteristics: $t_r \leq 40$ ns, $t_w \geq$ device turn-on time at the operating point.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 12$ pF.
 - D. R_G includes the total resistance of the generator and the external resistor.



WAVEFORMS



TEST CIRCUIT

FIGURE 15—COMMUTATING TURN-OFF TIME

- NOTES:
- E. Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50$ to 300 μ s, duty cycle = 1%. The pulse widths of V_1 and V_2 are ≥ 10 μ s.
 - F. Resistor R_1 is adjusted for $I_{RM} = 1$ A.

NOTE 9: The commutating turn-off time of the 2N3001 series thyristor is significantly affected by the source impedance of the gate firing circuit as shown in Figure 13. Faster turn-off times are achieved when this impedance is low. However, some circuits require the use of a high source impedance, even though fast turn-off is desired. In these applications, a diode may be used to by-pass the gate-cathode junction, as shown in the circuit in Figure 15. This diode improves commutating turn-off time by eliminating the effect of the gate-cathode recovery time.

7

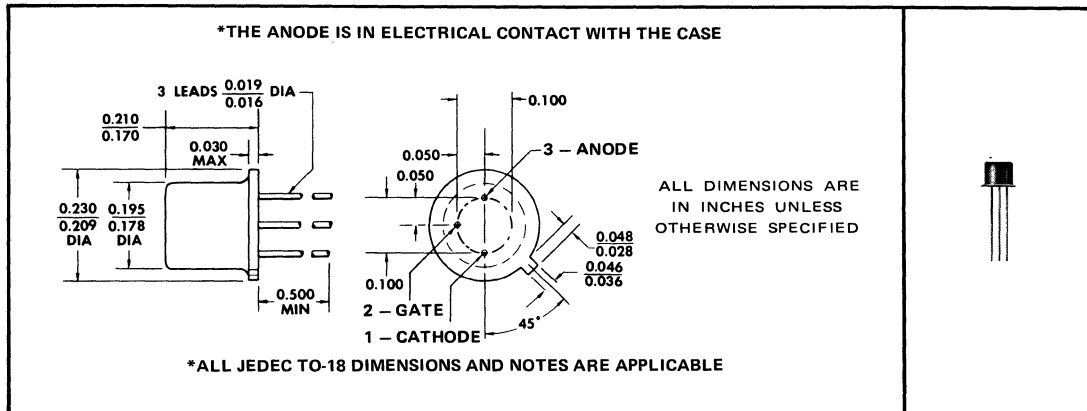
TYPES 2N3005, 2N3006, 2N3007, 2N3008 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

**350 mA • 30 to 200 VOLTS • 200 μ A GATE SENSITIVITY
ALL PLANAR, OXIDE-PASSIVATED JUNCTIONS—NO SOLDER OR FLUXES**

- High Operating Temperature
- Low Forward Voltage Drop
- High Surge Current Capability
- Gate Turn-Off Capability
- Fast Switching Speeds

mechanical data

The devices are in a hermetically sealed welded case with a glass-to-metal seal between case and leads. Approximate weight is 0.35 grams.



TYPES 2N3005, 2N3006, 2N3007, 2N3008
 BULLETIN NO. DLS-711866, DECEMBER 1971
 REPLACES DLS-694267, AUGUST 1969

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	2N3005	2N3006	2N3007	2N3008	UNIT
*Static Off-State Voltage, V_D (See Note 1)	30	60	100	200	V
*Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	30	60	100	200	V
*Static Reverse Voltage, V_R (See Note 2)	30	60	100	200	V
*Repetitive Peak Reverse Voltage, V_{RRM} (See Note 2)	30	60	100	200	V
*Continuous or RMS On-State Current at (or below) 55°C Free-Air Temperature (See Note 3)	350				mA
*Average On-State Current (180° Conduction Angle) at (or below) 55°C Free-Air Temperature (See Note 4)	250				mA
*Surge On-State Current (See Note 5)	6				A
Peak Negative Gate Voltage	8				V
*Peak Positive Gate Current (Pulse Width \leq 8 ms)	250				mA
*Average Gate Power Dissipation	100				mW
*Operating Free-Air Temperature Range	-65 to 200				°C
*Storage Temperature Range	-65 to 175				°C
*Lead Temperature 1/16 Inch from Case for 10 Seconds	300				°C

- NOTES:
1. These values apply when the gate-cathode resistance $R_{GK} \leq 1 \text{ k}\Omega$.
 2. These values apply when the gate-cathode resistance $R_{GK} < \infty$.
 3. This value applies for continuous d-c or single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C, derate according to Figure 13.
 4. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C, derate according to Figure 13.
 5. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

7

TYPES 2N3005, 2N3006, 2N3007, 2N3008

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _D Static Off-State Current	V _D = Rated V _D , R _{GK} = 1 kΩ		0.1		μA
	V _D = Rated V _D , R _{GK} = 1 kΩ, T _A = 150°C		100		
I _R Static Reverse Current	V _R = Rated V _R , R _{GK} = ∞		0.1		μA
	V _R = Rated V _R , R _{GK} = ∞, T _A = 150°C		100		
I _G Gate Current ¹	V _G = -5 V, I _A = 0		-5		μA
I _{GT} Gate Trigger Current	V _{AA} = 5 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs		90	200	μA
V _{GT} Gate Trigger Voltage	V _{AA} = 5 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs, T _A = -65°C		0.9		V
	V _{AA} = 5 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs		0.6	0.8	
	V _{AA} = 5 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs, T _A = 150°C	0.2			
I _H Holding Current	R _{GK} = 1 kΩ, R _L = 2 kΩ		1.8	5	mA
	R _{GK} = 1 kΩ, R _L = 2 kΩ, T _A = -65°C			8	
V _T On-State Voltage	I _T = 350 mA, R _{GK} ≥ 1 kΩ, See Note 6		1.2		V
I _{GQ} Static Gate Turn-Off Current	I _T = 200 mA (See Note 7),		40		mA
V _{GQ} Static Gate Turn-Off Voltage	V _{AA} ≤ 100 V (Not to exceed rated V _D)		-4		V
dv/dt Critical Rate of Rise of Off-State Voltage	V _D = 1 V		400		V/μs

NOTES: 6. The initial instantaneous value is measured using pulse techniques. On-state pulse width = 300 μs, PRR = 10 pps.

7. Anode current should not exceed 200 mA for gate turn-off applications.

*JEDEC registered data

switching characteristics at 25°C free-air temperature

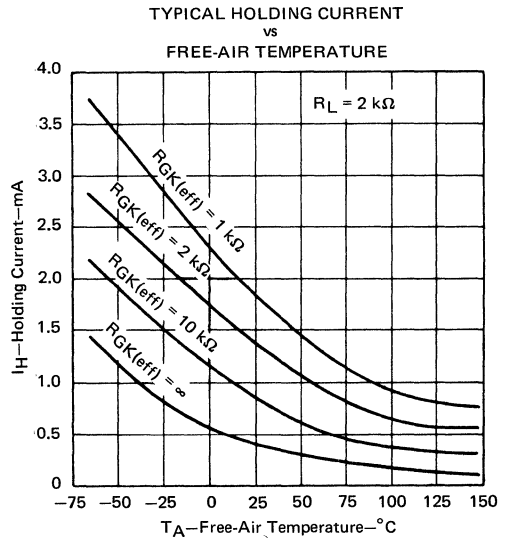
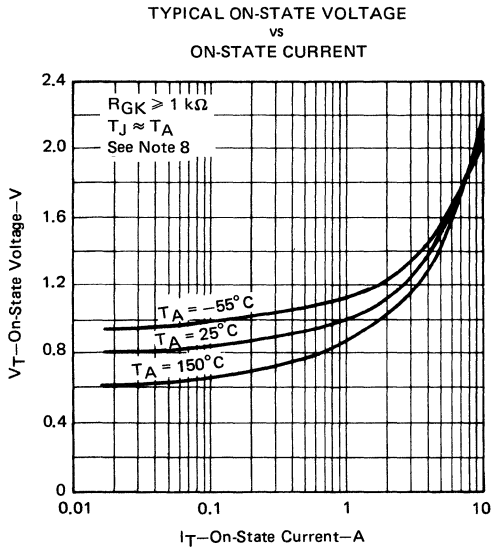
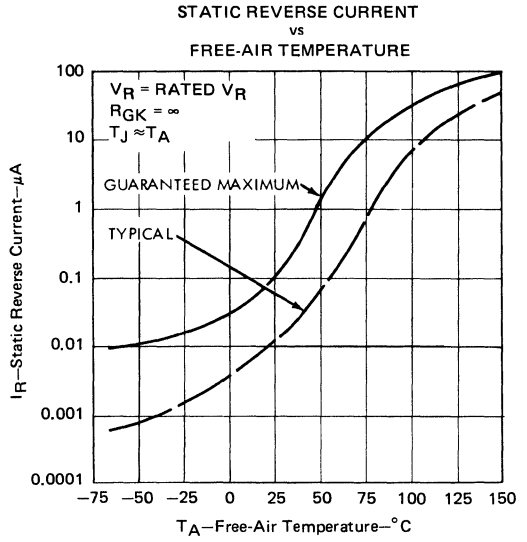
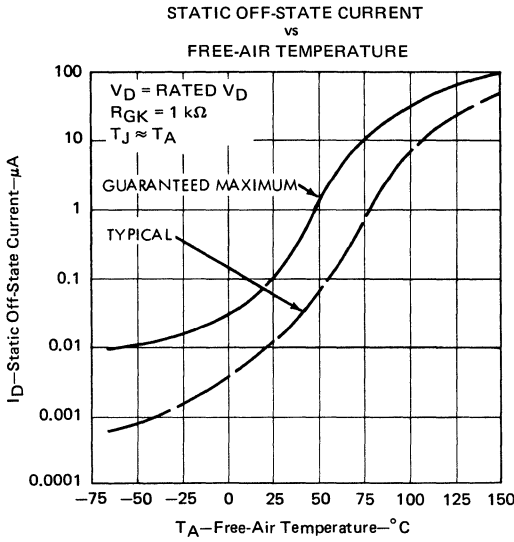
PARAMETER	TEST CONDITIONS	2N3008	UNIT
		TYPICAL	
t _{gt} Gate-Controlled Turn-On Time	V _{AA} = 200 V, R _L = 2.2 kΩ, R _G = 100 Ω, V _{in} = 3 V, See Figure 14	0.55	μs
t _q Circuit-Commutated Turn-Off Time	V _{AA} = 50 V, R _L = 140 Ω, 1N645 between gate and cathode, See Figure 15	2.2	

thermal characteristics

PARAMETER	TYPICAL	UNIT
R _{θJC} Junction-to-Case Thermal Resistance	75	°C/W
R _{θJA} Junction-to-Free-Air Thermal Resistance	275	

TYPES 2N3005, 2N3006, 2N3007, 2N3008 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

ANODE CHARACTERISTICS



7

NOTE 8: These parameters were measured using pulse techniques. $t_w = 300 \mu s$, PRR = 10 pps.

TYPES 2N3005, 2N3006, 2N3007, 2N3008

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

GATE CHARACTERISTICS

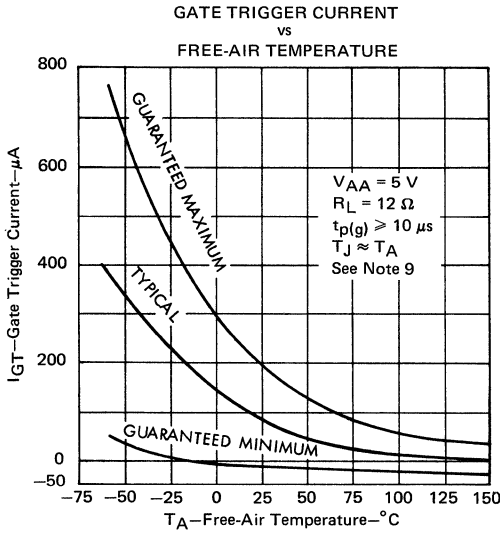


FIGURE 5

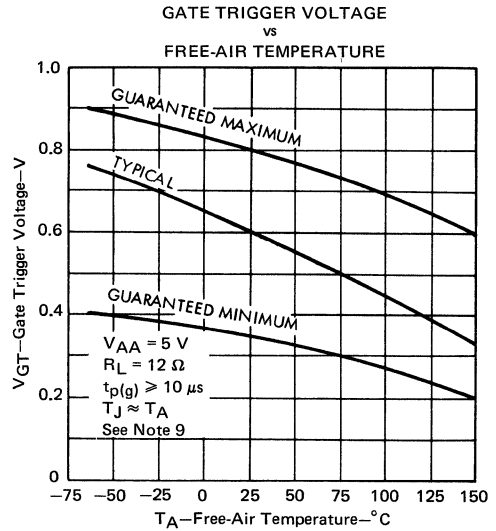


FIGURE 6

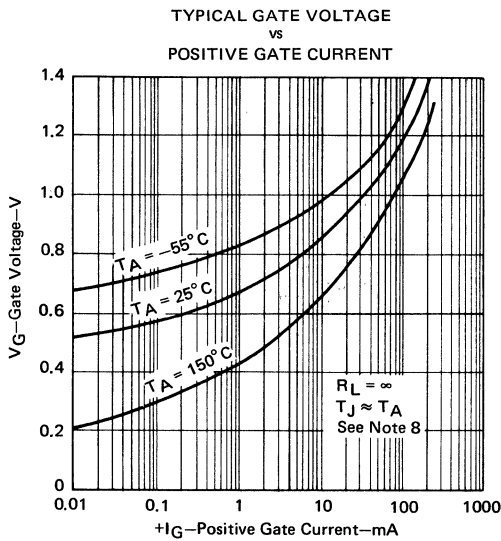


FIGURE 7

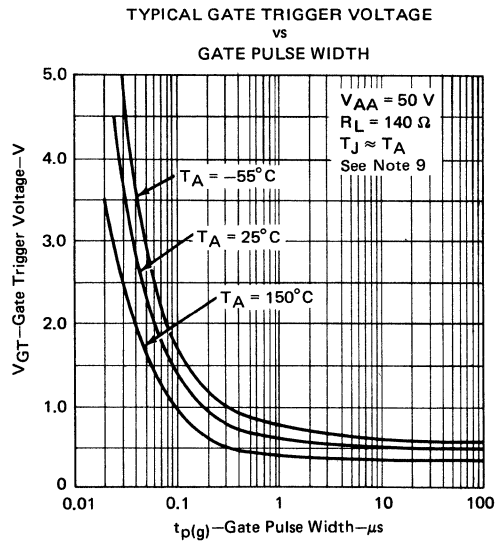
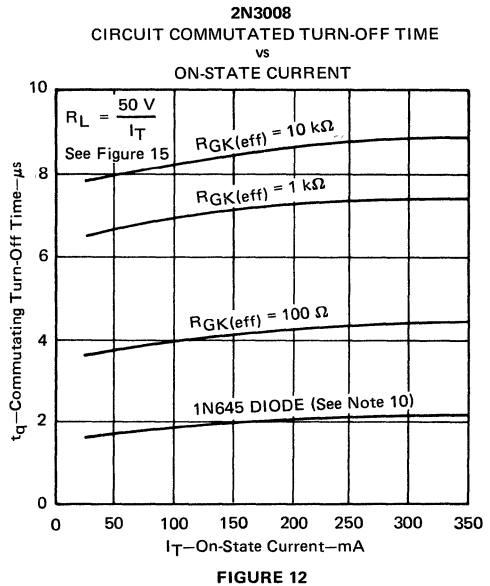
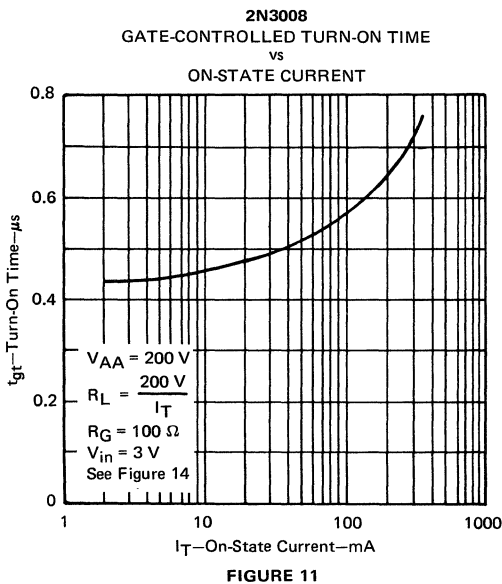
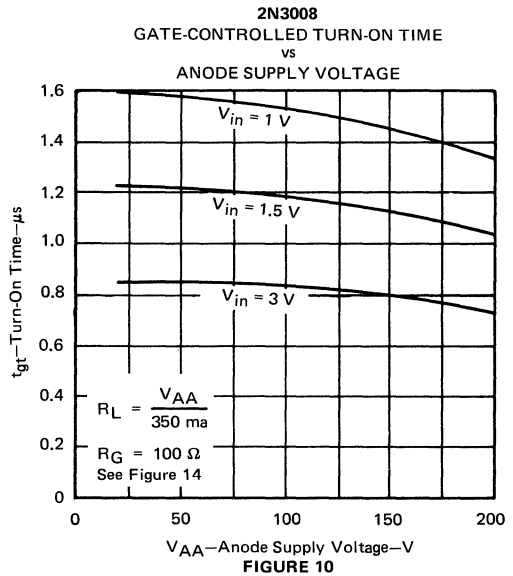
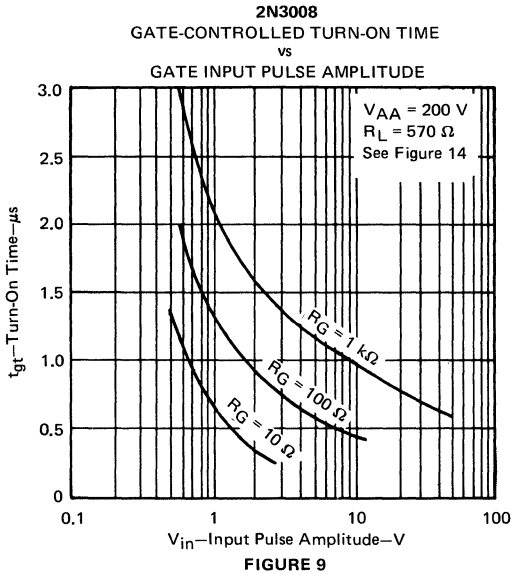


FIGURE 8

- NOTES: 8. These parameters were measured using pulse techniques. $t_w = 300 \mu s$, PRR = 10 pps.
 9. These parameters were measured using single-pulse techniques. $t_w = 300 \mu s$, duty cycle = 0.

TYPES 2N3005, 2N3006, 2N3007, 2N3008 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL SWITCHING CHARACTERISTICS, $T_A = 25^\circ\text{C}$



NOTE 10: The commutating turn-off time of the 2N3005 series thyristor is significantly affected by the source impedance of the gate firing circuit as shown in Figure 12. Faster turn-off times are achieved when this impedance is low. However, some circuits require the use of a high source impedance, even though fast turn-off is desired. In these applications, a diode may be used to by-pass the gate-cathode junction, as shown in the circuit in Figure 15. This diode improves commutating turn-off time by eliminating the effect of the gate-cathode recovery time.

TYPES 2N3005, 2N3006, 2N3007, 2N3008

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

ON-STATE CURRENT DERATING CURVE

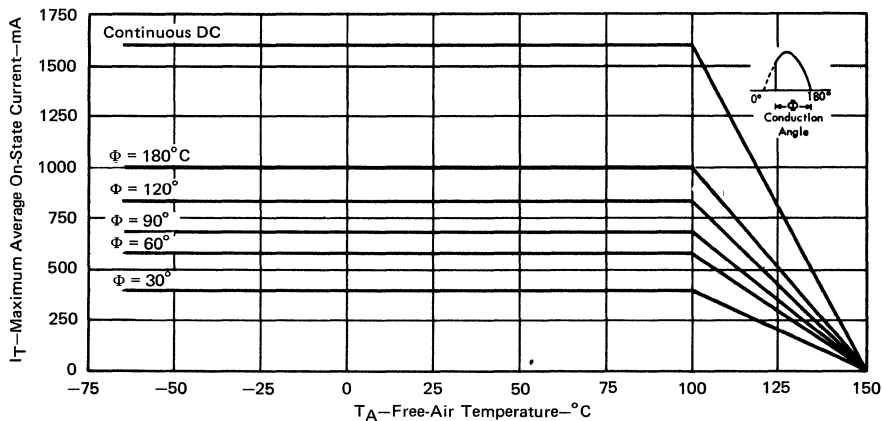
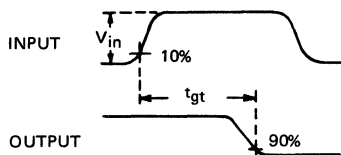
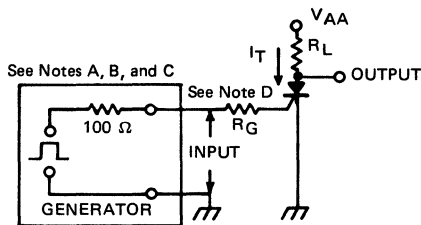


FIGURE 13

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS



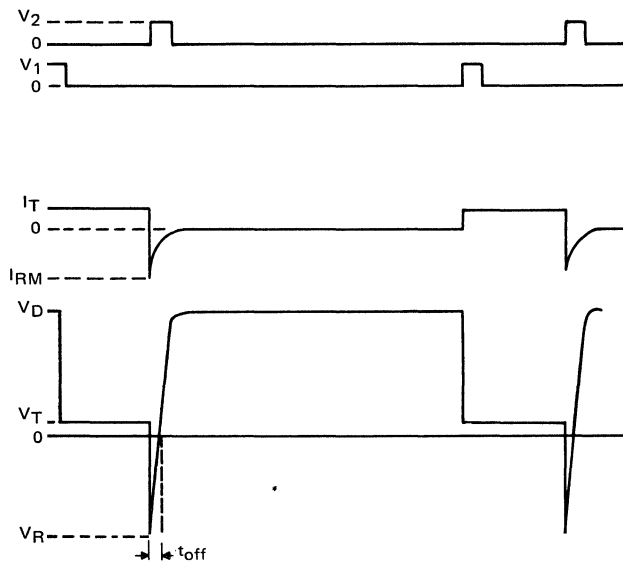
TEST CIRCUIT

FIGURE 14—TURN-ON TIME

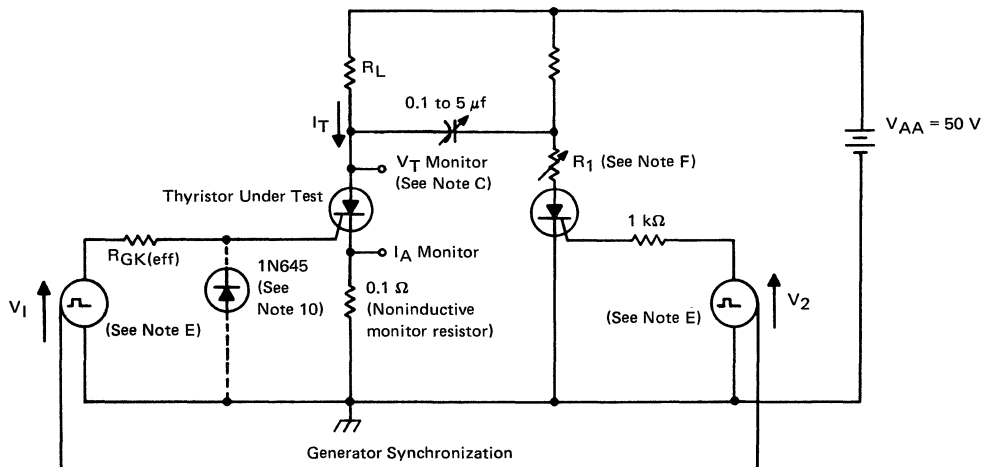
- NOTES: A. V_{in} is measured with gate and cathode terminals connected as shown and anode terminal open.
 B. The input waveform of Figure 14 has the following characteristics: $t_r \leq 40$ ns, $t_w \geq$ device turn-on time at the operating point.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 12$ pF.
 D. R_G includes the total resistance of the generator and the external resistor.

TYPES 2N3005, 2N3006, 2N3007, 2N3008 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

PARAMETER MEASUREMENT INFORMATION



WAVEFORMS



TEST CIRCUIT

- NOTES: E. Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50$ to $300 \mu\text{s}$, duty cycle = 1%. The pulse widths of V_1 and V_2 are $\geq 10 \mu\text{s}$.
 F. Resistor R_1 is adjusted for $I_{RM} = 1 \text{ A}$.

FIGURE 15—CIRCUIT COMMUTATED TURN-OFF TIME

NOTE 10: The commutating turn-off time of the 2N3005 series thyristor is significantly affected by the source impedance of the gate firing circuit as shown in Figure 12. Faster turn-off times are achieved when this impedance is low. However, some circuits require the use of a high source impedance, even though fast turn-off is desired. In these applications, a diode may be used to by-pass the gate-cathode junction, as shown in the circuit in Figure 15. This diode improves commutating turn-off time by eliminating the effect of the gate-cathode recovery time.

TYPES 2N3005, 2N3006, 2N3007, 2N3008

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL GATE TURN-OFF CHARACTERISTICS

The 2N3005 series thyristors exhibit gate-turn-off gain, in addition to the standard controlled switch characteristics. Figure 16 shows the typical gate-turn-off gain as a function of on-state current. This characteristic offers increased flexibility in the design of pulse-width modulators, pulse-forming networks, static switches, choppers, bistable circuits, and inverters.

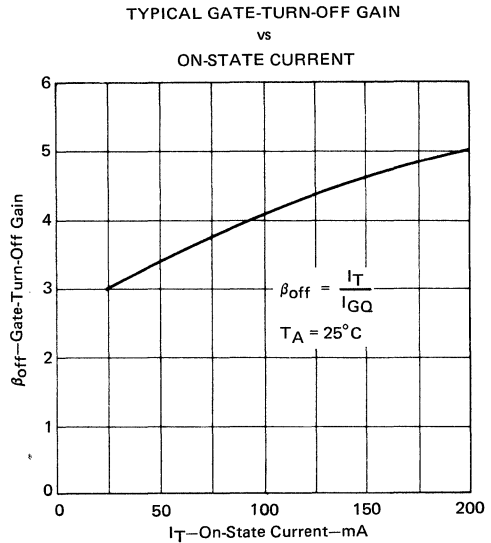
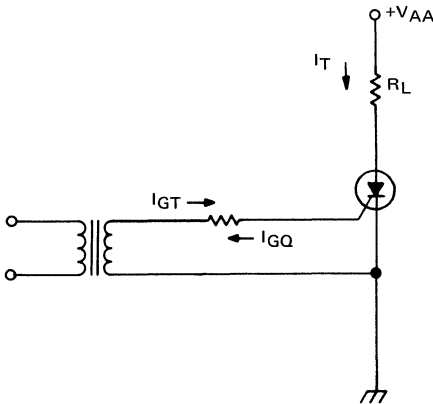
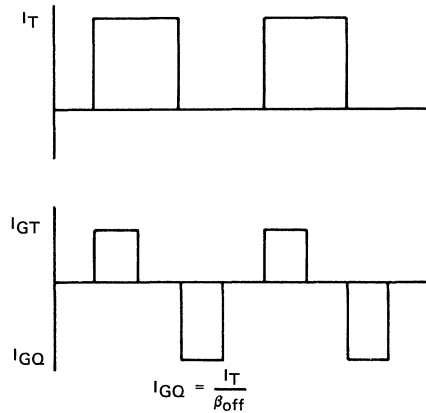


FIGURE 16

7



TYPICAL GATE-TURN-OFF CIRCUIT



TYPICAL WAVEFORMS

Improved turn-off time may be realized using the gate-turn-off method. A combination of gate-turn-off and standard commutating turn-off will further improve the turn-off time. For applications requiring a guaranteed β_{off} , contact your nearest TI Sales Office for information on special types.

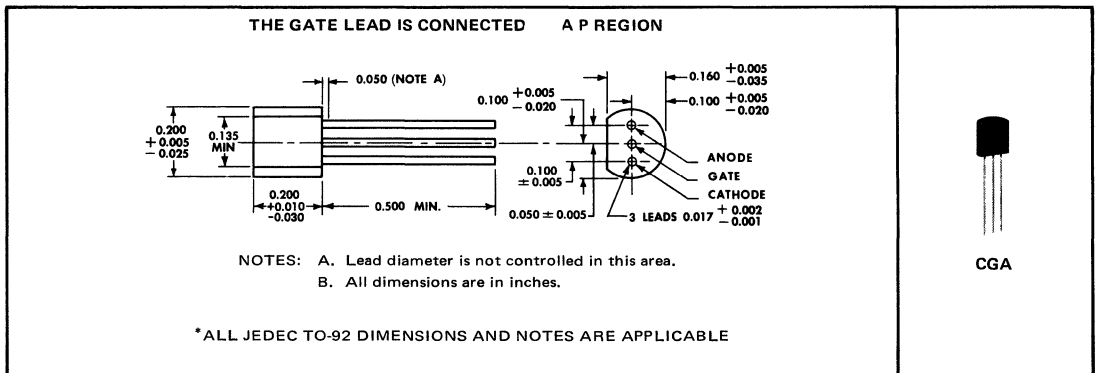
TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64 P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

SILECT† THYRISTORS‡
800 mA DC • 30 thru 200 VOLTS

TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64
BULLETIN NO. DL-S-7111587, NOVEMBER 1971

mechanical data

These thyristors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high-humidity conditions and are capable of meeting MIL-STD-202C method 106B. The thyristors are insensitive to light.



absolute maximum ratings at specified case temperature

		2N5060	2N5061	2N5062	2N5063	2N5064	UNIT	
		TIC60	TIC61	TIC62	TIC63	TIC64		
*Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	-65°C to 125°C	30	60	100	150	200	V	
*Repetitive Peak Reverse Voltage, V_{RRM}	-65°C to 125°C	30	60	100	150	200	V	
*Nonrepetitive Peak Reverse Voltage, V_{RSM} (Pulse Width \leq 5 ms)	-65°C to 125°C	45	80	125	180	230	V	
Continuous On-State Current (See Note 2)	-65°C to 50°C	800						mA
*Average On-State Current (180° Conduction Angle, See Note 3)	-65°C to 67°C	510						mA
*Surge On-State Current (See Note 4)	25°C	6						A
*Peak Positive Gate Current (Pulse Width \leq 300 μ s, $f \leq$ 120 pps)	25°C	1						A
*Peak Gate Reverse Voltage	-65°C to 125°C	5						V
*Average Gate Power Dissipation (See Note 5)	25°C	10						mW
*Peak Gate Power Dissipation (Pulse Width \leq 300 μ s)	25°C	100						mW
*Operating Case Temperature Range		-65 to 125						°C
*Storage Temperature Range		-65 to 150						°C
*Lead Temperature 1/16 Inch from Case for 10 Seconds		230						°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} = 1 \text{ k}\Omega$.
 2. These values apply for continuous d-c operation with resistive load. Above 50°C derate according to Figure 1.
 3. This value may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 67°C derate according to Figure 1.
 4. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
 5. This value applies for a maximum averaging time of 16.6 ms.

*JEDEC registered data. The asterisk identifies JEDEC registered data for the 2N5060 through 2N5064 only. This data sheet contains all applicable registered data in effect at the time of publication.

† Trademark of Texas Instruments

‡U.S. Patent No. 3,439,238

7

TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at specified case temperature

PARAMETER	TEST CONDITIONS	2N5060 THRU 2N5064		TIC60 THRU TIC64		UNIT
		MIN	MAX	MIN	MAX	
I_{DRM} Repetitive Peak Off-State Current	$V_D = \text{Rated } V_{DRM}, R_{GK} = 1 \text{ k}\Omega, 125^\circ\text{C}$		50*		50	μA
I_{RRM} Repetitive Peak Reverse Current	$V_R = \text{Rated } V_{RRM}, R_{GK} = 1 \text{ k}\Omega, 125^\circ\text{C}$		50*		50	μA
I_{GT} Gate Trigger Current	$V_{AA} = 7 \text{ V}, R_L = 100 \Omega, -65^\circ\text{C}$ $R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 1 \text{ ms}, 25^\circ\text{C}$		350*		200	μA
V_{GT} Gate Trigger Voltage	$V_{AA} = 7 \text{ V}, R_L = 100 \Omega, -65^\circ\text{C}$ $R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 1 \text{ ms}, 25^\circ\text{C}$		1.2*		0.8	V
	$V_D = \text{Rated } V_{DRM}, R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 1 \text{ ms}, 125^\circ\text{C}$	0.1*		0.1		
I_H Holding Current	$V_{AA} = 7 \text{ V}, R_{GK} = 1 \text{ k}\Omega, -65^\circ\text{C}$ Initiating $I_T = 20 \text{ mA}, 25^\circ\text{C}$		10*		5	mA
					5	
V_{TM} Peak On-State Voltage	$I_{TM} = 1.2 \text{ A}, \text{ See Note 6}, 25^\circ\text{C}$		1.7*		1.7	V

*thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	75	$^\circ\text{C/W}$

NOTE 6: This parameter must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 1\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

*JEDEC registered data

THERMAL INFORMATION

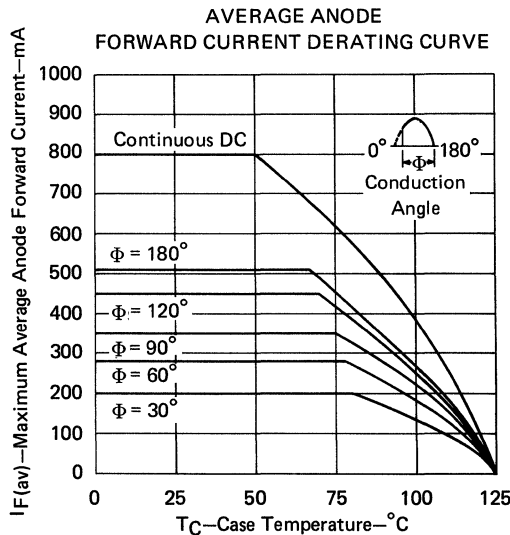


FIGURE 1

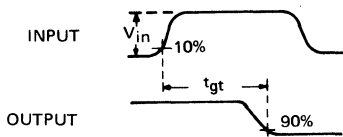
TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

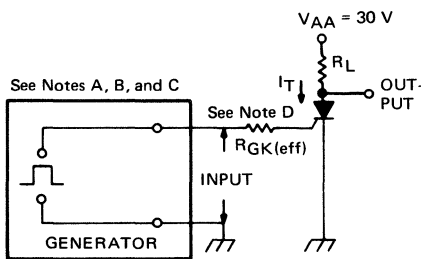
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{gt} Gate-Controlled Turn-On-Time	$V_{AA} = 30\text{ V}$, $R_L = 39\ \Omega$, $R_{GK(\text{eff})} = 20\ \text{k}\Omega$, $V_{in} = 20\text{ V}$, See Figure 2	3	μs
t_q Circuit-Commutated Turn-Off Time	$V_{AA} = 30\text{ V}$, $R_L = 30\ \Omega$, $I_{RM} \approx 7\text{ A}$, See Figure 3	7	μs

PARAMETER MEASUREMENT INFORMATION

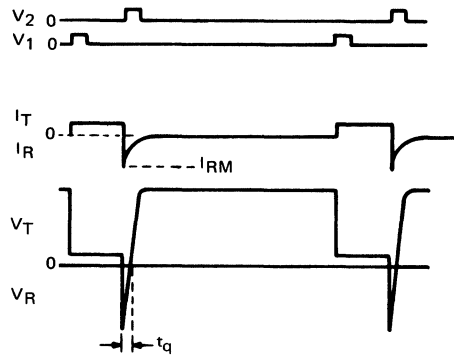


VOLTAGE WAVEFORMS

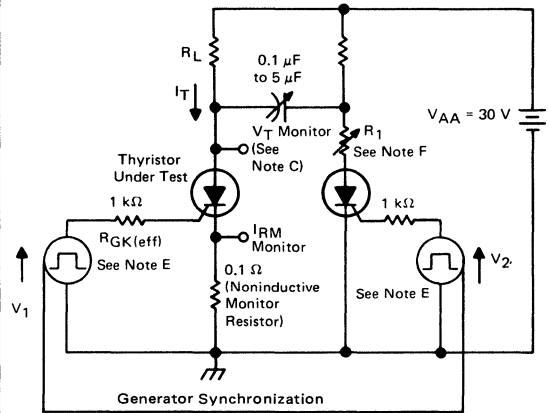


TEST CIRCUIT

FIGURE 2—GATE-CONTROLLED TURN-ON TIME



WAVEFORMS



TEST CIRCUIT

FIGURE 3—CIRCUIT-COMMUTATED TURN-OFF TIME

- NOTES:
- V_{in} is measured with gate and cathode terminals open.
 - The input waveform of Figure 2 has the following characteristics: $t_r \leq 40\text{ ns}$, $t_w \geq 20\ \mu\text{s}$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14\text{ ns}$, $R_{in} \geq 10\ \text{M}\Omega$, $C_{in} \leq 12\ \text{pF}$.
 - $R_{GK(\text{eff})}$ includes the total resistance of the generator and the external resistor.
 - Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50\text{ to }300\ \mu\text{s}$, duty cycle = 1%. The pulse widths of V_1 and V_2 are $\geq 10\ \mu\text{s}$.
 - Resistor R_1 is adjusted for $I_{RM} \approx 7\text{ A}$.

TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64 P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

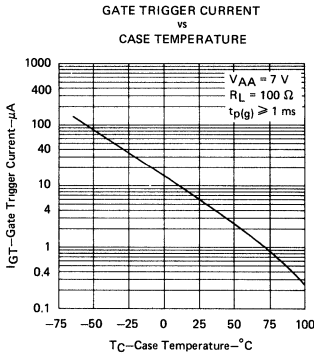


FIGURE 4

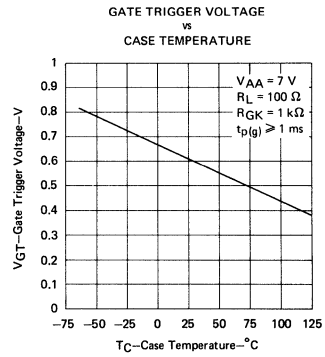


FIGURE 5

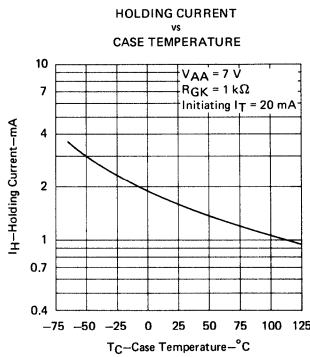


FIGURE 6

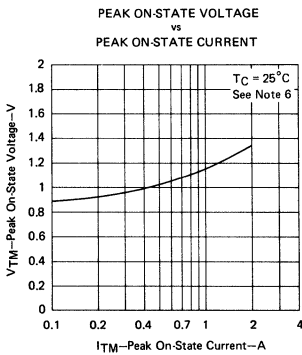


FIGURE 7

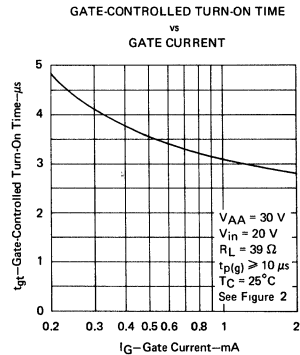


FIGURE 8

NOTE 6: This parameter must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

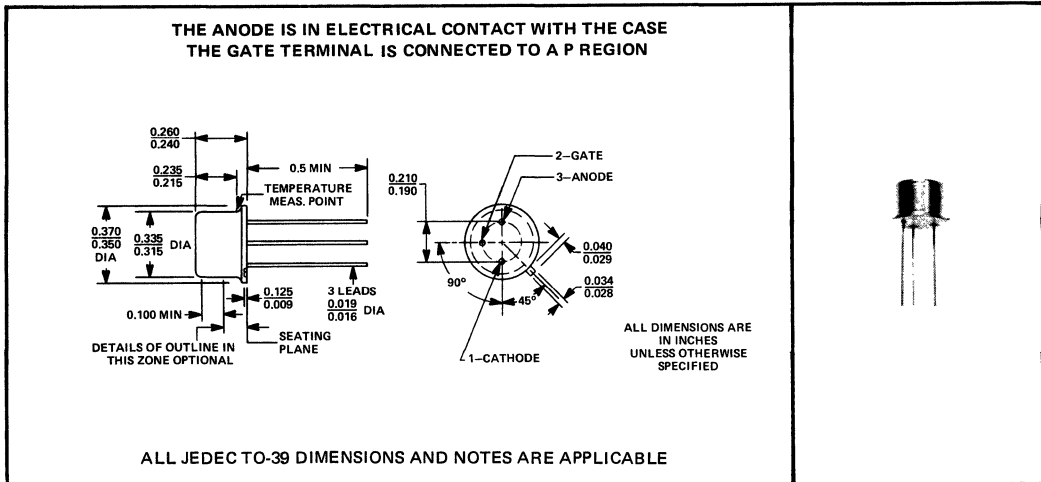
TYPES 2N6332 THRU 2N6337 PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

2 AMP DC • 30 to 400 VOLTS • 200 μ A GATE SENSITIVITY

- High Operating Temperatures
- High Surge Current Capability
- Fast Switching Speeds
- Low Forward Voltage Drop

TYPES 2N6332 THRU 2N6337
BULLETIN NO. DL-S-7211633, JANUARY 1972

mechanical data



*absolute maximum ratings over operating case temperature range (unless otherwise noted)

	2N6332	2N6333	2N6334	2N6335	2N6336	2N6337	UNIT
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	30	50	100	200	300	400	V
Repetitive Peak Reverse Voltage, V_{RRM}	30	50	100	200	300	400	V
Nonrepetitive Peak Reverse Voltage (See Note 2)	30	50	100	200	300	400	V
Continuous On-State Current at (or below) 80°C Case Temperature (See Note 3)	2						A
Average On-State Current (180° Conduction Angle) at (or below) 80°C Case Temperature (See Note 4)	1.25						A
Surge On-State Current (See Note 2)	20						A
Peak Negative Gate Voltage	5						V
Peak Positive Gate Current (Pulse Width \leq 300 μ s)	0.2						A
Peak Gate Power Dissipation (Pulse Width \leq 300 μ s)	1.3						W
Average Gate Power Dissipation (See Note 5)	0.3						W
Operating Case Temperature Range	-40 to 150						°C
Storage Temperature Range	-40 to 175						°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230						°C

- NOTES:
1. These values apply when the gate-cathode resistance $R_{GK} = 1 \text{ k}\Omega$.
 2. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
 3. These values apply for continuous d-c operation with resistive load. Above 80°C derate linearly 150°C case temperature at the rate of 28.6 mA/°C.
 4. This value may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 80°C derate linearly to 150°C case temperature at the rate of 17.9 mA/°C.
 5. This value applies for a maximum averaging time of 16.6 ms.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

7

TYPES 2N6332 THRU 2N6337

PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DRM} Repetitive Peak Off-State Current	V _D = Rated V _{DRM} , R _{GK} = 1 kΩ			5	μA
	V _D = Rated V _{DRM} , R _{GK} = 1 kΩ, T _C = 150°C			150	
I _{RRM} Repetitive Peak Reverse Current	V _R = Rated V _{RRM} , I _G = 0			10	μA
	V _R = Rated V _{RRM} , I _G = 0, T _C = 150°C			250	
I _{GM} Peak Gate Current	V _{GM} = -5 V, I _A = 0			-10	μA
I _{GT} Gate Trigger Current	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs, T _C = -40°C			500	μA
	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs			5 200	
V _{GT} Gate Trigger Voltage	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs, T _C = -40°C			1	V
	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs	0.55	0.8		
	V _{AA} = Rated V _{DRM} , R _L = 1 kΩ, t _{p(g)} ≥ 10 μs, T _C = 150°C	0.2			
I _H Holding Current	V _{AA} = 6 V, R _{GK} = 1 kΩ, Initiating I _{TM} = 35 mA, T _C = -40°C			15	mA
	V _{AA} = 6 V, R _{GK} = 1 kΩ, Initiating I _{TM} = 25 mA			3 5	
V _{TM} Peak On-State Voltage	I _{TM} = 3.9 A, R _{GK} ≥ 1 kΩ, See Note 6			2.5	V
V _T Static On-State Voltage	I _T = 2 A, R _{GK} ≥ 1 kΩ, See Note 6			1.75	V
dv/dt Critical Rate of Rise of Off-State Voltage	V _D = Rated V _{DRM} , V _{GK} = -1 V			400	V/μs

*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{gt} Gate-Controlled Turn-On Time	V _{AA} = Rated V _{DRM} , I _T = 3.9 A, R _G = 100 Ω, V _{in} = 3 V		0.3	2	μs
t _q Circuit-Commutated Turn-Off Time	V _{AA} = Rated V _{DRM} , I _T = 3.9 A, 1N645 between gate and cathode		15		μs

*thermal characteristics

PARAMETER	MAX	UNIT
R _{θJC} Junction-to-Case Thermal Resistance	20	°C/W

NOTE 6: This parameter must be measured using pulse techniques. t_w = 2 ms, duty cycle ≤ 2%. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

*JEDEC registered data

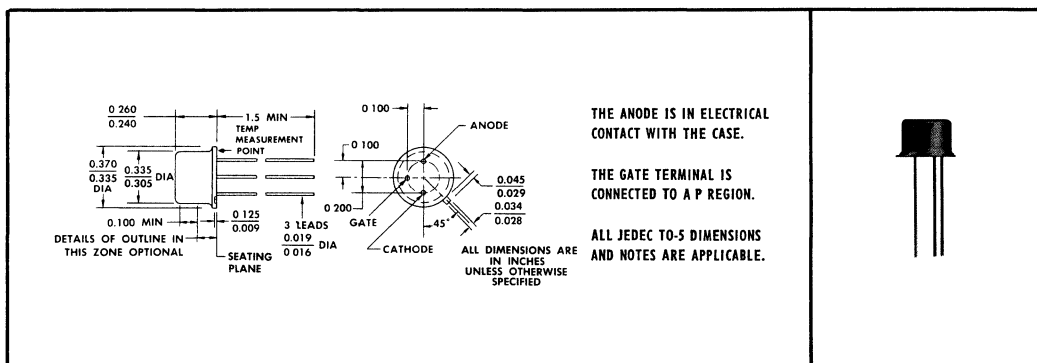
TYPES T1145A0 THRU T1145A4 P-N-P-N DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYISTORS

1.6 AMPS DC • 50 to 400 VOLTS

- High Surge Current Capability
- Low Forward Voltage Drop

TYPES T1145A0 THRU T1145A4
BULLETIN NO. DL-S-7111667, DECEMBER 1971
REPLACES BULLETIN NO. DL-S-668636, MAY 1966

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

	T1145A0	T1145A1	T1145A2	T1145A3	T1145A4	UNIT
Static Off-State Voltage, V_D (See Note 1)	50	100	200	300	400	V
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	50	100	200	300	400	V
Static Reverse Voltage, V_R (See Note 1)	50	100	200	300	400	V
Repetitive Peak Reverse Voltage, V_{RRM} (See Note 1)	50	100	200	300	400	V
Continuous or RMS On-State Current at (or below) 60°C Case Temperature (See Note 2)	1.6					A
Average On-State Current (180° Conduction Angle) at (or below) 60°C Case Temperature (See Note 3)	1.2					A
Surge On-State Current (See Note 4)	30					A
Peak Negative Gate Voltage	5					V
Peak Positive Gate Current (Pulse Width \leq 300 μ s)	2					A
Average Gate Power Dissipation (See Note 5)	300					mW
Operating Case Temperature Range	-65 to 105					°C
Storage Temperature Range	-65 to 150					°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300					°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} \leq \infty$.
2. This value applies for continuous d-c operation with resistive load. Above 60°C derate according to Figure 1.
3. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 60°C derate according to Figure 1.
4. These values apply for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
5. This value applies for a maximum averaging time of 16.6 ms.

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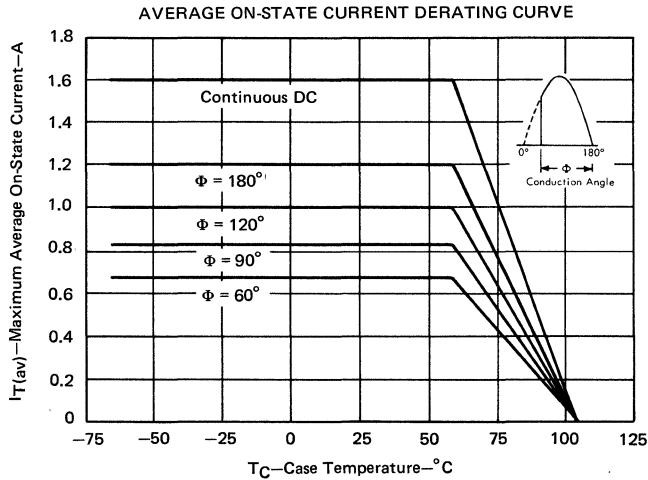
TYPES TI145A0 THRU TI145A4

P-N-P-N DIFFUSED SILICON REVERSE-BLOCKING TRIODE THYISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I _D	Static Off-State Current	V _D = Rated V _D , I _G = 0	0.25		mA
		V _D = Rated V _D , I _G = 0, T _C = 105°C		1	
I _R	Static Reverse Current	V _R = Rated V _R , I _G = 0	0.25		mA
		V _R = Rated V _R , I _G = 0, T _C = 105°C		1	
I _{GT}	Gate Trigger Current	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs	25		mA
V _{GT}	Gate Trigger Voltage	V _{AA} = 6 V, R _L = 12 Ω, t _{p(g)} ≥ 10 μs	0.25	3.5	V
I _H	Holding Current	R _L = 1 kΩ, I _G = 0	25		mA
V _T	On-State Voltage	I _T = 1 A, R _{GK} ≥ 1 kΩ		2	V

THERMAL INFORMATION



TYPES TIC35, TIC36

P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

 TYPES TIC35, TIC36
 BULLETIN NO. DLS-6911238, SEPTEMBER 1969

RADIATION-TOLERANT THYRISTORS

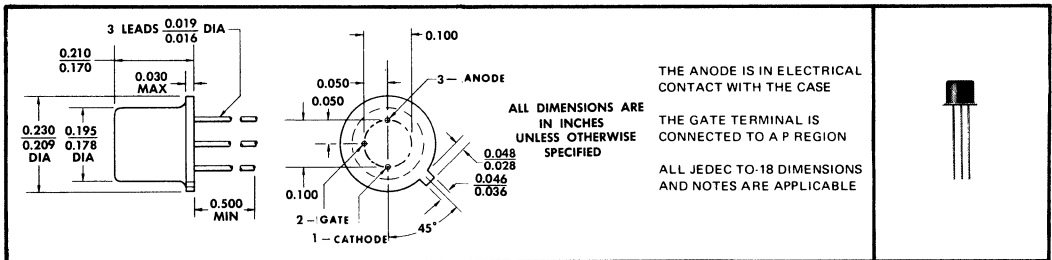
400 mA DC • 15 and 30 VOLTS

- Max I_{GT} of 5 mA after 1×10^{14} Fast Neutrons/cm²
- Max V_{TM} of 1.6 V at I_{TM} of 1 A after 1×10^{14} Fast Neutrons/cm²

description

The TIC35, TIC36 thyristors offer a significant advance in radiation-tolerant-device technology. Unique construction techniques produce thyristors which maintain useful characteristics after fast-neutron radiation fluences through 10^{15} n/cm².

mechanical data



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TIC35	TIC36	UNIT
Continuous Off-State Voltage, V_D (See Note 1)	15	30	V
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	15	30 ¹⁾	V
Continuous Reverse Voltage, V_R		5	V
Repetitive Peak Reverse Voltage, V_{RRM}		5	V
Nonrepetitive Peak Reverse Voltage, V_{RSM} (See Note 2)		5	V
Continuous On-State Current at (or below) 55°C Case Temperature (See Note 3)		400	mA
Continuous On-State Current at (or below) 25°C Free-Air Temperature (See Note 4)		225	mA
Average On-State Current (180° Conduction Angle) at (or below) 55°C Case Temperature (See Note 5)		320	mA
Surge On-State Current (See Note 6)		3	A
Peak Negative Gate Voltage		-4	V
Peak Positive Gate Current (Pulse Width $\leq 300 \mu s$)		250	mA
Peak Gate Power Dissipation (Pulse Width $\leq 300 \mu s$)		500	mW
Average Gate Power Dissipation		10	mW
Operating Free-Air or Case Temperature Range		-55 to 125	°C
Storage Temperature Range		-65 to 200	°C
Lead Temperature 1/16 Inch from Case for 10 Seconds		260	°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} = 1 \text{ k}\Omega$.
2. This value applies for a 5-ms rectangular pulse when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
3. These values apply for continuous d-c operation with resistive load. Above 55°C derate according to Figure 2.
4. These values apply for continuous d-c operation with resistive load. Above 25°C derate according to Figure 3.
5. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C derate according to Figure 2.
6. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

7

TYPES TIC35, TIC36

P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_D	Static Off-State Current	$V_D = \text{Rated } V_D$, $R_{GK} = 1 \text{ k}\Omega$, $T_A = 125^\circ\text{C}$			20	μA
I_R	Static Reverse Current	$V_R = 5 \text{ V}$, $R_{GK} = 1 \text{ k}\Omega$, $T_A = 125^\circ\text{C}$			100	μA
I_{GR}	Gate Reverse Current	$V_{KG} = 4 \text{ V}$, $I_A = 0$			5	μA
I_{GT}	Gate Trigger Current	$V_{AA} = 6 \text{ V}$, $R_L = 100 \Omega$, $V_{GG} = 6 \text{ V}$, $R_{G(\text{source})} \geq 10 \text{ k}\Omega$, $t_{p(g)} \geq 20 \mu\text{s}$, $T_A = -55^\circ\text{C}$			100	μA
		$V_{AA} = 6 \text{ V}$, $R_L = 100 \Omega$, $V_{GG} = 6 \text{ V}$, $R_{G(\text{source})} \geq 10 \text{ k}\Omega$, $t_{p(g)} \geq 20 \mu\text{s}$			20	
V_{GT}	Gate Trigger Voltage	$V_{AA} = 6 \text{ V}$, $R_L = 100 \Omega$, $R_{GK} = 1 \text{ k}\Omega$, $t_{p(g)} \geq 20 \mu\text{s}$, $T_A = -55^\circ\text{C}$			0.9	V
		$V_{AA} = \text{Rated } V_D$, $R_L = 100 \Omega$, $R_{GK} = 1 \text{ k}\Omega$, $t_{p(g)} \geq 20 \mu\text{s}$, $T_A = 125^\circ\text{C}$	0.2			
		$V_{AA} = 6 \text{ V}$, $R_L = 100 \Omega$, $R_{GK} = 1 \text{ k}\Omega$, $t_{p(g)} \geq 20 \mu\text{s}$			0.75	
I_H	Holding Current	$V_{AA} = 6 \text{ V}$, $R_{GK} = 1 \text{ k}\Omega$, Initiating $I_T = 10 \text{ mA}$, $T_A = -55^\circ\text{C}$			4	mA
		$V_{AA} = 6 \text{ V}$, $R_{GK} = 1 \text{ k}\Omega$, Initiating $I_T = 10 \text{ mA}$			2	
V_{TM}	Peak On-State Voltage	$I_{TM} = 1 \text{ A}$, See Note 7			1.6	V
dv/dt	Critical Rate of Rise of Off-State Voltage	$V_D = \text{Rated } V_D$, $R_{GK} = 1 \text{ k}\Omega$		12		V/ μs

7

post-irradiation electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	RADIATION FLUENCE†	MIN	TYP	MAX	UNIT
I_{GT}	Gate Trigger Current	$V_{AA} = 6 \text{ V}$, $R_L = 100 \Omega$	$1 \times 10^{14} \text{ n/cm}^2$			5	mA
V_{TM}	Peak On-State Voltage	$I_{TM} = 1 \text{ A}$, See Note 7	$1 \times 10^{14} \text{ n/cm}^2$			1.6	V

† Radiation is fast neutrons (n) at $E \geq 10 \text{ keV}$ (reactor spectrum).

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
θ_{J-C}	Junction-to-Case Thermal Resistance			124	$^\circ\text{C/W}$
θ_{J-A}	Junction-to-Free-Air Thermal Resistance			345	

NOTE: 7. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are used.

P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPES TIC35, TIC36

THERMAL INFORMATION

The minimum heat-sink requirements may be calculated for any anode-current, heat-sink combination by the following procedure:

1. Determine worst-case power dissipation from Figure 4.
2. Calculate maximum allowable case-to-free-air thermal resistance by use of the equation:

$$\theta_{C-A} = \frac{T_J - T_A}{P_{A(av)}} - \theta_{J-C}$$

where:

T_J = Junction temperature

T_A = Free-air temperature

$P_{A(av)}$ = Average anode power dissipation
(see Figure 4 for worst-case values)

θ_{J-C} = Junction-to-case thermal resistance
= 124°C/W maximum.

3. Determine area of heat sink from Figure 1.

EXAMPLE

Determine: Minimum size of 1/16"-thick copper heat sink for safe operation of thyristor at an average current of 0.3 A with a conduction angle of 180°.

Given: Maximum $T_J = 125^\circ\text{C}$
 $T_A = 35^\circ\text{C}$
 $\theta_{J-C} = 124^\circ\text{C/W}$

Solution: From Figure 4, $P_{A(av)} = 0.525\text{ W}$ for 0.3 A with 180° conduction angle. Using the equation of step 2 above:

$$\theta_{C-A} = \frac{125^\circ\text{C} - 35^\circ\text{C}}{0.525\text{ W}} - 124^\circ\text{C/W} = 47^\circ\text{C/W}$$

Figure 1 shows that for θ_{C-A} of 47°C/W, the area is 3.4 in². The minimum dimensions of the sides should be:

$$\sqrt{\frac{\text{area}}{2}} \sqrt{\frac{\text{area}}{2}} = \sqrt{\frac{3.4}{2}} \sqrt{\frac{3.4}{2}} = 1.3'' \times 1.3''$$

NOTES: 8. The thyristor is mounted in the center of a square heat sink vertically positioned in still free air with both sides exposed. The heat-sink area is twice the area of one side.

9. θ_{C-A} includes the case-to-heat sink thermal resistance, θ_{C-HS} , in addition to the heat-sink-to-free-air thermal resistance, θ_{HS-A} , and is defined by the equation, $\theta_{C-A} = \theta_{C-HS} + \theta_{HS-A}$.

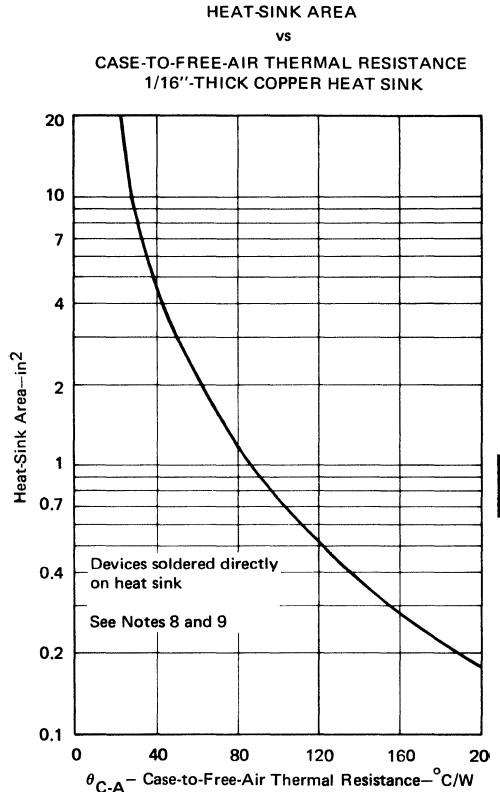


FIGURE 1

TYPES TIC35, TIC36 P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

THERMAL INFORMATION

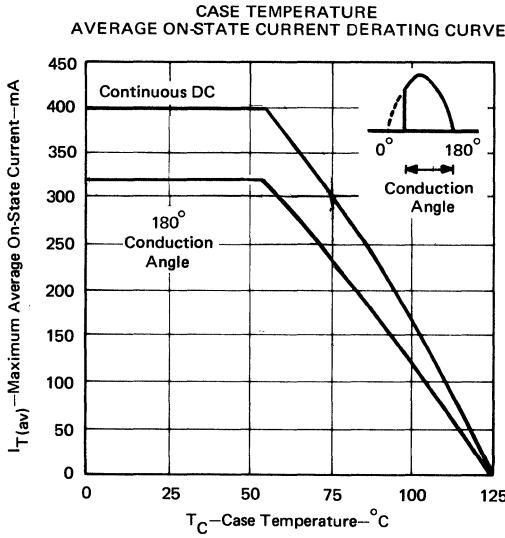


FIGURE 2

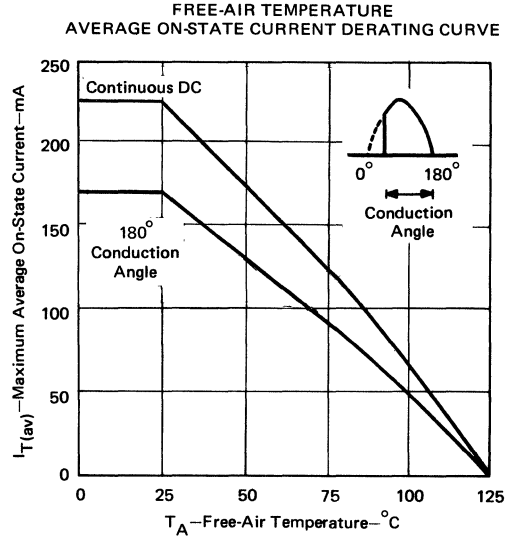


FIGURE 3

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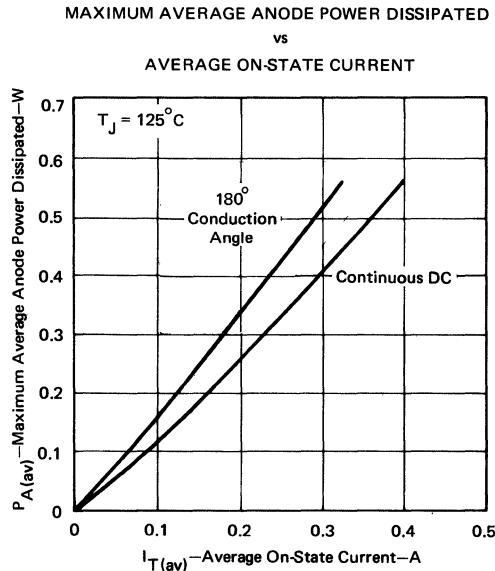
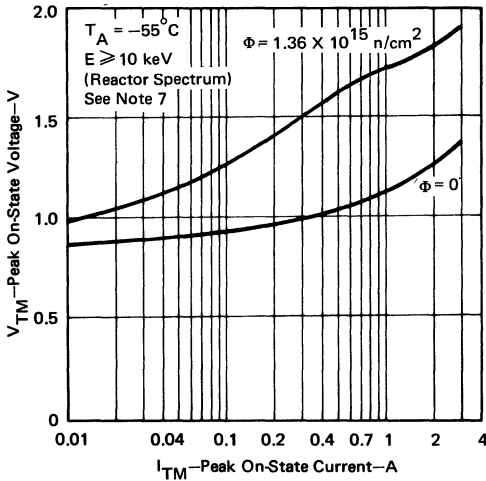


FIGURE 4

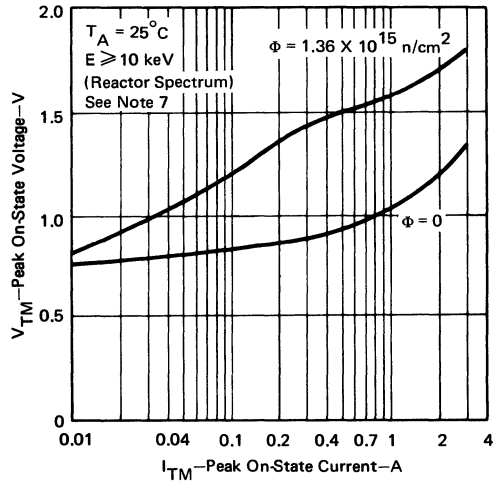
TYPES TIC35, TIC36 P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

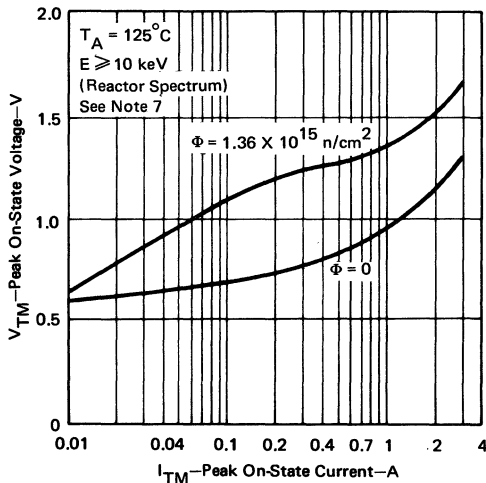
PEAK ON-STATE VOLTAGE
vs
PEAK ON-STATE CURRENT



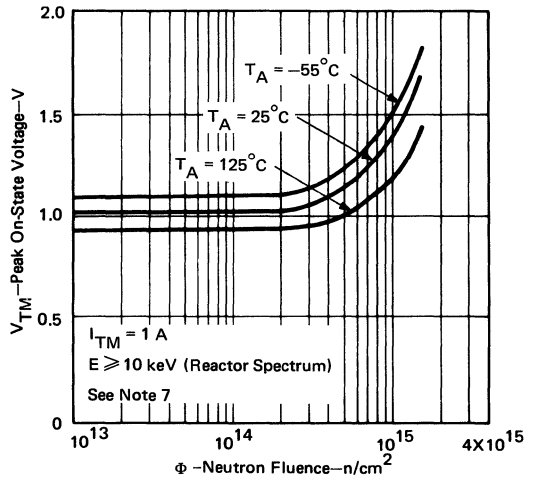
PEAK ON-STATE VOLTAGE
vs
PEAK ON-STATE CURRENT



PEAK ON-STATE VOLTAGE
vs
PEAK ON-STATE CURRENT



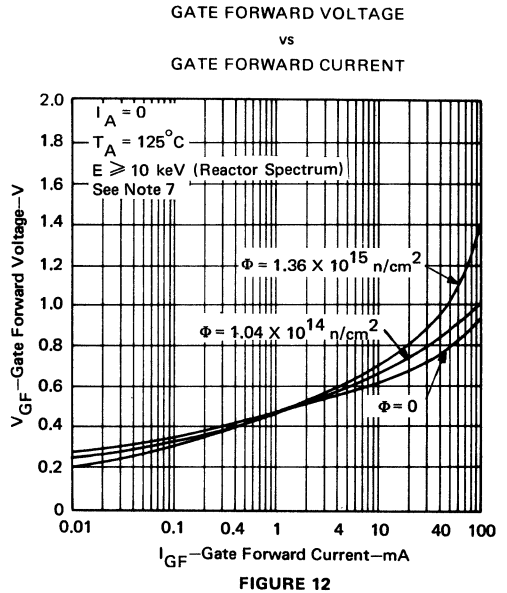
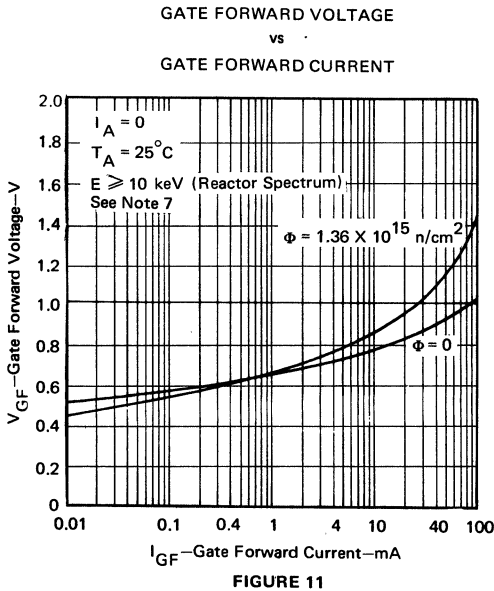
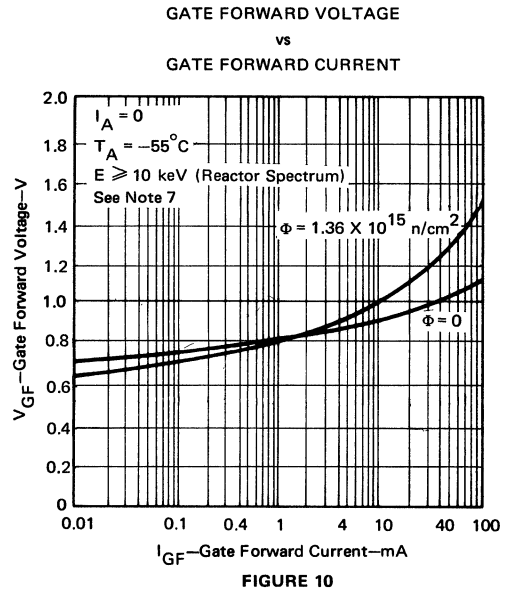
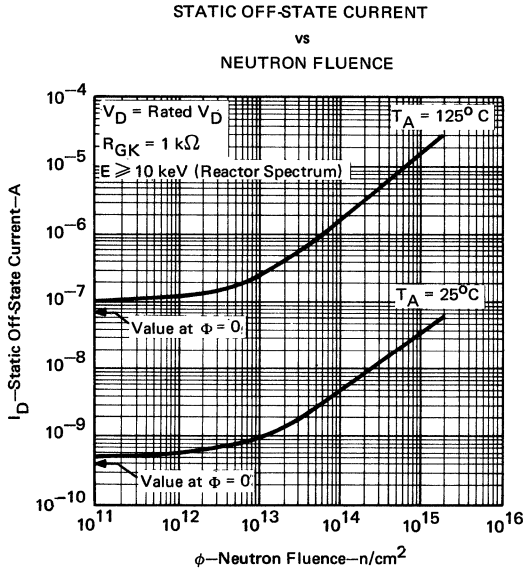
PEAK ON-STATE VOLTAGE
vs
NEUTRON FLUENCE



NOTE: 7. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are used.

TYPES TIC35, TIC36 P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS



NOTE: 7. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$. Voltage-sensing contacts separate from the current-carrying contacts, are used.

TYPES TIC35, TIC36 P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

GATE TRIGGER CURRENT
vs
NEUTRON FLUENCE

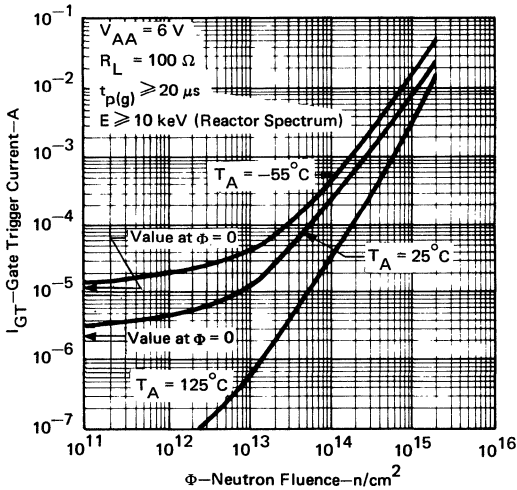


FIGURE 13

GATE TRIGGER VOLTAGE
vs
NEUTRON FLUENCE

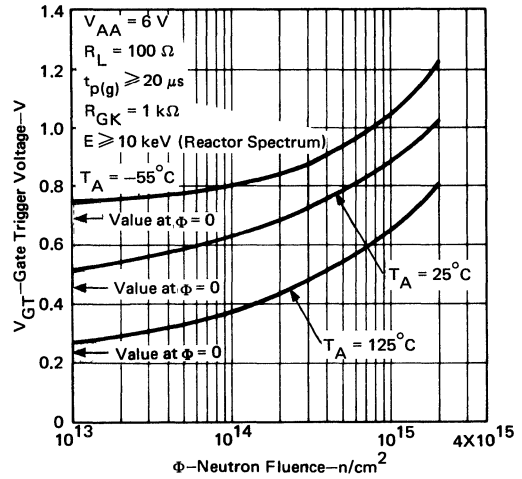


FIGURE 14

HOLDING CURRENT
vs
NEUTRON FLUENCE

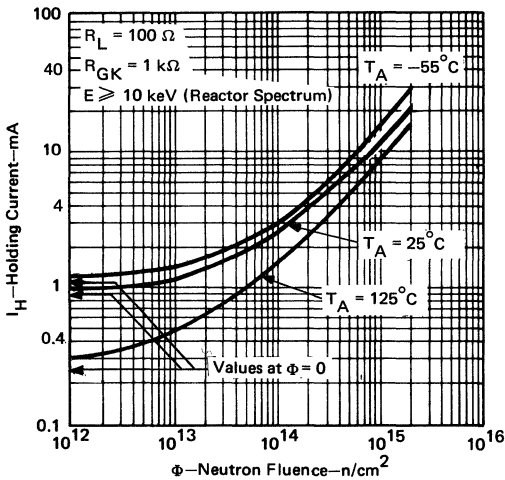


FIGURE 15

CRITICAL RATE OF RISE OF OFF-STATE VOLTAGE
vs
NEUTRON FLUENCE

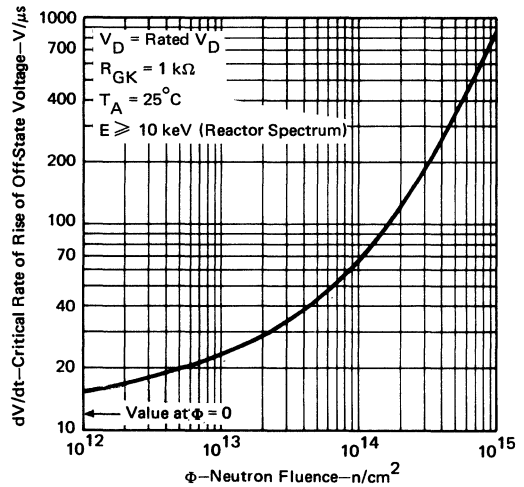
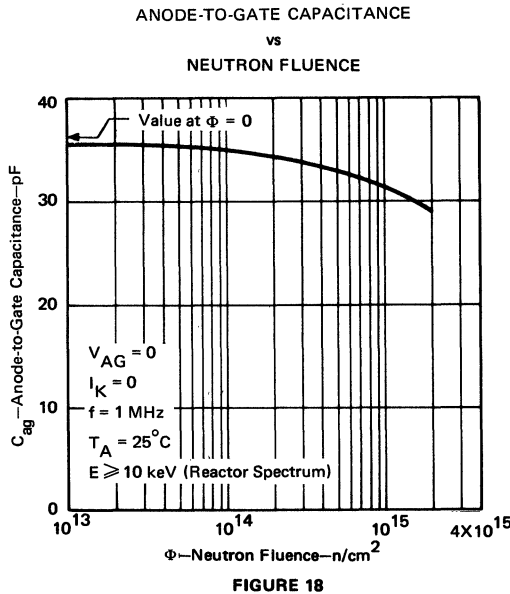
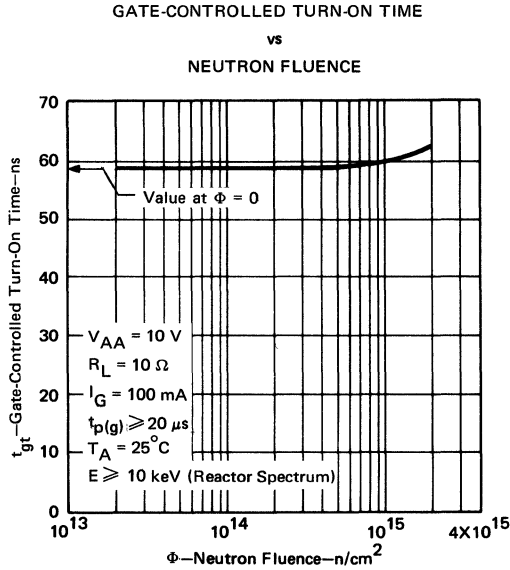


FIGURE 16

TYPES TIC35, TIC36 P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS



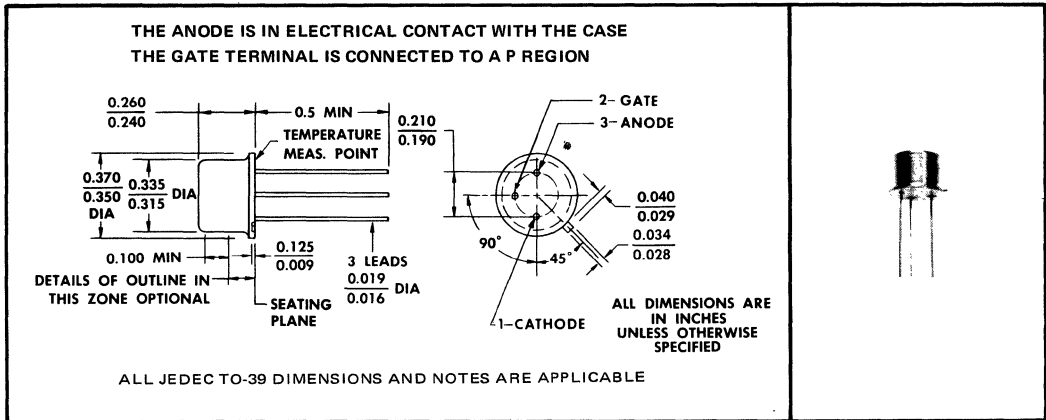
SERIES TIC39

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

SERIES TIC39
BULLETIN NO. DL-S-711631, DECEMBER 1971

- 2 A DC SCR
- 30 V to 400 V
- 20 A Surge-Current
- Max I_{GT} of 200 μ A

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

	TIC39Y	TIC39F	TIC39A	TIC39B	TIC39C	TIC39D	UNIT
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	30	50	100	200	300	400	V
Repetitive Peak Reverse Voltage, V_{RRM}	30	50	100	200	300	400	V
Continuous On-State Current at (or below) 80°C Case Temperature (See Note 2)	2						A
Average On-State Current (180° Conduction Angle) at (or below) 80°C Case Temperature (See Note 3)	1.25						A
Surge On-State Current (See Note 4)	20						A
Peak Positive Gate Current (Pulse Width \leq 300 μ s)	0.2						A
Peak Gate Power Dissipation (Pulse Width \leq 300 μ s)	1.3						W
Average Gate Power Dissipation (See Note 5)	0.3						W
Operating Case Temperature Range	-40 to 150						°C
Storage Temperature Range	-40 to 175						°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230						°C

- NOTES:
1. These values apply when the gate-cathode resistance $R_{GK} = 1 \text{ k}\Omega$.
 2. These values apply for continuous d-c operation with resistive load. Above 80°C derate linearly to 150°C case temperature at the rate of 28.6 $\text{mA}/^\circ\text{C}$.
 3. This value may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 80°C derate linearly to 150°C case temperature at the rate of 17.9 $\text{mA}/^\circ\text{C}$.
 4. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
 5. This value applies for a maximum averaging time of 16.6 ms.

SERIES TIC39

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRM}	Repetitive Peak Off-State Current	$V_D = \text{Rated } V_{DRM}$, $R_{GK} = 1 \text{ k}\Omega$, $T_C = 150^\circ\text{C}$		400		μA
I_{RRM}	Repetitive Peak Reverse Current	$V_R = \text{Rated } V_{RRM}$, $I_G = 0$, $T_C = 150^\circ\text{C}$		1		mA
I_{GT}	Gate Trigger Current	$V_{AA} = 6 \text{ V}$, $R_L = 100 \Omega$, $t_{p(g)} \geq 20 \mu\text{s}$		60	200	μA
V_{GT}	Gate Trigger Voltage	$V_{AA} = 6 \text{ V}$, $R_L = 100 \Omega$, $t_{p(g)} \geq 20 \mu\text{s}$	0.4	0.6	1	V
I_H	Holding Current	$V_{AA} = 6 \text{ V}$, $R_{GK} = 1 \text{ k}\Omega$, Initiating $I_{TM} = 50 \text{ mA}$, $T_C = -40^\circ\text{C}$		10		mA
		$V_{AA} = 6 \text{ V}$, $R_{GK} = 1 \text{ k}\Omega$, Initiating $I_{TM} = 10 \text{ mA}$		5		
V_{TM}	Peak On-State Voltage	$I_{TM} = 3.9 \text{ A}$, $R_{GK} \geq 1 \text{ k}\Omega$, See Note 6		2.5		V
V_T	Static On-State Voltage	$I_T = 2 \text{ A}$, $R_{GK} \geq 1 \text{ k}\Omega$, See Note 6		1.75		V
dv/dt	Critical Rate of Rise of Off-State Voltage	$V_D = \text{Rated } V_{DRM}$, $R_{GK} = 1 \text{ k}\Omega$, $T_C = 150^\circ\text{C}$		5		V/ μs

NOTE 6: These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	20	$^\circ\text{C/W}$

7

TYPES TIC44, TIC45, TIC46, TIC47 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

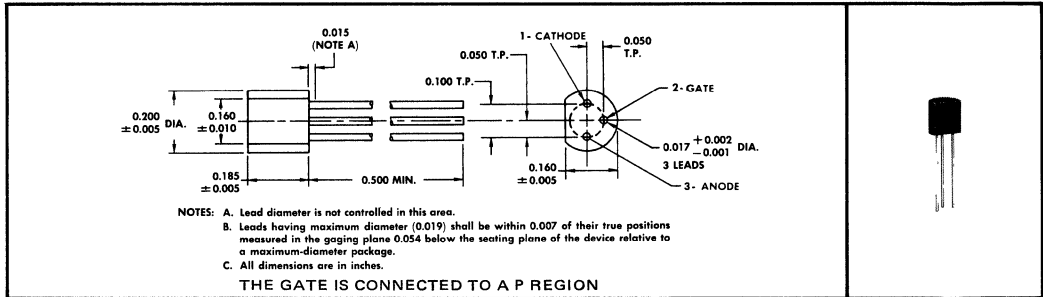
SILECT[†] THYRISTORS[‡]
600 mA DC • 30 thru 200 VOLTS

Rugged, One-Piece Construction with Standard TO-18 100-mil Pin-Circle Configuration

TYPES TIC44, TIC45, TIC46, TIC47
 BULLETIN NO. DL-S-711689, DECEMBER 1971
 REPLACES BULLETIN NO. DL-S-669051, SEPTEMBER 1966

mechanical data

These thyristors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high-humidity conditions and are capable of meeting MIL-STD-202C method 106B. The thyristors are insensitive to light.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TIC44	TIC45	TIC46	TIC47	UNIT
Static Off-State Voltage, V_D (See Note 1)	30	60	100	200	V
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	30	60	100	200	V
Static Reverse Voltage, V_R (See Note 1)	30	60	100	200	V
Repetitive Peak Reverse Voltage, V_{RRM} (See Note 1)	30	60	100	200	V
Continuous or RMS On-State Current at (or below) 55°C Case Temperature (See Note 2)	600				mA
Continuous or RMS On-State Current at (or below) 25°C Free-Air Temperature (See Note 3)	300				mA
Average On-State Current (180° Conduction Angle) at (or below) 55°C Case Temperature (See Note 4)	430				mA
Surge On-State Current (See Note 5)	6				A
Peak Negative Gate Voltage	8				V
Peak Positive Gate Current (Pulse Width ≤ 300 μs)	1				A
Peak Gate Power Dissipation (Pulse Width ≤ 300 μs)	4				W
Operating Free-Air Temperature Range	-55 to 125				°C
Storage Temperature Range	-55 to 150				°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	260				°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} \leq 1 \text{ k}\Omega$.
 2. These values apply for continuous d-c operation with resistive load. Above 55°C derate according to Figure 5.
 3. These values apply for continuous d-c operation with resistive load. Above 25°C derate according to Figure 6.
 4. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C derate according to Figure 5.
 5. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

[†]Trademark of Texas Instruments

[‡]U. S. Patent No. 3,439,238

7

TYPES TIC44, TIC45, TIC46, TIC47

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_D	Static Off-State Current	$V_D = \text{Rated } V_D, R_{GK} = 1 \text{ k}\Omega, T_A = 125^\circ\text{C}$	50		μA
I_R	Static Reverse Current	$V_R = \text{Rated } V_R, R_{GK} = 1 \text{ k}\Omega, T_A = 125^\circ\text{C}$	50		μA
I_{GT}	Gate Trigger Current (See Note 6)	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$	200		μA
V_{GT}	Gate Trigger Voltage (See Note 6)	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$	0.8		V
		$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}, T_A = 125^\circ\text{C}$	0.2		
I_H	Holding Current	$R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega$	5		mA
V_T	On-State Voltage	$I_T = 300 \text{ mA}, R_{GK} \geq 1 \text{ k}\Omega, \text{ See Note 7}$	1.4		V

NOTES: 6. When measuring these parameters, a 1-k Ω resistor should be used between gate and cathode to prevent triggering by random noise.

7. This parameter is measured using pulse techniques. $t_w = 1 \text{ ms}$, duty cycle $\leq 1\%$.

switching characteristics at 25°C free-air temperature

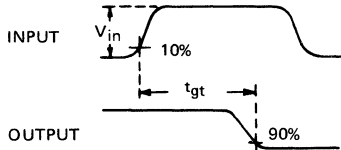
PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{gt}	Gate-Controlled Turn-On Time	$V_{AA} = 30 \text{ V}, R_L = 50 \Omega, R_G = 20 \text{ k}\Omega, V_{in} = 20 \text{ V}, \text{ See Figure 1}$	3.5	μs
t_q	Circuit-Commutated Turn-Off Time	$V_{AA} = 30 \text{ V}, R_L = 50 \Omega, I_{RM} = 1 \text{ A}, \text{ See Figure 2}$	6.8	μs

thermal characteristics

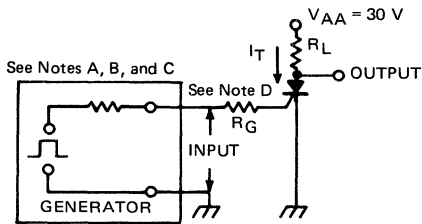
PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	75	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	275	

TYPES TIC44, TIC45, TIC46, TIC47 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

PARAMETER MEASUREMENT INFORMATION



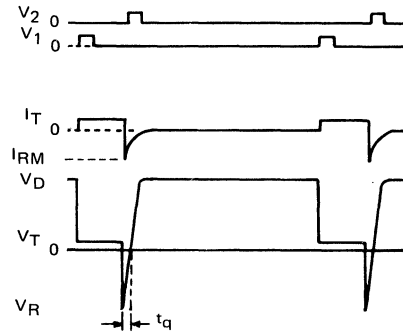
VOLTAGE WAVEFORMS



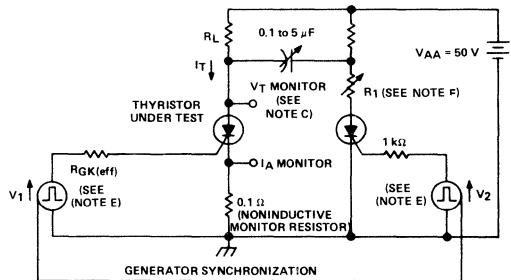
TEST CIRCUIT

FIGURE 1—TURN-ON TIME

- NOTES: A. V_{in} is measured with gate and cathode terminals connected as shown and anode terminal open.
- B. The input waveform of Figure 1 has the following characteristics: $t_r \leq 40$ ns, $t_w \geq 20$ μ s.
- C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 12$ pF.
- D. R_G includes the total resistance of the generator and the external resistor.



WAVEFORMS



TEST CIRCUIT

FIGURE 2—COMMUTATING TURN-OFF TIME

- NOTES: E. Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50$ to 300 μ s, duty cycle = 1%. The pulse widths of V_1 and V_2 are ≥ 10 μ s.
- F. Resistor R_1 is adjusted for $I_{RM} = 1$ A.

TYPES TIC44, TIC45, TIC46, TIC47 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

THERMAL INFORMATION

The minimum heat-sink requirements may be calculated for any on-state current, heat-sink combination by the following procedure:

1. Determine worst-case power dissipation from Figure 3.
2. Calculate maximum allowable case-to-free-air thermal resistance by use of the equation.

$$R_{\theta CA} = \frac{T_J - T_A}{P_{A(av)}} - R_{\theta JC}$$

where: T_J = Junction temperature

T_A = Free-air temperature

$P_{A(av)}$ = Average anode power dissipation (see Figure 3 for worst-case values)

$R_{\theta JC}$ = Junction-to-case thermal resistance = 75°C/W maximum.

3. Determine area of heat sink from Figure 4.

EXAMPLE

Determine: Minimum size of 1/16"-thick aluminum heat sink for safe operation of thyristor at an average current of 0.4 A with a conduction angle of 180°

Given: Maximum $T_J = 125^\circ\text{C}$

$T_A = 35^\circ\text{C}$

$R_{\theta JC} = 75^\circ\text{C}$

Solution: From Figure 3, $P_{A(av)} = 0.84\text{ W}$ for 0.4 A with 180° conduction angle. Using the equation of step 2 above:

$$R_{\theta CA} = \frac{125^\circ\text{C} - 35^\circ\text{C}}{0.84\text{ W}} - 75^\circ\text{C/W} = 32^\circ\text{C/W}$$

Figure 4 shows that for $R_{\theta CA}$ of 32°C/W, the area is 18 sq. in. The minimum dimensions of the sides should be:

$$\sqrt{\frac{\text{area}}{2}} \times \sqrt{\frac{\text{area}}{2}} = \sqrt{\frac{18}{2}} \times \sqrt{\frac{18}{2}} = 3'' \times 3''$$

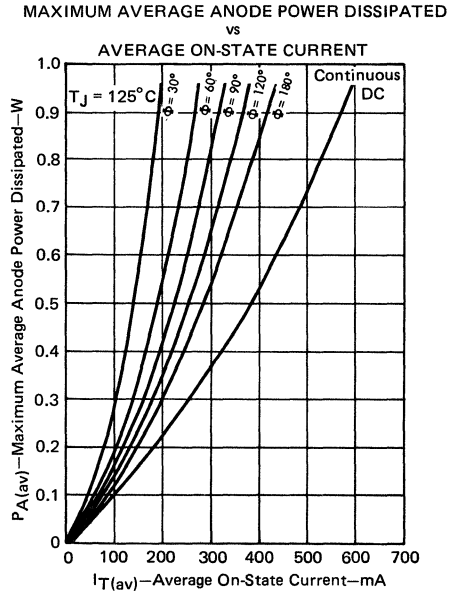


FIGURE 3

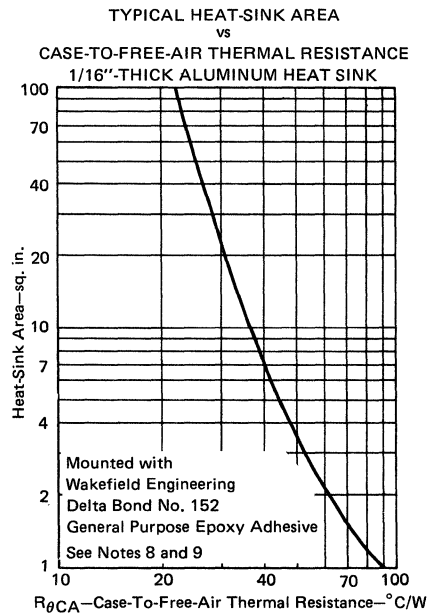


FIGURE 4

- NOTES: 8. The thyristor is mounted in the center of a square heat sink vertically positioned in still free air with both sides exposed. The heat-sink area is twice the area of one side.
9. $R_{\theta CA}$ includes the case-to-heat sink thermal resistance, $R_{\theta CHS}$, in addition to the heat-sink-to-free-air thermal resistance, $R_{\theta HSA}$ and is defined by the equation, $R_{\theta CA} = R_{\theta CHS} + R_{\theta HSA}$.

TYPES TIC44, TIC45, TIC46, TIC47 P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

THERMAL INFORMATION

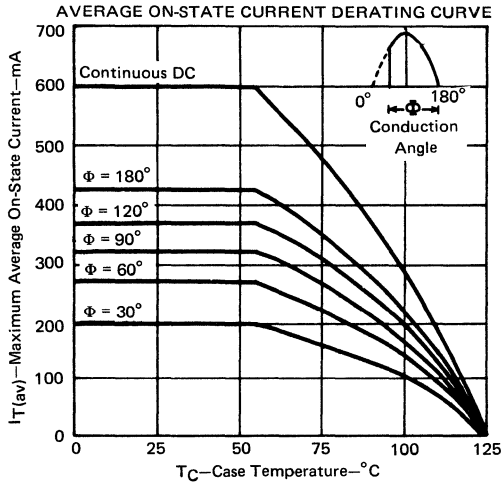


FIGURE 5

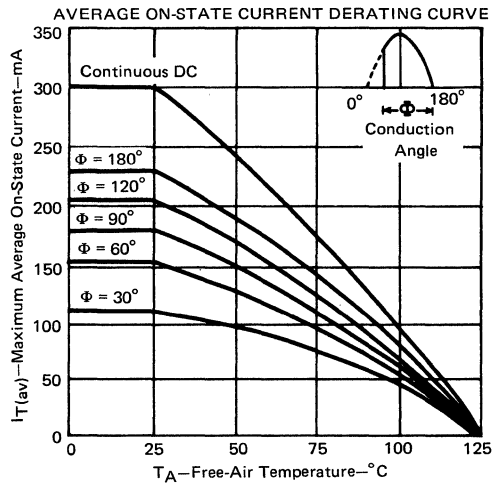


FIGURE 6

TYPICAL CHARACTERISTICS

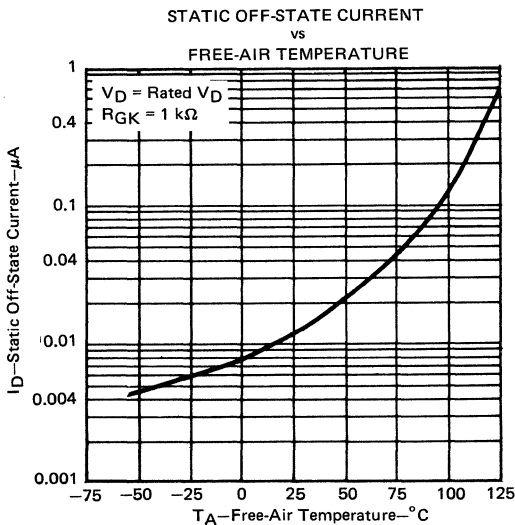


FIGURE 7

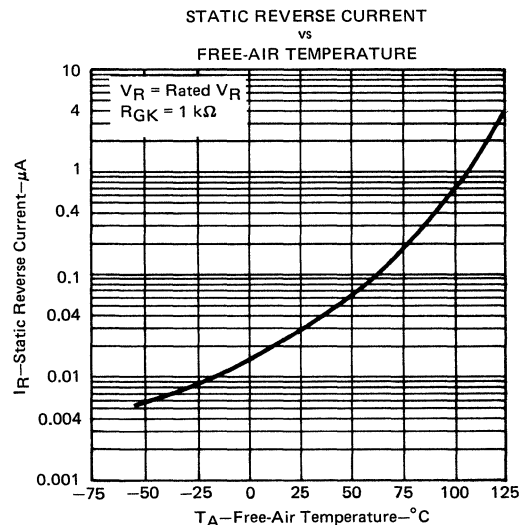


FIGURE 8

TYPES TIC44, TIC45, TIC46, TIC47

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

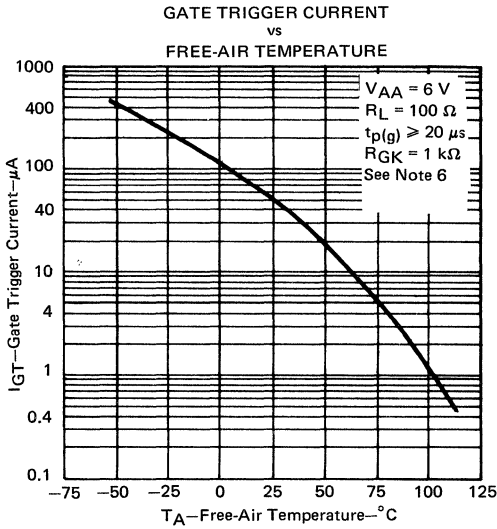


FIGURE 9

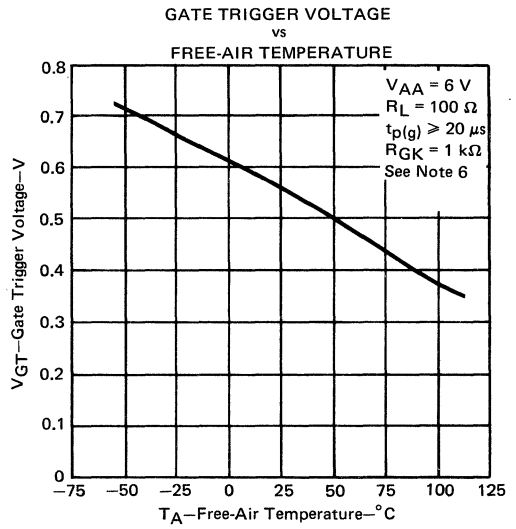


FIGURE 10

NOTE 6: When measuring these parameters, a 1-k Ω resistor should be used between gate and cathode to prevent triggering by random noise.

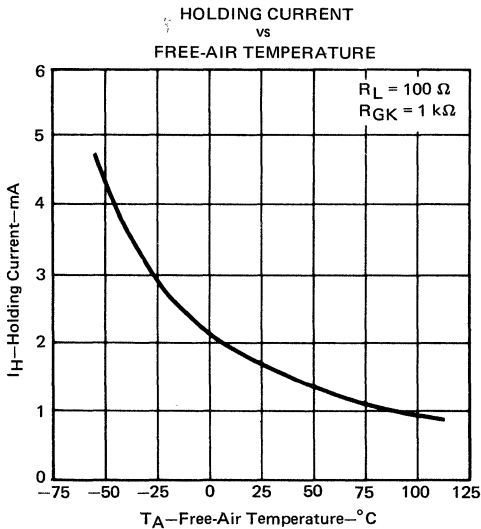


FIGURE 11

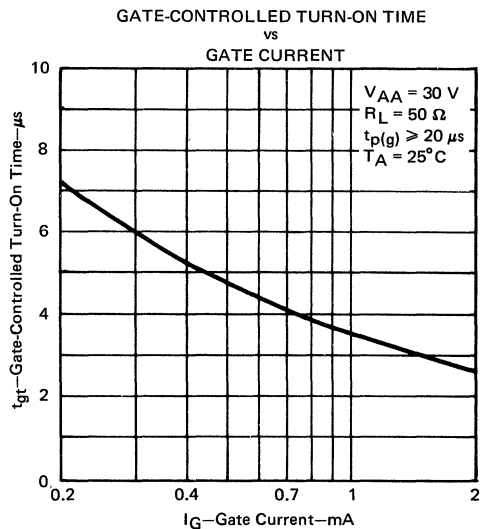


FIGURE 12

TYPES TIC67, TIC68 P-N-P-N PLANAR EPITAXIAL SILICON REVERSE-BLOCKING TRIODE THYRISTORS

 TYPES TIC67, TIC68
BULLETIN NO. DL-S-7111632, DECEMBER 1971

RADIATION-TOLERANT THYRISTORS

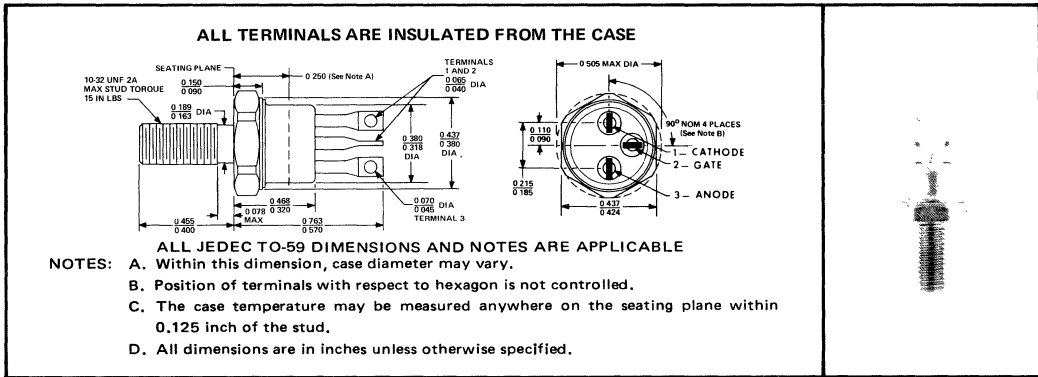
20 A DC • 60 and 80 VOLTS

- Max I_{GT} of 40 mA after 1×10^{14} Fast Neutrons/cm²
- Max V_{TM} of 1.5 V at I_{TM} of 20 A after 1×10^{14} Fast Neutrons/cm²

description

The TIC67 and TIC68 thyristors offer a significant advance in radiation-tolerant-device technology. Unique construction techniques produce thyristors which maintain useful characteristics after fast-neutron radiation fluences through 10^{14} n/cm².

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

	TIC67	TIC68	UNIT
Continuous Off-State Voltage, V_D	60	80	V
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	60	80	V
Continuous Reverse Voltage, V_R	60	80	V
Repetitive Peak Reverse Voltage, V_{RRM}	60	80	V
Nonrepetitive Peak Reverse Voltage, V_{RSM} (See Note 2)	60	80	V
Continuous On-State Current at (or below) 55°C Case Temperature (See Note 3)	20		A
Continuous On-State Current at (or below) 25°C Free-Air Temperature (See Note 3)	1.25		A
Average On-State Current (180° Conduction Angle) at (or below) 55°C Case Temperature (See Note 4)	12.5		A
Surge On-State Current (See Note 5)	75		A
Peak Positive Gate Current (Pulse Width $\leq 300 \mu s$)	3		A
Peak Gate Power Dissipation (Pulse Width $\leq 300 \mu s$)	5		W
Average Gate Power Dissipation	1		W
Operating Case Temperature Range	-55 to 125		°C
Storage Temperature Range	-65 to 200		°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	260		°C

- NOTES:
1. These values apply when the gate-cathode resistance $R_{GK} = 1 \text{ k}\Omega$.
 2. These values apply for a 5-ms rectangular pulse when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
 3. This value applies for continuous d-c operation with resistive load. Derate linearly to 125°C case temperature at the rate of 0.286 A/°C or 125°C free-air temperature at the rate of 12.5 mA/°C.
 4. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C derate linearly to 125°C case temperature at the rate of 0.179 A/°C.
 5. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

TYPES TIC67, TIC68

P-N-P-N PLANAR EPITAXIAL SILICON

REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRM} Repetitive Peak Off-State Current	$V_D = \text{Rated } V_{DRM}, R_{GK} = 1 \text{ k}\Omega, T_C = 125^\circ\text{C}$		100		μA
I_{RRM} Repetitive Peak Reverse Current	$V_R = \text{Rated } V_{RRM}, R_{GK} = 1 \text{ k}\Omega, T_C = 125^\circ\text{C}$		500		μA
I_{GT} Gate Trigger Current	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$		20		mA
V_{GT} Gate Trigger Voltage	$V_{AA} = \text{Rated } V_{DRM}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$		1		V
I_H Holding Current	$V_{AA} = 6 \text{ V}, R_{GK} = 1 \text{ k}\Omega, \text{Initiating } I_{TM} = 100 \text{ mA}$		20		mA
V_T Static On-State Voltage	$I_T = 20 \text{ A}, R_{GK} \geq 1 \text{ k}\Omega, \text{See Note 6}$		1.5		V
V_{TM} Peak On-State Voltage	$I_{TM} = 39 \text{ A}, R_{GK} \geq 1 \text{ k}\Omega, \text{See Note 6}$		3		V
dv/dt Critical Rate of Rise of Off-State Voltage	$V_D = \text{Rated } V_{DRM}, I_G = 0$	100			$\text{V}/\mu\text{s}$

post-irradiation electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	RADIATION FLUENCE [†]	MAX	UNIT
I_{GT} Gate Trigger Current	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \text{ ns}$	$1 \times 10^{14} \text{ n/cm}^2$	40	mA
V_T Static On-State Voltage	$I_T = 20 \text{ A}, \text{See Note 6}$	$1 \times 10^{14} \text{ n/cm}^2$	1.5	V

[†]Radiation is fast neutrons (n) at $E \geq 10 \text{ keV}$ (reactor spectrum).

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	2.33	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	87.5	$^\circ\text{C/W}$

NOTE 6: These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

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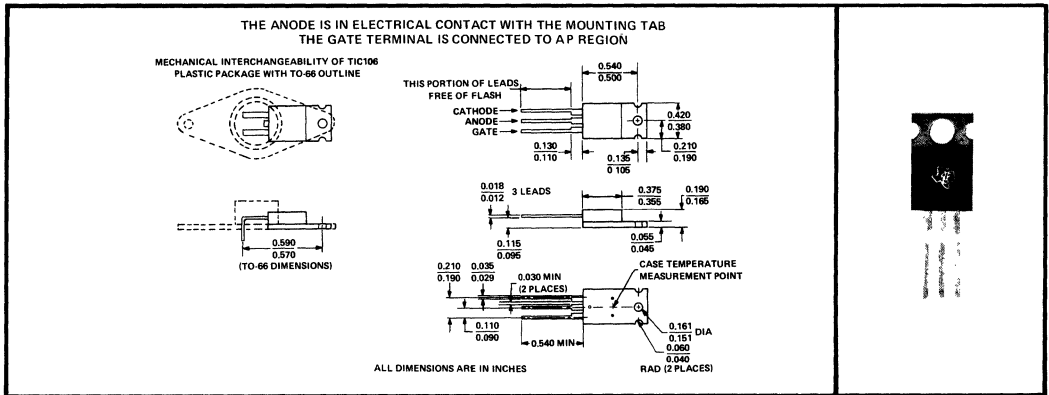
SERIES TIC106

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

SERIES TIC106
BULLETIN NO. DL-S-7111489, APRIL 1971

- 5 A DC
- 30 V to 400 V
- 30 A Surge-Current
- Max I_{GT} of 200 μ A

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

	TIC106Y	TIC106F	TIC106A	TIC106B	TIC106C	TIC106D	UNIT
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	30	50	100	200	300	400	V
Repetitive Peak Reverse Voltage, V_{RRM}	30	50	100	200	300	400	V
Continuous On-State Current at (or below) 80°C Case Temperature (See Note 2)	5						A
Average On-State Current (180° Conduction Angle) at (or below) 80°C Case Temperature (See Note 3)	3.2						A
Surge On-State Current (See Note 4)	30						A
Peak Positive Gate Current (Pulse Width \leq 300 μ s)	0.2						A
Peak Gate Power Dissipation (Pulse Width \leq 300 μ s)	1.3						W
Average Gate Power Dissipation (See Note 5)	0.3						W
Operating Case Temperature Range	-40 to 110						°C
Storage Temperature Range	-40 to 125						°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230						°C

- NOTES:
1. These values apply when the gate-cathode resistance $R_{GK} = 1 \text{ k}\Omega$.
 2. These values apply for continuous d-c operation with resistive load. Above 80°C derate according to Figure 3.
 3. This value may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 80°C derate according to Figure 3.
 4. This value applies for one 60-Hz half-sine-wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
 5. This value applies for a maximum averaging time of 16.6 ms.

SERIES TIC106

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25° C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRM} Repetitive Peak Off-State Current	$V_D = \text{Rated } V_{DRM}, R_{GK} = 1 \text{ k}\Omega, T_C = 110^\circ\text{C}$		400		μA
I_{RRM} Repetitive Peak Reverse Current	$V_R = \text{Rated } V_{RRM}, I_G = 0, T_C = 110^\circ\text{C}$		1		mA
I_{GT} Gate Trigger Current	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$	60	200		μA
V_{GT} Gate Trigger Voltage	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 20 \mu\text{s}, T_C = -40^\circ\text{C}$		1.2		V
	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 20 \mu\text{s}$	0.4	0.6	1	
	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 20 \mu\text{s}, T_C = 110^\circ\text{C}$	0.2			
I_H Holding Current	$V_{AA} = 6 \text{ V}, R_{GK} = 1 \text{ k}\Omega, \text{Initiating } I_T = 10 \text{ mA}, T_C = -40^\circ\text{C}$		8		mA
	$V_{AA} = 6 \text{ V}, R_{GK} = 1 \text{ k}\Omega, \text{Initiating } I_T = 10 \text{ mA}$		5		
V_{TM} Peak On-State Voltage	$I_{TM} = 5 \text{ A}, \text{See Note 6}$		1.7		V
dv/dt Critical Rate of Rise of Off-State Voltage	$V_D = \text{Rated } V_D, R_{GK} = 1 \text{ k}\Omega, T_C = 110^\circ\text{C}$	10			V/ μs

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	$^\circ\text{C/W}$

NOTE 6: This parameter must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

SERIES TIC106

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{gt} Gate-Controlled Turn-On-Time	$V_{AA} = 30\text{ V}$, $R_L = 6\ \Omega$, $R_{GK}(\text{eff}) = 5\ \text{k}\Omega$, $V_{in} = 50\text{ V}$, See Figure 1	1.75	μs
t_q Circuit-Commutated Turn-Off Time	$V_{AA} = 30\text{ V}$, $R_L = 6\ \Omega$, $I_{RM} \approx 8\text{ A}$, See Figure 2	7.7	μs

PARAMETER MEASUREMENT INFORMATION

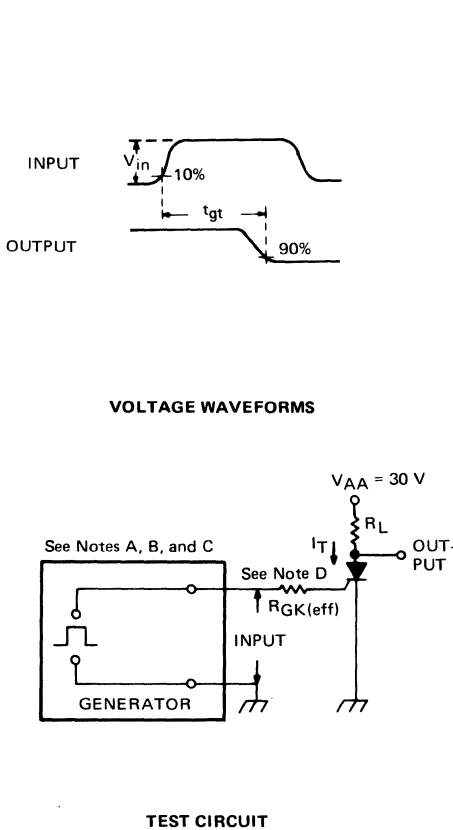


FIGURE 1 – GATE-CONTROLLED TURN-ON TIME

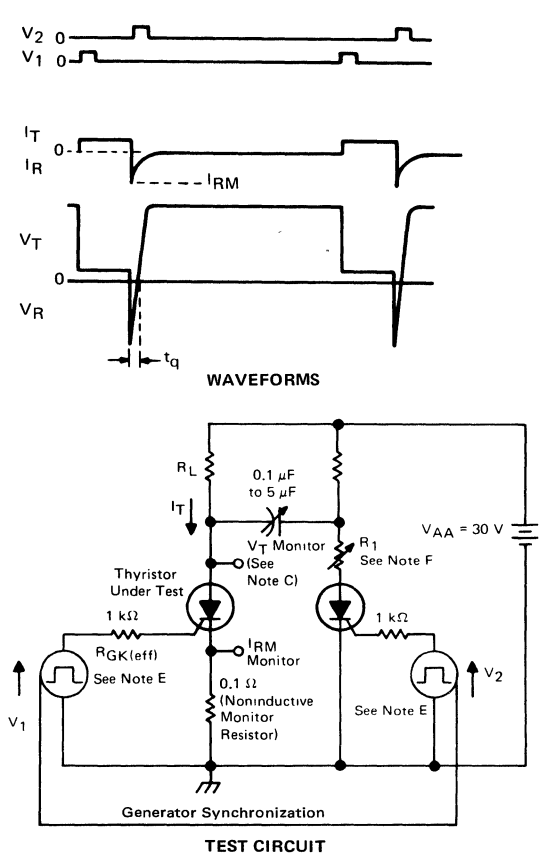


FIGURE 2 – CIRCUIT-COMMUTATED TURN-OFF TIME

- NOTES:
- A. V_{in} is measured with gate and cathode terminals open.
 - B. The input waveform of Figure 1 has the following characteristics: $t_r \leq 40\text{ ns}$, $t_w \geq 20\ \mu\text{s}$.
 - C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14\text{ ns}$, $R_{in} \geq 10\ \text{M}\Omega$, $C_{in} \leq 12\ \text{pF}$.
 - D. $R_{GK}(\text{eff})$ includes the total resistance of the generator and the external resistor.
 - E. Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50\text{ to }300\ \mu\text{s}$, duty cycle = 1%. The pulse widths of V_1 and V_2 are $\geq 10\ \mu\text{s}$.
 - F. Resistor R_1 is adjusted for $I_{RM} \approx 8\text{ A}$.

7

SERIES TIC106

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

THERMAL INFORMATION

AVERAGE ANODE FORWARD CURRENT DERATING CURVE

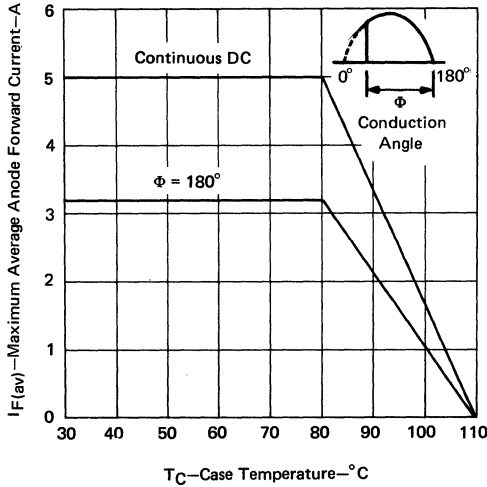


FIGURE 3

MAXIMUM CONTINUOUS ANODE POWER DISSIPATED vs CONTINUOUS ANODE FORWARD CURRENT

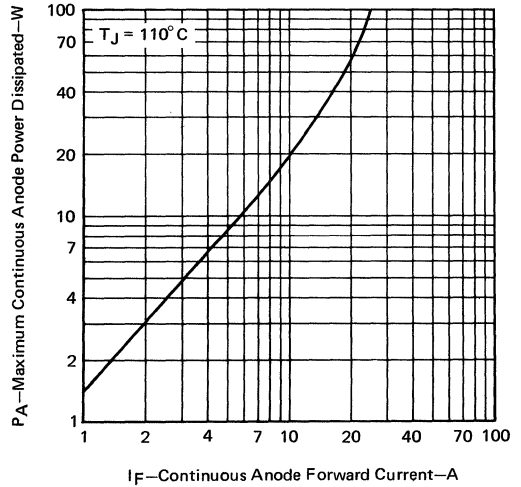


FIGURE 4

SURGE ON-STATE CURRENT vs CYCLES OF CURRENT DURATION

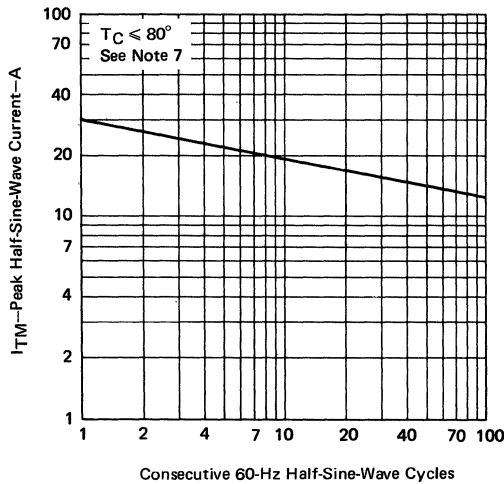


FIGURE 5

TRANSIENT THERMAL RESISTANCE vs CYCLES OF CURRENT DURATION

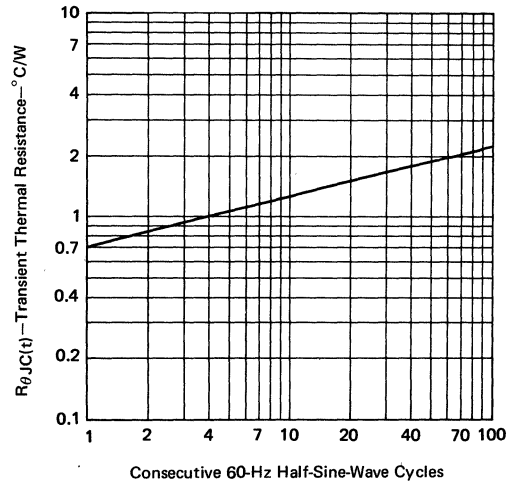


FIGURE 6

NOTE 7: This curve shows the maximum number of cycles of surge current for which gate control is guaranteed provided the device is initially at nonoperating thermal equilibrium.

SERIES TIC106 P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

GATE TRIGGER CURRENT
vs
CASE TEMPERATURE

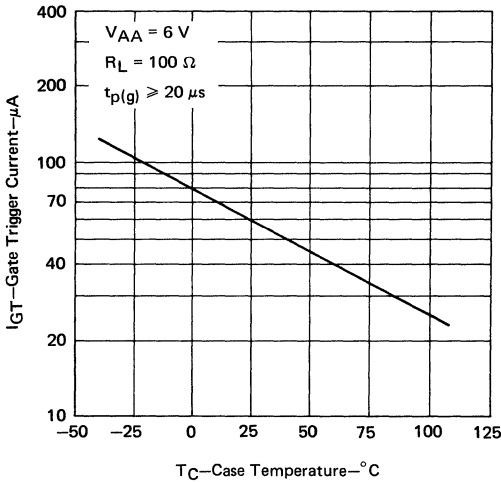


FIGURE 7

GATE TRIGGER VOLTAGE
vs
CASE TEMPERATURE

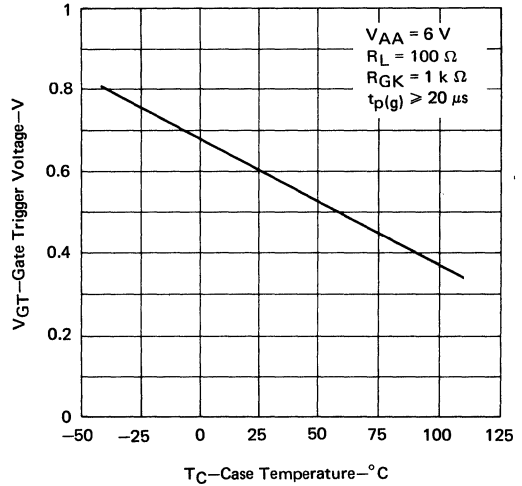


FIGURE 8

GATE FORWARD VOLTAGE
vs
GATE FORWARD CURRENT

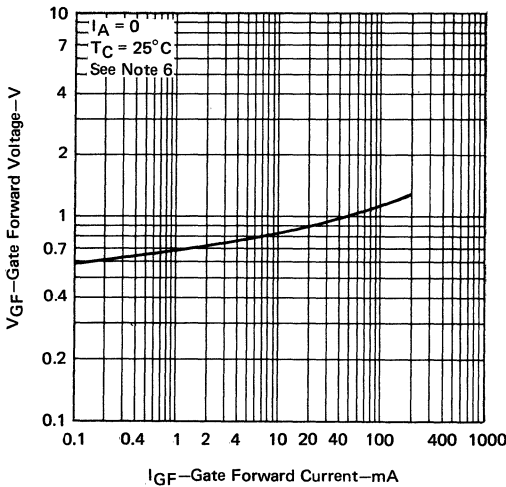


FIGURE 9

HOLDING CURRENT
vs
CASE TEMPERATURE

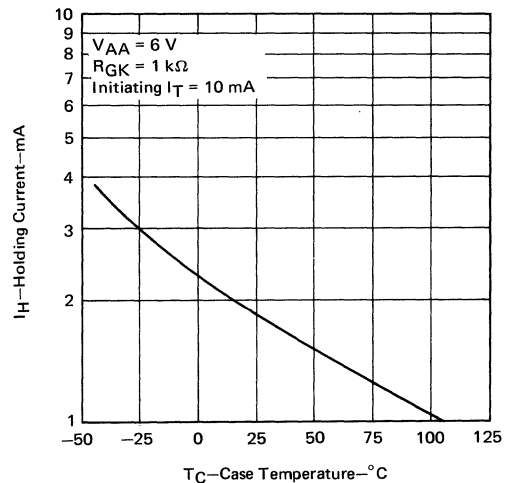


FIGURE 10

NOTE 6: This parameter must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

7

SERIES TIC106

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

PEAK ON-STATE VOLTAGE
vs
PEAK ON-STATE CURRENT

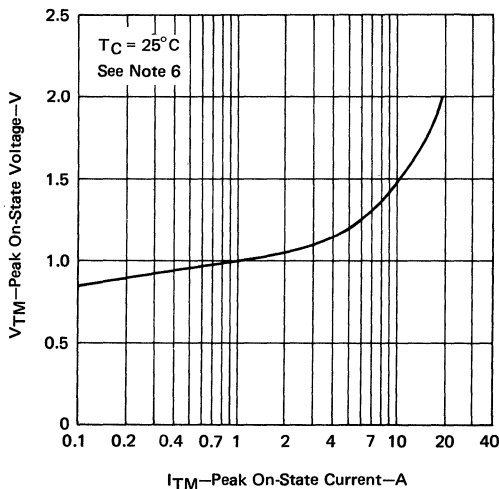


FIGURE 11

GATE-CONTROLLED TURN-ON TIME
vs
GATE CURRENT

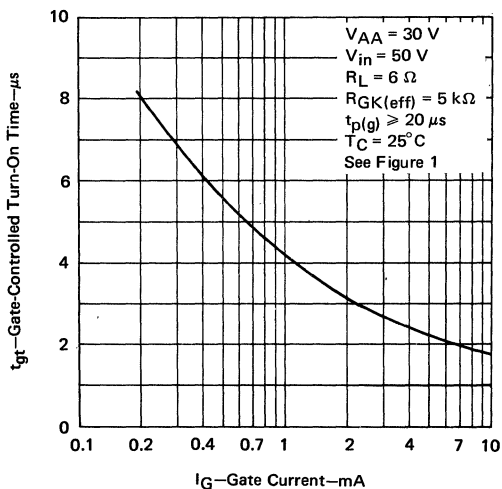


FIGURE 12

CIRCUIT-COMMUTATED TURN-OFF TIME
vs
CASE TEMPERATURE

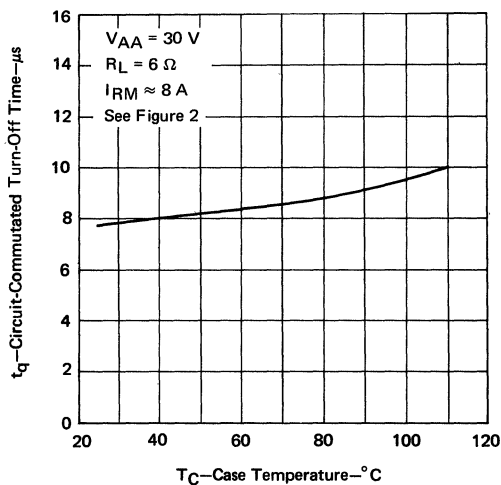


FIGURE 13

NOTE 6: This parameter must be measured using pulse techniques. $t_w = 300\ \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

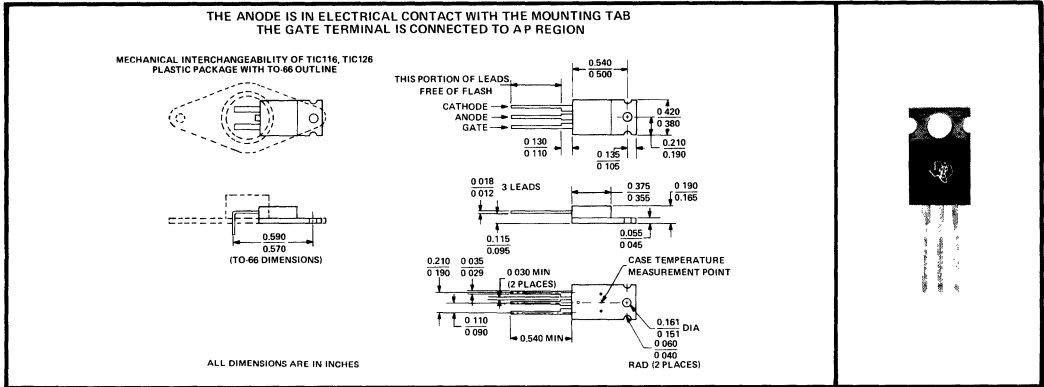
SERIES TIC116, TIC126

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

SERIES TIC116, TIC126
BULLETIN NO. DL-S-7111467, APRIL, 1971

- 8 A and 12 A DC
- 80 A and 100 A Surge Current
- 50 V to 600 V
- MAX I_{GT} of 20 mA

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

	SERIES	SERIES	UNIT
	TIC116	TIC126	
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	F Suffix	50	V
	A Suffix	100	
	B Suffix	200	
	C Suffix	300	
	D Suffix	400	
	E Suffix	500	
Repetitive Peak Reverse Voltage, V_{RRM}	F Suffix	50	V
	A Suffix	100	
	B Suffix	200	
	C Suffix	300	
	D Suffix	400	
	E Suffix	500	
Continuous On-State Current at (or below) 70°C Case Temperature (See Note 2)	8	12	A
Average On-State Current (180° Conduction Angle) at (or below) 70°C Case Temperature (See Note 3)	5	7.5	A
Surge On-State Current (See Note 4)	80	100	A
Peak Positive Gate Current (Pulse Width \leq 300 μ s)	3		A
Peak Gate Power Dissipation (Pulse Width \leq 300 μ s)	5		W
Average Gate Power Dissipation (See Note 5)	1		W
Operating Case Temperature Range	-40 to 110		°C
Storage Temperature Range	-40 to 125		°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230		°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} = 1 \text{ k}\Omega$.
2. These values apply for continuous d-c operation with resistive load. Above 70°C derate according to Figure 3.
3. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 70°C derate according to Figure 3.
4. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
5. This value applies for a maximum averaging time of 16.6 ms.

7

SERIES TIC116, TIC126

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SERIES	MIN	TYP	MAX	UNIT
I_{DRM} Repetitive Peak Off-State Current	$V_D = \text{Rated } V_{DRM}, R_{GK} = 1 \text{ k}\Omega, T_C = 110^\circ\text{C}$	All			2	mA
I_{RRM} Repetitive Peak Reverse Current	$V_R = \text{Rated } V_{RRM}, I_G = 0, T_C = 110^\circ\text{C}$	All			2	mA
I_{GT} Gate Trigger Current	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, t_{p(g)} \geq 20 \mu\text{s}$	All		5	20	mA
V_{GT} Gate Trigger Voltage	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 20 \mu\text{s}, T_C = -40^\circ\text{C}$	All			2.5	V
	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 20 \mu\text{s}$	All		0.8	1.5	
	$V_{AA} = 6 \text{ V}, R_L = 100 \Omega, R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 20 \mu\text{s}, T_C = 110^\circ\text{C}$	All		0.2		
I_H Holding Current	$V_{AA} = 6 \text{ V}, R_{GK} = 1 \text{ k}\Omega, \text{ Initiating } I_T = 100 \text{ mA}, T_C = -40^\circ\text{C}$	All			70	mA
	$V_{AA} = 6 \text{ V}, R_{GK} = 1 \text{ k}\Omega, \text{ Initiating } I_T = 100 \text{ mA}$	All			40	
V_{TM} Peak On-State Voltage	$I_{TM} = 8 \text{ A}, \text{ See Note 6}$	TIC116			1.7	V
	$I_{TM} = 12 \text{ A}, \text{ See Note 6}$	TIC126			1.4	
dv/dt Critical Rate of Rise of Off-State Voltage	$V_D = \text{Rated } V_D, I_G = 0, T_C = 110^\circ\text{C}$	All		100		V/ μs

7

thermal characteristics

PARAMETER	SERIES	SERIES	UNIT
	TIC116	TIC126	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	3	2.4	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	62.5	62.5	

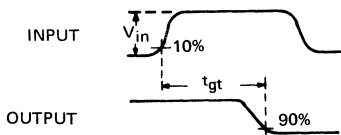
NOTE 6: This parameter must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

SERIES TIC116, TIC126 P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

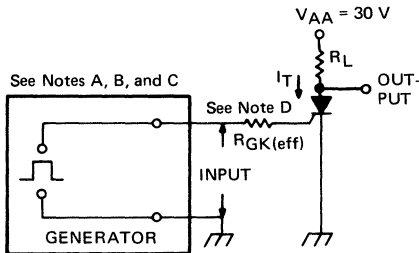
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{gt} Gate-Controlled Turn-On Time	$V_{AA} = 30\text{ V}$, $R_L = 6\ \Omega$, $R_{GK(\text{eff})} = 100\ \Omega$, $V_{in} = 20\text{ V}$, See Figure 1	0.8	μs
t_q Circuit-Commutated Turn-Off Time	$V_{AA} = 30\text{ V}$, $R_L = 6\ \Omega$, $I_{RM} = 10\text{ A}$, See Figure 2	11	μs

PARAMETER MEASUREMENT INFORMATION

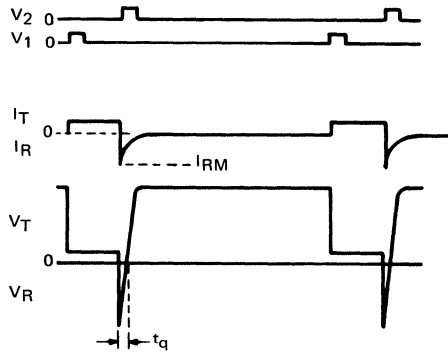


VOLTAGE WAVEFORMS

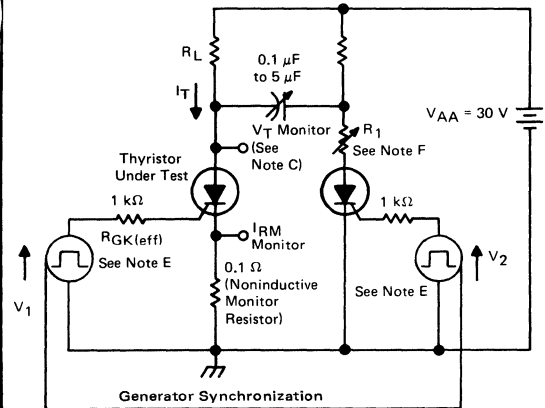


TEST CIRCUIT

FIGURE 1 – GATE-CONTROLLED TURN-ON TIME



WAVEFORMS



TEST CIRCUIT

FIGURE 2 – CIRCUIT-COMMUTATED TURN-OFF TIME

- NOTES:
- V_{in} is measured with gate and cathode terminals open.
 - The input waveform of Figure 1 has the following characteristics: $t_r \leq 40\text{ ns}$, $t_w \geq 20\ \mu\text{s}$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 12\text{ pF}$.
 - $R_{GK(\text{eff})}$ includes the total resistance of the generator and the external resistor.
 - Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50\text{ to }300\ \mu\text{s}$, duty cycle = 1%. The pulse widths of V_1 and V_2 are $\geq 10\ \mu\text{s}$.
 - Resistor R_1 is adjusted for $I_{RM} \approx 10\text{ A}$.

7

SERIES TIC116, TIC126

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

THERMAL INFORMATION

AVERAGE ON-STATE CURRENT DERATING CURVE

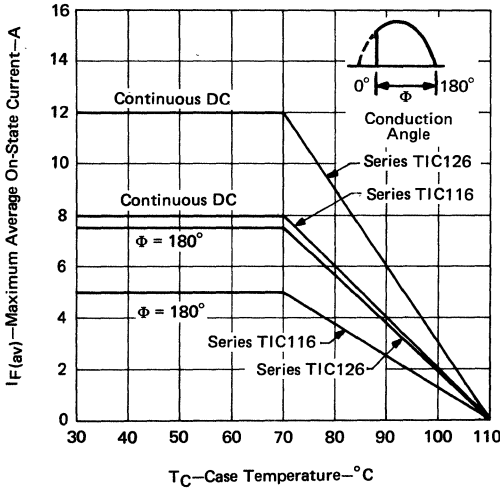


FIGURE 3

MAXIMUM CONTINUOUS ANODE POWER DISSIPATED
vs
CONTINUOUS ON-STATE CURRENT

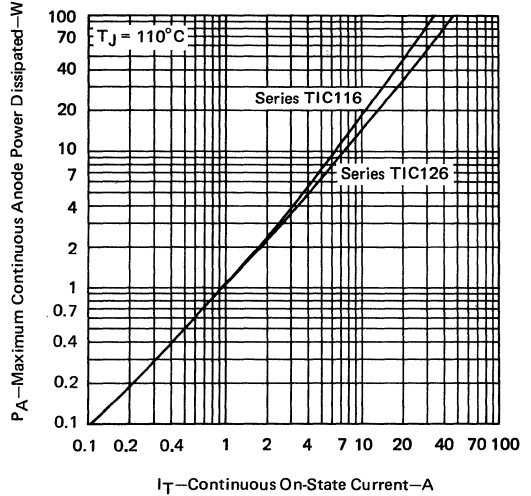


FIGURE 4

SURGE ON-STATE CURRENT
vs
CYCLES OF CURRENT DURATION

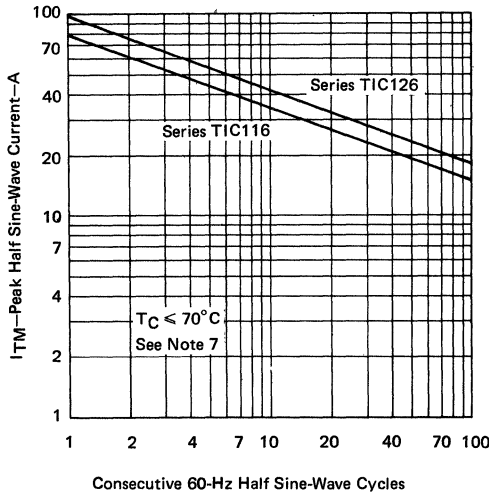


FIGURE 5

TRANSIENT THERMAL RESISTANCE
vs
CYCLES OF CURRENT DURATION

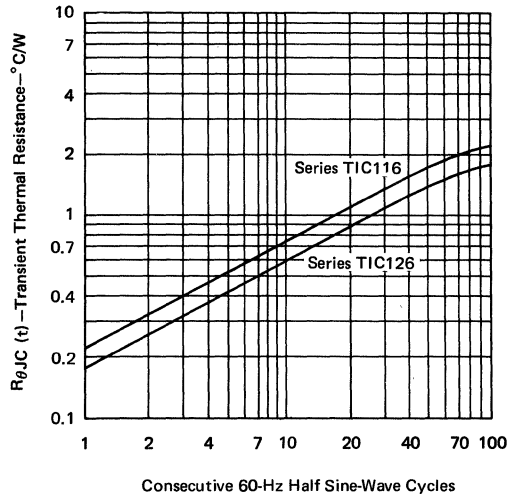


FIGURE 6

NOTE 7: This curve shows the maximum number of cycles of surge current for which gate control is guaranteed provided the device is initially at nonoperating thermal equilibrium.

SERIES TIC116, TIC126 P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

GATE TRIGGER CURRENT
vs
CASE TEMPERATURE

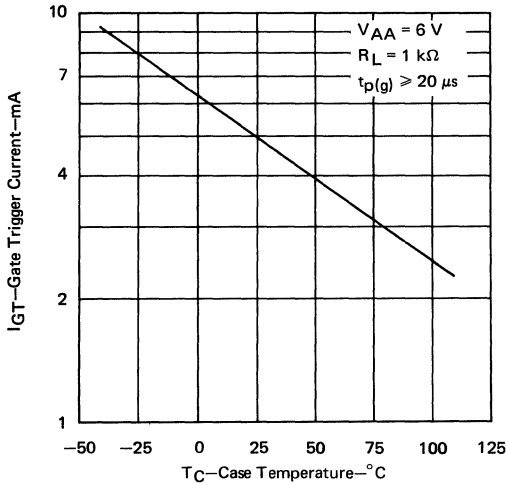


FIGURE 7

GATE TRIGGER VOLTAGE
vs
CASE TEMPERATURE

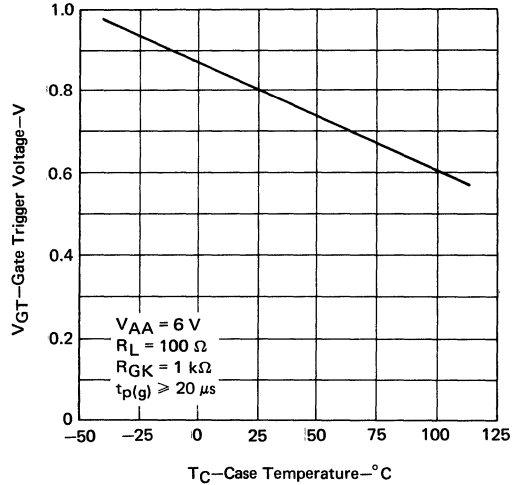


FIGURE 8

GATE FORWARD VOLTAGE
vs
GATE FORWARD CURRENT

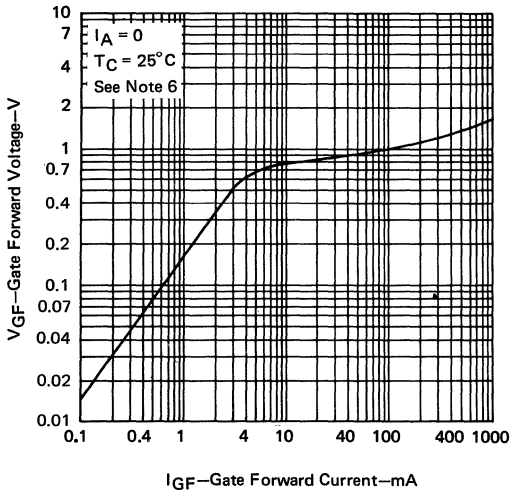


FIGURE 9

HOLDING CURRENT
vs
CASE TEMPERATURE

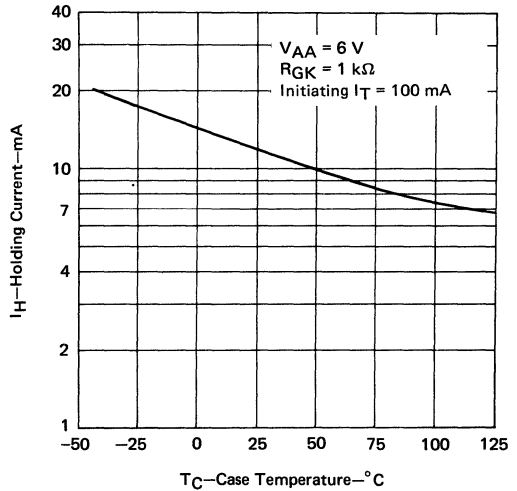


FIGURE 10

NOTE 6: This parameter must be measured using pulse techniques, $t_w = 300 \mu s$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

7

SERIES TIC116, TIC126

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

TYPICAL CHARACTERISTICS

PEAK ON-STATE VOLTAGE
vs
PEAK ON-STATE CURRENT

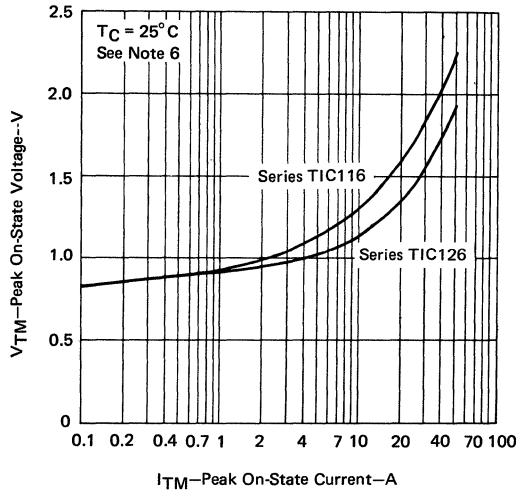


FIGURE 11

GATE-CONTROLLED TURN-ON TIME
vs
GATE CURRENT

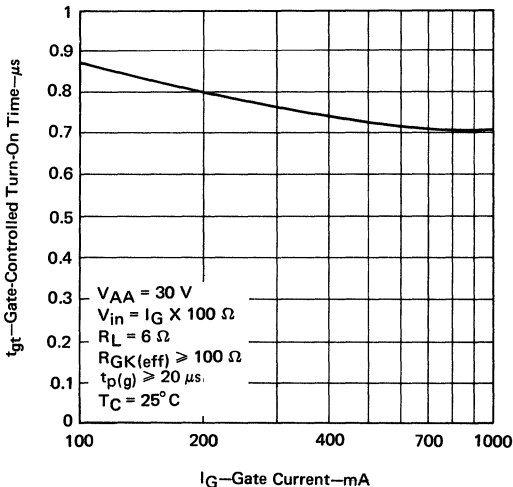


FIGURE 12

CIRCUIT-COMMUTATED TURN-OFF TIME
vs
CASE TEMPERATURE

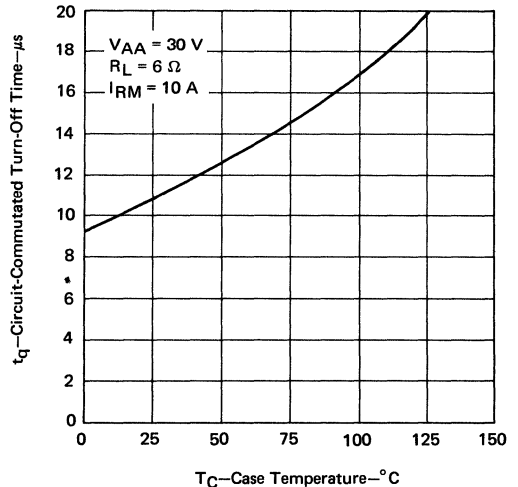


FIGURE 13

NOTE 6: This parameter must be measured using pulse techniques. $t_w = 300\ \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

SERIES TIC205, TIC206 SILICON BIDIRECTIONAL TRIODE THYRISTORS

SERIES TIC205, TIC206
BULLETIN NO. DL-S-711621, DECEMBER 1971

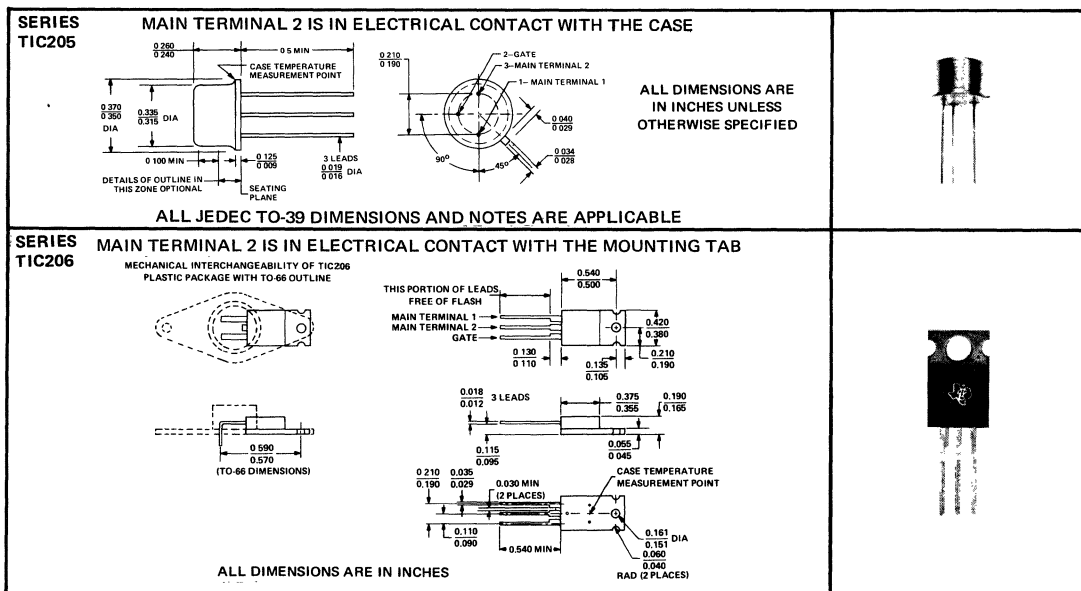
SENSITIVE-GATE TRIACS

- 2 A RMS (Series TIC205)
- 3 A RMS (Series TIC206)
- 100 V, 200 V, and 400 V V_{DRM}

description

These devices are bidirectional triode thyristors (triacs) which may be triggered from the off-state to the on-state by either polarity of gate signal with Main Terminal 2 at either polarity.

mechanical data



7

absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

	SERIES TIC205	SERIES TIC206	UNIT
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	A Suffix	100	V
	B Suffix	200	
	D Suffix	400	
Full-Cycle RMS On-State Current at (or below) 70°C Case Temperature, $I_T(RMS)$ (See Note 2)	2	3	A
Peak On-State Surge Current, Full-Sine-Wave, I_{TSM} (See Note 3)	20	20	A
Peak Gate Current, I_{GM}	± 1	± 1	A
Operating Case Temperature Range	-40 to 110		°C
Storage Temperature Range	-40 to 125		°C
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	230		°C

- NOTES: 1. These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.
 2. This value applies for 50-Hz to 60-Hz full-sine-wave operation with resistive load. Above 70°C derate linearly to 110°C case temperature at the rate of 50 mA/°C for Series TIC205 and 75 mA/°C for Series TIC206.
 3. This value applies for one 60-Hz full sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

[†]All voltage values are with respect to Main Terminal 1.

SERIES TIC205, TIC206

SILICON BIDIRECTIONAL TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	SERIES TIC205		SERIES TIC206		UNIT
		MIN	MAX	MIN	MAX	
I_{DRM} Repetitive Peak Off-State Current	$V_{DRM} = \text{Rated } V_{DRM}, I_G = 0, T_C = 110^\circ\text{C}$	±1		±1		mA
I_{GTM} Peak Gate Trigger Current	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	5		5		mA
	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-5		-5		
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-5		-5		
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	10		10		
V_{GTM} Peak Gate Trigger Voltage	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	2		2		V
	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-2		-2		
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-2		-2		
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	2		2		
V_{TM} Peak On-State Voltage	$I_{TM} = \pm 2.8\text{ A}, I_G = 50\text{ mA}, \text{ See Note 4}$	±1.9				V
	$I_{TM} = \pm 4.2\text{ A}, I_G = 50\text{ mA}, \text{ See Note 4}$			±2.2		
I_H Holding Current	$V_{supply} = +12\text{ V}^\dagger, I_G = 0, \text{ Initiating } I_{TM} = 100\text{ mA}$	30		30		mA
	$V_{supply} = -12\text{ V}^\dagger, I_G = 0, \text{ Initiating } I_{TM} = -100\text{ mA}$	-30		-30		

† All voltage values are with respect to Main Terminal 1.

- NOTES: 4. This parameter must be measured using pulse techniques. $t_w \leq 1\text{ ms}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.
5. The triacs are triggered by a 15-V (open-circuit amplitude) pulse supplied by a generator with the following characteristics: $R_G = 100\ \Omega, t_w = 20\ \mu\text{s}, t_r \leq 15\text{ ns}, t_f \leq 15\text{ ns}, f = 1\text{ kHz}$.

7

thermal characteristics

PARAMETER	SERIES TIC205		SERIES TIC206		UNIT
	MAX	MAX	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	13.7		7.8		°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	175		62.5		

SERIES TIC215, TIC216 SILICON BIDIRECTIONAL TRIODE THYRISTORS

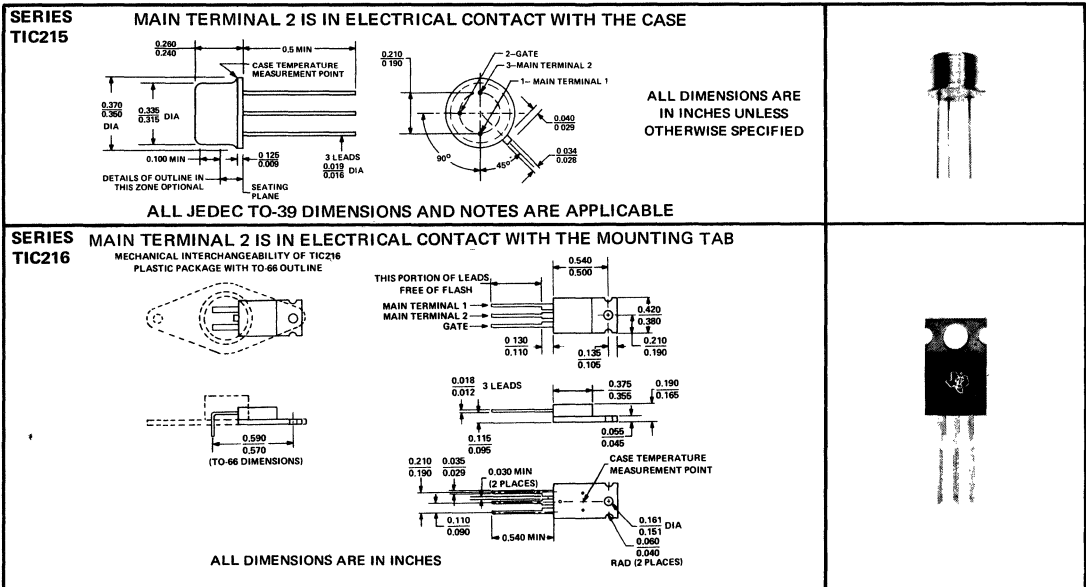
 SERIES TIC215, TIC216
BULLETIN NO. DL-S-711629, DECEMBER 1971

SENSITIVE-GATE TRIACS 3 A and 6 A RMS • 100 V, 200 V, and 400 V

description

These devices are bidirectional triode thyristors (triacs) which may be triggered from the off-state by either polarity of gate signal with Main Terminal 2 at either polarity.

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

	SERIES TIC215	SERIES TIC216	UNIT
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	A Suffix	100	V
	B Suffix	200	
	D Suffix	400	
Full-Cycle RMS On-State Current at (or below) 70°C Case Temperature, $I_T(RMS)$ (See Note 2)	3	6	A
Peak On-State Surge Current, Full-Sine-Wave, I_{TSM} (See Note 3)	20	60	A
Peak Gate Current, I_{GM}	±1	±1	A
Operating Case Temperature Range	-40 to 110		°C
Storage Temperature Range	-40 to 125		°C
Lead or Terminal Temperature 1/16 Inch from Case for 10 Seconds	230		°C

- NOTES: 1. These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.
 2. This value applies for 50-Hz to 60-Hz full-sine-wave operation with resistive load. Above 70°C derate linearly to 110°C case temperature at the rate of 75 mA/°C for Series TIC215 and 150 mA/°C for Series TIC216.
 3. This value applies for one 60-Hz full sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

[†]All voltage values are with respect to Main Terminal 1.

SERIES TIC215, TIC216

SILICON BIDIRECTIONAL TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	SERIES TIC215			SERIES TIC216			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
I_{DRM} Repetitive Peak Off-State Current	$V_{DRM} = \text{Rated } V_{DRM}, I_G = 0, T_C = 110^\circ\text{C}$			±2			±2	mA
I_{GTM} Peak Gate Trigger Current	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			5			5	mA
	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			-5			-5	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			-5			-5	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			10			10	
V_{GTM} Peak Gate Trigger Voltage	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			2.2			2.2	V
	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			-2.2			-2.2	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			-2.2			-2.2	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$			3			3	
V_{TM} Peak On-State Voltage	$I_{TM} = \pm 4.2\text{ A}, I_G = 100\text{ mA}, \text{ See Note 4}$			±2				V
	$I_{TM} = \pm 8.4\text{ A}, I_G = 100\text{ mA}, \text{ See Note 4}$						±1.7	
I_H Holding Current	$V_{supply} = +12\text{ V}^\dagger, I_G = 0, \text{ Initiating } I_{TM} = 100\text{ mA}$			30			30	mA
	$V_{supply} = -12\text{ V}^\dagger, I_G = 0, \text{ Initiating } I_{TM} = -100\text{ mA}$			-30			-30	
I_L Latching Current	$V_{supply} = +12\text{ V}^\dagger, \text{ See Note 5}$			50			50	mA
	$V_{supply} = -12\text{ V}^\dagger, \text{ See Note 5}$			-20			-20	

†All voltage values are with respect to Main Terminal 1.

NOTES: 4. This parameter must be measured using pulse techniques. $t_w \leq 1\text{ ms}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

5. The triacs are triggered by a 15-V (open-circuit amplitude) pulse supplied by a generator with the following characteristics: $R_G = 100\ \Omega, t_w = 20\ \mu\text{s}, t_r \leq 15\text{ ns}, t_f \leq 15\text{ ns}, f = 1\text{ kHz}$.

thermal characteristics

PARAMETER		SERIES TIC215	SERIES TIC216	UNIT
		MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance		8.6	5.1	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance		175	62.5	

7

TYPES TIC226B, TIC226D SILICON BIDIRECTIONAL TRIODE THYRISTORS

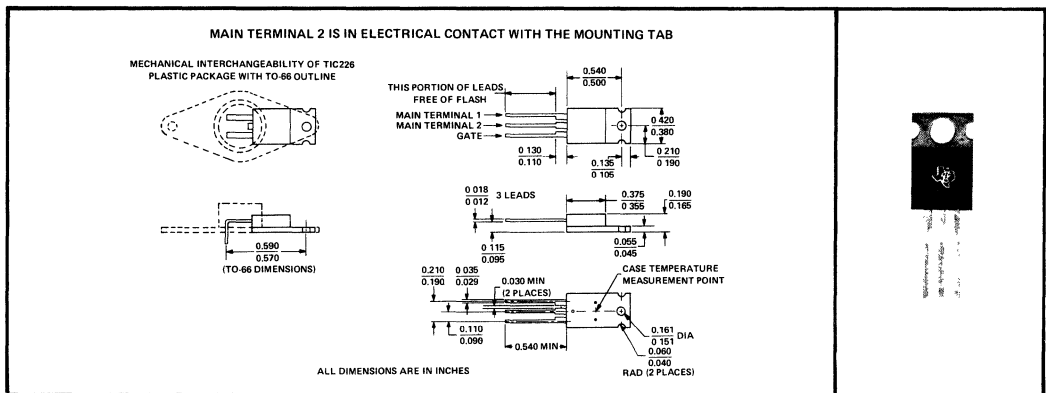
TYPES TIC226B, TIC226D
BULLETIN NO. DL-S-7111468, APRIL, 1971

8 A RMS • 200 V and 400 V
TRIACS
for
HIGH-TEMPERATURE, HIGH-CURRENT, and HIGH-VOLTAGE APPLICATIONS
• Typ dv/dt of 500 V/ μ s at 25°C

description

These devices are bidirectional triode thyristors (triacs) which may be triggered from the off-state to the on-state by either polarity of gate signal with Main Terminal 2 at either polarity.

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted) †

			UNIT
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	TIC226B	200	V
	TIC226D	400	
Full-Cycle RMS On-State Current at (or below) 85°C Case Temperature, $I_T(RMS)$ (See Note 2)		8	A
Peak On-State Surge Current, Full-Sine-Wave, I_{TSM} (See Note 3)		70	A
Peak On-State Surge Current, Half-Sine-Wave, I_{TSM} (See Note 4)		80	A
Peak Gate Current, I_{GM}		1	A
Peak Gate Power Dissipation, P_{GM} , at (or below) 85°C Case Temperature (Pulse Width \leq 200 μ s)		2.2	W
Average Gate Power Dissipation, $P_{G(av)}$, at (or below) 85°C Case Temperature (See Note 5)		0.9	W
Operating Case Temperature Range		-40 to 110	°C
Storage Temperature Range		-40 to 125	°C
Lead Temperature 1/16 Inch from Case for 10 Seconds		230	°C

- NOTES: 1. These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.
2. This value applies for 50-Hz to 60-Hz full-sine-wave operation with resistive load. Above 85°C derate according to Figure 2.
3. This value applies for one 60-Hz full sine wave when the device is operating at (or below) the rated value of on-state current. Surge may be repeated after the device has returned to original thermal equilibrium. During the surge, gate control may be lost.
4. This value applies for one 60-Hz half sine wave when the device is operating at (or below) the rated value of on-state current. Surge may be repeated after the device has returned to original thermal equilibrium. During the surge, gate control may be lost.
5. This value applies for a maximum averaging time of 16.6 ms.

† All voltage values are with respect to Main Terminal 1.

TYPES TIC226B, TIC226D

SILICON BIDIRECTIONAL TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted) †

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRM}	Repetitive Peak Off-State Current	$V_{DRM} = \text{Rated } V_{DRM}, I_G = 0, T_C = 110^\circ\text{C}$			±2	mA
I_{GTM}	Peak Gate Trigger Current	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		15	50	mA
		$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		-25	-50	
		$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		-30	-50	
		$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		75		
V_{GTM}	Peak Gate Trigger Voltage	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		0.9	2.5	V
		$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		-1.2	-2.5	
		$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		-1.2	-2.5	
		$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$		1.2		
V_{TM}	Peak On-State Voltage	$I_{TM} = \pm 12\text{ A}, I_G = 100\text{ mA}$, See Note 6			±2.1	V
I_H	Holding Current	$V_{supply} = +12\text{ V}^\dagger, I_G = 0$, Initiating $I_{TM} = 500\text{ mA}$		20	60	mA
		$V_{supply} = -12\text{ V}^\dagger, I_G = 0$, Initiating $I_{TM} = -500\text{ mA}$		-30	-60	
I_L	Latching Current	$V_{supply} = +12\text{ V}^\dagger$, See Note 7		30	70	mA
		$V_{supply} = -12\text{ V}^\dagger$, See Note 7		-40	-70	
dv/dt	Critical Rate of Rise of Off-State Voltage	$V_{DRM} = \text{Rated } V_{DRM}, I_G = 0, T_C = 110^\circ\text{C}$		500		V/ μs
dv/dt	Critical Rate of Rise of Commutation Voltage	$V_{DRM} = \text{Rated } V_{DRM}, I_{TRM} = \pm 12\text{ A}, T_C = 85^\circ\text{C}$, See Figure 3		5		V/ μs

† All voltage values are with respect to Main Terminal 1.

NOTES: 6. This parameter must be measured using pulse techniques. $t_w \leq 1\text{ ms}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

7. The triacs are triggered by a 15-V (open-circuit amplitude) pulse supplied by a generator with the following characteristics: $R_G = 100\ \Omega$, $t_w = 20\ \mu\text{s}$, $t_r \leq 15\text{ ns}$, $t_f \leq 15\text{ ns}$, $f = 1\text{ kHz}$.

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	1.8	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	62.5	

TYPES TIC226B, TIC226D SILICON BIDIRECTIONAL TRIODE THYRISTORS

PARAMETER MEASUREMENT INFORMATION

The *rate of rise of commutation voltage* is defined as the slope of the line connecting the 10% and 63% test voltage points.

The *critical rate of rise of commutation voltage* is the rate above which the device will not sustain the off-state following conduction but will conduct current in the opposite direction in the absence of a gate-trigger signal. While this failure to switch to the off-state is not detrimental to the thyristor, it does result in loss of control of power to the load.

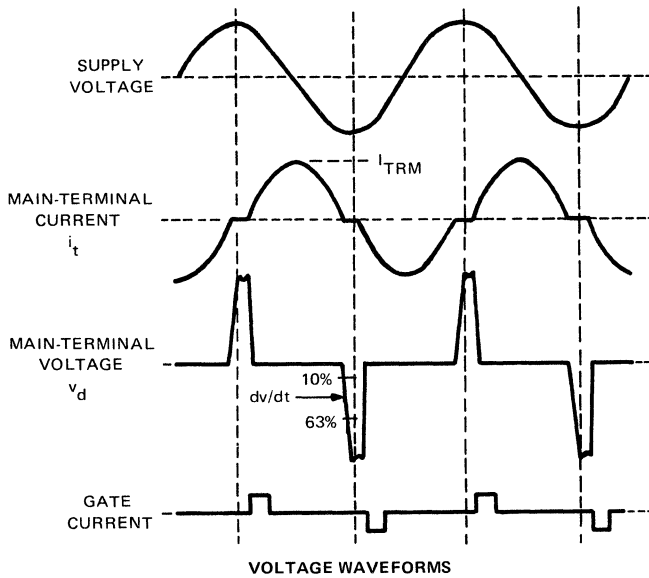
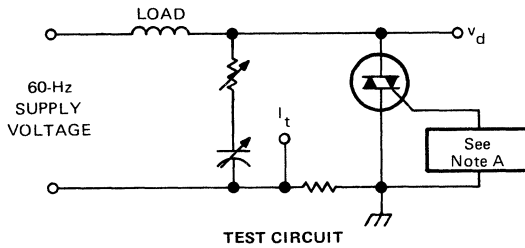


FIGURE 1—COMMUTATING dv/dt

NOTE A: The gate-current pulse is furnished by a trigger circuit which presents essentially an open circuit between pulses. The pulse is timed so that the off-state-voltage duration is approximately 800 μ s.

TYPES TIC226B, TIC226D SILICON BIDIRECTIONAL TRIODE THYRISTORS

THERMAL INFORMATION

MAXIMUM RMS ON-STATE CURRENT
VS
CASE TEMPERATURE

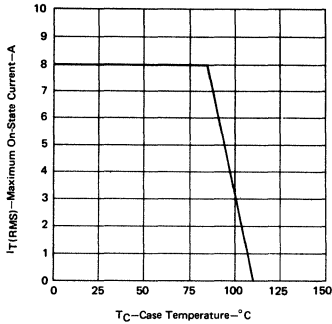


FIGURE 2
SURGE ON-STATE CURRENT
VS
CYCLES OF CURRENT DURATION

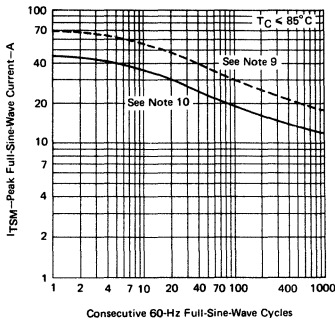


FIGURE 4

MAXIMUM AVERAGE POWER DISSIPATED
VS
RMS ON-STATE CURRENT

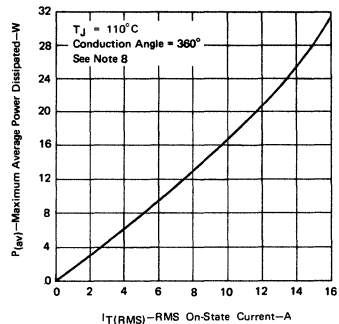


FIGURE 3

- NOTES: 8. For operation at current greater than 8 amps rms, see Figure 4.
9. The dashed curve shows the maximum number of cycles of surge current recommended for safe operation provided the device is initially operating at, or below, the rated value of on-state current; however, during the surge period gate control of the device may be lost.
10. The solid curve shows the maximum number of cycles of surge current for which gate control is guaranteed provided the device is initially at nonoperating thermal equilibrium.

TYPICAL CHARACTERISTICS

PEAK GATE TRIGGER CURRENT
VS
CASE TEMPERATURE

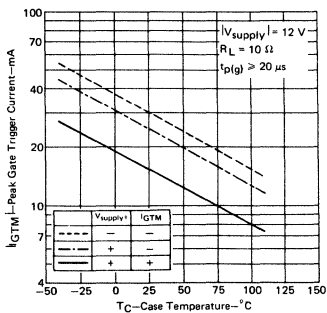


FIGURE 5

PEAK GATE TRIGGER VOLTAGE
VS
CASE TEMPERATURE

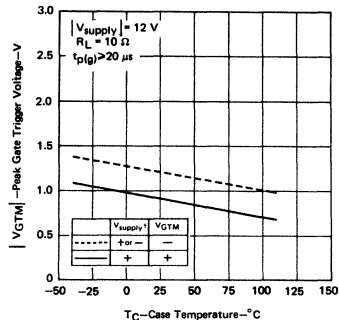


FIGURE 6

†The supply voltage is called positive when it causes Main Terminal 2 to be positive with respect to Main Terminal 1.

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SERIES TIC236, TIC246 SILICON BIDIRECTIONAL TRIODE THYRISTORS

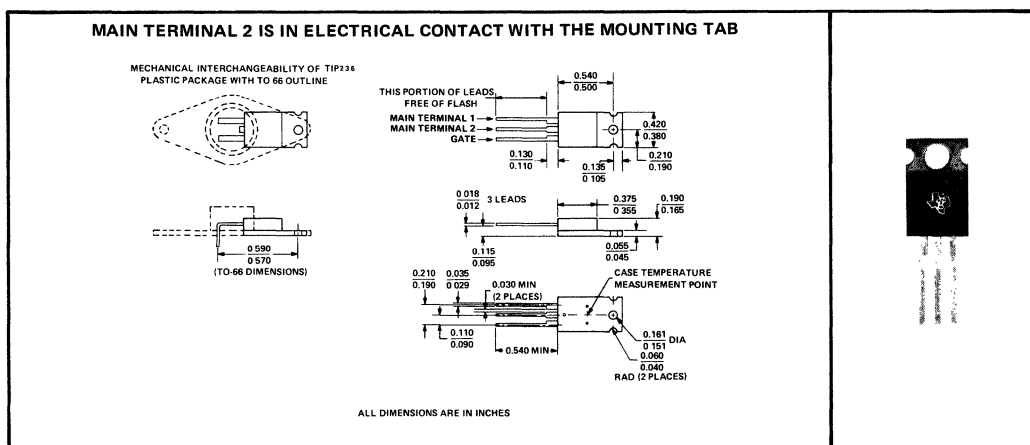
SERIES TIC236, TIC246
BULLETIN NO. DL-S-7111628, DECEMBER 1971

TRIACS 12 A and 16 A RMS • 200 V and 400 V

description

These devices are bidirectional triode thyristors (triacs) which may be triggered from the off-state by either polarity of gate signal with Main Terminal 2 at either polarity. This triac is available in the isolated tab package as a special device. For information contact a TI field sales office or Power Product Marketing, MS 51, P.O. Box 5012, Dallas, Texas 75222.

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted) †

	SERIES TIC236	SERIES TIC246	UNIT	
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	B Suffix	200	200	V
	D Suffix	400	400	
Full-Cycle RMS On-State Current at (or below) 70°C Case Temperature, $I_T(RMS)$ (See Note 2)		12	16	A
Peak On-State Surge Current, Full-Sine-Wave, I_{TSM} (See Note 2)		100	125	A
Peak Gate Current, I_{GM}		±1	±1	A
Operating Case Temperature Range	-40 to 110		°C	
Storage Temperature Range	-40 to 125		°C	
Terminal Temperature 1/16 Inch from Case for 10 Seconds	230		°C	

- NOTES: 1. These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.
2. This value applies for 50-Hz to 60-Hz full-sine-wave operation with resistive load. Above 70°C derate linearly to 110°C case temperature at the rate of 300 mA/°C for Series TIC236 and 400 mA/°C for Series TIC246.
3. This value applies for one 60-Hz full sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

† All voltage values are with respect to Main Terminal 1.

SERIES TIC236, TIC246

SILICON BIDIRECTIONAL TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted) †

PARAMETER	TEST CONDITIONS	SERIES TIC236		SERIES TIC246		UNIT
		MIN	TYP MAX	MIN	TYP MAX	
I _{DRM} Repetitive Peak Off-State Current	V _{DRM} = Rated V _{DRM} , I _G = 0 T _C = 110°C		±2		±2	mA
I _{GTM} Peak Gate Trigger Current	V _{supply} = +12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	15	50	15	50	mA
	V _{supply} = +12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	-25	-50	-25	-50	
	V _{supply} = -12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	-30	-50	-30	-50	
	V _{supply} = -12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	75		75		
V _{GTM} Peak Gate Trigger Voltage	V _{supply} = +12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	1.2	2.5	1.2	2.5	V
	V _{supply} = +12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	-1.2	-2.5	-1.2	-2.5	
	V _{supply} = -12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	-1.2	-2.5	-1.2	-2.5	
	V _{supply} = -12 V [†] , R _L = 10 Ω, t _{p(g)} ≥ 20 μs	1.2		1.2		
V _{TM} Peak On-State Voltage	I _{TM} = ±17 A, I _G = 100 mA, See Note 4	±2.1				V
	I _{TM} = ±22.5 A, I _G = 100 mA, See Note 4			±1.7		
I _H Holding Current	V _{supply} = +12 V [†] , I _G = 0, Initiating I _{TM} = 150 mA	50		50		mA
	V _{supply} = -12 V [†] , I _G = 0, Initiating I _{TM} = -150 mA	-50		-50		
I _L Latching Current	V _{supply} = +12 V [†] , See Note 5	20		20		mA
	V _{supply} = -12 V [†] , See Note 5	-20		-20		

† All voltage values are with respect to Main Terminal 1.

NOTES: 4. This parameter must be measured using pulse techniques. t_w ≤ 1 ms, duty cycle ≤ 2%. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

5. The triacs are triggered by a 15-V (open-circuit amplitude) pulse supplied by a generator with the following characteristics: R_G = 100 Ω, t_w = 20 μs, t_r ≤ 15 ns, t_f ≤ 15 ns, f = 1 kHz.

7

thermal characteristics

PARAMETER	SERIES TIC236	SERIES TIC246	UNIT
	MAX	MAX	
R _{θJC} Junction-to-Case Thermal Resistance	2	1.9	°C/W
R _{θJA} Junction-to-Free-Air Thermal Resistance	62.5	62.5	

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SERIES TIC253, TIC263 SILICON BIDIRECTIONAL TRIODE THYRISTORS

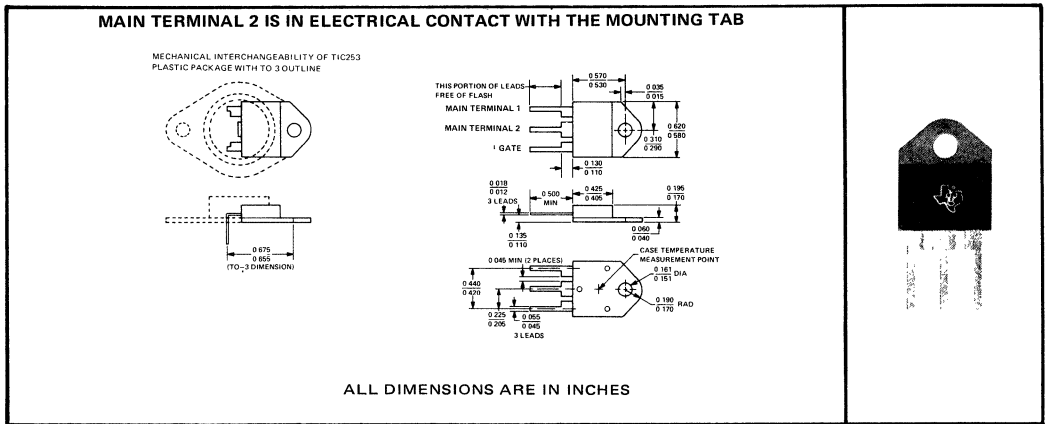
SERIES TIC253, TIC263
BULLETIN NO. DL-S-7111630, DECEMBER 1971

TRIACS
20 A and 25 A RMS • 200 V, 400 V, 500 V, and 600 V

description

These devices are bidirectional triode thyristors (triacs) which may be triggered from the off-state by either polarity of gate signal with Main Terminal 2 at either polarity. This triac is available in the isolated tab package as a special device. For information contact a TI field sales office or Power Product Marketing, MS 51, P.O. Box 5012, Dallas, Texas 75222.

mechanical data



7

absolute maximum ratings over operating case temperature range (unless otherwise noted) †

	SERIES TIC253	SERIES TIC263	UNIT
Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	B Suffix	200	V
	D Suffix	400	
	E Suffix	500	
	M Suffix	600	
Full-Cycle RMS On-State Current at (or below) 70°C Case Temperature, $I_T(RMS)$ (See Note 2)	20	25	A
Peak On-State Surge Current, Full-Sine-Wave, I_{TSM} (See Note 3)	150	175	A
Peak Gate Current, I_{GM}	±1	±1	A
Operating Case Temperature Range	-40 to 110		°C
Storage Temperature Range	-40 to 125		°C
Terminal Temperature 1/16 Inch from Case for 10 Seconds	230		°C

- NOTES: 1. These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.
2. This value applies for 50-Hz to 60-Hz full-sine-wave operation with resistive load. Above 70°C derate linearly to 110°C case temperature at the rate of 500 mA/°C for Series TIC253 and 625 mA/°C for Series TIC263.
3. This value applies for one 60-Hz full sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

†All voltage values are with respect to Main Terminal 1.

SERIES TIC253, TIC263 SILICON BIDIRECTIONAL TRIODE THYRISTORS

electrical characteristics at 25°C case temperature (unless otherwise noted) †

PARAMETER	TEST CONDITIONS	SERIES TIC253	SERIES TIC263	UNIT
		MIN TYP MAX	MIN TYP MAX	
I_{DRM} Repetitive Peak Off-State Current	$V_{DRM} = \text{Rated } V_{DRM}, I_G = 0, T_C = 110^\circ\text{C}$	±2	±2	mA
I_{GTM} Peak Gate Trigger Current	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	50	50	mA
	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-50	-50	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-50	-50	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	50	50	
V_{GTM} Peak Gate Trigger Voltage	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	2.5	2.5	V
	$V_{supply} = +12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-2.5	-2.5	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	-2.5	-2.5	
	$V_{supply} = -12\text{ V}^\dagger, R_L = 10\ \Omega, t_{p(g)} \geq 20\ \mu\text{s}$	1.2	1.2	
V_{TM} Peak On-State Voltage	$I_{TM} = \pm 28.2\text{ A}, I_G = 100\text{ mA}, \text{ See Note 4}$	±1.7		V
	$I_{TM} = 35.2\text{ A}, I_G = 100\text{ mA}, \text{ See Note 4}$		±1.7	
I_H Holding Current	$V_{supply} = +12\text{ V}^\dagger, I_G = 0, \text{ Initiating } I_{TM} = 100\text{ mA}$	50	50	mA
	$V_{supply} = -12\text{ V}^\dagger, I_G = 0, \text{ Initiating } I_{RM} = -100\text{ mA}$	-50	-50	
I_L Latching Current	$V_{supply} = +12\text{ V}^\dagger, \text{ See Note 5}$	20	20	mA
	$V_{supply} = -12\text{ V}^\dagger, \text{ See Note 5}$	-20	-20	

† All voltage values are with respect to Main Terminal 1.

NOTES: 4. This parameter must be measured using pulse techniques. $t_w \leq 1\text{ ms}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

5. The triacs are triggered by a 15-V (open-circuit amplitude) pulse supplied by a generator with the following characteristics: $R_G = 100\ \Omega, t_w = 20\ \mu\text{s}, t_r \leq 15\text{ ns}, t_f \leq 15\text{ ns}, f = 1\text{ kHz}$.

thermal characteristics

PARAMETER	SERIES TIC253	SERIES TIC263	UNIT
	MAX	MAX	
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.52	1.22	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	36	36	

7

Technical Response Lab

TECHNICAL RESPONSE LAB

The power semiconductor device industry can be considered to comprise two broad categories of products. There are the high-volume, low-cost devices filling "workhorse" needs for the consumer and industrial markets. The plastic package devices in this data book are representative of such products. A large segment of the market, however, particularly the military/aerospace industry, requires power devices of custom or near-custom design to fill the needs for special performance and/or environmental capability.

This section is devoted to a discussion of a special power device custom design and assembly facility at Dallas, Texas. Texas Instruments is proud to consider this facility, termed the Technical Response Lab (TRL), as a unique leadership contribution in the semiconductor industry.

TRL History

During the past decade, it has become increasingly apparent that power transistor technology was moving forward with a speed exceeded only by integrated circuits. With the vast improvements in integrated electronics, the power transistor function, in many circuits, has become highly specialized. TI, foreseeing the trend toward highly specialized devices, realized the need for a highly "state-of-the-art" dependent laboratory facility. From this vision in 1967, the original "Quick Reaction" lab was established. This lab was staffed with technicians trained in high-reliability assembly operations. An assembly engineering team was assigned with close liaison with semiconductor chip development engineering in order to coordinate the planning and introduction of new products.

By early 1969, the "Quick Reaction" lab had become so successful that the need for expansion became acute. Incorporating all of the best elements of TI's other high-reliability manufacturing areas, a newer and larger lab was built utilizing a laminar-flow clean-room approach. New equipment was installed and more technicians were added to bring the production capability to five thousand units per week. The name was changed to "Technical Response Lab" in recognition of the direct link to the chip development area.

At this time, the direction TRL was to take changed somewhat from a small "job shop" operation to a customer-oriented, high-reliability assembly operation. The assembly of all ultra-high-reliability power devices was shifted to TRL for such programs as *Minuteman*, *Poseidon*, *SRAM*, and *Spartan* to take advantage of the technical capabilities of the assembly operators.

Process control monitoring of all assembly operations has been increased, with a full-time process control technician assigned to the lab. Assembly is still controlled strictly and limited to a one-shift basis to optimize engineering effort on these products. Advanced computer-controlled lot tracking facilitates the isolation of diffusion runs within an assembly lot. The computer is again utilized for scheduling, inventory control, and work-in-process cycle time monitoring. Standard cycle time through assembly is now only three to four days. Two-day cycle time is readily available in emergency situations.

TRL Capabilities

Capabilities built into the original "Quick Reaction" area have been retained (and perhaps increased somewhat) during the expansion to the TRL phase. Customer requirements are such that some customers prefer "soft"[†] solder while others prefer "hard" solder. A conformal coating of the semiconductor is required more often than not. Radiation-hardening requirements have made use of gold in packaging unthinkable for some devices. All of these and many, many more requirements made state-of-the-art capability a necessity.

[†]See Power Semiconductor Technology, Section 10.

TECHNICAL RESPONSE LAB

TI leadership in packaging capability is felt to be well established, not only in design but in delivery requirements. A totally non-magnetic package (less than 0.1 gamma at 1" from sensor head) is now a standard item in TRL. For isolated uses such as magnetic detection of metallic objects or changes in magnetic field intensity during space flights, the totally non-magnetic package has become a necessity. This approach has been used on TO-3, TO-66, and a modified TO-121 package. The modified TO-121 package also has the capability of handling a range of requirements from a 450-MHz RF power device to a 30-ampere high-SOA switch. Cold welding is used on this and other packages to eliminate the possible weld flash particles that could be generated by resistance welding.

Virtually any power device package/chip combination is available from Technical Response Lab. Variations of standard packages are also available. TI realizes the obvious advantages of combining the best elements of several packages to satisfy a customer's special requirement. The knowledge and experience gained from such special designs provides the background for TRL to be able to react more quickly to future customer needs.

A complete list of available packages and their modified versions is listed in Table 1.

Custom Design Procedure

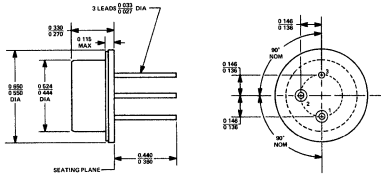
Normal procedure in industry seems to be for the circuit design engineer to try to use standard data sheet devices to develop the prototype circuits. This approach usually works satisfactorily except that it normally does not take full advantage of the possibility of merging the electrical capability of the device with the best packaging approach. The TRL engineering team is well versed in all of the packages in Table I and all of the standard data sheet devices in this catalog. It is to the design engineer's advantage to pick out the electrical parameters needed in a particular design slot, assume that the "device" will go in any package, and then contact TI for special samples. If there is a problem with chip size versus package, the TRL engineer will work with you toward the most equitable solution. Samples can then be supplied in as little as two days.

TABLE I

The following table lists the power packages available from the Technical Response Lab. If the package is a standard package, a JEDEC registration number which depicts its outline is listed for reference if such a designation has been assigned. For packages not shown on data sheets in this book, the outline is shown at the end of this section.

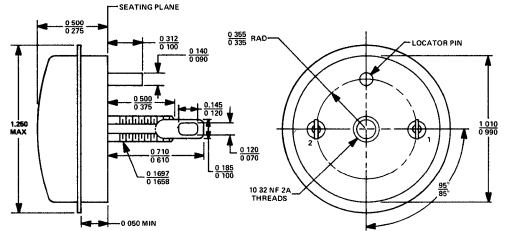
CASE TYPE	SEE DATA SHEET FOR OUTLINE	VERSIONS AVAILABLE
TO-3	2N5157	Moly mounting pad Eight-lead Non-magnetic 60-mil emitter pin 150-mil emitter pin
TO-5	2N3418	Isolated Coined-header Thermoslug
TO-8	See Figure 1	Copper-clad steel
TO-18	TIC35	Coined header
TO-33	2N5390	Thermoslug Coined header
TO-36/TO-67	See Figure 2	Cold weld
TO-37	See Figure 3	Coined header
TO-39	2N5151	Coined header
TO-46	See Figure 4	Coined header
TO-59	2N5003	Isolated collector Hot collector "Short" stud
TO-60	See Figure 5	Isolated collector
TI Outline ZZZZ	2N5938	"Short" stud Isolated collector
TO-61	2N4301 2N6127	Hot collector Isolated Collector
TO-62	See Figure 6	Hot collector
TO-63	2N4002	Hot collector Isolated collector 60-mil emitter post
TO-66	2N3583	Non-magnetic Moly mounting pad
TO-81	See Figure 7	Cold weld
TO-82	See Figure 8	Cold weld
TO-111	2N3998 2N3996	Hot collector Isolated collector
TO-114	TIXP547	Hot collector
TO-121	See Figure 9	Al ₂ O ₃ BeO
TI Outline 5G	See Figure 10	Totally non-magnetic < 0.1 gamma at 1/2" Lead configuration optional
TI Outline DDD	2N3551	BeO Al ₂ O ₃ Cold weld
TI Outline QQ	2N3263	Cold weld

TECHNICAL RESPONSE LAB



ALL JEDEC TO-8 DIMENSIONS AND NOTES ARE APPLICABLE
LEAD 3 IS IN ELECTRICAL CONTACT WITH THE CASE
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

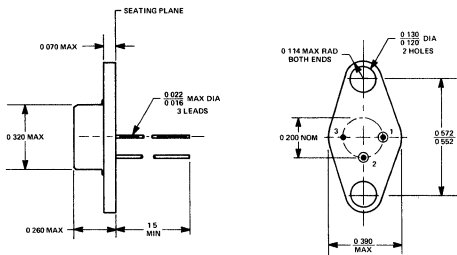
FIGURE 1—OUTLINE TO-8



ALL JEDEC TO-67 DIMENSIONS AND NOTES ARE APPLICABLE
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

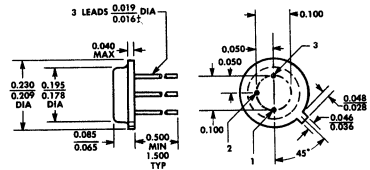
NOTE: TO-36 falls within these specifications.

FIGURE 2—OUTLINE TO-67



ALL JEDEC TO-37 DIMENSIONS AND NOTES ARE APPLICABLE
LEAD 3 IS IN ELECTRICAL CONTACT WITH THE CASE
ALL DIMENSIONS ARE IN INCHES

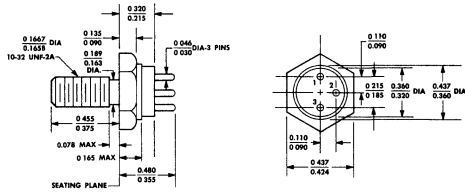
FIGURE 3—OUTLINE TO-37



ALL JEDEC TO-46 DIMENSIONS AND NOTES ARE APPLICABLE
LEAD 3 IS IN ELECTRICAL CONTACT WITH THE CASE
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

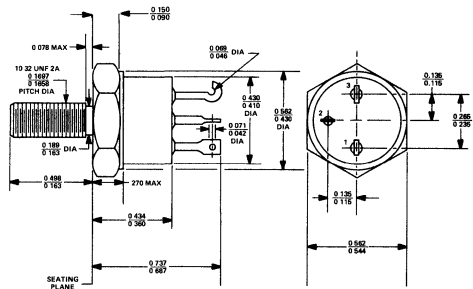
†T1 guaranteed minimum. The JEDEC registered minimum lead diameter for TO-46 is 0.012.

FIGURE 4—OUTLINE TO-46



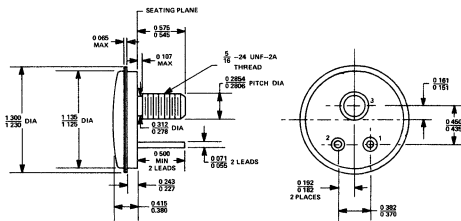
ALL JEDEC TO-60 DIMENSIONS AND NOTES ARE APPLICABLE
 ALL TERMINALS ARE INSULATED FROM THE CASE
 ALL DIMENSIONS ARE IN INCHES

FIGURE 5—OUTLINE TO-60



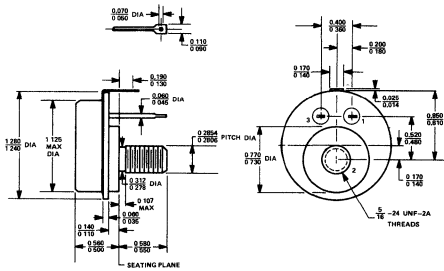
ALL JEDEC TO-62 DIMENSIONS AND NOTES ARE APPLICABLE
 TERMINAL 3 IS IN ELECTRICAL CONTACT WITH THE CASE
 ALL DIMENSIONS ARE IN INCHES

FIGURE 6—OUTLINE TO-62



ALL JEDEC TO-81 DIMENSIONS AND NOTES ARE APPLICABLE
 ALL DIMENSIONS ARE IN INCHES

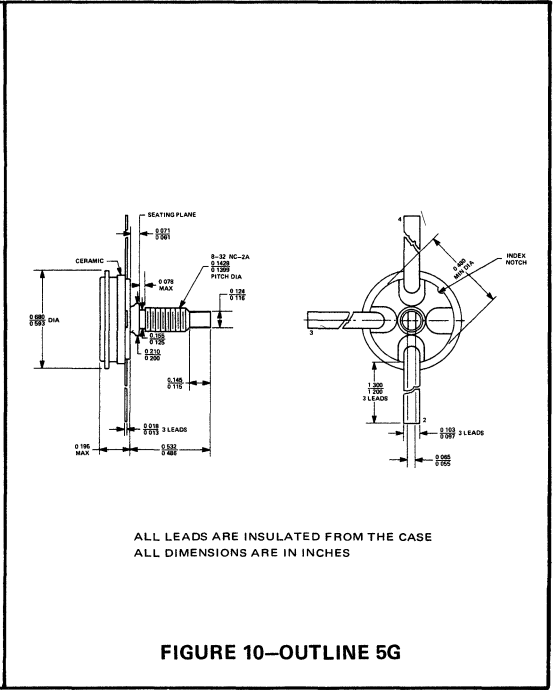
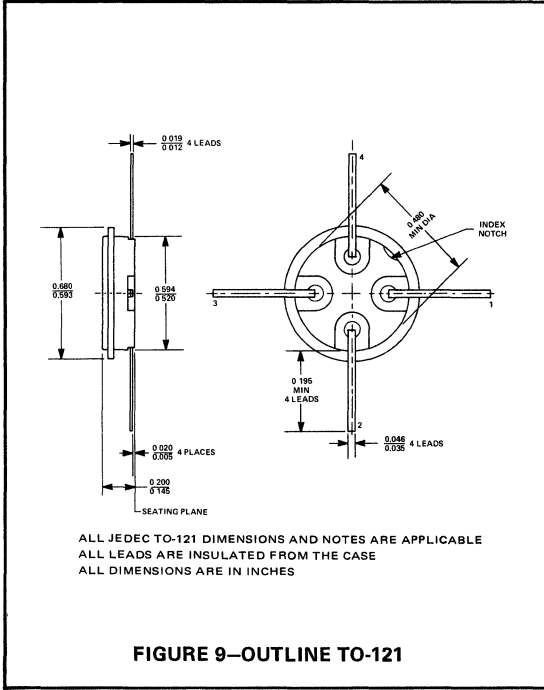
FIGURE 7—OUTLINE TO-81



ALL JEDEC TO-82 DIMENSIONS AND NOTES ARE APPLICABLE
 ALL DIMENSIONS ARE IN INCHES

FIGURE 8—OUTLINE TO-82

TECHNICAL RESPONSE LAB



Power Functions

GENERAL

A power function is a package of active and passive components able to perform a specified function requiring power transistors or thyristors. Thick-film circuits or printed circuit boards are used to achieve a cost-effective package to meet "black box" specifications. In most cases, power functions require heat sinks. Therefore, size and weight are not as important as for monolithic integrated circuits.

Texas Instruments manufactures a standard line of power functions:

Amplifiers

Inverters

Parallel Transistor Assemblies

Regulators

Relays

Surge Protectors

In addition to the standard line, TI makes custom power functions which are variations of the standard line. Custom power functions may also require completely new approaches involving TI experience in power semiconductor technology.

SOLID-STATE POWER FUNCTIONS

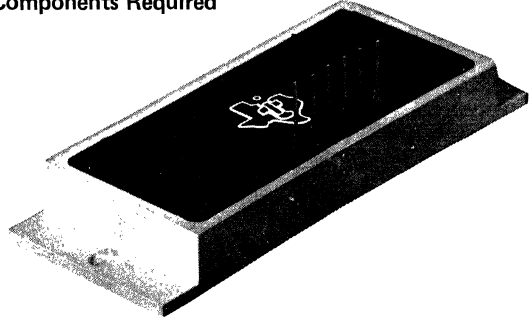
TYPE TIXH601 AUDIO POWER AMPLIFIER

TYPE TIXH601
BULLETIN NO. DL-S-711644, DECEMBER 1971

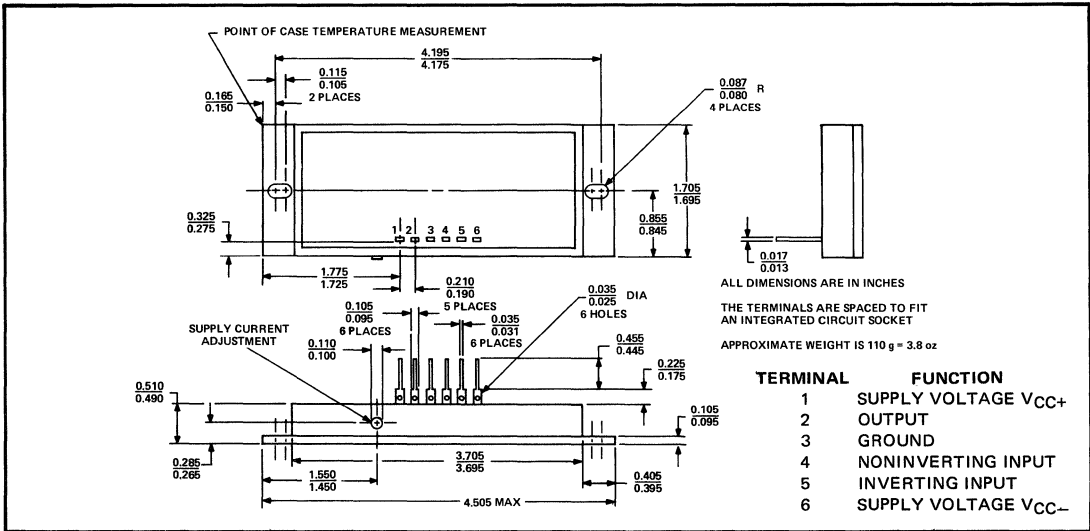
- 100-Watt RMS Power Output into 8 Ohms
- 25-Hz to 25-kHz Bandwidth at 80-W RMS Output
- No External Feedback Components Required

description

The TIXH601 amplifier is designed primarily for high-fidelity stereo systems, musical instruments, and other audio equipment. All necessary capacitors are supplied within the package. The amplifier uses a complementary-symmetry class-B output circuit with commutating diodes.



mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply Voltage V_{CC+} (See Note 1)	45 V
Supply Voltage V_{CC-} (See Note 1)	-45 V
Terminal-to-Case Voltage	± 500 V
Peak Input Voltage (See Note 1)	± 2 V
Peak Output Current	± 7 A
Power Dissipation at (or below) 50°C Case Temperature (See Note 2)	100 W
Power Dissipation at 85°C Case Temperature	65 W
Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	15 W
Operating Case Temperature Range	-25°C to 85°C
Storage Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 inch from Case for 5 Seconds	260°C

- NOTES: 1. Voltage values are with respect to device ground terminal.
2. Derate linearly to 65 W at 85°C case temperature at the rate of 1 W/°C.
3. Derate linearly to 85°C free-air temperature at the rate of 0.25 W/°C.

TENTATIVE DATA SHEET

This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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TYPE T1XH601 AUDIO POWER AMPLIFIER

electrical characteristics at 25°C case temperature (see figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A _v	Voltage Amplification	P _O = 80 W, f = 1 kHz	80	100		
		P _O = 100 W, f = 1 kHz	80			
f _{3db}	Cutoff Frequency	P _O = 1 W	Lower	10		Hz
			Upper	100		kHz
		P _O = 80 W	Lower	25		Hz
			Upper	25		kHz
THD	Total Harmonic Distortion (See Note 4)	P _O = 1 W, f = 1 kHz	0.2%	0.5%		
		P _O = 80 W, f = 1 kHz	0.6%			
		P _O = 100 W, f = 1 kHz	1%			
V _O	Output Voltage	Input open or shorted		±5		mV
z _i	Input Impedance	f = 1 kHz	20			kΩ

NOTE 4: The quiescent supply current I_{CC} should be adjusted for minimum crossover distortion which will occur typically at 35 mA.

PARAMETER MEASUREMENT INFORMATION

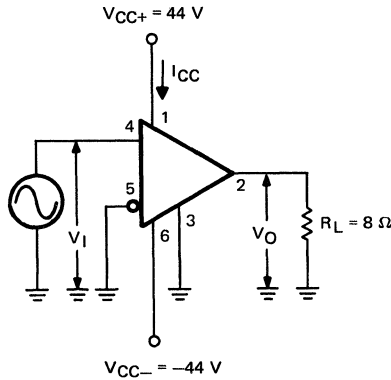


FIGURE 1

SOLID-STATE POWER FUNCTIONS

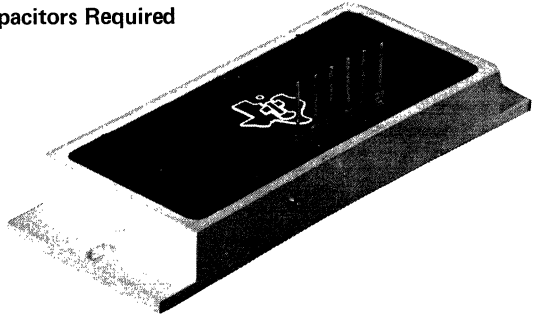
TYPE T1XH602 LINEAR POWER AMPLIFIER

TYPE T1XH602
BULLETIN NO. DLS-7111645, DECEMBER 1971

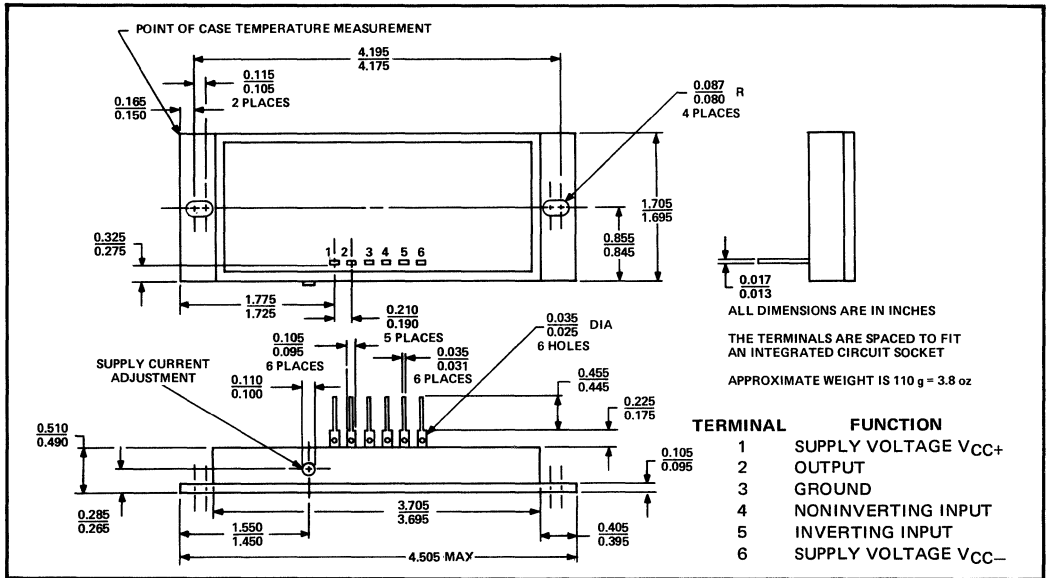
- Up to 100-Watt Power Output
- 7-A Peak Load Current
- No External Capacitors Required

description

The T1XH602 is designed primarily for servo applications using output current feedback. The amplifier uses a complementary-symmetry class-B output circuit designed to be operated from a split power supply. All necessary capacitors are supplied within the package.



mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply Voltage V_{CC+} (See Note 1)	40 V
Supply Voltage V_{CC-} (See Note 1)	-40 V
Terminal-to-Case Voltage	± 500 V
Peak Input Voltage (See Note 1)	± 2 V
Peak Output Current	± 7 A
Power Dissipation at (or below) 50°C Case Temperature (See Note 2)	100 W
Power Dissipation at 85°C Case Temperature	65 W
Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	15 W
Operating Case Temperature Range	-25°C to 85°C
Storage Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 Inch from Case for 5 Seconds	260°C

- NOTES: 1. Voltage values are with respect to device ground terminal.
 2. Derate linearly to 65 W at 85°C case temperature at the rate of 1 W/°C.
 3. Derate linearly to 85°C free-air temperature at the rate of 0.25 W/°C.

TENTATIVE DATA SHEET

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TYPE TIxH602 LINEAR POWER AMPLIFIER

electrical characteristics at 25°C case temperature (see figure 1)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
I_O D-C Output Current	$V_G = 0$		20	80	mA
	$V_G = 3\text{ V}$	2.9		3.1	A
	$V_G = -3\text{ V}$	-2.9		-3.1	
I_{OM} Peak Output Current	$V_{GM} = 6\text{ V}, f = 5\text{ kHz}$	5.8		6.2	A
θ Phase Shift	$V_{GM} = 6\text{ V}, f = 5\text{ kHz}$		10°		
THD Total Harmonic Distortion	$V_{GM} = 6\text{ V}, f = 1\text{ kHz}$		1%		

† V_G is d-c source voltage, V_{GM} is the peak value of a-c source voltage.

PARAMETER MEASUREMENT INFORMATION

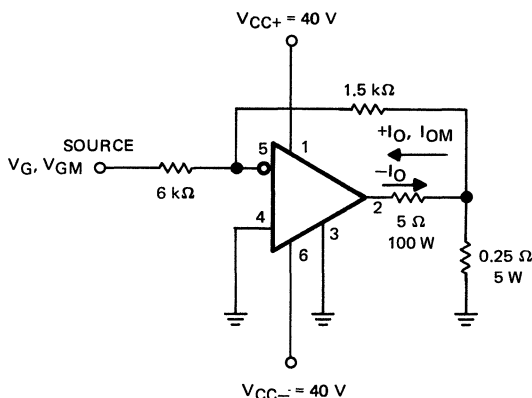


FIGURE 1

9

SOLID-STATE POWER FUNCTIONS

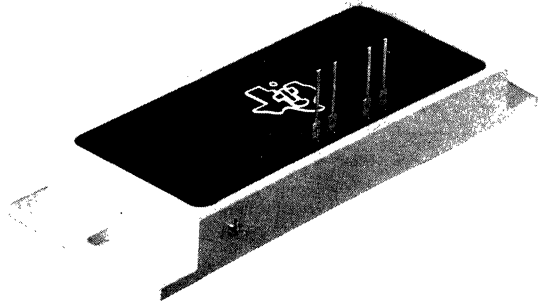
TYPES TIXH603, TIXH604 POSITIVE, NEGATIVE VOLTAGE REGULATORS

TYPES TIXH603, TIXH604
BULLETIN NO. DLS-711690, DECEMBER 1971

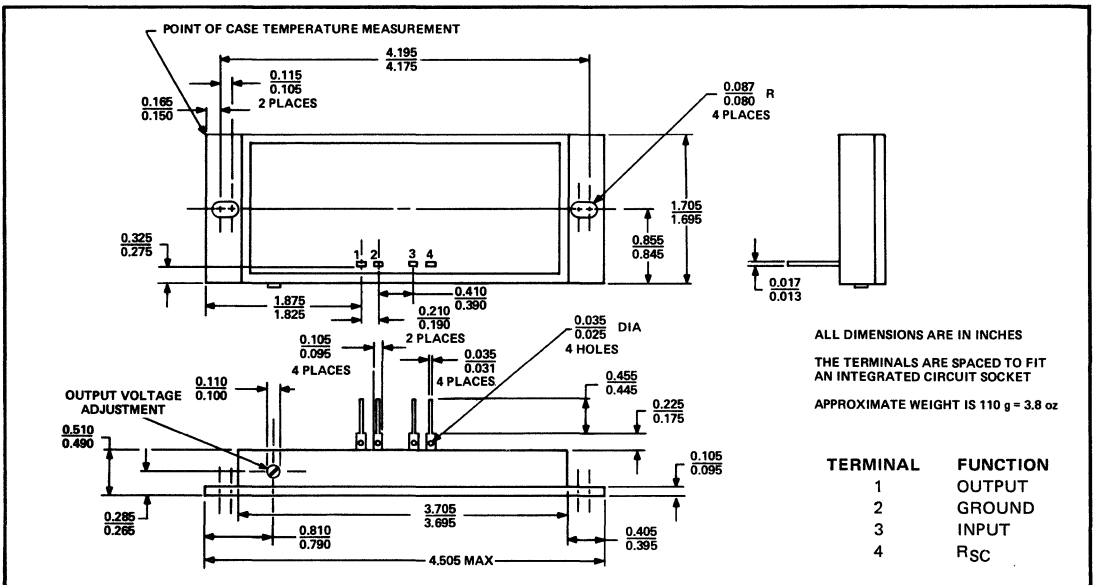
- Output Voltage Adjustable from 5 V to 30 V
- Output Current up to 4 A
- Input-to-Output Differential . . . 2 V to 35 V

description

The TIXH603 and TIXH604 are solid-state adjustable voltage regulators featuring low minimum input-to-output voltage differential. Current limiting can be obtained with the use of an external resistor. The TIXH603 positive voltage regulator is designed for use in negative-ground systems; the TIXH604 negative voltage regulator in positive-ground systems.



mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted, see note 1)

Input Voltage	40 V
Input-to-Output Voltage Differential	40 V
Terminal-to-Case Voltage	±500 V
Output Current	4 A
Power Dissipation at (or below) 50°C Case Temperature (See Note 2)	50 W
Power Dissipation at 85°C Case Temperature	32.5 W
Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	15 W
Operating Case Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 Inch from Case for 5 Seconds	235°C

- NOTES: 1. All voltage polarities shown apply for the positive voltage regulator type TIXH603. Reverse polarity for the TIXH604.
2. Derate linearly to 32.5 W at 85°C case temperature at the rate of 0.5 W/°C.
3. Derate linearly to 85°C free-air temperature at the rate of 250 W/°C.

TENTATIVE DATA SHEET

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TYPES T1XH603, T1XH604

POSITIVE, NEGATIVE VOLTAGE REGULATORS

electrical characteristics at 25°C case temperature (unless otherwise noted, see note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Regulation	$I_O = 1 \text{ A}$, $V_I = 7 \text{ V to } 10 \text{ V}$			0.2%	
Ripple Rejection	$I_O = 5 \text{ mA}$, $f = 50 \text{ Hz to } 10 \text{ kHz}$	45	60		dB
Load Regulation	$V_I = 7 \text{ V}$, $I_O = 50 \mu\text{A to } 1 \text{ A}$			0.5%	
Standby Current	$I_O = 0$		20		mA
Average Temperature Coefficient of Output Voltage	$I_O = 1 \text{ A}$, $T_C = 25^\circ\text{C to } 85^\circ\text{C}$		0.1		%/°C
Output Noise Voltage	$I_O = 5 \text{ mA}$, $\text{BW} = 10 \text{ Hz to } 1 \text{ MHz}$		0.5		mV

NOTE 4: See Figure 1. Unless otherwise specified, $V_I = 10 \text{ V}$, $V_O = 5 \text{ V}$.

DEFINITION OF TERMS

Input Regulation The percentage change in the output voltage for a specified change in the input voltage.

$$\text{Input Regulation} = \pm \left[\frac{V_O \text{ at } V_{I(2)} - V_O \text{ at } V_{I(1)}}{V_O \text{ at } V_{I(1)}} \right] 100 \%$$

Ripple Rejection The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Load Regulation The percentage change in the output voltage for a specified change in output current.

$$\text{Load Regulation} = \pm \left[\frac{V_O \text{ at } I_{O(2)} - V_O \text{ at } I_{O(1)}}{V_O \text{ at } I_{O(1)}} \right] 100 \%$$

where $I_{O(1)}$ and $I_{O(2)}$ are the specified low and high current extremes, respectively.

Standby Current The input current to the regulator with no output current and the $V_{(\text{ref})}$ terminal open.

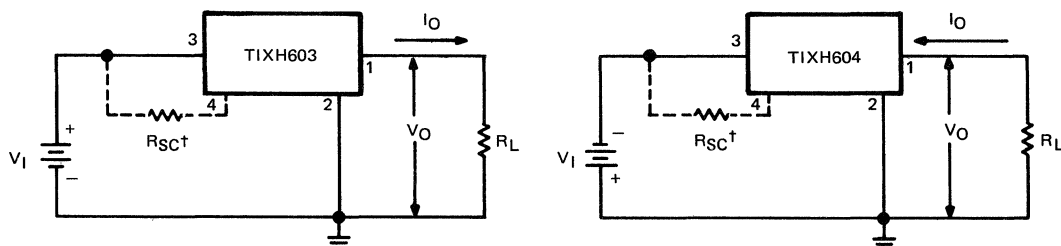
Average Temperature Coefficient of Output Voltage (αV_O) The ratio of the change in output voltage expressed as a percentage to the change in temperature. This is an average value for the specified temperature range.

$$\alpha V_O = \pm \left[\frac{V_O \text{ at } T_{C(2)} - V_O \text{ at } T_{C(1)}}{V_O \text{ at } 25^\circ\text{C}} \right] \frac{100\%}{T_{C(2)} - T_{C(1)}}$$

Output Noise Voltage The rms output noise voltage with a constant load and no input ripple.

9

PARAMETER MEASUREMENT INFORMATION



$\dagger I_O$ can be limited by an external resistor. $R_{SC} \approx \frac{1 \text{ V}}{I_{O(\text{limit})}}$

FIGURE 1

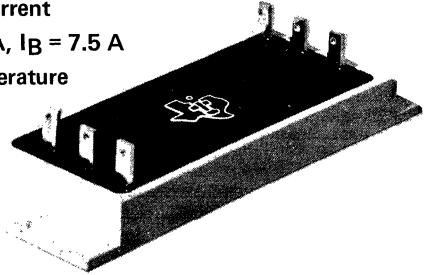
SOLID-STATE POWER FUNCTIONS

TYPE T1XH701 HIGH-CURRENT SWITCH

- 75-A Continuous Collector Current
- $V_{CE(sat)} \leq 1.3 \text{ V}$ at $I_C = 75 \text{ A}$, $I_B = 7.5 \text{ A}$
- 300 Watts at 25°C Case Temperature

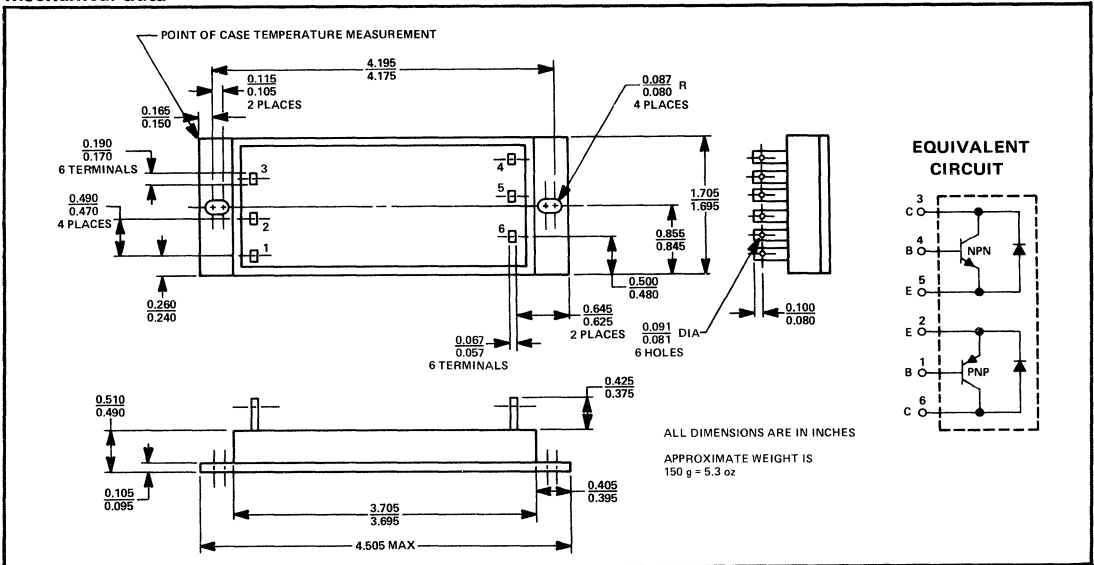
description

The T1XH701 is a high-current complimentary-symmetry power stage which is well suited for use in frequency-regulated inverters or dc-to-dc converters. The commutating diodes are included in the package for operation with inductive loads.



TYPE T1XH701
BULLETIN NO. D.L.S-7111640, DECEMBER 1971

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted, see note 1)

Terminal-to-Case Voltage	±500 V
Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 2)	100 V
Emitter-Base Voltage	5 V
Continuous Collector Current	75 A
Commutating-Diode Peak Current ($t_W \leq 300 \mu s$, See Note 3)	-75 A
Continuous Base Current	10 A
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 1
Continuous Total Package Dissipation at (or below) 25°C Case Temperature (See Note 4)	300 W
Unclamped Inductive Load Energy (See Note 5)	90 mJ
Operating Case and Storage Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 Inch from Case for 5 Seconds	260°C

- NOTES: 1. Throughout this data sheet current and voltage polarities are shown for the n-p-n switch. These are reversed for the p-n-p switch.
 2. This value applies when the base-emitter diode is open-circuited.
 3. This applies to the total collector-terminal current when the collector is at negative potential with respect to the emitter.
 4. Derate linearly to 120 W at 85°C case temperature at the rate of 3 W/°C. Power may be divided between the two switches in any proportion subject to the limitations of the Maximum Safe Operating Area, Figure 1.
 5. This rating is based on the capability of each switch to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. †. $L = 20 \text{ mH}$, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10 \text{ V}$, $V_{BB2} = 0 \text{ V}$, $R_L = 0.2 \Omega$, $V_{CC} = 10 \text{ V}$, $I_{CM} = 3 \text{ A}$. Energy $\approx I_C^2 L/2$.

† This circuit appears on page 5-1 of this data book.

TENTATIVE DATA SHEET

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TYPE T1XH701

HIGH-CURRENT SWITCH

electrical characteristics of each switch at 25°C case temperature (see note 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	100		V
I_{CES}	Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$	3		mA
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	4		mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 75 \text{ A}$, See Notes 6 and 7	10		
V_{BE}	Base-Emitter Voltage	$I_B = 7.5 \text{ A}$, $I_C = 75 \text{ A}$, See Notes 6 and 7	2		V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 7.5 \text{ A}$, $I_C = 75 \text{ A}$, See Notes 6 and 7	1.3		V
V_{ECF}	Commutating-Diode Forward Voltage	$I_C = -75 \text{ A}$, $I_B = 0$, See Notes 6 and 7	1.8		V

- NOTES: 1. Throughout this data sheet current and voltage polarities are shown for the n-p-n switch. These are reversed for the p-n-p switch.
 6. These parameters must be measured using pulse techniques, $t_W = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.2 inch from the device body.

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

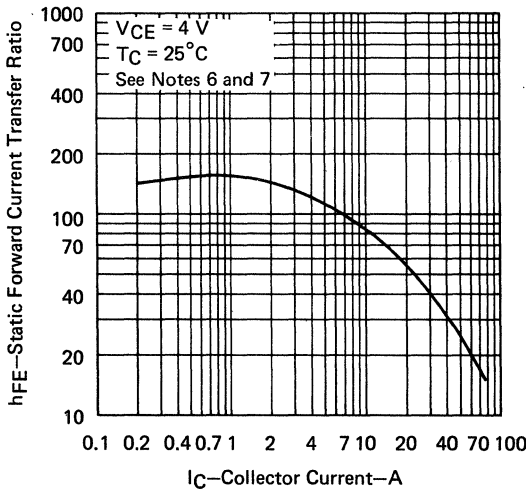


FIGURE 1

MAXIMUM SAFE OPERATING AREA

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

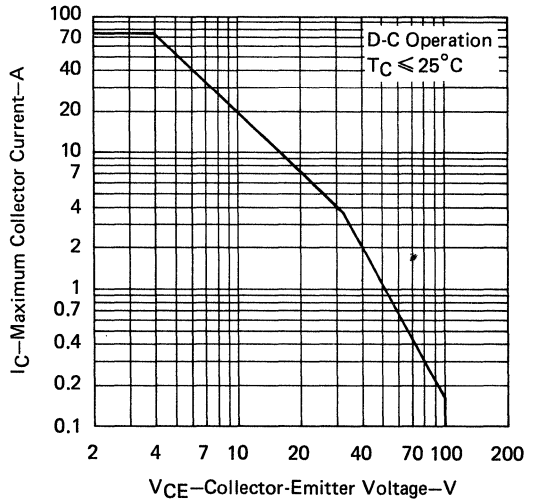


FIGURE 2

SOLID-STATE POWER FUNCTIONS

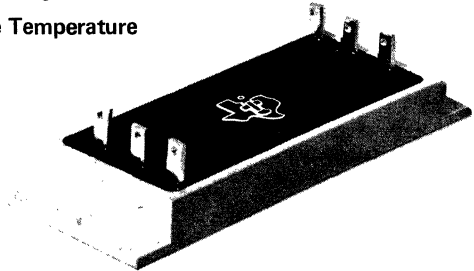
TYPE TIXH702 DUAL HIGH-CURRENT SWITCH

TYPE TIXH702
BULLETIN NO. DL-S-7111652, DECEMBER 1971

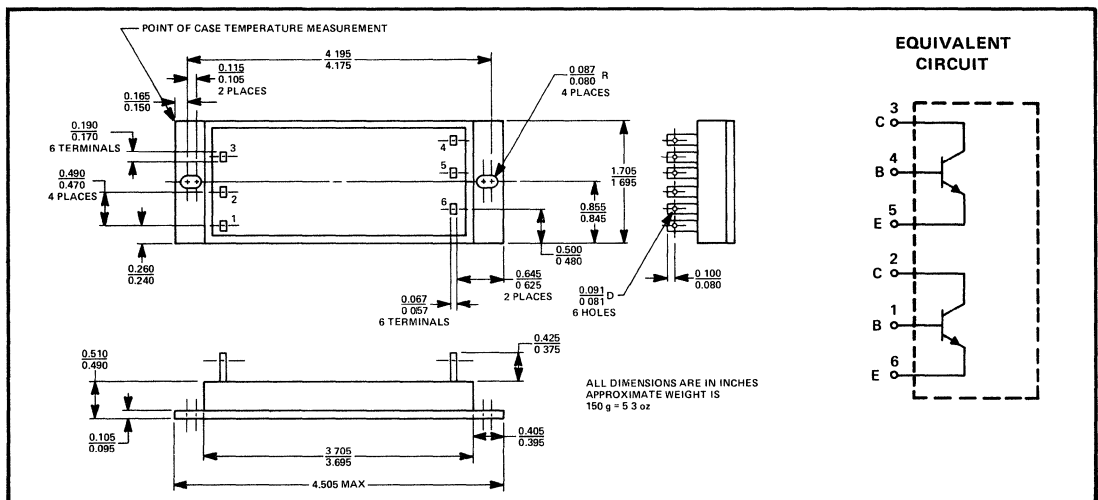
- 25-A Continuous Collector Current
- 400 V Collector-Base Voltage
- 300 Watts at 25°C Case Temperature

description

The TIXH702 is a high-voltage power stage which can be utilized in many types of circuit applications operating from a rectified 115-volt a-c line. Typical examples include motor controls and frequency conversion systems.



mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Terminal-to-Case Voltage	±500 V
Collector-Base Voltage	400 V
Collector-Emitter Voltage (See Note 1)	300 V
Emitter-Base Voltage	5 V
Continuous Collector Current	25 A
Continuous Base Current	10 A
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 2
Continuous Total Package Dissipation at (or below) 25°C Case Temperature (See Note 2)	300 W
Unclamped Inductive Load Energy (See Note 3)	90 mJ
Operating Case and Storage Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 Inch from Case for 5 Seconds	260°C

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. Derate linearly to 120 W at 85°C case temperature at the rate of 3 W/°C. Power may be divided between the two switches in any proportion subject to the limitations of the Maximum Safe Operating Area Curve, Figure 2.
 3. This rating is based on the capability of each switch to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*. † L = 20 mH, R_{BB1} = 20 Ω, R_{BB2} = 100 Ω, V_{BB1} = 10 V, V_{BB2} = 0 V, R_L = 0.2 Ω, V_{CC} = 10 V, I_{CM} = 3 A. Energy ≈ I_C²L/2.

† This circuit appears on page 5-1 of this data book.

TENTATIVE DATA SHEET

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TYPE T1XH702

DUAL HIGH-CURRENT SWITCH

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 1 \text{ mA}$, $I_B = 0$, See Note 4	300		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 400 \text{ V}$, $I_E = 0$		1	mA
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		4	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 5 \text{ V}$, $I_C = 25 \text{ A}$, See Notes 4 and 5	12		
V_{BE}	Base-Emitter Voltage	$I_B = 2.5 \text{ A}$, $I_C = 25 \text{ A}$, See Notes 4 and 5	4		V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 2.5 \text{ A}$, $I_C = 25 \text{ A}$, See Notes 4 and 5	3		V

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

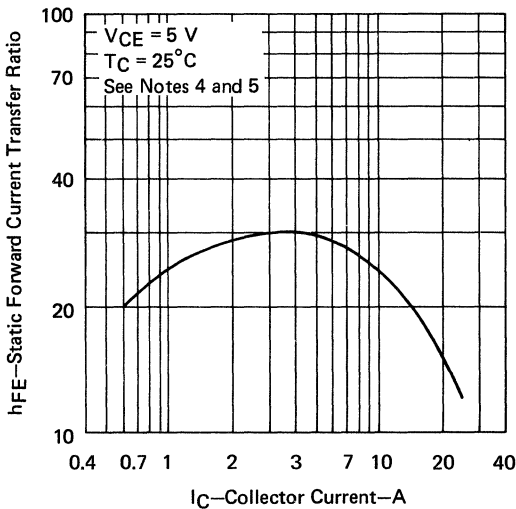


FIGURE 1

MAXIMUM SAFE OPERATING AREA

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

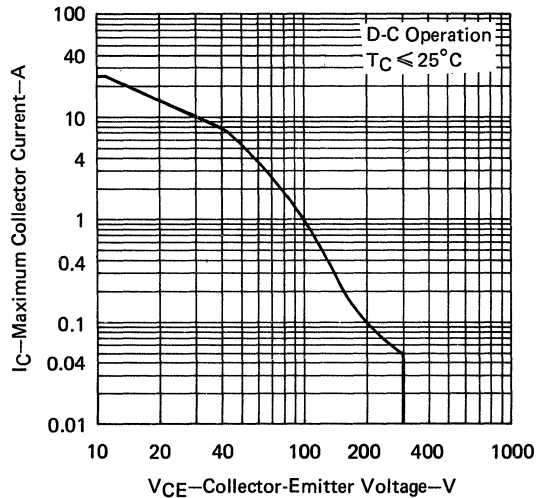


FIGURE 2

- NOTES: 4. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.2 inch from the device body.

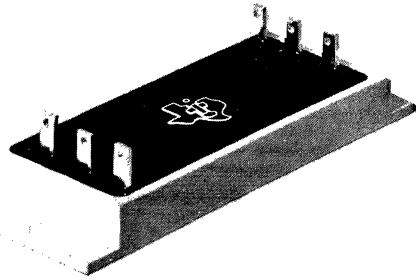
SOLID-STATE POWER FUNCTIONS

TYPE TIXH703 DUAL HIGH-CURRENT SWITCH

- For High-Gain Complementary Push-Pull Stages
- 50-A Continuous Collector Current
- $V_{CE(sat)} \leq 2.5 \text{ V}$ at $I_C = 50 \text{ A}$, $I_B = 0.25 \text{ A}$
- 300 Watts at 25°C Case Temperature

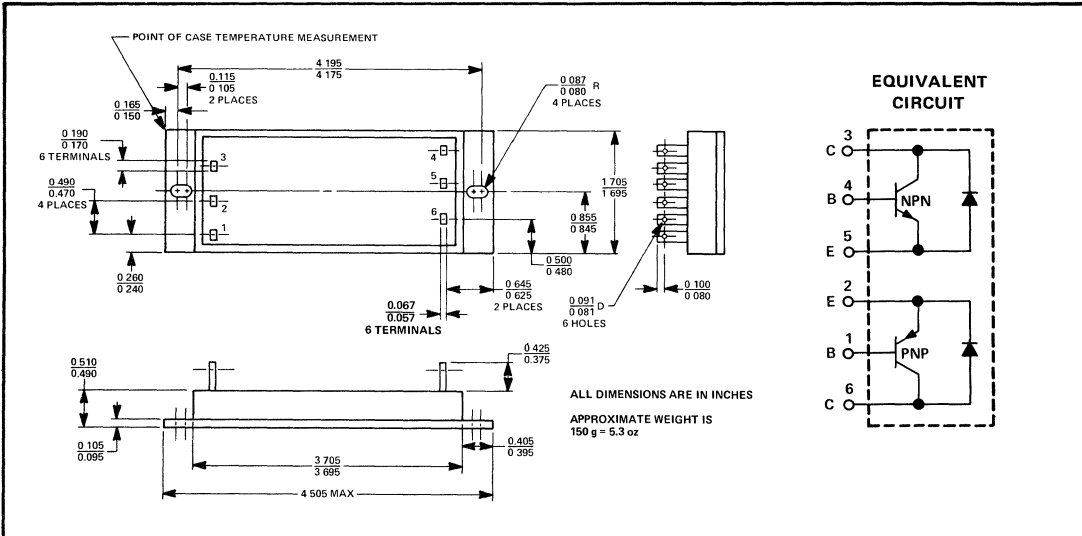
description

The TIXH703 is a high-current complementary-symmetry power stage which features extremely high gain. The low drive-current requirements make this circuit very attractive for linear power applications.



TYPE TIXH703
BULLETIN NO. DL-S-7111656, DECEMBER 1971

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted, see note 1)

Terminal-to-Case Voltage	±500 V
Collector-Base Voltage	100 V
Collector-Emitter Voltage (See Note 2)	100 V
Emitter-Base Voltage	5 V
Continuous Collector Current	50 A
Commutating-Diode Peak Current ($t_w \leq 300 \mu\text{s}$, See Note 3)	50 A
Continuous Base Current	3 A
Safe Operating Area at (or below) 25°C Case Temperature	See Figure 2
Continuous Total Package Dissipation at (or below) 25°C Case Temperature (See Note 4)	300 W
Unclamped Inductive Load Energy (See Note 5)	90 mJ
Operating Case and Storage Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 Inch from Case for 5 Seconds	260°C

- NOTES: 1. Throughout this data sheet current and voltage polarities are shown for the n-p-n portion. These are reversed for the p-n-p portion.
2. This value applies when the base-emitter diode is open-circuited.
3. This applies to the total collector-terminal current when the collector is at negative potential with respect to the emitter.
4. Derate linearly to 120 W at 85°C case temperature at the rate of 3 W/°C. Power may be divided between the two switches in any proportion subject to the limitations of the Maximum Safe Operating Area, Figure 2.
5. This rating is based on the capability of each switch to operate safely in the unclamped-inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*.[†] $L = 20 \text{ mH}$, $R_{BB1} = 20 \Omega$, $R_{BB2} = 100 \Omega$, $V_{BB1} = 10 \text{ V}$, $V_{BB2} = 0 \text{ V}$, $R_L = 0.2 \Omega$, $V_{CC} = 10 \text{ V}$, $I_{CM} = 3 \text{ A}$. Energy $\approx I_C^2 L/2$.

[†]This circuit appears on page 5-1 of this data book.

TENTATIVE DATA SHEET

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TYPE TIXH703

DUAL HIGH-CURRENT SWITCH

electrical characteristics at 25°C case temperature (see note 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V(BR)CEO	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, $I_B = 0$, See Note 6	100		V
I _{CES}	Collector Cutoff Current	$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$		1	mA
I _{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$		10	mA
h _{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, $I_C = 50 \text{ A}$, See Notes 6 and 7	1000		
V _{BE}	Base-Emitter Voltage	$I_B = 0.25 \text{ A}$, $I_C = 50 \text{ A}$, See Notes 6 and 7		3	V
V _{CE(sat)}	Collector-Emitter Saturation Voltage	$I_B = 0.25 \text{ A}$, $I_C = 50 \text{ A}$, See Notes 6 and 7		2.5	V
V _{ECF}	Commutating-Diode Forward Voltage	$I_C = -50 \text{ A}$, $I_B = 0$, See Notes 6 and 7		1.8	V

- NOTES: 1. Throughout this data sheet current and voltage polarities are shown for the n-p-n portion. These are reversed for the p-n-p portion.
 6. These parameters must be measured using pulse techniques. $t_W = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.2 inch from the device body.

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

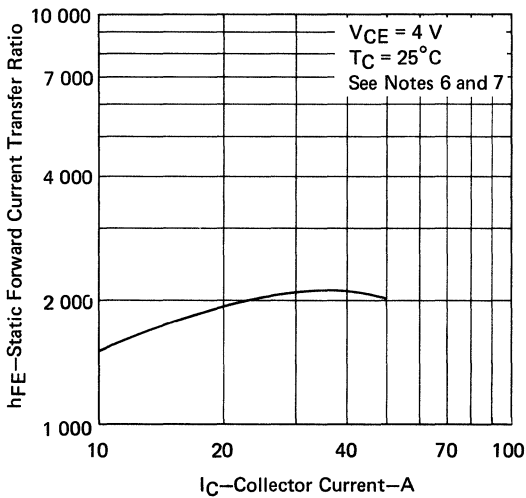


FIGURE 1

MAXIMUM SAFE OPERATING AREA

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

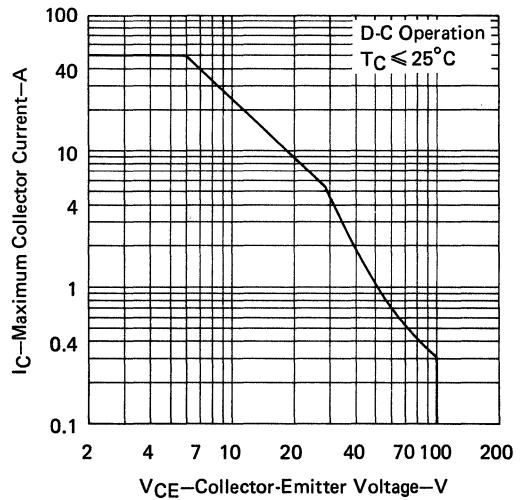


FIGURE 2

SOLID-STATE POWER FUNCTIONS

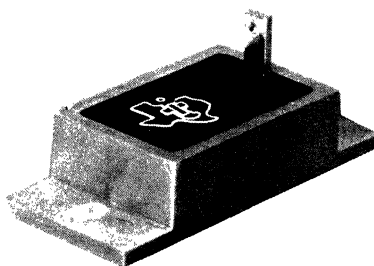
TYPE T1XH704 TRANSIENT VOLTAGE PROTECTOR

TYPE T1XH704
BULLETIN NO. DL-S-7111657, DECEMBER 1971

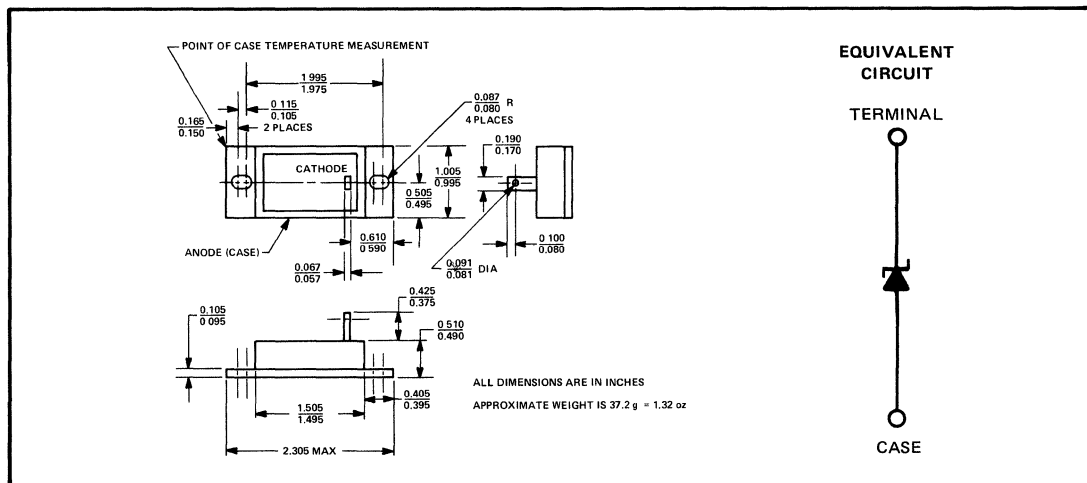
- Typical Dynamic Impedance . . . 0.1 Ω
- Clamp Voltage . . . 23 V
- Peak Reverse Current . . . 40 A

description

The T1XH704 is designed to suppress voltage transients having a high energy content. In case of a severe transient, the T1XH704 will short circuit thereby tripping the system's circuit breaker or blowing the fuse while still protecting the entire system.



mechanical data



absolute maximum ratings over operating temperature range (unless otherwise noted)

Continuous Forward Current	4 A
Continuous Reverse Current	2 A
Peak Forward Current (One 60-Hz Half Sine Wave)	10 A
Peak Reverse Current (One 60-Hz Half Sine Wave)	40 A
Average Power Dissipation at (or below) 85°C Case Temperature (See Note 1)	40 W
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	2.4 W
Operating Case Temperature Range	-25°C to 85°C
Storage Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 Inch from Case for 5 Seconds	260°C

NOTES: 1. This value applies for a maximum averaging time of 150 ms.
2. Derate linearly to 85°C free-air temperature at the rate of 40 mW/°C.

9

TYPE TIXH704 TRANSIENT VOLTAGE PROTECTOR

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	V_Z Regulator Voltage	$I_Z = 20 \text{ mA}$	See Figure 1	20	23	25
$I_Z = 35 \text{ A}$					30	V
I_R Reverse Current	$V_R = 18 \text{ V}$				0.1	mA
V_F Forward Voltage	$I_F = 1 \text{ A}$			2		V

PARAMETER MEASUREMENT INFORMATION

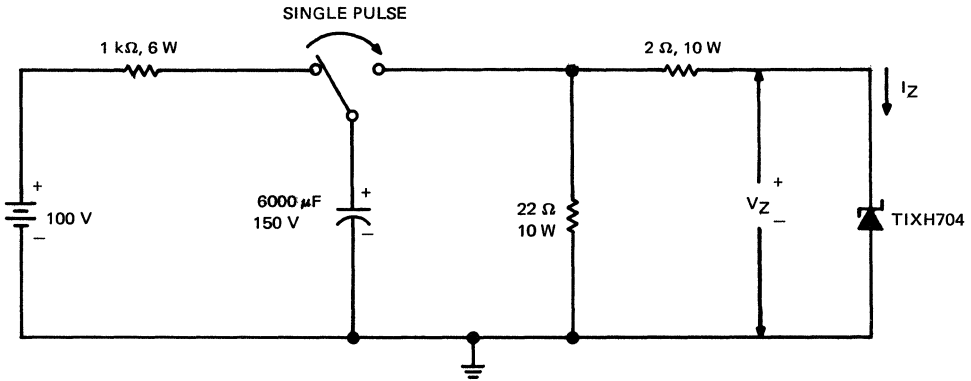


FIGURE 1

SOLID-STATE POWER FUNCTIONS

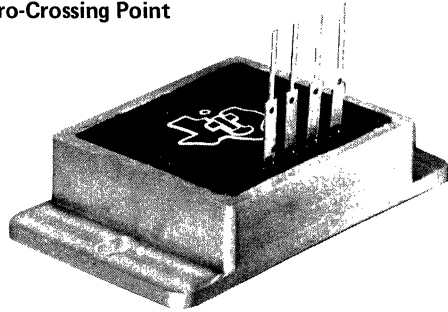
TYPES TIXH801, TIXH802 AC RELAYS

TYPES TIXH801, TIXH802
BULLETIN NO. DL-S-7111668, DECEMBER 1971

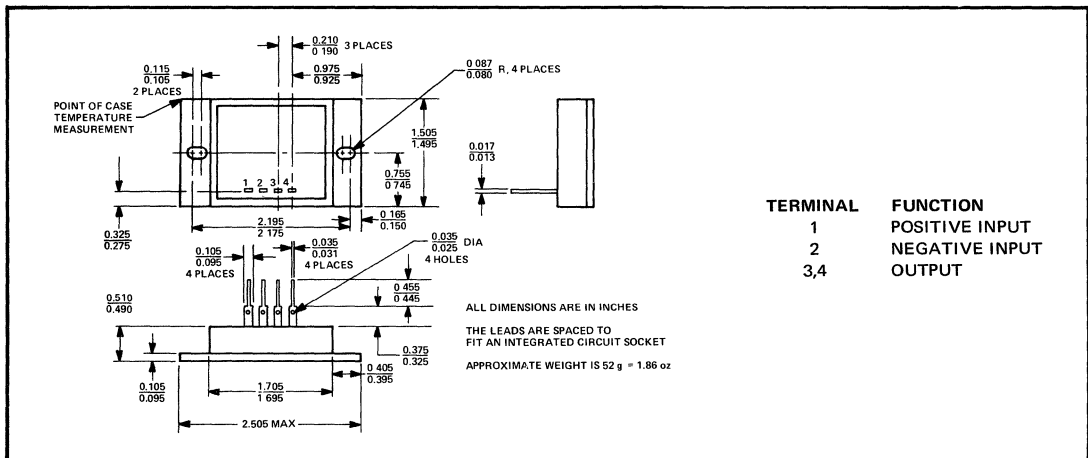
- SPST (Normally Open)
- 8 A, 200 V (TIXH801)
25 A, 200 V (TIXH802)
- Optically-Coupled Isolation between Control and Load Circuits
- Turn-On Only at a Line Voltage Zero-Crossing Point

description

The TIXH801 and TIXH802 a-c relays can be driven directly by standard DTL or TTL integrated circuits. They provide optically-coupled isolation between control circuitry and the power system. Zero-voltage switching minimizes RFI generated during load current turn-on. Absence of electro-mechanical components provides higher speed and eliminates contact wear and arcing.



mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

	TIXH801	TIXH802
Input Diode Reverse Voltage	← 3 V →	
Repetitive Peak Off-State Output Voltage	← ±200 V →	
Input-to-Output Voltage	← ±600 V →	
Terminal-to-Case Voltage	← ±600 V →	
Input Diode Continuous Forward Current at (or below) 25°C Case Temperature (See Note 1)	60 mA	60 mA
Full-Cycle RMS On-State Current at (or below) 85°C Case Temperature	8 A	25 A
Peak On-State Surge Current (See Note 2)	±80 A	±175 A
Operating Case Temperature Range	-25°C to 85°C	
Storage Temperature Range	-25°C to 85°C	
Terminal Temperature 1/8 Inch from Case for 5 Seconds	← 260°C →	

NOTES: 1. Derate linearly to 85°C case temperature at the rate of 1 mA/°C.

2. These values apply for one 60-Hz full sine wave when the device is operating at (or below) the rated value of on-state current. Surge may be repeated after 100 ms.

TENTATIVE DATA SHEET

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TYPES TIXH801, TIXH802

AC RELAYS

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TIXH801			TIXH802			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
$V_{I(off)}$	Input Voltage for Output in Off-State	0.4			0.4			V	
$I_{I(on)}$	Input Current for Output in On-State			10			10	mA	
V_I	Input Voltage	$I_I = 10 \text{ mA}$			1.2	1.5	1.2	1.5	V
I_{DRM}	Repetitive Peak Off-State Current	$V_I = 0.4 \text{ V}, V_O = \pm 200 \text{ V}$			± 3.5			± 5	mA
V_T	Output Voltage at Turn-On	See Figure 1			± 10			± 10	V
V_{TM}	Peak On-State Output Voltage	$I_I = 10 \text{ mA}, I_{TM} = \pm 12 \text{ A}$		See Note 3	± 2.5			± 2.5	V
		$I_I = 10 \text{ mA}, I_{TM} = \pm 25 \text{ A}$							
dv/dt	Critical Rate of Rise of Off-State Voltage (Exponential)	$V_{DRM} = \pm 200 \text{ V}, V_I = 0, T_C = 85^\circ \text{ C}$			500			500	V/ μs
R_{in-out}	Isolation, Input-to-Output	$V_{in-out} = \pm 1 \text{ kV}, \text{ See Note 4}$			$> 10^9$			$> 10^9$	Ω
C_{in-out}	Capacitance, Input-to-Output	$V_{in-out} = 0 \text{ V}, f = 1 \text{ MHz}, \text{ See Note 4}$			30			30	pF

- NOTES: 3. This parameter is measured using voltage-sensing contacts separate from the current-carrying contacts and located within 0.2 inch from the device body.
 4. This parameter is measured between both input terminals shorted together and both output terminals shorted together.

PARAMETER MEASUREMENT INFORMATION

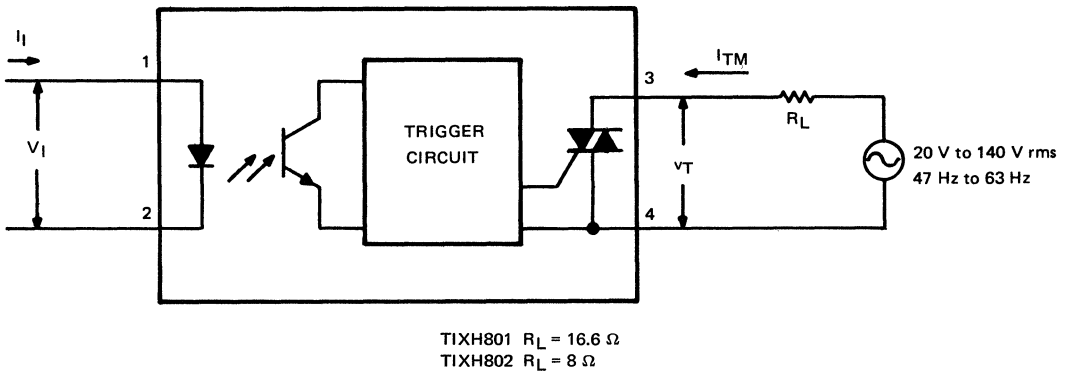


FIGURE 1

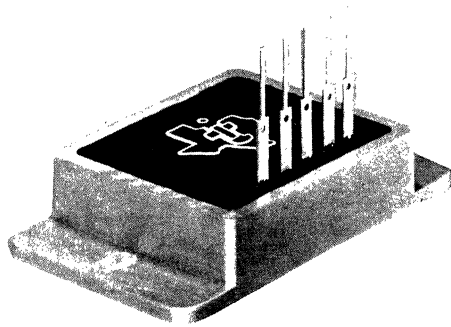
SOLID-STATE POWER FUNCTIONS

TYPES TIXH803, TIXH804 POSITIVE-GROUND AND NEGATIVE-GROUND DC RELAYS

- SPST (Normally Open) 80 V, 10 A
- Optical Isolation between Control and Load Circuit
- Short-Circuit Protected

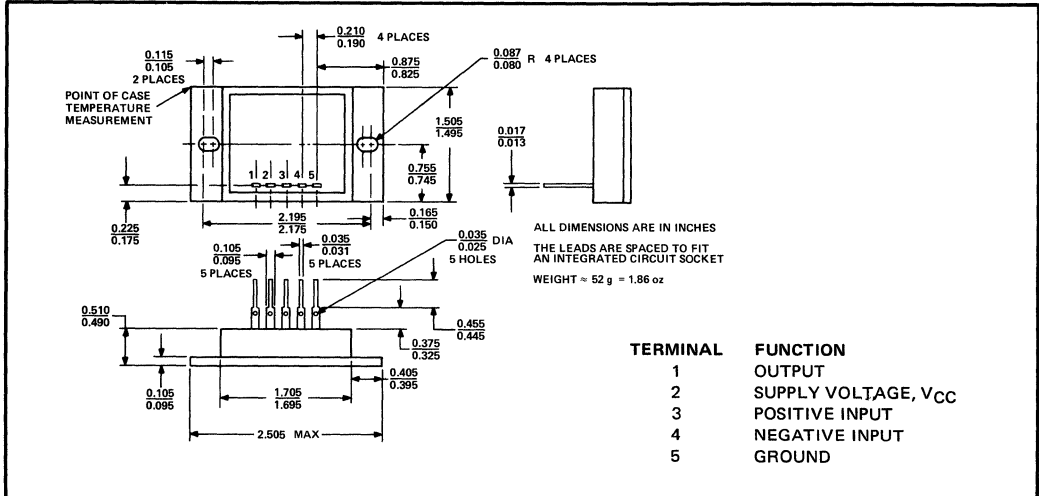
description

The TIXH803 and TIXH804 are designed to be driven directly from standard DTL and TTL integrated circuits. These relays provide isolation between control circuitry and power systems. The output may be short-circuited to ground without damage to the relay. The relay automatically senses the short circuit, shuts off, and resets on the next input pulse after the short is removed. The TIXH803 is designed for use in negative-ground systems; the TIXH804 in positive-ground systems.



TYPES TIXH803, TIXH804
BULLETIN NO. DLS-7111651, DECEMBER 1971

mechanical data



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Input-to-Output Voltage	±500 V
Terminal-to-Case Voltage	±500 V
Supply Voltage, V _{CC}	80 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current at (or below) 25°C Case Temperature (See Note 1)	60 mA
Continuous On-State Output Current at (or below) 85°C Case Temperature	10 A
Inductive Energy during Turn-Off (See Note 2)	100 mJ
Operating Case Temperature Range	-25°C to 85°C
Storage Temperature Range	-25°C to 85°C
Terminal Temperature 1/8 Inch from Case for 5 Seconds	260°C

- NOTES: 1. Derate linearly to 85°C case temperature at the rate of 1 mA/°C.
2. This rating is based on the capability of the relays to turn off a load of 0.2 Ω and 20 mH operating from a supply voltage of 10 V at a current of 3.2 A.

recommended operating conditions

	MIN	MAX	UNIT
Supply Voltage, V _{CC}	10	50	V
Operating Case Temperature, T _C	-25	85	°C

TENTATIVE DATA SHEET

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TYPES TIXH803, TIXH804 POSITIVE-GROUND AND NEGATIVE-GROUND DC RELAYS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(off)}$ Maximum Input Voltage for Output Off		0.4			V
$I_{I(on)}$ Minimum Input Current for Output On			10		mA
V_I Input Voltage	$I_I = 10 \text{ mA}$		1.2	1.5	V
$I_{O(off)}$ Off-State Output Current	$V_I = 0.4 \text{ V}, V_{CC} = 80 \text{ V}, R_L = 10 \text{ k}\Omega$			1	mA
$V_{CC}-V_O$ Relay Voltage Drop	$V_{CC} = 10 \text{ V}, I_I = 10 \text{ mA}, I_O = 10 \text{ A},$ See Note 3			2.5	V
$I_{CC(off)}$ Standby Supply Current	$V_I = 0, V_{CC} = 80 \text{ V}, R_L = \infty$			10	mA
$I_{CC(on)}$ On-State Supply Current	$I_I = 10 \text{ mA}, V_{CC} = 80 \text{ V}, R_L = \infty$		20		mA
R_{in-out} Isolation, Input-to-Output	$V_{in-out} = \pm 1 \text{ kV}$ See Note 4		10^{11}		Ω
C_{in-out} Capacitance, Input-to-Output	$V_{in-out} = \pm 1 \text{ kV},$ See Note 4 $f = 1 \text{ MHz}$		1		pF

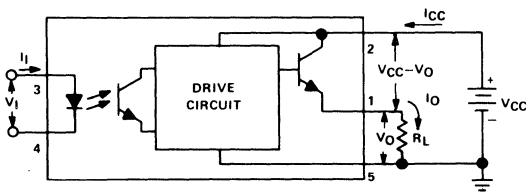
NOTES: 3. This parameter is measured using voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inches from the device body.

4. These parameters are measured between both input terminals shorted together and the output.

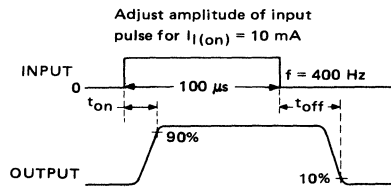
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TYPICAL	UNIT
t_{on} Turn-On Time	$V_{CC} = 80 \text{ V}, R_L = 8 \Omega, I_{I(on)} = 10 \text{ mA},$	1.5	μs
t_{off} Turn-Off Time	See Figure 1	35	

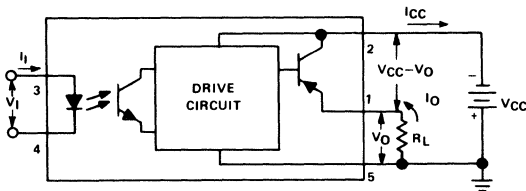
PARAMETER MEASUREMENT INFORMATION



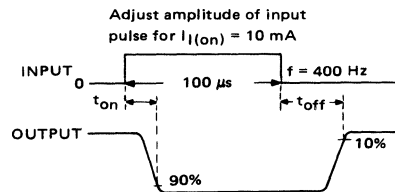
TIXH803 TEST CIRCUIT



TIXH803 VOLTAGE WAVEFORM



TIXH804 TEST CIRCUIT



TIXH804 VOLTAGE WAVEFORM

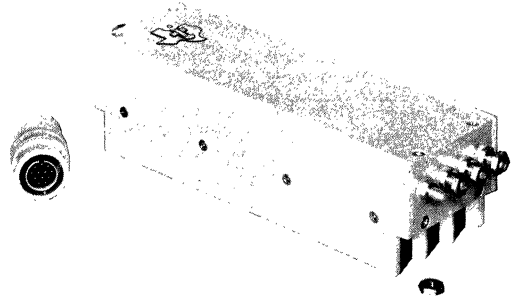
FIGURE 1—SWITCHING TIMES

SOLID-STATE POWER FUNCTIONS

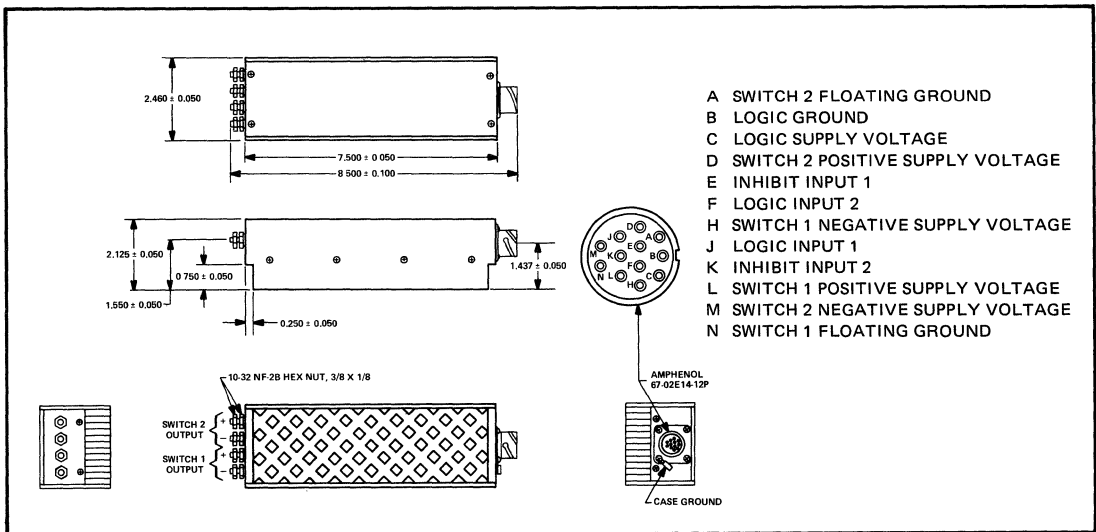
TYPE TIXH805 HYBRID SWITCH

TYPE TIXH805
BULLETIN NO. DL-S-7111659, DECEMBER 1971

- 200 A, 100 V
- Protected Against:
 - Short-Circuit Load
 - Overheating
- Operating Frequency . . . DC to 4 kHz



mechanical data



9

description

The TIXH805 hybrid switch is designed for precision power conversion equipment. The inputs can be driven by standard DTL and TTL integrated circuits. The TIXH805 contains two switches which may be connected together for a single push-pull output, or may be operated as two independent switches. It features optically coupled isolation between input circuitry and power system. Internal circuitry turns off each switch within approximately 10 microseconds if its load is short-circuited. To ensure that the total current (operating and surge) does not exceed 250 amperes within this time, the turn-on di/dt of the load current must be limited to 5 A/μs. Approximately 25 milliseconds after turn-off caused by a short-circuit, the switch becomes operational again. Should the short-circuit still exist, the switch will turn off again and recycle at a frequency of approximately 40 hertz until the short-circuit condition is removed. Protection is also provided against overheating. The signal for this condition is fed into a Schmitt trigger, which, because of its hysteresis, ensures that the temperature recovers by a safe margin before operation resumes.

TENTATIVE DATA SHEET

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TYPE TIXH805 HYBRID SWITCH

description (continued)

For operation in the push-pull mode, the logic and inhibit inputs of each side of the circuit are connected together. This provides inhibit and blanking functions. A high level at either inhibit input holds the switch of the opposite side off without regard to the logic input. If both inhibit inputs are high, both switches are off thus avoiding "line shoot-through". A rising transition at an inhibit input blanks or delays the corresponding switch from turning on for approximately five microseconds. This gives the switch that is on sufficient time to turn off before the other switch can turn on. For additional information on operation in the push-pull mode, see the typical application data section of this data sheet.

FUNCTION TABLE
logic input 1 connected to inhibit input 1
logic input 2 connected to inhibit input 2

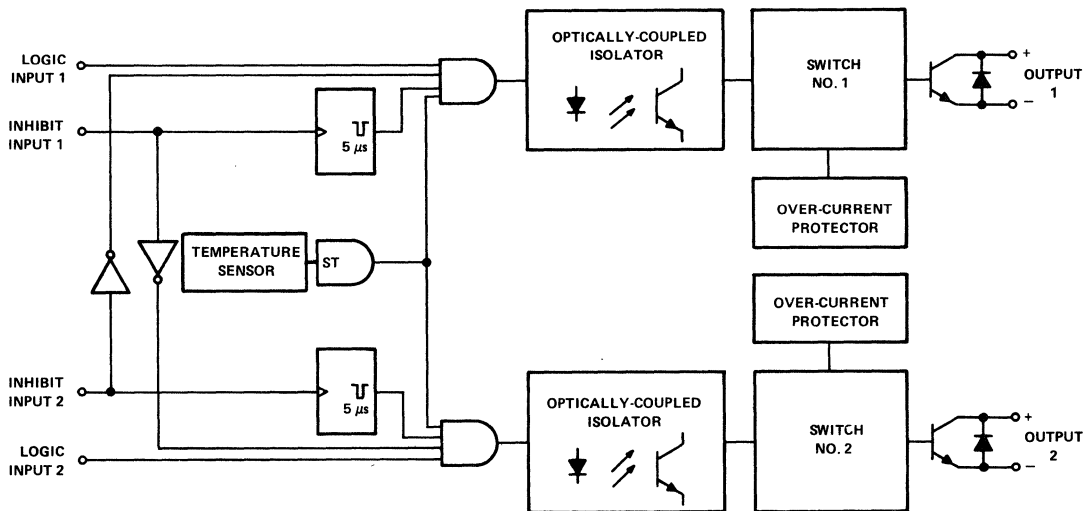
INPUT 1	INPUT 2	SWITCH 1	SWITCH 2
L	L	off	off
H	L	on	off
L	H	off	on
H	H	off	off

H = high level, L = low level

For operation as two independent power switches, both inhibit inputs are connected to logic ground. A high level at a logic input turns that switch on; a low level turns it off. Inhibit and blocking functions are not used since they are not needed for independent operation.

The hybrid switch enables construction of high-power-density, lightweight power-conversion equipment by eliminating large commutation capacitors necessary for SCR circuits. Due to the fast switching speed, a considerable weight decrease in filters can be achieved. The major applications for this device are dc-to-variable-ac inverters, switching regulators, and d-c choppers.

functional block diagram



▷ . . . Dynamic input activated by a transition from a low level to a high level.

TYPE TIXH805 HYBRID SWITCH

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Logic Supply Voltage (See Note 1)	5.6 V
Positive Supply Voltage, Each Switch (See Note 2)	5.6 V
Negative Supply Voltage, Each Switch (See Note 2)	-5.6 V
Logic and Inhibit Input Voltages (See Note 1)	5 V
Output Voltage (See Note 3)	100 V
Peak Operating Output Current (See Note 4)	200 A
Rate of Rise of Output Current	5 A/ μ s
Average Power Dissipation at (or below) 25°C Case Temperature (See Note 5)	500 W
Operating Case Temperature Range	-40°C to 85°C
Storage Temperature Range	-40°C to 85°C

- NOTES: 1. These voltages are with respect to the logic ground terminal.
 2. Supply voltages for each switch are with respect to the floating ground terminal of that switch.
 3. Output voltages are at the positive output terminal with respect to the negative output terminal of each switch.
 4. For pulses narrower than 1 ms derate according to Figure 3. For pulses wider than 1 ms the output current should be limited to 120 A.
 5. Derate linearly to 140 W at 85°C case temperature at the rate of 6 W/°C. This value applies for a maximum averaging time of 1 second.

recommended operating conditions

	MIN	MAX	UNIT
Logic Supply Voltage, V_{CC}	5	5.6	V
Positive Supply Voltage, Each Switch, V_{S+}	5	5.6	V
Negative Supply Voltage, Each Switch, V_{S-}	-5	-5.6	V
Operating Case Temperature Range	-40	85	°C

electrical characteristics at 25°C case temperature (unless otherwise noted, see figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-Level Input Voltage		2		V
V_{IL}	Low-Level Input Voltage			0.8	V
I_I	Input Current at Maximum Input Voltage	Logic Inputs	$V_I = 5$ V	1	mA
		Inhibit Inputs		2	
I_{IH}	High-Level Input Current	Logic Inputs	$V_I = 2.4$ V	50	μ A
		Inhibit Inputs		80	
I_{IL}	Low-Level Input Current	Logic Inputs	$V_I = 0.4$ V	-2	mA
		Inhibit Inputs		-3.2	
$I_{O(off)}$	Off-State Output Current	$V_I = 0.8$ V, $V_O = 100$ V, $T_C = 85^\circ$ C		10	mA
$V_{OM(on)}$	Peak On-State Voltage	$V_I = 2$ V, $I_{OM} = 200$ A, $f = 400$ Hz, $t_w = 100$ μ s		2.6	V
I_{CC}	Logic Supply Current	$V_{CC} = 5.5$ V		0.2	A
I_{SM+}	Peak Positive Supply Current, Either Switch	$V_{S+} = 5.5$ V		15	A
$I_{S(AV)-}$	Average Negative Supply Current, Either Switch	$V_{S-} = -5.5$ V		-3	A

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta CA}$	Case-to-Ambient Thermal Resistance	Free-Air			1	°C/W
		Forced-Air Cooling, 35 ft ³ /min, 50 lb/in ²			0.2	
τ_C	Thermal Time Constant of Case			8		min

9

TYPE T1XH805 HYBRID SWITCH

PARAMETER MEASUREMENT INFORMATION

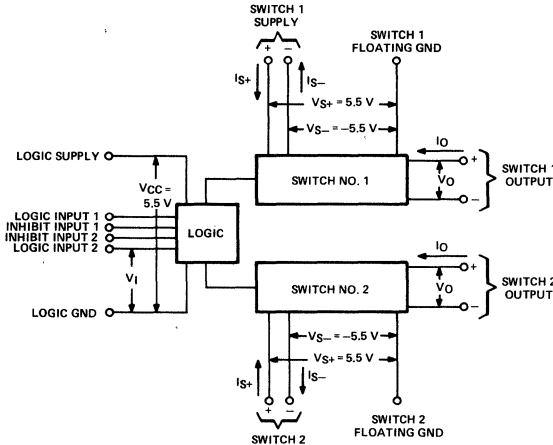
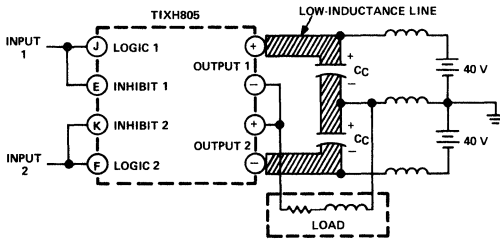


FIGURE 1

TYPICAL APPLICATION DATA

push-pull configuration

The switches are able to turn off current with a di/dt of $60 \text{ A}/\mu\text{s}$. This results in high voltage spikes with peaks equal to $L \cdot di/dt$ with very small values of line inductance. Therefore, the line connecting the commutating capacitors (C_C) must have an inductance less than $0.05 \mu\text{H}$, whereas the load inductance can be fairly high.



The commutating capacitors should be selected according to:

$$C_C = \frac{1}{10 \text{ V}} \int i_{com} dt$$

NOTE: i_{com} is the commutated current which charges the commutation capacitor an additional 10 V over the steady-state voltage.

Because of the voltage spikes during commutation, the supply voltages have to be smaller than 50 volts so that the peak voltage during switching does not exceed 100 volts.

FIGURE 2

THERMAL INFORMATION

MAXIMUM OUTPUT CURRENT vs DUTY CYCLE

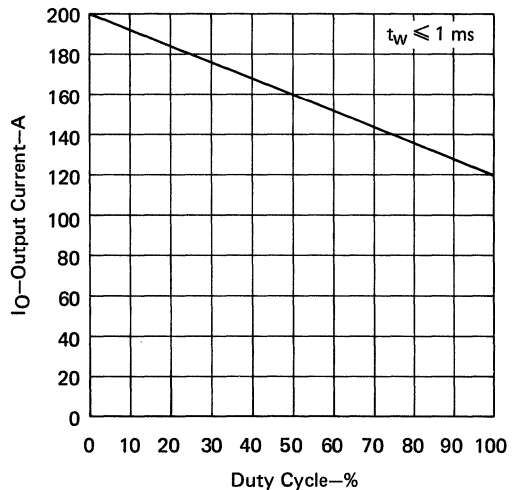


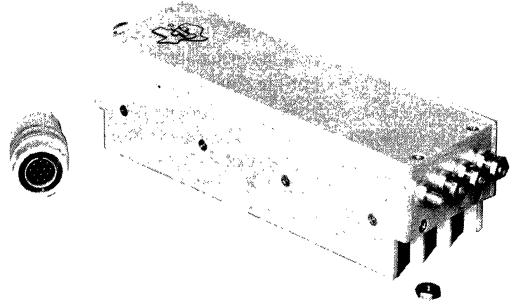
FIGURE 3

SOLID-STATE POWER FUNCTIONS

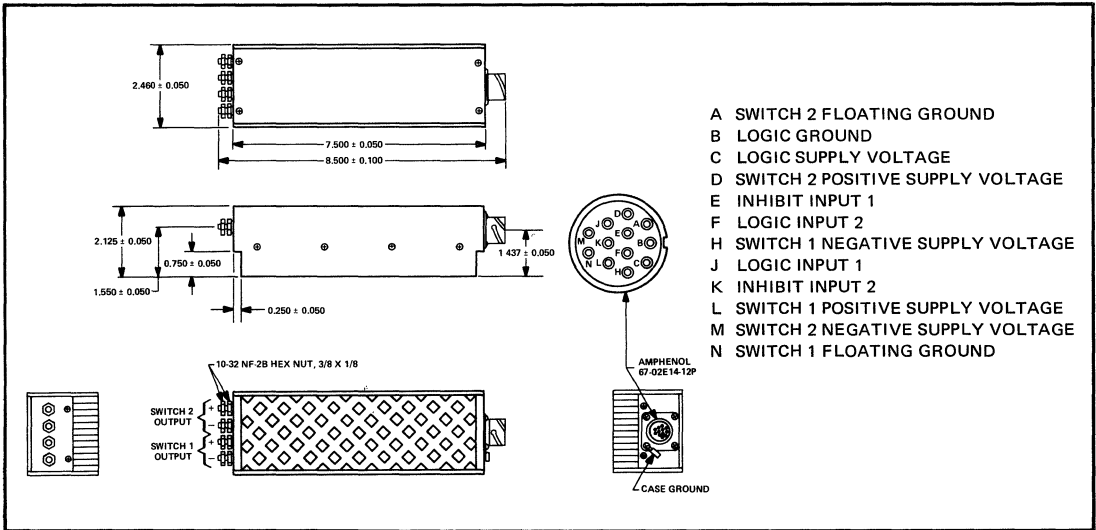
TYPE TIXH806 HYBRID SWITCH

TYPE TIXH806
BULLETIN NO. DL-S-7111660, DECEMBER 1971

- 60 A, 400 V
- Protected Against:
 - Short-Circuit Load
 - Overheating
- Operating Frequency . . . DC to 4 kHz



mechanical data



description

The TIXH806 hybrid switch is designed for precision power conversion equipment operated from rectified and roughly filtered 115-volt a-c lines. The inputs can be driven by standard DTL and TTL integrated circuits. The TIXH806 contains two switches which may be connected together for a single push-pull output, or may be operated as two independent switches. It features optically coupled isolation between input circuitry and power system. Internal circuitry turns off each switch within approximately 10 microseconds if its load is short-circuited. To ensure that the total current (operating and surge) does not exceed 110 amperes within this time, the turn-on di/dt of the load current must be limited to 10 A/ μ s. Approximately 25 milliseconds after turn-off caused by a short-circuit, the switch becomes operational again. Should the short-circuit still exist, the switch will turn off again and recycle at a frequency of approximately 40 hertz until the short-circuit condition is removed. Protection is also provided against overheating. The signal for this condition is fed into a Schmitt trigger, which, because of its hysteresis, ensures that the temperature recovers by a safe margin before operation resumes.

TENTATIVE DATA SHEET

This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE TIXH806 HYBRID SWITCH

description (continued)

For operation in the push-pull mode, the logic and inhibit inputs of each side of the circuit are connected together. This provides inhibit and blanking functions. A high level at either inhibit input holds the switch of the opposite side off without regard to the logic input. If both inhibit inputs are high, both switches are off thus avoiding "line shoot-through". A rising transition at an inhibit input blanks or delays the corresponding switch from turning on for approximately five microseconds. This gives the switch that is on sufficient time to turn off before the other switch can turn on. For additional information on operation in the push-pull mode, see the typical application data section of this data sheet.

FUNCTION TABLE

logic input 1 connected to inhibit input 1
logic input 2 connected to inhibit input 2

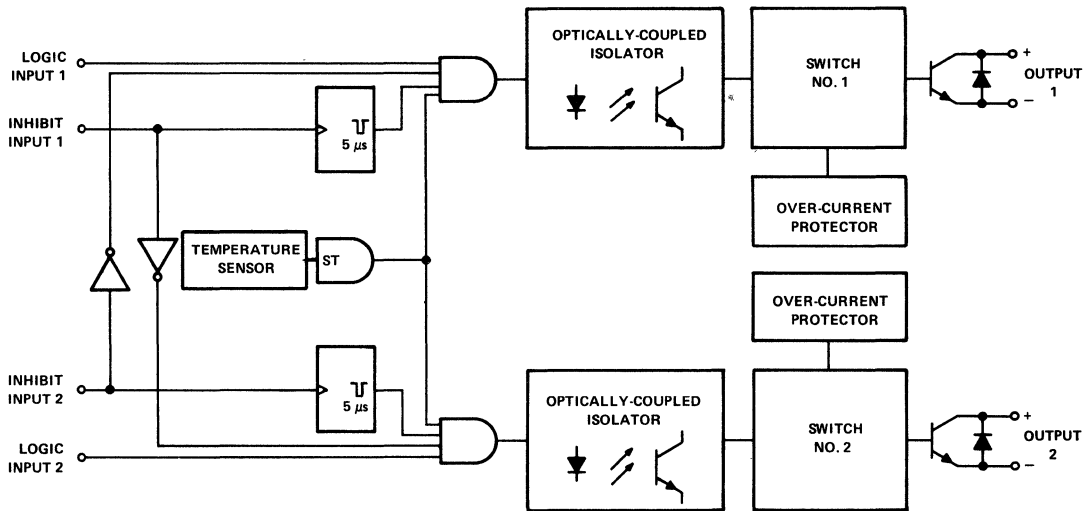
INPUT 1	INPUT 2	SWITCH 1	SWITCH 2
L	L	off	off
H	L	on	off
L	H	off	on
H	H	off	off

H = high level, L = low level

For operation as two independent power switches, both inhibit inputs are connected to logic ground. A high level at a logic input turns that switch on; a low level turns it off. Inhibit and blocking functions are not used since they are not needed for independent operation.

The hybrid switch enables construction of high-power-density, lightweight power-conversion equipment by eliminating large commutation capacitors necessary for SCR circuits. Due to the fast switching speed, a considerable weight decrease in filters can be achieved. The major applications for this device are dc-to-variable-ac inverters, switching regulators, and d-c choppers.

functional block diagram



Dynamic input activated by a transition from a low level to a high level.

TYPE T1XH806 HYBRID SWITCH

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Logic Supply Voltage (See Note 1)	5.6 V
Positive Supply Voltage, Each Switch (See Note 2)	5.6 V
Negative Supply Voltage, Each Switch (See Note 2)	-5.6 V
Logic and Inhibit Input Voltages (See Note 1)	5 V
Output Voltage (See Note 3)	400 V
Peak Output Current (See Note 4)	60 A
Rate of Rise of Output Current	5 A/ μ s
Average Power Dissipation at (or below) 25°C Case Temperature (See Note 5)	500 W
Operating Case Temperature Range	-40°C to 85°C
Storage Temperature Range	-40°C to 85°C

- NOTES: 1. These voltages are with respect to the logic ground terminal.
 2. Supply voltages for each switch are with respect to the floating ground terminal of that switch.
 3. Output voltages are at the positive output terminal with respect to the negative output terminal of each switch.
 4. For pulses narrower than 1 ms derate according to Figure 3. For pulses wider than 1 ms the output current should be limited to 35 A.
 5. Derate linearly to 140 W at 85°C case temperature at the rate of 6 W/°C. This value applies for a maximum averaging time of 1 second.

recommended operating conditions

	MIN	MAX	UNIT
Logic Supply Voltage, V_{CC}	5	5.6	V
Positive Supply Voltage, Each Switch, V_{S+}	5	5.6	V
Negative Supply Voltage, Each Switch, V_{S-}	-5	-5.6	V
Operating Case Temperature Range	-40	85	°C

electrical characteristics at 25°C case temperature (unless otherwise noted, see figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-Level Input Voltage		2		V
V_{IL}	Low-Level Input Voltage			0.8	V
I_I	Input Current at Maximum Input Voltage	Logic Inputs	$V_I = 5\text{ V}$	1	mA
		Inhibit Inputs		2	
I_{IH}	High-Level Input Current	Logic Inputs	$V_I = 2.4\text{ V}$	50	μ A
		Inhibit Inputs		80	
I_{IL}	Low-Level Input Current	Logic Inputs	$V_I = 0.4\text{ V}$	-2	mA
		Inhibit Inputs		-3.2	
$I_{O(off)}$	Off-State Output Current	$V_I = 0.8\text{ V}$, $V_O = 400\text{ V}$, $T_C = 85^\circ\text{C}$		10	mA
$V_{OM(on)}$	Peak On-State Voltage	$V_I = 2\text{ V}$, $I_{OM} = 60\text{ A}$, $f = 400\text{ Hz}$, $t_W = 100\ \mu\text{s}$		2.6	V
I_{CC}	Logic Supply Current	$V_{CC} = 5.5\text{ V}$		0.2	A
I_{SM+}	Peak Positive Supply Current, Either Switch	$V_{S+} = 5.5\text{ V}$		2	A
$I_{S(AV)-}$	Average Negative Supply Current, Either Switch	$V_{S-} = -5.5\text{ V}$		-1	A

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta CA}$	Case-to-Ambient Thermal Resistance	Free-Air			1	°C/W
		Forced-Air Cooling, 35 ft ³ /min, 50 lb/in ²			0.2	
τ_C	Thermal Time Constant of Case			8		min

TYPE TIxH806 HYBRID SWITCH

PARAMETER MEASUREMENT INFORMATION

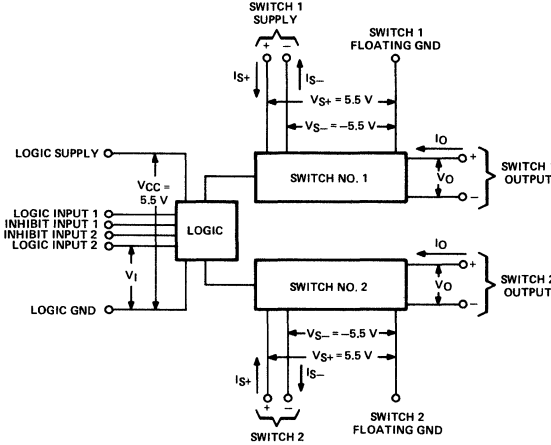
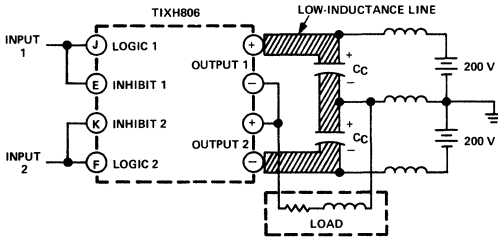


FIGURE 1

TYPICAL APPLICATION DATA

push-pull configuration

The switches are able to turn off current with a di/dt of $60 \text{ A}/\mu\text{s}$. This results in high voltage spikes with peaks equal to $L \cdot di/dt$ with very small values of line inductance. Therefore the line connecting the commutating capacitors (C_C) must have an inductance less than $0.05 \mu\text{H}$, whereas the load inductance can be fairly high.



The commutating capacitors should be selected according to:

$$C_C = \frac{1}{10 \text{ V}} \int i_{com} dt$$

NOTE: i_{com} is the commutated current which charges the commutation capacitor an additional 10 V over the steady-state voltage.

Because of the voltage spikes during commutation, the supply voltages have to be smaller than 200 volts so that the peak voltage during switching does not exceed 400 volts.

FIGURE 2

THERMAL INFORMATION

MAXIMUM OUTPUT CURRENT vs DUTY CYCLE

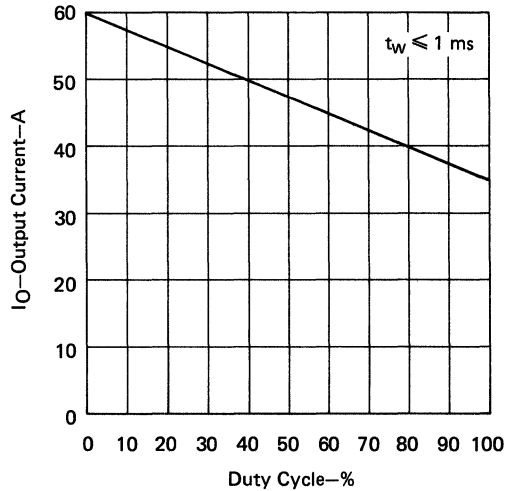


FIGURE 3

9

Power Semiconductor Technology

TABLE OF CONTENTS

SILICON POWER TRANSISTORS AND THYRISTORS

Mesa versus Planar versus Glass-Mesa Designs

Forward and Reverse Energy Considerations

Summary of Advantages and Disadvantages of Various Technologies

Chip-Mounting Techniques

Lead-Bonding Techniques

GERMANIUM POWER TRANSISTORS

Alloy Design

Diffused-Alloy Design

POWER SEMICONDUCTOR TECHNOLOGY

TECHNOLOGY DISCUSSION

SILICON POWER TRANSISTORS AND THYRISTORS

Mesa versus Planar versus Glass-Mesa Designs

Contemporary silicon power devices can be classified into two, broad, structurally different categories; planar and mesa.

A typical double-diffused epitaxial planar transistor structure is shown in Figure 1. The P-N junctions are all formed by diffusion and passivated by the oxide (SiO_2). A typical mesa transistor structure is shown in Figure 2. In this illustration the emitter-base junction is of planar structure. The collector-base junction is formed by selectively etching the silicon into a mesa-like structure. The exposed junction is usually coated with some insulating substance to protect it from contamination, humidity, and other adverse environments.

Typically, the planar structure is well-suited for higher frequency and faster switching. This is because the base width of the planar device can be made very narrow.

For the same reason, however, the breakdown voltage rating is usually limited to only several hundred volts. The mesa structure, due to its process limitations, is generally used for lower frequency and moderate switching speed. It does allow higher voltage devices to be built, however.

When operated under high-temperature conditions, the planar structure is generally the superior one. Through the intensive and fruitful effort in the advancement of the planar process, the oxide-silicon has become the best understood system in the semiconductor field. As a result, when the knowledge of planar technology is properly applied, planar devices with extremely low leakage current can be produced routinely and maintained with very high reliability.

Even though, historically, the mesa devices were among the first devices developed, the passivation of the exposed junction has not been well understood. As a result, the leakage currents are moderately higher and less stable than those of the planar devices. The knowledge of the planar technology has impacted the improvement of mesa junction passivation quite strongly. The development of glass passivation has contributed significantly to the reduction of leakage currents and improvement in stability in mesa structures. A typical glass-passivated structure is shown in Figure 3. This glass-passivated device offers the advantages of both the mesa and planar structures. Once the glass is in place, the unit is sealed against the rigors of assembly and can even be dipped into liquid solder without damage. This advanced concept is used in many power transistors and thyristors manufactured by Texas Instruments.

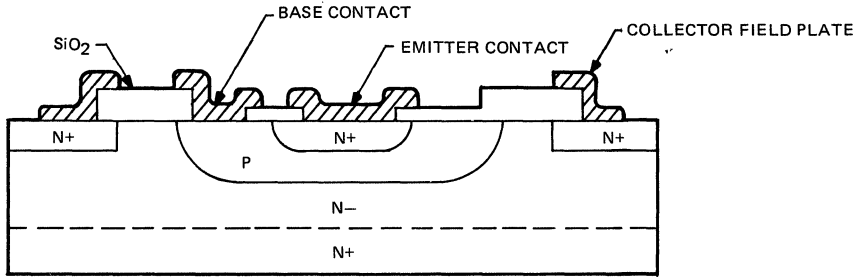


FIGURE 1—PLANAR TRANSISTOR STRUCTURE

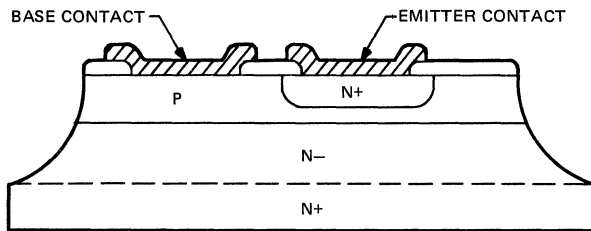


FIGURE 2—MESA TRANSISTOR STRUCTURE

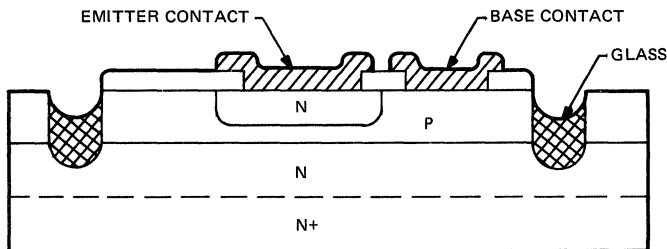


FIGURE 3—GLASS-PASSIVATED STRUCTURE

Forward and Reverse Energy Considerations

A power transistor must be designed not only to meet specific electrical specifications, but also to withstand the circuit application power requirements. A device with low thermal resistance does not guarantee that the device will operate in the circuit application. The application may exceed the second breakdown limitations of the device.

Transistors have two basic second breakdown modes. One mode is known as forward second breakdown and the other is reverse second breakdown. Forward second breakdown may occur when a device is operated in the amplifying mode. Most devices can handle more power in the low-voltage, high-current state than at the high-voltage, low-current condition. Second breakdown occurs when localized heating manifests itself in the emitter region. The cause for the "hot spot" is a non-uniform temperature profile across the emitter surface.

POWER SEMICONDUCTOR TECHNOLOGY

Because the V_{BE} characteristic of a transistor has a negative temperature coefficient, the "hot spot" area "hogs" the emitter current as the power is increased, thus leading to a thermal run-away condition. When the hot spot exceeds the eutectic temperature of the silicon-emitter-metal interface, the contact metal will diffuse through the emitter, causing a catastrophic failure.

Designing the emitter geometry such that the thermal resistance over the entire emitter region is constant will improve the forward second breakdown characteristics of the devices. All the recently announced TI power transistors utilize "isothermal" geometries to optimize the Safe Operating Area (SOA).

Reverse second breakdown may occur in a transistor during the turn-off transient. If a transistor is used for inductive switching, the device must dissipate the energy of the inductor when switching from a conducting state to an off state unless a protective circuit is used. The maximum energy that a transistor can dissipate in this transient condition is known as reverse energy capability. The reverse energy capability of a transistor can be increased by several orders of magnitude by using the optimum collector thickness and resistivity profile. Texas Instruments has developed a proprietary empirical method for calculating the starting material collector profile required to produce devices with optimum reverse energy capability versus other desired parameters.

Summary of Advantages and Disadvantages of Various Technologies

Now that these different general structures and design ideas have been discussed, a listing of specific designs and their advantages and disadvantages is provided below for ready reference.

Single-Diffused (Homogeneous-Base Mesa)

Advantages

- Excellent forward and reverse energy capability
- Low manufacturing cost

Disadvantages

- Low switching speed — excessive power dissipated during switching applications. Large-area heat sink required
- Very poor beta linearity versus collector current
- Inherent junction instabilities of a mesa device
- Requires at least 50% more silicon area for high-current performance
- Not practical for use in hybrid functions since junctions need to be passivated after assembly
- Complementary P-N-P type difficult to produce

TI Single-Diffused II (glass-passivated epi-base)

Advantages

- Excellent forward and reverse energy capability
- Low manufacturing cost
- Planar type leakages and stabilities due to glass-passivated junctions
- Faster switching speeds than homogeneous-base structure
- Complementary P-N-P types readily available at low cost
- No special processing required for utilization of chips in hybrid functions
- More linear beta versus collector current than homogeneous-base structure
- Less silicon required for high-current performance

Disadvantages

- Chip costs slightly higher due to additional slice processing

Triple-Diffused Mesa

Advantages

- Moderate switching speeds
- Good reverse energy capability
- Moderate saturation resistance
- High electrical yields

Disadvantages

- Mesa junction instabilities
- Long-duration high-temperature diffusions required for collector
- Chip must be passivated after being assembled to header
- Exposed junctions are sensitive to ambient conditions during wafer electrical probe

POWER SEMICONDUCTOR TECHNOLOGY

TI Triple-Diffused Glass-Passivated Mesa

Advantages

- Moderate switching speeds
- Good reverse energy capability
- Moderate saturation resistance
- High electrical yields
- No passivation of junction required after assembly
- Planar type leakage and stability due to glass-passivated junctions and N+ guard ring structure
- No special processing required for use of chips in hybrid functions.
- Wafer electrical probe can be set to tighter limits for high final test yields

Disadvantages

- Long-duration high-temperature diffusions required for collector

Epitaxial Planar

Advantages

- Fast switching speeds
- Excellent beta linearity versus collector current
- Low junction leakage and excellent stability
- P-N-P complement units are available
- Low saturation resistance

Disadvantages

- Generally lower energy capability
- Higher manufacturing costs

TI Isothermal Epitaxial Planar Transistors

Advantages

- Fast switching speeds
- Excellent beta linearity versus collector current
- Low junction leakage and excellent stability
- Good reverse and forward energy capability
- P-N-P complements available
- Low saturation resistance

Disadvantages

- Higher manufacturing costs

Chip-Mounting Techniques

Once the design of the silicon chip geometry has been achieved, the next problem to be addressed is how to assemble the unit.

The majority of mounting systems for power transistors and thyristors fall into two major categories—"hard" and "soft" solders. The "hard"-solder systems are often made up of a molybdenum mounting platform with a gold-base preform used to alloy the chip to the molybdenum. The coefficient of expansion of molybdenum approximates that of silicon such that the stresses of temperature excursions are minimized. In the "soft"-solder system, a lead-base solder is used to mount the chip directly to a copper platform. In this system, the flexible nature of the solder absorbs the stresses of mismatch between the silicon chip and the upper platform during temperature cycling. Disagreements exist as to which system is best but as with many similar questions, the answer depends upon the end use of the product. Both systems have their advantages and disadvantages. The hard-solder systems do not perform under repeated high-current surges as well as the soft-solder systems, and the soft systems, unless carefully chosen, tend to work-fatigue. Texas Instruments uses both systems with success.

Lead-Bonding Techniques

In bonding, as in mounting, there are two ways in which most power transistors and thyristors are assembled.

One method utilizes ultrasonic bonding of aluminum wire to the chip. The other technique is solder contact bonding. Again, each method has its advantages and disadvantages. When low volume and close control are available, the aluminum bond is very good, but the rugged solder contact method lends itself to volume production and is very readily process controlled. Texas Instruments uses both types of lead bonding methods in the construction of power transistors and thyristors, each serving the needs of the desired application.

POWER SEMICONDUCTOR TECHNOLOGY

GERMANIUM POWER TRANSISTORS

Texas Instruments is a high-volume manufacturer of an extremely broad line of germanium transistors. Manufacturing capabilities in virtually all areas of germanium semiconductor technology permit the production of devices ranging from high-power (150 watts) to high-frequency (3 GHz) low-noise amplifiers. Programs in mechanization and automation extending back to the mid-1950's at the Dallas, Texas, TI facility have permitted production of over 1,000,000,000 germanium transistors to satisfy the market needs for large volumes of high-quality devices.

During the assembly operations for germanium power devices, the collector portion of the element is mounted to the case (or header) to facilitate the transmittal of heat away from the element during the ultimate application of the device. After final surface treatment, the devices are hermetically sealed in a controlled, dry atmosphere.

Alloy Design

Germanium high-power and medium-power devices are available in P-N-P types which carry maximum ratings in the ranges of 180 volts, 25 amperes, and 150 watts. The majority of these devices are produced from alloy device elements and are particularly useful where low saturation voltage and high emitter-base breakdown voltage are important considerations. These devices are produced by alloying two (collector and emitter) dopant pellets, along with a base-contact ring, into a single-resistivity chip of germanium. This alloying operation is performed in a highly controlled-ambient atmosphere and temperature, in order to assure uniform functions in the devices.

Diffused-Alloy Design

A unique series of germanium power transistors is available in the JAN 2N1046 and 2N1908 devices. Their fabrication technique involved both alloying and diffusion technologies which produces devices that can operate at high frequencies (≈ 30 MHz), high current (≈ 20 A) levels, and that are useful as high-frequency power amplifiers.

Application Information

APPLICATION INFORMATION

APPLICATION REPORT SUMMARY

Introduction

Listed in this section are several application reports pertaining to the use of power semiconductors. Section A is a listing of abstracts of application reports previously published by Texas Instruments. Reprints of the full reports may be obtained by writing Texas Instruments Inc., P.O. Box 5012, M.S. 308, Dallas, Texas 75222

Section B contains a discussion of Safe Operating Areas and Secondary Breakdown Ratings of Power Transistors and Section C contains new application information covering Thermal Considerations in the use of Power Semiconductors.

A. APPLICATION REPORT SUMMARY

CA-66—SCR Switching Methods

This report describes various techniques for switching SCR's. Topics covered include: Electrical Characteristics of SCR's, Turning on SCR's, Effect of loads on switching, Turning off SCR's, and specific SCR switching applications.

CA-82—SCR Ring Counters

This report discusses the design and application of ring counter circuits using SCR's to perform digital logic functions.

CA-105—All Silicon 35-Watt Audio Power Amplifier

This report describes an all silicon, low-cost power amplifier featuring a transformerless, direct-coupled, complementary-symmetry, driver-output circuit. The class-AB output stage will deliver 35 watts rms (or 70 watts of peak power) into an 8-ohm load with a 55-volt supply.

With 35 watts (rms) output power, the frequency response is -3 dB at 7.4 Hz and 91 kHz. Total harmonic distortion is less than 0.5% from 60 Hz to 17 kHz, and less than 1% from 37 Hz to 54 kHz. Sensitivity at 1000 Hz is less than 1 volt for full power output.

CA-111—Low-Cost Solid-State Audio Amplifiers

This report presents two applications of TI's new low-cost, medium-power, silicon epitaxial base plastic transistors.

The circuits described in this note are a 15-watt (rms) complementary-symmetry audio power amplifier which is direct-coupled throughout, and a 3-watt (rms) class-A automotive audio power amplifier which uses a P-N-P output device.

Emphasis has been placed on obtaining a low-cost amplifier giving the maximum amount of output power possible from the device while using the minimum number of devices, holding the distortion to a reasonable level, and keeping the sensitivity compatible with typical amplifier requirements.

CA-116A—Low-Cost Plastic Power Audio Amplifiers

This report provides two examples of amplifier design (5 watts and 2.5 watts rms) using low-cost plastic single-diffused power transistors. Low-cost plastic power transistors are ideal components for use in the output stage of low-cost audio amplifiers. Excerpts from the subject data sheets are included.

APPLICATION INFORMATION

APPLICATION REPORT SUMMARY

CA-117—Low-Cost Plastic Power Drivers

This report describes two similar approaches to the preliminary design of an 80-watt (rms) audio power amplifier using low-cost plastic power transistors.

The first has a class-A driver stage and is suitable for a public address system. The other uses a slightly more complicated class-AB driver stage to obtain performance suitable for a high-quality music system.

Discussion is centered around design consideration of the driver stage.

CA-118—Economical Servo Control Amplifiers

This note describes a simple, reliable version of a servo amplifier that is particularly economical due to its use of a type of plastic power output transistor which exhibits high gain, high-dissipation capability, and low saturation voltages.

Devices used are single-diffused epitaxial-base plastic power transistors which are available in N-P-N and P-N-P polarities over a current range of one to 25 amperes.

CA-119—Economical Reversible D-C Motor Control

This report describes an economical solid-state circuit which regulates a single-polarity d-c power source to set the speed and direction of a reversible d-c motor, regardless of its shaft load (within the rating of the motor).

CA-120—Economical Power Voltage Regulators

In this report, an approach to output stage design is presented that is applicable to a wide variety of voltage regulators.

Complete designs are presented and compared for a series-pass and a switching-mode regulator.

CA-121—Fan Motor Thermostatic Speed Control

This report presents a thermostatic control circuit for two types of a-c motors suitable for air cooler, attic fans, and central air-conditioning blower motors.

The advantage of this circuit is its use of a triac as the power-control element. The circuit requires no power other than line voltage but uses low-voltage connections to remote-control elements.

A semiconductor thermistor (temperature-sensitive resistor) is the sensing element, and economical plastic transistors are used in the triac trigger circuit.

CA-123—Low-Cost 400-Watt Converter

This report discusses a converter with a saturating drive transformer and a non-saturating output transformer.

This converter steps up d-c from 20 V to 110 V and drives loads as large as 400 watts. Because the critical parts of the circuit are the power transistors and two transformers, the specifications of these devices are crucial to the design procedure.

11

APPLICATION INFORMATION

APPLICATION REPORT SUMMARY

CA-126—Economical High-Voltage Converters

This report describes the use of plastic-encapsulated single-diffused silicon power transistors in high-voltage converter applications. Two circuit concepts are discussed. The first one is a two-transistor converter using a single transformer for the drive and voltage-conversion function.

The second circuit is a single transistor blocking-oscillator type, common to high-voltage energy-discharge systems.

CA-137—Programmable Trigger Circuit for Triac Phase Control

This report discusses the theory and applications of the phase-shift technique of a-c power control using triacs. In this control system, power delivered to the load is varied by changing the phase angle during which the triac is conducting.

The designer may consider the basic circuit a universal building block which can be programmed for different applications by using different accessory networks.

CA-138—Triac Triggering Techniques

This report describes techniques to accomplish the triggering function and illustrates several different methods for controlling a-c power with triacs.

A sample triac data sheet is appended, and the important ratings of several popular TI triacs are tabulated.

CA-141—Universal Driver for Audio Amplifiers

This report describes a universal audio driver that, in conjunction with properly selected output transistors, can be made into an amplifier with an rms power capability of five watts to 50 watts.

By using low-cost plastic-encapsulated transistors and the minimum number of components, the cost has been kept to a minimum.

CA-142—Direct-Coupled Complementary 80-Watt Stereo Amplifier

The 80-watt-per-channel stereo system described in this report is an economical design with excellent performance. All transistors used are low-cost plastic devices with proven reliability and performance.

All the usual hi-fi inputs and equalization networks are provided.

CA-159—Voltage Feedback Methods to Improve Audio Amplifier Designs

This report examines the factors involved in utilizing voltage feedback, how these factors affect circuit performance, and how voltage feedback can best be employed to achieve the desired performance from an audio amplifier.

Discussions concern expressions for open-loop, closed-loop, and variations of certain closed-loop parameters with feedback, as well as boot-strapping and the effect of compensation on closed-loop performance.

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

B. SAFE OPERATING AREAS FOR POWER TRANSISTORS

The Safe Operating Area encloses all points representing simultaneous values of two variables which a transistor can safely handle under specified conditions. The majority of transistor applications can be reduced to one or more of the following operations:

- Forward-Biased Continuous Operation
- Pulsed Forward-Biased Operation
- Switching Between Saturation and Cutoff

Each operation is discussed in reference to:

- Presentation
- Test Circuit
- Test Points
- Test Procedure
- Temperature Derating

The maximum operating capability of each individual transistor is a complex function of I_C , V_{CE} , I_B , T_C and t_p . To characterize the full capability of a device would require an unreasonable number of test points. Therefore, it is necessary to simplify a rating and derating theory. No reference to the type of failure mode is made.

FORWARD-BIASED CONTINUOUS OPERATION

Presentation

Figure 1 shows a Forward-Biased Continuous Safe Operating Area. For $V_{CE} \leq V_{CE1}$ the total power dissipation P_T is limited by $I_{C\max}$. At increasing V_{CE} the power dissipation capability of most transistors is decreasing gradually. Because the rate of decrease depends on the individual transistor, it is suggested to use P_{T3} for $V_{CE2} < V_{CE} \leq V_{CE3}$ and P_{T4} for $V_{CE3} < V_{CE} \leq V_{CE4}$.

For the area given in Figure 1, safe operation is assured with forward bias only (I_B is positive for npn transistors, negative for pnp transistors). High-current germanium transistors may have I_{CEO} leakage currents of 1 A or more at high junction temperatures. It is not recommended to operate transistors continuously at currents smaller than I_{CEO} except in a temperature-stable cutoff condition.

Test Circuit

The Forward-Biased Continuous Safe Operating Area can be verified by using the temperature-stable common-base circuit illustrated in Figure 2. The Transistor Under Test (TUT) dissipates $P_T \approx I_C V_{CE}$ for $V_{CE} \gg 1\text{ V}$.

Test Points

The number of test points is arbitrary. The Safe Operating Area in Figure 1 requires three (3) test points: I_{C2} at V_{CE2} , I_{C3} at V_{CE3} and I_{C4} at V_{CE4} . Test points should be selected using the principle that only the verified P_{Tn} is assured for V_{CE} 's smaller than the test point voltage V_{CEn} .

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Test Procedure

Test Point Example: $I_C = I_{C2}$

$$V_{CE} = V_{CE2}$$

$$T_C = 55^\circ\text{C for } T_{J \max} \leq 125^\circ\text{C}$$

$$T_C = 100^\circ\text{C for } T_{J \max} > 125^\circ\text{C}$$

Test Duration: 1 minute

Determine: $R_C = \frac{V_{CE2}}{I_{C2}}$

$$R_E \geq \frac{5 \text{ V}}{I_{C2}}$$

Test Sequence:

1. Start with V_{CC} and V_{EE} at low voltage.
2. Increase V_{CC} to approximately V_{CE2} .
3. Increase V_{EE} to obtain I_{C2} .
4. Increase V_{CC} to two times V_{CE2} .
5. Adjust V_{EE} to obtain V_{CE2} and I_{C2} .
6. Operate transistor at specified case temperature for one (1) minute. The transistor is not acceptable if I_C varies more than $0.1 \cdot I_{C2}$ during the one (1) minute test.
7. Decrease V_{CC} to V_{CE2} .
8. Turn off V_{EE} .
9. Turn off V_{CC} .

Evaluation:

The device shall be capable of meeting the specification.

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Temperature Derating for Continuous Operation

The maximum allowable case temperature for a given P_T can be calculated as follows:

$$T_C \leq T_{J \max} - \frac{P_T}{P_{Tn}} (T_{J \max} - 55^\circ\text{C}) \text{ for } T_{J \max} \leq 125^\circ\text{C}$$

$$T_C \leq T_{J \max} - \frac{P_T}{P_{Tn}} (T_{J \max} - 100^\circ\text{C}) \text{ for } T_{J \max} > 125^\circ\text{C}$$

T_C = Case Temperature

$T_{J \max}$ = Maximum Operating Junction Temperature

P_T = Total power dissipation at $V_{CE} \leq V_{CEn}$

P_{Tn} = Total power Dissipation at Test Point V_{CEn} and
 $T_C = 55^\circ\text{C}$ for $T_{J \max} \leq 125^\circ\text{C}$ or $T_C = 100^\circ\text{C}$
 for $T_{J \max} > 125^\circ\text{C}$.

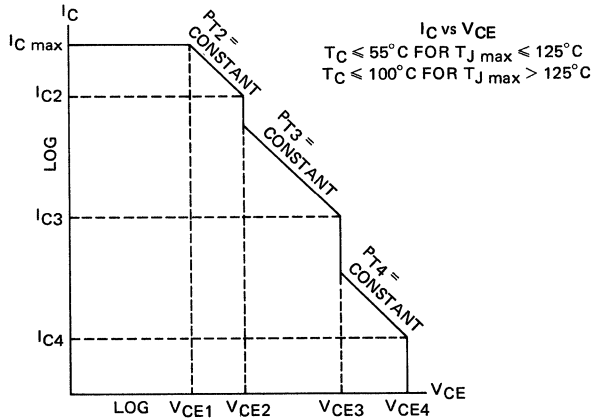


FIGURE 1

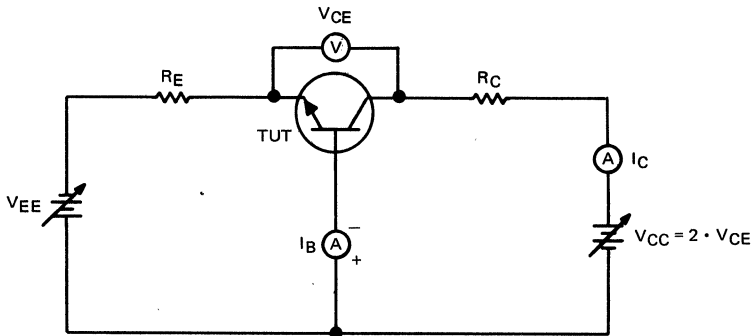


FIGURE 2

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

PULSED FORWARD-BIASED OPERATION

Presentation

Figure 3 shows three pulse width areas for $t_{p1} \geq t_{p2} \geq t_{p3}$; however additional pulse width areas may be added. The presentation in Figure 3 has the advantage of specifying the maximum capability of a transistor type at $I_C \text{ max}$ whereas the area in Figure 4 is based on maximum capability at highest allowable V_{CE} . The area in Figure 4 is limited by $I_C \text{ max}$ and curves representing constant $I_C \cdot V_{CE}$ product. Therefore, the test point at highest V_{CE} assures all other operating points within a given t_p area, but on the other hand, this method derates the capability of a transistor at $I_C \text{ max}$.

Test Circuits

In test circuit Figure 5 the Pulsed Forward-Biased capability of a transistor can be verified. The transistor Q_1 can be replaced by a switch such as a mercury relay. Some test circuits require an emitter resistor for the Transistor Under Test (TUT). Such a resistor is not desirable because it complicates specification writing as well as testing procedures.

Test Points

The number of test points equals the number of pulse width areas. The following table shows the required specification for verification at $T_C = 25^\circ\text{C}$:

FIGURE	TEST POINT	I_C	V_{CE}	t_p
3	#1	$I_C \text{ max}$	V_{CE5}	t_{p1}
	#2	$I_C \text{ max}$	V_{CE6}	t_{p2}
	#3	$I_C \text{ max}$	V_{CE7}	t_{p3}
4	#1	I_{C1}	V_{CE8}	t_{p1}
	#2	I_{C2}	V_{CE8}	t_{p2}
	#3	I_{C3}	V_{CE8}	t_{p3}

In addition the duty cycle has to be specified.

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Test Procedure

Test Point Example: $T_C = 25^\circ\text{C}$

$$I_C = I_{C \text{ max}}$$

$$V_{CE} = V_{CE5}$$

$$t_p = t_{p1}$$

$$\text{Duty Cycle} = d1$$

Determine: $V_{CC1} = V_{CE5} + I_{C \text{ max}} R_S$

The collector current capability of Q_1 should be approximately:

$$I_{CQ1} = 2 \left(\frac{V_{BB2} + 1.5 \text{ V}}{R_{BB2}} + \frac{I_{C \text{ max}}}{h_{FE \text{ min}} (\text{TUT})} \right)$$

The current supplied to the base of Q_1 should be sufficient to drive Q_1 into saturation for I_{CQ1} . Transistor Q_1 may be replaced by a relay. The rise and fall time of the collector current should be small compared to the pulse width t_p .

Test Sequence:

1. With all voltage supplies turned off adjust the pulse generator for $t_p = t_{p1}$ and $d = d1$.
2. Turn on V_{CC} to V_{CC1} .
3. Increase V_{BB1} until i_c reaches $I_{C \text{ max}}$ by applying single pulses.
4. Check that the following conditions are met:

$$t_r \ll t_p$$

$$t_f \ll t_p$$

$$T_C = 25^\circ\text{C}$$

5. The transistor is not acceptable if i_c varies more than $0.1 \cdot I_{C \text{ max}}$ during t_{p1} . The duration of test is only that time adequate to make the reading.
6. Adjust V_{BB1} to zero and turn off V_{CC} .

For subsequent transistors to be tested, only steps 2, 3, 5 and 6 have to be repeated.

Evaluation:

The device shall still be capable of meeting the specification.

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

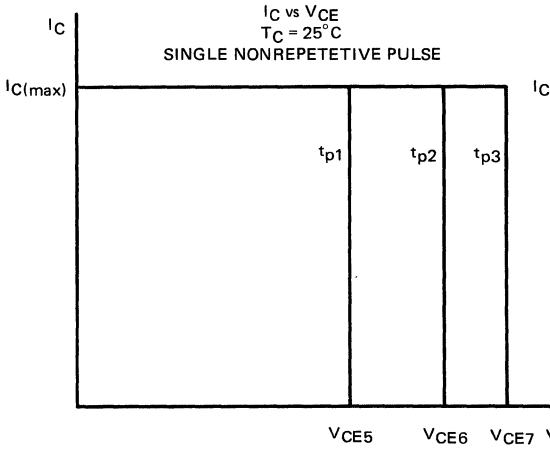


FIGURE 3

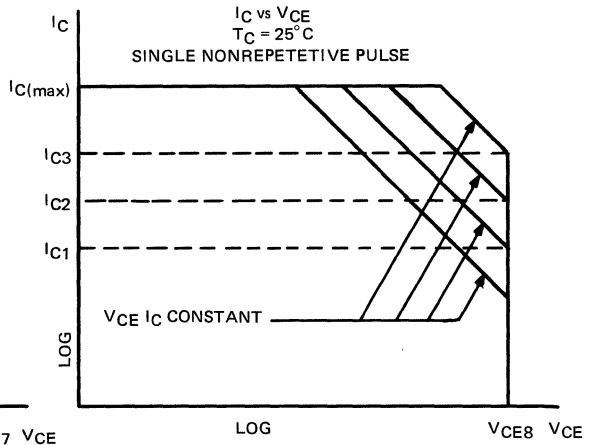


FIGURE 4

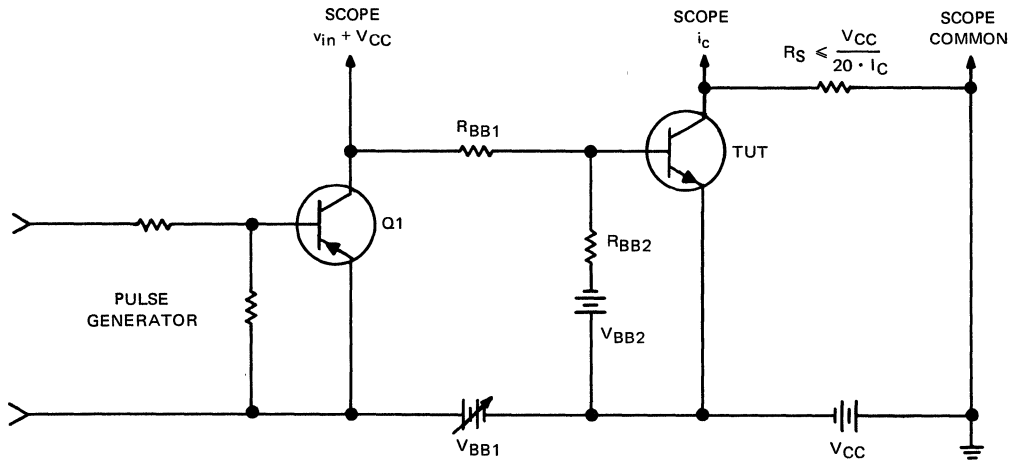


FIGURE 5

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

SWITCHING BETWEEN SATURATION AND CUTOFF

Resistive Load

Presentation

Figure 6 shows the area within which the load line has to be located for safe operation with a resistive load.

Test Circuit

Verification of the Safe Operating Area is performed by switching the transistor on and off with a single non-repetitive pulse in circuit Figure 7.

Test Points

Only one test point has to be verified. This is accomplished by switching from $V_{CE \text{ max}}$ to saturation at $I_C \text{ max}$ and back again to $V_{CE \text{ max}}$.

Test Procedure

Test Point Example: $T_C = 25^\circ\text{C}$

$$I_C = I_C \text{ max}$$

$$V_{CE} = V_{CE \text{ max}}$$

$$R_{BB1} = R_{BB1(1)}$$

$$R_{BB2} = R_{BB2(1)}$$

$$V_{BB1} = V_{BB1(1)}$$

$$V_{BB2} = V_{BB2(1)}$$

Determine:

$$R_L = \frac{V_{CE \text{ max}}}{I_C \text{ max}}$$

$$V_{CC} = V_{CE \text{ max}}$$

The collector current capability of Q_1 should be approximately:

$$I_{CQ1} = 2 \left(\frac{V_{BB2} + 1.5 \text{ V}}{R_{BB2}} + \frac{V_{BB1} - 1.5 \text{ V}}{R_{BB1}} \right)$$

The current supplied to be base of Q_1 should be sufficient to drive Q_1 into saturation for I_{CQ1} .

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Test Sequence

1. Adjust V_{BB1} , V_{BB2} , and V_{CC} .
2. Apply single pulses with increasing pulse width until $I_C = I_{C\max}$ using the specified duty cycle.
3. The transistor is not acceptable if the cutoff state after the pulse cannot be maintained. The duration of the test is only that time adequate to make the reading.
4. Turn off all supplies.

Evaluation:

The device shall still be capable of meeting the specification.

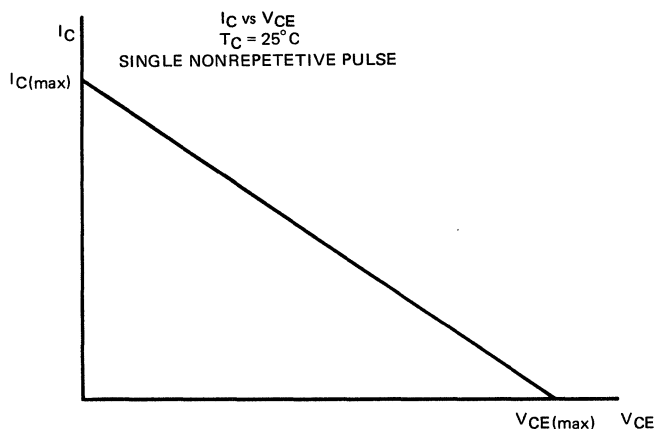


FIGURE 6

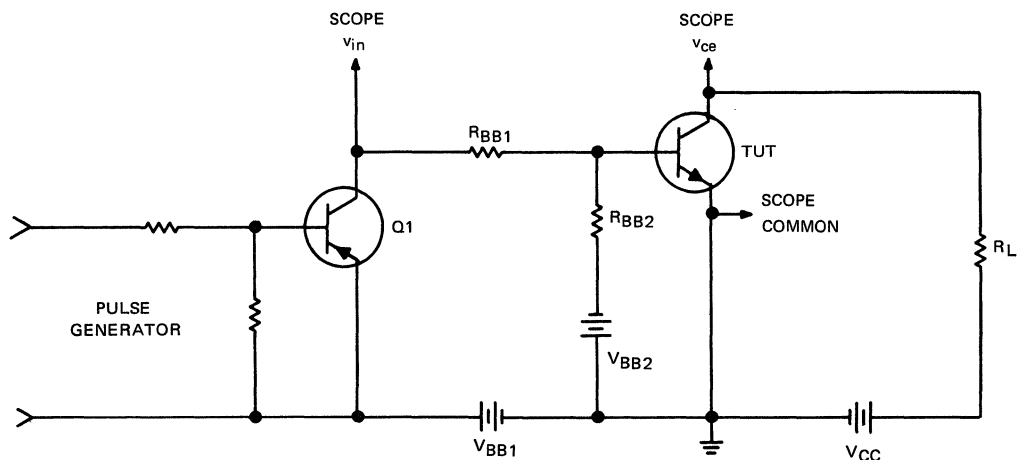


FIGURE 7

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Clamped Inductive Load

Presentation

Figure 8 shows the area within which the load line has to be located for safe operation with a clamped inductive load.

Test Circuit

The test circuit in Figure 9 is similar to the one shown in Figure 7 except for the load in the collector circuit. R_{LOAD} represents the total resistive part of the load.

Test Points

By switching through the worst allowable load line during turn off, the Safe Operating Area of Figure 8 can be verified.

Test Procedure:

Test Point Example: $T_C = 25^\circ\text{C}$

$$I_C = I_{C \max}$$

$$V_{CE} = V_{CE9}$$

$$R_L = R_{L1}$$

$$L = L_1$$

$$R_{BB1} = R_{BB1(1)}$$

$$R_{BB2} = R_{BB2(1)}$$

$$V_{BB1} = V_{BB1(1)}$$

$$V_{BB2} = V_{BB2(1)}$$

$$CR = 1NXXXX$$

$$V_{CC} = V_{CE9}$$

The collector current capability of Q_1 should be approximately:

$$I_{CQ1} = 2 \left(\frac{V_{BB2(1)} + 1.5 \text{ V}}{R_{BB2(1)}} + \frac{V_{BB1(1)} - 1.5 \text{ V}}{R_{BB1(1)}} \right)$$

The current supplied to the base of Q_1 should be sufficient to drive Q_1 into saturation for I_{CQ1} .

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Test Sequence

1. Adjust V_{BB1} to make $v_{in} = V_{BB1(1)}$, V_{BB2} to $V_{BB2(1)}$, and V_{CC} to V_{CE9} .
2. Apply single pulses with increasing pulse width until $i_c = I_{C \text{ max}}$ with duty cycle as specified.
3. The transistor is not acceptable if the cutoff state after the pulse cannot be maintained. The duration of the test is only that time adequate to make the reading.
4. Turn off all supplies.

Evaluation:

The device shall still be capable of meeting the specification.

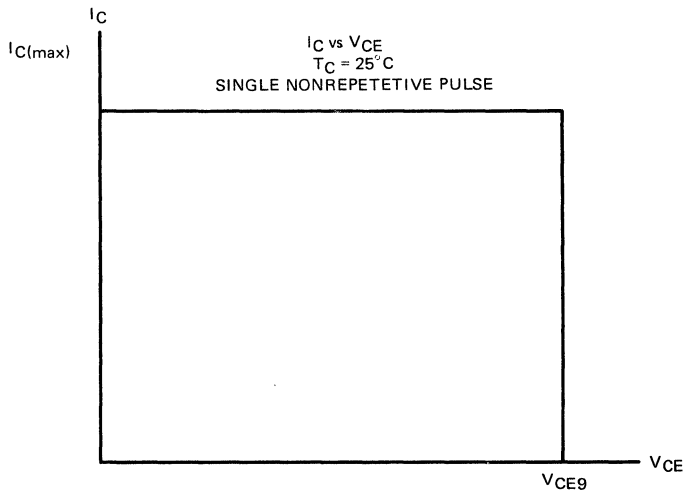


FIGURE 8

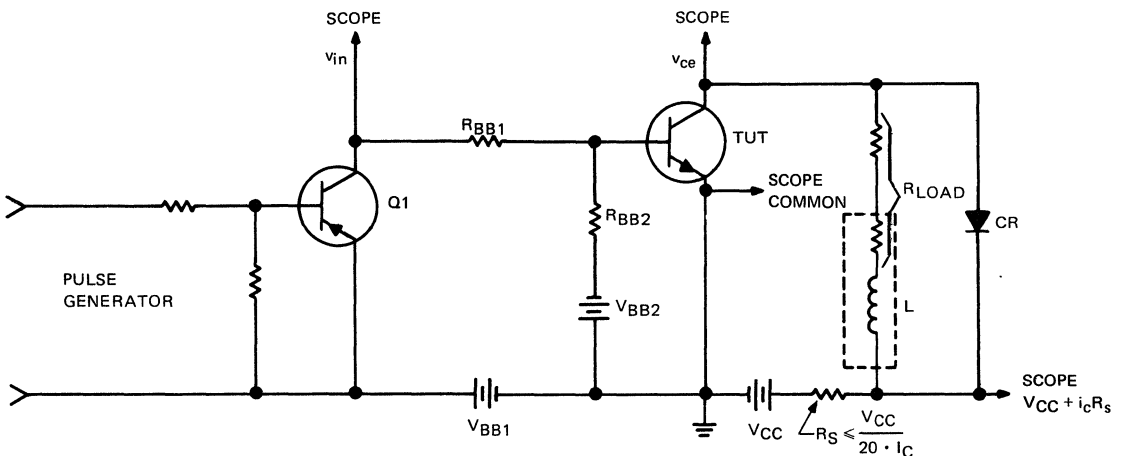


FIGURE 9

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Unclamped Inductive Load

Presentation

Figure 10 shows three different areas depending on V_{BB2} and R_{BB2} . The number of areas is arbitrary. The areas are limited by $I_{C\max}$, curves representing constant energy, $I_C^2 L/2$, and a reasonable amount of maximum inductance L_1 associated with circuits for which the transistor type is intended for.

Test Circuit

Verification of the Safe Operating Area is performed by switching the transistor from cutoff to saturation to cutoff with a single non-repetitive pulse in the circuit of Figure 11.

Test Points

Testing transistors with I_{C4} , I_{C5} , and I_{C6} and L_1 assures the respective safe operating areas because the capability of absorbing inductive energy increases with increasing collector current. This method derates the capability of a transistor at $I_{C\max}$ but decreases the amount of testing at higher currents otherwise necessary to verify a curve which attempts to follow the actual capability of the device.

The energy absorbed by the transistor is given by:

$$E_T = E_L + E_S - E_R = \frac{3 \cdot L \cdot I_C^2 \cdot V_{(BR)CEX}}{6 V_{(BR)CEX} - 6 V_{CC} + 4 R_L I_C}$$

where:

E_L = Inductive Energy Stored in L. $E_L = I_C^2 L/2$

E_S = Energy from Power Supply During "Turnoff" Transient

E_R = Energy Absorbed by Resistive Component of the Load During "Turnoff" Transient

E_T = Energy Absorbed by Transistor During "Turnoff" Transient.

$V_{(BR)CEX}$ = Breakdown Voltage of Transistor Under Test ($V_{(BR)CEO}$, $V_{(BR)CER}$ or $V_{(BR)CEX}$ - Depending on V_{BB2} and R_{BB2}).

Transistors with $V_{(BR)CEX} \gg V_{CC}$ absorb a lower energy E_T during the test than transistors with $V_{(BR)CEX} \approx V_{CC}$. If the E_T capability of a transistor has to be predicted without knowing $V_{(BR)CEX}$, the following E_T can be absorbed at $T_C = 25^\circ\text{C}$ for a single non-repetitive pulse:

$$E_T = \frac{1}{2} L \cdot I_C^2$$

It is desirable to choose $V_{CC} \leq 15\text{ V}$. This tends to decrease damage to transistors which are unable to pass the specified test point.

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Test Procedure

Test Point Example: $T_C = 25^\circ\text{C}$

$$I_C = I_{C4}$$
$$V_{CC} = V_{CC2} \leq 15\text{ V}$$
$$R_L = R_{L2} \leq V_{CC2}/2I_{C4}$$
$$L = L_2$$
$$R_{BB1} = R_{BB1(2)}$$
$$R_{BB2} = R_{BB2(2)}$$
$$V_{BB1} = V_{BB1(2)}$$
$$V_{BB2} = V_{BB2(2)}$$

Determine:

The approximate required pulse-width to reach I_{C4} is given by:

$$t_{p4} = \frac{L_2}{V_{CC}} I_C$$

The collector current capability of Q_1 should be approximately:

$$I_{CQ1} = 2 \left(\frac{V_{BB2(2)} + 1.5\text{ V}}{R_{BB2(2)}} + \frac{V_{BB1(2)} - 1.5\text{ V}}{R_{BB1(2)}} \right)$$

The current supplied to the base of Q_1 should be sufficient to drive Q_1 into saturation for I_{CQ1} .

Test Sequence

1. Adjust V_{BB1} to make $v_{in} = V_{BB1(2)}$, V_{BB2} to $V_{BB2(2)}$, and V_{CC} to V_{CC2} .
2. Apply single pulses with $t_p \ll t_{p4}$. Increase pulse width until $i_c = I_{C4}$. (Duty cycle should be such that $T_{J(AVG)} \approx 25^\circ\text{C}$.)
3. The transistor is not acceptable if the collector-emitter voltage collapses or oscillates during the collector current fall time t_f . The transistor must be capable to maintain $V_{(BR)CEX}$ during t_f within $\pm 10\%$ of $V_{(BR)CEX}$. The duration of the test is only that time adequate to make the reading.
4. Turn off all supplies.

Evaluation:

The device shall still be capable of meeting the specification.

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

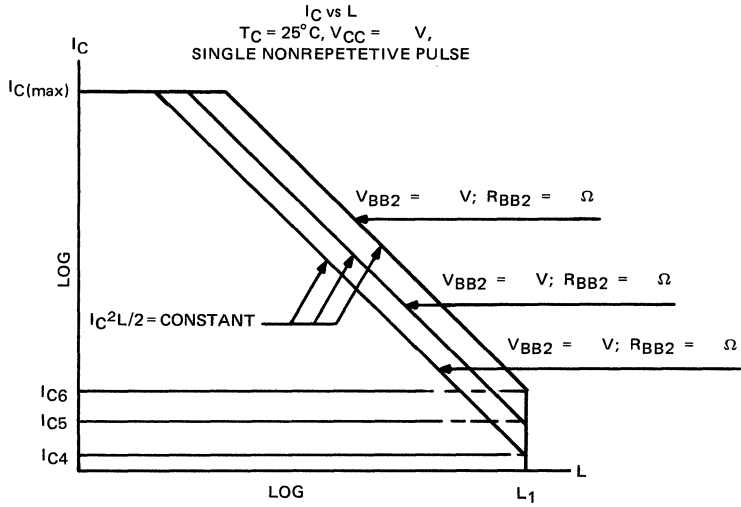


FIGURE 10

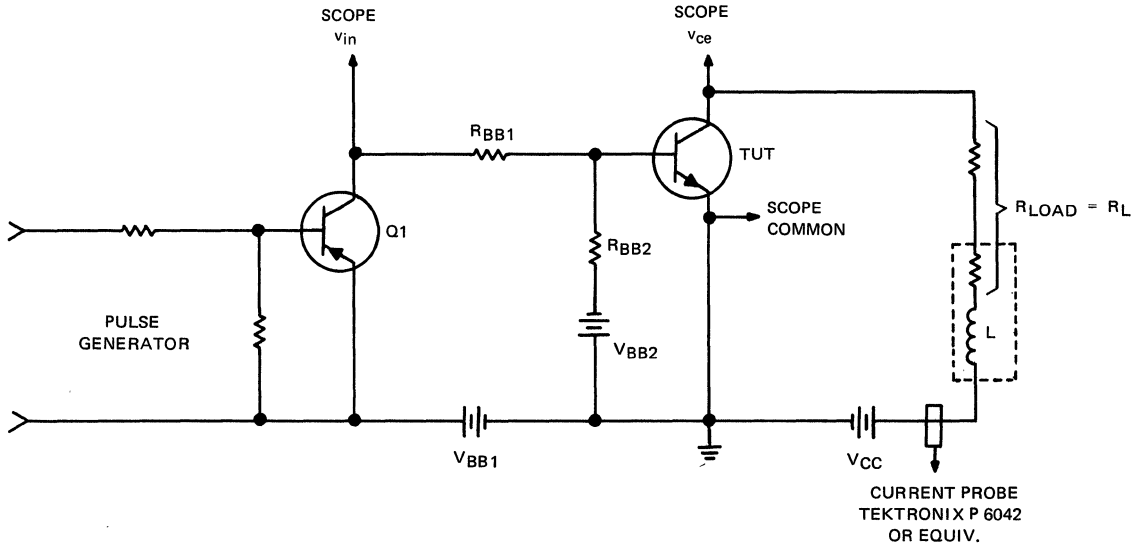


FIGURE 11

APPLICATION INFORMATION

SAFE OPERATING AREAS FOR POWER TRANSISTORS

Temperature Derating for Pulsed Forward-Biased Operation and Switching

A safe maximum case temperature ($T_C \geq 25^\circ\text{C}$) for a given I_C and average total power dissipation $P_{T(\text{AVG})}$ due to repetitive pulses can be calculated as follows:

$$T_C \leq T_{J \max} - \frac{I_C}{I_{Cn}} (T_{J \max} - 25^\circ\text{C}) - R_{\theta JC} P_{T(\text{AVG})}$$

T_C = Case temperature

$T_{J \max}$ = Maximum operating junction temperature.

I_C = Collector current during saturation

I_{Cn} = Maximum allowed collector current at $T_C = 25^\circ\text{C}$

$R_{\theta JC}$ = Thermal resistance junction to case

$P_{T(\text{AVG})}$ = Average total power dissipation

APPLICATION INFORMATION

THERMAL CONSIDERATIONS

C. THERMAL CONSIDERATIONS

Heat Flow

To understand the flow of heat through a solid, it is helpful to use an electrical analogy.

ELECTRICAL TERM	THERMAL TERM
V—Voltage differential [V]	T—Temperature differential [°C]
I—Current [A]	P—Power [W]
R—Resistance [Ω]	R_{θ} —Thermal resistance [°C/W]

Figure 1 illustrates the thermal circuit as it applies to a semiconductor device dissipating a continuous power into an air-cooled heat sink.

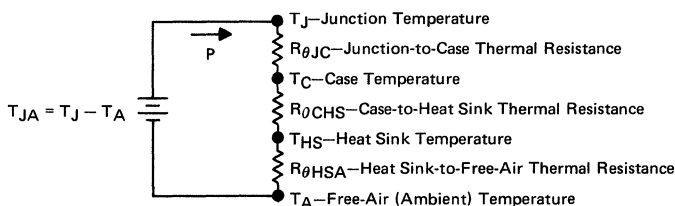


FIGURE 1

The corresponding thermal circuit for a device dissipating continuous power in free air is shown in Figure 2.

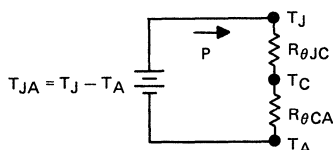


FIGURE 2

The most frequent thermal requirement which must be met is $T_J \leq T_{J(max)}$. For a given power dissipation this means the sum of all thermal resistances from junction-to-ambient must be:

$$R_{\theta JA} \leq \frac{T_{J(max)} - T_A}{P}$$

Junction-to-Case Thermal Resistance— $R_{\theta JC}$

$R_{\theta JC}$ is the temperature difference between the power dissipating junction and a point specified on the case divided by the power dissipation. Most T1 power device data sheets specify $R_{\theta JC}$. The case temperature measurement point is shown under "Mechanical Data". Derating should be performed as outlined in SECTION B, Safe Operating Areas for Power Transistors, under "Temperature Derating for Continuous Operation". This is necessary because $R_{\theta JC}$ increases with increasing collector-emitter voltage. Depending on the transistor construction, there is an additional increase or decrease of $R_{\theta JC}$ with increasing collector current. In applying the Safe Operating Area concept, $R_{\theta JC}$ variations with operating point do not have to be considered.

APPLICATION INFORMATION

THERMAL CONSIDERATIONS

Case-to-Heat-Sink Thermal Resistance— $R_{\theta CHS}$.

$R_{\theta CHS}$ is a function of the following conditions:

- Torque applied to the machine screw or stud
- Use of thermal compound and type of compound
- Use of insulator and material of insulator
- Flatness of device and heat sink
- Surface finish
- Heat-sink material

The effect of mounting torque as well as insulator material is shown in Figure 3 and Figure 4 for plastic transistors.

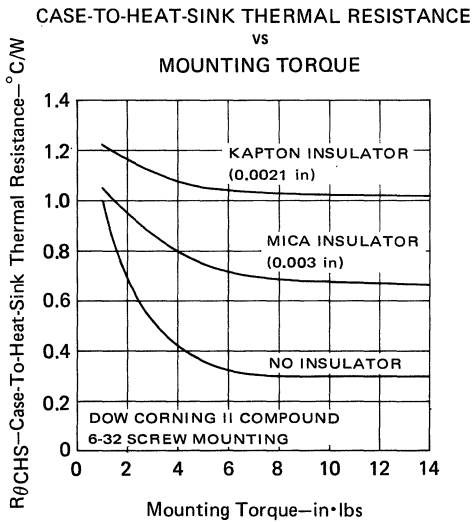
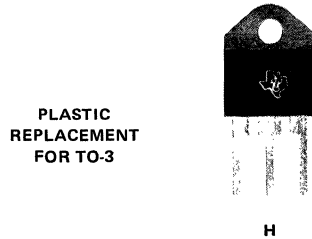
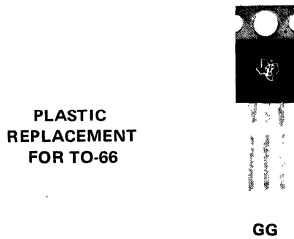


FIGURE 3

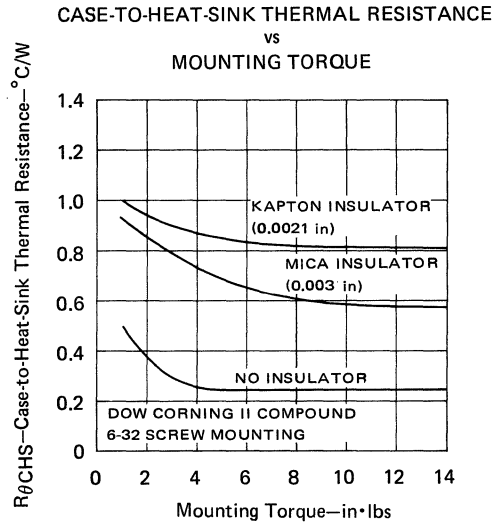


FIGURE 4

APPLICATION INFORMATION

THERMAL CONSIDERATIONS

Following is a table of $R_{\theta CHS}$ using a mica insulating washer. The heat sink used to determine this value was a smooth, flat, copper plate, with the thermocouple mounted 0.05 inch below the mounting surface in an area beneath the device. The device was mounted using a 2-mil mica washer to a clean, dry, heat-sink surface, without the use of a thermal compound. A torque of ten inch-pounds was applied to the stud or to each of the mounting screws.

PACKAGE	$R_{\theta CHS}$ [$^{\circ}C/W$]
TO-3	1.5
TO-53	1.6
TO-59, TO-60, TO-111	3.8
TO-61	1.3
TO-63	1.1

By using a thermal compound, the above thermal resistances can be decreased more than $0.6^{\circ}C/W$, depending upon the type of compound used.

Case-to-Free-Air Thermal Resistance— $R_{\theta CA}$

$R_{\theta CA}$ is more of a constant than $R_{\theta CHS}$ because $R_{\theta CA}$ is not dependent on so many variables. Most TI power device data sheets specify $R_{\theta JA}$ which is $R_{\theta JC} + R_{\theta CA}$.

Quality and Reliability Information

QUALITY AND RELIABILITY INFORMATION FACILITIES AND EQUIPMENT

FACILITIES AND EQUIPMENT

A. LIFE TEST AND BURN-IN FACILITIES

1. Texas Instruments Incorporated is equipped with extensive facilities to provide life test and burn-in capabilities for germanium power transistors, silicon power transistors, and thyristors.
2. Facilities are available for a wide range of tests including:
 - a. Storage life testing up to 300°C.
 - b. Voltage-temperature stress testing at both ambient and elevated temperature conditions.
 - c. Free-air operating for more than 20,000 silicon power and germanium transistors.
 - d. Case temperature operating for 8600 silicon power transistors at dissipation levels up to 200 watts.
 - e. Intermittent operating at various cycle times and power levels.

B. ENVIRONMENTAL FACILITIES

1. Test capabilities of the Environmental Laboratory are shown in two different ways. First, Military Standard Test Capability which lists capability per MIL-STD-202, MIL-STD-750, and MIL-STD-883 for each test category; and second, Overall Test Capability which lists capability limits and, where applicable, combined environment capability for each test category.
2. Laboratory capabilities required for performance of tests per MIL-STD-202, MIL-STD-750, and MIL-STD-883 are listed in Table I. Those tests which are noted as exceptions are beyond the capability of the Environmental Laboratory.
3. Laboratory capability limits, including limits of combined environments, are shown in Table II for each test category.

QUALITY AND RELIABILITY INFORMATION

FACILITIES AND EQUIPMENT

TABLE I—MILITARY STANDARD TEST CAPABILITY

TEST CATEGORY	MIL-STD-202	MIL-STD-750	MIL-STD-883
Altitude	All Conditions	All Conditions	All Conditions
Dew Point		All Conditions	All Conditions
Flammability	All Conditions		
Moisture Resistance	All Conditions	All Conditions	All Conditions
Resistance to Solvents (Symbolization)	All Conditions		
Salt Atmosphere		All Conditions	All Conditions
Salt Spray	All Conditions	All Conditions	
*Seal, Gross Leak	All Gross Leak Conditions (Method 112A, Conditions A, B, and Procedure IV of Condition C. Method 104A, Conditions A, B & C)†	All Gross Leak Conditions (Method 1071, Conditions C, D, E & F)†	All Gross Leak Conditions (Method 1014, Conditions C & D)†
Solderability	All Conditions	All Conditions	All Conditions
Soldering Heat		All Conditions	
Temperature Cycling	All Conditions EXCEPT: Method 107, Con- ditions D & F	All Conditions EXCEPT: Method 1051, Con- ditions D & E	All Conditions EXCEPT: Method 1010, Con- ditions E & F
Terminal Strength (Lead Integrity)	All Conditions	All Conditions	All Conditions
Thermal Shock (Glass Strain)		All Conditions	All Conditions
Acceleration, Sustained (Centrifuge)	All Conditions	All Conditions	All Conditions EXCEPT: Method 2001, Con- dition J NOTE: ¶ Method 2001, Con- dition G and H, may require special fixtur- ing. Limited capabil- ity for these condi- tions is available for special package types.
‡Shock (Mechanical)	All Conditions EXCEPT: Method 213, Con- ditions B, C, G, J, and K	All Conditions	All Conditions NOTE: ¶ Method 2002, Con- dition F and G, may require special fixtur- ing. Capability for these conditions is available for special package types.
Vibration, Fatigue		All Conditions	All Conditions
Vibration, Noise		All Conditions	All Conditions
▲Vibration, Random	All Conditions		
▲Vibration, Variable Frequency	All Conditions	All Conditions	All Conditions
Seal, Fine Leak (Radioactive Tracer Gas)	ONLY Method 112A, Condi- tion C, Procedure III.B	ONLY Method 1071, Condi- tion G only	ONLY Method 1014, Condition B only
◆X-Ray, Film	All Conditions	All Conditions	All Conditions
◆X-Ray, Real Time (TV X-Ray)	All Conditions	All Conditions	All Conditions

*See Radiographic Inspection Capability for Seal, Fine Leak.

†Items in parenthesis are the gross leak test conditions performed by Environmental Laboratory. Exception to these particular methods not listed.

‡Also perform mechanical shock per MIL-STD-810B, Method 516, Procedures I, III and IV.

▲Also perform random vibration and vibration variable frequency per MIL-STD-810B, Method 514.1, Procedures I, II, III, IV, and VII. Omit paragraph 4.5.1.1, Resonant Search, and paragraph 4.5.1.2, Resonant Dwell for Electronic Components.

¶Capability for testing approximately 15 major microelectric package types per MIL-STD-883, Method 2001, Conditions G and H (sustained acceleration) and for testing approximately 30 major microelectric packages per MIL-STD-883, Method 2002, Conditions F and G (mechanical shock) are presently available. These high "G" level conditions are used primarily for evaluation tests on small packages such as C-DIP, PIP, 4A header, TO-5, TO-18, etc.

◆Radiographic inspection is performed in accordance with many other government and customer specifications. Before any new radiographic specification is acceptable for use as a test standard with Components Group, it must be approved by Environmental Laboratory.

QUALITY AND RELIABILITY INFORMATION FACILITIES AND EQUIPMENT

TABLE II—OVERALL TEST CAPABILITY

TEST	CAPABILITY
Acceleration, Sustained (Centrifuge)	50-50,000 g (Standard) 50,000-100,000 g (Nonstandard)
Altitude (Barometric Pressure, Reduced)	450,000 ft. Simulated Altitude with -125° C to 125° C Capability
Cryogenic Exposure	-75° C to -196° C
Dew Point	-65° C to 150° C
Flammability	900° C to 1100° C
Moisture Resistance	2° C to 96° C, 40% to 100% RH
Radiographic Inspection (X-Ray)	
Film	Resolution to 0.001 Inch, 150 kV-5 mA
Real Time	360° Rotation—Resolution to 0.001 Inch
Salt Atmosphere/Spray	25° C to 71° C, Up to 20% Salt Solution by Weight
Seal	
Gross Leak	>5 X 10 ⁻⁶ , 150° C, Fluorocarbons, Mineral Oils, Ethylene Glycol Hydrostatic Pressure—0-300 psig
Radioactive Tracer Gas	≥ 1 X 10 ⁻¹¹
Symbolization (Resistance to Solvents)	
Shock (Mechanical)	PULSE SHAPE—APPROXIMATELY HALF-SINE 1,500-30,000 g @ 0.2 ms ± 0.1 ms 1,000-6,000 g @ 0.3 ms ± 0.1 ms 500-10,000 g @ 0.5 ms ± 0.15 ms 500-4,000 g @ 1 ms ± 0.3 ms 500 & 1,000 g @ 1.5 ms ± 0.45 ms 1,800 g @ 3 ms ± 0.6 ms 50-100 g @ 6 ms ± 0.9 ms 50-200 g @ 7 ms ± 1.05 ms 15-150 g @ 11 ms ± 1.65 ms PULSE SHAPE—SAWTOOTH 100 g @ 6 ms
Solderability/Soldering	Up to 280° C
Temperature Cycling	-185° C to 300° C
Terminal Strength (Lead Integrity)	Lead Fatigue, Tension, Stud Torque, Terminal Torque
Thermal Shock	-196° C to 200° C
Ultrasonics	0-100 psi at 25 kHz or 40 kHz
Ultraviolet Exposure	To 12.5 mW/cm ²
Vibration, Fatigue	10-100 Hz, 5-70 g
Vibration, Random	20-200 Hz, Power Density 1.3 g ² /Hz
Vibration, Variable	5-2,000 Hz as Limited by 1 Inch DA and 60 Inches/Second Velocity, 0-70 g (Standard), 70-100 g (Nonstandard)

QUALITY AND RELIABILITY INFORMATION PRODUCT RELIABILITY DATA

RELIABILITY DATA

The reliability data in this section covers a cross-section of device types included in this data book. The data is broken down into four major sections:

- Germanium Power Transistors
- Silicon Power Transistors
- Thyristors
- Single-Diffused Plastic Power Transistors

Germanium Power Transistors

2N1041

TEST		DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.	
STORAGE: 100°C		339,000	2 (I _{CB0})	0.89	
OPERATING: V _{CE} = 20 V, P = 1.2 W, T _C = 55°C		341,000	0	0.26	
PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CB0}	V _{CB} = 50 V		70 μA		70 μA
h _{FE}	V _{CE} = 0.5 V, I _C = 1 A	20	60	20	60

2N1046

TEST		DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.	
STORAGE: 95°C		96,000	0	0.93	
OPERATING: V _{CE} = 40 V, V _{BE} = 0.2 V, T _{stg} = 55°C		96,000	0	0.93	
PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CB0}	V _{CB} = 40 V		1 mA		2 mA
h _{FE}	V _{CE} = 1 V, I _C = 0.5 A	40	200	32	

Silicon Power Transistors

2N1049A, 2N1050A

TEST		DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.	
STORAGE: 200°C		689,080	1 (h _{FE})	0.29	
OPERATING: V _{CE} = 40 V, P _C = 23 W, T _C = 100°C		730,080	4 (I _{CB0})	0.69	
PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CB0}	V _{CB} = 30 V		15 μA		30 μA
h _{FE}	V _{CE} = 10 V, I _C = 500 mA	30	90	24	108

QUALITY AND RELIABILITY INFORMATION

PRODUCT RELIABILITY DATA

2N2151

TEST		DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.	
STORAGE: 200°C		468,000	0	0.19	
OPERATING: V _{CE} = 40 V, P _T = 30 W, T _C = 100°C		159,000	1 (I _{CES})	1.21	

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CES}	V _{CE} = 120 V		5 μA		10 μA
V _{(BR)CEO}	I _C = 50 mA	100 V		100 V	
h _{FE}	V _{CE} = 5 V, I _C = 1 A	40	120	36	144

2N2880

TEST		DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.	
STORAGE: 200°C		262,000	3 (2 h _{FE}) (1 I _{CBO})	1.52	
OPERATING: V _{CE} = 20 V, P _T = 30 W, T _C = 100°C		249,000	2 (I _{CBO})	1.20	

2N2880 (BURNED-IN FOR 168 HOURS)

TEST		DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.	
STORAGE: 200°C		944,000	3 (I _{CBO})	0.43	
OPERATING: V _{CE} = 20 V, P _T = 30 W, T _C = 100°C		679,000	2 (1 I _{CBO}) (1 I _{EBO})	0.44	

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CBO}	V _{CB} = 80 V		0.4 μA		0.8 μA
I _{EBO}	V _{EB} = 6 V		0.4 μA		0.8 μA
h _{FE}	V _{CE} = 5 V, I _C = 1 A	40	120	36	144

2N1724

TEST		DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.	
STORAGE: 200°C		906,508	1 (I _{CES})	0.22	
OPERATING: V _{CE} = 40 V, P _C = 50 W, T _C = 100°C		856,248	1 (I _{CES})	0.23	

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CES}	V _{CE} = 60 V		300 μA		600 μA
I _{EBO}	V _{EB} = 5 V		400 μA		500 μA
V _{(BR)CEO}	I _C = 200 mA	80 V		80 V	
h _{FE}	V _{CE} = 15 V, I _C = 2 A	30	90	27	108

QUALITY AND RELIABILITY INFORMATION PRODUCT RELIABILITY DATA

2N1722

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	285,000	3 (2 I _{EBO}) (1 I _{CES})	1.40
OPERATING: V _{CE} = 10 V, P _C = 50 W, T _C = 100°C	285,000	2 (1 I _{EBO}) (1 I _{CES})	1.05

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CES}	V _{CE} = 60 V		300 μA		600 μA
I _{EBO}	V _{EB} = 5 V		400 μA		500 μA
V _{(BR)CEO}	I _C = 200 mA	80 V		80 V	
h _{FE}	V _{CE} = 15 V, I _C = 2 A	30	90	27	108

2N3420 AND 2N3421

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	1,077,540	3 (I _{CES})	0.38
OPERATING:	2N3420 V _{CB} = 40 V, P _T = 1 W	7 (I _{CES})	0.79
	2N3421 V _{CB} = 60 V, P _T = 1 W		

2N3420 AND 2N3421 (BURNED-IN FOR 168 HOURS)

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	1,360,860	3 (1 O/S) [†] (2 I _{CES})	0.30
OPERATING:	2N3420 V _{CB} = 40 V, P _T = 1 W	2 (I _{CES})	0.22
	2N3421 V _{CB} = 60 V, P _T = 1 W		

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CES}	2N3420 V _{CE} = 80 V		0.5 μA		1 μA
	2N3421 V _{CE} = 120 V		0.5 μA		1 μA
V _{(BR)CEO}	2N3420 I _C = 50 mA	60 V		60 V	
	2N3421 I _C = 50 mA	80 V		80 V	
h _{FE}	2N3420 V _{CE} = 2 V, I _C = 1 A	20	60	16	72
	2N3421 V _{CE} = 2 V, I _C = 1 A	40	120	32	144

[†]O/S designates open or shorted.

QUALITY AND RELIABILITY INFORMATION

PRODUCT RELIABILITY DATA

2N3998 AND 2N3999

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	162,000	0	0.54
OPERATING: V _{CE} = 20 V, P _T = 30 W, T _C = 100°C	162,000	1 (I _{CES})	1.20

2N3998 AND 2N3999 (BURNED-IN FOR 168 HOURS)

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	710,000	3 (I _{CES})	0.56
OPERATING: V _{CE} = 20 V, P _T = 30 W, T _C = 100°C	497,000	1 (O/S)†	0.40

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CES}	V _{CE} = 100 V		5 μA		10 μA
V _{(BR)CEO}	I _C = 50 mA	80 V		80 V	
h _{FE}	V _{CE} = 2 V, I _C = 1 A	40	120	36	144
		80	240	72	288

2N1714, 2N1715, 2N1716, AND 2N1717

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	662,000	1 (h _{FE})	0.29
OPERATING: V _{CB} = 40 V, P _C = 0.8 W	676,000	4 (3 I _{CES}) (1 I _{CEX})	0.75

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CES}	V _{CE} = 60 V		2 μA		4 μA
V _{(BR)CEO}	I _C = 30 mA	60 V		60 V	
		100 V		100 V	
h _{FE}	V _{CE} = 5 V, I _C = 200 mA	20	60	16	72
		40	120	32	144

2N3996 AND 2N3997

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	110,000	0	0.80
OPERATING: V _{CE} = 20 V, P _T = 30 W, T _C = 100°C	110,000	0	0.80

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _{CES}	V _{CE} = 90 V		5 μA		10 μA
V _{(BR)CEO}	I _C = 50 mA	80 V		80 V	
h _{FE}	V _{CE} = 2 V, I _C = 1 A	40	120	36	144
		80	240	72	288

† O/S designates open or shorted.

QUALITY AND RELIABILITY INFORMATION

PRODUCT RELIABILITY DATA

2N389 AND 2N424

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	708,000	2 (V _{(BR)CER})	0.42
OPERATING: P = 48 W, T _C = 100°C	353,000	6 (V _{(BR)CER})	2.0

PARAMETER		CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
			MIN	MAX	MIN	MAX
V _{(BR)CER}	2N389	I _C = 20 mA, R _{BE} = 33 Ω	60 V		60 V	
	2N424		80 V		80 V	
h _{FE}		I _C = 1 A, V _{CE} = 15 V	15	60	12	75

2N497, 2N498, 2N656, AND 2N657

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 200°C	904,250	2 (1 I _{CBO}) (1 V _{(BR)CEO})	0.33
OPERATING: P = 0.8 W, T _A = 25°C	904,250	7 (4 I _{CBO}) (3 h _{FE})	0.90

PARAMETER		CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
			MIN	MAX	MIN	MAX
I _{CBO}	2N497, 2N656	V _{CB} = 50 V		1 μA		10 μA
	2N498, 2N657	V _{CB} = 80 V		1 μA		10 μA
h _{FE}	2N497, 2N656	V _{CE} = 10 V, I _C = 200 mA	12	36	9.6	45
	2N498, 2N657		30	90	24	117
V _{(BR)CEO}	2N497, 2N656	I _C = 30 mA	60 V		60 V	
	2N498, 2N657		100 V		100 V	

Thyristors

2N3557

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
DYNAMIC OPERATION: V _{RRM} = 100 V, I _{T(AV)} = 1 A, T _A = 25°C, f = 60 Hz	944,000	10	1.2

PARAMETER		CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
			MIN	MAX	MIN	MAX
I _D		V _D = 100 V, R _{GK} = 1 kΩ		30 nA		30 nA
I _R		V _R = 100 V, I _G = 0		0.1 μA		0.1 μA
I _{GT}		V _{AA} = 5 V, R _L = 12 Ω		200 μA		200 μA
I _H		R _{GK} = 1 kΩ, R _L = 12 Ω		5 mA		5 mA

QUALITY AND RELIABILITY INFORMATION

PRODUCT RELIABILITY DATA

2N3002

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
STORAGE: 150°C	336,000	4	1.5
OPERATING: I _T = 200 mA, V _D = 30 V, T _A = 25°C	336,000	4	1.5

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _D	V _D = 60 V, R _{GK} = 1 kΩ		20 nA		20 nA
I _R	V _R = -60 V, R _{GK} = ∞		100 nA		100 nA
I _{GR}	V _{GK} = -5 V, R _L = ∞		100 nA		100 nA
I _{GT}	V _{AA} = 5 V, R _L = 12 Ω		200 μA		200 μA
V _{GT}	V _{AA} = 5 V, R _L = 12 Ω		800 mV		800 mV
I _H	R _{GK} = 1 kΩ		5 mA		5 mA
V _T	I _T = 2 A		1.5 V		1.5 V

2N1596

TEST	DEVICE HOURS	FAILURES	F. R. X 10 ⁻⁵ 60% CONF.
DYNAMIC OPERATION: I _{T(AV)} = 250 mA, V _{DRM} = 100 V, T _A = 25°C, f = 60 Hz	247,000	2	1.2

PARAMETER	CONDITIONS	INITIAL LIMITS		POST TEST LIMITS	
		MIN	MAX	MIN	MAX
I _D	V _D = 100 V		250 μA		250 μA
I _R	V _R = 100 V		250 μA		250 μA
I _{GT}	V _F = 50 V, R _{GK} = 1 kΩ, R _L = 2 kΩ	6 mA	10 mA	6 mA	10 mA

QUALITY AND RELIABILITY INFORMATION

PRODUCT RELIABILITY DATA

Single-Diffused Plastic Power Transistors

TIP29-TIP32, TIP41, TIP42

BACKGROUND

Texas Instruments continuing Plastic Single-Diffused Reliability Program, an evaluation program for plastic power devices, has resulted in lowering device failure rates. All devices utilized in the reliability program are standard product "off-the-shelf" devices which have received no special screening or electrical tests. Since starting the reliability program we have generated over 500,000 actual life-test hours. Over 15,000 devices have undergone testing in the reliability program. Failures are based on leakage greater than twice the data sheet limit, h_{FE} outside data sheet limits by 20%, or $V_{CE(sat)}$ above data sheet limits. For the test environments listed below, MIL-STD-750 was used as the applicable test specification.

1. Mechanical Shock, Method 2016.
2. Vibration, Variable-Frequency, Method 2056.
3. Constant Acceleration, Method 2006.
4. Thermal Shock, Method 1056, Condition B.
5. Temperature Cycling, Method 1051.
6. Moisture Resistance (non-operating), Method 1021.
7. Humidity with Bias, $T_A = 85^\circ\text{C}$, RH = 85%
 $V_{CES} = 45\text{ V}$.
8. Humidity $T_A = 65^\circ\text{C}$, RH = 100%.
9. Pressure Cooker, $T_A = 121^\circ\text{C}$, 15 psi.
10. Solderability, Method 2026.
11. Salt Atmosphere, Method 1041.
12. Terminal Strength, Method 2036, Condition A.
13. Storage Life, Method 1032, $T_A = 150^\circ\text{C}$.
14. Operating Life, Method 1026, $T_A = 25^\circ\text{C}$, P = 2 watts.
15. Intermittent Operating, Method 1037, $\Delta T_C = 60^\circ\text{C}$, P = 1.8 watts, 5 minutes on, 5 minutes off.

LIFE TEST EVALUATIONS

Test devices employed in this evaluation were subjected to operational, intermittent operational, and storage life test conditions that were selected to demonstrate device capability in excess of normal operating requirements. The operating life test circuits used for testing power devices are in the parallel, common-base configuration. Voltage is applied collector to base.

A resistor is in series with the emitter, dropping at least 10% of the collector-base voltage to set the emitter current. For intermittent operating tests, the same circuit is used with the power being interrupted at specific time intervals.

Table 1-1
Summary of Life Testing for NPN Devices

Test Description	Number of Devices	Device Hours	Number of Failures	Failure Rate $\times 10^{-5}$	
				Point Est.	60% Conf.
150°C Storage	50	100,000	0	0	0.9
25°C Operating	140	212,500	2	0.9	1.4

Table 1-2
Summary of Life Testing for PNP Devices

Test Description	Number of Devices	Device Hours	Number of Failures	Failure Rate $\times 10^{-5}$	
				Point Est.	60% Conf.
150°C Storage	49	73,500	3	4.1	5.6
25°C Operating	50	62,500	3	4.8	6.5

Table 1-3
Summary of Intermittent Life Testing For NPN Devices

Test Description	Number of Devices	Device Cycles	Number of Failures	Failure Rate $\times 10^{-5}$	
				Point Est.	60% Conf.
$\Delta 60^\circ\text{C}$ Interm. Operating	88	880,000	0	0	0.1

ENVIRONMENTAL TESTING

Environmental evaluations are performed on power devices in order to establish capability for the mechanical and thermal stresses considered to be standard in the electronics industry. Sequential or step-stress testing is likewise employed to demonstrate package reliability in excess of standard product requirements. A brief description of test procedures follows:

QUALITY AND RELIABILITY INFORMATION

PRODUCT RELIABILITY DATA

1. Mechanical Shock – Performed from 1500 g to 6000 g in three orientations for 0.2 ms to 0.5 ms duration: 5 blows/plane, 15 blows total (non-operating).
2. Vibration, Variable Frequency – Performed from 20 g to 60 g in three orientations at 100 Hz to 2000 Hz (non-operating); 4 sweeps/plane, 4 minutes/sweep.
3. Constant Acceleration – Performed from 10,000 g to 40,000 g in six orientations; 1 minute/plane.
4. Thermal Shock—Performed from 0°C to 100°C for 50 cycles. Extreme times are 5 minutes with a maximum transfer time of 10 seconds. Liquid to liquid.
5. Temperature Cycle – Performed from -65°C to 150°C for 100 cycles. Extreme times are 30 minutes with a maximum transfer time of 5 minutes.
6. Temperature Cycle – Performed from -55°C to 125°C for 15 cycles. Extreme times are 10 minutes with a maximum transfer time of 5 minutes.
 - Thermal Shock – Performed in freezer at -30°C and boiling water. Extreme times are 10 minutes with immediate transfer.
 - Power Surge – Performed by storing at -45°C for 20 minutes and then applying maximum rated power for 1 minute. Total of 15 cycles.
 - Humidity – Performed by placing devices in humidity chamber at 40°C with 95% relative humidity for 96 hours.
7. Moisture Resistance – Performed in a non-operating state with the preconditioning omitted. Temperature cycling chamber conditions:
 - 25°C for 5 hours.
 - 65°C for 5 1/2 hours.
 - Chamber maintained at 90 to 98% relative humidity, -10°C chill excursion on all test cycles.
8. Humidity with Bias – Performed by placing devices in humidity chamber at 85°C with 85% relative humidity for 200 hours. A VCES of 45 V is applied to each device.
9. Humidity – Performed by placing devices in humidity chamber at 65°C with 100% relative humidity for 200 hours.
10. Pressure Cooker – Performed by placing devices in sealed chamber with 100% relative humidity at 121°C. Air pressure applied at 15 psi over atmosphere. Test repeated in 8-hour increments.
11. Solderability – Performed by dipping leads into type-W flux at 25°C to within 0.05 inches of case for a period of 5 to 10 seconds. Leads then dipped in molten solder at 230°C ± 15°C to within 0.05 inches of case at rate of 1 ± 1/4 inches per second for a period of 5 ± 1/2 seconds.
12. Salt Atmosphere – Performed by exposing devices to 35°C fog environment. Test duration: 72 hours (initial conditioning omitted). DC electrical test and visual examination endpoints.
13. Terminal Strength – Performed by attaching a 5-ounce weight to each external lead at a distance of 1/16 inch from case. A force is applied once in each of the 2 mutually perpendicular directions (90° + 10° - 0°). Test duration: 3 bending cycles.

SUMMARY

The Plastic Single-Diffused Reliability Program was designed to establish reliability data for encapsulated devices for commercial and consumer applications. The results of the tests show that these devices can also be used in military applications.

To obtain this objective over 15,000 transistors have undergone tests. Over 500,000 life-test hours have been accumulated. Detailed results have been listed in this report with summaries of the test procedures and conditions. If further information is required, please contact your nearest TI sales office or address inquiries to Texas Instruments Incorporated, Quality Reliability Assurance, Power Dept., Mail Station 2, P.O. Box 5012, Dallas, Texas 75222.

QUALITY AND RELIABILITY INFORMATION

PRODUCT RELIABILITY DATA

Table 2-1
Summary of Mechanical-Stability Testing for Both
PNP and NPN Devices

Test No.	Test Description	Number of Devices	Failures
(1)	Mechanical Shock		
	1500 g, 0.5 ms	24	0
	3000 g, 0.5 ms	24	0
	6000 g, 0.3 ms	24	0
(2)	Vibration, Var. Freq.		
	20 g	25	0
	30 g	25	0
	40 g	25	0
	50 g	25	0
	60 g	25	0
(3)	Constant Acceleration		
	10,000 g	24	0
	15,000 g	24	0
	20,000 g	24	0
	30,000 g	24	0
	40,000 g	24	0

NOTE: Stressing in each category is sequential. For example, the devices stressed on shock at 6000 g were pre-stressed on shock at 3000 g.

Table 3-1
Summary of Thermal-Stability Testing
for Both PNP and NPN Devices

Test No.	Test Description	Number of Devices	Failures
(4)	Thermal Shock (0° C to +100° C)		
	10 cycles	25	0
	20 cycles	25	0
	30 cycles	25	0
	40 cycles	25	0
	50 cycles	25	0
(5)	Temp Cycle (-65° C to +150° C)		
	50 cycles	75	0
	100 cycles	75	0
(6)	Environmental Test Sequence		
	Temperature Cycle	15	0
	Thermal Shock	15	0
	Power Surge	15	0
	Humidity	15	0

Table 4-1
Summary of Humidity Testing for Both
PNP and NPN Devices

Test No.	Test Description	Number of Devices	Failures
(7)	Moisture Resistance		
	10 cycles	25	0
	20 cycles	25	0
	30 cycles	25	1*
(8)	Humidity with Bias	50	0
(9)	Humidity	50	0
(10)	Pressure Cooker		
	8 hours	25	0
	16 hours	25	0
	24 hours	25	0
	32 hours	25	0

Table 5-1
Summary of Solderability, Salt-Atmosphere, and
Terminal-Strength Testing for Both
PNP and NPN Devices

Test No.	Test Description	Number of Devices	Number of Failures		
			Electrical	Visual	Mechanical
(11)	Solderability	50	0	0	N/A
(12)	Salt Atmosphere	50*	0	0	0
(13)	Terminal Strength	36	0	N/A	0

*For salt atmosphere, a visual failure is for marking and a mechanical failure is for corrosion.

*ICES failure, read 423 μ A, limit is 400 μ A.

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