PHY Layout

APPLICATION REPORT: SLLA020

Ron Raybarman
Burke S. Henehan
1394 Applications Group

Mixed Signal and Logic Products
Bus Solutions
November 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com
US 1394 email	1394@ti.com
US 1394 Web Site	http://www.ti.com/sc/1394

Contents

Figures

PHY Layout

Abstract

This document makes recommendations for the layout of the PHY and Link layer devices in an IEEE 1394 environment. The optimal performance of an IEEE 1394 bus can be dependent on good board layout. An IEEE 1394 board that does not adhere to good layout guidelines may be susceptible to noise and interference which could diminish the signal integrity. This document is not meant to be a general tutorial on good PWB layout practice; it is meant to highlight those areas of a 1394 node that may need special attention due to the special requirements of IEEE 1394 nodes.

World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

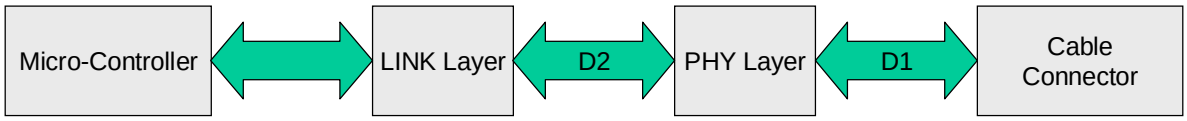
The URL specifically for the TI 1394 external web site is http://www.ti.com/sc/1394. On this page, one can subscribe to 1394 Times, which periodically updates subscribers on events, articles, products, and other news regarding 1394 developments.

Email

For technical issues or clarification on switching products, please send a detailed email to 1394@ti.com.

Introduction

Figure 1. A Typical IEEE 1394 Node

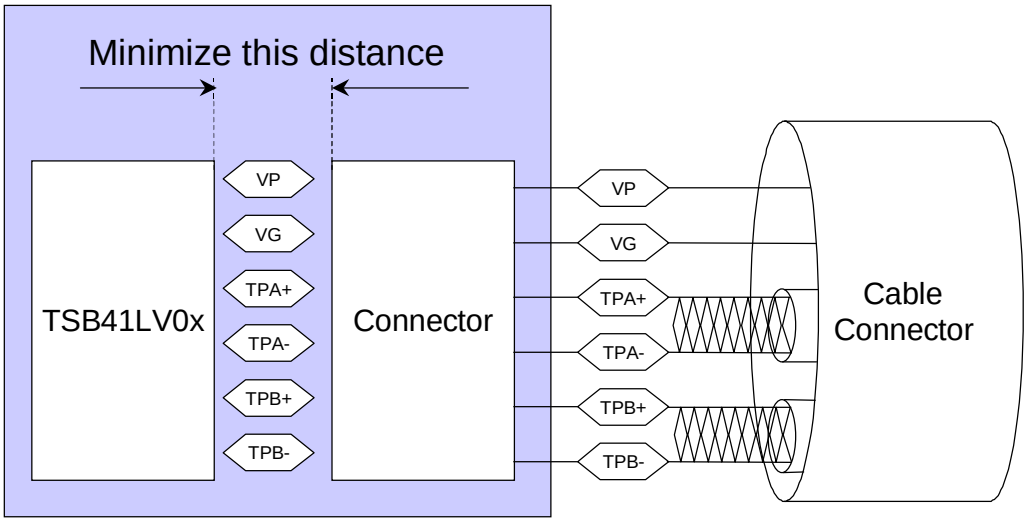


The Physical Layer (PHY) provides the digital logic and analog transceiver functions needed to implement a one or multiple port physical layer in an IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The 1394 link layer communicates with the physical layer, packetizes the data decoded by the physical layer, provides cycle timing functions, and communicates the packets to and from the node controller. Figure 1 illustrates the logical layout points discussed in this document. Distance D1 between the physical layer and the cable connector and distance D2 between the link layer and the physical layer are the two that will be discussed below. The layout for the distance between the micro-controller and link layer is very heavily dependent on the microprocessor chosen and is outside the scope of this document.

Guidelines for Layout

1) The physical layer should be as close as possible to the 1394 connector (refer to Figure 1 and Figure 2). Because of the frequencies involved (up to 200 MHz at 400Mbps) the etches propagating the differential twisted pair (TP) signal in a 1394 cable should be treated as transmission lines. The signal swing on the TP lines is relatively small (~110 mV) so any differential noise picked up on the twisted pair may affect the received signal. When the twisted pair signal is propagated on etch, without any shielding, the etch tends to behave as an antenna and pick up noise generated by the surrounding components and the environment. To minimize the effect of this behavior, as well as other artifacts documented below, minimize the distance the twisted pair signal must be propagated on etch. The shielding on a standard 1394 cable inhibits this sort of interference while the signal is being propagated through the cable.

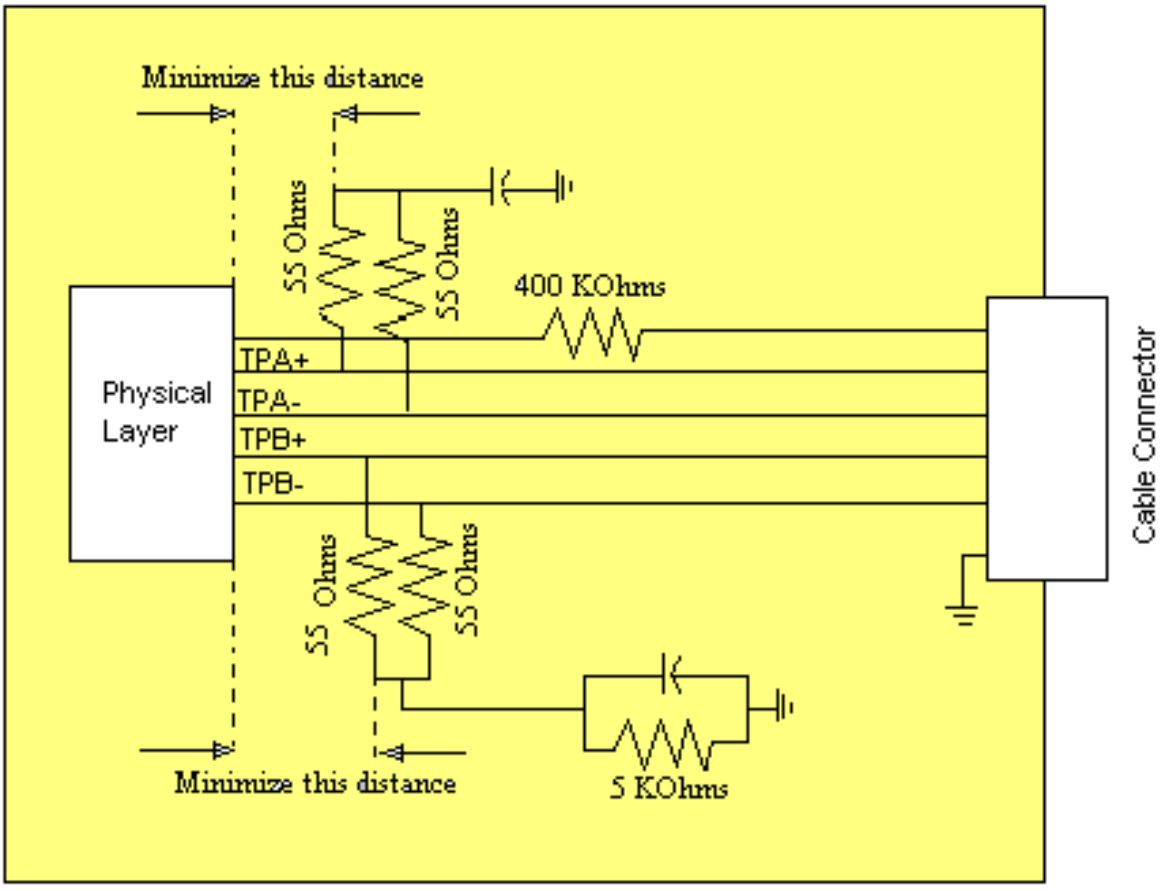
Figure 2. The PHY Connector and Cable Connector



2) Since the etch traces should be treated as transmission lines, they need to match impedances with the cable and connector they are connected to. The IEEE standard 1394 twisted pair cable is specified to have a 110 +/- 6 Ohms differential characteristic with a common mode characteristic impedance of 33 +/- 6 Ohms (IEEE 1394-1995 paragraph 4.2.1.4.1). The input impedance of a node is also specified as 110 +/- 1 Ohm in receive mode (IEEE 1394-1995 paragraph 4.2.2.5), hence the recommended termination network of 55 +/- 1% resistors

(please see the TSB41LV0x data sheet). To minimize reflections and maximize the power transmitted to the input pin, the etch length between the termination at the physical layer and the 1394 cable connector ports should be designed with a characteristic impedance of 110 Ohms between the TP+ and TP- lines with a minimum of 33 Ohms to ground. That is, the etch should have the same impedance as that of the cable and termination network. Having a different impedance will cause reflections with less power being transmitted to the input terminals on the physical layer, which may reduce signal integrity.

Figure 3. Terminating Resistor



3) In a note related to #2, the termination resistors (55 ohms +/- 1%) should be located as close as possible to the TP (twisted pair) pins on the 1394 physical layer (refer to Figure 3). The purpose of the terminating resistor network is to match impedance with the cable transmission line, minimizing induced signal reflections. Placing the termination resistors

close to the physical layer signal pin reduces the stub length between the physical layer terminal and the termination resistor. The longer the stub, the better the antenna it makes, and the more noise and interference it picks up that can distort the signal. There are tradeoffs between these first three recommendations. The better the etch impedance matches the cable, the longer the TP etches can be, to a point. The lower the induced noise sources around the etches, the longer they can be, to a point. The better the impedance match of the etches, the longer the termination resistors can be from the physical layer, to a point. And the point it breaks will vary with all of the above factors (and more).

Figure 4. The etch length for the differential signals are equal

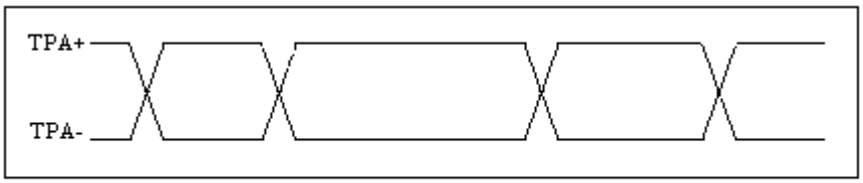


Figure 5. The etch length of TPA- is longer than TPA+

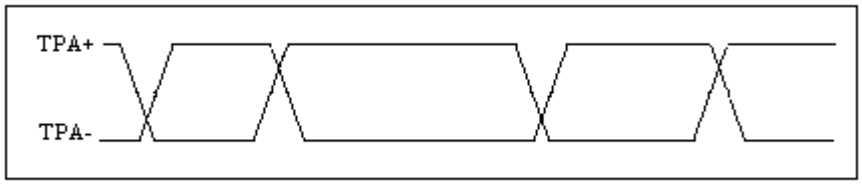


Figure 6. The etch length of both differential signal pairs are align headed

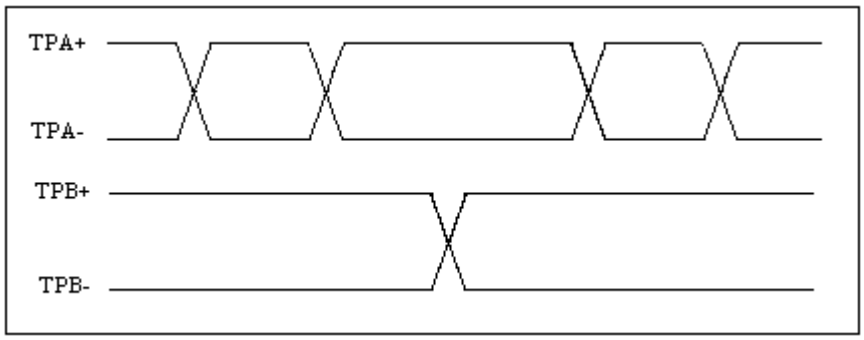
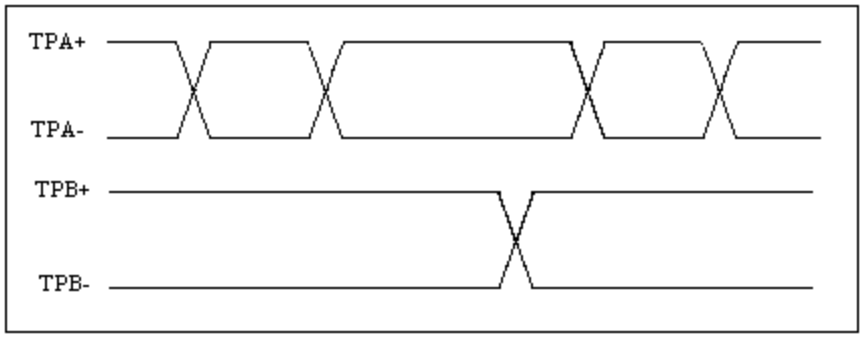
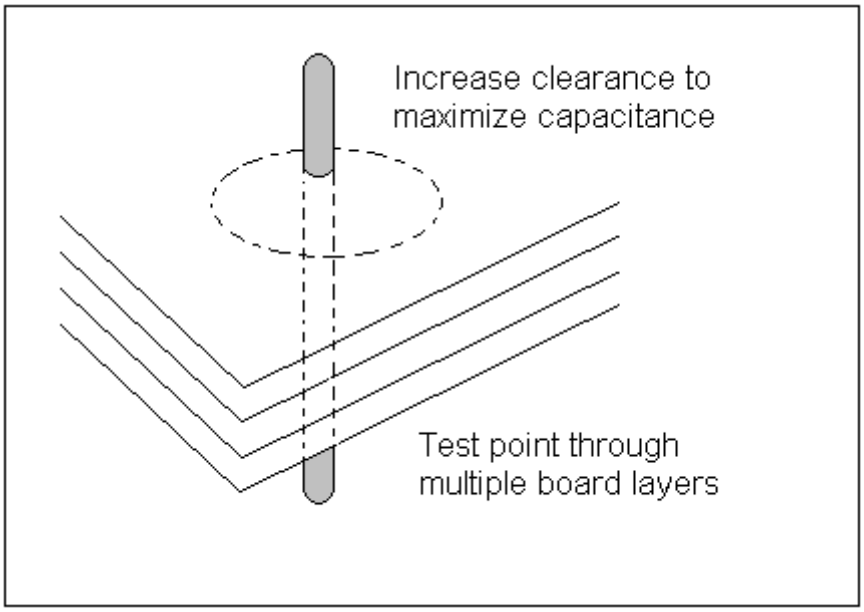


Figure 7. TPB pair etches matched to each other but longer than TPA pair



4) The etch lengths for the TPA+ and TPA- must be matched. For the same reasons, the TPB+ and TPB- etch lengths must be the same. In both cases this is required to reduce the skew in the differential signals (skew is measured by comparing the propagation delay on the two signals being measured). The sensed difference between the TPx+ and TPx- signals is what is sensed at the receiver to determine a one or a zero. Any difference in length will change the timing relationship between the signals, reducing the skew margin built into the system, (see Figure 5 for an illustration). Also related to this, the TPA pair should have approximately the same etch length as the TPB pair for a single port. The Data-Strobe encoding of the data being sent across the twisted pair depends on the relative timing between the “1”s and “0”s being signaled on the TPA and TPB differential pairs. If the delay of the signals through the etches is different, it will change the timing relationship of these signals, again reducing the skew margin of the coding. Therefore the etch lengths of the twisted pairs should be kept as close to the same as possible.

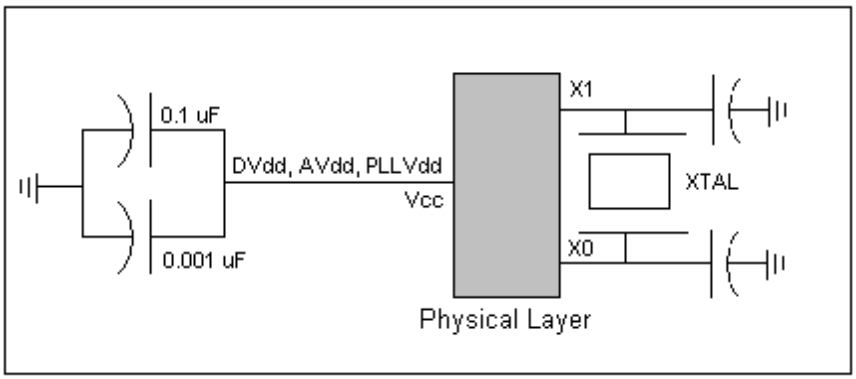
Figure 8. Via are more likely to pick up interference from other layers of the board



5) Try to minimize the number of vias in the twisted pair lines. When a via must be used, try to increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities into the signal's transmission line and increases the chance of picking up interference from the other layers of the board. For similar reasons be careful of using through-hole pins for test points on the twisted pair lines. Through-hole pins add inductance to the transmission line, which can reduce the signal integrity.

6) Keep the 24.576 MHz crystal and its load capacitors as close as possible to the PHY pins x0 and x1. (Refer to Figure 9). The greater the distance the more the chances of interference from noise which can interfere with the frequency lock of the internal Phase Locked Loop (PLL). The external crystal and internal oscillator drive the internal phase-locked loop, which generates the required reference signal. The reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information and the system clock (SCLK) sent to the link layer to synchronize the PHY-Link interface.

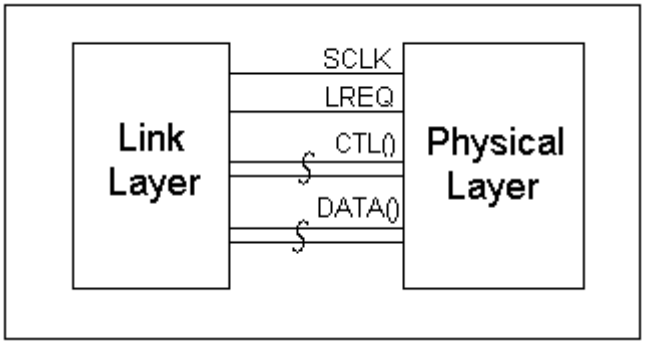
Figure 9. Power Supply and Clock Connection to the Physical Layer



7) Place power decoupling capacitors as close as possible to the PHY power supply pins. It is recommended that both 0.1μF and 0.001 μF capacitors be utilized. The capacitors create a filter to reduce the noise coupled into the device across the power plane, which helps maintain signal integrity. Keeping the etch short between the capacitors and the device minimizes the stub antenna, minimizing the noise coupled in on the device side of the filter network.

8) If you are using a switching power regulator to produce the regulated physical layer power from the unregulated cable power or from another higher voltage supply, it should be placed carefully. The switching regulator should be kept away from, specifically, the twisted pair etches, the external clock crystal (or clock oscillator if used), and the physical layer device in general. Switching regulators are a source of noise and if placed close to sensitive areas on a circuit board it increases the chance of the noise being coupled into a sensitive signal.

Figure 10. The Phy/Link interface signals should be close and have the same etch length



9) Try to keep the PHY-Link interface (SCLK, LREQ, CTL [0,1], and DATA [0:x] short (less than 4 inches if practical). The signals driven across the PHY-Link interface are at 3.3V CMOS levels (if both link and PHY are 3.3V CMOS) but are at 49.152 MHz and should be treated with due care. These signals should also all be approximately the same length. (Refer to Figure 10). The short distance is to minimize noise coupling from other devices and signal loss due to resistance. They should be kept the same length to reduce propagation delay mismatches across this synchronous interface.

EMI Interference

The significance of electromagnetic compatibility (EMC) of electronic circuits and systems has led to more stringent requirements for the electromagnetic properties of equipment. The EMC of an electronic circuit is mainly determined by how components are laid out with respect to each other and by how electrical connections are made between components.

Every current flowing in a line generates a current of the same magnitude flowing in a corresponding return line. This loop creates an antenna that can radiate electromagnetic energy whose magnitude is determined by the current amplitude, repetition frequency of the signal, and the geometry of the current loops.

One strategy to reduce radiated EMI is to terminate the SCLK signal to ensure a clean clock signal. This may be done with an approximately 10 to 20 Ohm series resistor at the source (PHY) side of the SCLK signal to increase the source impedance and reduce reflections. The impedance value used will be a function of the characteristic impedance of your board. In order to minimize the change in delays on the PHY-Link interface the same termination should also be placed on the data lines, the control lines, and the LREQ line.

Additionally, to reduce the EMI that is propagated through the cable shield, experiment with different values for the capacitors used in the parallel RC network to isolate the cable shield ground from chassis ground.

Additional recommendations to reduce EMI may be found in the TI application note “Printed Circuit Board Layout for Improved Electromagnetic Compatibility” at http://www.ti.com/sc/docs/psheets/appnote.htm.

- Ensure ground return paths are as close as possible to signal paths
- Avoid discontinuities in ground return paths
- Isolated ground planes should be capacitively coupled together to provide a signal return path
- Avoid sensitive signals or antennas when running traces especially digital signal traces.