

Section 6

DATA TRANSMISSION
IEEE1394 / FireWire

NOTICE

This presentation is a single chapter from
the 1996 Mixed Signal Products Seminar.

This presentation includes notes which can
be read in the notes page view.

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Why IEEE1394?

- Higher Throughputs
- Smaller Interconnects
- I/O Uniformity
- Digital Audio/Video Transmission
- “Plug and Play” Reliability/Durability

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Figure 6-44 Why IEEE1394?

IEEE1394 is a new bus interface standard being developed by an IEEE committee which describes a high speed serial bus that is designed for low system cost, while still providing the data transfer rate needed for a high performance peripheral bus.

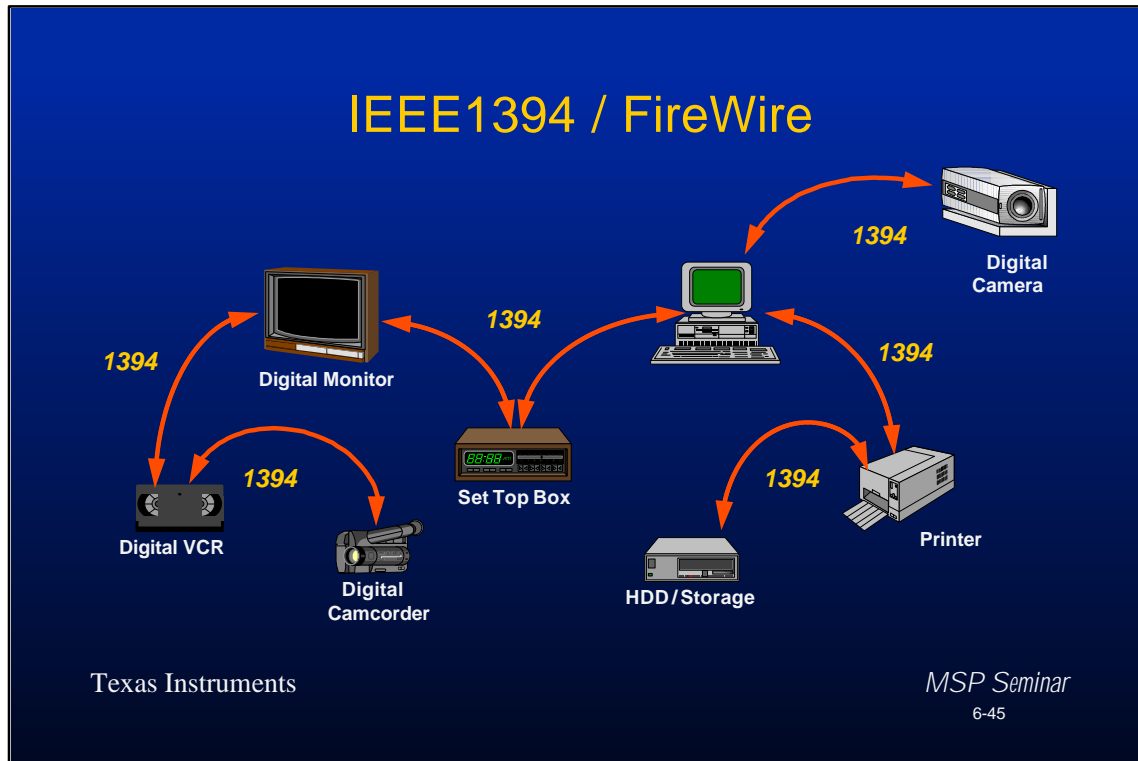


Figure 6-45 IEEE1394 / FireWire

IEEE1394 allows multiple devices of all types to be connected in a daisy chain fashion to a PC for high speed digital multimedia and high bandwidth applications. IEEE1394 can connect your PC to a set top box, digital monitor/TV, DVCR, camera, HDD, printer, plotter and much more. Devices using 1394 exist today with a large number of 1394-compliant devices currently in production. Get tomorrow's interface connection today with IEEE1394.

Highlights of IEEE1394

- Automatic assignment of node addresses
- Compatibility of multi-rate transfers for 100, 200, and 400 Mbit/s
- Isochronous ('Real-Time') transmission of data
- Low system level cost
- Universal I/O solution

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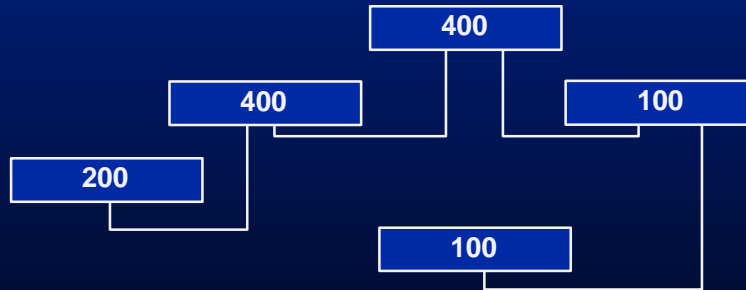
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Figure 6-46 Highlights of IEEE1394

1. There is no need for address switches due to the automatic assignment of node addresses.
2. As technology changes and data rates of 1394 increase, it will remain compatible with previous speeds.
3. The standard provides low overhead, guaranteed bandwidth and isochronous, i.e. real-time, data transmission. This transmission is dedicated for time critical data, e.g. digital video.
4. Low power devices may be powered through the 1394 cable, eliminating the need for a separate power source.
5. I/O port integration with 1394 and better space utilization with the smaller interconnects.

Other Benefits of Cable Topology

- Medium allows up to 16 connections of 4.5 m each, for total cable hop of 72 m
- Optimization of the protocol timing for smaller configurations
- Longer cable lengths possible
- 64 nodes addressable - up to 27 ports per node
- Allows branching and daisy chaining



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Figure 6-47 Other Benefits of Cable Topology

1. This allows 72 m of cabling distance between any two devices.
2. Gives optimum performance times for bus management.
3. Studies have been done to show that longer cable lengths are an option although they have not yet been adopted into the IEEE1394 Standard.

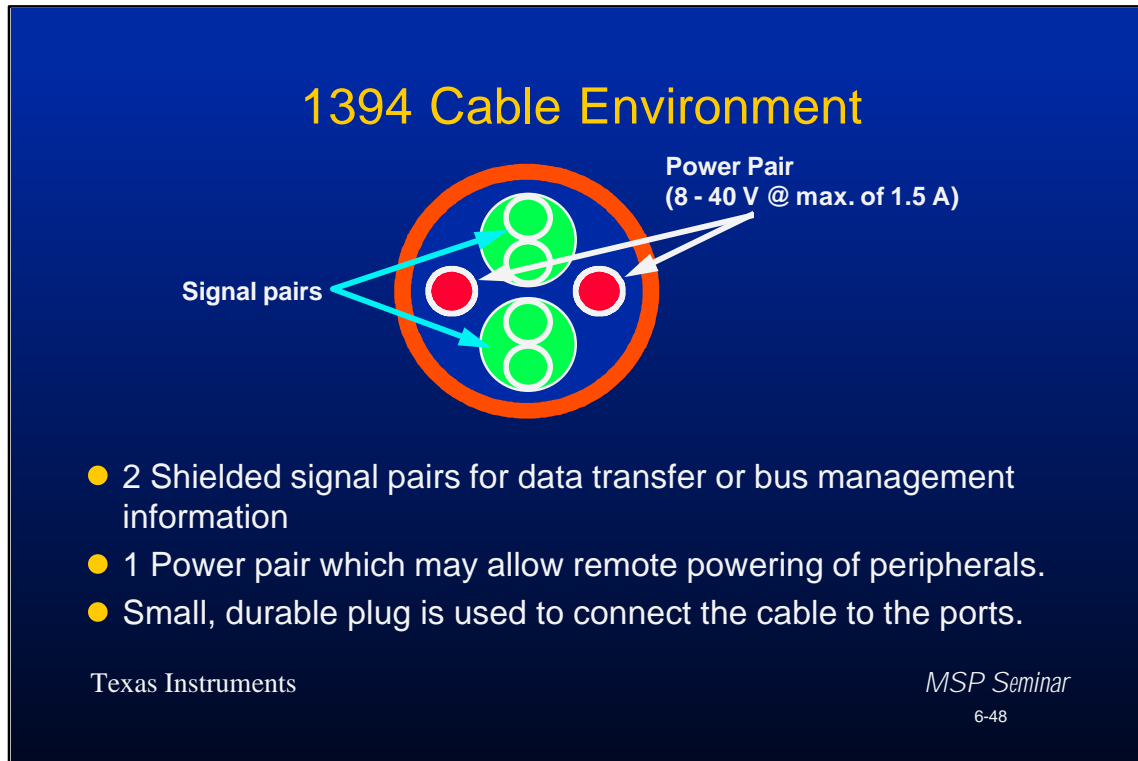


Figure 6-48 1394 Cable Environment

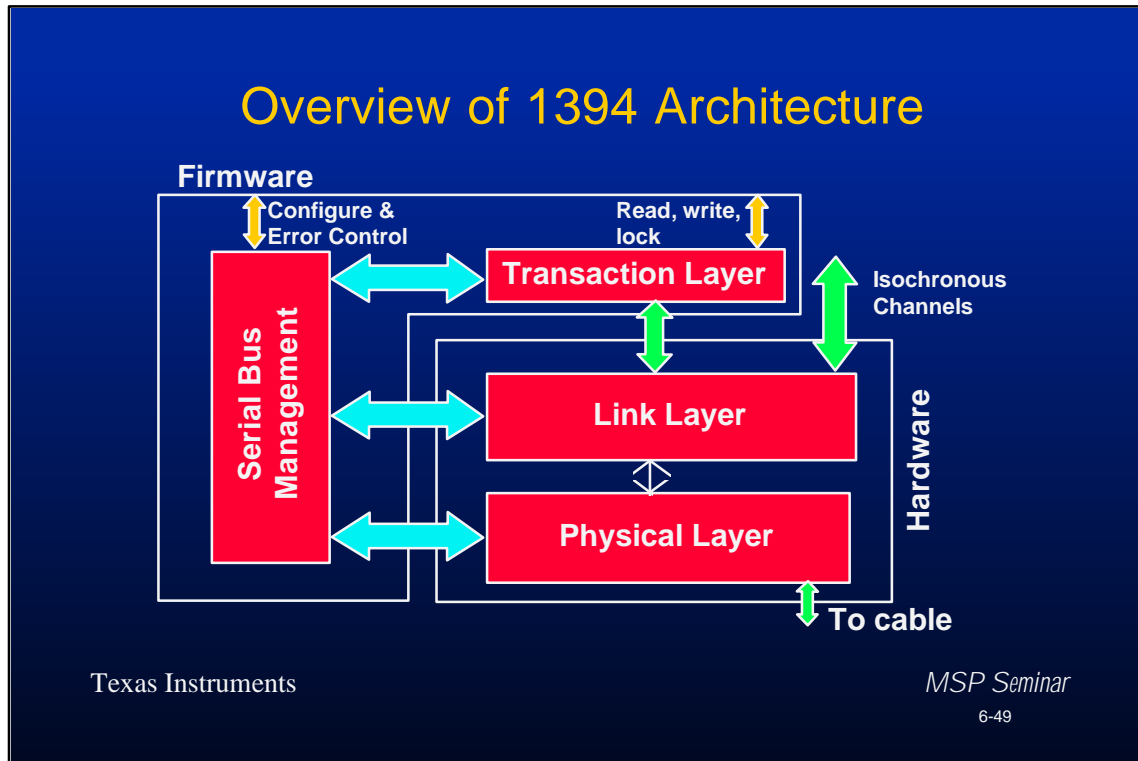


Figure 6-49 Overview of 1394 Architecture

The phy and the link are the hardware applications of 1394 and provide the direct interface to the cable environment as well as isochronous channels. Texas Instruments has developed the chipset to control the electrical connection to the cable which is made up of the:

TSB12C01A - Link Layer

TSB11C01 - Physical Layer

The software control of this hardware is implemented by the system layer architecture: serial bus management, and transaction layer.

Physical Layer (TSB11C01)

- Transmission and reception of data packets
- Arbitration
- Provision for the electrical and mechanical interface for three port node

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Figure 6-50 Physical Layer (TSB11C01)

The analog transceiver function is necessary to implement a 3 port node in the 1394 network. It is a set of 3 high speed, analog based transceivers which provide the electrical interface between different 1394 end equipment.

Link Layer

- Provides data transfer service between link and phy
- Transmits/Receives formatted 1394 packets
- Isochronous data transfer directly to the application

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Figure 6-51 Link Layer

The link layer provides the control for the transceiver or physical layer interface.

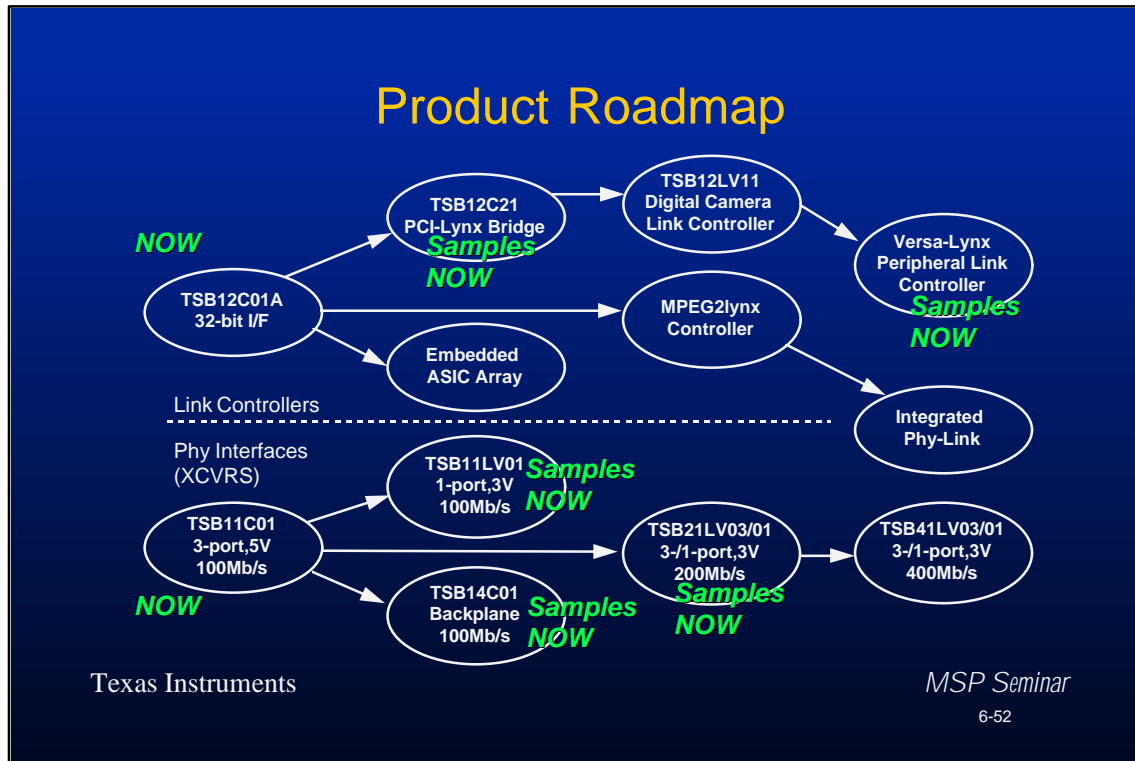


Figure 6-52 Product Roadmap

TSB12C01A Controller

Complies with IEEE1394 Serial-Bus Draft Standard

Supports speeds of 100, 200 or 400 Mb/s

Generic 32-bit host interface

Contains Asynchronous-, Isochronous- ("Real-Time") Transmit, and General-Receive FIFOs

Direct interface to TI's physical layer chips

PCILynx TSB12LV21

Complies with PCI bus specification revision 2.0

Supports Plug 'N Play specification

Provides complete PCI-to-1394 solution

Supports speeds of 100 and 200 Mbps

Programmable FIFOs

Five programmable DMA channels

8- or 16-bit zoom video (ZV) port for transferring data directly to an external video memory area; ZV port conforms to VESA and PCMCIA specifications

Direct interface to TI's physical layer chips