Texas Instruments Presents...

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MPEG2Lynx Agenda

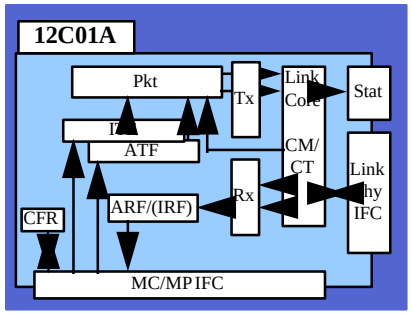
- Evolution
- Block Diagram
- System Diagrams
- Bulky Data Interface
- MicroC/P Interface
- Evaluation Board

Peripheral Link Evolution

IEEE-1394 LinkCore

Generic

12C01A



Cameras

DS-250

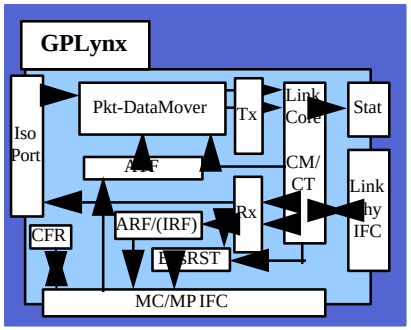
Cameras/Printers/Scanners/DVD/etc.

DV

Panasonic DV Camera w/ On Chip Phy

NV-DE3

GPLynx

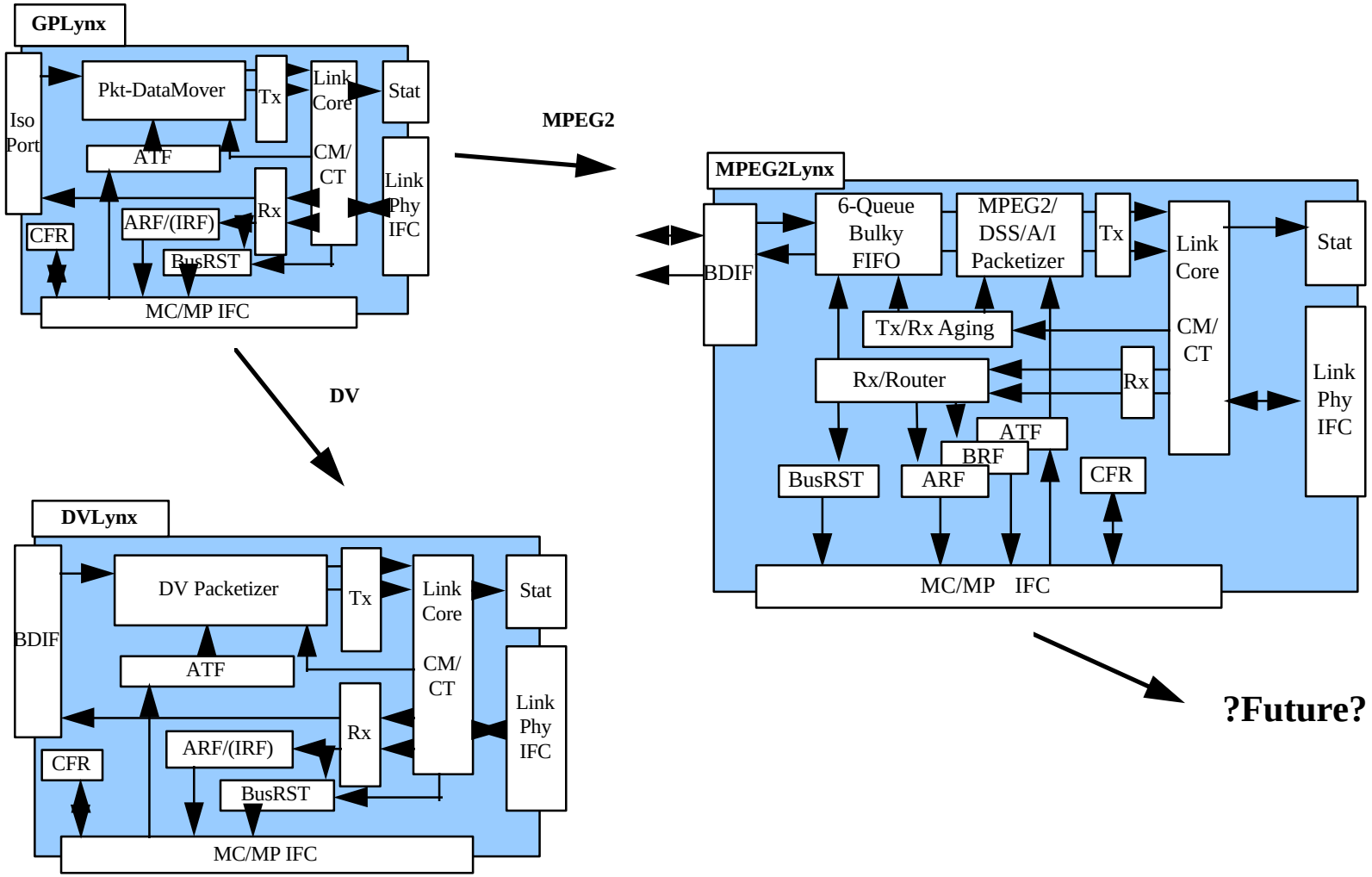


?Future?

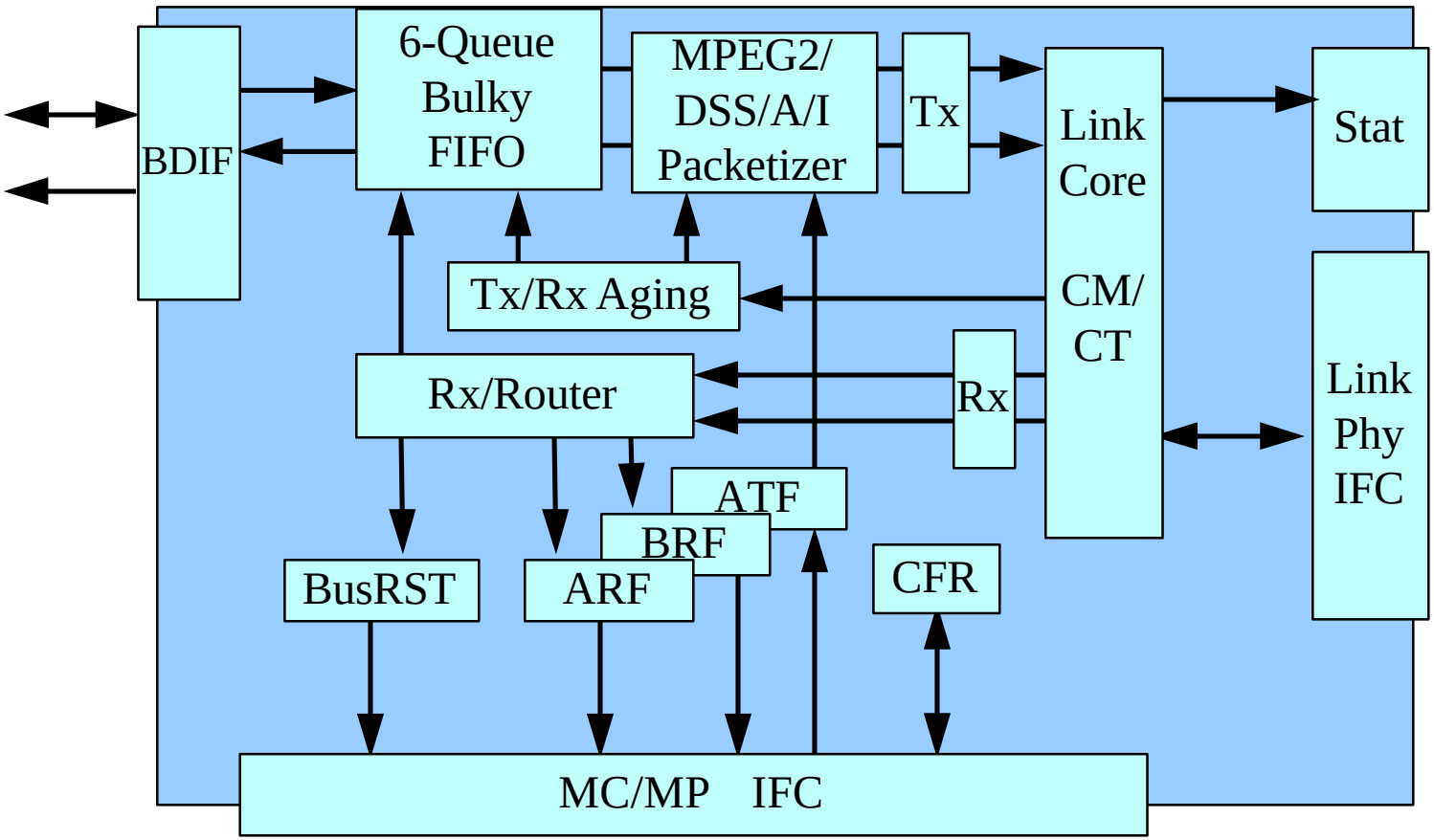
VX1000

PC-7

Peripheral Link Evolution Continues



MPEG2Lynx Architecture



MPEG2Lynx Features

- Fully Inter-operable with FireWire ™ Implementation of IEEE 1394–1995
- 3.3–V Supply Operation with 5–V Tolerance using 5–V Bias Terminals
- Supports Transfer Rates of 100/200 Mbps
- Programmable Microcontroller Interface - 8/16 Bit Data Bus with Multiple Modes
- Endianess Byte Swapping in HW set by SW
- 100 Pin TQFP

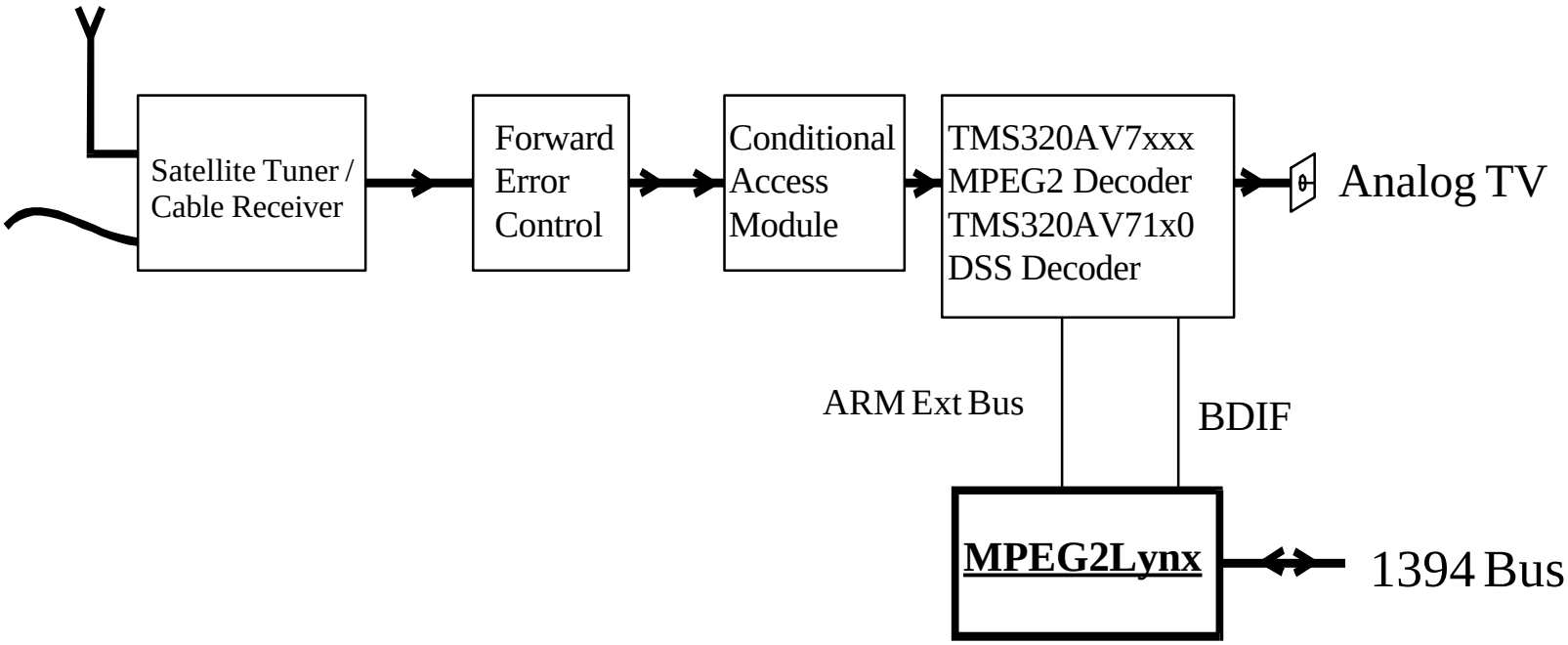
MPEG2Lynx Features

- Supports MPEG2 Formatted Isochronous Data Transfer According to IEC1883
- Supports DSS Formatted Isochronous Data Transfer
- Supports Full Time-stamp Offsets and Performs Age Filtering for MPEG2/DSS Rx/Tx.
- Supports Bi-Directional MPEG2 Transfers in the Same Isochronous Cycle

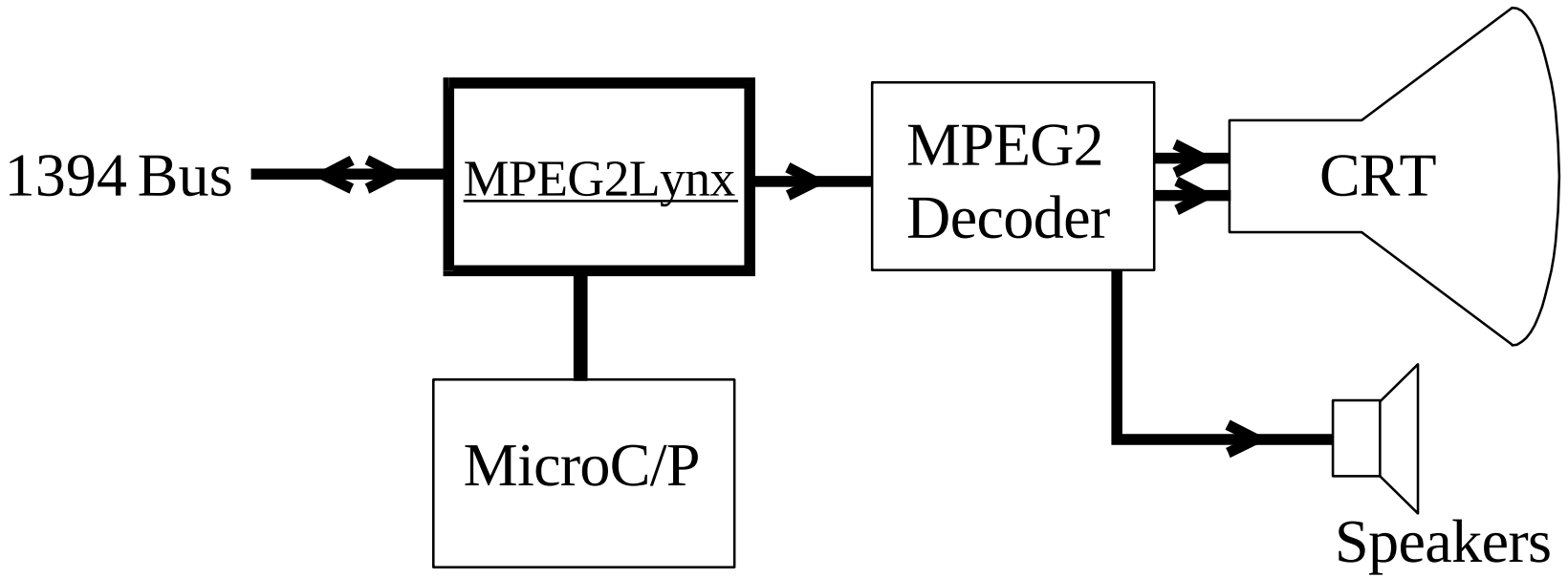
MPEG2Lynx Features

- Supports (Non-MPEG2/ DSS) Isochronous Transfers with Auto-packetization Feature
- Supports Asynchronous Transfers with Auto-packetization Feature
- Async DM Capability, Intimate Hooks for External DMA Implementation
- Supports Isochronous Transfers in Same Isochronous Period as MPEG2/DSS Transfers

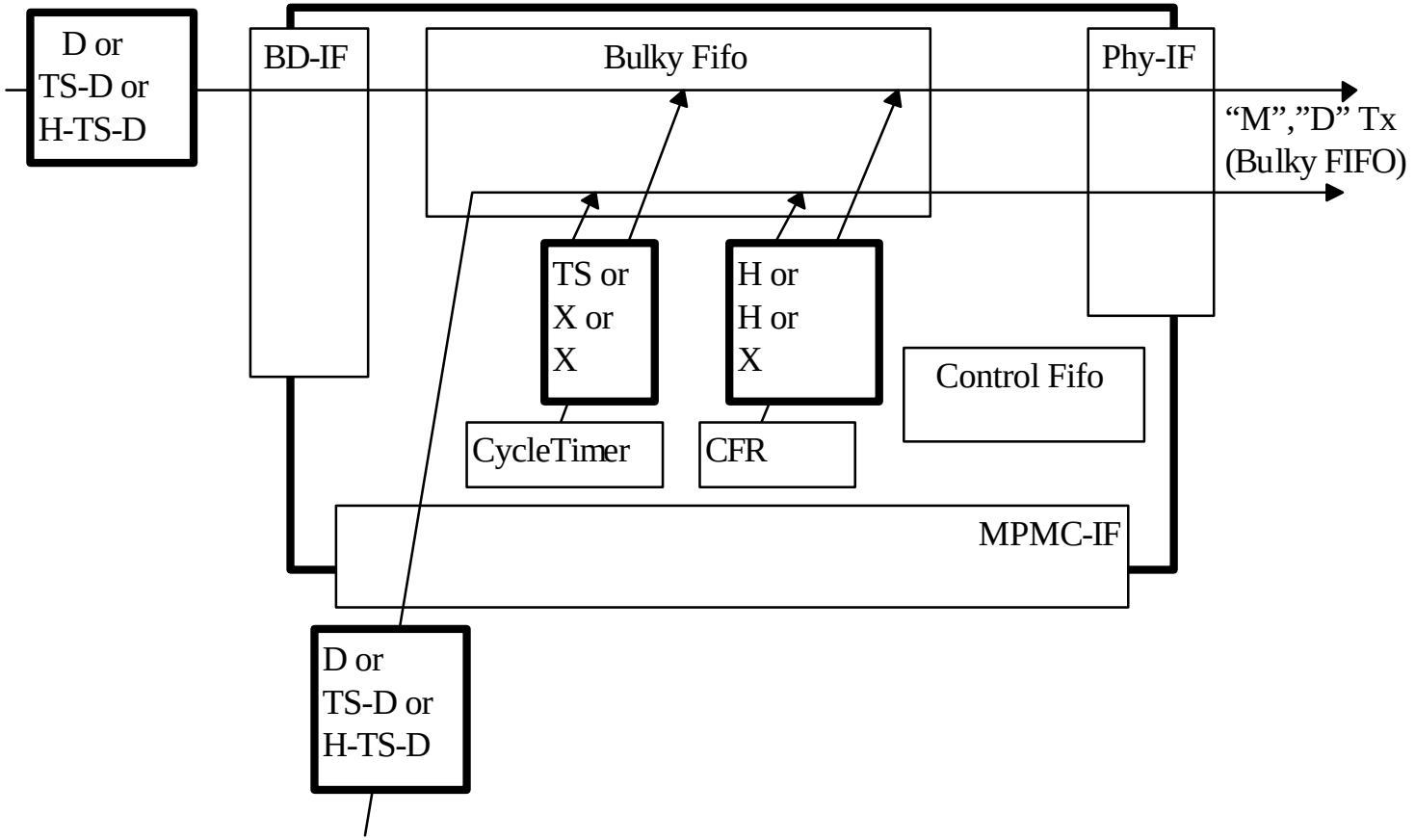
System Block Diagram (STB)



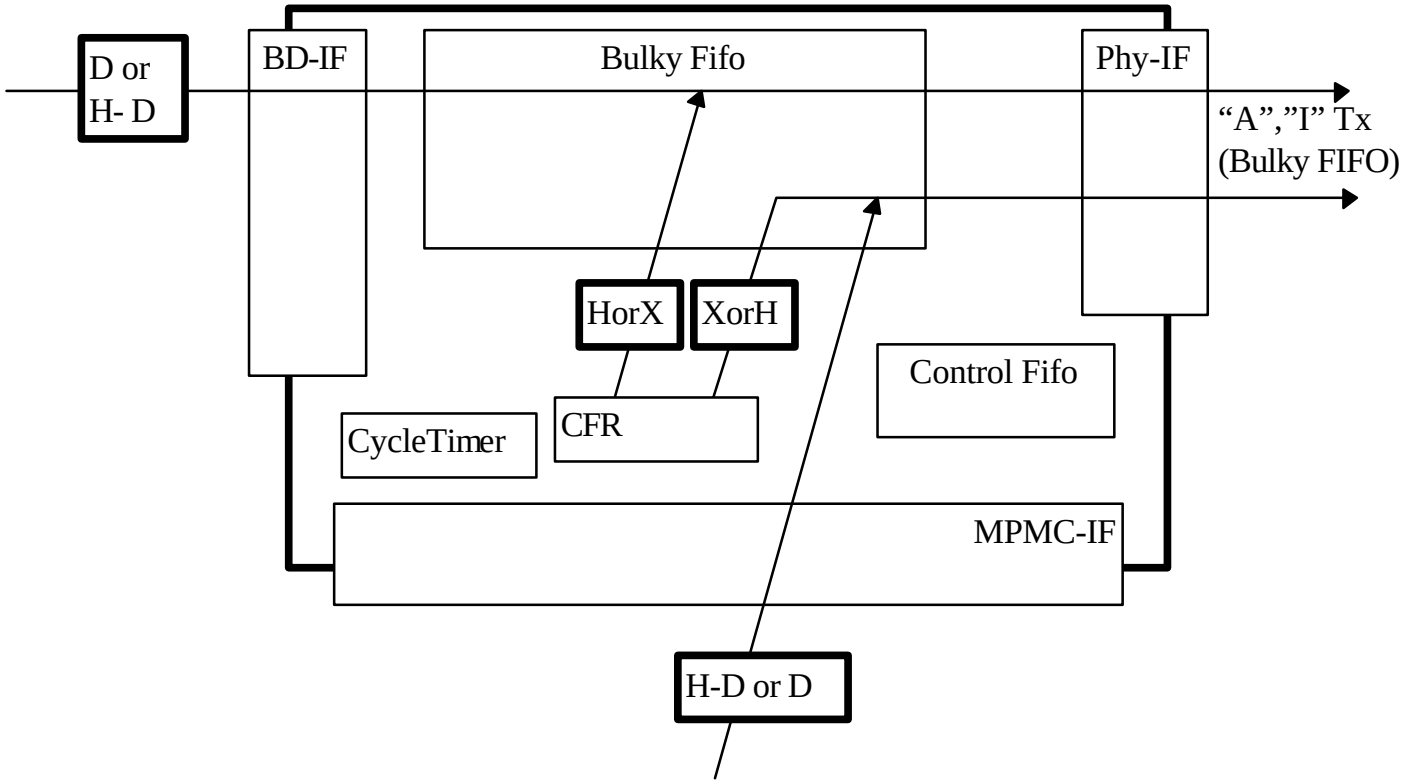
MPEG2 TV/Monitor



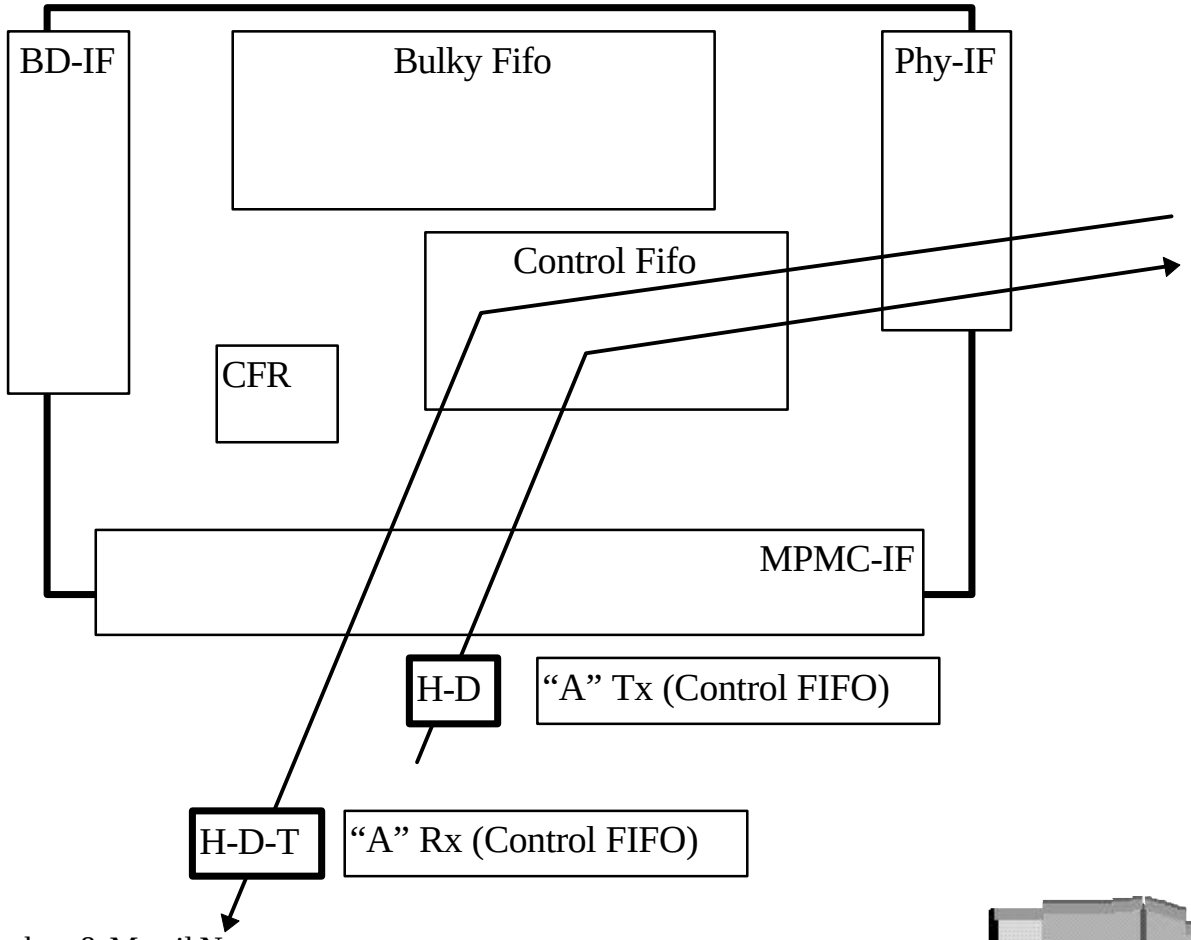
MPEG/DSS BDIF/Micro, Auto/Manual Header, Packet Paths



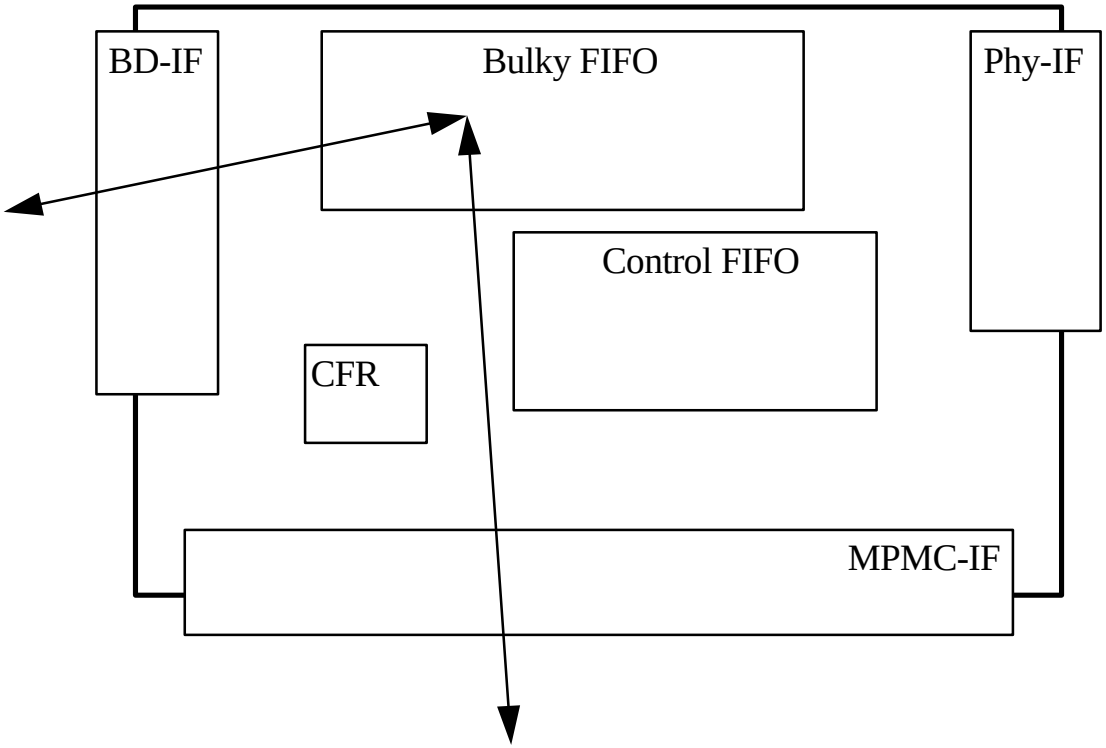
Transmit Isoc/Async, BDIF/Micro, Auto/Manual Header, Packet Paths



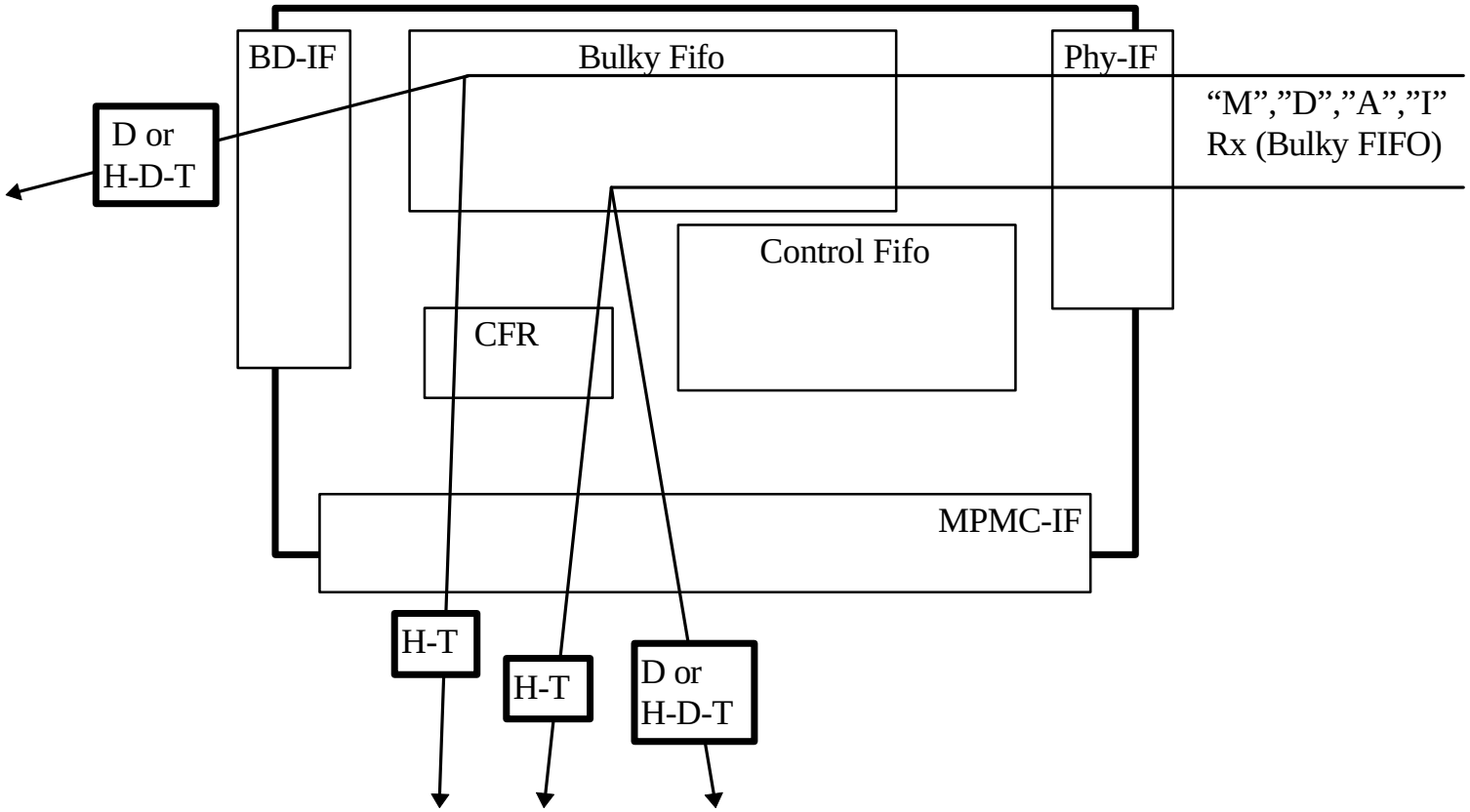
Transmit/Receive Async Path Through Control FIFO



Send Data Between Interfaces

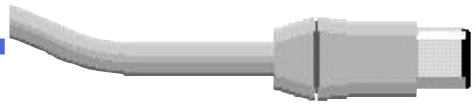


Packet Receives to BDIF/Micro



Bulky Data Interface (BDIF)

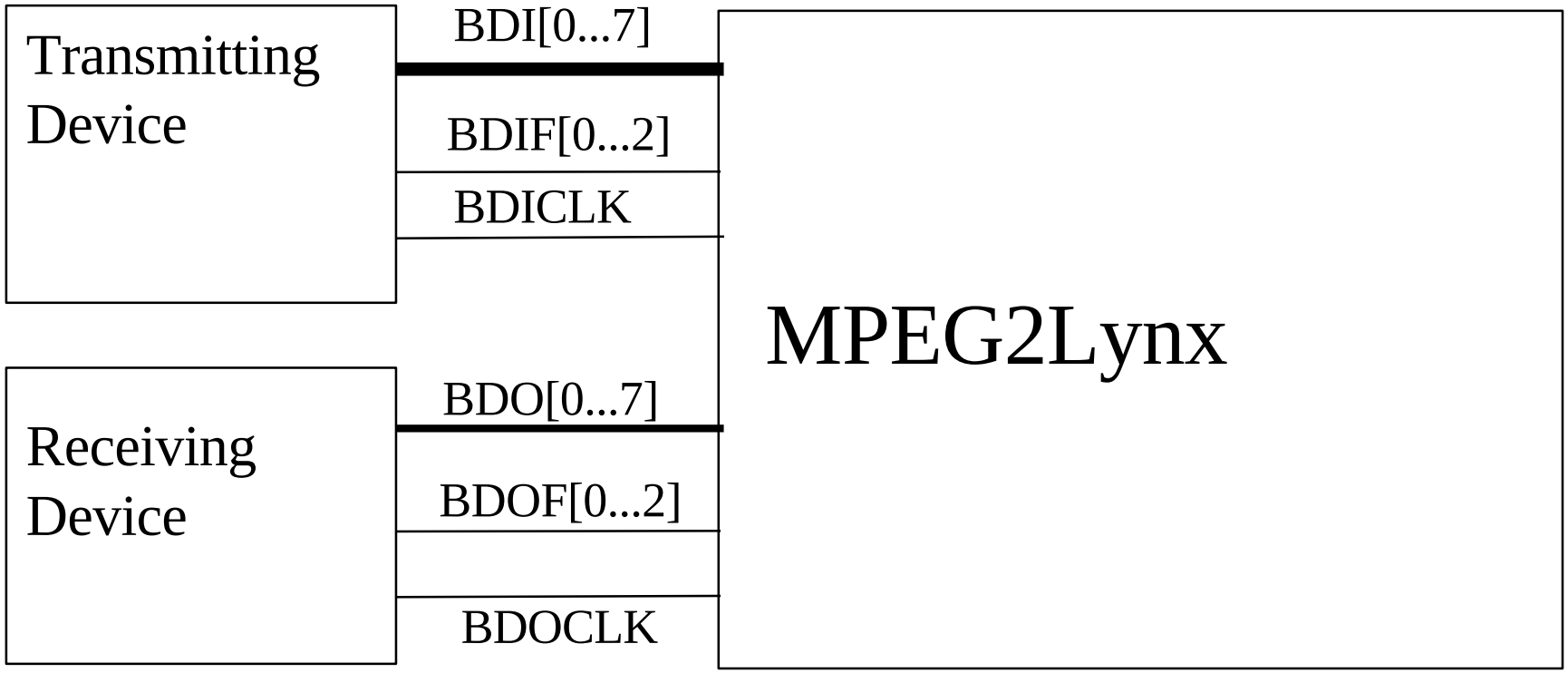
- Implements Bi-directional DVB/DSS, Async, Isoc, Compatible with TI TMS320AV7xxx MPEG2 Decoders
- Compatible with Unidirectional Mode of DSS Decoders



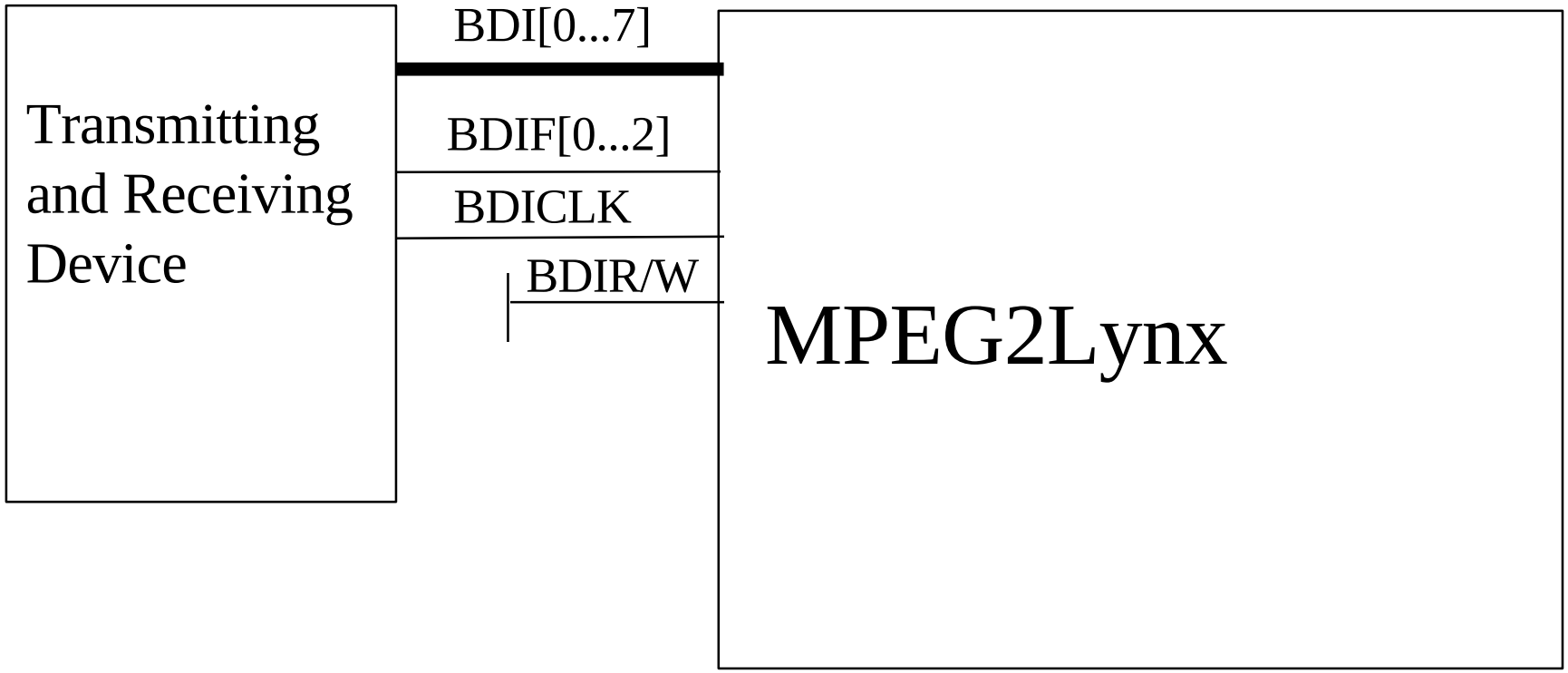
Bulky Data Interface (BDIF)

- Separate 8 bit Input and 8 bit Output Mode
- Multiplexed 8 bit Input/Output Mode
- Programmable Endianess

Separate Byte Wide Input & Output



Multiplexed Byte Wide



Micro Processor Interfacing

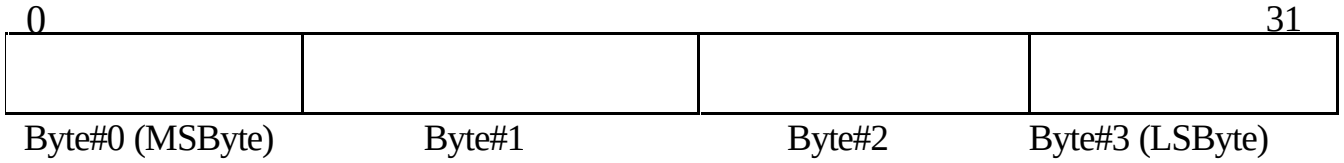
- TI MPEG TMS320AV7100, TI DSS TMS320AV7xxx Decoder Compatible (ARM)
- 68xxx Microcontroller Architecture compatible
- 8051 Microcontroller Architecture compatible

Micro Processor Interfacing

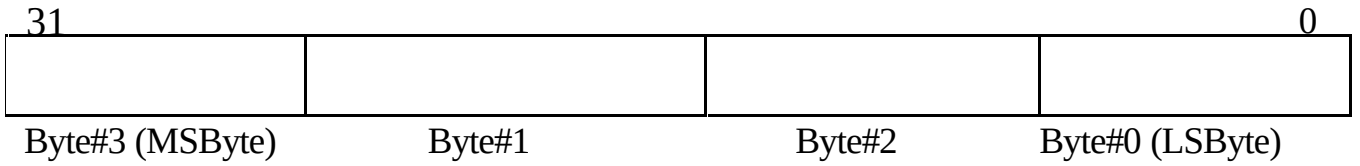
- Programmable Endianess
- “Blind” Access Mode to Unburden Micro

Endianess

Big Endian (1394, 68000, ARM)



Little Endian (TI DSP/Intel)



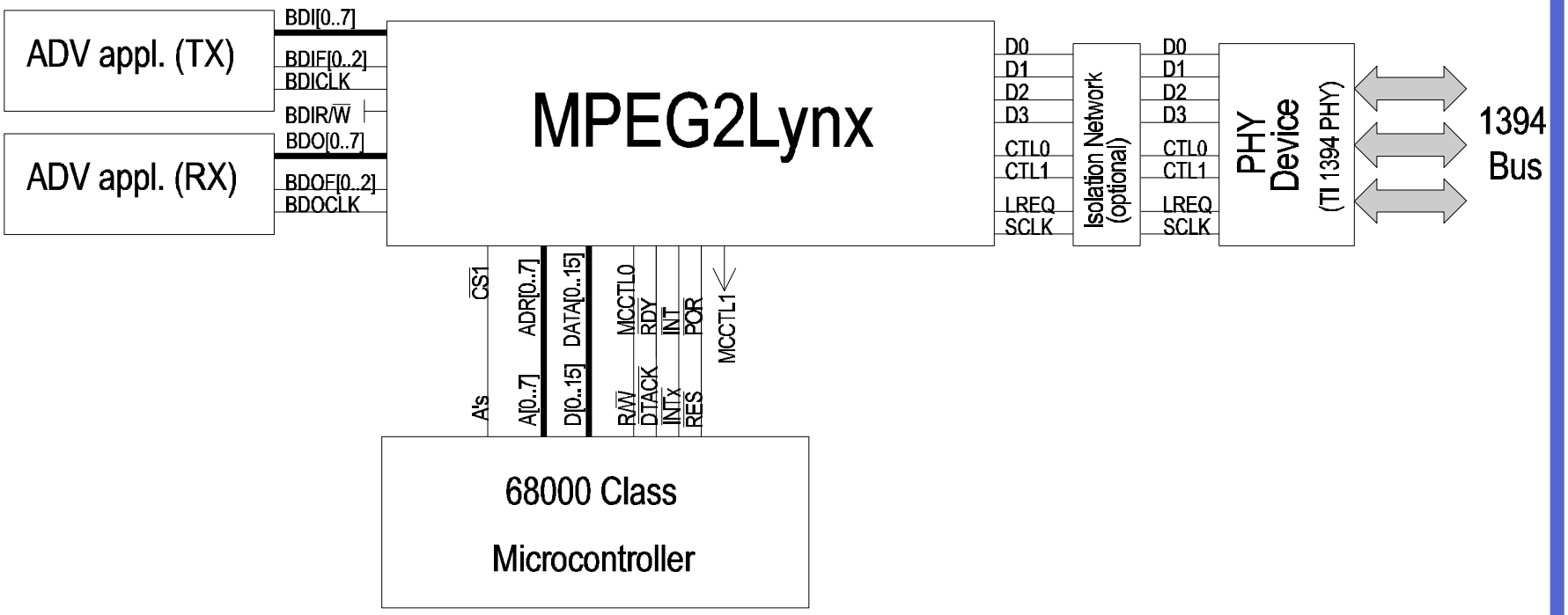
MPEG2Lynx Endianess

- Regardless of MicroP Endianess Connect MSbit of Micro to MSbit of TSB12LV41.
- Byte Swapping Is Done by TSB12LV41
  - Selectable by I/O Control Register Big Endian (BE) Bit and Data Invariant Endian Control (DIEC) Bit
  - Little Endian Processor
    - Address Invariant - BE bit=0, DIEC bit = 0
    - Data Invariant - BE bit = 0, DIEC bit = 1
  - Big Endian Processor
    - BE bit = 1, DIEC bit = Don’t Care if BE=1

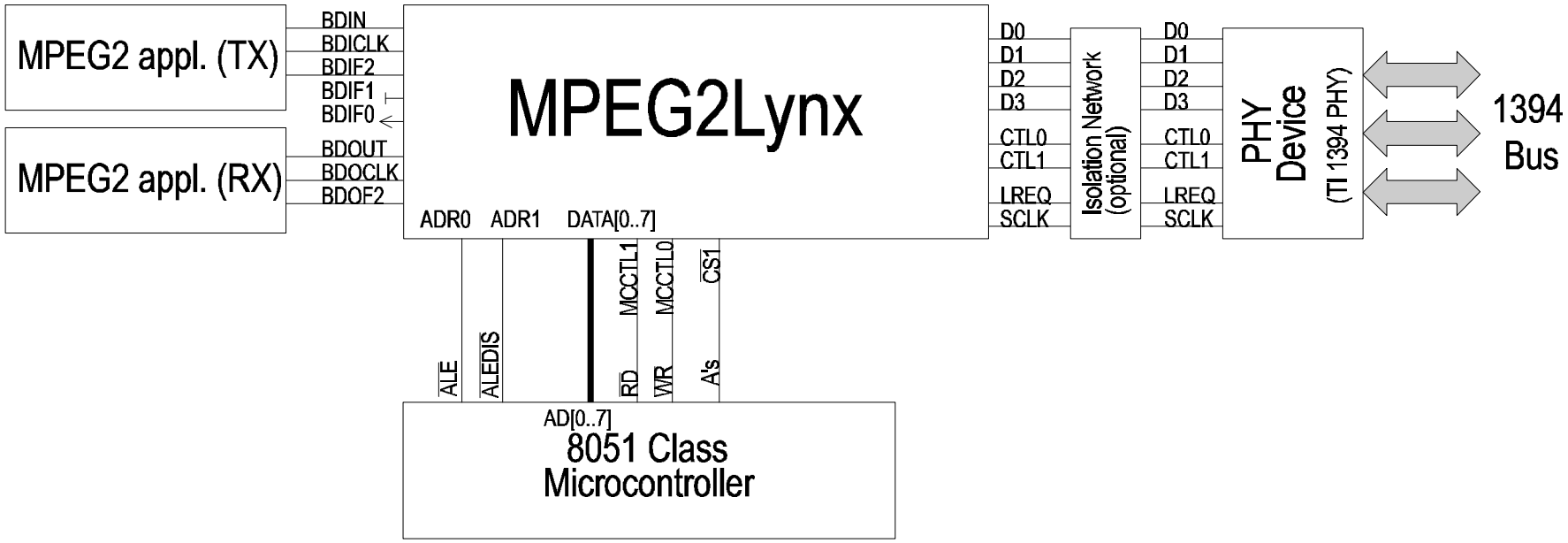
Blind Access Mode

- Currently Micro Asserts CS- and must wait for CA-, Could be Several Host Clock Cycles (Crossing Clock Domains)
- New Mode to not Hold Micro Waiting
  - Micro Asserts CS-, MPEG2Lynx Returns CA- Almost Immediately, (1 Clock Domain)
  - Repeat until 1 Quadlet is Placed into MPEG2Lynx
  - Micro May Then Poll a Register Bit for Transaction Completion Status

Big Endian (68000) Connection



Little Endian (8051) Connection



MPEG2Lynx EVM

- Interfacing Between PCI bus and MPEG2Lynx
- Connections to 200Mbps and 100Mbps Physical Layer
- Ability to Tristate all Signals to MPEG2Lynx Allowing Connection for External HW & Microcontroller

TSBKMPEG2 Block Diagram