TSB12C01A
Data Manual

1394 High-Speed Serial-Bus Link-Layer Controller

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TEXAS INSTRUMENTS

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1 Overview

1.1 Description

The TSB12C01A is an IEEE-1394 standard (from now on referred to only as 1394) high-speed serial-bus link-layer controller that allows for easy integration into an I/O subsystem. The TSB12C01A transmits and receives correctly formatted 1394 packets and generates and inspects the 32-bit cyclic redundancy check (CRC). The TSB12C01A is capable of being a cycle master and supports reception of isochronous data on two channels. It interfaces directly to the TSB11C01, TSB11LV01, and TSB21LV03 physical-layer chips and can support bus speeds of 100, 200, and 400 Mb/s. The TSB12C01A has a generic 32-bit host bus interface, which makes connection to most 32-bit host buses very simple. The TSB12C01A has software-adjustable FIFOs for optimal FIFO size and performance characterization and allows for variable-size asynchronous-transmit FIFO (ATF), isochronous-transmit FIFO (ITF), and general-receive FIFO (GRF).

This document is not intended to serve as a tutorial on 1394; users should refer to the IEEE draft standard 1394 serial bus for detailed information regarding the 1394 high-speed serial bus.

1.2 Features

The following are features of the TSB12C01A.

1.2.1 Link

- Complies With IEEE-1394 Standard Version 7.1v1
- Transmits and Receives Correctly Formatted 1394 Packets
- Supports Isochronous Data Transfer
- Performs Function of Cycle Master
- Generates and Checks 32-Bit CRC
- Detects Lost Cycle-Start Messages
- Contains Asynchronous, Isochronous, and General-Receive FIFOs

1.2.2 Physical-Link Interface

- Interfaces Directly to the TSB11C01, TSB11LV01, and TSB21LV03 Phy Chips
- Supports Speeds of 100, 200, and 400 Mb/s
- Implements the Physical-Link Interface Described in Annex J of the IEEE-1394 Standard

1.2.3 Host Bus Interface

- Provides Chip Control With Directly Addressable Registers
- Is Interrupt Driven to Minimize Host Polling
- Has a Generic 32-Bit Host Bus Interface

1.2.4 General

- Requires a Single 5-V ±5% Power Supply
- Manufactured with low-Power CMOS Technology
- Packaged in a 100-Pin thin quad flat package (TQFP) (PZ Package)

2 Architecture

2.1 Functional Block Diagram

The functional block architecture of the TSB12C01A is shown in Figure 2–1.

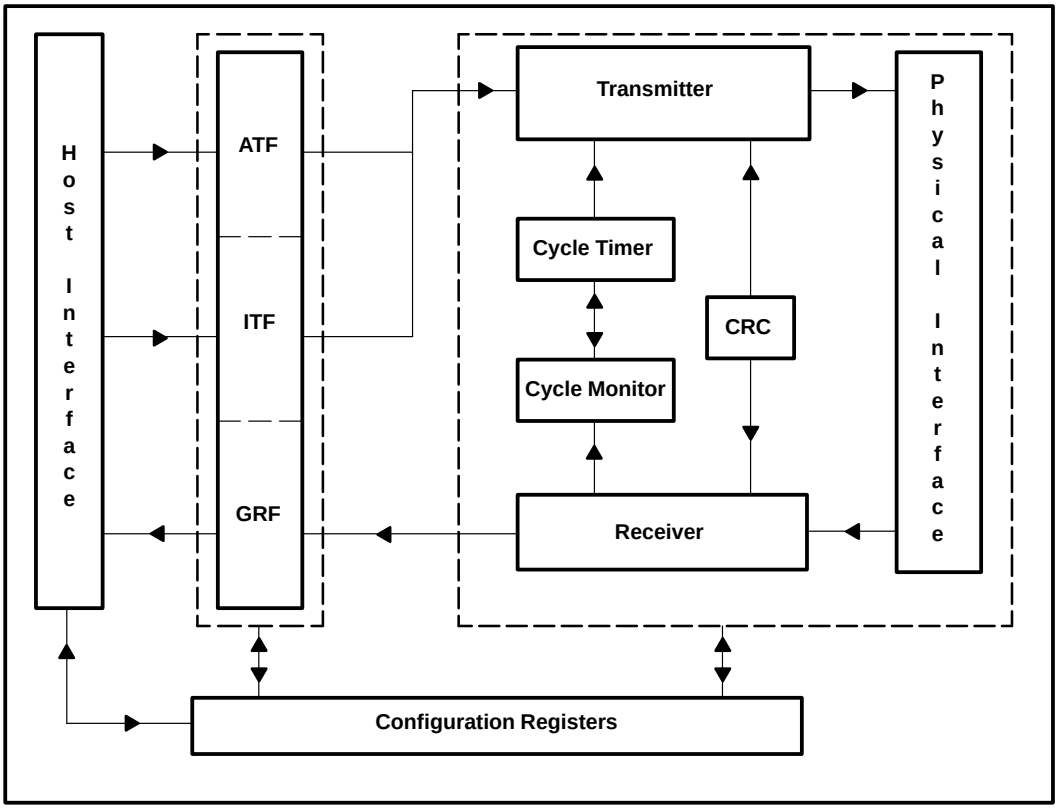


Figure 2–1. TSB12C01A Block Diagram

2.1.1 Physical Interface

The physical (phy) interface provides phy-level services to the transmitter and receiver. This includes gaining access to the serial bus, sending packets, receiving packets, and sending and receiving acknowledge packets.

The phy interface module also interfaces to the phy chip and conforms to the phy-link interface specification described in Annex J of the IEEE-1394 standard (refer to section 7 of this document for more information).

2.1.2 Transmitter

The transmitter retrieves data from either the ATF or the ITF and creates correctly formatted serial-bus packets to be transmitted through the phy interface. When data is present at the ATF interface to the transmitter, the TSB12C01A phy interface arbitrates for the serial bus and sends a packet. When data is present at the ITF interface to the transmitter, the TSB12C01A arbitrates for the serial bus during the next isochronous cycle. The transmitter autonomously sends the cycle-start packets when the chip is a cycle master.

2.1.3 Receiver

The receiver takes incoming data from the phy interface and determines if the incoming data is addressed to this node. If the incoming packet is addressed to this node, the CRC of the packet is checked. If the header CRC is good, the header is confirmed in the GRF. For block and isochronous packets, the remainder of the packet is confirmed one quadlet at a time. The receiver places a status quadlet in the GRF after the last quadlet of the packet is confirmed in the GRF. The status quadlet contains the error code for the packet. The error code is the acknowledge code that is sent for that packet. For broadcast packets that do not need acknowledge packets, the error code is the acknowledge code that would have been sent. This acknowledge code tells the transaction layer whether or not the data CRC is good or bad. When the header CRC is bad, the header is flushed and the rest of the packet is ignored.

When a cycle-start message is received, it is detected and the cycle-start message data is sent to the cycle timer. The cycle-start messages are not placed in the GRF like other quadlet packets. At the end of an isochronous cycle and if the cycle mark enable (CyMrkEn) bit of the control register is set , the receiver inserts a cycle-mark packet in the GRF to indicate the end of the isochronous cycle.

2.1.4 Transmit and Receive FIFOs

The TSB12C01A contains two transmit FIFOs (asynchronous and isochronous) and one receive FIFO (general receive). Each of these FIFOs are one quadlet wide and their length is software adjustable. These software-adjustable FIFOs allow customization of the size of each FIFO for individual applications. The sum of all FIFOs cannot be larger than 509 quadlets. To understand how to set the size of the FIFOs, see sections 3.2.11 through 3.2.13. The transmit FIFOs are write only from the host bus interface, and the receive FIFO is read only from the host bus interface.

An example of how to use software-adjustable FIFOs follows:

> In applications where isochronous packets are large and asynchronous packets are small, the implementer can set the ITF and GRF to a large size (200 quadlets each) and set the ATF to a smaller size (100 quadlets). Notice that the sum of all FIFOs is less than or equal to 509 quadlets.

2.1.5 Cycle Timer

The cycle timer is used by nodes that support isochronous data transfer. The cycle timer is a 32-bit cycle-timer register. Each node with isochronous data-transfer capability has a cycle-timer register as defined in the IEEE-1394 standard. In the TSB12C01A, the cycle-timer register is implemented in the cycle timer and is located in IEEE-1212 initial register space at location 200h and can also be accessed through the local bus at address 14h. The low-order 12 bits of the timer are a modulo 3072 counter, which increments once every 24.576-MHz clock periods (or 40.69 ns). The next 13 higher-order bits are a count of 8, 000-Hz (or 125 μs)cycles, and the highest 7 bits count seconds.

The cycle timer contains the cycle-timer register. The cycle-timer register consists of three fields: cycle offset, cycle count, and seconds count. The cycle timer has two possible sources. First, if the cycle source (CySrc) bit in the configuration register is set, then the CYCLEIN input causes the cycle count field to increment for each positive transition of the CYCLEIN input (8 kHz) and the cycle offset resets to all zeros. CYCLEIN should only be the source when the node is cycle master. When the cycle-count field increments, CYCLEOUT is generated. The timer can also be disabled using the cycle-timer-enable bit in the control register. See section 3.2.5, Cycle-Timer Register for more information.

The second cycle-source option is when the CySrc bit is cleared. In this state, the cycle-offset field of the cycle-timer register is incremented by the internal 24.576-MHz clock. The cycle timer is updated by the reception of the cycle-start packet for the noncycle master nodes. Each time the cycle-offset field rolls over, the cycle-count field is incremented and the CYCLEOUT signal is generated. The cycle-offset field in the cycle-start packet is used by the cycle-master node to keep all nodes in phase and running with a nominal isochronous cycle of 125 μs.

CYCLEOUT indicates to the cyclemaster node that it is time to send a cycle-start packet. And, on noncyclemaster nodes, CYCLEOUT indicates that it is time to expect a cycle-start packet. The cycle-start bit is set when the cycle-start packet is sent from the cyclemaster node or received by a noncyclemaster node.

2.1.6 Cycle Monitor

The cycle monitor is only used by nodes that support isochronous data transfer. The cycle monitor observes chip activity and handles scheduling of isochronous activity. When a cycle-start message is received or sent, the cycle monitor sets the cycle-started interrupt bit. It also detects missing cycle-start packets and sets the cycle-lost interrupt bit when this occurs. When the isochronous cycle is complete, the cycle monitor sets the cycle-done-interrupt bit. The cycle monitor instructs the transmitter to send a cycle-start message when the cycle-master bit is set in the control register.

2.1.7 Cyclic Redundancy Check (CRC)

The CRC module generates a 32-bit CRC for error detection. This is done for both the header and data. The CRC module generates the header and data CRC for transmitting packets and checks the header and data CRC for received packets. See the IEEE-1394 standard for details on the generation of the CRC†.

2.1.8 Internal Registers

The internal registers control the operation of the TSB12C01A. The register definitions are specified in section 3.

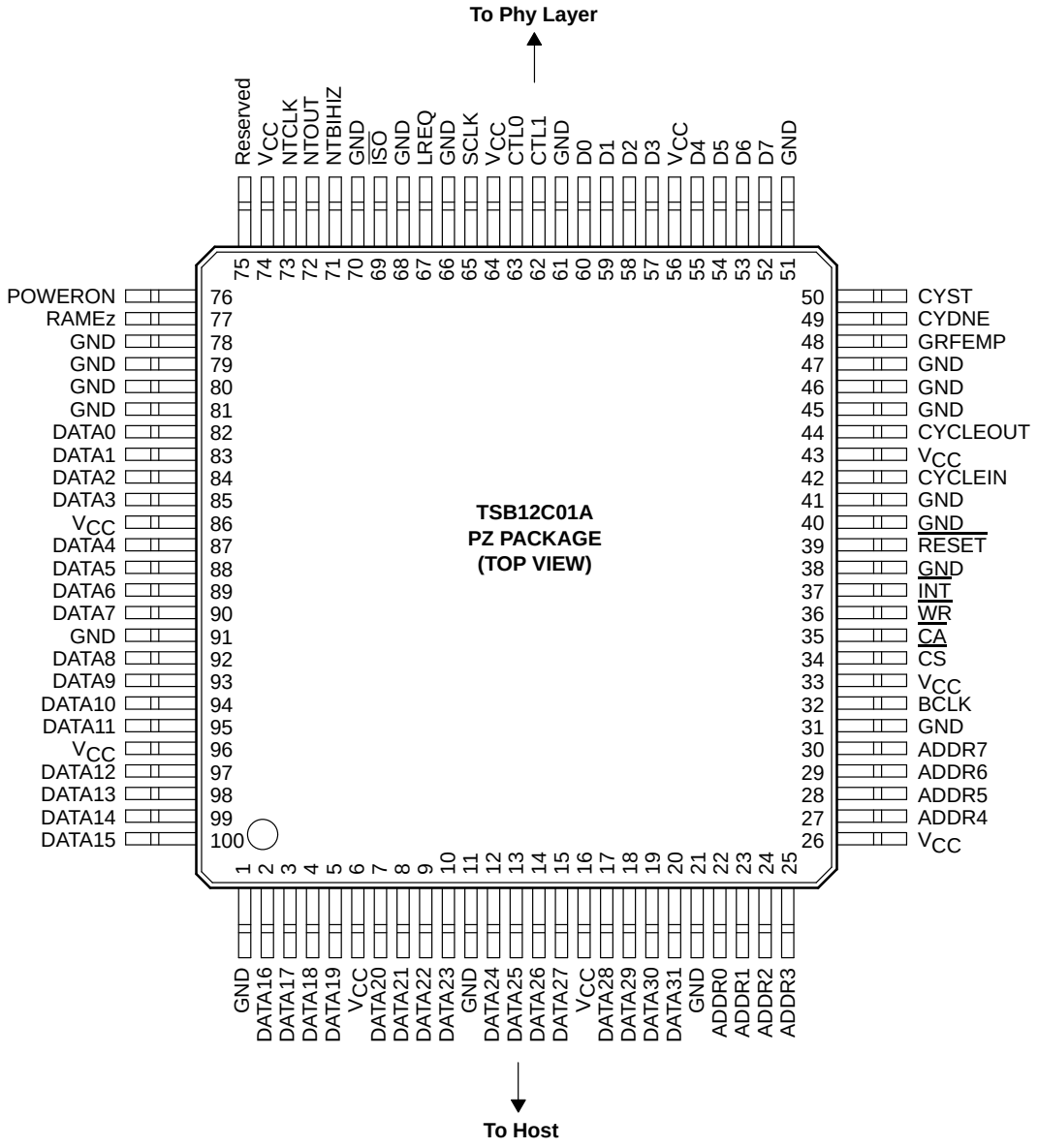
2.1.9 Host Bus Interface

The host bus interface allows the TSB12C01A to be easily connected to most host processors. This host bus interface consists of a 32-bit data bus and an 8-bit address bus. The TSB12C01A utilizes cycle-start and cycle-acknowledge handshake signals to allow the local bus clock and the 1394 clock to be asynchronous to one another. The TSB12C01A is interrupt driven to reduce polling.

† This is the same CRC used by the IEEE802 LANs and the X3T9.5 FDDI.

2.2 Terminal Assignments and Functions

2.2.1 Terminal Assignments



NOTES: A. Tie reserved terminals to GND.

B. Bit 0 is the most significant bit (MSB).

2.2.2 Terminal Functions

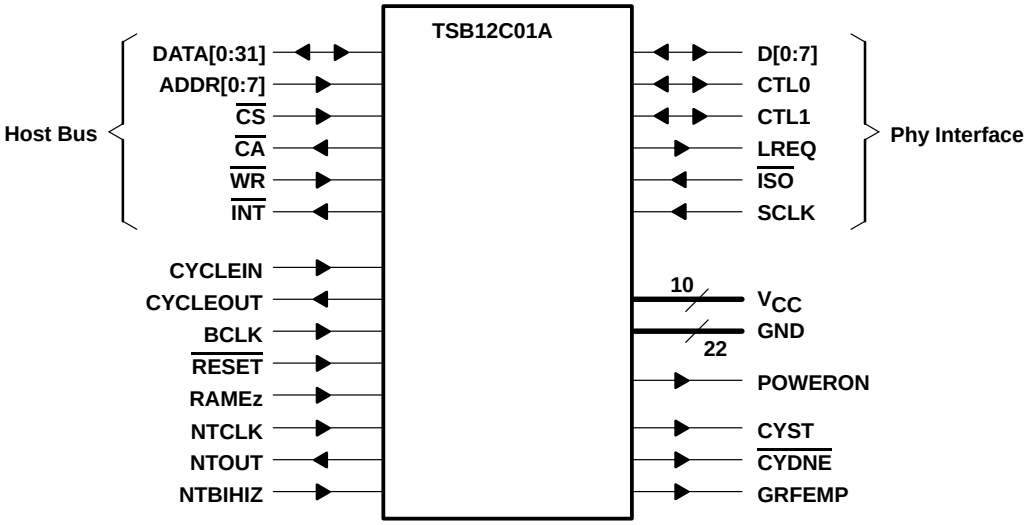


Figure 2–2. TSB12C01A Terminal Functions

2.2.3 TSB12C01A Terminal Functions

Table 2–1. Host Bus Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDR[0:7]	22–25 27–30	I	Address 0 through address 7. Host bus address bus bits 0 through 7 that address the quadlet-aligned FIFOs and configuration registers. The two least significant address lines, 6 and 7, must be grounded.
$\overline{CA}$	35	O	Cycle acknowledge (active low). $\overline{CA}$ is a TSB12C01A control signal to the host bus. When asserted (low), access to the configuration registers or FIFO is complete.
$\overline{CS}$	34	I	Cycle start (active low). $\overline{CS}$ is a host bus control signal to enable access to the configuration registers or FIFO.
DATA [0:31]	2–5 7–10 12–15 17–20 82–85 87–90 92–95 97–100	I/O	Data 0 through 31. DATA is a host bus data bus bits 0 through 31.
$\overline{INT}$	37	O	Interrupt (active low). When $\overline{INT}$ is asserted (low), the TSB12C01A notifies the host bus that an interrupt has occurred.
$\overline{WR}$	36	I	Read/$\overline{write}$ enable. When $\overline{WR}$ is deasserted (high) in conjunction with $\overline{CS}$, a read from the TSB12C01A is requested. When $\overline{WR}$ is asserted (low) in conjunction with $\overline{CS}$, a write to the TSB12C01A is requested.

Table 2–2. Phy Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CTL1, CTL0	62, 63	I/O	Control 1 and control 0 of the phy-link control bus. CTL1 and CTL0 indicate the four operations that can occur in this interface (see section 7 or annex J of the IEEE-1394 standard for more information about the four operations).
D[0:7]	52–55 57–60	I/O	Data 0 through data 7 of the phy-link data bus. Data is expected on D[0:1] for 100 Mb/s packets, D[0:3] for 200 Mb/s, and D[0:7] for 400 Mb/s.
$\overline{\text{ISO}}$	69	I	Isolation barrier (active low). This $\overline{\text{ISO}}$ is asserted (low) when an isolation barrier is present.
LREQ	67	O	Link request. LREQ is a TSB12C01A output that makes bus requests and accesses the phy layer.
POWERON	76	O	Power on indicator to phy interface. When active, POWERON has a clock output with 1/32 of the BCLK frequency and indicates to the phy interface that the TSB12C01A is powered.

Table 2–3. Miscellaneous Signals Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BCLK	32	I	Bus clock. BCLK is the host bus clock used in the host-interface module of the TSB12C01A. It is asynchronous to SCLK.
CYCLEIN	42	I	Cycle in. CYCLEIN is an optional external 8,000-Hz clock used as the cycle clock, and it should only be used when attached to the cycle-master node. It is enabled by the cycle source bit and should be tied high when not used.
CYCLEOUT	44	O	Cycle out. CYCLEOUT is the TSB12C01A version of the cycle clock. It is based on the timer controls and received cycle-start messages.
CYDNE	49	O	Status of CyDne bit. When the RevAEn bit of the control register is set, CYDNE indicates the value of the CyDne bit of the interrupt register. When RevAEn is cleared, CYDNE is a 3-state output.
CYST	50	O	Status of CySt bit. When the RevAEn bit of the control register is set, CYST indicates the value of the CySt bit of the interrupt register. When RevAEn is cleared, CYST is a 3-state output.
GND	1, 11, 21, 31, 38, 40, 41, 45–47, 51, 61, 66, 68, 70, 78–81, 91		Ground reference
GRFEMP	48	O	Status of Empty bit. When the RevAEn bit of the control register is set, GRFEMP indicates the value of the Empty bit of the GRF status register. When RevAEn is cleared, GRFEMP is a 3-state output.
RAMEz	77	I	RAM 3-state enable. When RAMEz is deasserted (low), FIFOs are enabled. When RAMEz is asserted, the FIFOs are 3-state outputs. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)
NTBIHIZ	71	I	NAND-tree bidirectional 3-state output. When NTBIHIZ is deasserted (low), the bidirectional I/Os operate in a normal state. When NTBIHZ is asserted (high), the bidirectional I/Os are in the 3-state output mode. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)

Table 2–3. Miscellaneous Signals Terminal Functions (Continued)

NTCLK	73	I	NAND clock input. The NAND-tree clock is used for V_{IH} and V_{IL} manufacturing tests. (This input should be grounded under normal operating conditions.)
NTOUT	72	O	NAND-tree output. This output should remain open under normal operating conditions.
$\overline{\text{RESET}}$	39	I	Reset (active low). $\overline{\text{RESET}}$ is the asynchronous reset to the TSB12C01A.
SCLK	65	I	System clock. SCLK is a 49.152-MHz clock from the phy, that generates the 24.576-MHz clock.
V_{CC}	6, 16, 26, 33, 43, 56, 64, 74, 86, 96		5-V ±5% power supplies

3 Internal Registers

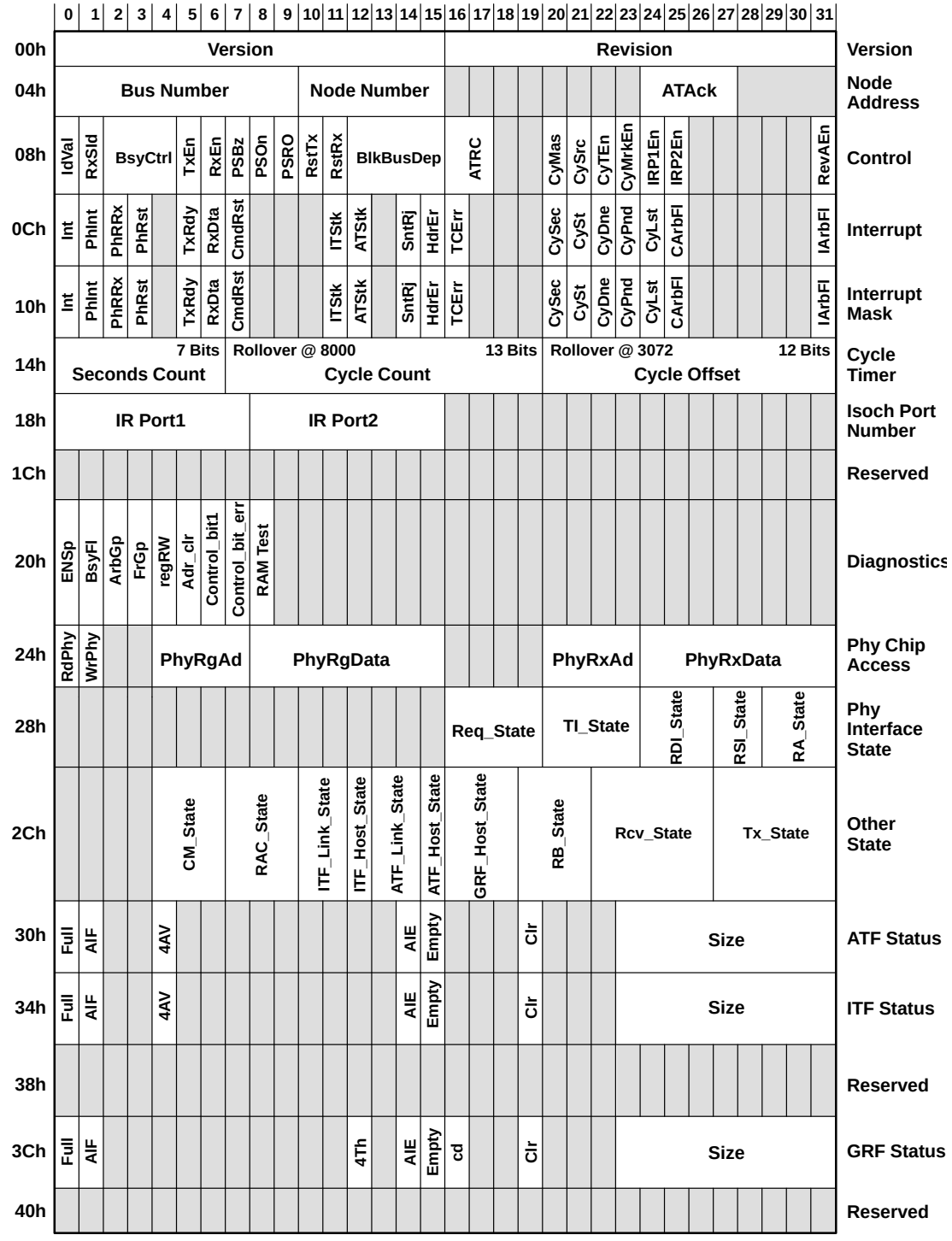
3.1 General

The host-bus processor directs the operation of the TSB12C01A through a set of registers internal to the TSB12C01A itself. These registers are read or written by asserting $\overline{CS}$ with the proper address on ADDR[0:7] and asserting or deasserting $\overline{WR}$ depending on whether a read or write is needed. Figure 3–1 lists the register addresses; subsequent sections describe the function of the various registers.

3.2 Internal Register Definitions

The TSB12C01A internal registers control the operation of the TSB12C01A. The bit definitions of the internal registers are shown in Figure 3–1 and are described in sections 3.2.1 through 3.2.13.

Figure 3–1. Internal Register Map



NOTE A: All gray areas (bits) are reserved bits.

3.2.1 Version/Revision Register

The version/revision register allows software to be written that supports multiple versions of the high-speed serial-bus link-layer controllers. This register is at address 00h and is read only. The initial value is 3031_3041h.

Table 3–1. Version/Revision Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–15	Version	Version	Version of the TSB12C01A
16–31	Revision	Revision	Revision of the TSB12C01A

3.2.2 Node-Address/Transmitter Acknowledge Register

The node-address/transmitter acknowledge register controls which packets are accepted/rejected, and it presents the last acknowledge received for packets sent from the ATF. This register is at offset 04h. The bus number and node number fields are read/write. The AT acknowledge (ATAck) received is normally read only. Setting the regRW bit in the diagnostic register makes these fields read/write. The initial value is FFFF_0000h.

Table 3–2. Node-Address/Transmitter Acknowledge Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–9	BusNumber	Bus number	BusNumber is the 10-bit IEEE 1212 bus number that the TSB12C01A uses with the node number in the SOURCE address for outgoing packets and to accept or reject incoming packets. The TSB12C01A always accepts packets with a bus number equal to 3FFh.
10–15	NodeNumber	Node number	NodeNumber is the 6-bit node number that the TSB12C01A uses with the bus number in the source address for outgoing packets and to accept or reject incoming packets. The TSB12C01A always accepts packets with the node address equal to 3Fh. See BlkBusDep bits for exceptions.
16–23	Reserved	Reserved	Reserved
24–27	ATAck	Address transmitter acknowledge received	ATAck is the last acknowledge received by the transmitting node in response to a packet sent from the asynchronous transmit-FIFO.
28–31	Reserved	Reserved	Reserved

3.2.3 Control Register

The control register dictates the basic operation of the TSB12C01A. This register is at address 08h and is read/write. The initial value is 0000_0000h.

Table 3–3. Control-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	IdVal	ID Valid	When IdVal is set, the TSB12C01A accepts packets addressed to the IEEE 1212 address set (Node Number) in the node-address register. When IdVal is cleared, the TSB12C01A accepts only broadcast packets.
1	RxSId	Received self-ID packets	When RxSId is set, the self-identification packets generated by phy chips during bus initialization are received and placed into the GRF as a single packet. Each self-identification packet is composed of two quadlets, where the second quadlet is the logical inverse of the first. If ACK (4 bits) equals 1h, then the data is good. If ACK equals Dh, then the data is wrong.

Table 3–3. Control-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
2–4	BsyCtrl	Busy control	These bits control which busy status the chip returns to incoming packets. The field is defined as below: 000 = follow normal busy/retry protocol, only send busy when necessary. 001 = send busyA when it is necessary to send a busy acknowledge. 010 = send busyB when it is necessary to send a busy acknowledge. 011 = reserved 100 = send a busy acknowledge to all incoming packets following the normal busy/retry protocol. 101 = send a busy acknowledge to all incoming packets by sending a busyA acknowledge. 110 = send a busy acknowledge to all incoming packets by sending a busyB acknowledge. 111 = reserved When retry_X is received and the receiving node needs to send a busy acknowledge signal, it sends an ack_busy_X signal.
5	TxEn	Transmitter enable	When TxEn is cleared, the transmitter does not arbitrate or send packets.
6	RxEn	Receiver enable	When is RXEn cleared, the receiver does not receive any packets.
7	PSBz	Physical DMA busy	When: 1) PSOn is set, 2) PSRO is cleared or the incoming packet is a read, 3) destination offset is in lower 4 Gbytes, and 4) PSBz is set, the TSB12C01A sends a busy acknowledge to the incoming packet.
8	PSOn	Physical DMA on	When PSOn is set, the TSB12C01A uses PSRO and PSBz to determine acceptance of incoming request packets addressed to the lower 4 Gbytes of initial memory space.
9	PSRO	Physical DMA read only	When PSOn is set, the TSB12C01A uses PSRO to determine acceptance of incoming write request packets addressed to the lower 4 Gbytes of initial memory space.
10	RstTx	Reset transmitter	When RstTx is set, the entire transmitter resets synchronously. This bit clears itself.
11	RstRx	Reset receiver	When RstRx is set, the entire receiver resets synchronously. This bit clears itself.
12–15	BlkBusDep	Block bus-dependent address	This field is used by the receiver to filter out broadcast packets to the bus-dependent area of CSR space. Setting the LSB of this field disables the reception of broadcast packets to the lowest 128 bytes of bus-dependent CSR space. Setting the MSB of this field disables the reception of broadcast packets to the highest 128 bytes of bus-dependent CSR space.
16–17	ATRC	AT retry code	This field contains the last retry code received. This code is logically ORed with the retry code field (00) in the transmit packet, and the packet is resent. This alleviates the need to change the retry code in the transmit packet. The retry encoding follows the IEEE-1394 standard 7.1v1. The retry code is as follows: 00 retry_o (new) 01 retry_X 10 retry_A 11 retry_B

Table 3–3. Control-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
18–19	Reserved	Reserved	Reserved
20	CyMas	Cycle master	When CyMas is set and the TSB12C01A is attached to the root phy, the cyclemaster function is enabled. When the cycle_count field of the cycle timer register increments, the transmitter sends a cycle-start packet.
21	CySrc	Cycle source	When CySrc is set, the cycle_count field increments and the cycle_offset field resets for each positive transition of CYCLEIN. When CySrc is cleared, the cycle_count field increments when the cycle_offset field rolls over.
22	CyTEn	Cycle-timer enable	When CyTEn is set, the cycle_offset field increments.
23	CyMrkEn	Cycle mark enable	When CyMrkEn is set, cycle marks are inserted into GRF at the end of each isochronous cycle (TSB12C01A compatible). When CyMrkEn is cleared, no cycle marks are generated.
24	IRP1En	IR port 1 enable	When IRP1En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port1 field.
25	IRP2En	IR port 2 enable	When IRP2En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port2 field.
26–30	Reserved	Reserved	Reserved
31	RevAEn		

3.2.4 Interrupt and Interrupt-Mask Registers

The interrupt and interrupt-mask registers work in tandem to inform the host bus interface when the state of the TSB12C01A changes. The interrupt register is at address 0Ch. The interrupt mask register is at address 10h. The interrupt mask register is read/write. Its initial value is 0000_0000h. When regRW is zero, the interrupt register (except for the Int bit) is write to clear. When regRW is set, the interrupt register (including the Int bit) is read/write. Its initial value is 1000_0000h.

The interrupt bits all work the same. For example, when a phy interrupt occurs, the PhInt bit is set. When the PhIntMask bit is set, the Int bit is set. When the IntMask is set, the $\overline{\text{INT}}$ signal is asserted. The logic for the interrupt bits is shown in Figure 3–2. Table 3–4 defines the interrupt and interrupt-mask register field descriptions.

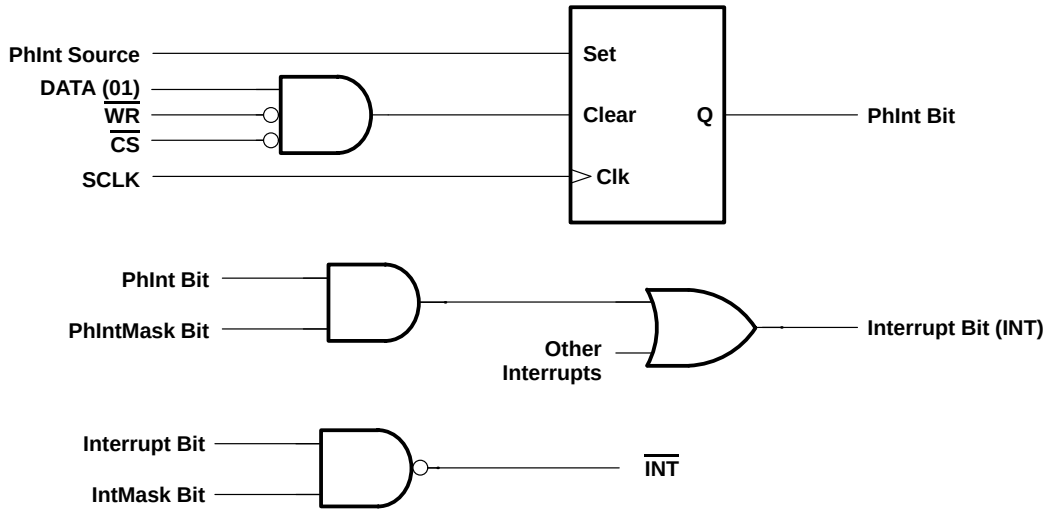


Figure 3–2. Interrupt Logic Diagram Example

Table 3–4. Interrupt- and Mask-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Int	Interrupt	Int contains the value of all interrupt and interrupt mask bits ORed together.
1	PhInt	Phy chip interrupt	When PhInt is set, the phy chip has signaled an interrupt through the Phy interface.
2	PhyRRx	Phy register information received	When PhyRRx is set, a register value has been transferred to the phy chip access register (offset 24h) from the Phy interface.
3	PhRst	Phy reset started	When PhRst is set, a phy-layer reconfiguration has started (1394 bus reset).
4	Reserved	Reserved	Reserved
5	TxRdy	Transmitter ready	When TxRdy is set, the transmitter is idle and ready.
6	RxDta	Receiver has data	When RxDta is set, the receiver has confirmed data to the GRF interface.
7	CmdRst	Command reset received	When CmdRst is set, the receiver has been sent a quadlet write request addressed to the RESET_START CSR register.
8–10	Reserved	Reserved	Reserved
11	ITStk	Transmitter is stuck (IT)	When ITStk is set, the transmitter has detected invalid data at the isochronous transmit-FIFO interface.
12	ATStk	Transmitter is stuck (AT)	When ATStk is set, the transmitter has detected invalid data at the asynchronous transmit-FIFO interface. If the first quadlet of a packet is not written to the ATF_First or ATF_First&Update, the transmitter enters a state denoted by an ATStuck interrupt. An underflow of the ATF also causes an ATStuck interrupt. If this state is entered, no asynchronous packets can be sent until the ATF is cleared via the CLR ATF control bit. Isochronous packets can be sent while in this state.
13	Reserved	Reserved	Reserved
14	SntRj	Busy acknowledge sent by receiver	When SntRj is set, the receiver is forced to send a busy acknowledge to a packet addressed to this node because the GRF overflowed.
15	HdrEr	Header error	When HdrEr is set, the receiver detected a header CRC error on an incoming packet that may have been addressed to this node.
16	TCErr	Transaction code error	When TCErr is set, the transmitter detected an invalid transaction code in the data at the transmit FIFO interface.
17–19	Reserved	Reserved	Reserved
20	CySec	Cycle second incremented	When CySec is set, the cycle-second field in the cycle-timer register incremented. This occurs approximately every second when the cycle timer is enabled.
21	CySt	Cycle started	When CySt is set, the transmitter has sent or the receiver has received a cycle-start packet.
22	CyDne	Cycle done	When CyDne is set, an arbitration gap has been detected on the bus after the transmission or reception of a cycle-start packet. This indicates that the isochronous cycle is over.
23	CyPnd	Cycle pending	When CyPnd is set, the cycle-timer offset is set to 0 (rolled over or reset) and remains set until the isochronous cycle ends.
24	CyLst	Cycle lost	When CyLst is set, the cycle timer has rolled over twice without the reception of a cycle-start packet. This occurs only when this node is not the cycle master.

Table 3–4. Interrupt- and Mask-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
25	CArbFI	Cycle arbitration failed	When CArbFI is set, the arbitration to send the cycle-start packet failed.
26–30	Reserved	Reserved	Reserved
31	IArbFI	Isochronous arbitration failed	When IArbFI is set, the arbitration to send an isochronous packet failed.

3.2.5 Cycle-Timer Register

The cycle-timer register contains the seconds_count, cycle_count and cycle_offset fields of the cycle timer. The register is at address 14h and is read/write. This field is controlled by the cycle master, cycle source, and cycle timer enable bits of the control register. Its initial value is 0000_0000h.

Table 3–5. Cycle-Timer Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–6	seconds_count	Seconds count	1-Hz cycle-timer counter
7–19	cycle_count	Cycle count	8,000-Hz cycle-timer counter
20–31	cycle_offset	Cycle offset	24.576-MHz cycle-timer counter

3.2.6 Isochronous Receive-Port Number Register

The isochronous receive-port number register controls which isochronous channels are received by this node. This register is at address 18h. The register is read/write, and its initial value is 0000_0000h.

Table 3–6. Isochronous Receive-Port Number Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–7	IRPort1	Isochronous receive port 1 channel number	IRPort1 contains the channel number of the isochronous packets the receiver accepts. The receiver accepts when IRP1En is set (bits 0 and 1 are reserved).
8–15	IRPort2	Isochronous receive port 2 channel number	IRPort2 contains the channel number of the isochronous packets the receiver accepts. The receiver accepts when IRP2En is set (bits 8 and 9 are reserved).
16–31	Reserved	Reserved	Reserved

3.2.7 Diagnostic Control and Status Register

The diagnostic control and status register allows for the monitoring and control of the diagnostic features of the TSB12C01A. The register is at address 20h. The regRW and enable snoop bits are read/write. When regRW is cleared, all other bits are read only. When regRW is set, all bits are read/write. Its initial value is 0000_0000h. For a RAM test read/write, enable RAM test mode and set Adr_clr to clear the RAM internal address counter. Do the host bus read/write to location 80h; this accesses RAM starting at location 00h. With each read/write the RAM internal address counter increments by one.

Table 3–7. Diagnostic Control and Status-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	ENSp	Enable Snoop	When ENSp is set, the receiver accepts all packets on the bus regardless of address or format. The receiver uses the snoop data format defined in Section 4.4, Quadlet Receive.
1	BsyFl	Busy flag	When BsyFl is set, the receiver sends an ack_busyB the next time the receiver must busy a packet. When cleared, the receiver sends an ack_busyA the next time the receiver must busy a packet.
2	ArbGp	Arbitration reset gap	When ArbGp is set, the serial bus has been idle for an arbitration reset gap.
3	FrGp	Fair gap	When FrGp is set, the serial bus has been idle for a fair-gap time (Sub-Action Gap).
4	regR/W	Register read/write access	When regR/W is set, most registers are fully read/write.
5	Adr_clr	Address clear	When Adr_clr is set, the internal RAM address counter and the Control_bit_err flag are cleared.
6	Control_bit1	Control bit for RAM test write	During RAM test mode, Control_bit1 is written into the control bit of RAM (bit 33) for RAM write transaction.
7	Control_bit_err	Control bit error flag	When Control_bit_err is set, the control bit of the RAM does not match Control_bit1 during RAM test mode.
8	RAMTest	RAM test mode	When RAMTest and regRW are set, RAM test mode is enabled.
9–31	Reserved	Reserved	Reserved

3.2.8 Phy-Chip Access Register

The phy-chip access register allows access to the registers in the attached phy chip. The most significant 16 bits send read and write requests to the phy-chip registers. The least significant 16 bits are for the phy chip to respond to a read request sent by the TSB12C01A. The phy-chip access register also allows the phy interface to send important information back to the TSB12C01A. When the phy interface sends new information to the TSB12C01A, the phy register-information-receive (PhyRRx) interrupt is set. The register is at address 24h and is read/write. Its initial value is 0000_0000h.

Table 3–8. Phy-Chip Access Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	RdPhy	Read phy-chip register	When RdPhy is set, the TSB12C01A sends a read register request with address equal to phyRgAd to the Phy interface. This bit is cleared when the request is sent.
1	WrPhy	Write phy-chip register	When WrPhy is set, the TSB12C01A sends a write register request with address equal to phyRgAd to the Phy interface. This bit is cleared when the request is sent.
2–3	Reserved	Reserved	Reserved
4–7	PhyRgAd	Phy-chip-register address	PhyRgAd is the address of the phy-chip register that is to be accessed.
8–15	PhyRgData	Phy-chip-register data	PhyRgData is the data to be written to the phy-chip register indicated in PhyRgAd.
16–19	Reserved	Reserved	Reserved
20–23	PhyRxAd	Phy-chip-register-received address	PhyRxAd is the address of the register from which PhyRxData came.
24–31	PhyRxData	Phy-chip-register-received data	PhyRxData contains the data from register addressed by PhyRxAd.

3.2.9 Phy-Interface State Register

The Phy-interface state register contains the state values of the internal state machines of the Phy interface module and is used for debugging purposes. The register is at 28h and is read only. Its initial value is 0000_0000h.

Table 3–9. Phy-Interface State Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–15	Reserved	Reserved	Reserved
16–19	Req_State	State of the request module	Req_State is the state value of the request module.
20–23	TI_State	State of the transmit interface module	TI_State is the state value of the transmit interface module.
24–26	RDI_State	State of the receiver data interface module	RDI_State is the state value of the receiver data interface module.
27–28	RSI_State	State of the receiver status interface module	RSI_State is the state value of the receiver status interface module.
29–31	RA_State	State of the receive acknowledge module	RA_State is the state value of the receive ack module.

3.2.10 Other State Register

The other state register contains state values of all other modules except phy interface module. It is used for debugging purposes. The register is at address 2Ch and is read only. Its initial value is 0000_0000h.

Table 3–10. Other State Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–3	Reserved	Reserved	Reserved
4–6	CM_State	Cycle monitor	CM_State is the state value of the cycle monitor module.
7–9	RAC_State	RAM access control	RAC_State is the state value of the RAM access control module
10–11	ITF_Link_State	Link transmit FIFO logic	ITF_Link_State is the state value of the link transmit FIFO logic module for the ITF
12	ITF_Host_State	Host transmit FIFO logic	ITF_Host_State is the state value of the host transmit FIFO logic module for the ITF.
13–14	ATF_Link_State	Link transmit FIFO logic	ATF_Link_State is the state value of the link transmit FIFO logic module for the ATF.
15	ATF_Host_State	Host transmit FIFO logic	ATF_Host_State is the state value of the host transmit FIFO logic module for the ATF.
16–18	GRF_Host_State	Host receive FIFO logic	GRF_Host_State is the state value of the host receive FIFO logic module for the GRF.
19–21	RB_State	Receive busy	RB_State is the state value of the receive busy module.
20–22	Rcv_State	Receive	Rcv_State is the state value of the receive module.
23–31	Tx_State	Transmit	Tx_State is the state value of the transmit module.

3.2.11 Asynchronous Transmit-FIFO (ATF) Status Register

The ATF status register allows access to the registers that control or monitor the ATF. The register is at address 30h. All the FIFO flag bits are read only, and the FIFO control bits are read/write. Its initial value is 0000_0000h.

Table 3–11. ATF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	ATF full flag	When Full is set, the FIFO is full. Writes are ignored.
1	AIF	ATF almost-full flag	When AIF is set, the FIFO can accept one more write.
2–3	Reserved	Reserved	Reserved
4	4AV	ATF-4-available flag	When 4AV is set, the FIFO has space available for at least four quadlets.
5–13	Reserved	Reserved	Reserved
14	AIE	ATF-almost-empty flag	When AIE is set, the FIFO has only one quadlet in it.
15	Empty	ATF-empty flag	When Empty is set, the FIFO is empty.
16–18	Reserved	Reserved	Reserved
19	Clr	ATF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–22	Reserved	Reserved	Reserved
23–31	Size	ATF-size control bits	Size is equal to the ATF size number in quadlets.

3.2.12 ITF Status Register

The ITF status register allows access to the registers that control or monitor the ITF. The register is at address 34h. All the FIFO flag bits are read only, and the FIFO control bits are read/write. Its initial value is 0000_0000h.

Table 3–12. ITF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	ITF full flag	When Full is set, the FIFO is full and all writes are ignored.
1	AlF	ITF almost-full flag	When AlF is set, the FIFO can accept only one more write.
2–3	Reserved	Reserved	Reserved
4	4AV	ITF-4-available flag	When 4AV is set, the FIFO has space for at least four more quadlets.
5–13	Reserved	Reserved	Reserved
14	AlE	ITF-almost-empty flag	When AlE is set, the FIFO has only one quadlet in it.
15	Empty	ITF-empty flag	When Empty is set, the FIFO is empty.
16–18	Reserved	Reserved	Reserved
19	Clr	ITF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–22	Reserved	Reserved	Reserved
23–31	Size	ITF-size control bits	The size is equal to the ITF size number in quadlets.

3.2.13 GRF Status Register

The GRF status register allows access to the registers that control or monitor the GRF. The register is at address 3Ch. All the FIFO flag bits are read only, and the FIFO control bits are read/write. Its initial value is 0000_0000h.

Table 3–13. GRF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	GRF full flag	When Full is set, the FIFO is full.
1	AlF	GRF-almost-full flag	When AlF is set, the FIFO can accept only one more write.
2–11	Reserved	Reserved	Reserved
12	4Th	GRF four there	When 4Th is set, the FIFO has at least four quadlets in it.
13	Reserved	Reserved	Reserved
14	AlE	GRF-almost-empty flag	When AlE is set, the FIFO has one quadlet in it.
15	Empty	GRF-empty flag	When Empty is set, the FIFO is empty and reads are ignored.
16	cd	GRF control bit	This is the control bit for the GRF. When cd is set, the first quadlet of a packet is being read from the GRF_Data address.
17–18	Reserved	Reserved	Reserved
19	Clr	GRF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–22	Reserved	Reserved	Reserved
23–31	Size	GRF-size control bits	The size is equal to the GRF size number in quadlets.

3.3 FIFO Access

Access to all the transmit FIFOs is fundamentally the same; only the address to where the write is made changes.

3.3.1 General

The TSB12C01A controller FIFO-access address map shown in Figure 3–3 illustrates how the FIFOs are mapped. The suffix _First denotes a write to the FIFO location where the first quadlet of a packet should be written when the writer wants the packet to be held in the FIFO until a quadlet is written to an update location.

The suffix _Continue denotes a write to the FIFO location where the second through n–1 quadlets of a packet could be written.

The suffix _First&Update denotes a write to the FIFO location where the first quadlet of a packet should be written when the writer wants the packet to be transmitted as soon as possible.

The suffix _Continue&Update denotes a write to the FIFO location where the second through n quadlets of a packet could be written when the writer wants the packet to be transmitted as soon as possible. The last quadlet of a multiple quadlet packet should be written to the FIFO location with the notation _Continue&Update.

	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
80h	ATF_First
84h	ATF_Continue
88h	ATF_First & Update
8Ch	ATF_Continue & Update
90h	ITF_First
94h	ITF_Continue
98h	ITF_First & Update
9Ch	ITF_Continue & Update
A0h	Reserved
A4h	Reserved
A8h	Reserved
ACh	Reserved
B0h	Reserved
B4h	Reserved
B8h	Reserved
BCh	Reserved
C0h	GRF Data
C4h	Reserved
C8h	Reserved
CCh	Reserved

Figure 3–3. TSB12C01A Controller-FIFO-Access Address Map

3.3.2 ATF Access

Access to the ATF is as follows:

1. Write to ATF location 80h: the data is not confirmed for transmission (first quadlet of the packet).
2. Write to ATF location 84h: the data is not confirmed for transmission (second n–1 quadlets of the packet).
3. Write to ATF location 88h: the data is confirmed for transmission (first quadlet of the packet). The read logic sees all data written to the FIFO since the last confirm (update).
4. Write to ATF location 8Ch: the data is confirmed for transmission (second n quadlets of the packet).

   If the first quadlet of a packet is not written to the ATF_First or ATF_First&Update, the transmitter enters a state denoted by an ATStuck interrupt. An underflow of the ATF also causes an ATStuck interrupt. When this state is entered, no asynchronous packets can be sent until the ATF is cleared via the CLR ATF control bit. Isochronous packets can be sent while in this state.

ATF access example:

The first quadlet of n quadlets is written to ATF location 80h. Quadlets (2 to n-1) are written to ATF location 84h. The last quadlet (nth) is written to ATF location 8Ch. If the ATFEmpty bit is true, it is set to false and the TSB12C01A requests the phy layer to arbitrate for the bus. To ensure that an ATF underflow condition does not occur, loading of the ATF in this manner is suggested.

3.3.3 ITF Access

Access to the ITF is as follows:

1. Write to ITF location 90h: the data is not confirmed for transmission (first quadlet of the packet).
2. Write to ITF location 94h: the data is not confirmed for transmission (second n–1 quadlets of the packet).
3. Write to ITF location 98h: the data is confirmed for transmission (first quadlet of the packet). The read logic sees all data written to the FIFO since the last confirm (update).
4. Write to ITF location 9Ch: the data is confirmed for transmission (second n quadlet of the packet).

   If the first quadlet of a packet is not written to the ITF_First or ITF_First&Update, the transmitter enters a state denoted by an ITStuck interrupt. An underflow of the ITF also causes an ITStuck interrupt. When this state is entered, no isochronous packets can be sent until the ITF is cleared by the CLR ITF control bit. Asynchronous packets can be sent while in this state.

ITF access example:

The first quadlet of n quadlets is written to ITF location 90h. Quadlets (2 to n-1) are written to ITF location 94h. The last quadlet (nth) is written to ITF location 9Ch. If the ITFEmpty is true, it is set to false and the TSB12C01A requests the phy layer to arbitrate for the bus. To ensure that an ITF underflow condition does not occur, loading of the ITF in this manner is suggested.

3.3.4 General-Receive-FIFO (GRF)

Access to the GRF is done with a read from the GRF, which requires a read from address C0h.

3.3.5 RAM Test Mode

The purpose of RAM test mode is to test the RAM with writes and reads. During RAM test mode, RAM, which makes up the ATF, ITF, and GRF, is accessed directly from the host bus. Different data is written to and read back from the RAM and compared with what was expected to be read back. ATF status, ITF status, and GRF status are not changed during RAM test mode, but the stored data in RAM is changed by any write transaction. To enable RAM test mode, set regRW bit and RAMTest bit of the diagnostics register. Before beginning any read or write to the RAM, the Adr_clr bit of the diagnostics register should be set to clear the internal RAM address counter. This action also clears the Adr_clr bit.

During RAM test mode, the host bus address should be 80h. The first host bus transaction (either read or write) accesses location 0 of the RAM. The second host bus transaction accesses location 1 of the RAM. The nth host bus transaction accesses location n–1 of the RAM. After each transaction, the internal RAM address counter is incremented by one.

The RAM has 512 locations with each location containing 33 bits. The most significant bit is the control bit. When it is set, that indicates the quadlet is the start of the packet. In order to set the control bit, Control-bit1 of the diagnostics register has to be set. In order to clear the control bit, Control_bit1 of the diagnostics register has to be cleared. When a write occurs, the 32 bits of data from the host bus is written to the low order 32 bits of the RAM and the value in Control-bit1 is written to the control bit. When a read occurs, the low order 32 bits of RAM are sent to the host data bus and the control bit is compared to Control_bit1. If the control bit and Control_bit1 do not match, Control_bit_err of the diagnostics register is set. This does not stop operation and another read or write can immediately be transmitted. To clear Control_bit_err, set Adr_clr of the diagnostics register, or transact another write.

4 TSB12C01A Data Formats

The data formats for transmission and reception of data are shown in the following sections. The transmit format describes the expected organization of data presented to the TSB12C01A at the host-bus interface. The receive formats describe the data format that the TSB12C01A presents to the host-bus interface.

4.1 Asynchronous Transmit (Host Bus to TSB12C01A)

Asynchronous transmit refers to the use of the asynchronous-transmit FIFO (ATF) interface. The general-receive FIFO (GRF) is shared by asynchronous data and isochronous data. There are two basic formats for data to be transmitted and received. The first is for quadlet packets, and the second is for block packets. For transmits, the FIFO address indicates the beginning, middle, and end of a packet. For receives, the data length, which is found in the header of the packet, determines the number of bytes in a block packet.

4.1.1 Quadlet Transmit

The quadlet-transmit format is shown in Figure 4–1. The first quadlet contains packet control information. The second and third quadlets contain the 64-bit, quadlet-aligned address. The fourth quadlet is data used only for write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

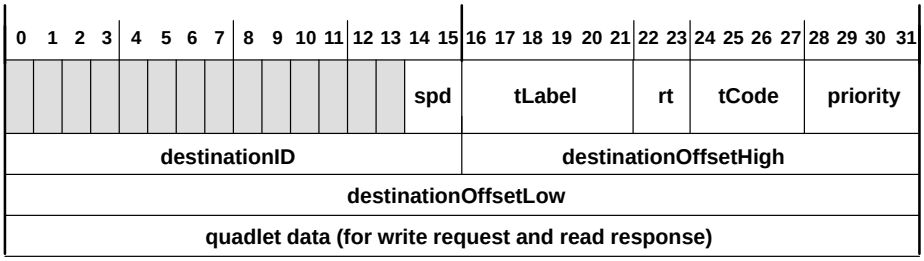


Figure 4–1. Quadlet-Transmit Format

Table 4–1. Quadlet-Transmit Format

FIELD NAME	DESCRIPTION
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is: 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet. (see Table 6–10 of IEEE-1394 standard)
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of this packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4).
quadlet data	For write requests and read responses, this field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.

4.1.2 Block Transmit

The block-transmit format is shown in Figure 4–2. The first quadlet contains packet-control information. The second and third quadlets contain the 64-bit address. The first 16 bits of the fourth quadlet contains the

dataLength field. This is the number of bytes of data in the packet. The remaining 16 bits represent the extended_tCode field. (See Table 6–11 of the IEEE-1394 standard for more information on extended_tCodes.) The block data, if any, follows the extended_tCode. Block write responses are identical to the quadlet write response and use the format described in section 4.1.3, Quadlet Receive.

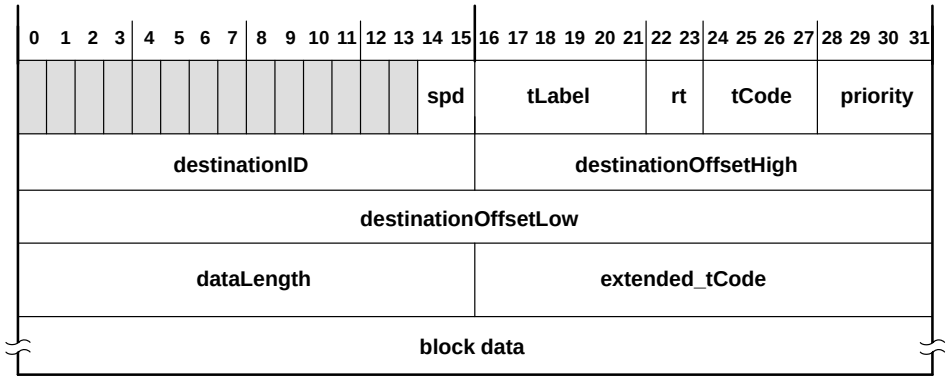


Figure 4–2. Block-Transmit Format

Table 4–2. Block-Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet (see Table 6–10 of IEEE-1394 standard).
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination node's address space. This address must be quadlet aligned (modulo 4). The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	The number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6–11 of the IEEE-1394 standard.
block data	The data to be sent. If dataLength is 0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in byte 0 of the first quadlet.

4.1.3 Quadlet Receive

The quadlet-receive format is shown in Figure 4–3. The first 16 bits of the first quadlet contain the destination node and bus id, and the remaining 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source, and the remaining 16 bits of the second and third quadlets contain the 48-bit, quadlet-aligned destination offset address. The fourth quadlet contains data that was used by write requests and read responses. For read requests and write responses, the quadlet data field is omitted. The last quadlet contains packet-reception status, added by the TSB12C01A.

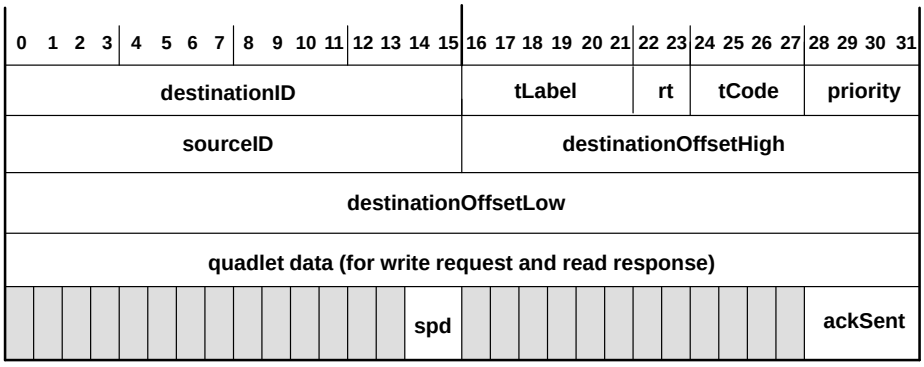


Figure 4–3. Quadlet-Receive Format

Table 4–3. Quadlet-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet. (See Table 6–10 of the IEEE-1394 standard).
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
sourceID	This is the node ID of the sender of this packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). (The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets, and the remaining bits are reserved.)
quadlet data	For write requests and read responses, this field holds the transferred data. For write responses and read requests, this field is not present.
spd	This field indicates the speed at which this packet was sent. 00 = 100 Mb/s, 01 = 200 Mb/s, 10 = 400 Mb/s, and 11 is undefined for this implementation.
ackSent	This field holds the acknowledge sent by the receiver for this packet. (See Table 6–13 in the draft standard.)

4.1.4 Block Receive

The block-receive format is shown in Figure 4–4. The first 16 bits of the first quadlet contain the node and bus ID of the destination node, and the last 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source node, and the last 16 bits of the second quadlet and all of the third quadlet contain the 48-bit, quadlet-aligned destination offset address. All remaining quadlets, except for the last one, contain data that is used only for write requests and read responses. For block read requests and block write responses, the data field is omitted. The last quadlet contains packet-reception status.

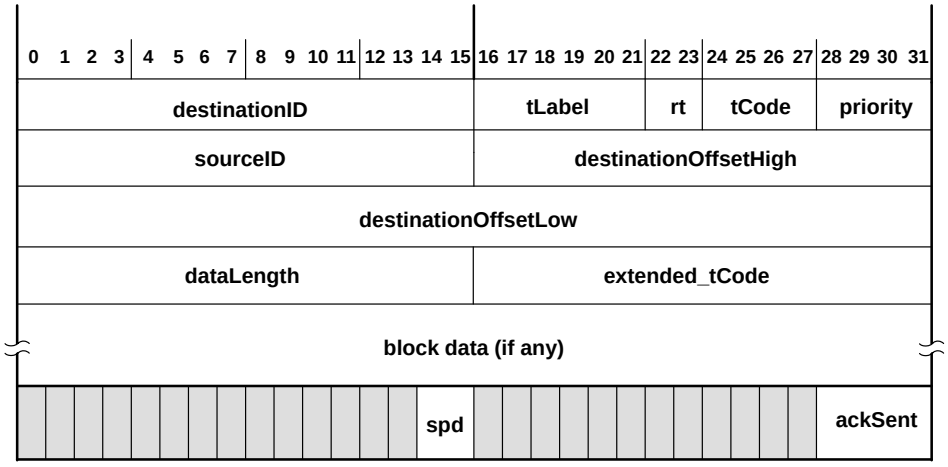


Figure 4–4. Block-Receive Format

Table 4–4. Block-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet. (See Table 6–10 of the IEEE-1394 standard).
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
sourceID	This is the node ID of the sender of this packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	For write request, read responses, and locks, this field indicates the number of bytes being transferred. For read requests, this field indicates the number of bytes of data to be read. A write-response packet does not use this field. Note that the number of bytes does not include the head, only the bytes of block data.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6–11 of the IEEE-1394 standard.
block data	This field contains any data being transferred for this packet. Regardless of the destination address or memory alignment, the first byte of the data appears in byte 0 of the first quadlet of this field. The last quadlet of this field is padded with zeros out to four bytes, if necessary.
spd	This field indicates the speed at which this packet was sent. 00 = 100 Mb/s, 01 = 200 Mb/s, 10 = 400 Mb/s, and 11 is undefined for this implementation.
ackSent	This field holds the acknowledge sent by the receiver for this packet.

4.2 Isochronous Transmit (Host Bus to TSB12C01A)

The format of the isochronous-transmit packet is shown in Figure 4–5. The data for each channel must be presented to the isochronous-transmit FIFO interface in this format in the order that packets are to be sent. The transmitter sends any packets available at the isochronous-transmit interface immediately following reception or transmission of the cycle-start message.

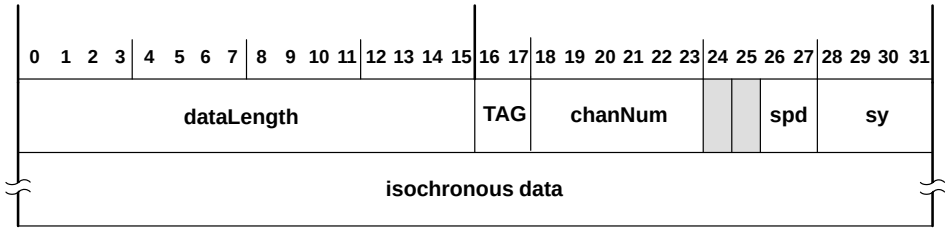


Figure 4–5. Isochronous-Transmit Format

Table 4–5. Isochronous-Transmit Functions

FIELD NAME	DESCRIPTION
dataLength	This field indicates the number of bytes in this packet
TAG	This field indicates the format of data carried by isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	This field carries the channel number with which this data is associated
spd	This field contains the speed at which to send this packet
sy	This field carries the transaction layer-specific synchronization bits
isochronous data	This field contains the data to be sent with this packet. The first byte of data must appear in byte 0 of the first quadlet of this field. If the last quadlet does not contain four bytes of data, the unused bytes should be padded with zeros.

4.3 Isochronous Receive (TSB12C01A to Host Bus)

The format of the iscohronous-receive data is shown in Figure 4–6. The data length, which is found in the header of the packet, determines the number of bytes in an isochronous packet.

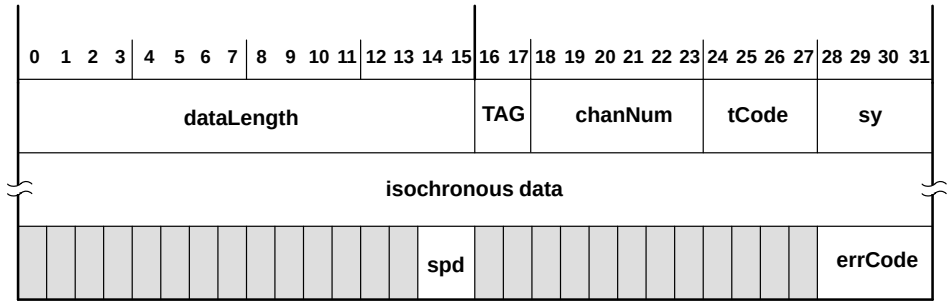


Figure 4–6. Isochronous-Receive Format

Table 4–6. Isochronous-Receive Functions

FIELD NAME	DESCRIPTION
dataLength	This field indicates the number of bytes in this packet
TAG	This field indicates the format of data carried by isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	This field contains the channel number with which this data is associated
tCode	This field carries the transaction code for this packet. (tCode = Ah)
sy	This field carries the transaction layer-specific synchronization bits
isochronous data	This field has the data to be sent with this packet. The first byte of data must appear in byte 0 of the first quadlet of this field. The last quadlet should be padded with zeros.
spd	This field indicates the speed at which this packet was sent
errCode	This field indicates whether this packet was received correctly. The possibilities are Complete, DataErr, or CRCErr and have the same encoding as the corresponding acknowledge codes.

4.4 Snoop

The format of the snoop data is shown in Figure 4–7. The receiver module can be directed to receive any and all packets that pass by on the serial bus. In this mode, the receiver presents the data received to the receive-FIFO interface.

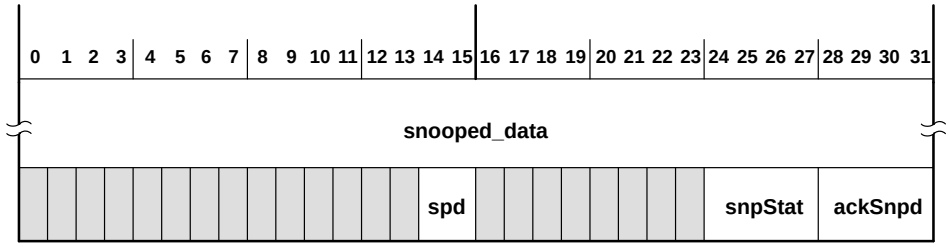


Figure 4–7. Snoop Format

Table 4–7. Snoop Functions

FIELD NAME	DESCRIPTION
snooped_data	This field contains the entire packet received or as much as could be received.
spd	This field carries the speed at which this packet was sent
snpStat	This field indicates whether the entire packet snooped was received correctly. A value equal to the complete acknowledge code indicates complete reception. A busyA or busyB acknowledge code indicates incomplete reception.
ackSnpd	This field indicates the acknowledge seen on the bus after the packet is received.

4.5 CycleMark

The format of the CycleMark data is shown in Figure 4–8. The receiver module inserts a single quadlet to mark the end of an isochronous cycle. The quadlet is inserted into the receive-FIFO.

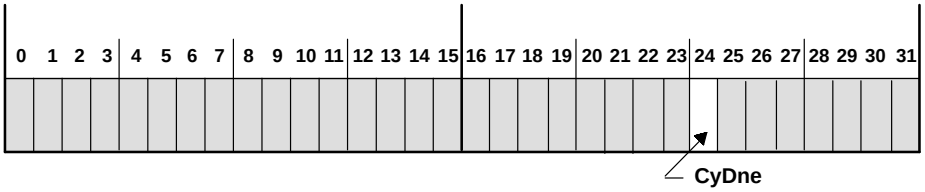


Figure 4–8. CycleMark Format

Table 4–8. CycleMark Functions

FIELD NAME	DESCRIPTION
CyDne	This field indicates the end of an isochronous cycle.

4.6 Phy Configuration

The format of the phy configuration packet is shown in Figure 4–9. The phy configuration packet transmit contains two quadlets, which are loaded into the ATF. The first quadlet is written to address 80h. The second quadlet is written to address 8Ch. The 00E0h in the first quadlet tells the TSB12C01A that this is the phy configuration packet. The Eh is then replaced with 0h before the packet is transmitted to the phy interface.

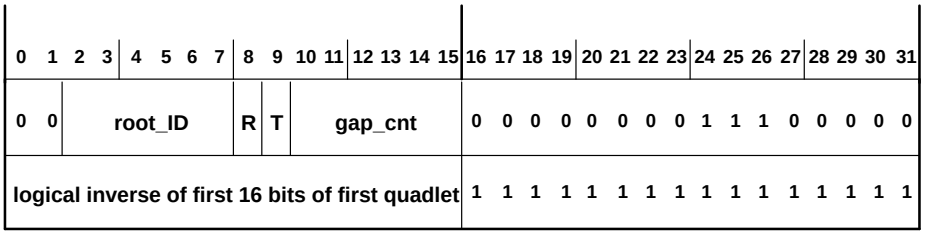


Figure 4–9. Phy Configuration Format

Table 4–9. Phy Configuration Functions

FIELD NAME	DESCRIPTION
00	This field is the phy configuration packet identifier.
root_ID	This field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R†	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T†	When T is set, the PHY_CONFIGURATION.gap_count field of all the nodes is set to the value in the gap_cnt field.
gap_cnt	This field contains the new value for PHY_CONFIGURATION.gap_count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, gap_cnt is set to 63h unless a new Phy configuration packet is received.

† A phy configuration packet with R = 0, and T = 0 is reserved and is ignored when received.

4.7 Receive Self-ID

The format of the receive self-ID packet is shown in Figure 4–10. When RxSId (bit 1 of the control register) is set, the receive self-ID packet is stored in GRF.

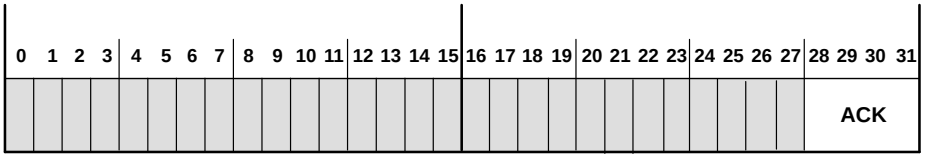


Figure 4–10. Receive Self-ID Format

Table 4–10. Receive Self-ID Functions

FIELD NAME	DESCRIPTION
ACK	When this field is set, the data in the self-ID packet is correct. When ACK is cleared, the data in the self-ID packet is incorrect.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 6 V
Input voltage range, at any input, V_I . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 2) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 3) . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 10 seconds, T_C . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. This applies to all inputs.
3. This applies to all outputs.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage, V_{IH}		2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	V
Clock frequency	BCLK		25	33	MHz
	SCLK		49.152		
Operating free-air temperature, T_A		0		70	°C
Virtual junction temperature range, T_J		0		115	°C

5.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –4 mA	V_{CC} – 0.8			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
V_{IT+}	Positive-going input threshold voltage		Phy interface			0.7 V_{CC}	V
			All other inputs (see Note 4)			2	
V_{IT-}	Negative-going input threshold voltage		Phy interface	0.2 V_{CC}			V
			All other inputs (see Note 4)	0.8			
I_{IL}	Low-level input current		V_I = GND			–1	µA
I_{IH}	High-level input current		V_I = V_{CC}			1	µA
I_{OZ}	High-impedance-state output current		V_I = V_{CC} or GND (see Note 5)			±10	µA
I_{CC}	Supply current		No load on outputs, SCLK = 49.152 MHz BCLK = 25 MHz		150		mA
C_i	Input capacitance	Input terminals	V_{CC} = 5 V, TA = 25°C		5		pF
		Bidirectional terminals			13		
C_o	Output capacitance				8		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 4. This applies for all inputs except SCLK, BCLK, and $\overline{\text{RESET}}$.
5. All outputs are in the high-impedance state.

5.4 Host-Interface Timing Requirements Over Operating Free-Air Temperature Range

PARAMETER		MIN	MAX	UNIT
t_{c1}	Cycle time, BCLK (see Figure 6–1)	30		ns
$t_{w1(H)}$	Pulse duration, BCLK high (see Figure 6–1)	10		ns
$t_{w1(L)}$	Pulse duration, BCLK low (see Figure 6–1)	10		ns
t_{su1}	Setup time, DATA[0:31] before BCLK↑ (see Figure 6–2)	4		ns
t_{h1}	Hold time, DATA[0:31] after BCLK↑ (see Figure 6–2)	2		ns
t_{su2}	Setup time, ADDR[0:7] before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h2}	Hold time, ADDR[0:7] after BCLK↑ (see Figures 6–2 and 6–3)	2		ns
t_{su3}	Setup time, $\overline{\text{CS}}$ before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h3}	Hold time, $\overline{\text{CS}}$ after BCLK↑ (see Figures 6–2 and 6–3)	2		ns
t_{su4}	Setup time, $\overline{\text{WR}}$ before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h4}	Hold time, $\overline{\text{WR}}$ after BCLK↑ (see Figures 6–2 and 6–3)	2		ns

5.5 Host-Interface Switching Characteristics Over Operating Free-Air Temperature Range, C_L = 45 pF (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 6–2)	4	16	ns
t_{d2}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 6–2)	4	16	ns
t_{d3}	Delay time, BCLK↑ to DATA[0:31] valid (see Figure 6–3)	4	24	ns
t_{d4}	Delay time, BCLK↑ to DATA[0:31] invalid (see Figure 6–3)	4	24	ns

5.6 Phy-Interface Timing Requirements Over Operating Free-Air Temperature Range

PARAMETER		MIN	MAX	UNIT
t_{c2}	Cycle time, SCLK (see Figure 6–4)	20.24	20.45	ns
$t_{w2(H)}$	Pulse duration, SCLK high (see Figure 6–4)	9		ns
$t_{w2(L)}$	Pulse duration, SCLK low (see Figure 6–4)	9		ns
t_{su5}	Setup time, DATA[0:7] before SCLK↑ (see Figure 6–6)	6		ns
t_{h5}	Hold time, DATA[0:7] after SCLK↑ (see Figure 6–6)	0		ns
t_{su6}	Setup time, CTL[0:1] before SCLK↑ (see Figure 6–6)	6		ns
t_{h6}	Hold time, CTL[0:1] after SCLK↑ (see Figure 6–6)	0		ns

5.7 Phy-Interface Switching Characteristics Over Operating Free-Air Temperature Range, C_L = 45 pF (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{d5}	Delay time, SCLK↑ to D[0:7] valid (see Figure 6–5)	3	14	ns
t_{d6}	Delay time, SCLK↑ to D[0:7] (see Figure 6–5)	3	14	ns
t_{d7}	Delay time, SCLK↑ to D[0:7] invalid (see Figure 6–5)	3	14	ns
t_{d8}	Delay time, SCLK↑ to CTL[0:1] valid (see Figure 6–5)	3	14	ns
t_{d9}	Delay time, SCLK↑ to CTL[0:1] (see Figure 6–5)	3	14	ns
t_{d10}	Delay time, SCLK↑ to CTL[0:1] invalid (see Figure 6–5)	3	14	ns
t_{d11}	Delay time, SCLK↑ to LREQ (see Figure 6–7)	3	14	ns

5.8 Miscellaneous Timing Requirements Over Operating Free-Air Temperature Range (see Figure 6–9)

PARAMETER		MIN	MAX	UNIT
t_{c3}	Cycle time, CYCLEIN	124.99	125.01	µs
$t_{w3(H)}$	Pulse duration, CYCLEIN high	62		µs
$t_{w3(L)}$	Pulse duration, CYCLEIN low	62		µs

5.9 Miscellaneous Signal Switching Characteristics Over Operating Free-Air Temperature Range

PARAMETER		MIN	MAX	UNIT
t_{d12}	Delay time, SCLK↑ to $\overline{INT}$ low (see Figure 6–8)	4	18	ns
t_{d13}	Delay time, SCLK↑ to $\overline{INT}$ high (see Figure 6–8)	4	18	ns
t_{d14}	Delay time, SCLK↑ to CYCLEOUT high (see Figure 6–10)	4	16	ns
t_{d15}	Delay time, SCLK↑ to CYCLEOUT low (see Figure 6–10)	4	16	ns

6 Parameter Measurement Information

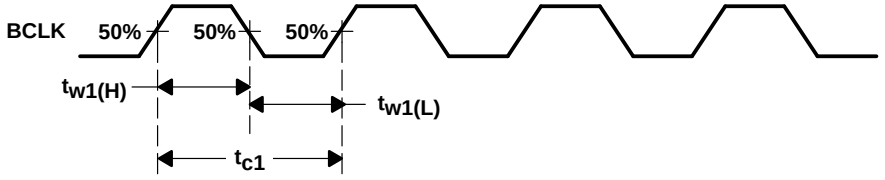
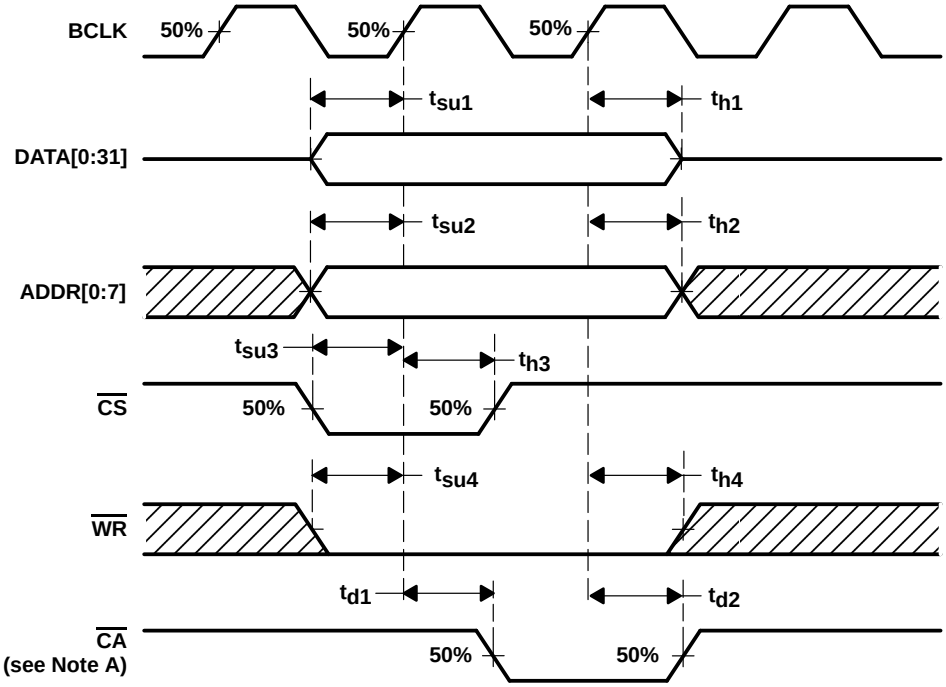
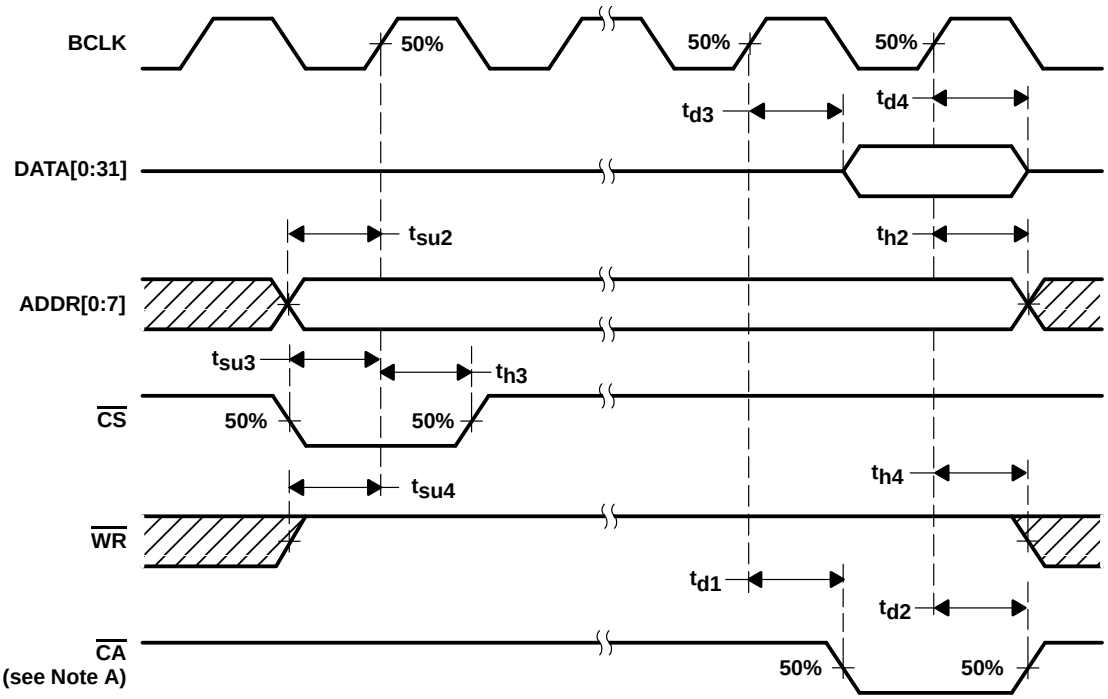


Figure 6–1. BCLK Waveform



NOTE A: When back-to-back write cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of $\overline{CS}$ before $\overline{CA}$ is asserted (low). DATA[0:31], ADDR[0:7], and $\overline{WR}$ need to remain valid until $\overline{CA}$ is asserted (low).

Figure 6–2. Host-Interface Write-Cycle Waveforms



NOTE A: When back-to-back read cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of $\overline{CS}$ and before $\overline{CA}$ is asserted (low). ADDR[0:7] and $\overline{WR}$ need to remain valid until $\overline{CA}$ is asserted (low).

Figure 6–3. Host-Interface Read-Cycle Waveforms

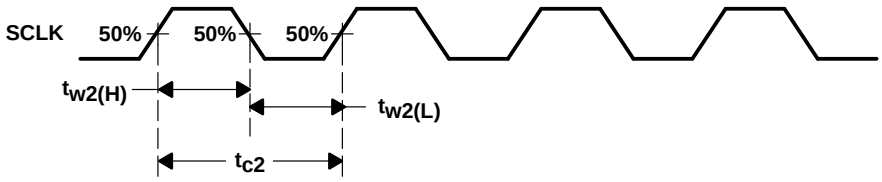


Figure 6–4. SCLK Waveform

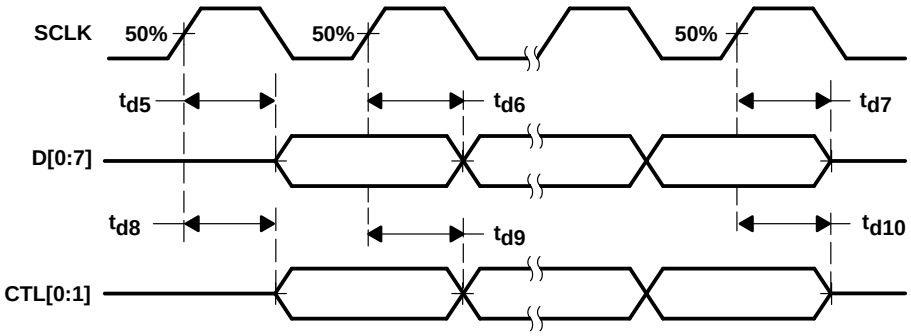


Figure 6–5. TSB12C01A-to-Phy-Layer Transfer Waveforms

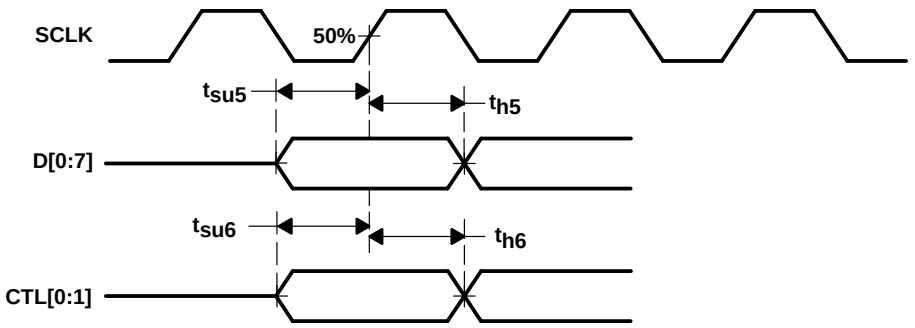


Figure 6–6. Phy-Layer-to-TSB12C01A Transfer Waveforms

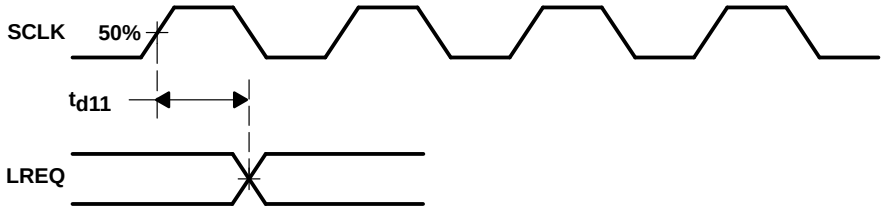


Figure 6–7. TSB12C01A-Link-Request-to-Phy-Layer Waveforms

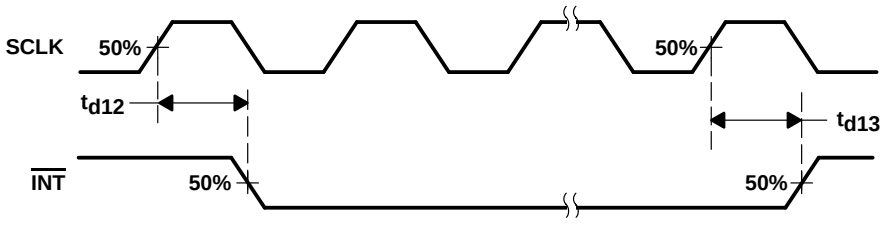


Figure 6–8. Interrupt Waveform

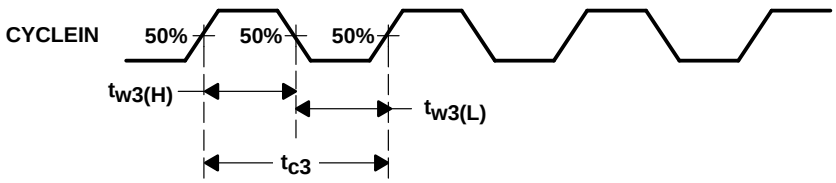


Figure 6–9. CYCLEIN Waveform

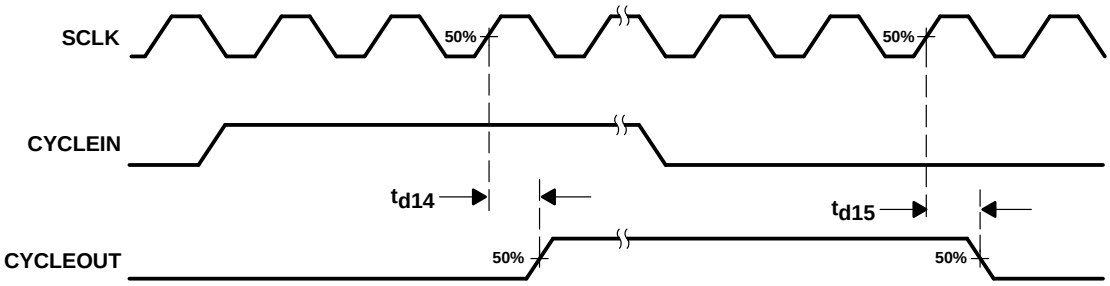


Figure 6–10. CYCLEIN and CYCLEOUT Waveforms

7 TSB12C01A to 1394 Phy Interface Specification

7.1 Introduction

This chapter provides an overview of a TSB12C01A to the phy interface. The information that follows helps guide you through the process of connecting the TSB12C01A to a 1394 physical-layer device. The part numbers referenced, the TSB11C01 and the TSB12C01A, represent the Texas Instruments implementation of the phy (TSB11C01) and link (TSB12C01A) layers of the IEEE-1394 standard.

The specific details of how the TSB11C01 device operates is not discussed in this document. Only those parts that relate to the TSB12C01A phy-link interface are mentioned.

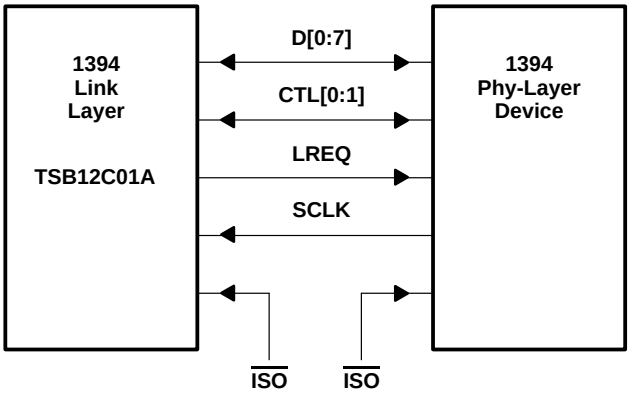
7.2 Assumptions

The TSB12C01A is capable of supporting 100 Mb/s, 200 Mb/s and 400 Mb/s phy-layer devices. For that reason, this document describes an interface to a 400-Mb/s (actually 393.216-Mb/s) device. To support lower-speed phy layers, adjust the width of the data bus by two terminals per 100 Mb/s. For example, for 100-, 200- and 400-Mb/s devices, the data bus is 2, 4, and 8 bits wide respectively. The width of the CTL bus and the clock rate between the devices, however, does not change regardless of the transmission speed that is used.

Finally, the 1394 phy layer has control of all bidirectional terminals that run between the phy layer and TSB12C01A. The TSB12C01A can drive these terminals only after it has been given permission by the phy layer. A dedicated request terminal (LREQ) is used by the TSB12C01A for any activity that you wish to initiate.

7.3 Block Diagram

The functional block diagram of the TSB12C01A to phy layer is shown in Figure 7–1.



NOTE A: See Table 2–2 for signal definition.

Figure 7–1. Functional Block Diagram of the TSB12C01A to Phy Layer

7.4 Operational Overview

The four operations that can occur in the phy-link interface are request, status, transmit, and receive. With the exception of the request operation, all actions are initiated by the phy layer.

The CTL[0:1] bus is encoded as shown in the following sections.

7.4.1 Phy Interface Has Control of the Bus

Table 7–1. Phy Interface Control of Bus Functions

CTL[0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	No activity is occurring (this is the default mode).
01	Status	Status information is being sent from the phy layer to the TSB12C01A.
10	Receive	An incoming packet is being sent from the phy layer to the TSB12C01A.
11	Transmit	The TSB12C01A has been given control of the bus to send an outgoing packet.

The TSB12C01A has control of the bus after receiving permission from the phy layer.

Table 7–2. TSB12C01A Control of Bus Functions

CTL[0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	The TSB12C01A releases the bus (transmission has been completed).
01	Hold	The TSB12C01A is holding the bus while data is being prepared for transmission, or the TSB12C01A wants to send another packet without arbitration.
10	Transmit	An outgoing packet is being sent from the TSB12C01A to phy layer.
11	Reserved	None

7.5 Request

A serial stream of information is sent across the LREQ terminal whenever the TSB12C01A needs to request the bus or access a register that is located in the phy layer. The size of the stream varies depending on whether the transfer is a bus request, a read command, or a write command. Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream.

Table 7–3. Request Functions

# of BITS	NAME
7	Bus Request
9	Read Register Request
17	Write Register Request

7.5.1 LREQ Transfer

The definition of the bits in the three different types of transfers are shown in Table 7–4.

7.5.1.1 TSB12C01A Bus Request

Table 7–4. Bus-Request Functions (Length of Stream: 7 Bits)

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Start bit indicates the beginning of the transfer (always set).
1–3	Request Type	Request type indicates the type of bus request (see Table 7–7 for the encoding of this field).
4–5	Request Speed	Request speed indicates the speed at which the phy interface sends the packet for this particular request (see Table 7–8 for the encoding of this field).
6	Stop Bit	Stop bit indicates the end of the transfer (always cleared).

7.5.1.2 TSB12C01A Read-Register Request

Table 7–5. Read-Register Request Functions (Length of Stream: 9 Bits)

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Start bit indicates the beginning of the transfer (always set).
1–3	Request Type	Request type indicates the type of request function (see Table 7–7 for the encoding of this field).
4–7	Address	The address of the phy register to be read.
8	Stop Bit	Stop bit indicates the end of the transfer (always cleared).

7.5.1.3 TSB12C01A Write-Register Request

Table 7–6. Write-Register Request (Length of Stream: 17 Bits)

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Start bit indicates the beginning of the transfer (always set).
1–3	Request Type	Request type indicates that this is a write-register request (see Table 7–7 for the encoding of this field).
4–7	Address	The address of the phy register to be written to.
8–15	Data	The data that is to be written to the specified register address.
16	Stop Bit	Stop bit indicates the end of the transfer (always cleared).

7.5.1.4 Request-Type Field for TSB12C01A Request

Table 7–7. TSB12C01A Request Functions

LREQ[1:3]	NAME	DESCRIPTION
000	TakeBus	Immediate request. Upon detection of an idle, take control of the bus immediately (no arbitration) for asynchronous packet ACK response.
001	IsoReq	Isochronous request. IsoReq arbitrates for control of the bus after isochronous gap.
010	PriReq	Priority request. PriReq arbitrates for control of the bus after a fair gap, ignore fair protocol.
011	FairReq	Fair request. FairReq arbitrates for control of the bus after a fair gap; use fair protocol.
100	RdReg	Read request. RdReg returns the specified register contents through a status transfer.
101	WrReg	Write request. WrReg writes to the specified register.
110, 111	Reserved	Reserved

7.5.1.5 Request-Speed Field for TSB12C01A Request

Table 7–8. TSB12C01A Request-Speed Functions

LREQ[4:5]	DATA RATE
00	100 Mb/s
01	200 Mb/s
10	400 Mb/s
11	Reserved

7.5.2 Bus Request

For fair or priority access, the TSB12C01A requests control of the bus at least one clock after the TSB12C01A phy interface becomes idle CTL[0:1] = 00, which indicates the physical layer is in an idle state. If the TSB12C01A senses that CTL[0:1] = 10, then it knows that its request has been lost. This is true any time during or after the TSB12C01A sends the bus request transfer. Additionally, the phy interface ignores any fair or priority requests when it asserts the receive state while the TSB12C01A is requesting the bus. The link then reissues the request one clock after the next interface idle.

The cycle master uses a normal priority request to send a cycle-start message. After receiving a cycle start, the TSB12C01A can issue an isochronous bus request. When arbitration is won, the TSB12C01A proceeds with the isochronous transfer of data. The isochronous request is cleared in the phy interface once the TSB12C01A sends another type of request or when the isochronous transfer has been completed.

The TakeBus request is issued when the TSB12C01A needs to send an acknowledgment after reception of a packet addressed to it. This request must be issued during packet reception. This is done to minimize the delay times that a phy interface would have to wait between the end of a packet reception and the transmittal of an acknowledgment. As soon as the packet ends, the phy interface immediately grants access of the bus to the TSB12C01A. The TSB12C01A sends an acknowledgment to the sender unless the header CRC of the packet turns out to be bad. In this case, the TSB12C01A releases the bus immediately; it is not allowed to send another type of packet on this grant. To ensure this, the TSB12C01A is forced to wait 160 ns after the end of the packet is received. The phy interface then gains control of the bus and the acknowledge with the CRC error sent. The bus is then released and allowed to proceed with another request.

Although highly improbable, it is conceivable that two separate nodes believe that an incoming packet is intended for them. The nodes then issue a TakeBus request before checking the CRC of the packet. Since both phys seize control of the bus at the same time, a temporary, localized collision of the bus occurs somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a ZZ line state, not a bus reset. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line state is removed. The only side effect is the loss of the intended acknowledgment packet (this is handled by the higher layer protocol).

7.5.3 Read/Write Requests

When the TSB12C01A requests to read the specified register contents, the phy interface sends the contents of the register to the TSB12C01A through a status transfer. When an incoming packet is received while the phy interface is transferring status information to the TSB12C01A, the phy interface continues to attempt to transfer the contents of the register until it is successful.

For write requests, the phy interface loads the data field into the appropriately addressed register as soon as the transfer has been completed. The TSB12C01A is allowed to request read or write operations at any time.

See section 7.6, Status, for a more detailed description of the status transfer.

7.6 Status

A status transfer is initiated by the phy interface when it has some status information to transfer to the TSB12C01A. The transfer is initiated by asserting the following: CTL[0:1] = 01 and D[0:7] = the appropriate states; see Table 7–9 for status-request functions.

The status transfer can be interrupted by an incoming packet from another node. When this occurs, the phy interface attempts to resend the status information after the packet has been acted upon. The phy interface continues to attempt to complete the transfer until the information has been successfully transmitted.

NOTE

There must be at least one idle cycle between consecutive status transfers.

7.6.1 Status Request

The definition of the bits in the status transfer is shown in Table 7–9.

Table 7–9. Status-Request Functions (Length of Stream: 16 Bits)

BIT(s)	NAME	DESCRIPTION
0	Arbitration Reset Gap	The arbitration-reset gap bit indicates that the phy interface has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the IEEE-1394 standard). This bit is used by the TSB12C01A in its busy/retry state machine.
1	Fair Gap	The fair-gap bit indicates that the phy interface has detected that the bus has been idle for a fair-gap time (this time is defined in the IEEE-1394 standard). This bit is used by the TSB12C01A to detect the completion of an isochronous cycle.
2	Bus Reset	The bus reset bit indicates that the phy interface has entered the bus reset state.
3	phy Interrupt	The phy interrupt bit indicates that the phy interface is requesting an interrupt to the host.
4–7	Address	The address bits hold the address of the phy register whose contents are transferred to the TSB12C01A.
8–15	Data	The data bits hold the data that is to be sent to the TSB12C01A.

Normally, the phy interface sends just the first four bits of data to the TSB12C01A. These bits are used by the TSB12C01A state machine. However, if the TSB12C01A initiates a read request (through a request transfer), then the phy interface sends the entire status packet to the TSB12C01A. Additionally, the phy interface sends the contents of the register to the TSB12C01A when it has some important information to pass on. Currently, the only condition where this occurs is after the self-identification process when the phy interface needs to inform the TSB12C01A of its new node address (physical ID register).

There may be times when the phy interface wants to start a second status transfer. The phy interface first has to wait at least one clock cycle with the CTL lines idle before it can begin a second transfer.

7.6.2 Transmit

When the TSB12C01A wants to transmit information, it first requests access to the bus through an LREQ signal. Once the phy interface receives this request, it arbitrates to gain control of the bus. When the phy interface wins ownership of the serial bus, it grants the bus to the TSB12C01A by asserting the transmit state on the CTL terminals for at least one SCLK cycle. The TSB12C01A takes control of the bus by asserting either hold or transmit on the CTL lines. Hold is used by the TSB12C01A to keep control of the bus when it needs some time to prepare the data for transmission. The phy interface keeps control of the bus for the TSB12C01A by asserting a data-on state on the bus. It is not necessary for the TSB12C01A to use hold when it is ready to transmit as soon as bus ownership is granted.

When the TSB12C01A is prepared to send data, it asserts transmit on the CTL lines as well as sends the first bits of the packet on the D[0:1] lines (assuming 100 Mb/s). The transmit state is held on the CTL terminals until the last bits of data have been sent. The TSB12C01A then asserts idle on the CTL lines for one clock cycle after which it releases control of the interface.

However, there are times when the TSB12C01A needs to send another packet without releasing the bus. For example, the TSB12C01A may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the TSB12C01A asserts hold instead of idle when the first packet of data has been completely transmitted. Hold, in this case, informs the phy interface that the TSB12C01A needs to send another packet without releasing control of the bus. The phy interface then waits a set amount of time before asserting transmit. The TSB12C01A can then proceed with the transmittal of the second packet. After all data has been transmitted and the TSB12C01A has asserted idle on the CTL terminals, the phy interface asserts its own idle state on the CTL lines. When sending multiple packets in this fashion, it is required that all data be transmitted at the same speed. This is required because the transmission speed is set during arbitration, and since the arbitration step is skipped, there is no way of informing the network of a change in speed.

7.6.3 Receive

When data is received by the phy interface from the serial bus, it transfers the data to the TSB12C01A for further processing. The phy interface asserts receive on the CTL lines and logic 1 on each D terminal. The phy interface indicates the start of the packet by placing the speed code on the data bus (see the following note). The phy interface then proceeds with the transmittal of the packet to the TSB12C01A on the D lines while still keeping the receive status on the CTL terminals. Once the packet has been completely transferred, the phy interface asserts idle on the CTL terminals that completes the receive operation.

NOTE

The speed code sent is a phy-TSB12C01A protocol and not included in the packets CRC calculation.

SPD = Speed code
D0 => Dn = Packet data

Table 7–10. Speed Code for Receive

D[0:7]	DATA RATE
00xxxxxx†	100 Mb/s
0100xxxx†	200 Mb/s
01010000	400 Mb/s
111111111	Data-on indication

† Note the x means transmitted as 0 and ignored by phy layer.

7.7 TSB12C01A to Phy Bus Timing

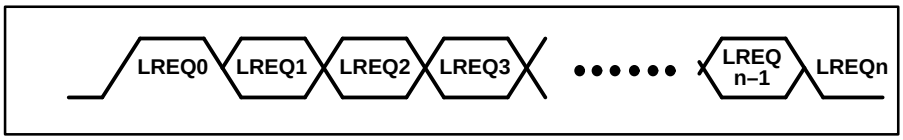


Figure 7–2. LREQ Timing

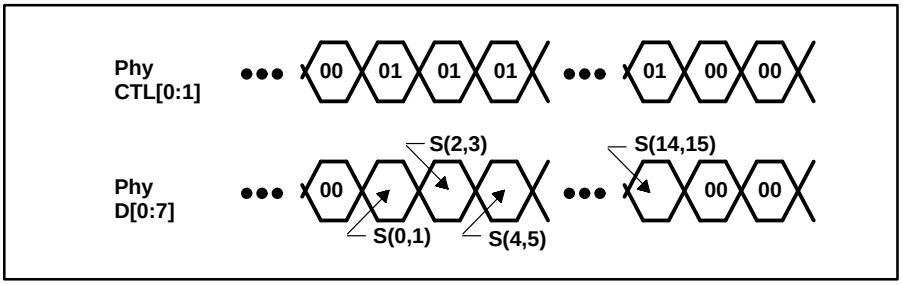
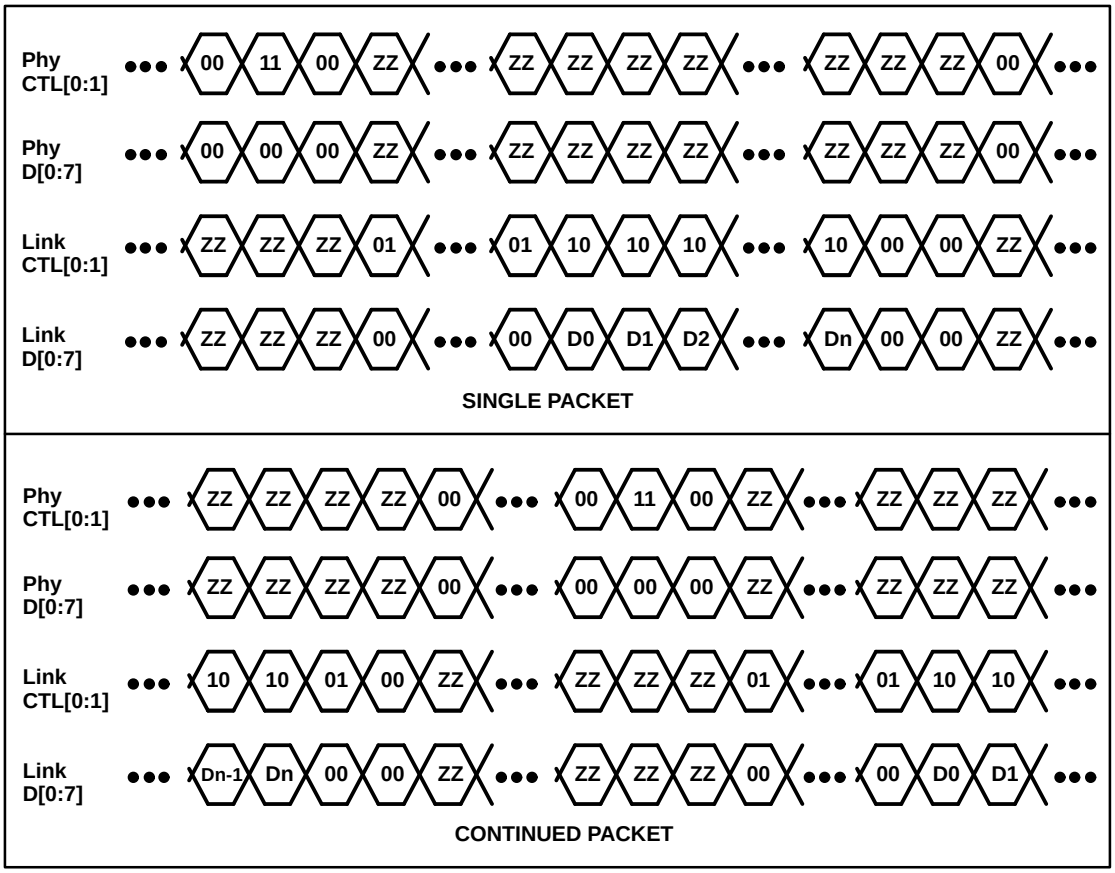


Figure 7–3. Status-Transfer Timing

NOTE A: Each cell represents one SCLK sample time.



NOTE A: ZZ = high-impedance state, D0 – Dn = packet data

Figure 7–4. Transmit Timing

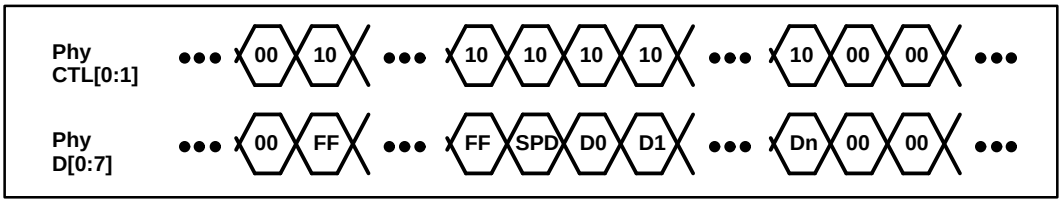


Figure 7–5. Receiver Timing

8 Mechanical Data

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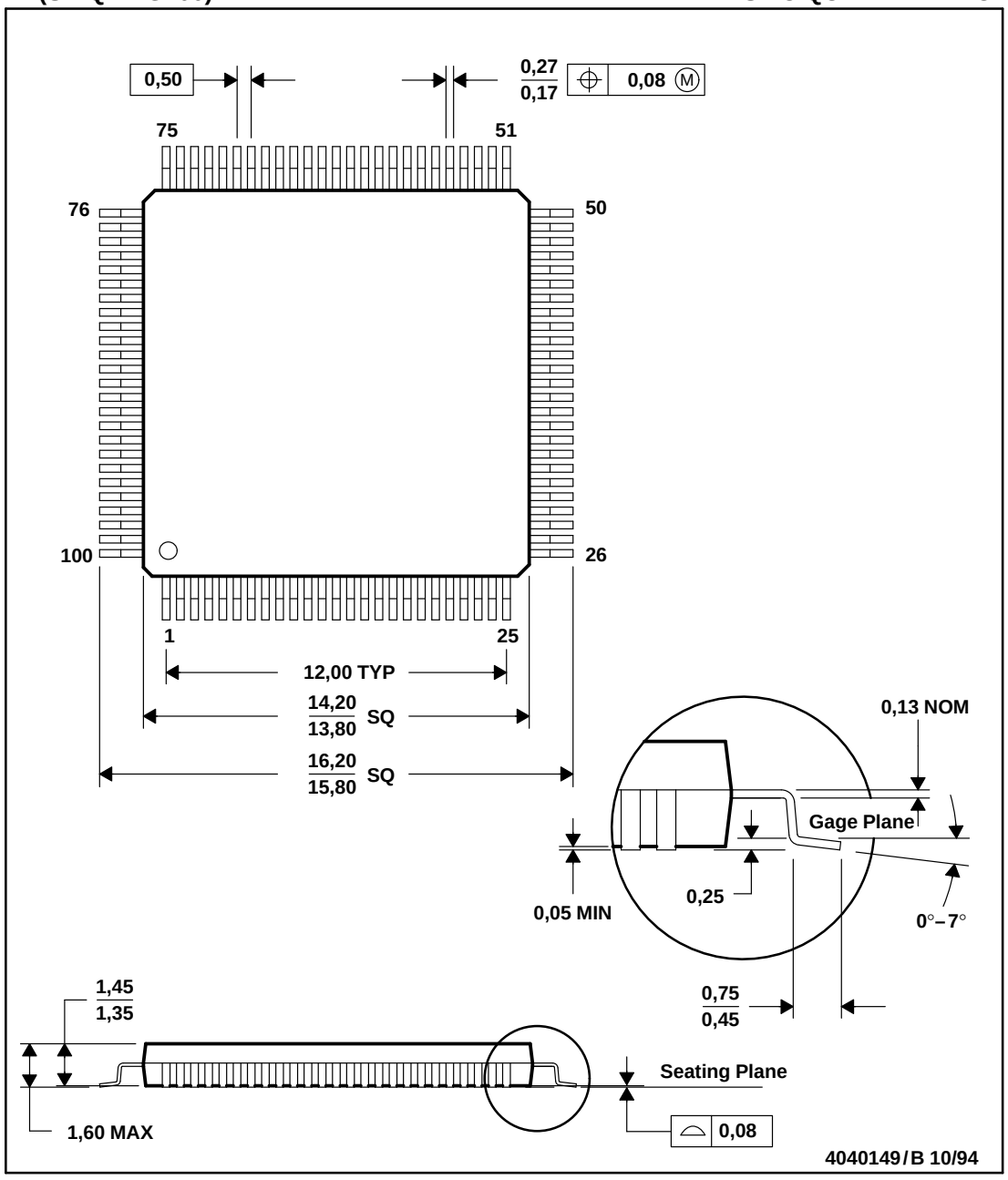

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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