TSB21LV03 Errata List
09/03/97

Errata for the initial production revision of the TSB21LV03 only:

1. There has been a problem with corrupted packets when the PHY supply voltage is at the high end of the spec range and temperature is also at the high end of the spec range. It is recommended that the supply voltage be maintained at the low end of the range, approximately 2.9 volts +/-5% to avoid this problem. This will be fixed in Rev. A. (Production release - TSB21LV03A)

2. The Arbitration Comparators have a wide threshold switching range. This has not caused any problems in applications that we are aware of, but could cause problems in a noisy environment. If it became a problem, the symptom would probably be corrupted packets. This will be fixed in Rev. A (Production Release - TSB21LV03A).

3. The Speed Comparators have a wide threshold range near the threshold region. Also delays through the speed comparators are about 50 ns. This has not caused any problems in applications that we are aware of, but could cause problems in a noisy environment. If it became a problem, the symptom would probably be corrupted packets. This will be fixed in Rev. A (Production Release - TSB21LV03A).

4. The twisted pair drivers have headroom problems under low Vdd and high common mode conditions. This has not caused any problem in applications that we are aware of, but typically would manifest itself in situations where the node was a power provider and maximum voltage drops occurred in the cable power leads. This will be fixed in Rev. A (Production Release - TSB21LV03A)

5. TPBias is not well regulated. This has not caused any problem in applications that we are aware of, but typically would manifest itself in situations where the node was a power provider and maximum voltage drops occurred in the cable power leads. This will be fixed in Rev. A (Production Release - TSB21LV03A)

6. A Pull-Down transistor on the /Reset pin activated by the Power Down (PD) pin was not implemented on the initial production design. This will be fixed in Rev. A (Production Release - TSB21LV03A)

7. The D2, D3 lines do not comply with informative Annex J of the 1394 spec, which specifies that unused data pins shall be driven to a logic 0 during packet reception. Currently, these pins are tri-stated. This will be fixed in Rev A. (Production Release - TSB21LV03A)

8. The TPBias output voltage limits have been relaxed to 1.165 volts minimum to 2.065 volts maximum. These limits should not be a problem in actual systems implementations. The limits are generally only exceeded at the min or max supply levels and there is enough guardband in the standard that it should not be a problem. This will be fixed in Rev A. (Production Release - TSB21LV03A)

9. In the data sheet the pin definitions for Power Programming pins (PC0 to PC2) are incorrect: The correct pin definitions are:

- pin 28 is PC2
- pin 29 is PC1
- pin 30 is PC0

This will be corrected in the datasheet released for the production revision A (TSB21LV03A).

10. In the data sheet on page seven in the row for R0 & R1 (pins 59 and 60) the tolerance on the resistor is incorrect. The correct tolerance is 0.5%. This will be corrected in the datasheet released for the production revision A (TSB21LV03A).

11. In the data sheet on page three in the third paragraph it states that when the power supply is removed the twisted pair drivers will go into a high impedance state. This is incorrect. When power is removed the twisted pair ports could drag down the TPBias of the ports connected to it. If connected to another TSB21LV03 this will only disable the port connected to the powered down TSB21LV03. If connected to a TSB11C01 this could incapacitate all three ports on the TSB11C01 since the TSB11C01 only has a single TPBias shared between the 3 ports. If a multi-port system is designed per the 1394 standard this will not occur since when a node is powered down its PHY is still powered using the 1394 cable power. This will NOT occur if the TSB21LV03 is powered down using the PD terminal since power is still being supplied to the device.

12. If transmitting data at 200 Mbps between nodes 5 or more hops apart, the 21LV03 may cause occasional spurious bus resets. As the number of hops increases the frequency of spurious bus resets will increase. Simulations predict that 4 hops may cause the problem but lab testing could only produce the problem with 5 or more hops with several minutes (five to twenty) between spurious resets. Having 5 hops in the network does not cause the problem, having 5 or more hops in the transmit path between the transmitting node and the furthest end of bus may cause the problem. The most critical path is the asynchronous acknowledge transmit path. This will be fixed in Rev. A (Production Release - TSB21LV03A)

13. When connected to a network with 3 or more hops between the root node and the furthest node on the network, upon bus reset the 21LV03 network may not initially issue the correct number of self-ID packets. If this occurs the 21LV03s that did not issue a self-ID packet will cause another bus reset. This bus reset process will continue until the correct number of self-ID packets are issued unless the process is interrupted by receipt of a non-self-ID packet. The frequency of occurrence (number of resets before multiple self-ID packages occur) averages: 3 hops ~ 1018 resets, 4 hops ~ 133 resets, 5 hops ~ 23 resets, 6 hops ~ 14 resets, 7+ hops ~ 7 resets. Workaround: Optimize your topology to place the root close to the center of the network. To allow the above described bus reset sequence to complete it must not be interrupted by cycle start packets or asynchronous packets. It is recommended that upon bus reset the isochronous resource manager node should wait for 450us after the start of the initial bus reset then check if another bus reset indication has been sent to the link. If another bus reset has been indicated, repeat the wait. If another bus reset has not been indicated then resume cycle start packets and asynchronous packets. The bus manager should use the final package of self_IDs received.
14. Lab test results have shown that there is a possibility of a glitch at the end of data transmission (transition from “data-strobe encoded data” to “data end arbitration line state” at the end of a packet). This glitch may cause an extra data bit to be “received” by the PHY which is then transmitted to the link. This can cause data CRC error acknowledges when asynchronous data is transmitted. Also, it can cause parity errors on the received acknowledge. This glitch will not necessarily cause a problem. It is very narrow, so it is very sensitive and dependent on the application. The problem is supply voltage, cable, layout, and port sensitive. It may be seen on the PHY-LINK interface as an extra 4 bits (at S200 speed) being sent to the link from the PHY, which causes the CRC and parity errors. This will be fixed in Rev. A (Production Release - TSB21LV03A)

Application Notes for both for production revisions (TSB21LV03 & TSB21LV03A):

15. The line A/B status (returned by a read of register 3) will be given as "b0000" if the read is performed immediately following a packet transfer between the PHY and LINK (either transmitter or receive). This is because the line A/B status is set to b0000 during packet transmission/reception, including during the DATA_END time following the actual data transfer of the packet. The link interface will enter the idle state after the data is transferred, but the PHY will still be transmitting/receiving the DATA_END for the packet (for approximately another 240 ns). If a read-register-3 request is performed at this time, the PHY will return b0000 as the line A/B status. This is likely to happen if there is a lot of traffic on the line, since the link will queue up the read-register request until any packet data transfers have completed (as indicated by the PHY-LINK interface going idle), then immediately perform the read-

register request. The line A/B status returned by a read of register 3 is invalid if there is any packet traffic on the line. Because of this, the line A/B status is not very useful for real-time monitoring of the line. Generally, the status will be either b0000 (packet traffic is on the line), or b1111 (the line is IDLE), though other line states are possible if the read is performed at just the right time (for example, during ARBITRATION, tree-ID, or self-ID).

16. On hardware reset only, during the Bus Reset process, the TSB21LV03 will send two status transfers. The first is "invalid" and reports that the local node is Root, with a Node Number of "0", and no other Phys are connected. Later during the same Bus Reset, the correct Root, Node Number and connection status are reported. This double status transfer only occurs during hardware reset, not during initiated software Bus Reset or from Bus Reset received over the bus. For the hardware reset condition only, the Micro must make sure that it does not read the "new" Node Number, Root, and Connection information too soon before the second, correct status transfer has taken place.

17. Due to potential bus hanging problems it is very important that the TSB21LV03's Gap Count setting should never be done directly from the Link by writing to the Phy register directly. The Gap count should only be set with Phy Config Packets. This is a standards issue. TI silicon meets the IEEE 1394-1995 Standard.

Application Changes for production revision A (TSB21LV03A):

18. Bus Holder functionality was added to:

- the Phy/Link interface data pins (pins 13, 14, 15, and 16)
- the Phy/Link interface control pins (pins 11 and 12)
- the Phy/Link interface Link Power Status pin (pin 2)
- the Phy/Link interface Link Request pin (pin 3), and
- the Phy/Link interface Power Down pin (pin 7)

If any of these pins are to be tied to a fixed state through a resistor, the resistor must be sized to provide enough current to overcome the bus hold function. The recommended value is a 1K Ohm resistor.

If pull-down resistors are used on the Control 0 and Control 1 pins these resistors should also use 1KOhm resistors.

The LPS pin is a special case. If the LPS pin is tied to the Link power plane directly it must be connected through a 1K Ohm resistor to avoid problems in the case of the PHY being powered down and the link being powered up. The 1K Ohm resistor

prevents the link power plane from supplying power via the LPS connection to the PHY when the PHY is powered down.

This requires changes to the opto-isolator based isolation circuits shown in the application portion of the data sheet. In the circuit for the LPS terminal (figure 14) change the 5KOhm resistor to a 1KOhm resistor and change the TIL191A to a TIL191B. In the circuit for the PD terminal (figure 18) change the 470 Ohm resistor to a 600 Ohm resistor, change the 7.2KOhm resistor to a 2KOhm resistor, and change the TIL191A to a TIL191B. Finally for consistency change the TIL191A to a TIL191B in figures 19 and 20. This will be changed in the documentation for production release A (TSB21LV03A).

19. The SYSCLK output is active when chip reset is active (Low) on TSB21LV03A. On the TSB21LV03 SYSCLK was not active when chip reset was low.