Texas Instruments
TSB12LV21A

# PCILynx Revision A Errata

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This errata applies to PCILynx TSB12LV21A **production** devices; PCI revision ID = 2 & 3.

# PCILynx Revision A Errata

**Errata 1**
Under some unusual conditions a slave access to PCILynx can be continuously retried on the PCI bus if posted writes are enabled.

Suggested Work Around:
The ENA_POST_WR bit in the MISCELLANEOUS CONTROL register must be set to 0.

**Errata 2**
No error indication is given when the following type of illegal packet is received. A packet containing a header with a tcode for a no-data or quadlet data packet which also contains a data block payload. In these cases the tcode specified that there should be no data block payload. If a data block payload is attached to such a packet, no error is indicated. In normal (other than snoop) mode, the PCILynx DMA transfers only the data specified in the header to the data buffer and the remaining data is flushed. In snoop mode, all data is transferred.

**Errata 3**
The ATF underflow counter is only incremented when an ack status of 10010 (type 1 code 2) is returned. In the case of a packet with multiple errors including an ATF underflow, the underflow will not be counted if the ack status reports another error.

**Errata 4**
There have been reports of transmit ack error code 11110 (type 1 code E) which specifies that the link reported a corrupted header before the packet was transmitted. The exact nature of this error is not known, however it is believed to be related to retries and/or underflow errors.