TSB12LV41 (MPEG2Lynx)

IEEE 1394-1995 Link-Layer Controller for MPEG-2 Transport

SLLS276A
AUGUST 1997

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1 Introduction

1.1 Description

The TSB12LV41 link-layer controller (LLC) (sometimes called MPEG2Lynx) complies with the IEEE 1394-1995 (from here on referred to as 1394) specification for high-performance serial bus, transmits and receives correctly formatted 1394 packets, detects lost cycle-start packets, and generates and inspects the 32-bit cyclic redundancy check (CRC). The TSB12LV41 is also capable of performing the functions of cycle master (CM), isochronous resource manager (IRM), and bus manager (BM).

The TSB12LV41 provides a 1394 interface for high-performance audio, video, and data applications at up to 200 Mbits/s and is suitable for set-top boxes, multimedia tape and disk drives, and other consumer electronic devices requiring MPEG-2 formatted isochronous data transfer according to the IEC61883 specification. The TSB12LV41 also supports non-MPEG-2/DSS isochronous and asynchronous data transfer with an auto-packetization feature.

The TSB12LV41 interfaces directly to most microprocessors and microcontrollers, including the TSM32AV7000 family of DSP solutions from Texas Instruments. The bulky data interface (BDIF) enables MPEG-2, DSS, isochronous, or asynchronous data transfer in bit-wide, byte-wide, and memory-mapped modes. A 256-byte control FIFO allows asynchronous transmit and receive control packets while an 8K-byte BDIF FIFO provides independent logical FIFOs for MPEG-2/DSS, isochronous, and asynchronous data transmit and receive. The BDIF FIFO performs a hardware asynchronous packet transmit retry for up to 256 times with intervals up to 256 $\times$ 125 μs. The TSB12LV41 supports full-width time-stamped offsets for MPEG-2 and DSS transmit and receive, and also performs age filtering functions.

1.2 Features

The TSB12LV41 supports the following features:

- Supports Provisions of IEEE 1394-1995 Standard for High-Performance Serial Bus
- Interoperable with FireWire™ Implementation of the 1394 standard
- Interfaces Directly to Texas Instruments TSB11C03, TSB11LV01, and TSB21LV03 Physical Layer (Phy) Devices (100/100/200Mbits/s)
- Interfaces Directly to Texas Instruments TMS320AV7100/7110/7200 Series DSS and MPEG-2 Decoders
- Multimode 8-/16-bit Microcontroller/Microprocessor Interface Supports Many Processors
- Interrupt Driven to Minimize Host Polling
- 8K × 8-bit FIFO supports MPEG-2/DSS, Asynchronous, and Isochronous Modes for Transmit and Receive
- 64 Quadlet (256-Byte) Control FIFO Accessed Through Microcontroller Interface Supports Command/Status Operations
- Supports Bus Functions and Automatic 1394 Self-ID Verification
- Single 3.3-V Supply Operation with 5-V Tolerance Using 5-V Bias Terminals
- High-Performance 100-Pin PZ (S-PQFP-G100) Package

1.3 Related Documents

- IEEE STD IEEE 1394-1995 High-Performance Serial Bus
- IEC 61883 Digital Interface for Consumer Electronic Audio/Video Equipment

FireWire is a trademark of Apple Computer, Incorporated.

1.4 Terminal Assignments

PZ PACKAGE
(TOP VIEW)

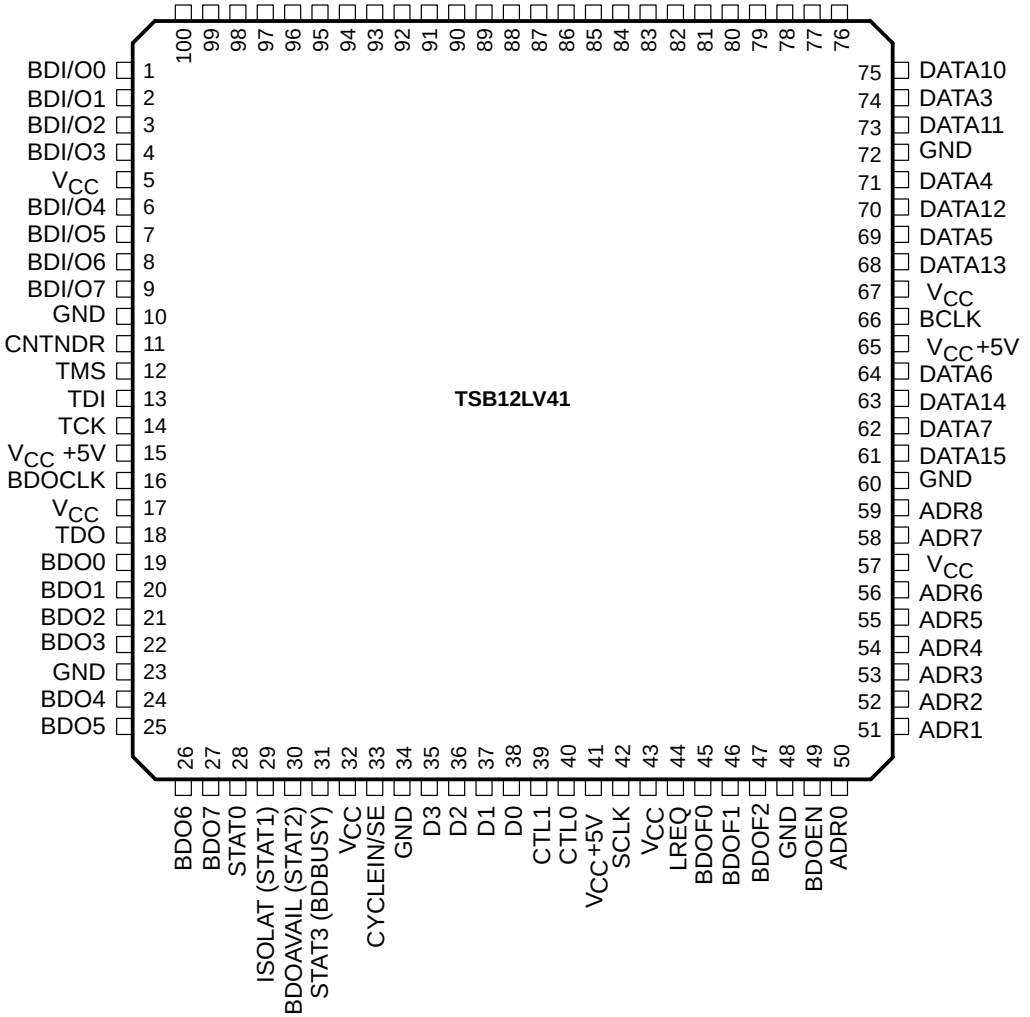

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Table 1–1. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADR0 – ADR8	50,51,52,53,54, 55,56,58,59	I	MP/MC address lines.
BCLK	66	I	Host Bus Clock
BDIF0 – BDIF2	98,99,100	I/O	Indicator lines for BDIF. BDIF0 – BDIF2 are used to select the type of data.
BDI/O0 – BDI/O7	1,2,3,4,6,7,8,9	I/O	I/O bus data. BDI/O0 – BDI/O7 are data lines for high speed I/O bus for audio/data/video applications.
BDICLK	91	I	Bulky data I/O clock. BDICLK operates at up to 40 MHz in parallel mode and up to 80MHz in serial mode.
BDIEN	93	I	BDI bus enable. When low, BDIEN causes accesses to BDI-bus to be ignored.
BDO0 – BDO7	19,20,21,22,24, 25,26,27		Bus data output. BDO0 – BDO7 are data lines for the high-speed output bus for audio/data/video applications compliant to several standard interfaces.
$\overline{\text{BDOAVAIL}}$(STAT2)	30	O	Bulky data output available/status output 2. $\overline{\text{BDOAVAIL}}$(STAT2) indicates that BDO is available.
BDOCLK		I	Bulky data output clock. The BDOCLK operates at up to 40 MHz in parallel mode and up to 80 MHz in serial mode.
BDOF0 – BDOF2	45,46,47	O	Indicator lines for high speed I/O bus.
BDOEN	49	I	BDO bus enable. When BDOEN is asserted low, accesses to BDO-bus are ignored.
CNTNDR	11	I/O	Bus manager contender. CNTNDR tells the LLC when the local node is a contender for IRM/BusManager. This signal can alos be driven by the LLC. The default state of this signal is input.
CS1	86	I	Chip select. CS1 must be asserted low when device is to be selected for reads and writes.
CTL0,CTL1	40,39	I/O	Control 0 and control 1 of the phy-link control bus. CTL0 and CTL1 control the four operations that can occur in this interface.
CYCLEIN/SE	33	I	Cycle in. CYCLEIN is an optional external 8-kHz clock used as the cycle clock, and it should only be used when attached to the cycle master node. CYCLEIN is enabled by the cycle source bit and should be tied high when not used.
D0 – D3	38,37,36,35	I/O	Phy-link data. D0 – D3 is data input from the phy-link data bus. Data is expected on D0 – D1 for 100 Mbps and D0 – D3 for 400 Mbps.
DATA0 – DATA15	80,78,76,74,71, 69,64,62,79,77, 75,73,7068,63, 61	I/O	Data 0 – 15 of MC/MP host processor; some of these have 2nd functions dependent on MCSEL pins
GND	10,23,34,48,60, 72,87,97		Ground reference
$\overline{\text{INT}}$	89	O	Interrupt. $\overline{\text{INT}}$ notifies the host that an interrupt has occurred. This line can be active low or active high dependent on the INTPOL bit in the IOCR register. It is is in a high-impedance state when no interrupt has occurred.

Table 1–1. Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{ISOLAT}}$(STAT1)	29	I/O	$\overline{\text{Isolation mode}}$/status output 1. $\overline{\text{ISOLAT}}$ (STAT1) is sampled during a hardware reset to determine if isolation is present. When this input signal is high, isolation is not present. $\overline{\text{ISOLAT}}$ (STAT1) is a status output signal after a hardware reset.
LREQ	44	O	Link request. LREQ is a TSB12LV41 output that makes bus request and accesses the phy.
MCCTL0, MCCTL1	82,83	I	Control lines for bus access function depends on MP/MC-type
MCSEL0, MCSEL1	84,85	I	Select lines for MP/MC-type used. Has impact on function MCTRL,ADR, RDY and DATA terminals.
RDY	88	O	Ready line. When asserted high, RDY indicates the end of an MP/MC access.
$\overline{\text{RESET}}$	96	I	Reset. $\overline{\text{RESET}}$ is the asynchronous power on reset to the TSB12LV41 and is active low.
SCKEN	94	I	Scan Enable. This signal is for test purposes only.
SCLK	42	I	System clock. SCLK is a 49.152-MHz clock from the phy. From SCLK the 24.576-MHz clock is generated.
STAT0	28	O	Status output 0.
STAT3(BDIBUSY)	31	O	Status output 3/bulky data interface is busy status. When high, STAT3(BDIBUSY) indicates that the bulky data interface is busy.
TCK	14	I	Test clock.
TDI	13	I	Test data in.
TDO	18	O	Test data out.
TMRST	95	I	Test mode reset. This signal is for test purposes only.
TMS	12	I	Test mode select. TMS is used for JPEG.
V_{CC}	5,17,32,43,57, 67,81,92		3.3V (3.0 V – 3.6 V) power supplies
V_{CC}+5V	15,41,65,90		5V ±5% power supplies

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2 Architecture

The following sections give an overview of the TSB12LV41. Figure 2–1 shows a functional block diagram of the TSB12LV41.

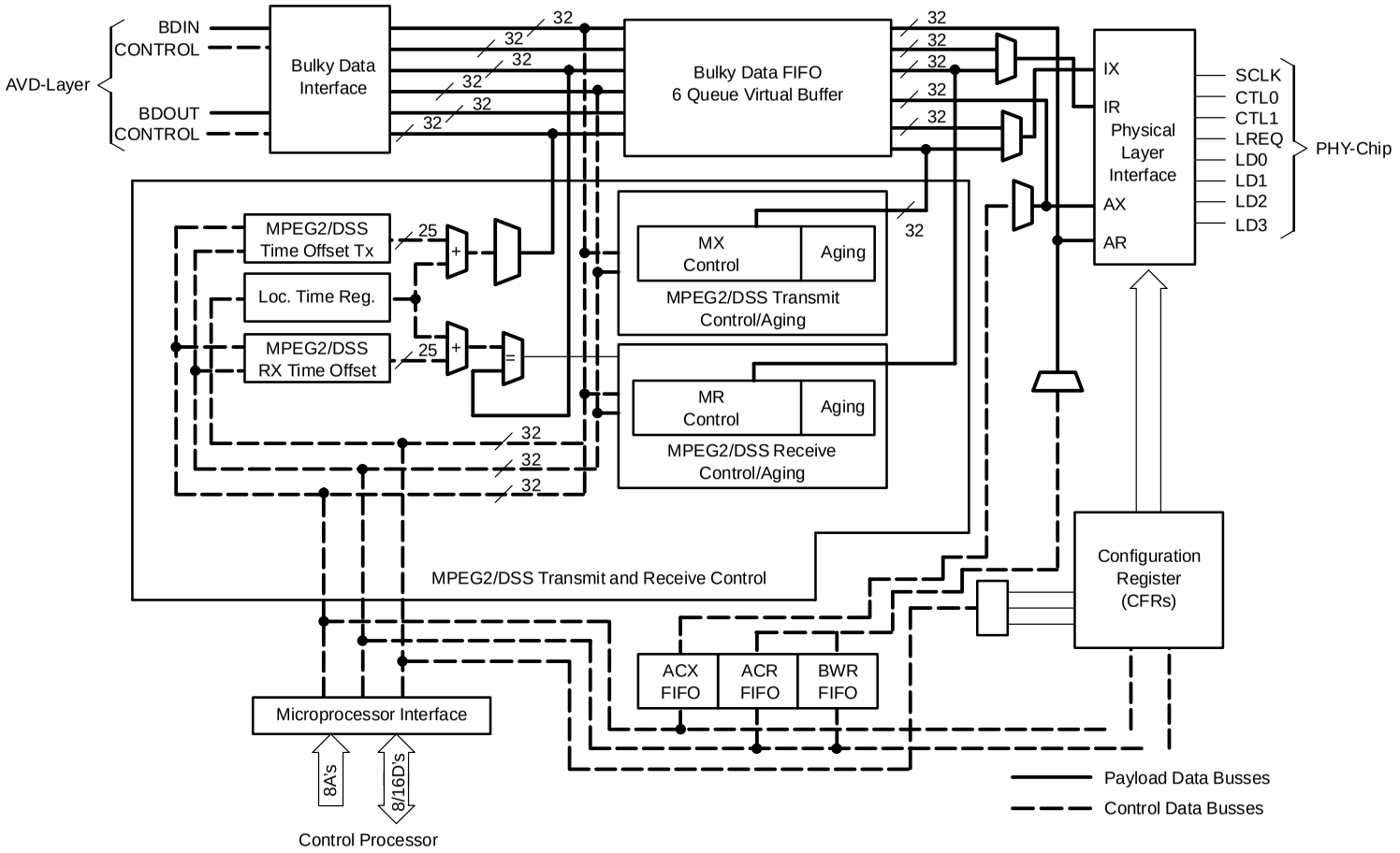


Figure 2–1. Functional Block Diagram

2.1 Bulky Data Interface

The bulky data interface (BDI) enables the TSB12LV41 to provide sustained data rates up to 160 Mbits/s. The BDIF FIFO supports MPEG-2/DSS, asynchronous, and isochronous packets for receive and transmit.

2.2 Bulky Data FIFO (6-Queue Virtual Buffer)

The Bulky Data FIFO is where transmit and receive data is buffered via the Bulky Data Interface (BDIF). The Bulky Data FIFO is partitioned into six logical FIFOs. Each of these logical FIFO's size is programmable on four quadlet boundaries. These six FIFO are called:

- BDIF MPEG2/DSS Transmit (BMDTX)
- BDIF MPEG2/DSS Receive (BMRDX)
- BDIF Asynchronous Transmit (BATX)
- BDIF Asynchronous Receive (BARX)
- BDIF Isochronous Transmit (BITX)
- BDIF Isochronous Receive (BIRX)

The following sections give functional descriptions of these logical FIFOs.

2.2.1 BDIF MPEG-2/DSS Transmit FIFO (BMDTX)

The BMDTX FIFO is used to transmit either MPEG2 or DSS data. Data is typically written to this FIFO from the BDIF or microcontroller in quadlets (four bytes). See Section 5 for more detail on using this FIFO to transmit MPEG/DSS data.

2.2.2 BDIF MPEG-2/DSS Receive FIFO (BMDRX)

The BMDRX FIFO is typically used to store MPEG2/DSS data received from the link layer core to be forwarded to a high-speed application via the BDIF. Data can be written to this FIFO by either the link layer core of the microcontroller. See section 5 for more details.

2.2.3 BDIF Asynchronous Transmit FIFO (BATX)

The BATX FIFO is typically used to transmit data packets from high-speed applications. Data can be loaded into this FIFO with the BDIF or the microcontroller.

2.2.4 BDIF Asynchronous Receive FIFO (BARX)

The BARX FIFO is typically used to store received bulky asynchronous data packets to be forwarded to a high-speed application via the BDIF. Data is provided to the BDIF or the microcontroller interface. See Section 5 for more details.

2.2.5 BDIF Isochronous Transmit FIFO (BITX)

The BITX FIFO is typically used to transmit data packets from high-speed applications. Data can be loaded into this FIFO with the BDIF of the microcontroller.

2.2.6 BDIF Isochronous Receive FIFO (BIRX)

The BIRX FIFO is typically used for receiving isochronous data forwarding it on to a high-speed application. Data is provided to the BDIF of microcontroller interface. See Section 5 for more details.

2.3 MPEG2/DSS Transmit and Receive Control

The following sections give information on MPEG2 and DSS transmit and receive control.

2.3.1 Local Time Register

This register is typically called the cycle timer. It contains the synchronized 1394 cycle timer as specified by the IEEE 1394-1995 standard. The Local Time register is used to timestamp packets (insert a snapshot of the timer value into a packet) and also used by the aging routine.

2.3.2 MPEG2/DSS Transmit and Receive Control/Aging

This circuitry controls automatic insertion of the CIP (common isochronous packet) header information as defined by the IEC61883 standard. An aging algorithm is also performed for both transmitted and received

MPEG2/DSS packets. The aging algorithm is used to invalidate packets based on the timestamp encapsulated in the MPEG2/DSS header.

2.4 Microprocessor/Microcontroller Interface

The microprocessor/microcontroller (MP/MC) interface is used as the host controller port and is designed to work with several standard MP/MCs including Motorola's 68000, Intel's 8051, and the built-in ARM processor in Texas Instruments's TMS320AV7100 set-top box decoder. This interface supports both 8-bit and 16-bit wide data busses as well as both little endian and big endian microprocessors. See Section 65 for more details.

2.5 Control FIFO

The Control FIFO is partitioned into three logical FIFOs. The size of each of these logical FIFOs is programmable on quadlet boundaries. These three FIFOs are called:

- Asynchronous Control Transmit FIFO (ACTX)
- Asynchronous Control Receive FIFO (ACRX)
- Broadcast Write Receive FIFO (BWRX)

2.5.1 Asynchronous Control Transmit FIFO (ACTX)

The ACTX FIFO is typically used to transmit small asynchronous control packets as sent by the microprocessor/microcontroller. The ACTX FIFO can also be used to support asynchronous traffic at very low data rates. Asynchronous packets are generated by using the ACTXF, ACTXC, ACTXFU, and the ACTXCU all of which access the ACTX FIFO.

2.5.2 Asynchronous Control Receive FIFO (ACRX)

The ACRX FIFO is typically used to receive asynchronous control packets other than the SelfID packet (See Section 2.5.3). Regular asynchronous control packets typically go to the ACRX FIFO. This FIFO is mapped to the ACRX register. A read from this register accesses the ACRX FIFO. Received asynchronous packets are steered into either the ACRX or BARX FIFOs or both.

2.5.3 Broadcast Write Receive FIFO (BWRX)

The BWRX FIFO is typically used to receive asynchronous broadcast write request packets.

2.6 Physical Layer Interface

The physical layer interface provides phy-level services to the transmitter and receiver. This includes gaining access to the serial bus, sending packets, receiving packets, and sending and receiving acknowledgement packets.

2.7 Configuration Register (CFR)

The TSB12LV41 is configured for various modes of operation using CFRs. These registers are accessed via the host microprocessor/microcontroller. Section 3 gives a map of all the registers and detailed descriptions of all register bits.

3 Detailed Operation and Programmers Reference

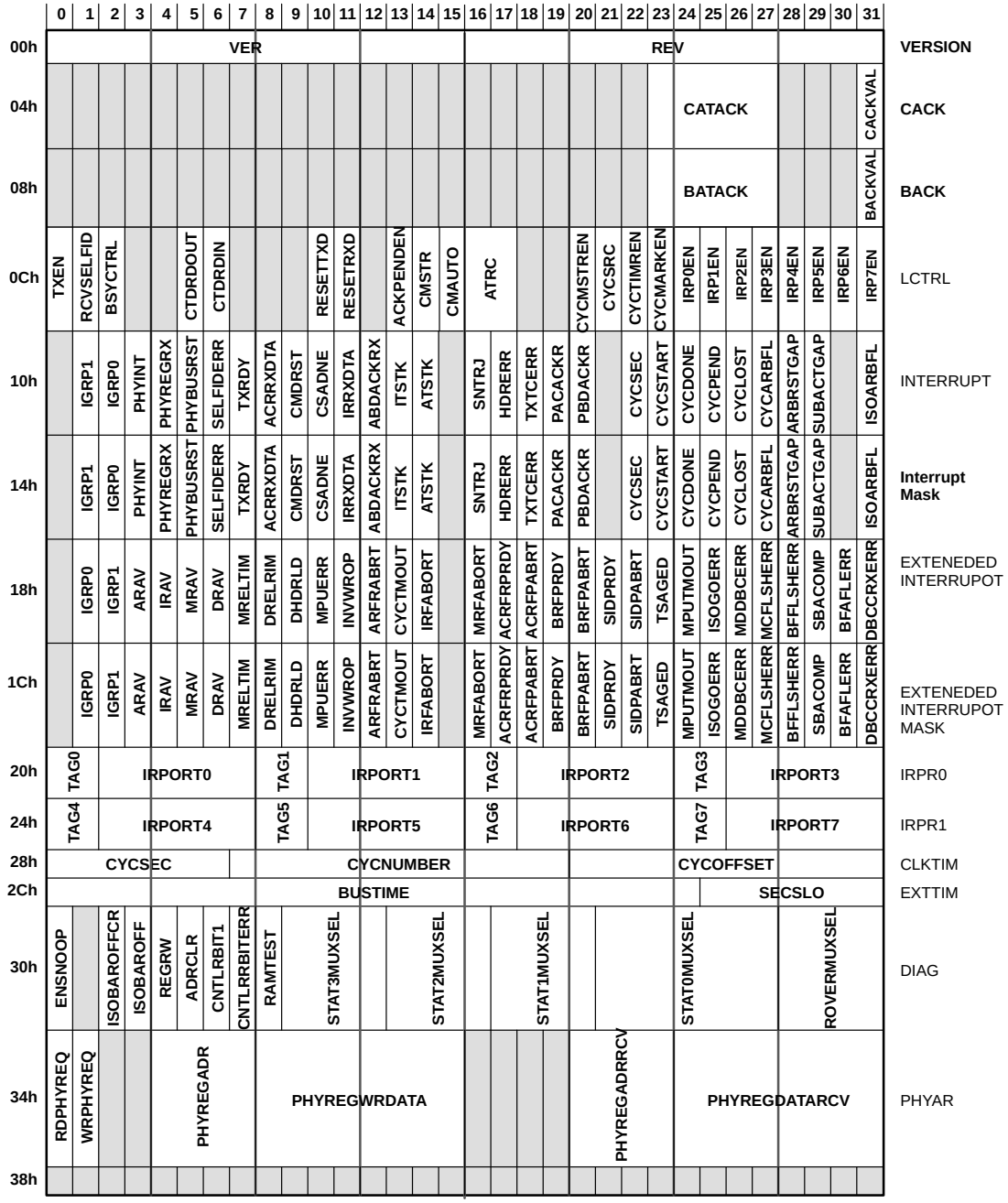
3.1 TSB12LV41 Configuration Register

The TSB12LV41 CFR map is shown in Figure 3–1.

NOTE:

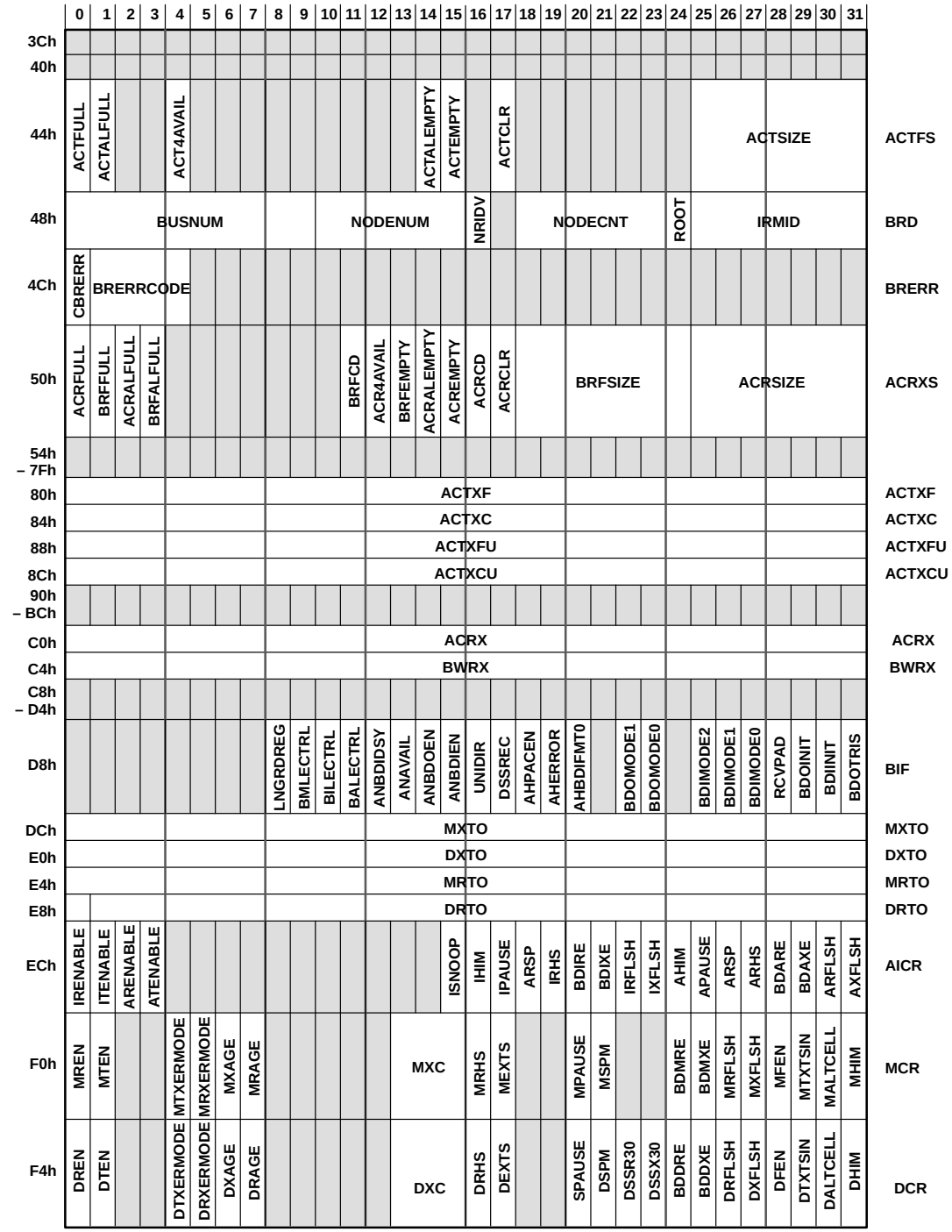
The following register pairs are aliased (are the same):

MXT0 (address DCh)	=	DXT0 (address E0h)
MRT0 (address E4h)	=	DRT0 (address E8h)
MCR (address F0h)	=	DCR (address F4h)
BMSZ (address 150h)	=	MDSZ (address 158h)
BMAVAL (address 154h)	=	BDAVAL (address 15Ch)
BMTXFC (address 160h)	=	BDTXFC (address 16Ch)
BMTXLS (address 164h)	=	BDTXLX (address 178h)
BMRX (address 168h)	=	BDRX (address 174h)
MRH (address 178h)	=	DRH (address 188h)
MCIPR0 (address 17Ch)	=	DCIPR0 (address 18Ch)
MCIPR1 (address 180h)	=	DCIPR1 (address 290h)
MRT (address 184h)	=	DRT (address 194h)
MXH (address 1C8h)	=	DXH (address 1D4h)
MCIPX0 (address 1CCh)	=	DCIPX0 (address 1D8h)
MCIPX1 (address 1D0h)	=	DCIPX1 (address 1DCh)



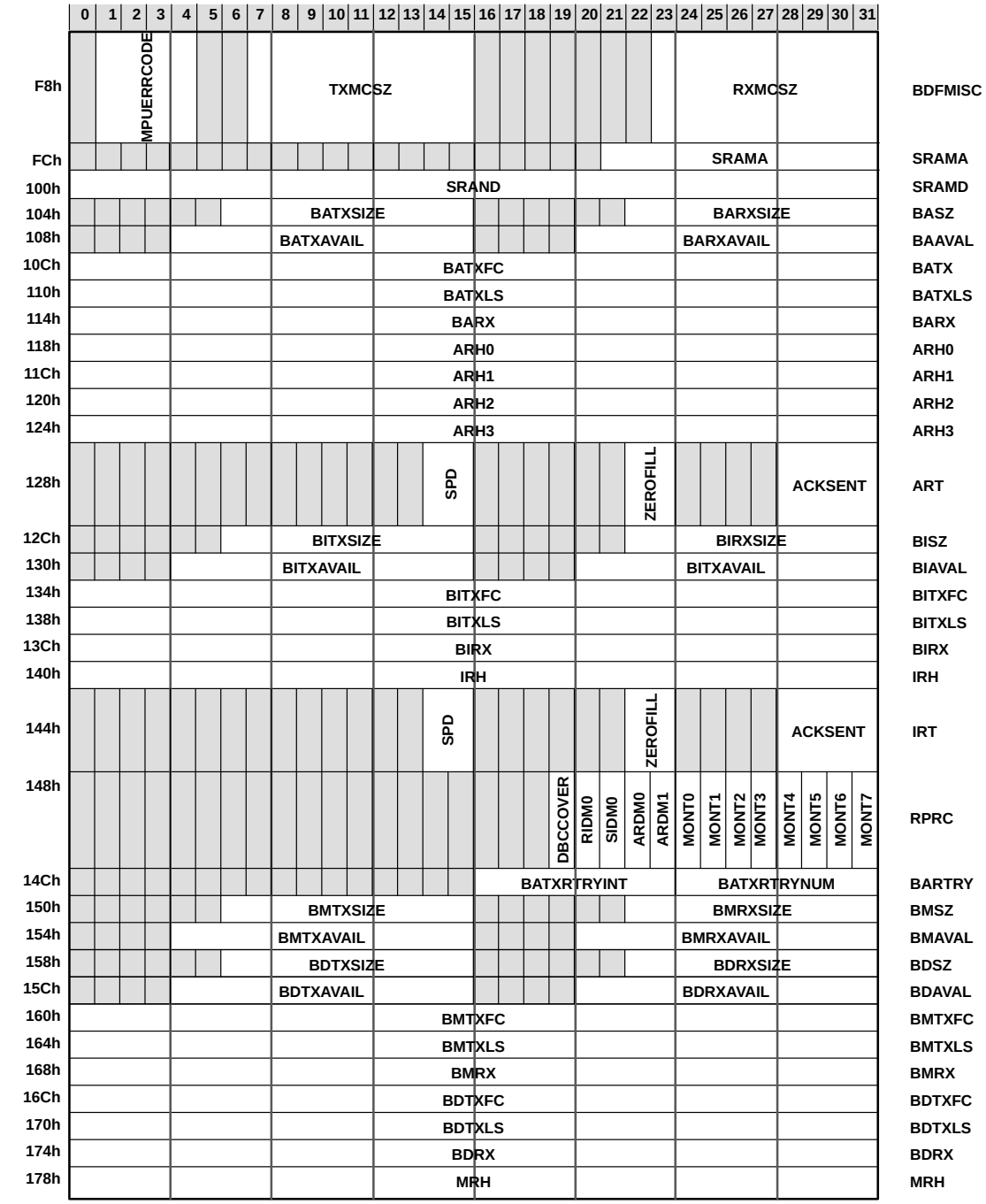
NOTE A: All gray areas (bits) are reserved bits.

Figure 3–1. Configuration Register (CFR) Map



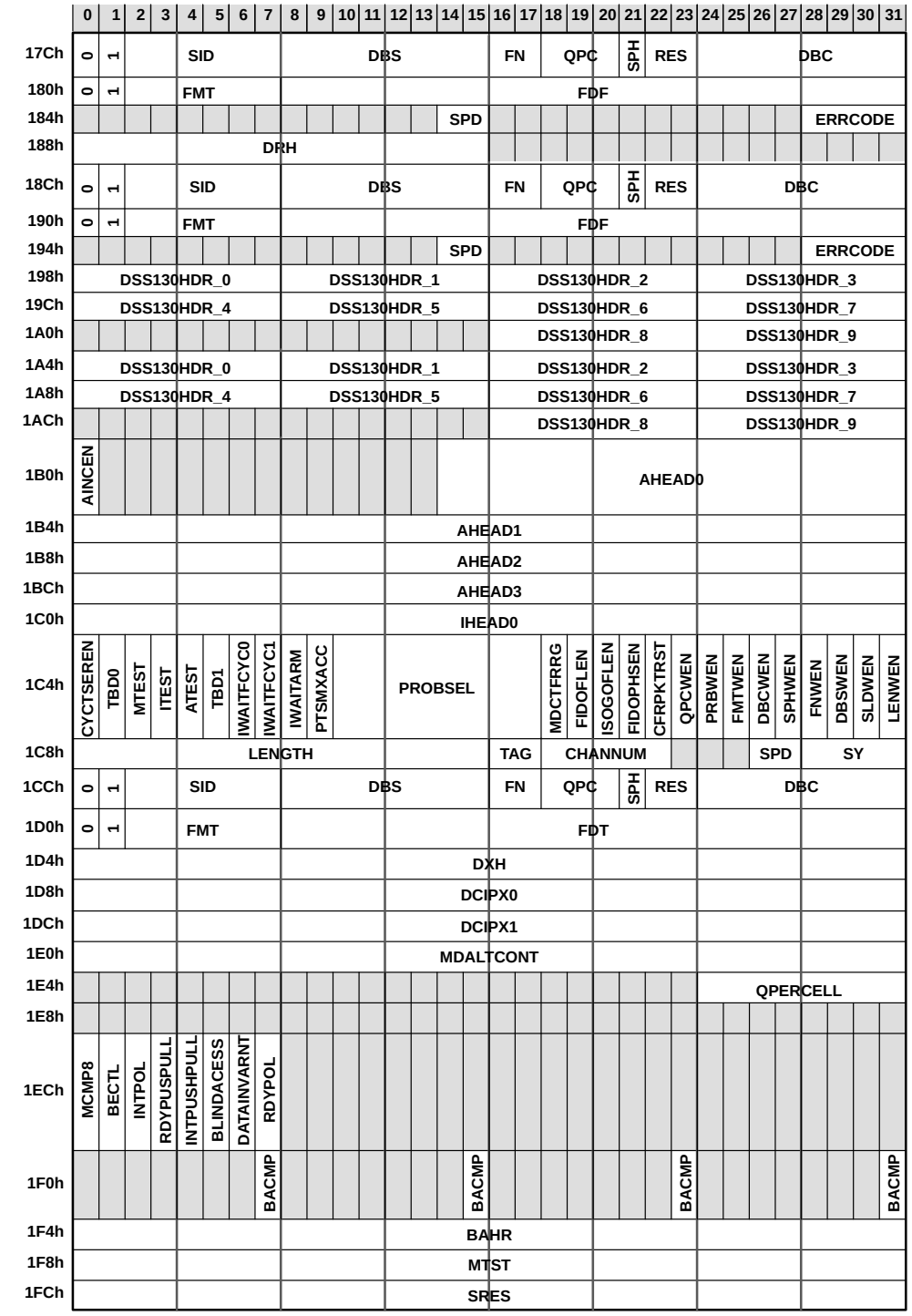
NOTE A: All gray areas (bits) are reserved bits.

Figure 3–1. Configuration Register (CFR) Map (continued)



NOTE A: All gray areas (bits) are reserved bits.

Figure 3–1. Configuration Register (CFR) Map (continued)



NOTE A: All gray areas (bits) are reserved bits.

Figure 3–1. Configuration Register (CFR) Map (continued)

3.2 Version Register (VERS @ Addr 0h)

This address port provides the application software with the version number and revision number of the MPEG2Lynx device. These numbers are hardwired in the logic of the device.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 15	VER	R	Version number. Hardwired value = CE03h
16 – 31	REV	R	Revision Number. Hardwired value = 1394h

3.3 C Acknowledge Register (CACK @ Addr 4h)

This register provides the application software with the last acknowledge that was received for an ASYNC packet transmitted from the ASYNC Transmit control FIFO. Unless otherwise specified the bits in this register are cleared to 0 on power-up or software initiated reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION	
00 – 22	Not Used	R		
23 – 27	CATACK	R	The acknowledge value received from the link transmitter for a packet that was transmitted from the ASYNC control transmit FIFO. These bits can be written to by setting the REGRW bit in the diagnostic test register (DIAG @ Addr 30h) to 1.	
			CATACK[23]	**CATACK[24:27]**
			0	Normal 1394 4 bit ack code.
			1	0000 – No Ack received. Ack timeout
			1	0001 – Ack pkt longer than 8 bits
			1	0010 – Ack pkt shorter than 8 bit
28 – 30	Not Used	R		
31	CACKVAL	R	This bit is set to logic 1 to indicate that the value of CATACK[23:37] has been updated with a new value. This bit is cleared to 0 when the application software reads this register to obtain the value of CATACK and CACKVAL. This bit can be written to by setting the REGRW bit in the diagnostic test register (DIAG @ Addr 30h) to 1.	

3.4 Backnowledge Register (BACK @ Addr 8h)

This register provides the application software with the last acknowledge that was received for an ASYNC packet transmitted from the ASYNC Transmit Bulky FIFO. Unless otherwise specified the bits in this register are cleared to 0 on power-up or software initiated reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 22	Not Used	R	
23 – 27	BATACK	R	The acknowledge value received from the link transmitter for a packet that was transmitted from the ASYNC bulky transmit FIFO. These bits can be written to by setting the REGRW bit in the diagnostic test register (DIAG @ Addr 30h) to 1.
			BATACK[23] / **BATACK[24:27]**
			0 / Normal 1394 4 bit ack code.
			1 / 0000 – No Ack received. Ack timeout
			1 / 0001 – Ack pkt longer than 8 bits
			1 / 0010 – Ack pkt shorter than 8 bit
28 – 30	Not Used	R	
31	BACKVAL	R	This bit is set to logic 1 to indicate that BATACK is valid. This bit can be written to by setting the **REGRW** bit in the diagnostic test register (**DIAG @ Addr 30h**) to 1.

3.5 Link Control Register (LCTRL @ Addr Ch)

This register provides the application software with the capability to control and configure the operation of the 1394 link layer logic. Unless otherwise specified the bits in this register are cleared to 0 on power-up or software initiated reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	TXEN	R/W	Transmit Enable. When set to logic 1 this bit enables the link transmitter to begin bus arbitration and packet transmission. When set to logic 0, the operation of the link transmitter is disabled from operating.
01	RCVSELFID	R/W	Receive self ID enable. When set to a logic 1 this bit enables the link layer to receive self ID packets during 1394 bus initialization.
02	BSYCTRL	R/W	Transaction layer busy override. When set to logic 1 the link receiver will unconditionally busy off all acknowledgeable incoming packets with BUSY_X. When set to logic zero the link receiver uses the availability of the selected receiving FIFO to determine if an incoming acknowledgeable packet is to be accepted or busy off (BUSY_X).
03 – 04	Not Used		

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
05	CTDRDOUT	R/W	Contender Data out. This bit is used to set the logic value of the external pin CONTENDER when it has been programmed to operate in output mode.
			DESCRIPTION
			0 = Link in not a contender for isochronous resource manager.
			1 = Link is a contender for isochronous resource manager.
06	CTDRDIN	R/W	Contender Data direction control. This bit is used in setting the direction of the external contender pin. This pin set to logic 1 on power–up or software reset.
06	CTDRDIN	R/W	**DESCRIPTION**
06	CTDRDIN	R/W	CONTENDER pin is in output mode and will be driven by the value of CTDRDOUT
06	CTDRDIN	R/W	CONTENDER pin is in input mode.
07 – 09	Not Used		
10	RESETTXD	R/W	Reset Link Transmitter. Writing a 1 to this bit will reset all state machines in the link layer which are involved in transmitting a packet. This bit is self clearing.
11	RESETRXD	R/W	Reset Link Receiver. Writing a 1 to this bit will reset all state machines in the link layer which are involved in the reception of a packet. This bit is self clearing.
12	Not Used		
13	ACKPENDEN	R/W	Ack pending enabled. When set to a 1 this bit enables the link receiver to acknowledge write and lock request packets with an ack pending code of (2h). If this bit is set to 0 then the receiver will use the ack_complete code of (1h). This bit is set to a 1 on power-up or software reset.
14	CMSTR	R/W	When CMAUTO is high and CMSTR is high the CYCMSTREN enable bit is automatically set to 1 if the root bit is 1 following a bus reset.
15	CMAUTO	R/W	When CMAUTO is high and CMSTR is high the CYCMSTREN and CYCTIMREN bits are automatically set to 1 if the root bit is 1 following a bus reset.
16 – 17	ATRC	R/W	Async transmit retry code. This code is logically OR'ed with the retry code field (00) in the transmit packet, and the packet is resent.
			DESCRIPTION
			00 = retry_O (new)
			01 = retry_X
			10 = retry_A
			11 = retry_B

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
18 – 19	Not Used		
20	CYCMSTREN	R/W	When this bit is set to 1 and the attached phy is the root, the cyclemaster function is enabled for transmitting cycle start packets.
21	CYCSRC	R/W	When CYCSRC is set to 1, the cycle_count field of the cycletimer increments and the cycle_offset field of the cycle timer resets for each positive transition of CYCLEIN. When CYCSRC is set to 0, the cycle_count field increments when the cycle_offset field rolls over.
22	CYCTIMREN	R/W	Cycle timer enable. The cycle timer is enabled to count when this bit is set to 1. The cycle timer is disabled when the bit is set to 0.
23	CYCMARKEN	R/W	Cycle mark enable. When this bit is set to 1, cycle marks are inserted into the bulky MPEG/DSS receive FIFO at the end of each isochronous cycle. When this bit is set to 0 then no cycle marks are inserted.
24	IRP0EN MPEG/DSS	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 0 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to an expected value. The packet is received if the comparator detects a match.
25	IRP1EN	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 1 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to and expected value. The packet is received if the comparator detects a match.
26	IRP2EN	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 2 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to and expected value. The packet is received if the comparator detects a match.
27	IRP3EN	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 3 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to and expected value. The packet is received if the comparator detects a match.
28	IRP4EN	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 4 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to and expected value. The packet is received if the comparator detects a match.
29	IRP5EN	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 5 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to and expected value. The packet is received if the comparator detects a match.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
30	IRP6EN	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 6 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to and expected value. The packet is received if the comparator detects a match.
31	IRP7EN	R/W	Iso receive port comparator enable. When this bit is set to 1 the channel 7 MPEG/DSS packet receive comparator is enabled for comparing the channel number and/or tag field of the incoming packet to and expected value. The packet is received if the comparator detects a match.

3.6 Interrupt Register/Interrupt Mask Register (IR @ Addr 10h/14h)

The interrupt and interrupt mask registers define the group 0 interrupt status bits. The bits in this register can be cleared to 0 by writing a a 1 to the bit. Unless otherwise specified the bits in this register are cleared to 0 on a power–up or software reset. With the exception of bit2, the bits in this register can be placed in a special test mode where the software can directly write to and/or read this register. This is done by setting the REGRW bit in the diagnostic test register (DIAG @ Addr 30h) to 1. The Interrupt Register is at 10h and the interrupt mask register is at 14h. All the bits in the Interrupt Mask register are cleared to 0 on power up. A specific interrupt can be masked off when the corresponding bit in the Interrupt Masks register is 0.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00			
01	IGRP1	R	When set to 1, one or more status bits in the extended interrupt status register @ (addr 14h) are set to 1.
02	IGRP0	R/W	When set to 1, one or more interrupt status bits in this register are set to 1.
03	PHYINT	R/W	Phy interrupt. When set to 1, the phy has signaled an interrupt through the phy interface.
04	PHYREGRX	R/W	Phy register data received. When set to 1 a register value has been transferred to the phy access register (@ offset 34h) from the phy interface.
05	PHYBUSRST	R/W	Phhy bus reset. When set to 1, the phy has entered the 1394 bus reset state.
06	SELFIDERR	R/W	Self ID error. A self ID quadlet/packet with errors has been received.
07	TXRDY	R/W	Transmitter ready. When this bit is set to 1, the link transmitter is IDLE and ready to start transmitting.
08	ACRRXDTA	R/W	Async packet received. When set to a 1, the link receiver has confirmed asynchronous data.
09	CMDRST	R/W	Command reset received. When this bit is set to 1, the receiver has been sent a quadlet request addressed to the Reset_Start CSR register.
10	CSADNE	R/W	Async control FIFO ack received. When this bit is set to 1, an ack has been received for a packet that was transmitted from the ASYNC control transmit FIFO.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
11	IRRXDTA	R/W	ISO packet received. When set to a 1, the link receiver has confirmed isochronous data.
12	ABDACKRX	R/W	Async Bulky FIFO ack received. When this bit is set to 1, an ack has been received for a packet that was transmitted from the ASYNC Bulky transmit FIFO.
13	ITSTK	R/W	Iso Transmit FIFO stuck. When this bit is set to a 1, the link transmitter has detected invalid data at the iso transmit-FIFO interface. To recover from this error, flush Bulky ISO transmit to recover .
14	ATSTK	R/W	ASYNC Transmit FIFO stuck. When this bit is set to a 1, the link transmitter has detected invalid data at the ASYNC transmit-FIFO interface. When this condition occurs Flush the Bulky ASYNC transmit FIFO and the ASYNC control transmit FIFO.
15	Not Used		
16	SNTRJ	R/W	Busy acknowledge sent by link receiver. When this bit is set to 1, the link receiver was forced to busy off the incoming packet addressed to this node because the selected receiving FIFO did not have enough space available for storing it.
17	HDRERR	R/W	Header error detected. This bit is set to a 1 when the receiver detects a CRC error on a packet that may have been addressed to this node.
18	TXTCERR	R/W	Transmit Tcode error. When this bit is set to 1, the link transmitter detected an invalid tcode in the packet header at the transmit-FIFO interface. To recover from this error flush The Bulky ASYNC transmit FIFO and the ASYNC control transmit FIFO.
19	PACACKR	R/W	ASYNC Transmit control FIFO ack received. When this bit is set to a 1, an ack for a packet transmitted from the ASYNC transmit control FIFO has been received.
20	PBDACKR	R/W	ASYNC bulky data FIFO ack received. When this bit is set to a 1, an ack for a packet transmitted from the ASYNC bulky transmit FIFO has been received.
21	Not Used		
22	CYCSEC	R/W	Cycle seconds. When set to to a 1, the cycle seconds field in the cycle timer register has incremented. This occurs approximately every second when the cycle timer is enabled.
23	CYCSTART	R/W	Cycle started. When set to a 1, the link transmitter has sent or the link receiver has received a cycle start packet.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
24	CYCDONE	R/W	Cycle done. When set to a 1, a sub action gap has been detected on the bus after the transmission or reception of a cycle start packet and any isochronous data packets that were transmitted or received. CYCDONE indicates that the isochronous bus period is over.
25	CYCPEND	R/W	Cycle pending. When set to a 1, the cycle timer offset is set to 0 (rolled over reset) and remains set until the isochronous cycle is over.
26	CYCLOST	R/W	Cycle lost. When set to a 1, the cycle timer has rolled over twice with out the reception of a cycle start packet. This occurs only when this node is not the cycle master.
27	CYCARBFL	R/W	Cycle arbitration failed. When set to a 1, the priority transmit request to send the cycle start packet failed to win bus arbitration.
28	ARBRSTGAP	R/W	Arbitration reset gap. When set to a 1, the link has detected that a arbitration reset gap has opened up on the 1394 bus.
29	SUBACTGAP	R/W	Sub action gap. When set to a 1, the link has detected that a sub action gap has opened up on the bus.
30	Not Used		
31	ISOARBFL	R/W	Isochronous arbitration failed. When set to a 1, the isochronous transmit request to send an isochronous packet failed to win bus arbitration.

3.7 Extended Interrupt Register/Extended Interrupt Mask Register (EIR @ Addr 18h/1Ch)

The Extended Interrupt register and the Extended Interrupt Mask register define the group 1 interrupt status bits. With the exception of bit 2, the bits in this register can be cleared to 0 by writing a a 1 to the bit. Unless otherwise specified the bits in this register are cleared to 0 on a power-up or software reset. With the exception of bit1, the bits defined in this register can be placed in a special test mode where the software can directly write to and/or read this register. This is done by setting the REGRW bit in the diagnostic test register (DIAG @ Addr 30h) to 1. The Extended Interrupt register is at 18h and the Extended Interrupt Mask register is at 1Ch. All bits in the Extended Interrupt Mask register are cleared to 0 on power up. A specific interrupt can be masked off when the corresponding bit in the Extended Interrupt Mask register is cleared to 0.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	Not Used		
01	IGRP0	R	This bit is set to 1 whenever 1 or more interrupt status bits from group 0 is set to 1. The group 0 interrupt status bits are located at address offset 10h.
02	IGRP1	R	When set to 1, one or more interrupt status bits in this register are set to 1.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
03	ARAV	R/W	When set to 1, a complete async packet has been received into the async bulky receive FIFO and the packet's header information has been copied into the async receive packet header registers.
04	IRAV	R/W	When set to 1, a complete ISO packet has been received into the ISO bulky receive FIFO and the packet's header information has been copied into the ISO receive packet header register.
05	MRAV	R/W	When set to 1, a complete MPEG packet has been received into the MPEG bulky receive FIFO and the packet's header information has been copied into the MPEG receive packet header registers.
06	DRAV	R/W	When set to 1, a complete DSS packet has been received into the DSS bulky receive FIFO and the packet's header information has been copied into the DSS receive packet header registers.
07	MRELTIM	R/W	When set to 1, the cycletimer has reached the value of the MPEG release time and an MCELL is now being released to the selected interface (bulky data interface or microprocessor interface)
08	DRELTIM	R/W	When set to 1, the cycletimer has reached the value of the DSS release time and an DSS cell is now being released to the selected interface (bulky data interface or microprocessor interface)
09	DHDRLD	R/W	When set to 1, the 10 byte DSS header has been loaded from the DTX registers in X130 mode into the MPEG/DSS transmit FIFO and the registers can now be updated with new values.
10	MPUERR	R/W	When set to 1, the microprocessor has attempted an illegal access to the FIFO. The MPU error code in the BDFMISC register located @ offset F8h bits 1 thru 4, will contain the reason for the error.
11	INVWROP	R/W	When set to 1, the application software has attempted an invalid write operation thru the microprocessor interface.
12	ARFRABRT	R/W	When set to 1, the receive packet routing control has detected and purged a partial packet from the ASYNC bulky receive FIFO
13	CYCTMOUT	R/W	When set to 1, the microprocessor interface has detected a timeout (17 BClk cycles reached) during TMS320AV7000 SIMBA handshake mode.
14	IRFABORT	R/W	When set to 1, receive packet routing control has detected and purged a partial ISO packet from the Bulky ISO receive FIFO.
15			
16	MRFABORT	R/W	When set to 1, receive packet routing control has detected and purged a partial MPEG packet from the Bulky MPEG receive FIFO.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
17	ACRFPRDY	R/W	When set to 1, the receive packet routing control has confirmed an entire packet into the ASYNC control receive FIFO.
18	ACRFPABRT	R/W	When set to 1, the receive packet routing control has detected and purged a partial packet from the ASYNC control receive FIFO.
19	BRFPRDY	R/W	When set to 1, the receive packet routing control has confirmed an entire packet into the BROADCAST control receive FIFO.
20	BRFPABRT	R/W	When set to 1, the receive packet routing control has detected and purged a partial packet from the BROADCAST control receive FIFO.
21	SIDPRDY	R/W	When set to 1, the receive packet routing control has detected the end of the self–ID period and has confirmed the entire set of set ID packets into the selected receive FIFO.
22	SIDPABRT	R/W	When set to 1, the receive packet routing control has detected and purged a partial accumulation of self ID packets from the selected receive FIFO. (Async bulky receive FIFO or BROADCAST control receive FIFO).
23	TSAGED	R/W	When set to 1, the MPEG/DSS packet that is waiting to be transmitted has aged, and has been flushed from the MPEG/DSS transmit FIFO.
24	MPUTMOUT	R/W	When set to 1, the microprocessor interface tried to access a FIFO resource that was unable to respond due to a higher transfer already in progress.
25	ISOGOERR	R/W	When set to 1, the packetizer has detected a premature iso go event.
26	MDDBCERR	R/W	When set to 1, the packetizer has detected a data block continuity error (DBC).
27	MCFLSHERR	R/W	When set to 1, the packetizer has flushed an MPEG/DSS cell from the MPEG/DSS transmit FIFO.
28	BFFLSHERR	R/W	When set to 1, the packetizer has flush the entire contents of the MPEG/DSS FIFO.
29	SBACOMP	R/W	When set to 1, the packetizer has successfully complete transmitting a packet from the bulky ASYNC transmit FIFO.
30	BFAFLERR	R/W	When set to a 1, the packet has failed to transmit an ASYNC packet from the bulky ASYNC transmit FIFO.
31	DBCCRXERR	R/W	When set to 1, the receive packet routing control has detected an error in the MPEG/DSS DBC count of the MPEG/DSS packet currently being received.

3.8 Isochronous Receive Comparators Register 0 (IRPR0 @ Addr 20h)

This register defines the tag and channel number values used by ISO receive packet comparators 0 thru 3 to determine if an incoming ISO packet is to be accepted or rejected. The comparator enable bits IRP0EN – IRP3EN(LCTRL register @addr Ch) and match on tag enable bits MONT0 – MONT3 (RMISC register @ addr 148h) are used in programming the filtering behavior of the comparators based on the following table. Unless otherwise specified the bits in this this register are cleared to 0 on power-up or software initiated reset.

IRPxEN†	MONTx†	COMPARE FUNCTION
0	0	Comparator x is disable
1	0	Match IRPORTx expected value to channel number of incoming ISO packet
0	1	Comparator disabled
1	1	Match IRPORTx and TAGx expected values to channel number and tag field of incoming ISO packet

† x = 1, 2, or 3.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 01	TAG0	R/W	MPEG/DSS Port 0 Tag field receive packet compare value.
02 – 07	IRPORT0	R/W	MPEG/DSS Port 0 ISO channel number receive packet compare value.
08 – 09	TAG1	R/W	ISO Port 1 Tag field receive packet compare value.
10 – 15	IRPORT1	R/W	ISO Port 1 ISO channel number receive packet compare value.
16 – 17	TAG2	R/W	ISO Port 2 Tag field receive packet compare value.
17 –23	IRPORT2	R/W	ISO Port 2 ISO channel number receive packet compare value.
24 – 25	TAG3	R/W	ISO Port 3 Tag field receive packet compare value.
26 – 31	IRPORT3	R/W	ISO Port 3 ISO channel number receive packet compare value.

3.9 Isochronous Receive Comparators Register 1 (IRPR1 @ Addr 24h)

This register defines the tag and channel number values used by ISO receive packet comparators 0 thru 3 to determine if an incoming ISO packet or MPEG/DSS packet is to be accepted or rejected. Comparator number 7 is used for receiving MPEG/DSS ISO packet types. The comparator enable bits IRP4EN – IRP7EN (LCTRL register @addr Ch) and match on tag enable bits MONT4 – MONT7 (RMISC register @ addr 148h) are used in programming the filtering behavior of the comparators based on the following table. Unless otherwise specified the bits in this register are cleared to 0 on power–up or software initiated resets.

IRPxEN†	MONTx†	COMPARE FUNCTION
0	0	Comparator x is disable
1	0	Match IRPORTx value to channel number of incoming ISO packet
0	1	Comparator disabled
1	1	Match IRPORTx and TAGx value to channel number and tag field of incoming ISO packet

† x = 4, 5, 6, or 7.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 01	TAG4	R/W	ISO Port 4 Tag field receive packet compare value.
02 – 07	IRPORT4	R/W	ISO Port 4 ISO channel number receive packet compare value
08 – 09	TAG5	R/W	ISO Port 5 Tag field receive packet compare value.
10 – 15	IRPORT5	R/W	ISO Port 5 ISO channel number receive packet compare value
16 – 17	TAG6	R/W	ISO Port 6 Tag field receive packet compare value.
17 –23	IRPORT6	R/W	ISO Port 6 ISO channel number receive packet compare value
24 – 25	TAG7	R/W	ISO Port 7 Tag field receive packet compare value.
26 – 31	IRPORT7	R/W	ISO Port 7 ISO channel number receive packet compare value

3.10 Cycle Timer Register (CLKTIM @ Addr 28h)

The register provides the application software with an read/write access interface to the cycle timer register. This register is comprised of three fields. They are: seconds_count, cycle_number_count and cycle_offset. The operation of the timer is controlled by control bits CYCMSTREN, CYCSRC, CYCTIMEN. These bits are located in the link control register (LCTRL @ Addr 0Ch). Unless other wise specified the cycle timer register is cleared to 0 on power-up or software initiated reset.

Table 3–1. Cycle Timer Program Function

CYCSRC	CYCMSTREN	CYCTIMEN	DESCRIPTION
X	X	0	Cycle timer is disabled from counting
0	0	1	This node is not the cycle master. The Cycle timer is enabled to count from the internal clock source and can be initialized with the cycle_time_data extracted from a cycle start packet that is received by this node.
0	1	1	This node is the cycle master. the cycle timer is enabled to count from the internal clock source.
1	0	1	This node is not the cycle master. The timer is enabled to increment whenever the external signal CYCLEIN is pulsed high for a minimum of 80ns. The Timer can be initialized with the cycle_time_data extracted from a cycle start packet that is received by this node
1	1	1	This node is the cycle master. The timer is enabled to increment whenever the external signal CYCLEIN is pulsed high for a minimum of 80ns.

Table 3–2. Cycle Time Register

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 06	CYCSEC	R/W	Cycle seconds. 1-Hz cycle timer counter
07 – 19	CYCNUMBER	R/W	8000 Hz cycle timer counter
20 – 31	CYCOFFSET	R/W	24.576 Mhz cycle timer counter

3.11 Bus Time Register (BUSTIM @ Addr 2Ch)

This bit map defines the extended bus time counter register. The bus time counter (BUSTIME) is incremented whenever the cycle timer rolls over in all 32 bits. The Extended Cycle timer is enabled to count when the CYCTIMEN bit located in link control register (LCTRL @ Addr 0Ch) is set to 1. Unless otherwise specified the extended cycle time register is cleared to 0 on a power-up or software initiated reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 24	BUSTIME	R/W	Extended bus timer in seconds.
25 – 31	SECSLO	R	the CYCSEC field of the cycle timer register.

3.12 Link Diagnostics Register (DIAG @ Addr 30h)

This register provides the application software with the capability to perform diagnostic testing. Unless otherwise specified this register is cleared to 0 on power-up or software initiated reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	ENSNOOP	R/W	When set to 1, enables the 1394 Link receiver to snoop 1394 bus traffic.
01	Not Used		
02	ISOBAROFFCR	R	The status value of the isolation barrier control state from the core logic. When set to 1, the isolation barrier is off. When set to 0, isolation barrier is on. This bit is set to 1 on power-up or software reset.
03	ISOBAROFF	R/W	When set to 1, isolation barrier function is turned off
04	REGRW	R/W	When set to 1 configures read only registers to function as read/write registers.
05	ADRCLR	R/W	When set to 1 causes the RAM test address generator to initialize to 0. This bit clears its self to 0.
06	CNTLRBIT1	R/W	When set to 1 the MSB of the test data that is being written into the Control FIFO RAM will be set to 1.
07	CNTLRRBITERR	R/W	When this bit is set to 1, the control bit value from the control FIFO RAM does not match the value of CNTLRBIT1.
08	RAMTEST	R/W	When this bit is set to 1 and the REGRW bit is set to 1, the ram used in the control FIFO can be directly addressed and tested with the FIFO control logic disabled.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
09 – 12	STAT3MUXSEL	R/W	STAT3 output internal signal mux select lines.
			Internal Signal Selected
			BDIBusyOut
			TxBndryLink
			TxWrLink
			TimeStampLink
			TxAbort
			TxAFIFOBsy
			TxIFIFOBsy
			TxMFIFOBsy
			RxAck
			BDIStk
			BDOStk
			TxMPEG
			TxAsync
			TxIso
			RxD130
			NClk

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
13 – 16	STAT2MUXSEL	R/W	STAT2 output internal signal mux select lines.
			Internal Signal Selected
			BDOAvailOut
			CATAckRcvd
			BATAckRcvd
			MTFRd
			ATFRd
			ITFRd
			ATFEmpty
			ITFEmpty
			BATFEmpty
			BATFRd
			BATRetry
			0
			BITFEmpty
			BITFRd
			MTimeStampValid
			MTxDataRegValid
17 – 20	STAT1MUXSEL	R/W	STAT1 output internal signal mux select lines.
			Internal Signal Selected
			0
			MRFull
			ACRFull
			BRFull
			1
			CycTimSerDat
			DSSHddrLdInt
			MPUErrorInt
			TimeStampLink
			ATFEmpty
			ITFEmpty
			MFlush
			MFLushAll
			CATFEmpty
			ARFull
			IRFull

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
21 – 27	STAT0MUXSEL	R/W	STAT0 output internal signal mux select lines.
			Internal Signal Selected
			PowerOn
			CycleStarted
			CycleDOne
			CyclePending
			ArbGap
			FairGap
			BusReset
			NewCycle
			ATAckRcvd
			CATAckRcvd
			BATAckRcvd
			ARAVInt
			IRAVInt
			MRAVInt
			DRAVInt
			MrelTimeInt
			CycleOut
			DSSHdrLdInt
			MPUErrorInt
			TimeStampLink
			ATFEmpty
			ITFEmpty
			MFLush
			MFLushAll
			CATFEmpty
			ARFull
			ITRFull
			MRFull
			ACRFull
			BRFull
			BDIBusyOut
			BDOAvailOut
			MTFRd
			ATFRd

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
21 – 27 (cont'd.)	STAT0MUXSEL	R/W	ITFRd
			ATFEmpty
			ITFEmpty
			BATFEmpty
			BATRd
			BATRetry
			BITEmpty
			BITRd
			MTimeStampValid
			MTxDataRegValid
			TxBndryLink
			TxWrLink
			TimeStampLink
			TxAbort
			TxAFIFOBsy
			TxIFIFOBsy
			TxMFIFOBsy
			RxAck
			BDIStk
			BDOStk
			TxMPEG
			TxAsync
			TxIso
			RxD130
			CycTimSerDat
			NClk
			0
			1
			RoverTestMuxOut
			FidoTestMuxOut
			PktTestMuxOut
28 – 31	ROVERMUXSEL	R/W	Receive packet routing control mux select lines for selecting internal signals for observation at the STAT0 output pin

3.13 Phy Access Register (PHYAR @ Addr 34h)

This register provides the application software with an interface for accessing the registers in the PHY layer. Unless otherwise specified this register is cleared to 0 on power-up or software initiated reset. The functionality of the register is defined by the Following bit map.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	RDPHYREQ	R/W	Read PHY register request. When this bit is set to a 1, phy register read request will be issued from the address specified PHYREGADR. This bit is cleared after the link has sent the request to the PHY layer.
01	WRPHYREQ	R/W	Write PHY register request. When this bit is set to a 1, a phy register write request will be issued to phy that contains the register address and write data obtained from PHYREGADR and PHYREGWRDATA. This request bit is cleared after the has sent the request to the PHY layer.
02 – 03	Not Used		
04 – 07	PHYREGADR	R/W	Phy register address. This field specifies the address of the PHY register that is read from or written to.
08 – 15	PHYREGWRDATA	R/W	Phy register write data. This field specifies the data that will be written to the PHY register specified by PHYREGADR.
16 – 19	Not Used		
20 – 23	PHYREGADRRCV	R	Phy register address received. These register bits buffer the register address returned by the PHY in response to a PHY register read request. The host processor can write to these bits when the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1.
24 – 31	PHYREGDATARCV	R	Phy register data received. These register bits buffer the data returned by the PHY in response to a PHY register read request. The host processor can write to these bits when the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1.

3.14 Reserved Register (RESERVED @ Addr 38h)

3.15 Reserved Register (RESERVED @ Addr 3ch–40h)

3.16 Reserved Register (RESERVED @ Addr 3Ch)

3.17 Reserved Register (RESERVED @ Addr 40h)

3.18 Asynchronous Control Data Transmit FIFO Status (ACTFS @ Addr 44h)

This register provides the application software with the capability to monitor the occupancy status of the ASYNC control transmit FIFO and to program its size. Unless otherwise specified this register is cleared to 0 on power-up, bus reset and software initiated reset

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	ACTFULL	R	When set to 1, ASYNC control transmit FIFO is full. The host processor can write and read these bits when the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1.
01	ACTALFULL	R	When set to 1, ASYNC control transmit FIFO is almost full. The host processor can write and read these bits when the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1.
02 – 03	Not Used		
04	ACT4AVAIL	R	When set to1, the ASYNC control transmit FIFO has 4 empty locations available for storing data. The host processor can write and read these bits when the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1.
05 – 13	Not Used		
14	ACTALEMPTY	R	When set to 1, the ASYNC control transmit FIFO is almost empty. The host processor can write and read these bits when the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1.
15	ACTEMPTY	R	When set to 1, the ASYNC control transmit FIFO is empty. The host processor can write and read these bits when the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1. This bit is set to 1 On power-up reset, bus reset and software reset.
16	Not Used		
17	ACTCLR	R/W	When set to a 1, the ASYNC control transmit FIFO is flushed. This bit is self clearing.
18 – 24	Not Used		
25 – 31	ACTSIZE	R/W	ASYNC control transmit FIFO size setting in quadlets. On power-up or software reset these bits are set to hex 14 (20 quadlets).

3.19 Bus Reset Data Register (BRD @ Addr 48h)

This register provides the application software with the capability to program the operation of the bus reset controller. Unless otherwise specified this register is cleared to 0 on power-up or software initiated reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 09	BUSNUM	R/W	Bus number. Set to a value which has been determined by the application software. The bus number defaults 3FFh on power-up or software initiated resets.
10 – 15	NODENUM	R/W	Node number. This value can be set by software or automatically set to the node ID value returned in a status response from the PHY, when it transmits its self-ID packet on the 1394 bus. The node number is set to 3Fh when a bus reset status response is received by the link or a power-up/software reset occurs.
16	NRIDV	R	Node count IRM ID valid. This bit is set to a 1 when NODECNT and IRMID are valid.
17	Not Used		
18 – 23	NODECNT	R	The number of nodes in the 1394 network. The node count is set to 1 on bus reset, power-up reset, and software reset.
24	ROOT	R	The root state of the local PHY.
25 – 31	IRMID	R	The ID of the IRM node. The 1RM ID is set to 3Fh on bus reset, power-up reset, and software reset.

3.20 Bus Reset Error Register (BRERR @ Addr 4Ch)

This register provides the application software with error status generated by bus reset controlled when it detects an error condition. The internal state machine vectors of the bus reset control are also provided in this register. Unless otherwise specified this register is cleared to 0 on power-up or software initiated reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	CBRERR	R/W	Clear bus reset controller error. When set to a 1, the BRERRCODE is set to 0000. This bit is self clearing.
01 – 04	BRERRCODE	R	Bus reset controller error code returned 0000 – no error occurred 0001 – last self–id does not have all ports marked as child 0010 – expected phyid != phyid 0011 – 2nd quad of self–ID not inverted from 1st quad 0100 – phyid incremented by two 0101 – phyid incremented any 3 or more 0110 – phyid not equal in packet 0111 – self-ID quads are not inverses of each other. 1000 – seif-ID quad is bad
05 – 15	Not Used		
16 – 17	Reserved		
18 – 19	Not Used		
20 – 22	Reserved		
23 – 31	Not Used		

3.21 Asynchronous Control Data Receive FIFO Status (ACRXS @ Addr 50h)

This register provides the application software with capability to monitor the occupancy status of the ASYNC control and BROADCAST control receive FIFOs an to also set their size. All of the bits that are indicated as read only, can be made read/write by the host processor. This is done by setting the REGRW bit in diagnostic control register (DIAG @ addr 30h) is set to 1.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	ACRFULL	R	When set to 1, the ASYNC control receive FIFO is full. On Bus_reset, Power up reset, and software reset this bit is cleared to 0.
01	BRFFULL	R	When set to 1, the Broadcast control receive FIFO is full. On Bus_reset, Power up reset, and software reset this bit is cleared to 0
02	ACRALFULL	R	When set to 1, the ASYNC control receive FIFO is almost full. On Bus_reset, Power up reset, and software reset this bit is cleared to 0
03	BRFALFULL	R	When set to 1, the Broadcast control receive FIFO is almost full. On Bus_reset, Power up reset, and software reset this bit is cleared to 0.
04 – 10	Not Used		
11	BRFCD	R	State of the control bit for the last data quadlet read from the broadcast receive FIFO. On Bus_reset, Power up reset, and software reset this bit is cleared to 0.
12	ACR4AVAIL	R	When set to 1, the Async control receive FIFO has 4 locations available for storage. On Bus_reset, Power up reset, and software reset this bit is cleared to 0.
13	BRFEMPTY	R	When set to 1, broadcast receive FIFO is empty. On Bus_reset, Power up reset, and software reset this bit is set to 1.
14	ACRALEMPTY	R	When set to 1, Async control receive FIFO is almost empty. On Bus_reset, Power up reset, and software reset this bit is set to 0
15	ACREMPTY	R	When set to 1, the Async control receive FIFO is empty. On Bus_reset, Power up reset, and software reset this bit is set to 1.
16	ACRCD	R	State of the control bit for the last data quadlet read from the async control receive FIFO. On Bus_reset, Power up reset, and software reset this bit is set to 0.
17	ACRCLR	R/W	Control receive FIFO clear. When set to 1, the ASYNC receive control and broadcast receive control FIFOs are flushed. This bit is self clearing and is also cleared on power-up or software reset.
18 – 24	BRFSIZE	R/W	Sets the size of the broadcast receive FIFO in quadlets. On power-up or software reset these bit are set to hex 15 (approximately 1 quadlet).
25 – 31	ACRSIZE	R/W	Sets the size of the ASYNC receive FIFO in quadlets. On power-up or software reset these bit are set to hex 15 (21 quadlets).

3.22 Reserved Register (RESERVED @ Addr 54h)

3.23 Reserved Register (RESERVED @ Addr 55h–7Fh)

3.24 Asynchronous Control Data Transmit FIFO First (ACTXF @ Addr 80h)

This write only port provides application software with the capability to write the first quadlet of a packet to the ASYNC control transmit FIFO where it is marked in the FIFO as the first quadlet of the packet.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ACTXF	W	ASYNC control transmit first

3.25 Asynchronous Control Data Transmit FIFO Continue

(ACTXC @ Addr 84h)

This write only port provides application software with the capability to write the remaining quadlets of a packet except the last quadlet, to the ASYNC control transmit FIFO.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ACTXC	W	ASYNC control transmit and continue

3.26 Asynchronous Control Data Transmit FIFO First & Update

(ACTXFU @ Addr 88h)

This write only port provides application software with the capability to write a quadlet to the ASYNC control transmit FIFO and have it confirmed for transmission.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ACTXFU	W	ASYNC control transmit first and update

Data written to this address goes to the ACTX FIFO and is confirmed for transmission.

3.27 Asynchronous Control Data Transmit FIFO Continue & Update

(ACTXCU @ Addr 8ch)

This write only port provides application software with the capability to write the last quadlet of a packet to the ASYNC control transmit FIFO and have the entire packet confirmed for transmission.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ACTXCU	W	ASYNC control transmit continue and update

3.28 Reserved Register (RESERVED @ Addr 90h–BCh)

3.29 Asynchronous Control Data Receive FIFO (ACRX @ Addr C0h)

This register port allows read accesses to the ACRX FIFO. If more than one quadlet is in this FIFO, each read outputs the next quadlet from this FIFO. If the FIFO is empty the last valid value is read. This FIFO is meant for low rate asynchronous control data. However it can also be used for application data which is accessed through the MP/MC interface. This register is cleared to all 0s on power-up, bus_reset, and software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ACRX	R	ASYNC control receive FIFO read port

3.30 Broadcast Write Receive FIFO (BWRX @ Addr 0C4h)

This register port allows accesses to the BWRX FIFO. If more than one quadlet is in this FIFO, each read outputs the next quadlet from this FIFO. If the FIFO is empty the last valid value is read. This FIFO is meant

for low rate asynchronous control data. However it can also be used for application data which is accessed through the MP/MC interface. This register is cleared to all 0s on power-up, bus_reset, and software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BWRX	R	Broadcast receive FIFO read port

3.31 Reserved Register (RESERVED @ Addr C8h)

3.32 Reserved Register (RESERVED @ Addr CCh)

3.33 Reserved Register (RESERVED @ addr D0h)

3.34 Reserved Register (RESERVED @ addr D4h)

3.35 Bulky Data Interface Control (BIF @ Addr D8h)

This register provides the application software with the capability to program and control the functionality of the bulky data interface. Unless otherwise specified the bits in this register are cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 07	Not Used		
08	LNGRDREG	R/W	If BDIMODE = 010 this bit causes the BDOAVAIL signal to remain active through the entire packet.
09	BMLECTRL	R/W	MPEG little endian control. When set to 1, causes MPEG interface to operate in little endian format.
10	BILECTRL	R/W	ISO little endian control. When set to 1, causes ISO interface to operate in little endian format.
11	BALECTRL	R/W	ASYNC little endian control. When set to 1, causes ASYNC interface to operate in little endian format.
12	AHBDIDSY	R/W	Active high control for BDIBUSY pin. When set to 1 causes signal to be active high. This bit is set to 1 on power-up or software reset.
13	AHAVAIL	R/W	Active high control for BDAVAIL pin. When set to 1 causes signal to be active high. This bit is set to 1 on power-up or software reset.
14	AHBDOEN	R/W	Active high control for BDOEN pin. When set to 1 causes signal to be active high. This bit is set to 1 on power-up or software reset.
15	AHBDIEN	R/W	Active high control for BDIEN pin. When set to 1 causes signal to be active high. This bit is set to 1 on power-up or software reset.
16	UNIDIR	R/W	If BDIMODE = 010 this bit causes the interface to be unidirectional.
17	DSSREC	R/W	Active if UNIDIR (bit 16) is set to 1 and BDIMODE = 010. When this bit is set to 1, it causes write functionality to be enabled and read functionality to be disabled.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
18	AHPACEN	R/W	If BDIMODE is set to 010 or 101, then if this bit is set to 1, it will cause the BDIF[2] (packet enable) pin to be active high. This bit is set to 1 on power-up or software reset.
19	AHERROR	R/W	If BDIMODE is set to 010 or 101, then if this bit is set to 1, it will cause the BDIF[1] (packet error) pin to be active high. This bit is set to 1 on power-up or software reset.
20	AHBDIFMT0	R/W	If BDIMODE is set to 101, then if this bit is set to 1, it will cause the BDIF[0] (valid) pin to be active high. This bit is set to 1 on power-up or software reset.
21	Not Used		
22	BDOMODE1	R/W	MSB of the BDOMODE select bits
23	BDOMODE0	R/W	LSB of the BDOMODE select bits
24	Not Used		
25	BDIMODE2	R/W	MSB of the BDIMODE select bits
26	BDIMODE1	R/W	Middle bit of the BDIMODE select bits
27	BDIMODE0	R/W	LSB of the BDIMODE select bits
28	RCVPAD	R/W	When set to 1, this allows 1394 padding bits through the interface port.
29	BDOINIT	R/W	Self clearing bi. When written to with a 1 causes the BDO logic to reset.
30	BDIINIT	R/W	Self clearing bit. When written to with a 1 causes the BDI logic to reset.
31	BDOTRIS	R/W	When set to 1, causes the BDO data bus to be forced high-impedance state.

3.36 MPEG2 Transmit Timestamp Offset Register (MXTO @ Addr DCh)

This register provides the application software with the capability to program the time stamp offset for a MPEG transmit cell. The hardware adds this offset to a sampled value of the cycle timer to determine the time stamp for the MPEG cell to be transmitted. Unless otherwise specified the bits in this register are cleared to 0 on power–up or software reset. This register is the same register as E0h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	MXTO	R/W	sign extended The 24/31 bit offset value.

3.37 DSS Transmit Timestamp Offset Register (DXT0 @ Addr E0h)

This register provides the application software with the capability to program the time stamp offset for a DSS transmit cell. The hardware adds this offset to a sampled value of the cycle timer to determine the time stamp for the DSS cell to be transmitted. Unless otherwise specified the bits in this register are cleared to 0 on power–up or software reset. This register is the same as DCh.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	DXTO	R/W	sign extended The 24/31 bit offset value.

3.38 MPEG2 Receive Timestamp Offset (MRTO @ Addr E4h)

This register provides the application software with the capability to program the time stamp offset for a MPEG receive cell. The hardware adds this offset to the time stamp of the received MPEG cell to determine

the time to release the cell to the application. Unless otherwise specified the bits in this register are cleared to 0 on power-up or software reset. This register is the same as E8h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	MRTO	R/W	The sign extended 24/31 bit offset value.

3.39 DSS Receive Timestamp Offset Register (DRT0 @ Addr E8h)

This register provides the application software with the capability to program the time stamp offset for a DSS receive cell. The hardware adds this offset to the time stamp of a received DSS cell to determine the release time of the cell to the application. Unless otherwise specified the bits in this register are cleared to 0 on power-up or software reset. This register is the same as E4h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	DRTO	R/W	The sign extended 24/31 bit offset value.

3.40 Asynchronous/Isochronous Application Data Control Register (AICR @ Addr ECh)

This register provides the application software with the capability to program and control the operational behavior and data path control for the ASYNC and ISO transmi and receive FIFOs. Unless otherwise specified all bits in the register are cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	IRENABLE	R/W	Iso receive enable. When set to 1, bulky ISO receive FIFO is enabled to receive data.
01	ITENABLE	R/W	Iso transmit enable. When set to 1, bulky ISO transmit FIFO is enabled to transmit data.
02	ARENABLE	R/W	ASYNC receive enable. When set to 1, ASYNC receive FIFO is enabled to receive data.
03	ATENABLE	R/W	ASYNC transmit enable. When set to 1, bulky ASYNC transmit FIFO is enabled to transmit data. This bit is cleared when 1394 bus reset occurs.
04 – 14	Not Used		
15	ISNOOP	R/W	Iso snoop. When set to 1, all incoming iso traffic will be snooped and stored to the bulky ISO receive FIFO.
16	IHIM	R/W	Iso header insert mode enable. When set to 1, automatic header insertion and packetization of ISO data from the ISO transmit FIFO is enabled. In this mode the hardware expects the application to load the ISO transmit FIFO with pure data that contains no header. When this bit is set to 0, the hardware will expect the ISO transmit FIFO to contain completely formatted 1394 ISO packets.
17	IPAUSE	R/W	Iso pause. When set to 1 pause the transfer of the ISO receive packet after the ISO header register is updated. When set to 0 continue transfer of the ISO receive packet after the ISO header register is updated.
18	IRSP	R/W	When set to 1, automatically set the IPAUSE bit after an ISO packet is delivered.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
19	IRHS	R/W	Iso header strip mode enable. When set to 1, the ISO header is stripped from the packet and only data payload is delivered to the application. The ISO header is copied to the register
20	BDIRE	R/W	Bulky data ISO receive FIFO data destination select. When set to 0: The MP/MC has access to the bulky data receive FIFO. Received ISO packets are not transferred to the application thru the BDIF. When set to 1: Received ISO packets are transferred to the application thru the BDIF. MP/MC read accesses are ignored.
21	BDIXE	R/W	Bulky data ISO transmit FIFO data source select. When set to 0: The MP/MC has write access to the bulky ISO transmit FIFO. Data writes from the BDIF are ignored. When set to 1: The application has write access to the bulky ISO transmit FIFO via the BDIF. MP/MC writes are ignored.
22	IRFLSH	W	Bulky ISO receive FIFO flush. Setting this bit to 1 flushes the ISO receive FIFO. This bit is self clearing
23	IXFLSH	W	Bulky ISO transmit FIFO flush. Setting this bit to a 1 flushes the ISO transmit FIFO. This bit is self clearing.
24	AHIM	R/W	ASYNC header insert mode enable. When set to 1, automatic header insertion and packetization of ASYNC data from the bulky ASYNC transmit FIFO is enabled. In this mode the hardware expects the application to load the ASYNC transmit FIFO with pure data that contains no header. When this bit is set to 0, the hardware will expect the ASYNC transmit FIFO to contain completely formatted 1394 ISO packets.
25	APAUSE	R/W	ASYNC pause. When set to 1: pause the transfer of the ASYNC receive packet after the ASYNC header registers are updated. When set to 0: continue transfer of the ASYNC receive packet after the ASYNC header registers are updated.
26	ARSP	R/W	When set to 1, automatically set the APAUSE bit after an ASYNC packet is delivered.
27	ARHS	R/W	ASYNC header strip mode enbale. When set to 1, the ASYNC header is stripped from the packet and only data payload is delivered to the application. The ASYNC header is copied to the ASYNC header registers

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
28	BDARE	R/W	Bulky data ASYNC receive FIFO data destination select. When set to 0: The MP/MC has access to the bulky data ASYNC receive FIFO. Received ASYNC packets are not transferred to the application thru the BDIF. When set to 1: Received ASYNC packets are transferred to the application thru the BDIF. MP/MC read accesses are ignored.
29	BDAXE	R/W	Bulky data ASYNC transmit FIFO data source select. When set to 0: The MP/MC has write access to the bulky ASYNC transmit FIFO. Data writes from the BDIF are ignored. When set to 1: The application has write access to the bulky ASYNC transmit FIFO via the BDIF. MP/MC writes are ignored.
30	ARFLSH	W	Bulky ASYNC receive FIFO flush. Setting this bit to 1 flushes the ASYNC receive FIFO. This bit is self clearing.
31	AXFLSH	W	Bulky ASYNC transmit FIFO flush. Setting this bit to a 1 flushes the ASYNC transmit FIFO. This bit is self clearing.

3.41 MPEG2 Formatter Control Register (MCR @ Addr F0h)

This register provides the application software with the capability to program and control the operational behavior and data path selection for the MPEG transmit and receive FIFOs. Unless otherwise specified all bits in the register are cleared to 0 on power-up or software reset. This register is the same register as F4h

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	MREN	R/W	MPEG receive enable. When set to 1 the bulky mpeg receive FIFO is enabled to receive mpeg packets.
01	MTEN	R/W	MPEG transmit enable. When set to 1 the bulky MPEG transmit FIFO is enable for transmitting packets.
02 – 03	Not Used		
04	MTXERMODE	R/W	When set to 1, DTX0 register bit = BDIF DSSTXERROR signal.
05	MRXERMODE	R/W	When set to 1, BDIF DSSRXERROR signal = bit 16 of register DSR0
06	MXAGE	R/W	MPEG transmit aging enabled. When set to 1, MPEG transmit aging is enabled.
07	MRAGE	R/W	MPEG receive aging enabled. When set to 1, MPEG receive aging is enabled.
08 – 12	Not Used		
13 – 15	MXC	R/W	Mpeg transmit class 000 – transmit source packet in 8 1/8 cell increments 001 – transmit source packet in 4 1/4 cell increments 010 – transmit source packet in 2 1/2 cell increments 011 – transmit 1 cell in source packet 100 – transmit 1 or 2 cells in source packet 101 – transmit 1 or 2 or 3 cells in source packet 110 – transmit 1 or 2 or 3 or 4 cells in source packet 111 – transmit 1 or 2 or 3 or 4 or 5 cells in source packet
16	MRHS	R/W	MPEG header strip enable. When set to 1 the ISO, CIP0, and CIP1 headers and trailer quadlet are stripped from the mpeg receive packet and copied into buffer registers. The remaining source packet is transferred to the application.
17	MEXTS	R/W	MPEG extended time stamp enable. When set to 1 a 32 bit time stamp will be used for both transmit and receive. When set to 0 a 25 bit time stamp is used for both transmit and receive.
18 –19	Not Used		
20	MPAUSE	R/W	MPEG receive pause. When set to 1: pause the transfer of the MPEG receive packet after the MPEG header registers are updated. When set to 0: continue transfer of the MPEG receive packet after the MPEG header registers are updated.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
21	MSPM	R/W	When set to 1, automatically set the MPAUSE bit after an MPEG packet is delivered.
22 – 23	Not Used		
24	BDMRE	R/W	Bulky data MPEG receive FIFO data destination select. When set to 0: The MP/MC has access to the bulky data MPEG receive FIFO. Received MPEG packets are not transferred to the application thru the BDIF. When set to 1: Received MPEG packets are transferred to the application thru the BDIF. MP/MC read accesses are ignored.
25	BDMXE	R/W	Bulky data MPEG transmit FIFO data source select. When set to 0: The MP/MC has write access to the bulky MPEG transmit FIFO. Data writes from the BDIF are ignored. When set to 1: The application has write access to the bulky MPEG transmit FIFO via the BDIF. MP/MC writes are ignored.
26	MRFLSH	W	Bulky MPEG receive FIFO flush. Setting this bit to 1 flushes the MPEG receive FIFO. This bit is self clearing.
27	MXFLSH	W	Bulky MPEG transmit FIFO flush. Setting this bit to a 1 flushes the MPEG transmit FIFO. This bit is self clearing.
28	MFEN	R/W	MPEG mode enable. When set to 1 operate in MPEG mode. When set to 0 operate in DSS mode.
29	MTXTSIN	R/W	MPEG time stamp insert enable. When set to 1 the time stamp is automatically inserted on MPEG transmits.
30	MALTCELL	R/W	When set to 1, use the transmit and receive alternate size defined in register BDFMISC.
31	MHIM	R/W	When set to 1 automatically insert the ISO and CIP headers on MPEG transmits.

3.42 DSS Formatter Control Register (DCR @ Addr F4h)

This register provides the application software with the capability to program and control the operational behavior and data path selection for the MPEG transmit and receive FIFOs. Unless otherwise specified all bits in the register are cleared to 0 on power-up or software reset. This register is the same as register F0h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	DREN	R/W	DSS receive enable. When set to 1 the bulky DSS receive FIFO is enabled to receive DSS packets.
01	DTEN	R/W	DSS transmit enable. When set to 1 the bulky DSS transmit FIFO is enable for transmitting packets.
02 – 03	Not Used		
04	DTXERMODE	R/W	When set to 1, DTX0 register bit = BDIF DSSTXERROR signal.
05	DRXERMODE	R/W	When set to 1, BDIF DSSRXERROR signal = bit 16 of register DSR0
06	DXAGE	R/W	DSS transmit aging enabled. When set to 1, DSS transmit aging is enabled.
07	DRAGE	R/W	DSS receive aging enabled. When set to 1, DSS receive aging is enabled.
08 – 12	Not Used		
13 – 15	DXC	R/W	DSS transmit class 001 – transmit source packet in 4 1/4 cell increments 010 – transmit source packet in 2 1/2 cell increments 011 – transmit 1 cell in source packet 100 – transmit 1 or 2 cells in source packet 101 – transmit 1 or 2 or 3 cells in source packet 110 – transmit 1 or 2 or 3 or 4 cells in source packet 111 – transmit 1 or 2 or 3 or 4 or 5 cells in source packet
16	DRHS	R/W	DSS header strip enable. When set to 1 the ISO, CIP0, and CIP headers and trailer quadlet are stripped from the DSS receive packet and copied into buffer registers.
17	DEXTS	R/W	DSS extended time stamp enable. When set to 1 a 32 bit time stamp will be used for both transmit and receive. When set to 0 a 25 bit time stamp is used for both transmit and receive.
18 –19	Not Used		
20	SPAUSE	R/W	DSS receive pause. When set to 1: pause the transfer of the DSS receive packet after the DSS header registers are updated. When set to 0: continue transfer of the DSS receive packet after the DSS header registers are updated.
21	DSPM	R/W	When set to 1, automatically set the MPAUSE bit after an DSS packet is delivered.
22	DSSR30	R/W	When set to 1, receive DSS130 formatted packets
23	DSSX30	R/W	When set to 1, transmit DSS130 formatted packets

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
24	BDDRE	R/W	Bulky data DSS receive FIFO data destination select. When set to 0: The MP/MC has access to the bulky data DSS receive FIFO. Received DSS packets are not transferred to the application thru the BDIF. When set to 1: Received DSS packets are transferred to the application thru the BDIF. MP/MC read accesses are ignored.
25	BDDXE	R/W	Bulky data DSS transmit FIFO data source select. When set to 0: The MP/MC has write access to the bulky DSS transmit FIFO. Data writes from the BDIF are ignored. When set to 1: The application has write access to the bulky DSS transmit FIFO via the BDIF. MP/MC writes are ignored.
26	DRFLSH	W	Bulky DSS receive FIFO flush. Setting this bit to 1 flushes the DSS receive FIFO. This bit is self clearing.
27	DXFLSH	W	Bulky DSS transmit FIFO flush. Setting this bit to a 1 flushes the DSS transmit FIFO. This bit is self clearing.
28	DFEN	R/W	DSS mode enable. When set to 1 operate in MPEG mode. When set to 0 operate in DSS mode.
29	DTXTSIN	R/W	DSS time stamp insert enable. When set to 1 the time stamp is automatically inserted on DSS transmits.
30	DALTCELL	R/W	When set to 1, use the transmit and receive alternate size defined in register BDFMISC
31	DHIM	R/W	When set to 1 automatically insert the ISO and CIP headers on DSS transmits.

3.43 Bulky Data FIFO Miscellaneous Control and Status (BDFMISC @ Addr F8h)

This register provides the application software with the capability to program an alternate cell size for MPEG and DSS cells and to decode the error status when the micro processor performs an illegal push or pop operation.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	RESERVED		
01 – 04	MPUERRCODE	R	0h – Power-up or software reset value 1h – MPU tried to pop an empty ASYNC RX FIFO 2h – MPU tried to pop a paused ASYNC RX FIFO 3h – MPU tried to push a full ASYNC TX FIFO 4h – MPU tried to pop an empty ISO RX FIFO 5h – MPU tried to pop a paued ISO RX FIFO 6h – MPU tried to push a full ISO TX FIFO 7h – MPU tried to pop an empty MPEG RX FIFO 8h – MPU tried to pop a paused MPEG RX FIFO 9h – MPU tried to pop a MPEG RX FIFO before timestamp release had occurred Ah – MPU tired to pop a MPEG RX FIFO while in BDIF mode Bh – MPU tried to push a full MPEG TX FIFO Ch – MPU tried to push a MPEG TX FIFO while in BDIF mode
05 – 06	RESERVED		
07 – 15	TXMCSZ	R/W	Alternate transmit cell size. Cleared to 0 on power–up or software reset.
16 – 22	RESERVED		
23 – 31	RXMCSZ	R/W	Alternate receive cell size. Cleared to 0 on power-up

3.44 SRAM Address (SRAMA @ Addr FCh)

This register interface provides the application software with the capability to load an 11 bit starting address for directly accessing the 8k x 33 SRAM that is used in implementing the bulky data FIFOs. This address will auto increment on every data read or data write from/to port (**SRAMD @ Addr 100h**).

This register is cleared to 0 on a power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 20	Not Used		
21 – 31	SRAMA	R/W	11 bit SRAM starting address where bit 21 is the MSB

3.45 SRAM Data (SRAMD @ Addr 100h)

This register interface provides the application software with the capability to directly read or write data from/to the 8K x 33 Bulky FIFO SRAM. The address of the read or write access is obtained from SRAMA located in register port (**SRAMA @ Addr Fch**).

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	SRAMD	R/W	Read or write data. Bit 00 is the MSB The default value returned on a read is 0.

3.46 Bulky "A" Size register (BASZ @ Addr 104h)

The register provides the application software with the capability to program the size in multiples of 4 quadlets, of the bulky ASYNC transmit and receive FIFOs. This register is cleared to 0 on a power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 05	Not Used		
06 – 15	BATXSIZE	R/W	Bulky ASYNC transmit FIFO size in multiples of 4 quadlets. Bit 06 is MSB.
16 –21	Not Used		
22 – 31	BARXSIZE	R/W	Bulky ASYNC receive FIFO size in multiples of 4 quadlets. Bit 22 is MSB.

3.47 Bulky "A" Avail register (BAAVAL @ Addr 108h)

This read only register provides the application software with the capability to read the occupancy status in quadlets for the bulky ASYNC transmit and receive FIFO's. This register is cleared to 0 on a power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 03	Not Used		
04 – 15	BATXAVAIL	R	Number of empty quadlet locations available in the bulky ASYNC transmit FIFO. Bit 04 is MSB. Value returned on a read performed right after a power-up or software reset is 0.
16 –19	Not Used		
20 – 31	BARXAVAIL	R	Number of data quadlets available in the bulky ASYNC receive FIFO. Bit 20 is MSB. Value returned on a read performed right after a power-up or software reset is 0.

3.48 Asynchronous Application Data Transmit FIFO First and Continue

(BATX @ Addr 10ch)

This write only port provides the application software with the capability to write the quadlets of a ASYNC transmit packet – except the last quadlet – to the Bulky async transmit FIFO.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BATXFC	W	32 bit data quadlet. Bit 00 is MSB

3.49 Asynchronous Application Data Transmit FIFO Last & Send (BATXLS @ Addr 110h)

This write only port provides the application software with the capability to write the last quadlet of a ASYNC transmit packet to the Bulky async transmit FIFO. This last write marks the quadlet as the last one in the packet and confirms the packet for transmission.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BATXLS	W	32 bit data quadlet. Bit 00 is MSB

3.50 Asynchronous Application Data Receive FIFO (BARX @ Addr 114h)

This write only port allows the application software to read data from the bulky ASYNC receive FIFO. If more than one quadlet is in this FIFO, each read outputs the next quadlet from this FIFO. If the FIFO is empty the last valid value is read.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BARX	R	32 bit data. Bit 00 is the MSB

3.51 Asynchronous Application Data Receive Header Register 0 (ARH0 @ Addr 118h)

This read only register allows the application software to read the first header quadlet of a received ASYNC packet header after the bulky receive FIFO control logic has copied the ASYNC header into registers ARH0 to ARH3**.** This register is cleared to 0 on power–up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ARH0	R	First quadlet of ASYNC header. bit 32 is MSB

3.52 Asynchronous Application Data Receive Header Register 1 (ARH1 @ Addr 11ch)

This read only register allows the application software to read the second header quadlet of a received ASYNC packet header after the bulky receive FIFO control logic has copied the ASYNC header into registers ARH0 to ARH3**.** This register is cleared to 0 on power–up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ARH1	R	Second quadlet of ASYNC header. Bit 32 is MSB

3.53 Asynchronous Application Data Receive Header Register 2 (ARH2 @ Addr 120h)

This read only register allows the application software to read the third header quadlet of a received ASYNC packet header after the bulky receive FIFO control logic has copied the ASYNC header into registers ARH0 to ARH3**.** This register is cleared to 0 on power–up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ARH2	R	Third quadlet of ASYNC header. Bit 32 is MSB

3.54 Asynchronous Application Data Receive Header Register 3 (ARH3 @ Addr 124h)

This read only register allows the application software to read the fourth header quadlet of a received ASYNC packet after the bulky receive FIFO control logic has copied the ASYNC header into registers ARH0 to ARH3**.** This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	ARH3	R	Fourth quadlet of ASYNC header. Bit 32 is MSB

3.55 Asynchronous Application Data Receive Trailer (ART @ Addr 128h)

This read only register allows the application software to read the trailer quadlet of a received ASYNC packet after the bulky ASYNC receive FIFO control logic has copied the trailer quadlet to this register**.** This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 13	Not Used		
14 – 15	SPD	R	1394 speed code of received packet 00 – 100 mbps 01 – 200 mbps 10 – Not valid 11 – Not valid
16 – 21	Not Used		
22 – 23	ZEROFILL	R	number of zero fill bytes in the last quadlet of the packet data payload 00 – no zero fill bytes 01 – 1 zero fill bytes 10 – 2 zero fill bytes 11 – 3 zero fill bytes
24 – 27	Not Used		
28 – 31	ACKSENT	R	The 1394 ack that was sent by the link receiver after receiving the packet. 0000 – Reserved 0001 – Ack complete 0010 – Ack pending 0011 – Reserved 0100 – Ack busy_X 0101 – Ack busy_A 0110 – Ack busy_B 0111 – 1100 – reserved 1101 – Ack data error 1110 – Ack type error 1111 – Reserved

3.56 Bulky "I" Size register (BISZ @ Addr 12Ch)

The register provides the application software with the capability to program the size in multiples of 4 quadlets, of the bulky ISO transmit and receive FIFOs. This register is cleared to 0 on a power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 05	Not Used		
06 – 15	BITXSIZE	R/W	bulky ISO transmit FIFO size in multiples of 4 quadlets. Bit 06 is MSB.
16 –21	Not Used		
22 – 31	BIRXSIZE	R/W	bulky ISO receive FIFO size in multiples of 4 quadlets. Bit 22 is MSB.

3.57 Bulky "I" Avail register (BIAVAL @ Addr 130h)

The read only register provides the application software with the capability to read the occupancy status in quadlets for the bulky ISO transmit and receive FIFOs. This register is cleared to 0 on a power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 03	Not Used		
04 – 15	BITXAVAIL	R	Number of empty quadlet locations available in the bulky ISO transmit FIFO. Bit 04 is MSB
16 –19	Not Used		
20 – 31	BIRXAVAIL	R	Number of data quadlets available in the bulky ISO receive FIFO. Bit 20 is MSB

3.58 Iso Transmit First & Continue (BITXFC @ Addr 134h)

This write only port provides the application software with the capability to write the quadlets of an ISO transmit packet – except the last quadlet– to the Bulky ISO transmit FIFO.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BITXFC	W	32 bit data quadlet. Bit 00 is MSB

3.59 Iso Transmit Last & Send (BITXLS @ Addr 138h)

This write only port provides the application software with the capability to write the last quadlet of an ISO transmit packet to the Bulky ISO transmit FIFO. This last write marks the quadlet as the last one in the packet and confirms the packet for transmission.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BITXLS	W	32 bit data quadlet. Bit 00 is MSB

3.60 Isochronous Receive FIFO (BIRX @ Addr 13ch)

This read only port allows the application software access to the Bulky ISO receive FIFO. If more than one quadlet is in this FIFO, each read outputs the next quadlet from this FIFO. If the FIFO is empty the last valid value is read. The value returned on a read immediately after power-up or software reset is 0.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BIRX	R	32 bit data quadlet. Bit 00 is MSB

3.61 Isochronous packed Received Header (IRH @ Addr 140h)

This read only register allows the application software to read the header quadlet of a received ISO packet header after the bulky ISO FIFO control logic has copied the ISO header into register IRH**.** This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	IRH	R	ISO header quadlet. Bit 00 is MSB

3.62 Isochronous Packet received Trailer (IRT @ Addr 144h)

This read only register allows the application software to read the trailer quadlet of a received ISO packet after the bulky ISO receive FIFO control logic has copied the trailer quadlet to this register**.** This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 13	Not Used		
14 – 15	SPD	R	1394 speed code of received packet 00 – 100 mbps 01 – 200 mbps 10 – Not valid 11 – Not valid
16 – 21	Not Used		
22 – 23	ZEROFILL	R	Number of zero fill bytes in the last quadlet of the packet data payload 00 – no zero fill bytes 01 – 1 zero fill bytes 10 – 2 zero fill bytes 11 – 3 zero fill bytes
24 – 27	Not Used		
28 – 31	ACKSENT	R	The 1394 ack that was sent by the link receiver after receiving the packet. 0000 – Reserved 0001 – Ack complete 0010 – Ack pending 0011 – Reserved 0100 – Ack busy_X 0101 – Ack busy_A 0110 – Ack busy_B 0111 – 1100 – reserved 1101 – Ack data error 1110 – Ack type error 1111 – Reserved

3.63 Receive Packet Routing Control Register (RPRC @ Addr 148h)

This register provides the application software with the capability to program and control the operation of the receive packet routing control logic. This register is cleared to 0 on power-up of software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 18	Not Used		
19	DBCCOVER	W	Disable data block continuity checking on receive. When set, data block continuity checking of incoming MPEG/DSS packets by the receive routing control logic is disabled.
20	RIDM0	R/W	Receive FIFO destination select for response packets that are matched by the expected response comparator (PHYSR @ addr 38h) RIDM0 = 0 The expected response packet is routed to bulky ASYNC Receive FIFO RIDM0 = 1 The expected response packet is routed to the ASYNC control received FIFO.
21	SIDM0	R/W	SelfID Receive FIFO destination select. SIDM0 = 0 Route SelfID packets to broadcast receive FIFO. SIDM0 = 1 Route SelfID packets to Bulky ASYNC Receive FIFO.
22	ARDM1	R/W	ASYNC Receive FIFO destination select bits (ACRF = ASYNC Control Receive FIFO BRF = Broadcast Control Receive FIFO BDARF = Bulky Data ASYNC Receive FIFO) ARDM1 = 0, ARDM0 = 0 — All non-broadcast ASYNC packets are routed to the ACRF. All broadcast ASYNC packets are routed to the ACRF. ARDM1 = 0, ARDM0 = 1 — Non-broadcast ROM/register space request ASYNC packets are routed to the ACRF. Broadcast ROM/register space request ASYNC packets are routed to BRF. All other ASYNC packets not meeting the above decode criteria are routed to the BDARF. ARDM1 = 1, ARDM0 = 0 — All ASYNC packets are routed to the BDARF. ARDM1 = 1, ARDM0 = 1 — Non-broadcast ASYNC request packets with addr => 48 bit destination address threshold are routed to the ACRF. Broadcast ASYNC request packets with addr => 48 bit destination address threshold are routed to the BRF. All other ASYNC packet not meeting the above criteria are routed to the BDARF.
23	ARDM0	R/W	

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
24	MONT0	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 0
25	MONT1	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 1
26	MONT2	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 2
27	MONT3	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 3
28	MONT4	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 4
29	MONT5	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 5
30	MONT6	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 6
31	MONT7	R/W	When set, this bit enables match on tag compare for MPEG/DSS ISO receive comparator 7

3.64 Bulky “A” Retry (BARTRY@ Addr 14Ch)

This register provides the application software with the capability to program the operation of the automatic retry control function for packets transmitted from the bulky ASYNC transmit FIFO. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 15	Not Used		
16 – 23	BATXRTRYINT	R/W	Number of Iso Cycle intervals to wait between retrys.
24 – 31	BATXRTRYNUM	R/W	Number of times to retry the ASYNC packet when the receiving node continues to ack the packet with a busy acknowledge.

3.65 Bulky “M” Size register (BMSZ @ Addr 150h)

The register provides the application software with the capability to program the size in multiples of 4 quadlets, of the bulky MPEG transmit and receive FIFO’s. This register is cleared to 0 on a power-up or software reset. This register is the same register as 158h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 05	Not Used		
06 – 15	BMTXSIZE	R/W	Bulky MPEG transmit FIFO size in multiples of 4 quadlets. Bit 06 is MSB.
16 – 21	Not Used		
22 – 31	BMRXSIZE	R/W	Bulky MPEG receive FIFO size in multiples of 4 quadlets. Bit 22 is MSB.

3.66 Bulky “M” Avail register (BMAVAL @ Addr 154h)

The read only register port provides the application software with the capability to read the occupancy status in quadlets for the bulky MPEG transmit and receive FIFOs. This register is cleared to 0 on power–up or software reset. This register is the same register as 15Ch.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 03	Not Used		
04 – 15	BMTXAVAIL	R	Number of empty quadlet locations available in the bulky MPEG transmit FIFO. Bit 04 is MSB
16 – 19	Not Used		
20 – 31	BMRXAVAIL	R	Number of data quadlets available in the bulky ISO receive MPEG. Bit 20 is MSB.

3.67 Bulky “D” Size register (BDSZ @ Addr 158h)

The register provides the application software with the capability to program the size in multiples of 4 quadlets, of the bulky DSS transmit and receive FIFOs. This register is cleared to 0 on a power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 05	Not Used		
06 – 15	BDTXSIZE	W	Bulky DSS transmit FIFO size in multiples of 4 quadlets. Bit 06 is MSB.
16 – 21	Not Used		
22 – 31	BDRXSIZE	W	bulky DSS receive FIFO size in multiples of 4 quadlets. Bit 22 is MSB.

3.68 Bulky “D” Avail register (BDAVAL @ Addr 15ch)

The register port provides the application software with the capability to read the occupancy status in quadlets for the bulky DSS transmit and receive FIFOs. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 03	Not Used		
04 – 15	BDTXAVAIL	R/W	Number of empty quadlet locations available in the bulky DSS transmit FIFO. Bit 04 is MSB
16 – 19	Not Used		
20 – 31	BDRXAVAIL	R/W	Number of data quadlets available in the bulky ISO receive DSS. Bit 20 is MSB

3.69 MPEG2 Transmit FIFO first & continue (BMTXFC @ Addr 160h)

This register provides the application software with the capability to write the quadlets of an MPEG transmit packet – except the last quadlet – to the Bulky MPEG transmit FIFO. This register is the same register as 16Ch.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BMTXFC	R/W	32 bit data quadlet. Bit 00 is MSB

3.70 MPEG Transmit FIFO last & send (BMTXLS @ Addr 164h)

This write only port provides the application software with the capability to write the last quadlet of an MPEG transmit packet to the Bulky MPEG transmit FIFO. This last write marks the quadlet as the last one in the packet and confirms the packet for transmission. This register is the same register as 178h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BMTXLS	W	last 32 bit data quadlet. Bit 00 is MSB

3.71 MPEG Formatted Packet Receive FIFO (BMRX @ Addr 168h)

This read only register port allows the application software access to the Bulky MPEG receive FIFO. If more than one quadlet is in this FIFO, each read outputs the next quadlet from this FIFO. If the FIFO is empty the last valid value is read. This register is cleared to 0 on power-up or software reset. This register is the same register as 174h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BMRX	R	32 bit data out. Bit 00 is MSB

3.72 DSS Transmit FIFO first & continue (BDTXFC @ Addr 16ch)

This register provides the application software with the capability to write the quadlets of an DSS transmit packet – except the last quadlet – to the Bulky DSS transmit FIFO.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BDTXFC	R/W	32 bit data quadlet. Bit 00 is MSB

3.73 DSS Transmit FIFO last & send (BDTXLS @ Addr 170h)

This write only port provides the application software with the capability to write the last quadlet of an DSS transmit packet to the Bulky DSS transmit FIFO. This last write marks the quadlet as the last one in the packet and confirms the packet for transmission.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BDTXLS	W	Last 32 bit data quadlet. Bit 00 is MSB

3.74 DSS Formatted Packet Receive FIFO (BDRX @ Addr 174h)

This read only register port allows the application software access to the Bulky DSS receive FIFO. If more than one quadlet is in this FIFO, each read outputs the next quadlet from this FIFO. If the FIFO is empty the last valid value is read. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BDRX	R	32 bit read data. Bit 00 is MSB

3.75 MPEG2 Receive Header (MRH @ Addr 178h)

This read only register port allows the application software to read the ISO header quadlet of a received MPEG packet after the bulky MPEG FIFO control logic has copied the ISO header into register MRH**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 188h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	MRH	R	1394 ISO Header Quadlet. Bit 00 is MSB

3.76 MPEG2 CIP Receive Header 0 (MCIPR0 @ Addr 17ch)

This read only register port allows the application software to read the CIP0 header quadlet of a received MPEG packet after the bulky MPEG FIFO control logic has copied the CIP0 header into register MCIPR0**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 18Ch

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	0	R	Logic 0
01	0	R	Logic 0
02 – 07	SID	R	Source node ID = variable from 000000 to 111111
08 – 15	DBS	R	Data block size = 00000110
16 – 17	FN	R	Fraction number = 11
18 – 20	QPC	R	Quadlet padding count = 000
21	SPH	R	Source packet header present = 1 Source packet header not present = 0
22 – 23	RES	R	Reserved
24 – 31	DBC	R	Data block continuity counter = variable 0 to 255

3.77 MPEG2 CIP Receive Header 1 (MCIPR1 @ Addr 180h)

This read only register port allows the application software to read the CIP1 header quadlet of a received MPEG packet after the bulky MPEG FIFO control logic has copied the CIP1 header into register MCIPR1**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 290h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	0	R	Logic 1
01	1	R	Logic 0
02 – 07	FMT	R	Format ID = 100000
08 – 31	FDF	R	Format dependent field

3.78 MPEG2 Receive Trailer Register (MRT @ Addr 184h)

This read only register port allows the application software to read the trailer quadlet of a received MPEG packet after the bulky MPEG receive FIFO control logic has copied the trailer quadlet to this register**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 194h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 13	Not Used		
14 – 15	SPD	R	MPEG receive packet speed 00 – 100 mbps 01 – 200 mbps 10 – invalid 11 – invalid
16 – 27	Not Used		
28 – 31	ERRCODE	R	MPEG receive packet error status.

3.79 DSS Formatted Packet Received Header (DRH @ Addr 188h)

This read only register port allows the application software to read the ISO header quadlet of a received DSS packet after the bulky DSS FIFO control logic has copied the ISO header into register DRH**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 178h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 15	DRH	R	DSS receive Packet 1394 ISO Header

3.80 DSS Formatter CIP 0 receive Register (DCIPR0 @ Addr 18ch)

This read only register port allows the application software to read the CIP0 header quadlet of a received DSS packet after the bulky DSS FIFO control logic has copied the CIP0 header into register DCIPR0**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 17Ch.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	0	R	Logic 0
01	0	R	Logic 0
02 – 07	SID	R	Source node ID = variable from 000000 to 111111
08 – 15	DBS	R	Data block size = 00001001
16 – 17	FN	R	Fraction number = 10
18 – 20	QPC	R	Quadlet padding count = 000
21	SPH	R	source packet header present = 1 source packet header not present = 0
22 – 23	RES	R	Reserved
24 – 31	DBC	R	Data block continuity counter = variable 0 to 255

3.81 DSS Formatter CIP 1 receive Register (DCIPR1 @ Addr 190h)

This read only register port allows the application software to read the CIP1 header quadlet of a received DSS packet after the bulky DSS FIFO control logic has copied the CIP1 header into register DCIPR1**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 180h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	0	R	Logic 1
01	1	R	Logic 0
02 – 07	FMT	R	Format ID = 100001
08 – 31	FDF	R	Format depended field. FDF[08] = TSF Time Shift Flag FDF[08] = 0 The stream is not time shifted FDF[08] = 1 The stream is time shifted

3.82 DSS Formatted Packet Received Trailer (DRT @ Addr 194h)

This read only register port allows the application software to read the trailer quadlet of a received DSS packet after the bulky DSS receive FIFO control logic has copied the trailer quadlet to this register**.** This register is cleared to 0 on power-up or software reset. This register is the same register as 184h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 13	Not Used		
14 – 15	SPD	R	DSS receive packet speed 00 – 100 mbps 01 – 200 mbps 10 – invalid 11 – invalid
16 – 27	Not Used		
28 – 31	ERRCODE	R	DSS receive packet error status.

3.83 DSS Receive Cell Header Register 0 (DRX0 @ Addr 198h)

This read only register port allows the application software to read the DSS source packet header bytes 0 – 3 of a received DSS packet after the bulky DSS receive FIFO control logic has copied the bytes to this register**.** This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 07	DSS130HDR_0	R	DSS source packet header byte 0
08 – 15	DSS130HDR_1	R	DSS source packet header byte 1
16 – 23	DSS130HDR_2	R	DSS source packet header byte 2
24 – 31	DSS130HDR_3	R	DSS source packet header byte 3

3.84 DSS Receive Cell Header Register 1 (DRX1 @ Addr 19Ch)

This read only register port allows the application software to read the DSS source packet header bytes 4 – 5 of a received DSS packet after the bulky DSS receive FIFO control logic has copied the bytes to this register**.** This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 07	DSS130HDR_4	R	DSS source packet header byte 4
08 – 15	DSS130HDR_5	R	DSS source packet header byte 5
16 – 23	DSS130HDR_6	R	DSS source packet header byte 6
24 – 31	DSS130HDR_7	R	DSS source packet header byte 7

3.85 DSS Receive Cell Header Register 2 (DRX2 @ Addr 1A0h)

This read only register port allows the application software to read the DSS source packet header bytes 8 – 9 of a received DSS packet after the bulky DSS receive FIFO control logic has copied the bytes to this register**.** This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 07	Not Used		
08 – 15	Not Used		
16 – 23	DSS130HDR_8	R	DSS source packet header byte 8
24 – 31	DSS130HDR_9	R	DSS source packet header byte 9

3.86 DSS Transmit Cell Header Register 0 (DTX0 @ Addr 1A4h)

This register provides the application software with the capability to program bytes 0 – 3 of a 10 byte DSS packet header that will be automatically inserted by the FIFO control logic into the MPEG/DSS FIFO when DSS 130 transmit mode is enabled. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 07	DSS130HDR_0	R/W	DSS source packet header byte 0
08 – 15	DSS130HDR_1	R/W	DSS source packet header byte 1
16 – 23	DSS130HDR_2	R/W	DSS source packet header byte 2
24 – 31	DSS130HDR_3	R/W	DSS source packet header byte 3

3.87 DSS Transmit Cell Header Register 1 (DTX1 @ Addr 1A8h)

This register provides the application software with the capability to program bytes 4 – 7 of a 10 byte DSS packet header that will be automatically inserted by the FIFO control logic into the MPEG/DSS FIFO when DSS 130 transmit mode is enabled. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 07	DSS130HDR_4	R/W	DSS source packet header byte 4
08 – 15	DSS130HDR_5	R/W	DSS source packet header byte 5
16 – 23	DSS130HDR_6	R/W	DSS source packet header byte 6
24 – 31	DSS130HDR_7	R/W	DSS source packet header byte 7

3.88 DSS Transmit Cell Header Register 2 (DTX2 @ Addr 1ACh)

This register provides the application software with the capability to program bytes 8 – 9 of a 10 byte DSS packet header that will be automatically inserted by the FIFO control logic into the MPEG/DSS FIFO when DSS 130 transmit mode is enabled. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 07	Not Used		
08 – 15	Not Used		
16 – 23	DSS130HDR_8	R/W	DSS source packet header byte 8
24 – 31	DSS130HDR_9	R/W	DSS source packet header byte 9

3.89 ASYNC Header 0 for Auto Tx (AHEAD 0) @ Addr 1B0h)

This register provides the application software with the capability to program the the first quadlet of an ASYNC header that will be used during ASYNC transmit auto packetization.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
0	AIncEn	R/W	Auto-A address Increment on Ack not-busy. Increments destination address by the data length. Cleared to 0 on power-up or software reset.
1–13	RESERVED		Always “zero” on read
14 – 31	AHEAD0	R/W	Asynchronous header register 0 used for Auto-A packetization Set to hex 0001_0010 on power-up or software reset.

3.90 ASYNC Header 1 for Auto Tx (AHEAD(1) @ Addr 1B4h)

This register provides the application software with the capability to program the the second quadlet of an ASYNC header that will be used during ASYNC transmit auto packetization.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	AHEAD1	R/W	Asynchronous header register 1 used for Auto-A packetization Set to hex 3FC1_0000 on power-up or software reset

This register provides the application software with the capability to program the the third quadlet of an ASYNC header that will be used during ASYNC transmit auto packetization.

3.91 ASYNC Header 2 for Auto Tx (AHEAD(2) @ Addr 1B8h)

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	AHEAD2	R/W	Asynchronous header register 2 used for Auto-A packetization Set to hex 0000_0000 on power-up or software reset.

3.92 ASYNC Header 3 for Auto Tx (AHEAD(3) @ Addr 1BCh)

This register provides the application software with the capability to program the the third quadlet of an ASYNC header that will be used during ASYNC transmit auto packetization.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	AHEAD3	R/W	Asynchronous header register 3 used for Auto-A packetization Set to hex 0008_0000 on power-up or software reset.

3.93 ISO Header for Auto Tx (IHEAD0 @ Addr 1C0h)

This register provides the application software with the capability to program the the header quadlet of an ISO header that will be used during ISO transmit auto packetization.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	IHEAD0	R/W	Isochronous header register used for Auto-I packetization Set to hex 0010_0010 on power-up or software reset.

3.94 Packetizer Control (PKTCTL @ Addr 1C4h)

This register provides the application software with the capability to configure and control the operation of the packetizer functionality.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	CYCTSEREN	R/W	Cycle Timer Serial output mode. Enabled when one. When enabled, MDAlt register used for Serial Cycle Timer Shift register. Set to 1 on power-up or software reset.
01	TBD0	R/W	Spare
02	MTEST	R/W	MPEG2 Packetizer test mode. Enabled when one. When enabled, sends MPEG2/DSS test packets based on the class that is selected. MPEG2/DSS data is an incrementing count. One MPEG/DSS packet sent per Iso cycle. Cleared to 0 on power-up or software reset.
03	ITEST	R/W	Bulky Iso Packetizer test mode. Enabled when one. When enabled, sends bulky Iso test packets based on the Ihead register. Bulky Iso data is an incrementing count. One Bulky Iso packet sent per Iso cycle. Cleared to 0 on power-up or software reset.
04	ATEST	R/W	Bulky Asynch Packetizer test mode. Enabled when one. When enabled, sends bulky Asynch test packets based on Ahead registers. Bulky Asynch data is an incrementing count. No auto retrys allowed. When in Bulky Asynch test mode, one Asynch packet is sent per “Iso”cycle to prevent continuous Asynch packets. Cleared to 0 on power-up or software reset.
05	TBD1	R/W	Spare
06	IWAITFCYC[0:1]	R/W	IWaitForCyc[0:1]: Bulky Iso enable mode bits. 00: Normal mode per Bulky Iso enables. 01: Always Off 10: Wait mode. Enable Bulky Iso Tx when Mdalt == CycleTimerValue. Once enabled, stays enabled until re-armed with I WaitArm. 11: Normal mode per Iso enables. Cleared to 0 on power-up or software reset.
08	IWAITARM	R/W	Re-arms IWaitForCyc operation. This is a self clearing bit. Cleared to 0 on power-up or software reset.
09	PTSMXACC	R/W	CFR access to Packetizer Test Multiplexer Output selected by PktProbeSel bits. Cleared to 0 on power-up or software reset.
10 – 17	PROBSEL	R/W	Packetizer Test Multiplexer Signal Selector. Selected signal can be routed to STAT pin or read at CFR PktTestMuxOutAccess. Cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
18	MDCTFRRG	R/W	MPEG2/DSS packetizer Control taken from Mdalt when enabled with a one. When enabled: {0000,Mdalt[0:7]} = number of quadlets to transmit. Mdalt[8:23] = data length loaded into header. Mdalt[24:31] = data block increment used. In this mode, the packet transmitted is always exactly per the class. Cleared to 0 on power-up or software reset.
19	FIDOFLEN	R/W	Master Fido Flush Enabled when one. Set to 1 on power-up or software reset.
20	ISOGOFLEN	R/W	Enable flushing of MPEG2 FIFO when the Iso cycle has begun and the Iso state machine is in a non-idle state. Set to 1 on power-up or software reset.
21	FIDOPHSEN	R/W	Enable flushing of MPEG2FIFO when the Packetizer expects a timestamp from Fido but the TimeStampValid signal is false. Set to 1 on power-up or software reset.
22	CFRPKTRST	R/W	CFR reset of the Packetizer State Machines. This is a self clearing bit. Cleared to 0 on power-up or software reset.
23	QPCWEN	R/W	When set to 1, Enable microprocessor writing of Quadlet per “Cell” register Cleared to 0 on power-up or software reset.
24	PRBWEN	R/W	When set to 1, Enable microprocessor writing of PktTestMuxOutAccess register for r/w test. Cleared to 0 on power-up or software reset.
25	FMTWEN	R/W	When set to 1, Enable microprocessor writing of CIP1 Fmt field. Cleared to 0 on power-up or software reset.
26	DBCWEN	R/W	When set to 1, Enable microprocessor writing of CIP0 DBC field. Cleared to 0 on power-up or software reset.
27	SPHWEN	R/W	When set to 1, Enable microprocessor writing of CIP0 SPH field. Cleared to 0 on power-up or software reset.
28	FNWEN	R/W	When set to 1, Enable microprocessor writing of CIP0 Fn field. Cleared to 0 on power-up or software reset.
29	DBSWEN	R/W	When set to 1, Enable microprocessor writing of CIP0 DBS field. Cleared to 0 on power-up or software reset.
30	SLDWEN	R/W	When set to 1, Enable microprocessor writing of CIP0 Sid field. Cleared to 0 on power-up or software reset.
31	LENWEN	R/W	When set to 1, Enable microprocessor writing of MXH DataLength field. Cleared to 0 on power-up or software reset.

3.95 MPEG2 Transmit Header Register (MXH @ Addr 1C8h)

This register provides the application software with the capability to program the the 1394 header quadlet of that will be used during MPEG transmit auto packetization. This register is the same register as 1D4h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 15	length[0:15]	R/W	PacketDataLength in Bytes. **LENWEN @addr 1C4h [bit 31]=1**, Micro must load. **LENWEN=0**, AutoLoaded by packetizer. Unaffected by BusReset. Set to hex 0008 on power-up or software reset.
16 – 17	TAG	R/W	Iso TAG Number. Micro must load. Unaffected by BusReset Set to 01 on power-up or software reset.
18 – 23	chanNum	R/W	Iso Channel Number. Micro must load. Unaffected by BusReset
24 – 25	RESERVED		Logic 0
26 – 27	spd	R/W	Iso Speed to send this packet. Micro must load. Unaffected by BusReset. Cleared to 00 on power-up or software reset.
28 – 31	sy	R/W	Iso Sync Bits. Resets to 0h. Micro must load. Unaffected by BusReset

3.96 MPEG2 CIP Transmit Header 0 (MCIPX0 @ Addr 1CCh)

This register provides the application software with the capability to program the the CIP0 header quadlet of that will be used during MPEG transmit auto packetization. This register is the same register as 1D8h.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	0	R/W	Logic 0
01	0	R/W	Logic 0
02 – 07	SID	R/W	CFRWEn=1, Micro must load. CFRWEn=0, Auto-Updated with all Phy register 0 transfers.
08 – 15	DBS	R/W	CFRWEn=1, Micro must load. CFRWEn=0, Defaults to 6(MPEG)/9(DSS). Unaffected by BusReset
16 – 17	FN	R/W	CFRWEn=1, Micro must load. CFRWEn=0, Defaults to 3(MPEG)/2(DSS). Unaffected by BusReset
18 – 20	QPC	R/W	Micro must load. Unaffected by BusReset
21	SPH	R/W	CFRWEn=1, Micro must load. CFRWEn=0, Auto set to 1 when TS included in the Pkt Unaffected by BusReset
22 – 23	RES	R/W	Logic 0
24 – 31	DBC	R/W	CFRWEn=1, Micro must load. CFRWEn=0, AutoLoaded/AutoIncremented by packetizer. Unaffected by BusReset.

3.97 MPEG2 CIP Transmit Header 1 (MCIPX1 @ Addr 1D0h)

This register provides the application software with the capability to program the the CIP1 header quadlet of that will be used during MPEG transmit auto packetization. This register is the same register as 1DCh.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00	0	R	Logic 1
01	1	R	Logic01
02 – 07	FMT	R	CFRWEn=1, Micro must load. CFRWEn=0, Defaults to 20(MPEG)/21(DSS) Unaffected by BusReset
08 – 31	FDF	R	Micro must load. Unaffected by BusReset

The CIP1 transmit header information for this packet.

3.98 DSS Formatted Isochronous Data Transmit Header (DXH @ Addr 1D4h)

DSS Shadow register. See MXH @ 1C8h.

3.99 DSS Formatter CIP 0 transmit Register (DCIPX0 @ Addr 1D8h)

DSS Shadow register. See MCIPX0 @ 1CCh.

3.100DSS Formatter CIP 1 transmit Register (DCIPX1 @ Addr 1DCh)

DSS Shadow register. See MCIPX1 @ 1D0h.

3.101MDAltCont (MDALT @ Addr 1E0h)

This register provides the application software with the multifunction capability as defined in the functional description. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	MDALTCONT	R/W	Provides: 1. Alternate control of the packetizer when enabled with register PKTCTL bit MDCTFRRG 2. Serial Cycle Timer Shift register when enabled with register PKTCTL bit CYCTSEREN 3. Delayed Bulky Isoch Transmit Enable. When enabled with register PKTCTL bits IWAITFCYC[0:1] Bulky Isoch Transmit begins when the Cycle Timer matches the value held in MDALTCONT.

3.102Micro Control Register (MDCTL @ Addr 1E4)

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 23	Not Used		
24 – 31	QPERCELL	R/W	

3.103Reserved (RSVD @ Addr 1e8h)

3.104Micro Input / Output Control Register (IOCR @ Addr 1ECh)

BIT	BIT NAME		BIT VALUE SETTING MEANING		POWER UP DEFAULT SETTING		
Number	**Symbol**	**Description**	**Value = 1**	**Value = 0**	**TMS320AV7000**	**Mot68000**	**Intel8051**
0	**MCMP8**	Micro bus is 8/16 bit access	Byte Access	Word Access	Word Access		Byte Access
1	**BeCtl**	Big Endian Control	Big Endian†	Little Endian	Big Endian		Little Endian
2	**IntPol**	Interrupt Polarity Control	High True	Low True	Low True		
3	**RdyPushPull**	"RDY" output signal control	Active Push/ Pull	Tri-State	Tri–State		N/A‡
4	**IntPushPull**	"INT" output signal control	Active Push/ Pull	Tri-State	Active Push/Pull	Tri–State	
5	**BlindAccess**	Blind Access Enable/ Disable	Enable Blind Access Mode	Disable Blind Access Mode	Enable Blind Access Mode	Disable Blind Access Mode	Enable Blind Access Mode
6	**DataInvarnt***	Data Invariant Endianess Cntl	Data Invariant	Address Invariant	Data Invariant		
7	**RdyPol**	Rdy output Polarity Control	High True	Low True	Low True		
8 – 31	Not Used. All these bits (8–31) are cleared to 0 on power-up or software reset.						

† When the BeCtl bit is set to "1" (Big Endian), the DataInvarnt bit setting has no effect.

‡ Although there is no RDY line connection in Intel 8051 Mode, reading the IOCR.RdyPushPull will still return value of "0" for this bit.

3.105Blind Access Status Register (BASTAT @ Addr 1F0h)

This register provides the external micro a mean to check whether the current Blind Read/Write Access to the chip is complete. This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 06	0	R	Logic 0
07	BACMP	R	When set to 1 means current Blind Access read/write process (to all address other than 1f0, 1f4 and 1ec) is complete and if read, the data returned is ready in the BAHR (Blind Access Holding Register).
08 – 14	0	R	Logic 0
15	BACMP	R	Mirror bit#7s function
16 – 22	0	R	Logic 0
23	BACMP	R	Mirror bit#7s function
24 – 30	0	R	Logic 0
31	BACMP	R	Mirror bit#7s function

3.106Blind Access Holding Register (BAHR @ Addr 1F4h)

This register holds the quadlet data returned for the last Blind Access read process upon BACMP bit of BASTAT register is set (except read to 1f0, 1f4 and 1ec). This register is cleared to 0 on power-up or software reset.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	BAHR bits	R	BAHR Quadlet Data

3.107Reserved Register (RESERVED @ Addr 1F8h)

3.108Software Reset Register (SRES @ Addr 1FCh)

Any write access to this register will generate a device reset regardless what kind of data is written into. The internal reset pulse has a width of four SClk cycle.

BIT NUMBER	BIT NAME	DIR	FUNCTIONAL DESCRIPTION
00 – 31	SRES	W	

PRODUCT PREVIEW

4 TSB12LV41 Data Formats

The data formats for transmission and reception of data are shown in the following sections. The transmit format describes the expected organization of data presented to the TSB12LV41 at the host-bus interface. The receive formats describe the data format that the TSB12LV41 presents to the host-bus interface.

4.1 Transmit Operation

4.1.1 Transmitting A-packets

“A” control packets are typically sent by the MP/MC using the ACTX FIFO. The Control Fifo Transmit/Receive modes of operation are shown in Figure 4–1. For Tx Header/Data is loaded into the ACTX by the Micro. For Rx Header/Data/Trailer is available in the ACRX.

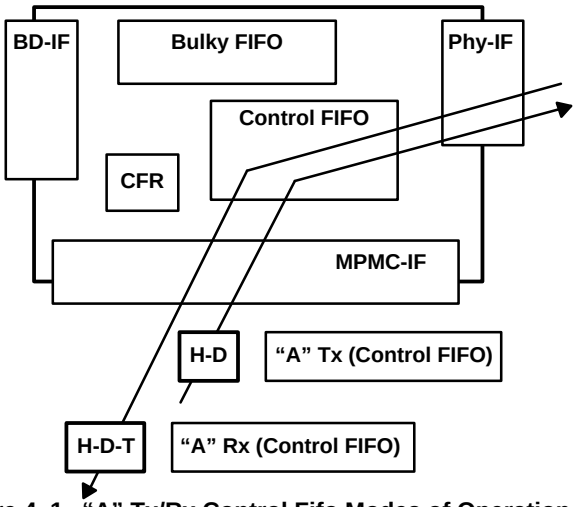


Figure 4–1. “A” Tx/Rx Control Fifo Modes of Operation.

“A” data packets from high speed applications will typically go through the BDIF using the BATX FIFO. The Bulky Fifo “A”/”I” Transmit modes of operation are shown in Figure 4–2. Four modes of operation are supported. Data from BDIF/Micro & Headers from CFR’s or Header/Data from BDIF/Micro & nothing from the CFR’s.

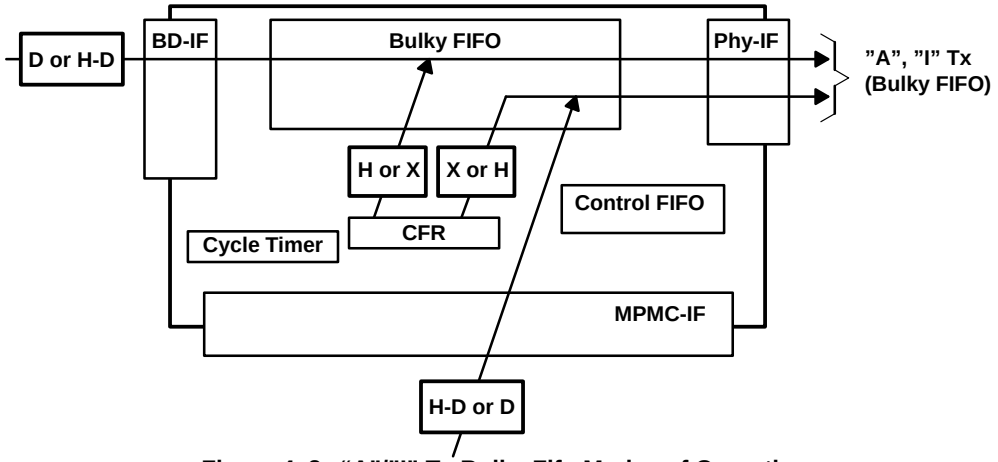


Figure 4–2. “A”/”I” Tx Bulky Fifo Modes of Operation.

4.1.1.1 “A” Control packets

“A” control packets are generated by writing to the ACTXF, ACTXC, ACTXFU and ACTXCU registers which access the ACTX FIFO. Writes to the ACTXF register mark the first quadlet of an “A” packet while writes to the ACTXC register are used for the other quadlets of an “A” packet. Writes to the ATCFFU and ACTXCU register start the transmission of the “A” packet.

The ACTX FIFO can also be used for Asynchronous Data traffic at low data rates.

4.1.1.2 “A” Data Packet Transmit.

The transmission of “A” data packets can be done in four ways.

Sending fully formatted “A” data packets via the BDIF {ATENABLE(1), BDAXE(1), AHIM(0)}.

The BDIF writes data to the BATX FIFO. This data must include all header related bytes with the actual “A” payload.

Sending fully formatted “A” data packets via the MP/MC IF {ATENABLE(1), BDAXE(0), AHIM(0)}.

The Microcontroller writes data to the BATX FIFO. This data must include all header related bytes with the actual “A” payload.

Sending Headerless “A” data packets with the BDIF {ATENABLE(1), BDAXE(1), AHIM(1)}.

The BDIF writes data to the BATX FIFO. This data does not include header related bytes with the actual “A” payload. The desired “A” header quadlets for this mode are loaded into the AHEAD0 – AHEAD3 registers. The “A” packet will be sent when enough data has been received to meet the data length threshold in the AHEADx registers.

Sending Headerless “A” data packets with the MP/MC {ATENABLE(1), BDAXE(0), AHIM(1)}.

The Microcontroller writes data to the BATX FIFO. This data does not include header related bytes with the actual “A” payload. The desired “A” header quadlets for this mode are loaded into the AHEAD0–AHEAD3 registers. The “A” packet will be sent when enough data has been received to meet the data length threshold in the AHEADx registers.

4.1.1.3 General

Packet Flush: The complete BATX FIFO can be flushed by setting the AXFLSH bit in the AICR register.

Packet Retries: Bulky “A” BATX packets may be automatically retried up to 256 times (BATxRetryNum in BARTRY register) in up to 256 Iso Cycle intervals (BATxRetryInt in BARTRY register).

4.1.2 Transmitting I Packets

4.1.2.1 “I” data packet transmit

The transmission of “A” data packets can be done in four ways.

Sending fully formatted “I” data packets via the BDIF {ITENABLE(1), BDIXE(1), IHIM(0)}.

The BDIF writes data to the BITX FIFO. This data must include all header related bytes with the actual “I” payload.

Sending fully formatted “I” data packets via the MP/MC IF {ITENABLE(1), BDIXE(0), IHIM(0)}.

The Microcontroller writes data to the BITX FIFO. This data must include all header related bytes with the actual “I” payload.

Sending Headerless “I” data packets with the BDIF {ITENABLE(1), BDIXE(1), IHIM(1)}.

The BDIF writes data to the BITX FIFO. This data does not include header related bytes with the actual “I” payload. The desired “I” header quadlet for this mode is loaded into the IHEAD register. The “I” packet will be sent when enough data has been received to meet the data length threshold in the IHEAD register.

Sending Headerless “I” data packets with the MP/MC {ITENABLE(1), BDIXE(0), IHIM(1)}.

The Microcontroller writes data to the BITX FIFO. This data does not include header related bytes with the actual “I” payload. The desired “I” header quadlet for this mode is loaded into the IHEAD register. The “I” packet will be sent when enough data has been received to meet the data length threshold in the IHEAD register.

4.1.2.2 General

Packet Flush: The complete BITX FIFO can be flushed by setting the IXFLSH bit in the AICR register.

4.1.3 Transmitting MPEG-2/DSS Formatted Isochronous Packets

The Bulky Fifo “M”/”D” Transmit modes of operation are shown in Figure 4–3. The following modes are supported. Data from BDIF/Micro, TS from CycleTimer & Headers from CFR’s. TS/ Data from BDIF/Micro & Headers from CFR’s. Header/TS/Data from BDIF/Micro.

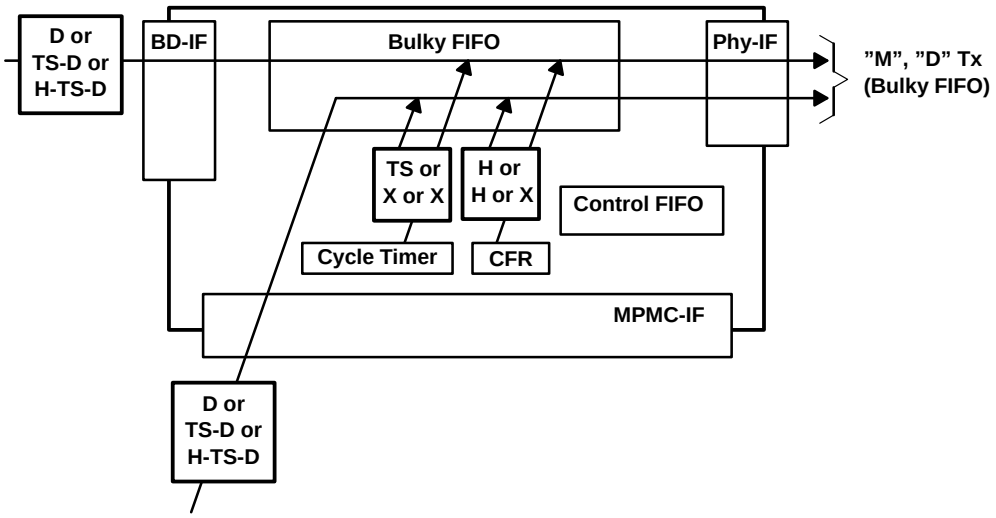


Figure 4–3. Bulky Fifo "M"/"D" Transmit Modes of Operation

For MPEG-2/DSS formatted isochronous packet transmission eight different bandwidth classes are defined. The bandwidth classes define the maximum bandwidth that can be used for an given "M"/"D" channel. On setup the initiator of an "M"/"D" channel with a given peak rate needs to request a higher BW class from the IRM. If this request is guaranteed then an isochronous channel (MPEG-2/DSS) with a BW up to the ADV BW of this class is allocated, and the "M"/"D" traffic can be initiated. The BW classes are selected by the MXC/DXC bits in the MCR/DCR register. These bits are static variables and must not be changed while "M"/"D" traffic is active.

MPEG-2/DSS cells are usually sent to the BDIF, here the single bytes will be packetized to quadlets (32bit). After four bytes are written to the BDIF, the complete quadlet is written to the BMDTX FIFO. The first byte of an "M"/"D" cell is indicated by setting the BDIF lines to first byte of "M"/"D" cell. A internal cyclic counter keeps track of "M"/"D" cell boundaries.

"M"/"D" packet contents are selected as follows:

Table 4–1. M/D Packet Contents

BDMXE/ BDDXE	MHIM/ DHIM	MTXTSIN/ DTXTSIN	TimeStamp from:	Header from:	Data from:
1	1	1	CycleTimer	CFR/Calc	BDIF
1	1	0	BDIF	CFR/Calc	BDIF
1	0	x	BDIF	BDIF	BDIF
0	1	1	CycleTimer	CFR/Calc	MPMC
0	1	0	MPMC	CFR/Calc	MPMC
0	0	x	MPMC	MPMC	MPMC

4.1.3.1 Writes to the MPEG-2/DSS transmit FIFO

If the BDMXE/BDDXE bit (MCR/DCR register) is set, then the BDIF has access to the BMDTX FIFO. An indication of the first byte of an "M"/"D" is given by the BDIF lines. If the BDMXE/BDDXE bit is set low then writes to the BMDTX FIFO go through the MPMC. The accessed address is the indicator what byte/quadlet is written (either first byte of "M"/"D" Cell or regular byte). The MHIM/DHIM bit (MCR/DCR register) selects

if the MPEG-2/DSS header register should be interleaved automatically (MHIM/DHIM=1) or if complete formatted MPEG-2/DSS cells are expected from the BDIF (MHIM/DHIM=0). If MHIM/DHIM=0 the MPEG-2/DSS header calculation is suspended. The MTXTSIN/DTXTSIN bit enables and disables the internal timestamp generation. If set to low a 192 byte MPEG-2 (144 byte for DSS) source packet is expected from the datasource. A counter on the input port of the BMDTX FIFO keeps track of cell boundaries (192 bytes for MPEG & 144 bytes for DSS). This counter is synchronized on each first byte indication and generates internal first byte strobes even when external first byte indicators are missing.

4.1.3.2 MPEG-2 Bandwidth Classes on 1394

Class 0 (0..1.5Mbit/s)

On each isochronous transmission timeslot the MPEG-2 framer checks if 24 valid bytes are available in the BMDTX FIFO; if so, these 24 bytes will be taken as the payload for an MPEG-2 packet and sent over 1394; if not, an empty MPEG-2 packet is sent.

The possible packet sizes are 44bytes (1/8 cell) and 20bytes (for an empty packet)

Class 1 (0..3Mbit/s)

On each isochronous transmission timeslot the MPEG-2 framer checks if 48 valid bytes are available in the M-TX FIFO; if so, these 48 bytes will be taken as the payload for an MPEG-2 packet and sent over 1394; if not, an empty MPEG-2 packet is sent.

The possible packet sizes are 68bytes (2/8 cell) and 20bytes (for an empty packet)

Class 2 (0..6Mbit/s)

On each isochronous transmission timeslot the MPEG-2 framer checks if 96 valid bytes are available in the M-TX FIFO; if so, these 96 bytes will be taken as the payload for an MPEG-2 packet and sent over 1394; if not, an empty MPEG-2 packet is sent.

The possible packet sizes are 116bytes (4/8 cell) and 20bytes (for an empty packet)

Class 3 (0..12Mbit/s)

The MPEG-2 framer checks if a complete M cell is available on an isochronous transmission timeslot. If so this M cell is used as payload for the M packet. If not a empty packet is sent.

The possible packet sizes are 204bytes and 20bytes.

Class 4 (0..24Mbit/s), Class 5 (0..36Mbit/s), Class 6 (0..48Mbit/s), Class 7 (0..60Mbit/s)

Classes 4–7 work like class 3; on each isochronous transmit a check is done how many complete M cells are available to be sent. The available M cells are then taken as the payload for the M packet. If there is no complete cell available then an empty packet is sent.

4.1.3.3 MPEG-2 CIP Header Calculations

static values

nMXH: tag,chanNum, spd, sy

nCIPX0:SID,FN,QPC,SPH

nCIPX1:FMT,FDF

calculated values

nMXH: length

nCIPX0: DBS, DBC

nCIPX1: Length Field

Table 4–2. Initial values for the CIP headers (to be set by SW)

Class	SID	FN	QPC	SPH	DBC	FMT	FDF
	source ID	11	000	1	0...0	100000	0...0
1	source ID	11	000	1	0...0	100000	0...0
2	source ID	11	000	1	0...0	100000	0...0
3	source ID	11	000	1	0...0	100000	0...0
4	source ID	11	000	1	0...0	100000	0...0
5	source ID	11	000	1	0...0	100000	0...0
6	source ID	11	000	1	0...0	100000	0...0
7	source ID	11	000	1	0...0	100000	0...0

(all binary values)

nDBC field calculation is done by adding the DBC inc. value of an M packet to be sent to the current DBC value.

nDBS field calculation is done by deciding what size of “M” packet can be sent over 1394 and interleaving the corresponding value to the link core.

nLength field calculation (in M-formatted I-packet header) is done by deciding what size of “M” packet can be sent over 1394 and interleaving the corresponding value to the link core.

Table 4–3. DBC incremental numbers, DBS value and length values for MPEG-2 packets

M-pck size	20	44	68	116	212	404	596	788	980
DBC inc.val.	0	1	2	4	8	16	24	32	40
DBS val.	6	6	6	6	6	6	6	6	6
length(MXH)	12	36	60	108	204	396	588	780	972

(all decimal numbers)

4.1.3.4 MPEG-2 on 1394 Bandwidth Table

Table 4–4.

Class MXC Value	Max. TSP BW (Mbits/s)	Max SP BW (Mbits/s)	Max 1394 BW (Mbits/s)	Possble M-packet sizes including CIP, M Hdr, and CRC’s
0	1.504	1.536	2.816	20 bytes, 44 bytes
1	3.008	3.072	4.352	20 bytes, 68 bytes
2	6.016	6.144	7.424	20 bytes, 116 bytes
3	12.032	12.288	13.568	20 bytes, 212 bytes
4	24.064	24.576	25.856	20, 212, 404 bytes
5	36.096	36.864	38.144	20, 212, 404, 596 bytes
6	48.128	49.152	50.432	20,212,404,596,788 bytes
7	60.160	61.440	62.720	20,212,404,596,788,980 bytes

TSP BW

Transport stream package bandwidth (based on 188 byte MPEG-2 cells/ BW on ADV layer)

SP BW

Source package bandwidth (based on 192 byte MPEG-2 source cells referenced in some standardization papers.)

1394 BW

Overall BW of 1394 bus on physical medium (includes 4-byte M-packet transmit header, 4-byte M-packet header CRC, 8-byte CIP header, 4-byte timestamp, actual payload and 4-byte payload CRC)

This is the BW which needs to be allocated by the initiator of an MPEG-2 transfer.

4.1.3.5 Simple MPEG-2 transmission over 1394

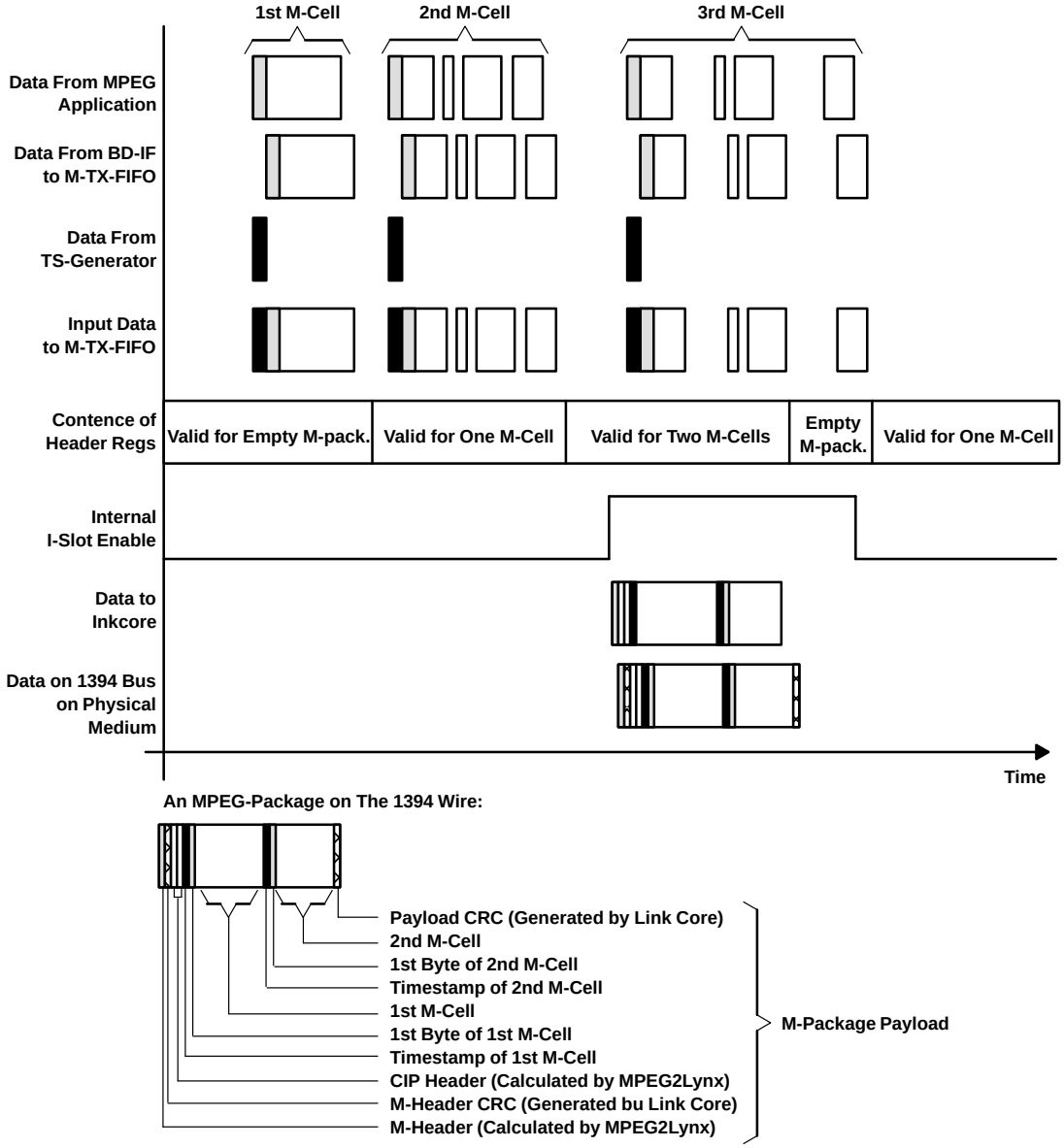


Figure 4–4. Simple MPEG-2 Transmission Over 1394

This diagram shows a simple scenario of a class 5 link (up to 36Mbit/s) as there were just two complete M cells available at the time M packages were to be sent, only two could be sent even if the TX timeslot was reserved for three M cells. The MPEG-2 data can be written to the BDIF in any manner (burst access, bursty access, serial, parallel).

4.1.3.6 DSS Bandwidth Classes on 1394

Class 0 (0..1Mbit/s)

This mode is not supported by the TSB12LV41.

Class 1 (0..2Mbit/s)

On each isochronous transmission timeslot the DSS framer checks if 36 valid bytes are available in the BMDTX FIFO; if so, these 36 bytes will be taken as the payload for an DSS packet and sent over 1394; if not, an empty DSS packet is sent instead. The possible packet sizes are 56bytes (for an quarter cell) and 20bytes (for an empty packet)

Class 2 (0..4Mbit/s)

On each isochronous transmission timeslot the DSS framer checks if 72 valid bytes are available in the BMDTX FIFO; if so, these 72 bytes will be taken as the payload for an DSS packet and sent over 1394; if not, an empty DSS packet is sent instead. The possible packet sizes are 92bytes (2 quarter cell) and 20bytes (for an empty packet)

Class 3 (0..8Mbit/s)

The DSS framer checks if a complete DSS cell is available on a isochronous transmission timeslot. If so this DSS cell is used as payload for the DSS packet. If not an empty packet is sent instead. The possible packet sizes are 164bytes and 20bytes.

Class 4 (0..16Mbit/s), Class 5 (0..24Mbit/s), Class 6 (0..32Mbit/s), Class 7 (0..40Mbit/s)

Classes 4–7 work like class 3; on each isochronous transmit a check is done how many complete DSS cells are available to be sent. The available DSS cells are then taken as the payload for the DSS packet. If there is no complete cell available then an empty packet is sent.

4.1.3.7 DSS packets CIP Header Calculations

static values

nDXH: tag,chanNum, spd, sy

nDCIPX0:SID,FN,QPC,SPH

nDCIPX1:FMT,FDF

calculated values

nDXH: Length

nDCIPX0: DBS, DBC

nDCIPX1: Length

Table 4–5. Initial values for the DCIP headers (to be set by SW)

Class	SID	FN	QPC	SPH	DBC	FMT	FDF
	Not Supported	Not Supported	Not Supported	Not Supported	Not Supported	Not Supported	Not Supported
1	source ID	10	000	1	0...0	100001	x0...0
2	source ID	10	000	1	0...0	100001	x0...0
3	source ID	10	000	1	0...0	100001	x0...0
4	source ID	10	000	1	0...0	100001	x0...0
5	source ID	10	000	1	0...0	100001	x0...0
6	source ID	10	000	1	0...0	100001	x0...0
7	source ID	10	000	1	0...0	100001	x0...0

NOTES: A. (all binary values)
B. x=0 means not time shifted
C. x=1 means the stream is time shifted

nDBC field calculation is done by adding the DBC inc. value of an DSS packet to be sent to the current DBC value.

nDBS field calculation is done by deciding what size of DSS packet can be sent over 1394 and interleaving the corresponding value to the link core.

nLength field calculation (in DSS-formatted I-packet header) is done by deciding what size of DSS packet can be sent over 1394 and interleaving the corresponding value to the link core.

Table 4–6. DBC incremental numbers, DBS value and length values for DSS packets

DSS-pck size	20	38	56	92	164	308	452	596	740
DBC inc.val.	0	n/a	1	2	4	8	12	16	20
DBS val.	9	n/a	9	9	9	9	9	9	9
length(DXH)	12	n/a	48	84	156	300	444	588	732

(all decimal numbers)

4.1.3.8 DSS on 1394 Bandwidth Table

Table 4–7.

Class DXC Value	Max. DSS130 BW (Mbits/s)	Max DSS140 BW (Mbits/s)	Max SP BW (Mbits/s)	Max 1394 BW (Mbits/s)	Possble DSS-packet sizes including DCIP, D Hdr, and CRC's
0	n/a	n/a		n/a	n/a
1	2.08	2.24	2.304	3.584	20 bytes , 56 bytes bytes
2	4.16	4.48	4.608	5.888	20 bytes , 92 bytes
3	8.32	8.96	9.216	10.486	20 bytes , 164 bytes
4	16.64	17.92	18.432	19.712	20, 164, 308 bytes
5	24.96	26.88	27.648	28.928	20, 164, 308, 452 bytes
6	33.28	35.84	36.864	38.144	20, 164, 308, 452, 596 bytes
7	41.60	44.80	46.08	47.360	20, 164, 308, 452, 596, 740 bytes

DSS130 BW

Transport stream package bandwidth (based on 130 byte DSS cells / BW on ADV layer)

DSS140 BW

Transport stream package bandwidth (based on 140 byte DSS cells / BW on ADV layer)

SP BW

Source package bandwidth (based on 144 byte DSS source cells)

1394 BW

Overall BW of 1394 bus on physical medium (includes 4-byte M-packet transmit header, 4-byte DSS-packet header CRC, 8-byte CIP header, 4-byte timestamp, actual payload and 4-byte payload CRC).

This is the BW which needs to be allocated by the initiator of an DSS transfer.

4.1.3.9 Simple DSS transmission over 1394

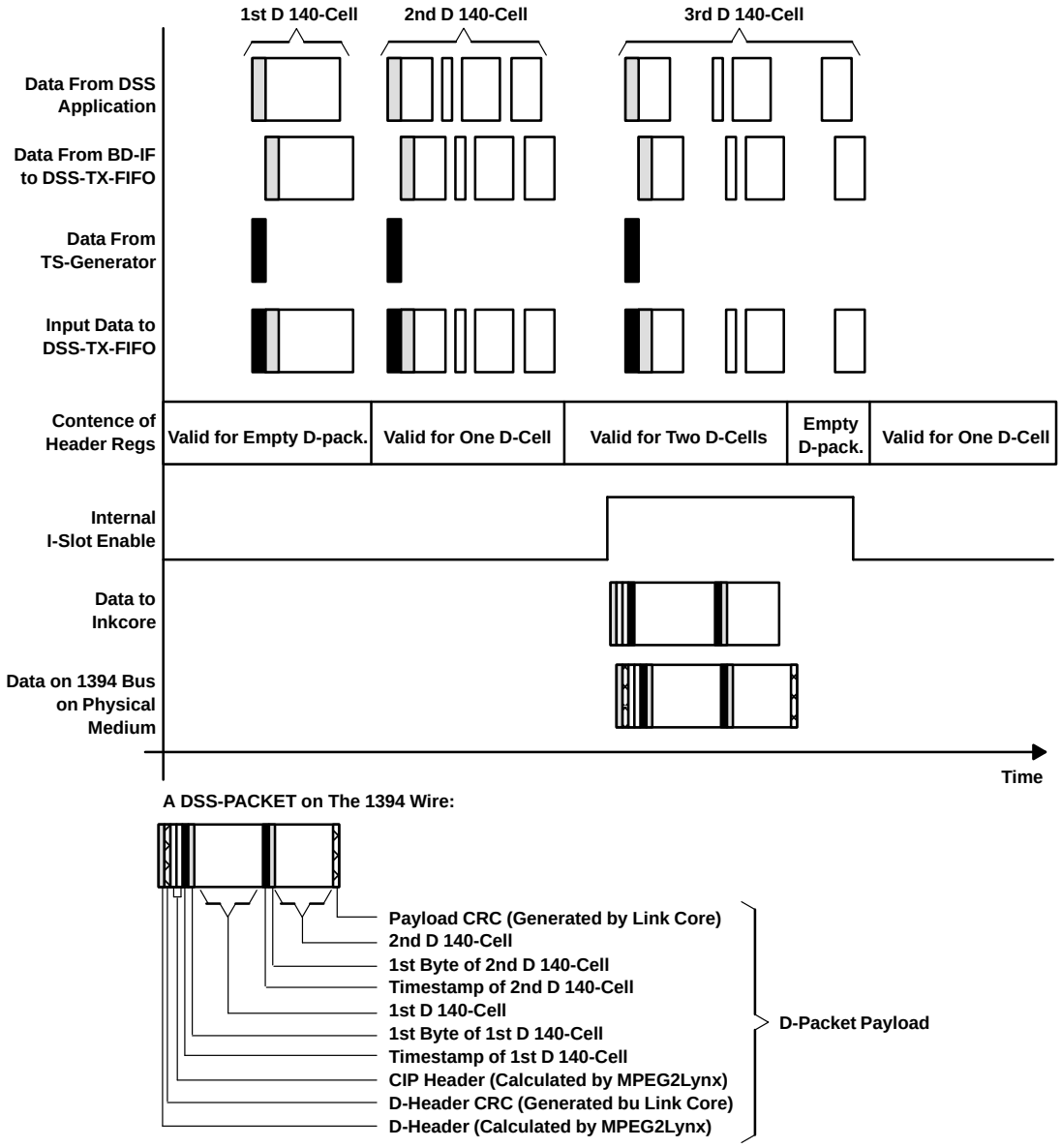


Figure 4–5. Simple DSS Transmission Over 1394

This diagram shows a simple scenario of a class 5 connection (up to 24Mbit/s) as there were just two complete DSS cells available at the time DSS packets can be sent only two could be sent even if there would have been time for three D140 cells. The DSS data can be written to the bulky data IF in any manner (burst access, bursty access, serial, parallel).

4.1.3.10 DSS130 / DSS140 differences

The TSB12LV41 supports the 130byte DSS-cell-format and the 140byte DSS-cell-format. As all DSS-cells need to be converted to 140 byte cells before they can be transmitted only the 130byte cells need to be adapted. If the X130 bit (DCR register) is high the 10 DSS header bytes in the DXX0, DXX1, DXX2 register

will be inserted on transmission. Only 130 bytes are expected on the bulky data interface. The DSS header bytes are inserted as a 10 byte block directly after the source packet header (timestamp quadlet). The insertion of the header bytes occurs directly after the first bit/byte of a DSS cell is sent to the bulky data interface. A couple of cycles later the DXX register can be set with new header values. On receive the DRX register will be always loaded with the DSS header bytes immediately after the DSS cell is to be released to the video application according its timestamp.

If the R130 bit in the DCR register is set only 130byte DSS cells are given out to the bulky data interface.

The conversion from DSS130 to DSS140 cells is done in the byte merger of the bulky data interface. If the MPMC writes and reads DSS cells via the MP/MC interface full DSS140 cells need to generated.

NOTE: DSS130 cells are only supported on the bulky data interface

DSS130 packets are embedded inside the DSS140 structure as follows:

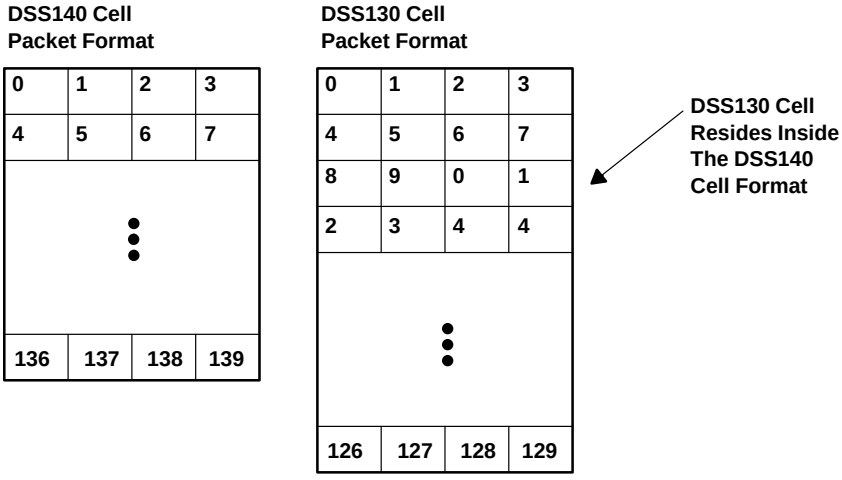


Figure 4–6. DSS130 Packets

4.1.4 MPEG-2/DSS Common Resources

The TSB12LV41 supports DSS and MPEG-2 exclusively (only one format at a time).

For ease of software implementation, the following register pairs are aliased:

nMCR == DCR

nMXH = DXH

nMCIPX0 == DCIPX0

nMCIPX1 == DCIPX1

nMXTO == DXTO

nMRH == DRH

nMCIPR0 == DCIPR0

nMCIPR1 == DCIPR1

nMRT == DRT

nMRTO == DRTO

Separate addresses have been chosen to allow concurrent support for later family members and to simplify software drivers.

The indication for first byte of a cell on the BDIF/BDOF lines are the same for MPEG-2 and DSS cells.

4.2 Receiver Operation

The Bulky FIFO Receive modes of operation are shown in Figure 4–7. The Header/Trailer is copied into CFR's. Either Data or Header/Data/Trailer are passed to the BDIF/Micro.

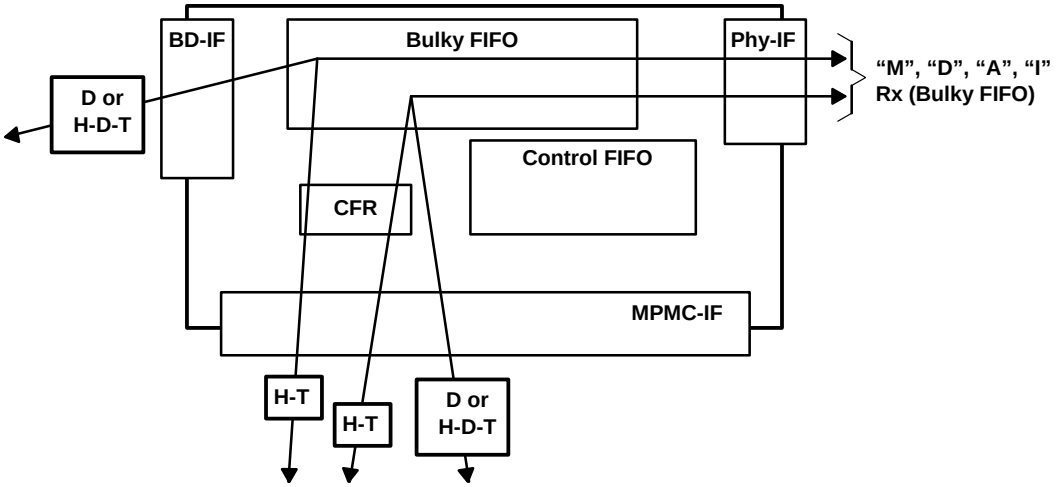


Figure 4–7. Bulky Fifo Receive Modes of Operation.

4.2.1 Receiving A-packets

Asynchronous traffic can be directed into either one or both asynchronous receive FIFOs depending on type of packet received. For asynchronous self ID packets a separate BWRX FIFO provides easy startup after reset.

Regular "A" control packets are meant to go to the ACRX FIFO while asynchronous data packets are meant to go directly to the BARX FIFO to be forwarded to a high speed application. The ARDM0, ARDM1, SIDM0, & RIDM0 bits in the RMISC register allow various packet steering options.

nSIDM0 =0 self ID packets will go to the BWRX FIFO

nSIDM0=1 selfID packets will go to the BARX FIFO

nRIDM0=0 Expected Response packets (tlabel/tcode in PHYSR register) will go to the ACRX FIFO. UnExpected Response packets (tlabel/tcode in PHYSR register) will go to the ACRX FIFO.

nRIDM0=1 Expected Response packets (tlabel/tcode in PHYSR register) will go to the BARX FIFO. UnExpected Response packets (tlabel/tcode in PHYSR register) will go to the ACRX FIFO.

During the reception of asynchronous packets, the destination FIFO is determined by decoding the destination address in the packet header. The type of steering that takes place is programmable using the ARDMx register as shown below:

Table 4–8. ARDMx Register Programming

ARDM1	ARDM0	"A" TRAFFIC FLOW	DESTINATION ADDRESS
0	0	All nonbroadcast "A" packets go to ACRX FIFO.	bus,node,00000,0000000 <= dest_addr <= bus,node,FFFFF,FFFFFFF
		All broadcast "A" packets go to BWRX FIFO.	bus,b_node,00000,0000000 <= dest_addr <= bus,b_node,FFFFF,FFFFFFF
0	1	Nonbroadcast nonRegister space "A" packets go to BARX FIFO.	bus,node,00000,0000000 <= dest_addr <– bus,node,FFFFE,FFFFFFF
		Broadcast nonRegister space "A" packets go to BARX FIFO.	bus,b_node,00000,0000000 <= dest_addr <– bus,b_node,FFFFE,FFFFFFF
		Nonbroadcast register space "A" packets go to ACRX FIFO.	bus,node,FFFFF,0000000 <= dest_addr <– bus,node,FFFFF,FFFFFFF
		Broadcast register space "A" packets go to BWRX FIFO.	bus,b_node,FFFFF,0000000 <= dest_addr <– bus,b_node,FFFFF,FFFFFFF
1	0	All nonbroadcast "A" packets go to BARX FIFO.	bus,node,00000,0000000 <= dest_addr <– bus,node,FFFFF,FFFFFFF
		All broadcast "A" packets go to BARX FIFO.	bus,b_node,00000,0000000 <= dest_addr <– bus,b_node,FFFFF,FFFFFFF
1	1	Nonbroadcast "A" packets addressed to lower half of node addressable space go to BARX FIFO.	bus,node,00000,0000000 <= dest_addr <– bus,node,7FFFF,FFFFFFF
		Broadcast "A" packets addressed to lower half of node addressable space go to BARX FIFO.	bus,b_node,00000,0000000 <= dest_addr <– bus,b_node,7FFFF,FFFFFFF
		Nonbroadcast "A" packets addressed to upper half (includes private and register space) of node addressable space go to ACRX FIFO.	bus,node,80000,0000000 <= dest_addr <– bus,node,FFFFF,FFFFFFF
		Broadcast "A" packets addressed to upper half (includes private and register space) of node addressable space go to BWRX FIFO.	bus,b_node,80000,0000000 <= dest_addr <– bus,b_node,FFFFF,FFFFFFF

NOTES: 1. bus = valid bus number or local bus number (Bus Number field in BRD register or 3FF respectively).
2. node = valid node number (Node Number field in BRD register).
3. b_node = broadcast node number (3F).

4.2.1.1 Reads from BWRX–FIFO

The BWRX FIFO is mapped to the BWRX register. Read accesses here will access the FIFO.

The Status of the this FIFO is mapped to the ACRXS register.

4.2.1.2 Reads from ACRX–FIFO

The ACRX FIFO is mapped to the ACRX register. Read accesses here will access the FIFO.

The Status of the this FIFO is mapped to the ACRXS register.

4.2.1.3 Receiving “A” packets to the BARX FIFO

The “A” packet header quadlets and the “A” packet trailer will be copied to the ARH[0..3] register and the ART register. If the ARHS bit (AICR register) is low, the complete “A” packet (including header and trailer) will be output from the BARX FIFO else only the data payload will be out from the BARX FIFO.

When BDARE (AICR register) is high, the BDIF (not the MPMC) has access to the BARX FIFO.

When ARSP (AICR register) is high, BDARE will be cleared every time an “A” packet is sent to the BDIF. The MPMC must set BDARE high again before another “A” packet is allowed to the BDIF.

When BDARE (AICR register) is low, the MPMC has access to the BARX FIFO via the BARX register.

The BARX size is located in BARXSize of the BASZ register.

The BARX Quadlet available count is located in BARXAvail of the BAAVAL register.

4.2.2 Receiving ‘I’-packets

The “I” packet header quadlet and the “I” packet trailer will be copied to the IRH register and the IRT register. If the IRHS bit (AICR register) is low, the complete “I”packet (including header and trailer) will be output from the BIRX FIFO else only the data payload will be output from the BIRX FIFO.

When BDIRE (AICR register) is high, the BDIF (not the MPMC) has access to the BIRX FIFO.

When IRSP (AICR register) is high, BDIRE will be cleared every time an “I” packet is sent to the BDIF. The MPMC must set BDIRE high again before another “I” packet is allowed to the BDIF.

When BDIRE (AICR register) is low, the MPMC has access to the BIRX FIFO via the BIRX register.

The BIRX size is located in BIRXSize of the BASZ register.

The BIRX Quadlet available count is located in BIRXAvail of the BAAVAL register.

4.2.3 Receiving ‘M’-packets

The “M” packet header quadlet and the M-packet trailer will be copied to the MRH register and the MRT register. If the MRHS bit (MCR register) is set low then the complete “M” packet (including header and trailer) will be output from the BMDRX FIFO else only the data payload will be output from the BMDRX FIFO.

If the BDMRE bit (MCR register) is low, then MPMC has access to the BMDRX FIFO via the MRF register. When BDMRE is high the “M” cells are accessed through the BDIF.

When the value of the CLKTIM register plus the value of the MRTO register equals the value of the time stamp of a received M-cell, the BDOF pins signal the first byte of an MPEG-2 cell to be read if the BDIF is selected as destination (BDMRE=high).

NOTE: On MRHS=low the receive release time calculation is disabled (test mode to receive complete M-packet)

4.2.4 Receiving ‘DSS’-packets

The DSS-packet header quadlet and the DSS-packet trailer will be copied to the DRH register and the DRT register. If the DRHS bit (DCR register) is set low then the complete DSS-packet (including header and trailer) will be stored to the BMDRX FIFO; if the DRHS bit is high then the header and trailer quadlet are stripped off (pure I-payload goes to the BMDRX FIFO).

On reception of an D-packet the DRAV interrupt in the extended interrupt register is generated.

If the BDDRE bit (DCR register) is clear, then MP/MC has access to the BMDRX FIFO via the DRF register. On BDDRE high the DSS-cells are accessed through the BDIF.

When the value of the CLKTIM register plus the value of the DRTO register equals the value of the time stamp of a received DSS-cell then the DRelTim interrupt bit in the EIR register is set; and the BDOF pins signal the first byte of an DSS-cell to be read if the BDIF is selected as destination (BDDRE=high).

NOTE: On DRHS=low (DCR register) the receive release time calculation is disabled (testmode to receive complete DSS–packets).

4.3 Asynchronous Transmit (Host Bus to TSB12LV41)

There are two basic formats for data to be transmitted and received. The first is for quadlet packets, and the second is for block packets. For transmits, the FIFO address indicates the beginning, middle, and end of a packet. For receives, the data length, which is found in the header of the packet, determines the number of bytes in a block packet.

4.3.1 Quadlet Transmit

The quadlet-transmit format is shown in Figure 4–8 and is described in Table 4–9. The first quadlet contains packet control information. The second and third quadlets contain the 64-bit, quadlet-aligned address. The fourth quadlet is data used only for write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

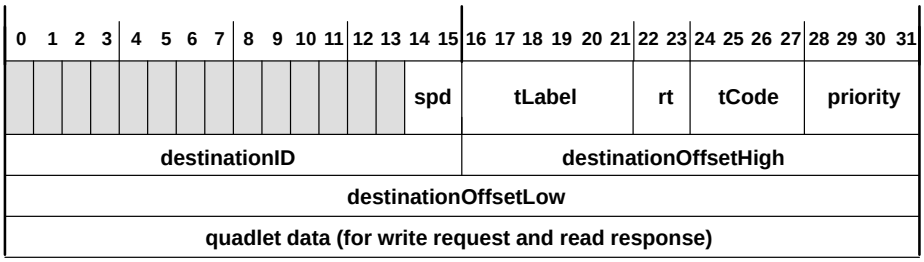


Figure 4–8. Quadlet-Transmit Format

Table 4–9. Quadlet-Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	The spd field indicates the speed at which the current packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is: 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6–10 of IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of the current packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4).
quadlet data	For write requests and read responses, the quadlet data field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.

4.3.2 Block Transmit

The block-transmit format is shown in Figure 4–9 and is described in Table 4–10. The first quadlet contains packet-control information. The second and third quadlets contain the 64-bit address. The first 16 bits of the fourth quadlet contains the dataLength field. This is the number of bytes of data in the packet. The remaining 16 bits represent the extended_tCode field (see Table 6–11 of the IEEE-1394 standard for more information on extended_tCodes). The block data, if any, follows the extended_tCode.

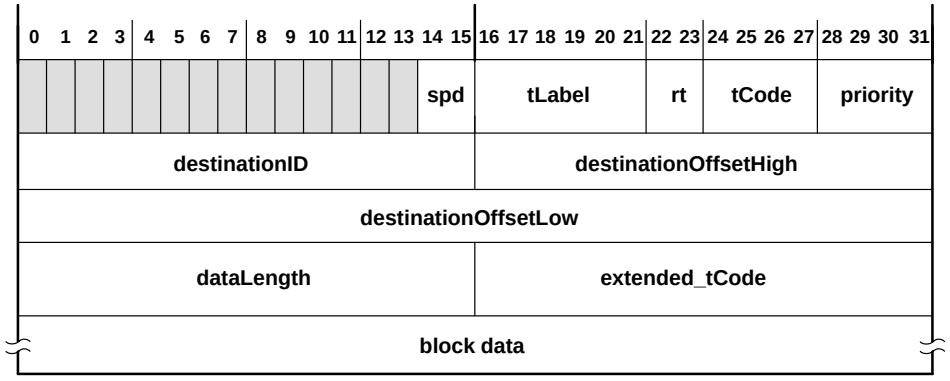


Figure 4–9. Block-Transmit Format

Table 4–10. Block-Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	The spd field indicates the speed at which the current packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for the current packet (see Table 6–10 of IEEE-1394 standard).
priority	The priority level for the current packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4). The upper 4 bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	The dataLength filed contains the number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in the current packet (see Table 6–11 of the IEEE-1394 standard).
block data	The block data field contains the data to be sent. If dataLength is 0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in byte 0 of the first quadlet.

4.3.3 Quadlet Receive

The quadlet-receive format is shown in Figure 4–10 and is described in Table 4–11. The first 16 bits of the first quadlet contain the destination node and bus ID, and the remaining 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source, and the remaining 16 bits of the second and third quadlets contain the 48-bit, quadlet-aligned destination offset address. The fourth quadlet contains data that is used by write requests and read responses. For read requests and write responses, the quadlet data field is omitted. The last quadlet contains packet-reception status that is added by the TSB12LV41.

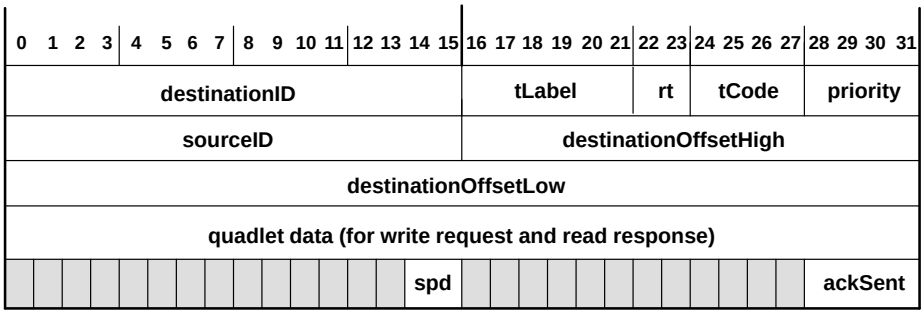


Figure 4–10. Quadlet-Receive Format for Control FIFO

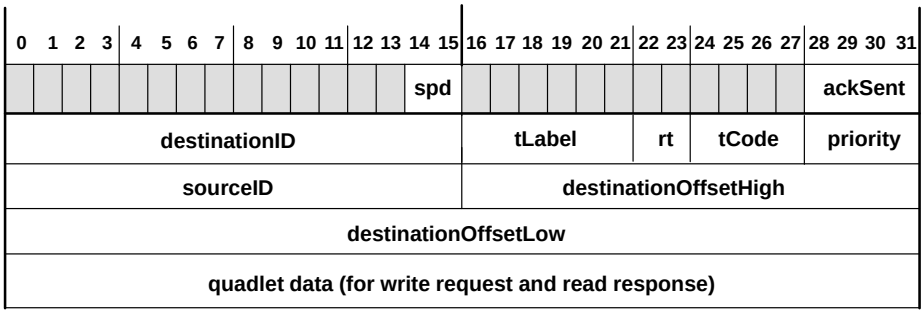


Figure 4–11. Quadlet-Receive Format for Bulky Data FIFO

Table 4–11. Quadlet-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	The destinationID field contains the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6–10 of the IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
sourceID	The sourceID field contains the node ID of the sender of the current packet.
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). (The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets, and the remaining bits are reserved.)
quadlet data	For write requests and read responses, the quadlet data field holds the transferred data. For write responses and read requests, this field is not present.
spd	The spd field indicates the speed at which the current packet was sent. 00 = 100 Mbits/s, 01 = 200 Mbits/s, 10 = 400 Mbits/s, and 11 is undefined for this implementation.
ackSent	The ackSent field holds the acknowledge sent by the receiver for the current packet (see Table 6–13 in the draft standard).

4.3.4 Block Receive

The block-receive format is shown in Figure 4–12 and is described in Table 4–12. The first 16 bits of the first quadlet contain the node and bus ID of the destination node, and the last 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source node, and the last 16 bits of the second quadlet and all of the third quadlet contain the 48-bit, quadlet-aligned destination offset address. All remaining quadlets, except for the last one, contain data that is used only for write requests and read responses. For block read requests and block write responses, the data field is omitted. The last quadlet contains packet-reception status.

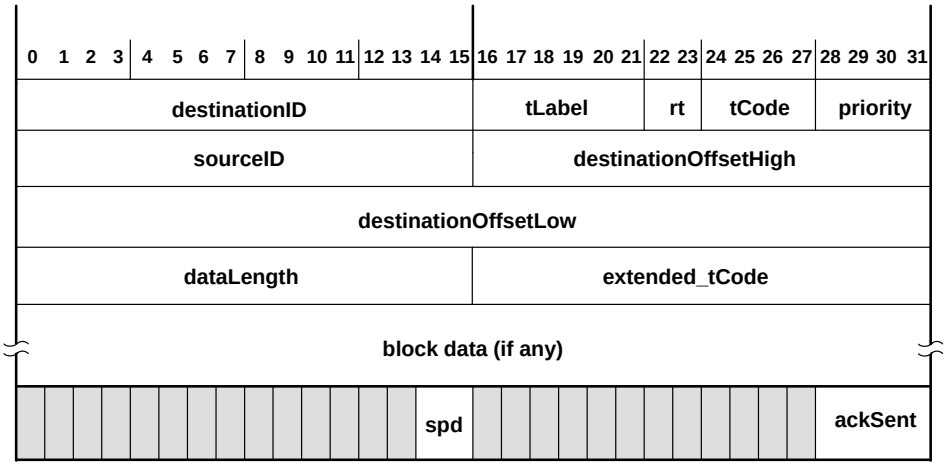


Figure 4–12. Block-Receive Format for Control FIFO

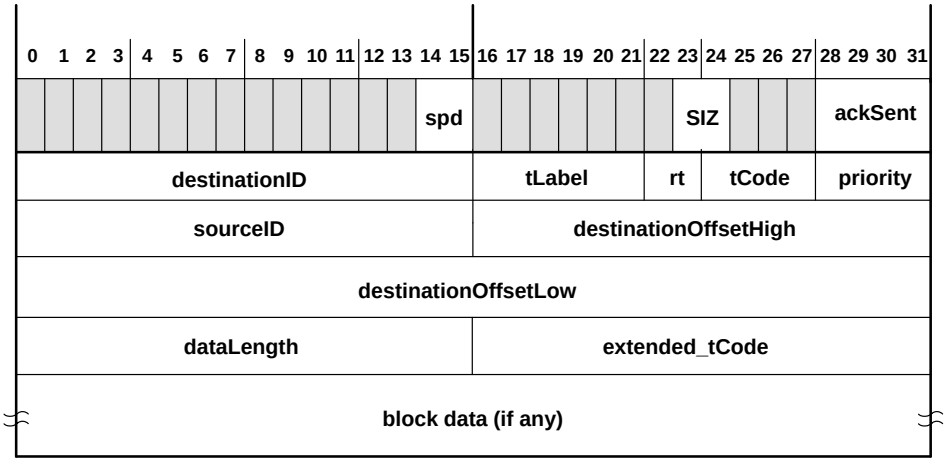


Figure 4–13. Block-Receive Format for Bulky Data FIFO

Table 4–12. Block-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field contains the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6–10 of the IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
sourceID	The sourceID field contains the node ID of the sender of the current packet.
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). The upper 4 bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	For write request, read responses, and locks, the dataLength field indicates the number of bytes being transferred. For read requests, the dataLength field indicates the number of bytes of data to be read. A write-response packet does not use this field. Note that the number of bytes does not include the head, only the bytes of block data.
extended_tCode	The extended_tCode field contains the block extended_tCode to be performed on the data in the current packet (see Table 6–11 of the IEEE-1394 standard).
block data	The block data field contains any data being transferred for the current packet. Regardless of the destination address or memory alignment, the first byte of the data appears in byte 0 of the first quadlet of this field. The last quadlet of the field is padded with zeros out to four bytes, if necessary.
spd	The spd field indicates the speed at which the current packet was sent. 00 = 100 Mb/s, 01 = 200 Mb/s, 10 = 400 Mb/s, and 11 is undefined for this implementation.
ackSent	The ackSent field holds the acknowledge sent by the receiver for the current packet.
SIZ	SIZ indicates the number of zero-filled bytes in the last quadlet of the packet.

4.4 Isochronous Transmit (Host Bus to TSB12LV41)

The format of the isochronous-transmit packet is shown in Figure 4–14 and is described in Table 4–13. The data for each channel must be presented to the isochronous-transmit FIFO interface in this format in the order that packets are to be sent. The transmitter sends any packets available at the isochronous-transmit interface immediately following reception or transmission of the cycle-start message.

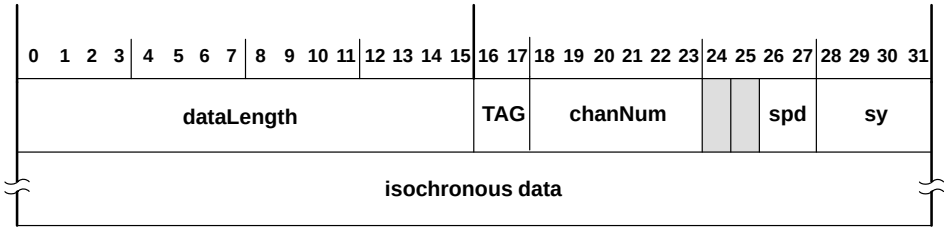


Figure 4–14. Isochronous-Transmit Format

Table 4–13. Isochronous-Transmit Functions

FIELD NAME	DESCRIPTION
dataLength	The dataLength field indicates the number of bytes in the current packet
TAG	The TAG field indicates the format of data carried by the isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	The chanNum field carries the channel number with which the current data is associated.
spd	The spd field contains the speed at which to send the current packet.
sy	The sy field carries the transaction layer-specific synchronization bits.
isochronous data	The isochronous data field contains the data to be sent with the current packet. The first byte of data must appear in byte 0 of the first quadlet of this field. If the last quadlet does not contain four bytes of data, the unused bytes should be padded with zeros.

4.5 Isochronous Receive (TSB12LV41 to Host Bus)

The format of the iscohronous-receive data is shown in Figure 4–15 and is described in Table 4–14. The data length, which is found in the header of the packet, determines the number of bytes in an isochronous packet.

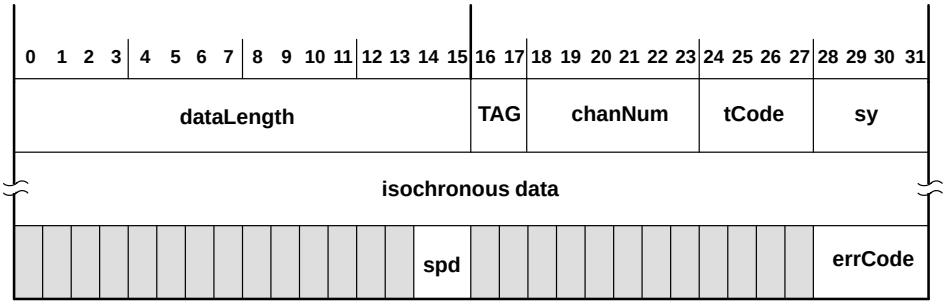


Figure 4–15. Isochronous-Receive Format for Control FIFO

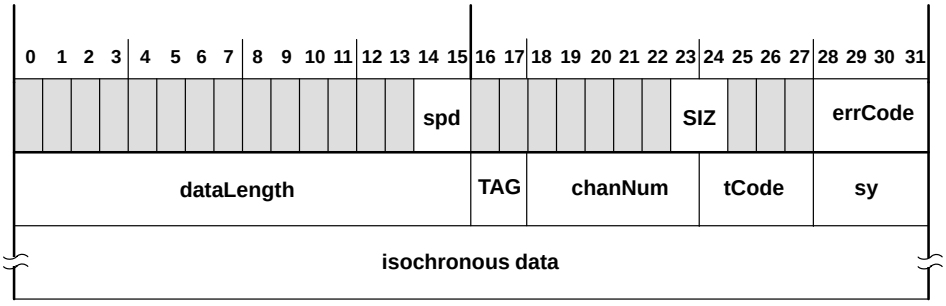


Figure 4–16. Isochronous-Receive Format for Bulky Data FIFO

Table 4–14. Isochronous-Receive Functions

FIELD NAME	DESCRIPTION
dataLength	The dataLength field indicates the number of bytes in the current packet.
TAG	The TAG field indicates the format of data carried by isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	The chanNum field contains the channel number with which this data is associated.
tCode	The tCode field carries the transaction code for the current packet (tCode = Ah).
sy	The sy field carries the transaction layer-specific synchronization bits.
isochronous data	The isochronous data field has the data to be sent with the current packet. The first byte of data must appear in byte 0 of the first quadlet of this field. The last quadlet should be padded with zeros.
spd	The spd field indicates the speed at which the current packet was sent.
errCode	The errCode field indicates whether the current packet has been received correctly. The possibilities are Complete, DataErr, or CRCErr, and have the same encoding as the corresponding acknowledge codes.
SIZ	SIZ indicates the number of zero-filled bytes in the last quadlet of the packet.

4.6 Snoop

The format of the snoop data is shown in Figure 4–17 and is described in Table 4–15. The receiver module can be directed to receive any and all packets that pass by on the serial bus. In this mode, the receiver presents the data received to the receive-FIFO interface.

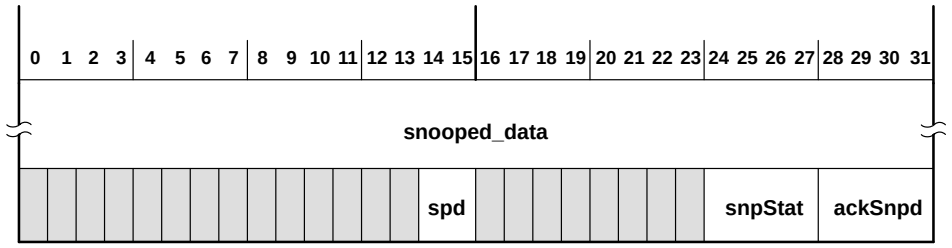


Figure 4–17. Snoop Format

Table 4–15. Snoop Functions

FIELD NAME	DESCRIPTION
snooped_data	The snooped_data field contains the entire packet received or as much as could be received.
spd	The spd field carries the speed at which the current packet was sent.
snpStat	The snpStat field indicates whether the entire packet snooped was received correctly. A value equal to the complete acknowledge code indicates complete reception. A busyA or busyB acknowledge code indicates incomplete reception.
ackSnpd	The ackSnpd field indicates the acknowledge seen on the bus after the packet is received.

4.7 CycleMark

The format of the CycleMark data is shown in Figure 4–18 and is described in Table 4–16. The receiver module inserts a single quadlet to mark the end of an isochronous cycle. The quadlet is inserted into the receive-FIFO.

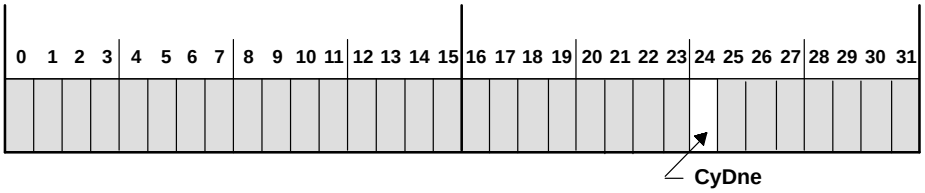


Figure 4–18. CycleMark Format

Table 4–16. CycleMark Function

FIELD NAME	DESCRIPTION
CyDne	Th CyDne field indicates the end of an isochronous cycle.

4.8 Phy Configuration

The format of the phy configuration packet is shown in Figure 4–19 and is described in Table 4–17. The phy configuration packet transmit contains two quadlets. The first quadlet tells the TSB12LV41 that this quadlet is the phy configuration packet. The Eh is then replaced with 0h before the packet is transmitted to the phy interface.

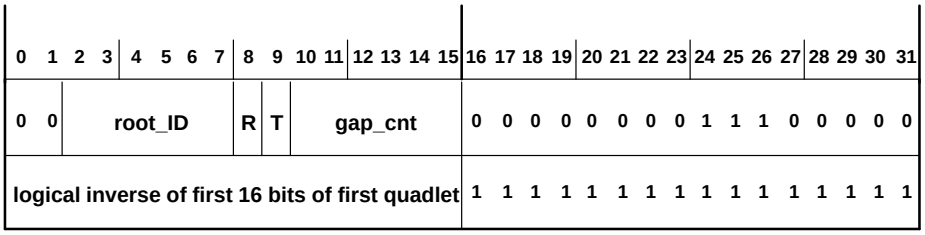


Figure 4–19. Phy Configuration Format

Table 4–17. Phy Configuration Functions

FIELD NAME	DESCRIPTION
00	The 00 field is the phy configuration packet identifier.
root_ID	The root_ID field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R†	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T†	When T is set, the PHY_CONFIGURATION.gap_count field of all the nodes is set to the value in the gap_cnt field.
gap_cnt	The gap_cnt field contains the new value for PHY_CONFIGURATION.gap_count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, gap_cnt is set to 63h unless a new phy configuration packet is received.

† A phy configuration packet with R = 0 and T = 0 is reserved and is ignored when received.

4.9 Receive Self-ID Packet

The format of the receive Self-ID packet is shown in Figure 4–20 and is described in Table 4–18. When RxSId (bit 1 of the control register) is set, the receive Self-ID packet is stored in Control FIFO.

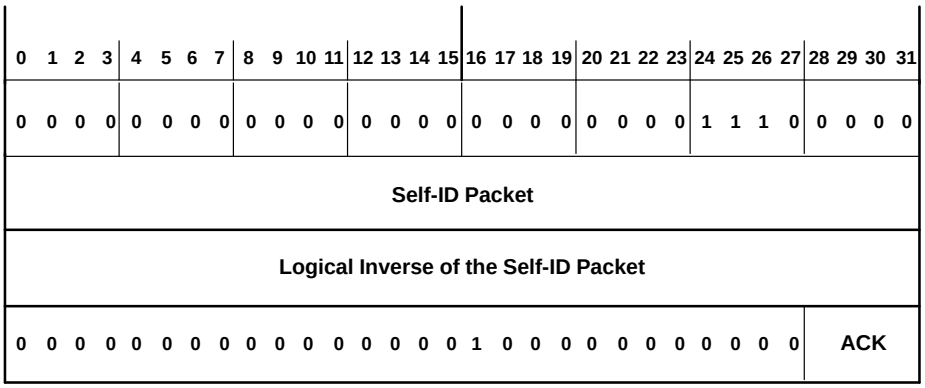


Figure 4–20. Receive Self-ID Format for Control FIFO

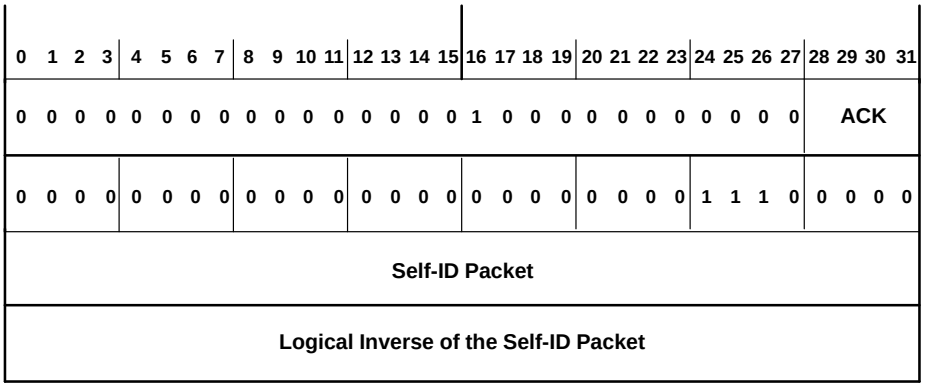


Figure 4–21. Receive Self-ID Format for Bulky Data FIFO

Table 4–18. Receive Self-ID Function

FIELD NAME	DESCRIPTION
ACK	When the ACK field is set (0001b), the data in the Self-ID packet is correct. When ACK is ≠ 0001b, the data in the Self-ID packet is incorrect.

When there is only one node (i.e., one phy/LLC pair) on the bus, following a bus reset, the FIFO contains 000_00E0h and the acknowledge quadlet only.

When there are three nodes on the bus, each with a phy having three or less ports, following a bus reset, the FIFO of any one of the LLCs is shown in Table 4–19.

Table 4–19. GRF Contents With Three Nodes on a Bus

GRF CONTENTS	DESCRIPTION
0000_00E0h	Header for Self-ID
self–ID1	Self_ID for phy #1
self–ID1 inverse	Self_ID for phy #1 inverted
self–ID2	Self_ID for phy #2
self–ID2 inverse	Self_ID for phy #2 inverted
0000_000_ACK	Trailing acknowledgement

The first quadlet in a Self-ID packet is 0000_00E0h. The second quadlet in the Self-ID packet is described in Figure 4–22, Figure 4–23, and Table 4–20. The third quadlet is the inverse of the Self-ID quadlet. The fourth and final Self-ID quadlet in the packet is the acknowledgement.

The cable phy sends one to four Self-ID packets at the base rate (100 Mbits/s) during the Self-ID phase of arbitration. The number of Self-ID packets sent depends on the number of ports. Figure 4–22 and Figure 4–23 show the formats of the cable phy Self-ID packets.

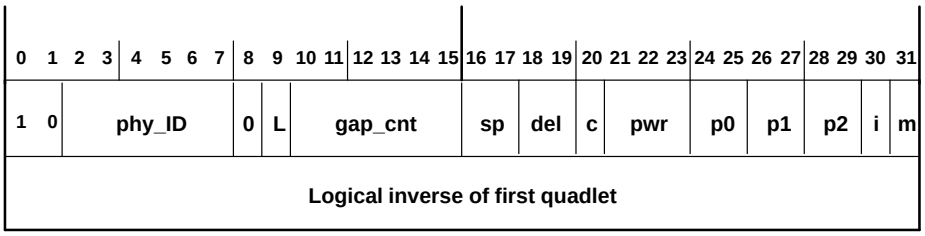
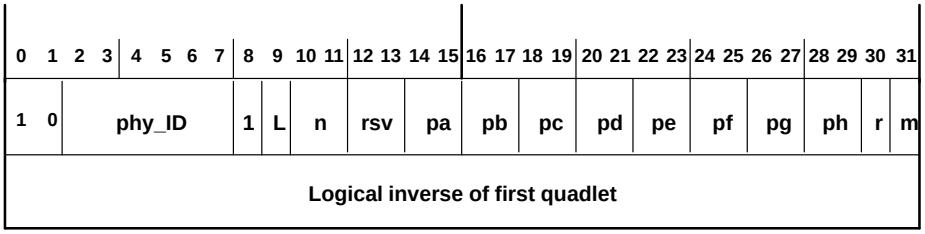


Figure 4–22. Phy Self-ID Packet #0 Format



PACKET #	n†	pa	pb	pc	pd	pe	pf	pg	ph
1	0	p3	p4	p5	p6	p7	p8	p9	p10
2	1	p11	p12	p13	p14	p15	p16	p17	p18
3	2	p19	p20	p21	p22	p23	p24	p25	p26

† For n = 3 – 7, fields pa through ph are reserved.

Figure 4–23. Phy Self-ID Packet #1, Packet #2, and Packet #3 Format

Table 4–20. Phy Self-ID Functions

FIELD NAME	DESCRIPTION	
10	The 10 field is the Self-ID packet identifier.	
c	When c is set and the link-active flag is set, this field indicates that the current node is a contender for the bus or isochronous resource manager.	
del	The del field contains the worst-case repeater-data delay time. The code is:	
	00	≤ 144 ns ≈ (14 / Base_Rate)
	01 – 11	Reserved
gap_cnt	The gap_cnt field contains the current value for the current node PHY_CONFIGURATION.gap_count field.	
i	When set, the i field indicates that the current node initiated the current bus reset (i.e., it started sending a bus reset signal before it received one†).If this function is not implemented, i is returned as 0.	
L	When L is set, the current node has an active LLC and transaction layer.	
m	When set, the m field indicates that another Self-ID packet for the current node immediately follows (i.e. when m is set and the next Self-ID packet received has a different phy_ID, then a Self-ID packet was lost).	

† There is no way to ensure that exactly one node has this bit set. More than one node can be requesting a bus reset at the same time.

Table 4–20. Phy Self-ID Functions (Continued)

FIELD NAME	DESCRIPTION	
n	The n field is the extended Self-ID packet sequence number. The code is:	
	0	Self-ID packet 1
	1	Self-ID packet 2
	2	Self-ID packet 3
phy_ID	The phy_ID field is the physical node identifier of the sender of the current packet.	
p0 – p26	The p0 – P26 field indicates the port status. The code is:	
	00	Not present on the current phy
	01	Not connected to any other phy
	10	Connected to the parent node
	11	Connected to the child node
pwr	The pwr field contains the bits that indicate the power consumption and source characteristics. The code is:	
	000	The node does not need power and does not repeat power.
	001	The node is self powered and provides a minimum of 15 W to the bus.
	010	The node is self powered and provides a minimum of 30 W to the bus.
	011	The node is self powered and provides a minimum of 45 W to the bus.
	100	The node can be powered from the bus and is using up to 1 W.
	101	The node is powered from the bus and is using up to 1 W. An additional 2 W is needed to enable the LLC and higher layers.‡
	110	The node is powered from the bus and is using up to 1 W. An additional 5 W is needed to enable the LLC and higher layers.‡
	111	The node is powered from the bus and is using up to 1 W. An additional 9 W is needed to enable the LLC and higher layers.‡
r	Reserved and set to all zeros.	
rsv	Reserved and set to all zeros.	
sp	The sp field contains the phy speed capability. The code is:	
	00	98.304 Mbits/s
	01	98.304 Mbits/s and 196.608 Mbits/s
	10	98.304 Mbits/s 196.608 Mbits/s, and 393.216 Mbits/s
	11	Reserved

† There is no way to ensure that exactly one node has this bit set. More than one node can be requesting a bus reset at the same time.

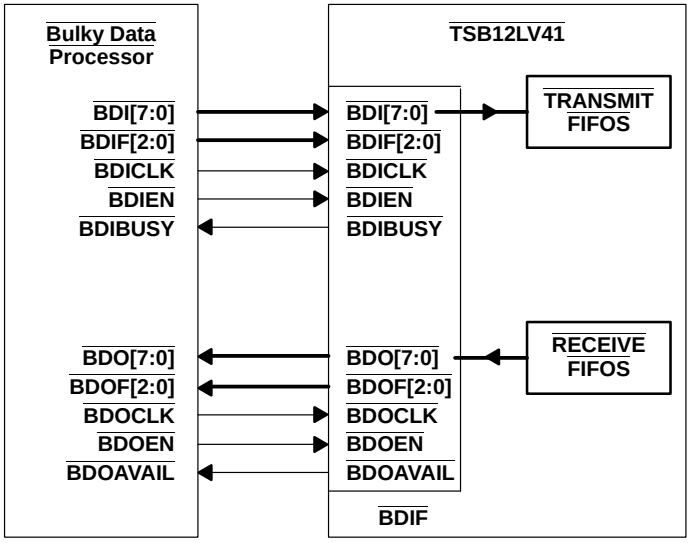
‡ The LLC and higher layers are enabled by the Link-On Phy packet.

5 External Interfaces

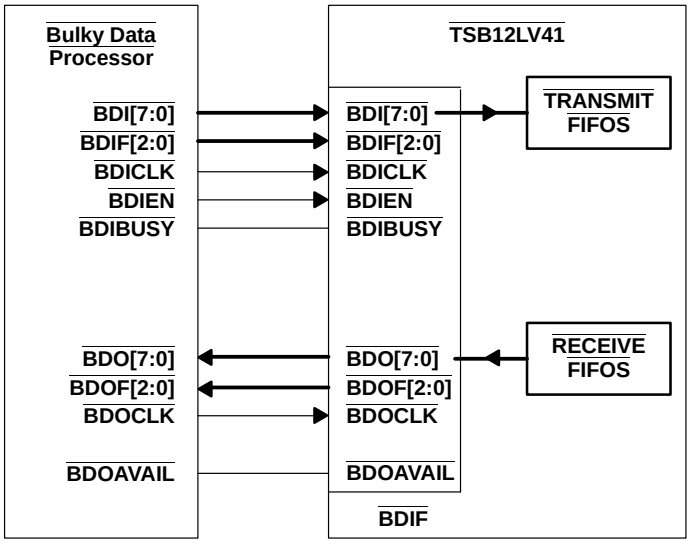
5.1 Bulky Data Interface

The bulky data interface (BDIF) provides a data transfer interface for use with high-speed hosts. This interface allows the host to read and write data to a 8K-byte FIFO that is divided into six logically separate FIFOs. Two bytewide data buses are used to transfer data between the LLC and the host. The BDIO[7:0] bus can be used as either a bidirectional or input-only bus depending on the programmed BDI mode. The BDO[7:0] bus is output only.

This interface supports bidirectional transmit and receive of DSS/DVB data on 1394 as defined by the IEC1883 standard. Asynchronous and isochronous data transmit and receive are also supported by this interface. The TSB12LV41 interfaces directly with Texas Instruments TSB320AV07000 Series of MPEG2 and DSS decoders via the BDI.



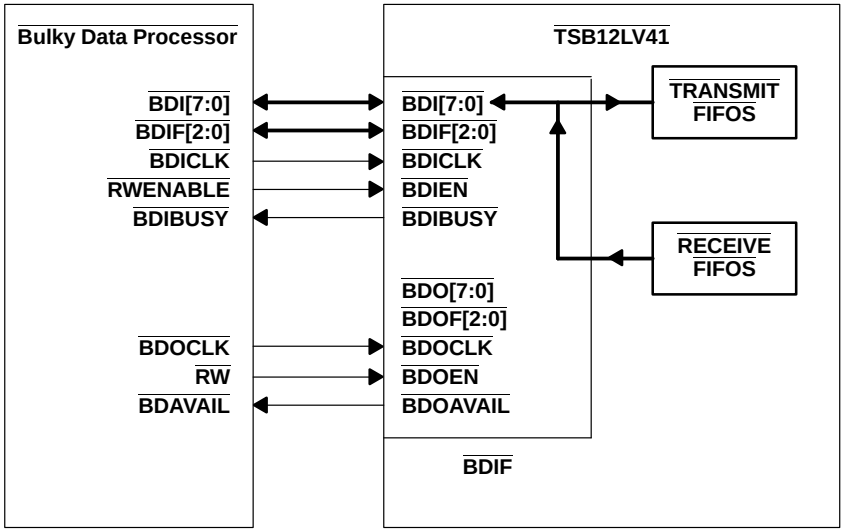
NOTE A: BDIMODE = 000, BDOMODE = 00, 8-bit parallel I/O



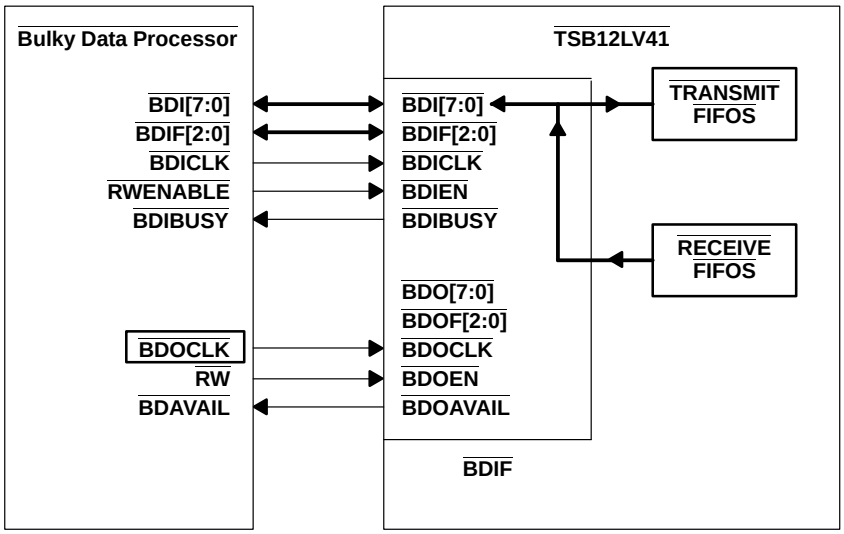
NOTE B: BDIMODE = 000, BDOMODE = 01, parallel I/O, no read control

Figure 5–1. Synchronous Two-Port Configuration

PRODUCT PREVIEW



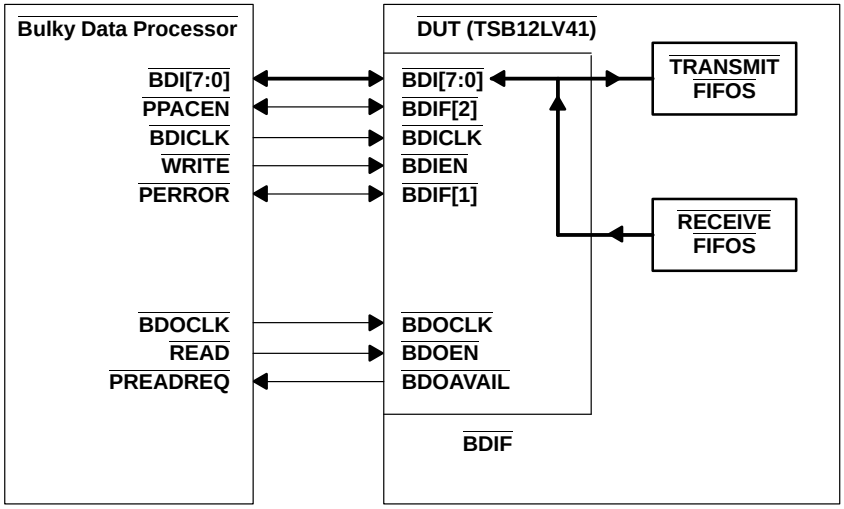
NOTE A: BDIMODE = 001, BDOMODE = 00



NOTE B: BDIMODE = 011, BDOMODE = 00

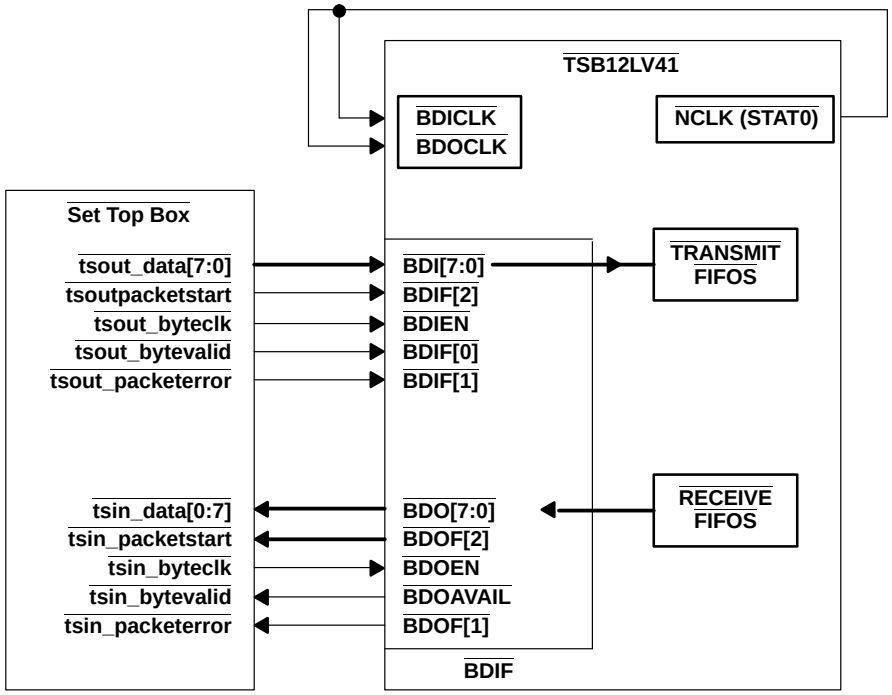
Figure 5–2. Operations Modes for Bulky Data Port With 1 Bidirectional I/O Port and 1 RW Control Signal

PRODUCT PREVIEW



NOTE A: BDIMODE = 010, BDOMODE = 00, bidirectional MPEG/DSS data only

Figure 5–3. Operation Mode for Bulky Data Port With 1 Bidirectional I/O Port, 1 Read, and 1 Write Control Signal



NOTE A: BSKYB BDIMODE = 3'b101, BDOMODE = 2'b11, port asynchronous RW strobes

Figure 5–4. Asynchronous Set-Top Box Connection

5.1.1 Bulky Data Interface Signals (BDIF)

SIGNAL NAME	INPUT/ OUTPUT	DESCRIPTION
BDI0/BDIN	IN/OUT	Parallel bulky data in/output 0 if BDIMode in I/O configuration register is set to 000,001,010,011. Serial bulky data input if BDIMode in BIF configuration register is set to 100.
BDI1/BDOUT	IN/OUT	Parallel bulky data in/output 1 if BDIMode in BIF configuration register is set to 000,001,010,011. Time Stamp input if BDIMode in BIF configuration register is set to 100 and MHIM is set to '0'.
BDI[7..1]	IN/OUT	Parallel bulky data I/O 1..7. Input only when BDIMode in BIF register is set to 000. Parallel bulky data in/output if BDIMode in BIF configuration register is set to 001,010,011.
BDICLK	IN	Bulky data input clock (up to 20.5 MHz in parallel mode; up to 80 MHz in serial mode)
BDIEN/W	IN	Bulky data input enable. When BDIMode is set to 010 this pin is used as a Write enable
BDIF[2] /PACEN	IN/OUT	Bulky data I/O format[2]. When BDIMode=010 this pin is used as a packet framing signal
BDIF[1] /PERROR	IN/OUT	Bulky data I/O format[1]. When BDIMode=010 this pin is used as a packet error signal
BDIF[0]	IN/OUT	Bulky data I/O format[0].
BDIF[2:0]		000 Reserved 001 byte of an MPEG2 cell 010 byte of an unformatted I–packet 011 byte of an A–packet 100 reset of BDIF receive part 101 first byte of an MPEG2 cell 110 last byte of an unformatted I–packet 111 last byte of an A–packet
BDO0/BDOUT	OUT	Parallel bulky data output 0 if BDOMode[1] I/O configuration register is set to 0. Serial bulky data output if BDOMode[1] I/O configuration register is set to 1.
BDO[7..1]	OUT	Parallel bulky data outputs 1..7
BDOCLK	IN	Bulky data output clock (up to 20.5 MHz in parallel mode BDIMode 000,001, up to 40 Mhz in parallel BDIMode 010,011 and up to 80 MHz in serial mode BDOMode[1]: 1)
BDOEN/RW*/R	IN	Bulky data output enable. Read/Write control in bidirectional mode BDIMode=000,001,011. Read in bidirectional mode BDIMode=010.
BDOF[2..0]	OUT	000 Reserved 001 byte of an MPEG2 cell 010 byte of an I-packet 011 byte of an A-packet 100 no output data available 101 first byte of an MPEG2 cell 110 last byte of an I-packet 111 last byte of an A-packet

BDAVAIL	OUT	The BDIF has data available to be read.
BDBUSY	OUT	The BDIF is Busy and will not accept input.

5.1.2 Bulky Data Interface Timing Modes

Connection to the BDIF is dependent on the mode selection. Note BDOAvail and BDIBusy terminals are shared terminals and are available on STAT2 and STAT3 respectively. Nclk (24.576 MHz) is available at STAT0. STAT terminal selection is defined in the Link Diagnostic register at address 30h.

BDIMode/ BDOMode	000/00	000/01	000/11	101/00	101/11	001/00	010/00	011/00
Data input	BDI/O	BDI/O	BDI/O	BDI/O ASYNC	BDI/O ASYNC	BDI/O	BDI/O	BDI/O
Data output	BDO	BDO	BDO	BDO ASYNC	BDO Synchronous	BDI/O ASYNC	BDI/O	BDI/O
Data bus	2	2	2	2	2	1	1	1
Duplex	Full	Full	Full	Full	Full	Half	Half	Half
Data input clock (MHz)	20.25	20.25	20.25	NCLK	NCLK	20.25	40.5	40.5
Data output clock (MHz)	20.25	20.25	NCLK	20.25	NCLK	20.25	40.5	40.5
Data throughtput Mbytes/s (max)	20 Write 20 Read	20 Write 20 Read	20 Write 10 Read	10 Write 20 Read	10 Write 10 Read	20.25	20.25	20.25
Controls:								
BDIEN	X	X	X	X	X	X	X	X
BDBUSY	X	X				X		X
BDOEN	X		X	X	X	X	X	X
BDOAVAIL	X	X	X	X	X	X	X	X
References	Fig 1	Fig 1	None	None	Fig 4	Fig 2	Fig 3	Fig 2

5.2 Microcontroller/microprocessor Interface Description

5.2.1 General

The TSB12LV41 operates in a big endian fashion. The Most Significant Bit (MSBit) is to the left with bit number zero. The Least Significant Bit (LSBit) is to the right with the largest bit number (in this case, 31). This is illustrated below. To avoid confusion, connect the MSBit of the processor controlling the TSB12LV41 to the TSB12LV41 MSBit, and likewise LSBit to LSBit, regardless of whether the processor is little or big endian. The correct swapping can be done by setting the Big Endian Control Bit (BeCtl in the IOCR register.

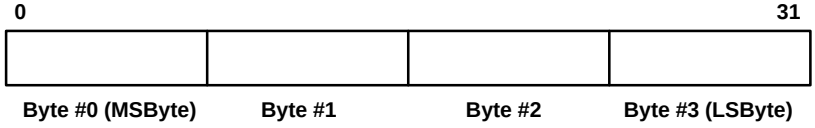


Figure 5–5. Big Endian Illustration chart

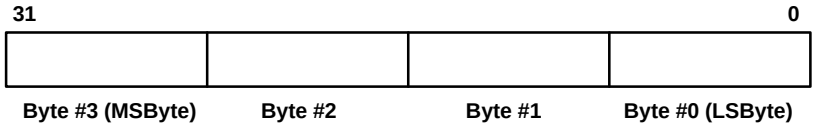


Figure 5–6. Little Endian Illustration chart

NOTE: To read in byte mode, the lower byte (bits 8–15) of the 16-bit data bus contain the byte data. The upper 16 bits will be all zero. To write, all the data should be put in the lower bits (bits 0–7). The data in the upper byte will not be written into the TSB12LV41.

There are two more considerations when dealing with endianness: Data Invariance and Address Invariance.

5.2.1.1 Data Invariant System Design

Figure TBD shows a Little Endian Data Invariant System Design example. In this system, the byte addresses are not preserved. Byte_0 of the host side microprocessor's little endian system is 33h. Byte_0 of the TSB12LV41 big endian system contains 30h. A data invariant design does not preserve the addresses when mapping between endian domains. If the data represents an integer, it is interpreted the same by both systems. If the data represents a string, an array, or some other type of byte indexed structure, it is interpreted differently by both systems.

The default setting of iocr.BeCtl is Big Endian (set to 1). iocr.DataInvarnt bit could be used to control the system design to be either data or address invariant. The power up default of iocr.DataInvarnt data invariant (set to 1).

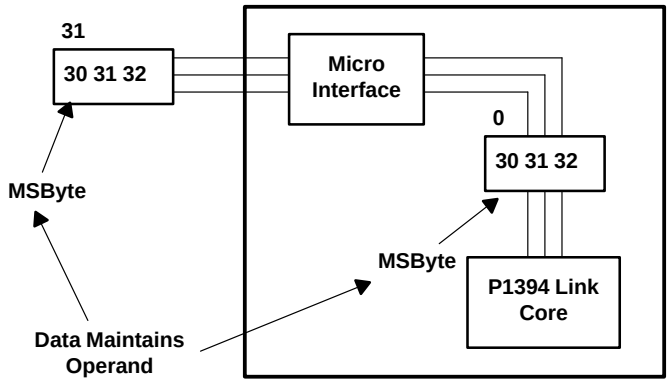


Figure 5–7. Little Endian Data Invariant System Illustration

5.2.1.2 Address Invariant System Design

Figure TBD shows a Little Endian Address Invariant System Design example. In this system, the byte addresses are preserved. Byte_0 of the host side microprocessor's little endian system is 33h. Byte_0 of the TSB12LV41's big endian system also contains 33h. This address invariant design preserves the addresses when mapping between endian domains. If the data represents a string, an array, or some other type of byte indexed structure, it is interpreted the same by both systems.

To accomplish this, set the iocr.BeCtl bit to "0" (Little Endian) and iocr.DataInvarnt bit to "0" (Address Invariant).

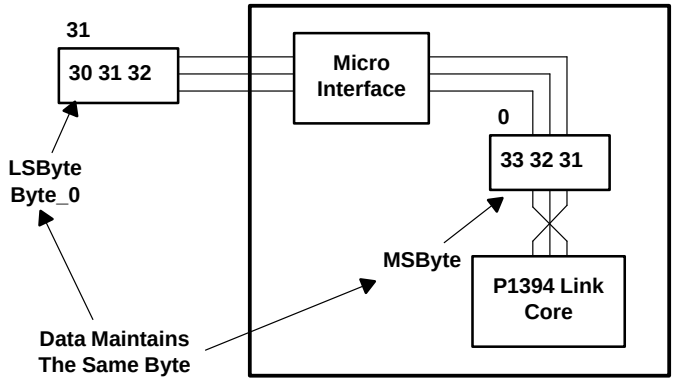


Figure 5–8. Little Endian Address Invariant System Illustration

NOTE: When the BeCtl bit is set to “1” (Big Endian), the DataInvarnt bit setting has no effect.

NOTE: When the BeCtl bit is set to the contrast value that is against the actual endianess of the microprocessor TSB12LV41 connected to, the actual data result passed through two different endianess domains is unpredictable.

5.3 Functional Description

The TSB12LV41 supports the TMS320AV700 architecture of Set–top box microprocessors from TI, the Motorola 680x0 class of microprocessors, and the Intel 8051 microcontroller. To detect which kind of microprocessor/microcontroller (MP/MC) is connected, MCSEL1 and MCSEL0 need to be driven to the correct levels during power up and reset. The values are as follows:

TMS320AV7000 Architecture	MCSEL1, MCSEL0 = 00
Motorola’s 680X0 class of microprocessors	MCSEL1, MCSEL0 = 01
Intel’s 8051 microcontroller	MCSEL1, MCSEL0 = 10

MCSEL1 and MCSEL0 share the same pins with BDOF1 and BDOF0 correspondingly (TBD, could be changed to dedicated pin or re-mapped to different pins during whole chip integration). (TBD: After power up reset, these two pins switch from input mode to output mode.)

Once the type of MP/MC has been determined, all the I/O control pins related to the MP/MC Interface map their functions to be applicable to the type of MP/MC detected. The following matrix table (Figure 6) defines the actual pin functions for particular type or MP/MCs:

Table 5–1. Extension Bus Pin/Function Matrix for MP/MC Interface

Name	MP/MC Type		
	Motorola 68000	TMS320AV7000	Intel 8051
ADR[0:8] (Mcaddr)	ADR[8:1] *	EXTADDR[8:0]	AD[7:0]**
DATA[0:15] (Mcdatain, Mcdataout)	D[15:0]	EXTDATA[15:0]	
CS/CSZ (_Mccs)	CS *	CSXZ	ALE
MCCTL0 (_Mcwr)	R/WZ	EXTR/WZ	WRZ
MCCTL1 (_Mcrd)			RDZ
RDY (McRdy)	DTACKZ	EXTWAITZ	

The TSB12LV41 Micro Interface Block is synchronized to BClk, which shares the same input pin with the NAND Tree Clock (NTCLK) only in the TMS320AV7000 Mode. BClk input is from the TMS320AV7000 extension bus external clock input (CLK40, 40.5MHz, 24.5ns). For all other modes (Motorola 68000 and Intel 8051), the Micro Interface is asynchronous. The internal clock used for these two modes is SClk, which is the 50MHz clock from the PHY.

Unless otherwise specified, all bus signals on the TSB12LV41 Micro Interface Block is denoted as: bit0 = MSB and bit15 = LSB. Mcdataouten is the MCAD0 – MCAD15 bi-directional address/data bus I/O control signal. The Mcdatain[0:15] and Mcdataout[0:15] are the input and output portion of this bus separately. Mcaddr[0:8] (MCADR0 – MAADR8) is the address bus of the TSB12LV41 in all the modes except Intel 8051 Mode.

Based on the particular Micro Mode, _Mcwr (MCCTL0) is the R/WZ or WRZ signal. _Mcrd (MCCTL1) is the RDZ signal only in Intel 8051 mode. McRdy is the ready/wait signal.

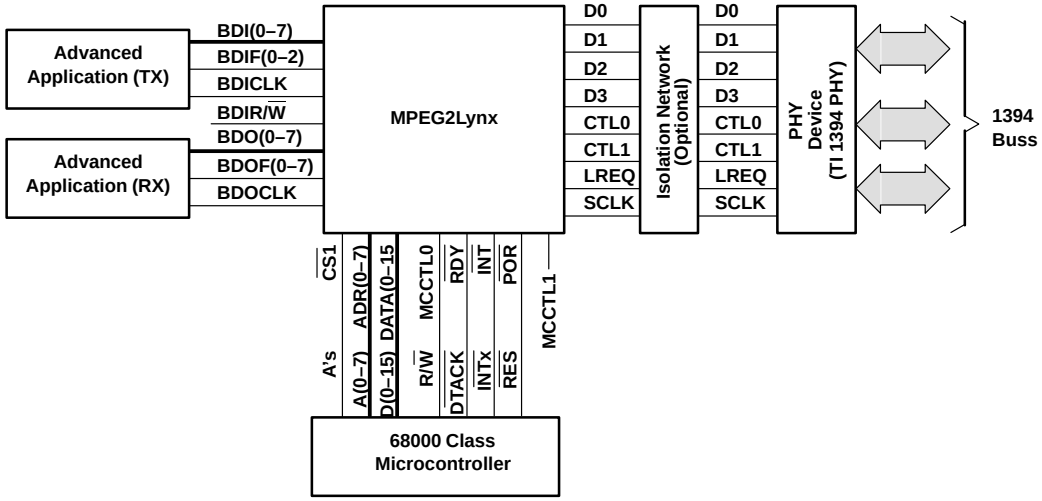


Figure 5–9. MPEG2Lynx Connections for 68XXX Class Microcontroller

This is for a complex audio, data, or video application connected in bytewide mode with independent RX and TX paths

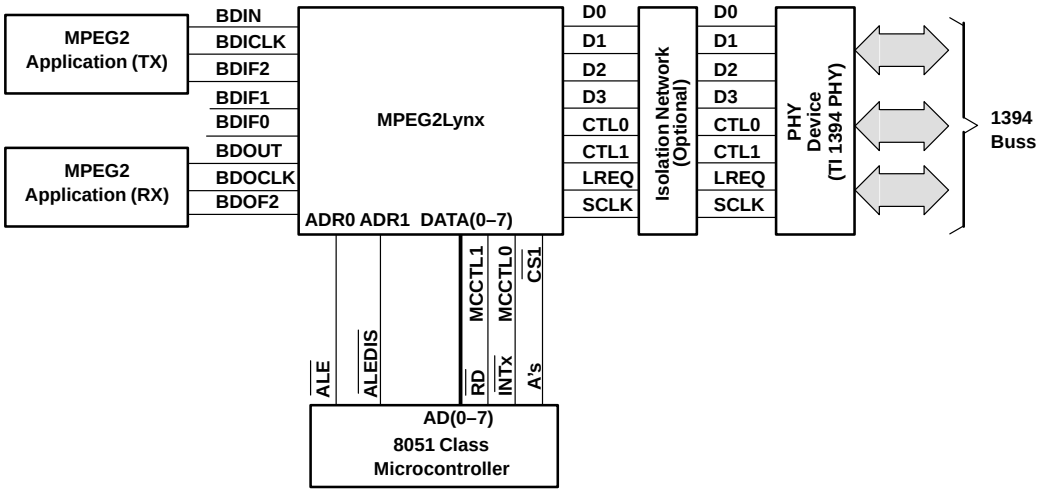


Figure 5–10. MPEG2Lynx Connections for 80XX Class Microcontroller

MPEG2 only video application connected in bit-serial mode with independent RX and TX paths.

Although IOCR provides a way to the extension bus interface, not all the settings are supported due to the function of the particular type of microprocessor. The following summarizes the special notes for all types of micros supported:

5.3.1 TMS320AV7000

Both Byte Access/Word Access are supported. Little Endian will be supported, although the TMS320AV7000 architecture is Big Endian.

5.3.1.1 Motorola 68000

Only Word Access is supported. To be able to load the right setting into the IOCR, 68000 will have to do four writes to finish the whole quadlet write, just as if it is a 8 bit processor. The upper byte of the first write has to be padded with zeros with the lower byte containing the actual setting information. All the other three writes could be loaded with all zeros. Blind Access Mode is not supported for this microprocessor.

5.3.1.2 Intel 8051

Word Access is not supported because it is an 8-bit processor.

5.3.2 General Read/Write Access

The microprocessor can access the TSB12LV41 in either handshake mode or Blind Access Mode. The handshake signal between the TSB12LV41 and the micro is RDY, which can be interpreted as either ready or wait depending on the type of micro connected. The read/write transaction cycle from the extension bus side is controlled by the chip select. In handshake mode, the micro normally drives the target address on the address bus, asserts the chip select and write/read control line for the type of transaction and provides data or waits for data on the data bus. The micro then counts on the Rdy/Wait signal from the TSB12LV41 micro interface to terminate the cycle. During Blind Access Mode, the micro doesn't count on the wait/ready signal to terminate the cycle. Instead, the micro always terminates the current transaction in a fixed number of cycles. It then polls the Blind Access Status Register to learn when the current transaction is finished or not. Regardless of the interface mode, there are some common read/write rules which have to be followed in order to carry out the correct transaction.

Because the data path from the Micro Interface to the Host Interface is 32 bit wide, the Micro Interface performs write byte stacking and read byte un-stacking. It also performs byte swapping for the required endianess setting.

For the read case, the TSB12LV41 Micro Interface initiates the read process to the internal link logic after it senses the read request to a new quadlet address generated by the microprocessor. The Micro Interface generates a cycle start (_Cs) to the Host Interface and passes along the read quadlet address. The Host Interface then starts generating a read AccessRequest based on the given read quadlet address, and waits for the AccessResponse being sent back from the link side. AccessRequest and AccessResponse are the handshake signals between the Host Interface and the internal link logic. They are called as non-return to zero type signals which mean they always toggle to its opposite state upon activating. For example, whenever the Micro Interface generates a cycle start _Cs, Host Interface's certain AccessRequest toggles and stays at that logic level until the next cycle start _Cs comes in. Once the AccessResponse comes back, an cycle acknowledge _Ca is generated to the Micro Interface to indicate the current quadlet read process is finished and the whole quadlet data is valid to be read out from the Host Interface's DataOut port. If handshake mode is selected for the Micro Interface via the IOCR register, TSB12LV41 will hold the Microprocessor read transaction cycle until the _Ca comes back from the Host Interface. Then TSB12LV41 releases its Rdy/Wait line to indicate to the microprocessor the current transaction cycle could be terminated. Micro Interface's temporary byte stacking storage holds the whole quadlet provided by the link. The follow up reads to different byte/word position within the same quadlet boundary can obtain the data from the stacking storage rather than access the link logic every time. Therefore the first read to the new quadlet address always takes a little more time than all the other follow up reads. The read access latency to the internal link logic is about 17 clock cycles (for a typical 40.5 MHz TMS320AV7000 clock). If you try to read the same byte/word position inside the same quadlet boundary twice, Micro Interface would think the second read is trying to get the new data therefore it will initiate a new read to the same quadlet again the obtain the new data. Figure 12 shows the Micro Interface's byte unstacking process for read transaction.

For the write case, TSB12LV41's Micro Interface will only initiate the write data transferring when the whole quadlet is filled up which means the first three byte write in byte mode or first word write in word mode only loads part of the quadlet into the temporary byte stacking storage in the Micro Interface. Once TSB12LV41 received the complete quadlet, it then starts generating a cycle start to the Host Interface (_Cs) and also pass along related accessing quadlet address, quadlet data. Then Host Interface starts distributing the quadlet data to the internal link logic based on the given quadlet address with the non-return to zero type handshake signal AccessRequest and AccessResponse. Meanwhile, it generates a cycle acknowledge (_Ca) to the Micro Interface even the AccessResponse doesn't come back. This would allow the Micro Interface to terminate the current transaction and accept a new transaction which can be a new read process or some write process's pre-loading of the first three byte or first word. If the microprocessor is very fast and link core is kind of slow to send back the AccessResponse signal, the Micro Interface could issue a new transaction with _Cs asserted again. At that time, if Host Interface is still busy on the first transaction, it will latch the new transaction and put the Host Interface's state machine into the "WAIT" state without generating another _Ca back to Micro Interface. This would block the third possible transaction if any. When the AccessResponse comes back, the Host Interface starts the new or latched transaction if any. Figure 11 shows the Micro Interface's byte stacking process for write transaction.

Different from the read case, even the handshake mode is selected for the Micro Interface via the IOCR register, TSB12LV41 will not hold the Microprocessor write transaction cycle even when the Host Interface is still working on delivering the quadlet data to the link side. This could gain some performance.

Summarizing above, the first read to the new quadlet address is the one to handshake with the internal link core to obtain the quadlet data. The follow up reads within the quadlet boundary only have to read data from Micro Interface's byte stacking storage. The last write to fill up the whole write quadlet is the one to handshake with the internal link core to transfer the whole quadlet to link core. The first three byte writes or first doublet write only load(s) data into Micro Interface's byte stacking storage.

Another issue needs to be mentioned is, the Mode 9 and Mode 9 Plus things are eliminated from both Micro and Host Interface logic. They are mainly introduced in Versalynx and Gplynx to cover the slow frequency dependent acknowledge (AccessResponse) being sent back from the link side. In some worst case, without this Mode9 stuff, the microprocessor could terminate the write cycle far before the AccessResponse being

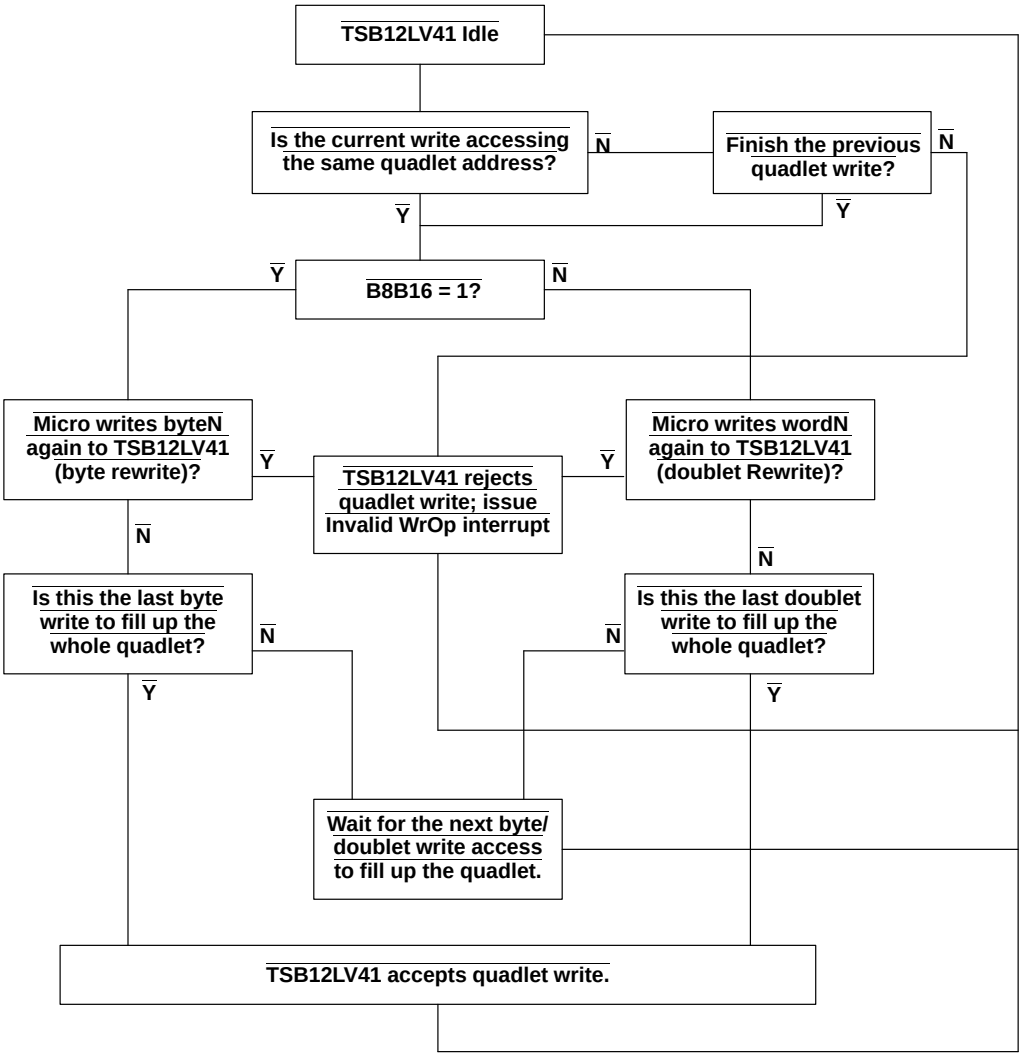
sent back. This could cause the link side to miss the write window. This problem is fixed in TSB12LV41 by extending the write control until the AccessResponse is back.

TSB12LV41 supports any byte/doublet order writes, as long as they are within the same quadlet boundary. If user tries to do either one of the following before he fills up the complete quadlet, the current write will be ignored and an Invalid-RdWr Interrupt will be issued:

- Write to a new quadlet address
- Have a read process:

  WR byte#3 → WR byte #1 → WR byte#2 → RD process → ERROR!
- Write to a byte address within the quadlet twice:

  WR byte#3 → WR byte #1 → WR byte#2 → WR byte#3 → ERROR!



The Read Byte Unstacking flow chart, read operation needs to be carried out very carefully. (Better description Consider the following scenario. If the current transaction is a read to a quadlet address 9'h054 with read to byte0 and byte1 done, you left the current transaction to do something else (maybe accessing another device) then come back to access TSB12LV41 again:

read to 9'h054 byte0 or byte1 will result in the new updated data.

read to 9'h054 byte2 or byte3 will get the held data stored in TSB12LV41 Micro Interface's stacking storage.

read to any address other than 9'h054 will get the new data from that new quadlet address.

have any write access to TSB12LV41 (doesn't matter valid or not) will clear a internal register called previous_read_address. This will cause that the next read to any address always gets the updated data.)

5.3.3 Micro Interface Timing Modes

5.3.3.1 TMS320AV7000 Architecture

The TSB12LV41 is designed to meet the read/write access timing for the TMS320AV7000 architecture. The following table shows the write timing for this interface:

Table 5–2. TMS320AV7000 Write Timing Parameter

PARAMETER	MIN	MAX	UNITS
td1	10		ns
td2	0		ns
td3		5	ns
td4		10	ns
td5	10		ns
td6	10		ns
td7	5		ns
td8	0		ns

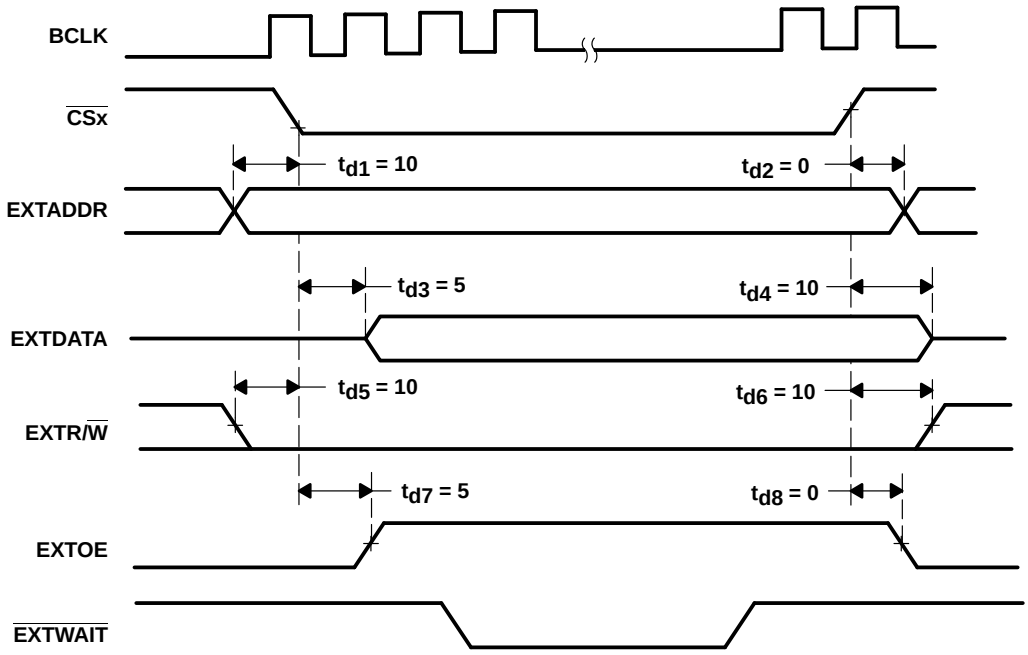


Figure 5–11. TMS320AV7000 Write Timing Diagram

NOTE: BClk is the input clock from the output of *TMS320AV7000*. Its frequency is 40.5 MHz (period about 25 ns).
NOTE: All the signals are inputs to the TSB12LV41, except EXTOE and EXTWAITZ. EXTOE is shown here for reference only. EXTWAITZ is the output wait signal to the *TMS320AV7000* driven by the TSB12LV41.
NOTE: The above notes apply to both the read and write timing diagrams.

For the write case, the TSB12LV41 latches the data at the next clock rising edge after CSxZ goes low, which meets the td3 (5ns) write data setup time requirement. Once the TSB12LV41 is ready to terminate the current cycle, it deasserts EXTWAITZ signal. After certain internal combinational logic delay, the TMS320AV7000 will sample this deassertion by the next rising edge of its CLK40 (same source of BClk). Half cycle later, at the falling edge of CLK40, the TMS320AV7000 deasserts its CSxZ.

Table 5–3. TMS320AV7000 Read Timing Parameter

PARAMETER	MIN	MAX	UNITS
td1	10		ns
td2	0		ns
td3	8		ns
td4	0		ns
td5	10		ns
td6	24		ns
td7	5		ns
td8	0		ns

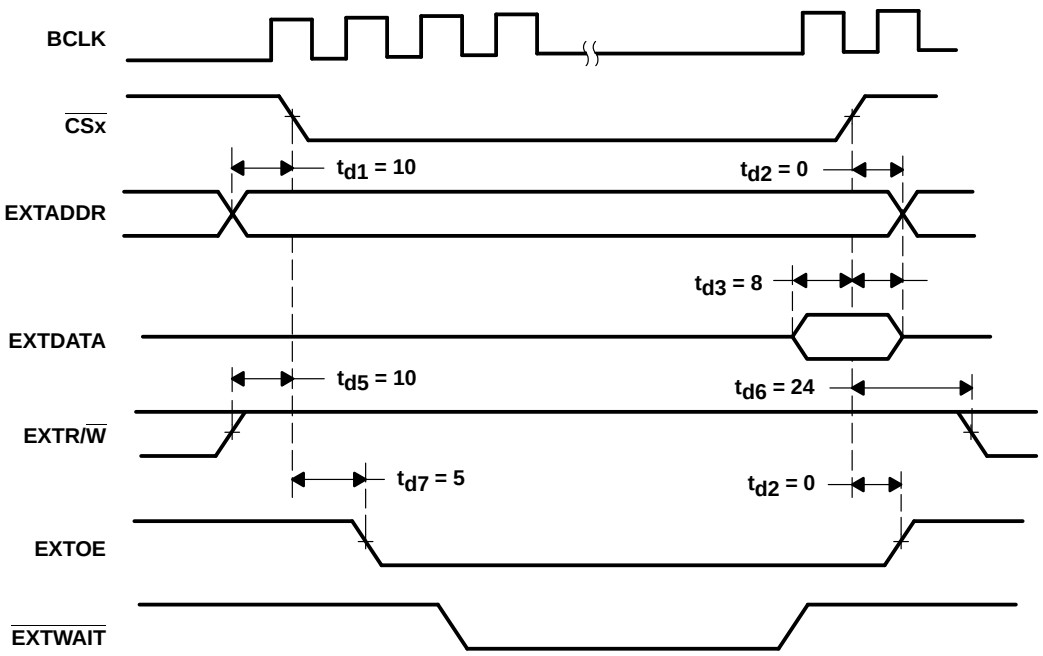


Figure 5–12. TMS320AV7000 Read Timing Diagram

For the read case, once the TSB12LV41 has the read data available, it deasserts EXTWAITZ. The TMS320AV7000 internal combinational logic senses the change. Then the output of this combinational logic is sampled by the next rising edge of its CLK40 and CSxZ will deassert at the same time. TSB12LV41 uses this CSxZ rising edge asynchronously to turn off the data bus. Therefore, turning off the read cycle after EXTWAITZ roughly takes 2 CLK40 cycles.

NOTE: 20 CLK40 Rule for EXTWAITZ signal.

NOTE: Refer to TMS320AV7000 draft spec Rev 3.1 on P.20, it is said that “Since the EXTWAITZ signal has the potential to stall the whole decoding process, the ARM will cap its waiting to 500ns (about 20 CLK40 cycles). Afterwards, the ARM assumes the devices that generated the EXTWAITZ has failed and will ignore EXTWAITZ from then on. Only a software or hardware reset can activate the EXTWAITZ signal again”. Another word, the maximum allowed EXTWAITZ assertion time is 500ns for each chip select, regardless the current transaction is 8–bit wide or 16–bit wide.

NOTE: In detail, once EXTWAITZ has been asserted more than 20 CLK40 cycles, TMS320AV7000 assumes EXTWAITZ fail and would deassert the CSxZ at the next CLK40 cycle. Then TMS320AV7000 would ignore EXTWAITZ generated by all the devices on the bus. From then on, all the devices can not use EXTWAITZ anymore, but TMS320AV7000 can still accept those read/write transactions without using the EXTWAITZ signal (by using the internal programmable wait state register).

NOTE: To avoid catastrophe error in case the LinkCore can not provide data or finish write process within the 20 CLK40 cycles, TSB12LV41 Micro Interface state machine is designed to abort the transaction and deassert the EXTWAITZ signal when TSB12LV41’s internal logic can’t finish the transaction after 17 BClk cycles.

NOTE: EXTWAITZ to be recognized by TMS320AV7000 at the beginning of the transaction.

NOTE: According to TMS320AV7000 spec, the EXTWAITZ signal must assert before the number of wait state (can be set up in TMS320AV7000’s wait state register) expires. The default wait state number is 3.

NOTE: TSB12LV41 is designed to always assert its wait line McRdy (low true in this mode) at the second BClk rising edge after it samples the falling edge of CSxZ.

NOTE: EXTWAITZ (TSB12LV41’s McRdy) Sharing Issue.

NOTE: Because TMS320AV7000 only has one EXTWAITZ input signal line, TSB12LV41 has to share this pin with other devices on the same extension bus. Since EXTWAITZ has been defined as an open–drain type in TMS320AV7000, users have to set the IOCR.RdyPushPull bit to zero to get the correct signal level output from TSB12LV41. TSB12LV41 does not provide any on–chip pull–up resistor for this pin.

NOTE: INT (interrupt) Output Line Sharing Issue.
NOTE: TMS320AV7000 have dedicated INT lines, therefore no sharing of this signal is needed. TSB12LV41 outputs normal totem–pole signal level for this pin.
NOTE: Also, the application is allowed to write a “1” to certain bit of TSB12LV41’s Interrupt Register to clear the interrupt, without using TMS320AV7000’s EXTACK signal (interrupt acknowledge).

5.3.4 Blind Access Mode

The Blind Access Mode is designed for slower Micros like Intel’s 8051 which does not have the external wait/ready line handshake signal.

Writes to the address SRES (Software Reset Register, @Addr 1FCh) will generate a internal SW reset. This SW reset will be prolonged internally for sixteen 1394 clocks (25MHz => approx. 640 ns). This 640 ns can be used by the host to do garbage collection.

Two Registers Involved in Blind Access Mode:

BASTAT (Blind Access Status Register, @Addr 1F0h)

BAHR (Blind Access Holding Register, @Addr 1F4h)

5.3.4.1 Access to BASTAT and BAHR will not activate read or write requests from/to other module within the TSB12LV41.

5.3.4.2 Reads from BASTAT

IF the bit BAcmp is set, it indicates that the current ongoing blind access is finished. For Blind Read, it means the required data from the request address is available in the BAHR register. For Blind Write, it means the write data has been delivered to the request address.

5.3.4.3 Blind Writes:

Just write to TSB12LV41. Blind Write still has to follow the general write rule, except it does not use RDY/*WAIT as the hand shake signal with CPU.

For consecutive writes, check the BAcmp bit and wait till previous access finished.

If the time period of consecutive write is bigger as write latency, then the BAcmp bit doesn’t need to be checked.

The first 3 bytes (byte access mode) or first 1 word (word access mode) write is very quick, normally takes only 3 cycles for each write. When the write of the last byte or word to fill up the whole quadlet comes in, the micro state machine sets the internal signal “BAccess_Busy”, it then starts delivering the whole quadlet to the address requested although it still terminates the write in 4 cycles. The BAccess_Busy signal is the inverse of the BAcmp bit only during the HW read/write to internal logic is ongoing.

By polling the BAcmp bit in BASTAT register, CPU can then detect the current blind access is finished or not.

Before the BAcmp bit is set or BAccess_Busy is cleared, except reads to BASTAT and BAHR registers, all other reads and all the writes are not allowed. Once the whole quadlet has been filled up with the valid writes, a write to the internal logic will be initiated and can not be stopped except by assert a device reset. If CPU mistakenly issues a new write or invalid read before BAcmp is set, a write/read error interrupt will be generated and this new write/read will be aborted.

5.3.4.4 Blind Reads

First read will result in a dummy value. It will however start a read HW procedure and the BAccess_Busy signal will be set.

The BAcmp bit in BASTAT can be checked for procedure finish status.

If the time period of consecutive read is bigger as read latency, then BAcmp bit

doesn't need to be checked (something else can be done during this time).

Before the BAcmp bit is set or BAccess_Busy is cleared, except reads to BASTAT and BAHR registers, all other reads and all the writes are not allowed. Once the HW read procedure starts, it can not be stopped except by assert a device reset. If CPU mistakenly issues a new write or invalid read before BAcmp is set, a write/read error interrupt will be generated and this new write/read will be aborted.

A follow-up read to BAHR can obtain the requested data after the BAcmp is set.

5.3.4.5 BAcmp bit clear

Normal Read/Write Cases:

Once BAcmp bit has been set, reading to either BASTAT or BAHR will cause the BAcmp bit to be cleared, regardless the current Blind Access is read or write. Because BAcmp bit could be set at any time, even during the read to the BHSTAT register, TSB12LV41's Micro Interface has ensured that:

If the _Ca (cycle acknowledge) from TSB12LV41's Host Interface module comes back before the first BClk rising edge inside chip select window of the current read cycle to BASTAT, the current read will return the status that BAcmp has been set and BAcmp bit will be cleared after the read.

If the _Ca comes back after the first BClk rising edge, but still inside the current read cycle to BASTAT, the current read will return the status that BAcmp has not been set. BAcmp bit will be set, held and will not be cleared by the current read to BASTAT.

Exception (needed to be re-simulated): read to BAHR will clear the BAcmp anyway as long as _Ca comes back before or at the current read BAHR cycle.

For those consecutive read/write whose accessing time interval is longer than the read/write latency (and a new Blind Write/Read is issued without reading to BASTAT to check BAcmp status), the trailing edge of the Csen (TSB12LV41 internal signal) is the time to clear the BAcmp. That means, for blind write, the last write to fill up the whole quadlet will clear the BAcmp (the first postedge of BClk after _Mccs goes low). For blind read, the first read transaction will clear the BAcmp.

5.3.4.6 Special Notes

Blind Read and Blind Write accesses cannot be nested into each other.

Only for TMS320AV7000 in 16-bit Access Mode in Read case:

when the first follow-up read to BAHR finished which clears the BAcmp bit, a new read to a new address is allowed even before CPU reads out the next word (doublet) from the BAHR register. CPU can take advantage of the time slot between the end of the new Blind Read cycle and the moment that the next BAcmp bit is set to grab the second doublet resulted from the previous Blind Read process out from the BAHR. -1/14 7:30PM simulation shows result OK! But real world TOO DANGEROUS! Decide not to recommend à may get 2nd read data instead of first read data. Also considering effect to clear the next BAcmp à simulation shows the read to first read to BAHR after new blind read is ok, the second read to BAHR (follows above) clears the BAcmp bit and gets the new data.

Only for TMS320AV7000 in 8-bit Access Mode or Intel 8051:

In 8-bit access mode, doesn't matter the previous blind access is read or write, a new blind write is allowed even the BAcmp for the previous blind access does not come back. This is due to the fact that the Csen which initiates the internal full quadlet data transferring will not be generated until the last byte of the quadlet comes in. So the latency from starting a new quadlet write to actually initiate the Csen is about 15 clocks which is at least less or equal to the worst case MP/MC–IF latency. (TBD: Intel8051. Double check and verify for the Intel 8051 case – worst case latency may not be 15 cycles).

There are four registers located inside the TSB12LV41's Micro Interface domain: IOCR (I/O Control Register), BASTAT (Blind Access Status Register), BAHR (Blind Access Holding Register), and SRES

(Software Reset Register). Accessing them in the Blind Access Mode doesn't need to go across the host2link synchronization boundary, therefore, the access is immediate and no status check to BASTAT is necessary (don't expect BAcmp bit to be set!)

User has to be very careful about the following scenario in the Blind Access Mode: if you first issued a blind read to certain register's byte0, you left for something else (to access device other than TSB12LV41) without reading the contents returned back in the BAHR register. Now you come back to issue a new blind read to the same previous register's byte address other than byte0. The final result is that you can only get the held data stored in the BAHR register and no new read process to the TSB12LV41's internal logic will be generated, because the general read rule for TSB12LV41 still applies. The similar result applies to Blind Read in word mode.

6 Interface Timing

6.1 Writes

Writes to BDIF are in bytewide mode (/BDIEN Burst)

6.1.1 MPEG2 Data

BDIF2 is used to mark 1st byte of M–cell

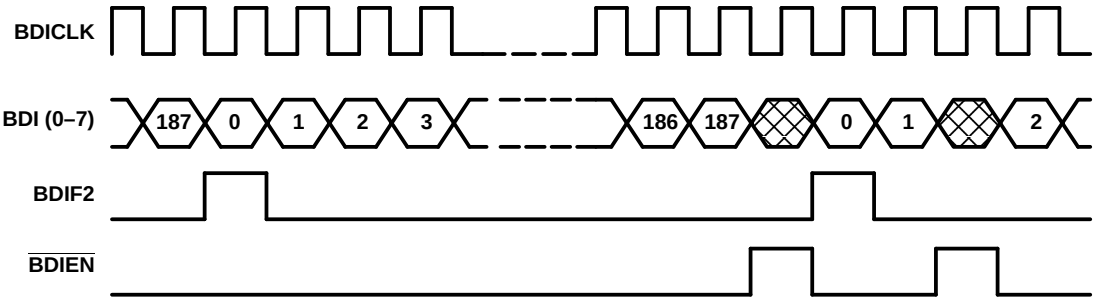


Figure 6–1.

I/O status: BDICLK=in; BDI[7..0]=in; BDIF[2..0] =in; /BDIEN=in; BDIMode=000; BDIF1=low; BDIF0=high; BDIClk max frequency= 20.25MHz;

6.1.1.1 “I” Data

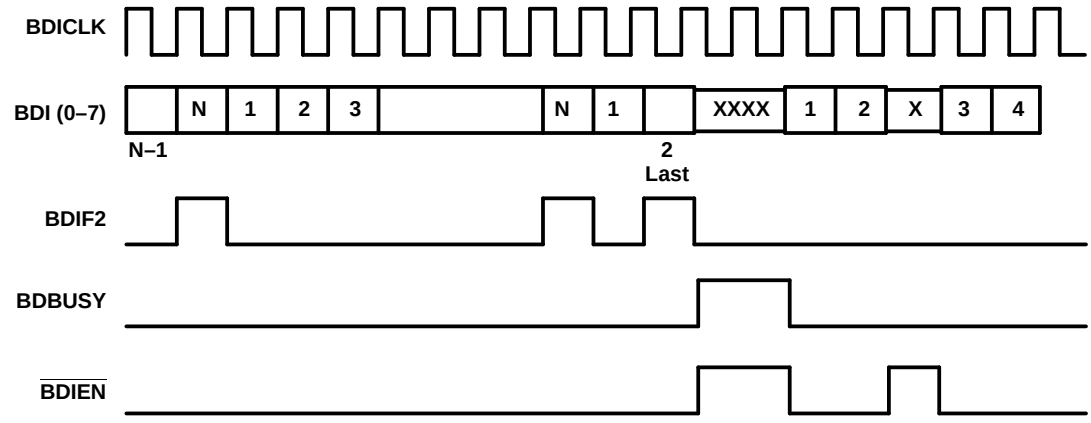


Figure 6–2.

I/O status: BDICLK=in; BDI[0..7]=in; BDIF[0..2] =in; BDIEN=in; BDIF1=high; BDIF0=low; BDIMode=000; BDICLK max frequency = 20.25 MHz

6.1.1.2 “A” Data

BDIF2 is used to mark last cell of a A-packet. The timing is the same as “I” packet above.

I/O status: BDICLK=in; BDI[7..0]=in; BDIF[2..0] =in; BDIEN=in; BDIF1=high; BDIF0=high; BDIMode=000; BDICLK max frequency = 20.25 MHz

6.1.1.3 Mixed mode

If A-, I- and M- data is to been written to the BDIF, then all three BDIF lines need to be encoded as qualifier for the data. Switching between A, I and M traffic is only allowed on quadlet boundaries.

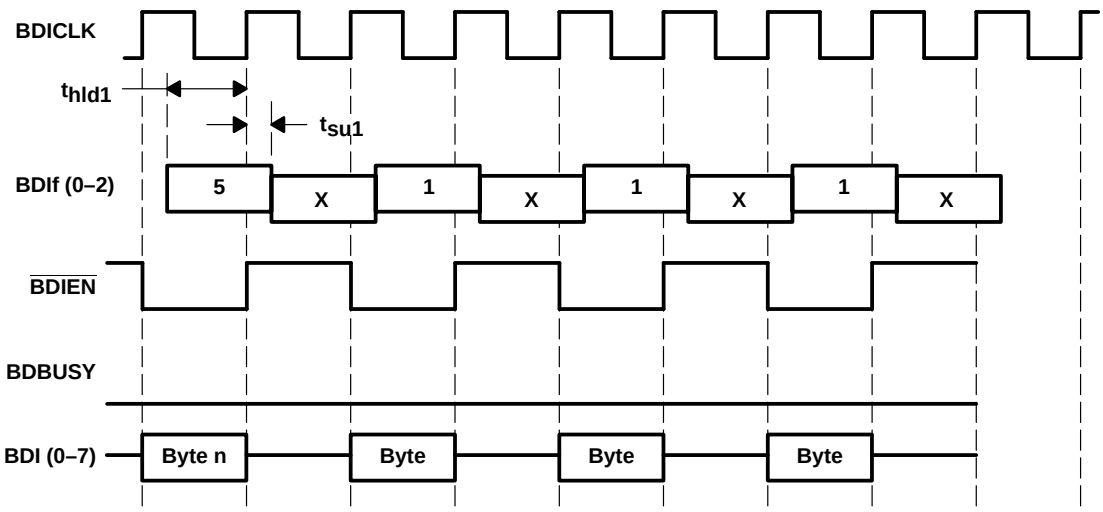


Figure 6–3. $\overline{\text{BDIEN}}$ Gated Writes to BDIF in Bytewide Mode

I/O Status: BDI[7:0]=in; BDIF[2:0]=in; BDIMode=000; BDIF[1]=low; BDIF[0]=high; BDICLK max frequency= 40.5 Mhz. Max Data rate 20.25 MB/s.

6.1.2 Serial MPEG2 Data

BDIF2 is used to mark 1st bit of 1st byte of an M-cell.

BDIMode = 100; BDICLK max frequency=80MHz. BDIF1=low; BDIF0=high; for MPEG2 accesses

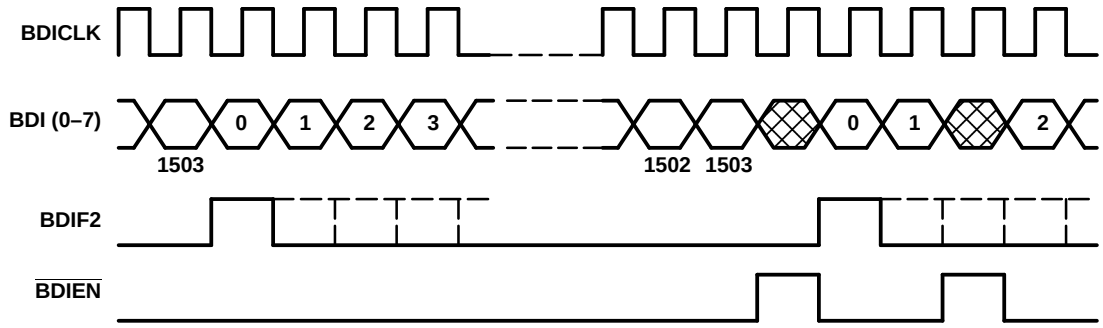


Figure 6–4.

6.1.2.1 “A” Data

BDIF2 is used to mark 1st bit of last byte of an A-packet

BDIMode = 100; BDICLK max frequency=80MHz.; BDIF1=high; BDIF0=high; for “A” accesses

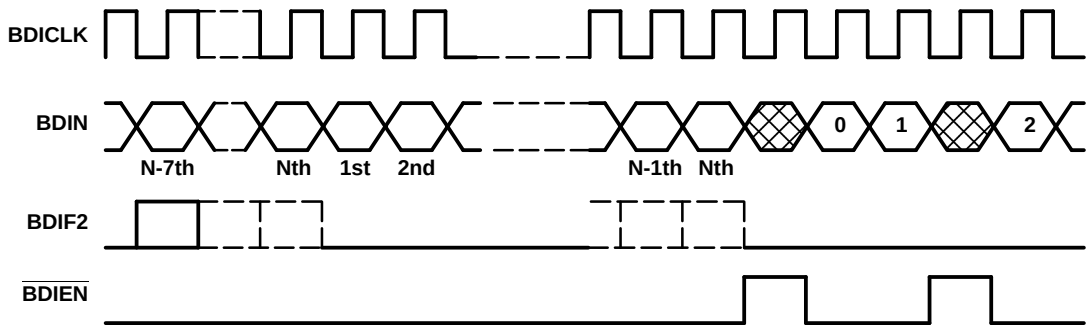


Figure 6–5.

6.1.2.2 “I” Data

BDIF2 is used to mark 1st bit of last byte of an I–packet

BDIMode = 100; BDICLK max frequency=80MHz.; BDIF1=high; BDIF0=low; for “I” accesses

The timing is the same as for “A” packets.

6.1.2.3 Mixed mode:

This is the same as in bytewide mode.

6.2 Reads

Check BDAVAIL for available data.

6.2.1 MPEG2 Data

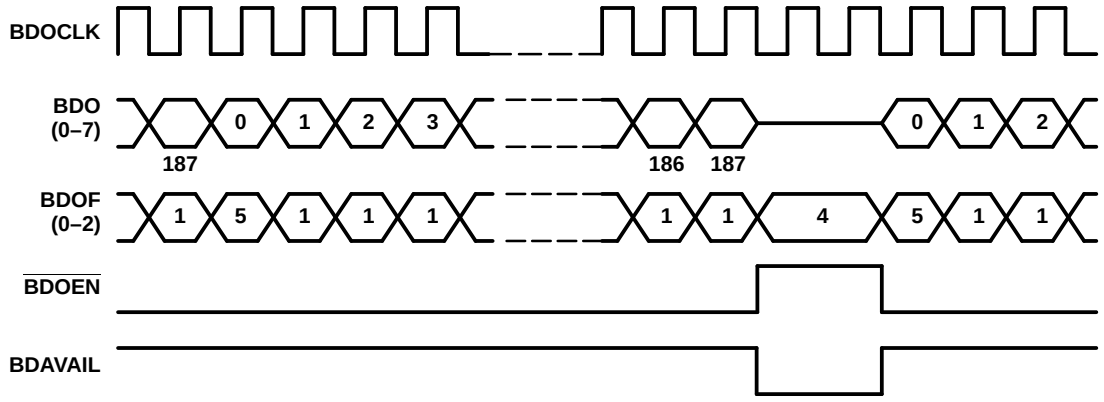


Figure 6–6.

BDICLK max frequency = 20.25MHz; BDOMode=00;

6.2.1.1 “I” Data

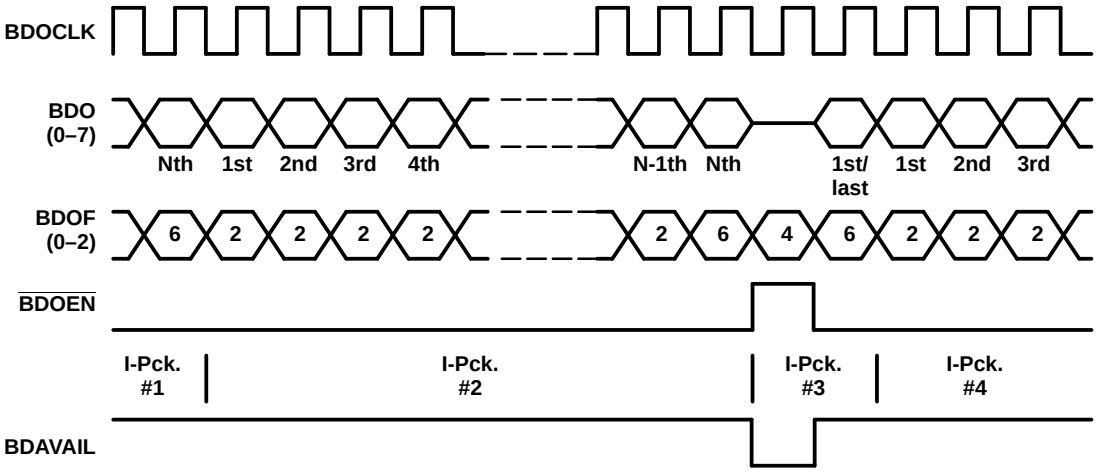


Figure 6–7.

BDICLK max frequency = 20.25MHz; BDOMode=00;

6.2.1.2 “A” Data

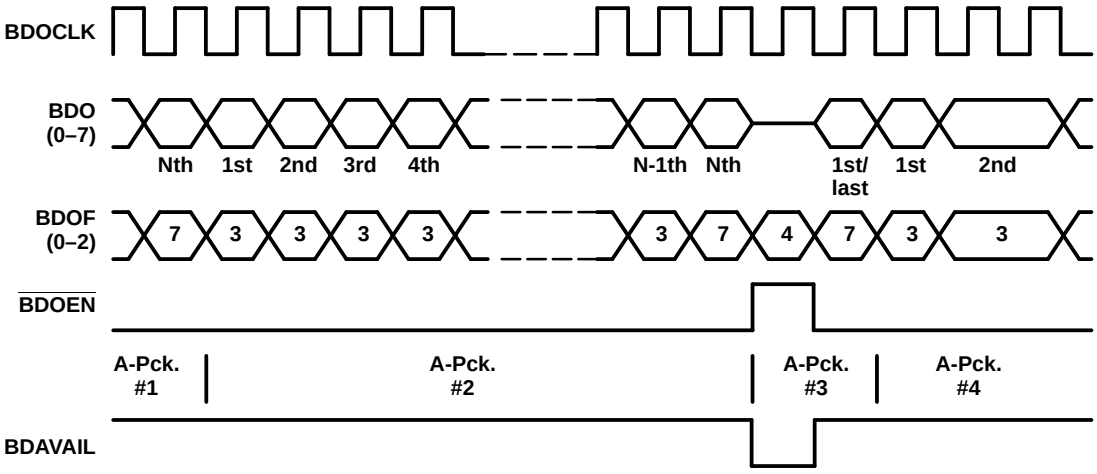


Figure 6–8.

BDICLK max frequency = 20.25MHz; BDOMode=00;

6.2.1.3 Mixed mode

If A-, I- and M-data is supplied interleaved the BDOF lines need to be decoded to see which data is available. If several Rx–FIFOs contain data, the data is prioritized by the FIFO and is as follows:

1. MPEG2 formatted data
2. I-packets
3. A-packets

6.2.1.4 Gated /BDOEN Reads from BDIF in bytewide mode

BDOMode = 00; BDOCLK max frequency = 40.5 Mhz

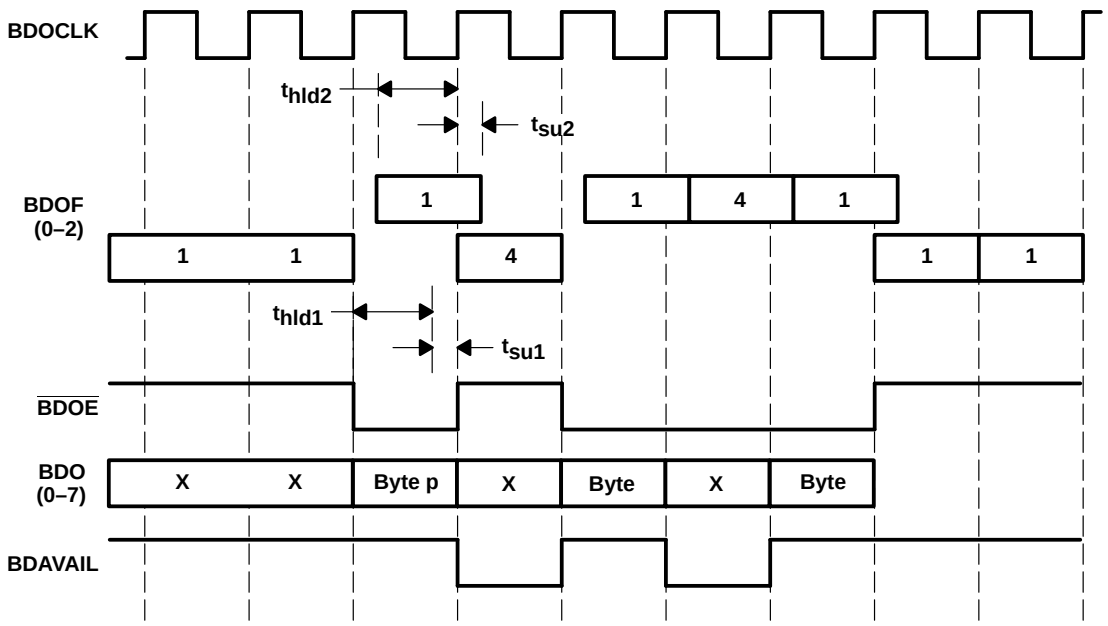


Figure 6–9.

Reads from BDIF in bitwide mode

Up to the first eight bits of the separator byte are marked as start of M-cell, minimum requirement is the first bit.

6.2.2 MPEG2 Data

check BDAVAIL for available data. Max BDOCLK frequency= 80MHz. BDOMode=10;

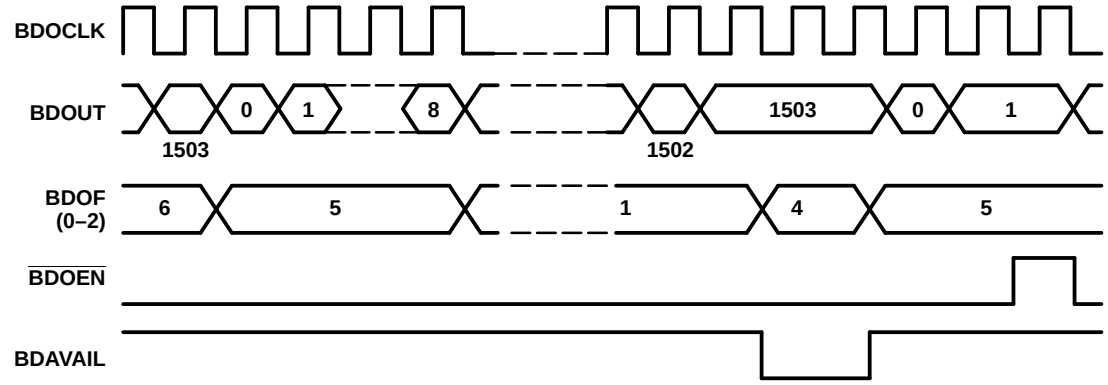


Figure 6–10.

6.2.2.1 “A” & “I” packets

The timing is the same as for M-cell except last byte is marked.

6.2.2.2 Mixed mode

Requires full decoding of BDOF lines. The priority is the same as in bytewide mode if several data available simultaneously. Standard timing as in bitserial mode.

6.3 Bidirectional Bus Modes

BDIF[2:0] and BDI[7..0] are bi-directional. Polarity of control signals are programmable.

6.3.1 Bidirectional Mode

BDIMode=001,011; BDIEN used to enable input. BDICLK max frequency for BDIMode=001 is 20.25Mhz and data can be written/read on every clock. Max BDICLK frequency for BDIMode=011 is 40.5 Mhz and data is written/read every other clock

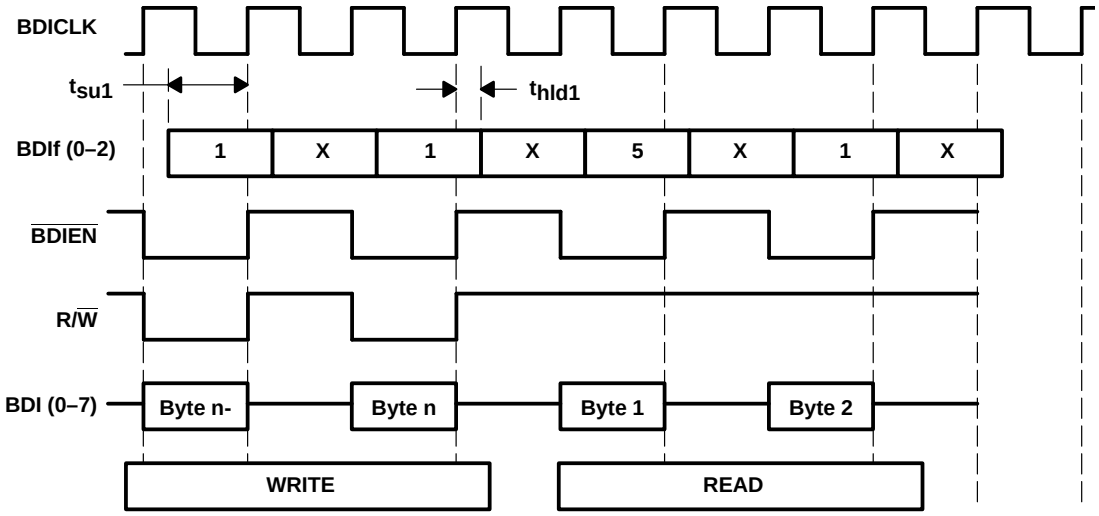


Figure 6–11.

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6.3.2 TSB12LV41 Bidirectional Mode

BDIMode=010; W used to enable write input. R uses to enable reads. BDICLK max frequency is 40.5Mhz and data can be written/read on every other clock.

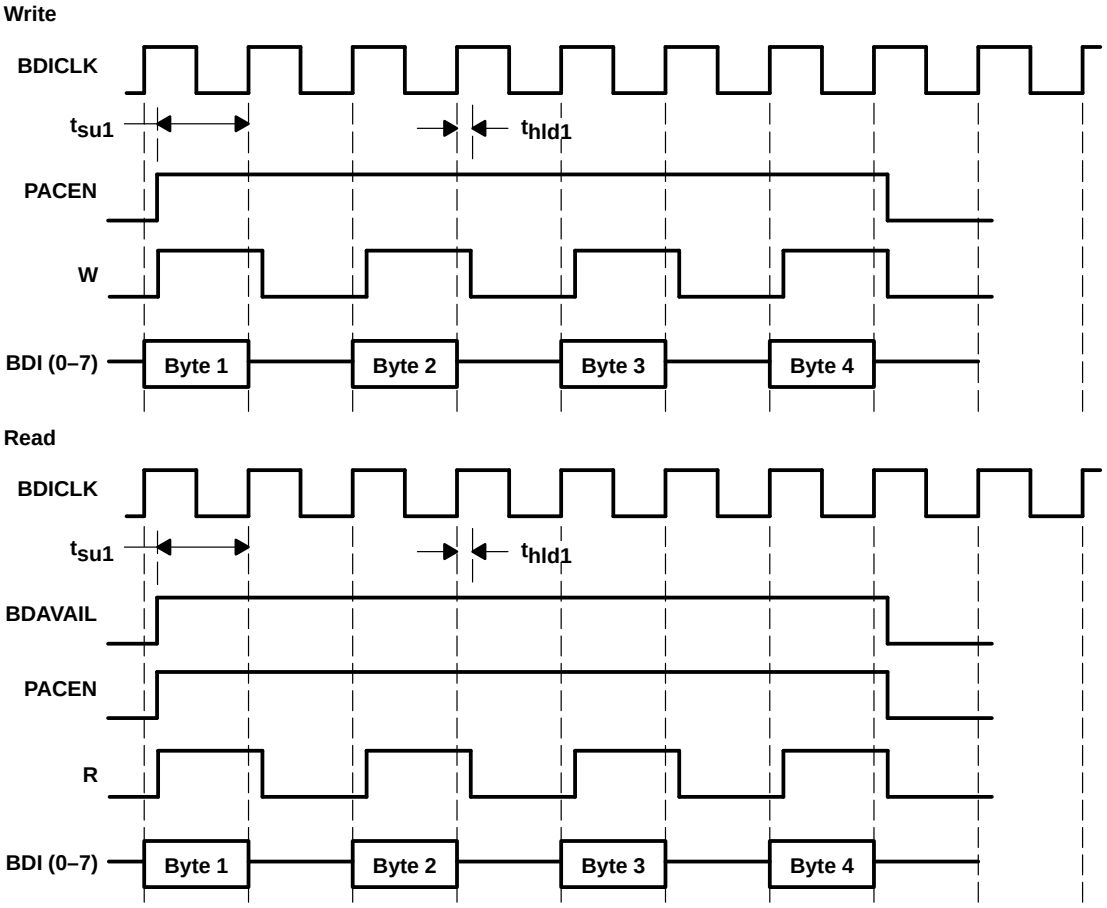

Figure 6–12.

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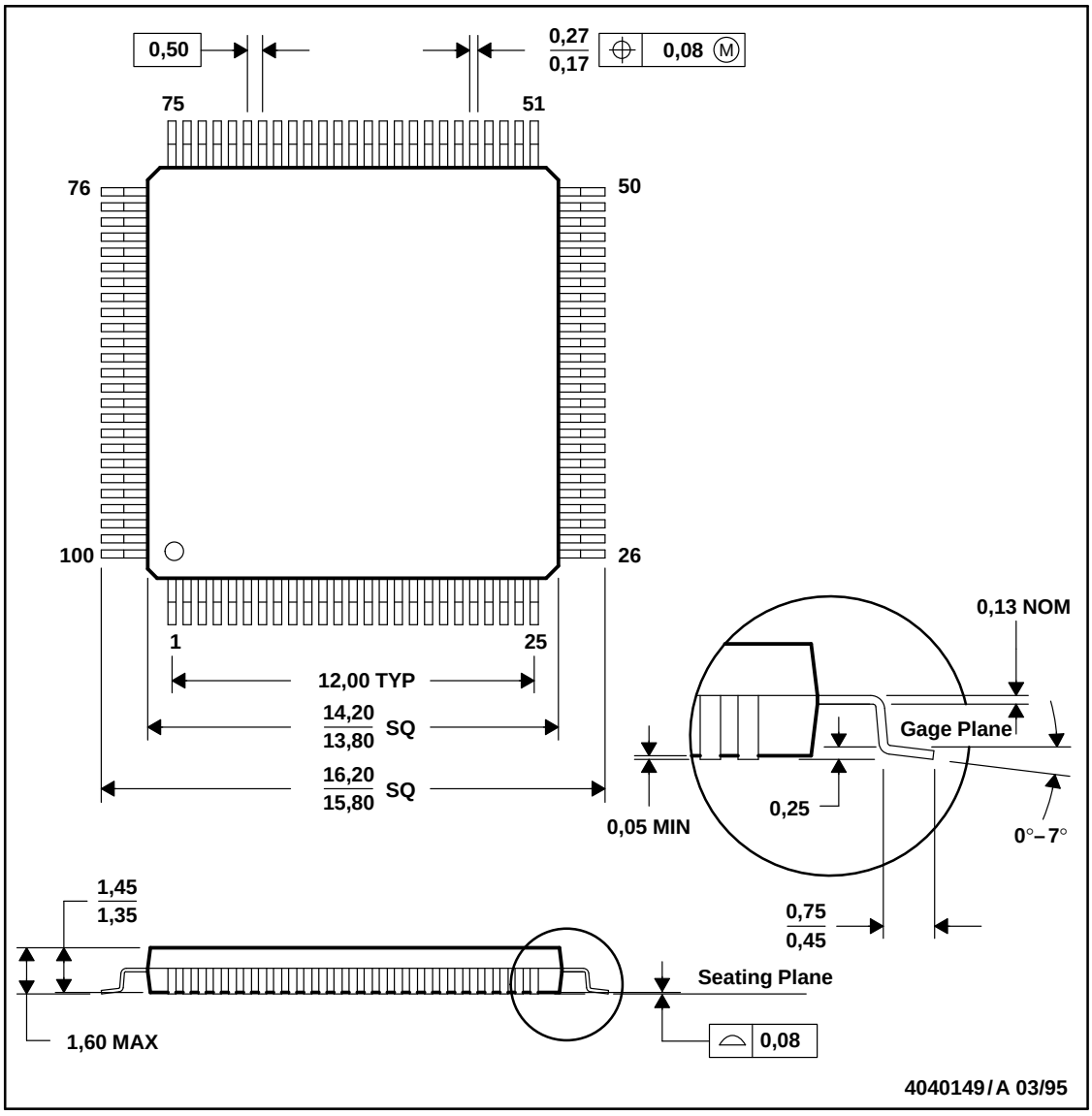
7 Mechanical Information

The TSB12LV41 is packaged in a high-performance 100-pin PZ package. The following shows the mechanical dimensions of the PZ package.

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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