Understanding the TSB12LV4x Bulky Data Interface

APPLICATION REPORT: SLLA017

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Abstract

This document describes the operation and features of the Bulky Data Interface (BDIF) of the TI TSB12LV4x 1394 Link Layer Controller device family. The Bulky Data Interface provides a data transfer interface for use with high speed peripherals. The interface can provide sustained data rates up to 160Mbit/s. In addition, the BDIF has access to an 8Kbyte FIFO which supports isochronous, asynchronous and MPEG2/DV data transfers. This interface supports bidirectional transmit and receive of DSS/DVB/DV formatted data on 1394 as defined by the IEC61883 specification (depending on individual device capability). Asynchronous and non IEC61883 formatted isochronous data transmit and receive are also supported by this interface.

This document assumes the reader is familiar with the hardware and terminology of the IEEE 1394-1995 standard and the TI TSB12LV4x family of devices. Further information and data sheets can be obtained via the Internet at http://www.ti.com/sc/1394.

Product Support

Related Documentation

Further information and data sheets can be obtained via the Internet at http://www.ti.com/sc/1394.

The following documents are available via links from the TI 1394 external web page:

- Errata List for TSB12LV21, TSB12LV21A, TSB12C01A, TSB11C01, TSB11LV01, TSB21LV03, TSB21LV03A, and TSB14C01.
- Data sheets for all TI 1394 devices.
- Information on designer kits, including TSBKPCI, TSBKPCITST, TSKBGPLYNX, TSBKBACKPL, TSBKPRPHRL, TSBKMPEG2.

The IEEE 1394-1995 standard is available for purchase at http://standards.ieee.org/catalog/index.html

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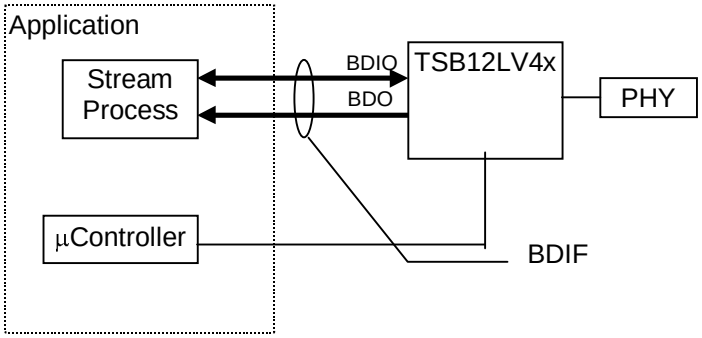
Introduction

The Bulky Data Interface or BDIF is a pair of ports supported by the TSB12LV4x Link Layer controllers. The BDIF is the physical medium by which autonomous streams of different types are piped to an application that uses the TSB12LV4x. A system diagram is shown below:

Figure 1. Bulky Data Interface (BDIF) System Diagram



Since the BDIF has two ports, data can be full duplex. One port is bidirectional and the other is output only. Each port has its own independent clock, control signals, and modes of operation. The ports can operate in asynchronous clock domains.

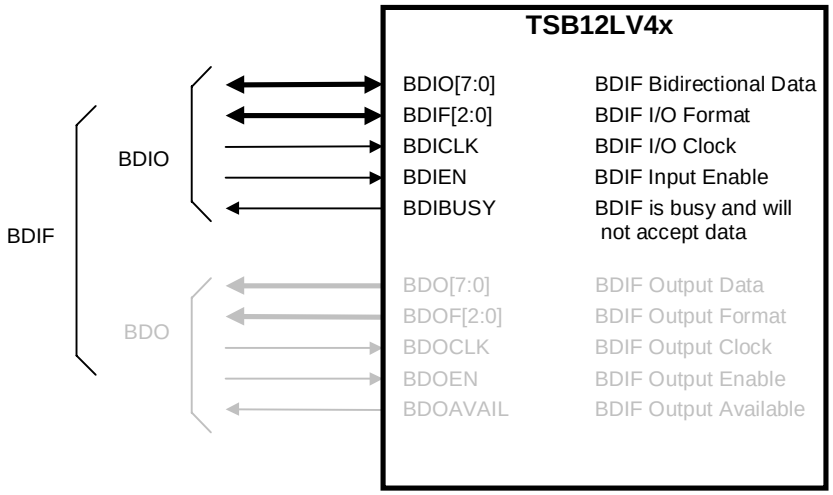
The BDIF handles three stream types:

1) Asynchronous
2) Isochronous
3) MPEG2/DSS/DV (a special Isochronous type, depending on device)

These stream types are identified by a Format bus bound to the port. The encodings on the Format bus also frame packets within the stream. BDIF[2..0] is the Format bus for BDIO and BDOF[2..0] is the Format bus for BDO.

A more detailed look at the BDI's signaling is in order. Even though the two ports (BDIO and BDO) have some control signal and clock dependencies, we first look at them separately.

Figure 2. BDIO Port

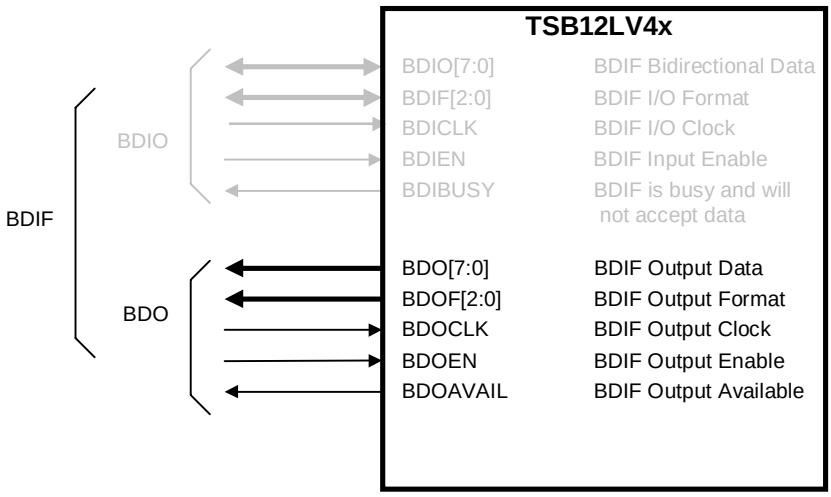


The signals of the bidirectional port (BDIO) have the following characteristics.

Table 1. Bidirectional Port (BDIO) Signal Characteristics

BDIO Signal Name	Driver Type	Description
BDIO[7:0]	I/O	Bidirectional BDI port (can be configured for input only). BDI[7] = MSB and BDI[0] = LSB.
BDIF[2:0]	I/O	Bidirectional BDIO Format (can be configured for input only). 000 Reserved 001 A byte of an MPEG2/DSS/DV cell 010 A byte of an unformatted Isochronous packet 011 A byte of an Asynchronous packet 100 Idle 101 First byte of an MPEG2/DSS/DV cell 110 Last byte of an unformatted Isochronous packet 111 Last byte of an Asynchronous packet
BDICLK	I	BDIO data input clock
BDIEN	I	BDI Enable: Read or write enable for BDIO port.
BDIBUSY	O	Signals busy condition on BDIO for writes. This signal goes high when the FIFO being written to is full. When BDIBUSY is high, writing to the full FIFO is disabled.

Figure 3. BDO Port



The signals of the unidirectional output only port (BDO) have the following characteristics.

Table 2. Unidirectional Output Only Port (BDO) Signal Characteristics

BDIO Signal Name	Driver Type	Description
BDO[7:0]	O	Unidirectional BDO port. BDO[7] = MSB and BDO[0] = LSB.
BDOF[2:0]	O	Unidirectional BDO Format. 000 Reserved 001 A byte of an MPEG2/DSS/DV cell 010 A byte of an unformatted Isochronous packet 011 A byte of an Asynchronous packet 100 Idle 101 First byte of an MPEG2/DSS/DV cell 110 Last byte of an unformatted Isochronous packet 111 Last byte of an Asynchronous packet
BDOCLK	I	BDIO or BDO data output clock
BDOEN	I	BDO Enable: Qualifies data on BDO for reads Read/Write* control for BDIO when it is bidirectional
BDOAVAIL	O	Signals data is available on BDO and/or BDIO for reads.

BDIF Control Register (D8h) Configuration : The BDIF is programmed by writes to the BDIF control register. This register is located at address D8h in the TSB12LV4x microcontroller address space. The register format and bit definitions are shown below.

Figure 4. BDIF Control Register Configuration

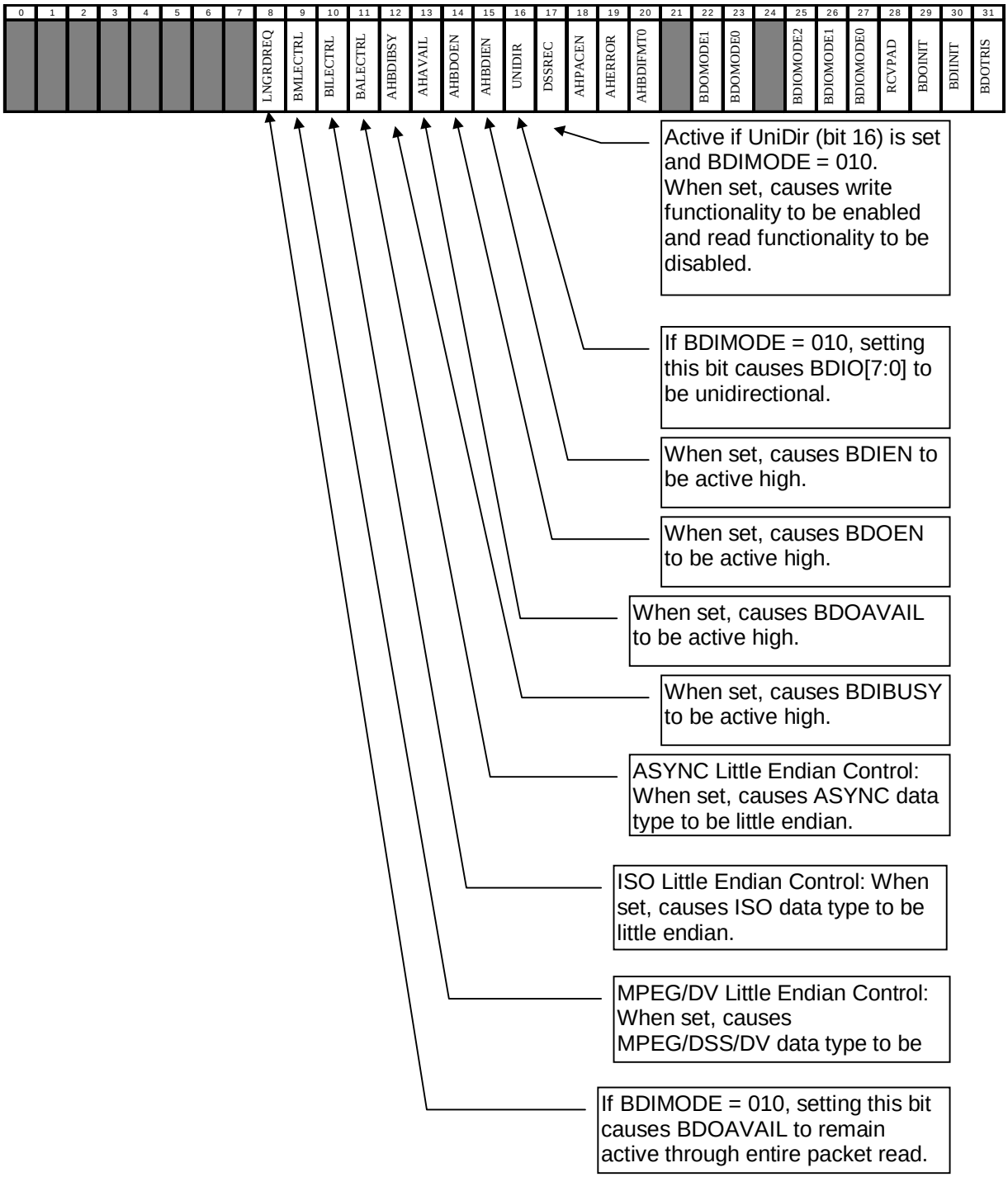
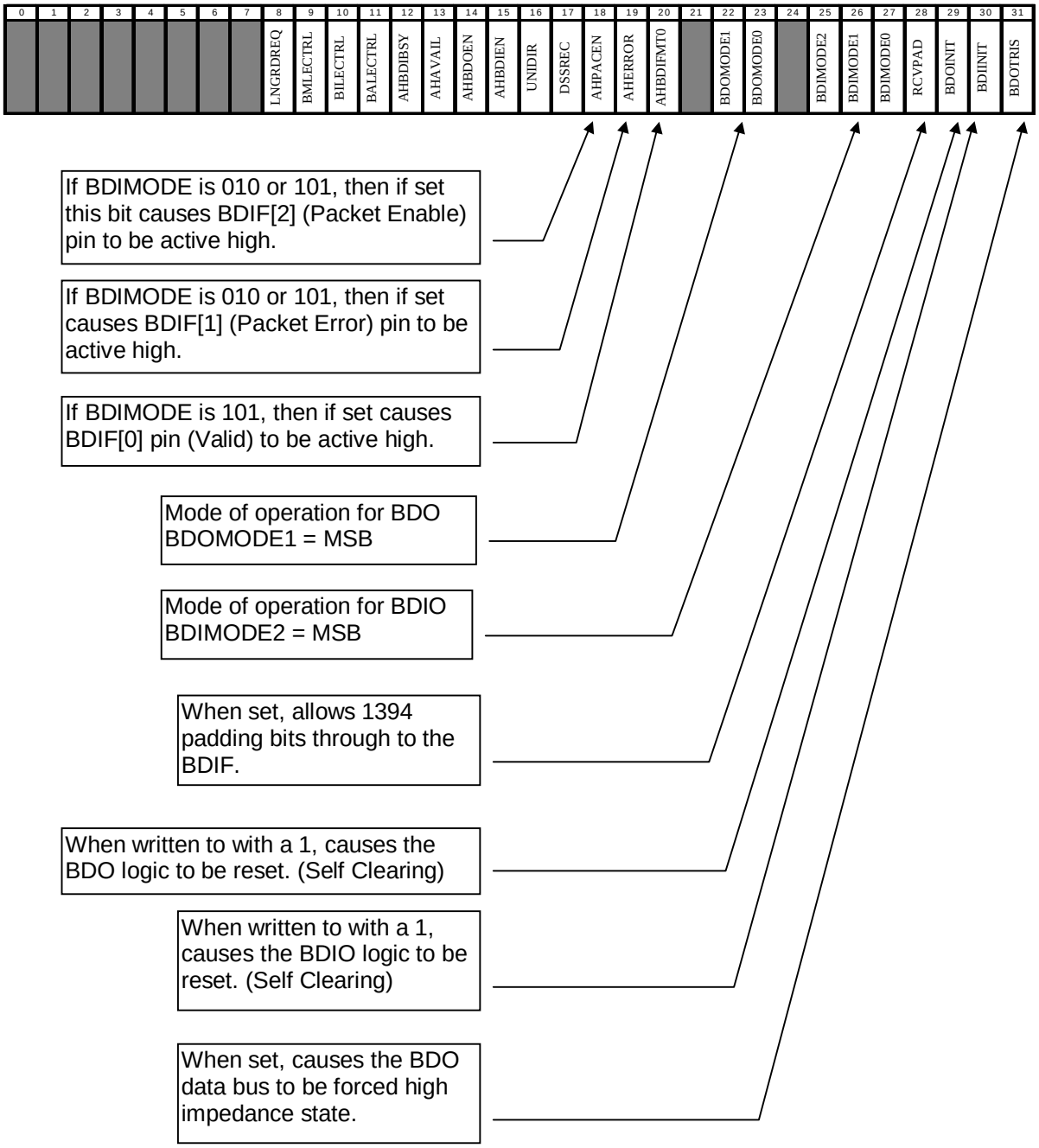


Figure 5. BDIF Control Register Configuration (cont'd)



Modes of the Bulky Data Interface (BDIF)

The BDIF has eight valid modes of operation. These modes are selected using the BDIMODE and BDOMODE fields of the BDIF control register. The table below shows the basic features of each mode.

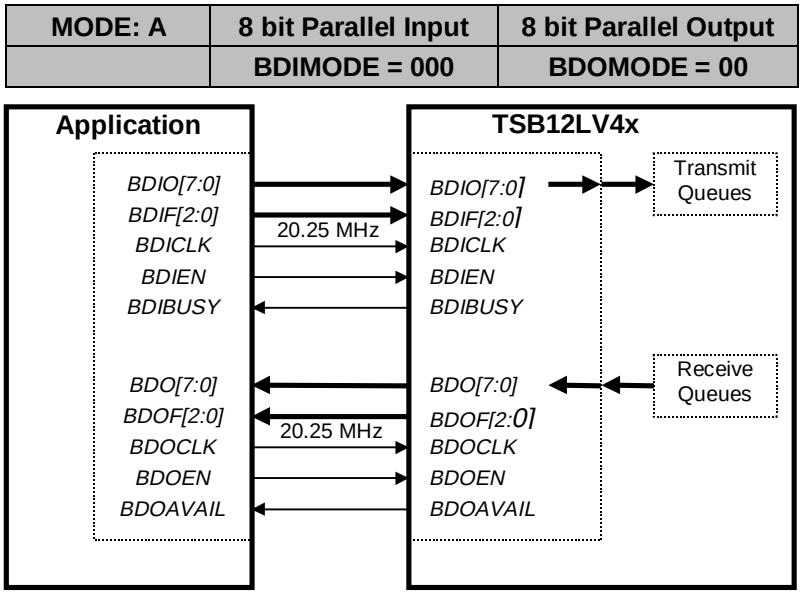
Table 3. Modes of the BDIF

MODE	A	B	C	D	E	F	G	H
BDIMODE	000	000	000	101	101	001	010	011
BDOMODE	00	01	11	00	11	00	00	00
Data Input	BDIO	BDIO	BDIO	BDIO Async	BDIO Async	BDIO	BDIO	BDIO
Data Output	BDO	BDO	BDO Async	BDO	BDO Async	BDIO	BDIO	BDIO
Data Bus	2	2	2	2	2	1	1	1
Duplex	full	full	full	full	full	half	half	half
Data Input Clock MHz	20.25	20.25	20.25	NClk	NClk	20.25	40.5	40.5
Data Output Clock MHz	20.25	20.25	NClk	20.25	NClk	20.25	40.5	40.5
Data Throughput Mbyte/sec (max)	20 Write 20 Read	20 Write 20 Read	20 Write 10 Read	10 Write 20 Read	10 Write 10 Read	20.25	20.25	20.25
Control signal use:								
BDIEN	✓	✓	✓	✓	✓	✓	✓	✓
BDIBUSY	✓	✓				✓		✓
BDOEN	✓		✓	✓	✓	✓	✓	✓
BDOAVAIL	✓	✓	✓	✓	✓	✓	✓	✓

Detailed descriptions of each mode are contained in the sections that follow.

NOTE:
These eight modes are the ONLY valid mode settings for the TSB12LV4x BDIF.

Figure 6. Mode A Application Block Diagram



In this mode, the BDIO bus is input only. The BDO bus is output only. There are 2 data busses that connect the BDIF with Bulky Data FIFOs. These buses go to the transmit and receive queues.

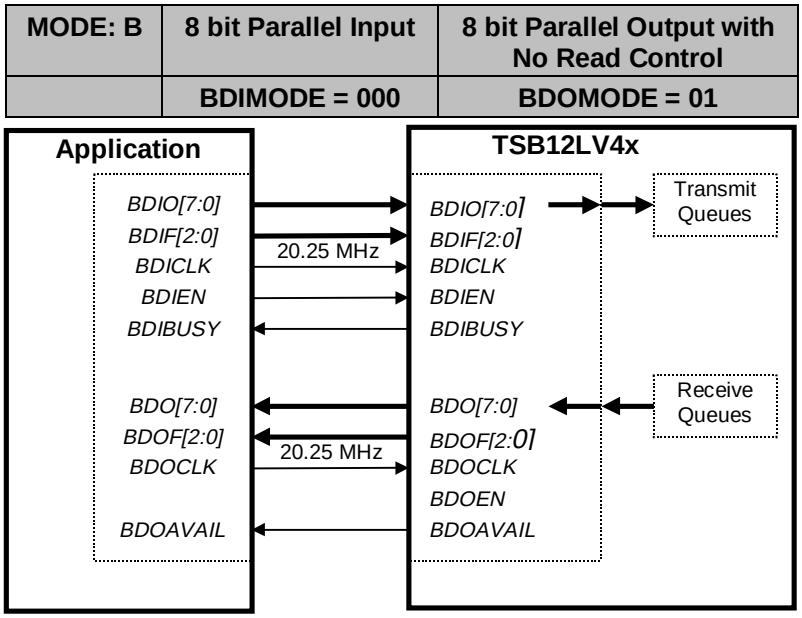
This mode is synchronous for both input and output. Both of the data input (BDICLK) and output (BDOCLK) clocks run at 20.25 MHz. The BDIF expects new data every clock period.

The BDIF operates in full duplex mode. In this mode, the BDIF can receive data at the BDIO port and transmit data from the BDO port simultaneously. With input/output clock speeds of 20.25 MHz, this allows a maximum throughput of 40.5 Mbyte/s.

BDIEN qualifies data on BDIO for writes. BDIBUSY signals a busy condition on BDIO for writes.

BDOEN qualifies data on BDO for reads. BDOAVAIL signals data is available on BDO for reads.

Figure 7. Mode B Application Block Diagram

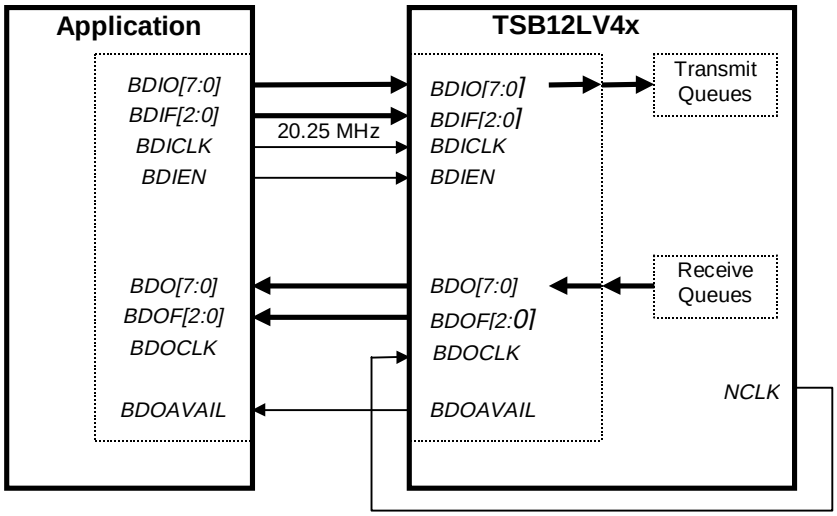


The data input and output for this mode are similar to the MODE A mode. The BDIO is input only. BDO is output only. The clock speeds, data rates, and full duplex capability are the same as for MODE A. The BDIF expects new data every clock period.

The difference between this mode and MODE A is the absence of BDOEN, the bulky data output enable. Since MODE B does not use BDOEN, data is continuously output to the host whether or not it can accept the data. The main advantage of this mode is that no signal is required by the host to transmit. However, if the host FIFO is full, data may be lost.

Figure 8. Mode C Application Block Diagram

MODE: C	8 bit Parallel Input	8 bit Parallel Output (Asynchronous)
	BDIMODE = 000	BDOMODE = 11



The BDIO is input only. The output on the BDO bus is asynchronous only. The data input for this mode at the BDIO port is for synchronous. This mode provides 2 data buses to the transmit and receive FIFOs. The mode operates in full duplex mode.

The data input clock runs at 20.25MHz. Since BDO is asynchronous, an application will not provide BDOCLK. In this case, an internal clock, NCLK, can be used to sample the BDO port. This clock rate is 24.576MHz (or SCLK/2). NCLK is available at STAT0 or STAT3.

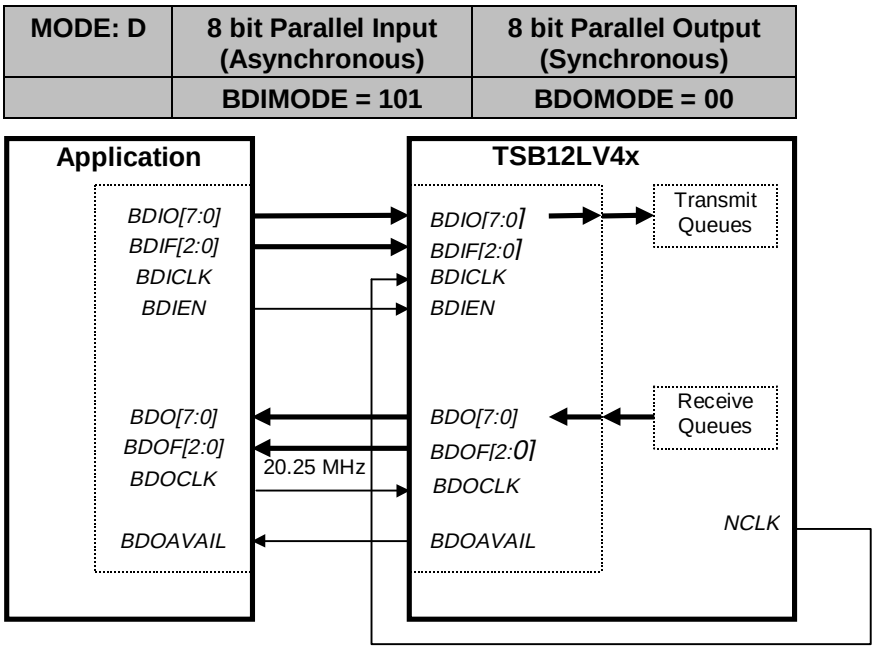
NOTE:
Driving BDOCLK with NCLK is not required. The user may drive BDOCLK with another external clock.

The maximum data throughput is 20 Mbytes/s for write and 10 Mbytes/s for read.

There is no BDBUSY available in this mode. This means that there is no way for the TSB12LV4x to signal to the application that it is busy and can not accept any more data.

In this mode, new data is expected every clock period on BDIO.

Figure 9. Mode D Application Block Diagram



The BDIO is input only. The data input for this mode at the BDIO bus is for asynchronous. The output on the BDO bus is synchronous. This mode provides 2 data buses to the transmit and receive FIFOs. It operates in full duplex mode.

Since BDIO is asynchronous, an application will not provide BDICLK. In this case, an internal clock, NCLK, can be used to sample the BDIO port. This clock rate is 24.576, or (SYSCLK/2). NCLK is available at STAT0 or STAT3.

NOTE:

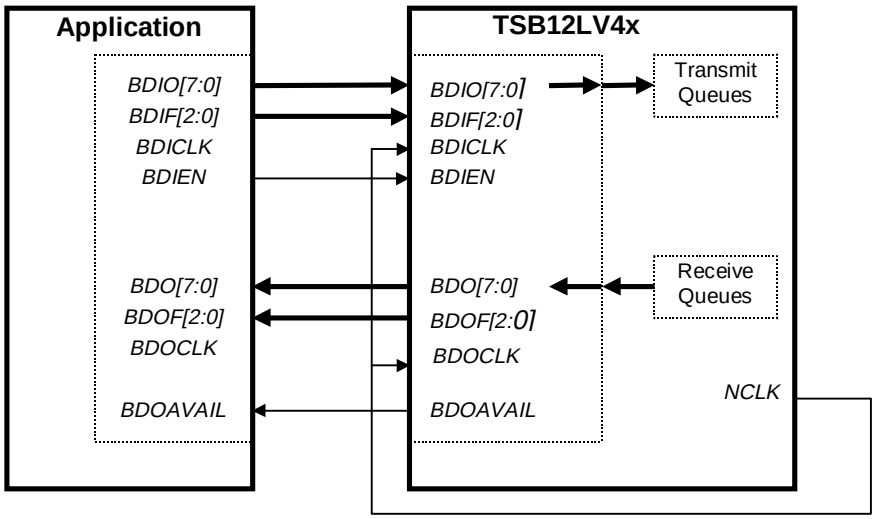
Driving BDICLK with NCLK is not required. The user may drive BDICLK with another external clock.

This mode has the maximum data throughput capability of 10Mbyte/s for a write and 20Mbyte/s for a read.

There is no BDBUSY available in this mode. This means that there is no way for the TSB12LV4x to signal to the application that it is busy and can not accept any more data.

Figure 10. Mode E Application Block Diagram

MODE: E	8 bit Parallel Input (Asynchronous)	8 bit Parallel Output (Asynchronous)
	BDIMODE = 101	BDOMODE = 11



The BDIO is input only. The data input for this mode at the BDIO bus is asynchronous. The data output at BDO is also asynchronous. This mode provides two data buses, one for the transmit and one for the receive FIFO. This mode operates in full duplex.

Since both BDIO and BDO are asynchronous, an application will not provide BDICLK or BDOCLK. In this case, an internal clock, NCLK, may be used to sample both the BDIO and BDO port. This clock rate is 24.576 MHz, or SYSCLK/2. NCLK is available at STAT0 or STAT3.

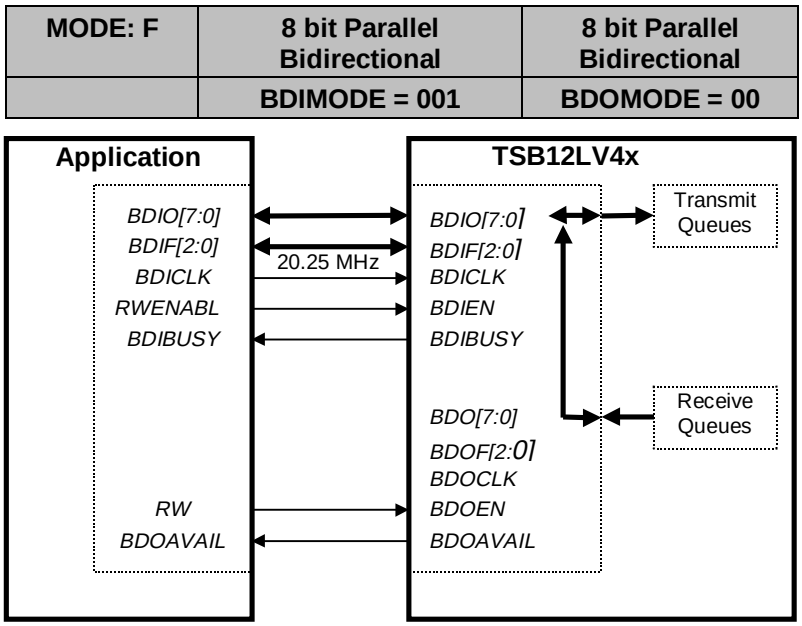
NOTE:

Driving BDICLK or BDOCLK with NCLK is not required. The user may drive BDICLK or BDOCLK with another external clock.

This mode has a maximum data throughput capability of 10Mbyte/s for a write and 10Mbyte/s for a read.

There is no BDBUSY available in this mode. This means that there is no way for the TSB12LV4x to signal to the application that it is busy and can not accept any more data.

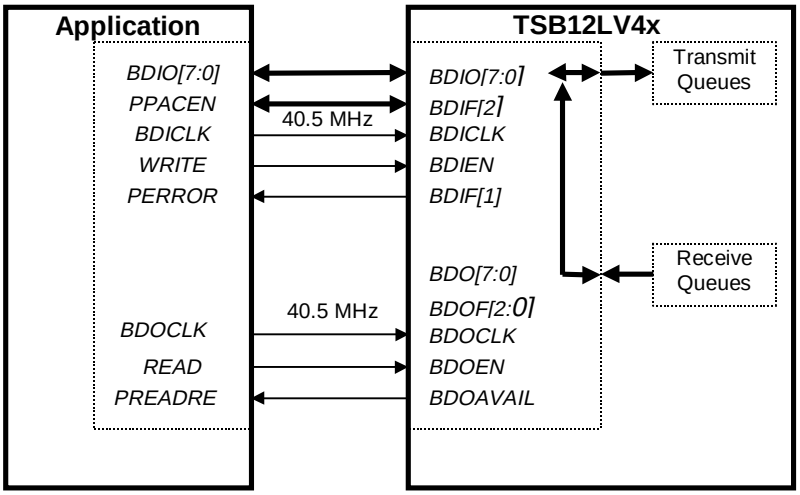
Figure 11. Mode F Application Block Diagram



This is a bidirectional mode. The data input and data output share the BDIO port. BDOEN is a Read/Write* control in bi-directional mode. The device in this mode operates in half duplex. The data input/data output clocks are both at 20.25MHz. The BDIO expect new data every clock cycle in this mode.

Figure 12. Mode G Application Block Diagram

MODE: G	8 bit Parallel Double Clocked Bidirectional Bus with Separate R/W Strobe.	8 bit Parallel Double Clocked Bidirectional Bus with Separate R/W Strobe.
	BDIMODE = 010	BDOMODE = 00



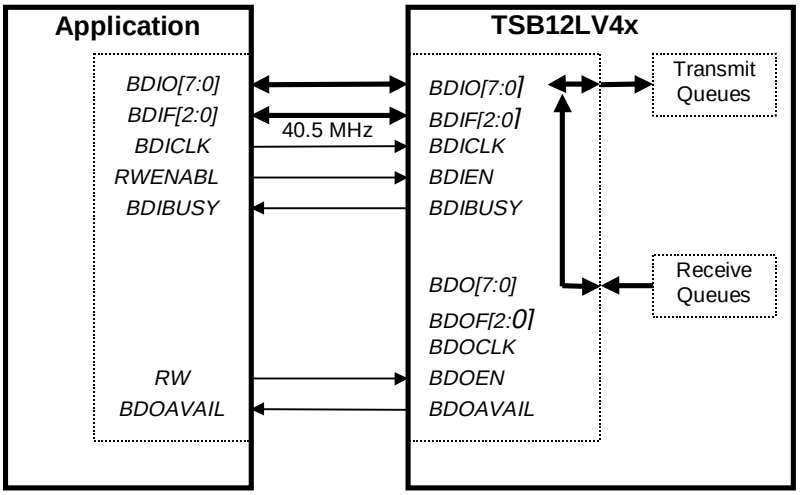
This is a bidirectional mode. All of the bus inputs and outputs go through BDIO. The BDO port is unused. In this mode BDIEN is used as write control. BDOEN is used as read control.

In this mode, BDIF[1] is used as a packet error signal (PERROR) and BDIF[2] is used as a packet framing signal (PPACEN).

The BDIF can only write to and read from MPEG/DSS BDIF FIFOs. It is designed to interface directly with Texas Instruments TMS320AV7000 series of MPEG2 and DSS decoders using the BSkyB specification. However, it can interface with other devices using the Serial Synchronous Interface (SSI) configuration defined in the DVB CATV/SMATV headends specification.

Figure 13. Mode H Application Block Diagram

MODE: H	8 bit Parallel Double Clocked Bidirectional Bus with Separate R/W Strobe.	8 bit Parallel Double Clocked Bidirectional Bus with Separate R/W Strobe.
	BDIMODE = 011	BDOMODE = 00



This mode is bidirectional. All inputs and outputs to the BDIF occur at the BDIO port. BDOEN is used as a Read/Write* control in bi-directional mode. Both the input and output are clocked at 40.5 MHz. This mode operates in half duplex. New data is expected every other clock period.