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Galvanic Isolation of the IEEE 1394-1995 Serial Bus

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Galvanic Isolation of the IEEE 1394-1995 Serial Bus

Burke Henehan
Dan Yaklin
Bob Gugel
Jeff Akgul

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Galvanic Isolation of the IEEE 1394-1995 Serial Bus

ABSTRACT

The IEEE 1394-1995 cable is designed to transmit and receive data at various data rates and to also source and/or sink power to/from remote nodes. This allows remote nodes that either do not have their own source of power or have their power turned off to continue to function in the IEEE 1394-1995 network. The signaling in 1394 requires that every physical layer on a bus be operating at the same ground potential. In a 1394-1995 system, this is accomplished by connecting all physical layer grounds together using the 1394 cable logic ground (the ground wire of the cable power and ground pair). Because all nodes are connected together, this has the potential to form ground loops when not galvanically isolated. Also, since multiple nodes connected together are allowed to source power simultaneously, grounding problems are created in the system when galvanic isolation between nodes is not handled properly. This application report describes the three isolation requirements set forth in IEEE 1394-1995 for:

- Shield termination
- Cable power isolation
- Signal isolation

All three of these requirements must be met to ensure isolation.

The majority of this application report is dedicated to describing the Texas Instruments (TI™) patent-pending signal isolation method.

1 The Need for Isolation

Due to the distances allowed between nodes in an IEEE 1394-1995 network, different nodes on the network could be plugged into grounded (3-prong) ac outlets that are in different ground domains, commonly referred to as green-wire grounds. The potential difference between these grounds can be dc, ac at 60 Hz along with its harmonics, and various noise components. If these grounds are connected together by the 1394 cable logic ground or shielding, a ground loop exists and current flows in the cable. These ground-loop currents can have several negative effects on the 1394 network, which include degradation of data signals on the cable, excessive EMI from the cable, ground currents high enough to damage components in the system, and if the potential difference is large enough, a personal shock hazard. Figure 1 illustrates how different ground domains might be connected together in two nodes of an IEEE 1394-1995 network.

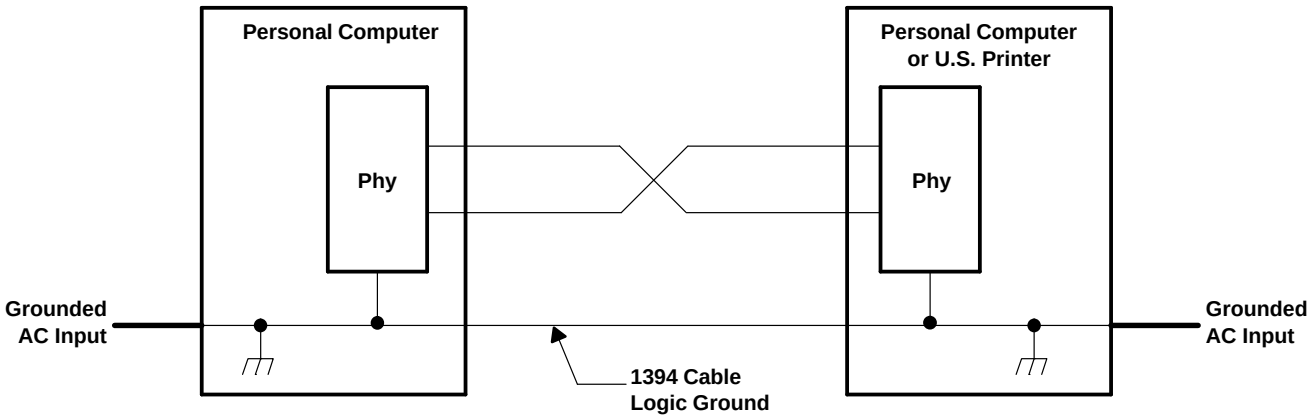

Figure 1. No Galvanic Isolation

To avoid these problems there are three electrical isolation requirements described in Annex A.4 of the IEEE 1394-1995 standard that should be followed for proper operation and safety of the serial bus. These requirements deal with the isolation of cable shielding, signal line isolation, and cable power line isolation.

Some systems may not have a signal-line or power-line isolation problem. Consumer equipment typically uses a two-prong plug and a transformer in the power supply. For this type of system, isolation is inherent in the isolated power supply and no further isolation is required (see Figure 2). Since the IEEE 1394-1995 network is not connected to a green-wire ground, different ground domains do not pose a problem.

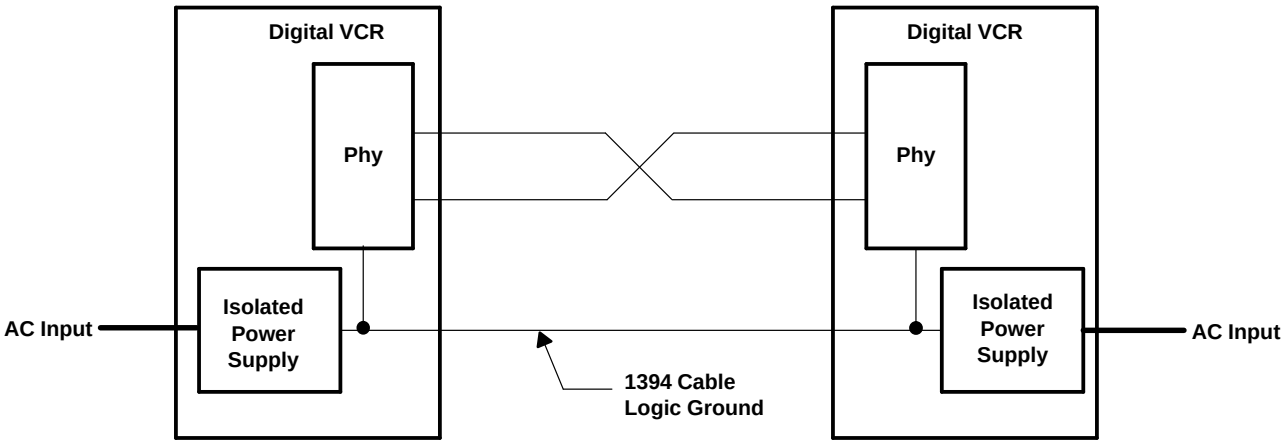

Figure 2. Isolation By Way of Isolated Power Supplies

When a camera is powered only from the IEEE 1394-1995 cable, it would not normally be connected to a green-wire ground and probably would not require that isolation be incorporated in this particular configuration (see Figure 3).

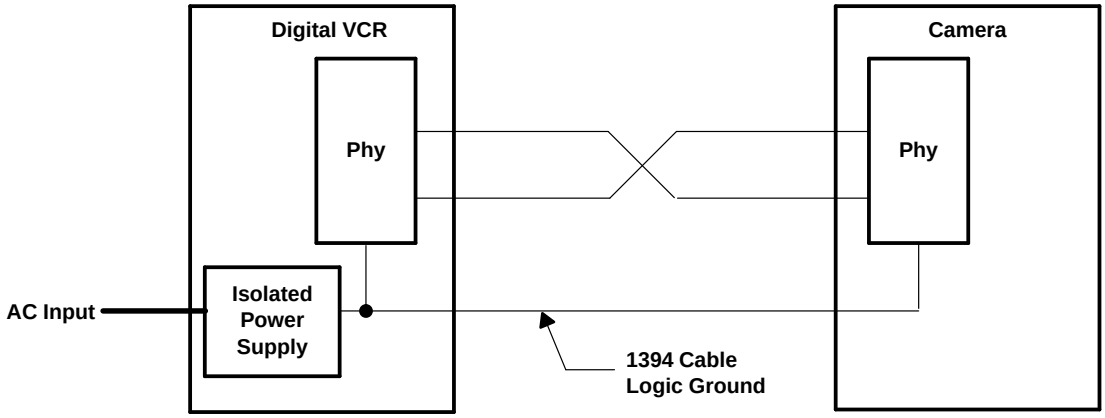

Figure 3. Leaf Node Not Requiring Isolation

In the case of a peripheral that is battery powered and using the 4-signal wire audio/video cable where there is no cable-power logic ground or cable-power wire in the 1394 cable, it probably would not be connected to a green-wire ground. However, there is still the potential that a battery-powered or cable-powered leaf node may be grounded through some accessory device. Figure 4 shows an example of a potential problem where the shield isolation is not implemented.

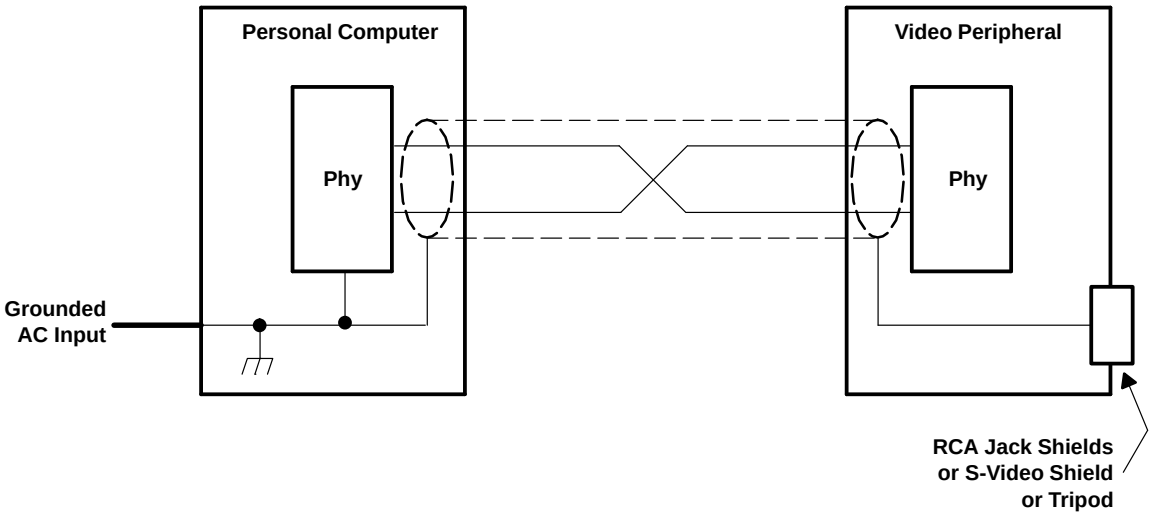

Figure 4. Potential Problem Due To Shield Termination

Each node implementing the IEEE 1394-1995 standard must be looked at to determine if isolation is required for that particular application. When it is required, the following section should help in determining the best method of achieving the required isolation. There are three electrical isolation requirements described in Annex A.4 of the IEEE 1394-1995 standard; isolation of cable shielding, cable-power isolation, and signal-line isolation. The cable shield isolation is specified in paragraph 4.2.1.4.8 of the IEEE 1394-1995 standard and an example is shown in Figure 3–30 of that standard. Terminating the shield of a cable nominally consists of connecting the outer cable shield to chassis ground through a parallel combination of a 1-MΩ resistor and a 0.1-μF capacitor to provide a relatively high-impedance coupling at low frequencies and a relatively low-impedance coupling at high frequencies. Cable power is described in section A.4 of the IEEE 1394-1995 standard with explanation and examples. Basically, when a node sources cable power, it must use an isolating supply to provide that power. This supply can be dedicated to supplying cable power (see DC/DC Converter in Figure 5) or it can be the isolated supply for the entire node (see Figure A–2 of the IEEE 1394-1995 specification and Figure 2 in this document). The remainder of this application report addresses signal-line isolation.

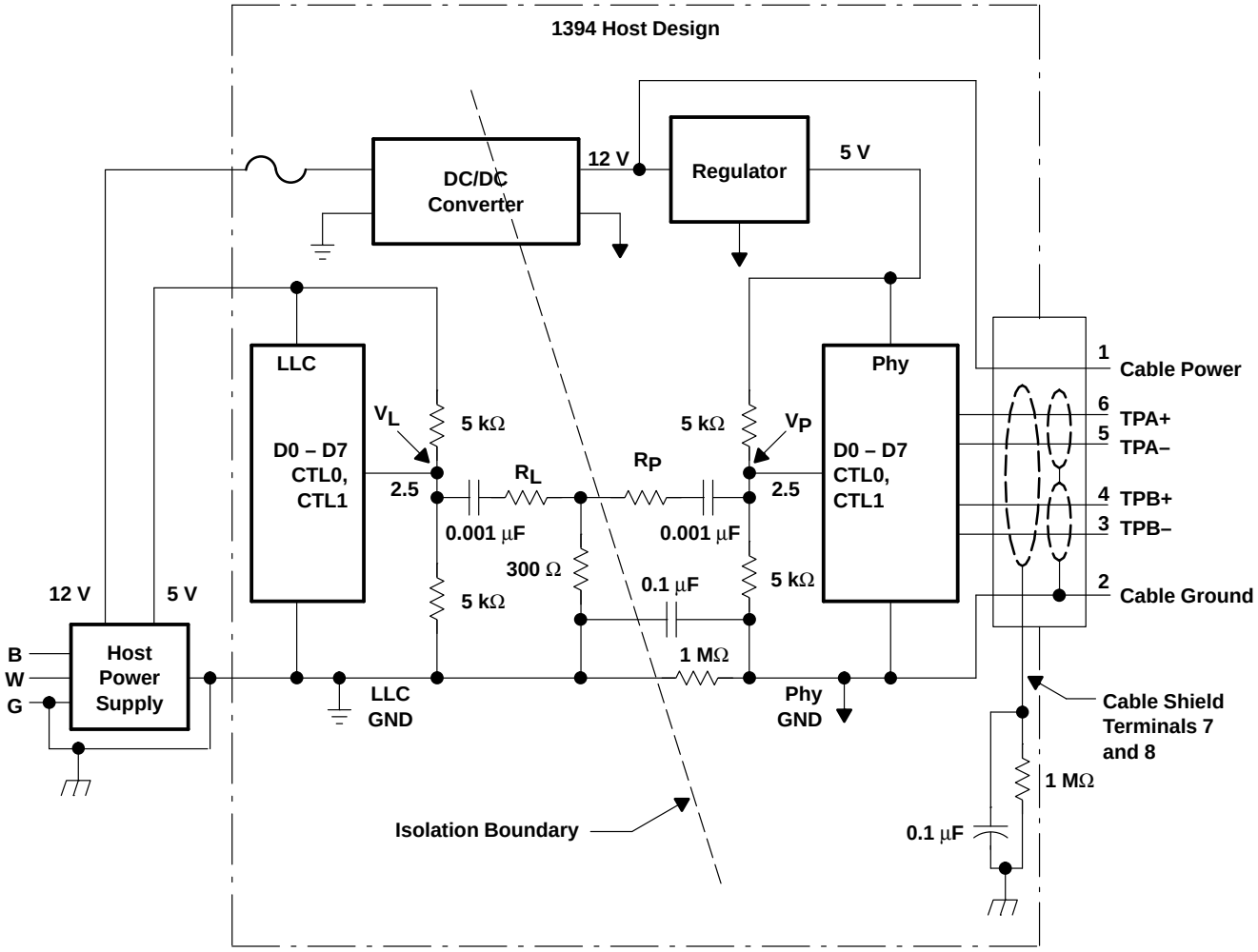

Figure 5. IEEE 1394-1995 Annex J Capacitive Isolation

2 IEEE 1394-1995 Physical Layer–Link Layer Interface Isolation

Annex A in the IEEE 1394-1995 standard discusses the various places that galvanic isolation can be implemented when necessary to achieve galvanic isolation of the node. One of the most cost effective places to isolate a node is at the physical layer controller (Phy)-link layer controller (LLC) interface due to the relatively small number of signals that need to be isolated. Annex J of the IEEE 1394-1995 standard illustrates two techniques to achieve Phy-LLC galvanic isolation. One method uses capacitive-isolation circuitry and the other uses a transformer-isolation circuit on each Phy-LLC signal. The capacitive isolation-circuit is able to galvanically isolate up to the working voltage of the capacitors used in the circuit. The transformer circuit would typically be able to galvanically isolate to higher voltage levels due to its generally higher voltage capability between primary and secondary windings.

The Phy-LLC interface consists of the following signal lines: LLC request (LREQ), system clock (SYSCLK), two interface control lines (CTL0 and CTL1), and up to 8 data lines (D0 – D7) plus several additional signals that may or may not require galvanic isolation depending upon the design of the system. These additional signal lines that may require isolation on the Texas Instruments Phys are the reset input ($\overline{\text{RESET}}$), LLC power status (LPS), power down (PD), configuration manager contender input with link-on output (C/LKON), and cable not active (CNA).

Figure 5 shows a capacitively coupled Phy and LLC that use the capacitive-isolation circuit described in Annex J of the IEEE standard. Each bidirectional signal requires the network shown in Figure 5. A typical application for this type of design would be a host computer with an IEEE 1394-1995 port that is connected to a green-wire ground through a nonisolated power supply and a three-wire ac plug. Note that since the machine power supply is not isolated, an isolating dc/dc converter is required to isolate the host power domain from the cable power domain powering the Phy. In these examples it is assumed that the dc/dc converter is internally protected from sinking any current supplied from the cable power domain. The terminal numbers shown on the 1394 connector are according to Table 4–3 of IEEE 1394-1995. The cable shield terminations labeled 7 and 8 are actually the connector tabs connected to the metal shell of the printed-wire board (PWB) 1394 connector.

The capacitive-isolation circuit and the transformer-isolation circuit operate basically the same. In order for signals to cross the isolation boundary, the driving side output must first be differentiated. Whenever the line state changes, the Phy-LLC interface signal is driven to the new state. When the line state remains constant for more than one clock period, the signal is sent into a high-impedance state. When the output signal is at the high-impedance state, the input signals quickly return to $V_{DD}/2$. The differentiation is handled internally in the Phy and LLC integrated circuits. Figure 6 shows the logical line state at the output buffer, V_L, when the LLC is driving, and V_P when the Phy is driving.

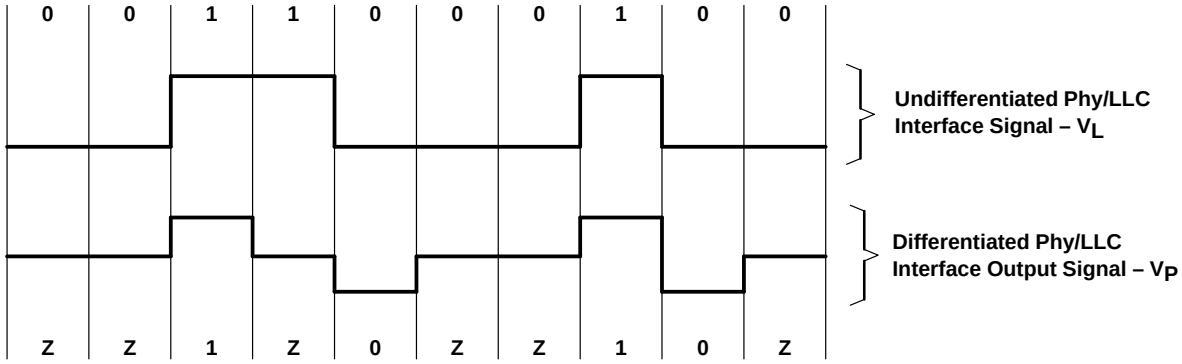

Figure 6. Differentiation of Interface Signal ($\overline{\text{ISO}}$ Terminal low)

The signal at the input buffer is shown in Figure 7. This waveform is for a 5-V device. A 3-V device would have the signals ratioed down accordingly.

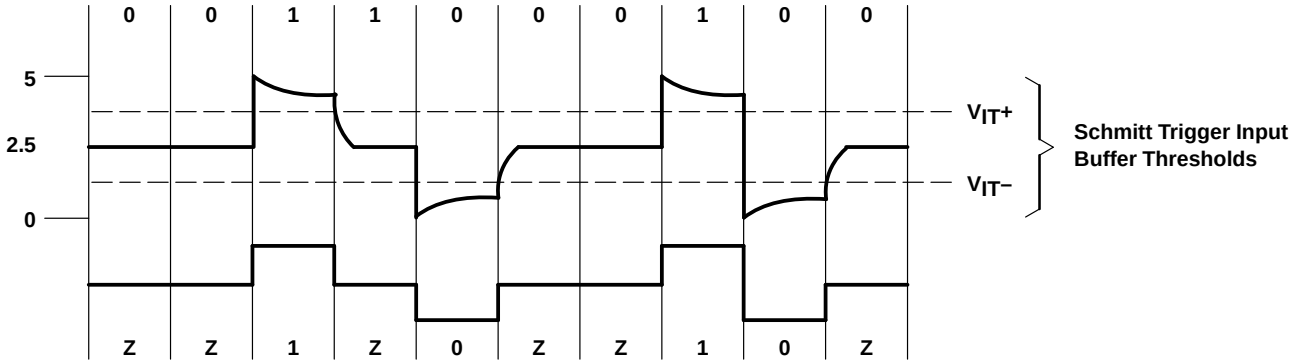

Figure 7. Line Levels of Differentiated Interface Signals

The input buffer output remains in its previous state until a hysteresis threshold is crossed, thus recreating the original undifferentiated signal. On the TI TSB21LV03 Phy differentiation is done when the $\overline{\text{ISO}}$ terminal is held low. To turn the $\overline{\text{ISO}}$ terminal on for the Texas Instruments devices, it must be held to a low logic level.

There are several design challenges with the Annex J type of galvanic isolation barrier. They are:

- The input thresholds must be maintained accurately at $V_{DD}/2$.
- The input hysteresis must be fairly wide and it too must be maintained accurately.
- Two capacitors and seven resistors are required for each bidirectional line to be isolated. This adds to component costs and board space.
- Differentiation circuitry is required in each output buffer, and circuitry to decode the differentiated signal must be added to each input buffer.
- Supply current in the input buffer can be quite high because the input is normally sitting at midsupply. When using CMOS-type input buffers, as much as 1 mA of supply current can be wasted in each input.
- Supply current is wasted in the external bias resistors that are connected between the supply rail and ground.

- The propagation delay through this isolation circuit can typically be 2 ns to 3 ns. This delay reduces the setup and hold-time windows allowed for each input.
- Noise margins on the input buffer are very low. The noise margin is the difference between the maximum threshold level and the minimum hysteresis level on the high side and the difference between the minimum threshold level and the maximum hysteresis level on the low side.
- During power up of either the Phy, the LLC, or both, care must be taken to ensure that the output state and the input state are synchronized; in other words, ensure that the voltage levels on each side of the isolation capacitor represent the same logic state. Input power-up glitches can cause output and input states to be out of synchronization causing communication errors between the Phy and the LLC. As data is passed through the isolation barrier, the output and input eventually synchronize, but there is the possibility of locking up the system before synchronization occurs.

3 The Texas Instruments Bus Holder Galvanic Isolation Barrier

The Texas Instruments patent-pending bus-holder galvanic isolation technique simplifies most of the previously mentioned design challenges. Bus-holder circuits are required on the receiving side (both sides when bidirectional) of the single capacitor that forms the galvanic isolation barrier. The bus-hold function consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. This prevents bus lines from floating without using pullup or pulldown resistors. The high-impedance inputs of these internal CMOS buffers are connected to the input terminals of the device. The feedback path on the internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver. Active bus-hold circuitry typically holds unused or floating-data inputs at valid logic levels and eliminates the need for pullup or pulldown resistors. These bus holders can be integrated into the Phy and LLC devices at extremely low cost. If either the Phy, the LLC, or both does not have the bus holders integrated, external bus holders can be implemented. Bus holder integrated circuits (ICs) or ICs with bus-holder inputs are available commercially that are capable of performing this function. TI plans to integrate bus holders internally on future revisions of its Phys and LLCs. Figure 8 shows a typical implementation using Phy and LLC devices with internal bus holders.

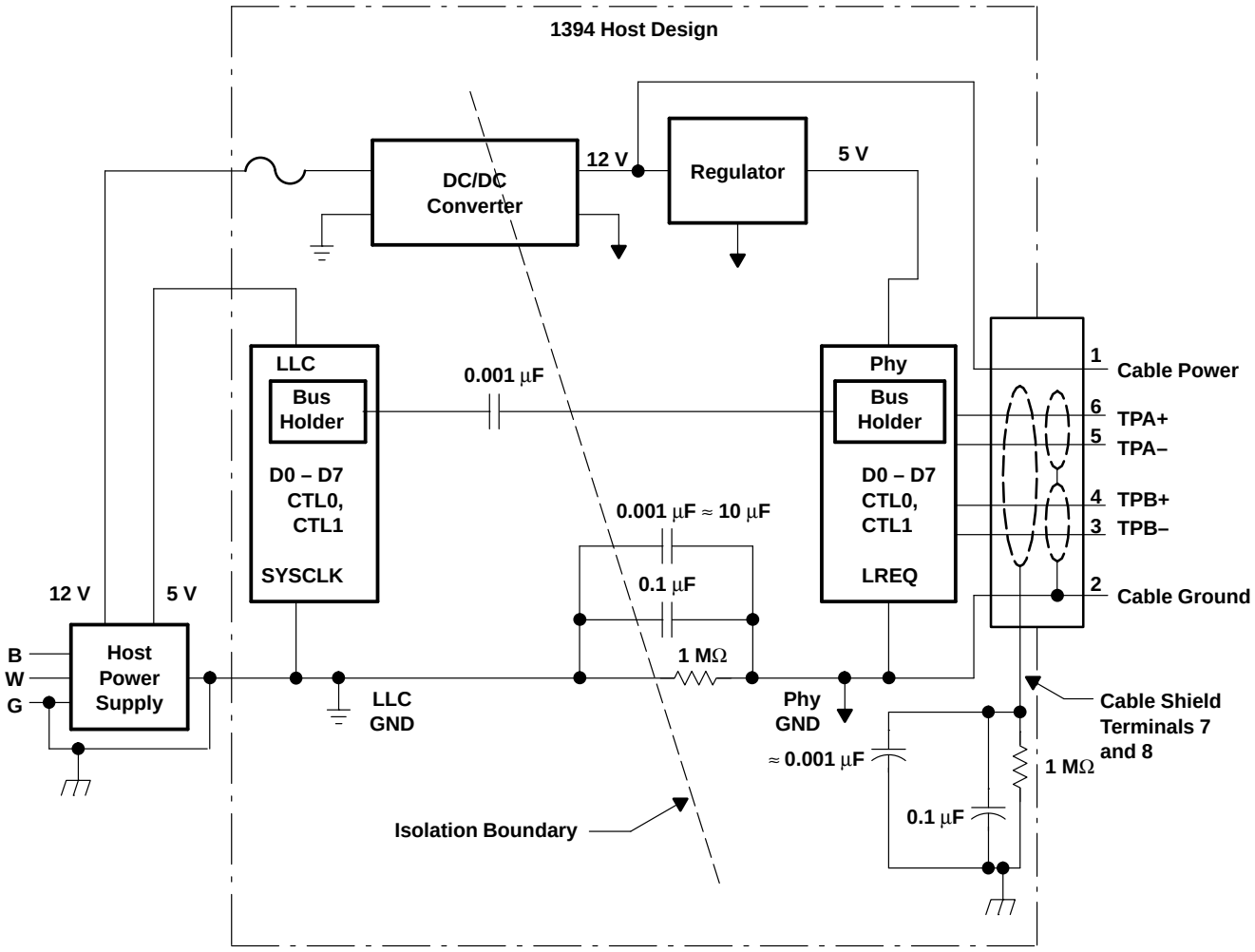

Figure 8. Internal Bus-Holder Isolation

The bus-holder isolation technique is cost effective and eliminates most of the components required for the implementation of galvanic isolation described in the IEEE 1394-1995 High Performance Serial Bus Standard in Appendix J.6. Only one 0.001-μF capacitor per signal line is required. The principal of operation is straight forward. When the output node switches states, the charge on the capacitor is maintained, and voltage on the input node is pulled in the same direction as the output node. The bus holder then maintains the input state until the output makes another transition. This allows normal input buffers to be used that do not require critical threshold values. Critical hysteresis levels also are not required. Board area and external component cost are reduced. Differentiation circuitry in the output buffers is not needed. High supply currents in the input buffers are eliminated. Supply current wasted in the external bias resistors is eliminated. The propagation delay through the single isolation capacitor is extremely small. And finally, noise margins on the input buffer are essentially the same as for the nonisolated CMOS signal levels.

NOTE:

Since no differentiation is needed, the $\overline{ISO}$ terminal on TI devices needs to be held in a high-logic state (differentiation is turned off) to correctly function with bus-holder isolation.

When higher voltage isolation is required than can be provided by the working voltage of a single capacitor, then multiple capacitors can be implemented in series. The working voltages then increase, but the capacitance values of each individual capacitor must be increased to maintain the same voltage for the series combination.

Experience has shown that to properly provide for a return path for the small circuits that are propagated across an isolated Phy-LLC interface requires not just a single parallel combination of a 0.1 μF capacitor and a 1 MΩ resistor. It also requires an additional capacitor(s) in parallel with the 0.1 μF. Values of up to 10 μF have been shown to aid error-free operation.

As with the isolation method described in the IEEE 1394-1995 standard, care must be taken to ensure that the input and output are synchronized during power up of either the Phy, LLC, or both. This can be accomplished internally in some cases such as with the LREQ terminal. During power up reset the LREQ input of the Phy can be pulled low, which should also be the driving state of the LREQ output of the LLC device during power up. The LREQ terminal has the potential of hanging the Phy-LLC interface if the Phy senses a high input while the LLC continues driving low after a power up of either or both devices.

TI LLCs released after April 1997 (TSB12LV41 and those after) contain bus-hold circuitry and circuitry to ensure correct initialization of the Phy-Link interface. In the LLCs before that time (TSB12C01A, TSB12LV21, and the TSB12LV31) circuitry should be added to the LLC side of the isolation capacitor to ensure upon power up and hardware reset, the logic state on the link side of the isolation capacitor is a logic low.

Another Phy-LLC signal with the potential to cause problems when the states across the Phy-LLC interface do not match is the link power status (LPS) signal. For instance, when attempting to pass the LPS signal in as a dc signal across a bus-holder and capacitor-type isolation, there are challenges to be met. If the LLC powers up first, while the Phy was still powered down, the isolation capacitor could have a charge induced on it. In a 3-V system the LLC side of the capacitor would be charged to 3 V while the Phy side remained at ground potential. When the Phy was then powered up, the capacitor and the bus holder could keep the LPS input signal at the low level and the states would not be synchronized. This would then cause the Phy to disable all Phy-LLC interface terminals, and the node could lock up. By transitioning the logic levels on each side of the capacitor, the states can be synchronized. In the LPS example, a case has been hypothesized where the LLC side of the isolation capacitor is logic high while the Phy side is low. If the LLC then drives a low level, the Phy side of the capacitor also tries to swing the same voltage down . However since the Phy side of the isolation capacitor is already in the low state, the voltage goes negative until the clamping diode is turned on. This diode to ground clamps the voltage and dissipates the charge on the capacitor bringing the state on each side of the isolating capacitor into synchronization. For the dc-type signals, these transitions do not cause a loss of information. However for the ac signals (i.e., LREQ) the first bit of the transmission is lost, making this method of achieving synchronization only useful if a dummy transition of the signal can be generated and tolerated. A much better approach for the LPS signal would be to use an ac signal across the bus holder and capacitor isolation. The TI physical-layer device LPS terminal recognizes a square wave of between 220-kHz and 5.5-MHz as the signal that the LLC is on. The generation of this square-wave signal would need to be designed such that whenever the LLC is powered up, the signal is on. On the TSB12C01A, TSB12LV31, and TSB12LV41 LLC devices, this signal is supplied as the power on terminal (see Figure 9).

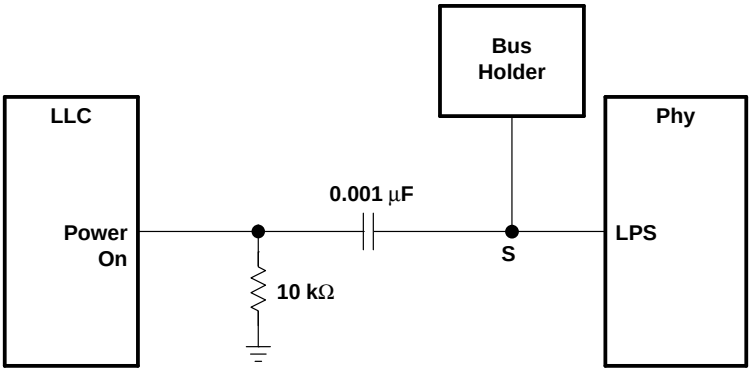

Figure 9. External Bus-Holder Implementation for AC LPS Line

Since the TSB12LV21 does not supply a square-wave signal, the system designer needs to provide either an ac or dc signal to the Phy if this feature is desired. A TIL191B optoisolator can provide dc signal for slightly more than $0.30 (September 1996) a line (see Figure 10).

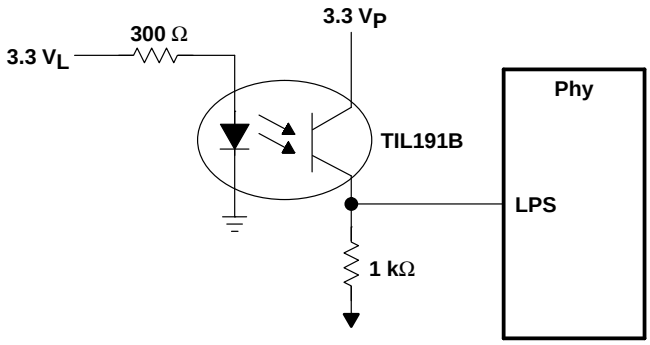

Figure 10. Implementation of Isolation for DC LPS Signal Using TIL191A Optoisolator

A note on optoisolators, it is recommended that optoisolators only be used on slow signals (times in ms) like $\overline{\text{RESET}}$ or power down (PD) that are essentially dc signals. There currently are no known optoisolators that have a large enough bandwidth and low enough latency to meet the requirements of the data and control lines of the Phy-LLC interface. Since each system is different and requires different sequences associated with startup and power down, it falls back to the system designer to be responsible to check all possible conditions that can occur on the Phy-LLC interface to ensure that this type of nonsynchronized state either does not occur or is resolved correctly. Table 1 lists several signal states associated with Phy and LLC devices.

NOTE:

Whenever LPS is driven low then the CMC/contender should, at the same time, also be driven low.

Table 1. Phy-LLC Interface Initial Signal States

SIGNALS	PHY DEVICES†			LLC DEVICES†		
	TSB21LV03	TSB11LV01	TSB11C01	TSB12C01A	TSB12LV21	TSB12LV31
Phy-LLC Data	L	L	L	I	I	I
Phy-LLC CTL	L	L	L	I	I	I
SCLK	49.152 MHz	49.152 MHz	49.152 MHz	I	I	I
LREQ	I	I	I	L	L	L
LPS	L	I	I	N/A	N/A	N/A
Power-On	N/A	N/A	N/A	BCLK/32	N/A	BCLK/32
$\overline{\text{RESET}}$	I	I	I	I	I	I
PD	I	I	N/A	N/A	N/A	N/A
CMC	I	I	I	N/A	N/A	I
Link-On	Z	Z	Z	N/A	N/A	N/A
CNA	Port State	Port State	N/A	N/A	N/A	N/A
GPIO	N/A	N/A	N/A	N/A	Z	N/A

† H – driven high, I – Input, L – driven low, N/A – not applicable, Z – high-impedance state

When the Phy and/or the LLC device is not designed with internal bus holders, this bus-holder isolation scheme can still be implemented with external bus holders. Figure 11 illustrates a circuit implementation where neither the Phy or the LLC have internal bus holders. External bus holders are provided on each side of the isolation barrier.

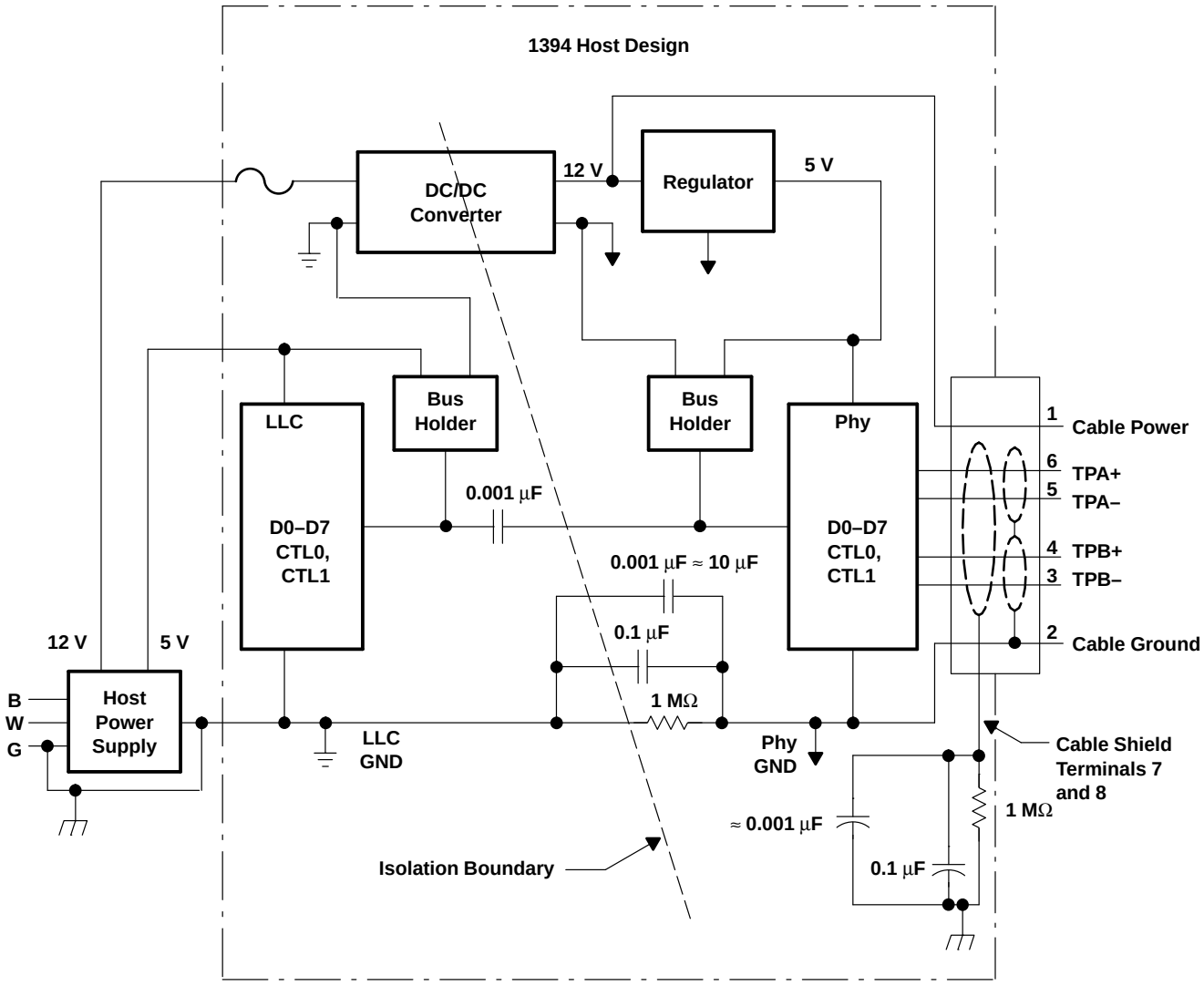

Figure 11. External Implementation of Bus-Holder Isolation

When either the Phy or the LLC have internal bus holders present, then the device without bus holders will require that an external bus holder to be implemented on its side of the isolation barrier. There are several choices for external bus holders. Depending on the application, the least expensive approach can be to use the inputs to buffer circuits that have bus holders built into their inputs. Several alternative devices that have bus holder circuits on the inputs are available. For 3.3-V applications, the SN74LVCH244, SN74LVCH245, and SN74LVCH16244 are available. For 5-V applications, the SN74ABTH245, SN74ACT1071, or SN74ACT1073 are available. Figure 12 and Figure 13 show the implementation of the bus-holder isolation for a monodirectional signal.

NOTE:

A bus holder is only required on the receiving side of the isolation capacitor, regardless of whether that side is in the LLC power domain or the Phy power domain.

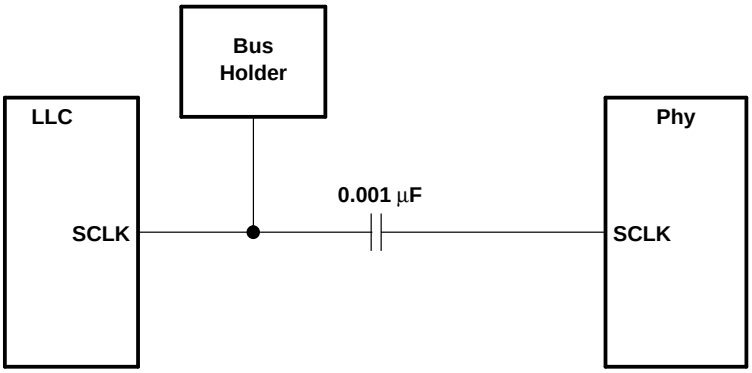

Figure 12. External Implementation of Bus-Holder Isolation for SCLK Line

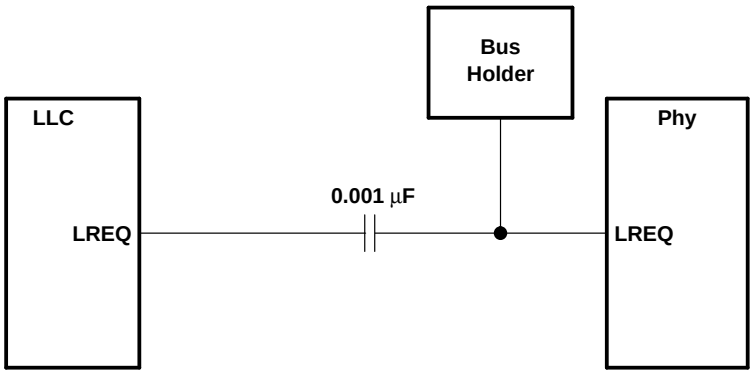

Figure 13. External Implementation of Bus-Holder Isolation for LREQ Line

The bus-holder isolation works well on the other ac signals that may be used in the Phy-LLC interface. As noted above, the LPS signal can be a square wave of between 220 kHz and 5.5 MHz. The LPS signal easily passes through the bus-holder isolation network from the LLC to the Phy. The same can be said of the link-on signal, with a frequency of 6.114 MHz it can also use the bus-holder isolation to pass from the Phy to whatever digital circuitry is implemented to use this signal to turn on the LLC.

Several other useful dc signals or functions can be implemented across an isolation barrier when required. The cable not active (CNA) signal is a dc signal and while it can be transmitted directly across the isolation barrier using bus holders or optoisolators, the same information is available in the Phy register space as the connected bit in the individual port status registers. This information can be transferred across the isolation barrier on the data lines using a Phy register read request, unless the CNA signal is being used in the LLC power domain to turn on and off the Phy using the power-down line. When this is the case, the CNA electrical signal must be brought across the isolation barrier.

All of the Texas Instruments low-voltage Phys have a power-down signal (PD) to enable a power-saving mode for battery operation. This signal was made a dc signal since battery-powered devices are usually leaf nodes not typically connected to two different power domains. The PD signal can be transmitted across the isolation interface using either bus-holder isolation or optoisolators (see Figure 14).

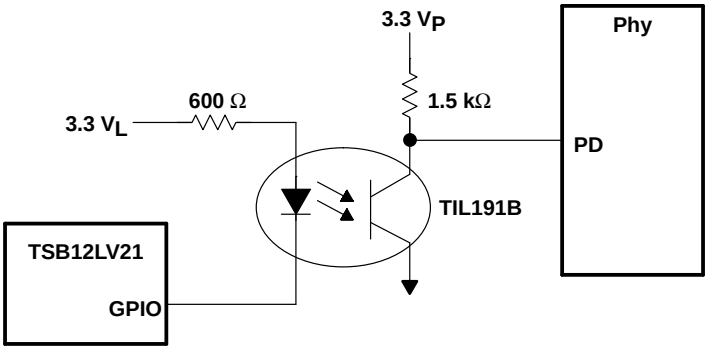

Figure 14. Isolation of PD Signal Using An Optoisolator

The power-up reset of TI Phy devices is designed to be used with a 0.1-μF capacitor connected to the reset terminal. This provides the necessary delay (2 ms minimum) to allow the analog circuitry to reach a quiescent state before suppling power to the rest of the device. Since no connection to the LLC is required, no isolation is required. While the $\overline{\text{RESET}}$ signal may be transmitted across the isolation interface using bus-holder isolation or optoisolation, it typically would not need to be. When it is required to have control over the Phy device reset from the LLC power domain, an example implementation is shown in Figure 15. The $\overline{\text{RESET}}$ line needs to be held low for a minimum of 2 ms and the LLC driver needs to be able to sink 11 mA. In the implementation shown in Figure 15, the optoisolator drains the charge from the 0.1 μF reset capacitor when asserted. When the reset signal is removed, the capacitor charges through a current source in the Phy that sets a time constant long enough for correct reset operation.

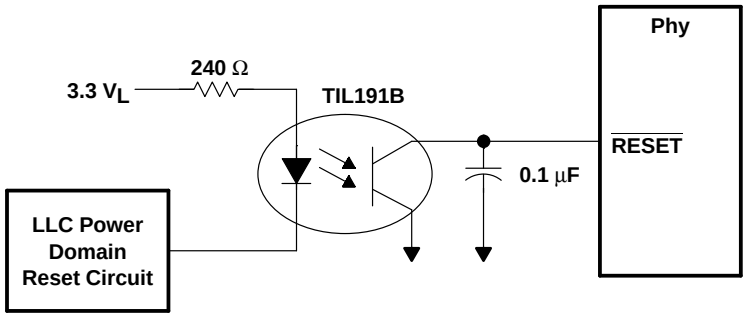

Figure 15. Optoisolator Isolation for Phy Reset Terminal

The current implementation on the TSB21LV03, TSB11LV01, and TSB11C01 of the configuration-manager contender (CMC) bit is as a terminal tied high or low on the Phy. During each bus reset, the state of the CMC/LKON terminal is sampled just before the SelfID (SID) is sent to determine the state of the

Contender bit in the SelfID packet. Since this can be set on the Phy without need for a connection to the LLC, no isolation is required. However when control of the status of the configuration-manager contender bit state is desired from the LLC power domain, isolation may be accomplished by using a combination of bus-holder isolation and an optoisolator as shown in Figure 16. This signal isolation is complicated by the fact that it shares a terminal with the ac signal LKON. The top path is for the link-on signal from the Phy to the LLC through an isolating capacitor with a bus holder on the receiving (LLC) side of the capacitor. The bottom path is to pass a dc signal to program the state of the CMC bit. This dc signal is isolated using an optoisolator. The output path of the optoisolator on the Phy side contains an in-line resistor to dissipate the energy produced by the LKON signal without damaging the optoisolator. A pulldown resistor is provided on the LLC side of the optoisolator to ensure that the power-on state of the configuration-management contender bit is low. The LVCH244 is needed in this configuration to source and sink the current required for the chosen optoisolator. It is assumed that a spare buffer is available if external bus holders are used and the inputs to LVCH244 are used to provide them.

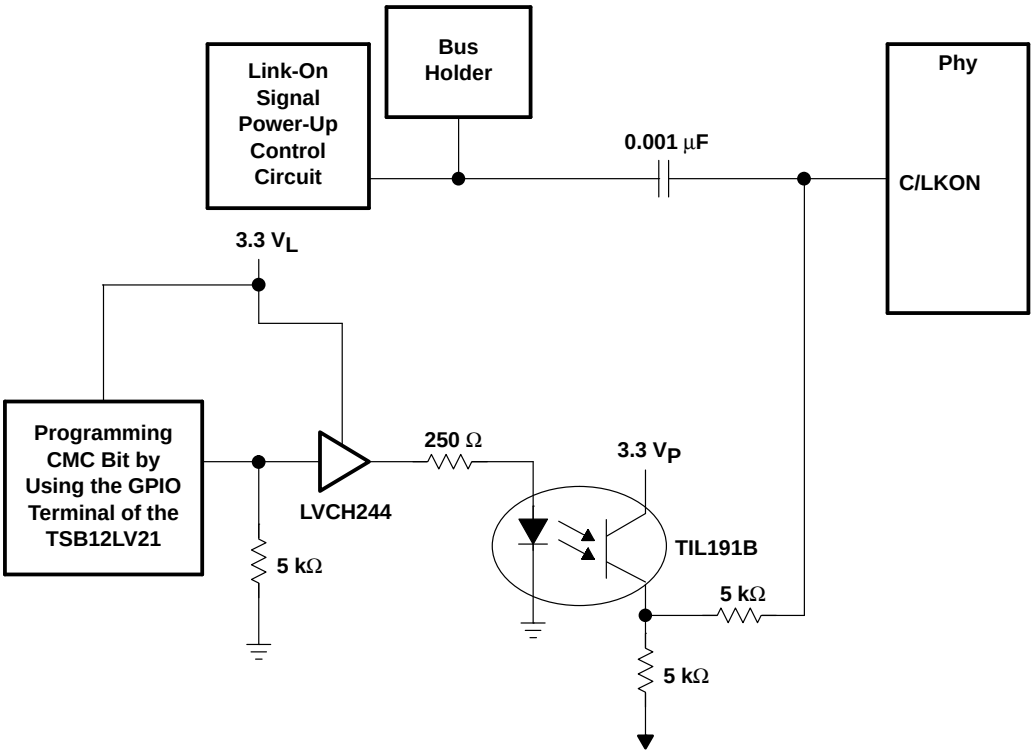

Figure 16. External Implementation of Bus-Holder Isolation for Phy Link-On Signal and Circuit for Setting CMC Bit (C/LKON)

The implementation of the TSB41LV0x Phy is much simpler. The inital state of the CMC/LKON terminal is only sampled upon power-up reset. After that time the value of the Contender bit is controlled by a bit in the TSB41LV0x registers that is readable and writeable using the Phy-LLC interface. Since the state of the Contender bit can be controlled across the normal Phy-LLC interface only the LKON signal needs to be transmitted across the isolation barrier. Instead of an optoisolator being required, all that is needed is a 10-kΩ pullup resistor when the intial state is to be a contender. When the intial state is not to be a contender, a 10-kΩ pulldown resistor would be used.

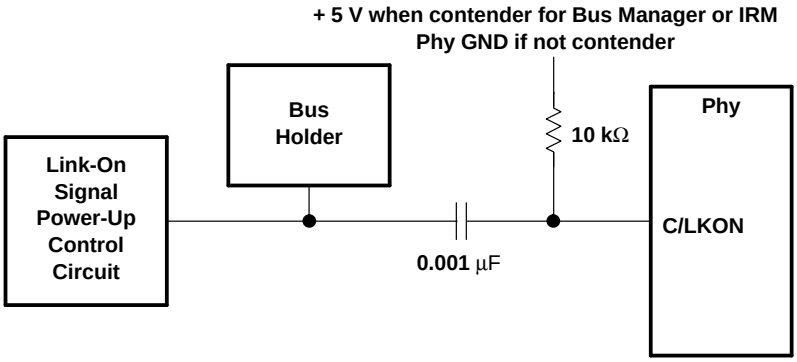

Figure 17. Isolation of LKON Signal Using a Bus Holder

Table 2 lists those terminals of the connected device that need isolation.

Table 2. Terminals That Need Isolation

TERMINAL	COMMENT
D0 – D7	Isolation circuitry required on data lines used (D0, D1 for S100; D0 – D3 for S200; D0 – D7 for S400)
CTL0, CTL1	Isolation circuitry required
LREQ	Isolation circuitry required
SCLK	Isolation circuitry required
LPS	Isolation circuitry required if implementing link-on packets or implementing nodes that power down the link layer while maintaining power to the Phy layer. When not implementing link-on packets LPS can be tied high in the Phy power domain to always have the Phy-LLC interface enabled, but it puts incorrect LLC power status into Self-ID packet if the LLC is powered down.
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ only requires isolation circuitry if software control over hardware reset is required. Normally $\overline{\text{RESET}}$ is connected to a 0.1-μF capacitor in the Phy power domain and resets itself upon power up, thus requiring no isolation circuit. Other means of resetting the Phy include: • Initiating a bus reset results in an almost complete Phy layer reset • The power down terminal on TI low-voltage parts powers down the entire chip except for the CNA circuit • The LLC power status terminal, when pulled low, powers down the Phy-LLC interface
PD	PD only requires isolation circuitry if software control over the power-down mode is required. When control is not required PD is normally pulled low in the Phy power domain.
CNA	CNA only requires isolation circuitry when cable not active is used in the LLC power domain, for example, to determine what state to drive the PD terminal. CNA still operates when the Phy is in power-down mode and gives LLC power domain circuitry an indication when a cable has been plugged into the Phy and to power up or power down the Phy. Otherwise CNA is not connected and the connected status of a Phy port is determined by reading the Phy registers
LKON	Isolation circuitry is required if implementing link-on packets. Otherwise LKON is not connected to LLC power domain.
CMC	CMC only requires isolation circuitry if software control over the state of the configuration-manager contender (CMC) bit is required. When software control is not required it may be pulled high to be a CMC or low to not be a CMC in the Phy power domain

The bus-holder isolation, as described previously, can be used with mixed voltage systems with modification. When the driving side is at a low-power-level device then the bus holders on the high-power-level receiving side pull a high logic level to the higher supply voltage rail. When the transition to the low side takes place, the 3.3-V swing may not be enough to pass the thresholds if 5-V bus holders are used on the receiving side. To compensate for this, a 3.3-V bus holder can be used on the inputs to the 5-V device (this requires the 5-V device to have TTL input thresholds). A diode chain can lower the voltage of the power supplied to the bus holder as shown in Figure 17. The low-voltage bus holder limits the voltage swing and the thresholds to be compatible with the swing induced by the low-voltage driver on the other side of the isolation capacitor. When the 5-V device (an LLC in Figure 17) has TTL inputs, the ≈ 3.2-V powered bus holder meets those thresholds.

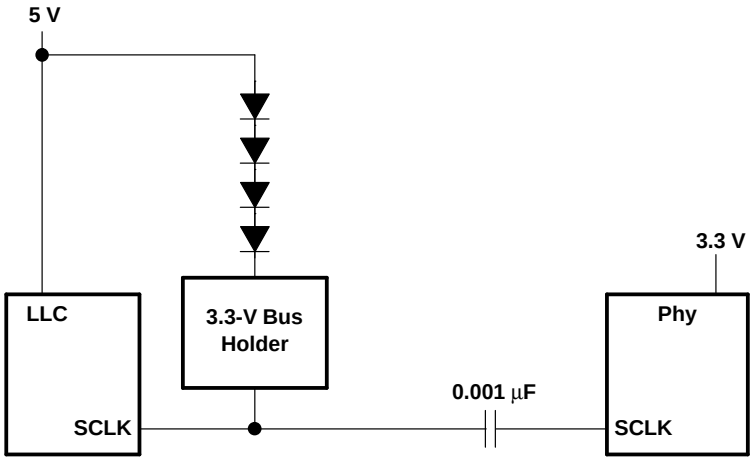

Figure 18. Isolated Mixed-Voltage System

4 Summary

Determination of whether a node requires galvanic isolation of IEEE 1394-1995 nodes is a node-by-node requirement of the system designer. Isolation of 1394 nodes requires three parts: cable shielding, cable-power isolation, and signal-line isolation. Cable shielding requires the correct termination of the cable outer shield, nominally with a parallel combination of a 1-MΩ resistor and a 0.1-μF capacitor. Cable power isolation requires isolation of the cable power supply when providing power, or keeping cable power physically separate when not providing cable power, or keeping cable power physically separate when not using cable power exclusively for the entire node (with no other outside connections). Texas Instruments recommends its bus-holder isolation technique for signal-line isolation. It is superior in cost and performance to the method described in Annex J of the IEEE 1394-1995 standard. Table 3 compares the aspects of the capacitive isolation shown in the informative Annex J of IEEE1394-1995 with the TI bus-holder isolation.

Table 3. Implementation Comparison

EXAMPLE COMPARISON FOR 200-Mbits/s NODE (DATA, CTL, LREQ, SYSCLK)			
PARAMETERS	**ANNEX J METHOD**	**TI METHOD**	**TI BUS-HOLDER BENEFITS**
External capacitors	14	8	Reduced PWB area Reduced complexity Reduced cost
External resistors	48	0	Reduced PWB area Reduced power Reduced complexity Reduced cost
Voltage swing	$V_{DD}/2$	Rail to rail	Better noise margin
Digital differentiaters on outputs	Required	None	Reduced complexity Reduced cost
Special threshold requirements	Required	None	Reduced complexity Reduced cost
Isolation network power drain	Holds input cells at $V_{DD}/2$	Method causes no impact	Minimal quiescent power drain No special input cell requirement Reduced cost
Hysteresis on inputs	Requires Schmitt triggers on inputs	None	Reduced complexity Reduced cost
Delay through network	Introduces 2-ns to 3-ns delay	Introduces near-zero delay	Fewer timing issues

A Cable Shielding Termination and EMI

Home consumer equipment is required to pass FCC Class B testing. Several PC card venders experience[7] with the testing process has led to them shorting the overall external cable shield directly to the chassis ground on a PC. This connects the “Faraday cage” of the PC chassis to the “Faraday cage” of the cable shield to reduce electric field emission. If this is done, the chassis grounds of every node connected in this manner will be shorted together and isolation defeated for these nodes.

Others[8,9] have achieved reduced emissions by including smaller capacitors in the parallel 1-M, 0.1 μF network connecting the overall cable shield to chassis ground and maintaining galvanic isolation.

B 4-Pin Consumer Cables and Connectors

As previously stated, 1394 signalling requires each physical layer to share the same ground. Since the 4-pin cable does not have a logic ground wire, it connects Phy ground domains using the cable shields, see Figure 4–11 in the P1394A[10] document. Therefore, the 1394-1995 standard recommended shield isolation must only be used to isolate the shields from chassis ground. The shields must be directly shorted to the Phy ground (see Figure 19). However all the same problems that exist with the 6-pin connector also exist for the 4-pin connector, so isolation must still be considered.

The wiring of the cables may also create problems . The 6-pin to 4-pin cable ties the shields of the cable directly to the logic ground of the 6-pin connector. This means that on the 6-pin connector side of the cable, the signal shields are tied to the overall cable shield, and all three are tied to the cable logic ground (cable power ground, pin 2 on the connector). Please refer to Figure 4–10 in the P1394A[10] document.

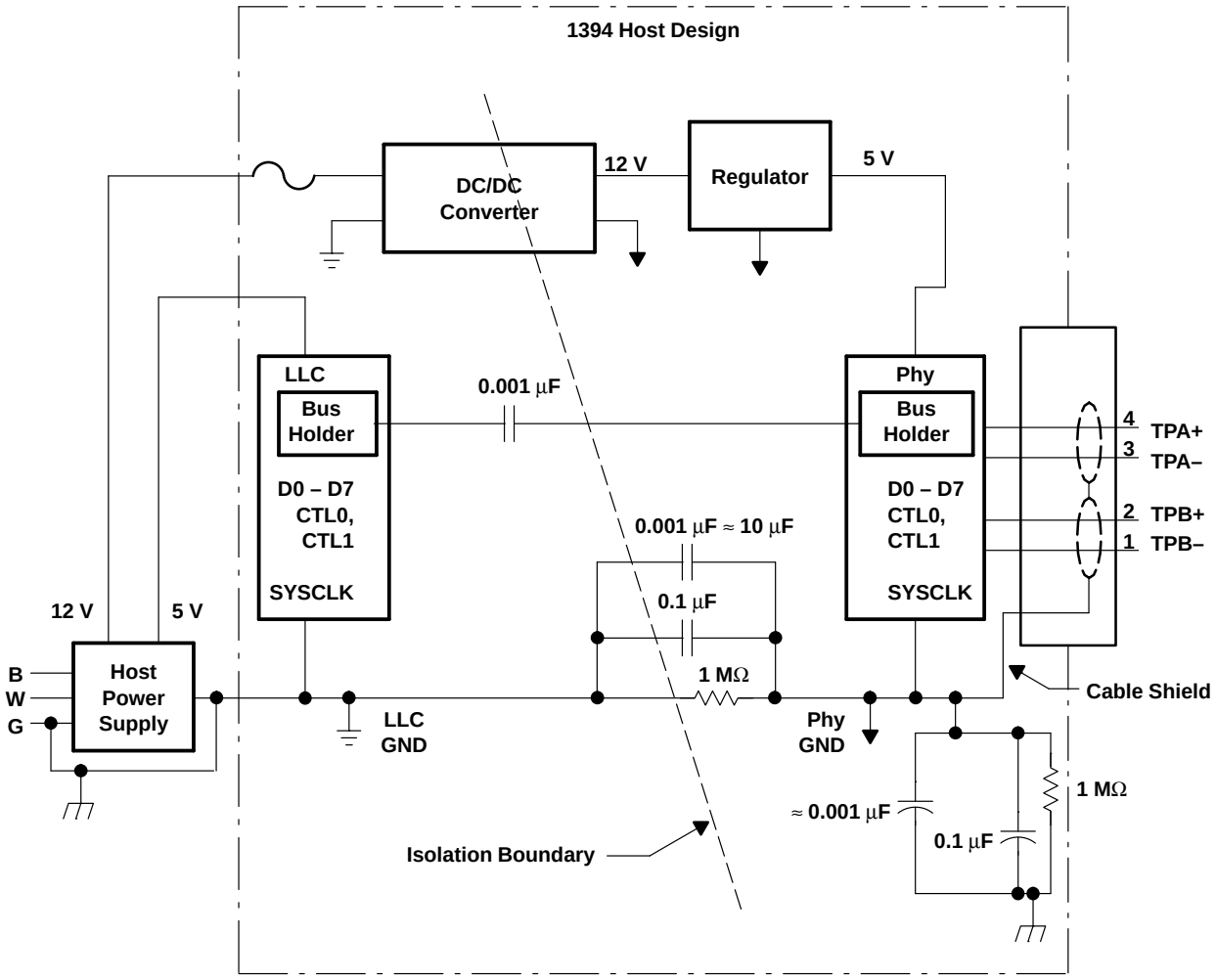

Figure 19. Internal Bus-Holder Isolation with 4-Pin Cable

C Testing Isolation

Care must be taken when testing isolation circuits. It must be carefully thought out to ensure that the two ground domains being isolated are not shorted together. Most desktop PCs use a green wire (3-prong plug) grounded power supply and therefore any device connected to the PC's ground shares this ground. Monitors also are green-wire grounded and will ground any machine connected to them to the monitor's ground domain. Most lab test equipment is also green-wire grounded and will ground any equipment its ground probes are connected to. To verify a circuit is isolated, one of the ground domains should be floated and offset by a dc voltage that is gradually applied. If more than a milliampere or two of current flows, there is a probably some path shorting the domains together. Floating a domain will mean using a 3-prong to 2-prong adapter along with isolation transformers and dc power supplies. Be sure to check with your safety personnel about using ungrounded equipment in your lab.

References

1. IEEE 1394-1995: Standard for a High Performance Serial Bus, 12/95
   - Figure 3-30 Cable Shield Termination
   - Paragraph 4.2.1.4.8 Shield AC Coupling
   - Paragraph 4.2.2.7 Power and Ground
   - Annex A.4 Electrical isolation requirements (summary)
   - Annex J.6 Isolation barrier
2. 1394 Link Core Seminar Notes, 10/95, Texas Instruments
3. 1394 Power and Isolation white paper - July 10, 1995, Apple Computer
4. Data sheet for TI SN74ACT1071, 10-Bit Bus Termination Array with Bus Hold Function, Literature Number SCAS192-D3994, April 1993
5. Data sheet TI TIL191A&B, 193A&B Optocouplers, Literature Number SOES026, October 1995
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7. July 1997 1394 Developers Conference, Mike Field Presentation
8. July 1997 1394 Developers Conference, Gerhard Ringel Presentation
9. July 1997 1394 Developers Conference, Carl Selander Presentation
10. P1394A Draft Document, version 1.0