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TSB12LV31

IEEE 1394-1995 General-Purpose Link-Layer Controller

Data Manual

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Data Manual

IEEE 1394-1995 General-Purpose Link-Layer Controller

For Computer Peripherals and Consumer Audio/Video Electronics

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Contents

Contents (continued)

List of Illustrations

List of Tables

List of Tables (continued)

1 Overview

1.1 Description

The TSB12LV31 performs bidirectional asynchronous/isochronous data transfers to and from an IEEE 1394-1995 serial bus physical layer (phy) device. The TSB12LV31 is tailored and optimized for use as a *peripheral* link-layer controller (LLC). TSB12LV31 asynchronous and isochronous operations are summarized as follows:

TSB12LV31 asynchronous transmit:	From asynchronous transmit FIFO (ATF)
TSB12LV31 asynchronous receive:	To general receive FIFO (GRF)
TSB12LV31 isochronous transmit:	From 8-bit IsoPort
TSB12LV31 isochronous receive:	To 8 bit IsoPort, To GRF, or To 8-bit IsoPort and To GRF

This document is not intended to serve as a tutorial on the 1394; users should refer to the IEEE 1394-1995 standard for more detailed information.

1.2 Features

The TSB12LV31 supports the following features:

- Supports Provisions of IEEE 1394-1995 Standard for High-Performance Serial Bus (1394)†
- Fully Interoperable with FireWire™ Implementation of 1394
- Compatible with Texas Instruments TSB11LV01 and TSB21LV03 Physical Layer Controllers (Phys)
- Single 3.3-V supply operation with 5-V Tolerant Capabilities using 5-V Bias Terminals
- High-performance 100-Pin PZ (S–PQFP–G100) package.
- Programmable Microcontroller Interface with 8-Bit or 16-Bit Data Bus, Three Modes of Operation, and Clock Frequency to 50 Mhz
- 50-quadlet (200-Byte) FIFO Accessed Through Microcontroller Interface Supports Asynchronous and Isochronous Operations
- Programmable FIFO Size For Asynchronous Transmit FIFO and General-Receive FIFO
- Single-Channel Support for Isochronous Transmit from Unbuffered 8-Bit Isochronous Port (IsoPort)
- Isochronous Receive to FIFO or to Unbuffered 8-Bit IsoPort
- Isochronous Header Synchronous-Bit Detection on Receive
- Automatically Reports IRM NODE_ID and Verifies Automatic 1394 Self-ID
- Supports Transfer Rates of 100 Mbits/s and 200 Mbits/s
- Asynchronous Packet Reception to Internal FIFO (Accessed Through the Microcontroller Interface)
- Asynchronous Packet Transmission from Internal FIFO (Accessed Through the Microcontroller Interface)
- Generation of External Microcontroller Clock from SCLK (SCLK/4)
- Generation of 32-Bit Cyclic Redundancy Check (CRC) for Transmission of 1394 Packets
- 32-Bit CRC Checking on Reception of 1394 Packets

† Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thomson, Limited.
FireWire is a trademark of Apple Computer, Incorporated.

1.3 Related Documents

The following document is applicable and should be referenced for additional information:

- IEEE STD IEEE 1394-1995 High Performance Serial Bus

1.4 Functional Block Diagram

The functional block diagram of the TSB12LV31 is shown in Figure 2–1.

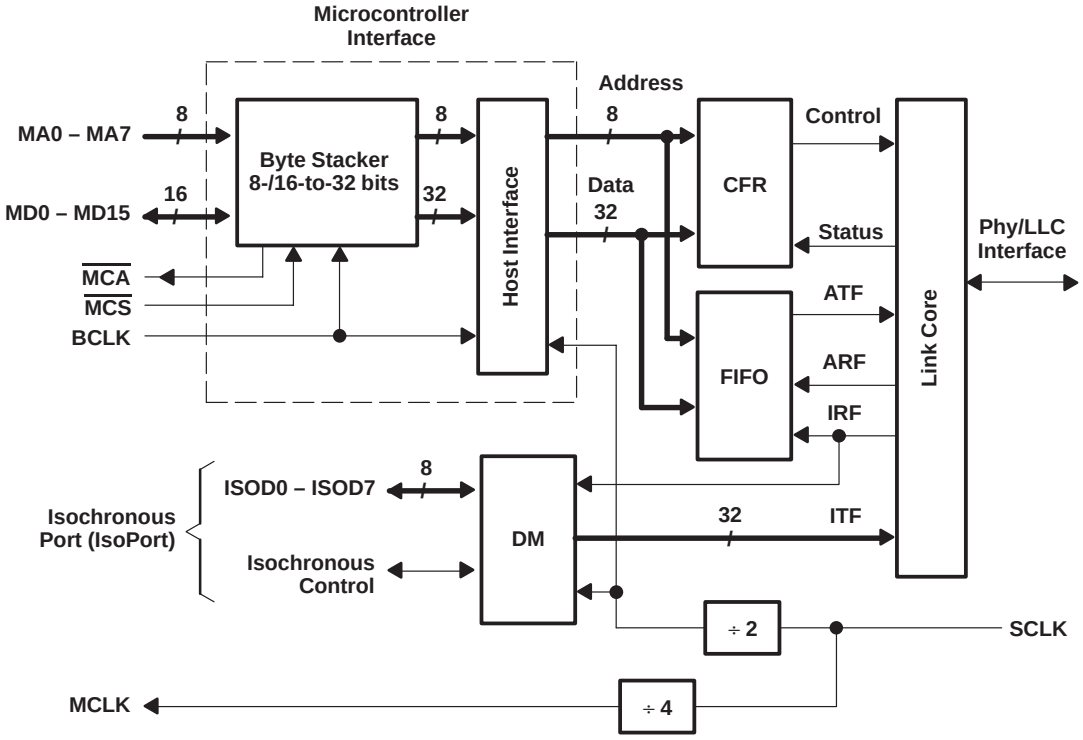


Figure 1–1. TSB12LV31 Functional Block Diagram

1.5 Terminal Assignments

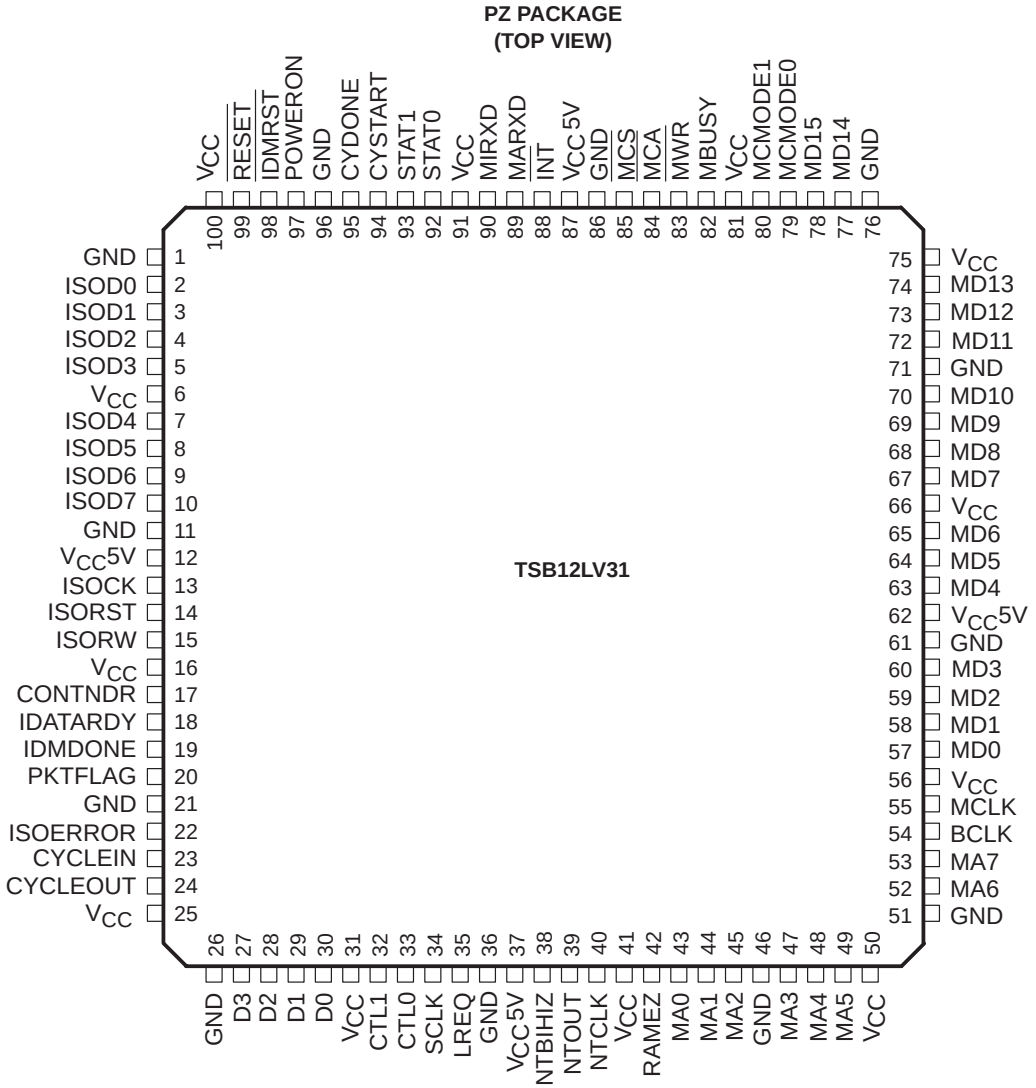


Figure 1–2. Terminal Assignments

1.6 Terminal Functions

The terminal functions are described in Table 1–1.

Table 1–1. Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Microcontroller Interface			
BCLK	54	I	Microcontroller clock. BCLK is supplied to the TSB12LV31 and has a maximum speed rating of 50 MHz.
$\overline{\text{INT}}$	88	O	Interrupt from the TSB12LV31 to microcontroller. When asserted low, $\overline{\text{INT}}$ indicates that an interrupt has occurred.
MA0 – MA7	43 – 45 47 – 49 52 – 53	I	Microcontroller address bus. MA0 is the MSB of these 8 bits.
MARXD	89	O	Asynchronous packet received indicator. MARXD pulses for one ISOCK cycle.
MBUSY	82	I	Microcontroller busy indicator. When MBUSY is asserted high, the TSB12LV31 returns an acknowledge packet with a busy code even when the GRF is not full.
$\overline{\text{MCA}}$	84	O	Microcontroller cycle acknowledge. When asserted low, $\overline{\text{MCA}}$ signals an acknowledge of the microcontroller cycle from the TSB12LV31.
MCLK	55	O	General-purpose clock output. MCLK is equal to SCLK/4, which is 12.288 MHz nominal.
MCMODE0 MCMODE1	79 80	I	Microcontroller mode select: 00: 16-bit data bus (MD0 – MD15), CS/CA handshake mode 01: 16-bit data bus (MD0 – MD15), fixed CS/CA timing 10: 8-bit data bus (MD8 – MD15), CS/CA handshake mode 11: 8-bit data bus (MD8 – MD15), fixed CS/CA timing
$\overline{\text{MCS}}$	85	I	Microcontroller cycle start. When asserted low, $\overline{\text{MCS}}$ signals the microcontroller cycle start.
MD0 – MD7	57 – 60 63 – 65 67	I/O	Microcontroller data bus. MD0 – MD7 are the MSBs of MD. MD0 is the MSB of these 8 bits.
MD8 – MD15	68 – 70 72 – 74 77 – 78	I/O	Microcontroller data bus. MD8 – MD15 are the LSBs of MD. MD8 is the MSB of these 8 bits.
MIRXD	90	O	Isochronous packet received indicator. MIRXD pulses for one ISOCK cycle.
$\overline{\text{MWR}}$	83	I	Microcontroller write/read indicator. When asserted high, $\overline{\text{MWR}}$ indicates a read to the TSB12LV31. When asserted low, $\overline{\text{MWR}}$ indicates a write.

Table 1–1. Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
IsoPort Interface			
IDATARDY	18	I	External isochronous data is ready. IDATARDY is a handshaking signal used for isochronous transmit. When data is ready for transmiting IDATARDY must be asserted high. IDMDONE is asserted low indicating that the transmitter is ready to accept data. At the conclusion of the entire block transmit, IDMDONE is asserted high and IDATARDY is asserted low.
IDMDONE	19	O	Isochronous transfer has completed. IDMDONE is a handshaking signal used for isochronous transmit. When data is ready for transmiting IDATARDY must be asserted high. IDMDONE is asserted low indicating that the transmitter is ready to accept data. At the conclusion of the entire block transmit, IDMDONE is asserted high and IDATARDY is asserted low.
$\overline{\text{IDMRST}}$	98	I	Reset for isochronous DMA state machine, active low. $\overline{\text{IDMRST}}$ is valid for isochronous transmits only. It performs an immediate abort of any isochronous transmit activity.
ISOCK	13	O	IsoPort clock. Read Clock (25 Mhz)
ISOD0 – ISOD7	2 – 5 7 – 10	I/O	IsoPort data. ISOD0 – ISOD carry the IsoPort data. ISOD0 is the MSB.
ISOERROR	22	O	Isochronous error. When set, ISOERROR indicates an error in the received packet.
ISORST	14	O	Reset IsoPort Read address pointer to zero. The ISORST pulses for one ISOCK clock period when: • The transmitting node has one or more synchronous bits set in the Iso Header register **and** • The corresponding bit is also set in the ISyncRcvN field (see subsection 3.2.6) of the IsoPort Number register of the receiving mode. For isochronous transmit, ISORST pulses at the beginning of a new data block fetch sequence.
ISORW	15	O	Enable to increment external IsoPort address pointer. ISORW is valid for both transmit and receive. For transmit, ISORW goes high indicating that isochronous data is clocked-in from the IsoPort (ISOD0 – ISOD7) at the ISOCK clock rate. For receive, ISORW goes high and indicates that data is present on ISOD0 – ISOD7 and must be clocked out with ISOCK.
PKTFLAG	20	O	Packet flag. When set, PKTFLAG indicates the first or last quadlet of a packet
Phy Interface			
CTL0 CTL1	33 32	I/O	Control 1 and control 0 of the phy-link control bus. CTL0 is the MSB.
D0 – D3	30 – 27	I/O	Data 0–3 of the phy-link data bus. Data is expected on D0 and D1 at 100 Mbits/s and D0 – D3 at 200 Mbits/s. D0 is the MSB.
LREQ	35	O	LLC request to phy. LREQ makes bus requests and accesses the phy.
SCLK	34	I	System clock. SCLK is a 49.152-MHz clock from the phy and from which the 24.576-MHz clock is generated.

Table 1–1. Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Miscellaneous Functions			
CONTNDR	17	I	Bus contender. When asserted, this node is designated as a contender for Isochronous Resource Manager or Bus Manager functions. The state of CONTNDR must match the state of the phy contender terminal.
CYCLEIN	23	I	Cycle in. This input is an optional external 8-kHz clock used as the cycle clock, and it should only be used if attached to the cycle-master node. It is enabled by the cycle source bit and should be tied high when not used.
CYCLEOUT	24	O	Cycle out. This output is the LLC version of the cycle clock. It is based on the timer controls and received cycle-start messages.
CYDONE	95	O	Isochronous cycle done indicator. CYDONE pulses for one ISOCK cycle.
CYSTART	94	O	Isochronous cycle start indicator. CYSTART pulses for one ISOCK cycle.
GND	1,11,21 26,36,46 51,61,71 76,86,96		Ground reference
NTBIHIZ	38	I	NAND tree bidirectional 3–state output. When NTBIHIZ is low, the bidirectional I/Os operate in a normal state. When NTBIHIZ is high, the bidirectional I/Os are in the 3–state output mode. This is a manufacturing test mode and should be grounded under normal operating conditions.
NTCLK	40	I	NAND clock input. The NAND-tree clock is used for V_{IH} and V_{IL} manufacturing tests. This input should be grounded under normal operating conditions.
NTOUT	39	O	NAND tree output. This output should remain open under normal operating conditions.
POWERON	97	O	Link power-on indicator (BCLK/32 square wave)
RAMEZ	42	I	RAM 3-state enable. When RAMEZ is low, the FIFOs are enabled. When RAMEZ is high, the FIFOs are 3-state outputs. This is a manufacturing test mode condition and should be grounded under normal operating conditions.
$\overline{\text{RESET}}$	99	I	Reset (active low). $\overline{\text{RESET}}$ is the asynchronous reset to the LLC.
STAT0 STAT1	92 93	O	Status signal. STATn is the output signal selected with the CFR address 20h (see Table 1–2).
V_{CC}	6,16,25 31,41,50 56,66,75 81,91,100		3.3-V (±0.3 V) power supplies
$V_{CC}5V$	12,37,62 87		5.0-V (±0.5-V) power supplies. $V_{CC}5V$ is 3.3 V (±0.3 V) on a 3-V only system.

1.6.1 STAT0 and STAT1 Programming

STAT0 and STAT1 are programmable output terminals. Each terminal can be independently programmed to show one of eight possible internal hardware statuses. STAT0 is controlled by StatSel0 (see subsection 3.2.7). STAT1 is controlled by StatSel1 (see subsection 3.2.7).

Table 1–2. STAT0 and STAT1 Programming

StatSel0 or StatSel1			STAT0/STAT1	DESCRIPTION
0	0	0	GRF full (default setting for STAT0)	GRF full is set when the value of GRF Remain = 0 (see subsection 3.2.13).
0	0	1	GRF empty	GRF empty is set when the size of the GRF is equal to the value of GRF Remain (see subsection 3.2.13).
0	1	0	ATF full	ATF full is set when the value of ATF Remain = 0 (see subsection 3.2.13).
0	1	1	ATF empty (default setting for STAT1)	ATF empty is set when the size of the ATF is equal to the value of ATF Remain (see subsection 3.2.13).
1	0	0	Bus Reset	Bus reset is set for one ISOCK cycle when a bus reset is detected.
1	0	1	Arbitration Reset gap	Arbitration reset gap is set for one ISOCK cycle when an arbitration reset gap is detected.
1	1	0	Subaction gap	Subaction gap is set for one ISOCK cycle when a subaction gap is detected.
1	1	1	Isochronous transmit buffer empty	Isochronous transmit buffer empty is set when an entire packet has been transmitted or, conversely, is low indicating that a packet is in the process of being transmitted.

2 Architecture

2.1 Functional Block Diagram

The functional block diagram of the TSB12LV31 is shown in Figure 2–1.

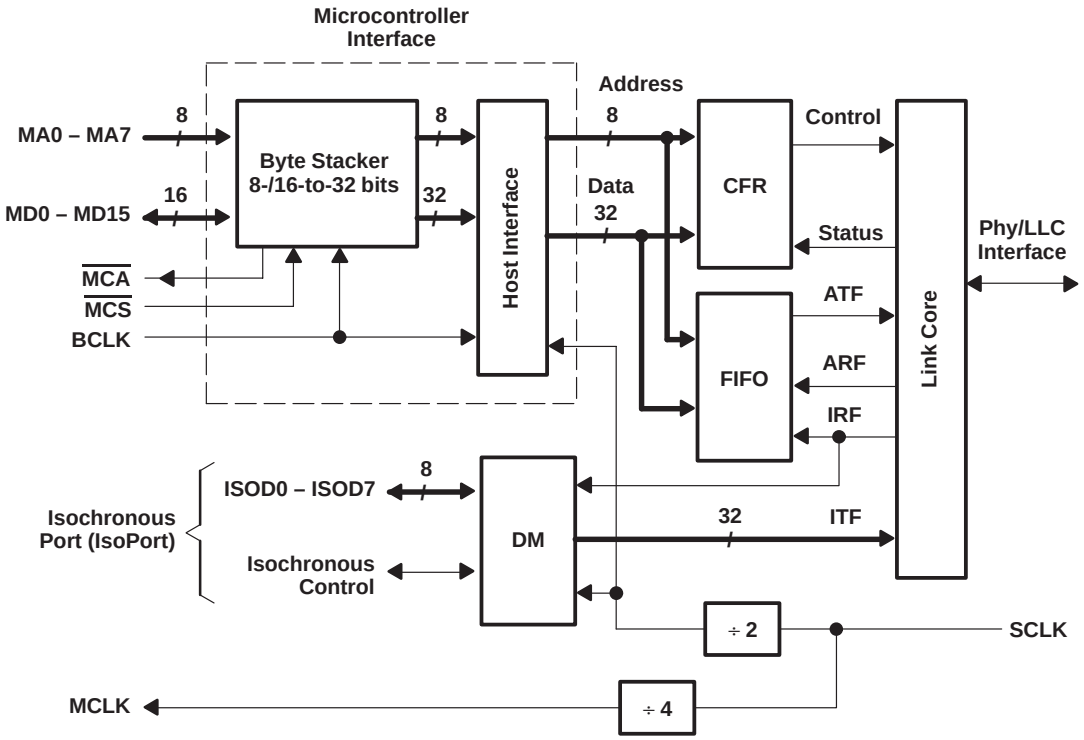


Figure 2–1. TSB12LV31 Functional Block Diagram

2.1.1 FIFO

The internal physical FIFO can be partitioned into two logical FIFOs. Each FIFO is programmable in size from 0 to 50 quadlets. For a given combination of FIFO sizes, the sum total of the two FIFO sizes must be less than or equal to 50 quadlets.

2.1.2 Microcontroller Interface

All microcontroller reads/writes are initiated by the microcontroller. Microcontroller modes of operation are shown in Figure 2–2, Figure 2–4, and Figure 2–5. Microcontroller operational protocol is described in Figure 2–7 and Figure 2–8. Microcontroller write/read timing is shown in Figure 4–1 and Figure 4–3.

2.1.2.1 Byte Stacker/Host Interface

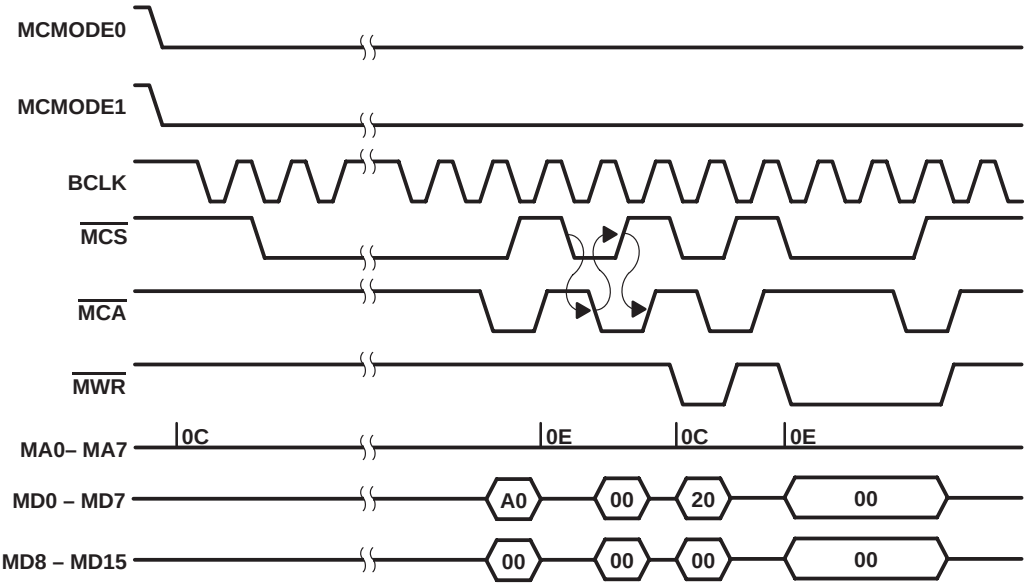
The byte stacker allows the TSB12LV31 to be easily connected to most host processors. The byte stacker consists of a programmable 8-/16-bit data bus and an 8-bit address bus. The TSB12LV31 uses cycle-start and cycle-acknowledge handshake signals to allow the local bus clock and the 1394 clock to be asynchronous to one another. The TSB12LV31 is interrupt driven to reduce polling.

2.1.2.2 Microcontroller Handshake Mode

Figure 2–2 shows a typical handshake sequence in doublet (16-bit) mode for a read followed by a write. In this example, the quadlet value A0 00 00 00h is being read from the configuration register 0Ch followed immediately by a write to the same register with the value 20 00 00 00h. Also see Figure 6–1 and Figure 6–2.

The handshake mode timing sequence is as follows:

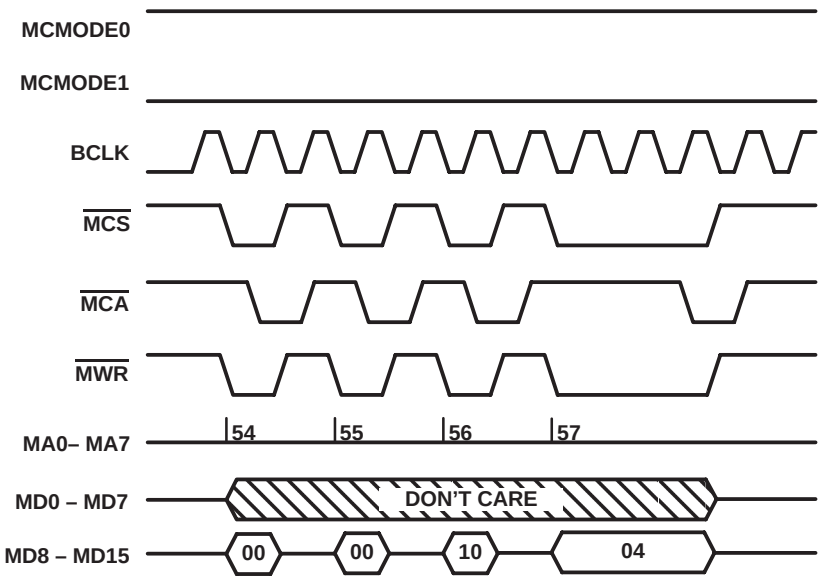
1. The host takes $\overline{\text{MCS}}$ low to signal start of access.
2. The TSB12LV31 takes $\overline{\text{MCA}}$ low to signal that the requested operation is complete.
3. The host takes $\overline{\text{MCS}}$ high to signal the end of the access.
4. The TSB12LV31 takes $\overline{\text{MCA}}$ high to acknowledge the end of the access.



NOTE A: MCMODE0 = 0, MCMODE1 = 0 handshake read/write

Figure 2–2. Typical Handshake Doublet-Mode Timing Waveforms

Figure 2–3 shows a typical handshake sequence in byte (8-bit) mode for a write operation. In this example, the quadlet value 00 00 10 04h is being written to the configuration register 54h. Note that the most significant byte of the data bus, MD0 – MD7, is not used in this mode. Also see Figure 6–1 and Figure 6–2.



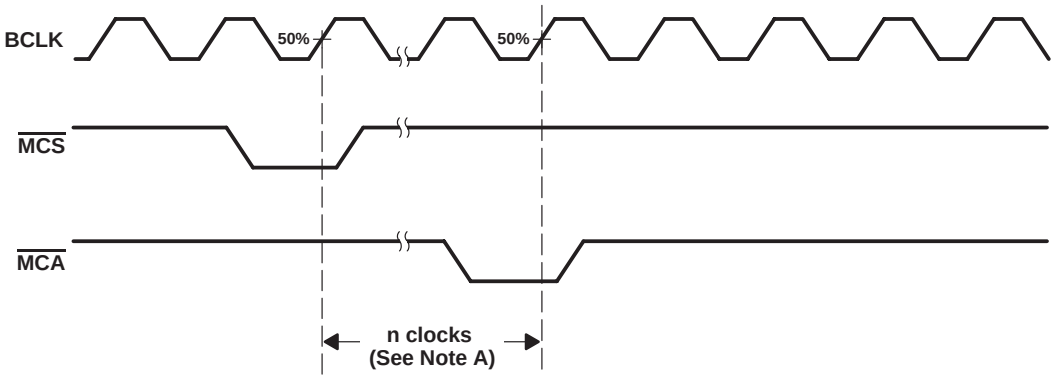
NOTE A: MCMODE0 = 1, MCMODE1 = 0 handshake byte write

Figure 2–3. Typical Handshake Byte-Mode Timing Waveforms

2.1.2.3 Microcontroller Pulse Mode

Figure 2–4 shows typical timing in pulse mode. The pulse-mode timing sequence is as follows:

1. The host pulses $\overline{\text{MCS}}$ low for one clock cycle to signal the start of the access.
2. After n clocks, the TSB12LV31 pulses $\overline{\text{MCA}}$ low for one clock cycle to signal that the requested operation is complete.



NOTE A: In this figure, n clocks is determined by clock synchronization and by which byte of the quadlet is being addressed.

Figure 2–4. Pulse Mode Timing Waveforms

2.1.2.4 Microcontroller 16-Bit Pulse Mode with Fixed Timing

Figure 2–5 shows a pulse with a fixed timing sequence in doublet (16-bit) mode for a write operation with XtendClk set to 0. In this example, the quadlet value 00 0C 13 1Ch is being written to the configuration register 5Ch. Also see Figure 6–1 and Figure 6–2.

The timing sequence for pulse mode with fixed timing is as follows:

1. The host pulses $\overline{\text{MCS}}$ low for one clock cycle to signal the start of the access
2. After n clocks, the TSB12LV31 pulses $\overline{\text{MCA}}$ low for one clock cycle to signal the requested operation is complete.

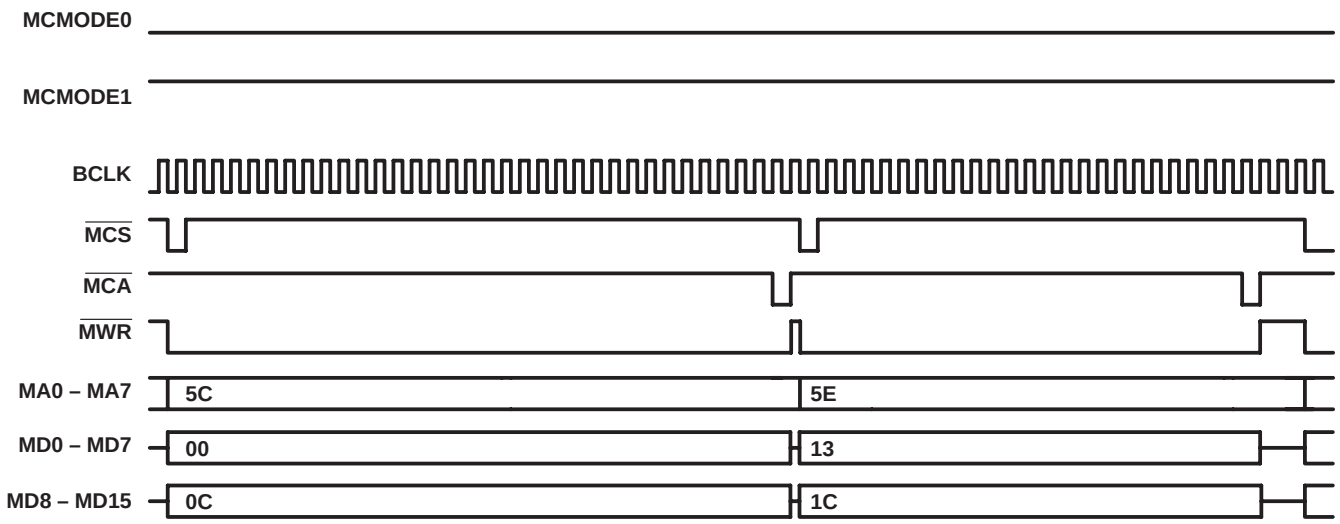


Figure 2–5. Timing Waveforms for 16-Bit Pulse Mode with Fixed Timing

2.1.2.5 Microcontroller 8-Bit Pulse Mode with Fixed Timing

Figure 2–6 shows a pulse with a fixed timing sequence in byte (8-bit) mode for a write operation with XtendClk set to 11h. In this example, the quadlet value 00 00 08 02h is being written to the configuration register 54h. Note that MD0 – MD7 is not used in this mode (see Figure 6–1 and Figure 6–2).

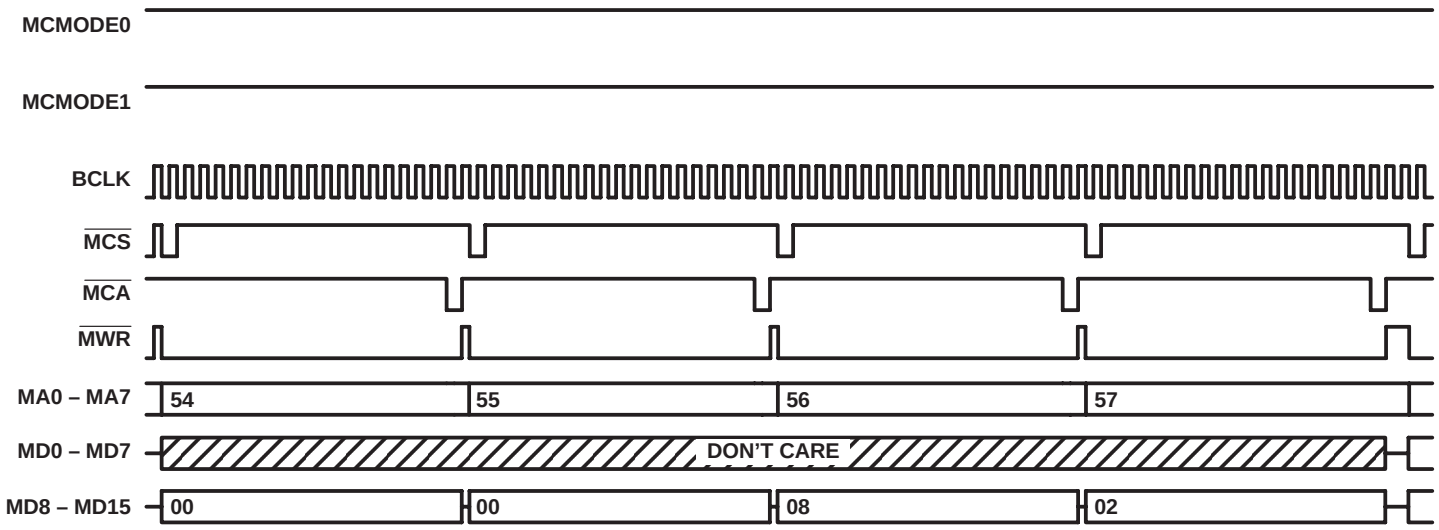


Figure 2–6. Timing Waveforms for 8-Bit Pulse Mode with Fixed Timing

2.1.2.6 Microcontroller Byte Stack (Write) Operation

The microcontroller byte stack (write) protocol is shown in Figure 2–7.

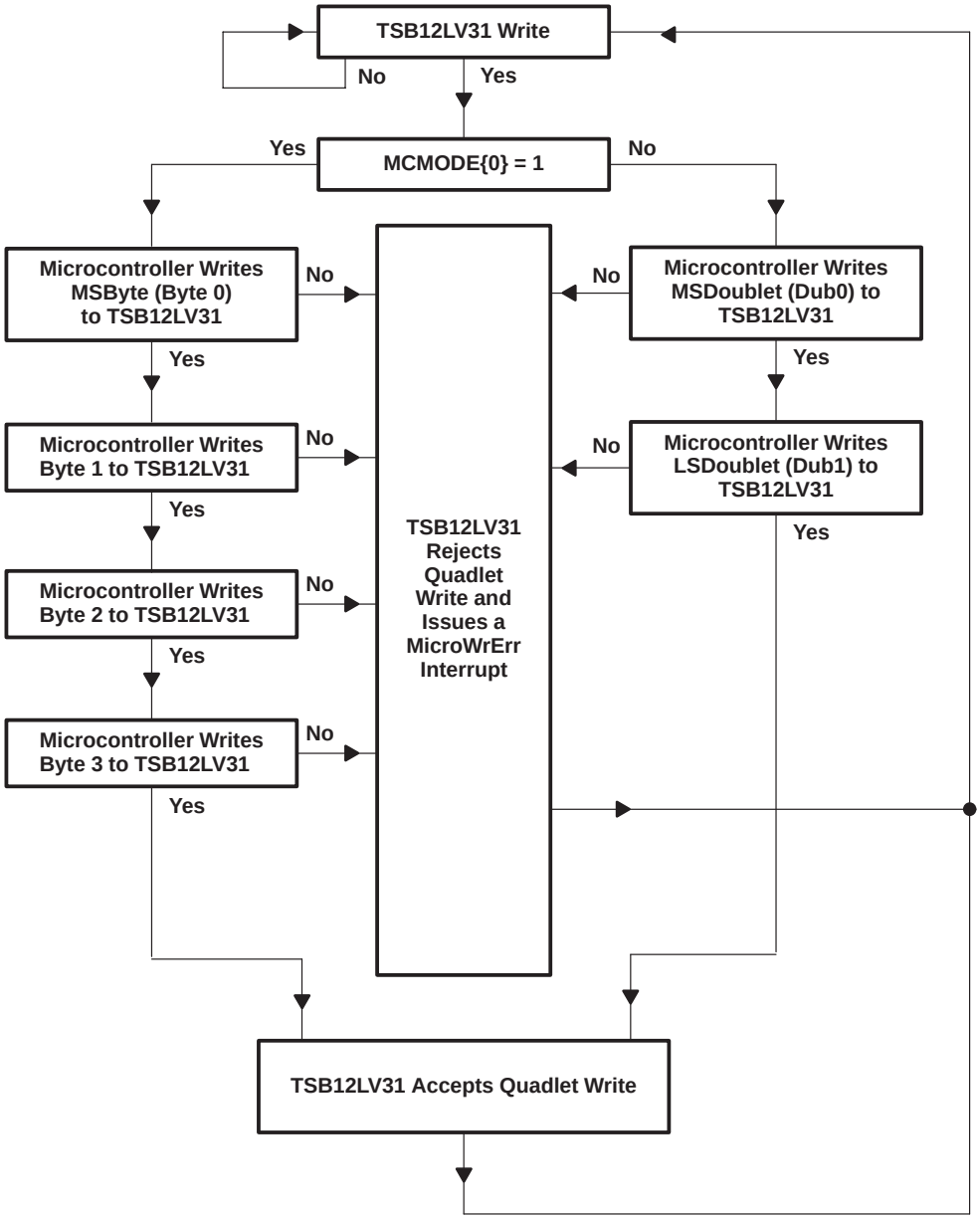


Figure 2–7. Microcontroller Byte Stack Operation (Write)

2.1.2.7 Microcontroller Byte Unstack (Read)

The microcontroller byte unstack (read) protocol is shown in Figure 2–8.

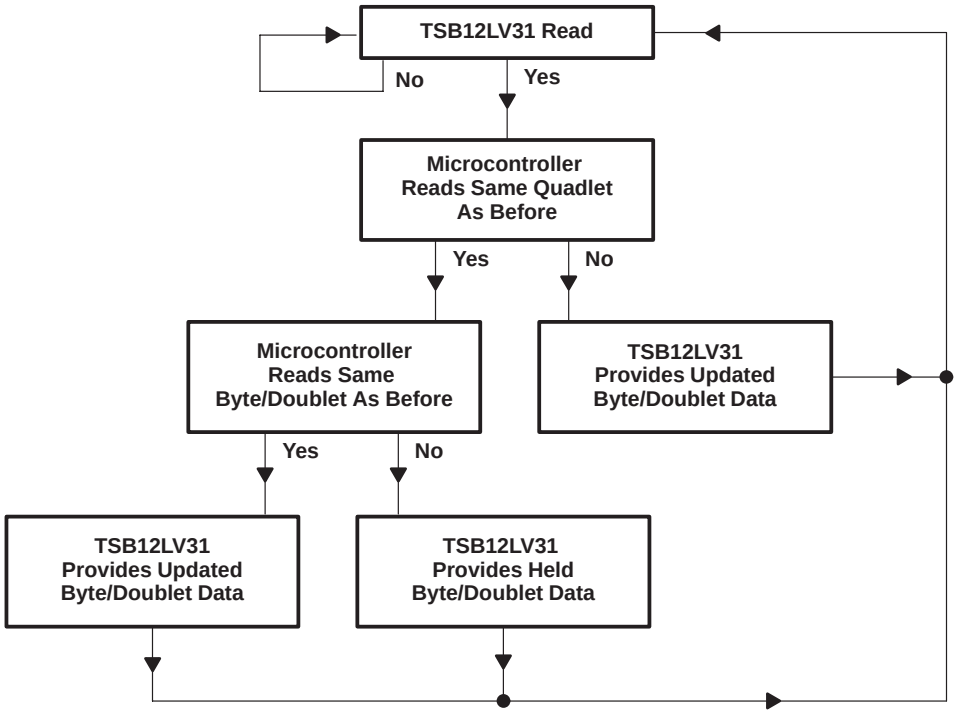


Figure 2–8. Microcontroller Byte UnStack Operation (Read)

2.1.3 Link Core

This section describes the link core components and operations. Figure 2–9 shows the link core components.

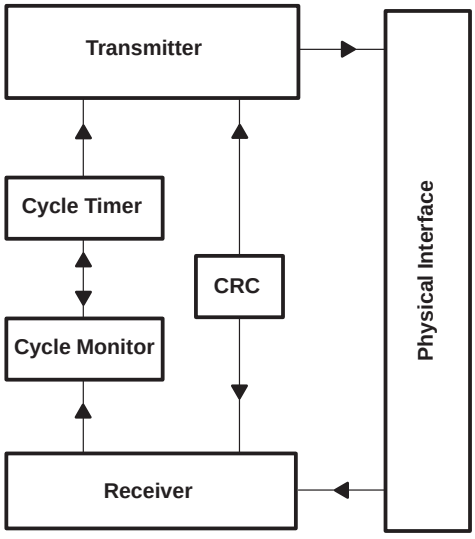


Figure 2–9. Link Core Components

2.1.3.1 Physical Interface

The physical (phy) interface provides phy-level services to the transmitter and receiver. This includes gaining access to the serial bus, sending packets, receiving packets, and sending and receiving acknowledge packets.

The phy interface module also interfaces to the phy chip and conforms to the phy-LLC interface specification described in Annex J of the IEEE-1394 standard.

2.1.3.2 Transmitter

The transmitter retrieves data from either the asynchronous transmit FIFO (ATF) or the IsoPort and creates correctly formatted serial-bus packets to be transmitted through the phy interface. When data is present at the ATF interface to the transmitter, the TSB12LV31 phy interface arbitrates for the serial bus and sends a packet. When data is present at the IsoPort, the TSB12LV31 arbitrates for the serial bus during the next isochronous cycle. The transmitter autonomously sends the cycle-start packets when the chip is a cycle master.

2.1.3.3 Receiver

The receiver takes incoming data from the phy interface and determines if the incoming data is addressed to this node. When the incoming packet is addressed to this node, the CRC of the packet is checked. If the header CRC is good, the header is confirmed in the general-receive FIFO (GRF). For block and isochronous packets, the remainder of the packet is confirmed one quadlet at a time. The receiver places a status quadlet in the GRF after the last quadlet of the packet is confirmed in the GRF. The status quadlet contains the error code for the packet. The error code is the acknowledge code that is sent for that packet. For broadcast packets that do not need acknowledge packets, the error code is the acknowledge code that would have been sent. This acknowledge code tells the transaction layer whether or not the data CRC is good or bad. When the header CRC is bad, the header is flushed and the rest of the packet is ignored.

When a cycle-start message is received, it is detected and the cycle-start message data is sent to the cycle timer. The cycle-start messages are not placed in the GRF like other quadlet packets. At the end of an isochronous cycle and if the cycle mark enable (CyMrkEn) bit of the control register is set, the receiver inserts a cycle-mark packet in the GRF to indicate the end of the isochronous cycle.

2.1.3.4 Cycle Timer

The cycle timer is used by nodes that support isochronous data transfer. The cycle timer is a 32-bit cycle-timer register. Each node with isochronous data-transfer capability has a cycle-timer register as defined in 1394. In the TSB12LV31, the cycle-timer register is implemented in the cycle timer and is located in the IEEE-1212 initial register space at location 200h and can also be accessed through the local bus at address 14h. The low-order 12 bits of the timer are a modulo 3072 counter, which increments once every 24.576-MHz clock periods (or 40.69 ns). The next 13 higher-order bits are a count of 8,000-Hz (or 125-μs) cycles, and the highest 7 bits count seconds.

The cycle timer contains the cycle-timer register. The cycle-timer register consists of three fields: cycle offset, cycle count, and seconds count. The cycle timer has two possible sources. First, when the cycle source (CySrc) bit in the configuration register is set, then the CYCLEIN input causes the cycle count field to increment for each positive transition of the CYCLEIN input (8 kHz) and the cycle offset resets to all zeros. CYCLEIN should only be the source when the node is the cycle master. When the cycle-count field increments, CYCLEOUT is generated. The timer can also be disabled using the cycle-timer-enable bit in the control register.

The second cycle-source option is when the CySrc bit is cleared. In this state, the cycle-offset field of the cycle-timer register is incremented by the internal 24.576-MHz clock. The cycle timer is updated by the reception of the cycle-start packet for the noncycle master nodes. Each time the cycle-offset field rolls over, the cycle-count field is incremented and the CYCLEOUT signal is generated. The cycle-offset field in the cycle-start packet is used by the cycle-master node to keep all nodes in phase and running with a nominal isochronous cycle of 125 μs.

CYCLEOUT indicates to the cyclemaster node that it is time to send a cycle-start packet. And, on noncyclemaster nodes, CYCLEOUT indicates that it is time to expect a cycle-start packet. The cycle-start bit is set when the cycle-start packet is sent from the cyclemaster node or received by a noncyclemaster node.

2.1.3.5 Cycle Monitor

The cycle monitor is only used by nodes that support isochronous data transfer. The cycle monitor observes chip activity and handles scheduling of isochronous activity. When a cycle-start message is received or sent, the cycle monitor sets the cycle-started interrupt bit. It also detects missing cycle-start packets and sets the cycle-lost interrupt bit when this occurs. When the isochronous cycle is complete, the cycle monitor sets the cycle-done-interrupt bit. The cycle monitor instructs the transmitter to send a cycle-start message when the cyclemaster bit is set in the control register.

2.1.3.6 Cyclic Redundancy Check (CRC)

The CRC module generates a 32-bit CRC for error detection. This is done for both the header and the data. The CRC module generates the header and data CRC for transmitting packets and checks the header and data CRC for received packets (see the IEEE-1394 standard for details on the generation of the CRC†).

2.1.4 Data Mover (DM) Control

The following sections describe the transmit and receive data mover control.

2.1.4.1 Isochronous Transmit DM

In order to successfully transmit an isochronous packet, the following must occur:

1. The external source for the isochronous data must be ready to begin transmitting one byte (at 200 Mbits/s operation) of isochronous data per ISOCK clock cycle.
2. The transmitter must be enabled by setting the TxEn bit (see subsection 3.2.3).
3. The isochronous mode must be set to transmit by setting the isomode bits to 00 (see subsection 3.2.15). This is the default value of the isomode bits.
4. The isodmen bit must be set (see subsection 3.2.15).
5. CFR must be programmed for the isochronous sequence that is about to start (see subsection 3.2.15 and subsection 3.2.16).

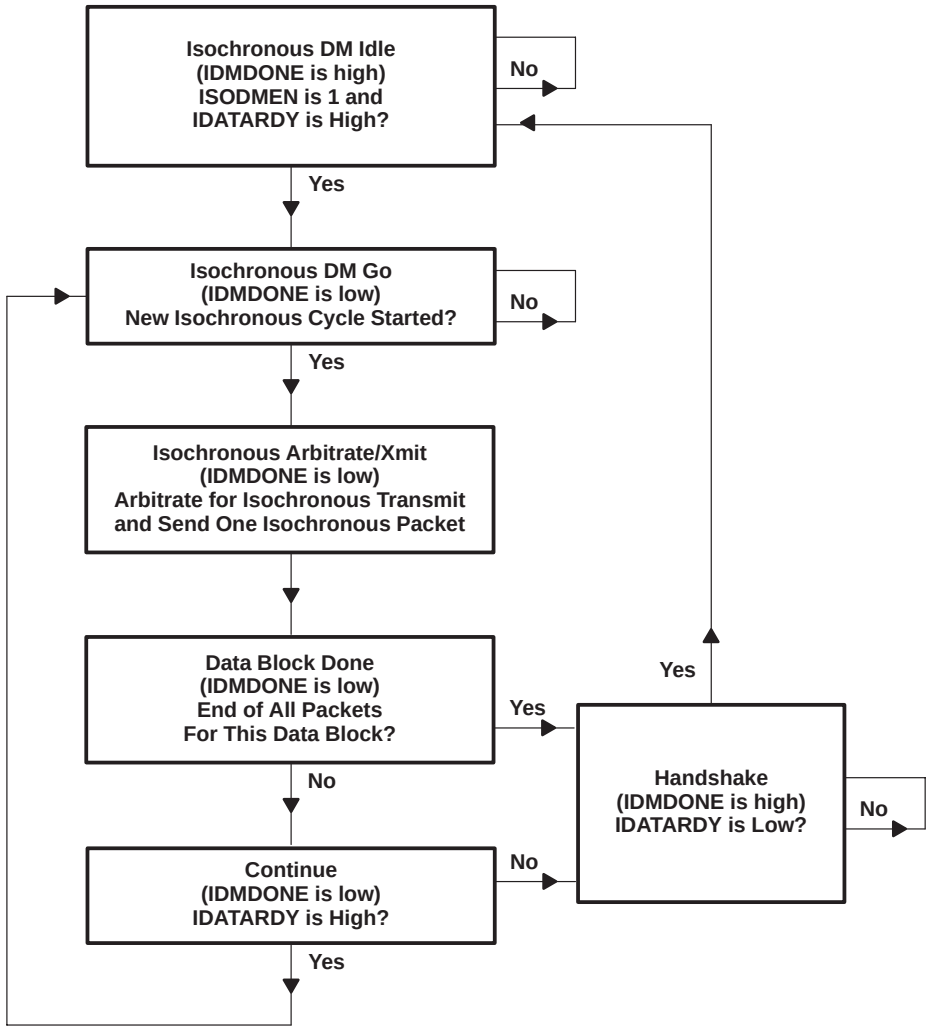
   For example:
   When CFR= 00 00 18 03h, this indicates that three quadlets make up a packet and two packets define a block of data (see subsection 3.2.15).

   When CFR = 00 0C 01 18h, this indicates that the channel addressed is channel 1, the Tag field is not used, the speed to be used is 200 Mbits/s, and the Sync field is set (see subsection 3.2.16 and subsection 3.2.3).

   The isochronous header is defined by the Iso Header register (see subsection 3.2.16) and is inserted into the isochronous stream. The CRC is generated and transmitted along with the header and the data.
6. IDATARDY is asserted high to start the isochronous transmit sequence.

The isochronous transmit DM reads digital data from the IsoPort (ISOD0 – ISOD7) and passes it to the 1394 isochronous transmit interface in accordance with Figure 2–10. The isochronous data path is shown in Figure 2–11.

† This is the same CRC used by the IEEE802 LANs and the X3T9.5 FDDI.



NOTE A; ISODMEN is a Configuration register bit, IDATARDY is an input terminal, and IDMDONE is an output terminal.

Figure 2–10. Isochronous DM Flow Control (TSB12LV31 Transmit)

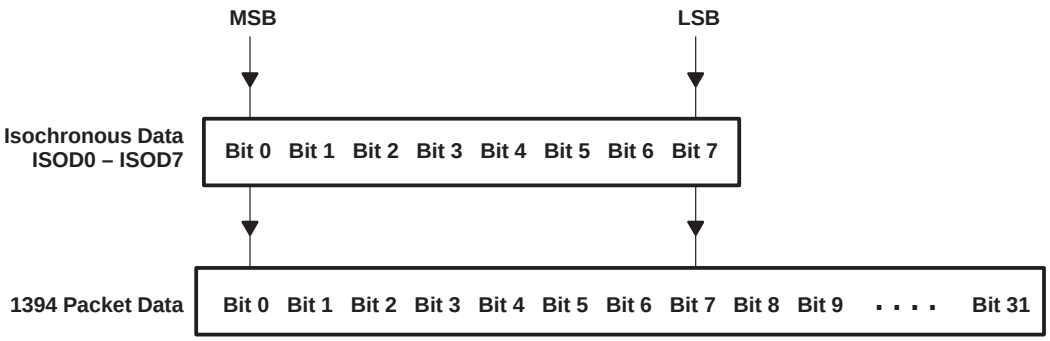


Figure 2–11. Isochronous Transmit Data Path

2.1.4.2 Isochronous Transmit Packet Structure

The isochronous packet structure is described in the following list and is shown in Table 2–1:

- 1394 isochronous header (data length, tg, channel, tcode, sy).
  Note that the microcontroller must calculate and supply the data length.
- Header CRC
- Data payload block (from ISOD0 – ISOD7)
- Data CRC

Table 2–1. Isochronous Transmit Packet Structure

Isochronous Packet Component	Source of Isochronous Packet Component
1394 Isochronous Header	Sourced from CFRs
Header CRC	Calculated and inserted by link core
Data Payload Block	Data presented to ISOD0–ISOD7 terminals
Data CRC	Calculated and inserted by link core

2.1.4.3 Isochronous Receive DM

The isochronous receive logic moves data from the 1394 bus (by way of the phy) to the IsoPort when the TSB12LV31 receiver is enabled (i.e., RxEn is set in the control register, see subsection 3.2.3), and isochronous mode is set to receive (i.e., IsoMode = 01 in the IsoMode register, see subsection 3.2.16), **and**

- Bit IRcvall is set (IsoPort number register, see subsection 3.2.6) **or**
- IRP1En or IRP2En (see subsection 3.2.3) is set and the incoming isochronous packet matches IR Port1 or IR Port2 (see subsection 3.2.6) **or**
- MOnTag bit (see subsection 3.2.6) is set, IRP1En or IRP2En (see subsection 3.2.3) is set and the incoming isochronous packet matches IR Port1 or IR Port2 (see subsection 3.2.6), and the tag field matches the incoming isochronous packet header Tag field.

The isochronous receive logic moves data from the 1394 bus, by way of the phy, to the GRF when:

- The TSB12LV31 receiver is enabled (i.e., RxEn is set in the Control register, see subsection 3.2.3), **and**
- The GRF size in the GRF Status register (see subsection 3.2.12) is set to a value greater than 0, **and**
- One of the following occurs:
  - The IRcvall bit is set in IsoPort Number register (see subsection 3.2.6), **or**
  - The IRP1En or IRP2En bit (see subsection 3.2.3) is set and the incoming isochronous packet matches IR PORT1 or IR PORT2 (see subsection 3.2.6), **or**
  - The MOnTag bit (see subsection 3.2.6) is set, the previous item is satisfied, and the Tag field (see subsection 3.2.6) matches the incoming Tag field of the isochronous packet header.

The header and the data are received by the IsoPort as well as by the the GRF (when applicable). The trailer is inserted by the hardware and is also available at the port and GRF. The CRC is not saved in the GRF nor is it available to the IsoPort (see Figure 6–6).

3 Internal Registers

3.1 Memory and Configuration Address Space Register Map

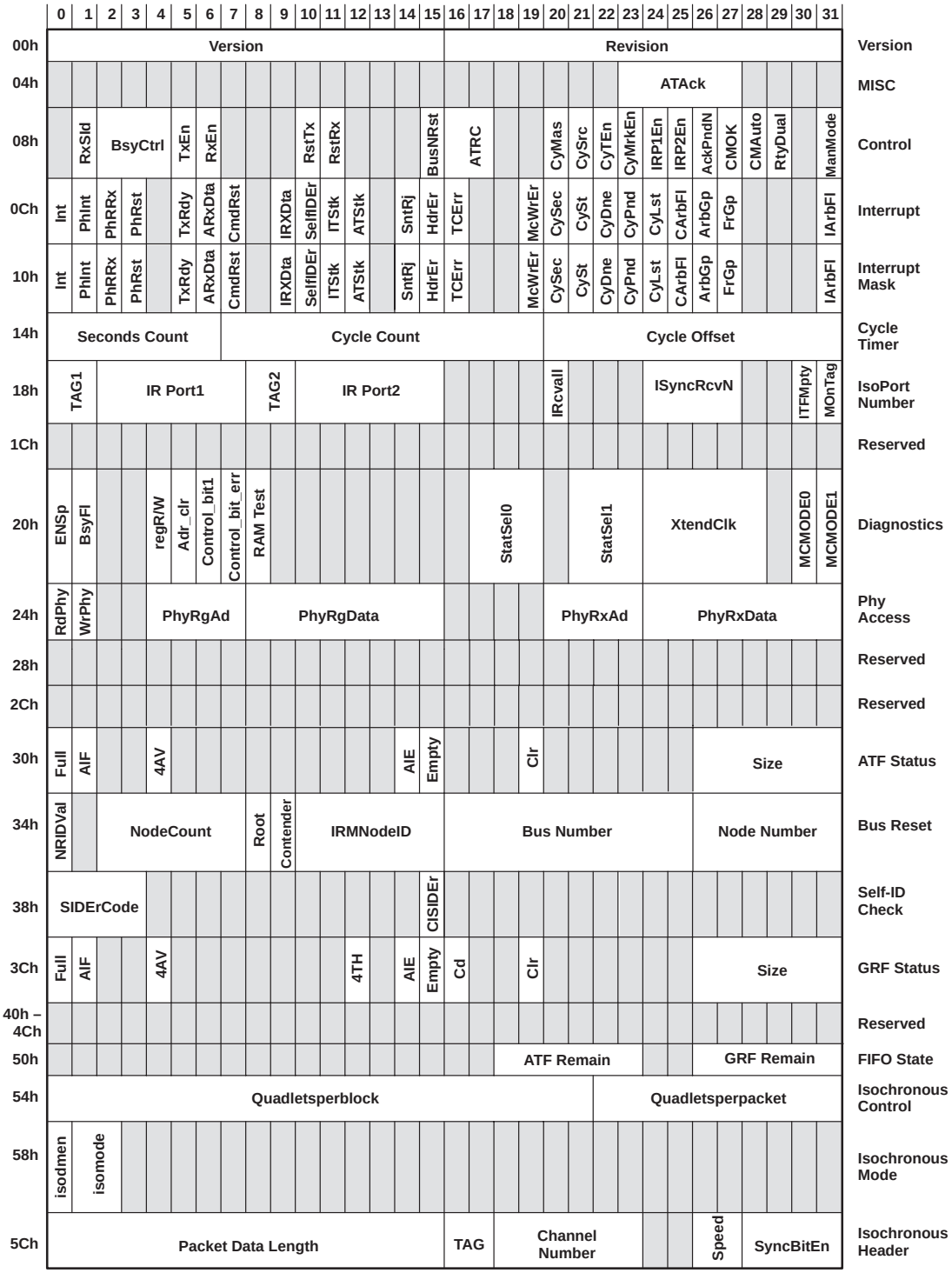
Table 3–1 lists the memory and configuration address space sections and their locations.

Table 3–1. Memory and Configuration Address Space Map

ADDRESS FROM MA0 – MA7	CONFIGURATION ACCESS ADDRESS SPACE
00h 50h	1394 LLC and phy configuration registers
54h 5Ch	Isochronous DM configuration registers
80h CCh	FIFO configuration registers
D0h F8h	Reserved

3.1.1 TSB12LV31 Configuration Registers

The TSB12LV31 CFR map is shown in Figure 3–1.



NOTE A: All gray areas (bits) are reserved bits.

Figure 3–1. Configuration Register (CFR) Map

3.2 Configuration Register Definitions

3.2.1 Version Register @00h

The Version register @00h contains the value CE02_1394h and is read only.

3.2.2 MISC Register @04h

The MISC register @04h is shown in Table 3–2.

Table 3–2. MISC Register Field Descriptions @04h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0 – 22		Reserved	Reserved
23 – 27	ATAck	Address transmitter acknowledge received	ATAck is the last acknowledge received by the transmitting node in response to a packet sent from the asynchronous transmit FIFO. These bits can be programmed only when the regR/W bit has been set in the Diagnostics register @20h.
28 – 31		Reserved	Reserved

3.2.3 Control Register @08h

The Control register dictates the basic operation of the TSB12LV31. The Control register @08h is shown in Table 3–3. The initial value is 0200_0000h after device reset.

Table 3–3. Control Register Field Descriptions @08h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION	
0		Reserved	Reserved	
1	RxSId	Received self-ID packets	When RxSId is set, the self-identification packets generated by phy chips during the bus initialization are received and placed into the GRF as a single packet. The default setting of bit 1 is 1.	
2–4	BsyCtrl	Busy control	BsyCtrl controls which busy status the chip returns to incoming packets. The field is defined in the following:	
			000	Follow normal busy/retry protocol, only send busy when necessary.
			001	Send busyA when it is necessary to send a busy acknowledge.
			010	Send busyB when it is necessary to send a busy acknowledge.
			011	Reserved
			100	Send a busy acknowledge to all incoming packets following the normal busy/retry protocol.
			101	Send a busy acknowledge to all incoming packets by sending a busyA acknowledge.
			110	Send a busy acknowledge to all incoming packets by sending a busyB acknowledge.
			111	Reserved
			When retry_X is received and the receiving node needs to send a busy acknowledge signal, it sends an ack_busy_X signal.	
5	TxEn	Transmitter enable	When TxEn is cleared, the transmitter does not arbitrate or send packets. This bit is cleared following a bus reset.	
6	RxEn	Receiver enable	When RXEn is cleared, the receiver does not receive any packets. This bit is not affected by a bus reset and is set after a power-on reset.	

Table 3–3. Control Register Field Descriptions @08h (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
7 – 9		Reserved	Reserved
10	RstTx	Reset transmitter	When RstTx is set, the entire transmitter resets synchronously. This bit clears itself.
11	RstRx	Reset receiver	When RstRx is set, the entire receiver resets synchronously. This bit clears itself.
12 – 14	Reserved		Reserved
15	BusNRst	Bus number reset enable	When this enable is set to high, the Bus Number field clears to 3FFh when a local bus reset is received.
16 – 17	ATRC	AT retry code	ATRC contains the last retry code received. This code is logically ORed with the retry code field (00) in the transmit packet, and the packet is resent. This alleviates the need to change the retry code in the transmit packet. The retry encoding follows the IEEE-1394 standard 7.1v1. The retry code is as follows:
			00 retry_o (new)
			01 retry_X
			10 retry_A
			11 retry_B
18 – 19	Reserved		Reserved
20	CyMas	Cycle master	When CyMas is set and the TSB12LV31 is attached to the root phy, the cyclemaster function is enabled. When the cycle_count field of the Cycle Timer register increments, the transmitter sends a cycle-start packet.
21	CySrc	Cycle source	When CySrc is set, the cycle_count field increments and the cycle_offset field resets for each positive transition of CYCLEIN. When CySrc is cleared, the cycle_count field increments when the cycle_offset field rolls over.
22	CyTEn	Cycle timer enable	When CyTEn is set, the cycle_offset field increments.
23	CyMrkEn	Cycle mark enable	When CyMrkEn is set, cycle marks are inserted into the GRF at the end of each isochronous cycle (TSB12LV31 compatible). When CyMrkEn is cleared, no cycle marks are generated.
24	IRP1En	IR port 1 enable	When IRP1En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port1 field.
25	IRP2En	IR port 2 enable	When IRP2En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port2 field.
26	AckPndN	Acknowledge pending enable	When AckPndN is enabled, incoming asynchronous packets are acknowledged as pending.
27	CMOK	Cycle master candidate	When CMAuto is high and CMOK is high, the TSB12LV31 automatically enables CyMas when the root is following a bus reset.
28	CMAuto	Auto set cycle master	When CMAuto is high and CMOK is high, the TSB12LV31 automatically enables CyMas when the root is following a bus reset.
29	RtryDual	Dual retry	When RtryDual is high, the TSB12LV31 uses the dual phase retry protocol. When RtryDual is low, the TSB12LV31 uses the single phase retry protocol.

Table 3–3. Control Register Field Descriptions @08h (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
30	Reserved		Reserved
31	ManMode	Manual mode	When set, ManMode allows a write to the node number of CFR@34h.

3.2.4 Interrupt/Interrupt Mask Register @0Ch/10h

The Interrupt/Interrupt Mask registers @0Ch/10h are shown in Table 3–4. The Interrupt and Interrupt Mask registers work in tandem to inform the host bus interface when the state of the TSB12LV31 changes. The interrupt is at address 0Ch and the interrupt mask is at address 10h. The power-up default for the Interrupt Mask register is 8000_1000h (i.e., interrupts are allowed, the microcontroller interrupt is allowed, and the Interrupt Mask register is fully read/writable).

Each bit of the Interrupt register represents a unique interrupt. A particular interrupt can be masked off when the corresponding bit in the Interrupt Mask register is 0.

The Interrupt register always shows the status of the individual bits even when the interrupt mask is off. For example, when the Interrupt Mask register is F77B_9FE1h (i.e., all interrupts except FairGap are allowed to generate an interrupt) and a Fair Gap occurred, the Interrupt register @0Ch would equal 000_0010h.

To clear an interrupt, write 1 to the corresponding interrupt bit (i.e., to clear a PhInt, write 4000_000h to 0Ch).

For testing, each interrupt bit can be set manually. This is done by first setting the regR/W bit @20h and then setting the individual interrupt bit. This is also true for bit 0 @0Ch. In this test mode, the Interrupt Mask register is irrelevant.

NOTE:
Never leave the regR/W bit set. This prevents normal interrupts. Always clear the regR/W bit for proper operation of this part.

Table 3–4. Interrupt/Interrupt Mask Register Field Descriptions @0Ch/10h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Int	Interrupt	Int contains the value of all interrupt and interrupt mask bits ORed together.
1	PhInt	Phy chip interrupt	When PhInt is set, the phy has signaled an interrupt through the phy interface.
2	PhyRRx	Phy register information received	When PhyRRx is set, a register value has been transferred to the Phy Access register (offset 24h) from the phy interface.
3	PhRst	Phy reset started	When PhRst is set, a phy-LLC reconfiguration has started (1394 bus reset).
4	Reserved		Reserved
5	TxRdy	Transmitter ready	When TxRdy is set, the transmitter is idle and ready.
6	ARxDta	Asynchronous data received	The receiver has confirmed asynchronous data.
7	CmdRst	Command reset received	When CmdRst is set, the receiver has been sent a quadlet write request addressed to the Reset_Start CSR register.
8	Reserved		Reserved
9	IRxDta	Isochronous re-ceived	The receiver has confirmed isochronous data.
10	SelfIDEr	Self-ID packet error	A Self-ID quadlet/packet with errors has been received.
11	ITStk	Transmitter is stuck (IT)	When ITStk is set, the transmitter has detected invalid data at the isochronous transmit-FIFO interface.

Table 3–4. Interrupt/Interrupt-Mask Register Field Descriptions @0Ch/10h (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
12	ATStk	Transmitter is stuck (AT)	When ATStk is set, the transmitter has detected invalid data at the asynchronous transmit-FIFO interface. If the first quadlet of a packet is not written to the ATF_First or ATF_First&Update, the transmitter enters a state denoted by an ATStuck interrupt. An underflow of the ATF also causes an ATStuck interrupt. When this state is entered, no asynchronous packets can be sent until the ATF is cleared by way of the CLR ATF control bit. Isochronous packets can be sent while in this state.
13	Reserved		Reserved
14	SntRj	Busy acknowledge sent by receiver	When SntRj is set, the receiver is forced to send a busy acknowledge to a packet addressed to this node because the GRF overflowed.
15	HdrEr	Header error	When HdrEr is set, the receiver detected a header CRC error on an incoming packet that may have been addressed to this node.
16	TCErr	Transaction code error	When TCErr is set, the transmitter detected an invalid transaction code in the data at the transmit-FIFO interface.
17 – 18	Reserved		Reserved
19	McWrEr	Microcontroller error	When McWrEr is set, the microcontroller quadlet write protocol has been violated.
20	CySec	Cycle second incremented	When CySec is set, the cycle-second field in the Cycle Timer register incremented. This occurs approximately every second when the cycle timer is enabled.
21	CySt	Cycle started	When CySt is set, the transmitter has sent or the receiver has received a cycle-start packet.
22	CyDne	Cycle done	When CyDne is set, an arbitration gap has been detected on the bus after the transmission or reception of a cycle-start packet. This indicates that the isochronous cycle is over.
23	CyPnd	Cycle pending	When CyPnd is set, the cycle timer offset is set to 0 (rolled over or reset) and remains set until the isochronous cycle ends.
24	CyLst	Cycle lost	When CyLst is set, the cycle timer has rolled over twice without the reception of a cycle-start packet. This occurs only when this node is not the cycle master.
25	CArbFl	Cycle arbitration failed	When CArbFl is set, the arbitration to send the cycle-start packet failed.
26	ArbGp	Arbitration gap	When ArbGp is set, the serial bus has been idle for an arbitration reset gap.
27	FrGp	Fair gap	When FrGp is set, the serial bus has been idle for a fair-gap time (subaction gap). This bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
28 – 30	Reserved		Reserved
31	IArbFl	Isochronous arbitration failed	When IArbFl is set, the arbitration to send an isochronous packet failed.

3.2.5 Cycle Timer Register @14h

The Cycle Timer register contains the seconds_count, cycle_count and cycle_offset fields of the cycle timer. The register is @14h and is read/write. This field is controlled by the cycle master, cycle source, and cycle timer enable bits of the Control register. Its initial value is 0000_0000h. The Cycle Timer register @14h is shown in Table 3–5.

Table 3–5. Cycle Timer Register Field Descriptions @14h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–6	seconds_count	Seconds count	1-Hz cycle timer counter
7–19	cycle_count	Cycle count	8,000-Hz cycle timer counter
20–31	cycle_offset	Cycle offset	24.576-MHz cycle timer counter

3.2.6 IsoPort Number Register @18h

The IsoPort Number register @18h is shown in Table 3–6.

Table 3–6. IsoPort Number Register Field Descriptions @18h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–1	TAG1	Tag Field 1	The TAG1 field can further qualify the isochronous reception.
2–7	IR Port1	Isochronous receive port 1 channel number	IR Port1 contains the channel number of the isochronous packets that the receiver accepts. The receiver accepts isochronous packets when IRP1En is set.
8–9	TAG2	Tag Field 2	The TAG2 field can further qualify the isochronous reception.
10–15	IR Port2	Isochronous receive port 2 channel number	IR Port2 contains the channel number of the isochronous packets that the receiver accepts. The receiver accepts isochronous packets when IRP2En is set.
16 – 19	Reserved		Reserved
20	IRcvall	Receive all isochronous packets	When the IRcvAll bit is set high, the TSB12LV31 receives all isochronous packets regardless of the channel number or tag number. The default is off.
21 – 23			Reserved
24 – 27	ISyncRcvN	Synchronous enable	In isochronous receive to IsoPort mode when the ISyncRcvN enable bits are high, the ISORST terminal pulses when an isochronous header is received with the corresponding synchronous bits set to 1 (see the synchronous enable field in Table 3–17). The default is 0000b.
28 – 29	Reserved		Reserved
30	ITFMpty	ITF empty	ITFMpty indicates the status of isochronous transmitter control. This bit is read only.
31	MOnTag	Match on tag	MOnTag is set, when the channel number matches the tag number. When set, MOnTag indicates that isochronous receive data is accepted. The default is off.

3.2.7 Diagnostics Register @20h

The Diagnostics register @20h is shown in Table 3–7.

Table 3–7. Diagnostics Register Field Descriptions @20h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	ENSp	Enable Snoop	When ENSp is set, the receiver accepts all packets on the bus regardless of address or format. The receiver uses the snoop data format defined in Section 4.4.
1	BsyFl	Busy flag	When BsyFl is set, the receiver sends an ack_busyB the next time the receiver must busy a packet. When cleared, the receiver sends an ack_busyA the next time the receiver must busy a packet. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
2 – 3	Reserved		Reserved
4	regR/W	Register read/write access	When regR/W is set, write-protected bits in various registers can be written to.
5	Adr_clr	Address clear	When Adr_clr is set, the internal RAM address counter and the Control_bit_err flag are cleared.
6	Control_bit1	Control bit for RAM test write	During RAM test mode, Control_bit1 is written into the control bit of RAM (bit 33) for RAM write transaction. The default state of this bit is cleared.
7	Control_bit_err	Control bit error flag	When Control_bit_err is set, the control bit of the RAM does not match Control_bit1 during RAM test mode. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
8	RAMTest	RAM test mode	When RAMTest and regR/W are set, RAM test mode is enabled. The default state of this bit is cleared.
9 – 16	Reserved		Reserved
17 – 19	StatSel0	Stat0 select	See Table 2–6
20	Reserved		Reserved
21 – 23	StatSel1	Stat1 select	See Table 2–6
24 – 28	XtendClk	Clock adder	Number of clocks to add to the microcontroller CS/CA clock fixed mode timing (see subsection 3.2.7.1).
29	Reserved		Reserved
30	McMode0	Mc mode	Current status of the input terminal MCMODE0. This bit is read only.
31	McMode1	Mc mode	Current status of the input terminal MCMODE1. This bit is read only.

3.2.7.1 XtendClk

XtendClk (@20h[24–28]) is valid only in pulse mode with fixed timing. The power-on default value is 1Fh. In fixed timing mode, TSB12LV31 responds to a MCS pulse with a MCA pulse after a fixed number of BCLK cycles have elapsed. This number is XtendClk + 2 (i.e., the power-on default for pulse mode with fixed timing is 33 (1Fh + 2 = 21h)). The acceptable range for MCA response is dependent on the frequency of the BCLK. If XtendClk is set at too low a value the microcontroller hangs. This requires a hardware reset to correct. The value zero is a special case. When XtendClk is set to zero then the time between MCS and MCA is at its maximum value of 34. It is recommended that XtendClk be tuned once and left unchanged.

Table 3–8. Recommended Range for XtendClk

BCLK FREQUENCY (MHz)	XtendClk	DECIMAL VALUE
12.5	06h	6
25	07h	7
33	0Ah	10
50	0Fh	15

3.2.8 Phy Access Register @24h

The Phy Access register allows access to the registers in the attached phy. The most significant 16 bits send read and write requests to the Phy registers. The least significant 16 bits are for the phy to respond to a read request sent by the TSB12LV31. The Phy Access register also allows the phy interface to send important information back to the TSB12LV31. When the phy interface sends new information to the TSB12LV31, the Phy register-information-receive (PhyRRx) interrupt is set. The Phy Acess register is at address 24h and is a read/write register.The Phy Access register has an initial value of 0000_0000h.

Table 3–9. Phy Access Register @24h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	RdPhy	Read phy register	When RdPhy is set, the TSB12LV31 sends a read register request with the address equal to phyRgAd to the phy interface. This bit is cleared when the request is sent.
1	WrPhy	Write phy register	When WrPhy is set, the TSB12LV31 sends a write register request with the address equal to phyRgAd to the phy interface. This bit is cleared when the request is sent.
2–3	Reserved		Reserved
4–7	PhyRgAd	Phy-register address	PhyRgAd is the address of the Phy register that is to be accessed.
8–15	PhyRgData	Phy-register data	PhyRgData is the data to be written to the Phy register indicated in PhyRgAd.
16–19	Reserved		Reserved
20–23	PhyRxAd	Phy-register-received address	PhyRxAd is the address of the register from which PhyRxData came. These bits can be set only when the regR/W bit has been set in the Diagnostics register @20h.
24–31	PhyRxData	Phy-register-received data	PhyRxData contains the data from the register addressed by PhyRxAd. For testing, these bits can be set only when the regR/W bit has been set in the Diagnostics register @20h.

3.2.9 ATF Status Register @30h

The ATF Status register @30h allows access to the registers that control or monitor the ATF. The ATF Status register is at address 30h. All the FIFO flag bits are read only, and the FIFO control bits are read/write. The ATF Status register has an initial value of 0000_0000h.

Table 3–10. ATF Status Register @30h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	ATF full flag	When Full is set, the FIFO is full. Writes are ignored. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
1	AlF	ATF almost-full flag	When AlF is set, the FIFO can accept one more write. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
2–3	Reserved		Reserved
4	4AV	ATF-4-available flag	When 4AV is set, the FIFO has space available for at least four quadlets. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
5–13	Reserved		Reserved
14	AlE	ATF-almost-empty flag	When AlE is set, the FIFO has only one quadlet in it. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
15	Empty	ATF-empty flag	When Empty is set, the FIFO is empty. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
16–18	Reserved		Reserved
19	Clr	ATF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–25	Reserved		Reserved
26–31	Size	ATF-size control bits	Size is equal to the ATF size number in quadlets. The power-up reset value of these bits is 000000.

3.2.10 Bus Reset Register @34h

The Bus Reset register @34h is shown in Table 3–11.

Table 3–11. Bus Reset Register @34h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	NRIDVal	Valid	When set, NRIDVal indicates that the Node ID, IRM Node ID, Node Count, and Root information is valid. This bit is read only.
1	Reserved		Reserved
2 – 7	NodeCount	Node count	NodeCount contains the number of nodes detected in the system. These bits are read only.
8	Root	Root	Root is set when the current node is the root node. This bit is read only.
9	Contender	Contender	Contender conatins the status of the CONTNDR terminal. This bit is read only.
10 – 15	IRMNodeID	IRM node identification	IRMNodeID is the isochronous resource manager node identification. These bits are read only.
16 – 25	BusNumber	Bus number	BusNumber is the 10-bit IEEE-1212 Bus Number. These bits are set to 3FFh when RbusNum is set and there is a bus reset.
26 – 31	NodeNumber	Node number	NodeNumber is the node number of the current node. These bits are automatically updated following a bus reset. These bits are read/write only when ManMode is set (see subsection 3.2.3).

3.2.11 Self-ID Check Register @38h

The Self-ID check register @38h is shown in Table 3–12.

Table 3–12. Self-ID Check Register @38h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION	
0 – 3	SIDErCode	Self-ID error code	SIDErCode contains the error code of the first Self-ID Error. The error code is as follows:	
			0000	No error
			0001	Last Self-ID received was not all child
			0010	Received phy ID in Self-ID not as expected
			0011	Quadlet not inverted (phase error)
			0100	Phy ID sequence error (two or more gaps in IDs)
			0101	Phy ID sequence error (large gap in IDs)
			0110	Phy ID error within packet
			0111	Quadlet not the invertion of the prior quadlet
			1000	Faulty quadlet received
			1001–1111	Reserved
			SIDErCode is cleared to 0000 by a bus reset or CISIDER. These bits are read only.	
4 – 14	Reserved		Reserved	
15	ClSIDEr	Clear error	When ClSIDEris set, SIDErCode is cleared.	
16 – 31	Reserved		Reserved	

3.2.12 GRF Status Register @3Ch

The GRF Status register @3Ch allows access to the registers that control or monitor the GRF. The register is at address 3Ch. All the FIFO flag bits are read only, and the FIFO control bits are read/write. The GRF register has an initial value of 0000_0000h. The GRF Status register is shown in Table 3–13.

Table 3–13. GRF Status Register @3Ch

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	GRF full flag	When Full is set, the FIFO is full. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
1	AlF	GRF-almost-full flag	When AlF is set, the FIFO can accept only one more write. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
2–3	Reserved		Reserved
4	4AV	ATF-4-available flag	When 4AV is set, the FIFO has space available for at least four quadlets. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
5–11	Reserved		Reserved
12	4Th	GRF four there	When 4Th is set, the FIFO has at least four quadlets in it. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
13	Reserved		Reserved
14	AlE	GRF-almost-empty flag	When AlE is set, the FIFO has one quadlet in it. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
15	Empty	GRF-empty flag	When Empty is set, the FIFO is empty and reads are ignored. For testing, this bit can be set only when the regR/W bit has been set in the Diagnostics register @20h.
16	Cd	GRF control bit	Cd is the control bit for the GRF. When Cd is set, the first quadlet of a packet is being read from the GRF_Data address. This bit is read only.
17–18	Reserved		Reserved
19	Clr	GRF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–25	Reserved		Reserved
26–31	Size	GRF-size control bits	Size is equal to the GRF size in quadlets. The power-up reset value is 32h (the maximum GRF size).

3.2.13 FIFO State Register @50h

The FIFO State register @50h is shown in Table 3–14.

Table 3–14. FIFO State Register @50h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0 – 17	Reserved		Reserved
18 – 23	ATF Remain	ATF Remaining	ATF Remain indicates the amount of quadlets remaining in the ATF. These bits are read only.
24 – 25	Reserved		Reserved
26 – 31	GRF Remain	GRF Remaining	GRF Remain indicates the number of quadlets remaining in the GRF. These bits are read only.

3.2.14 Isochronous Control Register @54h

The Isochronous Control register @54h is shown in Table 3–15.

Table 3–15. Isochronous Control Register @54h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
00 – 21	Quadperblock	Quadlet per block	Quadperblock indicates the number of quadlets per block.
22 – 31	Quadperpkt	Quadlet per packet	Quadperpkt indicates the number of quadlets per packet.

3.2.15 Isochronous Mode Register @58h

The Isochronous Mode register @58h is shown in Table 3–16.

Table 3–16. Isochronous Mode Register @58h

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION	
0	isodmen	Isochronous start enable	When isodmen is set, the device is ready to begin isochronous transmit (reset to 0).	
1 – 2	isomode	Isochronous mode	The isomode bits determine whether the isochronous operational mode is in a transmit or receive state. The code is:	
			00	Transmit isochronous data from the port to serial bus This is the default value of isomode (reset to 00)†.
			01	Receive isochronous data from the serial bus to the port
			10–11	Reserved
03 – 31	Reserved		Reserved	

† Isochronous data can be received into the GRF regardless of the isomode setting. Isochronous data into the GRF is controlled by IRPxEn bits in the Control register (see CRF @08h, Table 3–6, and Table 3–7).

3.2.16 Isochronous Header Register @5Ch

The Isochronous Header register @5Ch is shown in Table 3–17.

Table 3–17. Isochronous Mode Register @5Ch

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0 – 15	Packet Data Length	Packet data length	Packet Data Length indicates the number of bytes in the current packet.
16 – 17	TAG	Tag field	TAG conatins the TAG field for the isochronous packet.
18 – 23	Channel number	Channel number	Channel number contains the channel number with which the current data is associated.
24 – 25	Reserved		Reserved
26 – 27	Speed	Speed	Speed contains the speed at which to send the current packet. The default value is 00.
28 – 31	SyncBitEn	Synchronous enable	For isochronous transmit, when SyncBitEn is set, the corresponding synchronous bit is set in the isochronous header synchonous field for the first packet of data (see the ISRxSYEn field in Table 3–6). The default value is 0000.

4 FIFO Access

4.1 FIFO Access

Access to all the FIFOs is fundamentally the same, only the addresses to where the write is made changes. Figure 4–1 shows the FIFO-address access map and illustrates how and where the FIFOs are accessed.

	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
80h	ATF_First
84h	ATF_Continue
88h	Reserved
8Ch	ATF_Continue & Update
90h	Reserved
94h	Reserved
98h	Reserved
9Ch	Reserved
A0h	Reserved
A4h	Reserved
A8h	Reserved
ACh	Reserved
B0h	Reserved
B4h	Reserved
B8h	Reserved
BCh	Reserved
C0h	GRF Data
C4h	Reserved
C8h	Reserved
CCh	Reserved

Figure 4–1. TSB12LV31 Controller-FIFO-Access Address Map

4.1.1 ATF Access

Access to the ATF is as follows:

1. Write to ATF location 80h: the data is not confirmed for transmission (first quadlet of the packet).
2. Write to ATF location 84h: the data is not confirmed for transmission (second n–1 quadlets of the packet).
3. Write to ATF location 8Ch: the data is confirmed for transmission (second n quadlets of the packet).

   If the first quadlet of a packet is not written to the ATF_First, the transmitter enters a state denoted by an ATStuck interrupt. An underflow of the ATF also causes an ATStuck interrupt. When this state is entered, no asynchronous packets can be sent until the ATF is cleared by way of the CLR ATF control bit. Isochronous packets can be sent while in this state.

ATF access example:

The first quadlet of n quadlets is written to ATF location 80h. Quadlets (2 to n-1) are written to ATF location 84h. The last quadlet (nth) is written to ATF location 8Ch. If the ATFEmpty bit is set, it is cleared and the TSB12LV31 requests the phy layer to arbitrate for the bus. To ensure that an ATF underflow condition does not occur, loading of the ATF in this manner is suggested.

4.1.2 General-Receive-FIFO (GRF)

Access to the GRF is done with a read from the GRF, which requires a read from address C0h.

5 TSB12LV31 Data Formats

The data formats for transmission and reception of data are shown in the following sections. The transmit format describes the expected organization of data presented to the TSB12LV31 at the host-bus interface. The receive formats describe the data format that the TSB12LV31 presents to the host-bus interface.

5.1 Asynchronous Transmit (Host Bus to TSB12LV31)

Asynchronous transmit refers to the use of the asynchronous-transmit FIFO (ATF) interface. The general-receive FIFO (GRF) is shared by asynchronous data and isochronous data. There are two basic formats for data to be transmitted and received. The first is for quadlet packets, and the second is for block packets. For transmits, the FIFO address indicates the beginning, middle, and end of a packet. For receives, the data length, which is found in the header of the packet, determines the number of bytes in a block packet.

5.1.1 Quadlet Transmit

The quadlet-transmit format is shown in Figure 5–1 and is described in Table 5–1. The first quadlet contains packet control information. The second and third quadlets contain the 64-bit, quadlet-aligned address. The fourth quadlet is data used only for write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

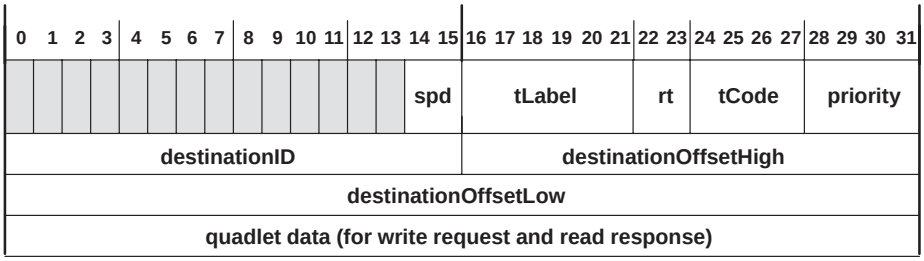


Figure 5–1. Quadlet-Transmit Format

Table 5–1. Quadlet-Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	The spd field indicates the speed at which the current packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is: 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6–10 of IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of the current packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4).
quadlet data	For write requests and read responses, the quadlet data field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.

5.1.2 Block Transmit

The block-transmit format is shown in Figure 5–2 and is described in Table 5–2. The first quadlet contains packet-control information. The second and third quadlets contain the 64-bit address. The first 16 bits of the fourth quadlet contains the dataLength field. This is the number of bytes of data in the packet. The remaining 16 bits represent the extended_tCode field (see Table 6–11 of the IEEE-1394 standard for more information on extended_tCodes). The block data, if any, follows the extended_tCode.

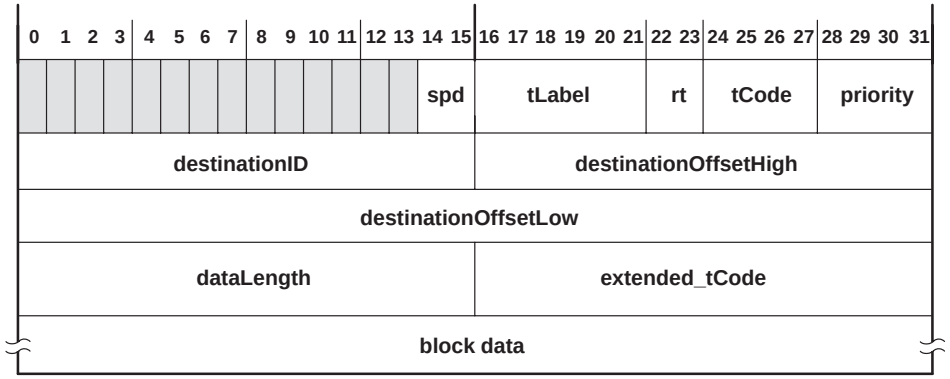


Figure 5–2. Block-Transmit Format

Table 5–2. Block-Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	The spd field indicates the speed at which the current packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for the current packet (see Table 6–10 of IEEE-1394 standard).
priority	The priority level for the current packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4). The upper 4 bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	The dataLength filed contains the number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in the current packet (see Table 6–11 of the IEEE-1394 standard).
block data	The block data field contains the data to be sent. If dataLength is 0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in byte 0 of the first quadlet.

5.1.3 Quadlet Receive

The quadlet-receive format is shown in Figure 5–3 and is described in Table 5–3. The first 16 bits of the first quadlet contain the destination node and bus ID, and the remaining 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source, and the remaining 16 bits of the second and third quadlets contain the 48-bit, quadlet-aligned destination offset address. The fourth quadlet contains data that is used by write requests and read responses. For read requests and write responses, the quadlet data field is omitted. The last quadlet contains packet-reception status that is added by the TSB12LV31.

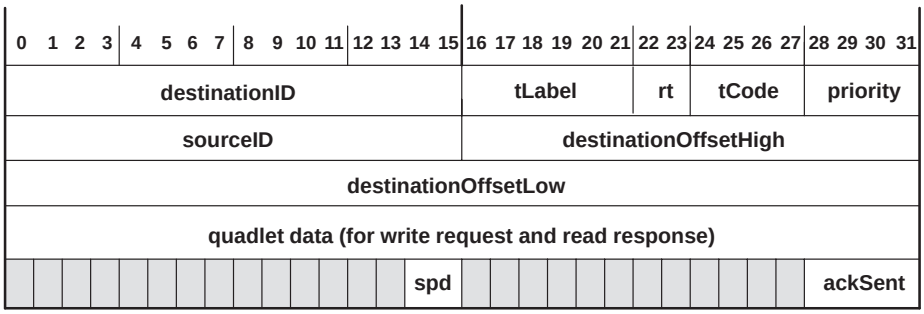


Figure 5–3. Quadlet-Receive Format

Table 5–3. Quadlet-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	The destinationID field contains the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6–10 of the IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
sourceID	The sourceID field contains the node ID of the sender of the current packet.
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). (The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets, and the remaining bits are reserved.)
quadlet data	For write requests and read responses, the quadlet data field holds the transferred data. For write responses and read requests, this field is not present.
spd	The spd field indicates the speed at which the current packet was sent. 00 = 100 Mbits/s, 01 = 200 Mbits/s, 10 = 400 Mbits/s, and 11 is undefined for this implementation.
ackSent	The ackSent field holds the acknowledge sent by the receiver for the current packet (see Table 6–13 in the draft standard).

5.1.4 Block Receive

The block-receive format is shown in Figure 5–4 and is described in Table 5–4. The first 16 bits of the first quadlet contain the node and bus ID of the destination node, and the last 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source node, and the last 16 bits of the second quadlet and all of the third quadlet contain the 48-bit, quadlet-aligned destination offset address. All remaining quadlets, except for the last one, contain data that is used only for write requests and read responses. For block read requests and block write responses, the data field is omitted. The last quadlet contains packet-reception status.

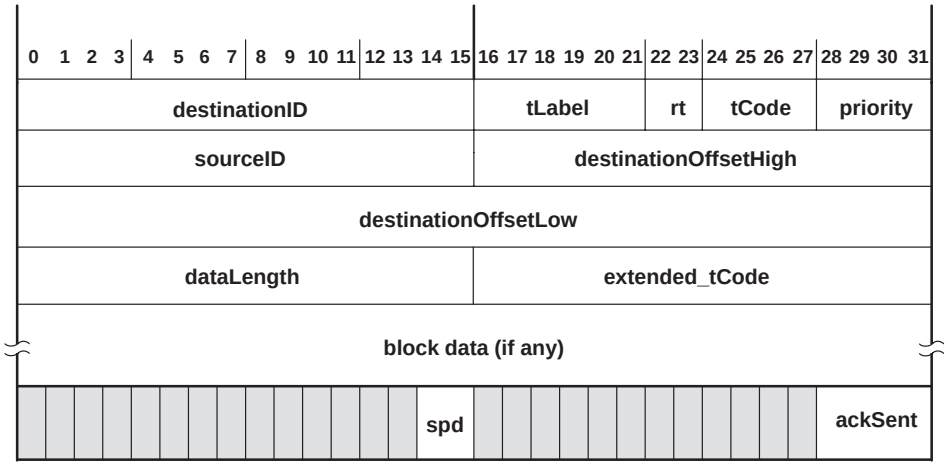


Figure 5–4. Block-Receive Format

Table 5–4. Block-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field contains the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6–10 of the IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
sourceID	The sourceID field contains the node ID of the sender of the current packet.
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). The upper 4 bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	For write request, read responses, and locks, the dataLength field indicates the number of bytes being transferred. For read requests, the dataLength field indicates the number of bytes of data to be read. A write-response packet does not use this field. Note that the number of bytes does not include the head, only the bytes of block data.
extended_tCode	The extended_tCode field contains the block extended_tCode to be performed on the data in the current packet (see Table 6–11 of the IEEE-1394 standard).
block data	The block data field contains any data being transferred for the current packet. Regardless of the destination address or memory alignment, the first byte of the data appears in byte 0 of the first quadlet of this field. The last quadlet of the field is padded with zeros out to four bytes, if necessary.
spd	The spd field indicates the speed at which the current packet was sent. 00 = 100 Mb/s, 01 = 200 Mb/s, 10 = 400 Mb/s, and 11 is undefined for this implementation.
ackSent	The ackSent field holds the acknowledge sent by the receiver for the current packet.

5.2 Isochronous Transmit (Host Bus to TSB12LV31)

The format of the isochronous-transmit packet is shown in Figure 5–5 and is described in Table 5–5. The data for each channel must be presented to the isochronous-transmit FIFO interface in this format in the order that packets are to be sent. The transmitter sends any packets available at the isochronous-transmit interface immediately following reception or transmission of the cycle-start message.

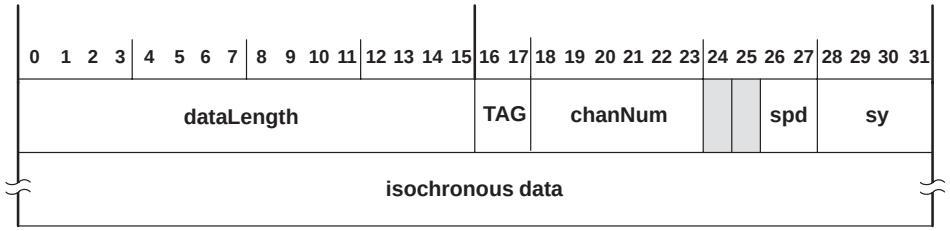


Figure 5–5. Isochronous-Transmit Format

Table 5–5. Isochronous-Transmit Functions

FIELD NAME	DESCRIPTION
dataLength	The dataLength field indicates the number of bytes in the current packet
TAG	The TAG field indicates the format of data carried by the isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	The chanNum field carries the channel number with which the current data is associated.
spd	The spd field contains the speed at which to send the current packet.
sy	The sy field carries the transaction layer-specific synchronization bits.
isochronous data	The isochronous data field contains the data to be sent with the current packet. The first byte of data must appear in byte 0 of the first quadlet of this field. If the last quadlet does not contain four bytes of data, the unused bytes should be padded with zeros.

5.3 Isochronous Receive (TSB12LV31 to Host Bus)

The format of the iscohronous-receive data is shown in Figure 5–6 and is described in Table 5–6. The data length, which is found in the header of the packet, determines the number of bytes in an isochronous packet.

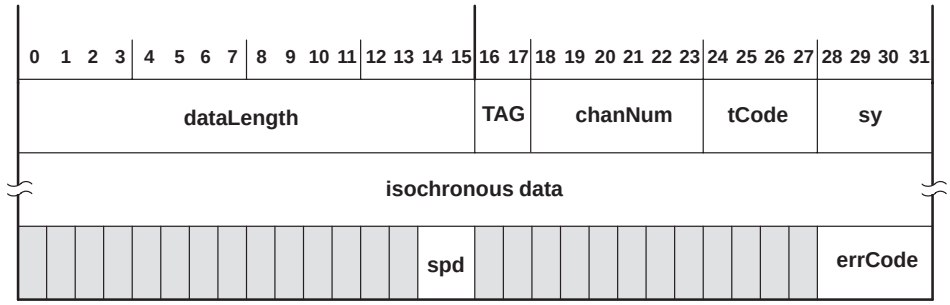


Figure 5–6. Isochronous-Receive Format

Table 5–6. Isochronous-Receive Functions

FIELD NAME	DESCRIPTION
dataLength	The dataLength field indicates the number of bytes in the current packet.
TAG	The TAG field indicates the format of data carried by isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	The chanNum field contains the channel number with which this data is associated.
tCode	The tCode field carries the transaction code for the current packet (tCode = Ah).
sy	The sy field carries the transaction layer-specific synchronization bits.
isochronous data	The isochronous data field has the data to be sent with the current packet. The first byte of data must appear in byte 0 of the first quadlet of this field. The last quadlet should be padded with zeros.
spd	The spd field indicates the speed at which the current packet was sent.
errCode	The errCode field indicates whether the current packet has been received correctly. The possibilities are Complete, DataErr, or CRCErr, and have the same encoding as the corresponding acknowledge codes.

5.4 Snoop

The format of the snoop data is shown in Figure 5–7 and is described in Table 5–7. The receiver module can be directed to receive any and all packets that pass by on the serial bus. In this mode, the receiver presents the data received to the receive-FIFO interface.

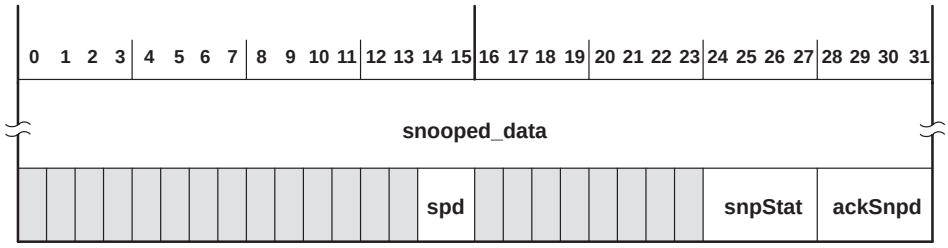


Figure 5–7. Snoop Format

Table 5–7. Snoop Functions

FIELD NAME	DESCRIPTION
snooped_data	The snooped_data field contains the entire packet received or as much as could be received.
spd	The spd field carries the speed at which the current packet was sent.
snpStat	The snpStat field indicates whether the entire packet snooped was received correctly. A value equal to the complete acknowledge code indicates complete reception. A busyA or busyB acknowledge code indicates incomplete reception.
ackSnpd	The ackSnpd field indicates the acknowledge seen on the bus after the packet is received.

5.5 CycleMark

The format of the CycleMark data is shown in Figure 5–8 and is described in Table 5–8. The receiver module inserts a single quadlet to mark the end of an isochronous cycle. The quadlet is inserted into the receive-FIFO.

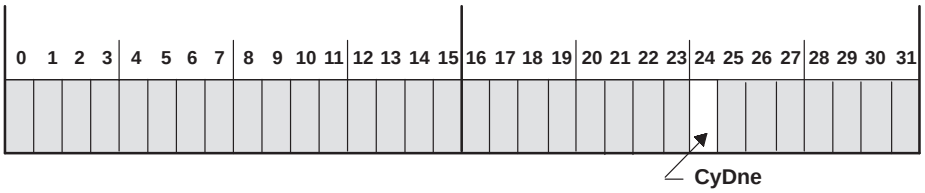


Figure 5–8. CycleMark Format

Table 5–8. CycleMark Function

FIELD NAME	DESCRIPTION
CyDne	Th CyDne field indicates the end of an isochronous cycle.

5.6 Phy Configuration

The format of the phy configuration packet is shown in Figure 5–9 and is described in Table 5–9. The phy configuration packet transmit contains two quadlets, which are loaded into the ATF. The first quadlet is written to address 80h. The second quadlet is written to address 8Ch. The 00E0h in the first quadlet tells the TSB12LV31 that this quadlet is the phy configuration packet. The Eh is then replaced with 0h before the packet is transmitted to the phy interface.

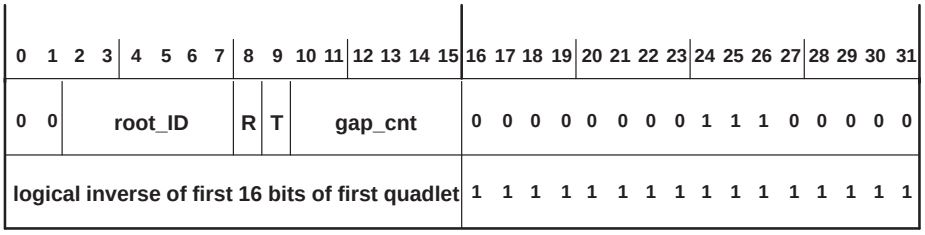


Figure 5–9. Phy Configuration Format

Table 5–9. Phy Configuration Functions

FIELD NAME	DESCRIPTION
00	The 00 field is the phy configuration packet identifier.
root_ID	The root_ID field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R†	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T†	When T is set, the PHY_CONFIGURATION.gap_count field of all the nodes is set to the value in the gap_cnt field.
gap_cnt	The gap_cnt field contains the new value for PHY_CONFIGURATION.gap_count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, gap_cnt is set to 63h unless a new phy configuration packet is received.

† A phy configuration packet with R = 0 and T = 0 is reserved and is ignored when received.

5.7 Receive Self-ID Packet

The format of the receive Self-ID packet is shown in Figure 5–10 and is described in Table 5–10. When RxSId (bit 1 of the control register) is set, the receive Self-ID packet is stored in GRF.

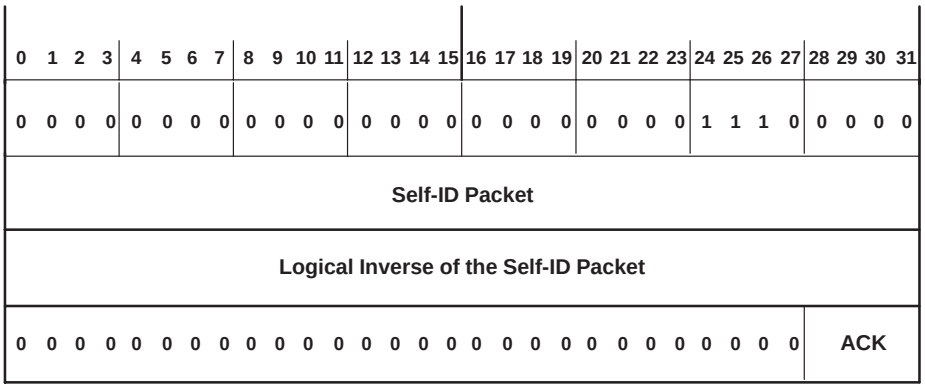


Figure 5–10. Receive Self-ID Format

Table 5–10. Receive Self-ID Function

FIELD NAME	DESCRIPTION
ACK	When the ACK field is set (0001b), the data in the Self-ID packet is correct. When ACK is ≠ 0001b, the data in the Self-ID packet is incorrect.

When there is only one node (i.e., one phy/LLC pair) on the bus, following a bus reset, the GRF contains 000_00E0h and the acknowledge quadlet only.

When there are three nodes on the bus, each with a phy having three or less ports, following a bus reset, the GRF of any one of the LLCs is shown in Table 5–11.

Table 5–11. GRF Contents With Three Nodes on a Bus

GRF CONTENTS	DESCRIPTION
0000_00E0h	Header for Self-ID
self–ID1	Self_ID for phy #1
self–ID1 inverse	Self_ID for phy #1 inverted
self–ID2	Self_ID for phy #2
self–ID2 inverse	Self_ID for phy #2 inverted
0000_000_ACK	Trailing acknowledgement

The first quadlet in a Self-ID packet is 0000_00E0h. The second quadlet in the Self-ID packet is described in Figure 5–11, Figure 5–12, and Table 5–12. The third quadlet is the inverse of the Self-ID quadlet. The fourth and final Self-ID quadlet in the packet is the acknowledgement.

The cable phy sends one to four Self-ID packets at the base rate (100 Mbits/s) during the Self-ID phase of arbitration. The number of Self-ID packets sent depends on the number of ports. Figure 5–11 and Figure 5–12 show the formats of the cable phy Self-ID packets.

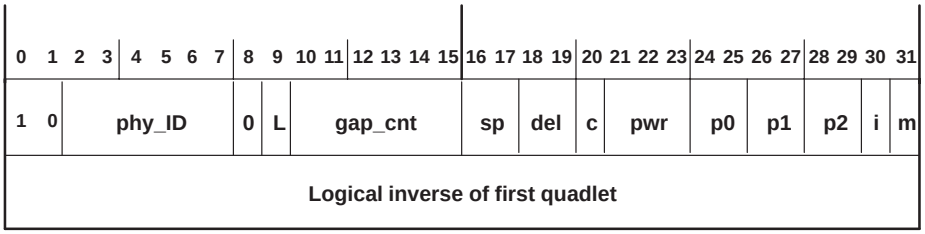
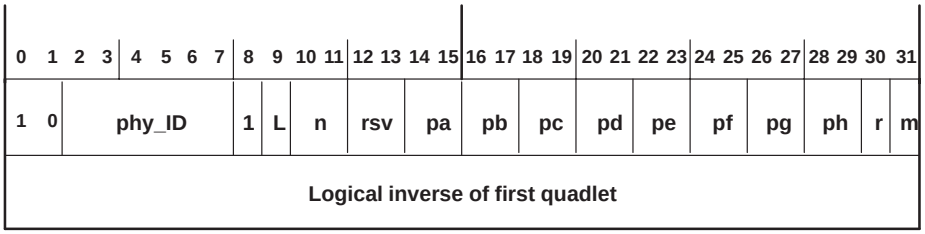


Figure 5–11. Phy Self-ID Packet #0 Format



PACKET #	n†	pa	pb	pc	pd	pe	pf	pg	ph
1	0	p3	p4	p5	p6	p7	p8	p9	p10
2	1	p11	p12	p13	p14	p15	p16	p17	p18
3	2	p19	p20	p21	p22	p23	p24	p25	p26

† For n = 3 – 7, fields pa through ph are reserved.

Figure 5–12. Phy Self-ID Packet #1, Packet #2, and Packet #3 Format

Table 5–12. Phy Self-ID Functions

FIELD NAME	DESCRIPTION	
10	The 10 field is the Self-ID packet identifier.	
c	When c is set and the link-active flag is set, this field indicates that the current node is a contender for the bus or isochronous resource manager.	
del	The del field contains the worst-case repeater-data delay time. The code is:	
	00	≤ 144 ns ≈ (14 / Base_Rate)
	01 – 11	Reserved
gap_cnt	The gap_cnt field contains the current value for the current node PHY_CONFIGURATION.gap_count field.	
i	When set, the i field indicates that the current node initiated the current bus reset (i.e., it started sending a bus reset signal before it received one†).If this function is not implemented, i is returned as 0.	
L	When L is set, the current node has an active LLC and transaction layer.	
m	When set, the m field indicates that another Self-ID packet for the current node immediately follows (i.e. when m is set and the next Self-ID packet received has a different phy_ID, then a Self-ID packet was lost).	

† There is no way to ensure that exactly one node has this bit set. More than one node can be requesting a bus reset at the same time.

Table 5–12. Phy Self-ID Functions (Continued)

FIELD NAME	DESCRIPTION	
n	The n field is the extended Self-ID packet sequence number. The code is:	
	0	Self-ID packet 1
	1	Self-ID packet 2
	2	Self-ID packet 3
phy_ID	The phy_ID field is the physical node identifier of the sender of the current packet.	
p0 – p26	The p0 – P26 field indicates the port status. The code is:	
	00	Not present on the current phy
	01	Not connected to any other phy
	10	Connected to the parent node
	11	Connected to the child node
pwr	The pwr field contains the bits that indicate the power consumption and source characteristics. The code is:	
	000	The node does not need power and does not repeat power.
	001	The node is self powered and provides a minimum of 15 W to the bus.
	010	The node is self powered and provides a minimum of 30 W to the bus.
	011	The node is self powered and provides a minimum of 45 W to the bus.
	100	The node can be powered from the bus and is using up to 1 W.
	101	The node is powered from the bus and is using up to 1 W. An additional 2 W is needed to enable the LLC and higher layers.‡
	110	The node is powered from the bus and is using up to 1 W. An additional 5 W is needed to enable the LLC and higher layers.‡
	111	The node is powered from the bus and is using up to 1 W. An additional 9 W is needed to enable the LLC and higher layers.‡
r	Reserved and set to all zeros.	
rsv	Reserved and set to all zeros.	
sp	The sp field contains the phy speed capability. The code is:	
	00	98.304 Mbits/s
	01	98.304 Mbits/s and 196.608 Mbits/s
	10	98.304 Mbits/s 196.608 Mbits/s, and 393.216 Mbits/s
	11	Reserved

† There is no way to ensure that exactly one node has this bit set. More than one node can be requesting a bus reset at the same time.

‡ The LLC and higher layers are enabled by the Link-On Phy packet.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings Over Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC} (5-V tolerant TTL terminals) . . . . . −0.5 V to 5.5 V
Input voltage range, V_I (5-V tolerant TTL terminals) . . . . . −0.5 V to 5V V_{CC} + 0.5 V
Output voltage range, V_O (TTL terminals) . . . . −0.5 V to V_{CC} + 0.5 V (4.6 V maximum)
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2) . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This parameter applies to external input and bidirectional buffers without hysteresis. V_I > V_{CC} does not apply to fail-safe terminals. For 5-V tolerant and universal PCI use V_O > V_{CC} 5 V.
2. This parameter applies to external input and bidirectional buffers without hysteresis. V_O > V_{CC} does not apply to fail-safe terminals. For 5-V tolerant and universal PCI use V_O > V_{CC} 5 V.

6.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Supply voltage, V_{CC} (5 V)		4.5	5	5.5	V
Output voltage, V_O	TTL and LVCMOS terminals	0		V_{CC}	V
High-level input voltage, V_{IH}	TTL and LVCMOS terminals	2		V_{CC}	V
Low-level input voltage, V_{IL}	TTL and LVCMOS terminals	0		0.8	V
Clock frequency	BCLK			50	MHz
	SCLK			50	
Operating free-air temperature, T_A		0		70	°C
Virtual junction temperature range, T_J		0		115	°C

6.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –12 mA‡	V_{CC} – 0.6			V
			I_{OH} = –8 mA§	V_{CC} – 0.6			
V_{OL}	Low-level output voltage		I_{OL} = 12 mA‡			0.4	V
			I_{OL} = 8 mA§			0.4	
I_{IL}	Low-level input current		V_I = GND			–1	µA
I_{IH}	High-level input current		V_I = V_{CC}			1	µA
I_{OZ}	High-impedance-state output current		V_I = V_{CC} or GND		±20		µA
I_{CC}	Supply current		No load on outputs, SCLK = 49.152 MHz, BCLK = 25 MHz		37		mA
C_i	Input capacitance	Input terminals	V_{CC} = 3.3 V, T_A = 25°C		5		pF
		Bidirectional terminals			13		
C_o	Output capacitance				8		pF

† All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
‡ Terminals: 27–30, 32, 33, 35, 57–60, 63–65, 67–70, 72–74, 77, 78, and 84
§ Terminals: All other outputs

6.4 Microcontroller Write Switching Characteristics Over Operating Free-Air Temperature Range

Table 6–1. Microcontroller Write Timing

PARAMETER		MIN	MAX	UNIT
t_{su1}	Setup time, MD0 – MD31, MA0 – MA7, $\overline{MWR}$, and $\overline{MCS}$ valid before BCLK↑ (see Figure 6–1 and Figure 6–2)	9.6		ns
t_{h1}	Hold time, BCLK↑ before MD0 – MD31, MA0 – MA7, $\overline{MWR}$, and $\overline{MCS}$ invalid (see Figure 6–1 and Figure 6–2)	1.2		ns
t_{d1}	Delay time, BCLK↑ to $\overline{MCA}$ ↓↑ (see Figure 6–1 and Figure 6–2)	3.6	11.4	ns

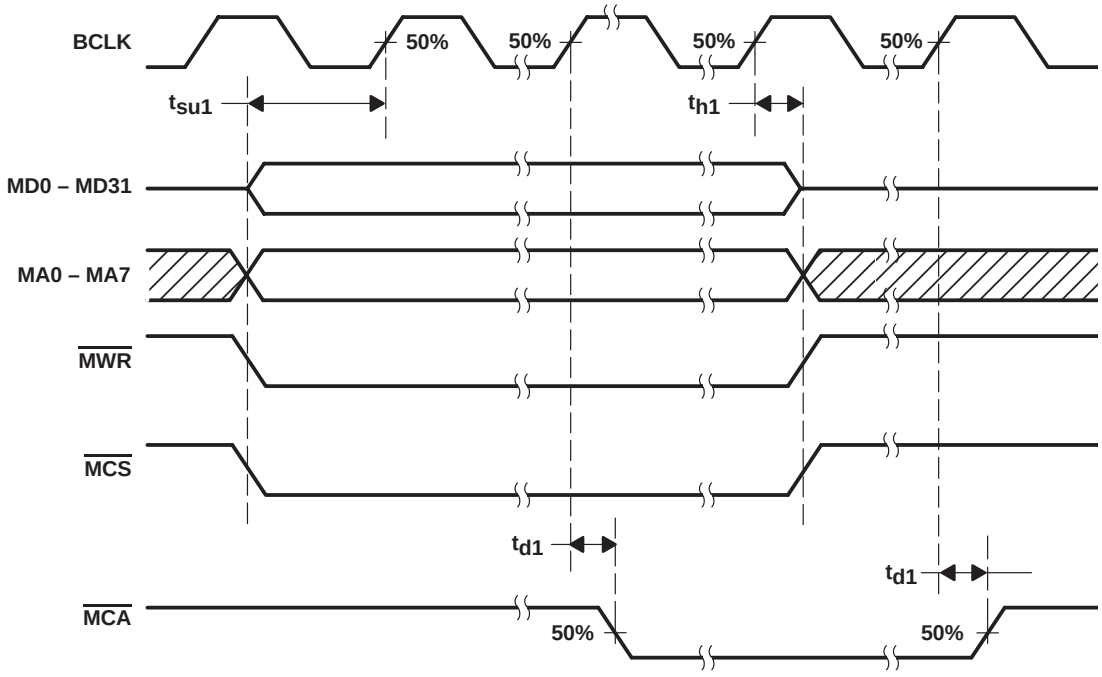


Figure 6–1. Microcontroller Write-Operation Timing Waveforms

6.5 Microcontroller Read Switching Characteristics Over Operating Free-Air Temperature Range

Table 6–2. Microcontroller Read Timing

PARAMETER		MIN	MAX	UNIT
t_{d2}	Delay time, BCLK↑ to MD0 – MD15 ↑↓ (see Figure 6–2)	3.7	13.6	ns

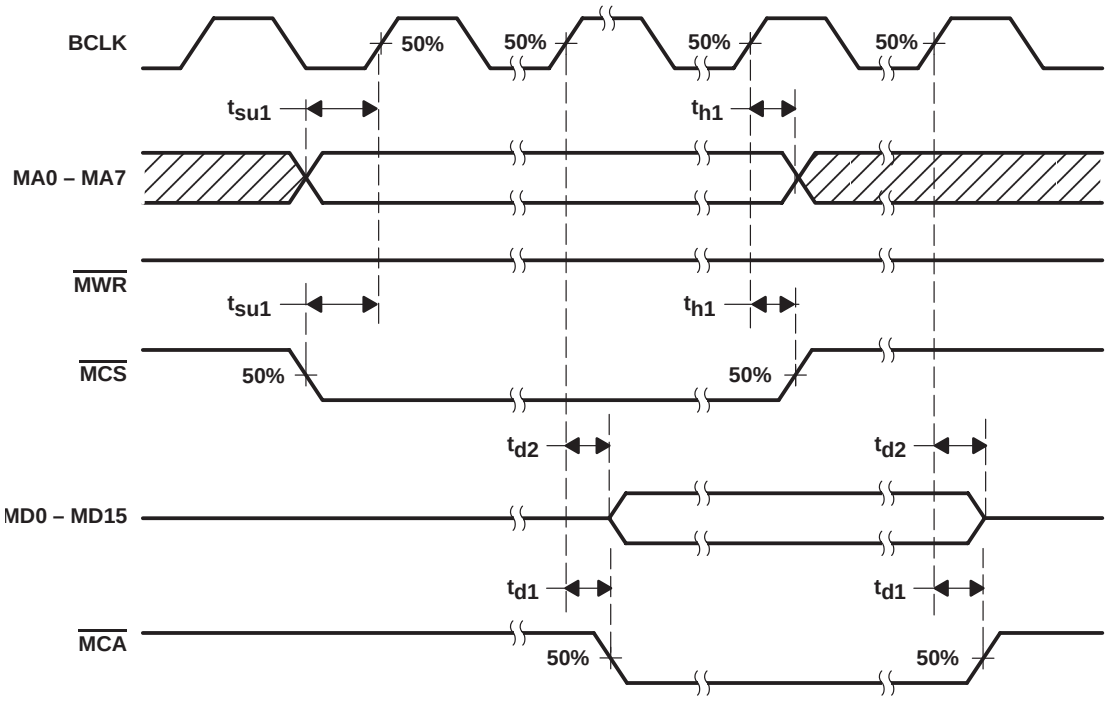
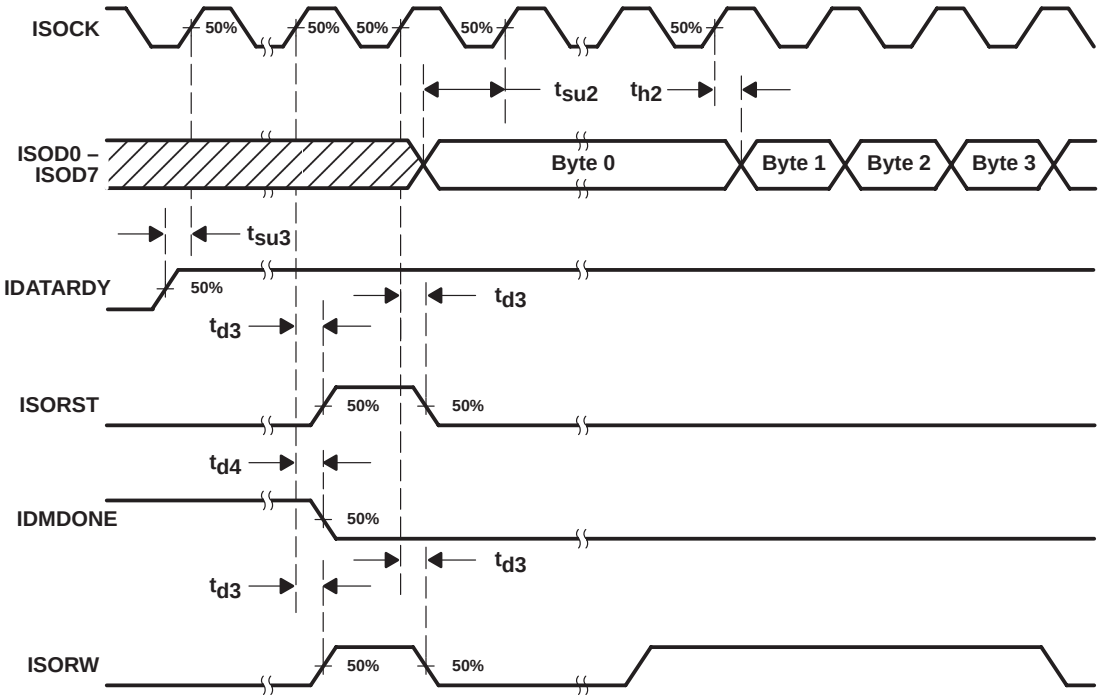


Figure 6–2. Microcontroller Read Operation Timing Waveforms

6.6 IsoPort Phase 1, 2, and 3 Switching Characteristics Over Operating Free-Air Temperature Range

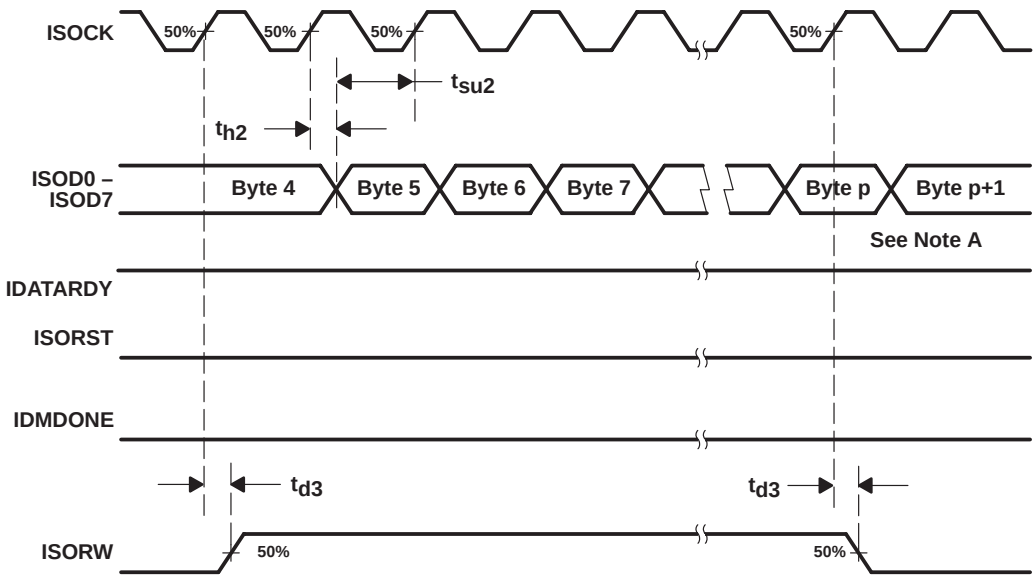
Table 6–3. IsoPort Timing Phases 1, 2, and 3

PARAMETER		MIN	MAX	UNIT
t_{su2}	Setup time, ISDO0 – ISDO7 valid before ISOCK↑ (see Figure 6–3, Figure 6–4, and Figure 6–5)	14		ns
t_{su3}	Setup time, IDATARDY↑ before ISOCK↑ (see Figure 6–3)	14		ns
t_{h2}	Hold time, ISOCK↑ before ISOD0 – ISOD7↑↓ (see Figure 6–3, Figure 6–4, and Figure 6–5)	0		ns
t_{d3}	Delay time, ISOCK↑ to ISORST↑↓, ISORW↑↓ (see Figure 6–3, Figure 6–4, and Figure 6–5)	2.8	14.1	ns
t_{d4}	Delay time, ISOCK↑ to IDMDONE↓ (see Figure 6–3)	2.2	6.5	ns



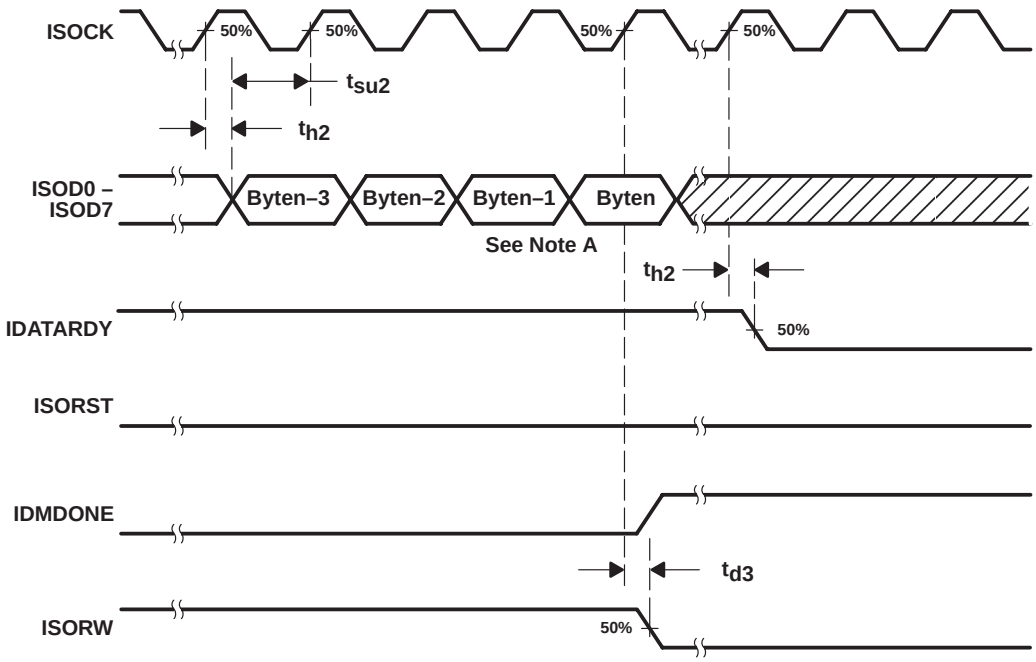
NOTE A: Transmit speed = 100/200 Mbits/s

Figure 6–3. IsoPort Phase 1 (Four-Byte Preread) Timing Waveforms



NOTES: A: Byte p is the last byte of the packet. Byte p+1 is the first byte of the next packet.
B. Transmit speed = 200 Mbits/s

Figure 6–4. IsoPort Phase 2 (Data Transmit to End of Packet) Timing Waveforms



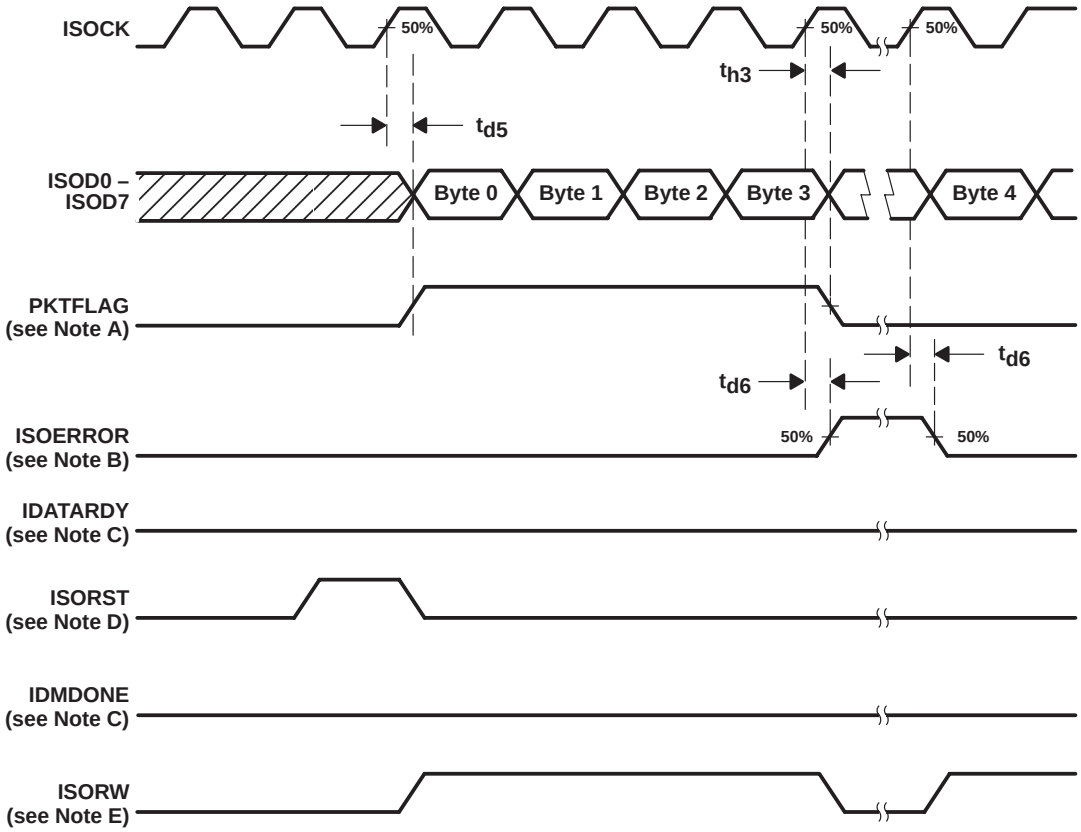
NOTES: A: Byte n is the last byte of the block.
B: Transmit speed = 200 Mbits/s

Figure 6–5. IsoPort Phase 3 (End of Block) Timing Waveforms

6.7 IsoPort Receive Switching Characteristics Over Operating Free-Air Temperature Range

Table 6–4. IsoPort Receive Timing

PARAMETER		MIN	MAX	UNIT
t_{h3}	Hold time, ISOCK↑ to ISODn↓↑, PKTFLAG↓	2.4		ns
t_{d5}	Delay time, ISOCK↑ to ISODn ↓↑, PKTFLAG↑		14	ns
t_{d6}	Delay time, ISOCK↑ to ISOERROR↓↑	2.3	6.8	ns



NOTES: A. PKTFLAG is high during isochronous header and trailer.
B. ISOERROR pulses for one clock to indicate an error in the received packet.
C. For isochronous receive, IDATARDY and IDMDONE are not used.
D. ISORST pulses for one clock when address 18h of CFR[24:27] are set and the isochronous header received with corresponding synchronous bits set high.
E. ISORW asserted high signals that the data is valid.

Figure 6–6. IsoPort Receive Timing Waveforms

Figure 6–7 shows a one-quadlet receive operation preceded by an isochronous reset. Notice the header quadlet under ISORW and PKTFLAG. The header 000401A8h indicates a data payload = 4 bytes, TAG field = 0, channel number = 01, tCode = A, and sy field = 8. MIRXD is pulsed for one clock cycle indicating an isochronous receive interrupt. The header is followed by the data 11111111h. Finally the trailer is inserted at the end of the packet. The trailer value, 00010001h, indicates a speed of 200 Mbits/s. The completion code, 01h, indicates a satisfactory completion.

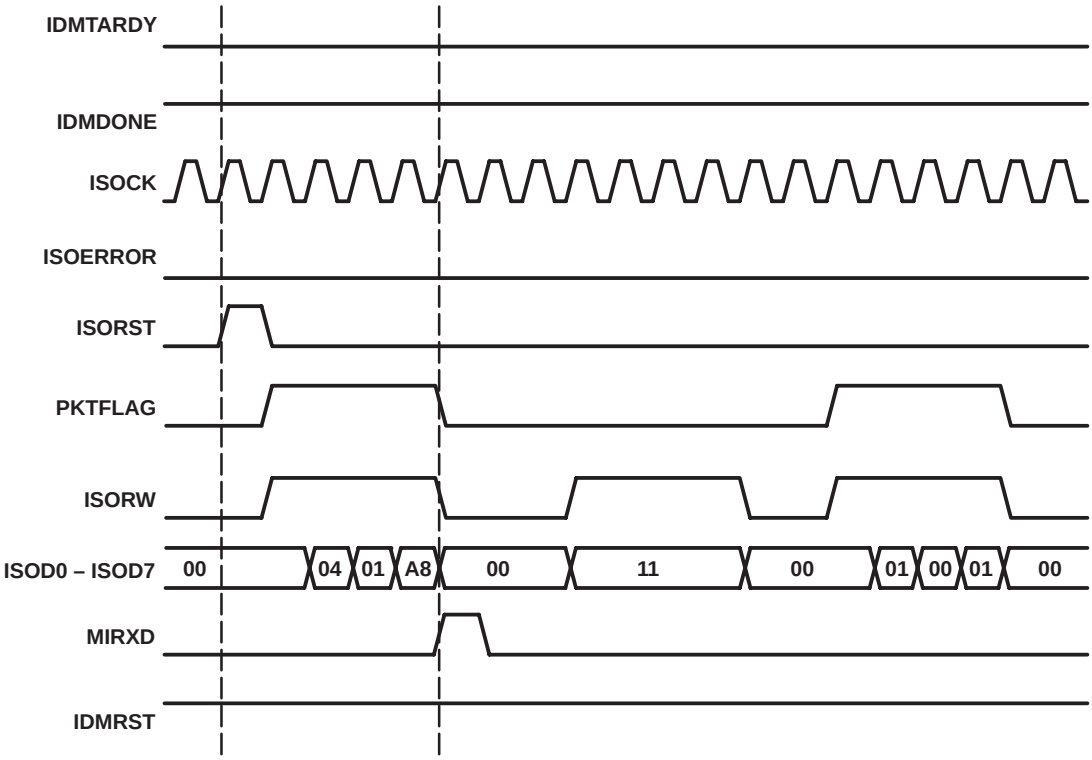


Figure 6–7. Isochronous Receive of One Quadlet at 200 Mbits/s

Figure 6–8 shows a four-quadlet receive operation with a data error. The header value, 001001A0h, indicates the data payload = 16 bytes, the TAG field = 0, the channel number = 01h, the tCode = Ah, and the sy field = 0h. MIRXD is pulsed for one clock cycle indicating an isochronous receive interrupt. The header is followed by the data, and finally the trailer is inserted at the end of the packet. Notice that the ISOERROR signal pulses for one cycle indicating a data error. The trailer value, 0001000Dh, indicates a speed of 200 Mbits/s and a completion code of 0Dh, which is a data error.

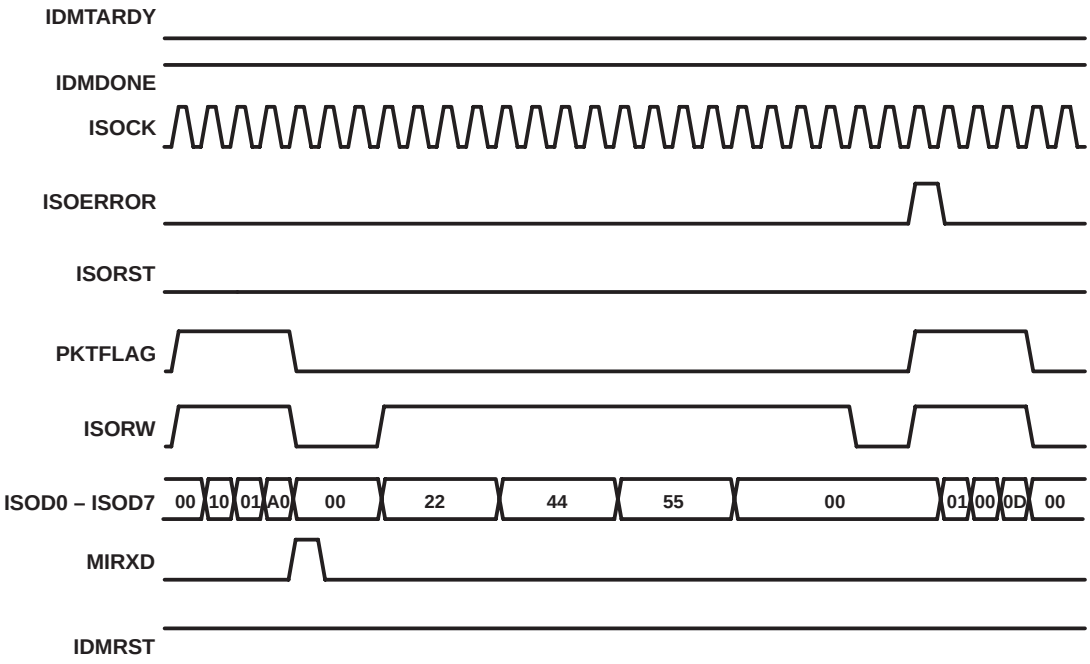


Figure 6–8. Isochronous-Receive Four Quadlets with Data Error at 200 Mbits/s

6.8 Link Read/Write Switching Characteristics Over Operating Free-Air Temperature Range

Table 6–5. Link Read/Write Timing

PARAMETER		MIN	MAX	UNIT
t_{su4}	Setup time, CTLn, D0 – D3↑ before SCLK↑ (see Figure 6–9)	6		ns
t_{h4}	Hold time, SCLK↑ to CTLn, D0 – D3↓ (see Figure 6–9)	1		ns
t_{d7}	Delay time, SCLK↑ to CTLn, D0 – D3, LREQ↑↓ (see Figure 6–10)	3.8	15.16	ns

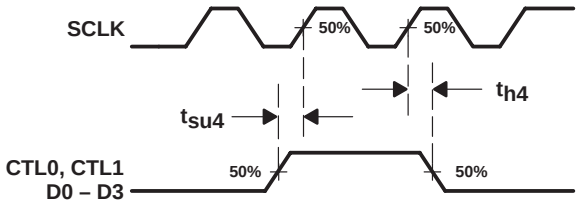


Figure 6–9. Link Read Waveforms

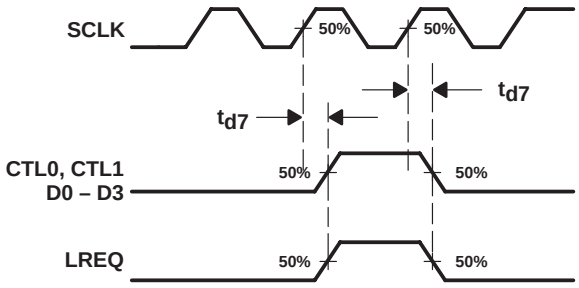


Figure 6–10. Link Write Waveforms

6.9 Output Signals Synchronous with ISOCK Switching Characteristics Over Operating Free-Air Temperature Range

Table 6–6. Synchronous ISOCK Output Timing

PARAMETER		MIN	MAX	UNIT
t_{d8}	Delay time, ISOCK↑ to STAT0, STAT1↑↓	2.8	19.5	ns
t_{d9}	Delay time, ISOCK↑ to MARxD, MIRxD↑↓	2.9	19.1	ns
t_{d10}	Delay time, ISOCK↑ to CYSTART, CYDONE↑↓	3	12.9	ns
t_{d11}	Delay time, ISOCK↑ to $\overline{INT}$↑↓	1.4	3.8	ns

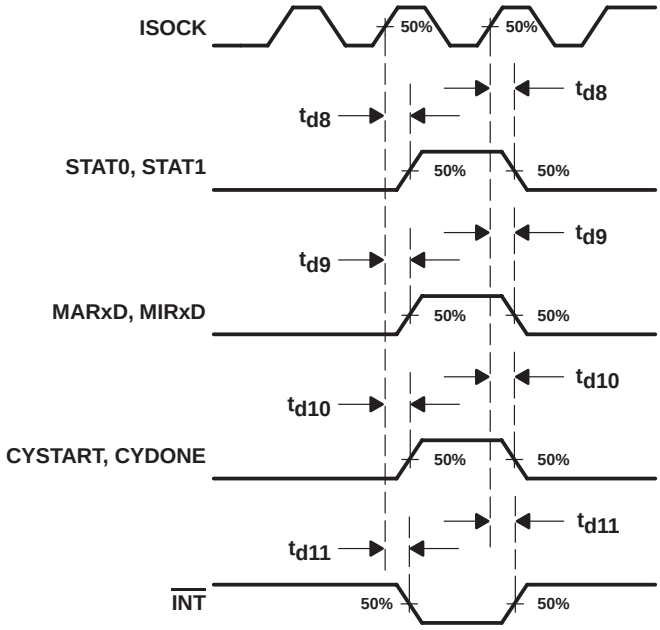
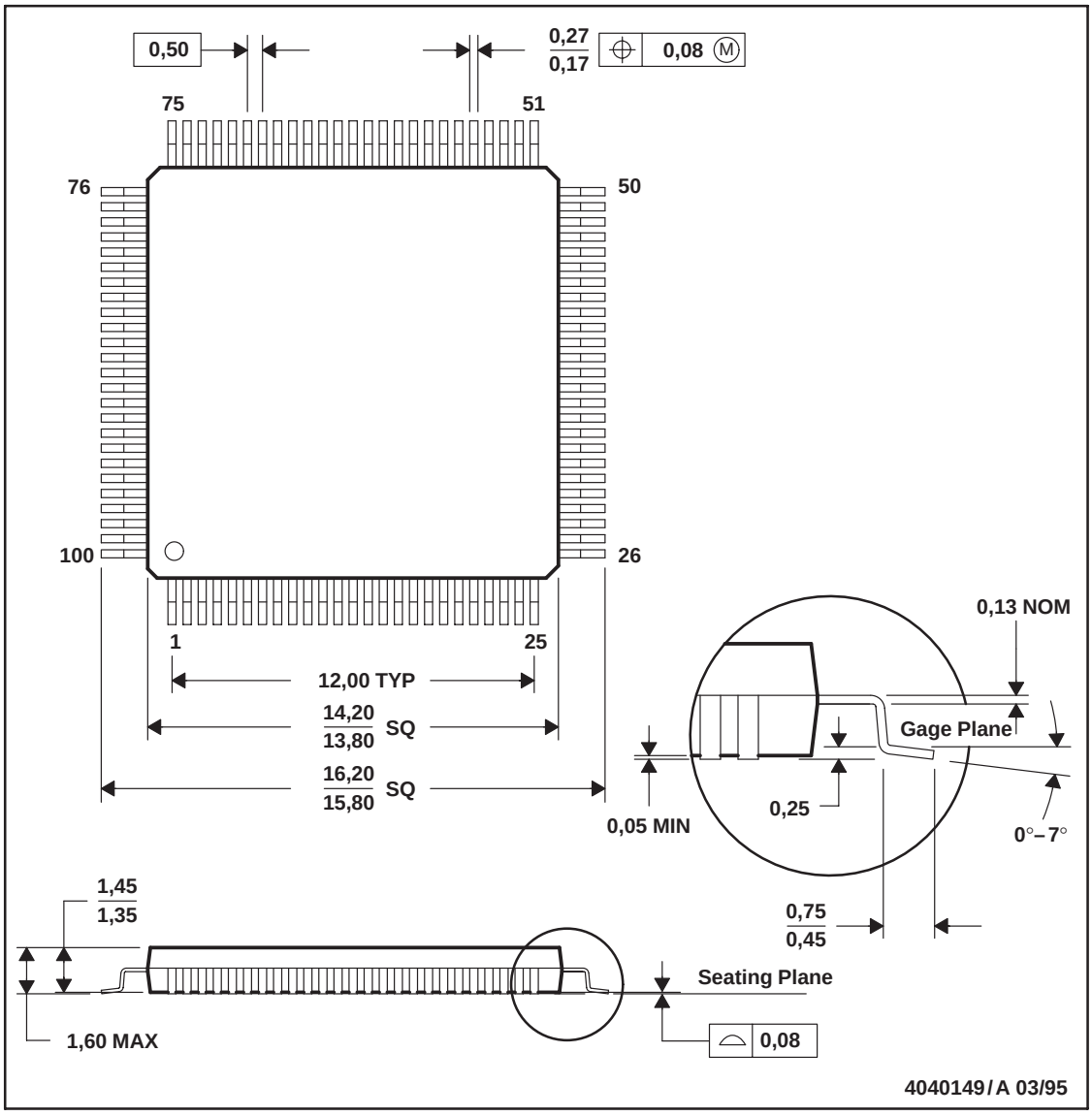


Figure 6–11. Synchronous ISOCK Output Waveforms

7 Mechanical Information

The TSB12LV31 is packaged in a high-performance 100-pin PZ package. The following shows the mechanical dimensions of the PZ package.

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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