1394 Design Schematic (TSBKBACKPL)

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TEXAS INSTRUMENTS

1394 Solutions Leader

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TSBKBACKPL EVM

- Interfacing TMS320C52 DSP to 12C01A
- Example of 12C01A to 14C01 to FB1650 (LLC to Backplane Phy to BTL Backplane)
- Example of 12C01A to 11C01 (100Mbps)
- Example of 12C01A to 21LV03 (200Mbps)
- Bridging BP to Cable and Cable to Cable
- FPGA Code, DSP C Code
- DM from 12C01A to SRAM

Acknowledgement:

The TSBKBACKPL (Backplane) evaluation board was designed for Texas Instruments, Inc. by Technobox, Inc.

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Errata for Backplane EVM board - 07/06/96

On schematic page 7 & 8:
The connections to the power programming pins on the TSB11C01 and TSB21LV03 are all tied low. Per the 1394-1995 standard table for the Self-ID Packet this is incorrect. This node is self-powered and supplies power to the cable. The amount of power will depend on the power supply used with the external power connector shown on schematic page 5.

Also note this board correctly pulls the TSB11C01 and TSB21LV03 Configuration Manager Contender (CMC) pin low to indicate that this board is not a contender to be the bus manager or isochronous resource manager. However what is missing for this board to be eligible for those roles is the necessary SW. If the user creates SW to support these roles this pin would need to be pulled high.

The files for the backplane/bridging reference design have the following extensions:

.asm - TMS320C52 assembler source code
.bat - DOS batch files
*.c - TMS320C52 C source code
.cfg - PCAD configuration files
.cmd - Command files for the DOS based TMS320C52 linker, emulator, & ROM HEX code generator
.HEX - ROM code
.HXM - Hex map created by ROM HEX code generator
.LIB - Library file
.LST - Listing file
.map - Link map
.obj - TMS320C52 intermediate object code
.out - TMS320C52 executable code
.pcb - PCAD PWB database
.sch - ORCAD format schematic pages
.src - Source code for the programming inside the Mach445 FPGA

This design does not incorporate galvanic isolation.

TSBKBACKPL (Backplane) Evaluation Module (EVM) board

Discussion

The backplane test board design has several goals in mind: serve as a test vehicle for the TSB14C01 backplane PHY, demonstrate use of the TSB21LV03 and TSB11C01 PHYs, and, via appropriate software, demonstrate 1394 to 1394 bridging.

As seen in the block diagram there are three TSB12C01A link layer controllers (LLC) connected to corresponding TSB11C01, TSB21LV03, and TSB14C01 PHY chips. These LLCs are all connected to a common 32-bit central bus. The 32-bit bus also connects to a 32K x 32 bit SRAM (128KB total) and a 2-byte to 4-byte bus sizer.

The controlling processor in this design is a TMS320C52 DSP. The DSP runs at 33.33 MIPs, synchronous to the 33.3 MHz clock input to the TSB12C01A LLCs. The DSP handles a 1-port RS232 async interface, and firmware in the DSP emulates an N-8-1 UART at 19.2Kbaud. A 29F100 Flash Memory provides 64Kword program store for the DSP.

The 128KB SRAM is visible from the DSP in its 'Data Space' (i.e., when DS output from the DSP is asserted). A 2-byte to 4-byte bus sizer, controlled by the MACH-445, handles transfers between the 16-bit DSP bus and the SRAM on the 32-bit central bus.

A MACH445 complex PLD is incorporated into the design to control the board. Functions include DSP address decode resulting in I/O read/write strobe generation, Bus sizer control, LLC handshake control (CS/CA), and a single channel DMA controller.

The DMA controller performs transfers between a selected TSB12C01A LLC and SRAM. A 'link' register inside the MACH445 is programmed by the DSP to identify which TSB12C01A will participate in the DMA transfer. The MACH445 maintains a 14-bit address counter, and 8-bit transfer counter, and logic to handle transfers between the SRAM and the selected LLC. The transfer counter counts quadlets, and therefore up to one K-byte can be transferred per DMA operation.

All communication with the TSB12C01A LLC, including accessing programming registers, is done through this DMA mechanism. DMA transfers between LLC and SRAM are all 32-bit, and the 16-bit DSP has full visibility of the data stored in SRAM via the 2-byte to 4-byte Bus Sizer.

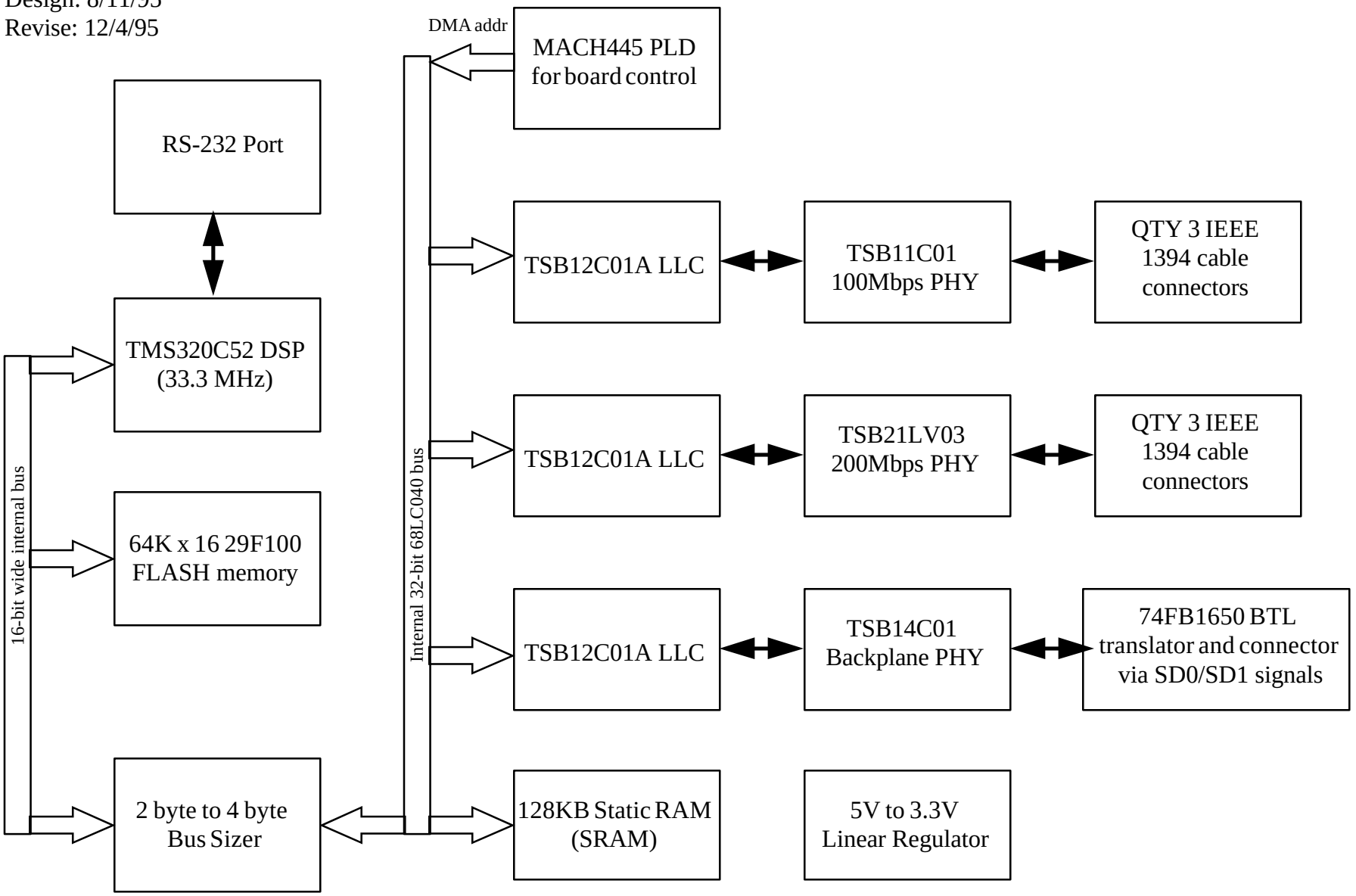
DMA transfers require that the DSP identify tow addresses: one is the SRAM address of the transfer, which is written to the MACH445 address counter, and a second identifies the TSB12C01A register address. An external latch for each TSB12C01A holds the TSB12C01A address input as programmed from the DSP.

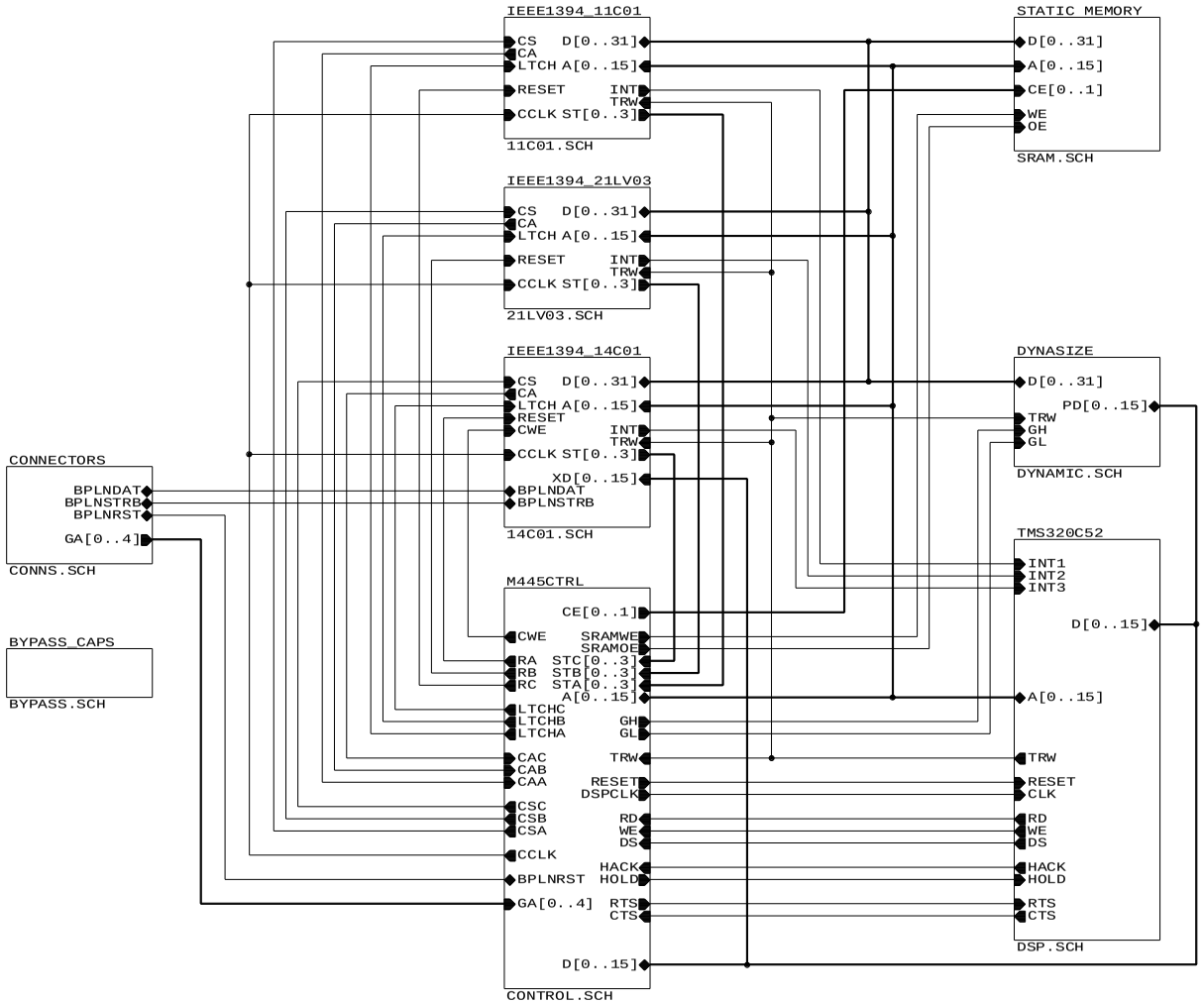
1394-to-1394 bridging can be accomplished by DSP software which reads packets from a source TSB12C01A LLC in SRAM buffers, and then transfers the packets in the SRAM buffer to a destination TSB12C01A.

The design features several 20-pin headers connected to key signals for logic analysis using an Hewlett Packard logic analyzer with standard termination adapters (See attached information on termination adapter). Also, there are 25-mil spare test points on the 1394 serial bus lines for observation using an oscilloscope.

TSBKBACKPL EVM Board

Design: 8/11/95
Revise: 12/4/95





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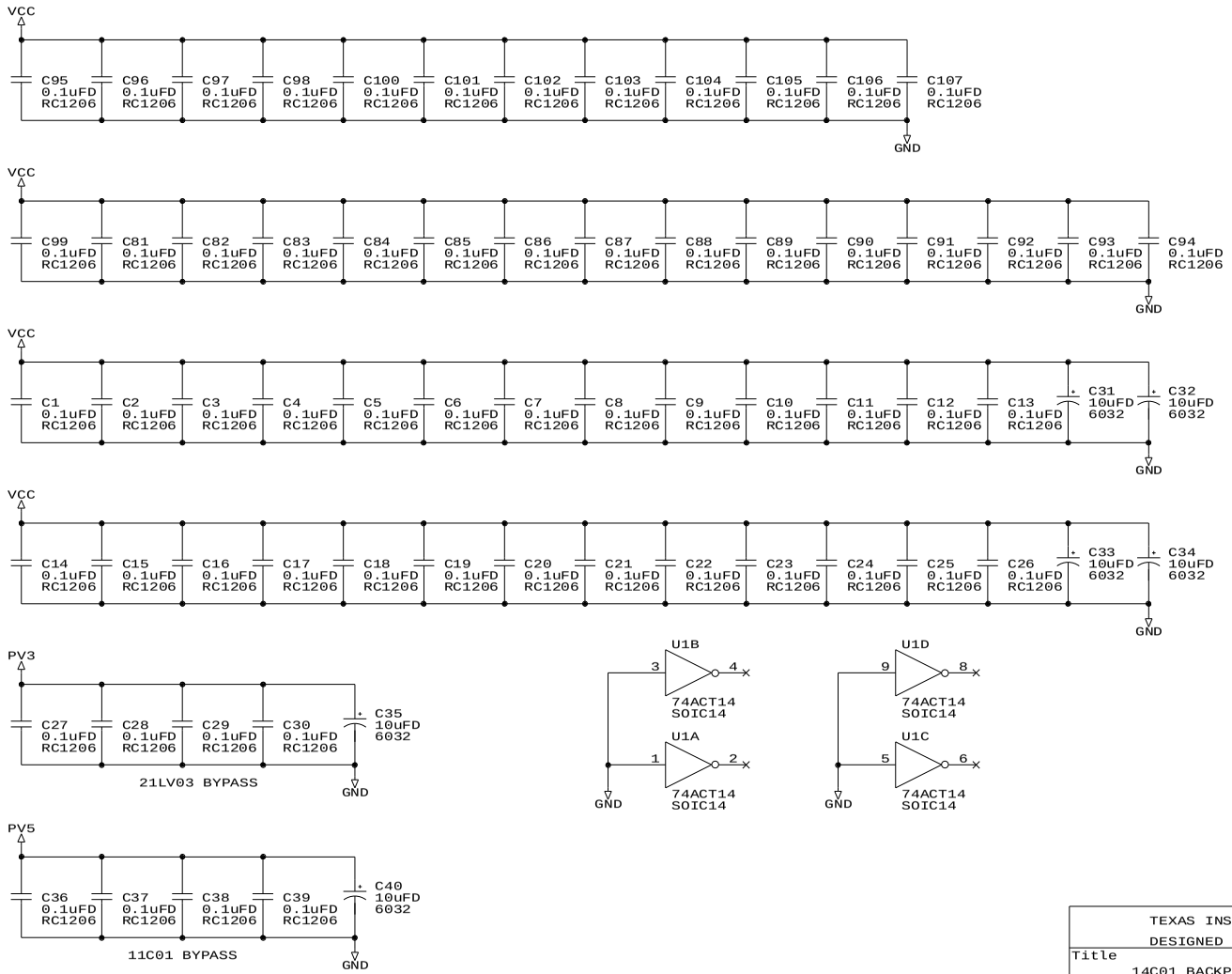
Title		
IEEE 1394 Backplane PHY board		
Size: B	Document Number	REV: 1
Date: September 2, 1996	Sheet 1 of 10	



TEXAS INSTRUMENTS, INC DESIGNED BY TECHNOBOX, INC.		
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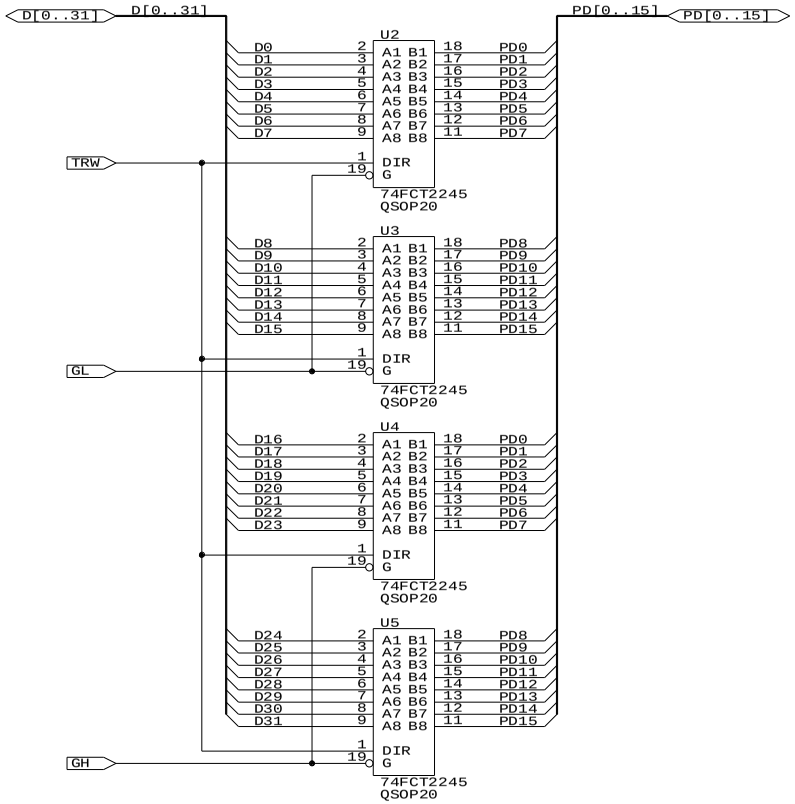
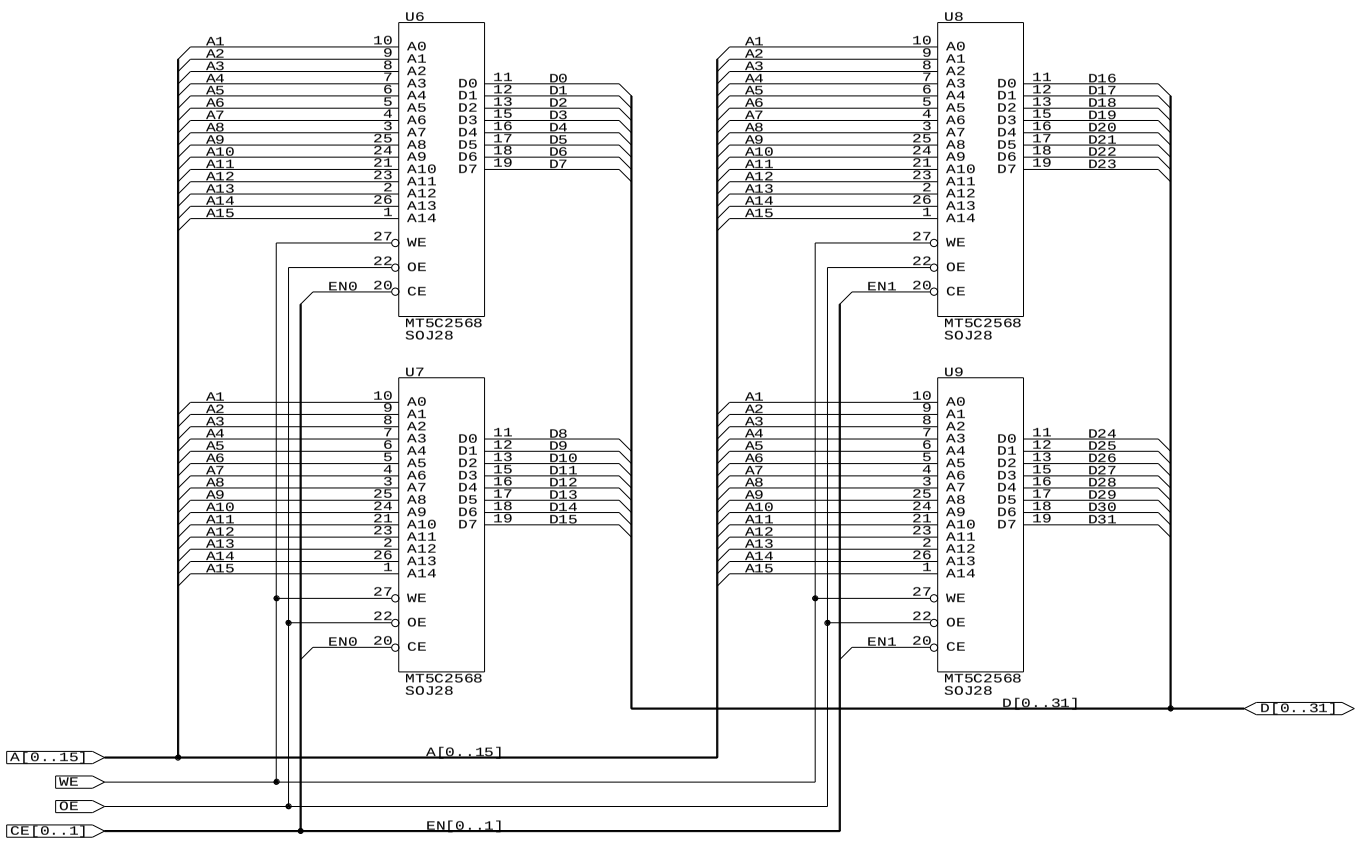
Size B	Document Number BPLN1394	REV 1
Date: December 16, 1995	Sheet 2 of 10	



DYNAMIC BUS SIZER

TEXAS INSTRUMENTS, INC DESIGNED BY TECHNOBOX, INC.		
Title 14C01 BACKPLANE PHY TEST BOARD		
Size B	Document Number BPLN1394	REV 1
Date: April 2, 1996	Sheet 3 of 10	



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DESIGNED BY TECHNOBOX, INC.		
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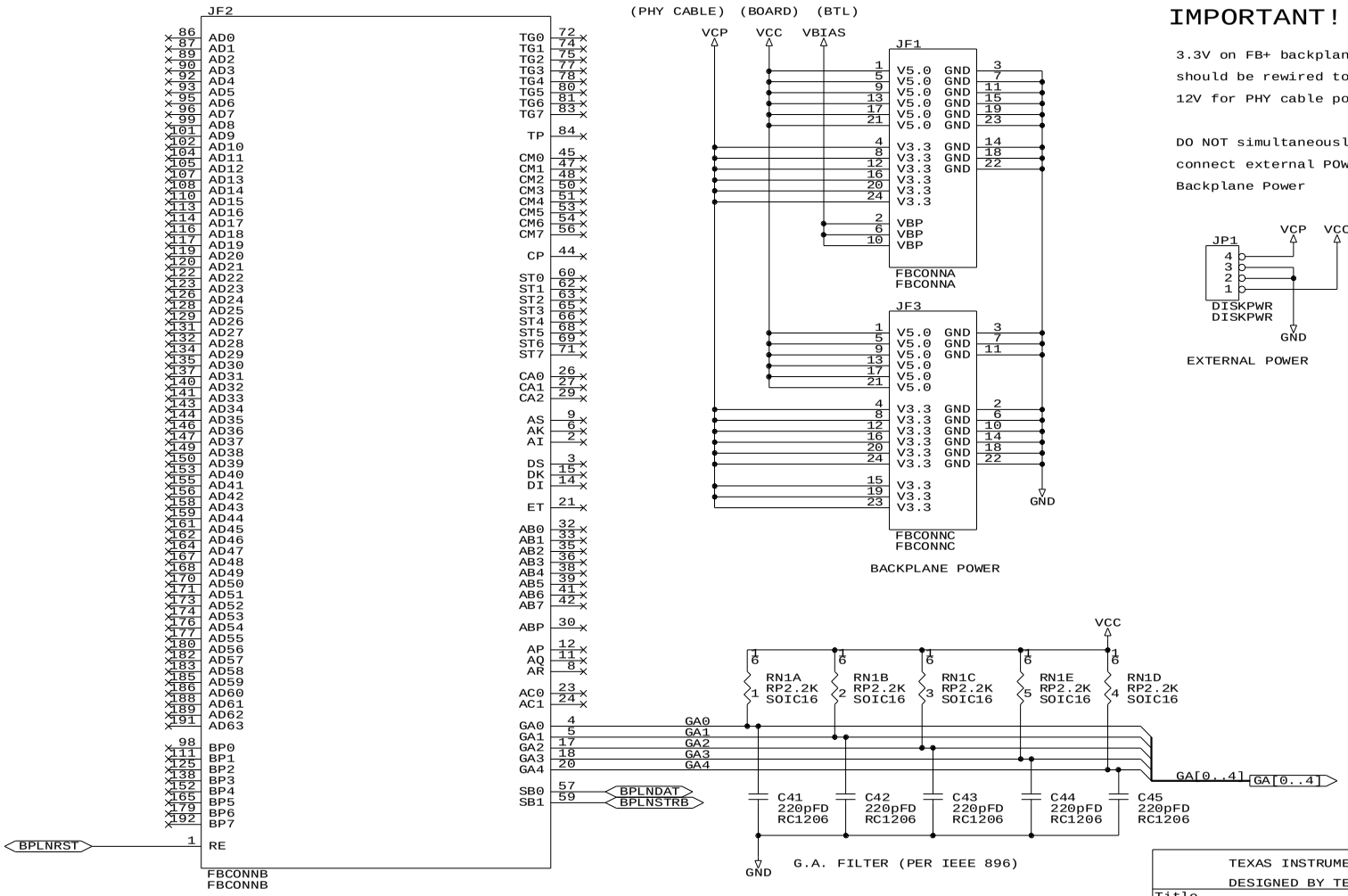
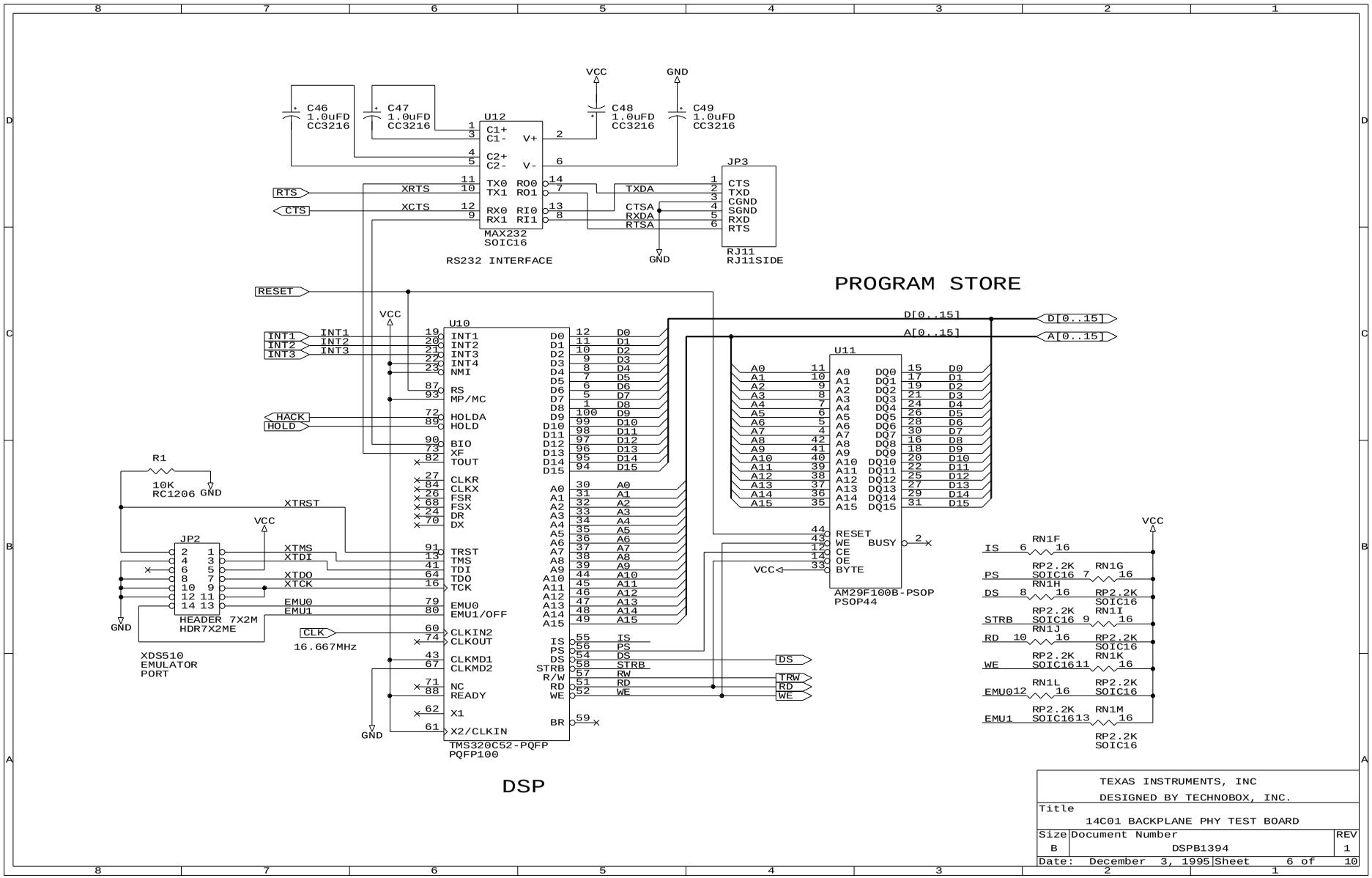
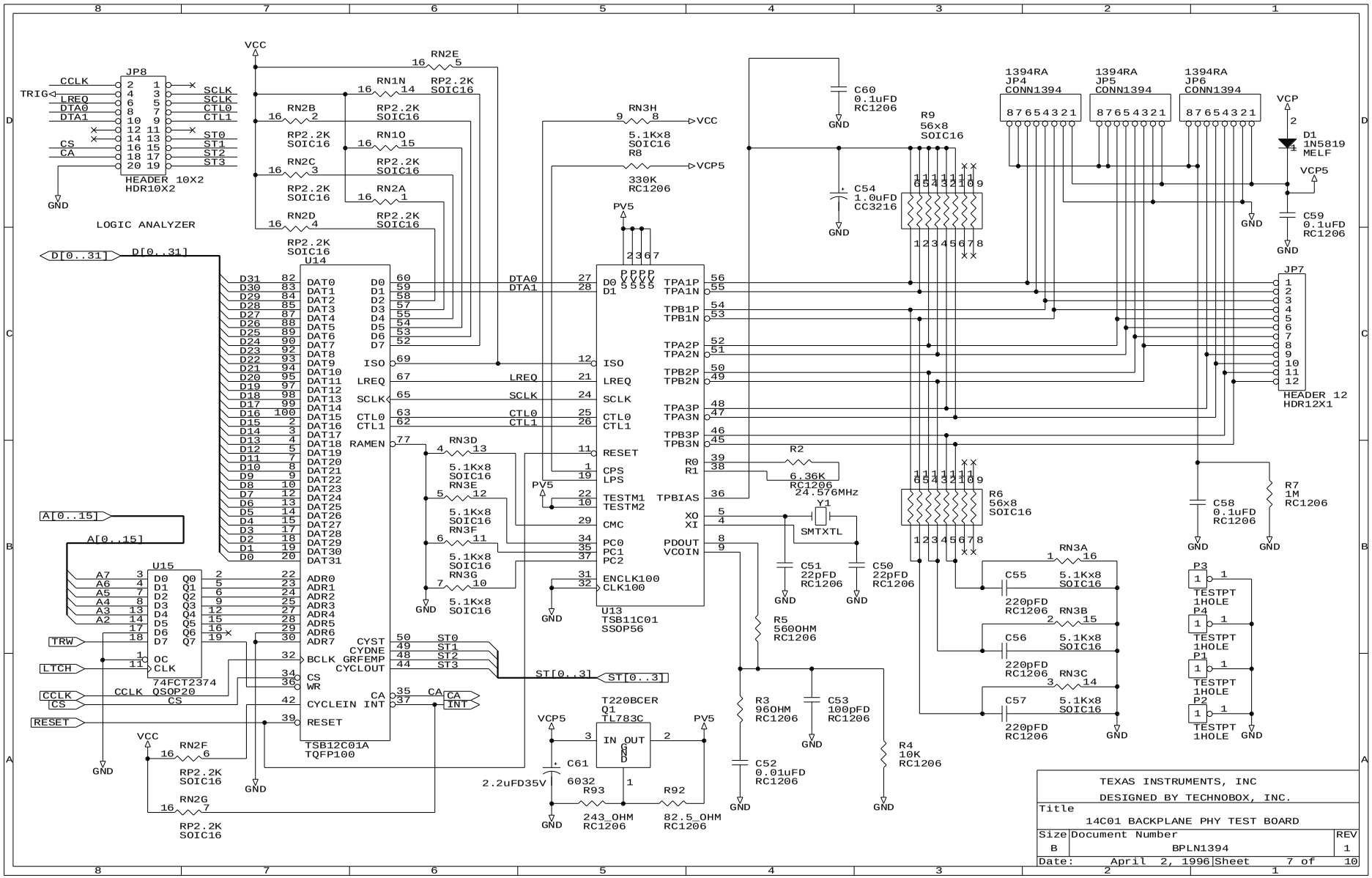
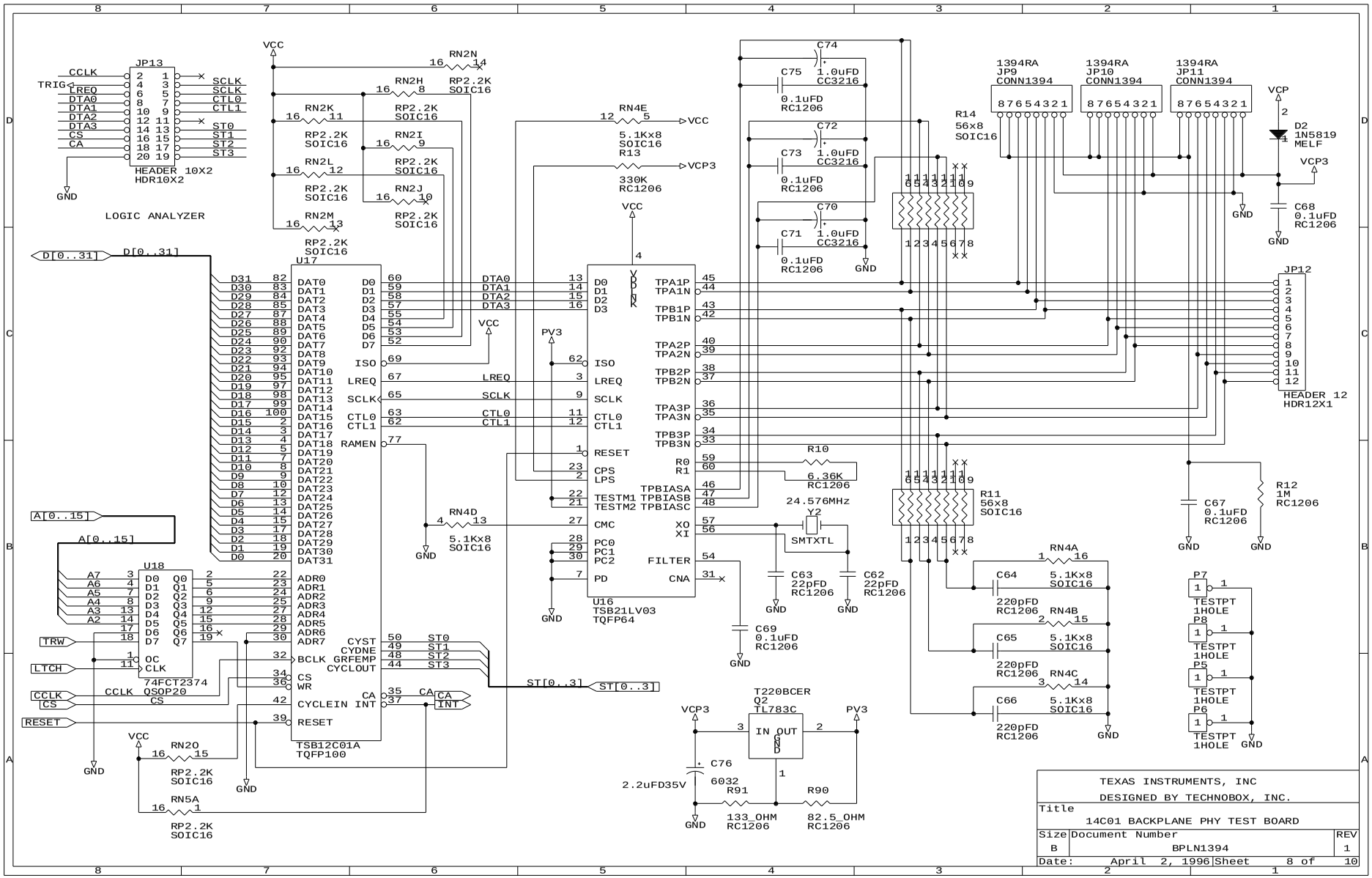
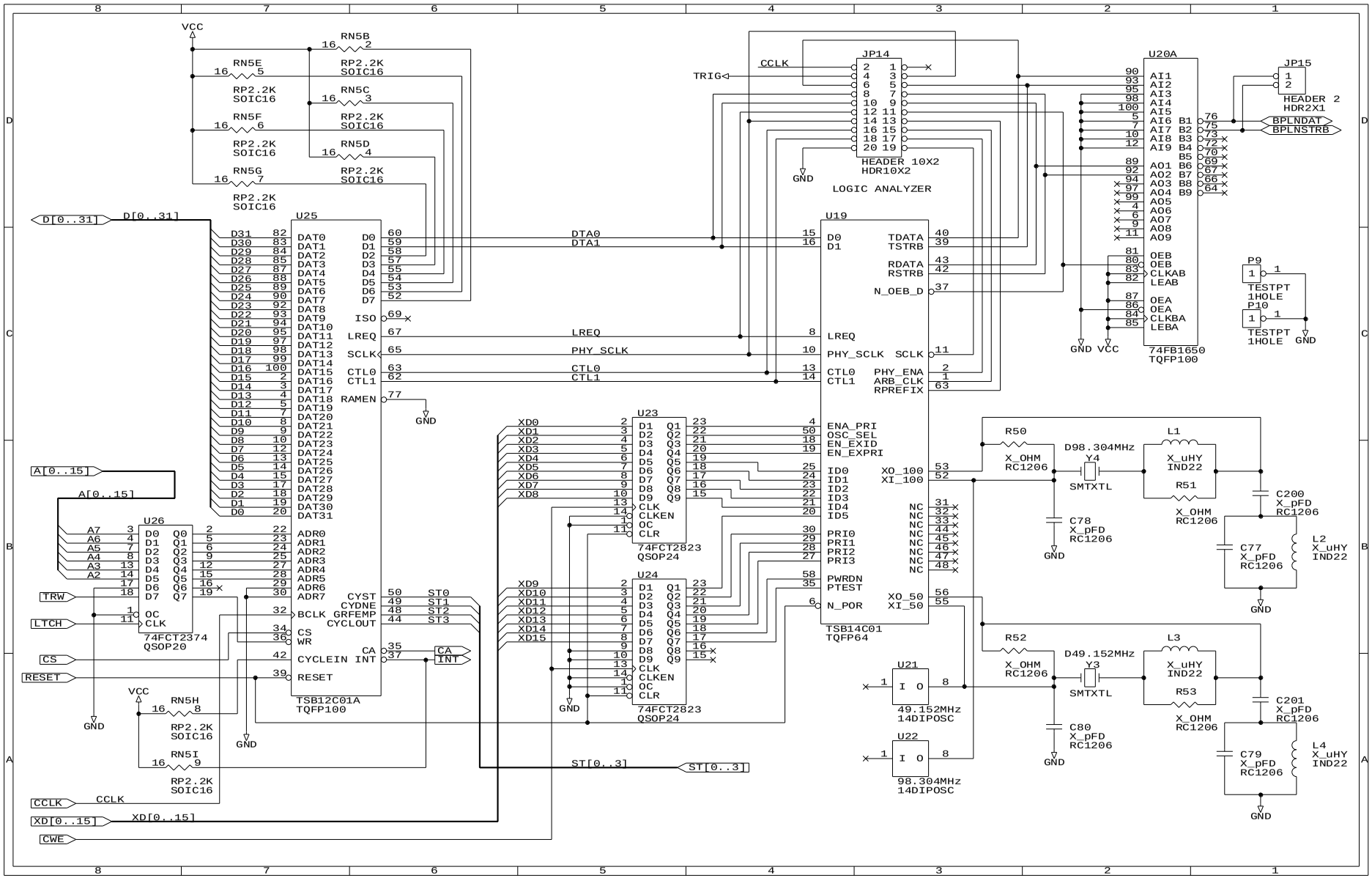
Size: B	Document Number: BPLN1394	REV: 1
Date: December 3, 1995	Sheet 4 of 10	


JF2
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
AD32
AD33
AD34
AD35
AD36
AD37
AD38
AD39
AD40
AD41
AD42
AD43
AD44
AD45
AD46
AD47
AD48
AD49
AD50
AD51
AD52
AD53
AD54
AD55
AD56
AD57
AD58
AD59
AD60
AD61
AD62
AD63
BP0
BP1
BP2
BP3
BP4
BP5
BP6
BP7
RE
TG0
TG1
TG2
TG3
TG4
TG5
TG6
TG7
TP
CM0
CM1
CM2
CM3
CM4
CM5
CM6
CM7
CP
ST0
ST1
ST2
ST3
ST4
ST5
ST6
ST7
CA0
CA1
CA2
AS
AK
AI
DS
DK
DI
ET
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
ABP
AP
AQ
AR
AC0
AC1
GA0
GA1
GA2
GA3
GA4
SB0
SB1
BPLNRST
BPLNDAT
BPLNSTRB
FBCONNB
FBCONNB
(PHY CABLE) (BOARD) (BTL)
VCP
VCC
VBIAS
JF1
V5.0
GND
V3.3
VBP
FBCONNA
FBCONNA
JF3
FBCONNC
FBCONNC
GND
BACKPLANE POWER
IMPORTANT!
3.3V on FB+ backplane
should be rewired to
12V for PHY cable power
DO NOT simultaneously
connect external POWER and
Backplane Power
JP1
DISKPWR
DISKPWR
EXTERNAL POWER
RN1A
RN1B
RN1C
RN1E
RN1D
RP2.2K
SOIC16
C41
C42
C43
C44
C45
220pFD
RC1206
G.A. FILTER (PER IEEE 896)
GA[0..4]
TEXAS INSTRUMENTS, INC
DESIGNED BY TECHNOBOX, INC.
Title
14C01 BACKPLANE PHY TEST BOARD
Size
B
Document Number
BPLN1394
REV
1
Date: December 15, 1995
Sheet 5 of 10


C46 1.0uFD CC3216
C47 1.0uFD CC3216
C48 1.0uFD CC3216
C49 1.0uFD CC3216
VCC
GND
U12
C1+
C1-
V+
C2+
C2-
V-
TX0
TX1
RO0
RO1
RX0
RX1
RI0
RI1
MAX232
SOIC16
RS232 INTERFACE
RTS
CTS
XRTS
XCTS
TXDA
CTSA
RXDA
RTSA
JP3
CTS
TXD
CGND
SGND
RXD
RTS
RJ11
RJ11SIDE
PROGRAM STORE
RESET
D[0..15]
A[0..15]
U11
AM29F100B-PSOP
PSOP44
U10
INT1
INT2
INT3
INT4
NMI
RS
MP/MC
HOLDA
HOLD
BIO
XF
TOUT
CLKR
CLKX
FSR
FSX
DR
DX
TRST
TMS
TDI
TDO
TCK
EMU0
EMU1/OFF
CLKIN2
CLKOUT
CLKMD1
CLKMD2
NC
READY
X1
X2/CLKIN
BR
R1
10K
RC1206
XTRST
JP2
XTMS
XTDI
XTDO
XTCK
EMU0
EMU1
HEADER 7X2M
HDR7X2ME
XDS510
EMULATOR
PORT
CLK
16.667MHz
IS
PS
DS
STRB
R/W
RD
WE
TRW
RN1F
RN1G
RN1H
RN1I
RN1J
RN1K
RN1L
RN1M
RP2.2K
SOIC16
DSP
TEXAS INSTRUMENTS, INC
DESIGNED BY TECHNOBOX, INC.
Title
14C01 BACKPLANE PHY TEST BOARD
Size
B
Document Number
DSPB1394
REV
1
Date: December 3, 1995
Sheet 6 of 10


JP8
HEADER 10X2
HDR10X2
LOGIC ANALYZER
U14
TSB12C01A
TQFP100
U15
74FCT2374
U13
TSB11C01
SSOP56
JP4
JP5
JP6
1394RA
CONN1394
JP7
HEADER 12
HDR12X1
Y1
24.576MHz
SMTXTL
Q1
TL783C
TEXAS INSTRUMENTS, INC
DESIGNED BY TECHNOBOX, INC.
Title
14C01 BACKPLANE PHY TEST BOARD
Size B
Document Number BPLN1394
REV 1
Date: April 2, 1996
Sheet 7 of 10


JP13
HEADER 10X2
HDR10X2
LOGIC ANALYZER
U17
TSB12C01A
TQFP100
U18
74FCT2374
QSOP20
U16
TSB21LV03
TQFP64
JP12
HEADER 12
HDR12X1
1394RA
JP9
CONN1394
1394RA
JP10
CONN1394
1394RA
JP11
CONN1394
Q2
TL783C
Y2
24.576MHz
SMTXTL
TESTPT
1HOLE
TEXAS INSTRUMENTS, INC
DESIGNED BY TECHNOBOX, INC.
Title
14C01 BACKPLANE PHY TEST BOARD
Size
B
Document Number
BPLN1394
REV
1
Date: April 2, 1996
Sheet 8 of 10


VCC
RN5B
RN5E
RN5C
RN5F
RN5D
RN5G
RP2.2K SOIC16
D[0..31]
U25
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
DAT8
DAT9
DAT10
DAT11
DAT12
DAT13
DAT14
DAT15
DAT16
DAT17
DAT18
DAT19
DAT20
DAT21
DAT22
DAT23
DAT24
DAT25
DAT26
DAT27
DAT28
DAT29
DAT30
DAT31
ISO
LREQ
SCLK
CTL0
CTL1
RAMEN
ADR0
ADR1
ADR2
ADR3
ADR4
ADR5
ADR6
ADR7
CYST
CYDNE
BCLK
GRFEMP
CYCLOUT
CS
WR
CA
CYCLEIN
INT
RESET
TSB12C01A
TQFP100
GND
DTA0
DTA1
LREQ
PHY SCLK
CTL0
CTL1
ST0
ST1
ST2
ST3
ST[0..3]
A[0..15]
U26
74FCT2374
QSOP20
OC
CLK
TRW
LTCH
CS
RESET
CA
INT
RN5H
RN5I
CCLK
XD[0..15]
CWE
U23
U24
74FCT2823
QSOP24
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
XD8
XD9
XD10
XD11
XD12
XD13
XD14
XD15
CLK
CLKEN
OC
CLR
TRIG
JP14
HEADER 10X2
HDR10X2
LOGIC ANALYZER
U19
D0
D1
TDATA
TSTRB
RDATA
RSTRB
N_OEB_D
LREQ
PHY_SCLK
SCLK
CTL0
CTL1
PHY_ENA
ARB_CLK
RPREFIX
ENA_PRI
OSC_SEL
EN_EXID
EN_EXPRI
ID0
ID1
ID2
ID3
ID4
ID5
PRI0
PRI1
PRI2
PRI3
PWRDN
PTEST
N_POR
XO_100
XI_100
XO_50
XI_50
NC
TSB14C01
TQFP64
U20A
AI1
AI2
AI3
AI4
AI5
AI6
AI7
AI8
AI9
AO1
AO2
AO3
AO4
AO5
AO6
AO7
AO8
AO9
B1
B2
B3
B4
B5
B6
B7
B8
B9
OEB
OEB
CLKAB
LEAB
OEA
OEA
CLKBA
LEBA
74FB1650
TQFP100
JP15
HEADER 2
HDR2X1
BPLNDAT
BPLNSTRB
P9
P10
TESTPT
1HOLE
R50
R52
X_OHM
RC1206
D98.304MHz
D49.152MHz
Y4
Y3
SMTXTL
L1
L3
X_uHY
IND22
R51
R53
C200
C201
X_pFD
RC1206
C78
C77
C80
C79
L2
L4
U21
U22
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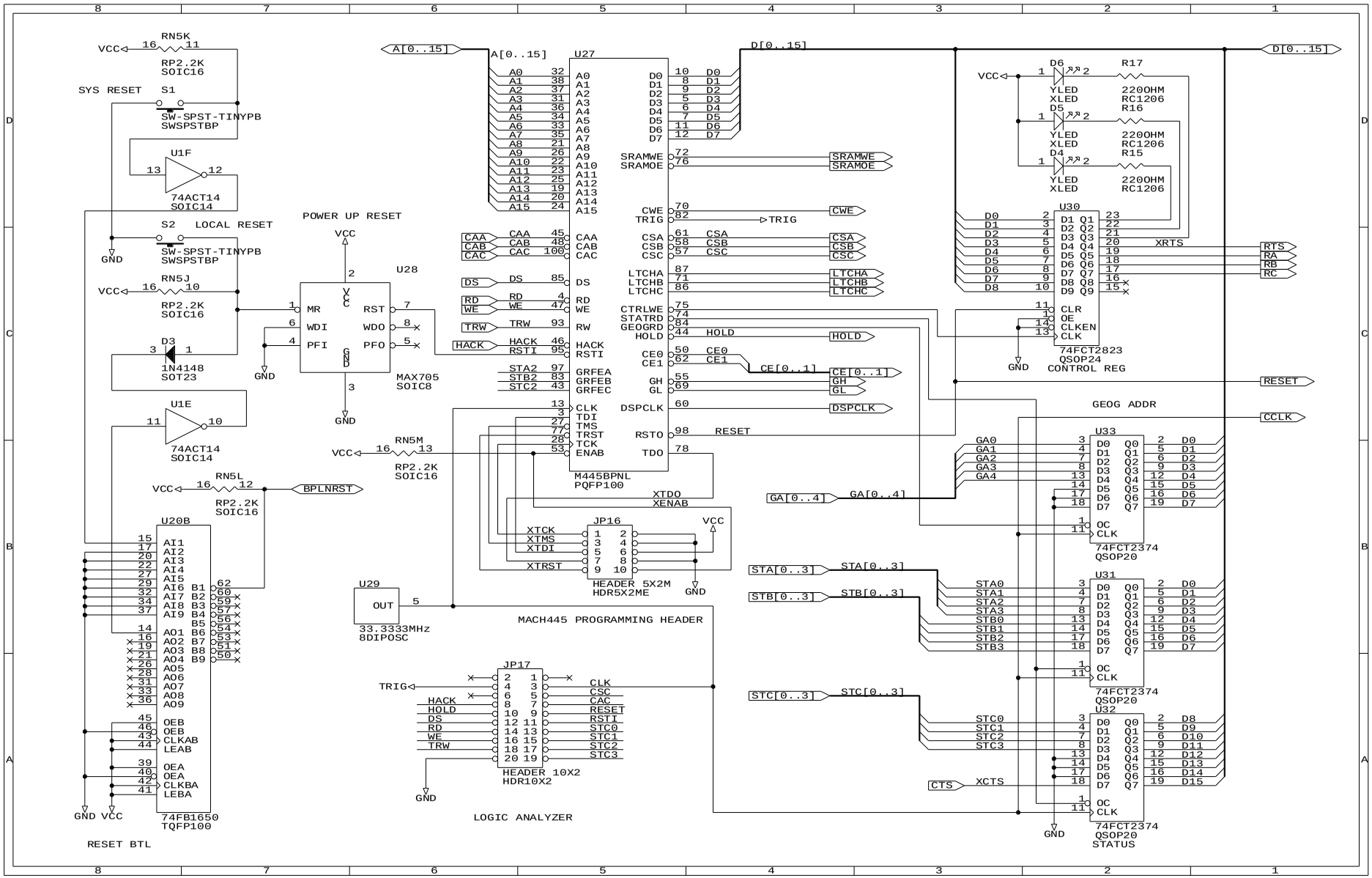
14DIPOSC
98.304MHz


RN5K
RP2.2K
SOIC16
SYS RESET
S1
SW-SPST-TINYPB
SWSPSTBP
U1F
74ACT14
SOIC14
S2 LOCAL RESET
SW-SPST-TINYPB
SWSPSTBP
RN5J
RP2.2K
SOIC16
D3
1N4148
SOT23
U1E
74ACT14
SOIC14
POWER UP RESET
U28
MAX705
SOIC8
RN5M
RP2.2K
SOIC16
RN5L
RP2.2K
SOIC16
BPLNRST
U20B
74FB1650
TQFP100
RESET BTL
U29
33.3333MHz
8DIPOSC
U27
M445BPNL
PQFP100
JP16
HEADER 5X2M
HDR5X2ME
MACH445 PROGRAMMING HEADER
JP17
HEADER 10X2
HDR10X2
LOGIC ANALYZER
D6
D5
D4
R17
R16
R15
220OHM
RC1206
YLED
XLED
U30
74FCT2823
QSOP24
CONTROL REG
XRTS
RTS
RA
RB
RC
RESET
CCLK
GEOG ADDR
U33
U31
U32
74FCT2374
QSOP20
STATUS
XCTS
CTS
GND
VCC