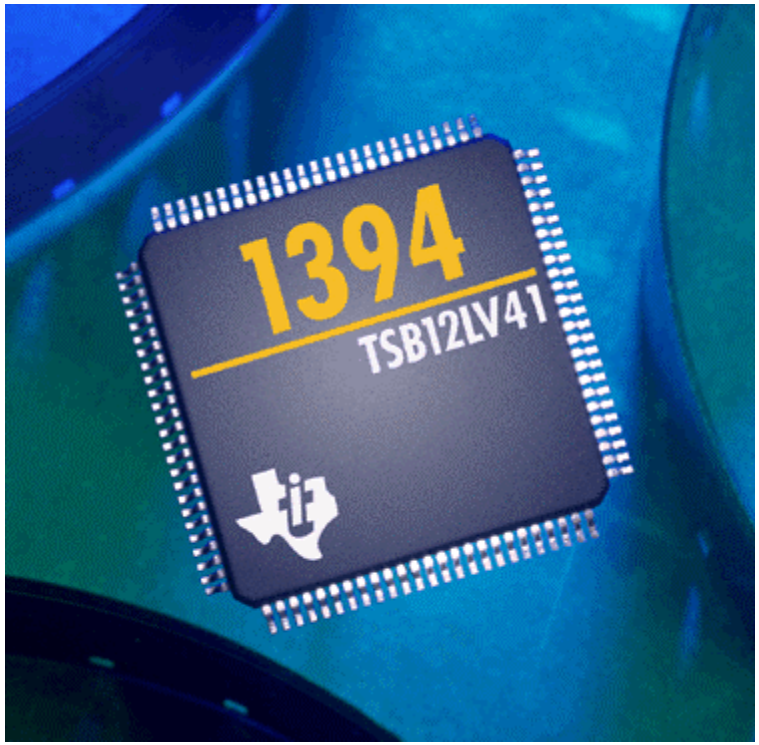
Texas Instruments TSB12LV41

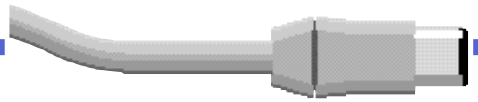
1394-1995 Link-Layer Controller for MPEG2 Transport



Steve Schnier

MPEG2Lynx Overview Agenda

- Overview of Market and Applications for MPEG2Lynx
- MPEG2 transmission over 1394 (IEC1883)
- Features of MPEG2Lynx
- Description of MPEG2Lynx Interfaces (BDIF, Micro)
- Software Architecture
- Software Flows
- Physical Layers for Complete Solution



Consumer Market

Products include:

DV Camcorders

Digital Recorder Decks

Digital Still Cameras

Digital Set-top Boxes

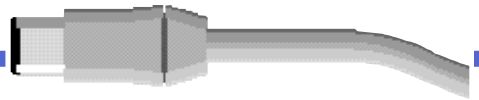
Isochronous HDD

DVD Movie Players

Musical I/O Devices

Digital TVs

Converter Boxes



Consumer Market - Notes

Consumer Electronics Applications for 1394

The majority of the informative illustrations in the 1394 standard show interconnections between consumer video devices, with and without attached PCs. Based on the draft standard, 1394 Trade Association documents, and conversations with members of the Association, following are the primary consumer electronics applications anticipated for the High Performance Serial Bus. The products are listed in the author's forecast order of their introduction to the retail market.

•Digital camcorders and DVCRs (Sony DCR-VX700, DCR-VX1000, and DCR-PC7 camcorders, Sony DHR-1000

•DVCR, Sony DSR-30 DVCAM DVTR, and new Panasonic DV camcorders)

•Digital videoconferencing systems using the Sony CCM-DS250 digital camera, which became generally available in early 1997

•Direct-to-home (DTH) satellite video and audio MPEG-2 data streams*

•Musical synthesizers with MIDI and digital audio capabilities, initially from Yamaha

•Printers for video and computer data

•Fixed and removable PC disk drives, internal and external

•PC-to-PC networking (the 1394 "home PC network") and PC peripheral component sharing

•Cable TV and MMDS ("wireless cable") set-top boxes

•Digital video disk (DVD) drives

*Thomson/RCA receivers for DirecTV and USSB DSS satellite programming presently have an unused high-speed parallel data port intended to transmit MPEG-encoded video and audio to a digital tape recorder for time-shift recording. A Thomson/Hitachi digital VCR using JVC's D-VHS 1/2-inch bitstream recording format was announced in 1994 for availability in early 1996, together with an upgraded version of the Thomson/RCA DBS receiver. Despite the press releases, this combination didn't arrive. At the 1997 Winter Consumer Electronics show, Hitachi exhibited a prototype of its DX815 D-VHS recorder, which uses a non-standard implementation of 1394 to connect the recorder to a Hitachi DSS set-top box. Thomson did not display a D-VHS deck, but is expected to announce a similar product later in 1997. The R-4.1 ATV Receiver Interface Subcommittee of the Consumer Electronics Manufacturers Association (CEMA, formerly the Consumer Electronics Group) of the Electronic Industries Association is supporting a proposal to the IEC TC84 committee for a transport layer over fully-compliant 1394 to handle MPEG-2 and other digital data streams associated with Digital (Standard- and High-Definition) TV.

Implementation of the consumer electronics device control protocol is the subject of "Specifications of AV/C Command and Transaction Set for Digital Interface," by Sony Corp. and Matsushita Electric Industry Co., Ltd., presented to the January 1996 meeting of the 1394 Trade Association. This specification defines VCR-like commands, such as Play, Record, Rewind, etc. This specification has been submitted to the IEC as proposal 61883.

1394 Specified by Standards Organizations

- VESA
  - Specified as connection for in-room cluster
  - Long distance and Bridging will be required for inter-room specification
- DAVIC
  - Specified as the required multimedia data port for the set-top box
  - Specified as the A0 (NIU to STB) connection if implemented separately
- "Blue Book"
  - Specification of Digital Interface for Consumer Electronic Audio/Video Equipment (12/95 HD Digital VCR Conference) proposed to IEC (IEC1883)
  - AV/C command set fully specified for DVC and MPEG
- EIA
  - EIA 4.1 subcommittee voted 1394 as the point-to-point interface for digital TV
  - Voted as the multi-point interface for entertainment systems
- ANSI
  - SCSI-3 Serial Bus Protocol (SBP) for HDD, CD-ROM, Printer, Scanner, etc.

1394 Specified by Standards Organizations - Notes

VESA

1394 is specified for the local (in-room) cluster, and is also tentatively specified for the longer (between rooms) connections. Long distance 1394 is needed for this, as are 1394 Bridges

DAVIC

Version 1.1 of the DAVIC specification was frozen at the September meeting, for publication at the December meeting. This includes 1394 as a required multimedia data port for the set top box. 1394 is also used as the connection between the NIU and STU parts of a set top box if the manufacturer chooses to build the box as two separate units.

The DAVIC Physical Layer Technical Committee accepted the 1394 TA liaison response that the NIU-STU 1394 connection should be standard 1394. DAVIC had considered specifying a slightly nonstandard implementation. The 1394 TA Silicon Working Group was able to provide a technical response that showed the DAVIC committee the advantages of the standard implementation.

Blue Book

AV/C command set specified for DVC and MPEG functions for DVCR, DV Camcorder, STB, DVHS, DVD, etc.

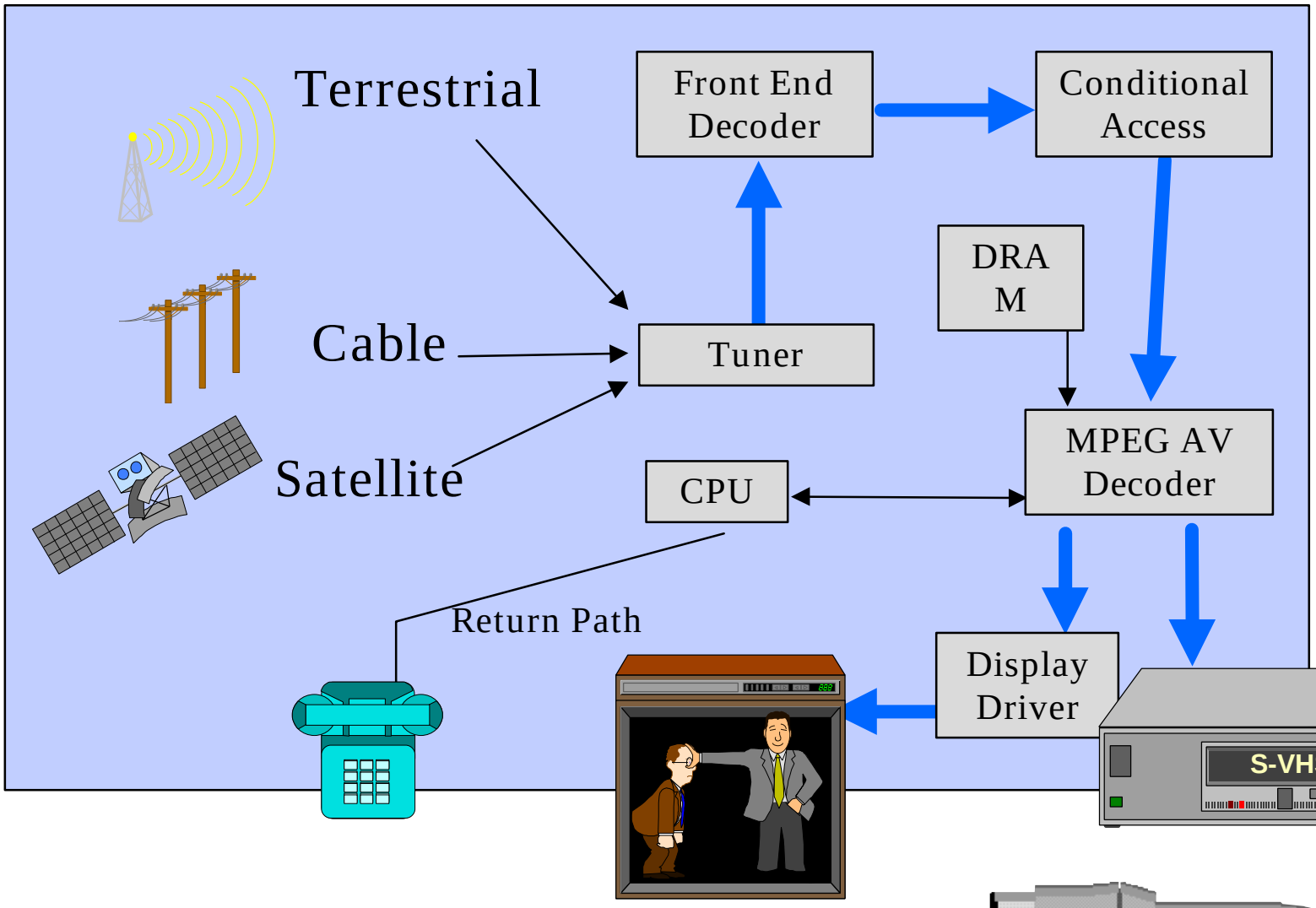
EIA

EIA 4.1 subcommittee has voted for IEEE 1394 as the point-to-point interface for digital TV as well as the multi-point interface for entertainment systems. The European Digital Video Broadcasters (DVB) have endorsed IEEE 1394 as their digital television interface as well.

ANSI

SCSI-3 Serial Bus Protocol (SBP), ANSI X3T10/992D revision 21 (HDD, CD-ROM, Printer, Scanner, PC)

Set-top Box with Analog Audio/Video Input



Set-top Box with Analog Audio/Video Input - Notes

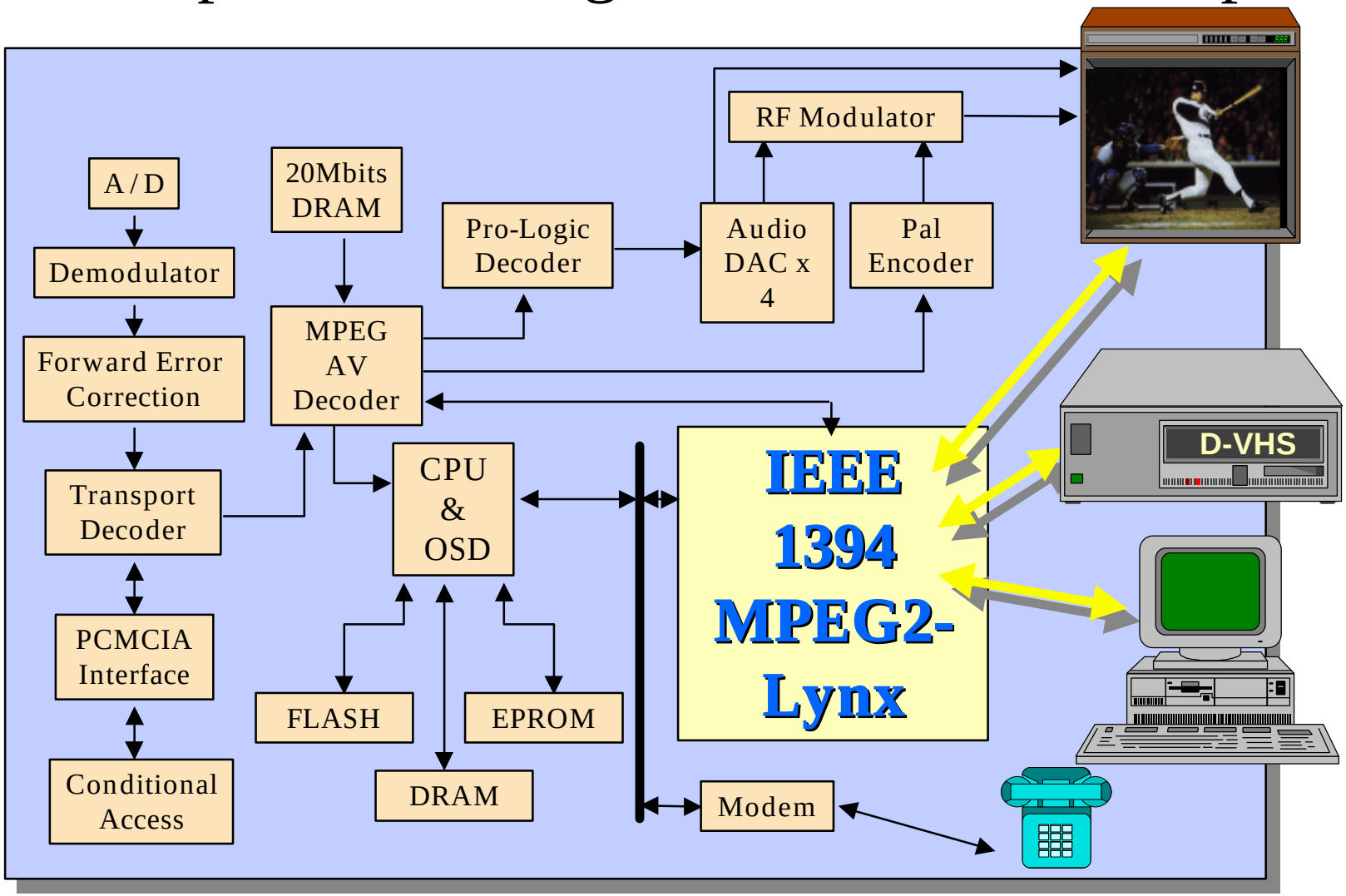
SUMMARY:

This is the basic architecture of a digital STB.

HIGHLIGHTS:

• Notice that the MPEG signal is digital, yet must be converted to an analog format for recording or display to a television.

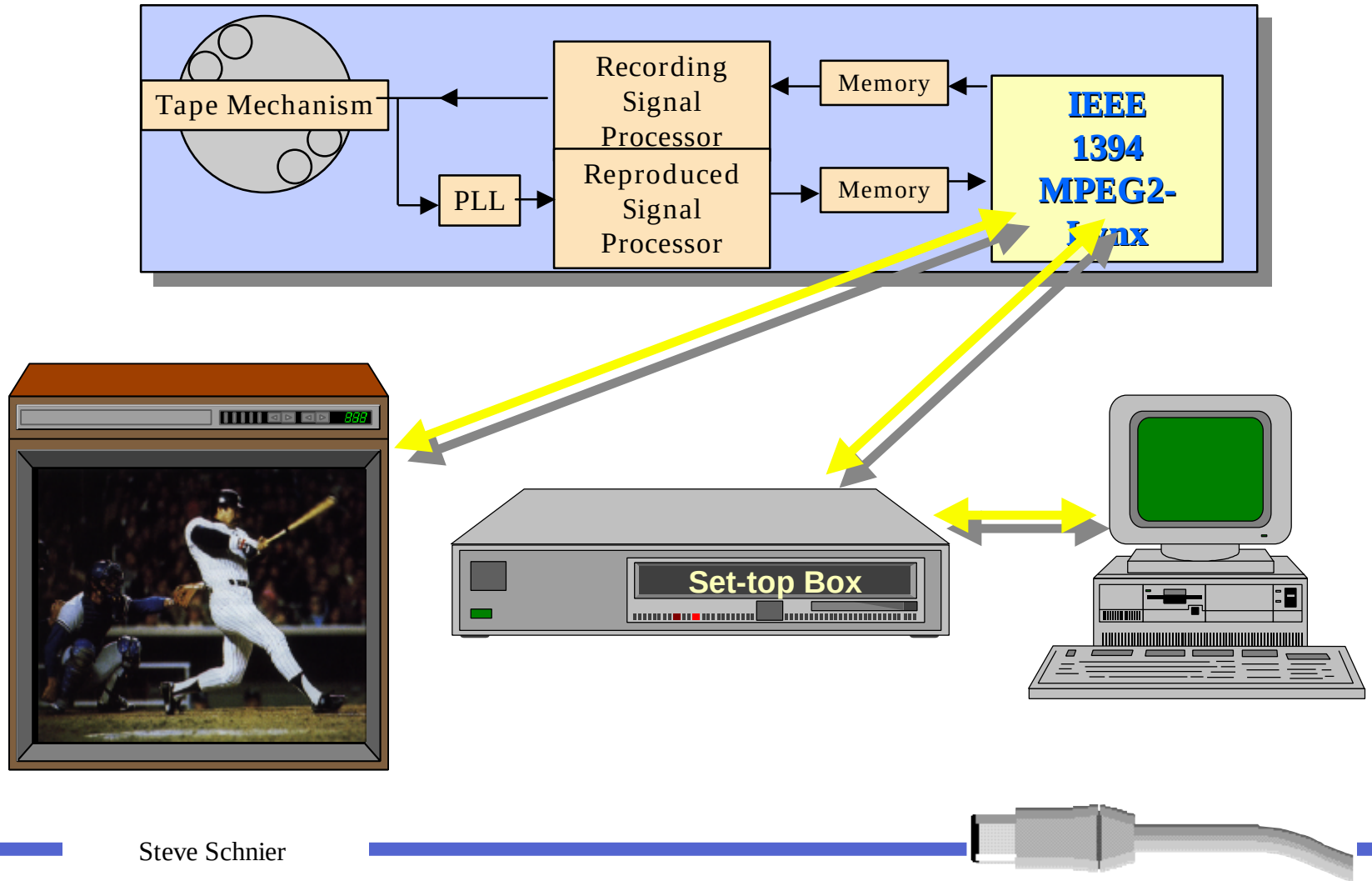
Set-top Box with digital Audio/Video Output



Set-top Box with digital Audio/Video Output - Notes

- By having an all digital solution, higher quality is achieved. The digital recording and playback, combined with the digital 1394 interface, completely eliminates the noise pick-up and signal losses that occur in analog systems and interconnects. The digital record/playback avoids the audio flutter and video picture jitter that is common in present analog systems.
- This superiority in quality drives large demand for these products.

Digital VCR with Digital Interface



Digital VCR with Digital Interface - Notes

Summary:

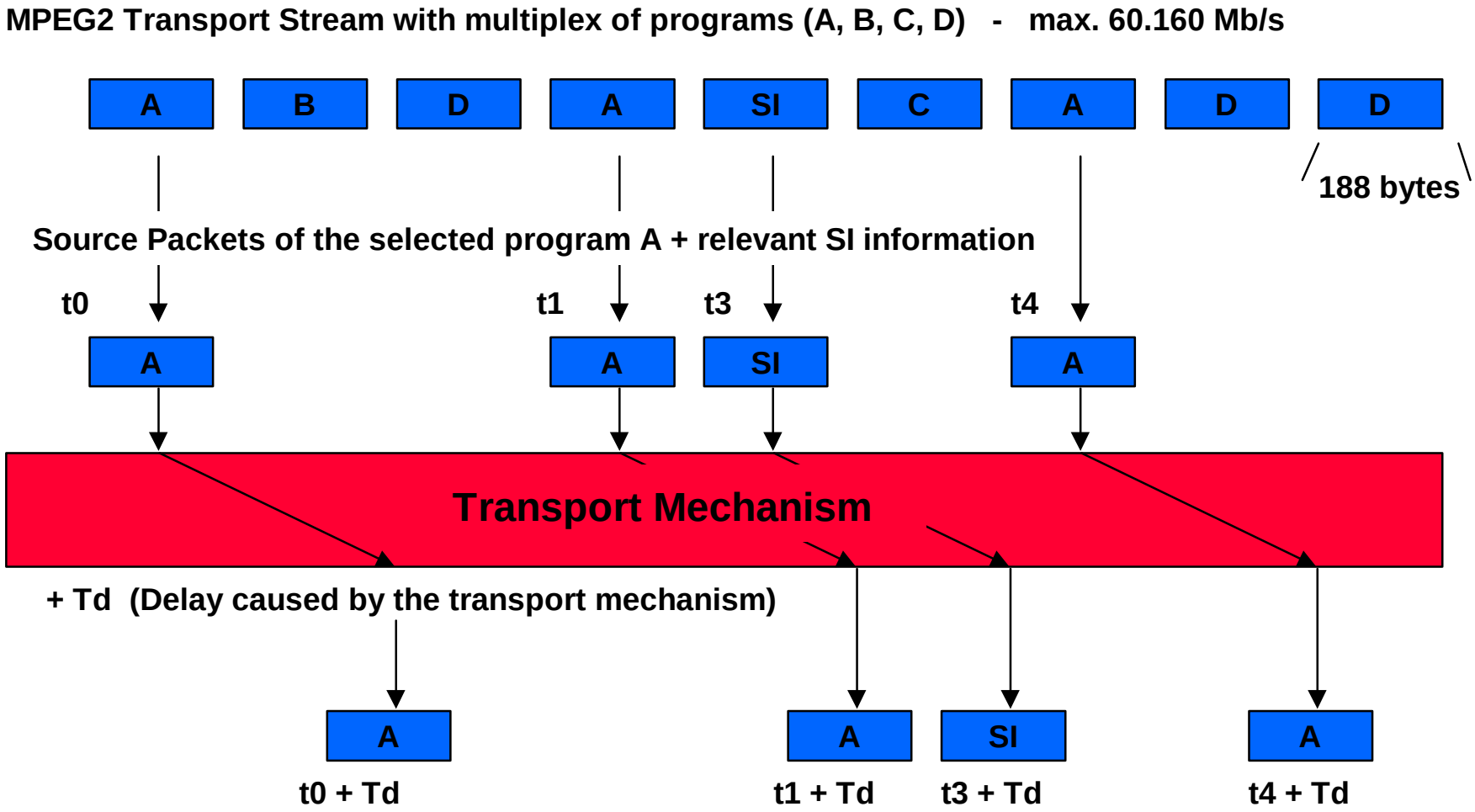
A digital recording device would be able to time-shift digital programs received through a DSS, DVB, or other digital receiver.

The set-top box would send the demuxed MPEG-2 audio and video stream to the VCR, where it would be recorded for playback at a later time. With the MPEG2Lynx, the memory requirement may be reduced depending on the latencies involved in the tape mechanism.

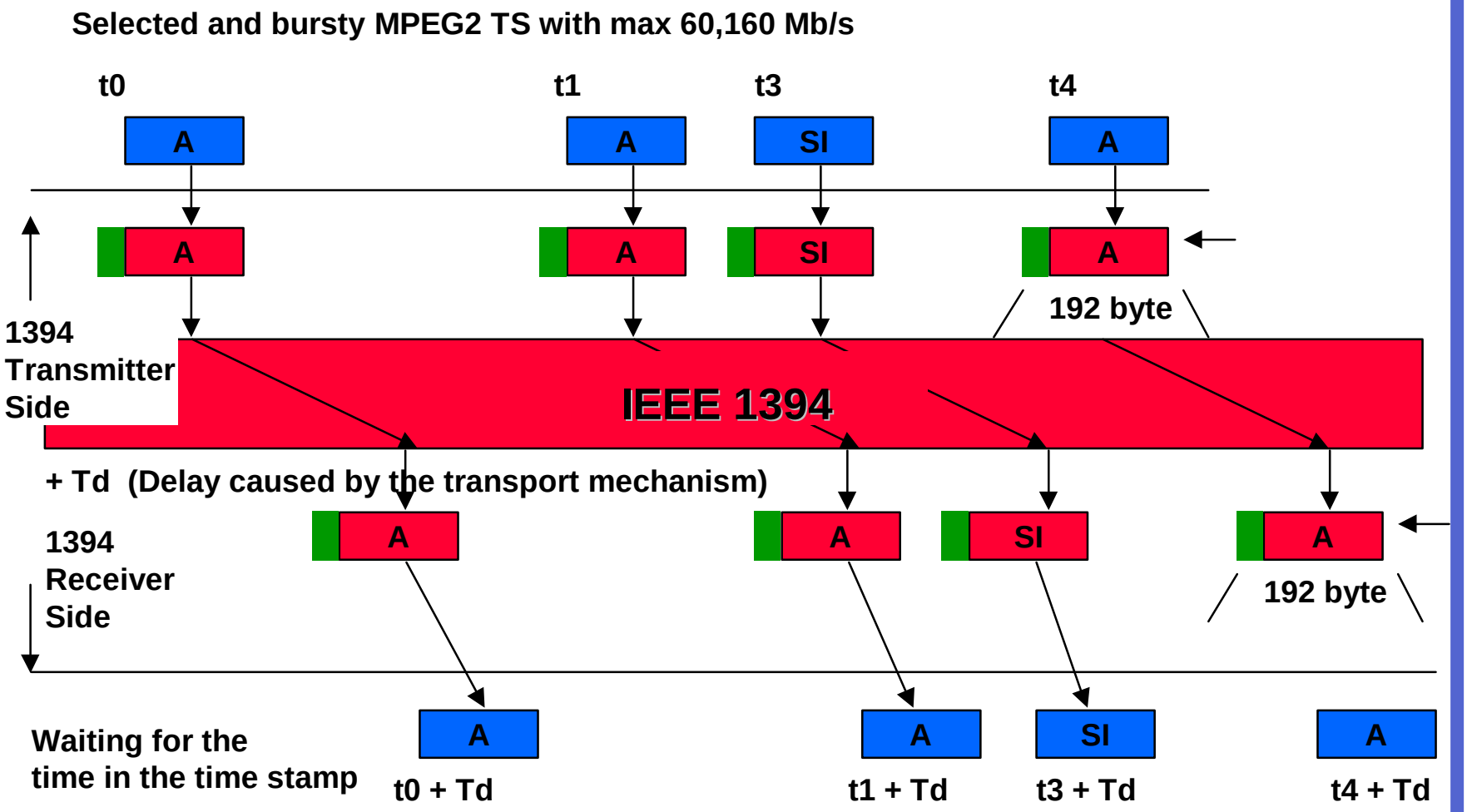
Work on a digital data interface is being performed by the EIA's R-4.1 subcommittee on ATV Receiver Interfaces. R-4.1 intends to define a baseband serial digital interface so that devices may exchange packetized data, for example, when a digital VCR is connected to a digital television receiver.

It is recommended that manufacturers of digital television receivers wishing to include a digital data interface give consideration to the interface developed by R4.1. Currently, this interface is defined as IEEE 1394-1995.

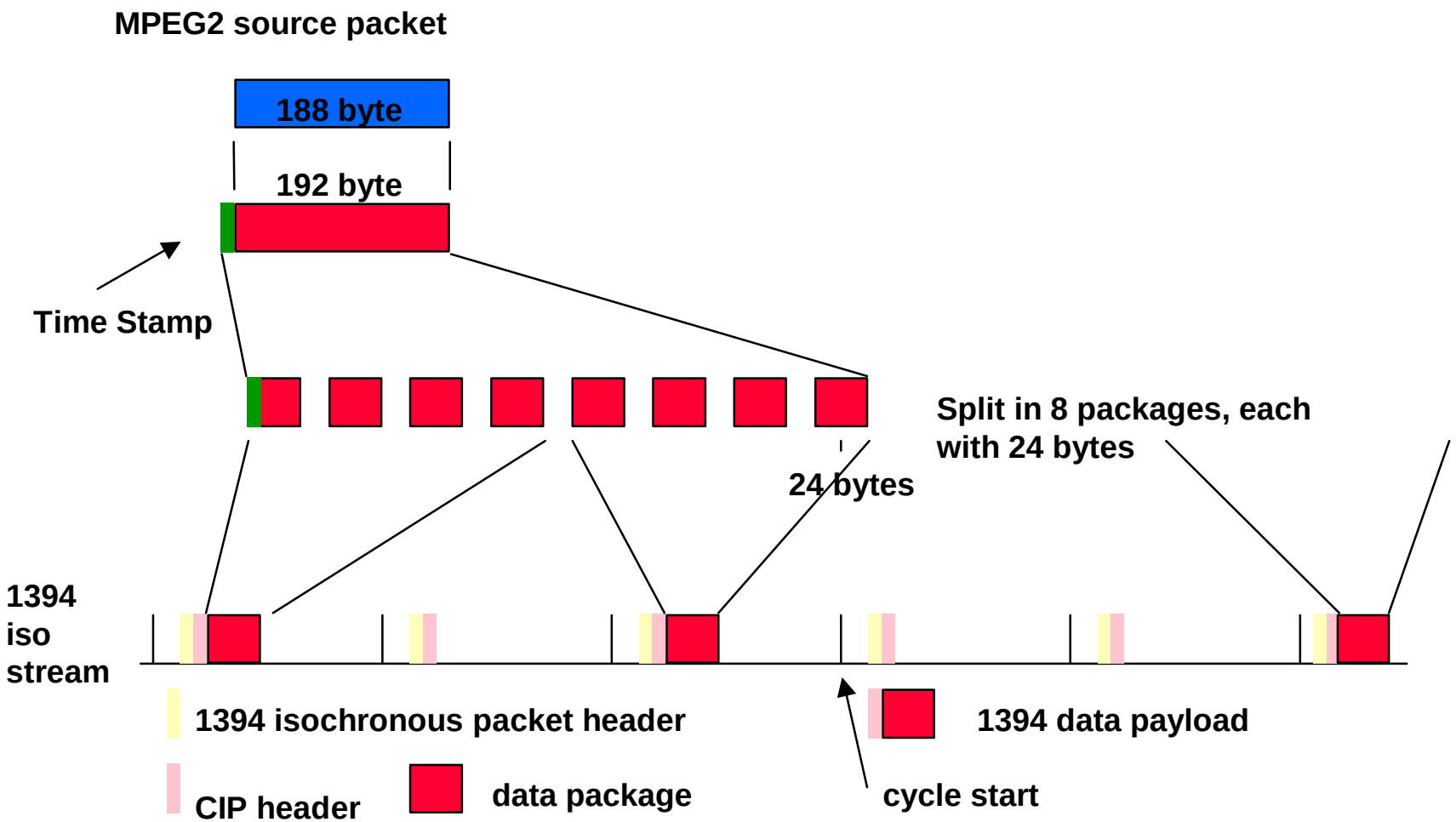
MPEG2 transport over IEEE-1394 serial bus



MPEG2 transport over IEEE-1394 serial bus (cont.)



MPEG2 transport over IEEE-1394 serial bus (cont.)



MPEG2 transport over IEEE-1394 serial bus - Notes

An MPEG2 transport stream (TS) consists of transport stream packets (TSPs) with a length of 188 bytes. The above diagram shows a TS which consists of several different programs. In most cases, only one program will be transmitted to the Digital TV or Digital recording device, which is what is shown above.

Because a smoothing buffer introduces transmitter jitter, the transport mechanism must compensate for this so that the packets arrive at the target destination with the correct time correlation to each other.

The source packet that is sent over the 1394 interface is 192 bytes long: TSP = 188 bytes, and the source packet header is 4 bytes.

The time stamp in the source packet header is used by isochronous data receivers for reconstructing the correct timing of the TSPs at the target side of the 1394 interface. The time stamp indicated the intended delivery time of the first bit/byte of the TSP from the receiver output to the transport stream target decoder.

The TSB12LV41 automatically inserts this timestamp when MPEG2 or DSS packets are transmitted. If on the receiving side, the TSB12LV41 inspects the timestamp and determines if the packet is on time or late, and discards the late packets.

Each source packet (192 bytes) is split into 8 data blocks (24 bytes). Zero or more data blocks can be transmitted on any one isochronous cycle.

The isochronous packet header contains information about the isochronous packet such as: Data length, Isochronous data format tag, isochronous channel number, transaction code (t-code), synchronization code (sy code), and header CRC. At the end of the data payload, the data CRC is inserted.

The Common Isochronous Packet (CIP) header contains information about the MPEG2 TS such as: Source node ID (node ID of transmitter), Data block size in quadlets, Fraction number (number of data blocks into which the source packet is divided), Quadlet padding count (the number of dummy quadlets padded to a source packet to equalize the size of the divided data blocks), Source packet header (indicates if the timestamp is attached to this packet), data block counter (number to be counted as the packets are received), Format ID (identifies DVCR, MPEG, etc. data types), and SYT (contains information about the timestamp).

The TSB12LV41 automatically does the CIP header and Isochronous header insertion. The information is provided to the TSB12LV41 from the MicroController or microprocessor presenting the data to MPEG2Lynx.

TSB12LV41 - MPEG2Lynx

- **Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus**
- **Interoperable with FireWire™ Implementation of IEEE 1394-1995**
- **Interfaces Directly to Texas Instruments TSB11C03, TSB11LV01 & TSB21LV03 Physical Layer Devices (100/100/200Mbps)**
- **Interfaces Directly to Texas Instruments TMS320AV7100/7110/7200 Series DSS & MPEG2 Decoders**
- **Programmable 8/16 bit MicroController/MicroProcessor interface supports many processors including 68000 and 80xx architectures**
- **Interrupt driven to minimize host polling**
- **Supports Bi-directional Isochronous Data transfer according to IEC1883 specification**
- **8K x 8bit FIFO supports MPEG2/DSS, Asynchronous, & Isochronous modes for Transmit and Receive**
- **64 Quadlet (256 byte) Control FIFO accessed through MicroController Interface supports Command/Status operations**
- **Hardware Endianess Byte Swapping controlled by Software**
- **Supports Bus Functions and Automatic IEEE-1394 Self-ID Verification**
- **Single 3.3V Supply Operation with 5V Tolerance using 5V bias pins**
- **High Performance 100-pin PZ (S-PQFP-G100) Package**

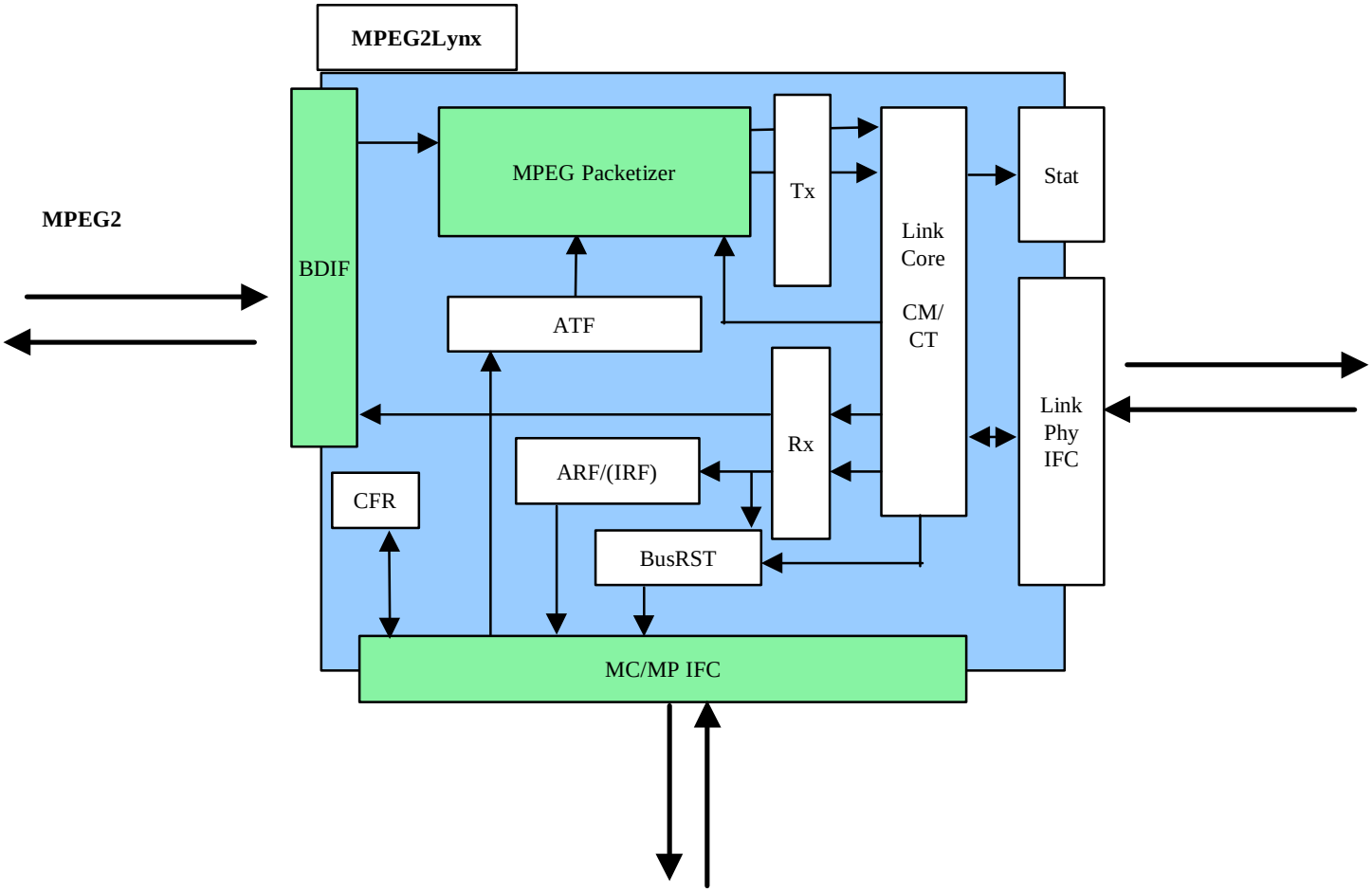
TSB12LV41 - MPEG2Lynx (Notes)

•The TSB12LV41 link layer controller complies with the IEEE 1394-1995 specification for high performance serial bus, transmits and receives correctly formatted 1394 packets, detects lost cycle-start packets, and generates and inspects the 32-bit cyclic redundancy check (CRC). The TSB12LV41 is also capable of performing the functions of Cycle Master (CM), Isochronous Resource Manager (IRM), and Bus Manager (BM).

•The TSB12LV41 provides a 1394 interface for high performance audio, video, and data applications at up to 200 Mbps, suitable for set-top boxes, multimedia tape and disk drives, and other consumer electronic devices requiring MPEG-2 formatted isochronous data transfer according to the IEC61883 specification.

•The TSB12LV41 interfaces directly to most microprocessors and microcontrollers, including the TMS320AV7000 family of DSP solutions from Texas Instruments. The Bulky Data InterFace (BDIF) enables MPEG-2, DSS, isochronous, or asynchronous data transfer in bitwide, bytewide and memory mapped modes. A 256 byte control FIFO allows asynchronous transmit and receive control packets while an 8K byte BDIF FIFO provides independent logical FIFOs for MPEG-2/DSS, isochronous, and asynchronous data transmit and receive. The TSB12LV41 supports full width timestamp offsets for MPEG-2 and DSS transmit and receive, and also performs age filtering functions.

MPEG2Lynx - TSB12LV41



MPEG2Lynx - TSB12LV41 (Notes)

•BDIF - The “Bulky Data InterFace” is a high speed data interface for isochronous data transfer to/from hardware for coding/decoding of real-time data

•6-Queue FIFO - This FIFO can be logically partitioned into MPEG2/DSS transmit, MPEG2/DSS receive, Asynchronous transmit, Asynchronous receive, Isochronous transmit and Isochronous receive FIFO’s. Sizing of these FIFO’s can be done to optimize data flow.

•MPEG2/DSS/A/I Packetizer - Packets can be parsed automatically according to IEC1883 rules. Asynchronous packets can be steered into either the Control FIFO or the BDIF FIFO

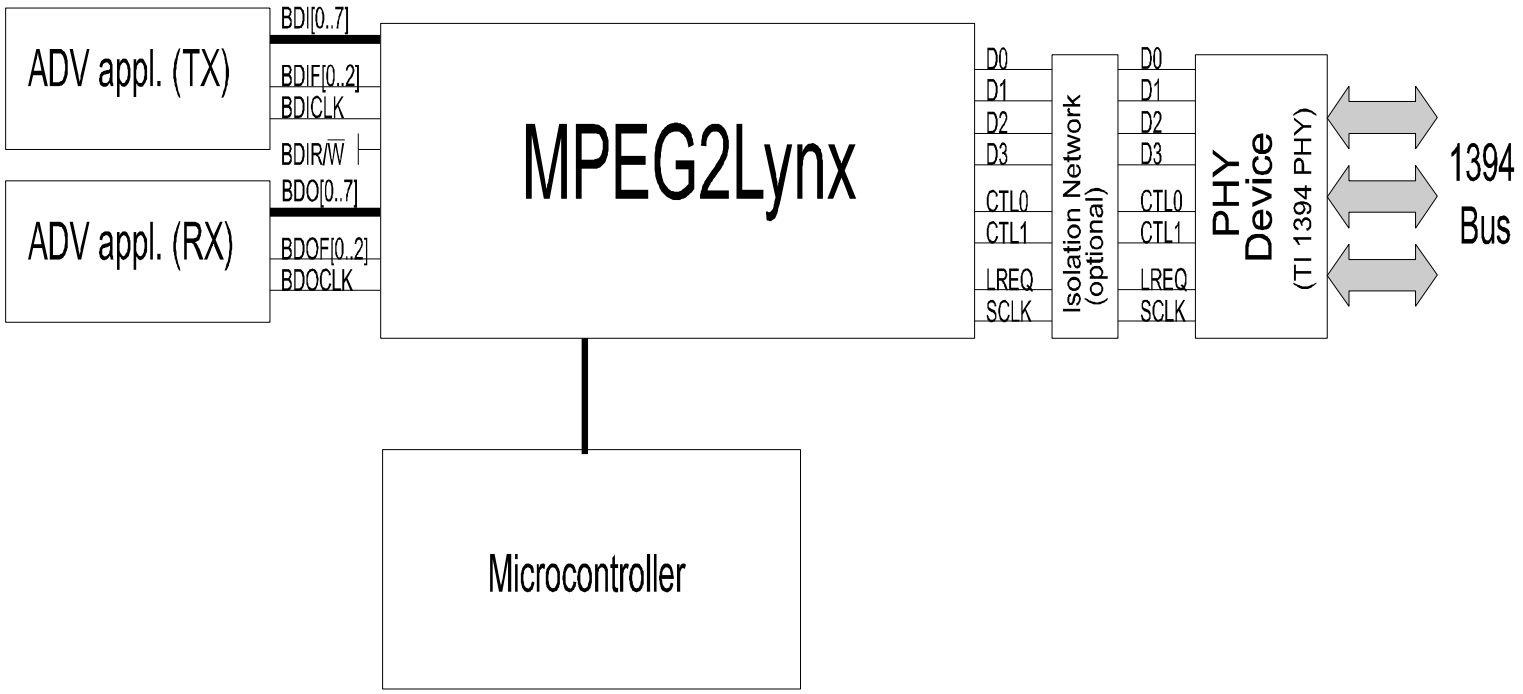
•TX/RX Aging - The TSB12LV41 automatically determines if a received packet is aged, and attaches a forward-looking time-stamp to MPEG2 packets to be transmitted.

•BusRST - performs a bus reset

•MC/MP Interface controller - This MicroController/Microprocessor interface controller is software programmable to support the TMS320AV7000 architecture, Motorola 68000 family, and Intel 8051.

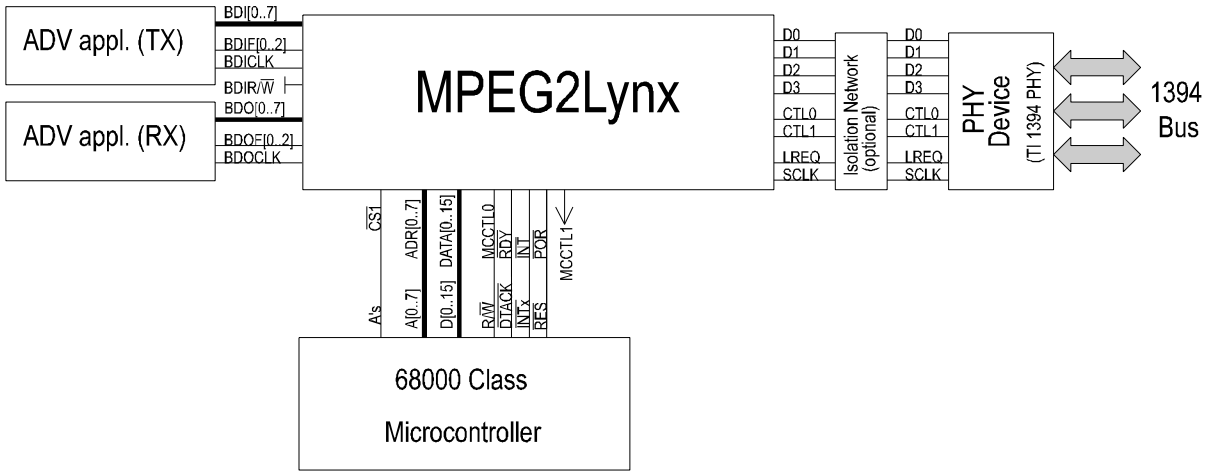
The link core presents and accepts the data to/from the phy/link interface according to the 1394-1995 standard.

MPEG2Lynx System Block Diagram

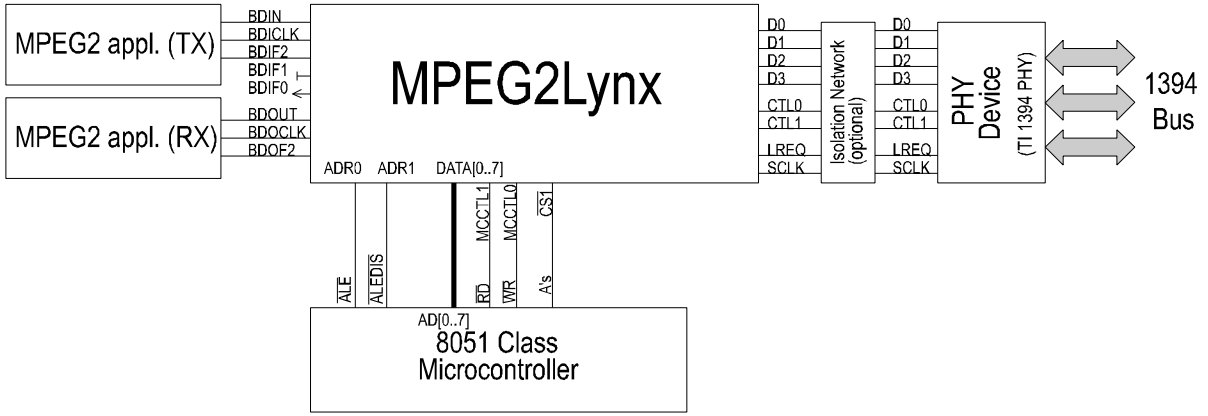


MPEG2Lynx System Block Diagrams (cont.)

MPEG2Lynx interface to 68XXX

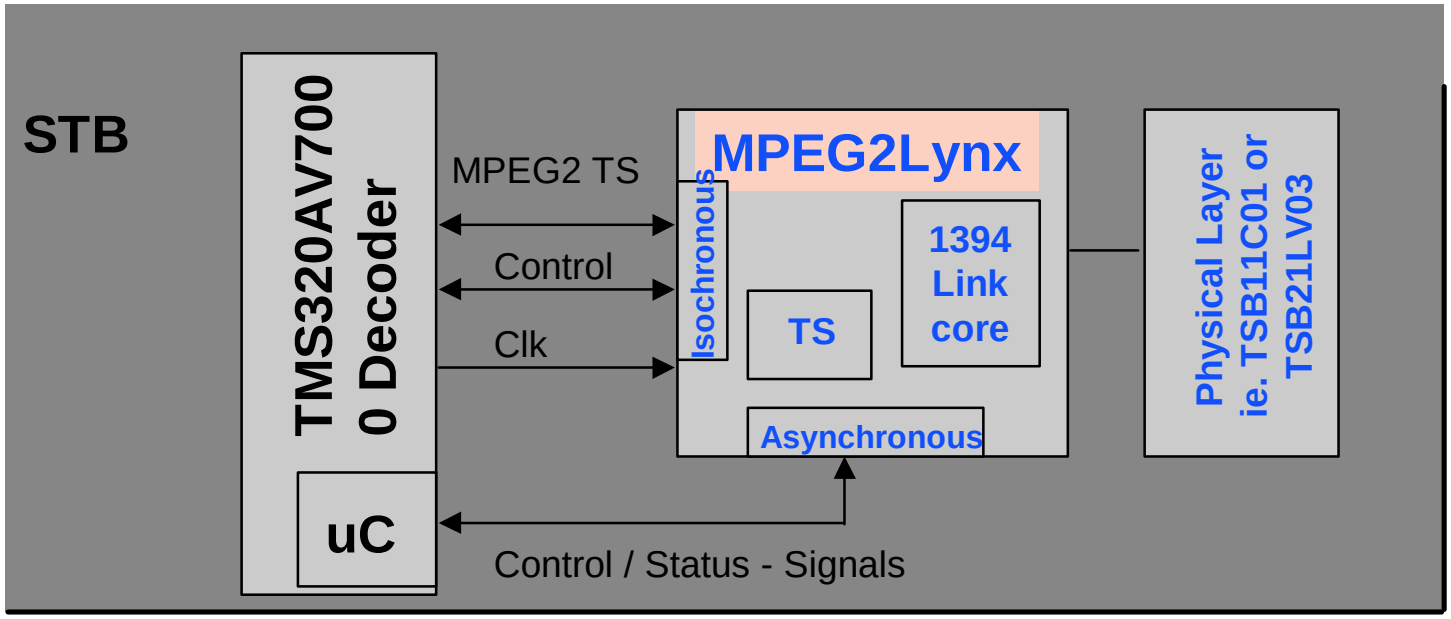


MPEG2Lynx interface to 8051



MPEG2Lynx System Block Diagrams (cont.)

MPEG2Lynx interface to TMS320AV7000 Architecture



MPEG2Lynx System Block Diagrams - Notes

The TSB12LV41 is intended for high speed audio, video, and data applications at up to 200 Mbps. The TSB12LV41 communicates with other devices that perform decompression algorithms or transaction layer functions through either the Bulky Data Interface (BDIF) or MicroController/Microprocessor (MC/MP) interface. The bulky data interface has been implemented to support long term datarates up to 60 Mbps, however burst datarates can go up to 80 Mbps in bit serial mode and 160 Mbps in byte parallel mode.

The Bulky data Interface consists of two eight-bit ports, Bulky Data In (BDI[0:7]) and Bulky Data Out (BDO[0:7]), a Bulky Data Input Clock pin (BDICLK), a Bulky Data Output Clock pin (BDOCLK), and a Bulky Data Read/Write pin (BDIR/W). The BDI can be configured as a parallel input/output data source for MPEG2Lynx, hence the need for the BDIR/W pin. Bulky data is usually buffered in the BDIF FIFO, which supports MPEG2/DSS, Asynchronous and Isochronous data. MPEG2/DSS data can be written to the BDIF in any manner (burst access, bursty access, serial, parallel).

MPEG2Lynx System Block Diagrams - Notes

The Micro Interface is programmable to behave in three distinct modes: TMS320AV7000 Architecture, Motorola 68000 Architecture, and Intel 8051 Architecture.

•MPEG2Lynx interface to 68XXX

This figure shows the TSB12LV41 set up with the 68000 class MicroController. This application could support audio, video, and data in bytewide mode with independent Transmit and Receive paths.

•MPEG2Lynx interface to 8051

This figure shows the TSB12LV41 set up with the 8051 class MicroController. This application could only support video when connected in bitserial mode with independent Transmit and Receive paths.

A special 'Blind Access' mode is incorporated into the TSB12LV41 to compensate for slow microprocessors such as the 8051 that don't have an external wait/ready handshake signal.

MPEG2Lynx interface to TMS320AV7000

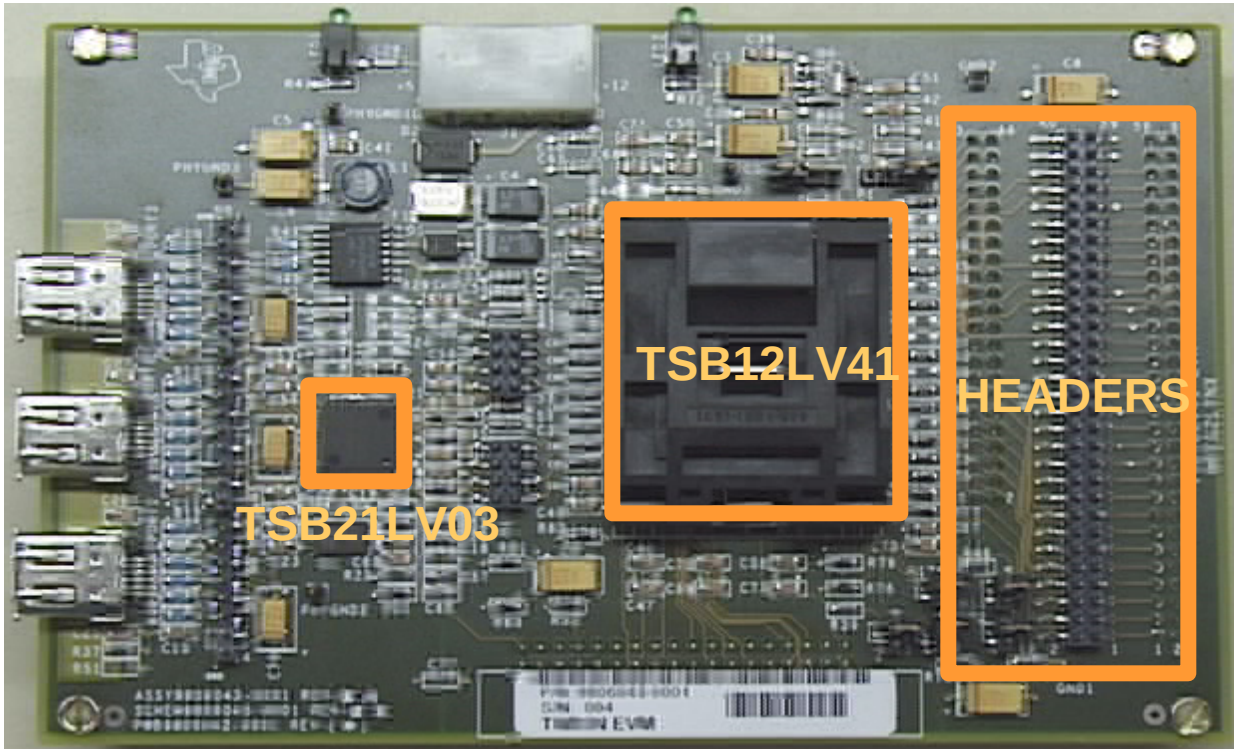
The interface to the micro is synchronous with the 'AV7000 extension bus external clock. The other modes operate asynchronously.

Control data can be transmitted over the MC/MP interface while high bandwidth audio/video/data is transmitted of the BDIF.

For detailed information on the AV7000 products and their development boards, please contact Syed Haider @ 972-480-6409

MPEG2Lynx Evaluation Board

- BDIF Header enables connection to MPEG2 decoder board, including TMS320AV7000 DB
- uC/uP Header enables connection to various controllers, including 68xxx, 80xx, and ‘AV7000



MPEG2Lynx Evaluation Board (Notes)

Overview of the TSBKMPEG2 Evaluation Module

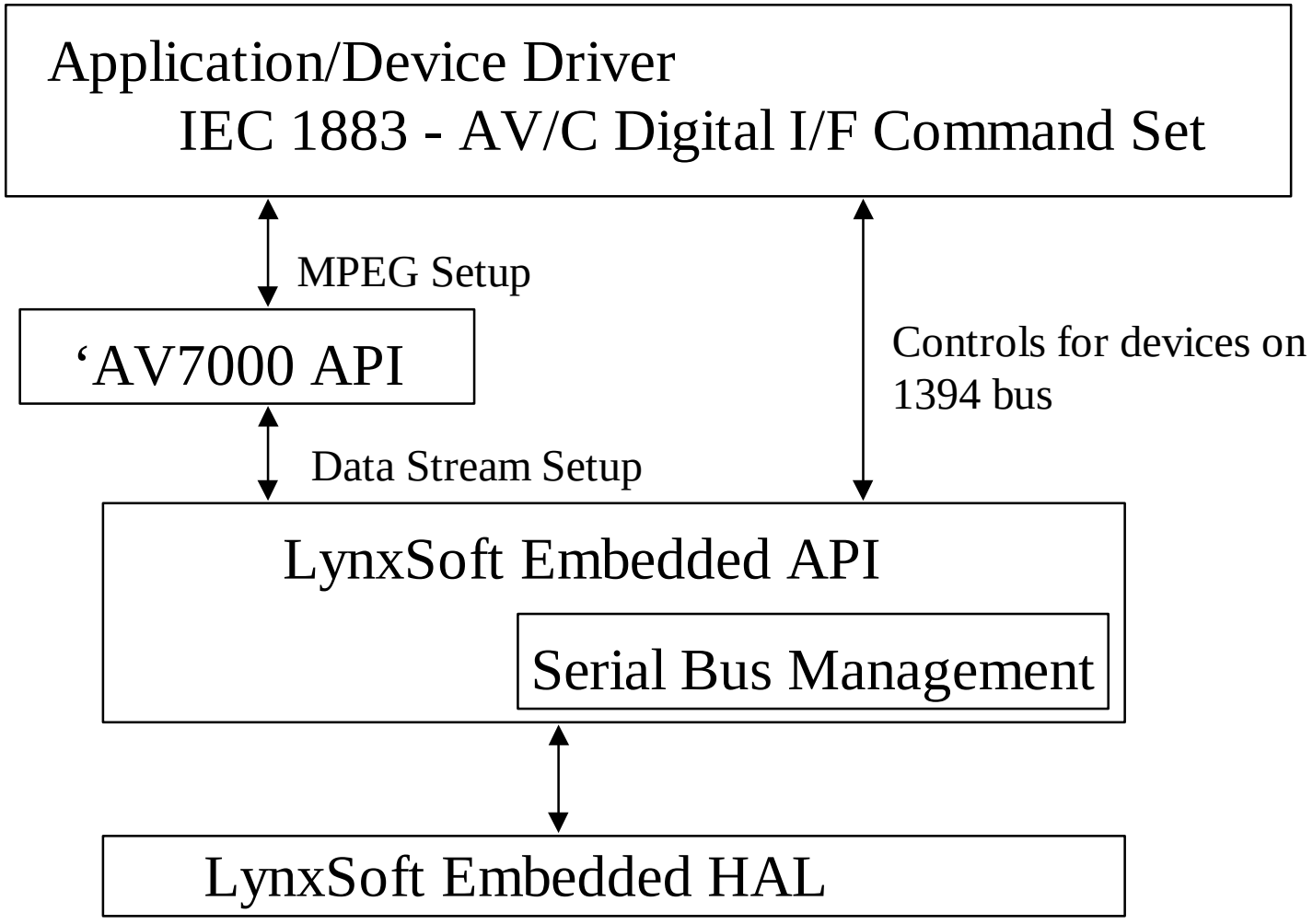
The MPEG2Lynx Development Board uses TI's TSB12LV41 (MPEG2Lynx) link layer controller and TSB21LV03 (dual footprinted for TSB11C03) to create a known good node for consumer electronics product development. The TSB12LV41 enables direct connection to various microprocessors or microcontrollers, including the 80xx, 68xxx, and TMS320AV7000 architecture of set-top box devices from TI. The TSB12LV41 supports MPEG2 formatted isochronous data transfer according to IEC61883, supports timestamp offsets for MPEG2 Transmit and Receive, and performs age filtering functions.

The TSB12LV41 is able to communicate to the Microcontoller/Microprocessor and MPEG2 decoder through two separate headers on the board. One header provides the 8/16 data lines and 8 address lines for the uC/uP, and the other header provides the address, data and control lines for the MPEG2 decoder.

Hardware Abstraction Layer (HAL) software, written in ANSI C, is available for transaction layer functionality. An Application Programmer Interface is available for serial bus management functions. The API performs the necessary functions required to do 1394 operations of isochronous and asynchronous nature.

The TSBKMPEG2 EVM is designed to connect to a TMS320AV7100 Development Board via a special connector (included). The TSBKMPEG2 may also be used with other microcontrollers/microprocessors if a connector is built for this purpose.

Software Hierarchy



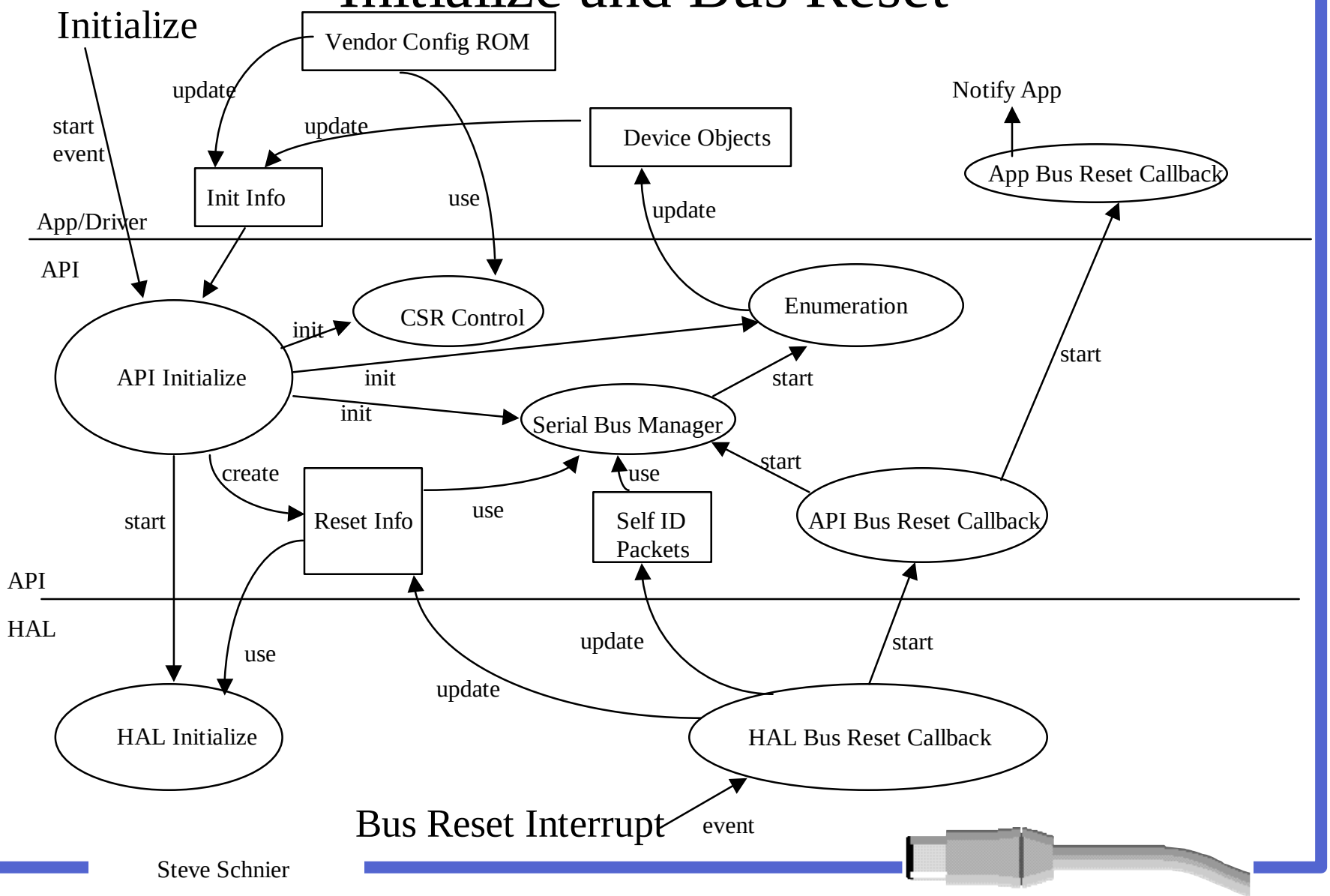
Software Hierarchy - Notes

The LynxSoft software for embedded systems consists of the LynxSoft Embedded Hardware Abstraction Layer (HAL) and the LynxSoft Embedded Application Programmer Interface (API)

The HAL is provided to isolate the programmer from the logical commands that need to be performed by the transaction layer.

The API is provided to give the programmer functions with which he can assemble the data and present it to the HAL in the correct format.

Initialize and Bus Reset



Initialize and Bus Reset - Notes

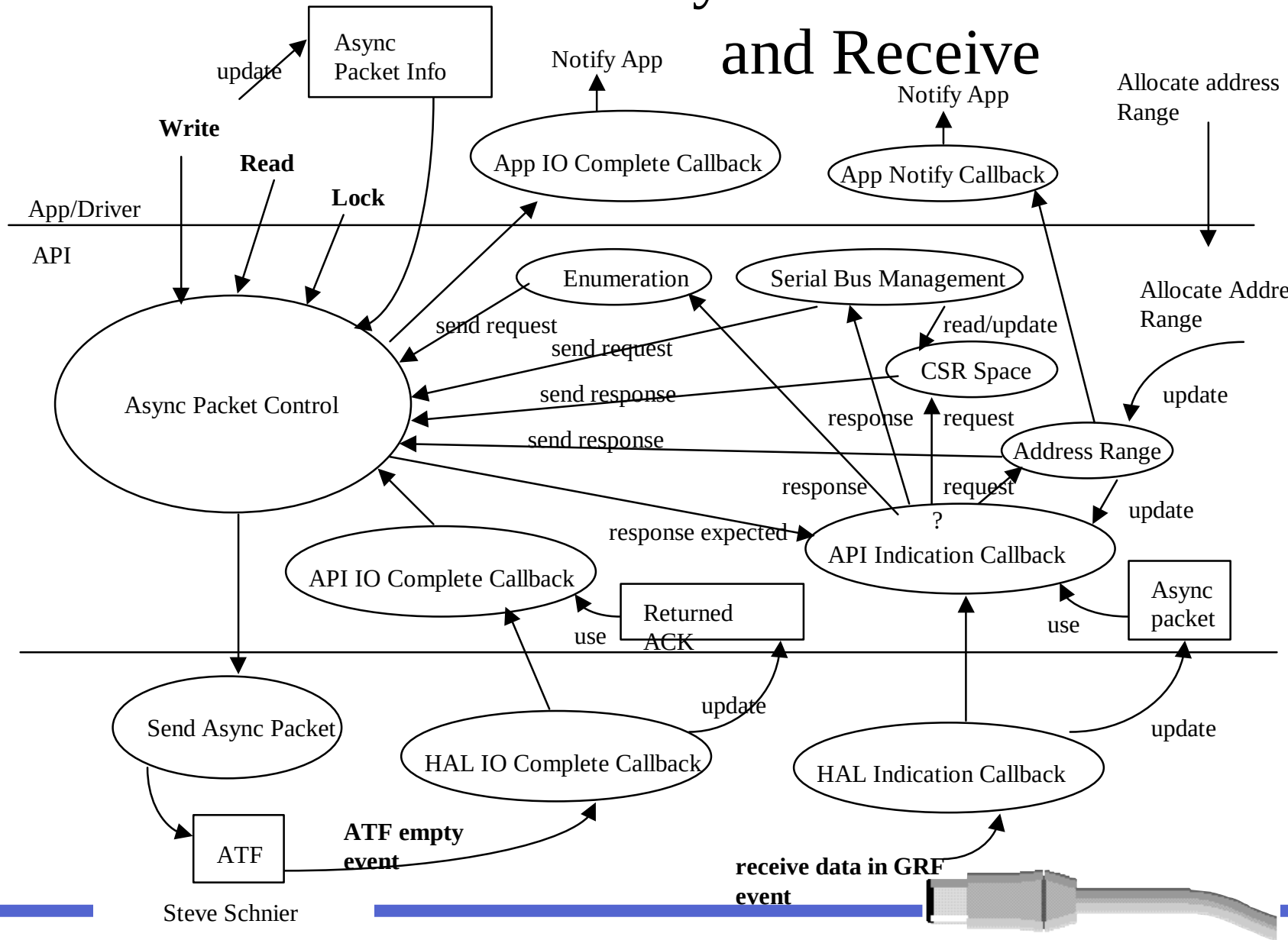
This complex foil boils down to two things:

A bus reset can be initiated by the 1394 bus (ie, a device has been added or removed)

A bus reset can be initiated by the device connected to the bus (ie, it is trying to gain bus master, iso resource manager, etc.)

The flow details the operations that are carried out by the HAL and API, and what needs to be provided by/to the Application layer for the bus reset to be complete.

Asynchronous Send and Receive



Asynchronous Send and Receive - Notes

This complicated foil shows the basic flow of sending or receiving asynchronous data.

Sending/Receiving Async data

To send data asynchronously, the Application (driver) commands the API to perform a Read (get data from another device on the bus), a Write (send data to another device on the bus), or a Lock (assures that the data in memory at the target device will not change if there is a split transaction). The API then directs the assembly of the data to be loaded into the Asynchronous Transmit FIFO (ATF) by the HAL.

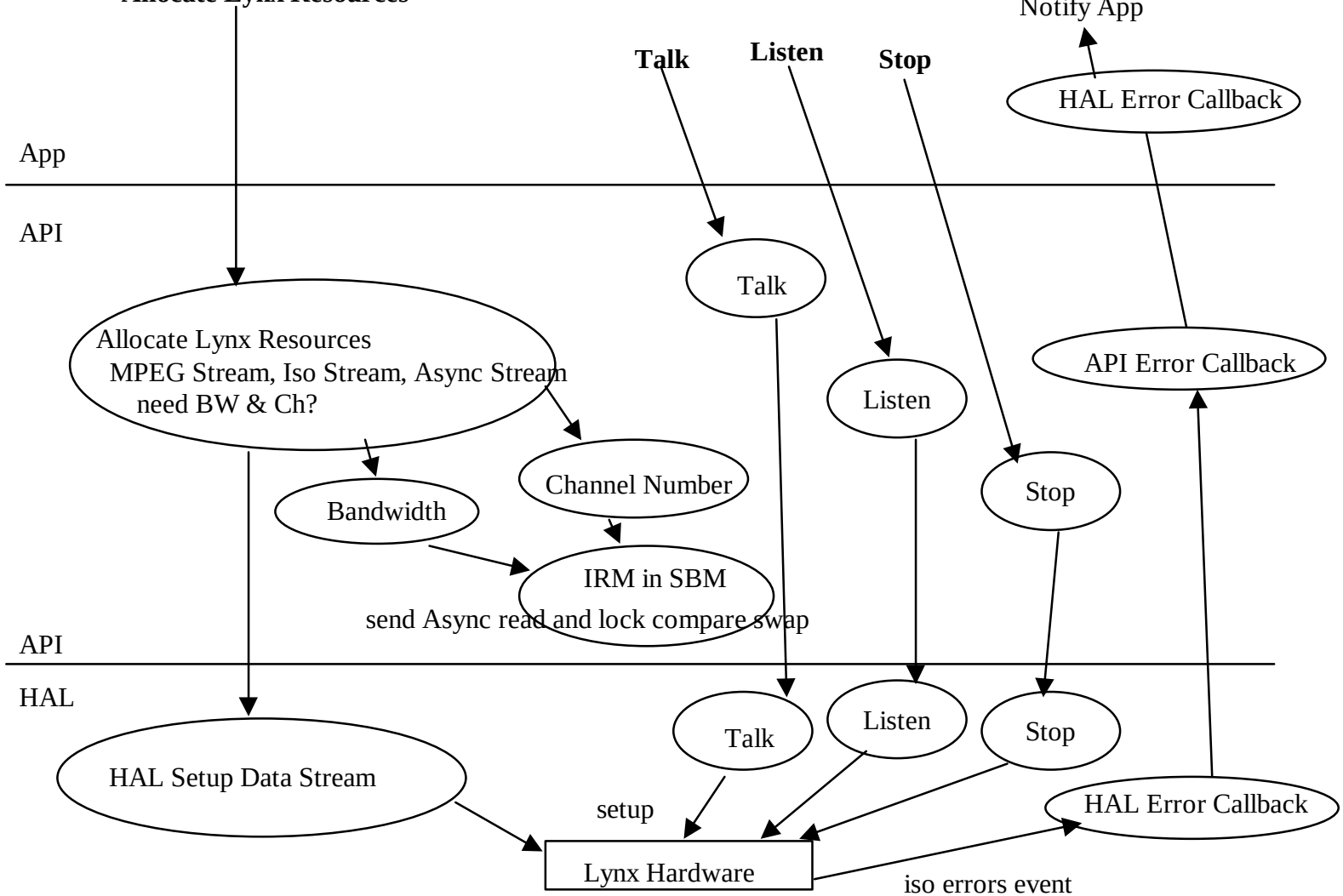
When another device on the bus wishes to send/receive data, the HAL removes the data from the General Receive FIFO (GRF), where the API readies the data for presentation to the Application.

This data is usually passed through the control FIFO in the TSB12LV41.

The LynxSoft API requires the application software to provide a memory buffer to handle asynchronous traffic. This function associates this memory buffer with the caller provided 1394 address range and then allows other devices on the bus to read or write into this 1394 address range as specified by the caller.

CSR architecture registers, Serial Bus registers and Serial Bus-Dependent registers in the Initial Unit Space will be provided by the LynxSoft API and will allow external devices access to these registers as described in the 1394 Spec. The Config ROM content will be provided by the caller and this function will allow external devices to only read this space.

Data Stream Control



Data Stream Control - Notes

Control of the various types of data streams accepted and processed by the TSB12LV41 can be performed by the HAL and API. The HAL sets up the TSB12LV41 to send/receive MPEG2/DSS, Isochronous, or Asynchronous data through a combination of the BDIF and MC/MP interfaces. The API and HAL also give the Application access to commands such as Talk, Listen, and Stop.

The basic flow to set up, perform, and conclude isochronous communication is as follows:

- Initialize LynxSoft API software and Lynx hardware.
- Setup the Lynx device to send/receive the expected data stream.
- Begin the receive operation.
- Begin the transmit operation.
- Halt/Pause the transfer.
- Free the allocated Lynx resource.
- Shut down the 1394 interface if no more 1394 operations are intended.

HAL Functions

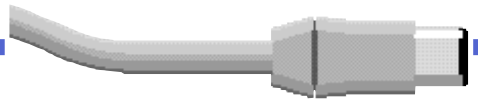
• **LynxHALInit**	initialize the HAL sub-system
• **LynxHALTerminate**	Disable callbacks, disconnect interrupts
• **LynxHALSendAsyncPacket**	Send Async transaction packet
• **LynxHALSendPhyPacket**	Send PHY packet
• **LynxHALSaveAsyncPacket**	Remove and save Async packet in GRF
• **LynxHALBusyOff**	Used to throttle incoming Async packets
• **LynxHALStartCycleMaster**	Used if node is to be Cycle Master
• **LynxHALTalk**	Start Transmit data stream
• **LynxHALListen**	Start Receive data stream
• **LynxHALStop**	Stop Transmit or Receive data stream
• **LynxHALPresentVersion**	Returns SW and HW version
• **LynxHALPresentGapCount**	Returns Gap Count
• **LynxHALCauseBusReset**	Generates a bus reset
• **LynxHALGetThisNodesID**	Returns this node's Self ID packet
• **LynxHALGetCycleTime**	Returns Cycle Timer register.
• **LynxHALGetBusID**	Returns Bus ID
• **LynxHALSetBusID**	Set Bus ID
• **LynxHALNodeISR**	Interrupt handler

Used for MPEG2Lynx:

• **LynxHALAllocateLynxResources**	Setup bulky data streams M/D, I, A

TI 1394 Physical Layer Devices

	PORTS	VOLTAGE (V)	DATA RATE (Mbps)	PACKAGE	FEATURE
TSB11C01	3	5	100	56-pin SSOP	
TSB11LV01	1	3.3	100	48-pin SQFP	5V tolerant
TSB21LV03	3	3.3	200	64-pin SQFP	5 V tolerant
TSB14C01	1	5.0	50 or 100	64-pin SQFP	Backplane Phy



TI 1394 Physical Layer Devices - Notes

Released:

Phy's are differentiated by speed, ports, and power.

*TSB11C01 - first phy, 100Mbps, 3-port, 5V - will be TTL compatible for operation with MPEG2Lynx

*TSB11LV01 - 100Mbps, 1-port, 3.3V

*TSB21LV03 - 200Mbps, 3-port, 3.3V

*TSB14C01 - 100Mbps, 1-port, 5V phy for backplane applications. Requires separate transceiver for specific backplane technology (TTL, BTL, etc.)

In development:

*The other phy developments will conform to future upgrades in the standard. We are active in all the development meetings, and are pursuing these upgrades. However, we are NOT pursuing the non-backward compatible (serial express) technology.