- **Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus†**
- **Fully Interoperable With FireWire™ Implementation of IEEE 1394-1995**
- **Provides A Single Fully-Compliant Cable Port at 100 Megabits per Second (Mbits/s)**
- **Cable Port Monitors Line Conditions for Active Connection to a Remote Node**
- **Inactive Port Disabled to Save Power**
- **Cable Inactivity Monitor Output and Power-down Input Provided for Additional Sleep-Mode Power Savings**
- **Internal Bandgap Reference Provided for Setting Stable Operating Bias Conditions**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Data Interface to Link Layer Controller (Link) Provided Through Two Parallel Signal Lines at 50 Mbits/s**
- **25-MHz Crystal Oscillator and PLL Provide Transmit, Receive Data, and Link Layer Controller Clocks at 50 MHz**
- **Digital I/Os are 5 V tolerant**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Cable Bias and Driver Termination Voltage Supply**
- **Single 3-V Supply Operation**
- **Separate Multiple Package Terminals Provided for Analog and Digital Supplies and Grounds**
- **High Performance 48-Pin TQFP (PT) Package**

description

The TSB11LV01 provides the analog transceiver functions needed to implement a single port node in a cable based IEEE 1394-1995 network. The cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB11LV01 is designed to interface with a link layer controller, such as the TSB12C01A.

The TSB11LV01 requires an external 24.576-MHz crystal, which drives an internal phase-locked loop (PLL) generating the required 98.304-MHz reference signal. The 98.304-MHz reference signal is internally divided to provide the 49.152-MHz ±100 ppm system clock signals that control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link for synchronization of the two chips and is used for resynchronization of the received data. The power-down function, when enabled by asserting the PWRDN terminal high, stops operation of the PLL.

Data bits to be transmitted are received from the link on two parallel paths and are latched internally in the TSB11LV01 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304-Mbits/s as the outbound data-strobe information stream. During transmit, the encoded data information is transmitted differentially on the TPB cable pair, and the encoded strobe information is transmitted differentially on the TPA cable pair.

NOTE

In this document, phy is the physical layer and link is the link layer controller.

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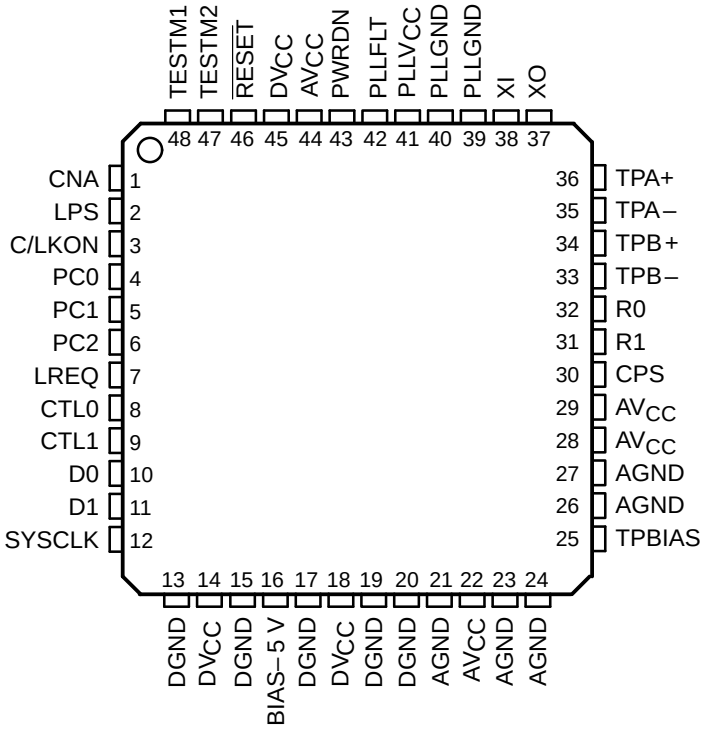
† Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thomson, Limited.
FireWire is a trademark of Apple Computer, Incorporated.

PT PACKAGE
(TOP VIEW)



description (continued)

During packet reception the TPA and TPB transmitters of the cable port are disabled, and the receivers of the port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two parallel streams, resynchronized to the local system clock and sent to the associated link.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this bias voltage is an indication of cable connection status. The cable connection status signal is internally debounced in the TSB11LV01. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect, the debounce delay is 335 ms. On a connect-to-disconnect there is minimal debounce.

The TSB11LV01 provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The value of this bias voltage has been chosen to allow interoperation between transceiver chips operating from either 5-V nominal supplies or 3-V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of at least 1 μF.

The transmitter circuitry is disabled under the following conditions: powerdown, cable not active, reset, or transmitter disable. The receiver circuitry is disabled during powerdown, cable not active, or receiver disable. The twisted-pair bias voltage circuitry is disabled during the powerdown or reset conditions. The power-down condition occurs when the PWRDN input is asserted high. The cable-not-active condition occurs

description (continued)

when the cable connection status indicates no cable is connected and is not debounced. The device reset condition occurs when the $\overline{\text{RESET}}$ input terminal is asserted low. The transmitter disable and receiver disable conditions are determined from the internal logic.

The line drivers in the TSB11LV01 operate in the high-impedance current mode and are designed to work with external 112-Ω line matching resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that are directly connected to the twisted-pair A-package terminals is connected to the TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B-package terminals is coupled to ground through a parallel resistance-capacitance (R-C) network with the recommended value of 5 kΩ and 250 pF. The values of the external resistors are designed to meet the IEEE 1394-1995 standard specifications when connected in parallel with the internal receiver circuits (see Figure 3).

An internal reference circuit (bandgap) provides stable bias voltages for the TSB11LV01 transceiver circuits. The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between terminals R1 and R0, and has a value of 6 kΩ ±0.5%.

Two of the package terminals set up various test conditions used in manufacturing. These terminals, TESTM1 and TESTM2, should be connected to V_{CC} for normal operation.

Four package terminals are inputs to set four configuration status bits in the self-identification (Self-ID) packet. These terminals are hardwired high or low as a function of the equipment design. PC0, PC1, and PC2 (corresponds to bits 21, 22, and 23 of the Self-ID packet) are three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal, C/LKON (corresponds to bit 20 of the Self-ID packet), indicates if a node is a contender for bus manager. C/LKON may also output a 6.114-MHz ±100 ppm signal, indicating reception of a link-on packet. See Table 4-29 of the IEEE 1394-1995 standard for additional details.

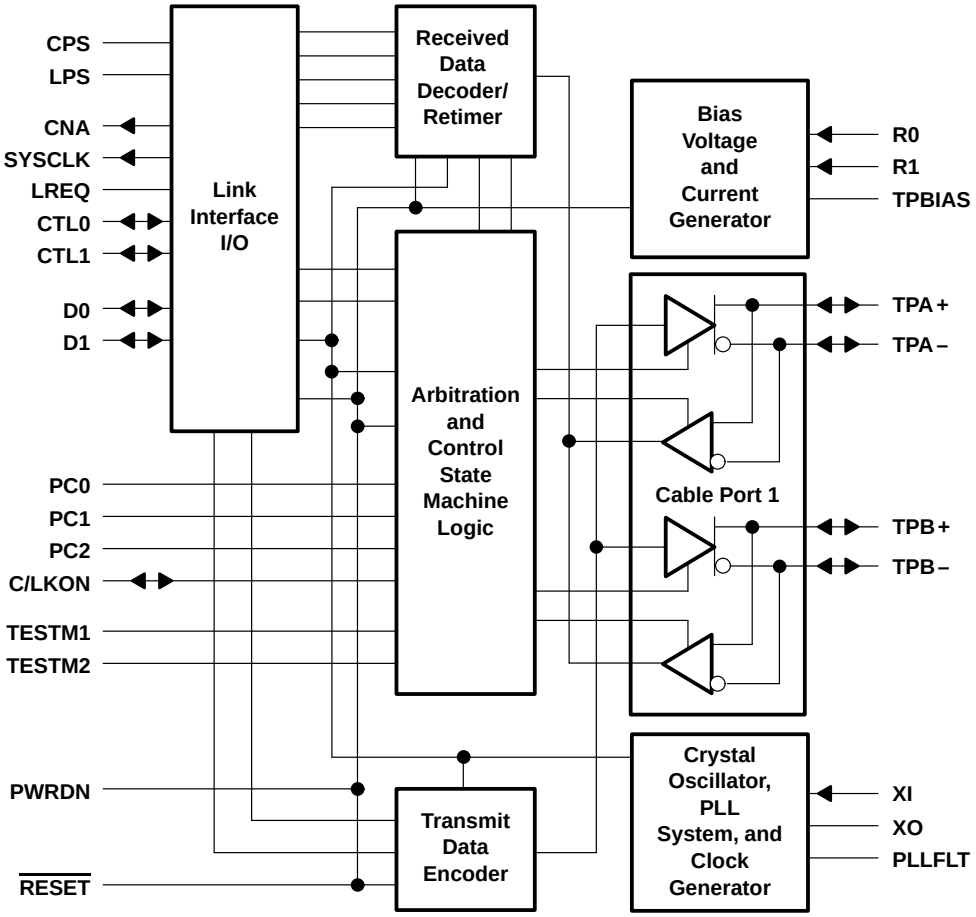
In order to operate with power supplies as low as 2.7 V, this device is restricted to applications that do not provide cable power. See Note A in clause 4.2.2.2 of the IEEE 1394-1995 standard.

When the TSB11LV01 is used in applications with a 5-V link layer controller, such as the TSB12C01A, the BIAS–5V terminal should be connected to the link layer controller 5-V supply. Otherwise, connect this terminal to DV_{CC}.

A power-down terminal (PWRDN) is provided to allow most of the TSB11LV01 circuits to be powered down to conserve energy in battery-driven applications. A cable status terminal (CNA) provides a high output when the twisted-pair cable port is disconnected. This output is not debounced. The CNA output can determine when to power the device down. In the power-down mode all circuitry is disabled except the CNA detection circuitry.

If the power supply of the TSB11LV01 is removed while the twisted-pair cables are connected, the TSB11LV01 transmitter and receiver circuitry has been designed to present a high-impedance signal to the cable and not load the TPBIAS voltage on the other end of the cable.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	TYPE	DESCRIPTION
AGND	21, 23, 24, 26, 27	–	Supply	Analog circuit ground. The AGND terminals should be tied to the low-impedance circuit board ground plane.
AV_{CC}	22, 28, 29, 44	–	Supply	Analog circuit power. AV_{CC} supplies power to the analog portion of the device. It is recommended that a combination of high-frequency decoupling capacitors be connected to AV_{CC} (i.e., paralleled 0.1 μF and 0.001 μF). Lower frequency 10-μF filtering capacitors can also be used. These supply pins are separated internally in the device to provide noise isolation. These terminals should also be tied at a low-impedance point on the circuit board. Individual filtering networks for each is desired.
C/LKON	3	I/O	CMOS	Bus manager capable (input). When set as an input, C/LKON is used to specify in the Self-ID packet that the node is bus manager capable.
				Link-on (output). When set as an output, C/LKON indicates the reception of a link-on message by asserting a 6.114-MHz signal. The bit value programming is done by tying the terminal through a 10-kΩ resistor to V_{CC} (high) or to GND (low). Using either the pullup or pulldown resistor allows the LKON output to override the input value when necessary.
CNA	1	O	CMOS	Cable not active. CNA is asserted high when the TSB11LV01 port is not connected to another active port.
CPS	30	I	CMOS	Cable power status. CPS is normally connected to the cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This information is maintained in two internal registers and is available to the link by way of a register read. See the Phy-Link Interface Application Note in the IEEE 1394-1995 standard.
CTL0, CTL1	8, 9	I/O	CMOS	Control I/O. The CTL terminals are bidirectional communications control signals between the TSB11LV01 and the link. These signals control the passage of information between the two devices.
D0, D1	10, 11	I/O	CMOS	Data I/O. The D terminals are bidirectional and pass data between the TSB11LV01 and the link.
DGND	13, 15, 17, 19, 20,	–	Supply	Digital circuit ground. The DGND terminals should be tied to the low-impedance circuit board ground plane.
DV_{CC}	14, 18, 45	–	Supply	Digital circuit power. DV_{CC} supplies power to the digital portion of the device. It is recommended that a combination of high-frequency decoupling capacitors be connected to DV_{CC} (i.e., paralleled 0.1 μF and 0.001 μF). Lower frequency 10-μF filtering capacitors can also be used. These supply pins are separated internally in the device to provide noise isolation. These terminals should also be tied at a low-impedance point on the circuit board. Individual filtering networks for each is desired.
BIAS–5V	16	–	Supply	5 V bias. BIAS-5V should be connected to the link V_{CC} supply when a 5-V link is connected to the phy. When a 3-V link is used, BIAS-5V should be connected to the phy DV_{CC}.
LPS	2	I	CMOS	Link power status. This terminal is connected to either the V_{CC} supplying the link or to a pulsed output that is active when the link is powered for the purpose of monitoring the link's power status. When this input is low for more than 2.56 μs, then the link is considered powered down. When this input is high for more than 80 ns, then the link is considered powered up. If the link is not powered, the phy–link interface is disabled, and the TSB11LV01 performs only the basic repeater functions required for network initialization and operation.
LREQ	7	I	CMOS	Link request. LREQ is an input from the link that signals the TSB11LV01 of a request to perform some service.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	TYPE	DESCRIPTION
PC0, PC1, PC2	4, 5, 6	I	CMOS	Power class indicators. the PC signals set the bit values of the three power class bits in the Self-ID packet (bits 21, 22, and 23). These bits can be programmed by tying the terminals to V_{CC} (high) or to GND (low).
PLLFLT	42	I	CMOS	PLL filter. PLLFLT is connected to a 0.1-μF capacitor and then to AGND to complete the internal lag-lead filter. This filter is required for stable operation of the frequency multiplier PLL running off of the crystal oscillator.
PLLGND	39, 40	–	Supply	PLL circuit ground. The PLLGND terminals should be tied to the low-impedance circuit board ground plane.
$PLLV_{CC}$	41	–	Supply	PLL circuit power. $PLLV_{CC}$ supplies power to the PLL portion of the device. It is recommended that a combination of high-frequency decoupling capacitors be connected to $PLLV_{CC}$ (i.e., paralleled 0.1 μF and 0.001 μF). Lower frequency 10-μF filtering capacitors can also be used. These supply pins are separated internally in the device to provide noise isolation. These terminals should also be tied at a low impedance point on the circuit board. Individual filtering networks for each is desired.
PWRDN	43	I	CMOS	Powerdown. When asserted high, PWRDN turns off all internal circuitry except the CNA monitor circuits that drive the CNA terminal.
R1, R0	31, 32	–	Bias	Current setting resistor. An internal reference voltage is applied to a resistor connected between these two terminals to set the operating current and the cable driver output current. A low TCR 6 kΩ ±5% resistor should be used to meet the IEEE 1394-1995 standard requirements for output voltage limits.
$\overline{\text{RESET}}$	46	I	CMOS	Reset. When $\overline{\text{RESET}}$ is asserted low (active), a bus reset condition is set on the active cable ports and the the internal logic is reset to the reset start state. An internal pullup resistor, which is connected to V_{CC}, is provided so only an external delay capacitor is required. This input is a standard logic buffer and can also be driven by an open-drain logic output buffer.
SYSCLK	12	O	CMOS	System clock. SYSCLK provides a 49.152-MHz clock signal, which is synchronized with the data transfers, to the link.
TESTM1, TESTM2	48, 47	I	CMOS	Test mode control. TESTM1 and TESTM2 are used during manufacturing test and should be tied to V_{CC}.
TPA+	36	I/O	Cable	Port cable pair A. TPA is the port A connection to the twisted pair cable. Board traces from these terminal should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA–	35			
TPB+	34	I/O	Cable	Port cable pair B. TPB is the port B connection to the twisted pair cable. Board traces from these terminal should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB–	33			
TPBIAS	25	O	Cable	Twisted-pair bias. TPBIAS provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes.
XO, XI	37, 38	–	Crystal	Crystal oscillator. X0 and X1 connect to a 24.576-MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used. The suggested values of 12 pF are appropriate for a crystal with 15 pF specified loads.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4 V
Input voltage range, V_I . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PT	1315 mW	10.5 mW/°C	842 mW

† This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted 95°C/W.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC(SP)}$		3	3.3	3.6	V
Supply voltage, $V_{CC(NSP)}$		2.7‡	3	3.6	V
High-level input voltage, V_{IH}	CMOS inputs	0.7 V_{CC}			V
Low-level input voltage, V_{IL}	CMOS inputs			0.2 VCC	V
Differential input voltage, V_{ID}	Cable inputs	142		260	mV
Common-mode input voltage, V_{IC}	Cable inputs, V_{CC} > 3 V	1.165		2.515	V
	Cable inputs, V_{CC} < 3 V	1.165		2.015‡	V
Receive input jitter	TPA, TPB cable inputs			±1.08	ns
Receive input skew	Between TPA and TPB cable inputs			±0.8	ns
High- or low-level output current, I_{OL} or I_{OH}	SYSCLK	–16		16	mA
	CTL0, CTL1, D0, D1, CNA	–12		12	mA
Output current, I_O	TPBIAS	–2		1	mA

‡ This parameter is for a node that does not source power (see section 4.2.2.2 in IEEE 1394-1995 standard).

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
V_{OD}	Differential output voltage	56-Ω load	172	265	mV
$I_{(DIFF)}$	Driver difference output current	Driver enabled	–1.05§	1.05§	mA
V_D	Off-state voltage			20	mV

§ This parameter limits are defined as algebraic sum of TPA+ and TPA– driver currents. These limits also apply to TPB+ and TPA– algebraic sum of driver currents.

receiver

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
I_{IC}	Common-mode input current	Driver disabled	–20	20	μA
z_{ID}	Differential input impedance	Driver disabled	5	6	kΩ pF
z_{IC}	Common-mode input impedance	Driver disabled	20	24	kΩ pF
V_{IT1}	Receiver input threshold voltage		–30	30	mV
	Cable-bias detect threshold, TPB cable input	Driver disabled	0.6	1	V

device

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IT2}	Power status input threshold voltage (CPS)	400-kΩ resistor	4.7		7.5	V
V_{OH}	High-level output voltage	I_{OH} = max, V_{CC} = min	V_{CC} –0.55			V
V_{OL}	Low-level output voltage	I_{OL} = min, V_{CC} = max			0.5	V
	Input current (LREQ, LPS, PD, PC0, PC1, PC2)	V_I=V_{CC} or 0			±1	μA
I_{OZ}	High-impedance-state output current (CTL0, CTL1, D0, D1, C/LKON)	V_O= V_{CC} or 0			±5	μA
	Pullup input current, $\overline{\text{RESET}}$	V_I =1.5 V	–20	–40	–80	μA
		V_I =0	–22	–45	–90	μA
	Power-up reset time, $\overline{\text{RESET}}$		2			ms
$V_{(TO)+}$	Positive arbitration comparator threshold voltage		89		168	mV
$V_{(TO)–}$	Negative arbitration comparator threshold voltage		–168		–89	mV
V_O	TPBIAS output voltage		1.665		2.015	V
I_{CC}	Supply current, receiver active	V_{CC} = 3.6 V			115	mA
$I_{CC(PD)}$	Supply current, power-down mode	V_{CC} = 3 V		10		mA

thermal characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		95		°C/W
$R_{\theta JA}$	Junction-to-case-thermal resistance			19		°C/W

switching characteristics

PARAMETER		MEASURED	TEST CONDITION	MIN	MAX	UNIT
	Jitter, transmit	TPA, TPB			±0.8	ns
	Skew time, transmit	Between TPA and TPB			±0.4	ns
t_r	Rise time, transmit	10% to 90%	R_L = 55 Ω, C_L = 10 pF		3.2	ns
t_f	Fall time, transmit	90% to 10%	R_L = 55 Ω, C_L = 10 pF		3.2	ns
t_{su}	Setup time, D, CTL, LREQ low or high before SYSCLK	50% to 50%	See Figure 1	5		ns
t_h	Hold time, D, CTL, LREQ low or high after SYSCLK	50% to 50%	See Figure 1	2		ns
t_d	Delay time, SYSCLK high to D, CTL low or high	50% to 50%	See Figure 2	2	11	ns

PARAMETER MEASUREMENT INFORMATION

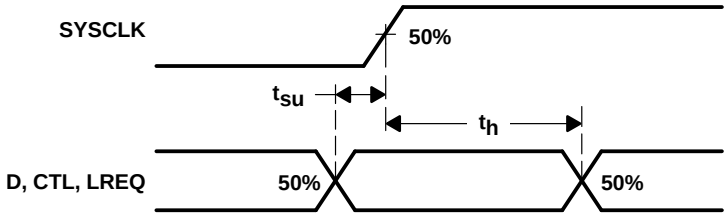


Figure 1. D, CTL, LREQ Input Setup and Hold Timing Waveforms

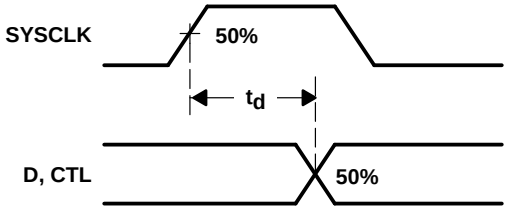


Figure 2. D and CTL Output Delay Timing Waveforms

APPLICATION INFORMATION

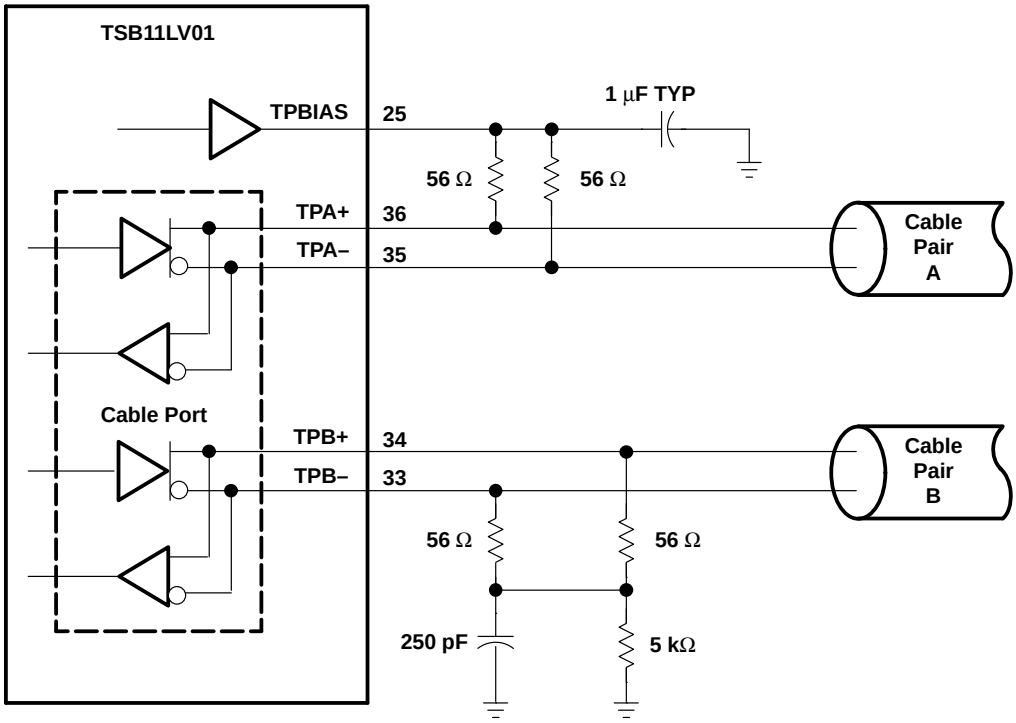


Figure 3. Twisted-Pair Cable Interface Connections

APPLICATION INFORMATION

internal register configuration

The accessible internal registers of this device are listed in Table 1. Descriptions of the internal register fields are given in Table 2.

Table 1. Accessible Internal Registers

Address	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD		Rev		NP			
0011	AStat		BStat		Ch	Con	Reserved	
0100	Reserved							
0101	Reserved							
0110	LoopInt	CPSInt	CPS	IR	Reserved			
0111	Reserved							
1000	Reserved							

Table 2. Internal Register Field Descriptions

Field	Size (Bits)	Type	Description
AStat	2	Read only	AStat contains the line state of TPA. The status is indicated by the following: 11 = Z 01 = 1 10 = 0 00 = Invalid data state. Power-up reset initializes to this line state. This line state is also output during transmit and receive operations. The line state outputs are generally valid during arbitration and idle conditions on the bus.
BStat	2	Read only	BStat contains the line state of TPB. The status is indicated by the following: 11 = Z 01 = 1 10 = 0 00 = Invalid data state. Power up reset initializes to this line state. This line state is also output during transmit and receive operations. The line state outputs are generally valid during arbitration and idle conditions on the bus.
Ch	1	Read only	When Ch = 1, the port is a child, otherwise it is a parent. This bit is invalid after a hardware reset or a bus reset until tree-ID processing is completed.
Con	1	Read only	Con indicates the connection status of the port. When Con = 1, the port is connected, otherwise it is disconnected. This bit is set to 1 by a hardware reset and is updated to reflect the actual cable connection status of the port during bus reset. The TSB11LV01 contains connection debounce circuitry that prevents a new cable connection on a port from initiating a bus reset until the connection status has been stable for at least 335 ms. Similarly, a cable disconnect must be stable for 1.3 ms before a bus reset is initiated.
CPS	1	Read only	Cable power status (CPS) contains the status of the CPS input terminal. When cable power voltage has dropped too low for reliable operation, this bit is reset (0). This bit is included twice in the internal registers to expedite handling of the CPSInt.
CPSInt	1	Read/Write	CPSint indicates that a cable power status interrupt has occurred. This interrupt occurs whenever the CPS input goes low. The interrupt indicates that the cable power voltage has dropped too low to ensure reliable operation. This bit is cleared (0) by a hardware reset or by writing a 0 to this register. However, if the CPS input is still low, another cable power status interrupt immediately occurs.

Table 2. Internal Register Field Descriptions (continued)

Field	Size (Bits)	Type	Description
GC	6	Read/Write	The gap count (GC) register sets the fair and arb-reset gap times. The gap count may be set to a particular value to optimize bus performance. Typically, the gap count should be set to 2 times the maximum number of hops on the bus and should be set to the same value for all nodes on the bus. The gap count can be set by either a write to this register or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to a 3Fh after a hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either a write to the gap count register by the link or a PHY_CONFIG packet).
IBR	1	Read/Write	When set, initiate bus reset (IBR) causes this node to immediately initiate a bus reset. IBR is cleared (0) after a hardware reset or a bus reset.
IR	1	Read/Write	IR indicates that the last bus reset was initiated in this TSB11LV01 phy. This bit is also included in the Self-ID packet.
LoopInt	1	Read/Write	LoopInt indicates that a configuration loop timeout has occurred. This interrupt occurs when the arbitration controller waits for too long a period of time during tree-ID. This interrupt can indicate that the bus is configured in a loop. This bit is cleared (0) by a hardware reset or by writing a 0 to this register bit. It should be noted that the TSB11LV01 never generates this interrupt since it has only one available port and, therefore, cannot be part of a loop.
NP	4	Read only	The number of ports (NP) contains the number of ports implemented in the core logic (not the number of ports actually on the device). For the TSB11LV01, NP is set to 0011.
Physical ID	6	Read only	Physical ID contains the physical address of the local node. The physical ID defaults to a 09h after a hardware reset or a bus reset until the Self-ID process has been completed. A complete Self-ID is indicated by an unsolicited status transfer of the register 0 contents to the link.
R	1	Read only	R indicates whether this node is the root node or not. This bit is cleared (0) on a hardware reset or a bus reset. This bit is set during tree-ID when this node is root.
Rev	2	Read only	The revision (Rev) bits indicate the design revision of the core logic. For the TSB11LV01, Rev is set to 01.
RHB	1	Read/Write	When set, the root hold-off bit (RHB) instructs the local node to try to become the root during the next bus reset. RHB is reset (0) during a hardware reset and is not affected by a bus reset.
SPD	2	Read only	The speed (SPD) bits indicates the top signaling speed of the local port and for the TSB11LV01 is set to 00.

APPLICATION INFORMATION

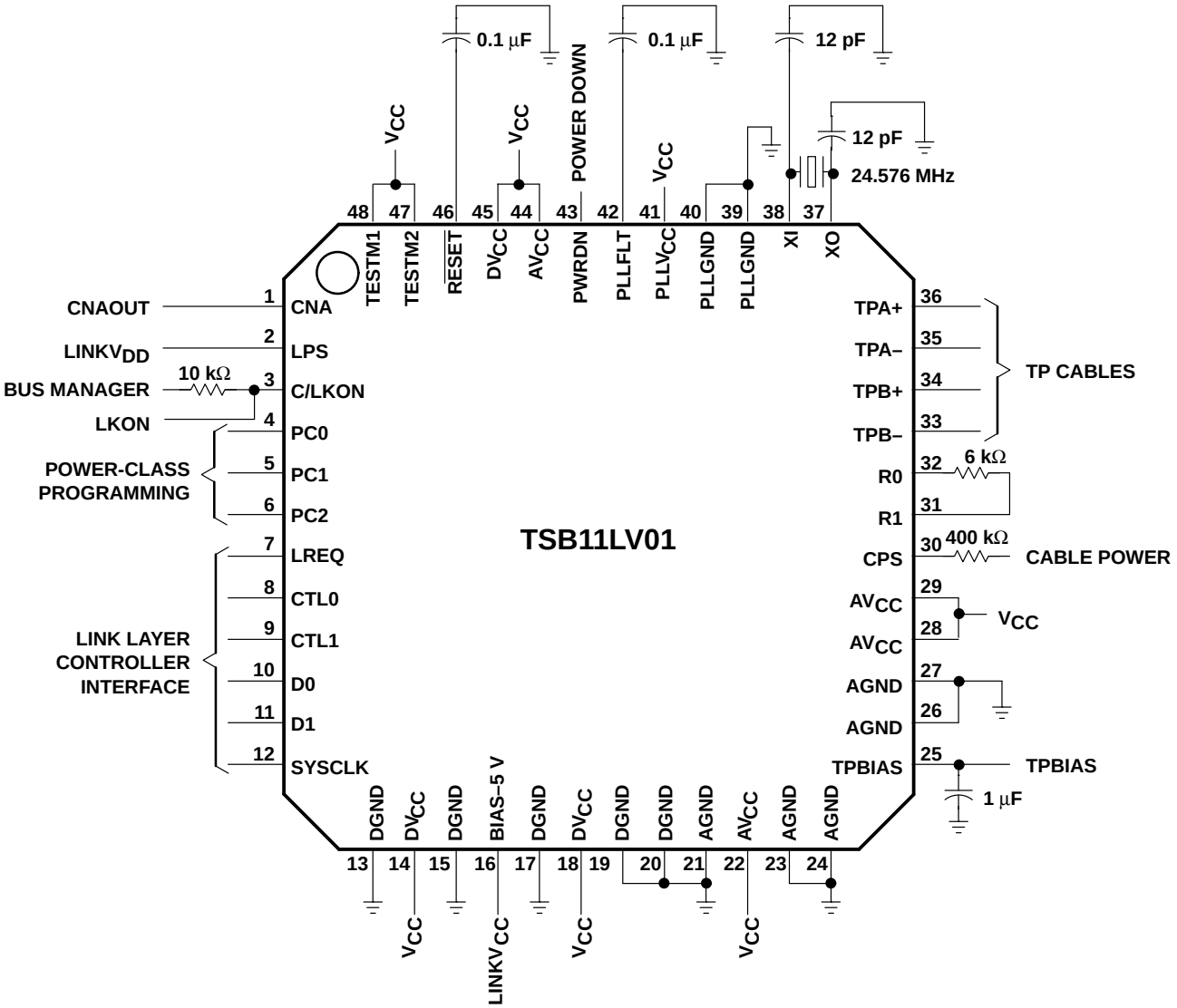


Figure 4. External Component Connections

PRINCIPLES OF OPERATION

The TSB11LV01 is designed to operate with a link layer controller such as the Texas Instruments TSB12C01A. These devices use a direct-connect interface such as described in Annex J of the IEEE 1394-1995 standard. Details of how the TSB12C01A (link) devices operates are described in the TSB12C01A data sheet. The following paragraphs describes the operation of the phy-link interface.

The TSB11LV01 supports 100 Mbits/s data transfers, and has two bidirectional data lines (D0 and D1) crossing the interface. In addition there are two bidirectional control lines (CTL0 and CTL1), the 50-MHz SYSCLK line from the phy to the link, and the link request line (LREQ) from the link to the phy. The TSB11LV01 phy has control of all the bidirectional terminals. The link is allowed to drive these terminals only after it has been given permission by the phy. The dedicated LREQ request terminal is used by the link for any activity that it wishes to initiate.

There are four operations that may occur in the phy-link interface: request, status, transmit, and receive. With the exception of the request operation, all actions are initiated by the phy.

When the phy has control of the bus, the CTL0 and CTL1 lines are encoded as shown in Table 3.

Table 3. CTL Status When Phy Has Control of the Bus

CTL0, CTL1	Name	Description of Activity
00	Idle	No activity is occurring (this is the default mode)
01	Status	Status information is being sent from the phy to the link
10	Receive	An incoming packet is being sent from the phy to the link
11	Transmit	The link has been given control of the bus to send an outgoing packet

When the link has control of the bus (with phy permission), the CTL0 and CTL1 lines are encoded as shown in Table 4.

Table 4. CTL Status When Link Has Control of the Bus

CTL0, CTL1	Name	Description of Activity
00	Idle	The link releases the bus (transmission has been completed)
01	Hold	The link is holding the bus while data is being prepared for transmission or sending another packet without arbitrating
10	Transmit	An outgoing packet is being sent from the link to the phy
11	Reserved	None

When the link wishes to request the bus or access a register that is located in the TSB11LV01 phy, a serial stream of information is sent across the LREQ line. The length of the stream varies depending on whether the transfer is a bus request, a read command, or a write command (see Table 5). Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. Bit 0 is the most significant, and is transmitted first. The LREQ terminal is required to idle low.

Table 5. Link Bus Request or Register Access Request Bit Length

Request Type	Number of Bits
Bus Request	7
Read Register Request	9
Write Register Request	17

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For a Bus Request the length of the LREQ data stream is 7 bits and is shown in Table 6.

Table 6. Link Bus Request

Bit(s)	Name	Description
0	Start Bit	This bit indicates the beginning of the transfer (always 1).
1–3	Request Type	These bits indicate the type of bus request (see Table 9 for the encoding of this field).
4–5	Request Speed	These bits should always be 00 for TSB11LV01 100 Mbits/s speed.
6	Stop Bit	This bit indicates the end of the transfer (always 0).

For a Read Register Request the length of the LREQ data stream is 9 bits and is shown in Table 7.

Table 7. Link Read Register Access

Bit(s)	Name	Description
0	Start Bit	This bit indicates the beginning of the transfer (always 1).
1–3	Request Type	These bits are always 100 indicating that this is a read register request.
4–7	Address	These bits are the address of the phy register to be read.
8	Stop Bit	This bit indicates the end of the transfer (always 0).

For a Write Register Request the length of the LREQ data stream is 17 bits and is shown in Table 8.

Table 8. Link Write Register Access

Bit(s)	Name	Description
0	Start Bit	This bit indicates the beginning of the transfer (always 1).
1–3	Request Type	These bits are always 101 indicating that this is a write register request.
4–7	Address	These bits are the address of the phy register to be written to.
8–15	Data	These bits are the data that is written to the specified register address.
16	Stop Bit	This bit indicates the end of the transfer (always 0).

The 3-bit Request Type fields are described in Table 9.

Table 9. Link Bus Request Type

LREQ1 – LREQ3	Name	Description
000	ImmReq	Immediate request. When an idle is detected, take control of the bus immediately (no arbitration).
001	IsoReq	Isochronous request. Arbitrate for the bus with no gaps.
010	PriReq	Priority request. Arbitrate after a subaction gap and ignore fair protocol.
011	FairReq	Fair request. Arbitrate after a subaction gap and use fair protocol.
100	RdReg	Read register. Return the specified register contents through a status transfer
101	WrReg	Write register. Write to the specified register.
110, 111	Reserved	Reserved

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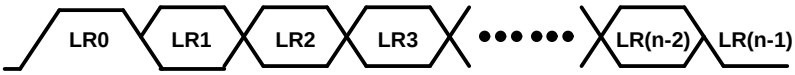
request



NOTE A: Each cell in this timing diagram represents one clock sample time.

Figure 5. LREQ Timing

bus request

For fair or priority access, the link requests control of the bus at least one clock after the phy-link interface becomes idle. If the link senses that the CTL terminals are in a receive state (CTL0 and CTL1 = 10), then it knows that its request has been lost. This is true anytime during or after the link sends the bus request transfer on LREQ. Additionally, the phy ignores any fair or priority requests if it asserts the receive state while the link is requesting the bus. The link then reissues the request one clock after the next interface idle.

The cycle master uses a priority request to send a cycle start message. After receiving a cycle start, the link can issue an isochronous bus request. When arbitration is won, the link proceeds with the isochronous transfer of data. The phy clears an isochronous request only when the bus has been won. The isochronous request register is cleared in the phy once the link sends another type of request or when the isochronous transfer has been completed. The isochronous request must be issued during a packet reception. Usually this occurs during the reception of a cycle start packet.

The ImmReq request is issued when the link needs to send an acknowledgment after reception of a packet addressed to it. This request must be issued during packet reception. This is done to minimize the delays that a phy would have to wait between the end of a packet and the transmittal of an acknowledgment. As soon as the packet ends, the phy immediately grants access of the bus to the link. The link sends an acknowledgment to the sender unless the header cyclic redundancy check (CRC) of the packet turns out to be bad. In this case, the link releases the bus immediately; it is not allowed to send another type of packet on this grant. To ensure another packet is not sent, the link is forced to wait 160 ns after the end of the packet is received. The phy then gains control of the bus and the acknowledgment with the CRC error is sent. Then the bus is released and allowed to proceed with another request.

Although highly improbable, it is conceivable that two separate nodes could believe that an incoming packet is intended for them. The nodes then issue a ImmReq request before checking the CRC of the packet. Since each phy seizes control of the bus at the same time, a temporary, localized collision of the bus occurs somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a ZZ line state and not a bus reset. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line state is removed. The only side effect would be the loss of the intended acknowledgment packet (this is handled by the higher-layer protocol).

phy register read/write requests

When the link requests to read the specified register contents, the phy sends the contents of the register to the link through a status transfer. If an incoming packet is received while the phy is transferring status information to the link, the phy continues to attempt to transfer the contents of the register until it is successful.

For write requests, the phy loads the data field into the appropriately addressed register as soon as the transfer has been completed. The link is allowed to request register read or write operations at any time.

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status

A status transfer is initiated by the phy when it has status information to transfer to the link. The phy waits until the interface is idle before starting the transfer. The transfer is initiated by asserting the following on the the control terminals: CTL0 and CTL1 = 01 along with the first two bits of status information on the D0 and D1 terminals. The phy maintains CTL0 and CTL1 = 01 for the duration of status transfer. The phy may prematurely end a status transfer by asserting something else other than CTL0 and CTL1 = 01 on the control terminals. This could be caused by an incoming packet from another node. The phy continues to attempt to complete the transfer until the information has been successfully transmitted. There must be at least one idle cycle in between consecutive status transfers.

The phy normally sends just the first four bits of status to the link. These bits are status flags that are needed by the link state machines. The phy sends an entire status packet to the link after a request transfer that contains a read request, or when the phy has pertinent information to send to the link or transaction layers. The only defined condition where the phy automatically sends a register to the link is after Self-ID, when it sends the Physical-ID register, which contains the new node address.

The descriptions of the bits in the status transfer are listed in Table 10 and the timing is shown in Figure 6.

Table 10. Status Transfer Bit Description

Bit(s)	Name	Description
0	Arbitration Reset Gap	This bit indicates that the phy has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the IEEE 1394-1995 standard). This bit is used by the link in its busy/retry state machine.
1	Subaction Gap	This bit indicates that the phy has detected that the bus has been idle for a subaction gap time (this time is defined in the IEEE 1394-1995 standard). This bit is used by the link to detect the completion of an isochronous cycle.
2	Bus Reset	This bit indicates that the phy has entered the bus reset state.
3	CPS	This bit indicates that the cable power has dropped below the threshold for reliable operation.
4–7	Address	These bits hold the address of the phy register whose contents are transferred to the link.
8–15	Data	These bits contain the data that is to be sent to the link.

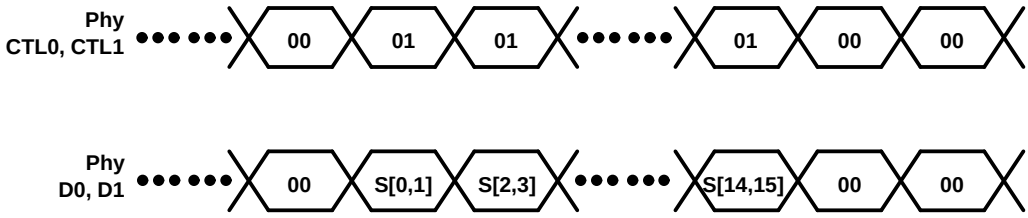


Figure 6. Status Transfer Timing

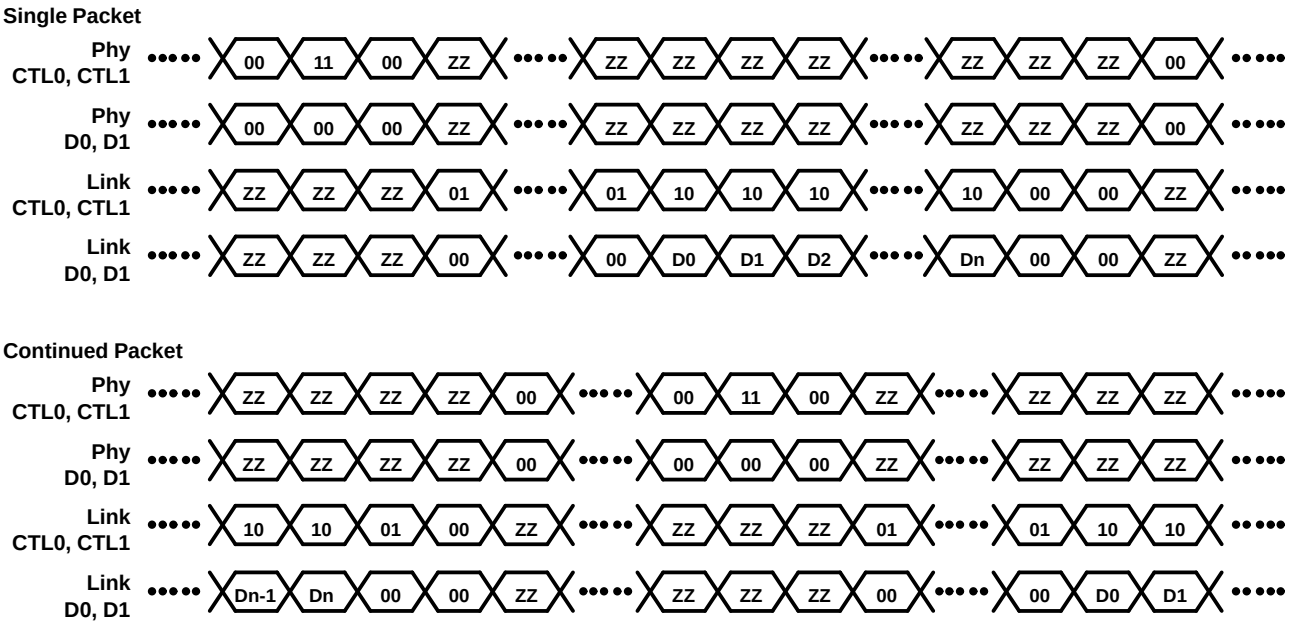
PRINCIPLES OF OPERATION

transmit

When the link wants to transmit information, it first requests access to the bus through the LREQ terminal. Once the phy receives this request, it arbitrates to gain control of the bus. When the phy wins ownership of the serial bus, it grants the bus to the link by asserting the transmit state on the CTL terminals for at least one SYSCLK cycle. The link takes control of the bus by asserting either hold or transmit on the CTL lines. Hold is used by the link to keep control of the bus when it needs some time to prepare the data for transmission. The phy keeps control of the bus for the link by asserting a data-on state on the bus. It is not necessary for the link to use hold when it is ready to transmit as soon as bus ownership is granted.

When the link is prepared to send data, it asserts transmit on the CTL lines as well as sending the first bits of the packet on the D0 and D1 lines (assuming 100 Mbits/s). The transmit state is held on the CTL terminals until the last bits of data have been sent. The link then asserts idle on the CTL lines for one clock cycle after which it releases control of the interface.

However, there are times when the link needs to send another packet without releasing the bus. For example, the link may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the link asserts a hold instead of an idle when the first packet of data has been completely transmitted. Hold, in this case, informs the phy that the link needs to send another packet without releasing control of the bus. The phy then waits a set amount of time before asserting transmit. The link can then proceed with the transmittal of the second packet. After all data has been transmitted and the link has asserted idle on the CTL terminals, the phy asserts its own idle state on the CTL lines. When sending multiple packets in this fashion, it is required that all data be transmitted at the same speed. This is required because the transmission speed is set during arbitration and since the arbitration step is skipped, there is no way of informing the network of a change in speed.



NOTE A: ZZ = High Impedance State
D0 => Dn = Packet data

Figure 7. Transmit Timing Waveforms

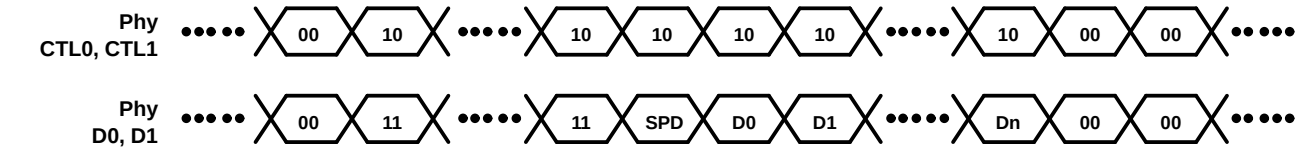
PRINCIPLES OF OPERATION

receive

When data is received by the phy from the serial bus, the phy transfers the data to the link for further processing. The phy asserts receive on the CTL lines and asserts each D terminal high. The phy indicates the start of the packet by placing the speed code on the data bus. The phy then proceeds with the transmittal of the packet to the link on the D lines while still keeping the receive status on the CTL terminals. Once the packet has been completely transferred, the phy asserts idle on the CTL terminals, which completes the receive operation.

NOTE

The speed is a phy-link protocol and not included in the CRC.



NOTE A: SPD = Speed Code
D0 => Dn = Packet data

Figure 8. Receive Timing Waveforms

Table 11. Speed Code For the Receiver

Speed Code (D0, D1)	Data Rate
00	100 Mbits/s

power class bits in the Self-ID packet

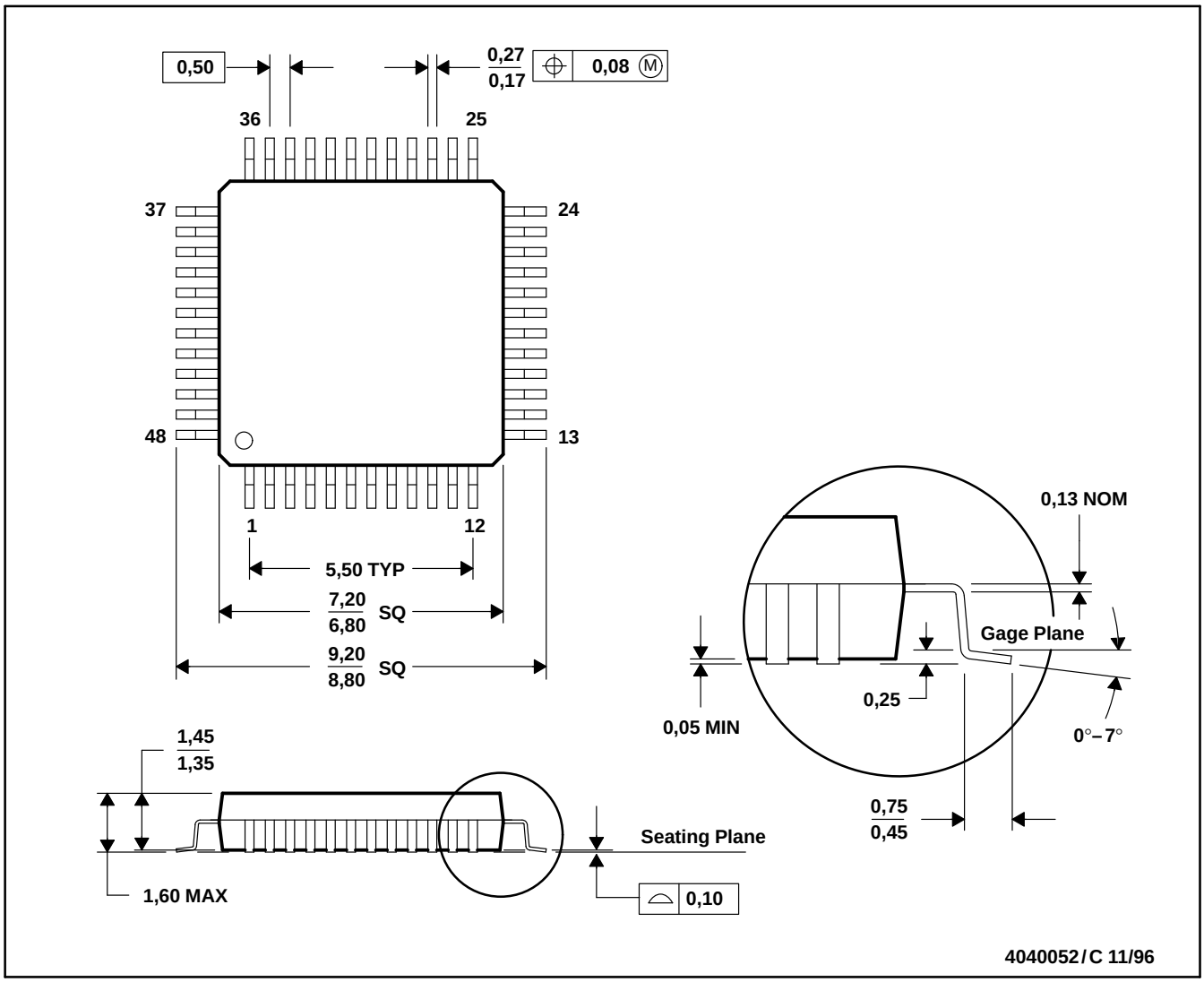
Table 12 contains a description of each power class bit in the power field (bits 21, 22, and 23) of the Self-ID packet.

Table 12. Self-ID Packet Power Field Bit Description

PC0 – PC2	Description
000	Node does not need power and does not repeat power.
001	Node is self powered and provides a minimum of 15 W to the bus.
010	Node is self powered and provides a minimum of 30 W to the bus.
011	Node is self powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 1 W.
101	Node may be powered from the bus and is using up to 1 W. An additional 2 W is needed to enable the link and higher layers.
110	Node may be powered from the bus and is using up to 1 W. An additional 5 W is needed to enable the link and higher layers.
111	Node may be powered from the bus and is using up to 1 W. An additional 9 W is needed to enable the link and higher layers.

MECHANICAL INFORMATION

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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