TSBKPCI12C01A
Reference Design Guide

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TSB12C01A and TSB11C01

TEXAS INSTRUMENTS

1394 Solutions Leader

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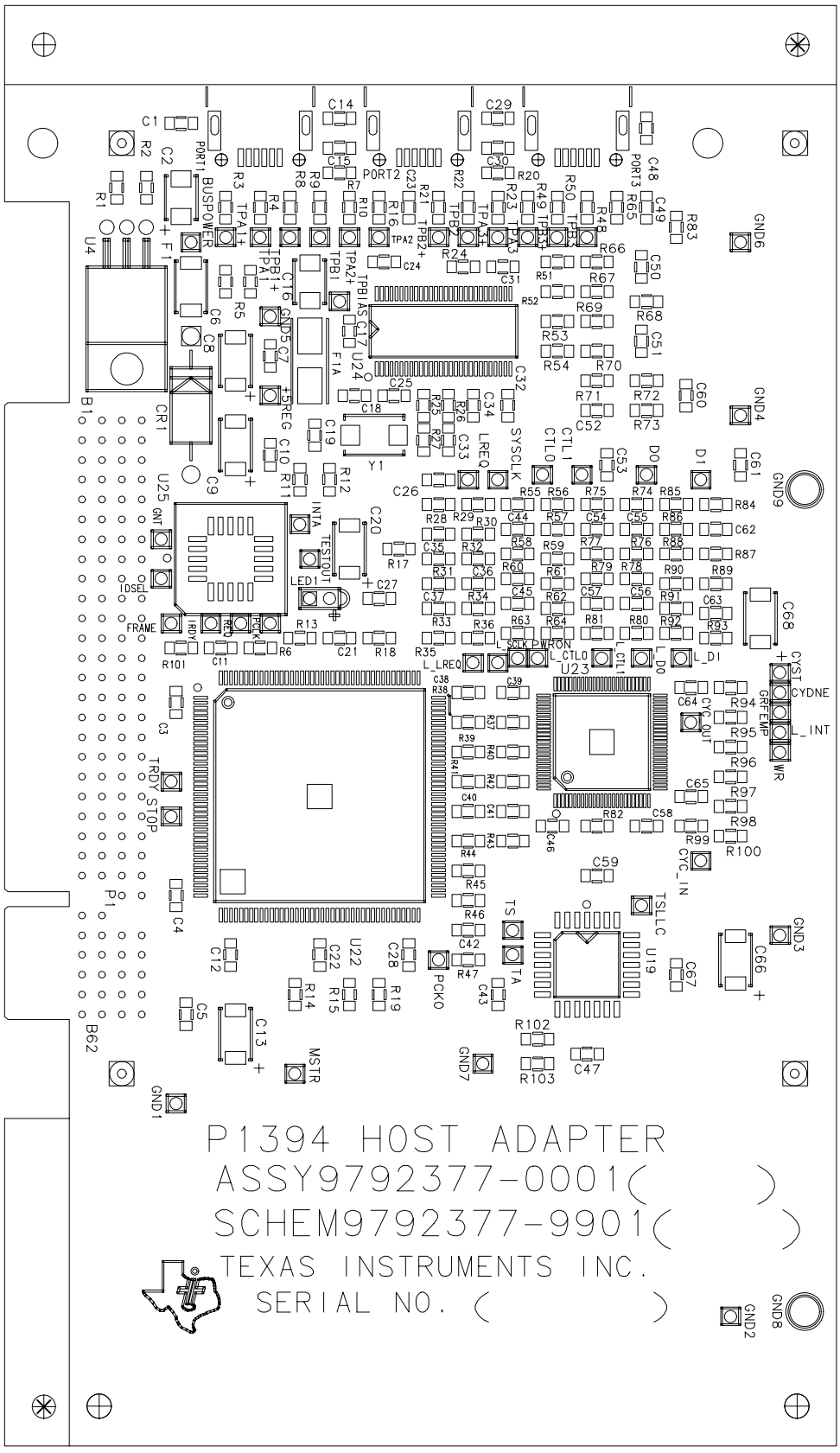
PCI Host Adapter (TSBKPCI12C01A)

- TSB12C01A Link Layer, TSB11C01 Physical Layer
- Example of connecting up TSB12C01A to TSB11C01 with 1394-1995 isolation circuitry (currently not supported by silicon)
- Cable Power
- Cable PWB connections
- Specification for Custom ASIC to connect to PCI


P1394 HOST ADAPTER
ASSY9792377-0001( )
SCHEM9792377-9901( )
TEXAS INSTRUMENTS INC.
SERIAL NO. ( )

Revised 06/05/96

These are things to keep in mind when looking at the TSB11C01 reference design schematic. This is the design of a circuit board we use to test our chips in a PC environment in our lab.

1. Page 4 shows the circuitry for a 3 port cable physical layer chip (TSB11C01) using an external 24.576MHz crystal for the clock reference. On this schematic page note that to disable isolation mode pin 12 (ISO-) should be tied high.
The connections shown for the shields of PORTS 1->3 are incorrect. The terminals labeled 7 and 8 are both connected to the outside shield of the connector (the internal shields of the twisted pairs are connected to the terminal labeled 2, phy_gnd). The schematic shows all of the terminal 7 and 8 s as connected to chassis_gnd. This is incorrect and will connect all the chassis grounds on boards like this one on the 1394 bus together. The correct connection is to have the external shield connected to chassis ground through a 1MOhm resister in parallel with a 0.1 uF capacitor as shown in figure 3-30 in the 1394 Standard (rev8.0v2).

2. Page 5 shows the connections for the suggested IEEE 1394-1995 capacitive isolation between the PHY and link layer chip (link). Currently our chip set does not support isolation this isolation scheme (but does support bus holder isolation, TI patent pending). To remove the isolation circuitry:

Remove: R56,R59,R62,R63, R75,R61,R81,R64, R85,R88,R91,R80, R84,R90,R92,R93, R34,R36, R29,R30,R33, and R35 on page 5.
Replace with a short (0 Ohm): R58,R60,C45, R77,R79,C57, R76,R78,C56, R87,R89,C63, R32,C36, R31, and C37.
Replace with a 274 Ohm resister: R55, R57, R74, R86, and R28.
Replace with a 220 Ohm resister: C44, C54, C55, C62, and C35.
And remove resistor R73 on page 4 (see note [1]).

Note that to disable isolation mode:

pin 12 (ISO-) on the TSB11C01 should be tied high and
pin 69 (LNK_ISOBAR) on the TSB12C01A should be tied high.

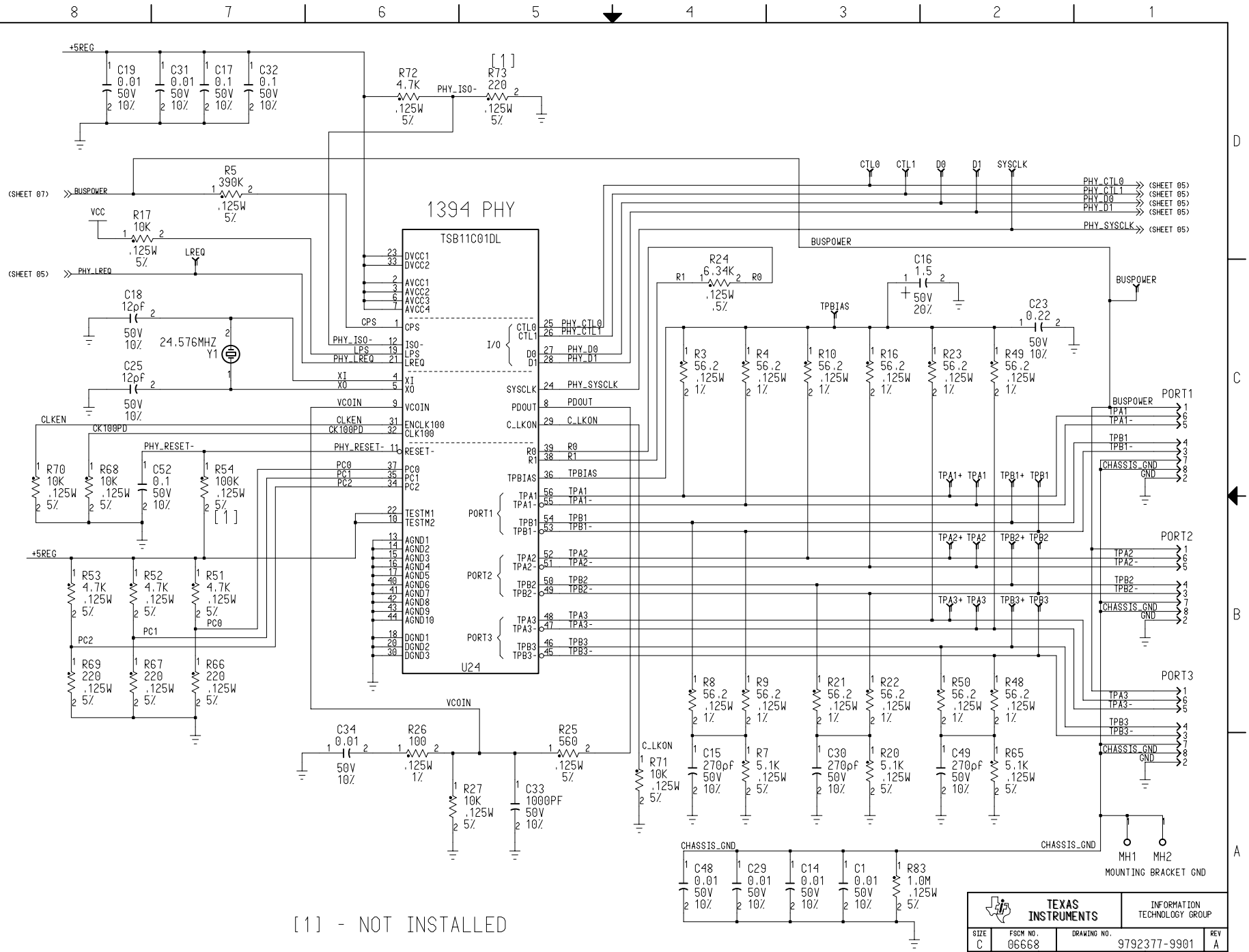
3. Page 6 is the connections to the custom ASIC TI used to connect to a PCI bus to create this test board. The ASIC as designed is not a catalog part but in 1996 a catalog part called PCI-Lynx (TSB12LV21) will be in production that connects a 1394 physical layer chip with a PCI bus along with lots of other functionality.

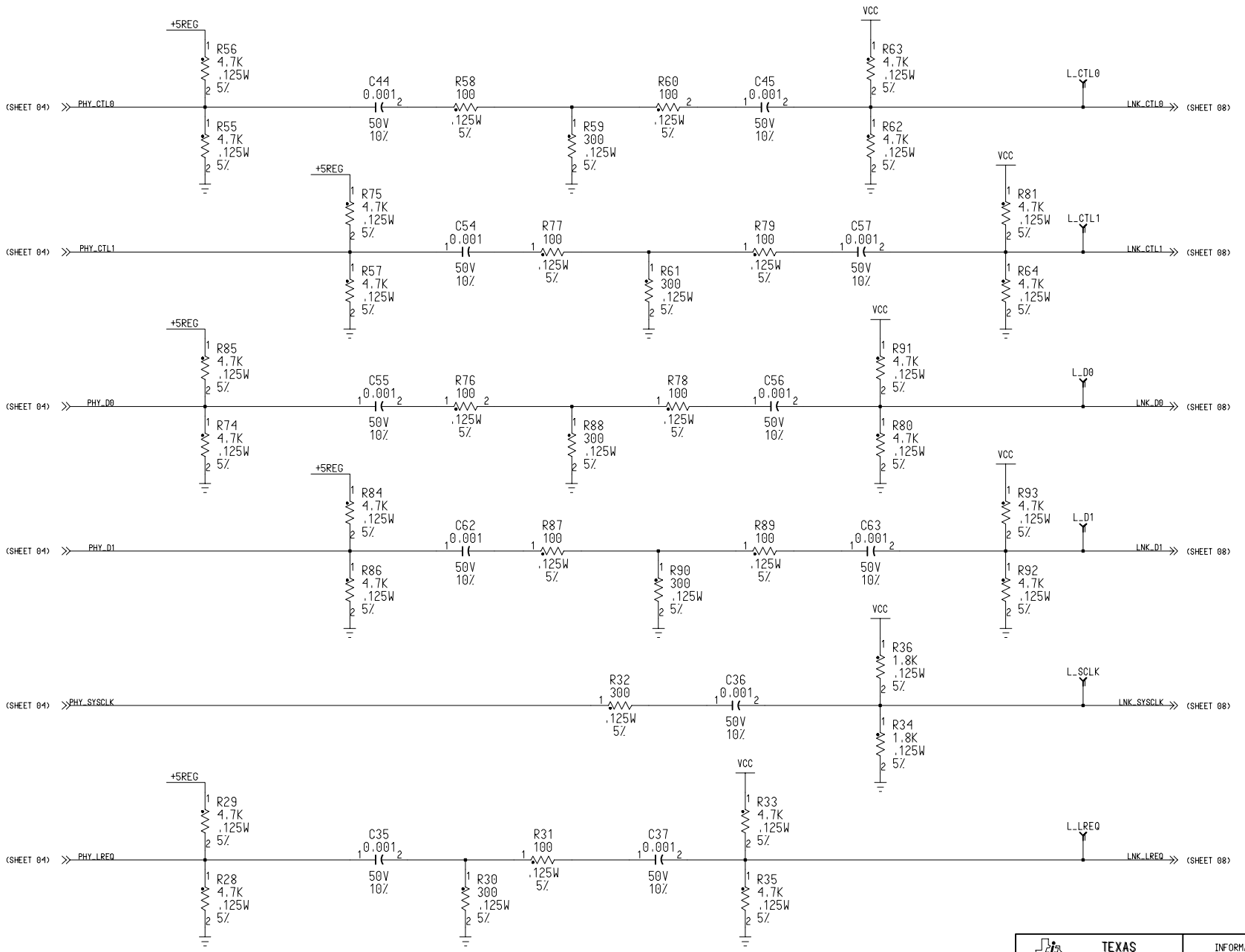
4. Page 7 contains the voltage regulator to provide cable power to the PHY chips. The PAL U19 is needed to provide delays if using the 12C01 link layer chip. If using the TSB12C01A link chip it is not needed.

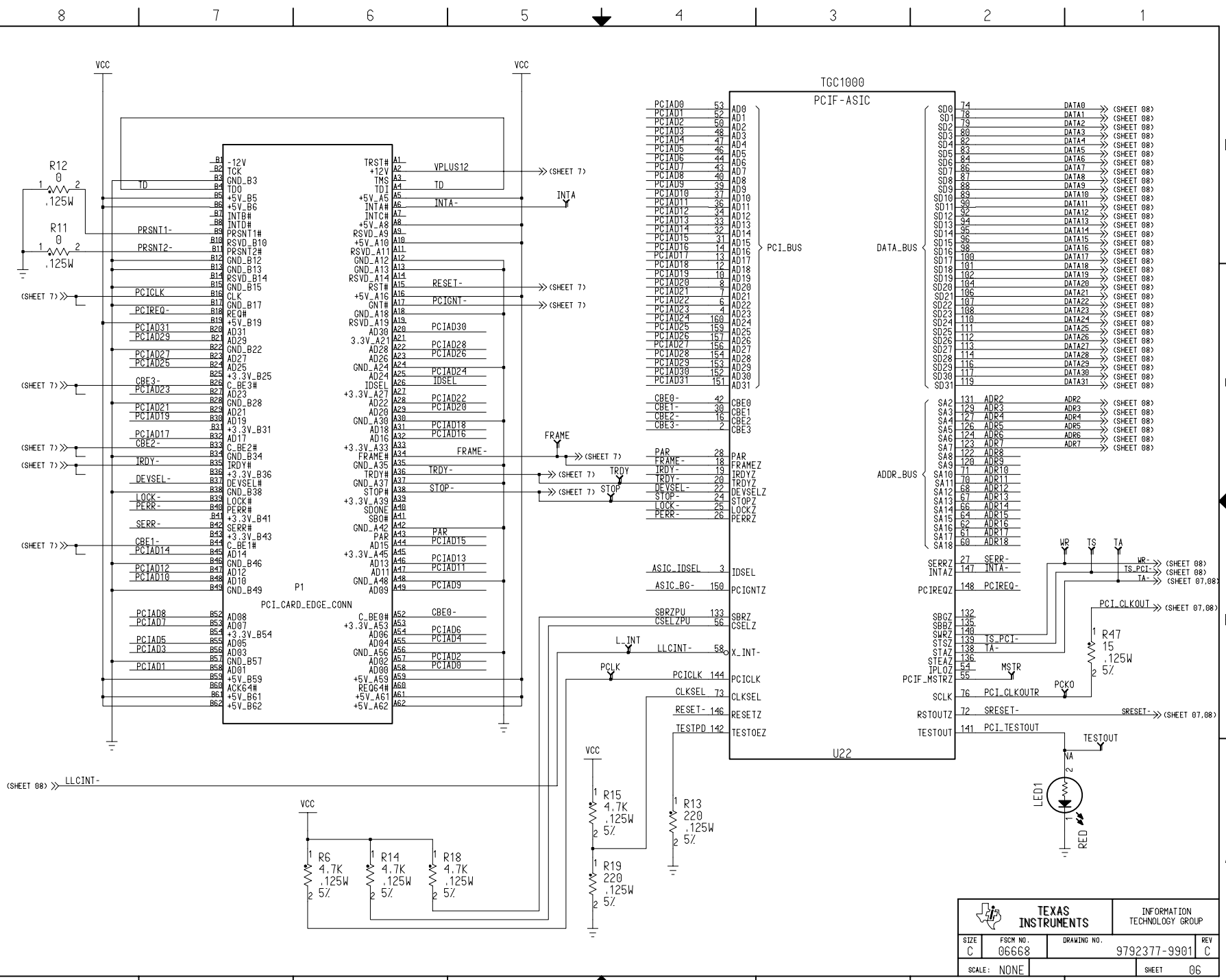
5. Page 8 show the connections to the TSB12C01A link layer chip. Note that to disable isolation mode pin 69 (ISOBAR) should be tied high.

6. Page 9 is the power decoupling capacitors.

TI 1394 Applications Support - 1394@msg.ti.com


1394 PHY
TSB11C01DL
U24
[1] - NOT INSTALLED
TEXAS INSTRUMENTS
INFORMATION TECHNOLOGY GROUP
SIZE C
FSCM NO. 06668
DRAWING NO. 9792377-9901
REV A
SCALE: NONE
SHEET 04
MOUNTING BRACKET GND


+5REG
R56 4.7K ,125W 5%
R55 4.7K ,125W 5%
C44 0.001 50V 10%
R58 100 ,125W 5%
R59 300 ,125W 5%
R60 100 ,125W 5%
C45 0.001 50V 10%
VCC
R63 4.7K ,125W 5%
R62 4.7K ,125W 5%
L_CTL0
(SHEET 04) PHY_CTL0
LNK_CTL0 (SHEET 08)
+5REG
R75 4.7K ,125W 5%
R57 4.7K ,125W 5%
C54 0.001 50V 10%
R77 100 ,125W 5%
R61 300 ,125W 5%
R79 100 ,125W 5%
C57 0.001 50V 10%
VCC
R81 4.7K ,125W 5%
R64 4.7K ,125W 5%
L_CTL1
(SHEET 04) PHY_CTL1
LNK_CTL1 (SHEET 08)
+5REG
R85 4.7K ,125W 5%
R74 4.7K ,125W 5%
C55 0.001 50V 10%
R76 100 ,125W 5%
R88 300 ,125W 5%
R78 100 ,125W 5%
C56 0.001 50V 10%
VCC
R91 4.7K ,125W 5%
R80 4.7K ,125W 5%
L_D0
(SHEET 04) PHY_D0
LNK_D0 (SHEET 08)
+5REG
R84 4.7K ,125W 5%
R86 4.7K ,125W 5%
C62 0.001 50V 10%
R87 100 ,125W 5%
R90 300 ,125W 5%
R89 100 ,125W 5%
C63 0.001 50V 10%
VCC
R93 4.7K ,125W 5%
R92 4.7K ,125W 5%
L_D1
(SHEET 04) PHY_D1
LNK_D1 (SHEET 08)
R32 300 ,125W 5%
C36 0.001 50V 10%
VCC
R36 1.8K ,125W 5%
R34 1.8K ,125W 5%
L_SCLK
(SHEET 04) PHY_SYSCLK
LNK_SYSCLK (SHEET 08)
+5REG
R29 4.7K ,125W 5%
R28 4.7K ,125W 5%
C35 0.001 50V 10%
R30 300 ,125W 5%
R31 100 ,125W 5%
C37 0.001 50V 10%
VCC
R33 4.7K ,125W 5%
R35 4.7K ,125W 5%
L_LREQ
(SHEET 04) PHY_LREQ
LNK_LREQ (SHEET 08)
TEXAS INSTRUMENTS
INFORMATION TECHNOLOGY GROUP
SIZE C
FSCM NO. 06668
DRAWING NO. 9792377-9901
REV A
SCALE: NONE
SHEET 05


TGC1000
PCIF-ASIC
P1
PCI_CARD_EDGE_CONN
PCI_BUS
DATA_BUS
ADDR_BUS
U22
R12
R11
R6
R14
R18
R15
R19
R13
R47
LED1
VCC
INTA
FRAME
TRDY
STOP
L_INT
PCLK
LLCINT-
TESTOUT
PCI_CLKOUT
SRESET-
TEXAS INSTRUMENTS
INFORMATION TECHNOLOGY GROUP
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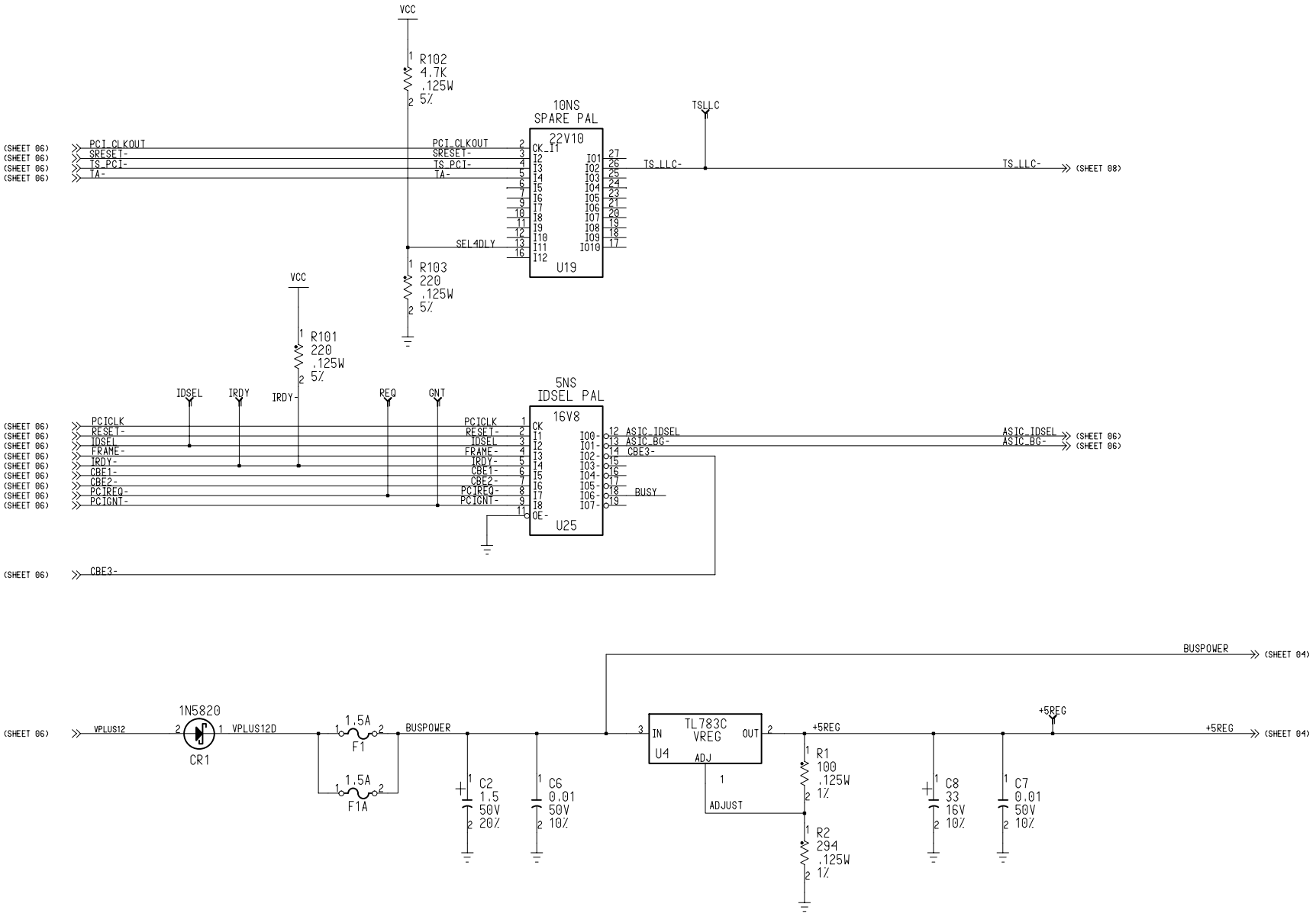
FSCM NO. 06668
DRAWING NO. 9792377-9901
REV C
SCALE: NONE
SHEET 06



TEXAS INSTRUMENTS			INFORMATION TECHNOLOGY GROUP
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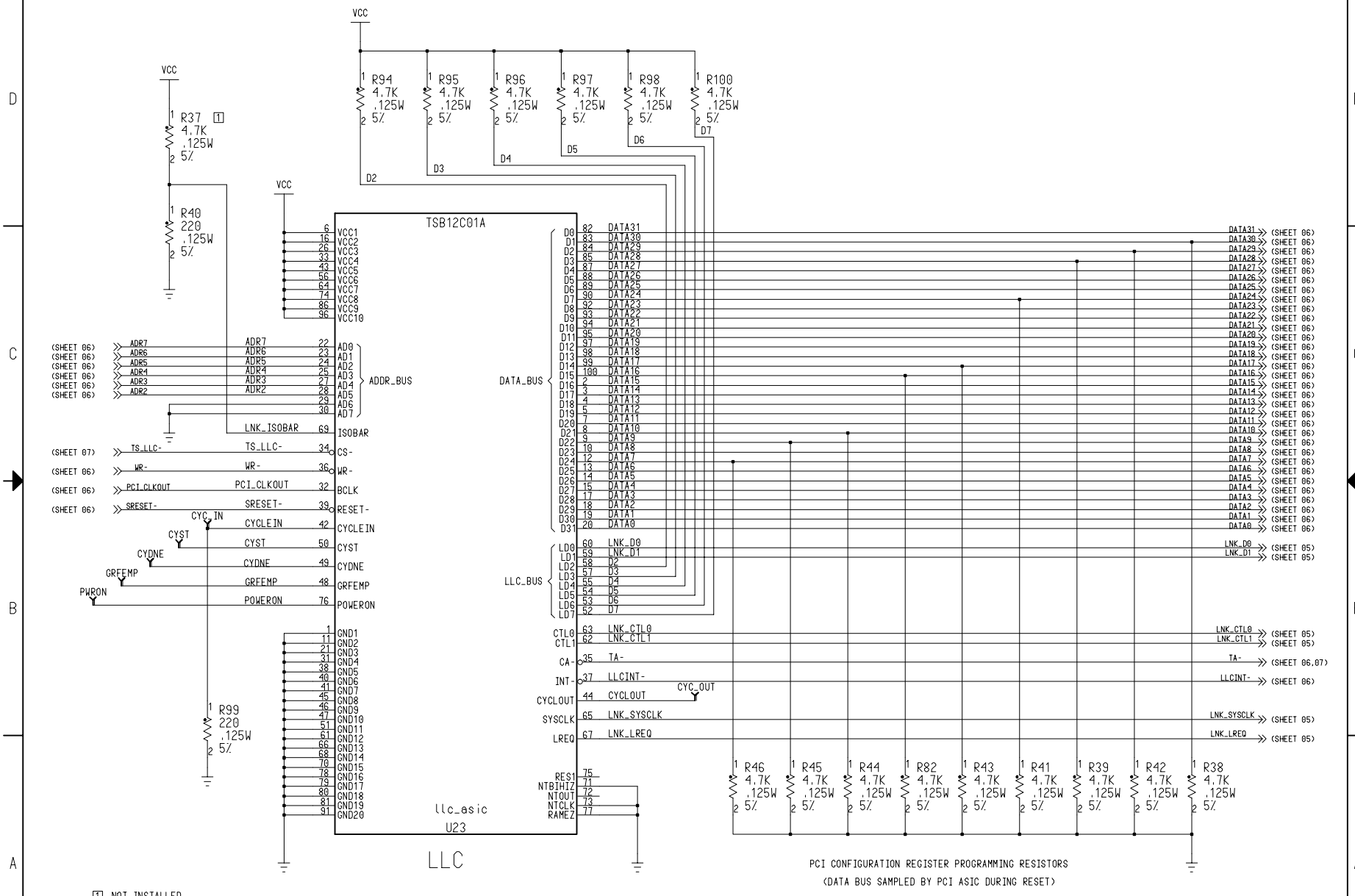
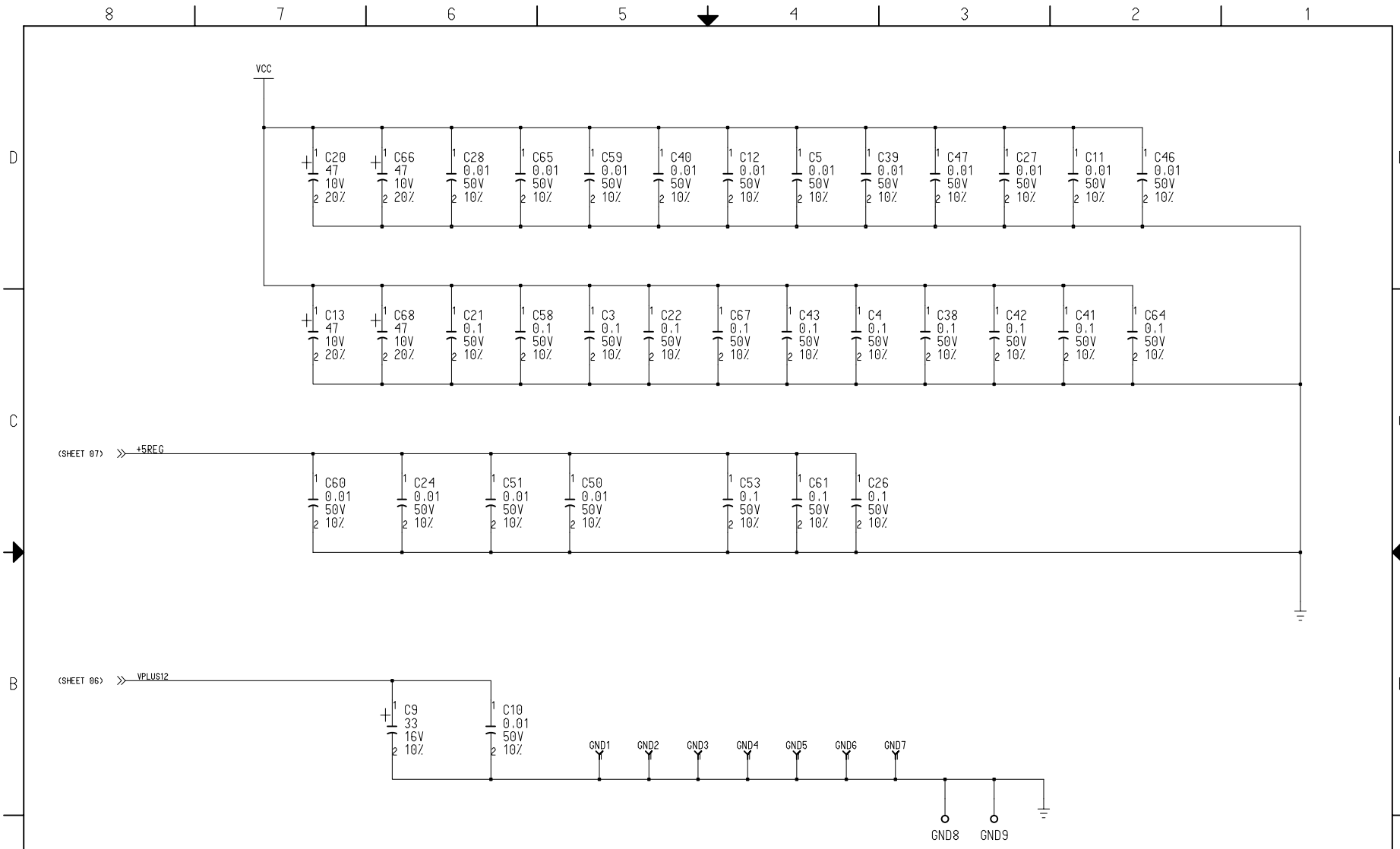
SCALE: NONE			SHEET 07


TSB12C01A
llc_asic
U23
LLC
R37 [1] 4.7K .125W 5%
R40 220 .125W 5%
R94 4.7K .125W 5%
R95 4.7K .125W 5%
R96 4.7K .125W 5%
R97 4.7K .125W 5%
R98 4.7K .125W 5%
R100 4.7K .125W 5%
R99 220 .125W 5%
R46 4.7K .125W 5%
R45 4.7K .125W 5%
R44 4.7K .125W 5%
R82 4.7K .125W 5%
R43 4.7K .125W 5%
R41 4.7K .125W 5%
R39 4.7K .125W 5%
R42 4.7K .125W 5%
R38 4.7K .125W 5%
ADDR_BUS
DATA_BUS
LLC_BUS
PCI CONFIGURATION REGISTER PROGRAMMING RESISTORS
(DATA BUS SAMPLED BY PCI ASIC DURING RESET)
[1] NOT INSTALLED
TEXAS INSTRUMENTS
INFORMATION TECHNOLOGY GROUP
SIZE C
FSCM NO. 06668
DRAWING NO. 9792377-9901
REV D
SCALE: NONE
SHEET 08



TEXAS INSTRUMENTS			INFORMATION TECHNOLOGY GROUP
SIZE C	FSCM NO. 06668	DRAWING NO. 9792377-9901	REV C
SCALE: NONE			SHEET 09

P1394 PROJECT (TI LINEAR, DALLAS, TEXAS)

SPECIFICATION FOR PCI INTERFACE ASIC

Revision * Dated 3/31/94

1.0 SCOPE

This document specifies requirements for an Application Specific Integrated Circuit (ASIC) that interfaces the Peripheral Component Interface (PCI) bus to the P1394 Link Layer Controller (TI - TSB12C01) with a "68040-like" secondary bus that provides the following features:

- master and slave PCI interface
- secondary (040 processor) bus interface
- DMA capability
- Status and control register

2.0 RELATED DOCUMENTS

Peripheral Component Interface Standard (PCI Std Rev. 2.0)

Motorola 68EC040 Processor Users Manual

TI TGC1000 ASIC Gate Array Design Documentation Kit

3.0 TERMINOLOGY AND CONVENTIONS

3.1 LOGIC STATE CONVENTIONS

A true signature shall be in the active state or asserted or logic 1 when the voltage level of the signal is high. The true signal shall be in the inactive or de-asserted or logic 0 when the voltage level of the signal is low.

A low-true, or low-active, signature, designated by a negation bar (-) appended to the signature, shall be in the active state or asserted or logic 1 when the voltage level of the signal is low. The low-true signal shall be in the inactive or de-asserted or logic 0 when the voltage level of the signal is high.

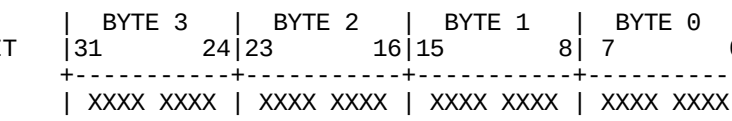
3.2 HEXADECIMAL NOTATION

Hexidecimal notation is identified by a ">" preceding the number.

3.3 BYTE ORDERING

The byte ordering of all the buses associated with this ASIC are "little endian". That is to say, for a 32 bit bus, the least significant byte is byte 0 and the most significant byte is byte 3.

The bits are numbered with bit 0 representing the least significant bit.



```
+-----------+-----------+-----------+-----------+
```

3.4 DEFINITIONS

DWord - 32 bit data item consisting of 4 bytes. Byte 0 of a DWord is the low order byte of the word (least significant) and byte 3 of a DWord is the high order byte of the DWord (most significant).

4.0 FUNCTIONAL DESCRIPTION

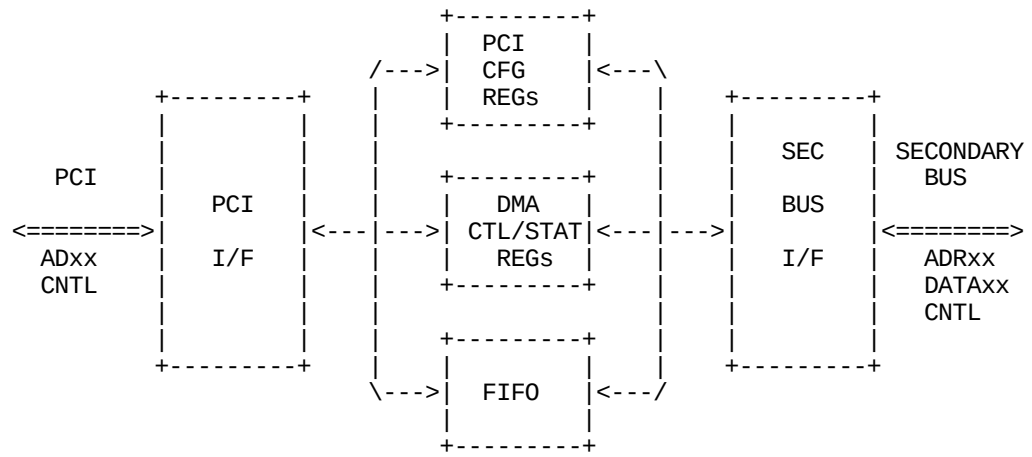
The PCI Interface ASIC provides the following features:

- PCI Bus interface
  - Meets PCI Local Bus Specification, Rev. 2.0 bus pinout/driver requirements
  - PCI Slave: access to secondary bus, registers, or configuration area;
  - PCI Master: under internal DMA control only (PCI Bus is not directly accessible from the secondary bus)
- Secondary Bus interface
  - 68040-like bus pinout/drive requirements
    - supports Motorola 68EC040 microprocessor
    - supports P1394 Link Layer Interface Controller
  - Secondary Bus Master: controlled by PCI Slave or internal DMA machine
  - Secondary Bus Slave: access to internal DMA and PCI Configuration registers

- Auxilary Functions
  - Secondary bus arbitration
  - Secondary bus external pull-down resistors provide power up configuration data
  - Test functions (ASIC OE, Open pin detect, Test Mux)

4.1 OVERVIEW

A block diagram of the PCI Interface ASIC is shown below. The major functional sections are described below:



PCI ASIC BLOCK DIAGRAM

4.1.1 PCI INTERFACE

The PCI slave interface provides access to the ASIC internal registers as well as providing master access to the secondary bus. The PCI interface supports PCI Configuration commands, PCI Memory commands, and PCI I/O commands.

The ASIC is a PCI master only when acting under internal DMA machine control. The internal DMA machine can be accessed from either the PCI or the Secondary buses.

4.1.2 SECONDARY INTERFACE

The Secondary bus interface provides an 68040-like bus to provide connectivity to the P1394 Link Layer Controller, or other 68040-like resources.

4.1.3 DMA MACHINE

The internal DMA machine provides a simple DMA mechanism for high-speed transfer of blocks of data between the PCI interface and the Secondary bus. The DMA machine transfers only DWORDs that are DWORD aligned. Dedicated PCI Address and Secondary Address registers provide source and destination addresses for the DMA transfers. The Secondary address may optionally not increment. Completion interrupts may be optionally provided to either the PCI bus or locally to the Secondary logic.

4.1.4 OPEN PIN DETECT

The PCI ASIC provides a board-level testability feature to verify that almost all I/O pins can be easily tested for proper connectivity to the PWB assembly. After power reset, the TESTOUT pin outputs the AND of all tested I/O pins; and all these I/O pins have internal pull-up current sources. This allows each connecting etch to be forced low individually, and the response verified by observing the TESTOUT pin, thus verifying connectivity.

This logic is also used for the ASIC Vih/Vil testing.

4.2 PIN DESCRIPTIONS

See 5.1 for pin assignments.

4.2.1 PCI LOCAL BUS SIGNALS

Signature	Type	Description
AD(31:0)	I/O	Multiplexed Address/Data Bus
C/BE(3:0)-	I/O	Multiplexed Command/Byte Enable
PAR	I/O	Parity
FRAME-	I/O	FRAME indicates duration of a bus transaction
TRDY-	I/O	Target Ready

IRDY-	I/O	Initiator Ready
STOP-	I/O	Target requests the Master to stop
DEVSEL-	I/O	Device Select
IDSEL-	input	Initialization Device Select
PERR-	I/O	Parity Error detected
SERR-	I/O	System Error detected
REQ-	output	PCI Bus Request
GNT-	input	PCI Bus Grant
PCI_CLK	input	PCI clock
PCI_RST-	input	PCI Reset

4.2.2 CONTROLLER INTERFACE SIGNALS

Signature	Type	Description
CADR(31:0)	I/O	Address Bus
CDATA(31:0)	I/O	Data Bus
TS-	I/O	Transfer Start
TA-	I/O	Transfer Acknowledge
READ	I/O	Read (!write)
NMI-	output	Non-Maskable Interrupt
IRQ-	output	Interrupt request
CS-	input	ASIC chip select

4.2.3 OTHER LOGIC SIGNALS

Signature	Type	Description

4.4.11 Command Register (CMD - >48)

The Command Register provides the control information for the DMA state machine. Bits in this register control starting the DMA state machine, determining completion status (DMA state machine has returned to the idle state), and controlling the operations executed by this machine. The operations controlled by this register include:

- select either read or write operation
- start the DMA state machine
- transfer count
- address increment option
- perform data transfer
- perform error correction
- perform a ROM write operation

Reset state is >0000 0000.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMD >48	DMA TRANSFER COUNT (DWORD TRANSFER COUNT)								0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	CLR FIFO	INC LOC ADR	WRT	OP CMPT	STRT / BUSY

Bit Definitions

START/BUSY - write of 1 starts DMA state machine
- reads status of DMA state machine busy
(1 = busy, 0 = not busy)

OPERATION COMPLETE - state machine sets to 1 when it returns to idle
(read only -- reset in interrupt status register)

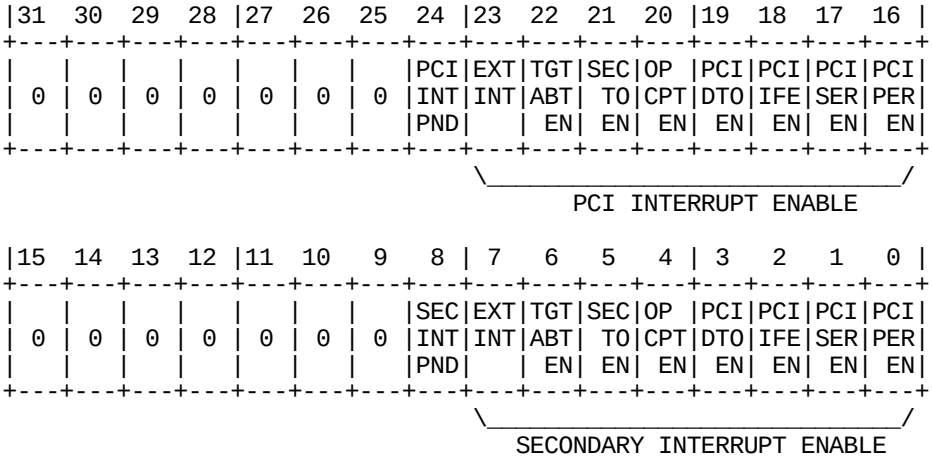
WRITE - 0 sets DMA data transfer from PCI to Secondary bus
- 1 sets DMA data transfer from Secondary to PCI bus

INCREMENT LOCAL ADDRESS - 0 selects no increment for local (secondary) address
1 selects increment for local (secondary) address

CLEAR FIFO - 1 clears datapath/FIFO (always reads as 0)
- 0 does not clear datapath

4.4.8 Interrupt Enable Register (IEN - >4C)

Sixteen bit read/write register accessed by the operating firmware to enable and disable selected interrupts. Reset state is >0000 0000. (See IST register for bit definition).



1 = interrupt enable
0 = interrupt not enabled

4.4.9 Interrupt Status Register (IST - >50)

This read/write register normally set by various interrupt generating sources. The operating firmware can access this register to determine the source(s) of an interrupt. Reset state is >0000 0000.

This register is not changed by a read access.

A write access to this register clears the bits corresponding to a "1" when the interrupting source is no longer active.

Interrupt sources and register bit definitions are:
 bit 0 - Any PCI data parity error detected
 bit 1 - PCI System Error (SERR Driven)
 bit 2 - Interface Error (PCI slave cycle - PCI address/Byte enable error)
         (or Secondary TA error - secondary timeout)
 bit 3 - PCI Device Select Timeout (DEVSEL_TO) (master cycles only)
 bit 4 - Op complete
 bit 5 - Secondary Bus Timeout (master or slave)
 bit 6 - Target Abort (master cycles only)
 bit 7 - External interrupt
 bit 8 - Local (Secondary) bus interrupt pending (read only)
 bit 9 - PCI Interrupt pending (read only)

An interrupt condition is set when:

```
           INT(set) = (Parity Error * Parity Error Enable)
                                    +
                      (System Error * System Error Enable)
                                    +
                         (I/F Error * I/F Error Enable)
                                    +
    (PCI Device Select Timeout * PCI Device Select Timeout Enable)
                                    +
                       (Op Complete * Op Complete Enable)
                                    +
        (Secondary Bus Timeout * Secondary Bus Timeout Enable)
                                    +
                      (Target Abort * Target Abort Enable)
                                    +
           (External Interrupt * External Interrupt Enable)
```

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IST >50	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	PCI INT PND	SEC INT PND	EXT INT	TGT ABT	SEC TO	OP CPT	PCI DEV TO	PCI IF ERR	PCI SER	PCI PER

4.4.12 Test Functions Register (TST - >54)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TST >54	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TEST OUTPUT				TST	TST	TST	DIS	DIS				TST	TST	TST	TST	FRC

SELECT (3:0)	MUX OUT	FI FO	PA CTR	PU	SEC TO	0	0	LAT TMR	CMD	SEC ADR	PCI ADR	IST

Bit Definitions

Force Interrupt/Status Reg - 0 (reset)
- 1 Interrupt/Status Reg test mode

Test PCI Address Reg - 0 (reset)
- 1 PCI Address Reg test mode

Test Secondary Address Reg - 0 (reset)
- 1 Secondary Address Reg test mode

Test Command Register - 0 (reset)
- 1 forces command reg test mode

Test Latency Timer TO - 0 (reset)
- 1 Latency timer test mode

Disable Secondary Timeout - 0 (reset)
- 1 disable secondary bus timeout

Test Mux output (read test mux output -- read only)

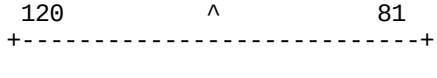
Test output select(3:0) - selects various internal nodes for viewing on external TESTOUT pin for debug purposes

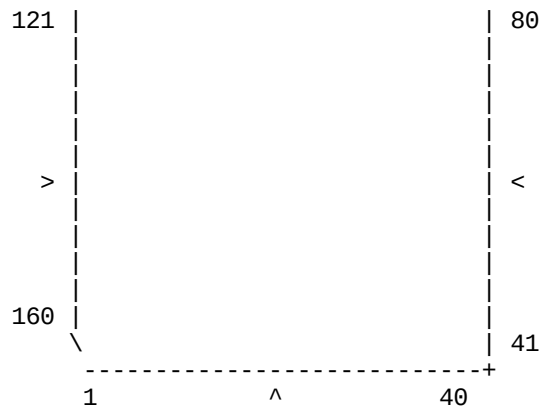
0 0 0 0	I/O pin test (AND chain) output (reset)
0 0 0 1	PSLV_BSY
0 0 1 0	PSLV_DATA
0 0 1 1	PSLV_XFR
0 1 0 0	PSLV_RDY
0 1 0 1	DMA_BUSY
0 1 1 0	DMA_XFR
0 1 1 1	DMA_XFR
1 0 0 0	PCI_XFR
1 0 0 1	PMST_ADDR
1 0 1 0	PMST_DATA
1 0 1 1	FIFOMPTY
1 1 0 0	FIFOFULL
1 1 0 1	FINRDY
1 1 1 0	FOUTRDY
1 1 1 1	P56_in (GPIN - spare input on pin 56)

5.0 ELECTRICAL SPECIFICATIONS

5.1 PIN DESCRIPTIONS

ASIC package is 160 pin PQFP. See TGC1000 Series Data Sheet for physical pin locations and mechanical data.





PIN NO.	SIGNATURE		
1	VCC1		
2	CBE(3)	I/O	
3	IDSEL	IN	
4	AD(23)	I/O	
5	GND1	STD GND	
6	AD(22)	I/O	
7	AD(21)	I/O	
8	AD(20)	I/O	
9	GND2		
10	AD(19)	I/O	
11	VCC2	STD VCC	
12	AD(18)	I/O	
13	AD(17)	I/O	
14	AD(16)	I/O	
15	VCC3		
16	CBE(2)	I/O	
17	GND3	STD GND	
18	FRAMEz	I/O	
19	IRDYz	I/O	
20	TRDYz	I/O	<---
21	GND4		
22	DEVSELz	I/O	
23	VCC4	STD VCC	
24	STOPz	I/O	
25	LOCKz	I/O	
26	PERRz	I/O	
27	SERRz	I/O	(out, open-drain)
28	PAR	I/O	
29	GND5	STD GND	
30	CBE(1)	I/O	
31	AD(15)	I/O	
32	AD(14)	I/O	
33	AD(13)	I/O	
34	AD(12)	I/O	
35	VCC5	STD VCC	
36	AD(11)	I/O	
37	AD(10)	I/O	
38	GND6		
39	AD(9)	I/O	
40	AD(8)	I/O	_____

41	VCC6	
42	CBE(0)	I/O
43	AD(7)	I/O
44	AD(6)	I/O
45	GND7	STD GND
46	AD(5)	I/O
47	AD(4)	I/O
48	AD(3)	I/O
49	GND8	
50	AD(2)	I/O
51	VCC7	STD VCC
52	AD(1)	I/O
53	AD(0)	I/O
54	IPL0z	I/O (out)
55	PCIF_MSTRz	I/O (out)
56	CSELz	IN
57	GND9	STD GND
58	EXTINTz	IN
59	VCC8	
60	SA(18)	I/O <---
61	SA(17)	I/O
62	SA(16)	I/O
63	VCC9	STD GND
64	SA(15)	I/O
65	GND10	
66	SA(14)	I/O
67	SA(13)	I/O
68	SA(12)	I/O
69	GND11	STD GND
70	SA(11)	I/O
71	SA(10)	I/O
72	RSTOUTz	I/O (out)
73	CLKSEL	IN
74	SD(0)	I/O
75	VCC10	STD VCC
76	SCLK	I/O (determined by CLKSEL)
77	GND12	
78	SD(1)	I/O
79	SD(2)	I/O
80	SD(3)	I/O _____
81	VCC11	
82	SD(4)	I/O
83	SD(5)	I/O
84	SD(6)	I/O
85	GND13	STD GND
86	SD(7)	I/O
87	SD(8)	I/O
88	SD(9)	I/O
89	SD(10)	I/O
90	SD(11)	I/O
91	VCC12	STD VCC
92	SD(12)	I/O
93	GND14	
94	SD(13)	I/O
95	SD(14)	I/O
96	SD(15)	I/O
97	GND15	STD GND
98	SD(16)	I/O
99	VCC13	

100	SD(17)	I/O	<---
101	SD(18)	I/O	
102	SD(19)	I/O	
103	VCC14	STD VCC	
104	SD(20)	I/O	
105	GND16		
106	SD(21)	I/O	
107	SD(22)	I/O	
108	SD(23)	I/O	
109	GND17	STD GND	
110	SD(24)	I/O	
111	SD(25)	I/O	
112	SD(26)	I/O	
113	SD(27)	I/O	
114	SD(28)	I/O	
115	VCC15	STD VCC	
116	SD(29)	I/O	
117	SD(30)	I/O	
118	GND18		
119	SD(31)	I/O	
120	SA(9)	I/O	_____
121	VCC16		
122	SA(8)	I/O	
123	SA(7)	I/O	
124	SA(6)	I/O	
125	GND19	STD GND	
126	SA(5)	I/O	
127	SA(4)	I/O	
128	GND20		
129	SA(3)	I/O	
130	VCC17	STD VCC	
131	SA(2)	I/O	
132	SBGz	I/O (out)	
133	SBRz	IN	
134	VCC18		
135	SBBz	I/O	
136	STEAz	I/O (out)	
137	GND21	STD GND	
138	STAz	I/O	
139	STSz	I/O	
140	SWRz	I/O	<---
141	TESTOUT	OUT	(AND tree chain end)
142	TESTOEz	IN	(AND tree chain begin)
143	VCC19	STD VCC	
144	PCICLK	IN	
145	GND22		
146	RESETz	IN	
147	INTAz	I/O (out, open-drain)	
148	PCIREQz	I/O (out)	
149	GND23	STD GND	
150	PCIGNTz	IN	
151	AD(31)	I/O	
152	AD(30)	I/O	
153	AD(29)	I/O	
154	AD(28)	I/O	
155	VCC20	STD VCC	
156	AD(27)	I/O	
157	AD(26)	I/O	
158	GND24		

159	AD(25)	I/O	
160	AD(24)	I/O	_____

TGC1000 PIN SUMMARY

GND	24 pins
VCC	20 pins
SIGNAL	116 pins
TOTAL	160 pins

IEEE 1394 TSBKPCI12C01A Card Assy # 9792377

BILL OF MATERIALS 5/06/96 ***PRELIMINARY - SUBJECT TO CHANGE WITHOUT NOTICE!***

PART DESCRIPTION	SUPPLIER	PART NUMBER	PKG TYPE	QTY	REFERENCE DESIGNATOR
DIODE, 1N5820	MOTOROLA	1N5820RL	pth700	1	CR1
RES, 15, 5%	KOA	RM73B2BT150J	1206	1	R47
RES, 56.2, 1%	KOA	RK73H2BT56R2	1206	12	R3 R4 R8 R9 R10 R16 R21 R22 R23
					R48 R49 R50
RES, 220, 5%	KOA	RM73B2BT221J	1206	7	R13 R19 R66 R67 R69 R99 R101
RES, 4.7K, 5%	KOA	RM73B2BT472J	1206	25	R6 R14 R15 R18 R38 R39 R41 R42 R37
					R43 R44 R45 R46 R51 R52 R53 R72
					R82 R94 R95 R96 R97 R98 R100 R102
RES, 0, n/a	KOA	RM73Z2BT	1206	23	R11 R12 R31 R32 R58 R60 R76 R77
					R78 R79 R87 R89
					C35 C36 C37 C44 C45 C54 C55 C56
					C57 C62 C63
RES, 1.0M, 5%	KOA	RM73B2BT105J	1206	1	R83
RES, 6.34K, 0.5%	KOA	RK73H2BT6341D	1206	1	R24
RES, 390K, 5%	KOA	RM73B2BT394J	1206	1	R5
CAP, 0.01, 10%	KEMET	C1206C103K5RAC	1206	25	C1 C5 C6 C7 C10 C11 C12 C14 C19
					C24 C27 C28 C29 C31 C34 C39 C40
					C46 C47 C48 C50 C51 C59 C60 C65
CAP, 1000PF, 10%	KEMET	C1206C102K5GAC	1206	1	C33
CAP, 47, 20%	KEMET	T491D476M010AS	2816	4	C13 C20 C66 C68
CAP, 1.5uF, 50V	KEMET	T491C155M050AS	2313	2	C2 C16
CAP, 22uF, 25V	AVX	TAJD226M025R	2816	2	C8 C9
RES, 5.1K, 5%	KOA	RM73B2BT512J	1206	3	R7 R20 R65
TL783CKC	TI	TL783CKC	pth-to220	1	U4
FUSE, 1.5A	RayChem	SMD150-2	2816	1	F1A
CAP, 0.1, 10%	KEMET	C1206C104K5RAC	1206	17	C3 C4 C17 C21 C22 C26 C32 C38 C41
					C42 C43 C52 C53 C58 C61 C64 C67
CAP, 0.22, 10	AVX	12063C224KAT4A	1206	1	C23
LLC-ASIC (TSB12C01A)	TI-SC	TSB12C01A	tqfp100	1	U23
XTAL, 24.576MHZ	FOX	FE 24.576 20PF	pth	1	Y1
PCIF-ASIC(CF64174PCM)	TI-SC	CF64174PCM	qfp160	1	U22
1394 R/A Flat Header	Molex	53462-0611	pth-6pin	3	PORT1 PORT2 PORT3
22V10,10NS (TSDLY 2424-1)	TI-SC	PALCE22V10H-10JC/5	plcc28	1	U19
TSB11C01DL	TI-SC	TSB11C01DL	ssop56	1	U24
RES, 560, 5%	KOA	RM73B2BT561J	1206	1	R25
RES, 10K, 5%	KOA	RM73B2BT103J	1206	5	R17 R27 R68 R70 R71
RES, 100, 1%	KOA	RK73H2BT1000F	1206	2	R1 R26
CAP, 12PF, 10%	KEMET	C1206C120K5GAC	1206	2	C18 C25
16V8, 5ns (IDSEL 2422-1)	AMD	PALCE16V8H-5JC/5	plcc20	1	U25
270PF, 5%	KEMET	C1206C271J5GAC	1206	3	C15 C30 C49
RES, 294, 1%	KOA	RK73H2BT2940F	1206	1	R2
PCI BRACKET	GLOBE	PCI BRACKET	spec.	1	
HEX HEAD SCREW	MEDALIST	SEMS, 4-40 X 1/4		2	