- **Supports Provisions of IEEE 1394-1995 Standard† for High Performance Serial Bus and 1394.A**
- **1394.A Support Includes: Arbitrated Short Reset, Multispeed Concatenation, Ack Accelerated Arbitration, Programmable Port Disable, PHY IDs Do Not Increment Past 63**
- **Compliant with the IEEE 1394 Open Host Controller Interface (OHCI) Specification**
- **Provides Three Fully Compliant Cable Ports at 100/200/400 Megabits per Second (Mbit/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Device Power-Down Feature to Conserve Energy in Battery Powered Applications**
- **Inactive Ports Disabled to Save Power**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Single 3.3-V Supply Operation**
- **Interface to Link-Layer Controller Supports Optional Annex J Electrical Isolation and TI™ Bus-Holder Isolation**
- **Data Interface to Link-Layer Controller Through 2/4/8 Parallel Lines at 50 MHz**
- **25-MHz Crystal Oscillator and PLL Provide Transmit/Receive Data at 100/200/400 Mbits/s, and Link-Layer Controller Clock at 50 MHz**
- **Interoperable with 1394 Link-Layer Controllers Using 5-V Supplies**
- **Interoperable Across 1394 Cable with Physical Layers (PHY) Using 5-V Supplies**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Separate Cable Bias and Driver Termination Voltage Supply for Each Port**
- **Cable Connection Debounce**
- **High Performance 80-Pin TQFP (PFP) Thermally Enhanced Package**
- **Register Bits Give Software Control of Contender Bit, Power Class Bits, Link Active Bit and 1394.A Features**

PRODUCT PREVIEW

description

The TSB41LV03 provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41LV03 is designed to interface with a link-layer controller (LLC), such as the TSB12LV22, TSB12LV21A, TSB12LV31, TSB12LV41, or TSB12C01A. The TSB41LV03 requires an external 24.576-MHz crystal or crystal oscillator. An internal crystal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information. A 49.152-MHz clock signal is supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

The TSB41LV03 supports an optional isolation barrier between itself and its LLC. When the $\overline{\text{ISO}}$ input terminal is tied high, the LLC interface outputs behave normally. When the $\overline{\text{ISO}}$ terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in IEEE 1394-1995 Annex J. To operate with TI Bus-Holder isolation, the $\overline{\text{ISO}}$ terminal must be tied high.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE 1394-1995 Standard
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description (continued)

Data bits to be transmitted through the cable ports are received from the LLC on two, four or eight parallel paths (depending on the requested transmission speed) and are latched internally in the TSB41LV03 in synchronization with the 49.152 MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304 Mbit/s, 196.608 Mbit/s, or 393.216 Mbit/s as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two-, four- or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152 MHz system clock and sent to the associated LLC. The received data is also transmitted (repeated) on the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable connection status. The cable connection status signal is internally debounced in the TSB41LV03 and is used to initiate a bus-reset.

The TSB41LV03 provides a 1.86-V nominal bias voltage at the TPBIAS terminal for driver load termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceiver chips operating from either 5-V nominal supplies or 3-V nominal supplies. This bias voltage source must be stabilized by an external filter capacitor of approximately 1 μF.

The line drivers in the TSB41LV03 operate in a high-impedance current mode, and are designed to work with external 110-Ω line-termination resistor networks. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 55-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted pair A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 250 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. The driver output current, along with other internal operating currents, is set by an external resistor connected between the R0 and R1 terminals. This current setting resistor has a value of 6.3 kΩ, ±0.5%.

The port transmitter and receiver circuitry is disabled during power-down (when the PD input terminal is asserted high), during reset (when the $\overline{\text{RESET}}$ input terminal is asserted low), when no active cable is connected to the port, or as controlled by the internal arbitration logic. The port twisted-pair bias voltage circuitry is disabled during power-down, during reset, or when the port is disabled as commanded by the LLC.

If the power supply of the TSB41LV03 is removed while the twisted pair cables are connected, then the TSB41LV03 transmitter and receiver circuitry present a high impedance to the cable and do not load the TPBIAS voltage at the other end of the cable.

If the TSB41LV03 is being used with one or more of the ports not being brought out to a connector, the twisted-pair terminals must be terminated for reliable operation. For each unused port, the TPB+ and TPB– terminals must be pulled to ground, thus disabling the port. The TPA+, TPA–, and TPBIAS terminals of an unused port may be left unconnected.

description (continued)

The TESTM, SE and SM terminals are used to set-up various manufacturing test conditions. For normal operation, the TESTM terminal should be connected to V_{CC}, and the SE and SM terminals should be connected to ground.

Four package terminals are used as inputs to set the default value for four configuration status bits in the self-identification (SelfID) packet. These terminals are hardwired high or low as a function of the equipment design. The PC0 – PC2 terminals are used to indicate the power-class status for the node (the need for power from the cable or the ability to supply power to the cable). The C/LKON terminal is used as an input to indicate whether the node is a contender for bus manager. The C input corresponds to the c field (bit 20) in the SelfID packet, and PC0 – PC2 inputs correspond to the pwr field (bits 21, 22 and 23, respectively). See Table 4-29 of the IEEE 1394-1995 standard for additional details.

The PD (power-down) terminal is provided to allow a low power mode where most of the TSB41LV03 circuits are disabled to conserve energy in battery-powered applications. When the device is powered-down it does not act as a repeater.

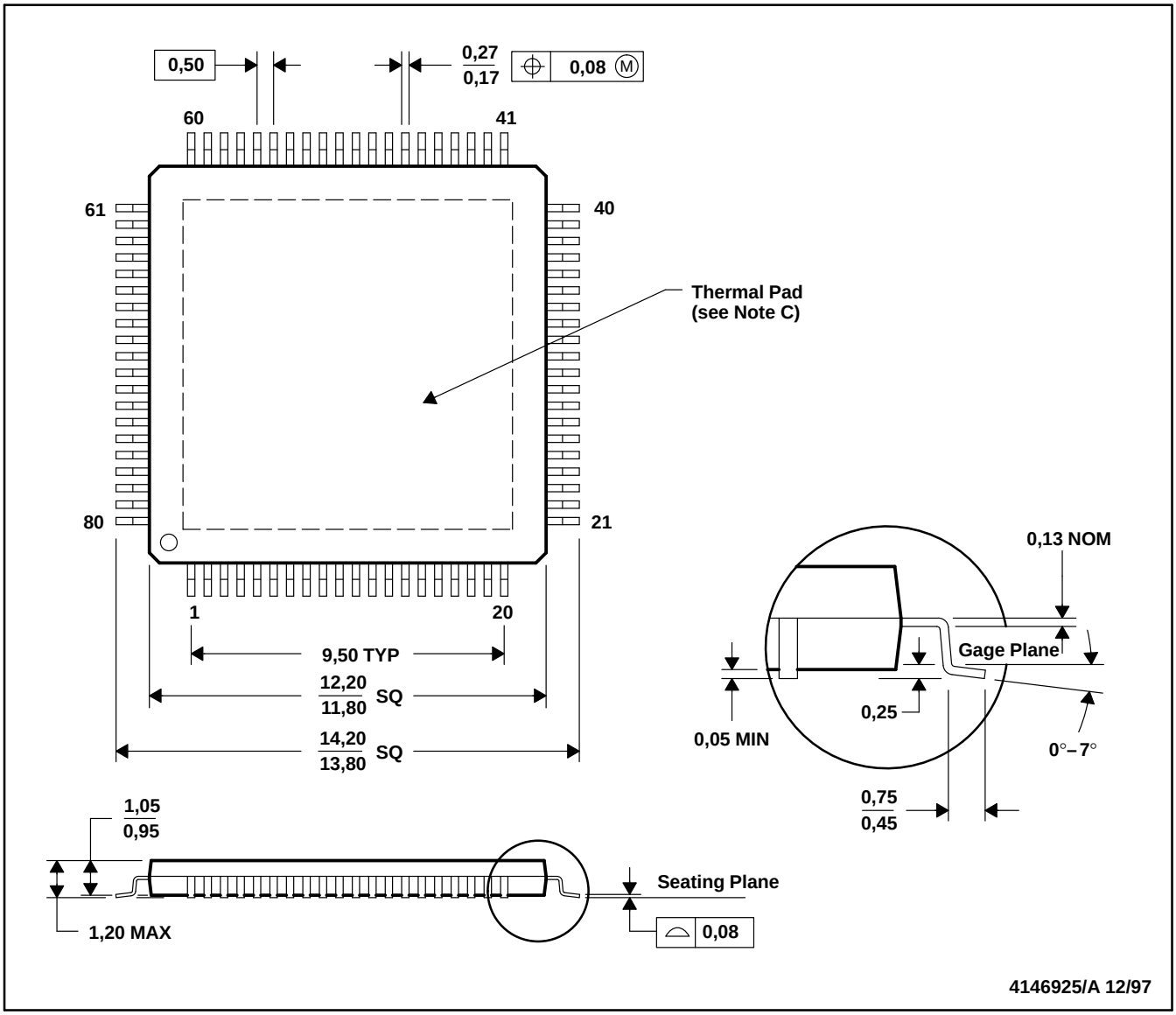
The CNA (cable-not-active) terminal provides a high output when all twisted-pair cable ports are disconnected, and can be used to determine when to power-down the TSB41LV03. The CNA output is not debounced. In power-down mode, the CNA detection circuitry remains enabled.

The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC indicates to the PHY that the LLC is powered up and active. During LLC power-down mode, as indicated by the LPS input being low for more than 2.56 μs, the TSB41LV03 deactivates the PHY-LLC interface to save power. The TSB41LV03 continues the necessary repeater function required for network operation during this power-down state.

If the PHY receives a link-on packet from another node, the C/LKON terminal is activated to output a 6.114-MHz signal. This LKON signal can be used by circuitry that recognizes it and reactivates the powered-down LLC. After power-up of the LLC, the LLC notifies the PHY of the power-on status by way of the LPS terminal. The PHY confirms notification by deactivating the 6.114-MHz signal on the C/LKON terminal, then enables the PHY-link interface.

MECHANICAL INFORMATION

PFP (S-PQFP-G80) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This solderable pad is electrically and thermally connected to the backside of the die and possiblly selected leads.

PRODUCT PREVIEW

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