For:dbrune
Printed on:Fri, Jun 28, 1996 19:56:33
From book:SLLS180 (A) VIEW
Document:TEXT VIEW
Last saved on:Fri, Jun 28, 1996 19:56:27

ERRATA TO THE TSB11C0A DATA SHEET

(TEXAS INSTRUMENTS LITERATURE NO. SLLS167A, MARCH 1996)

ALSO INCLUDED IN

(DATA TRANSMISSION DATA BOOK, VOLUME 2, COMMUNICATIONS CONTROLLERS, SLDS003)

The following bulleted list contains corrections to the information contained in the TSB11C01 data sheet. This data sheet is also included in the Data Transmission Data Book, Volume 2, Communications Controllers beginning on page 4–3.

- The output voltage at TPBIAS (pin 36) is approximately 50 mV below the target design value. This can cause the measured TPBIAS output voltage to fall outside the specified limits when operated under the worst-case conditions of minimum supply voltage and maximum load current.

  To adjust the output voltage of TPBIAS to the specified limit, connect an external resistor of approximately 685 Ω between TPBIAS and AV_{CC} (pins 2, 3, 6, or 7).

  The nominal TPBIAS output voltage will be adjusted to the target design value on a future revision of this device.

- The TPBIAS output voltage limits have been changed to match the limits of the IEEE 1394-1995 standard. TPBIAS minimum is 1.665 V and maximum is 2.015 V.

- To ensure reliable operation when this device is the root node and is connected to a link layer controller that is the cycle master, the application must wait for a cycle-done interrupt (CyDne, bit 22 of the Interrupt register of the link layer controller [TSB12C01A]) before making a TSB11C01 register access. The register access must be completed before the next cycle start interrupt (CySt, bit 21 of the Interrupt register of the link layer controller [TSB12C01A]).

- The following changes should be made to the switching characteristics table on page 6 of the data sheet (page 4–9 in the data book).

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_h	Hold time, D, CTL, LREQ low or high after SYSCLK↑		2		ns
t_d	Delay time, SYSCLK to D, CTL		2	11	ns

- The status transfer timing diagram in Figure 6 is in error. The following diagram is the correct version.

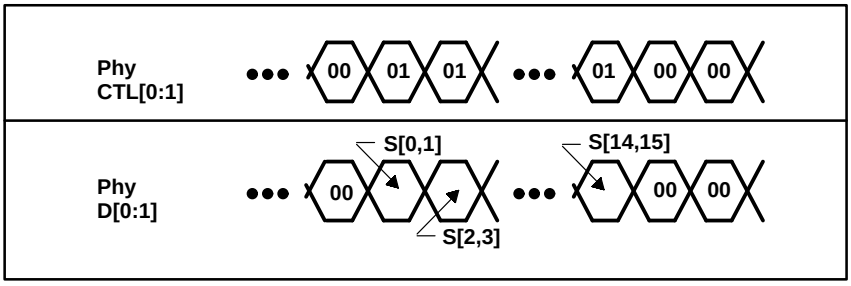

Figure 6. Status Transfer Timing

ERRATA TO THE TSB11C0A DATA SHEET

(CONTINUED)

- The bottom paragraph on page 2 of the data sheet (page 4–4 in the data book) states C/LKON outputs a 6.114 MHz signal. The correct value is exactly 1/16 of the oscillator frequency or
  (998.304 MHz ± 100 ppm)/16 = 6.144 MHz ± 100 ppm
- An interrupt status packet is not sent to the link layer controller for cable power failure. The cable power status must be polled occasionally.
- A write to the phy layer control register 1 from the link layer controller causes the register to remain in a write-enabled state. The phy layer logic does not automatically unaddress the write operation to control register 1. A subsequent phy configuration packet would be unable to change the GAP count unless control register 1 write-enable logic is unaddressed first. This can be done from the link layer controller by either reading control register 1 or performing a read or write access to any of the other registers in the phy layer.
- On page 6 of the data sheet (page 4–9 in the data book), the titles of Figures 1 and 2 should be switched to read as follows.

  Figure 1. D, CTL, LREQ Input Setup and Hold Time Waveforms

  Figure 2. D, CTL Output Delay Relative to SYSCLK Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.