1394 Design Schematic (TSBKMPEG2)

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Rev B

DRAFT

TEXAS INSTRUMENTS

1394 Solutions Leader

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Features of the TSBKMPEG2Lynx Evaluation Module

- TSB12LV41 (MPEG2Lynx) Link Layer Controller
    - Interfaces directly to Texas Instruments TSB21LV03 physical layer device on this board, able to interface directly to TSB11C03 and TSB11LV01
    - Interfaces Directly to Texas Instruments TMS320AV7000 Architecture of DSS and MPEG2 Decoders through Bulky Data Interface (BDIF) and Microprocessor/Microcontroller Interface
    - Microprocessor/Microcontroller Interface supports direct connection to Intel 8051 and Motorola 68000 architectures
    - 8K x 8bit FIFO supports MPEG2/DSS, Asynchronous, and Isochronous modes for transmit and receive
    - Supports bus functions and automatic IEEE-1394 Self-ID verification
    - Single 3.3V Supply Operation, 5V tolerance using 5V bias pins
    - High performance 100-pin PZ (S-PQFP-G100) package
- TSB21LV03 Physical Layer Device
    - Provides three fully compliant cable ports at 100/200 Mbps
    - Device Power-Down feature to conserve energy
    - Inactive ports disabled to save power
    - Logic performs system initialization and arbitration functions
    - Provides node power-class information signaling for system power management
    - cable power presence monitoring
    - Single 3.3V supply operation
    - High Performance 64-pin PM (TQFP) package
- Connectors/headers provided for;
    - MPEG2/DSS decoder through BDIF header
    - Microcontroller/Microprocessor through header
    - Other 1394 nodes through three fully compliant 1394 connectors
    - Power through 1394 cable or alternate power supply through power connector

Overview of the TSBKMPEG2Lynx Evaluation Module

The MPEG2Lynx Development Board uses TI's TSB12LV41 (MPEG2Lynx) link layer controller and TSB21LV03 (dual footprinted for TSB11C03) to create a known good node for consumer electronics product development. The TSB12LV41 enables direct connection to various microprocessors or microcontrollers, including the 80xx, 68xxx, and TMS320AV7000 architecture of set-top box devices from TI. The TSB12LV41 supports MPEG2 formatted isochronous data transfer according to IEC1883, supports timestamp offsets for MPEG2 Transmit and Receive, and performs age filtering functions.

The TSB12LV41 is able to communicate to the Microcontoller/Microprocessor and MPEG2 decoder through two separate headers on the board. One header provides the 8/16 data lines and 8 address lines for the uC/uP, and the other header provides the address, data and control lines for the MPEG2 decoder.

Hardware Abstraction Layer (HAL) software, written in ANSI C, is available for transaction layer functionality. An Application Programmer Interface is available for serial bus management functions. The API performs the necessary functions required to do 1394 operations of isochronous and asynchronous nature.

The TSBKMPEG2Lynx EVM is designed to connect to a TMS320AV7100 Development Board via a special connector (included). The TSBKMPEG2Lynx may also be used with other microcontrollers/microprocessors if a connector is built for this purpose.

TSB12LV41 / TMS320AV7100 Interconnect

	TSB12LV41			TMS320AV7100		
	Pin #	*Pin Name*	*I/O*	*Pin #*	*Pin Name*	*I/O*
1	9	BDI/O7	I/O	189	PDATA7	I/O
2	8	BDI/O6	I/O	188	PDATA6	I/O
3	7	BDI/O5	I/O	187	PDATA5	I/O
4	6	BDI/O4	I/O	184	PDATA4	I/O
5	4	BDI/O3	I/O	183	PDATA3	I/O
6	3	BDI/O2	I/O	182	PDATA2	I/O
7	2	BDI/O1	I/O	181	PDATA1	I/O
8	1	BDI/O0	I/O	180	PDATA0	I/O
9	93	BDIEN	I	194	PWRITE	O
10	49	BDOEN	I	197	PREAD	O
11	100	BDIF2	I/O	192	PPACEN	I/O
12	30	BDOAVAIL	O	191	PREADREQ	I
13	99	BDIF1	I/O	190	PERROR	I/O
14	91	BDICLK	I	193	CLK40	O
15	16	BDOCLK	I	193	CLK40	O
16	59	ADR8	I	91	EXTADDR0	O
17	58	ADR7	I	92	EXTADDR1	O
18	56	ADR6	I	93	EXTADDR2	O
19	55	ADR5	I	94	EXTADDR3	O
20	54	ADR4	I	97	EXTADDR4	O
21	53	ADR3	I	98	EXTADDR5	O
22	52	ADR2	I	99	EXTADDR6	O
23	51	ADR1	I	100	EXTADDR7	O
24	50	ADR0	I	101	EXTADDR8	O
25	61	DATA15	I/O	90	EXTDATA0	I/O
26	63	DATA14	I/O	88	EXTDATA1	I/O
27	68	DATA13	I/O	84	EXTDATA2	I/O
28	70	DATA12	I/O	82	EXTDATA3	I/O
29	73	DATA11	I/O	80	EXTDATA4	I/O
30	75	DATA10	I/O	78	EXTDATA5	I/O

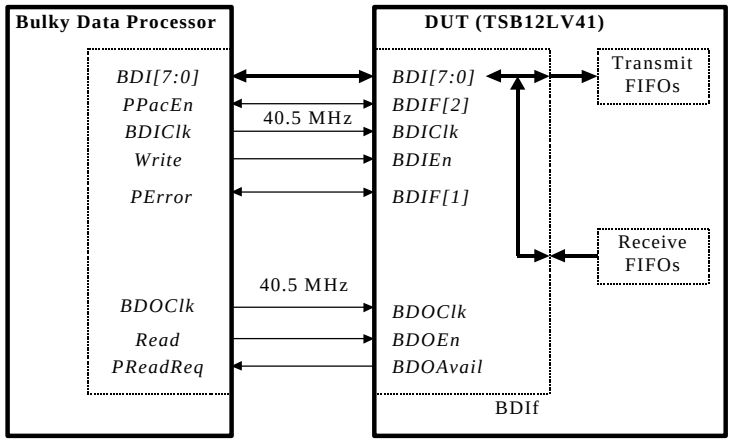
TSB12LV41 / TMS320AV7100 Interconnect

	TSB12LV41			TMS320AV7100		
31	77	DATA9	I/O	74	EXTDATA6	I/O
32	79	DATA8	I/O	72	EXTDATA7	I/O
33	62	DATA7	I/O	89	EXTDATA8	I/O
34	64	DATA6	I/O	87	EXTDATA9	I/O
35	69	DATA5	I/O	83	EXTDATA10	I/O
36	71	DATA4	I/O	81	EXTDATA11	I/O
37	74	DATA3	I/O	79	EXTDATA12	I/O
38	76	DATA2	I/O	77	EXTDATA13	I/O
39	78	DATA1	I/O	73	EXTDATA14	I/O
40	80	DATA0	I/O	71	EXTDATA15	I/O
41	86	CS1	I	156	CS5	O
42	82	MCCTL0	I	111	EXTR/W	O
43	88	RDY	O	112	EXTWAIT	I

NOTES:

1. BDIMode(2:0) in the Bulky FIFO Control register (Address “d8h” in the TSB12LV41) must be “010” to select TMS320AV7100 interface on the Bulky Data Interface port (BDIF).
2. BDIF0 (pin 98 of the TSB12LV41) should be pulled low with a 220 ohm resistor.
3. MCSEL[1:0] (pins 85 and 84 of the TSB12LV41) must be set to “00” to select the TMS320AV7100 ARM processor interface on the TSB12LV41 microcontroller interface.
4. Pin 83 (MCCTL1) of the TSB12LV41 should be pulled high with a 4.7K resistor.
5. BDI/O[7:0] are bidirectional lines. BDIEN is Write enable and BDOEN is Read enable. BDICLK max frequency is 40.5MHz and data can be wrttien/read on every other clock.
6. It is suggested that the BDI/O[7:0] signals between the TMS320AV7100 and the TSB12LV41 have pull down resistors added for the case where neither part is driving this bus.

TSB12LV41 / TMS320AV7100 Interconnect



BDIMode 010, BDOMode 00: Bi-directional DSS/MPEG data only

Table 1. Bulky Interface Control Register Description

BIT	Name	Description	Setting
0 - 7	Unused		-
8	LngRdReq	If BDIMode = 3’b010 this bit causes the bdoavail to remain active through entire packet read	0
9	BMLECtrl	MPEG Little Endien control, when set causes MPEG interface Little Endien	0
10	BILECtrl	ISO Little Endien control, when set causes ISO interface to be Little Endien	0
11	BALECtrl	ASYNC Little Endien control, when set causes ASYNC interface to be Little Endien	0
12	AHBDIBsy	Active High control for BDIBusy pin, when set causes signal to be active high	0
13	AHAvail	Active High control for BDAvail pin, when set causes signal to be active high	1
14	AHBDOEn	Active High control for BDOEn pin, when set causes signal to be active high	1
15	AHBDIEn	Active High control for BDIEn pin, when set causes signal to be active high	1
16	UniDir	If BDIMode = 2’b010 this bit causes the interface to be unidirectional	1
17	DSSRec	Active if UniDir (bit 16) is set and BDIMode = 3’b010, when set causes Write functionality to be enabled and Read functionality to be disabled	
18	AHPacEn	If BDIMode is set to 3’b010 or 3’b101, then if set causes BDIF[2] (Packet Enable) pin to be active high	1
19	AHError	If BDIMode = 3’b010 or 3’b101, then if set causes BDIF[1] (Packet Error) pin to be active high	1
20	AHBDIFmt 0	If BDIMode=3’b101, then, if set causes BDIF[0] pin (Valid) to be active high	0
21	Unused		-
22	BDOMode1	MSB of the BDOMode select bits.	0
23	BDOMode0	LSB of the BDOMode select bits.	0
24	Unused		-

25	BDIMode2	MSB of the BDIMode select bits	0
26	BDIMode1	Middle bit of the BDIMode select bits	1
27	BDIMode0	LSB of the BDIMode select bits	0
28	RcvPad	When set this allows 1394 padding bits through to the interface port	1
29	BDOInit	Self Clearing bit, when written to with a 1 causes the BDO logic to be reset.	0
30	BDIInit	Self Clearing bit, when written to with a 1 causes the BDI logic to be reset	0
31	BDOTris	When set causes the BDO data bus to be forced Tri-State	0

REVISIONS			
REV	ECN NO / CLASS / DRAFTER / DATE	DATE	APPROVED

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE II DESCRIPTION	NOTES

NEXT ASSY	USED ON
APPLICATION	

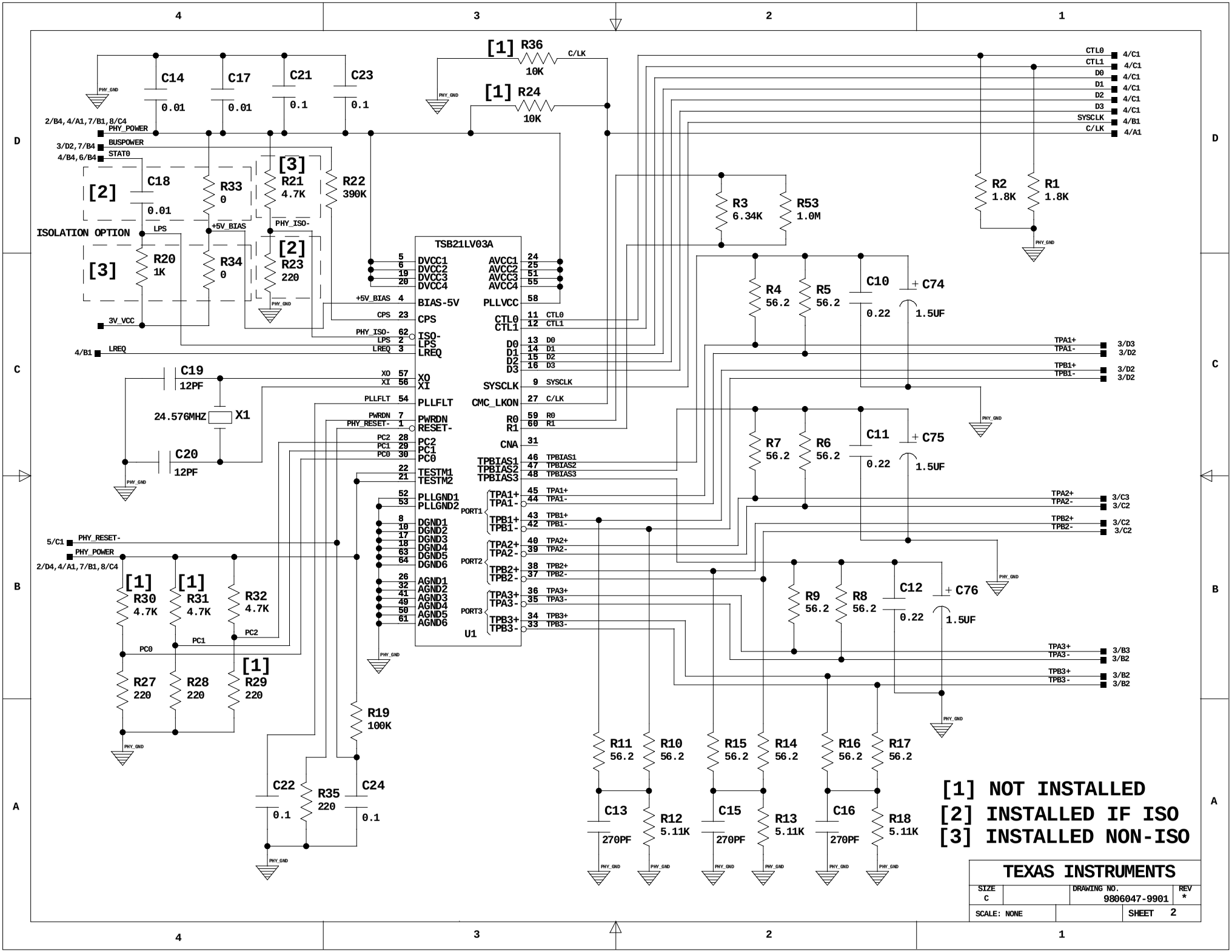
DWN	
CHK	
ENGR-DSGN	
ENGR-MGR	
QA	
MFG	
PROD SAF	
PLSE	

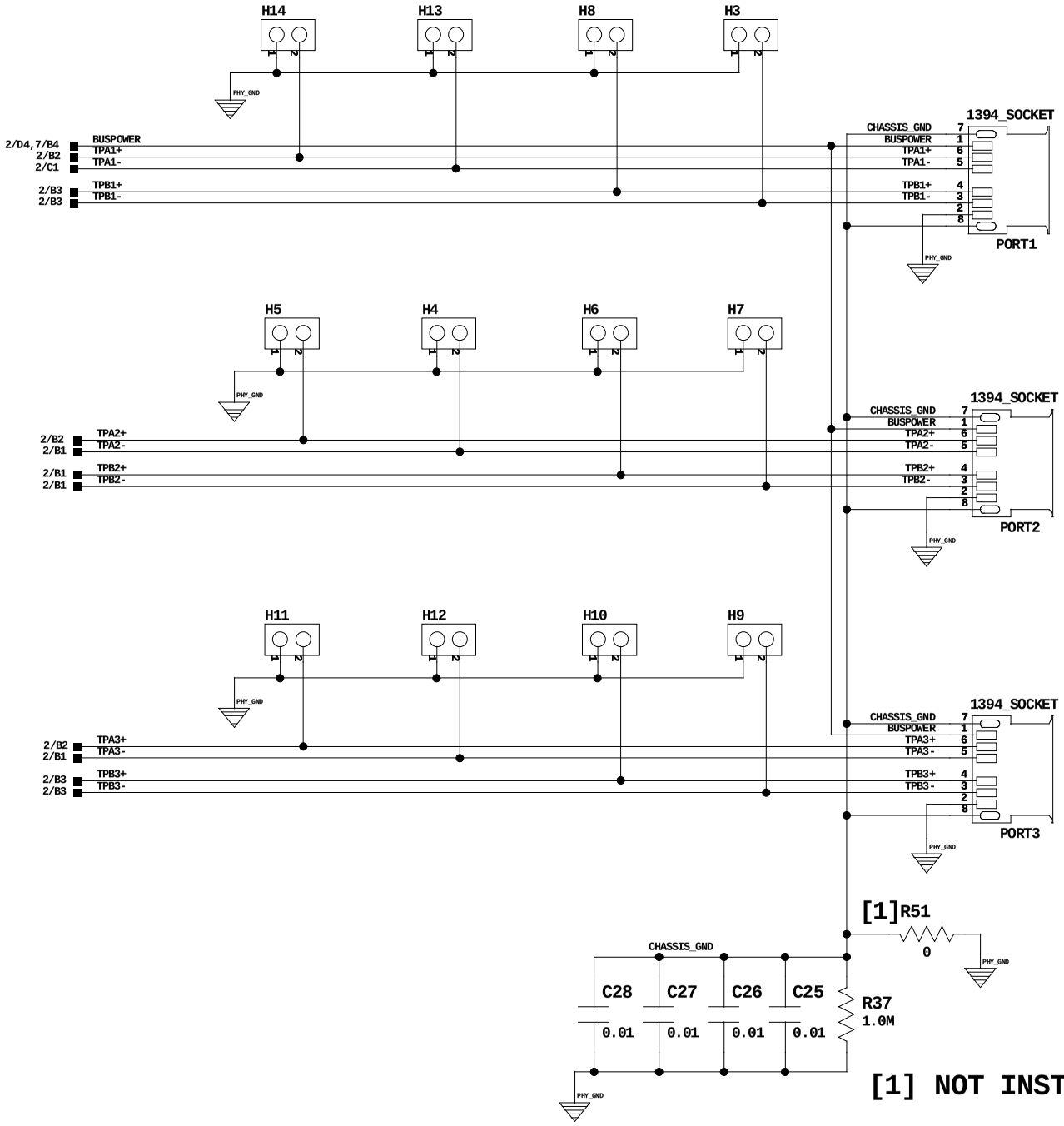
TEXAS INSTRUMENTS

LOGIC DIAGRAM

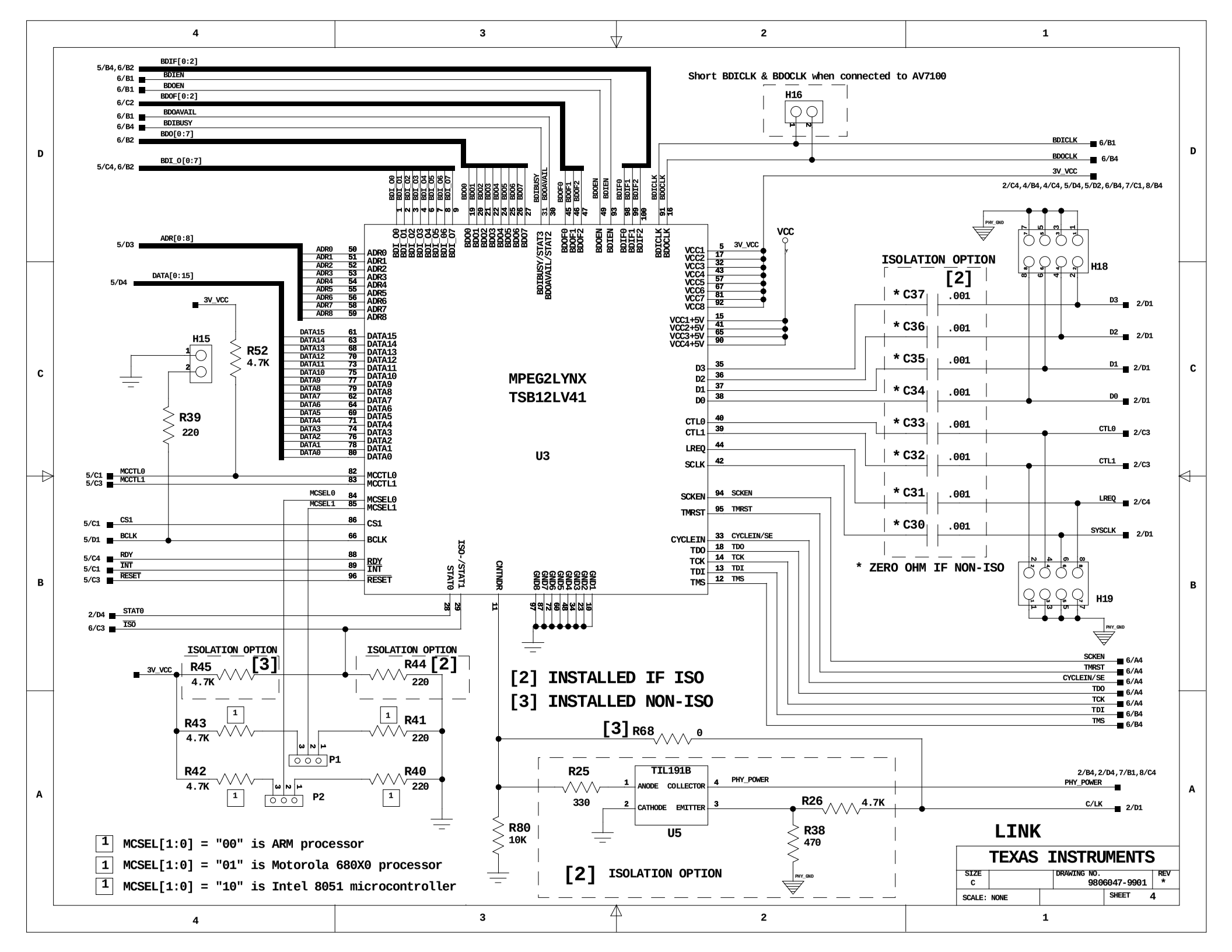
MPEG2LYNX EVAL BOARD

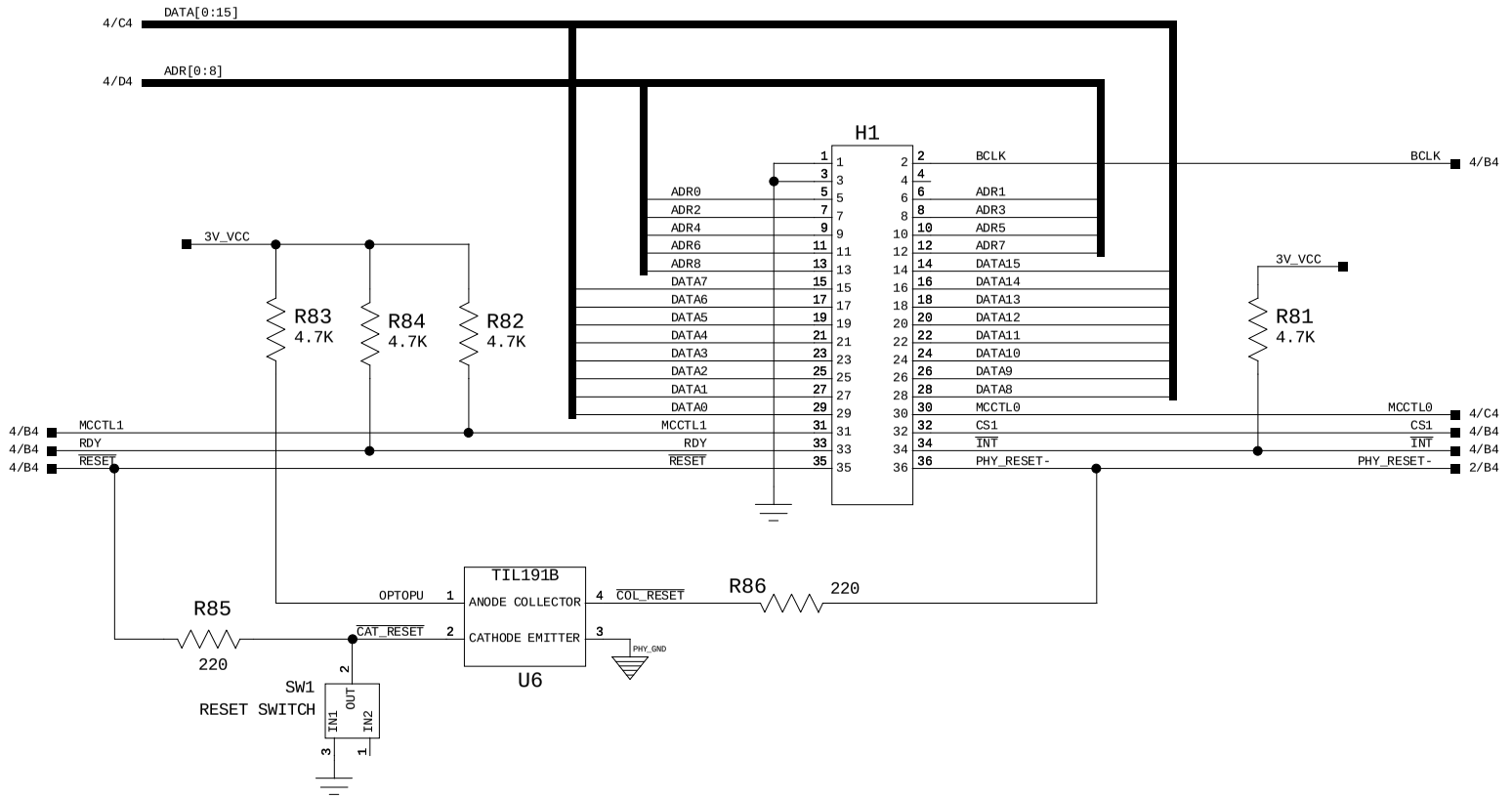
SIZE		DRAWING NO.
C		9806047-9901
SCALE:	7-1-1997_13:44	SHEET = 1 OF 8

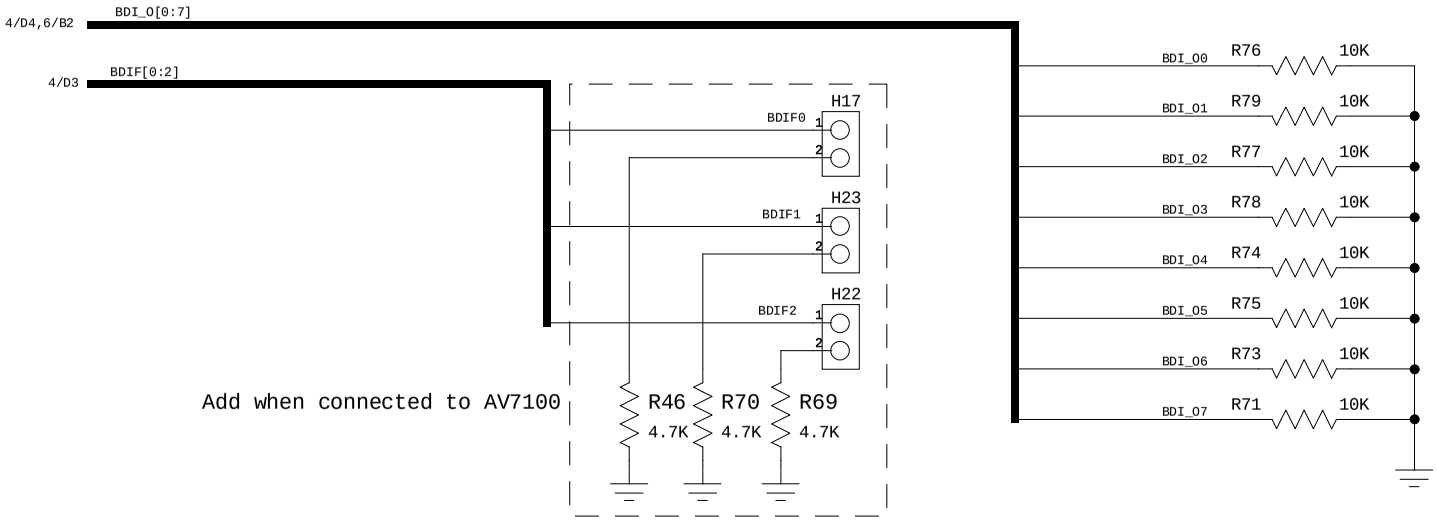

TSB21LV03A
U1
C14 0.01
C17 0.01
C21 0.1
C23 0.1
[1] R36 10K C/LK
[1] R24 10K
C18 0.01
[2]
ISOLATION OPTION
[3]
R33 0
R20 1K
R34 0
[3] R21 4.7K
R22 390K
[2] R23 220
R3 6.34K
R53 1.0M
R2 1.8K
R1 1.8K
R4 56.2
R5 56.2
C10 0.22
C74 1.5UF
R7 56.2
R6 56.2
C11 0.22
C75 1.5UF
R9 56.2
R8 56.2
C12 0.22
C76 1.5UF
C19 12PF
C20 12PF
24.576MHZ X1
R30 4.7K
R31 4.7K
R32 4.7K
R27 220
R28 220
[1] R29 220
R19 100K
C22 0.1
R35 220
C24 0.1
R11 56.2
R10 56.2
R15 56.2
R14 56.2
R16 56.2
R17 56.2
C13 270PF
R12 5.11K
C15 270PF
R13 5.11K
C16 270PF
R18 5.11K
PHY_POWER
BUSPOWER
STAT0
+5V_BIAS
3V_VCC
LPS
PHY_ISO-
LREQ
PHY_RESET-
CPS
PHY_GND
CTL0
CTL1
D0
D1
D2
D3
SYSCLK
C/LK
TPA1+
TPA1-
TPB1+
TPB1-
TPA2+
TPA2-
TPB2+
TPB2-
TPA3+
TPA3-
TPB3+
TPB3-
[1] NOT INSTALLED
[2] INSTALLED IF ISO
[3] INSTALLED NON-ISO
TEXAS INSTRUMENTS
SIZE C
DRAWING NO. 9806047-9901
REV *
SCALE: NONE
SHEET 2



TEXAS INSTRUMENTS			
SIZE C		DRAWING NO. 9806047-9901	REV *
SCALE: NONE			SHEET 3


Short BDICLK & BDOCLK when connected to AV7100
MPEG2LYNX
TSB12LV41
U3
[2] INSTALLED IF ISO
[3] INSTALLED NON-ISO
ISOLATION OPTION
[2]
[3]
* ZERO OHM IF NON-ISO
[2] ISOLATION OPTION
1 MCSEL[1:0] = "00" is ARM processor
1 MCSEL[1:0] = "01" is Motorola 680X0 processor
1 MCSEL[1:0] = "10" is Intel 8051 microcontroller
LINK
TEXAS INSTRUMENTS
SIZE C
DRAWING NO. 9806047-9901
REV *
SCALE: NONE
SHEET 4

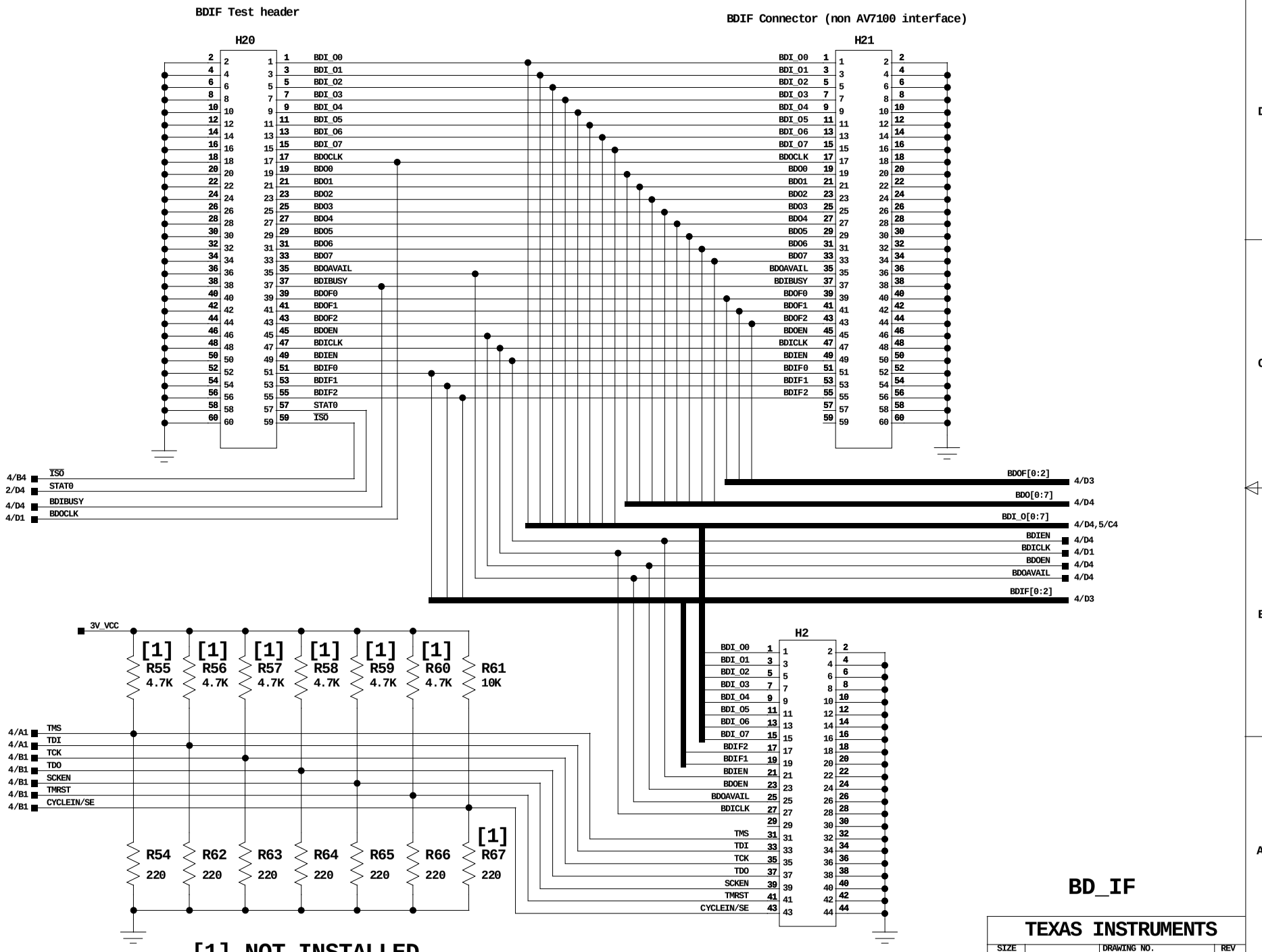


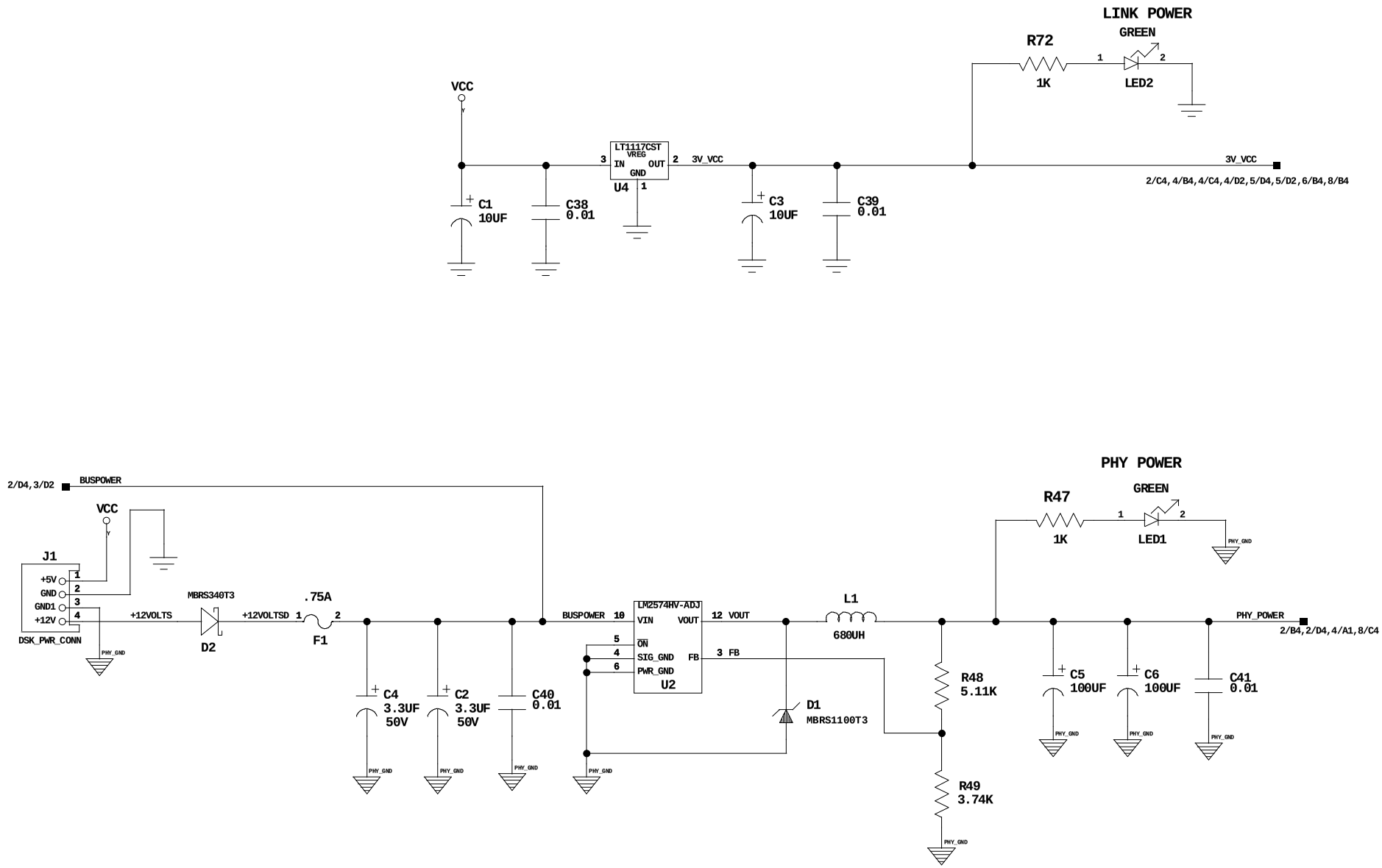


TIMON_IF

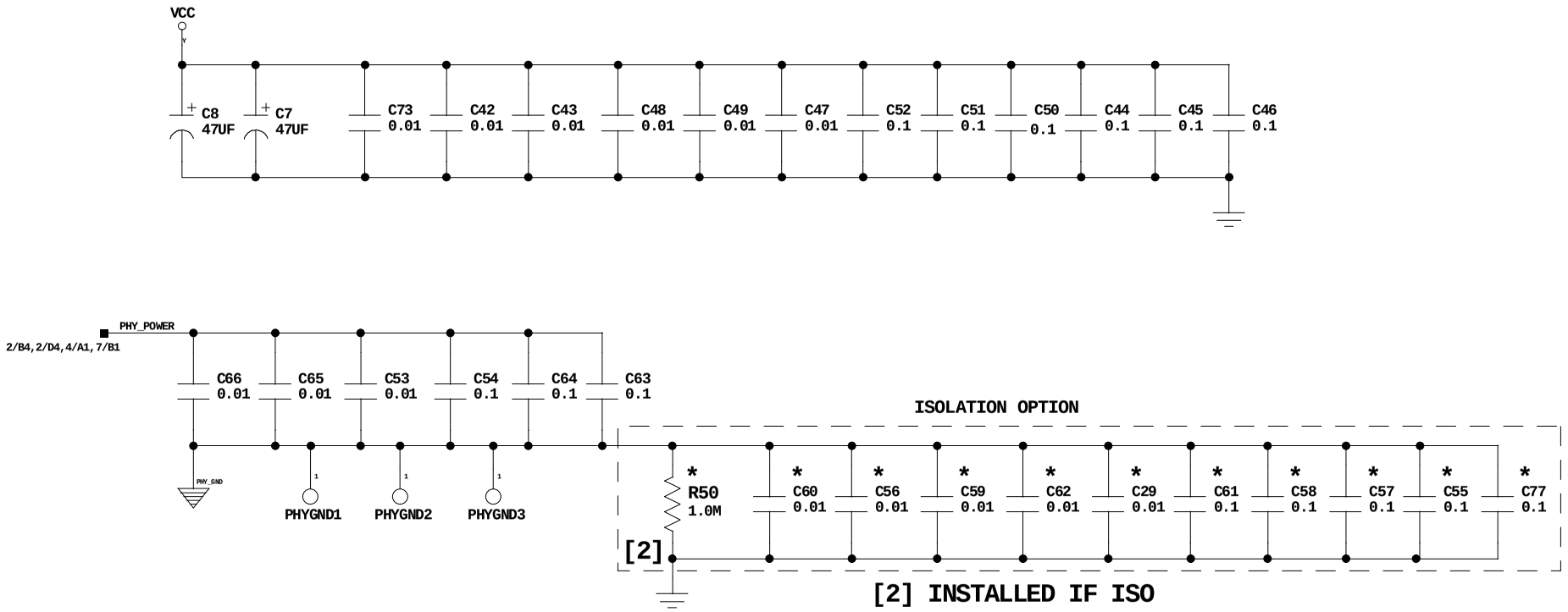
TEXAS INSTRUMENTS

SIZE		DRAWING NO.	REV
C		9806047-9901	*
SCALE: NONE			SHEET 5


BDIF Test header
H20
BDIF Connector (non AV7100 interface)
H21
BDI_00
BDI_01
BDI_02
BDI_03
BDI_04
BDI_05
BDI_06
BDI_07
BDOCLK
BDO0
BDO1
BDO2
BDO3
BDO4
BDO5
BDO6
BDO7
BDOAVAIL
BDIBUSY
BDOF0
BDOF1
BDOF2
BDOEN
BDICLK
BDIEN
BDIF0
BDIF1
BDIF2
STAT0
ISO
4/B4 ISO
2/D4 STAT0
4/D4 BDIBUSY
4/D1 BDOCLK
BDOF[0:2] 4/D3
BDO[0:7] 4/D4
BDI_O[0:7] 4/D4,5/C4
BDIEN 4/D4
BDICLK 4/D1
BDOEN 4/D4
BDOAVAIL 4/D4
BDIF[0:2] 4/D3
3V_VCC
[1] R55 4.7K
[1] R56 4.7K
[1] R57 4.7K
[1] R58 4.7K
[1] R59 4.7K
[1] R60 4.7K
R61 10K
4/A1 TMS
4/A1 TDI
4/B1 TCK
4/B1 TDO
4/B1 SCKEN
4/B1 TMRST
4/B1 CYCLEIN/SE
R54 220
R62 220
R63 220
R64 220
R65 220
R66 220
[1] R67 220
H2
[1] NOT INSTALLED
Connector for AV7100 Dev. Board 1394 Interface
BD_IF
TEXAS INSTRUMENTS
SIZE C
DRAWING NO. 9806047-9901
REV *
SCALE: NONE
SHEET 6

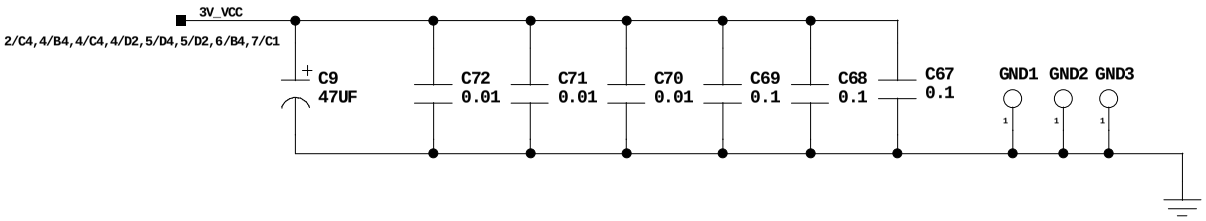


TEXAS INSTRUMENTS			
SIZE C		DRAWING NO. 9806047-9901	REV *
SCALE: NONE			SHEET 7



[2] INSTALLED IF ISO

* ZERO OHM IF NON-ISO



TEXAS INSTRUMENTS			
SIZE C		DRAWING NO. 9806047-9901	REV *
SCALE: NONE			SHEET 8