1394 Link Layer Controller chip (TSB12C01A) Errata:

Last Changed on 07/06/96 - bsh, rgg

0. Electrical isolation as described in Appendex J of IEEE 1394-1995 is not supported by the TSB12C01APZ . TI has an improved isolation technique, that is the recommended isolation solution.

1. The receiving 12C01A won't receive:
    a. a lock response with no data and an error rcode
    b. a read response with no data and an error rcode

2. There is a narrow window after the end of the transmission of a cycle start packet where making a request to send ISO data (sending an LREQ to the phy layer) will cause the phy-link I/F to hang when using the TSB11C01. A similar problem may occur if a status is sent from the phy to the link in a very narrow window just as or just after a LREQ is sent from the link to the phy. This may cause the phy/link interface to hang up in the HOLD state.

The suggested work around for both is:

a. Write the 1st iso data quadlet to ITF_First, and write quadlets 2 to (n-1) to ITF_Continue. This data is now queued up.

b. Wait for CyDne, then immediately write the final quadlet to ITF_Continue_&_Update. This final quadlet must to written before the end of the current 125 microsecond ISO period to ensure the packet will go out on the next ISO period. Be aware of how much time may be consumed by the PC servicing interrupts. If an interrupt requires too much time it should be masked out during the writes to the ITF.

c. The data will go out on the next iso cycle.

3. When receiving an acknowledge for an asynchronous packet sent at S200 and S400 data rates, the received acknowledge speed decode logic is incorrect. The TSB12C01A has no problem transmitting and receiving data packets at S200 or S400, but the acknowledge packet for an asynchronous transmit is not correctly decoded. This can result in the transmitting node not being able to receive or correctly receive an acknowledge, see #1 under Addition Information below.

4. The self_id period is currently terminated by an arbitration reset gap. It should be a subaction gap. This has not caused any known problems.

5. The receiver will always return an ack code of ack_complete to a write request that was not busied off. It correctly sends the busy ack code for a busy state on the receiving node.

6. The 12C01A can't receive 0-length iso packets.

7. The receiver does not check available space in the GRF properly when receiving self_id packets. After the GRF is full, the incoming self-ID packets are lost.

8. If there is activity on the Phy/Link interface, fast back to back writes to the transmit FIFOs of the 12C01A may cause overwriting of the previously written quadlet of data before it has been placed into the transmit FIFO. This may happen even if the host has waited until CA- was asserted before attempting another write.
The workaround is to wait a minimum of 3 BCLK cycles after CA- is asserted between each write to the ITF or ATF.

9. There is a small possibility that due to activity on both the Host/Link interface and Phy/Link interface that a FIFO contention might occur. If the final quadlet written to a transmit FIFO is confirmed exactly when a quadlet is being written from 1394 into the GRF a contention could occur. This contention could result in a data quadlet coming in the Phy/Link interface not being written into the GRF. The workaround is to write the final quadlet into the ATF or ITF when the 12C01A is not in receive mode. The suggested mechanism to do this is to wait until the GRFEMP pin is set (or bit 15 of the GRF Status register is set) before writing the final quadlet into the ATF or ITF.

TSB12C01A Data Book Errata:
1. Page 4-8 (Section 4.7 Receive Self-ID) should be replaced with the following page.

4.7 Receive Self-ID

The format of the receive self-ID packet is shown in Figure 4-10. The first quadlet is the packet header with the special tCode of Eh. The quadlets following are a concatenation of all the received self-ID packets, followed by the final packet status quadlet.

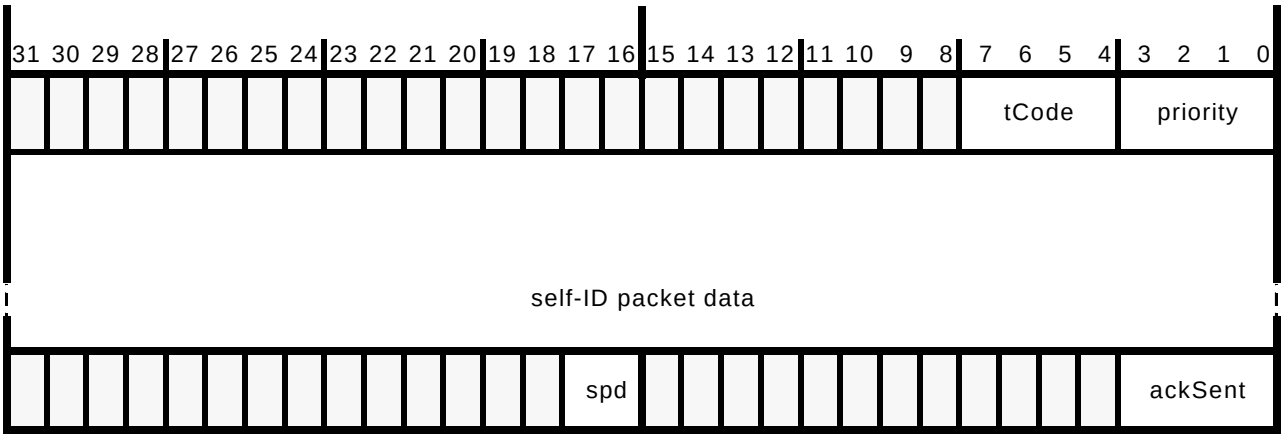

Figure 4-10. Receive Self-ID Format

Table 4-10 Receive Self-ID Functions

Field Name	**Description**
tCode	Special transaction code of 1110b
priority	The priority level for this packet.
Self-ID packet data	The concatenation of all self-ID packets recieved.
spd	This field indicates the speed at which this packet was sent. All self-id packets are sent at the base rate of 100Mbs. spd = 00 for 100 Mbs
ackSent	This field holds the acknowledge sent by the receiver for this packet.

2. Figure 2-2 TSB12C01A Terminal Functions has an error. The signal CYDNE is an active HIGH signal. The labeling of the figure should NOT have a bar over CYDNE.

Additional Information

1. Ack code = 0000b is reserved, however the TSB12C01A uses ATAck code = 0000b as “no Acknowledge received”. For example, if a Async write is addressed to a non-existant address, the 12C01A waits until timeout, then sets the ATAck (in the Node Address register) to 0000b. After the Async command is sent, the sender will read ATAck. If ATAck is equal to 0000b, it means a timeout occurred, i.e. no response from any node was received.
The recommended Async transfer procedure:
After loading the ATF with an Async. packet, the driver needs to wait until the bit TxRdy of the Interrupt register (bit 5) equals 1, which indicates the transmitter has already received an ACK or timeout. Then read ATAck from the Node address register. In order to receive the next Ack code, TxRdy needs to be then reset to 0.

2. There is a possibility of a false header error on receipt of a phy configuration packet. If the first 16 bits of a phy configuration packet (PHY config packet id + phy_ID + force_root bit flag + set gap_count flag + gap_count) happen to match a node’s destination id (Bus number + Node number) the 12C01A on that node will issue a header error since it will misinterpret the phy config packet as a data packet addressed to the node. The suggested work around is to assign bus numbers which all have the MSb = 1. Since the all ones case is reserved for addressing the local bus, this leaves only 511 available unique bus ids.
This is due to the wording of the IEEE 1394 Standard.

3. The RxDta interrupt bit is currently set whenever a data quadlet has been received by the GRF. This generates a large numbers of interrupts. In a future revision of this part this interrupt shall be changed to only occur when a complete packet has been received by the GRF.