TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

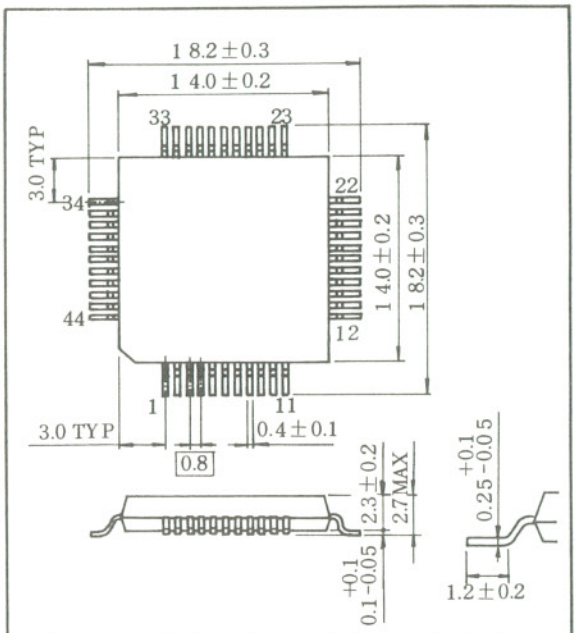
TA8512AF

TOSHIBA BIPOLAR INTEGRATED CIRCUIT

SILICON MONOLITHIC

READ/WRITE IC (For Floppy Disk Drive)

Unit in mm



Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15 mm.

JEDEC	—
TOSHIBA	QFP44-P-1414B

Weight: 1.2g

TA8512AF is a bipolar monolithic developed for R/W IC for 3~8 inch floppy disk drive.
The read circuit and write circuit and various control circuits for the floppy disk drive are integrated on one chip to realize small size and low power dissipation.

- To decrease the power dissipation when it is not operated the system has a power save function (The state where read, write, and erase are not performed), and the power dissipation under power save state is 9mW(Typ.)(at 5V single power supply use).
- The system operates by dual power suppies of V_{CC}=12V±10% and V_{DD}=5V±10% or single power supply of $V_{CC}=V_{DD}$=5V±10%.
- As a read/write change-over diode switch is built in, the read amplifier differential voltage gain can be set either 100 times or 200 times by the gain select terminals.
- The write current can be optionally set by an external resistance 60 25mADC.
- As the write current change-over circuit is built in, the current value can be changed-over either internal or external circumference of the disk.
- The read circuit, write circuit, and erase circuit are incorporated in a chip and control can be make in independent timing by $\overline{WG}$ and $\overline{EG}$.
- The power supply monitoring circuit is incorporated to inhibit abnormal writing at the rise of power supply and occurrence of abnormal power.
- A capacitor for time domain filter's time constant is incorporated and the time constant can be set by an external resistance.
- As the time domain filter's time c-nstant changed-over circuit is built in, the period (t1) of the first one shot can be change-over either internal or circumfrence of the disk.
- As the differentiator component change-over circuit is incorporated, the frequency characteristic of the differentiator can be changed-over.

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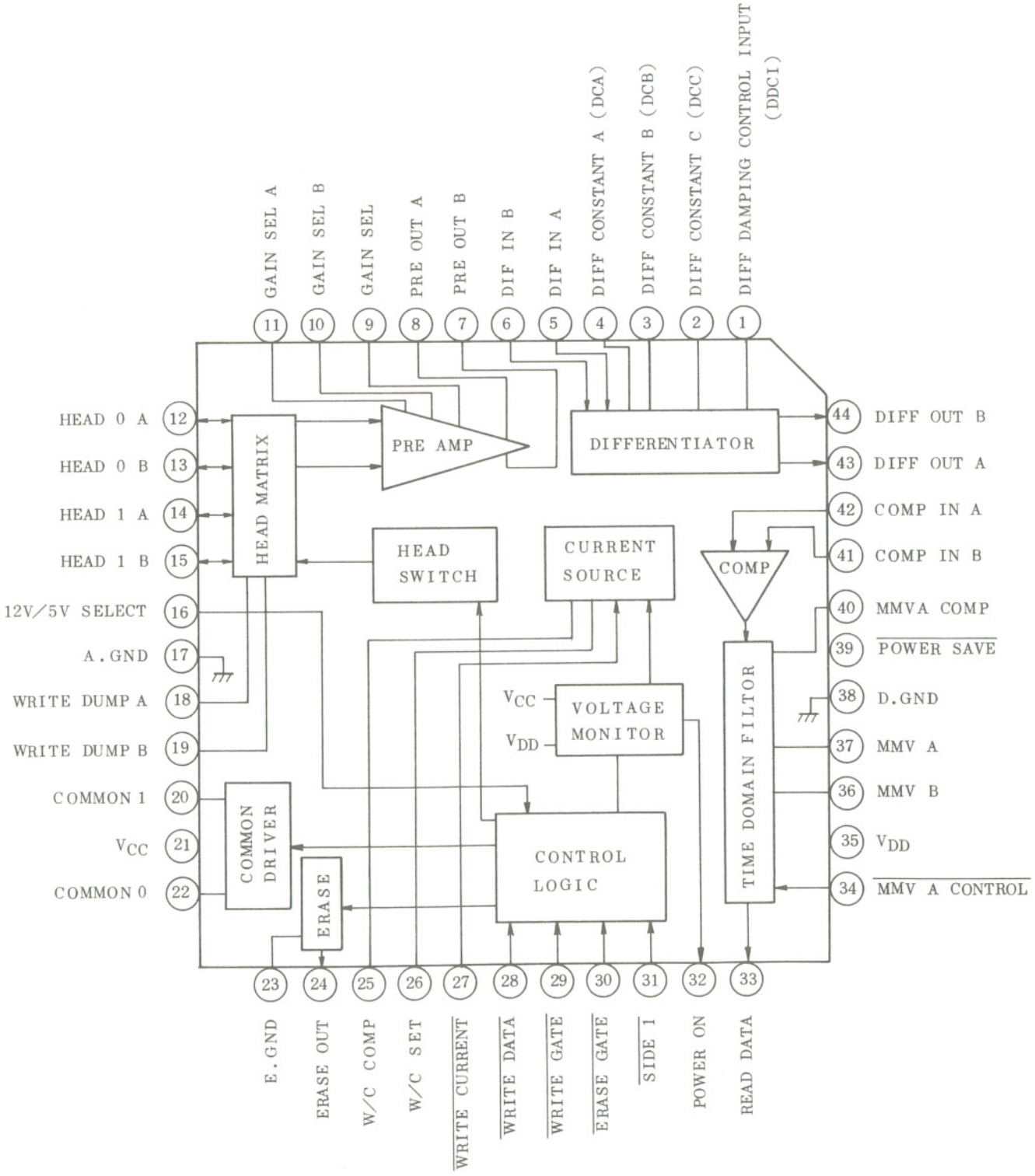
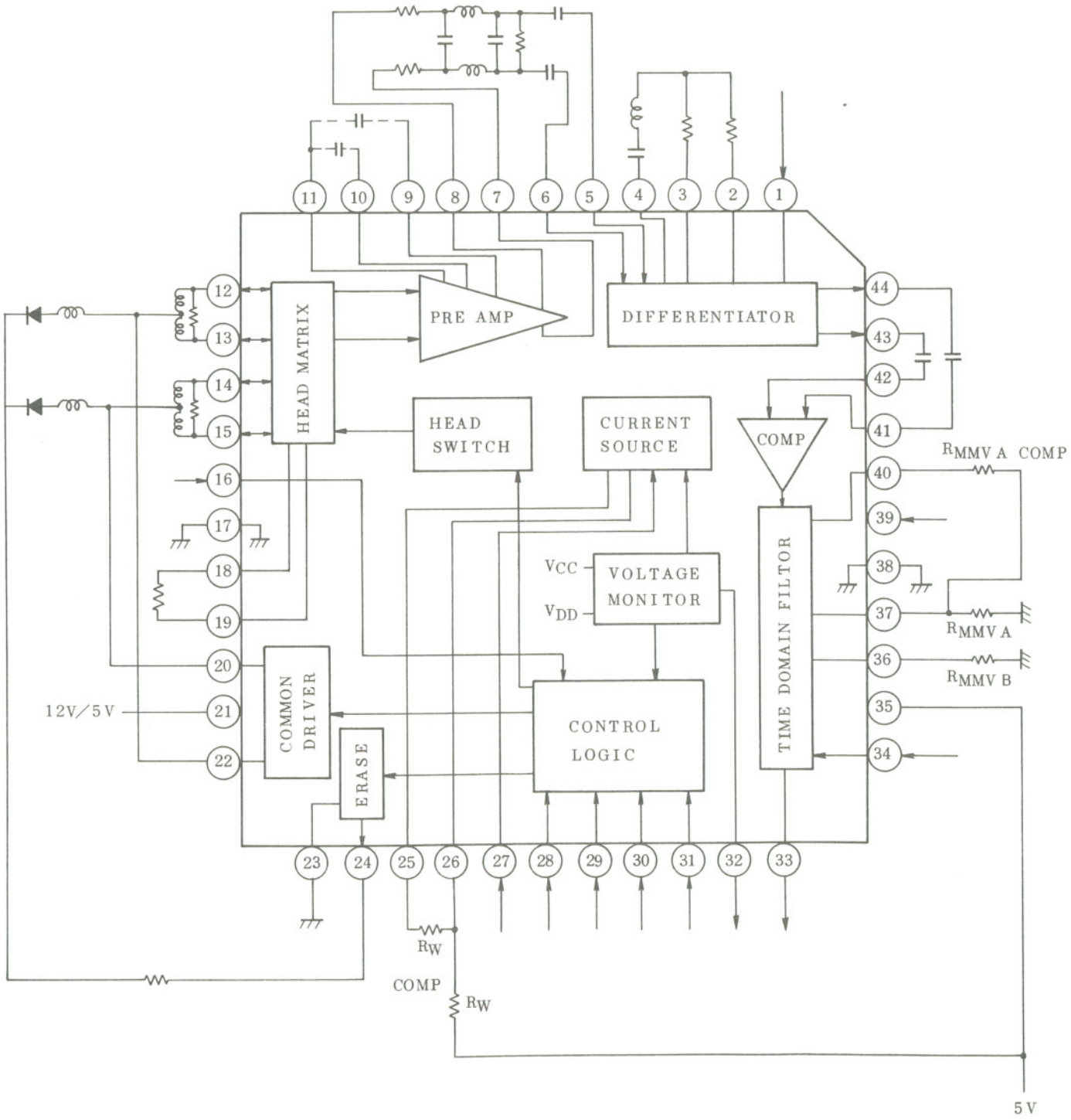
PIN CONNECTIONS/BLOCK DIAGRAM



Please not that 9, 11, 12, 13, 15 pin is not endurable enough against ESD.
(~ ±100V)

TYPICAL APPLICATION



PIN DESCRIPTION TABLE

PIN No.	NAME	DESCRIPTION
1	DIFF DAMPING CONTROL INPUT	Active Differentiator Components Select: When logical voltage "L" is input, component between 3 and 4 terminal and at logical voltage "H", between 2 and 4 terminal is selected.
2 3 4	DIFF CONSTANT C DIFF CONSTANT B DIFF CONSTANT A	Active Differentiator Components: Active differentiator components are connected between 4 and 2 terminal or between 4 and 3.
5 6	DIFF IN A DIFF IN B	Active Differentiator Inputs: From the two preamplifier output terminals, the read signal is differentially input through the filter circuit.
7 8	PRE OUT B PRE OUT A	Preamplifier Outputs: From the tow terminals, the read signal is differentially input to the differentiator input terminals through the filter circuit.
9 10 11	GAIN SEL GAIN SEL B GAIN SEL A	Preamplifier Gain Selects: By AC coupling short between terminal 9 and 11, preamplifier gain of 200 times, and by AC coupling short between terminals 10 and 11, preamplifier gain of 100 times can be selected.
12 13	HEAD 0 A HEAD 0 B	Head 0 Connects: A magnetic head for record/regeneration having a center tap and a head damping resistance at the read mode is connected.
14 15	HEAD 1 A HEAD 1 B	Head 1 Connects: These are another input/output terminals of one more magnetic head the similar as above.
16	12V/5V SELECT	V_{CC} Power Supply Select: When logical "L" is input, the mode of V_{CC}=5V use is selected.
17	A·GND	Analog Ground
18 19	WRITE DUMP A WRITE DUMP B	Write Damping Resistance Connects: Between these terminals a head damping resistance is connected at the write mode.

PIN DESCRIPTION TABLE

PIN No.	NAME	DESCRIPTION
20	COMMON 1	Cneter Tap 1: This terminal is connected to the center tap of the magnetic head 1 and sets the read/write voltage of the head 1.
21	V_{CC}	+12V or +5V Power Supply
22	COMMON 0	Center Tap 0: This terminal is connected to the center tap of the magnetic head 0 and sets the read/write voltage of the head 0.
23	E·GND	Erase Ground
24	ERASE OUTPUT	Erase Current Output: This is the open collector terminal for performing sink of earsing current.
25	W/C COMP	R_W COMP Connect: Between this terminal and 26 terminal, the RW COMP is connected and sets the increasing write current value. (Formula) $I_{WC} = \frac{1.3 - V_{WC}}{\text{RW COMP } (\Omega)} \times 10(\text{ADC})$
26	W/C SET	R_W Connect: Between this terminal and 35 terminal, the R_W is connected and sets the write current value. (Formula) $I_W = \frac{1.3}{R_W\ (\Omega)} \times 10(\text{ADC})$
27	$\overline{\text{WRITE CURRENT}}$	$\overline{\text{WRITE CURRENT}}$ Input: At the time of the logical voltage "L" inputs, the write current is determined by the sum of I_W and I_{WC}, and at logical voltage "H", the write current is I_W only.
28	$\overline{\text{WRITE DATA}}$	$\overline{\text{WRITE DATA}}$ Input: This is the $\overline{\text{WRITE DATA}}$ input terminal, and triggered at digital input H→L.
29	$\overline{\text{WRITE GATE}}$	$\overline{\text{WRITE GATE}}$ Input: This is a pull up terminal which becomes the write system active by the input of the logical voltage "L".

PIN DESCRIPTION TABLE

PIN No.	NAME	DESCRIPTION
30	$\overline{\text{ERASE GATE}}$	$\overline{\text{ERASE GATE}}$ Input: This is a pull up terminal which becomes the erase system active by the input of the logical voltage "L".
31	$\overline{\text{SIDE 1}}$	$\overline{\text{SIDE 1}}$ Input: This is a pull up terminal, and at the input of the logical voltage "L" the Head 1 system becomes active, and at the input of the logical voltage "H", the Head 0 system becomes active.
32	POWER ON	Power On Output: This is the open collector terminal which outputs "L" when at least either one of power supply V_{DD} and V_{CC} is less than the specified value.
33	READ DATA	Read Data Output: From this terminal digital signal (Read Data) outputs.
34	$\overline{\text{MMVA CONTROL}}$	$\overline{\text{MMVA CONTROL}}$ Input: When logical voltage "L" inputs, the period (t1) of the one-shot time becomes narrow.
35	V_{DD}	+5V Power Supply
36	MMVB	R_{MMVB} Connect: This terminal is connected with the period (t2) of the one-shot time setting resistance R_{MMVB}. The period of the second one-shot time is determined by $t2=27\times(R_{MMVB}\ (\Omega)+100)\times10^{-12}$ (ns)
37	MMVA	R_{MMVA} Connect: This terminal is connected with the period (t1) of the one-shot time setting resistance R_{MMVA}. The period of the first one-shot time is determined by $t1=53.5\times(R_{MMVA}\ (\Omega)+100)\times10^{-12}$ (ns) Note: Setting of $R_A=R_{MMVA}$ when logical voltage "H" inputs to MMVA CONTROL. When logical voltage "L" inputs to MMVA CONTROL, $R_A=R_{MMVA}$// R_{MMVA} COMP and the period t1 becomes narrow.

PIN DESCRIPTION TABLE

PIN No.	NAME	DESCRIPTION
38	D·GND	Digital Ground
39	$\overline{\text{POWER SAVE}}$	$\overline{\text{POWER SAVE}}$ Input: When logical voltage "L" inputs to $\overline{\text{POWER SAVE}}$, reduces the power dissipation of R/W IC (at the power save mode). During the power save mode, read, write, and erase are not carried out. (Power supply monitor circuit is operating.)
40	MMVA COMP	R_{MMVA} COMP Connect: This is an open collector terminal for connecting the corrected period (t1) of one-shot time setting resistance R_{MMVA} COMP to the terminal 37.
41 42	COMP IN B COMP IN A	Comparator Inputs: From active differentiator output terminals, the read signals are differentially input to these terminals through AC coupling capacitor.
43 44	DIFF OUT A DIFF OUT B	Active Differentiator Output: From these terminal, the read signals are differentially input to the comparator input terminals thorugh the AC coupling capacitor.

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage (Pin 21)		V_{CC}	17	V
Power Supply Voltage (Pin 35)		V_{DD}	7	V
Digital Input Voltage	(Note 1)	-	-0.5~5.5	V
Power On Detector Applied Voltage	(Note 2)	-	17	V
Erase Output Applied Voltage	(Note 3)	-	17	V
Head 0/1 Applied Voltage	(Note 4)	-	17	V
Common Output Source Current		I_{COM}	75	mA
Erase Sink Current		I_E	50	mA
Write Current		I_W	25	mADC
Power On Sink Current	(Note 2)	-	7	mA
Operating Ambient Temperature Range		Ta	-20~75	°C
Operating Junction Temperature		Tj	150	°C
Storage Temperature		T_{stg}	-65~150	°C
Power Dissipation (Ta=25°C)	(Note 5)	P_D	0.96	W

(Note 1) These ratings apply to $\overline{\text{WRITE CURRENT}}$, $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE DATE}}$, $\overline{\text{ERASE GATE}}$ $\overline{\text{SIDE 1}}$, $\overline{\text{MMVA CONTROL}}$, $\overline{\text{POWER SAVE}}$, DDC1, 12V/5V SELECT.

(Note 2) This rating applies to POWER ON (pin 32).

(Note 3) This rating applies to ERASE OUTPUT (pin 24).

(Note 4) These rating apply to (Pin 12)(Pin 13)(Pin 14)(Pin 15).

(Note 5) In the actual operation refer to Fig.1.

ELECTRICAL CHARACTERISTICS

(1) SUPPLY CURRENT I (Ta=25°C, V_{CC}=12V, V_{DD}=5V)

CHARACTERISTIC		SYMBOL	FIGURE	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
Read Mode	V_{DD} Supply Current	I_{DDR}	-		-	17.6	27.5	mA
	V_{CC} Supply Current	I_{CCR}	-		-	7.2	8.6	mA
Write Mode	V_{DD} Supply Current	I_{DDW}	-	I_W=0	-	8.8	12.6	mA
	V_{CC} Supply Current	I_{CCW}	-		-	3.4	5.1	mA
Erase Mode	V_{DD} Supply Current	I_{DDE}	-		-	8.8	12.4	mA
	V_{CC} Supply Current	I_{CCE}	-		-	3.6	5.6	mA
Write + Erase Mode	V_{DD} Supply Current	I_{DDW+E}	-	I_W=0	-	11.5	21.7	mA
	V_{CC} Supply Current	I_{CCW+E}	-		-	3.3	5.3	mA
Power Save Mode	V_{CC} Supply Current	I_{DDPS}	-		-	1.3	2.7	mA
	V_{CC} Supply Current	I_{CCPS}	-		-	0.35	0.5	mA
	Total Power Dissipation	P_{DPS}	-		-	10.7	19.5	mW

SUPPLY CURRENT II (Ta=25°C, V_{CC}=5V, V_{DD}=5V)

CHARACTERISTIC		SYMBOL	FIGURE	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
Read Mode	V_{DD} Supply Current	I_{DDR}	-		-	17.7	23.4	mA
	V_{CC} Supply Current	I_{CCR}	-		-	7.5	8.6	mA
Write Mode	V_{DD} Supply Current	I_{DDW}	-	I_W=0	-	9.5	15.4	mA
	V_{CC} Supply Current	I_{CCW}	-		-	12.3	18.8	mA
Erase Mode	V_{DD} Supply Current	I_{DDE}	-		-	9.4	13.9	mA
	V_{CC} Supply Current	I_{CCE}	-		-	12.6	19.2	mA
Write + Erase Mode	V_{DD} Supply Current	I_{DDW+E}	-	I_W=0	-	12.3	19.4	mA
	V_{CC} Supply Current	I_{CCW+E}	-		-	12.3	18.8	mA
Power Save Mode	V_{DD} Supply Current	I_{DDPS}	-		-	1.35	2.7	mA
	V_{CC} Supply Current	I_{CCPS}	-		-	0.27	0.4	mA
	Total Power Dissipation	P_{DPS}	-		-	8.1	15.5	mW

ELECTRICAL CHARACTERISTICS

(2) POWER SUPPLY MONITOR (Ta=25°C, V_{CC}=0~16V, V_{DD}=0~7V)

CHARACTERISTIC		SYMBOL	FIGURE	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
5V Power Supply (V_{DD}, V_{CC}) Threshold Voltage	Positive	V_T+	-		-	4.0	4.2	V
	Negative	V_T-	-		3.6	4.0	-	
12V Power Supply (V_{CC}) Threshold Voltage	Positive	V_T+	-	V_{DD}=5V	-	9.0	10.0	V
	Negative	V_T-	-		8.2	9.0	-	
5V Power Supply Hysteresis		V_T+-V_T-	-		-	150	-	mV
12V Power Supply Hysteresis		V_T+-V_T-	-		300	-	-	mV
Power On Output (Pin 32) Saturated Voltage			-	V_{DD}=3.6V I_{SINK}=5mA	-	-	0.4	V
Power On Output (Pin 32) Leakage Current			-	V_{DD}>4.5V	-	-	10	μA

ELECTRICAL CHARACTERISTICS

(3) PRE AMPLIFIER·ACTIVE DIFFERENTIATOR·COMPARATOR (Ta=25°C, V_{CC}=12V~5V, V_{DD}=5V)

	CHARACTERISTIC	SYMBOL	FIGURE	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
Head Matrix/Pre Amplifier	Differential Voltage Gain	G_{V1}	2	f=1MHz	170	200	230	V/V
		G_{V2}	2	f=1MHz	85	100	115	
	Bandwidth (-3dB)	BW	2		-	5	-	MHz
	Common Mode Rejection Ratio	CMRR	-	Input Sine Wave f=1MHz, 200mVrms	50	-	-	dB
	Power Supply Rejection Ratio	PSRR	-	Supperposed Sine Wave f=10MHz, 1Vp-p	70	-	-	dB
	Differential Input Resistance	R_{IN}	-	f=62.5~500kHz	-	10	-	k
	Differential Input Capacitance	C_{IN}	-	f=125kHz	-	-	-	pF
Pre Amplifier	Differential Input Voltage Linear Operation	V_{IN}	-	Gain × 100 times	0.8	-	15	mVp-p
	Differential Output Voltage Linear Operation	V_{OUT}	2		2.0	3.0	-	Vp-p
	Differential Output Sink Current	I_{OUT}	-		3.0	4.0	5.0	mAp-p
	Differential Output Off Set	V_{OFS}	-		-	-	0.5	V
	Noise Voltage Refered to Input	E_N	2	Head Connected Terminals Short BW=400Hz~1MHz	-	4.0	6.0	μV_{rms}
Active Differentiator	Band Width (-3dB)	F_{CD}	-		10	15	-	MHz
	Differential Output Voltage Linear Operation	$V_{OUT\ D}$	-		-	2	-	Vp-p
	Differential Output Off Set	$V_{OF\ D}$	-		-	20	-	mV
	Differential Input Resistance	$R_{IN\ D}$	-		12	-	-	kΩ
	Differential Output Resistance	$R_{OUT\ D}$	-		-	200	-	Ω
	Sink Current (Pin 2,3,4)	$I_{SINK\ D}$	-		1.4	2.0	-	mA
Comparator	Differential Input Voltage Linear Operation	$V_{IN\ C}$	-		-	2	-	Vp-p
	Differential Input Resistance	$R_{IN\ C}$	-		12	-	-	kΩ

ELECTRICAL CHARACTERISTICS

(4) TIME DOMAIN FILTER · DIGITAL OUTPUT (Ta=25°C, V_{CC}=12V~5V, V_{DD}=5V)

CHARACTERISTIC		SYMBOL	FIGURE	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
Timing Range of First One-shot		t_1	3		200	-	3000	ns
Timing Range of Second One-shot		t_2	3		100	-	1200	ns
R_{MMVA} Comp Connect (Pin 40) Saturated Voltage		V_{MMC}	-	I_{SINK}=10μA	-	-	50	mV
Timing Accuracy of First One-shot		E_{TM1}	3		-18	-	+18	%
Timing Accuracy of Second One-shot		E_{TM2}	3		-20	-	+20	%
Corrected Timing Accuracy of First One-shot		E_{TM1C}	3		-15	-	+15	%
Peak Shift		P_S	3	Comparator Input Wave f=250kHz, Differential Input Level 200mVp-p	-	-	1	%
Digital Output (Pin 33)	Output Voltage Low Level	$V_{L\ OUT}$	-	I_{OL}=2mA	-	-	0.5	V
	Output Voltage High Level	$V_{H\ OUT}$	-	I_{OH}=-10μA	3.5	-	-	V
				I_{OH}=-0.4mA	2.8	-	-	
	Sink Current	I_{SIRD}	-	V_{OUT}=0.8V	2	4	-	mA
	Soure Current	I_{SORD}	-	V_{OUT}=2.8V	0.4	1	-	mA
	Output Rise Time	t_r	3	From 0.5~2.2V at 20pF Capacitance Load	-	-	25	ns
	Output Fall Time	t_f			-	-	25	

ELECTRICAL CHARACTERISTICS

(5) WRITE DRIVER · ERASE DRIVER (Ta=25°C, V_{CC}=12V~5V, V_{DD}=5V)

	CHARACTERISTIC	SYMBOL	FIGURE	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
Common Driver	Output Voltage High Level at Write Mode 1	V_{WCMH12}	-	V_{CC}=12V, I_W=25mADC	10.8	-	-	V
	Output Voltage High Level at Write Mode 2	V_{WCMH5}	-	V_{CC}=5V, I_W=25mADC	4.4	-	-	V
	Output Voltage Low Level at Write Mode	V_{WCML}	-		-	-	0.2	V
	Output Voltage High Level at Read Mode	V_{RCMH}	-		2.3	2.6	2.9	V
	Output Voltage Low Level at Read Mode	V_{RCML}	-		-	-	0.2	V
	Output Current Range	I_{COM}	-		-	-	75	mA
Erase Driver	Erase Current Output (Pin 24) Saturated Voltage	V_{ER}	-	I_E=50mA	-	0.2	0.5	V
	Erase Current Output (Pin 24) Leakage Current	I_{LKER}	-		-	-	15	μA
	Erase Current Range	I_E	-		-	-	50	mA
Write Driver	Write Current Range (Single)	I_W	-		-	-	20	mADC
	Corrected Write Current Range (Single)	I_{WC}	-		-	-	5	mADC
	Write Current Setting Accuracy	E_W	-		-8	-	+8	%
		E_{WC}	-		-10	-	+10	
	Write Current Unbalance	D_W	-		-	-	1	%
	R_W Comp Connect (Pin 25) Saturated Voltage	V_{WC}	-	I_{SOURCE}=0.5mA	-	50	300	mV
Head Connect (Pin12,Pin13, Pin14,Pin15)	Leakage Current	I_{LKW}	-		-	-	10	μA
	Saturated Voltage	V_{SAT}	-		-	2	-	V
	Differential Output Capacitance	C_{OUT}	-		-	23	-	pF
	Differential Output Resistance	R_{OUT}	-	f=1MHz	-	280	-	kΩ

ELECTRICAL CHARACTERISTICS

(6) CONTROL LOGIC (Ta=25°C, V_{CC}=12V, V_{DD}=5V)

CHARACTERISTIC			SYMBOL	FIGURE	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
Digital Input Level	Input Voltage Low Level		V_{LIN}	-		-	-	0.8	V
	Input Voltage High Level		V_{HIN}	-		2.0	-	-	V
	Input Current Low Level	Power SAVE Input (Pin 39)	I_{LIN}	-	V_{IN}=0.4V	-	-	50	μA
		Other Pins		-	V_{IN}=0.4V	-	-	250	
	Input Current High Level (Pin 28,29,30,31)		I_{HIN1}	-	V_{IN}=2.4V	-	-	10	μA
	Input Current High Level (Pin 27)		I_{HIN2}	-	V_{IN}=2.4V	-	-	130	μA
	Input Current High Level (Pin 34)		I_{HIN3}	-	V_{IN}=2.4V	-	-	80	μA
Write Data Input (Pin28)	Negative Threshold Voltage		V_{LINS}	-		0.8	1.0	-	V
	Positive Threshold Voltage		V_{HINS}	-		-	1.6	2.0	V
	Hysteresis		V_{HINS}-V_{LINS}	-		0.3	0.6	-	V

(7) AC SWITCHING CHARACTERISTICS (Ta=25°C, V_{CC}=12V~5V, V_{DD}=5V)

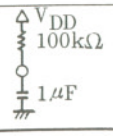
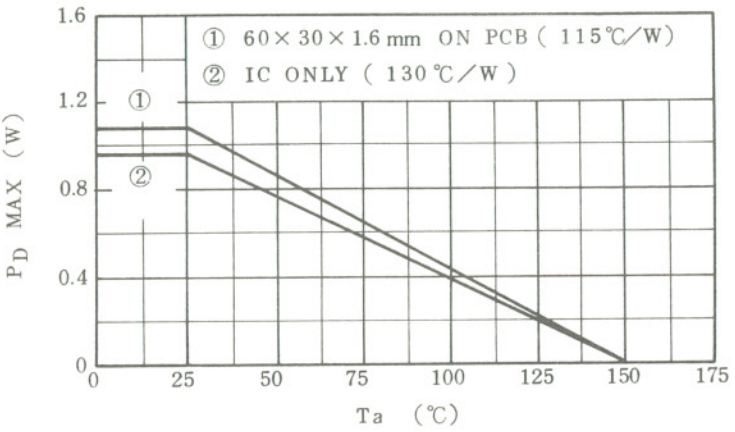
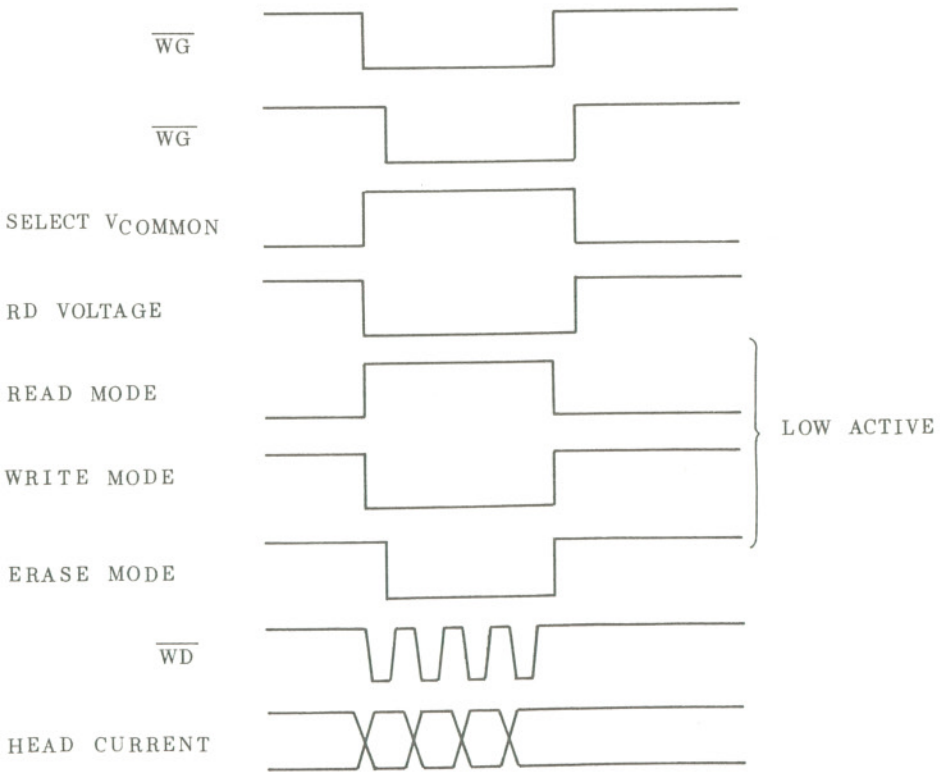
CHARACTERISTIC	MEASURE CONDITION	MIN.	TYP.	MAX.	UNIT
Dealy from PS Going High Through 2V to Read Mode	$\overline{PS}$ OFF→DIFF Output 90~110%	-	1	2	ms
Head Selecting Time		-	-	4	μs
Delay from WG Going High Through 2V to Read Mode	$\overline{WG}$ OFF→Select V_{COM} Voltage 90%	-	-	1	μs
WD-I_W Delay		-	-	0.3	μs
Write Current Rise Time 1	Lh=0mH	-	-	0.1	μs
Write Current Rise Time 2	Lh=1mH, R_D=8.2kΩ, h=30pF	-	0.2	-	μs
Delay from EG Going High Through 2V to Read Mode	$\overline{EG}$ OFF→DIFF Output 90~110%	-	-	20	μs
Read Recovery Time	$\overline{WG}$, $\overline{EG}$ OFF→DIFF Output 90%	-	30	40	μs
Power On Output Sink Current Rise or Fall Time (Pin 32)	Load (Pin 32) 	-	-	100	ms

Fig. 1 Power Dissipation (Pd)-Operating Ambient Temperature (Ta)



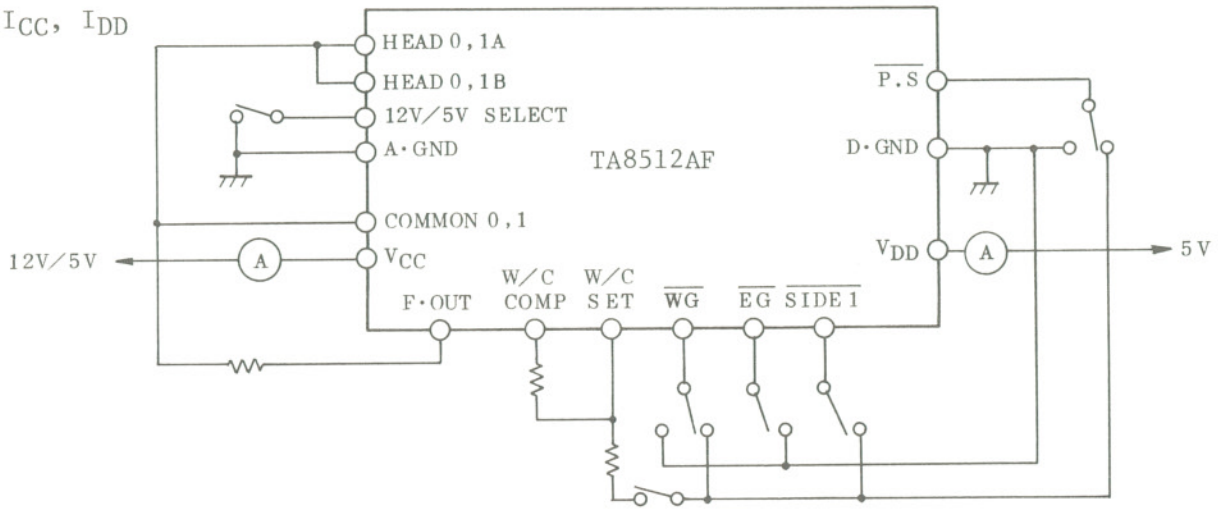
The maximum of operating ambient temperature (Ta) of TA8512AF is 75°C, but the power dissipation (P_D) differs according to the ambient temperature, so that in the actual operation refer to the above graph.

TIMING CHART

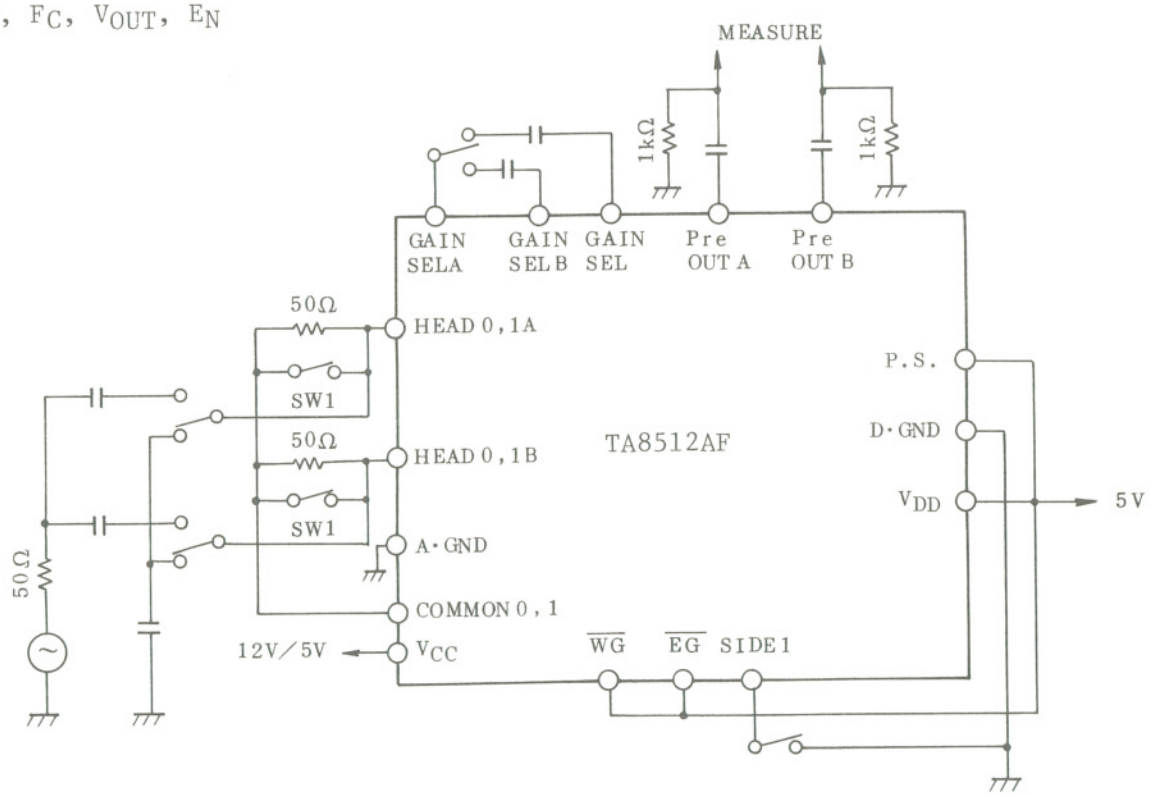


TEST CIRCUIT

1. I_{CC}, I_{DD}



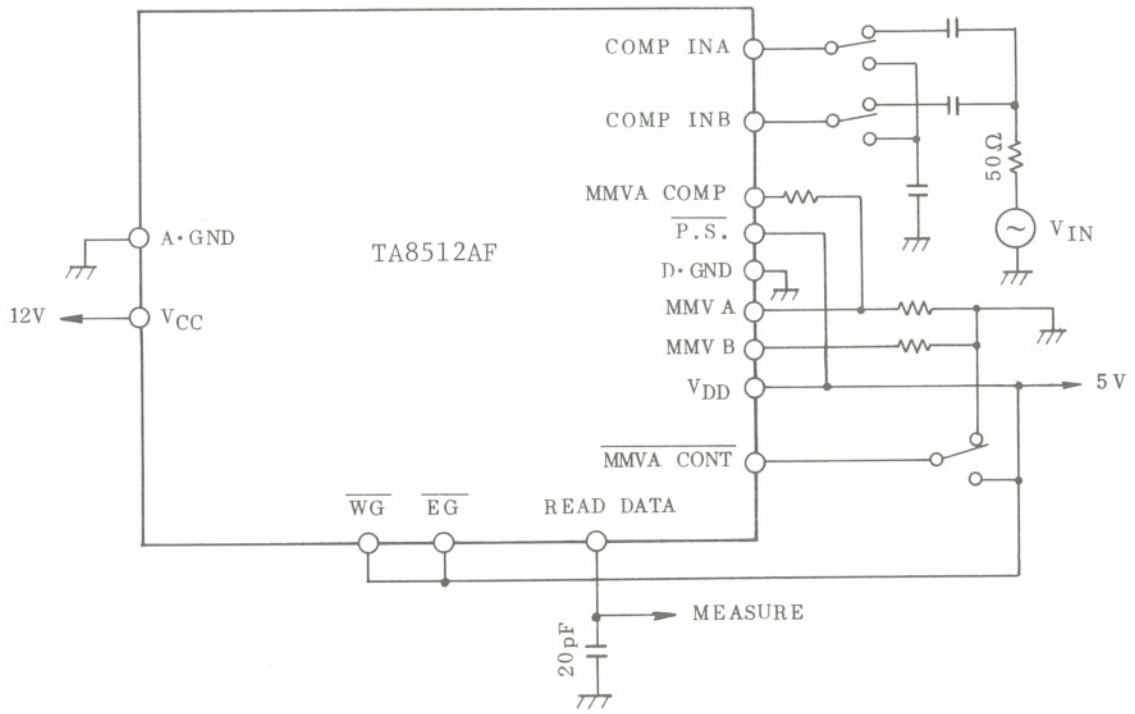
2. G_V, F_C, V_{OUT}, E_N

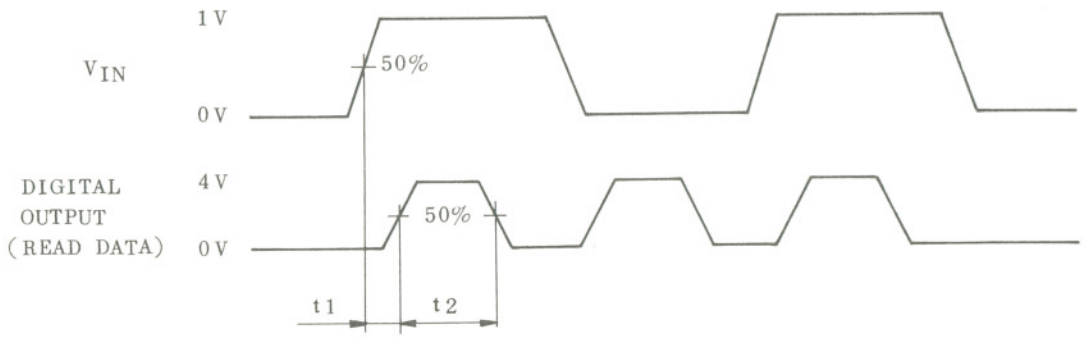


Note 1 : In the measurement of G_V, F_C and V_{OUT}, the input signal is applied to either selected one terminal of HEAD 0.1A or HEAD 0, 1B.

Note 2 : In measuring E_N only, SW1 is closed.

3. t1, T2, EMT1, EMT2, EMTIC, PS, t_r, t_f





Fir.3-1 t1, t2

(1) Timing accuracy of frist and secound one-shot.

R_{MMVA} and R_{MMVB} which set the period (t1) of first one-shot to 1μs, the period (t2) of secound to 0.5μs connect and measure the digital output as above.

ETM1, ETM2 are difined as follows:

ETM1 = (1-t1/1) ×100 (%) (t1[μs], t2[μs])

ETM2 = (0.5-t2/0.5) ×100 (%)

(2) Corrected timing accuracy of first one-shot

R_{MMVA} and R_{MMVA} comp which set difference t1-t1' to 1μs connect.
(t1 is the period of first one-shot when applies 2V to $\overline{\text{MMVA CONTROL}}$, t1' is that one when applies 0.8V to $\overline{\text{MMVA CONTROL}}$.)
EMTIC is difined as follow:

$$\text{EMTIC} = [1 - (t1-t1')\quad] \times 100 \quad (\%)$$

(3) PEAK SHIFT

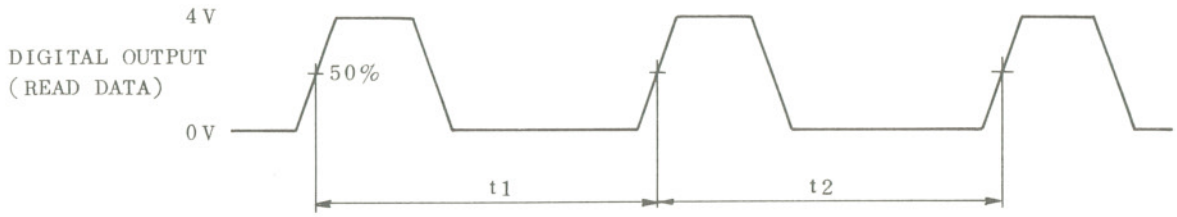
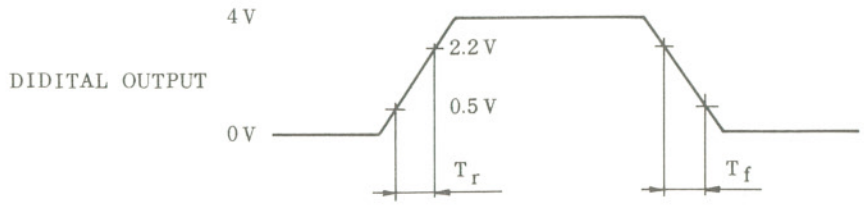


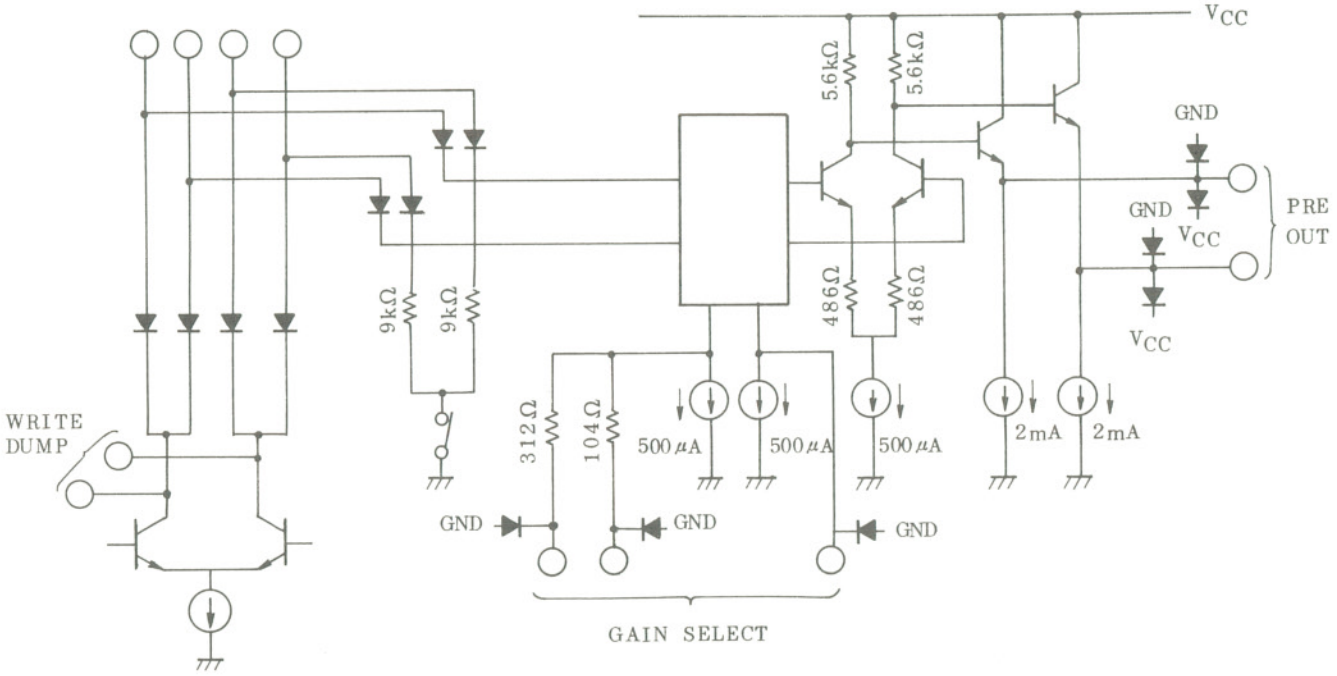
Fig. 3-2 P.S.

$$PS = \frac{1}{2} \times \frac{t1-t2}{t1+t2} \times 100 \quad (\%)$$

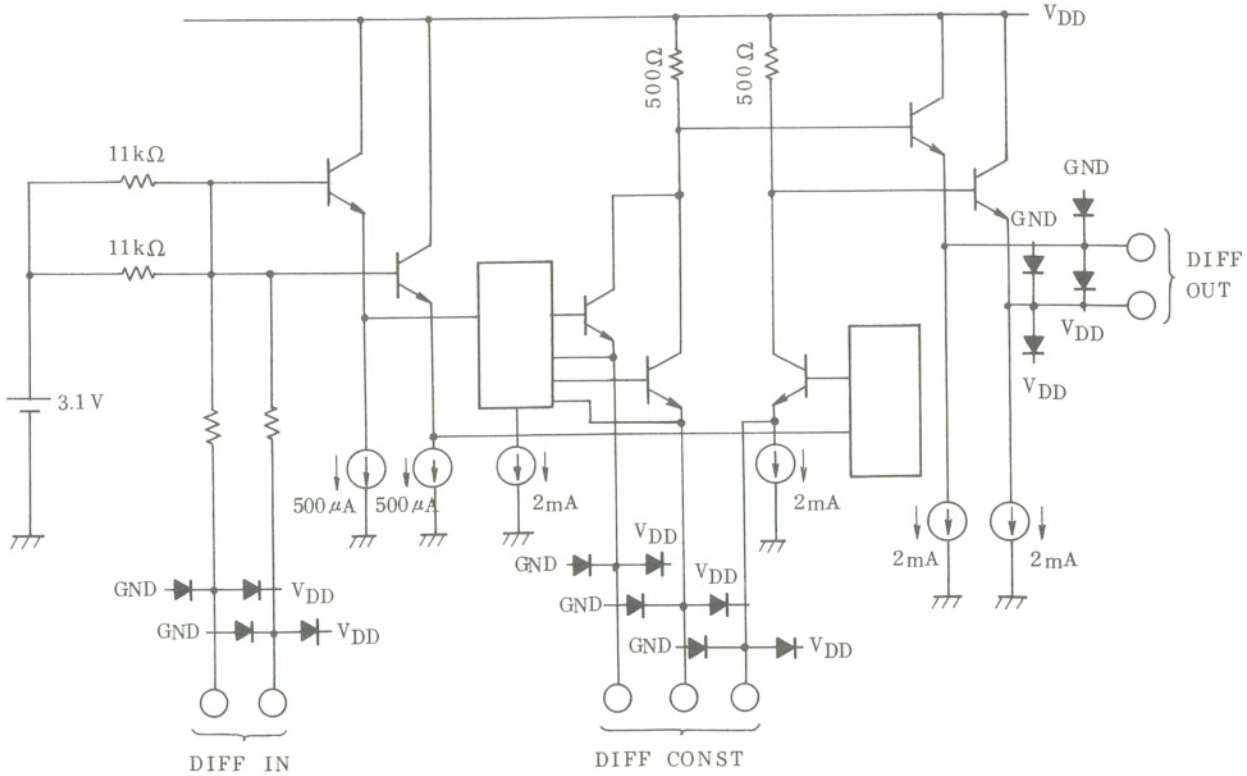
(4) Digital Output (Read Data) Rise Time, Fall Time



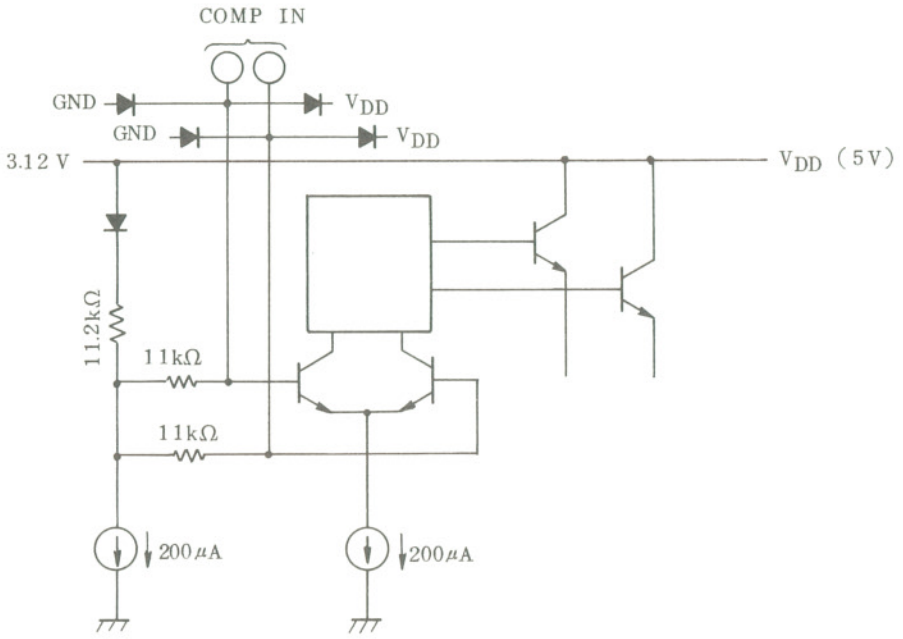
PREAMPLIFIER



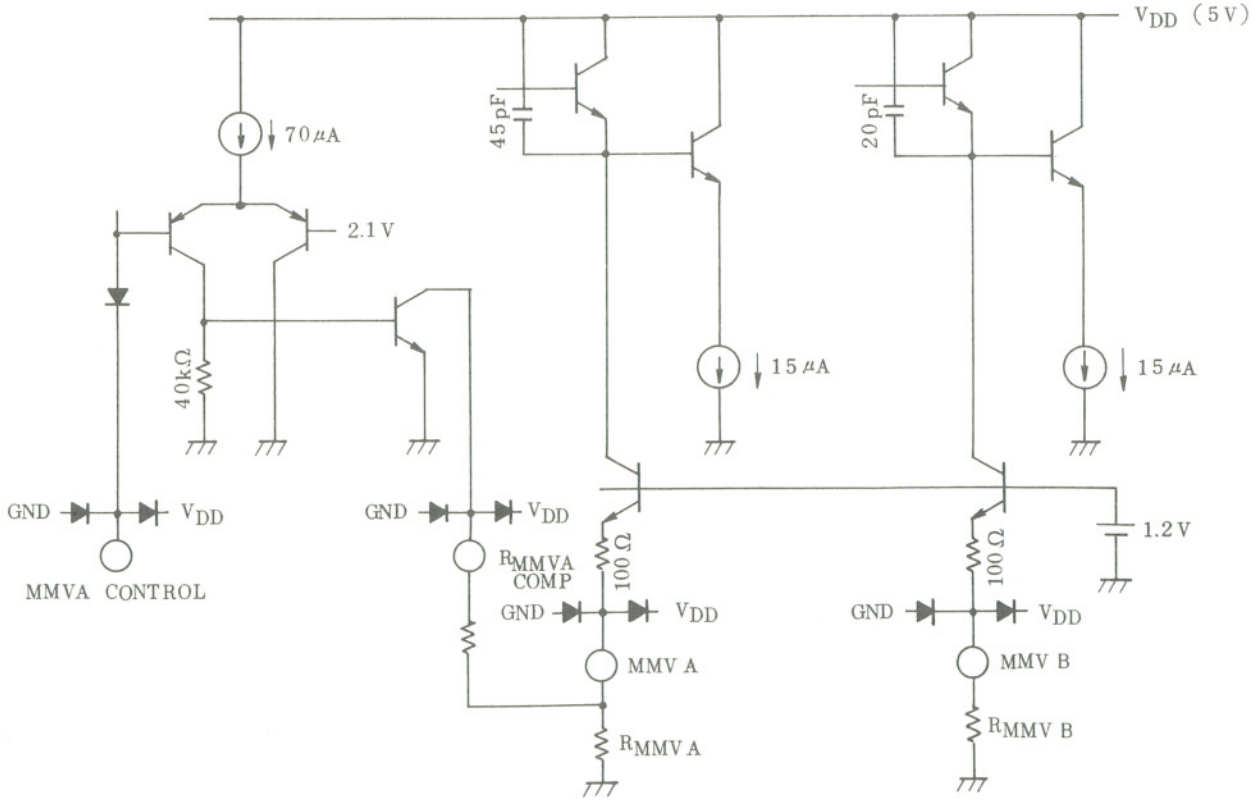
ACTIVE DIFFERENTIATOR



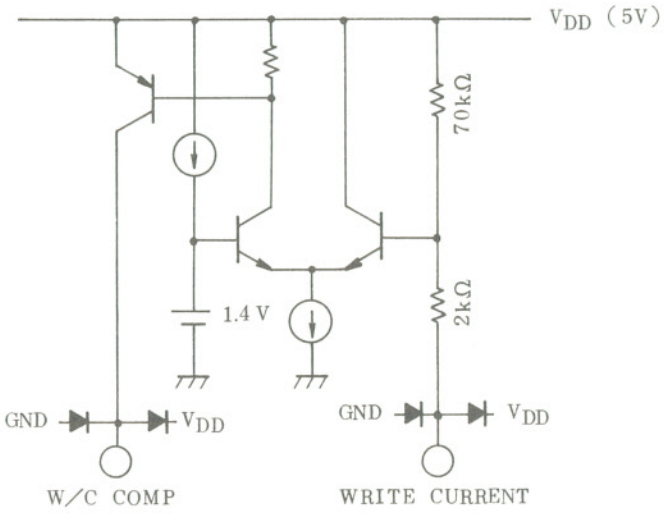
COMPARATOR



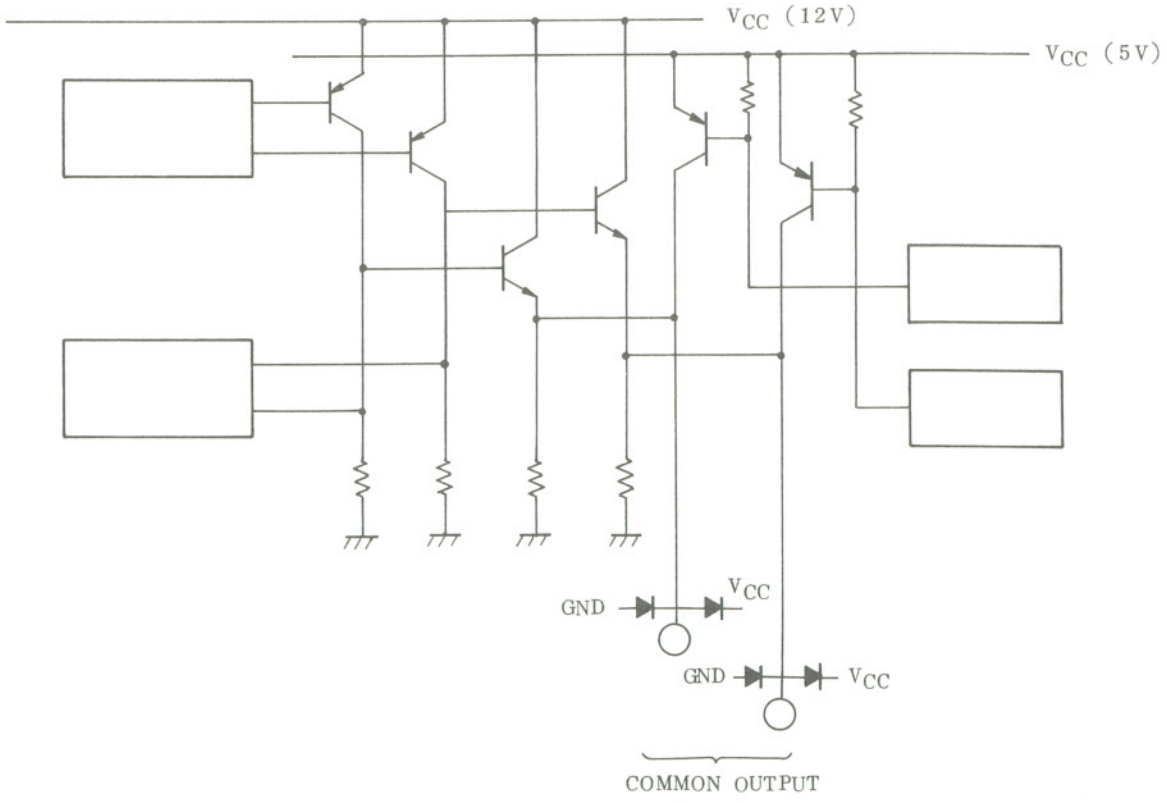
TIME DOMAIN FILTER



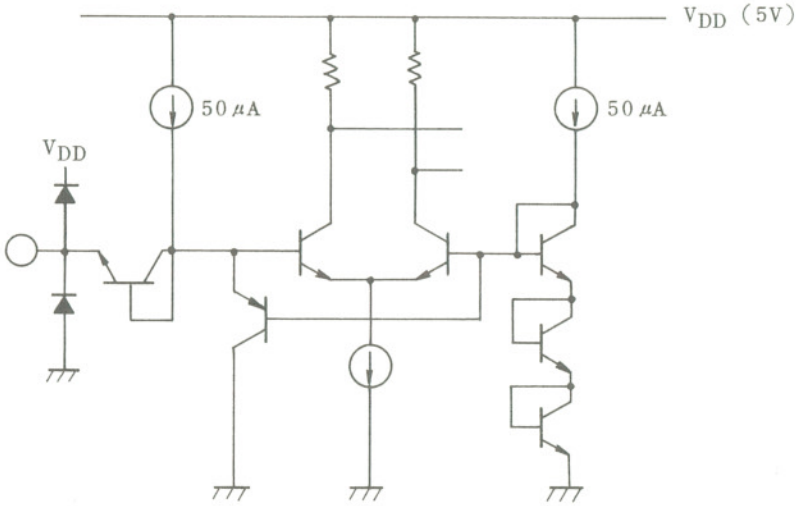
W/C CONTROL



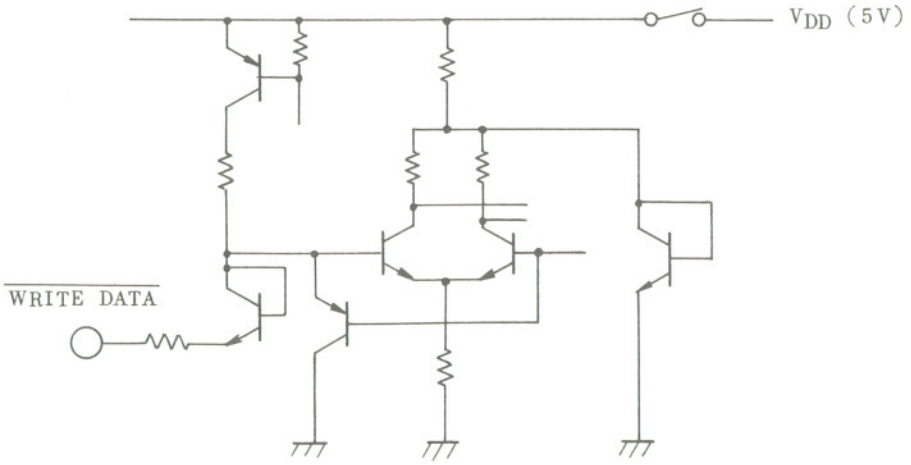
COMMON DRIVER OUTPUT



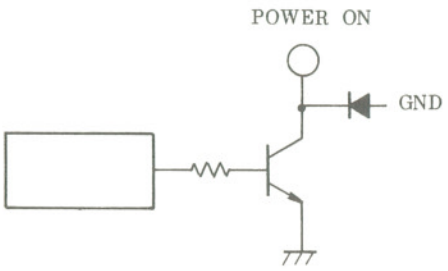
$\overline{\text{WRITE GATE}}$, $\overline{\text{ERASE GATE}}$, $\overline{\text{SIDE 1}}$ INTERFACE



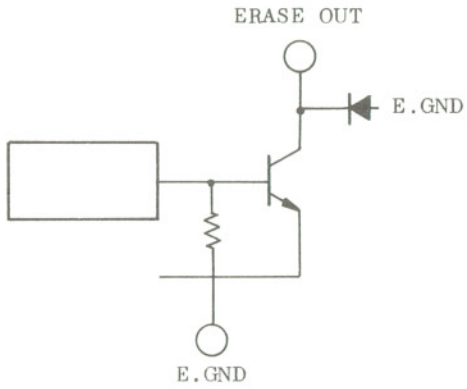
WRITE DATA INTERFACE



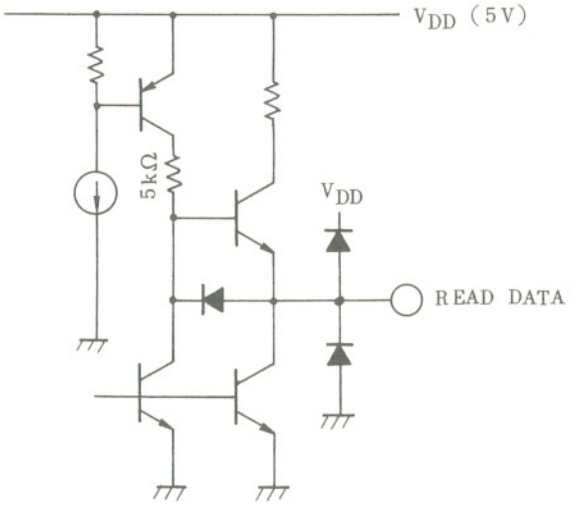
POWER SUPPLY VOLTAGE



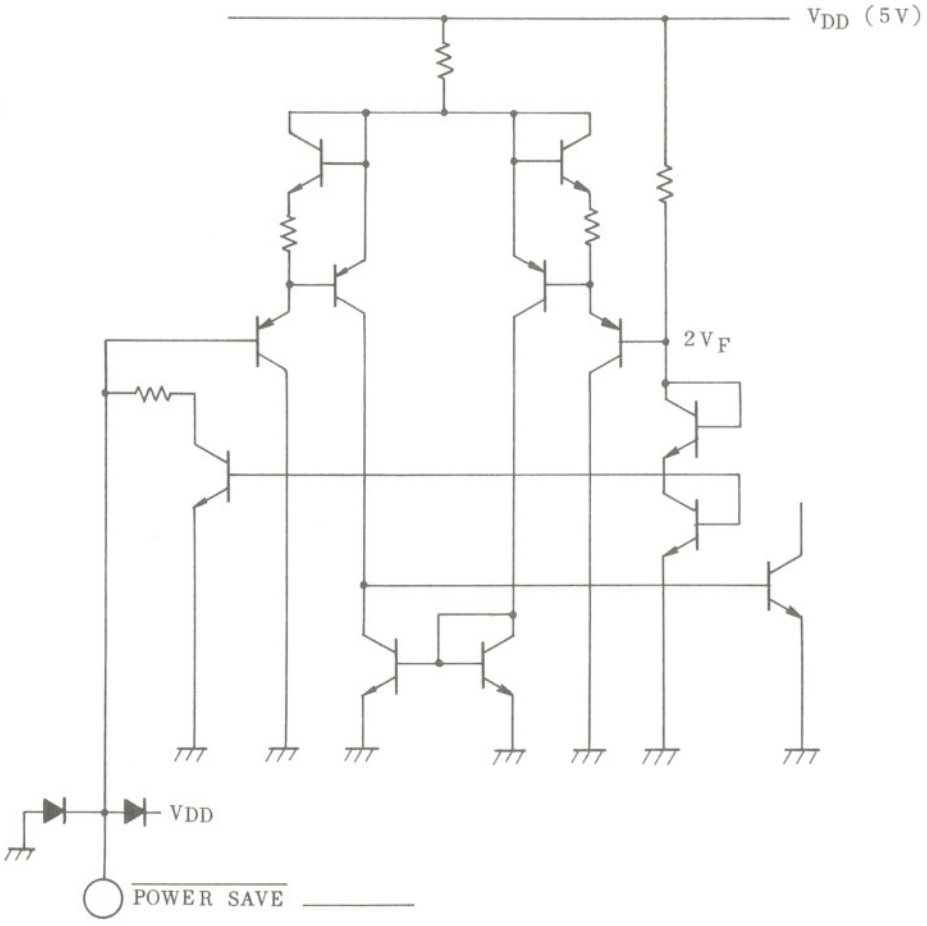
ERASE OUTPUT



DIGITAL OUTPUT



$\overline{\text{POWER SAVE}}$ INTERFACE



INPUT VOLTAGE	POWER SAVE MODE
H	In Active
L	Active
OPEN	Active