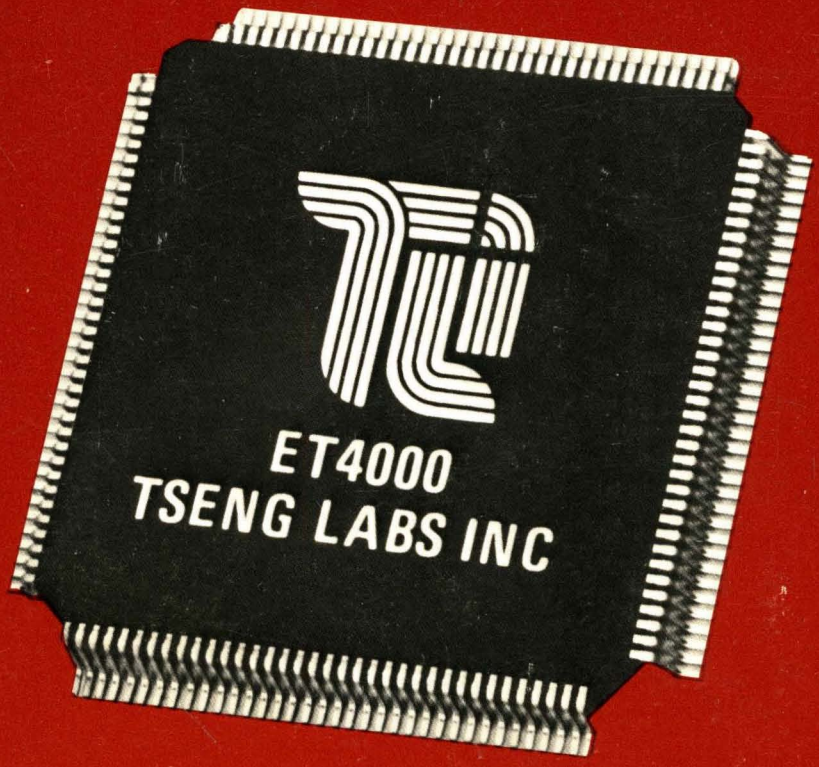


DATA BOOK

ET4000 Graphics Controller

High-Performance Video Technology

Tseng Labs, Inc.

DATA BOOK

ET4000 Graphics Controller

High-Performance Video Technology

ET4000 DATA BOOK TABLE OF CONTENTS

TABLES

FIGURES

1.0 INTRODUCTION

The ET4000 VLSI Video Graphics Controller chip has been designed to optimize cost/performance trade-off considerations, providing a cost-efficient solution to OEM's next generation of display controllers. The ET4000 is specifically designed for IBM PC/XT/AT, Personal System/2, and compatible systems offering 100% register-level compatibility in all video standards using VGA, EGA, CGA, MDA and Hercules modes .

The ET4000 is a single 1.0 micron VLSI chip which is distinguished from the previous generation of VGA controllers by its high-level of intelligence and flexibility in managing memory resources. Recently, memory technology has changed from wider (more available pins) to deeper (more memory) configurations. This characteristic places greater importance on graphics controller Application Specific Integrated Circuits (ASIC).

Tseng Labs has created a completely new design for the ET4000, which initiates a new generation of design techniques, particularly relating to memory resource management capabilities. The ET4000 has multiple blocks of Cache Memory, multiple blocks of FIFOs, a Memory Management Unit (MCU), and a System Priority Controller (SPC). These added capabilities translate to minimum memory requirements and higher system performance.

In a VGA display controller implementation, only two 1MB memory devices are needed to maintain comparable VGA performance. Faster, or additional memory chips installed with the ET4000 will provide better performance (up to 17 times that of the VGA) and achieve zero wait state during memory write accesses.

Another aspect of the ET4000's memory resource management features is its capability to be reconfigured for the amount of usable memory on board. For example, in maximum memory implementation, if some defective memory is detected during a diagnostic procedure, it is possible to reconfigure the ET4000 with minimum video memory, albeit with some loss of performance.

The ET4000 is packaged in either 144- (ET4000-144) or 160- (ET4000-160) pin PFP (Plastic Flat Package) configurations. The following is an overview of the ET4000 graphics controller specifications.

I. Input Interface
   A. Host processor:
      1. Data bus: 8 or 16-bit memory and I/O bus via ET4000's internal system configuration register
      2. Address: 20-bit linear address, and 4-bit segment address
      3. Bus control: PC/AT or PS/2 MCA compatible interface defined by the ET4000's UCPC input pin

II. Output Interface
   A. Monitor:
      1. Interlaced or non-interlaced V-SYNC and H-SYNC with polarity control
      2. 8-bit palettes: SI SR SG SB PI PR PG PB

   B. External DAC look-up: pixel clock, blanking, and external DAC read/write decode controls

III. Resource Management
   A. Memory management:
      1. Graphics data controller: VGA compatible data rotate/mask/logical functions
      2. Cache: LRU (Less Recently Used) and block transfer
      3. FIFO: up to two FIFOs for display pixel data
      4. Memory Control Unit (MCU):
         a. memory type: 1MB (256K x 4) DRAM or VRAM;
            256KB (64K x 4) DRAM
         b. memory size: VRAM: 8 to up to 16-bit random access and 8 to up to 16-bit serial access;
            DRAM: 8 to up to 32-bit random access
         c. memory timing: programmable RAS/CAS timing in terms of system clock (independent of display clock); programming via the ET4000's RCONF register

   B. System Priority Controller (SPC): Intelligent SPC to resolve multiprocessors and ET4000 resource requests to optimize MCU resource utilization.

   C. CRT controller:
      1. Horizontal: 8-bit programmable display enable, blanking, and H-SYNC
      2. Vertical: 11-bit programmable line counter for display enable, blanking, split screen, and V-SYNC

D. Display address controller:
   1. Linear address generator: 18-bit linear address with programmable starting address, row address offset
   2. Row address generator: 5-bit row scan address provides up to 32-line character height
      a. cursor: 18-bit cursor position and 5-bit cursor start, 5-bit cursor end control

E. Attribute controller:
   1. Text mode: support for up to two 256 character sets;
      IBM-compatible text attribute decoding;
      IBM-compatible cursor blink/underline;
      AT&T-compatible underline decoding (in color text mode)
      Font width: programmable text font width: 8, 9, 10, 12,and 16 pixel
   2. Graphics: plane graphics, linear-byte/word (packed pixel), monochrome and CGA color graphics format; VGA-compatible color LUT (look-up table)

F. Timing interface: select up to 8 MCLK (pixel clock): 65MHz (graphics), 56MHz (text); system clock, 40MHz

IV. Display data format
   A. Plane, Linear byte, Linear word graphics and VGA-compatible text format up to 16-bit wide character
   B. Display capability:
      1. Resolution: up to 1024 x 768 in 256 colors interlaced or non-interlaced in graphics mode
      2. Pixel clock rate: graphics mode, 65MHz; text mode, 56MHz

V. Compatibility
   A. Register level: CGA/MDA/HERC/EGA/VGA
   B. Display level: 8514A
   C. Monitor: IBM's 8503, 8512, 8513, 8514, 5154, 5153, 5151, NEC's MultiSync, MultiSync Plus, XL, and other monitors with up to 1024 x 1024-pixel resolution

The ET4000 offers performance starting with all of the IBM VGA/EGA features and provides enhanced performance with features summarized in tables 1.1-1 and 1.1-2.

This document represents a dynamic source of structured information designed to reflect the most current products from TLI. This means that The Data Book details information relating to the ET4000 and will reflect revisions and replacement products from the ET4000 as they evolve.

1.1 ET4000 Features

- Single +5V supply.
- IBM Video Graphics Array (VGA), Enhanced Graphics Adapter (EGA), CGA/MDA (6845), and AT&T/Olivetti register-level compatibility.
- Raw performance of up to 17 times the speed of the previous generation ET3000 when 4 VRAM are used.
- All display memory can be read from or written to with minimum WAIT states and are fully programmable via 8 or 16-bit data bus.
- All internal registers can be read from or written to and are fully programmable via 8 or 16-bit data bus.
- Up to 64-bit display memory modification in plane graphics mode.
- Up to 64-bit color comparison function, allows byte-wide pixel-to-color comparison facilitating area fill operations.
- I/O register translation in both read and write operation.
- Interlaced or non-interlaced display scan.
- Bit-masking of CPU data, software-selectable, enabling pixel-specific manipulation of display memory.
- Software-selectable X-first (replicate CPU byte for each plane), Z-first (map CPU byte bitwise across planes), and block move (write latched bytes) write access to display memory.
- Dot frequency response at up to 65MHz.
- Full cursor text and all-points-addressable graphics capabilities. Text mode supports programmable underline and cursor height.
- Single-cycle software-selectable data rotation of CPU data.
- Byte-wide software-selectable boolean functions (MOVE, AND, OR, XOR) of CPU data and latched display memory data.
- Plane-wide and linear byte-wide data structures to support both 16- and 256-color formats.
- Supports color and monochrome applications.
- 1M-byte display memory addressing to support up to 1024x768 256-color formats. Addressing may be linear byte, linear word, double word, or with memory planes paired into double-sized planes.
- Programmable memory timing control for any-speed dynamic RAM interfaces.
- Programmable CAS before RAS refresh, providing memory refresh during blanking.
- 5-bit raster scan addressing, supporting 32-scan-line fonts. Double scanning may be software selected.
- Completely independent software control of horizontal display enable, blanking, and sync signals and vertical display enable, blanking, and sync signals. Cursor, horizontal display enable, and horizontal sync signals may be skewed independently.

1.1 ET4000 Features (continued)

- X-Y memory addressing, allowing definition of a virtual display area wider than the CRT surface. The horizontal panning supported by the Attribute Controller permits smooth movement around the virtual display area.
- 18-bit linear start and cursor address.
- Programmable display memory start address, for vertical panning/scrolling applications around a virtual screen higher than the CRT surface. Raster address presetting allows smooth (single scan line) scrolling even in text mode.
- Supports both PEL and byte panning.
- Split-screen feature, allows second independent window starting at display memory address zero. Split-screen window occupies full width of screen, with starting scan line software-selectable. Panning can be disabled within a split screen.
- Graphics mode blinking, allows full emulation of text mode in bit-mapped graphics mode, since intensity, underline, reverse video, and cursor can all be simulated by software.
- Supports up to two simultaneous soft fonts.
- Programmable character width, up to 16-dot-per-character modes.
- Programmable internal color lookup table, with 16 x 6-bit entries.
- Supports external palette RAM interface.
- Border color, programmable to one of 256 colors.
- Software-selectable CPU interrupt generated on vertical retrace.
- Easy interfacing with all popular microprocessors, including the 8086, 80286, 80386, 68000, and Z8000 families.

1.2 Video Modes Supported By The ET4000

Table 1.1-1 summarizes some of the video graphic modes supported by the ET4000 graphics controller chip, while Table 1.1-2 summarizes some of the video text modes supported. Other modes may be created with variation of MCLK and CRTC/ATC programming.

Table 1.1-1: ET4000 Graphic Modes

Mode	Resolution	Board	Colors
4,5	320 x 200	CGA	4
		EGA	4 OUT OF 64
		MCGA	4 OUT OF 256K
		VGA	4 OUT OF 256K
6	640 x 200	CGA	2
		EGA	2 OUT OF 64
		MCGA	2 OUT OF 256K
		VGA	2 OUT OF 256K
D	320 x 200	EGA	16 OUT OF 64
		VGA	16 OUT OF 256K
E	640 x 200	EGA	16 OUT OF 64
		VGA	16 OUT OF 256K
F	640 x 350	EGA	MONOCHROME
		VGA	MONOCHROME
10	640 x 350	EGA	16 OUT OF 64
		VGA	16 OUT OF 256K
11	640 x 480	MCGA	2 OUT OF 256K
		VGA	2 OUT OF 256K
12	640 x 480	VGA	16 OUT OF 256K
13	320 x 200	MCGA	256 OUT OF 256K
		VGA	256 OUT OF 256K
25	640 x 480	TLI	16 OUT OF 256K
29	800 x 600	TLI	16 OUT OF 256K
2D	640 x 350	TLI	256 OUT OF 256K
2F	640 x 400	TLI	256 OUT OF 256K
2E	640 x 480	TLI	256 OUT OF 256K
30	800 x 600	TLI	256 OUT OF 256K
37	1024 x 768	TLI	16 OUT OF 256K
38	1024 x 768	TLI	256 OUT OF 256K

Table 1.1-2 : ET4000 Alpha Modes

Mode	Rows	Cols	Board	Char. Box	Resolution	Colors
0,1	25	40	CGA	8X8	320 x 200	16
			EGA	8X14	320 x 350	16 OUT OF 64
			MCGA	8X16	320 x 400	16 OUT OF 256K
			VGA	9X16	360 x 400	16 OUT OF 256K
2,3	25	80	CGA	8X8	640 x 200	16
			EGA	8X14	640 x 350	16 OUT OF 64
			MCGA	8X16	640 x 400	16 OUT OF 256K
			VGA	9X16	720 x 400	16 OUT OF 256K
7	25	80	MDA	9X14	720 x 350	MONOCHROME
			EGA	9X14	720 x 350	MONOCHROME
			VGA	9X16	720 x 400	MONOCHROME
18	44	132	TLI	8X8	1056 x 352	MONOCHROME
19	25	132	TLI	9X14	1188 x 350	MONOCHROME
1A	28	132	TLI	9X13	1188 x 364	MONOCHROME
22	44	132	TLI	8X8	1056 x 352	16 OUT OF 256K
23	25	132	TLI	8X14	1056 x 350	16 OUT OF 256K
24	28	132	TLI	8X13	1056 x 364	16 OUT OF 256K
26	60	80	TLI	8X8	640 x 480	16 OUT OF 256K
2A	40	100	TLI	8X15	800 x 600	16 OUT OF 256K

2.0 APPLICATION NOTES

2.1 Typical Board-level Configuration

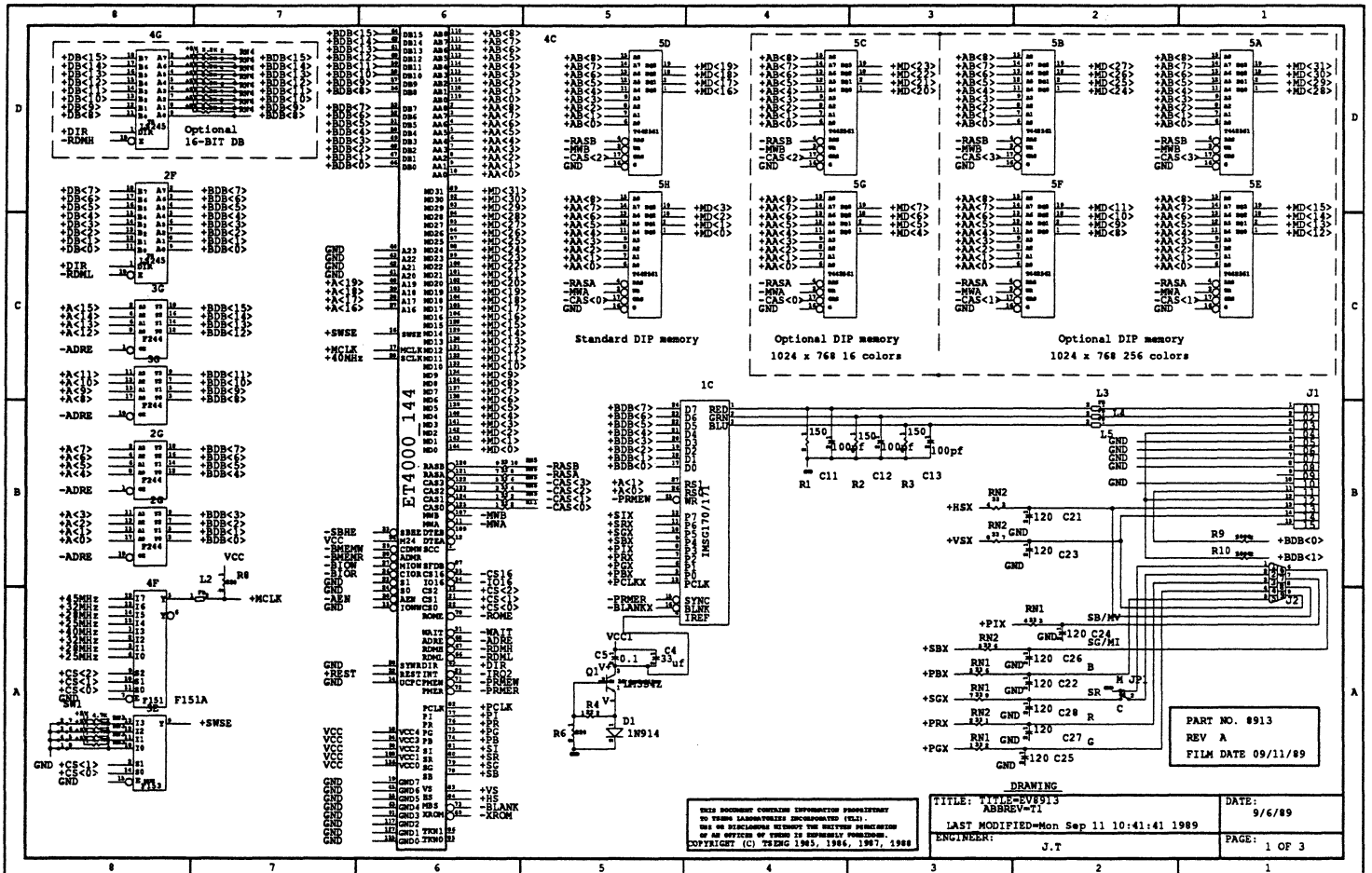


FIG. 2.1-1 TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — AT BUS — 1 of 3

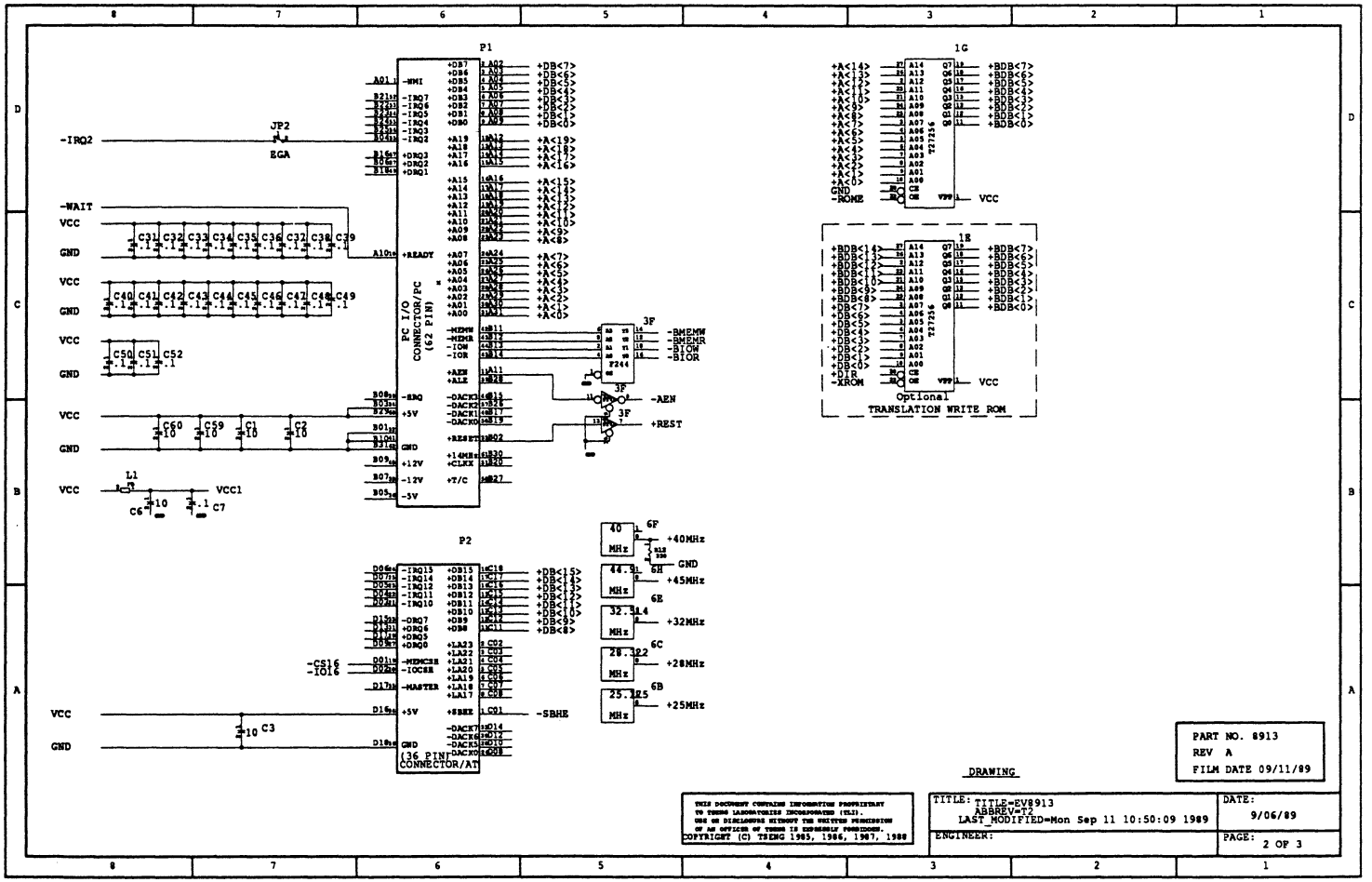


FIG. 2.1-1 TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — AT BUS — 2 of 3

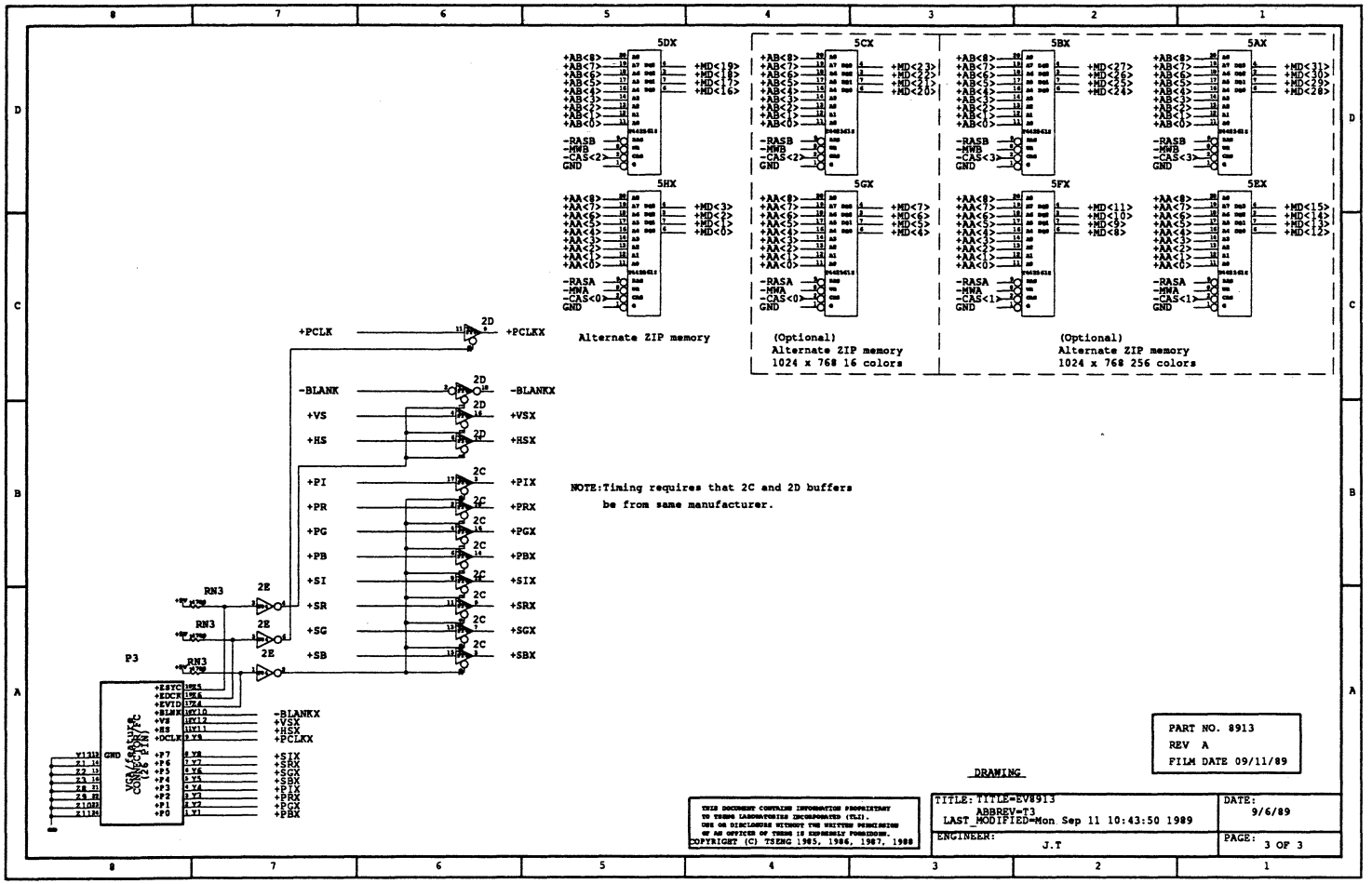


FIG. 2.1-1 TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — AT BUS — 3 of 3

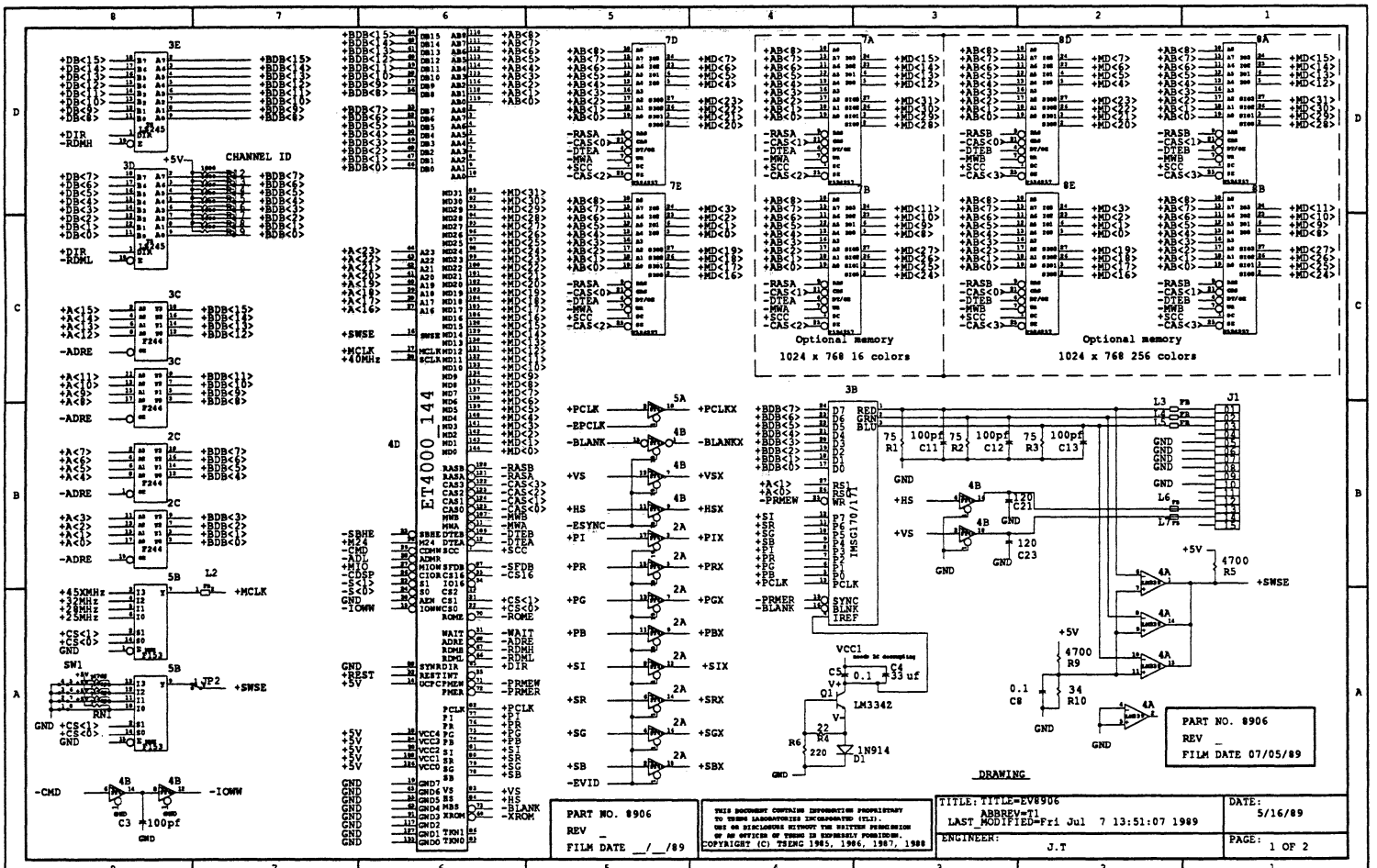


FIG. 2.1-1a TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — MICRO CHANNEL BUS — 1 of 2

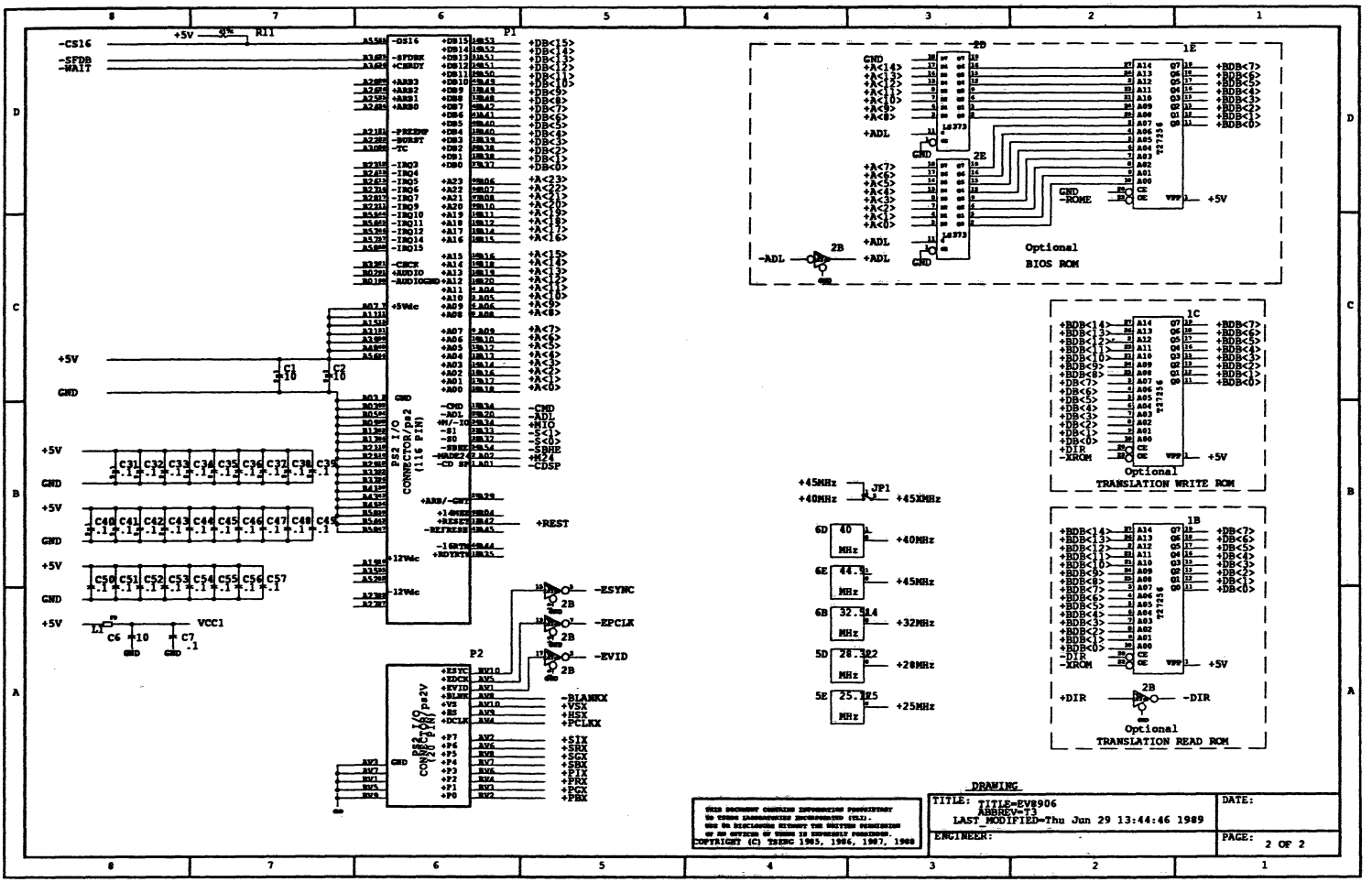


FIG. 2.1-1A TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — MICRO CHANNEL BUS — 2 of 2

The ET4000 is a highly integrated, highly flexible single-chip controller that can propel a video design using a minimum number of components. A complete VGA design can use as few as 9 chips configured with only two 1MB DRAMs. The ET4000 requires no additional support chips to interface to the PC/AT and MCA busses. This means it uses less space and fewer overall components, and provides high performance, high reliability, and reduced cost. These attributes make the ET4000 ideal for video subsystem motherboard integration. Delivering resolutions up to 1024x768 with 256 simultaneous colors, interlaced or non-interlaced display scan, greater flexibility is provided for interfacing with a wide assortment of monitors.

The ET4000 can be easily programmed and configured to function as a VGA/EGA/CGA/MDA controller with only two 100ns 1MB DRAMs, and the typical board-level configurations based on the ET4000 chip described below.

As shown in Figs. 2.1-1 (standard PC/AT bus) and 2.1-1a (Micro Channel bus), a basic configuration consists of a single memory bank as display buffer, the ET4000 VLSI chip, an external color look-up DAC (Digital to Analog Converter), and data/address buffers/multiplexers as support logic.

The PS/2 Video connector allows interfacing to a color or monochrome monitor. The CPU bus interface shown in Fig. 2.1-1 is based on the IBM PC/XT bus timing, and Fig. 2.1-1a is based on the IBM PS/2 MCA bus timing.

Both configurations can be programmed, via a single register, to be 100% register-level compatible with a VGA/EGA/CGA, or MDA controller. All of the VGA/EGA text and graphic modes are supported, and all of the VGA/EGA hardware assist features including data latching, bit mask, rotation, logical functions and plane-selects are provided at a register-compatible level.

Major Components include:

2.1.1 ET4000 VLSI Chip

All major components of the ET4000 are contained within a single 144- or 160-pin Plastic Flat Package. The following is breakdown of the major elements of the ET4000 controller.

CRT Controller (CRTC)

The ET4000 internal CRT Controller (CRTC) provides an 18-bit linear address cursor control and VS and HS controls to external raster-scan CRT displays. Internally, CRTC derives all reference timing in two dimensions: the horizontal display/blanking/sync and vertical display/blanking/sync. Each cycle in horizontal and vertical is evolved around the ET4000's CHARACTER and LINE reference logic. Each character is based on multiple of 8 or 9 MCLK. Both CHARACTER and LINE reference logic can be asynchronously initialized via the SYNR input pin.

Memory Control Unit (MCU)

The Memory Control unit consists of four parts:

Memory control: RAS/CAS/MW/DTE/SCC timing/sequence control; the trp (RAS pre-charge), trcd (RAS to CAS delay), tcas (CAS pulse width), and tcp (CAS pre-charge), are programmable via RCONF register.

Memory address: provides up to 1 megabyte addressing space via AB(8:0) and AA(8:0).

Memory data: provides from 8-bit display memory data width to 32-bit data width via MD(31:0) data interface.

Memory refresh: programmable refresh frequency via CRTC Indexed Register 36.

System Priority Control (SPC)

The SPC's main task is to orchestrate the ET4000's internal resources requests including: the FIFOs, Graphics Data Controller, Cache Controller, and RAM refresh. The system performance is based on two major factors: the ATC demand, i.e.; the display resolution and color; and the memory bandwidth, i.e.; the memory bus width and access time.

Other factors also can contribute to the overall performance. For example, the cache controller can be optimized for sequential access and CPU write operations. The 16-bit CPU bus interface also results in faster data transfer, particularly in the plane graphics mode (a 16-bit CPU write = up to a 64-bit data transfer). For further discussion refer to Memory Design Considerations, section 2.2.3.

Timing Sequencer (TS)

The Timing Sequencer is a set of registers responsible for providing basic timing control for both the CRTC and ATC. Seven of these eight registers are internally indexed, which means that they are accessed via a common I/O address, with one of the seven registers that is selected by the TS Index register. Timings controlled by the TS registers include:

-Horizontal count resolution: 8 or 9 dots/character
-SCLK/2, MCLK/2, MCLK/4, and DCLK/2 (dotclock)
-Video load control: every 8, 16, or 32 dot clocks

Graphics Display Controller (GDC)

The GDC optimizes bit-mapped display memory data manipulation by assisting the CPU in the operation of displaying memory data-related functions. This includes rotate/mask/z-plane, with any of four boolean functions—in response to a single CPU write. By putting basic bit map operations in high-speed hardware, the ET4000 dramatically increases graphics processing throughput over software-driven solutions. The data manipulation capability implemented in the GDC is, however, applicable only for Plane systems and not for Linear Byte systems. This is because all the processing functions are designed to manipulate pixel data with one bit sourced from each plane. For example, the color compare function allows four bits across four planes (one pixel) to be compared to a pre-defined color, thereby allowing eight pixels to be color-compared simultaneously by processing 32 bits of video data (one byte from each plane).

Attribute Controller (ATC)

The internal Attribute Controller (ATC) provides flexible high-speed video shifting and attribute processing, designed for both text and graphics video display applications. The ATC can process up to 16-bits of display data at the rate of 45MHz or 8-bit display data at a rate of 84MHz. In graphics modes, memory bits are reformatted into pixel color data in groups of 16, 8, 2, or 1 adjacent bits, translated through an internal 16-element color look-up table, and sent out serially to the video display. Through this pixel mapper, the ATC supports "PLANE" (for 16 colors), "BYTE" (256 colors) and "WORD" (65,536 colors) oriented pixel structures.

In text mode, eight bits of character code data and eight bits of attribute data are loaded; the character code is used as a lookup into a font table that is then loaded as the 16 bits of font data. The attribute is then applied to the font/cursor data, translated through the color lookup table, and sent out serially to produce 16 colors of text data at speeds of up to 56MHz.

In high resolution modes, the SRC⟨0⟩ bit in the ATC auxiliary register will, when set to 1, process the pixel at half the MCLK rate internally and provide the full pixel clock (PCLK) at the same rate as MCLK. The high-resolution modes should be used when the desired PCLK is greater than 45MHz. Refer to the ET4000's BIOS mode tables starting in section 3.2.4.

2.1.2 Support Logic

Display Memory

In the basic configuration, 256KB of memory is needed as the display buffer. To support IBM-compatible 16-color graphics, a Plane system is employed where the 256KB of display buffer can be viewed as four simultaneously addressable bit planes of 64KB each. (See section 3.2.2 Two Major Types of System Configurations, for definitions of system configurations.) Each pixel is represented by four bits from the four planes, selecting up to 16 colors. To support 256 colors, a Linear Byte system is employed whereby the memory are mapped as a linear byte-oriented memory of 256K in depth. Each pixel is represented by one single byte, selecting up to 256 colors. Note that, in a linear byte system, the physical addressing space is four times greater than in the plane system. There is a memory Segment Select Register to provide all addressable points.

In summary, the memory interface consists of:
- 2 RAS (RASAL, RASBL), 4 CAS (CASL⟨3:0⟩)
- 2 Memory output transfer (DTEBL, DTEAL)
- 2 Memory output enable (SOEBL, SOEAL)*
- 2 Serial clock control (SCC)
- 2 Memory write (MWBL, MWAL)
- 32-bit memory data bus (MD⟨31:0⟩)
- 18-bit memory multiplexed address bus (AB⟨8:0⟩ and AA⟨8:0⟩)

* Derived from CAS⟨3:2⟩

On reading, an 18-bit address is used to access each of the 1024KB deep memory, with up to 32 bits read from memory. On writing, any one of four memory planes from either bank can be written by proper control of RASBL, RASAL, CASL⟨3:0⟩ and MWBL/MWAL lines.

Host Interfaces

Address buffers are needed to multiplex the host processor's lower 16-bit address, A⟨15:0⟩, so that they can be time-multiplexed over the 16-bit address/data bus (DB⟨15:0⟩) into the ET4000 chip. The address input enable signal (ADREL) is generated by the ET4000 to enable the 16-bit addresses onto ET4000's DB⟨15:0⟩ bi-directional data bus at the beginning of each memory or I/O operation.

Two bi-directional bus transceivers (LS245) are required to interface the upper DB⟨15:8⟩ and lower DB⟨7:0⟩ data bus from the host processor. Three separate control signals, RDMHL, RDMLL, and DIR, are provided to enable the transceivers and determine their direction, respectively.

Master Clock Select

A variable Master Clock (MCLK) (14-65MHz), is used internally by the ET4000 to derive the video, vertical, and horizontal timing for the various video modes. Depending on the video monitor and display timing desired, up to eight different frequencies can be selected using an external multiplexer as shown in Fig. 2.1-1. The clock source is controlled by clock select signals (CS⟨2:0⟩) generated by the ET4000 as programmed. (See also section 4.3, CRTC Indexed Register 34: 6845 Compatibility Control Register.)

System Clock Select

The System Clock (SCLK) is required to sequence the ET4000's internal control logic. In addition, the SCLK is used to produce the memory interface control timing: RAS, CAS and MW etc.

The SCLK also affects the overall "balance" of the ET4000's performance. Therefore, designers must fully understand the effect of SCLK when cost/performance trade-offs are considered. In general, the SCLK's cycle time should be equal to the CAS low pulse width and less than 25ns. (See also section 4.3, CRTC Indexed Register 32: RAS/CAS Configuration.)

External Color Look-up DAC

An external Palette RAM with Digital-to-Analog Converter (DAC) is used to translate 8- or 16 bits of digital video signal into the three Analog outputs (R, G, B).

For complete Palette RAM interface, the following output pins are available from the ET4000:

PMERL, PMEWL, PCLK, MBSL, SI, SR, SG, SB, PI, PR, PG, PB

2.1.3 ET4000 BIOS ROM

The ET4000 BIOS ROM contains modules that provide generic video BIOS functions to support both VGA- and EGA-compatible modes. (See section 3.2.4 for operation modes.) When the BIOS ROM option is employed, the CPU reads the BIOS ROM during the bootstrap operation, and the ROM Enable signal (ROMEL) will be activated to enable the ROM data onto the DB bus, with the DIR signal driven high to allow the ROM data to be read by the host processor.

2.2 Board-level Design Considerations

The following are some additional notes for board-level designs using the ET4000.

2.2.1 Display Support and Video Timing

VGA-compatible video subsystems are used as an example here to discuss display support and video timing for an ET4000-based video design. The VGA-compatible video subsystem supports attachment of 31.5kHz horizontal sweep frequency direct-drive analog displays. These displays have a vertical sweep frequency capability of 50 to 70 cycles per second, providing extended color and sharpness and reduced flicker in most modes. The following table summarizes the VGA-compatible analog display and high-resolution interlaced monitor characteristics.

Parameter	Color	Monochrome	HiRes Color (Interlaced)
Horizontal Scan Rate	31.5kHz	31.5kHz	35.5kHz
Vertical Scan Rate	50 to 70 Hz	50 to 70 Hz	43.5 Hz
Video Bandwidth	28MHz	28MHz	44.9MHz
Displayable Colors*	256/256K Max.	64/64 Shades Gray	256/256K Max.
Max. Horiz. Resolution	720 PELs	720 PELs	1024 PELs
Max. Vert. Resolution	480 PELs	480 PELs	768 PELs

* Controlled by Video Circuit

All IBM-compatible VGA/EGA modes have the same horizontal sweep rate. The vertical height of the display is controlled by the polarity of the vertical and horizontal pulses. This is done so that 350, 400, or 480 lines can be displayed without adjusting the height of the display.

The BIOS sets the ET4000 registers to generate the video modes. The video modes are shown in tables 1.1-1 and 1.1-2. All of these modes are 70 Hz vertical retrace except for modes 11 and 12. These two modes are 60 Hz vertical retrace. The ET4000 generates timings that are within the specifications for the supported displays using these modes.

The VGA-compatible analog displays operate from 50 to 70 Hz vertical retrace frequency. The following timing diagrams represent only the vertical frequencies set by the BIOS.

VSYNC Polarity	HSYNC Polarity	Vertical Size
+	+	768 lines
+	-	400 lines
-	+	350 lines
-	-	480 lines

Signal Time	Typical
1	2.765 milliseconds
2	11.504 milliseconds
3	0.985 milliseconds
4	14.268 milliseconds
5	0.064 milliseconds

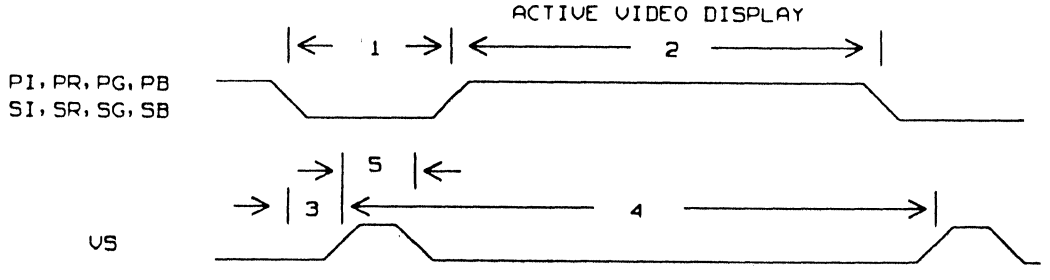


FIG. 2.2.1-1 DISPLAY VERTICAL SYNC, 350 LINES

Signal Time	Typical
6	1.112 milliseconds
7	13.156 milliseconds
8	0.159 milliseconds
9	14.268 milliseconds
10	0.064 milliseconds

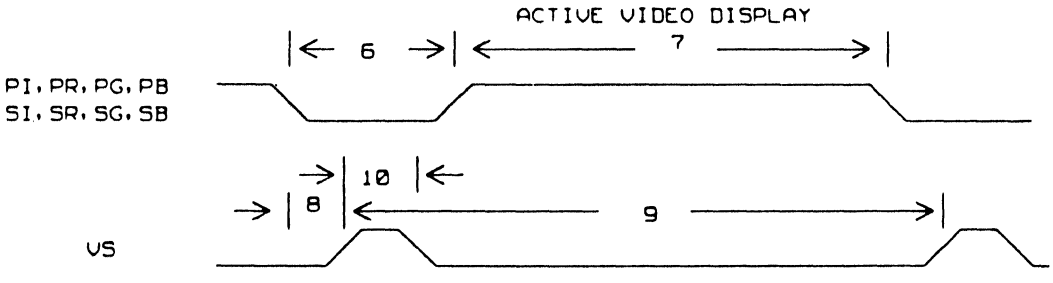


FIG. 2.2.1-2 DISPLAY VERTICAL SYNC, 400 LINES

Signal Time	Typical
11	0.922 milliseconds
12	15.762 milliseconds
13	0.064 milliseconds
14	16.683 milliseconds
15	0.064 milliseconds

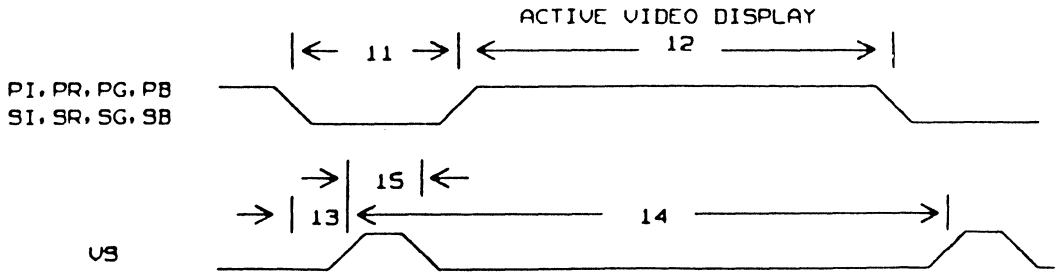


FIG. 2.2.1-3 DISPLAY VERTICAL SYNC, 480 LINES

Signal Time	Typical
16	5.720 microseconds
17	26.058 microseconds
18	0.318 microseconds
19	3.813 microseconds
20	1.589 microseconds
21	31.778 microseconds

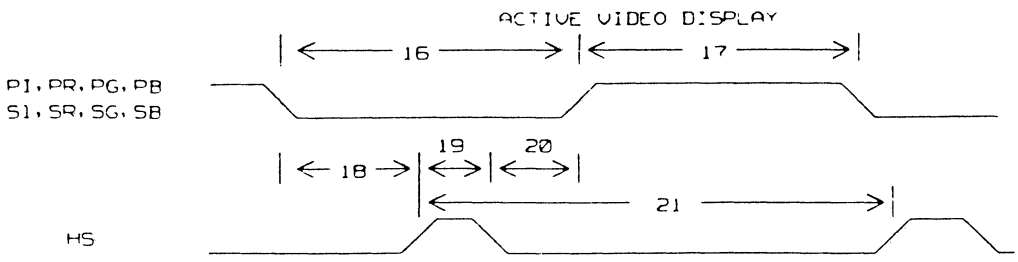


FIG. 2.2.1-4 DISPLAY HORIZONTAL TIMING, 80 COLUMN WITH BORDER

Signal Time	Typical
22	6.356 microseconds
23	25.422 microseconds
24	0.636 microseconds
25	3.813 microseconds
26	1.907 microseconds
27	31.778 microseconds

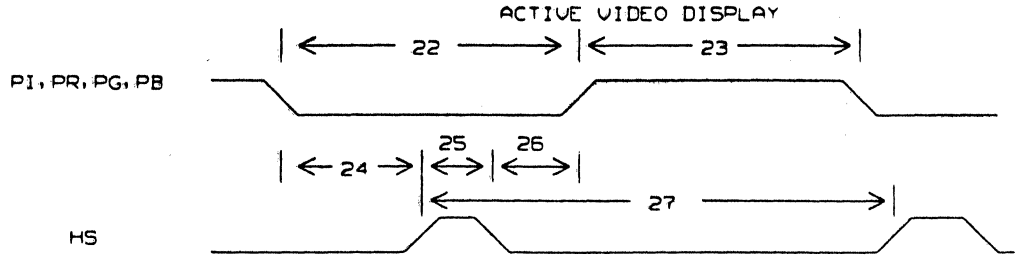


FIG. 2.2.1-5 DISPLAY HORIZONTAL TIMING, 40/80 COLUMN, NO BORDER

Signal Time	Typical
28	1.38 microseconds
29	21.62 microseconds
30	0.014 microseconds
31	23.0 microseconds
32	0.112 microseconds

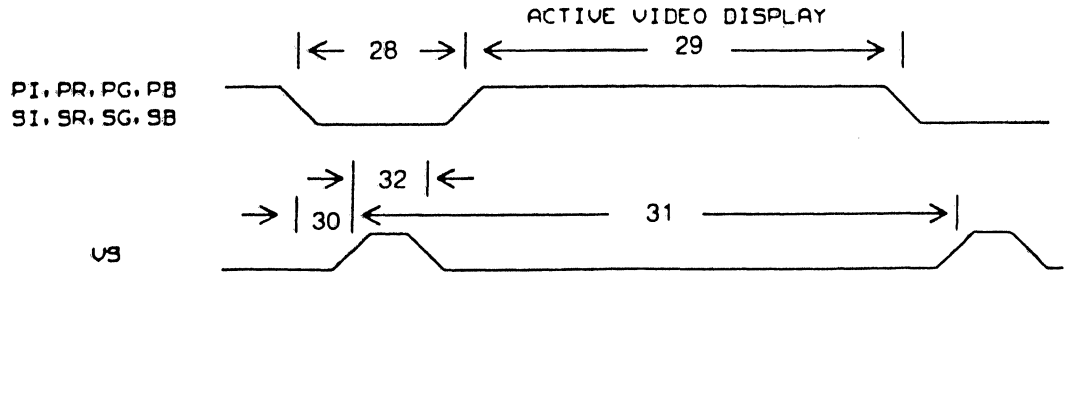


FIG. 2.2.1-6 DISPLAY VERTICAL SYNC TIMING, 768 LINES

2.2.2 Selection of Clock Frequency of MCLK

The MCLK can be selected by programming the Miscellaneous Output Register (I/O address = 3C2) bits (3,2) = Clock select CS⟨1,0⟩ (Refer to Fig. 2.1-1). The recommended hardware connection, and programming of the CS⟨1,0⟩ bits are shown below:

Clock Inputs	Selected By	Type
CK1 = 25.175MHz	CS⟨1,0⟩ = 00	VGA mode
CK2 = 28.322MHz*	= 01	VGA mode/CGA*
CK3 = 32.514MHz	= 10	EGA* mode
CK4 = 40.0MHz	= 11	Extended mode

* Use MCLK/2 internally to yield half MCLK.

The ET4000 provides one additional clock select CS⟨2⟩ for up to eight clock sources; CRTC Indexed Register 34 Bit 1, clock select CS⟨2⟩, when used in conjunction with CS⟨1:0⟩.

2.2.3 Memory Design Considerations

Memory type considerations:

ET4000 supports the following memory type and sizes:

	Size	Min. #	Max. #	Total Size (Max)
DRAM	64K x 4	2*	8	256K x 8
DRAM	256K x 4	2	8	1024K x 8
VRAM	256K x 4	2	8	1024K x 8

* supports CGA/MDA/HERC modes only

During the power-up sequence, the BIOS determines the memory type and number of available memory devices: (assuming SCLK = 40MHz)

Memory Width/Depth Determination

```
testmem(p) /* return 1 if there is display memory *p, else 0 */
char far *p;
{       int i:
  for (i=0; i<=40); i=i+8)p[i]=0x55;          /* write extra locations so char *p */
  if (*p!=0x55) return (0);                   /* will no longer be in cache */
  for (i=0; i<=40; i=i+8)p[i]=0xAA;
  if (*p!=0xAA) return (0);
  return (1);
}

  char far *fp=0xA000000L;                    /*A000:0000 */
  int memory__config;

start:
  /* set to linear graphics mode */

  outp(0x3C4,2);outp(0x3C5,0xF);              /* TS 2: enable all planes */
  outp(0x3C4,4);outp(0x3C5,0xC);              /* TS 4: chain 4, not odd/even */
  outp(0x3CE,1);outp(0x3CF,0);                /* GDC 1: no set/reset */
  outp(0x3CE,3);outp(0x3CF,0);                /* GDC 3: no rotate/func */

  outp(0x3CE,5);outp(0x3CF,0x40)              /* GDC 5 write/read mode 0 */

  outp(0x3CE,6);outp(0x3CF,5)                 /* GDC 6 memory map=A0000h for
                                                 64K, graphics mode */
  outp(0x3CE,8);outp(0x3CF,OxFF);             /* GDC 8; bitmask=all bits */
  outp(0x3CD,0);                              /* select segment 0 */

  /* determine memory width here */
  /* assume the KEY is on ! */
  outp(0x3D4,0x37);                           /* CRTC VSCONF2 */
  outp(0x3D5,3);                              /* assume 32-bit */
  if (testmem (fp+3)) memory__config=3;
                                              /* test if memory in I plane (offset 3) */
  else {
    outp(0x3D4,0x37);                         /* CRTC VSCONF2 */
    outp(0x3D5,2);                            /* assume 16-bit */
    if (testmem (fp+3)) memory__config=2;
                                              /* test if memory in I plane (offset 3) */
```

```
    else {
      outp(0x3D4,0x37);                    /* CRTC VSCONF2 */
      outp(0x3D5,1);                       /* assume 8-bit */
      if (testmem (fp+3)) memory_config=1;
      else error("Minimum 8-bit of memory not found");
      }
  }
/* all width has been set, and determine memory depth here */
switch (memory_config) {
  case 1 :                                 /* 8-bit */
    outp(0x3CD,0x22);                      /* read/write segment 2,
                                              @128K boundry */
    break;
  case 2 :                                 /* 16-bit */
    outp(0x3CD,0x44);                      /* read/write segment 4,
                                              @256 boundry */
    break;
  case 3 :                                 /* 32-bit */
    outp(0x3CD,0x88);                      /* read/write segment 8,
                                              @512K boundary */
    break;
  }
if (testmem (fp))memory_config |= 8;       /* Set to 1MB memory else set
                                              to 256K memory */

/* now set the register */
outp(0x3D4,0x37);
outp(0x3D5,memory_config);
```

Memory Type Programming

```
outp(0x3D4,0x32);                          /* CRTC RCCONF */
outp(0x3D5,0x70);                          /* use -10 memory */

/* some examples of memory timing: refer to Figure 2.3.2-2
 * 0x70: Trcd=75ns,Trsw=100ns,Trsp=75ns,Tcsw=25/50ns,Trc=200ns
 * 0x28: Trcd=75ns,Trsw=100ns,Trsp=75ns,Tcsw=25ns,Trc=175ns
 * 0x09: Trcd=50ns,Trsw=100ns,Trsp=75ns,Tcsw=50ns,Trc=175ns
 */
```

Memory resource considerations:

Depending on the intended modes of operations and operating clock frequencies, memory devices of different access times may be employed for the display buffer. The system clock (SCLK) is used to derive all display memory related timings.

The display memory in conjunction with the ET4000's Memory Control Unit (MCU) provide the supply side of system resources within a video subsystem. These resources consist of the number of display memory's I/O pins connected to the ET4000's DM(31:0) bus; the speed of the memory, including both the random access RAS cycle and the page mode CAS cycle; and whether DRAM or VRAM is being used.

The ET4000 supports up to eight 256K x 4 or 64K x 4 display memory devices. The total resource is represented in bit/ns. Consider the following:

SCLK = 40MHz and, 8 256K x 4 DRAM with RAS cycle time of 175ns and CAS cycle time of 50ns

Resource maximum = (8 x 4) bit/50ns or .64 bit/ns
Resource minimum = (8 x 4) bit/175ns or .183 bit/ns
Resource under ET4000's SPC controller with resource management efficiency of K = .85, then the resource of the ET4000 is approximately:

Resource ET4000 = .85((.64 x 14) + (.183 x 2)) /16 bit/ns or .495 bit/ns

NOTE: It is advisable to always keep the Tcas and Tcsp to 1 SCLK clock period.

Consider next, the system demands, taken in two parts: First the display requirements and then the CPU requirements.

Display requirements:

PCLK = 65MHz
Resolution = 1024 x 768
Color = 256
Display to scan line ratio = .8

then:
Demand disp = 8 x .8 bit x 65MHz or .416 bit/ns

therefore: the available resource Ra to CPU is the difference between Resource ET4000 and Demand disp:

Ra = (.495 -.416) bit/ns or .079 bit/ns

CPU requirements:

Using the above conditions, with the CPU performing a 16-bit write to display memory at a rate of one access every 200ns, the ET4000 is likely to keep up with CPU's demand with zero wait state. Furthermore, the designer should consider the proper memory resource requirements for the worse case display mode, with reasonable CPU performance.

Another important aspect of the memory design, from a reliability viewpoint, is that it is possible to reconfigure the video memory to fulfill minimum requirements via the BIOS when some memory defect occurs.

2.2.4 Extending BIOS ROM Address Space

The ET4000 is designed to decode C0000-C5FFF; C6800-C7FFF (hex) as the EROM address space on power-up, providing 30KB code size for the ET4000 BIOS ROM modules. This address space can be redefined to a full 32KB by programming TS Index Register 7 (TS Auxiliary Register) bits 5 and 3.

If the BIOS ROM is part of the main "motherboard" BIOS, then bits 5 and 3 of TS Indexed Register 7: Auxiliary Mode should be set to 0,1, thus disabling the decoding of ROM BIOS address space.

2.2.5 Translation of CRTC Index Registers and Clock Frequency

In order to support various video modes on a variety of monitors, the CRTC data registers and the Miscellaneous Output register need to be programmed accordingly to provide proper timing for the display. The ET4000 is designed to provide such adjustments via the hardware. The mechanism of translating the CRTC registers and Miscellaneous Output register is described in the following pages.

Translation of CRTC data registers

Two alternatives are provided to allow the CRTC registers to be re-programmed to the desired values: (1) use of external translation ROM, (2) use of Non-Maskable Interrupt (NMI). These two approaches are further described as follows:

Use of Translation ROM:

Hardware configuration - (refer to board schematic, Figs. 2.1-1; 2.1-1a)

- ET4000 output pin "XROML" (active low) shall be used to enable both the read/write translation ROMs.
- ET4000 data bus bits 14 to 8 (BDB⟨14:8⟩) and the lower byte of the CPU data bus (DB⟨7:0⟩) (total of 15 bits) shall be used to address 32K bytes of write translation ROM
- ET4000 data bus bits 14 to 8 (BDB⟨14:8⟩) and the lower byte of the ET4000 data bus (BDB⟨7:0⟩) (total of 15 bits) shall be used to address 32K bytes of read translation ROM
- 8-bit data output of the write translation ROM shall be fed back to source the lower 8 bits of ET4000 data bus (BDB⟨7:0⟩)
- 8-bit data output of read translation ROM shall be fed back to source the lower 8 bits of the CPU data bus (DB⟨7:0⟩)
- The DIR output from the ET4000 should be used to enable the write translation ROM
- The DIR output from the ET4000 with logical inversion should be used to enable the read translation ROM

Programming requirements -

- 6845 Compatibility Control Register (CRTC Index 34) bit 5 = 1, to enable write translation mode
- 6845 Compatibility Control Register (CRTC Index 34) bit 4 = 1, to enable read translation mode
- Video System Configuration Register (CRTC Index 36) bit 7 = 0, to disable 16-bit I/O operation
- Feature Control Register (Port 3#A) bit 7 = 0 or not in 6845 mode

Theory of operation -

After the above programming, translation via use of read/write translation ROM is enabled:

In EGA/VGA modes:

Any I/O read/writes to the CRTC Index registers 0—1F, (port address = 3#5) will cause translation to occur as follows:

-BDB⟨15:8⟩ will be sourced by ET4000 (during XROML active) as follows:

BDB⟨15⟩ = TS Index 7 bit 7
BDB⟨14⟩ = CRTC Index 34 bit 7 (complemented)
BDB⟨13⟩ = Misc. Output Register bit 2
BDB⟨12:8⟩ = CRTC Index value to be written

-The translation ROM enabled by XROML goes from 1 to 0, BDB⟨15:8⟩ (sourced from ET4000) and DB⟨7:0⟩ (sourced from CPU) will address the translation ROM for the desired value to be written to the CRTC index register. See Fig. 2.2.5-1.

Similarly, an I/O write to the Miscellaneous Output register (port address 3C2) will cause the ET4000 to activate XROML and source BDB⟨15:8⟩, with the exception that BDB⟨12:8⟩ will be sourced as "11010", to access a desired value for the Miscellaneous Output register (MISCOUT).

Note that the CS⟨0⟩ bit (contained in the MISCOUT register) is also an address input to the translation ROM. The MISCOUT register should be set prior to setting the CRTC values in order to select the proper EGA-to-PS/2 translation table (see Figure 2.2.5-1). Since the table to be used is unknown when the MISCOUT register is set, identical values should be in both tables at index 1A (from which the MISCOUT register is translated).

The translation of the MISCOUT allows the clock select bits (bits 2,3) and horizontal and vertical sync polarity bits (bits 6,7) to be properly adjusted.

In CGA modes:

Any I/O writes to CRTC Index registers 0—F will cause the above translation to occur, allowing the 16 CRTC registers to be automatically adjusted.
Note that BDB⟨12⟩ = CRTC Index Register 24 bit 0.

Use of Non-Maskable interrupt:

Hardware configuration -

- Output pin XROML shall be connected to the NMI input to the processor, which is a tri-state output that will go active low, to generate NMI when CPU writes to CGA/MDA mode register (3#8)

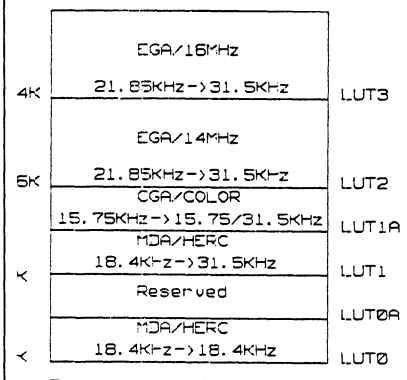
Programming requirements -

- 6845 Compatibility Control Register (CRTC Index 34) bit 7=1, to enable 6845 emulation
- 6845 Compatibility Control Register (CRTC Index 34) bit 5=0, to disable translation mode
- Feature Control Register (Port 3#A) bit 7=1, to enable generation of NMI

Theory of operation -

After the above programming, a NMI to the processor is enabled:

A mode switching (writing to the 6845 MODE register) will generate an NMI active low pulse to the processor, allowing all the CRTC index registers to be re-programmed by the interrupt service routine. Note that once the NMI is invoked, CRTC Index 0 - 9 will be write protected.




```
case A: EGA -> PS/2 analog monitor:
        Translate ROM mapping = LUT2 or 3
        Index 34= 2D or 21

case B: CGA -> PS/2 analog monitor:
        Translate ROM = LJT1A
        Set I/O port 03DE=01 (double scan)
        Select MCLK = 28 MHz
        Set bit 7 & 6 of Miscellaneous Output Reg = 0 1
        Index 34= E1
case C: CGA -> CGA/EGA  monitor:
        Translate ROM = LJT1A
        Select MCLK = 28/2 (14MHz)
        Set bit 7 & 6 of Miscellaneous Output Reg = 0 0
        Index 34= A1
case D: MDA/HERC -> PS/2 analog monitor:
        Trans ate ROM = LJT1
        Select MCLK = 28 MHz (MISCRW bit 2 = 1)
        Set bit 7 & 6 of Miscellaneous Output Reg = 1 0
        Index 34= A0

case E: MDA/HERC -> TTL monochrome monitor:
        Translate ROM = LJT0
        Select MCLK = 16 MHz (MISCRW bit 2 = 0)
        Set bit 7 & 6 of Miscellaneous Output Reg = 1 0
        Index 34= A0
```

FIG. 2.2.5-1 TRANSLATION ROM

2.2.6 16-bit Data Bus Interface

Programming requirements -

- Video System configuration Register (CRTC Index 36) bit 6 = 1, to enable 16-bit display memory access.
- Video System configuration Register (CRTC Index 36) bit 7 = 1, to enable 16-bit I/O access.

To support this 8-bit/16-bit interface, the hardware configuration is shown as in the board schematic (See Figures 2.1-1, 2.1-1a). The signals "SBHEL" and "A⟨0⟩" are inputs to the ET4000 to identify whether an 8-bit/16-bit read/write operation is intended. The ET4000 will respond to 16-bit bus operation via the CS16L/IO16L output pins. In the case of 16-bit I/O access, the leading edge of IOWWL input must ensure proper data set-up time as specified.

2.3 I/O Pin Description

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
Clock Interface					
MCLK	17	18	I	TTL	A variable frequency clock used to generate the necessary video, vertical and horizontal timing for the ET4000. Various video clocks can be selected as the proper clock frequency, by the output clock select signals CS⟨2:0⟩ from ET4000 depending on the display mode programmed by the host processor.
SCLK	20	23	I	TTL	System clock used to generate all memory timing and ET4000's internal states.
General Host Interface					
CDMWL	29	33	I	CMOS Schmitt-Trigger	PC: A low active memory write request generated by a host microprocessor, to write into the Display Memory. MC:Command, a low activate command input for read/write cycle.
ADMRL	28	32	I	CMOS Schmitt-Trigger	PC: A low active memory read request generated by a host microprocessor, to read the Display Memory or BIOS ROM. MC:Address/Status latch control input.
MIOWL	27	31	I	CMOS Schmitt-Trigger	PC: A low active I/O write request generated by a host microprocessor, to write to the ET4000 control registers. MC:Memory/Input Output, when this signal is high,it indicates a memory cycle. A low indicates an I/O cycle.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
CIORL	26	29	I	CMOS Schmitt-Trigger	PC: A low active I/O read request generated by a host microprocessor, to read the ET4000 control registers. MC:Card Setup input driven by system board.
IOWWL	15	16	I	TTL	PC: A low active I/O write request derived from IOW command. MC:A low active I/O write request derived from CMD command. **NOTE:** This input is used only if: 16-bit I/O is enabled and the DB⟨15:0⟩ set-up time to IOW (PC bus) or CMD (MC bus) command is less than the specified timing requirement. Otherwise, this input can be terminated with a logical 0.
A⟨23:16⟩	44,43, 42,41, 40,39, 38,37	48,47, 46,45, 44,43, 42,41	I	TTL	Upper 8 bit address bus interfaced to an external host microprocessor.
M24	36	40	I	TTL	Extended address enable. This line must be driven active high during all memory accesses.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
DB⟨7:0⟩	53,52, 51,50, 49,48, 47,46	58,57, 56,55, 54,53, 52,51	I/O	TTL/TS	Data bus, 8-bit address/data time multiplexed bus, interfaced to an external host microprocessor. INPUTS lower 8-bit processor address, 8-bit lower data (memory or I/O writes) or OUTPUTS lower 8-bit data (memory or I/O reads) for memory or I/O operations initiated by host processor. During power-up RESET low to high transition, state of DB⟨7:0⟩ are latched internally. For micro channel interface, these 8-bit latched data are channel ID. Additionally, the bit 0 and 1 of latched data are available to be read back via Status Register Zero for the monitor ID.
DB⟨15:8⟩	64,62, 61,60, 59,58, 57,56	72,69, 68,67, 66,65, 64,63	I/O	TTL/TS	Data bus, 8-bit address/datatime multiplexed bus, interfaced to an external host microprocessor. INPUTS middle 8-bit processor address, 8-bit upper data (memory or I/O writes) or OUTPUTS upper 8-bit data (memory or I/O reads) for memory or I/O operations initiated by host processor.
WAITL	31	35	O	TTL/TS	A low active signal generated to asynchronously stretch the host microprocessor during memory read/write and I/O (in micro channel) operations.
ADREL	68	76	O	TTL	Low active enable signal, enables the lower 16-bit processor address signals for the DB⟨15:0⟩ inputs.
RDMHL	67	75	O	TTL	A low active signal, used to enable upper 8-bit of external bi-directional bus drivers connecting the Data Bus (DB⟨15:8⟩) to the data bus of the host microprocessor.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
RDMLL	66	74	O	TTL	A low active signal, used to enable lower 8-bit of external bi-directional bus drivers connecting the Data Bus (DB⟨7:0⟩) to the data bus of the host microprocessor.
DIR	65	73	O	TTL	A signal used to control the direction of bidirectional drivers connecting the Data Bus (DB⟨15:0⟩) to the data bus of the host microprocessor. A logical 1 will be generated during memory and I/O reads to allow the ET4000 to drive the data bus. A logical 0 will be generated during write operations, allowing the ET4000 to receive data from the host.
CS16L	35	39	O	TS	This is the -CD DS16 (n) signal for identifying a 16-bit memory device on the PC/MC microprocessor bus and I/O device on the MC microprocessor bus. This signal shall be high impedance for 8-bit data transfers, and low for 16-bit data transfers. This signal should be pulled high using a 1K resistor in microchannel applications to conform to Micro Channel specifications.
IO16L	34	38	O	TS	This is the -CD IO16 (n) signal for identifying a 16-bit I/O device on the PC microprocessor bus. This signal shall be high impedance for 8-bit data transfers, and low for 16-bit data transfers.
REST	32	36	I	TTL	High active system reset signal generated by the host processor to reset the ET4000's internal registers.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
AENL	30	34	I	TTL	Low active I/O address valid enable signal.
SBHEL	33	37	I	TTL	An input signal to the ET4000 which, along with A⟨0⟩, identify whether an 8- or 16-bit read/write operation is intended.
SFDBL	87	96	O	TTL	Card Select Feedback, active low output to indicate to micro channel host the availability of ET4000's Memory and I/O resources. PC Mode: 16-bit Memory Access Enable. This signal can be used to generate early CS16 if required in certain high-speed motherboard designs.
S⟨1:0⟩	23,24	26,27	I	TTL	Status bit 1 and 0: These lines defines the current cycle is read or write. **NOTE:** In PC bus configuration, these lines should be terminated to logical 0.
DRAM/VRAM Memory Interface					
RASAL	121	134	O	TTL/TS	DRAM: Row address AA⟨8:0⟩ latch control for lower memory plane pairs MD⟨15:0⟩. VRAM: Row address AB⟨8:0⟩latch for first 512KB memory bank A. **NOTE:** AA⟨8:0⟩ is not used in VRAM configuration.
RASBL	120	133	O	TTL/TS	DRAM: Row address AB⟨8:0⟩ latch control for upper memory plane pairs MD⟨31:16⟩. VRAM: Row address AB⟨8:0⟩ latch for first 512KB memory bank B.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
CASL⟨0⟩	125	138	O	TTL/TS	DRAM: Column address AA⟨8:0⟩ latch control for lower plane MD⟨7:0⟩. VRAM: Column address AB⟨8:0⟩ latch control for lower 8-bit memory plane MD⟨7:0⟩.
CASL⟨1⟩	124	137	O	TTL/TS	DRAM: Column address AA⟨8:0⟩ latch control for lower plane MD⟨15:8⟩. VRAM: Column address AB⟨8:0⟩ latch control for upper 8-bit memory plane MD⟨15:8⟩.
CASL⟨2⟩	123	136	O	TTL/TS	DRAM: Column address AB⟨8:0⟩ latch control for upper plane pair MD⟨23:16⟩. VRAM: Serial output enable for first 512KB memory bank A.
CASL⟨3⟩	122	135	O	TTL/TS	DRAM: Column address AB⟨8:0⟩ latch control for upper plane pairs MD⟨31:24⟩. VRAM: Serial output enable for second 512KB memory bank B.
MWAL	11	12	O	TTL/TS	Write Command to display memory. DRAM: write control for lower memory planes MD⟨15:0⟩. VRAM: write control for first 512KB memory bank A.
MWBL	107	119	O	TTL/TS	Write Command to display memory. DRAM: write control for upper memory planes MD⟨31:24⟩. VRAM: write control for second 512KB memory bank B.
DTEAL	12	13	O	TTL/TS	VRAM: Low active output enable signal, used to enable VRAM memory access to first 512KB memory bank A, comprised of four 256Kx4 memory devices. DRAM: DRAM's OE input pin to enable the output data bus during a read operation (AA<8:0>).

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
DTEBL	109	121	O	TTL/TS	VRAM: Low Active Output Enable signal, used to enable VRAM memory access to second 512KB memory bank B, comprised of four 256Kx4 memory devices. DRAM: DRAM's OE input pin to enable the output data bus during a read operation (AB⟨8:0⟩).
MD⟨7:0⟩	137,138, 139,140, 141,142, 143,144	153,154, 155,156, 157,158, 159,160	I/O	TTL/TS	DRAM: Memory Data Bus bit 7-0. VRAM: Memory Data Bus bit 7-0.
MD⟨15:8⟩	128,129, 130,131, 132,133, 134,136	143,144, 145,146, 147,148, 149,152	I/O	TTL/TS	DRAM: Memory Data Bus bit 15-8. VRAM: Memory Data Bus bit 15-8.
MD⟨23:16⟩	99,100, 101,102, 103,104, 105,106	111,112, 113,114, 115,116, 117,118	I/O	TTL/TS	DRAM: Memory Data Bus bit 23-16. VRAM: Serial Data Bus bit 7-0.
MD⟨31:24⟩	89,92, 93,94, 95,96, 97,98	98,103, 104,105, 106,107, 108,109	I/O	TTL/TS	DRAM: Memory Data Bus bit 31-24. VRAM: Serial Data Bus bit 15-8.
AA⟨8:0⟩	2,3, 4,5, 6,7, 8,9, 10	2,3, 4,5, 6,7, 8,9, 11	O	TTL/TS	DRAM: Row/Column address time multiplexed bus addressing memory plane pairs MD⟨15:0⟩. **NOTE:** AA⟨8:0⟩ is only used in DRAM configuration.
AB⟨8:0⟩	110,111, 112,113, 114,115, 116,118, 119	122,123, 124,125, 126,127, 128,131, 132	O	TTL/TS	DRAM: Row/Column address time multiplexed bus addressing memory plane pairs MD⟨31:16⟩. VRAM: Time multiplexed row address for both 512KB memory banks A/B.
SCC	1	1	O	TTL/TS	DRAM: High active graphics Status output. VRAM: Serial clock control.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
Display Output Interface					
PCLK	82	91	O	TTL/TS	Pixel clock used to load the video output signals (PI,PR,PG,PB,SI,SR,SG,SB) into the Digital to Analog Converters (DAC). The video output signals shall be loaded using the rising edge of the Pixel clock.
SI	81	89	O	TTL/TS	Secondary intensity, video color look-up table address bit 7.
SR	80	88	O	TTL/TS	Secondary red, video color look-up table address bit 6.
SG	79	87	O	TTL/TS	Secondary green, video color look-up table address bit 5.
SB	78	86	O	TTL/TS	Secondary blue, video color look-up table address bit 4.
PI	77	85	O	TTL/TS	Primary intensity, video color look-up table address bit 3.
PR	76	84	O	TTL/TS	Primary red, video color look-up table address bit 2.
PG	75	83	O	TTL/TS	Primary green, video color look-up table address bit 1.
PB	74	82	O	TTL/TS	Primary blue, video color look-up table address bit 0.
MBSL	73	81	O	TTL/TS	A low signal indicates that a blanking period is active. During this time, the video output lines shall be cleared. This signal shall be used in conjunction with the digital video output to external DAC to produce the required R,G,B analog output.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
PMERL	72	80	O	TTL/TS	Low active select for external Digital to Analog Converter (DAC) register during I/O read.
PMEWL	71	79	O	TTL/TS	Low active select for external Digital to Analog Converter (DAC) register during I/O write.
VS	83	92	O	TTL/TS	Vertical retrace synchronization signal, supplied to the CRT monitor.
HS	84	93	O	TTL/TS	Horizontal retrace synchronization signal, supplied to the CRT monitor.
General Input Interface					
UCPC	14	15	I	TTL	Bus type select input: when set to a logical 1, the ET4000 will respond to all microprocessor interfaces according to micro channel specification. When this input is set to a logical 0, the ET4000 will respond to all microprocessor interfaces according to PC bus specification.
SYNR	88	97	I	TTL	A active high synchronous reset signal. When this signal is high, it indicates a request to reset the ET4000's internal LINE and CHARACTER counters.
SWSE	16	17	I	TTL	Input status, can be read via input status 0 bit 4.

2.3 I/O Pin Description (continued)

ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION					
SYMBOL	PIN# 144-PIN PFP	PIN# 160-PIN PFP	I/O	TYPE	FUNCTION
General Output Interface					
ROMEL	70	78	O	TTL	Low active signal, used to enable external BIOS ROM.
CS⟨2:0⟩	13,21, 22	14,24, 25	O	TTL	Clock select signal, to select 1 of 8 possible MCLK clock.
TKN⟨1:0⟩	86,85	95,94	O	TTL/TS	Token Status output: TKN⟨1⟩ = ET4000's MCU is processing font cycle. TKN⟨0⟩ = ET4000's MCU is processing pixel cycle. TKN⟨1:0⟩ are redefined if CRTC index 35 bit 5 = 1: TKN⟨1⟩ = interlace mode active. TKN⟨0⟩ = even field.
XROML	69	77	O	TTL	A low active signal. It is used to enable an external translation read/write ROMs.
INTL	25	28	O	TTL/TS	Low active interrupt request signal to host microprocessor.
Power Source Interface					
VSS	19,45, 55,63, 91,117, 127,135	10,21, 22,30, 49,50, 61,62, 70,71, 90,101, 102,110, 129,130, 141,142, 150,151	I	GND	Ground.
VDD	18,54, 90,108, 126	19,20, 59,60, 99,100, 120,139, 140	I	+5V	+5V.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Storage Temperature	-40 to +125 deg C
Operating free-air temperature range	0 to +70 deg C
Supply Voltage Applied to Ground Potential	-0.5 to +7.0 V
DC Voltage Applied to Outputs for High Output State	-0.5 to Vdd max.
DC Input Voltage	-0.5 to +5.25 V
Supply Current	70mA typ 160mA max.

ELECTRICAL CHARACTERISTICS

The following condition Applies Unless Otherwise Specified.

T(A) = 0 to + 70 deg C Vdd = 5.0 V +/- 5%

DC CHARACTERISTICS OVER OPERATING TEMPERATURE

	Min.	Typ.	Max.	Units
V(OH) Output High Voltage I(OH) = 2.0 mA	4.0			Volts
V(OL)Output Low Voltage I(OL) = 4 mA	0.4			Volts
RASAL, RASBL, CASL⟨3:0⟩, PCLK, DB⟨15:0⟩, VS, HS, ADREL = 4 mA*	0.4			Volts
AA⟨8:0⟩, AB⟨8:0⟩, MWAL, MWBL, SCC, SFDBL, WAITL, DIR, CS16L, I016L, INTL = 6 mA*	0.4			Volts
All Others = 2 mA*	0.4			Volts
V(IH)Input High Level I(IH) = +/- 10 μA	2.0			Volts
V(IL)Input Low Level I(IL) = 10 μA			0.8	Volts

*See Addendum 6.1 for ET4000AX Rev. E revised voltages

NOTE: Stress beyond those listed under "Maximum Ratings" may cause permanent damage to the device. Exposure to maximum rated conditions for extended periods may affect device reliability.

Life Support Disclaimer

Tseng Labs, Inc. does not sanction, authorize, or certify any chip-level or board-level products for use in the design, construction, or use in or as critical components of life-support systems or devices. Products of this nature are defined as follows:

a) Life-support systems and/or devices are those which are used to support/sustain life, or are used to the same effect when applied as a surgical implant, and whose failure to perform may result in serious injury or fatality.

b) Critical components are those which are integral and essential to the design and construction of life-support devices which are used to support/sustain life, and whose failure to perform can be expected to significantly reduce the effectiveness of said devices, which may result in serious injury or fatality.

2.3.1 Timing Specification

Refer to timing diagrams shown in Figures 2.3.2-1 to 2.3.2-17

Clock Interface					
No.	Symbol	Description	min.	max.	unit
1	c(MCLK)	MCLK Period	11.9		ns
2	c(SCLK)	SCLK Period	24.0		ns
3	tw(SCLKH)	SCLK High Pulse width	11.5		ns
4	tw(SCLKL)	SCLK Low Pulse width	11.5		ns
5	tw(MCLKH)	MCLK High pulse width	5.5		ns
6	tw(MCLKL)	MCLK Low pulse width	5.5		ns
General Host Interface					
No.	Symbol	Description	min.	max.	unit
10	tw(RESTH)	REST high pulse width	10		ns
11	tw(WAITL)	Wait line low during CPU read/write display memory	0	(*2)	ns
20	td(ROMEL)	Delay from memory read to ROMEL Low	5.6	26.0	ns
21	td(ROMEH)	Delay from memory read to ROMEL High	3.8	17.4	ns
22	td(ADREH)	Delay from Read or Write Command to ADREL High	5.9	22.8	ns
23	td(ADREL)	Delay from Read or Write Command to ADREL Low	3.4	13.0	ns
24	td(XROML)	Delay from Read or Write Command to XROML Low	9.0	42.5	ns
25	td(XROMH)	Delay from Read or Write Command to XROML High	6.0	30.2	ns
26	td(RDMEL)	Delay from Read or Write Command to RDMHL or RDMLL Low	6.8	26.4	ns
27	td(RDMEH)	Delay from Read or Write Command to RDMHL or RDMLL High	5.0	19.1	ns
28	td(DIRH)	Delay from Read Command to DIR High	3.3	16.8	ns
29	td(DIRL)	Delay from Read Command to DIR Low	5.5	24.0	ns
30	td(IORDA)	Delay from I/O Read command to DB out	5	30	ns

2.3.1 Timing Specification (continued)

No.	Symbol	Description	min.	max.	unit
31	td(CSNH)	Delay from MCLK to INTL low to High-Z	8.7	33.7	ns
32	td(CSNH)	Delay from I/O Write Command to CS⟨2:0⟩ High	4.5	28.5	ns
33	td(CSNL)	Delay from I/O Write Command to CS⟨2:0⟩ Low	4.5	29.5	ns
34	td(XRDB)	Delay from XROML low to DB⟨15:8⟩ valid translation ROM address	- 5.0	2.5	ns
40	ts(ADIOWW)	I/O address setup time to IOWWL	10		ns
41	ts(DWRCS)	CPU Write Data set up time	30		ns(*4,6)
42	ts(DRDCS)	CPU Read Data set up time	20		ns(*6)
43	ts(IRDCS)	I/O Read Data set up time	20		ns(*6,11)
44	ts(IWRCS)	I/O Write Data set up time			ns(*6,12)
		16-bit I/O write	5		ns
		8-bit I/O write	10		ns
50	th(IWRCH)	I/O Write Data hold time	10		ns(*6)
51	th(IRDCH)	I/O Read Data hold time	13	20	ns(*6)
52	th(DWRCH)	CPU Write Data hold time	5		ns(*6)
53	th(DRDCH)	CPU read Data hold time	10	20	ns(*6,11)
		PC Bus Host Interface			
No.	Symbol	Description	min.	max.	unit
60	tw(IORWL)	I/O Read or Write pulse width low	30		ns(*3)
61	tw(IORWH)	I/O Read or Write pulse width high	20		ns(*3)
62	tw(MEMRW)	Memory Read or Write Command pulse width low (active)	30		ns(*9,10)
63	tw(MEMRW)	Memory Read or Write Command pulse width high	20		ns
64	td(WAITL)	Delay from Memory Read or Write Command (ADMRL,CDMWL) to WAITL low	6.0	23.4	ns
65	td(CS16L)	Delay from host address to CS16L low	6.4	24.8	ns(*6)
66	td(IO16L)	Delay from host address to I016L	6.0	24.2	ns
67	ts(ADRIO)	Host address setup time to I/O read or write command	10		ns(*6)
68	ts(ADRMIO)	Host address setup time to read or write command	10		ns(*6)
69	th(MEMADR)	Host address hold time from memory read or write command	10		ns(*6)

2.3.1 Timing Specification (continued)

Micro Channel Bus Host Interface					
No.	Symbol	Description	min.	max.	unit
75	tw(ADRLL)	ADMRL pulse width low	10		ns
76	tw(ADRLH)	ADMRL pulse width high	10		ns
77	tw(CDML)	Command (CDMWL) pulse width low	30		ns
78	tw(CDMH)	Command (CDMWL) pulse width high	20		ns
79	tw(S01H)	Status (S0,S1) pulse width high	20		ns
80	td(SCDM)	Command (CDMWL) delay from status	20		ns
81	td(CS16L)	CS16L delay from status (S0,S1) for I/O read or write	5.7	21.8	ns
82	td(SFDS)	SFDBK delay from status (S0,S1)			
		a. for I/O read or write	4.5	17.3	ns
		b. for display memory read or write	6.9	26.5	ns
83	td(WAITL)	WAITL delay from status (S0,S1) low			
		a. for I/O reads and writes	5.7	21.8	ns
		b. for memory reads or writes	7.1	27.0	ns
90	ts(MIOADL)	MIOWL set up time from ADMRL high	10		ns
91	ts(ADRAL)	Host Address setup time to ADMRL low	10		ns(*6)
92	ts(S01ADL)	S0,S1 setup time to ADMRL low	10		ns
93	ts(WRCDM)	Write data setup time to CDMWL high	10		ns(*6)
94	ts(SBHADL)	SBHEL setup time to ADMRL low	10		ns
100	th(WRCDM)	Write data hold time from CDMWL high	0		ns(*6)
101	th(S01ADL)	S0,S1 hold time from ADMRL high	5		ns
102	th(ADRADL)	Host Address hold from ADMRL high	5		ns(*6)
103	th(MIOADL)	MIOWL hold time from ADMRL high	5		ns
104	th(SBEADL)	SBHEL hold time from ADMRL high	5		ns

2.3.1 Timing Specification (continued)

DRAM/VRAM Memory Timing					
No.	Symbol	Description	min.	max.	unit
110	tw(RSW)	RASAL or RASBL Low pulse width	nc- 3.0	nc- 1.5	ns(*4,5,7) n=3-5
111	tw(RSP)	RASAL or RASBL High pulse width	nc+ 1.7	nc+ 2.9	ns(*4,5,8) n=2-5
112	tw(CSW)	CASL Low pulse width	nc- 2.9	nc- 2.1	ns(*4,5)n=1-2
113	tw(CSP)	CASL High pulse width	nc+ 0.8	nc+ 2.5	ns(*4,5) n=1-2
114	tw(MWL)	MWAL or MWBL Low pulse width	nc- 2.9	nc- 1.5	ns(*4,5) n=1-2
119	td(CAC)	Delay from CASL to read data valid	5.0	c+ 5.0	ns(*4,5)
120	td(RCD)	Delay from RASAL or RASBL to CASL	nc- 2.7	nc+ 3.7	ns(*4,5)n=2-3
121	ts(MWL)	MWAL or MWBL CAS set up time	1.0	2.0	ns
122	ts(ASR)	AA, AB Address RAS set up time	c+11.5	c+12.5	ns(*5)(*14)
123	ts(ASC)	AA, AB Address CAS set up time	c-13.5	c-11.0	ns(*5)(*14)
124	ts(DS)	Memory Write Data Set up time	4.5	9.5	ns(*1)(*14)
130	th(RAH)	AA, AB Address RAS hold time	nc-12.0	nc+5.0	ns(*4,5) n=2-3(*13)
131	th(CAH)	AA, AB Address CAS hold time	c+5.5	c+13.0	ns(*5)
132	th(DH)	Memory Write Data hold time	48.0	51.1	ns(*1)
133	th(RAL)	RAS hold time from AA, AB address	nc+11.5	nc+14.0	ns(*4,5) n=0-1
134	th(OFF)	Memory read Data hold time	5		ns
VRAM Memory Timing					
No.	Symbol	Description	min.	max.	unit
140	tw(SC)	SCC high pulse width	hc+0.8	hc+3.5	ns(*5)
141	tw(SCP)	SCC low pulse width	lc-3.5	lc-0.8	ns(*5)
142	tw(DTEL)	DTEAL, DTEBL pulse width low	nc-0.5	nc-3.5	ns(*4,5) n=1-6
150	td(SCC)	Delay From SCLK High to SCC High	5.4	20.5	ns
151	td(SCC)	Delay From SCLK Low to SCC Low	6.2	24.0	ns
152	td(TSD)	First SCC delay from DTEAL or DTEBL for read transfer cycles	c-0.3	c-1.3	ns(*5)
153	td(SCA)	Delay from SCC to serial data valid	5.0	c+5.0	ns(*5)
160	ts(TLS)	DTEAL, DTEBL setup to RAS low	c+0.0	c+1.0	ns(*5)
161	th(TRD)	DTEAL, DTEBL hold to RAS high	-nc-0.0	-nc-3.0	ns(*4,5) n=0-1
General Output Timing					
No.	Symbol	Description	min.	max.	unit
170	td(TKN0H)	TKN0 high delay from SCLK high	19.7	47.2	ns
171	td(TKN0L)	TKN0 low delay from SCLK high	23.0	60.0	ns
172	td(TKN1H)	TKN1 high delay from SCLK high	18.7	43.7	ns
173	td(TKN1L)	TKN1 low delay from SCLK high	7.9	30.8	ns
174	td(PMEL)	Delay from I/O Read or Write Command to PMERL or PMEWL Low	6.3	24.5	ns
175	td(PMEH)	Delay from I/O Read or Write Command to PMERL or PMEWL High	4.6	17.5	ns

2.3.1 Timing Specification (continued)

Display Timing					
No.	Symbol	Description	min.	max.	unit
180	td(CO)	Delay from MCLK to HS, VS outputs	5.9	39.6	ns
181	td(PCLKH)	Delay from MCLK to PCLK High			
		High Resolution Mode	3.0	11.4	ns
		High Color Mode	6.3	24.4	ns
		Normal Mode	4.5	17.1	ns
182	td(PCLKL)	Delay from MCLK to PCLK Low			
		High Resolution Mode	4.5	17.3	ns
		High Color Mode	7.6	29.4	ns
		Normal Mode	6.2	24.1	ns
183	td(IRGB)	Video/blank delay time from PCLK High			
		High Resolution Mode	2.0	12.0	ns
		High Color Mode	- 5.8	1.0	ns
		Normal Mode	2.0	12.0	ns
184	td(IRGB)	Video/blank delay time from PCLK Low			
		High Color Mode	- 10.0	- 1.4	ns

NOTES:

(*1) Depending on the clock frequency and duty cycle.
The assumptions for this timing specification are:
SCLK (c) = 40MHz, 50% duty cycle.

(*2) Maximum WAIT delay varies dependent on the minimum available memory Band Width to CPU.

(*3) Width may increase if slower (access time) translation EPROM is used.

(*4) n = programmable, n is the result of programmed value according to CRTC index 32.

(*5) c = SCLK cycle time
hc = SCLK high pulse width
lc = SCLK low pulse width

(*6) Times indicated do not reflect any delays on the address/data bus due to board logic delay (74F244 = 5 ns, EPROM = 150 ns delay etc..).

(*7) Based on random cycle.

(*8) Based on back to back RAS cycles.

(*9) This value must be greater than the SCLK period.

(*10) Width may increase if slower (access time) BIOS EPROM is used.

(*11) If ROMEL or PMERL active, then DB⟨15:0⟩ bus is in tri-state condition.

(*12) In 16-bit I/O write, ts(IWRCS) is measured from leading edge of IOWWL.
In 8-bit I/O write, ts(IWRCS) time is measured from trailing edge of MIOWL or IOWWL.

(*13) ET4000AX Rev. E RAS addresses hold time reduced from n=2 to n=1 to improve external font access timing.

(*14) See Addendum 6.1 for ET4000 Rev. E adjustments to timing.

2.3.1 Timing Specification (continued)

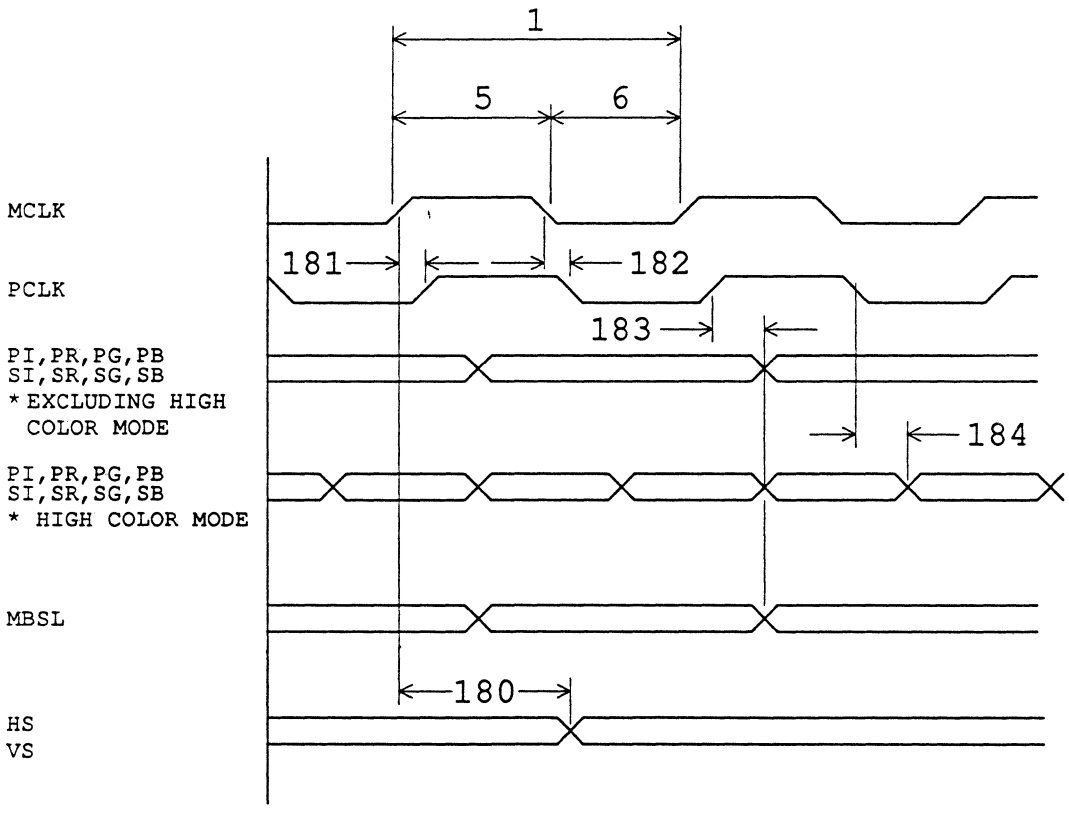


FIG. 2.3.2-1 CRTC OUTPUT TIMING

2.3.1 Timing Specification (continued)

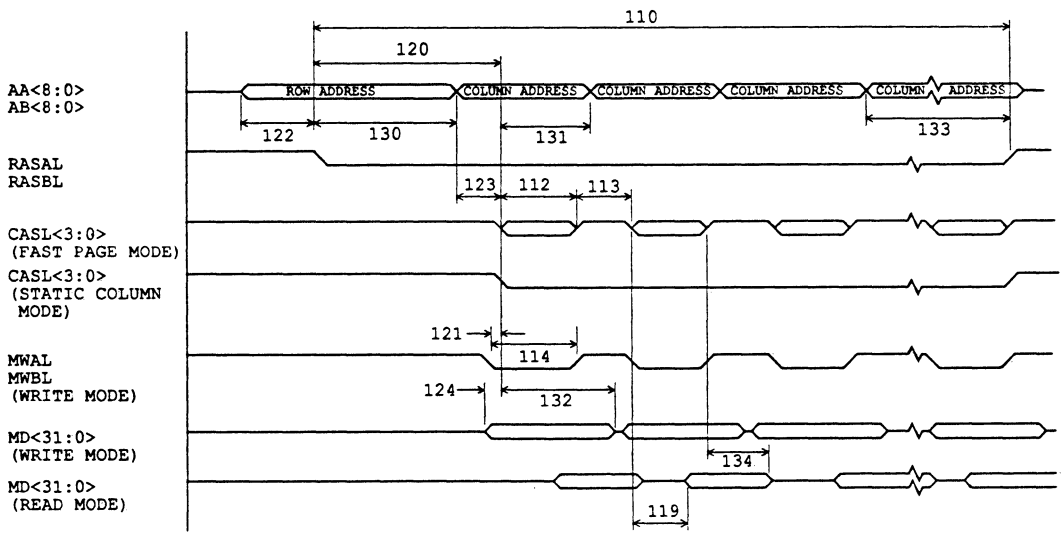


FIG. 2.3.2-2 DISPLAY MEMORY READ/WRITE TIMING

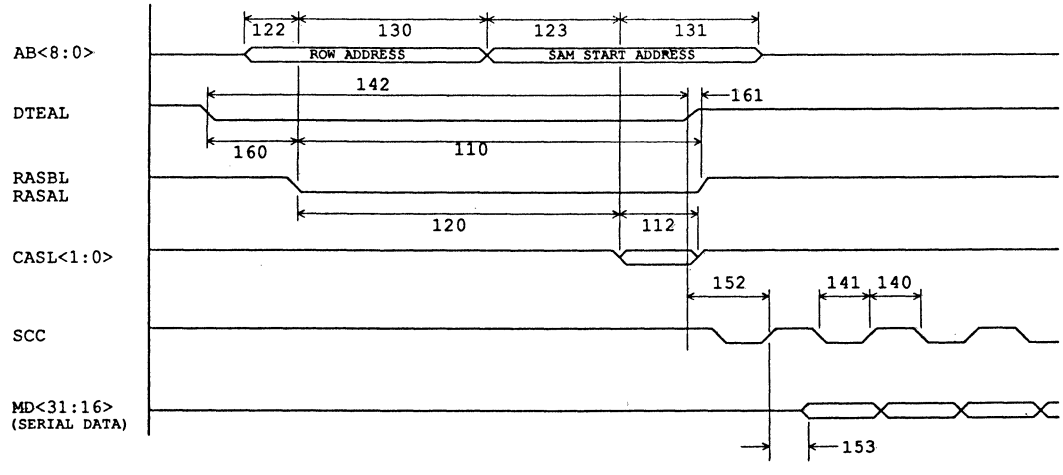


FIG. 2.3.2-3 VRAM TRANSFER CYCLE AND SERIAL READ TIMING

2.3.1 Timing Specification (continued)

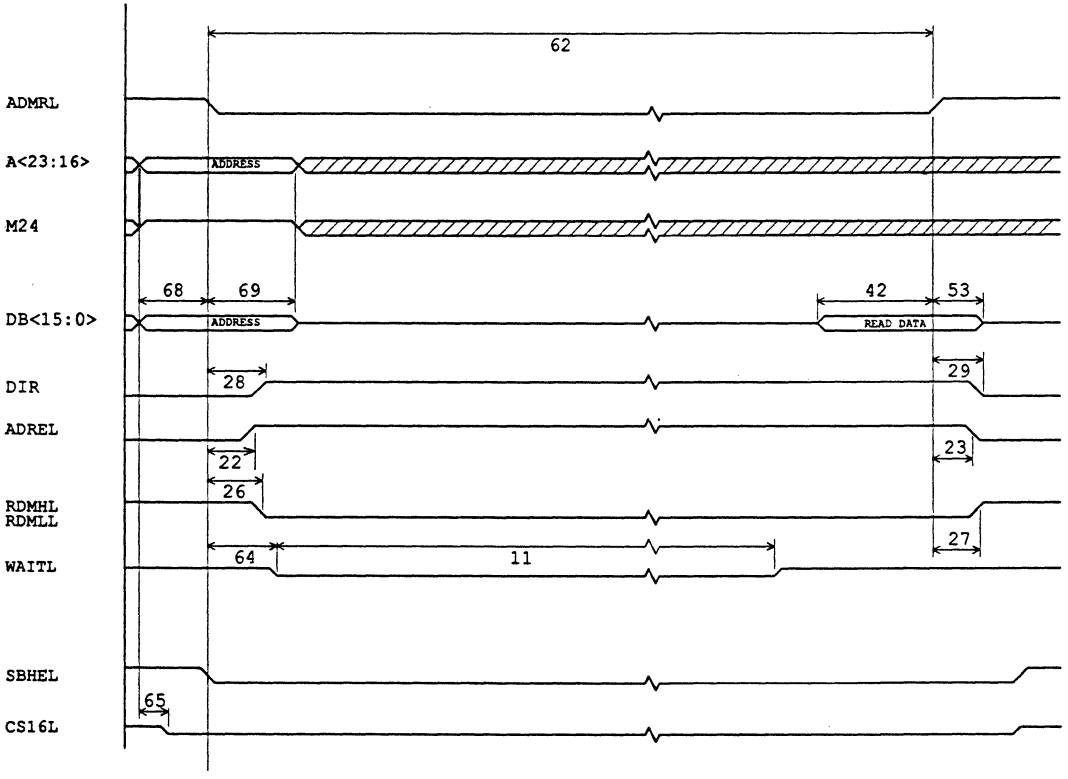


FIG. 2.3.2-4 DISPLAY MEMORY READ TIMING (CPU CYCLE — AT BUS)

2.3.1 Timing Specification (continued)

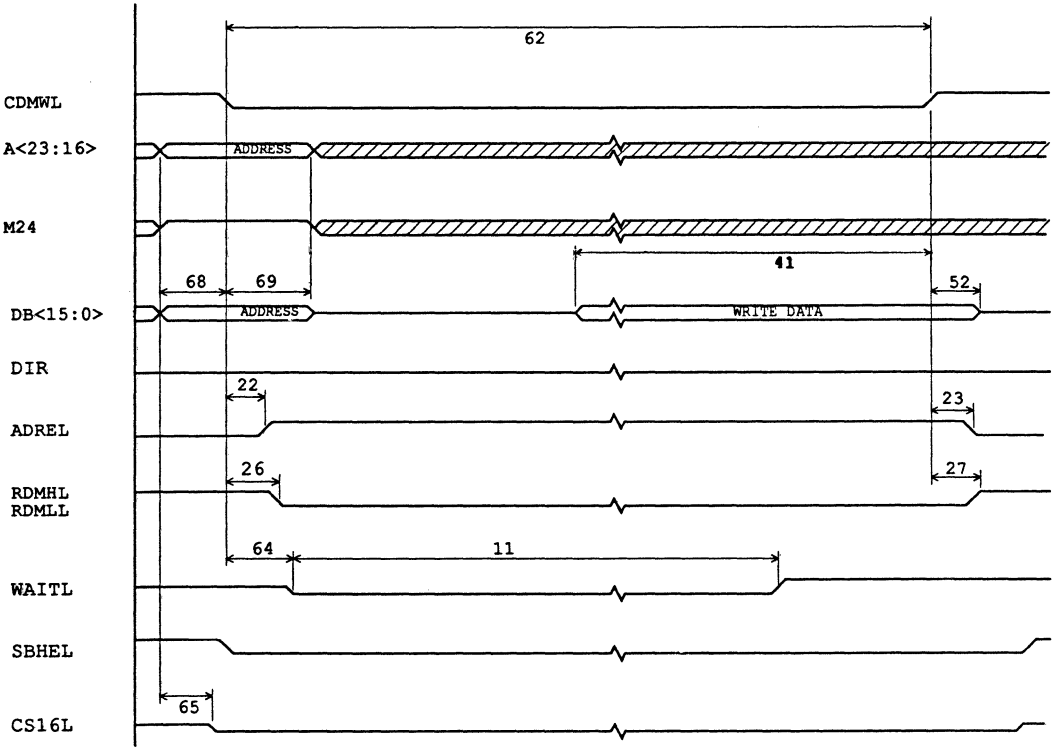


FIG. 2.3.2-5 DISPLAY MEMORY WRITE TIMING (CPU CYCLE – AT BUS)

2.3.1 Timing Specification (continued)

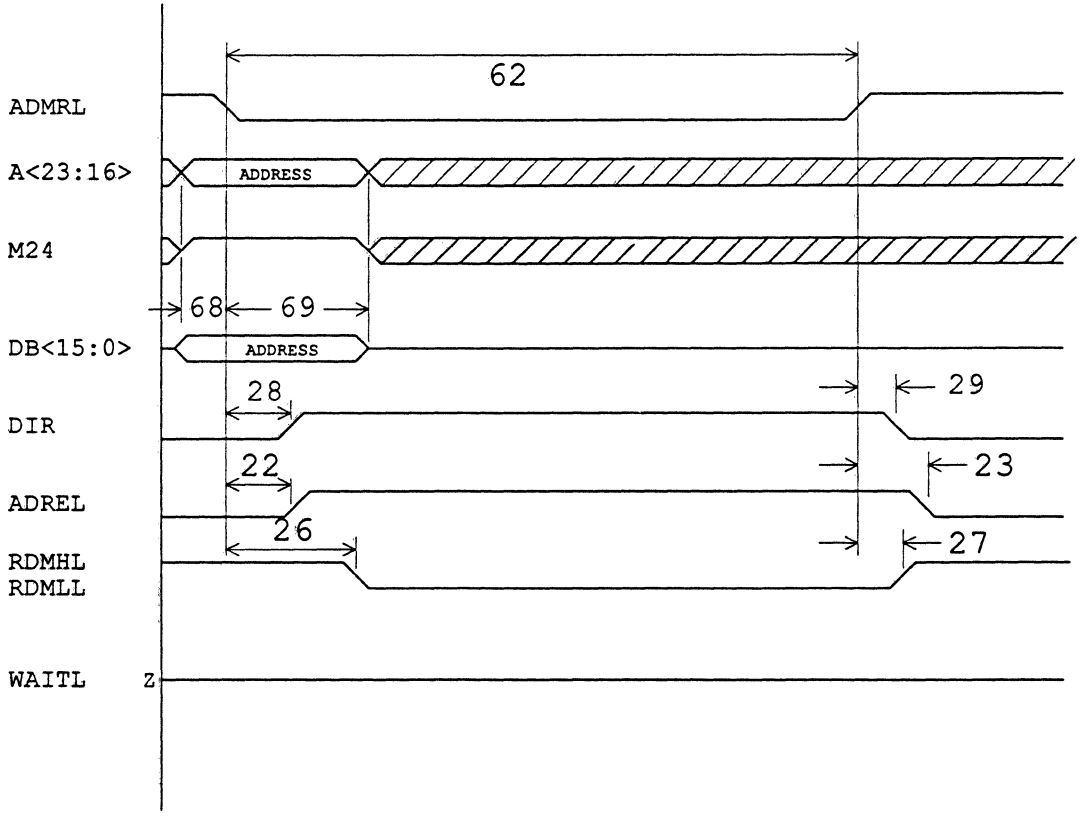


FIG. 2.3.2-6 BIOS EPROM MEMORY READ TIMING (CPU CYCLE – AT BUS)

2.3.1 Timing Specification (continued)

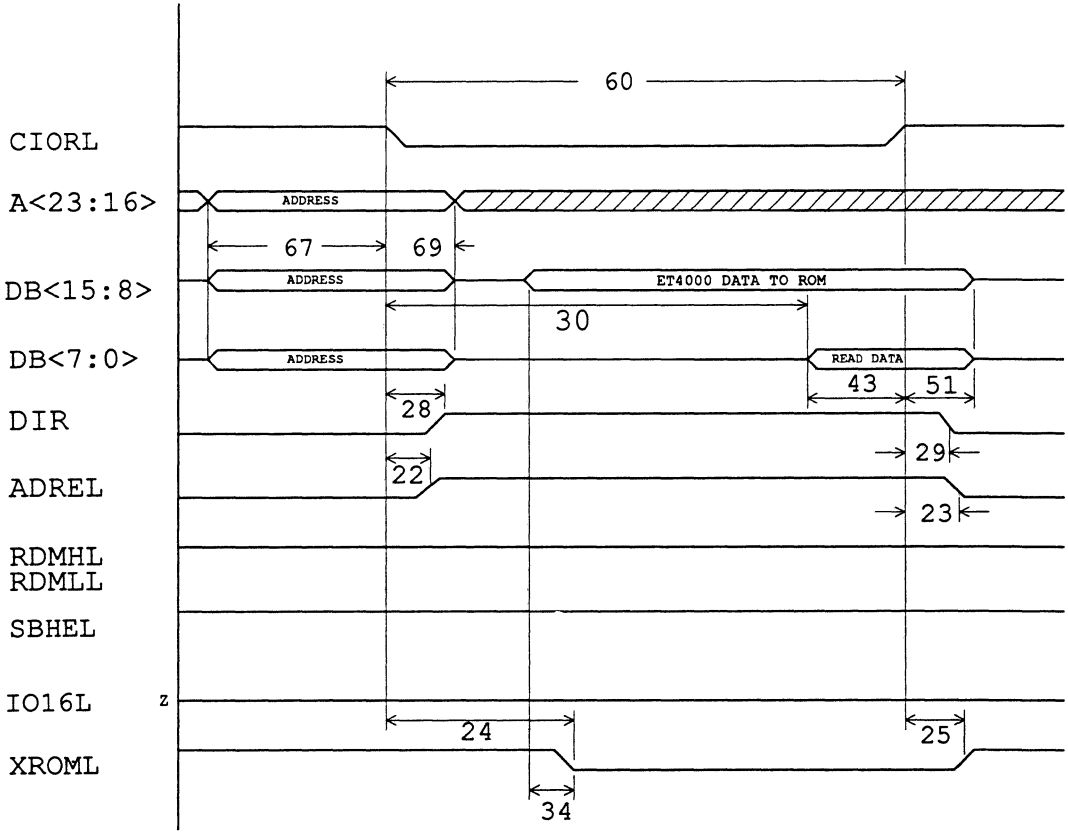


FIG. 2.3.2-7 I/O READ TIMING (CPU CYCLE – AT BUS)
(WITH TRANSLATION ROM ACCESS)

2.3.1 Timing Specification (continued)

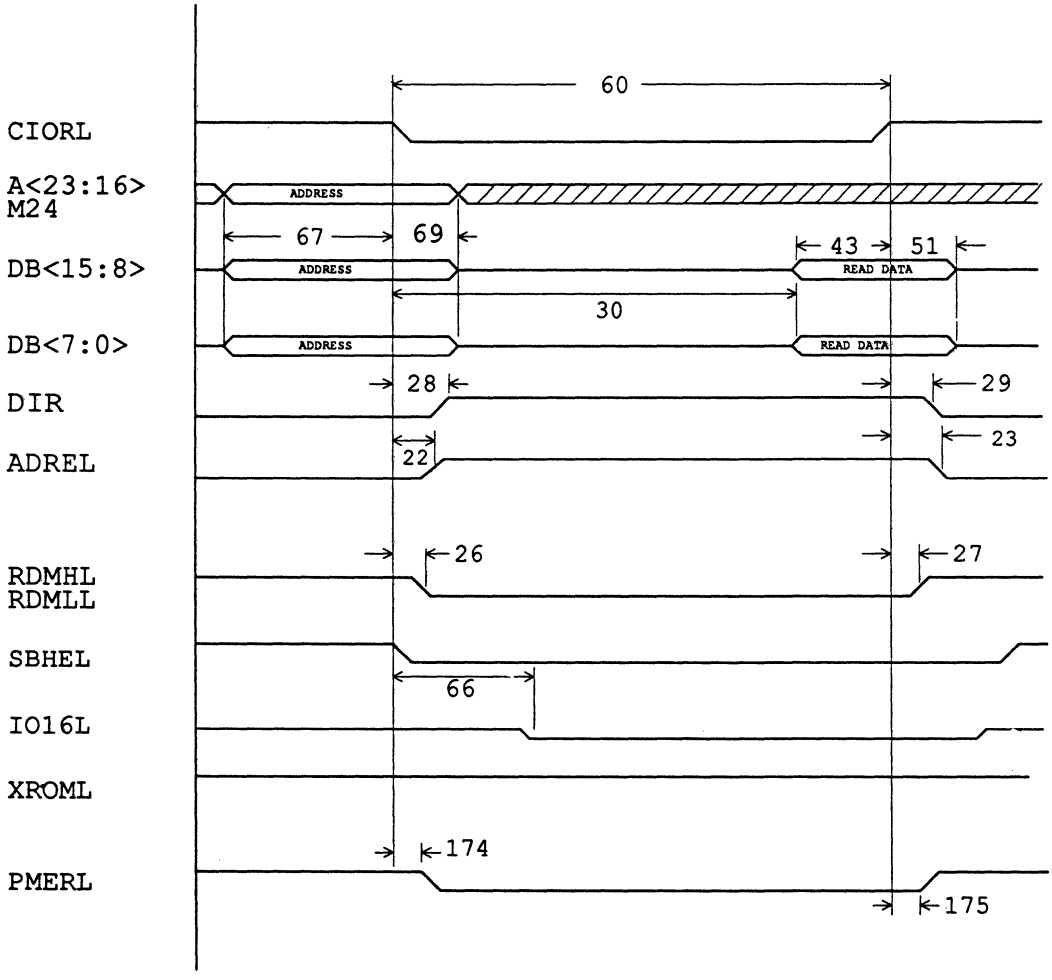


FIG. 2.3.2-8 I/O READ TIMING (CPU CYCLE – AT BUS)
(WITHOUT TRANSLATION ROM ACCESS)

2.3.1 Timing Specification (continued)

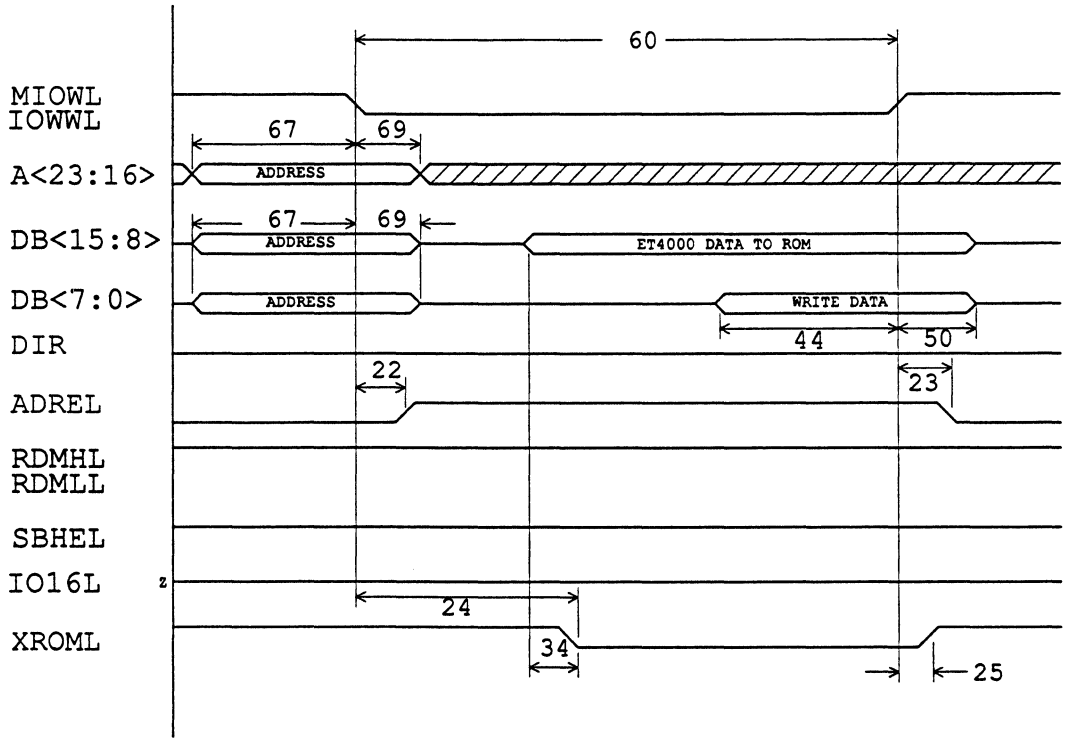


FIG. 2.3.2-9 I/O WRITE TIMING (CPU CYCLE — AT BUS)
(WITH TRANSLATION ROM ACCESS)

2.3.1 Timing Specification (continued)

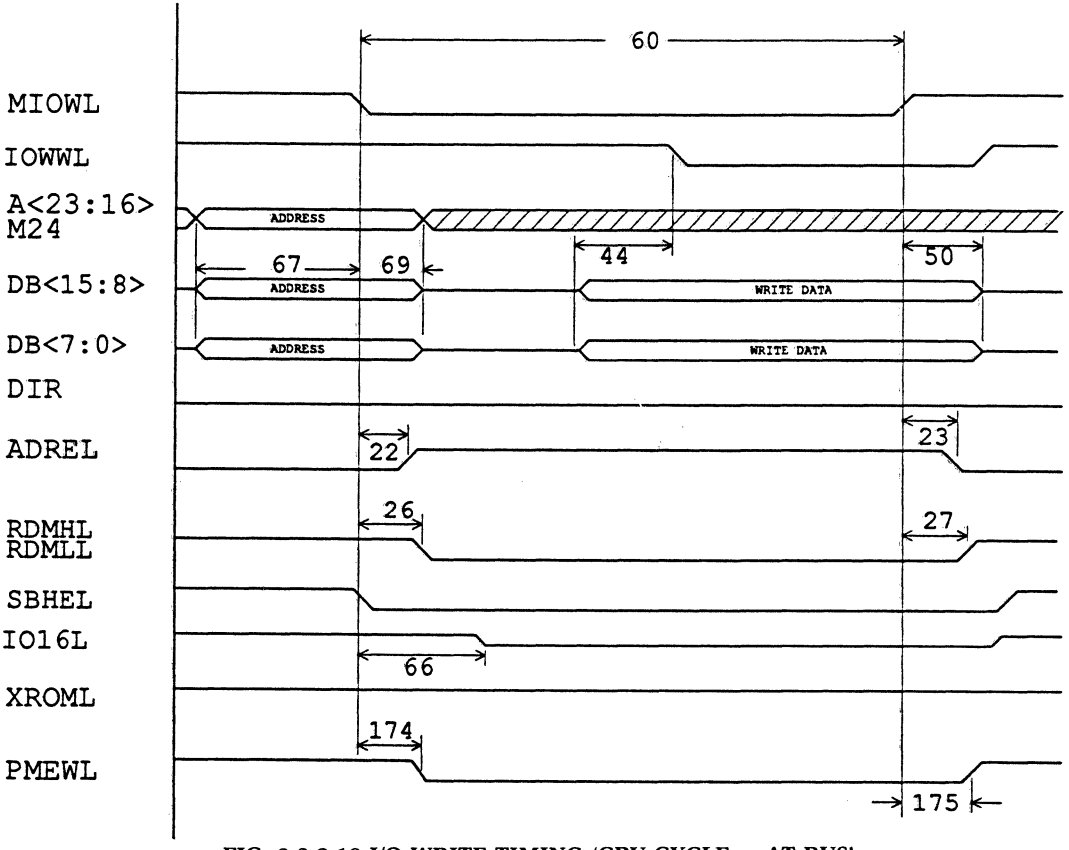


FIG. 2.3.2-10 I/O WRITE TIMING (CPU CYCLE – AT BUS)
(WITHOUT TRANSLATION ROM ACCESS)

2.3.1 Timing Specification (continued)

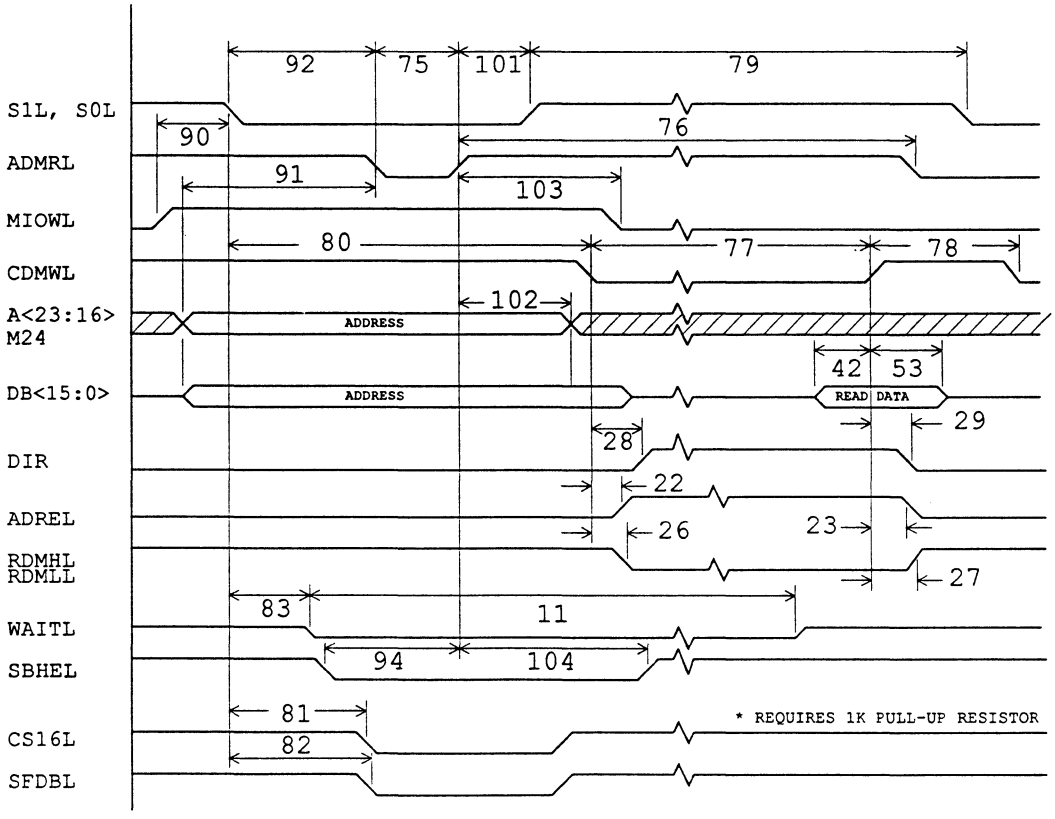


FIG. 2.3.2-11 DISPLAY MEMORY READ TIMING (CPU CYCLE — MICRO CHANNEL BUS)

2.3.1 Timing Specification (continued)

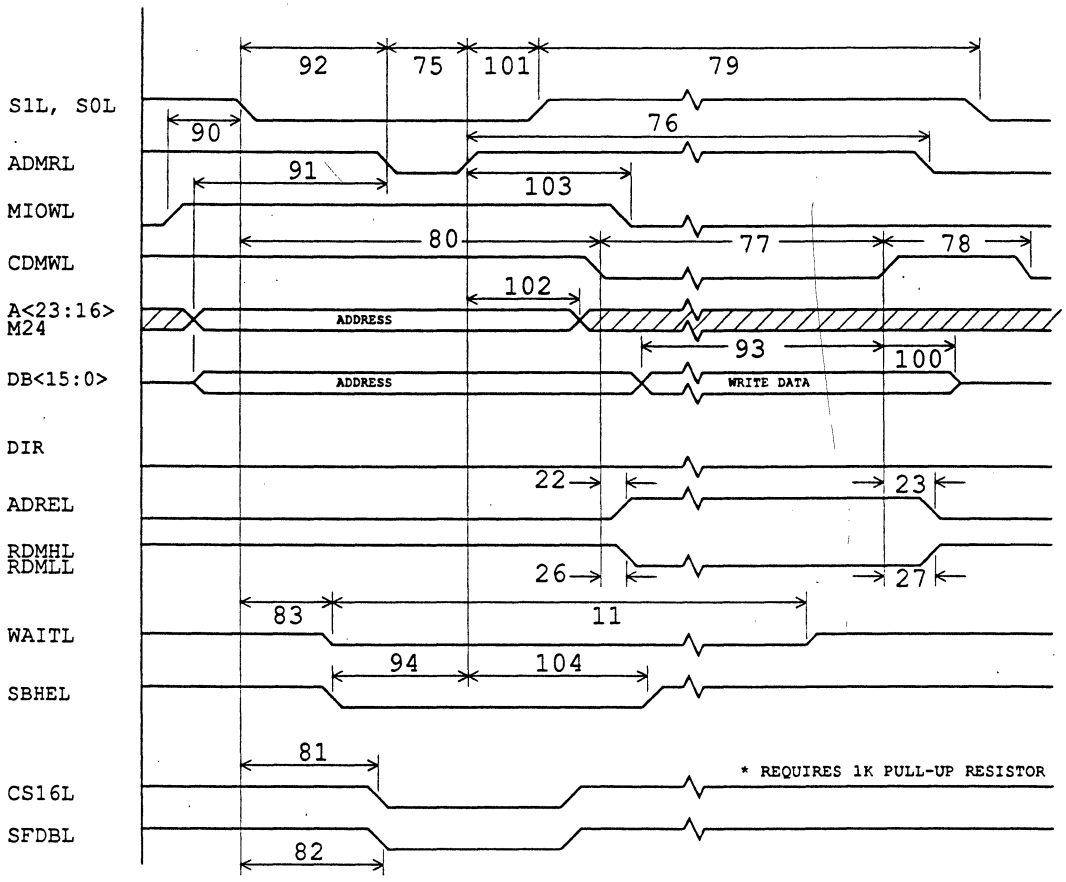


FIG. 2.3.2-12 DISPLAY MEMORY WRITE TIMING (CPU CYCLE — MICRO CHANNEL BUS)

2.3.1 Timing Specification (continued)

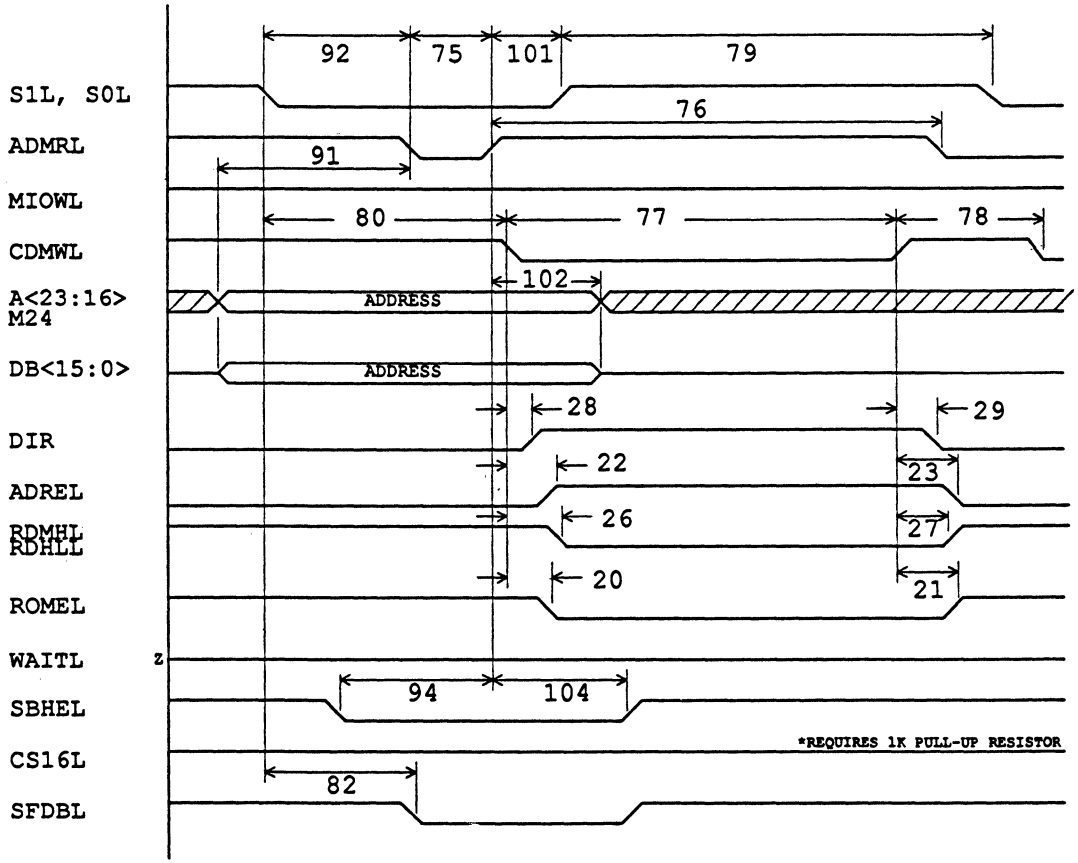


FIG. 2.3.2-13 BIOS EPROM MEMORY READ TIMING (CPU CYCLE — MICRO CHANNEL BUS)

2.3.1 Timing Specification (continued)

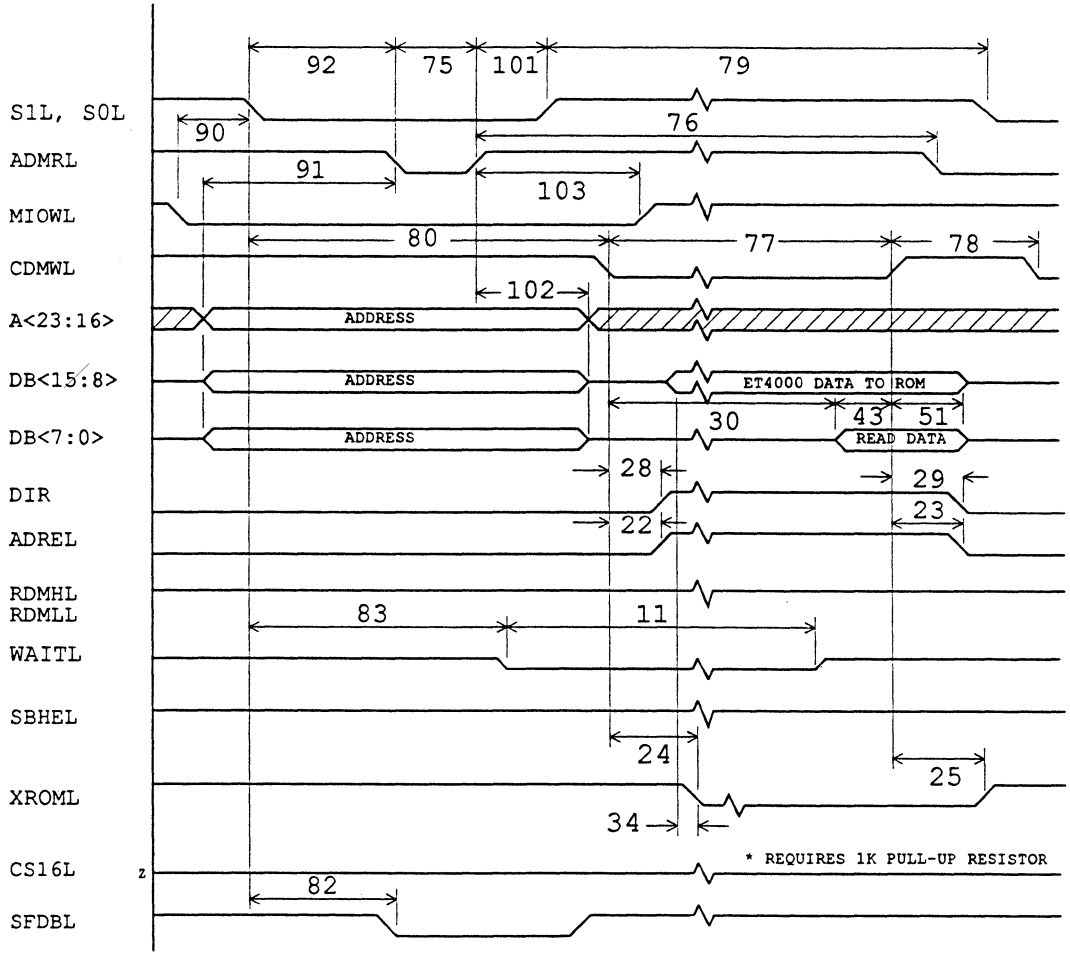


FIG. 2.3.2-14 I/O READ TIMING (CPU CYCLE — MICRO CHANNEL BUS) (WITH TRANSLATION ROM ACCESS)

2.3.1 Timing Specification (continued)

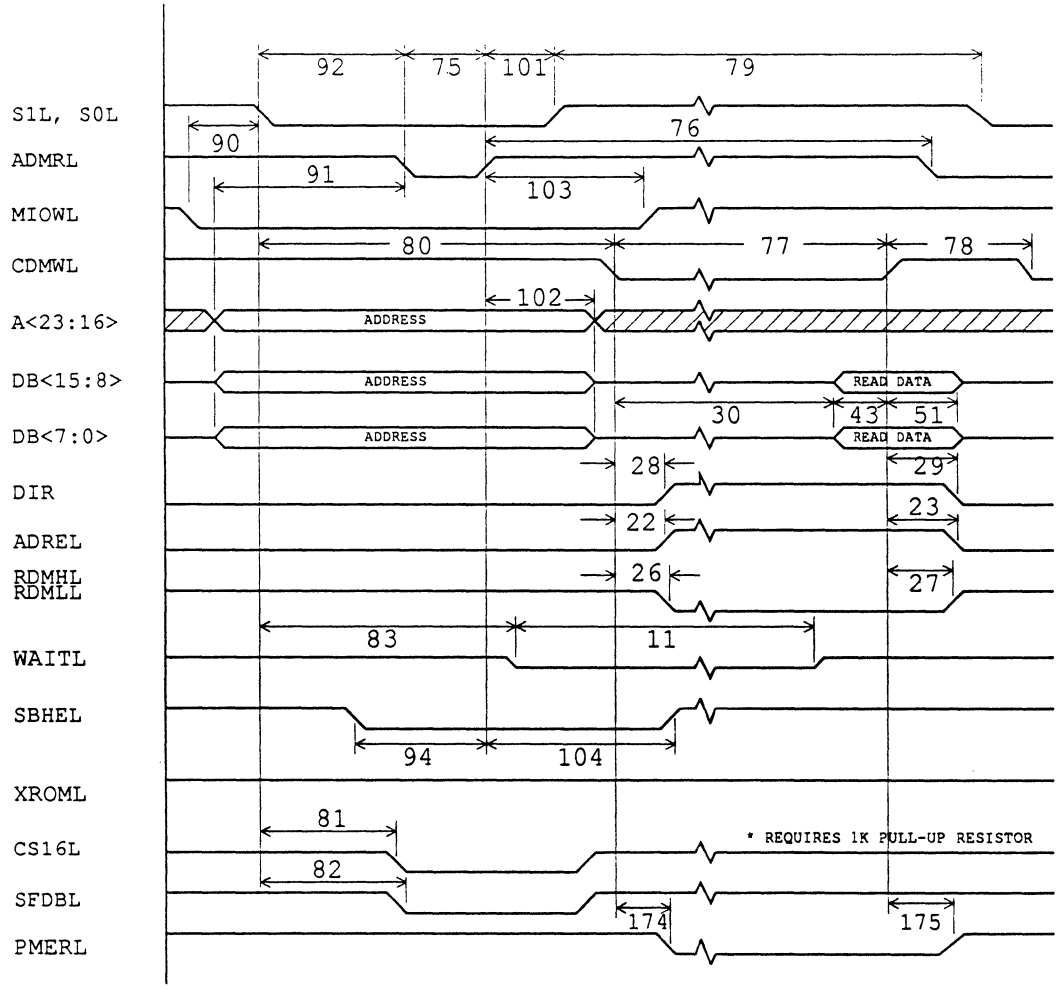


FIG. 2.3.2-15 I/O READ TIMING (CPU CYCLE – MICRO CHANNEL BUS)
(WITHOUT TRANSLATION ROM ACCESS)

2.3.1 Timing Specification (continued)

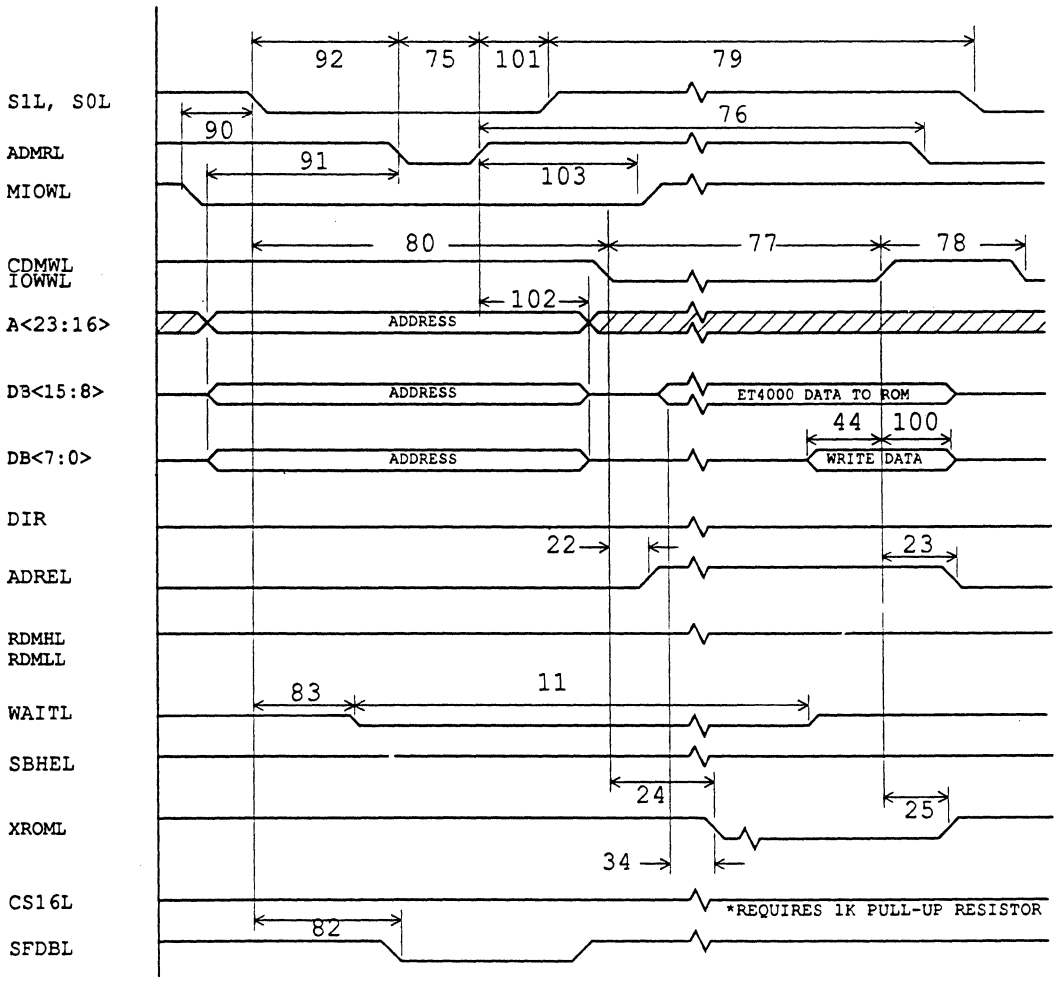


FIG. 2.3.2-16 I/O WRITE TIMING (CPU CYCLE — MICRO CHANNEL BUS) (WITH TRANSLATION ROM ACCESS)

2.3.1 Timing Specification (continued)

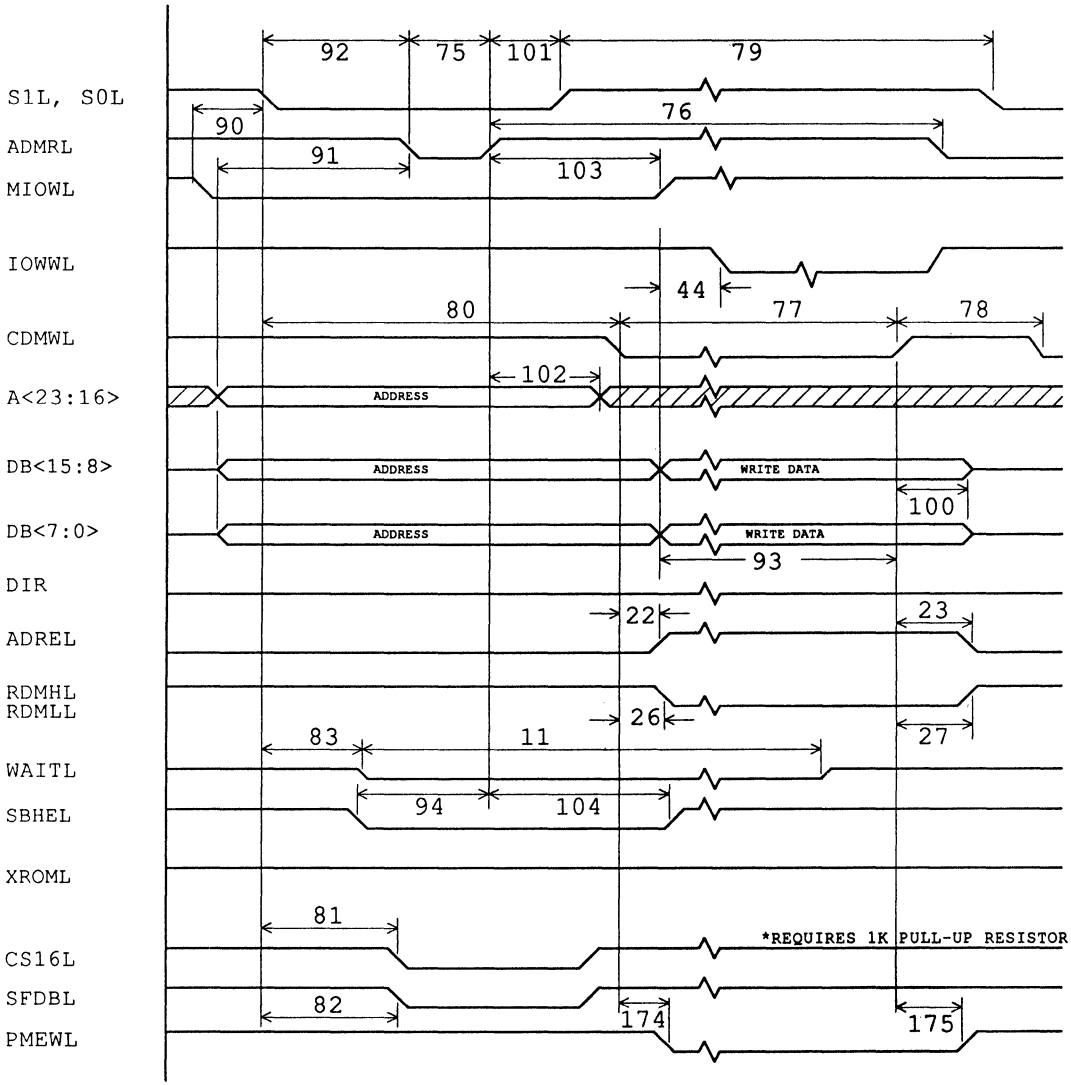


FIG. 2.3.2-17 I/O WRITE TIMING (CPU CYCLE — MICRO CHANNEL BUS) (WITHOUT TRANSLATION ROM ACCESS)

3.0 ET4000 PROGRAMMING CONSIDERATIONS

3.1 Modes of Operation

ET4000 supports all the VGA/EGA video graphic/text modes and more as summarized in Tables 1.1-1 and 1.1-2 in Section 1. These modes are described below.

3.1.1 Text Modes

Data Format

Four bit planes are provided to allow more efficient use of video memory. The use of these planes depends on the mode being selected.

When an alphanumeric mode is selected, four bit planes are divided into two pairs of odd/even planes. The BIOS transfers character patterns from the ROM to the upper plane pair—bit planes 2 and 3. The system microprocessor stores the character and attribute data in the lower plane pair—bit planes 0 and 1. The programmer can view bit planes 0 and 1 as a single buffer in alphanumeric modes. The CRTC generates sequential word addresses and fetches one character/attribute word at a time. This allows the execution of programs having the character code in even byte addresses and the attribute data for that character in the odd byte address that follows.

Every display character position in the alphanumeric mode is defined by two bytes in the display buffer. Both the color/graphics and the monochrome emulation modes use the following 2-byte character/attribute format.

Bit	Attributes
7	Blink/background intensity
6	Background color, red
5	Background color, green
4	Background color, blue
3	Foreground intensity/character select
2	Foreground color, red
1	Foreground color, green
0	Foreground color, blue

Notes:
1. Bit 7 can be used for either Blink or Background Intensity characters. See function "AH = 10h, AL = 3 (Toggle Intensity/Blinking Bit)" in Section 5.
2. Bit 3 can be used for either Foreground Intensity or Character Set Select.

VGA/TLI compatible text modes supported by the ET4000's GENERIC BIOS are described below:

40x25 Text (Modes 0 and 1):
40 characters per row x 25 rows
Display buffer starts at hex B8000
Up to eight display pages
Require 2,000 bytes of read/write memory per page.

Memory allocations for display pages:

Page	Start Address
1	B8000
2	B8800
3	B9000
4	B9800
5	BA000
6	BA800
7	BB000
8	BB800

80x25 Text (Modes 2, 3, and 7):
80 characters per row x 25 rows
Display buffer starts at hex B8000 (modes 2,3), B0000 (mode 7)
Up to 8 display pages
Require 4,000 bytes of read/write memory per page.

Memory allocations for display pages:

Page	Modes 2 and 3 start address	Mode 7 start address
1	B8000	B0000
2	B9000	B1000
3	BA000	B2000
4	BB000	B3000
5	BC000	B4000
6	BD000	B5000
7	BE000	B6000
8	BF000	B7000

132x44 Text (Modes 18 and 22):
132 characters per row x 44 rows
Display buffer starts at hex B0000 (mode 18), B8000 (mode 22)
Up to 2 display pages
Require 11,616 bytes of read/write memory per page.

Memory allocations for display pages:

Page	Modes 18 start address	Mode 22 start address
1	B0000	B8000
2	B4000	BC000

132x25 Text (Modes 19 and 23):
132 characters per row x 25 rows
Display buffer starts at hex B0000 (mode 19), B8000 (mode 23)
Up to 4 display pages
Require 6,600 bytes of read/write memory per page.

Memory allocations for display pages:

Page	Modes 19 start address	Mode 23 start address
1	B0000	B8000
2	B2000	BA000
3	B4000	BC000
4	B6000	BE000

132x28 Text (Modes 1A and 24):
132 characters per row x 28 rows
Display buffer starts at hex B0000 (mode 1A), B8000 (mode 24)
Up to 4 display pages
Require 7,392 bytes of read/write memory per page.

Memory allocations for display pages:

Page	Modes 1A start address	Mode 24 start address
1	B0000	B8000
2	B2000	BA000
3	B4000	BC000
4	B6000	BE000

80x60 Text (Mode 26):
80 characters per row x 60 rows
Display buffer starts at hex B8000
Up to 2 display pages
Requires 9,600 bytes of read/write memory per page.

Memory allocations for display pages:

Page	start address
1	B8000
2	BC000

100x40 Text (Mode 2A):
100 characters per row x 40 rows
Display buffer starts at hex B8000
Up to 4 display pages
Requires 8,000 bytes of read/write memory per page.

Memory allocations for display pages:

Page	start address
1	B8000
2	BA000
3	BC000
4	BE000

3.1.2 Graphic Modes

VGA/TLI compatible graphics modes supported by the ET4000's GENERIC BIOS are described below:

320x200 Four Color (Modes 4 and 5):
4 colors per PEL, 4 PELs per byte
320 PELs per row x 200 rows
Display buffer starts at hex B8000
Use one display page
Require 16,000 bytes of read/write memory.

The ET4000 should be programmed to be in IBM VGA mode in Modes 4 and 5.

Each data byte contains two color bits for four PELs:

Bit	
7,6	C1,C0 of first PEL
5,4	C1,C0 of second PEL
3,2	C1,C0 of third PEL
1,0	C1,C0 of fourth PEL

where the color bits combine to give:

C1	C0	
0	0	Black
0	1	Green or cyan
1	0	Red or magenta
1	1	Brown or intense white

C0 is stored in bit plane 0; C1 is stored in bit plane 1.

The display buffer is partitioned into two sections of 8000 bytes each. One section contains PELs for display on even scan lines (lines 0, 2, 4 through 198), the other contains PELs for the odd scan lines:

Section	Lines	Start Address	End Address
0	Even	B8000	B9F3F
1	Odd	BA000	BBF3F

Notes:
1. Hex B8000 contains PEL data for the upper-left corner of the display area.
2. Odd scan lines are offset from even scan lines by 8K.

640x200 Two Color (Mode 6):
2 colors per PEL, 8 PELs per byte
640 PELs per row x 200 rows
Display buffer starts at hex B8000
Use one display page
Requires 16,000 bytes of read/write memory.

Each data byte defines a row of eight PELs on the screen. Each bit defines 2 colors for each PEL as follows:

0	Black
1	Intensified white

16/256K Colors (Modes D, E, 10 and 12):
These 4 modes share the same 16-color data format:
16 colors per PEL, 1 bit from each bit-plane per PEL,
discussed together as follows:

Mode D: 320 PELs per row x 200 rows, requires 32,000 bytes RAM
Mode E: 640 PELs per row x 200 rows, requires 64,000 bytes RAM
Mode 10: 640 PELs per row x 350 rows, requires 112,000 bytes RAM
Mode 12: 640 PELs per row x 480 rows, requires 153,600 bytes RAM

Starting addresses for the display pages are:

	Mode D	Mode E	Mode 10	Mode 12
Number of display pages:	8	4	2	1
Starting addresses for each page: Page				
1	A0000	A0000	A0000	A0000
2	A2000	A4000	A8000	
3	A4000	A8000		
4	A6000	AC000		
5	A8000			
6	AA000			
7	AC000			
8	AE000			

Four bit planes, each starting at location hex A0000, provide the four color bits required for each PEL as follows:

Plane 3	C3	Intensity
Plane 2	C2	Red
Plane 1	C1	Green
Plane 0	C0	Blue

Within each bit plane, each data byte defines a row of eight PELs on the screen, for a specific color bit. The planes are accessed simultaneously and the color bits together address one register in a table of 16 color registers.

If the values in the registers are the supplied default values, the colors will be:

C3	C2	C1	C0	
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	Intense White

The 16 colors are mapped to the supported monochrome monitor as 16 shades ranging from black to intense white.

The graphics program interface to the bit planes is through the READ DOT and WRITE DOT functions; C0 through C3 are bits 0 through 3 of the color data.

640x350 Monochrome (Mode F):

4 monochrome attributes per PEL
1 bit from each of plane 0 and 2 per PEL
640 PELs per row x 350 rows
Display buffer starts at hex A0000
Two display pages
Requires 56,000 bytes of read/write memory per page.

Memory allocation for the display pages are:

Page	Start Address
1	A0000
2	A8000

Two bytes (one from plane 0 and one from plane 2) together define a row of eight PELs on the screen. Bit planes 2 and 0 are accessed simultaneously, to support graphics on displays that use the following attributes: black, video, blinking video, and intensified video. Bit plane 2 provides color bit C2 and plane 0 provides color bit C0, combining to give the attributes as follows:

C2	C0	
0	0	Black
0	1	Video
1	0	Blink video
1	1	Intense video

The graphics program interface to the bit planes is through the READ DOT and WRITE DOT functions; C0 and C2 are bits 0 and 2 of the color data.

640x480 Two Color (Mode 11):
2 colors per PEL, 8 PELs per byte
640 PELs per row x 480 rows
Display buffer starts at hex A0000
Requires 38,400 bytes of read/write memory.

Each data byte defines a row of eight PELs on the screen. Each bit defines 2 colors for each PEL as follows:

0	Black
1	Intensified white

256/256K Colors (Mode 13):
256 Colors per PEL, 1 PEL per byte
320 PELs per row x 200 rows
256 colors or 64 shades of gray
Display buffer starts at hex A0000
One display page
Requires 64,000 bytes of read/write memory.

The four memory planes are chained together to form a linear display buffer 256KB deep starting at address hex A0000. Each byte defines the 8-bit color data for one PEL on the screen.

Color data read from the display buffer is used as a pointer to address one register in a table of 256 color registers (the External Palette RAM). The default color mapping is:

Registers 0 through 15 map to the 16 EGA colors;
Registers 16 through 31 map to evenly spaced shades of gray;
Registers 32 through 247 map to a range of color shades based on a Hue/ Saturation/Intensity model that provides a usable set of colors.

NOTE: Changing the internal palette (that which is compatible with the Enhanced Graphics Adapter) from the default setting will produce unpredictable results. If you want to change the colors, change the values in the individual color registers.

16/256K Colors (Modes 25, 29, 37):
These modes share the same 16-color data format as modes D, E, 10 and 12 described previously. For a detailed description of the color format and access to Palette RAM, refer to the prior description. The resolution and display buffer map are, however, different and are described below:

Mode 25:
16 colors per PEL, 1 bit from each bit-plane per PEL 640 PELs per row x 480 rows
Display buffer starts at A0000
One display page
Requires 153,600 bytes read/write memory.

Mode 29:
16 Colors per PEL, 1 bit from each bit-plane per PEL 800 PELs per row x 600 rows
Display buffer starts at A0000
One display page
Requires 240,000 bytes read/write memory.

Mode 37:
16 Colors per PEL, 1 bit from each bit-plane per PEL
1024 PELs per row x 768 rows
Display buffer starts at A0000
One display page
Requires 393,216 bytes read/write memory.

256/256K Colors (Modes 2D, 2E, 2F, 30 and 38):

These modes share the same 256-color data format as mode 13. For a detailed description of the color format and access to External Palette RAM, refer to the description following "256/256K Colors (Mode 13):"

The resolution and display buffer map are different, however, and are described below:

Mode 2D:
256 colors per PEL, 1 PEL per byte
640 PELs per row x 350 rows
Display buffer starts at A0000
One display page
Requires 224,000 bytes of read/write memory.

Mode 2E:
256 Colors per PEL, 1 PEL per byte
640 PELs per row x 480 rows
Display buffer starts at A0000.
One display page
Requires 307,200 bytes of read/write memory.

Mode 2F:
256 Colors per PEL, 1 PEL per byte
640 PELs per row x 400 rows
Display buffer starts at A0000
One display page
Requires 256,000 bytes of read/write memory.

Mode 30:
256 Colors per PEL, 1 PEL per byte
800 PELs per row x 600 rows
Display buffer starts at A0000
One display page
Requires 480,000 bytes of read/write memory.

Mode 38:
256 Colors per PEL, 1 PEL per byte
1024 PELs per row x 768 rows
Display buffer starts at A0000
One display page
Requires 786,432 bytes read/write memory.

3.2 Video Memory Organization

3.2.1 Video Memory Address Space Allocation

The video display buffer consists of 256KB of memory for the basic configuration, and can be increased to a total of 1024KB with up to eight 1MB memory devices. In maximum configuration, support is available for up to 1024x768-pixel resolution in 256-colors.

The address space allocated for the video display buffer is, however, limited to only 128K bytes in the IBM systems, programmable via the GDC Miscellaneous Register (GDC Index Register 6) as follows:

GDC Misc. Reg. ⟨3, 2⟩	Address space	Size	Mode
0 0	A0000-BFFFF	128KB	Hi-resolution
0 1	A0000-AFFFF	64KB	
1 0	B0000-B7FFF	32KB	
1 1	B8000-BFFFF	32KB	

With this address limitation, the display buffer, which can be up to 1024KB in size, needs to be partitioned into memory segments for proper addressing. Each memory segment will be addressed using the same address space, along with a segment number programmable in a segment pointer. The GDC Segment Select Register (port 3CD) contains four read segment pointers and four write segment pointers.

IMPORTANT:
In the extended VGA or high-resolution modes, the 128KB address size should not be used. Instead, the 64KB size should be used with the segment pointers to provide all addressable points.

3.2.2 Two Major Types of System Configurations

From a programming viewpoint, the display data can be structured into video bit-planes (under a Plane System), or into memory arrays (under a Linear Byte System), depending on the particular video mode to be supported. A discussion of these two types of systems, along with their addressing scheme and typical modes, follows.

Plane System

In VGA-compatible 16-color modes, a "Plane" configuration is used, where four independently addressable bit planes (I,R,G,B) are accessed in parallel, and each pixel is represented by up to four bits from the four planes, selecting up to 16 colors. The size of each plane depends on the resolution supported.

The CPU shall access the display buffer using the Read Plane Select (RPS) (GDC Index Register 4) and Write Plane Mask (WPM) (TS Index register 2), applicable only for Plane Systems, with 16-bit address lines addressing up to 64KB on each plane.

For planes greater than 64KB, the Segment Select Register is used.

The major advantages of a Plane system include:

3.0

(1) Allows parallel access of all four color planes (32 bits or eight PELs), through one CPU I/O operation, therefore minimizing the frequency of CPU accesses.

(2) By spreading four bits per PEL over four bit-planes, the total address space per plane is reduced by a factor of 4, therefore minimizing the need of crossing 64KB segment boundaries.

(3) The ET4000 provides two types of read and four types of write operations, during which the display data can be processed, provided they are structured as four planes. These operations include "color compare" to expedite color-fill functions, block move operations, set/reset functions to facilitate initialization of the display buffer, and bit-masking facilities to allow modification of up to sixteen PELs by a single CPU I/O operation.

Linear Byte System

To support either 256 or 65,536 colors (Figs. 3.2.3-6, 3.2.3-7), a "Linear Byte" system is used, whereby all memory planes are chained together as a linear byte-oriented memory. Each pixel is represented by 1 single byte in 256 colors or 2 adjacent bytes in 65,536 colors. The depth of the linear array depends on the resolution or number of colors supported, and therefore the amount of display buffer required.

The CPU shall access the display buffer using address lines and the segment select register, while the Read Plane Select (RPS) and Write Plane Mask (WPM) are IGNORED.

The major advantages of a Linear Byte system include:

(1) Each PEL is represented by a single byte (256 colors), which eliminates the need to manipulate data across byte boundaries associated with Plane systems.

(2) Simplifies the color shading function which is needed to adjust the color of each PEL, since addressing a PEL does not require any I/O port access as does a plane system.

3.2.3 Video Memory Organization

The figures on the following pages illustrate the video memory organization for all the text and graphics modes supported by the ET4000.

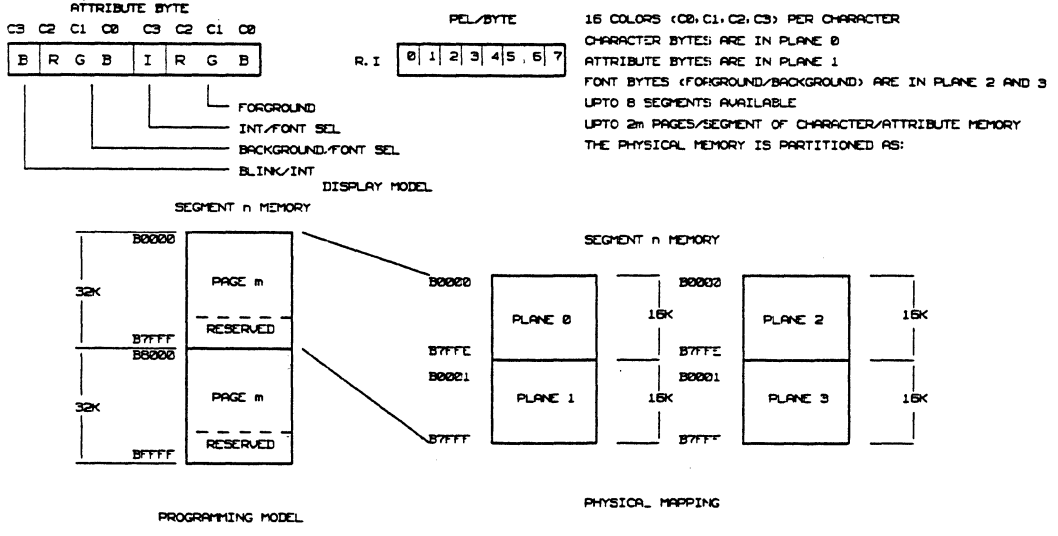


FIG. 3.2.3-1 TEXT MODE (MODE 0, 1, 2, 3, 7, 18, 19, 1A, 22, 23, 24, 26, 2A)

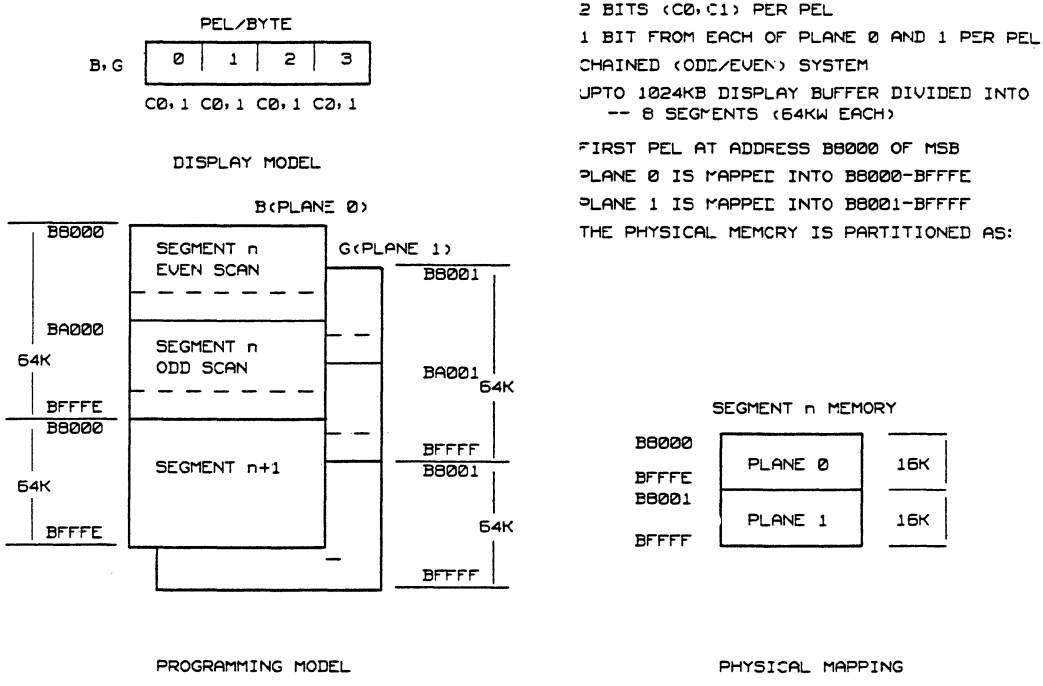


FIG. 3.2.3-2 4 COLORS CHAINED GRAPHICS (MODE 4, 5)

3.0

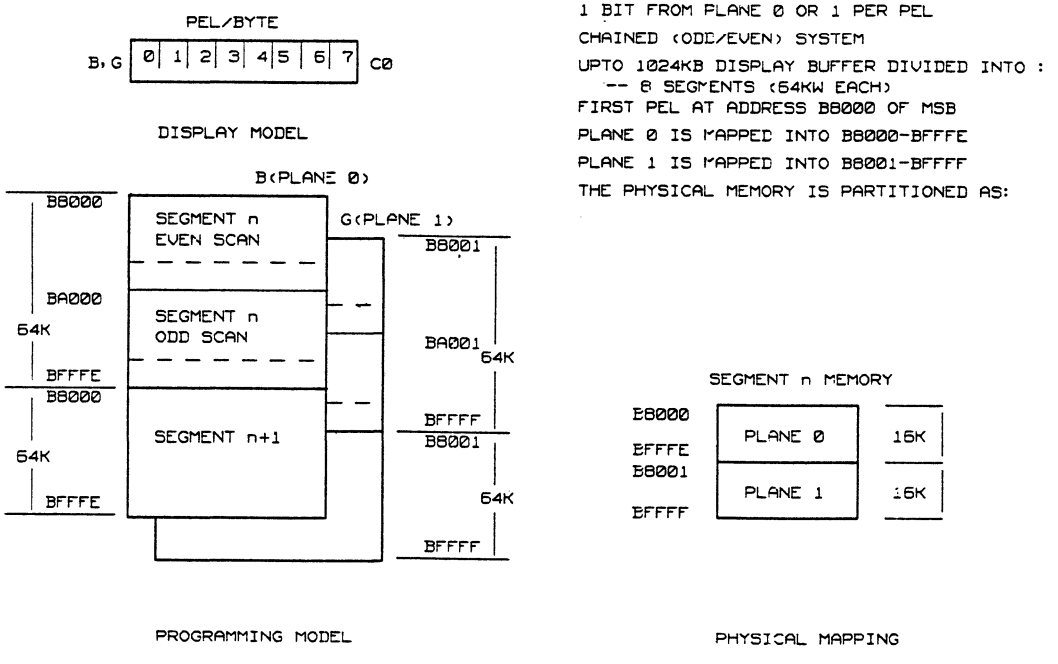


FIG. 3.2.3-3 2 COLORS CHAINED GRAPHICS (MODE 6)

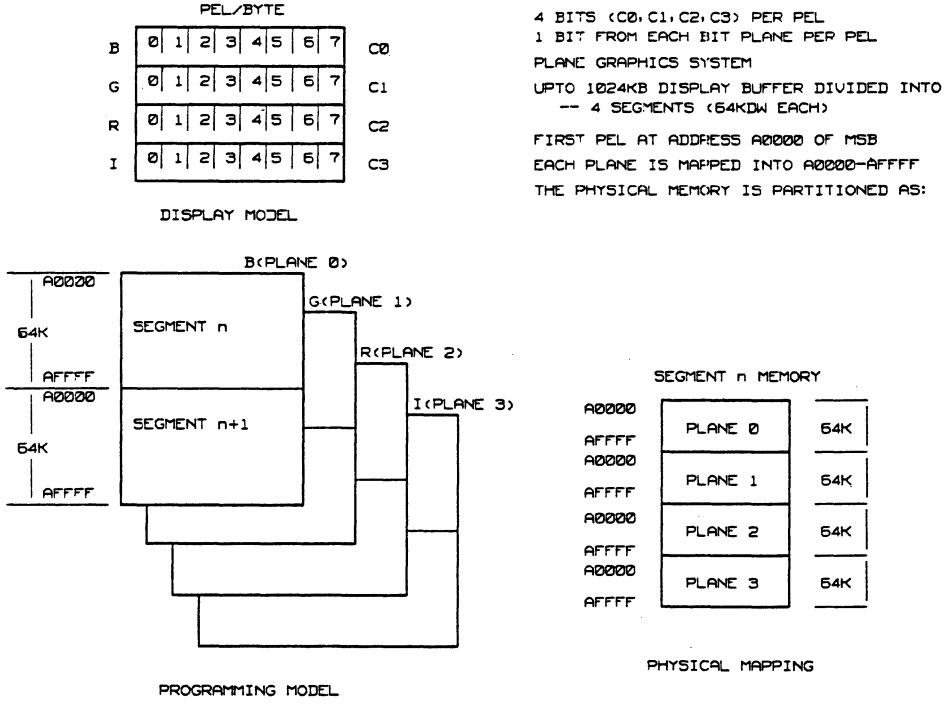


FIG. 3.2.3-4 16 COLORS PLANE GRAPHICS (MODE D, E, 10, 12, 25, 29,37)

3.0

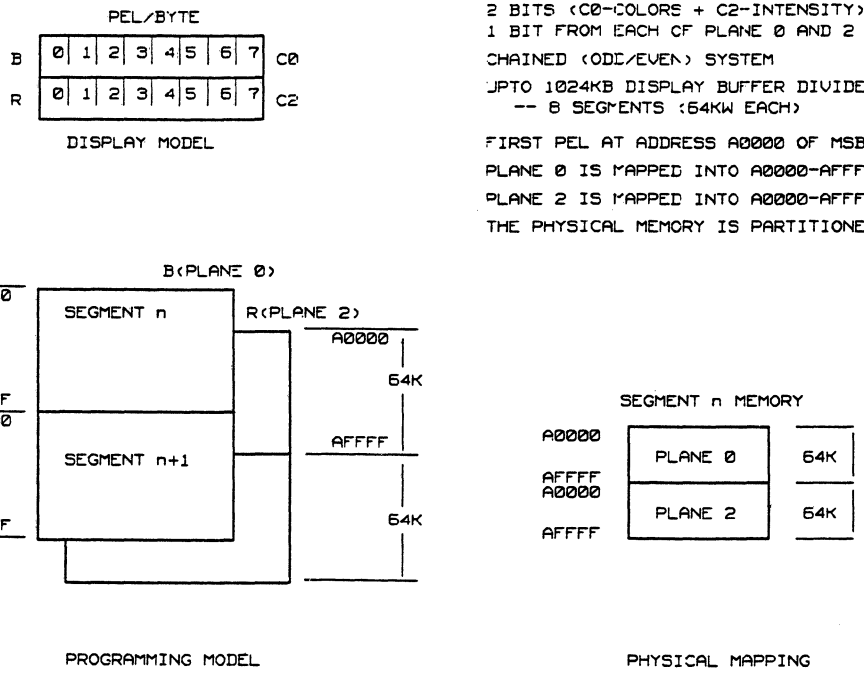


FIG. 3.2.3-5 2 COLORS CHAINED GRAPHICS (MODE F)

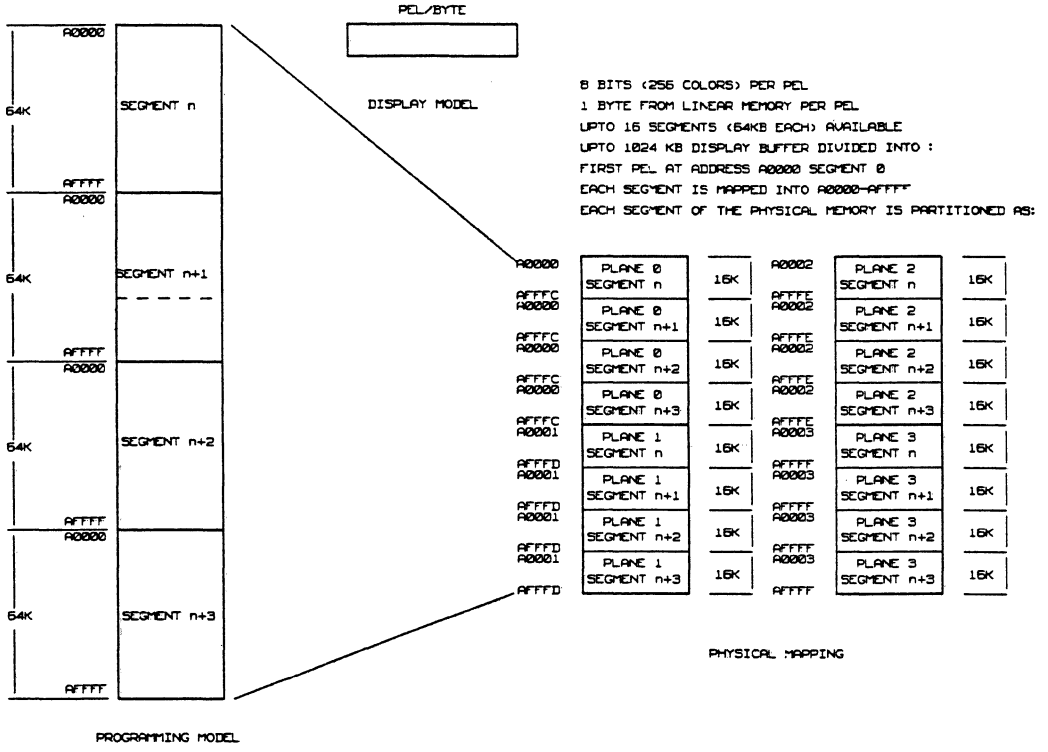


FIG. 3.2.3-6 256 COLOR GRAPHICS (MODE 13, 2D, 2E, 2F, 30, 38, ETC.)

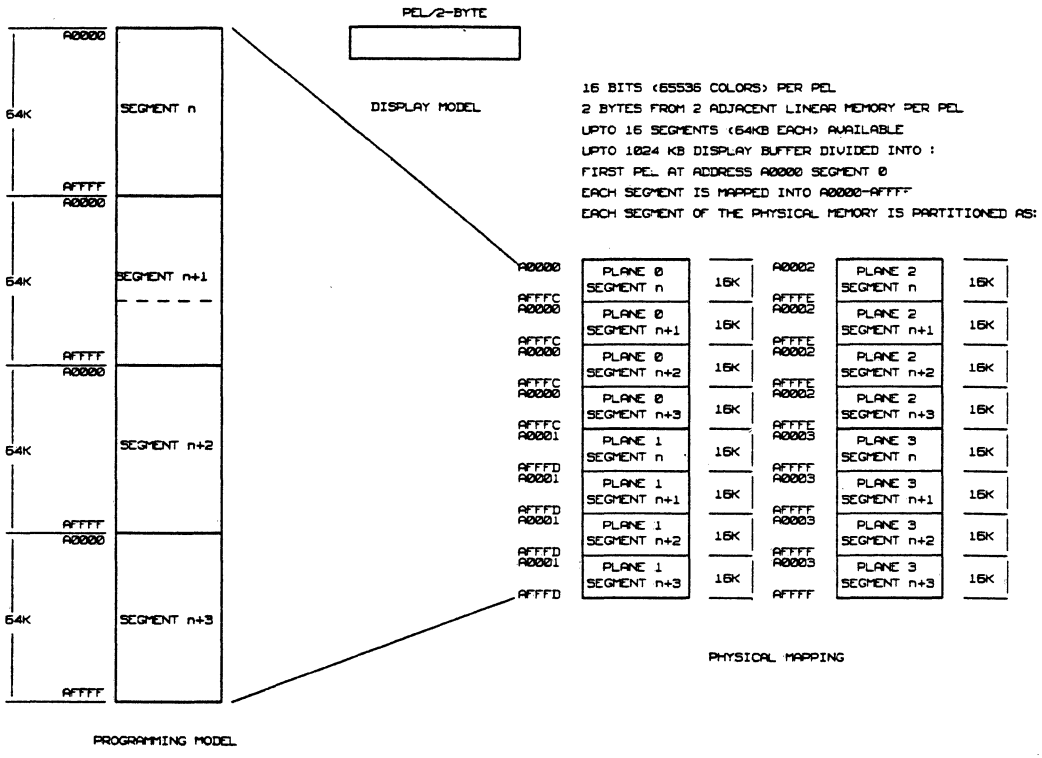


FIG. 3.2.3-7 65536 COLOR GRAPHICS

VGA MODES

Table 3.2.4-1 General Registers

General Registers

Name	Register Port	Index	MODE OF OPERATION 0/0*/0+	1/1*	2/2*/2+	3/3*	4	5	6	7/7+	D	E	F	10	11	12	13	22	23	24	25	26	29	2A	2D	2E	30	37i	37n	2F	38i	38n
Misc Output	3CC/3C2		63/A/3/63	63/A3	63/A3/63	63/A3	63	63	63	A2/62	63	63	A2	A3	E3	E3	63	A7	A7	A7	E3	E3	EF	EF	A3	E3	EF	2F	3F	63	2F	3F

Timing Sequencer

Table 3.2.4-2 Timing Sequencer Registers

Name	Register Port	Index	MODE OF OPERATION 0/0*/0+	1/1*	2/2*/2+	3/3*	4	5	6	7/7+	D	E	F	10	11	12	13	22	23	24	25	26	29	2A	2D	2E	30	37i	37n	2F	38i	38n
TS Index	3C4																															
Synch Reset	3C5	00	03/03/03	03/03	03/03/03	03/03	03	03	03	03/03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
TS Mode	3C5	01	09/09/08	09/09	01/01/00	01/01	09	09	01	00/00	09	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
Wrte Plane Msk	3C5	02	03/03/03	03/03	**03/03/03**	03/03	03	03	01	03/03	0F	0F	0F	0F	0F	0F	0F	03	03	03	0F	03	0F	03	0F	0F	0F	0F	0F	0F	0F	0F
Font Select	3C5	03	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Memory Mode	3C5	04	02/02/02	02/02	02/02/02	02/02	02	02	06	03/02	06	06	06	06	06	06	0E	03	03	03	06	02	06	03	0E	0E	0E	06	06	0E	0E	0E
Reserved	3C5	05																														
TS STAT	3C5	06	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
TS Aux Mode	3C5	07	BC/BC/BC	BC/BC	BC/BC/BC	BC/BC	BC	BC	BC	BC/BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC

CRT Controller Registers

Table 3.2.4-3 CRT Controller Registers

Name	Port	Register Index	MODE OF OPERATION 0/0*/0+	1/1*	2/2*/2+	3/3*	4	5	6	7/7+	D	E	F	10	11	12	13	22	23	24	25	26	29	2A	2D	2E	30	37i	37n	2F	38i	38n
CRTC Index	3D4		-	-	-	-	-	-	-	-																						
Horiz Tot	3D5	00	2D/2D/2D	2D/2D	5F/5F/5F	5F/5F	2D	2D	5F	5F/5F	2D	5F	5F	5F	5F	5F	5F	97	97	97	5F	5F	7F	7F	5F	5F	7F	99	A1	5F	99	A1
Hor Dis End	3D5	01	27/27/27	27/27	4F/4F/4F	4F/4F	27	27	4F	4F/4F	27	4F	4F	4F	4F	4F	4F	83	83	83	4F	4F	63	63	4F	4F	63	7F	7F	4F	7F	7F
Hor Blnk Strt	3D5	02	28/28/28	28/28	50/50/50	50/50	28	28	50	50/50	28	50	50	50	50	50	50	84	84	84	50	50	64	64	50	50	64	7F	80	50	7F	80
Hor Blnk End	3D5	03	90/90/90	90/90	82/82/82	82/82	90	90	82	82/82	90	82	82	82	82	82	82	1A	1A	1A	82	82	02	02	82	82	02	1D	04	82	1D	04
Hor Sync Strt	3D5	04	2B/2B/2B	2B/2B	55/55/55	55/55	2B	2B	54	55/55	2B	54	54	54	54	54	54	8D	8D	8D	54	55	64	65	54	54	64	83	88	54	83	88
Hor Sync End	3D5	05	A0/A0/A0	A0/A0	81/81/81	81/81	80	80	80	81/81	80	80	80	80	80	80	80	16	16	16	80	81	17	18	80	80	17	17	9E	80	17	9E
Vert Tot	3D5	06	BF/BF/BF	BF/BF	BF/BF/BF	BF/BF	BF	BF	BF	BF/BF	BF	BF	BF	BF	0B	0B	BF	76	77	7A	0B	0B	77	77	C0	0B	77	2F	26	BF	2F	26
Ovrflow Low	3D5	07	1F/1F/1F	1F/1F	1F/1F/1F	1F/1F	1F	1F	1F	1F/1F	1F	1F	1F	1F	3E	3E	1F	1F	1F	1F	3E	3E	F0	F0	1F	3E	F0	F5	FD	1F	F5	FD
Init Row Addr	3D5	08	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Max Row Addr	3D5	09	C7/4D/4F	C7/4D	C7/4D/4F	C7/4D	C1	C1	C1	4D/4F	C0	C0	40	40	40	40	41	47	4D	4C	40	47	60	6E	40	40	60	60	60	40	60	60
Cursor Strt	3D5	0A	06/0B/0D	06/0B	06/0B/0D	06/0B	00	00	00	0B/0D	00	00	00	00	00	00	00	06	0B	0A	00	06	00	0C	00	00	00	00	00	00	00	00
Cursor End	3D5	0B	07/0C/0E	07/0C	07/0C/0E	07/0C	00	00	00	0C/0E	00	00	00	00	00	00	00	07	0C	0B	00	07	00	0D	00	00	00	00	00	00	00	00
Lin Strt Mid	3D5	0C	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Lin Strt Low	3D5	0D	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Cursor Mid	3D5	0E	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Cursor Low	3D5	0F	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Vrt Sync Strt	3D5	10	9C/83/9C	9C/83	9C/83/9C	9C/83	9C	9C	9C	83/9C	9C	9C	83	83	EA	EA	9C	66	64	6E	EA	EA	60	60	83	EA	60	08	08	9C	08	08
Vrt Sync End	3D5	11	8E/85/8E	8E/85	8E/85/8E	83/85	8E	8E	8E	85/8E	8E	8E	85	85	8C	8C	8E	88	86	80	8C	8C	82	82	85	8C	82	80	8A	8E	80	8A
Vrt Dis End	3D5	12	8F/5D/8F	8F/5D	8F/5D/8F	8F/5D	8F	8F	8F	5D/8F	8F	8F	5D	5D	DF	DF	8F	5F	5D	6B	DF	DF	57	57	5D	DF	57	FF	FF	8F	FF	FF
Row Offset	3D5	13	14/14/14	14/14	28/28/28	28/28	14	14	28	28/28	14	28	28	28	28	28	28	42	42	42	28	28	32	32	50	50	64	40	40	50	80	80
Underline Row	3D5	14	1F/1F/1F	1F/1F	1F/1F/1F	1F/1F	00	00	00	0D/0F	00	00	0F	0F	00	00	40	1F	1F	1F	00	1F	00	1F	60	60	60	00	00	60	60	60
Vrt Blnk Strt	3D5	15	96/63/96	96/63	96/63/96	96/63	96	96	96	63/96	96	96	63	63	E7	E7	96	62	60	6C	E7	E7	5B	5B	63	E7	5B	FF	04	96	FF	04
Vrt Blnk End	3D5	16	B9/BA/B9	B9/BA	B9/BA/B9	B9/BA	B9	B9	B9	BA/B9	B9	B9	BA	BA	04	04	B9	75	75	7A	04	04	75	75	BA	04	75	30	22	B9	30	22
CRTC Mode	3D5	17	A3/A3/A3	A3/A3	A3/A3/A3	A3/A3	A2	A2	C2	A3/A3	E3	E3	E3	E3	C3	E3	A3	A3	A3	A3	E3	A3	C3	A3	AB	AB	AB	C3	C3	AB	AB	AB
Line Compare	3D5	18	FF/FF/FF	FF/FF	FF/FF/FF	FF/FF	FF	FF	FF	FF/FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
Display Memory	3D5	32																														
Ext'd Strt Add	3D5	33	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Compat. Ctrl	3D5	34																														
Overflow Hi	3D5	35	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	80	00	00	80	00	
Video Sys. 1	3D5	36																														
Video Sys. 2	3D5	37																														

* EGA 350 scan line mode +VGA 400 scan line mode i = interlaced n = non-interlaced

NOTE: EGA-compatible modes are = 010; VGA-compatible modes are = 013; all others are TLI extended modes.

3.2.4 Operation Mode Tables

The following tables summarize the values to be programmed into the ET4000 registers for the various modes of operation.

Table 3.2.4-4 GDC Registers

GDC Registers

Name	Register Port	Index	Mode of Operation																												
			0/0*/0+	1/1/1*	2/2*/2+	3/3/3*	4	5	6	7/7+	D	E	F	10	11	12	13	22	23	24	25	26	29	2A	2D	2E	30	37i	37n	2F	38i	38n
PEL Add/Dat Wd	3CB																														
Segment Select	3CD																														
GDC Index	3CE																														
Set/Reset	3CF	00	00/00/00	00/00/00	00/00/00	00/00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Enabl Set/Res	3CF	01	00/00/00	00/00/00	00/00/00	00/00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Color Compare	3CF	02	00/00/00	00/00/00	00/00/00	00/00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Data Rotate	3CF	03	00/00/00	00/00/00	00/00/00	00/00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Read Plane Sel	3CF	04	00/00/00	00/00/00	00/00/00	00/00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
GDC Mode	3CF	05	10/10/10	10/10/10	10/10/10	10/10/10	30	30	00	10/10	00	00	00	00	00	00	40	10	10	10	00	10	00	10	40	40	40	00	00	40	40	40
Miscellaneous	3CF	06	0E/0E/0E	0E/0E/0E	0E/0E/0E	0E/0E/0E	0F	0F	0D	0A/0A	05	05	05	05	05	05	05	0E	0E	0E	05	0E	05	0E	05	05	05	05	05	05	05	05
Color Care	3CF	07	00/00/00	00/00/00	00/00/00	00/00/00	00	00	00	00/00	0F	0F	05	0F	01	0F	0F	00	00	00	0F	0F	0F	00	0F	0F	0F	0F	0F	0F	0F	0F
Bit Mask	3CF	08	FF/FF/FF	FF/FF/FF	FF/FF/FF	FF/FF/FF	FF	FF	FF	FF/FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

Table 3.2.4-5 ATC Indexed Registers

ATC Indexed Registers

Name	Register Port	Index	Mode of Operation																												
			0/0*/0+	1/1*	2/2*/2+	3/3*	4	5	6	7/7+	D	E	F	10	11	12	13	22	23	24	25	26	29	2A	2D	2E	30	37i	37n	2F	38i	38n
ATC Index R/W 3C0 All=R:3C1/W:3C0																															
Palette		00	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Palette		01	01/01/01	01/01	01/01/01	01/01	13	13	17	08/08	01	01	08	01	3F	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01
Palette		02	02/02/02	02/02	02/02/02	02/02	15	15	17	08/08	02	02	00	02	3F	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02	02
Palette		03	03/03/03	03/03	03/03/03	03/03	17	17	17	08/08	03	03	00	03	3F	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03	03
Palette		04	04/04/04	04/04	04/04/04	04/04	02	02	17	08/08	04	04	18	04	3F	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04	04
Palette		05	05/05/05	05/05	05/05/05	05/05	04	04	17	08/08	05	05	18	05	3F	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05	05
Palette		06	06/14/14	06/14	06/14/14	06/14	06	06	17	08/08	06	06	00	14	3F	14	06	14	14	14	14	14	14	14	06	06	06	14	14	06	06	06
Palette		07	07/07/07	07/07	07/07/07	07/07	07	07	17	08/08	07	07	00	07	3F	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
Palette		08	10/38/38	10/38	10/38/38	10/38	10	10	17	10/10	10	10	00	38	3F	38	08	38	38	38	38	38	38	38	08	08	08	38	38	08	08	08
Palette		09	11/39/39	11/39	11/39/39	11/39	11	11	17	18/18	11	11	08	39	3F	39	09	39	39	39	39	39	39	39	09	09	09	39	39	09	09	09
Palette		0A	12/3A/3A	12/3A	12/3A/3A	12/3A	12	12	17	18/18	12	12	00	3A	3F	3A	0A	3A	3A	3A	3A	3A	3A	3A	0A	0A	0A	3A	3A	0A	0A	0A
Palette		0B	13/3B/3B	13/3B	13/3B/3B	13/3B	13	13	17	18/18	13	13	00	3B	3F	3B	0B	3B	3B	3B	3B	3B	3B	3B	0B	0B	0B	3B	3B	0B	0B	0B
Palette		0C	14/3C/3C	14/3C	14/3C/3C	14/3C	14	14	17	18/18	14	14	00	3C	3F	3C	0C	3C	3C	3C	3C	3C	3C	3C	0C	0C	0C	3C	3C	0C	0C	0C
Palette		0D	15/3D/3D	15/3D	15/3D/3D	15/3D	15	15	17	18/18	15	15	18	3D	3F	3D	0D	3D	3D	3D	3D	3D	3D	3D	0D	0D	0D	3D	3D	0D	0D	0D
Palette		0E	16/3E/3E	16/3E	16/3E/3E	16/3E	16	16	17	18/18	16	16	00	3E	3F	3E	0E	3E	3E	3E	3E	3E	3E	3E	0E	0E	0E	3E	3E	0E	0E	0E
Palette		0F	17/3F/3F	17/3F	17/3F/3F	17/3F	17	17	17	18/18	17	17	00	3F	3F	3F	0F	3F	3F	3F	3F	3F	3F	3F	0F	0F	0F	3F	3F	0F	0F	0F
Mode Ctrl		10	08/08/0C	08/08	08/08/0C	08/08	01	01	01	0E/0E	01	01	0B	01	01	01	41	08	08	08	01	00	01	08	01	01	01	01	01	01	01	01
Overscan Clr		11	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Clr Plane En		12	0F/0F/0F	0F/0F	0F/0F/0F	0F/0F	03	03	01	0F/0F	0F	0F	05	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
Hor Pix Pan		13	00/00/08	00/00	00/00/08	00/00	00	00	00	08/08	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Color Select		14	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Miscellaneous		16	00/00/00	00/00	00/00/00	00/00	00	00	00	00/00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

* EGA 350 scan line mode
+VGA 400 scan line mode
NOTE: EGA-compatible modes are <= 010;
VGA-compatible modes are <= 013;
all others are TLI extended modes.
i=interlaced n=non-interlaced

Table 3.2.4-6 General Registers
General Registers

Name	Register Port	Index	Mode of Operation											
			0/0	1/1	2/2	3/3	4	5	6	7	D	E	F	10
Misc 1	3C2	-	23/A7	23/A7	23/A7	23/A7	23	23	23	A6	23	23	A2	A7
Input Stat 0	3C2	-	-/-	-/-	-/-	-/-	-	-	-	-	-	-	-	-
Input Stat 1	3DA	-	-/-	-/-	-/-	-/-	-	-	-	-	-	-	-	-
Feature Ctrl	3DA	-	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00

Table 3.2.4-7 Timing Sequencer Registers
Timing Sequencer

Name	Register Port	Index	Mode of Operation											
			0/0	1/1	2/2	3/3	4	5	6	7	D	E	F	10
TS Index	3C4	-	-/-	-/-	-/-	-/-	-	-	-	-	-	-	-	-
Synch Reset	3C5	00	03/03	03/03	03/03	03/03	03	03	03	03	03	03	03	03
TS Mode	3C5	01	0B/0B	0B/0B	01/01	01/01	0B	0B	01	00	0B	01	01	01
Wrte Plane Msk	3C5	02	03/03	03/03	03/03	03/03	03	03	01	03	0F	0F	0F	0F
Font Select	3C5	03	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Memory Mode	3C5	04	03/03	03/03	03/03	03/03	02	02	06	03	06	06	06	06

Table 3.2.4-8 CRT Controller Registers
CRT Controller Registers

Name	Register Port	Index	Mode of Operation											
			0/0	1/1	2/2	3/3	4	5	6	7	D	E	F	10
CRTC Index	3D4	-	-/-	-/-	-/-	-/-	-	-	-	-	-	-	-	-
Horiz Tot	3D5	00	37/2D	37/2D	70/5B	70/5B	37	37	70	60	37	70	60	5B
Hor Dis End	3D5	01	27/27	27/27	4F/4F	4F/4F	27	27	4F	4F	27	4F	4F	4F
Hor Blnk Strt	3D5	02	2D/2B	2D/2B	5C/53	5C/53	2D	2D	59	56	2D	59	56	53
Hor Blnk End	3D5	03	37/2D	37/2D	2F/37	2F/37	37	37	2D	3A	37	2D	3A	37
Hor Sync Strt	3D5	04	31/28	31/28	5F/51	5F/51	30	30	5E	51	30	5E	50	52
Hor Sync End	3D5	05	15/6D	15/6D	07/5B	07/5B	14	14	06	60	14	06	60	00
Vert Tot	3D5	06	04/6C	04/6C	04/6C	04/6C	04	04	04	70	04	04	70	6C
Ovrflow Low	3D5	07	11/1F	11/1F	11/1F	11/1F	11	11	11	1F	11	11	1F	1F
Init Row Addr	3D5	08	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Max Row Addr	3D5	09	07/0D	07/0D	07/0D	07/0D	01	01	01	0D	00	00	00	00
Cursor Strt	3D5	0A	06/06	06/06	06/06	06/06	00	00	00	0B	00	00	00	00
Cursor End	3D5	0B	07/07	07/07	07/07	07/07	00	00	00	0C	00	00	00	00
Lin Strt Mid	3D5	0C	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Lin Strt Low	3D5	0D	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Cursor Mid	3D5	0E	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Cursor Low	3D5	0F	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Vrt Sync Strt	3D5	10	E1/5E	E1/5E	E1/5E	E1/5E	E1	E1	E0	5E	E1	E0	5E	5E
Vrt Sync End	3D5	11	24/2B	24/2B	24/2B	24/2B	24	24	23	2E	24	23	2E	2B
Vrt Dis End	3D5	12	C7/5D	C7/5D	C7/5D	C7/5D	C7	C7	C7	5D	C7	C7	5D	5D
Row Offset	3D5	13	14/14	14/14	28/28	28/28	14	14	28	28	14	28	28	28
Underline Row	3D5	14	08/0F	08/0F	08/0F	08/0F	00	00	00	00	00	00	0D	0F
Vrt Blnk Strt	3D5	15	E0/5E	E0/5E	E0/5E	E0/5E	E0	E0	DF	5E	E0	DF	5E	5F
Vrt Blnk End	3D5	16	F0/0A	F0/0A	F0/0A	F0/0A	F0	F0	EF	0E	F0	EF	0E	0A
CRTC Mode	3D5	17	A3/A3	A3/A3	A3/A3	A3/A3	A2	A2	C2	A3	E3	E3	E3	E3
Line Compare	3D5	18	FF/FF	FF/FF	FF/FF	FF/FF	FF	FF	FF	FF	FF	FF	FF	FF

HiRes/Attached to HiRes monitor
(HiRes >16K; HiRes monitor >640x350 pixel resolution)

Table 3.2.4-9 GDC Registers
GDC Registers

Name	Register Port	Index	Mode of Operation 0/0	1/1	2/2	3/3	4	5	6	7	D	E	F	10
PEL Add/Dat Wd	3CB													
Segment Select	3CD													
GDC Index	3CE	-/-	-/-	-/-	-/-	-	-	-	-	-	-	-	-	-
Set/Reset	3CF	00	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Enabl Set/Res	3CF	01	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Color Compare	3CF	02	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Data Rotate	3CF	03	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Read Plane Sel	3CF	04	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
GDC Mode	3CF	05	10/10	10/10	10/10	10/10	30	30	00	10	00	00	00	00
Miscellaneous	3CF	06	0E/0E	0E/0E	0E/0E	0E/0E	0F	0F	0D	0A	05	05	05	05
Color Care	3CF	07	00/00	00/00	00/00	00/00	00	00	00	00	0F	0F	0F	0F
Bit Mask	3CF	08	FF/FF	FF/FF	FF/FF	FF/FF	FF	FF	FF	FF	FF	FF	FF	FF
Microseq Mode	3CF	0D												
Microseq Reset	3CF	0E												

HiRes/Attached to HiRes monitor
(HiRes >16K; HiRes monitor >640x350 pixel resolution)

Table 3.2.4-10 ATC Registers
ATC Indexed Registers

Name	Register Port	Index	Mode of Operation 0/0	1/1	2/2	3/3	4	5	6	7	D	E	F	10
ATC Index R/W 3C0 All = R:3C1/W:3C0		-/-	-/-	-/-	-/-	-/-	-	-	-	-	-	-	-	-
Palette		00	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Palette		01	01/01	01/01	01/01	01/01	13	13	17	08	01	01	08	01
Palette		02	02/02	02/02	02/02	02/02	15	15	17	08	02	02	00	02
Palette		03	03/03	03/03	03/03	03/03	17	17	17	08	03	03	00	03
Palette		04	04/04	04/04	04/04	04/04	02	02	17	08	04	04	18	04
Palette		05	05/05	05/05	05/05	05/05	04	04	17	08	05	05	18	05
Palette		06	06/14	06/14	06/14	06/14	06	06	17	08	06	06	00	14
Palette		07	07/07	07/07	07/07	07/07	07	07	17	08	07	07	00	07
Palette		08	10/38	10/38	10/38	10/38	10	10	17	10	10	10	00	38
Palette		09	11/39	11/39	11/39	11/39	11	11	17	18	11	11	08	39
Palette		0A	12/3A	12/3A	12/3A	12/3A	12	12	17	18	12	12	00	3A
Palette		0B	13/3B	13/3B	13/3B	13/3B	13	13	17	18	13	13	00	3B
Palette		0C	14/3C	14/3C	14/3C	14/3C	14	14	17	18	14	14	00	3C
Palette		0D	15/3D	15/3D	15/3D	15/3D	15	15	17	18	15	15	18	3D
Palette		0E	16/3E	16/3E	16/3E	16/3E	16	16	17	18	16	16	00	3E
Palette		0F	17/3F	17/3F	17/3F	17/3F	17	17	17	18	17	17	00	3F
Mode Ctrl		10	08/08	08/08	08/08	08/08	01	01	01	0E	01	01	0B	01
Overscan Clr		11	00/00	00/00	00/00	00/00	00	00	00	00	00	00	00	00
Clr Plane En		12	0F/0F	0F/0F	0F/0F	0F/0F	03	03	01	0F	0F	0F	05	0F
Hor Pix Pan		13	00/00	00/00	00/00	00/00	00	00	00	08	00	00	00	00

HiRes/Attached to HiRes monitor
(HiRes)16K; HiRes monitor)640x350 pixel resolution)

4.0 ET4000 REGISTER DESCRIPTIONS

4.1 Overview

The following is a general overview of the ET4000 registers relating to I/O addresses, and type.

Table 4.1-1 ET4000 Registers, R/W Operation, Port Addresses

Register	R/W Operation	I/O Port Address
General		
Misc. Output	W	03C2
	R	03CC
Input Status 0	R	03C2
Input Status 1	R	03#A
Feature Control	W	03#A
	R	03CA
Video Subsystem Enable	RW	03C3/46E8
External Palette RAM		
PEL MASK	RW	003C6
PEL WRITE ADDRESS	RW	003C8
PEL DATA	RW	003C9
PEL READ ADDRESS	W	003C7
DAC STATE	R	003C7
ATC		
Address/Index	W	03C0 (Index)
	R	03C0
Indexed registers	W	03C0 (Data)
	R	03C1
CRTC		
Address/Index	RW	03#4
Indexed registers	RW	03#5
TS		
Address/Index	RW	03C4
Indexed registers	RW	03C5
GDC		
Segment Select	RW	03CD
Address/Index	RW	03CE
Indexed registers	RW	03CF

= B in monochrome emulation modes; D in color emulation modes, controlled by bit 0 in the Miscellaneous Output Register.

These registers are described in more detail as follows.

4.2 General Registers

The ET4000 has five General Registers, each with its own port address allowing direct programming access, and requiring no pairing of index and data registers. The Input Status #1 and Feature Control registers have separate addresses for monochrome and color modes.

Miscellaneous Output Register
This is a read/write register.
R/W : Port address = 3CC input; 3C2 output

Bit	Description
0	I/O Address Select.
1	Enable RAM.
2	Clock Select 0.
3	Clock Select 1.
4	Reserved.
5	Page Select for Odd/Even.
6	Horizontal Retrace Polarity.
7	Vertical Retrace Polarity.

Hardware resets return all bits to zero.

Bit 0, when set to 1, sets CRTC addresses to 3DX and Input Status Register 1's address to 3DA for Color/Graphics Monitor Adapter emulation. A logical 0 sets CRTC addresses to 3BX and Input Status Register 1's address to 3BA for monochrome emulation.

Bit 1, when set to 1, enables Display Memory Access to respond at addresses designated by the Control Data Select value programmed into the Graphics Controllers. A logical 0 disables Display Memory Access from the processor.

Bits 3 and 2 are used to select the clock rate according to the following table:

Bits 3 2	
0 0	Selects MCLK clock 1
0 1	Selects MCLK clock 2
1 0	Selects MCLK clock 3
1 1	Selects MCLK clock 4

Bits 3 and 2 of the MISCOUT register (CS⟨1:0⟩) can be translated to provide compatibility between the EGA mode and the EGA monitor when the external clock select circuit is connected as follows:

CS1	CS0	Clock Frequency
1	1	---
1	0	32.514MHz
0	1	28.322MHz
0	0	25.175MHz

The clock select bits CS⟨1:0⟩ can be translated by the ET4000 according to the following conditions:

NOTES: 1. EMCK = CRTC index 34 bit 0 and ENXL = CRTC index bit 5.
2. If CS⟨1:0⟩ are used to select the external switch setting, care must be taken to ensure proper selection of the switch setting after the translation of CS⟨1:0⟩.

In VGA mode:

a. If EMCK bit is set to 0: CS⟨1:0⟩ are equal to the programmed value.
b. If EMCK bit is set to 1: CS⟨1⟩ is equal to the programmed value, and CS⟨0⟩ is equal to inversion of programmed value.

In EGA mode:

a. if ENXL = 0 then:

programmed CS⟨1:0⟩	output CS⟨1:0⟩
1 1	0 0
1 0	1 1
0 1	1 0
0 0	0 1

b. if ENXL = 1 then:
a. If EMCK bit is set to 0: CS⟨1:0⟩ are equal to the programmed value.
b. If EMCK bit is set to 1: CS⟨1⟩ is equal to the programmed value, and CS⟨0⟩ is equal to inversion of programmed value.

In 6845 modes: CS⟨1:0⟩ are equal to the programmed value.

Bit 5 selects between two 64K pages of memory when in the Odd/Even modes (0,1,2,3,7). When set to 1, it is the default for operation of the HiRes text mode. A logical 0 selects the high page of memory.

Bit 6, when set to 1, selects negative horizontal retrace polarity. A logical 0 selects positive horizontal polarity retrace.

Bit 7, when set to 1, selects negative vertical retrace. A logical 0 selects positive vertical retrace. The relationship between vertical screen size and polarities is as follows:

Vsync polarity	Hsync polarity	Vertical size
+	+	768 lines
+	-	400 lines
-	+	350 lines
-	-	480 lines

Input Status Register Zero
This is a read-only register.
R/O : Port address = 3C2

Bit	Description
0-3	Reserved.
4	Switch Sense.
5	Feature code 0.
6	Feature code 1.
7	CRT Interrupt.

NOTE: the "KEY" must be set in order to read bits 5 and 6.

To set the KEY:
- Write 03 to Hercules Compatibility Register (3BF);
- Write A0 to Mode Control Register (3#8);

```
mov     dx,3BFh
mov     al,3
out     dx,al
mov     dx,3D8h      ;3B8h in mono mode
mov     al,0A0h
out     dx,al
```

Bit 4 input can be used to determine the default video mode upon power up, or the type of monitor connected to the system. The Clock Select field (bits 2,3 in the Miscellaneous Output Register) setting determines the switch to read.

Bit 5 and 6 inputs can be used to determine the type of monitor connected to the system. Input status is from external feature input.

NOTE: The external feature input bits 6 & 5 are DB⟨1:0⟩ bus status at the last REST low-to-high transition. If the DB⟨1:0⟩ are not "pull-down" by a 1K resistor, then an "11" status will be the default value.

Bit 7, when set to 1, indicates a pending vertical retrace interrupt. A logical 0 means that the vertical retrace interrupt has been cleared.

Input Status Register One

This is a read/only register.
R/O : Port address = 3BA (mono)/3DA (color)

Bit	Description
0	Display enable complement.
1-2	Reserved (=0).
3	Vertical retrace.
4-5	Video display feedback test.
6	Reserved (=0).
7	Vertical retrace complement.

Bit 0, when set to 1, indicates a vertical or horizontal retrace interval and is the realtime status of the inverted display enable signal.

Bit 3, when set to 0, indicates that video data is currently being displayed. A logical 1 indicates a vertical retrace interval during the vertical sync pulse.

Bits 4 and 5 are used for diagnostic purposes. They are selectively connected to two of the eight color outputs of the Attribute Controller. The Color Plane Enable (ATC Indexed Register 12) register controls the multiplexer for the video wiring. Available combinations are:

Color Plane Register Bits	
5	4
0	0
0	1
1	0
1	1

Input Status Register One Bits	
5	4
P2	P0
P5	P4
P3	P1
P7	P6

Bit 7, when set to 1, indicates that video data is currently being displayed. A logical 0 indicates a vertical retrace interval during the vertical sync pulse.

Feature Control Register

This is a read/write register.
R/W : Port address = 3CA input; 3BA/3DA output

Bit	Description
0	Feat (0)
1	Feat (1)
2	Reserved
3	Reserved
4	Reserved
5	Reserved.
6	Reserved
7	Enable NMI generation

NOTE: The "KEY" must be set in order to read bit 7. See Input Status Register Zero for definition of "KEY".

Bits 0,1 are Feat(0) and Feat(1) bits from the Feature Connector.

Bit 7, when set to 1, enables a non-maskable interrupt (NMI). This bit can only be set when in 6845 compatibility mode (CRTC 34 bit 7 = 1).

Normally, the XROML output pin is defined as external translation ROM enable. When bit 7 of the Feature Control Register is set to 1, the XROML output will be defined as the NMI output pin (See Section 2.2.6). This bit can only be set if the 6845 emulation mode is active.

Video Subsystem Register

This is a read/write register.
R/W : Port address = 3C3/46E8

Bit	Description
0	Select video subsystem (address 03C3).
1-2	Reserved.
3	Select video subsystem (address 46E8).
4-7	Reserved (=0).

Bit 0, when set to 1, enables the video subsystem when the port address is configured for address 3C3).

Bit 3, when set to 1, selects the video subsystem when the port address is configured for 46E8.

To configure the VSE (Video Subsystem Enable) register to 3C3, the CRTC Index Register 34 bit 3 (ENVS) must be set to 0. This is the power-up default configuration. When this bit is set to 1, the VSE port address is 46E8.

4.2.1 6845 Compatibility

The ET4000 features register-level compatibility with the 6845 chip. The input/output control ports used in setting up the basic display formats are as follows:

Port	I/O Port Address
6845 CRT control register	03#4
6845 CRT data register	03#5
Display mode control	03#8
Display color control	03D9
Display status control	03#A

Display Mode Control Register
This is a read/write register.
R/W : Port address = 3D8 (color)

Bit	Description
0	80x25 text mode.
1	Enable graphics mode.
2	B&W mode.
3	Enable screen display.
4	640x200 mode.
5	Enable blink (text mode only).
6	Bit 1 of the Hercules Compatibility Register (3BF).
7	Reserved.

Bit 0, when set to 1, selects the 80x25 A/N mode. When set to 0, selects 40x25 A/N mode.

Bit 1, when set to 1, selects the 320x200 APA mode. When set to 0, selects the A/N mode.

Bit 2, when set to 1, selects the black and white mode. When set to 0, selects color mode.

Bit 3, when set to 1, enables the video signal during mode changes.

Bit 4, when set to 1, selects the 640x200 black and white graphics mode.

Bit 5, when set to 1, changes the character background intensity to the blinking attribute function in A/N modes.

Bit 6, bit 1 of the Hercules Compatibility Register, is a read-only bit.

Display Mode Control Register

This is a read/write register.
R/W : Port address = 3B8 (monochrome)

Bit	Description
0	80x25 text mode.
1	Monochrome graphics mode.
2	Reserved.
3	Enable screen display.
4	Reserved.
5	Enable blink.
6	Bit 1 of the Hercules Compatibility Register (3BF).
7	Page select.

Bit 0, when set to 1, selects the 80x25 A/N mode. When set to 0, selects 40x24 A/N mode.

Bit 1, when set to 1, selects the monochrome graphics mode.

Bit 3, when set to 1, enables the video signal during mode changes.

Bit 5, when set to 1, changes the character background intensity to the blinking attribute function in A/N modes.

Bit 6, bit 1 of the Hercules Compatibility Register, is a read-only bit.

Bit 7, when set to 1, selects the top 32KB page starting at B8000 for display (for Hercules display compatibility). When set to 0, selects the low 32KB page (starting at B0000).

NOTE: This bit can be set only when bit 1 of the Hercules Compatibility Register (3BF) is set to 1.

Color Select Register
This is a write/only register.
W/O : Port address = 3D9

This 6-bit output register determines the border color, background color, and color intensity.

Bit	Description
0	Blue border color in A/N mode. Blue background color in 320x200 APA mode. Blue foreground color in 640x200 APA mode.
1	Green border color in A/N mode. Green background color in 320x200 APA mode. Green foreground color in 640x200 APA mode.
2	Red border color in A/N mode. Red background color in 320x200 APA mode. Red foreground color in 640x200 APA mode.
3	Intensified border color in A/N mode. Intensified background color in 320x200 APA mode. Intensified foreground color in 640x200 APA mode.
4	Select intensified foreground colors in 320x200 APA mode.
5	320x200 color set select.
6	Reserved.
7	Reserved.

Bits 0-3 are used to select the background color in the 320x200 graphics mode, the foreground color in the 640x200 graphics mode, and the border color in the 40x24 alphanumeric mode.

Bit 4, when set to 1, selects intensified foreground colors for 320x200 graphics mode.

Bit 5, used only in 320x200 graphics mode, is used to select an active set of colors for the screen display.

When bit 5 is set to 1 the colors are as follows:

C1	C0	Colors
0	0	Background (defined by bits 0:3 at 3D9).
0	1	Cyan.
1	0	Magenta.
1	1	White.

When bit 5 is set to 0 the colors are as follows:

C1	C0	Colors
0	0	Background (defined by bits 0:3 at 3D9).
0	1	Green.
1	0	Red.
1	1	Brown.

C1 and C0 are the high and low order bits, respectively, of the 2-bit pixel.

AT&T Mode Control Register

This is a write/only register.
W/O : Port address = 3DE

This is an 8-bit write-only register used to produce 640x400 AT&T-compatible resolution. To enable this register, bit 7 of the 6845 Compatibility Control Register (CRTC Index 34) must be enabled. (Bit 6 is enabled just by bit 6 of CRTC 34; bit 0 requires both bits 6 and 7 of CRTC 34 to be set.) This register must be set while in color mode (Misc. Output Register bit 0=1).

Bit	Description
0	Double scan line mode.
1	Reserved.
2	Alternate font select.
3	Alternate page select.
4	Reserved.
5	Reserved.
6	Underline color attribute enable.
7	Reserved.

Bit 0, double scan bit, when set to 1, simulates AT&T 400-line graphics. When set to 0, simulates IBM 200-line graphics.

Bit 2, Alternate font select, is used to select one of two character fonts stored in font blocks 0 and 1 to be displayed. The font stored in font block 0 is the default font.

Bit 3, Alternate page select, is used to select either of two 16KB pages in memory to be displayed. (**NOTE:** bit 0 must=0 to get 2nd page.)

Bit 6, when set to 1 and the attribute byte (ATT) = 01, the normal blue foreground color attribute will be disabled and the white underline attribute of that character will be enabled.

Hercules Compatibility Register

This is a write/only register.
W/O : Port address = 3BF

This is an 8-bit register with a single bit used to enable the second page of memory (B8000) to provide a full 64K of display memory.

Bit	Description
0	Reserved.
1	Enable second page.
2-7	Reserved.

Bit 1, when set to 1, enables the second page of display memory, starting at B8000, providing 64KB of display memory. This bit can be read from bit 6 of the Display Mode Control Register (3#8).

The following table lists the 6845 CRT controller internal data registers, their functions, and the hexadecimal values used for the illustrated modes.

Table 4.2-1 6845 Color CRT Controller Registers, Functions, and Parameters

Register	Register Number	TEXT 80 x 25	GRAPHICS 40 x 25	320x200 4-color 2-color
Horizontal Total	R0	71h	38h	38h
Horizontal Displayed	R1	50h	28h	28h
Hsync Position	R2	5Ah	2Dh	2Dh
Hsync Width	R3	0Ah	0Ah	0Ah
Vertical Total	R4	1Fh	1Fh	7Fh
Vertical Adjust	R5	06h	06h	06h
Vertical Displayed	R6	19h	19h	64h
Vsync Position	R7	1Ch	1Ch	70h
Interlace Mode	R8	02h	02h	02h
Max. Scan Line Addr.	R9	07h	07h	01h
Cursor Start	R10	06h	06h	06h
Cursor End	R11	07h	07h	07h
Start Address (H)	R12	00h	00h	00h
Start Address (L)	R13	00h	00h	00h
Cursor (H)	R14	00h	00h	00h
Cursor (L)	R15	00h	00h	00h

Table 4.2-2 6845 Monochrome/Hercules CRT Controller Registers, Functions and Parameters

Register	Register Number	TEXT 80 x 25	HERCULES 720 x 348
Horizontal Total	R0	61h	38h
Horizontal Displayed	R1	50h	2Dh
Hsync Position	R2	52h	2Eh
Hsync Width*	R3	OFh	07h
Vertical Total	R4	19h	5Bh
Vertical Adjust	R5	06h	02h
Vertical Displayed	R6	19h	57h
Vsync Position	R7	19h	57h
Interlace Mode	R8	02h	02h
Max. Scan Line Addr.	R9	0Dh	03h
Cursor Start	R10	0Bh	00h
Cursor End	R11	0Ch	00h
Start Address (H)	R12	00h	00h
Start Address (L)	R13	00h	00h
Cursor (H)	R14	00h	00h
Cursor (L)	R15	00h	00h

*Bit 4, during 6845 CRTC mode operation, defines the vertical synchronous output pulse width as either sixteen lines wide (bit 4=0) or two line wide (bit 4=1).

Register descriptions for the 6845 can be found in the register description pages of Motorola and Hitachi chip product catalogs.

4.3 ET4000 CRTC Register Description

The CPU interface to the ET4000 internal CRTC Controller (CRTC) consists of 32 read/write registers. Of these registers, one Register, the CRTC Index Register, is accessed by a separate independent I/O address (3#4, where # = B in monochrome emulation modes; D in color emulation modes, as controlled by bit 0 in the Miscellaneous Output Register.) The remaining 31 registers are internally indexed, which means that they are accessed via a common I/O address (3#5) with one of the 31 registers that is actually accessed selected by the CRTC Index Register.

All values are in hexadecimal unless otherwise noted.

Table 4.3-1 CRTC Index Register

Register Name		Port Address
CRTC Index Register	(Read/Write)	3#4

Table 4.3-2 CRTC Indexed Registers

CRTC Indexed Register Name	CRTC Indexed Address	Port Address
Horizontal Total	0 (Read/Write)	3#5
Horizontal Display End	1 (Read/Write)	3#5
Horizontal Blank Start	2 (Read/Write)	3#5
Horizontal Blank End	3 (Read/Write)	3#5
Horizontal Sync Start	4 (Read/Write)	3#5
Horizontal Sync End	5 (Read/Write)	3#5
Vertical Total	6 (Read/Write)	3#5
Overflow Low	7 (Read/Write)	3#5
Initial Row Addr (Raster Counter)	8 (Read/Write)	3#5
Maximum Row Address	9 (Read/Write)	3#5
Cursor Start Row Address	A (Read/Write)	3#5
Cursor End Row Address	B (Read/Write)	3#5
Linear Starting Address Middle	C (Read/Write)	3#5
Linear Starting Address Low	D (Read/Write)	3#5
Cursor Address Middle	E (Read/Write)	3#5
Cursor Address Low	F (Read/Write)	3#5
Vertical Sync Start	10 (Read/Write)	3#5
Vertical Sync End	11 (Read/Write)	3#5
Vertical Display End	12 (Read/Write)	3#5
Row Offset	13 (Read/Write)	3#5
Underline Row Address	14 (Read/Write)	3#5
Vertical Blank Start	15 (Read/Write)	3#5
Vertical Blank End	16 (Read/Write)	3#5
CRTC Mode	17 (Read/Write)	3#5
Split Scr Start Low (Line Compare)	18 (Read/Write)	3#5
RAS/CAS Configuration	32 (Read/Write)	3#5
Extended Start Address	33 (Read/Write)	3#5
6845 Compatibility Control	34 (Read/Write)	3#5
Overflow High	35 (Read/Write)	3#5
Video System configuration 1	36 (Read/Write)	3#5
Video System configuration 2	37 (Read/Write)	3#5

= B in monochrome emulation modes; D in color emulation modes, controlled by bit 0 in the Miscellaneous Output Register.

NOTE: The "KEY" must be set in order to write CRTC indices above 18, except indices 33 and 35 (CRTC 35 is protected by bit 7 of CRTC 11). See Input Status Register Zero for definition of "KEY".

Many of the CRTC values, such as the Linear Starting Address and the Vertical Sync Start, are broken up into numerous non-adjacent registers. This is because of the need to maintain IBM VGA and EGA compatibility. For example, vertical sync start bits 0-7 are in Register 10 hex, Vertical Sync Start Bits 8 and 9 are in Register 7, Overflow Low. These two registers provide the 10-bit vertical sync start value in IBM's VGA. The ET4000 chip supports 11-bit vertical values, so Register 35 hex, Overflow High, contains bit 10 of the vertical sync start value. Although this can sometimes be awkward, it is the only way to provide both IBM VGA and EGA compatibility and the extended functionality of the ET4000 chip.

Because there are so many ET4000 registers and because many CRTC values are spread over numerous registers, the following table lists many of the registers arranged according to general function.

Table 4.3-3 CRTC Registers By Function

Primary Function	Sub Function	CRTC Index	Indexed Register Name
Horizontal timings	Scan line length	0	Horizontal Total (bit 7:0)
	Display enable	1 3	Horizontal Display End (bit 7:0) Horizontal Blank End (bit 6:5) (Horizontal Display Enable Skew)
	Blanking	2 3 5	Horizontal Blank Start (bit 7:0) Horizontal Blank End (HBE bit 0:4) Horizontal Sync End (HBE bit 5)
	Sync	4 5	Horizontal Sync Start (bit 7:0) Horizontal Sync End (bit 4:0)
Vertical timings	Frame height	6 7 35	Vertical Total (bit 7:0) Overflow Low (VT bit 8,9) Overflow High (VT bit 10)
	Display enable	12 7 35	Vertical Display End (bit 7:0) Overflow Low (VDE bit 8,9) Overflow High (VDE bit 10)
	Blanking	15 7 9 35 16	Vertical Blank Start (bit 7:0) Overflow Low (VBS bit 8) Maximum Row Address (VBS bit 9) Overflow High (VBS bit 10) Vertical Blank End (bit 7:0)
	Sync	10 7 35 11	Vertical Sync Start (bit 7:0) Overflow Low (VSS bit 8,9) Overflow High (VSS bit 10) Vertical Sync End (bit 3:0)
Cursor	Address	F E 33	Cursor Address Low (bit 7:0) Cursor Address Middle (bit 15:8) Extended Start Address (CURA bit 17:16)
	Row Address	A B	Cursor Start Row Address (bit 4:0) Cursor Stop Row Address (bit 4:0)
	Skew	B	Cursor Stop Row Address (bit 6,5)
Memory address	Linear address	D C 33	Linear Start Addr Low (bit 7:0) Linear Start Addr Middle (bit 15:8) Extended Start Address (LA bit 17:16)
	Row offset	13	Row Offset (bit 7:0)
Split screen	Start scan line	9 18 7 35	Maximum Row Addr (Split Scr bit 9) Line Compare (bit 7:0) Overflow Low (Line Compare bit 8) Overflow High (Line Compare bit 10)

For the rest of the descriptions in this section: # = B in monochrome emulation modes; D in color emulation modes, controlled by bit 0 in the Miscellaneous Output Register.

CRTC Index

This is a read/write register.
R/W : Port address 3#4

Bit	Description
0-5	Current CRTC index.
6-7	Reserved.

Bits 0-5 provide the index of the currently selected internally indexed register. The CRTC Index register determines which CRTC indexed register will be accessed when a read/write is performed using port address 3#5.

CRTC Indexed Registers

The following registers are CRTC indexed registers. These registers are accessed by first writing the index of the desired register to the CRTC Index register and then accessing the register using the address 3#5.

CRTC Indexed Register 0: Horizontal Total

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Total character times per horizontal scan line (-5 VGA, -2 for EGA mode).

The Horizontal Total register defines the horizontal scan line time by controlling the length of the scan line in character times units.

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CRTC Indexed Register 1: Horizontal Display End

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Character count of horizontal display enable end -1

The Horizontal Display End register contains the 8-bit value of the internal horizontal character counter after which the horizontal display enable period is to end. The total number of characters displayed per horizontal scan line is one greater than the contents of the Horizontal Display End register.

CRTC Indexed Register 2: Horizontal Blank Start

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Character count of horizontal blanking start.

The Horizontal Blank Start register contains the 8-bit value of the internal horizontal character counter at which horizontal blanking is to start.

CRTC Indexed Register 3: Horizontal Blank End

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-4	Character count of horizontal blanking end modulo 32 (EGA); 5 least significant bits of character count of horizontal blanking end modulo 64 (VGA mode).
5-6	Display enable skew.
7	Test bit.

Bits 0-4 EGA mode: Provides the 5-bit value of the internal horizontal character counter at which horizontal blanking is to end. Since the character counter is an 8-bit counter and the Horizontal Blank End is a 5-bit register, the upper 3 bits of the character counter are ignored in making this comparison. This means that the horizontal blanking end position is defined relative to the horizontal blanking start position; the first time after the start of horizontal blanking that the Horizontal Blank End register matches the lower 5 bits of the character counter, horizontal blanking will end.

VGA mode: The Horizontal Blank End register value is increased to six bits; the five bits will provide the least significant five bits of this value, while the most significant bit is found in CRTC register 5 (Horizontal Sync End register) bit 7.

Bits 6 and 5 of the Horizontal Blank End register form a 2-bit integer that defines the skew of the horizontal display enable in character clocks as follows:

Bit 6	Bit 5	Skew
0	0	0 character clocks.
0	1	1 character clock.
1	0	2 character clocks.
1	1	3 character clocks.

Bit 7, 1 = normal mode of operation.

CRTC Indexed Register 4: Horizontal Sync Start

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Character count of horizontal sync start.

The Horizontal Sync Start register contains the 8-bit value of the internal horizontal character counter at which horizontal sync (the horizontal retrace pulse) is to start.

CRTC Indexed Register 5: Horizontal Sync End

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-4	Character count of horizontal sync end modulo 32.
5-6	Horizontal sync skew.
7	Bit 5 of Horizontal Blank End for VGA modes.

Bits 0-4 of the Horizontal Sync End register contain the 5-bit value of the internal horizontal character counter at which horizontal sync is to end. Since the character counter is an 8-bit counter and horizontal sync end is a 5-bit value, the upper three bits of the character counter are ignored in making this comparison. This means that the horizontal sync end position is defined relative to the horizontal sync start position; the first time after the start of horizontal sync that the Horizontal Sync End register matches the lower 5 bits of the character counter, horizontal sync will end.

Bits 6 and 5 of the Horizontal Sync End register form a 2-bit integer that defines the skew of the horizontal sync signal in character clocks as follows:

Bit 6	Bit 5	Skew
0	0	0 character clocks.
0	1	1 character clock.
1	0	2 character clocks.
1	1	3 character clocks.

Bit 7 provides bit 5 of the Horizontal Blank End value for VGA modes.

CRTC Indexed Register 6: Vertical Total

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	VGA mode: Horizontal scan lines per vertical frame -2 (bits 0-7). EGA Mode: Horizontal scan lines per vertical frame -1 (bits 0-7).

The Vertical Total register contains the lower eight bits of the 11-bit vertical total value, which defines the number of horizontal scan lines per vertical frame.

Note that bits 8 and 9 of the vertical total value are in the Overflow Low register, and bit 10 is in the Overflow High register.

CRTC Indexed Register 7: Overflow Low

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0	Vertical Total (bit 8).
1	Vertical Display Enable End (bit 8).
2	Vertical Sync Start (bit 8).
3	Vertical Blank Start (bit 8).
4	Line Compare (Split Screen) (bit 8).
5	Vertical Total (bit 9).
6	Vertical Display Enable End (bit 9).
7	Vertical Sync Start (bit 9).

The Overflow register contains one extra bit for each of five values that cannot fit in a single byte. Bits 8 and 9 of the Vertical Total, Vertical Display Enable End, and Vertical Sync Start are contained in the Overflow register, as is bit 8 for Vertical Blank Start and Line Compare.

CRTC Indexed Register 8: Preset Row Scan/Initial Row Address

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-4	Initial row address after vertical sync.
5-6	Byte Panning.
7	Reserved.

Bits 0-4 of the Initial Row Address register define the row address of the first scan line following vertical sync.

In 6845 compatibility mode, this register address is CRTC Indexed Register 35.

Bits 5 and 6 control horizontal byte panning in modes programmed as multiple shift modes.

To access this register in 6845 compatibility mode, use CRTC Indexed Register 35 for the register address (instead of CRTC Indexed Register 8).

CRTC Indexed Register 9: Maximum Row Address

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-4	Number of scan lines per character row -1.
5	Vertical Blank Start bit 9.
6	Line Compare (Split Screen) bit 9.
7	Double Scan Enable: 200-to-400 scan line conversion.

Bits 0-4 of the Maximum Row Address register define the height in scan lines of each character row. It is used to select the desired scan line from the font character being displayed.

Bit 5 is bit 9 of the Vertical Blank register.

Bit 6 is bit 9 of the Line Compare (Split Screen) register.

Bit 7 is used to set scan lines to 400 from 200 when set to a one (1). This divides the clock in the row scan counter by 2, effectively doubling the lines displayed by displaying every line twice. A zero (0) returns the row scan counter clock equal to the horizontal scan rate.

CRTC Indexed Register A: Cursor Start Row Address

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-4	The row address at which the cursor starts being enabled.
5	Used to turn the cursor off (=1) or on (=0).
6-7	Reserved.

Bits 0-4 of the Cursor Start Row Address register contain the value of the internal row address counter at which the cursor is to begin to be enabled.

CRTC Indexed Register B: Cursor End Row Address

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-4	The row address at which the cursor stops being enabled.
5-6	Cursor skew.
7	Reserved.

Bits 0-4 of the Cursor End Row Address register contain the row address at which the cursor is to stop being enabled. That is,

Cursor End Row Address register =
last cursor row address displayed + 1

Bits 6 and 5 of the Cursor End Row Address register form a 2-bit integer that defines the skew of the cursor signal in character clocks as follows:

Bit 6	Bit 5	Skew
0	0	0 character clocks.
0	1	1 character clock.
1	0	2 character clocks.
1	1	3 character clocks.

In general, the cursor location must maintain a relationship with the display enable signal such that a cursor positioned at both the extreme left and extreme right of the screen will always appear.

CRTC Indexed Register C: Linear Starting Address Middle

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Linear starting address (bits 8-15).

The Linear Starting Address Middle register contains bits 8-15 of the 18-bit linear starting address. The linear starting address is the display memory address at which the regen buffer (the area of memory scanned by the linear counter for video data) begins; the linear counter is set to this value at the start of the vertical frame. The linear starting address can be incremented or decremented to perform horizontal character panning; the ATC's horizontal pixel panning feature can be used for finer horizontal panning. In graphics modes, the linear starting address can be incremented or decremented by the value of the Row Offset register to perform smooth (scan line) vertical scrolling. In text modes, the linear starting address can be used to perform character vertical scrolling; in this case, the Initial Row Address register can be used to adjust, on a scan line basis, to smooth-scroll the text.

Note that bit 16-17 of the linear starting address are in the Extended Start Address register and bits 0-7 are in the Linear Starting Address Low register.

CRTC Indexed Register D: Linear Starting Address Low

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Linear starting address (bits 0-7).

The Linear Starting Address Low register contains bits 0-7 of the 18-bit linear starting address. See the Linear Starting Address Middle register for details on the linear starting address.

CRTC Indexed Register E: Cursor Address Middle

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Cursor start address (bits 8-15).

The Cursor Address Middle register contains bits 8-15 of the 18-bit cursor address. The cursor address is the display memory address at which the cursor is located in text mode.

Note that bits 0-7 of the cursor address are in the Cursor Address Low register, and bit 16-17 are in the Extended Start Address register.

CRTC Indexed Register F: Cursor Address Low

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Cursor start address (bits 0-7).

The Cursor Address Low register contains bits 0-7 of the 18-bit cursor address. See the Cursor Address Middle register for details on the cursor address.

CRTC Indexed Register 10: Vertical Sync Start

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Scan line at which vertical sync starts (bits 0-7).

The Vertical Sync Start register contains the lower eight bits of the 11-bit vertical sync start value. The vertical sync start value specifies the value of the internal line counter at which vertical sync (the vertical retrace pulse) is to start.

Note that bits 8 and 9 of the vertical sync start value are in the Overflow Low register, and bit 10 is in the Overflow High register.

CRTC Indexed Register 11: Vertical Sync End

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-3	Scan line at which vertical sync ends modulo 16.
4	Clear vertical interrupt when low.
5	Enable vertical interrupt when low.
6	Reserved.
7	Protection bit.

Bits 0-3 of the Vertical Sync End register contain the 4-bit value of the internal line counter at which the vertical sync signal is to end. Since the line counter is an 11-bit counter and vertical sync end is a 4-bit value, the upper 7 bits of the line counter are ignored in making this comparison. This means that the vertical sync end position is defined relative to the vertical sync start position; the first time after the start of vertical sync that the Vertical Sync End register matches the lower 4 bits of the line counter, vertical sync will end.

Bit 4 is set to 0 to clear the vertical interrupt. If bit 5 is low and the vertical interrupt is cleared, then output in "INTL" will be asserted when output line "VS" becomes true. The vertical interrupt should be cleared whenever a vertical interrupt occurs, before re-enabling interrupts.

Bit 5 of the Vertical Sync End register is set to 0 to enable the vertical interrupt to occur. If bit 5 is set to 1, vertical interrupts cannot occur. If bit 5 is set to 0 and the vertical interrupt is cleared, then "INTL" will be asserted when "VS" becomes true.

Bit 7, when set to 1, prevents CRTC registers 0-7 and 35, from being written to, with the exception of bit 4 of the Overflow register (CRTC Register 7), and bits 4,7 of CRTC Indexed Register 35.

CRTC Indexed Register 12: Vertical Display End

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Number of last scan line displayed vertically (bits 0-7).

The Vertical Display End register contains the lower eight bits of the 11-bit vertical display end value.

Note that bits 8 and 9 of the vertical display end value are in the Overflow Low register, while bit 10 is in the Overflow High register.

CRTC Indexed Register 13: Row Offset

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Word memory address offset between the start of one displayed row and the next.

The Row Offset register specifies the amount to be added to the internal linear counter when advancing from one screen row to the next. This addition is performed whenever the internal row address counter advances past the maximum row address value, indicating that all the scan lines in the present row have been displayed. The Row Offset register is programmed in terms of CPU-addressed words per scan line, counted as either words or doublewords, depending on whether byte or word mode is in effect. If the CRTC Mode register is set to select byte mode, the Row Offset register is programmed with a word value, so for a 640-pixel (80-byte) wide graphics display, a value of 80/2 = 40 (28 hex) would normally be programmed, where 80 is the number of bytes per scan line. If the CRTC Mode register is set to select word mode, then the Row Offset register is programmed with a doubleword, rather than a word, value. For instance, in 80-column text mode, a value of 160/4 = 40 (28 hex) would be programmed, because from the CPU-addressing side, each character requires 2 linear bytes (character code byte and attribute byte), for a total of 160 (A0 hex) bytes per row.

In effect, the Row Offset register defines a virtual screen width, so that the physical screen area could be considered a window onto a virtual screen that has a width defined by the Row Offset register. The horizontal pixel panning feature of the ATC can be used with the linear start address to move horizontally around a virtual screen larger than the actual screen size, and the linear start address and the Initial Row Address register can be used to move vertically.

CRTC Indexed Register 14: Underline Row Address

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-4	Row address at which underline signal is to be asserted.
5	Linear address count by 4.
6	Doubleword addressing.
7	Reserved (=0).

Bits 0-4 of the Underline Row Address register contain the value of the row address counter at which the underline is to be enabled. The ATC enables underline attribute decoding and displays the underline whenever the underline attribute is true during that scan line. The underline may be disabled by setting the Underline Row Address register to a value greater than the setting of the Maximum Row Address register. The value set is equal to the scan line number requested minus one.

Bit 5, when set to 1, clocks the memory address counter with the character clock divided by 4, used when doubleword addressing is used. Note when Bit 3 of the CRTC Mode Register is also = 1, then the linear counter will increment twice per character.

Bit 6, when set to 1, indicates that memory addresses being used are doubleword addresses.

CRTC Indexed Register 15: Vertical Blank Start

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Scan line at which vertical blanking begins -1 (bits 0-7).

The Vertical Blank Start register contains bits 0-7 of the 11-bit Vertical Blank Start value. The Vertical Blank Start specifies the value of the internal line counter at which vertical blanking is to start -1.

Note that bit 8 of the Vertical Blank Start value is in the Overflow Low register, and bit 9 of the Vertical Blank Start value is in the Maximum Row Address register, while bit 10 is in the Overflow High register.

CRTC Indexed Register 16: Vertical Blank End

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Scan line at which vertical blanking ends.

Bits 0-7 of the Vertical Blank End register contain the 8-bit value of the internal line counter at which vertical blanking is to end. Since the line counter is an 11-bit counter and the Vertical Blank End is a 8-bit register, the upper three bits of the line counter are ignored in making this comparison. This means that the vertical blanking end position is defined relative to the Vertical Blanking Start position; the first time after the start of vertical blanking that the Vertical Blank End register matches the lower 8 bits (In EGA mode only bits 0-4 are used in the comparison) of the line counter, vertical blanking will end.

CRTC Indexed Register 17: CRTC Mode

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0	Alternate address line LA13 output.
1	Alternate address line LA14 output.
2	Line counter count by 2.
3	Linear counters count by 2.
4	Memory address output control.
5	Alternate address line +MA00 output.
6	Word/byte mode select.
7	Hold control.

Bit 0 of the CRTC Mode register provides an alternate value for LA13 output during the display enable period; that is, the display memory address line, LA13, is multiplexed. When this bit is set to 0, the LA13 output line is equal to row address bit 0, so each odd scan line is addressed 8KB after the corresponding even scan line. This is used to emulate the 6845 CRT Controller used in the IBM Color/Graphics Adapter. When bit 0 is set to 1, linear counter bit 13 or bit 12, in byte or word mode, respectively, is multiplexed to LA13.

Bit 1 of the CRTC Mode register provides an alternate value for LA14 output during the display enable period; that is, the display memory address line LA14 is multiplexed. When this bit is set to 0, the LA14 output line is equal to row address bit 1, so that out of each group of four scan lines, scan lines 2 and 3 are addressed 16KB after the corresponding even scan lines 0 and 1.

When bit 1 is set to 1, linear counter bit 14 or bit 13, in byte or word mode, respectively, is multiplexed to LA14.

Bit 2 of the CRTC Mode register is set to 1 to cause the line counter to increment on every other scan line, rather than incrementing on every scan line. This has the effect of doubling all vertical timings without affecting any horizontal timings. When set to 0, the line counter increments with every scan line.

Bit 3 of the CRTC Mode register is set to 1 to cause the linear counter to increment on every other character clock, rather than incrementing on every character clock. When set to 0, the linear counter is incremented on every character clock. This is typically associated with situations where DOTCLK is not divided by two but VLOAD is divided by two and word mode addressing is selected; the linear counting is divided by two to synchronize the linear counters with the ATC video data rate. If VLOAD and DOTCLK are both divided by two, then bit 3 should not be set to 1. NOTE: When this bit = 1 and Bit 5 of the Underline Row Address Register also = 1, then the linear counter will increment twice per character.

Bit 4 of the CRTC Mode register is set to 1 to cause the LA(17:00) lines to become tri-state.

Bit 5 of the CRTC Mode register provides an alternate value for LA00 output during the display enable period; that is, the display memory address line LA00 is multiplexed. In word mode, when this bit is set to 0, the LA00 output line is equal to linear counter bit 13. When this bit is set to 1, the LA00 output line is equal to linear counter bit 15. In byte mode, bit 5 has no effect, and linear counter bit 0 is always multiplexed to LA00. Word mode is typically used in text mode.

The reason for selecting this alternate value for LA00 is so that the CRTC display memory mapping matches the CPU display memory mapping. In text mode, even/odd mode (see the TS Memory Mode register) is active to allow CPU memory addressing to match the CRTC organization of display memory. In even/odd mode, the CPU A⟨0⟩ line is used to select between plane 0 and plane 1, with planes 2 and 3 storing the soft character font.

The CRTC matches this by shifting the linear address counter up one bit before placing it on the LA(17:00) lines (refer to the discussion of bit 6, word/byte mode select, below), and then the full 16 bits of the character code and attribute for a given character are accessed in parallel to generate the character. Consequently, the linear counter provides no direct value for the LA00 line. The highest useful linear address counter value should be wrapped to LA00, to provide the maximum addressable memory in text modes. When 16KB per plane is installed, bit 5 should be set to 0 to wrap linear address bit 13 to LA00, providing the CRTC with 16KB

CRTC Indexed Register 17: CRTC Mode (continued)

addressing. When more than 16KB of memory per plane is installed, bit 5 should be set to 1 to wrap linear address bit 15 to LA00, providing the CRTC with 64KB of addressing.

Externally, the CPU address line A⟨14⟩ or A⟨16⟩ or a page select bit, should correspond to the LA00 line in even/odd mode. In non-even/odd mode, the CPU address line A⟨0⟩ should correspond to the LA00 line.

Bit 6 of the CRTC Mode register is set to 0 to select word mode, and set to 1 to select byte mode.

Bit 7 of the CRTC Mode register is set to 0 to place all horizontal and vertical timing control circuitry into a hold state.

The following table describes the external memory address mapping relationship between the CRTC address and CPU address lines.

Table 4.3-4 CPU/CRTC Addressing Modes

S1 = PG, S0 = OE, S2 = LG SF = text font

CPU					CRTC				
MD	PG	OE0	OE1	LG1	S1	S0*	S0	S2	SF
A0	RW0	A0	A0	A0	00	00	00	00	#
A1	RW1	RW1	RW1	A1	00	00	00	00	#
A2	A0	PGS	A1	A2	L0	L15	L0	L0	RA⟨0⟩
A3	A1	A1	A2	A3	L1	L0	L1	L1	RA⟨1⟩
A4	A2	A2	A3	A4	L2	L1	L2	L2	RA⟨2⟩
A5	A3	A3	A4	A5	L3	L2	L3	L3	RA⟨3⟩
A6	A4	A4	A5	A6	L4	L3	L4	L4	RA⟨4⟩
A7	A5	A5	A6	A7	L5	L4	L5	L5	CC⟨0⟩
A8	A6	A6	A7	A8	L6	L5	L6	L6	CC⟨1⟩
A9	A7	A7	A8	A9	L7	L6	L7	L7	CC⟨2⟩
A10	A8	A8	A9	A10	L8	L7	L8	L8	CC⟨3⟩
A11	A9	A9	A10	A11	L9	L8	L9	L9	CC⟨4⟩
A12	A10	A10	A11	A12	L10	L9	L10	L10	CC⟨5⟩
A13	A11	A11	A12	A13	L11	L10	L11	L11	CC⟨6⟩
A14	A12	A12	A13	A14	L12	L11	L12	L12	CC⟨7⟩
A15	A13	A13	A14	A15	L13	L12	L13	L13	FS⟨2⟩
A16	A14	A14	A15	PL0	L14	L13	L14	L14	FS⟨0⟩
A17	A15	A15	PL0	PL1	L15	L14	L15	L15	FS⟨1⟩
A18	PLX	PL0	PL1	PL2	L16	L15	L16	L16	-
A19	PLY	PL1	PL2	PL3	L17	L16	L17	L17	-

NOTES:

1. A⟨15:0⟩ = CPU ADDRESS BIT 15 TO 0
2. MD⟨15:0⟩ = ET4000 MEMORY ADDRESS BUS 15 TO 0
3. PL⟨3:0⟩ = 4-BIT READ SEGMENT POINTER (GDC SEGMENT SELECT REGISTER ⟨7:4⟩ ON (READ))
   = 4-BIT WRITE SEGMENT POINTER (GDC SELECT REGISTER ⟨3:0⟩) ON WRITE
   PLX = PL0 or A16
   PLY = PL1 or A17
4. L⟨17:0⟩ = LINEAR COUNTER BIT 17 to 0
   RA ⟨4:0⟩ = CHARACTER ROW SCAN 4 to 0
   CC ⟨7:0⟩ = CHARACTER CODE BIT 7 to 0
   FS ⟨2:0⟩ = CHARACTER FONT SELECT 2 to 0
5. * Selected when SKP⟨0⟩ (IBME*/SBW⟨0⟩) = 1 selection between S0 and S0* via CRTC index 36 bit 5 (IBME) bit
6. # In text mode, I/R planes are font planes and G/B planes are attribute/character code planes
7. RW⟨1:0⟩ = read plane select (RPS⟨1:0⟩) and write map mask (MM⟨3:0⟩)
8. PGS = /PSEL*CHAN*(CDS⟨1⟩|CDS⟨0⟩)
   A⟨16⟩*CHAN*/(CDS⟨1⟩|CDS⟨0⟩)
   A⟨0⟩*/CHAN

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CRTC Indexed Register 18: Line Compare (Split Screen)
This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-7	Line Compare (bits 0-7).

The Line Compare register contains bits 0-7 of the compare target. The line compare target value specifies the value of the internal line counter at which the internal linear counter is to be reset to 0. This means that at the scan line after the scan line specified by the line compare target value the display will reflect the contents of display memory starting at address 0. This split screen section will continue to the bottom of the screen, and will remain unchanged even if the linear starting address is changed.

Note that bit 8 of the line compare value is contained in the Overflow Low register, bit 9 is in the Maximum Row Address register, while bit 10 is in the Overflow High register.

The following CRTC registers are TLI's extended registers. To write to these register(s) (except indices 33 and 35), the "KEY" must be set. (CRTC Indexed Register 35 is protected by bit 7 of CRTC 11.) See Input Status Register Zero for definition of "KEY".

CRTC Indexed Register 32: RAS/CAS Configuration (RCCONF; protected by key)
This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-1	CSW⟨1:0⟩ ($1+1)*SCLK, CAS low pulse-width.
2	CSP⟨0⟩ ($1+1)*SCLK, CAS pre-charge time.
3-4	RSP⟨1:0⟩ ($1+2)*SCLK, RAS pre-charge time.
5	RCD RAS to CAS time, 1=3 clock, 0=2 clock.
6	RAL RAS & CAS column setup time.
7	Static column memory.

Bits 0-1, CSW⟨1:0⟩, plus 1 ($1 + 1), form the programmed value for low pulse width control (Tcas). The actual pulse width is equal to the programmed value plus 1 of the SCLK clock period.

Bit 2, CSP⟨0⟩, plus 1 ($1+1), is the 1-bit programmed value for CAS⟨3:0⟩ pre-charge control (Tcsp). The actual pulse width high is equal to the programmed value plus 1 of SCLK clock period.

Bits 3-4, RSP⟨1:0⟩, plus 2, form a programmed value for RASB, RASA pre-charge control (Trsp). The actual pulse width high is equal to the programmed value plus 2 of SCLK clock period.

Bit 5, when set to 1, causes the Trcd time to be equal to 3 SCLK clock periods. When set to 0, the Trcd time is reduced to 2 SCLK periods.

Bit 6 provides 1-bit column address hold time control (Tral). When set to 1, an additional SCLK clock period will be added to the RAS low pulse width and to the last CAS low pulse width of each RAS cycle. This will effectively increase the column address hold time by one additional SCLK clock period. Note that the RAS pre-charge time will be reduced by one SCLK clock period.

Bit 7, when set to 1, causes the CAS⟨3:0⟩ outputs to remain active during the entire memory read operation. When set to 0, the CAS⟨3:0⟩ will be toggled during a fast page memory read operation.

NOTE: 1. The RAS low pulse width is equal to Trcd + n(Tcsw) + (n-1)Tcsp + Tral, where n is number of CAS cycles.

2. The RAS high pulse width is equal to Trsp—Tral

4.0

CRTC Indexed Register 33: Extended Start Address

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-1	Linear start address bits 16 & 17.
2-3	Cursor address bit 16 & 17.

Bits 0-1 are bits 16 and 17 of the 18-bit Linear Starting Address value.

Bits 2-3 are bits 16 and 17 of the 18-bit Cursor Address value.

CRTC Indexed Register 34: 6845 Compatibility Control Register (protected by key)
This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0	EMCK 1=enable translation of CS0 bit.
1	CS2 MCLK clock select 2 (select up to 8 clocks).
2	TRIS 1=tri-state the ET4000's output tri-state pins.
3	ENVS VSE register port address (1=46E8, 0=3C3).
4	ENXR 1=enable translation ROM when reading CRTC/MISCOUT.
5	ENXL 1=enable translation ROM when writing CRTC/MISCOUT.
6	ENBA 1=enable double scan/underline in AT&T compatible mode.
7	6845 1=enable 6845 compatibility.

Bit 0, when set to 1, is used to enable the ET4000 to translate the clock select bits (CS1,CS0). (See Miscellaneous Output Register.) Also, during ENXL set to 1, EMCK is used to select the external translation ROM's map while in 6845 mode (see Miscellaneous Output Register).

Bit 1, clock select 2 (CS2), in conjunction with the MISCOUT⟨3:2⟩ clock select lines (CS1, CS0), provides up to eight video clocks to be selected.

Bits CRTC I(34) 1	(MISCOUT) 3 2	
0	0 0	-Selects MCLK clock 1.
0	0 1	-Selects MCLK clock 2.
0	1 0	-Selects MCLK clock 3.
0	1 1	-Selects MCLK clock 4.
1	0 0	-Selects MCLK clock 5.
1	0 1	-Selects MCLK clock 6.
1	1 0	-Selects MCLK clock 7.
1	1 1	-Selects MCLK clock 8.

Bit 2, when set to 1 (Output tri-state control), causes all output pins to go to a tri-state condition. The symbols are as follows; see section 2.3.1 for pin numbers.

RASB, RASA, CAS⟨3:0⟩, MWB, MWA, SCC, DTEB, DTEA,
MD⟨31:0⟩, AB⟨9:0⟩, AA⟨9:0⟩, VS, HS, SI, SR, SG, SB,
PI, PR, PG, PB, PCLK, MBS

Bit 3, when set to 1, will set the Video Subsystem Enable register port address to 46E8; 0 = 3C3.

Bits 5,4 (bit 5 for write, bit 4 for read) when set to 1, disable the RDMEL output when an I/O read/write to the CRTC Data register 3#5 or MISCOUT register is performed. This allows the external translation ROM to be enabled for the CRTC register. To use the translation, external ROM must be incorporated. When set to 0, the Translation Mode is disabled.

Bit 6, when set to 1, enables the double scan and underline color attributes. (see AT&T Mode Control Register.)

Bit 7, when set to 1, enables 6845 compatibility. Several steps need to be taken in order to program for 6845 compatibility. The ET4000 internal registers should be programmed as follows in order to fully emulate the IBM CGA/MDA or Hercules modes:

A. Load the font and set the external palette appropriately for the mode to be selected
   1. color: set 200-scan line mode 3 first to load font, set external palette.
   2. mono: set 350-scan line mode 7 first to load font, set external palette.
B. Set the appropriate EGA/VGA table for the correct mode (See Table 4.3-5).*
C. Set bit 7 of the CRTC Indexed Register 34 for CGA/MDA/Hercules compatibility.**
D. Set the appropriate Display Mode Control register (3#8).
E. Program the 6845 CRTC registers (3#4, 3#5) for the compatibility mode to be selected (CGA/MDA/Hercules). (In color mode, also set the color register (3D9).)

* Note that the values programmed into the Miscellaneous Output Register and TS Indexed Register 7 (relating to the clock and sync polarities) can vary depending on the adapter's clock configuration, whether or not translation is enabled, and the target monitor. The ROM configuration also affects TS Indexed Register 7.

** Other bits in CRTC Indexed Register 34, in addition to bit 0 of the AT&T Mode Control Register ((3DE) for double scan) may also need to be set depending on the target monitor and whether or not translation is enabled.

A driver is needed to select for EGA/VGA modes, and, to in turn, select for 6845 monochrome, or 6845 color compatibility.

Table 4.3-5 ET4000 6845 Color Emulation Setup Register Values

Register Name	Port	Index	Mode of Operation	
			CGA	MDA
Misc. Output	3C2	-	37	AA

Timing Sequencer

Register Name	Port	Index	Mode of Operation	
			CGA	MDA
TS Index	3C4	-		
Synch Reset	3C5	00	03	03
TS Mode	3C5	01	00	00
Wrte Plane Msk	3C5	02	03	03
Font Select	3C5	03	00	00
Memory Mode	3C5	04	02	02
Reserved	3C5	05		
State Control	3C5	06	00	00
TS Aux Mode	3C5	07	48	48

CRT Controller Registers

Register Name	Port	Index	Mode of Operation	
			CGA	MDA
CRTC Index	3D4	-		
Horiz Tot	3D5	00	50	50
Hor Dis End	3D5	01	00	00
Hor Blnk Strt	3D5	02	00	00
Hor Blnk End	3D5	03	20	20
Hor Sync Strt	3D5	04	00	00
Hor Sync End	3D5	05	60	20
Vert Tot	3D5	06	F0	F0
Overflow Low	3D5	07	10	10
Init Row Addr	3D5	08	00	00
Max Row Addr	3D5	09	00	00
Cursor Strt	3D5	0A	00	00
Cursor End	3D5	0B	00	00
Lin Strt Mid	3D5	0C	00	00
Lin Strt Low	3D5	0D	00	00
Cursor Mid	3D5	0E	00	00
Cursor Low	3D5	0F	00	00
Vrt Sync Strt	3D5	10	00	00
Vrt Sync End	3D5	11	20	20
Vrt Dis End	3D5	12	00	00
Row Offset	3D5	13	00	00
Underline Row	3D5	14	1F	0D
Vrt Blnk Strt	3D5	15	00	00
Vrt Blnk End	3D5	16	00	00
CRTC Mode	3D5	17	A0	A0
Line Compare	3D5	18	FF	FF
Ext'd Strt Add	3D5	33	00	00
Overflow Hi	3D5	35	00	00

GDC Registers

Register Name	Port	Index	Mode of Operation CGA	MDA
GDC Index	3CE			
Set/Reset	3CF	00	00	00
Enabl Set/Res	3CF	01	00	00
Colr Compare	3CF	02	00	00
Data Rotate	3CF	03	00	00
Read Plane Sel	3CF	04	00	00
GDC Mode	3CF	05	10	10
Miscellaneous	3CF	06	0E	0A
Color Care	3CF	07	00	00
Bit Mask	3CF	08	FF	FF

ATC Indexed Registers

Register Name	Port	Index	Mode of Operation CGA	MDA
ATC Index	R/W 3C0			
Palette	R:3C1/W:3C0	00	00	00
Palette	R:3C1/W:3C0	01	01	08
Palette	R:3C1/W:3C0	02	02	08
Palette	R:3C1/W:3C0	03	03	08
Palette	R:3C1/W:3C0	04	04	08
Palette	R:3C1/W:3C0	05	05	08
Palette	R:3C1/W:3C0	06	06	08
Palette	R:3C1/W:3C0	07	07	08
Palette	R:3C1/W:3C0	08	10	10
Palette	R:3C1/W:3C0	09	11	18
Palette	R:3C1/W:3C0	0A	12	18
Palette	R:3C1/W:3C0	0B	13	18
Palette	R:3C1/W:3C0	0C	14	18
Palette	R:3C1/W:3C0	0D	15	18
Palette	R:3C1/W:3C0	0E	16	18
Palette	R:3C1/W:3C0	0F	17	18
Mode Ctrl	R:3C1/W:3C0	10	00	00
Overscan Clr	R:3C1/W:3C0	11	00	00
Clr Plane En	R:3C1/W:3C0	12	00	00
Hor Pix Pan	R:3C1/W:3C0	13	00	08
Color Select	R:3C1/W:3C0	14	00	00
Miscellaneous	R:3C1/W:3C0	16	00	00

CRTC Indexed Register 35: Overflow High

This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0	Vertical Blank Start Bit 10.
1	Vertical Total Bit 10.
2	Vertical Display End Bit 10.
3	Vertical Sync Start Bit 10.
4	Line Compare (Split Screen) Bit 10.
5	External sync reset (gen-lock) the line/chr counter (1=enable).
6	Alternate RMW control.
7	Vertical interlace mode (1=enable).

Bits 0-4 are bit 10 of the Vertical Blank Start, Vertical Total, Vertical Display End, Vertical Sync Start, and Line Compare (Split Screen Start) values, respectively.

Bit 5, when set to 1, will enable the SYNR input to reset the ET4000's internal line and character counter asynchronously. Also, the TKN⟨1:0⟩ outputs are redefined as TKN⟨1⟩= interlace mode active, TKN⟨0⟩=EVEN field. For additional details see the I/O pin description.

Bit 6, when set to 1, will enable ET4000 to perform a Read-Modify-Write operation after a read. This bit should be set to 0 normally.

Bit 7, when set to 1, will enable the vertical interlace mode where the odd-numbered lines will be displayed, followed by the even-numbered lines, thus doubling the effective vertical resolution with the same vertical timing.

Note: CRTC bit 7 must equal 0 to write to all bits here except bits 4,7.

CRTC Indexed Register 36: Video System Configuration 1

(VSCONF1); protected by key.
This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-2	Refresh count per line -1.
3	Font width control (1=up to 16-bit, 0=8-bit font).
4	Segment/linear system configuration (0=segment, 1=linear system).
5	Addressing mode (0=IBM; 1=TLI).
6	16-bit display memory read/write (1=enable).
7	16-bit I/O read/write (1=enable).

Bits 0-2 form a 3-bit value equal to the refresh counter minus one.

Bit 3, when set to 1, will enable the text font width to be greater than 8 pixels wide. Note that, the VGA's 9-pixel font width, with the line-graph enable on, does not require this bit to be set. When set to 0, enables the VGA-compatible font width.

Bit 4, when set to 1, will define the most significant 4-bits of display memory address lines as directly from the microprocessor address bus (linear system). Note also that GDC Indexed Register 6, bits 3 & 2 must be set for 128K bytes (0,0).

Since the linear system responds to a contiguous 1MB address space, the host addresses (A⟨23:20⟩) should be used to avoid address conflicts with the host.

When set to 0, defines these address lines as derived from the Segment Select Register (port 3CD).

Bit 5, when set to 1, will enable the address mapping of the display memory to be contiguous. This enables much more efficient use of the ET4000's internal resources and thereby, improves the performance. When set to 0, will enable address mapping compatible with the VGA's. Note that use of this bit will not affect the compatibility with all video modes unless the software assumes the relationship of the address mapping between modes.

Bit 6, when set to 1, will enable the 16-bit CPU memory read/write data bus interface at the DB⟨15:0⟩ input. This bit is power-up default set to 1.

Bit 7, when set to 1, will enable the 16-bit CPU I/O read/write data bus interface at the DB⟨15:0⟩ input. This bit is power-up default set to 0.

CRTC Indexed Register 37: Video System Configuration 2

(VSCONF2); protected by key.
This is a read/write register.
R/W : Port address = 3#5

Bit	Description
0-1	Display Memory data bus width.
2-3	Display Memory data depth.
4	16-bit ROM enable.
5	Priority threshold control (0=more memory BW).
6	Test: 1=TLI internal test mode.
7	DRAM display memory type (1=VRAM, 0=DRAM).

Bits 0-1 determine the width (from 8-bit to 32-bit) of the DM⟨31:0⟩ bi-directional display memory data bus:

In DRAM mode:

Bit 0 1	DM⟨31:24⟩	DM⟨23:16⟩	DM⟨15:8⟩	DM⟨7:0⟩	Bus Width
1 1	DM⟨31:24⟩	DM⟨23:16⟩	DM⟨15:8⟩	DM⟨7:0⟩	32
0 1	—	DM⟨15:8⟩	—	DM⟨7:0⟩	16
1 0	—	DM⟨7:4⟩	—	DM⟨3:0⟩	8
0 0	Reserved				

In VRAM mode:

Bit 0 1	DM⟨31:24⟩	DM⟨23:16⟩	DM⟨15:8⟩	DM⟨7:0⟩	Bus Width
1 1	Reserved				
0 1	SM⟨15:8⟩	SM⟨7:0⟩	DM⟨15:8⟩	DM⟨7:0⟩	16
1 0	—	SM⟨7:0⟩	—	DM⟨7:0⟩	8
0 0	Reserved				

Bit 2 determines the ET4000's internal MD⟨31:0⟩ bus read data latch. When set to 1, latches MD⟨31:0⟩ bus at the end of each CAS read cycle; when set to 0, causes one clock delay after each CAS read cycle.

Bit 3 determines the depth of display memory used:

Bit 3	Memory
1	256K x 4
0	64K x 4

Bit 4, when set to 1, enables the 16-bit ROM configuration.

Bit 5, when set to 0, will increase the utilization of the display memory's bandwidth. However, the memory's response time will also be increased. This bit should normally be set to 0 for better performance.

NOTE: Bits 3 & 5 of TS Indexed Register 7: TS Auxiliary Mode must be set to 1,1 so that the ROM size is set to 32K.

Bit 6, when set to 1, directs the ET4000 to internal test mode set-up. This bit must set to 0 at all other times for normal operation.

Bit 7, when set to 1, will define ET4000's display memory I/O interface to Video Memory (VRAM). When set to 0, defines the interface to DRAM. This bit must be set at power-up time and is default set to DRAM.

4.4 ET4000 TS Register Description

The CPU interface to the ET4000 internal Timing Sequencer (TS) consists of eight read/write registers. Of these registers, one register, the TS Index Register, is accessed by a separate independent I/O address (3C4). The remaining seven registers are internally indexed, which means that they are accessed via a common I/O address (3C5), with one of the seven registers that is actually selected by the TS Index register.

Table 4.4-1 TS Index Register

Register Name		Port Address
TS Index Register	(Read/Write)	3C4

Table 4.4-2 TS Indexed Registers

TS Indexed Register Name	TS	Indexed Address	Port Address
Synchronous Reset	0	(Read/Write)	3C5
TS Mode	1	(Read/Write)	3C5
Write Plane Mask	2	(Read/Write)	3C5
Font Select	3	(Read/Write)	3C5
Memory Mode	4	(Read/Write)	3C5
Reserved	5		
TS State Control	6	(Read/Write)	3C5
TS Auxiliary Mode	7	(Read/Write)	3C5

4.0

TS Index

This is a read/write register.
R/W : Port address = 3C4

Bit	Description
0-2	Current TS index.
3-7	Reserved.

Bits 0-2 provide the index of the currently selected internally indexed register. The TS Index register determines which TS indexed register will be accessed when a read/write is performed using port address 3C5.

TS Indexed Registers

The following registers are TS indexed registers. These r
writing the index of the desired register to the TS Index
the register using address 3C5.

TS Indexed Register 0: Synchronous Reset

This is a read/write register.
R/W : Port address = 3C5

Bit	Description
0	Asynchronous reset control.
1	Synchronous reset control.
2-7	Reserved.

Bit 0, when set to 0, commands the timing sequencer to asynchronously clear and halt. When set to 1 the sequencer will run unless bit 1 is set to 0.

Bit 1, when set to 1, commands the timing sequencer to synchronously clear and halt. Both bits 0 and 1 must be set to 1 for the timing sequencer to run.

A synchronous reset should also be in effect whenever selecting the external SCLK (if applicable). In general, synchronous reset periods should be kept as short as possible to prevent possible loss of display memory data.

TS Indexed Register 1: TS Mode

This is a read/write register.
R/W : Port address = 3C5

Bit	Description
0	Timing sequencer state (bit 0).
1	Reserved.
2	Video load/2.
3	Dot clocks/2.
4	Shift 4.
5	Screen off (fast mode).
6-7	Reserved.

Bit 0 of the TS Mode register is used to set the timing sequencer state value. When set to a 0, the TS is set to State 0, or the 9-dot character clock; when set to a 1, the TS is set to State 1, or the 8-dot character clock.

when set to 1, loads the video shifter (such as the ATC) input latches at the video load rate.

Bit 3, when set to 1, provides sequencer clocking at half the MCLK rate, known as dot clocks/2 mode. This generates the dot clock signals at half the normal rate, effectively halving the pixel rate provided by the master clock. In VGA/EGA compatible operation, dot clocks/2 mode is used in all display modes that have 320, rather than 640, pixels per scan line.

Bit 4, when set to one 1, will allow the video shifter input latches to be loaded at quarter rate.

Bit 5, when set to one 1, will force blanking on the screen, allowing CPU access of video memory to go into a fast mode.

TS Indexed Register 2: Write Plane Mask

This is a read/write register.
R/W : Port address = 3C5

Bit	Description
0	Write enable display memory plane 0.
1	Write enable display memory plane 1.
2	Write enable display memory plane 2.
3	Write enable display memory plane 3.
4-7	Reserved.

The Write Plane Mask register enables or disables CPU write access to display memory planes on a plane-by-plane basis, and is only useful for 16-color (plane) systems. In 256 color mode, this register should be set to "0F" hex.

4.0

TS Indexed Register 3: Font Select

This is a read/write register.
R/W : Port address = 3C5

Bit	Description
4,1,0	Font Select A (FSA<2:0>).
5,3,2	Font Select B (FSB<2:0>).
6-7	Reserved.

FSA or FSB (as selected by Attribute bit 3) is used to select one of eight possible soft fonts, providing two simultaneous character sets for display.

Based on the Selection bits derived, the font memories are selected as follows:

Selection Bits (SEL⟨2:0⟩)	Selected Segment	Offset in Font Memory
0 0 0	0	0
0 0 1	1	16K
0 1 0	2	32K
0 1 1	3	48K
1 0 0	4	8K
1 0 1	5	24K
1 1 0	6	40K
1 1 1	7	56K

TS Indexed Register 4: Memory Mode

This is a read/write register.
R/W : Port address = 3C5

Bit	Description
0	Reserved.
1	Extended memory.
2	Odd/even mode.
3	Enable Chain 4.
4-7	Reserved.

Bit 1 of the Memory Mode Register is set to 1 to enable selection among multiple fonts, where one of up to eight fonts can be selected (See Font Select Register).

Bit 2 of the Memory Mode Register is set to 0 to select odd/even mode, in which even display memory planes (0 and 2) are active on display CPU accesses to even memory addresses (A0 = 0), while odd memory planes (1 and 3) are active on accesses to odd memory addresses (A0 = 1). When set to 1, causes the processor addresses to write to display memory planes according to the Write Map mask register.

Bit 3, when set to a 1, will enable Chain 4 (linear graphics) mode, where all four memories are chained linearly into a byte-oriented memory array whereby each byte will provide the eight bits (256-color) for each pixel. When set to 0, the processor will access data sequentially in the bit plane. When set to 1, causes the two low-order bits of the address (A1 and A0) to select the plane that is accessed:

A1	A0	Plane
0	0	0
0	1	1
1	0	2
1	1	3

TS Indexed Register 6: TS State Control (protected by KEY)
This is a read/write register.
R/W : Port address = 3C5

Bit	Description
0	Reserved.
1-2	Timing sequencer state (bit 1 & 2).
3-7	Reserved.

Bits 1 and 2 of the TS State Control Register is used to set the extended timing sequencer state value. In conjunction with bit 0 of the TS Mode register, the additional states are used to define the number of dots per character in text mode:

Bit ⟨2:0⟩	dots/char
1 1 1	16
1 0 0	12
0 1 1	11
0 1 0	10
0 0 1	8
0 0 0	9

IMPORTANT: All CRTC "character" timing calculations, with the exception of 9 dots/char are based on 8 dots/char regardless of the bit 1 and 2 of TS State Control Register's programmed value.

TS Indexed Register 7: TS Auxiliary Mode (protected by KEY)
This is a read/write register.
R/W : Port address = 3C5

Bit	Description
0	Select MCLK/4.
1	Select SCLK/2.
2	Set to 1 (always).
3	BIOS ROM Address Map 1.
4	Set to 1 (always) (ET4000AX Rev. E).
5	BIOS ROM Address Map 2.
6	Select MCLK/2 (if bit 0 is set to 0).
7	VGA mode.

Bit 0, when set to 1, selects the MCLK/4.

TS Indexed Register 7: TS Auxiliary Mode (continued)

Bit 1, when set to 1, will divide the SCLK input clock frequency by two.

Bits 3 and 5, are selection of ROM BIOS address space:

Bit 3 5	ROM BIOS Address Map Space Allocation	Total Memory Used
0 0	C0000-C3FFF	16KB
0 1	disabled	0KB
1 0	C0000-C5FFF; C6800-C7FFF	30KB
1 1	C0000-C7FFF*	32KB
	* Power-up default	

Bit 4 (ET4000AX Rev. E) should be set to 1 to eliminate possible corruption of video memory when GDC Indexed Register 6 bit 0 is toggled while ATC Indexed Register 10 bit 0 is set to 0. **NOTE:** When bit 4 is set to 1, CRTC Indexed Register 17 bit 7 cannot be set to 0 while GDC Indexed Register 6 bit 0 is switched and video memory is accessed, or the system will lock up.

Bit 6, when set to 1, will divide the MCLK input clock frequency by two.

Bit 7, when set to 1, enables VGA compatibility. A logical 0 will enable EGA compatibility. **NOTE:** The ET4000 is set to default on power-up to VGA mode.

4.5 ET4000 GDC Register Description

The CPU interface to the ET4000 internal Graphics Data Controller (GDC) consists of 11 read/write registers. Of these registers, two are accessed by separate independent I/O addresses. The remaining 9 registers are internally indexed, which means that they are accessed via a common I/O address (3CF), with one of the 9 registers that is actually accessed selected by the GDC Index register.

Table 4.5-1 GDC Registers and Addresses

Register Name	Port Address	Indexed Address
Segment Select	R/W : 3CD	
GDC Index register	R/W : 3CE	
Indexed Register Name		
Set/Reset	R/W : 3CF	0
Enable Set/Reset	R/W : 3CF	1
Color Compare	R/W : 3CF	2
Data Rotate	R/W : 3CF	3
Read Plane Select	R/W : 3CF	4
GDC Mode	R/W : 3CF	5
Miscellaneous	R/W : 3CF	6
Color Care	R/W : 3CF	7
Bit Mask	R/W : 3CF	8

GDC Segment Select

This is a read/write register.
R/W : Port address = 3CD

Bit	Description
0-3	Write segment pointer (WSP⟨0:3⟩).
4-7	Read segment pointer (RSP⟨0:3⟩).

When CRTC Indexed Register 36 (Video System Configuration 1) bit 4 is set to 0, then:

Bits 0-3: A 4-bit segment pointer selects one of sixteen segments (segment 0 to F) for CPU write operations.

Bits 4-7: A 4-bit segment pointer selects one of sixteen segments (segment 0 to F) for CPU read operations.

To enable the access of this register, the "KEY" must be set at least once after each power-on reset or a synchronous reset (done by setting TS Indexed Register bit 1 = 0).

GDC Index

This is a read/write register.
R/W : Port address = 3CE

Bit	Description
0-3	Current index.
4-7	Reserved.

Bits 0-3 provide the index of the currently selected internally indexed register. The GDC Index register determines which GDC indexed register will be accessed when a read/write is performed using port address 3CF.

GDC Indexed Registers

The remaining GDC registers are indexed registers, accessed by first writing the index value into the GDC Index register, and then accessing the indexed register using port address 3CF.

GDC Indexed Register 0: Set/Reset

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0	Set/reset value for map 0.
1	Set/reset value for map 1.
2	Set/reset value for map 2.
3	Set/reset value for map 3.
4-7	Reserved.

Each set/reset bit specifies the value to be written to all bits of the addressed byte of the corresponding memory map, 0 through 3, when the set/reset function is enabled for that map. If the set/reset bit for a plane is 1, enabling the set/reset function, then a 0 byte is written—if the set/reset bit for that plane is 0. If the set/reset bit for a plane is 1, enabling the set/reset function, then a 0 byte is written—if the set/reset bit for that plane is 0. If the set/reset bit for that plane is 1, a hexadecimal FF byte is written.

GDC Indexed Register 1: Enable Set/Reset

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0	Enable set/reset value for map 0.
1	Enable set/reset value for map 1.
2	Enable set/reset value for map 2.
3	Enable set/reset value for map 3.
4-7	Reserved.

Each enable set/reset bit enables or disables the set/reset function for the corresponding memory map, 0-3. When any of bits 0-3 are set to 0, the set/reset function in the corresponding plane will be disabled. When set to 1, the set/reset function will be enabled. When enabled, the set/reset function stores either a 0 or FF value in the addressed byte of a given plane, depending on the set/reset value (see GDC Indexed Register 0). When set/reset is enabled for a plane, the logical functions (see GDC Indexed Register 3) operate on the set/reset value for each plane and the latched data for that plane; the bit mask (see GDC Indexed Register 8) is also in effect. When the set/reset function is disabled, the addressed byte in a given plane is written as a combination of latched and CPU data, according to the write mode in effect and the bit mask, and the set/reset value has no effect. The set/reset function has no effect in write mode 1.

GDC Indexed Register 2: Color Compare

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0	Color compare value for plane 0 bits.
1	Color compare value for plane 1 bits.
2	Color compare value for plane 2 bits.
3	Color compare value for plane 3 bits.
4-7	Reserved.

The Color Compare register is used in read mode 1 to determine which pixels from the display memory location, read by the CPU, match a specified color. The 4-bit color value in the color compare register is compared to the 4-bit color value of each of the eight pixels, spread across the four planes.

From this comparison, a bit value of 1 is returned in the data byte to the CPU, at the position corresponding to each pixel that matches the Color Compare register, and 0 is returned for each pixel that does not match the Color Compare register. In other words, an 8-bit value is returned to identify the comparison for all eight pixels.

NOTE: Both the Color Compare and Color Care registers are useful only in the "PLANE" (16 colors) systems. In the "LINEAR BYTE" (256 colors) systems, the color compare operation should be performed at the CPU level.

GDC Indexed Register 3: Data Rotate and Function Select

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0-2	Rotate count.
3-4	Function select.
5-7	Reserved.

Bits 0-2 set the number of bits (0-7) by which CPU data should be rotated to the right before it is sent to the ALU for bit masking and logical functions. Rotation is circular, with bit 0 feeding back to bit 7.

Bits 3 and 4 select the logical operation to be performed by the ALU on incoming CPU data and latched data. The logical operation is performed on only those bits that are enabled by the bit mask register; mask-disabled bits are written as the latched value (resulting from previous memory reads) only. For those bits that are mask enabled, one of four logical operations may be performed between CPU data and latched data by setting the function select as follows:

Bit 4	Bit 3	Logical operation
0	0	MOVE CPU data through unchanged.
0	1	AND CPU data with latched data.
1	0	OR CPU data with latched data.
1	1	XOR CPU data with latched data.

Note that write mode 1 may be used to write latched data unmodified; the same effect could be obtained by ANDing a CPU data byte of FF, ORing or XORing a CPU data byte of 0, or by setting the bit mask register to 0. The logical functions operate in write modes 0, 2 and 3 only; they are ignored in write mode 1.

GDC Indexed Register 4: Read Plane Select

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0-1	Plane select.
2-7	Reserved.

Bits 0-1 select the memory plane 0-3 from which the addressed byte is to be read and returned on the CPU data bus, in the "PLANE" (16 colors) configurations. Only one plane can be read at any one time.

GDC Indexed Register 5: GDC Mode

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0-1	Write mode.
2	Reserved.
3	Read mode.
4	Odd/even mode.
5	Shift.
6	Enable 256 color mode.
7	Reserved.

Bits 0 and 1 select the mode in which data bytes are to be written to screen memory. The write modes are:

Bit (1:0)	Write Mode Selected
0 0	Write mode 0. Each CPU data byte written to display memory, as modified by the current rotation setting (see GDC Indexed Register 3), is combined with the latched data for each map according to the current logical function (see GDC Indexed Register 3) and written to each memory map. The byte written by the CPU is passed identically to the ALU for each map; differences in the byte actually written to the screen may occur due to differences in the latch contents for different maps. If the set/reset function is enabled for any map (see GDC Indexed Register 1), then the set/reset bit value for that map (see GDC Indexed Register 0) is written to every bit of the addressed byte of that map regardless of the CPU data. The bit mask (see GDC Indexed Register 8) applies in write mode 0, and causes the latch data alone to be written to each bit that is mask disabled.
0 1	Write mode 1. The data contained in the latches is written unmodified to the addressed byte in screen memory. All maps are written. This is useful for rapid data movement from display memory to display memory, as all maps can be latched with a single read and then written with a single write mode 1 operation. The bit mask is ignored, as is the selected logical function. The set/reset function is also ignored.
1 0	Write mode 2. Each bit, 0-3, of the data written by the CPU is extended to a byte and written to the four corresponding planes. Bit 0 of the data byte is extended to a byte and written to the addressed byte of map 0, bit 1 is extended to a byte and written to map 1, and so on up to bit 3, which is extended to a byte and written to map 3. The bit mask applies to the data byte for each map; that is, after the bit for each map from the CPU data written is extended to a byte, the byte for each map is masked as if it were the CPU data byte. The selected logical function operates normally on the byte for each map and the latched data for that map. The set/reset operation functions normally, overriding the write mode 2 bit for a given map when enabled. The data rotate register has no effect in write mode 2.
1 1	Write mode 3. Eight bits of the value contained in the Set/Reset register are written for each map. Rotated CPU data are ANDed with data from the bit mask register (see GDC Indexed Register 8) to produce an 8-bit value that functions as the bit mask register does in write modes 0 and 2.

3 selects the read mode. When bit 3 is 0 (Read Mode 0), the data read from the map indicated by the read map select register (see GDC Indexed Register 4) is returned on the CPU data bus. This is the normal read mode of operation. When bit 3 is 1, the color compare operation is enabled on a CPU read. (See Color Compare Register).

Bit 4 is set to 1 to select odd/even addressing mode, in which even maps are accessed with even addresses and odd maps are accessed with odd addresses. The function of this bit is to determine from which display map data is to be routed to the CPU data bus on a CPU read in odd/even mode. If bit 4 is 1 and the Read Map Select register selects either of two maps in a given pair, then the even map is selected if address line 0 is 0, and the odd map is selected if address line 0 is 1. Bit 2 of CRTC Timing Sequencer Indexed Register 4 should be set to 0 to select odd/even mode, to generate all address control other than the read data selection in odd/even addressing mode. Odd/even addressing mode is useful for text modes.

Bit 5, when set 1, enables the ATC's shift registers to shift for pixel formatting to support the 320x200 4-color CGA mode.

Bit 6, when set to 0, permits the loading of the ATC's shift registers to be controlled by bit 5. When set to one, the registers are loaded to support the 256-color mode.

GDC Indexed Register 6: Miscellaneous

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0	Graphics mode enable.
1	Enable odd/even mode.
2-3	Memory map.
4-7	Reserved (= 0).

4.0

Bit 0, when set to 1, enables graphics mode.

Bit 1, when set to 1, enables odd/even mode, will cause the replacement of the CPU address bit 0 with a high-order bit, and the odd/even maps are "chained" via the CPU A0 bit.

Bits 2,3 Memory Map—Control mapping of the Regen Buffer into CPU address space. **NOTE:** Bits 2 & 3 should be set to 0 when bit 4 of CRTC Indexed Register 36 is set to 1 (linear system).

Bits 3 2	
0 0	Hex A0000 for 128K bytes.
0 1	Hex A0000 for 64K bytes.
1 0	Hex B0000 for 32K bytes.
1 1	Hex B8000 for 32K bytes.

NOTE: The value 00 should not be programmed in all extended high-resolution/ color modes.

GDC Indexed Register 7: Color Care

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0	Enable color compare color output 0.
1	Enable color compare color output 1.
2	Enable color compare color output 2.
3	Enable color compare color output 3.
4-7	Reserved.

Each bit, 0-3, enables or disables the participation of the corresponding plane in a read mode 1 color comparison. If a bit is 1, then the color compare is enabled for that plane (see the GDC Indexed Register 2: Color Compare). If a bit is 0, then the value in that plane has no effect on the value returned by the color comparison.

GDC Indexed Register 8: Bit Mask

This is a read/write register.
R/W : Port address = 3CF

Bit	Description
0-7	Controls CPU data routing for corresponding bits 0-7 of addressed screen map byte.

Each bit 0-7 of the Bit Mask register either blocks the corresponding CPU data bit from affecting the value written to the screen or allows the CPU data bit through. A zero (0) value blocks and a 1 value passes CPU data. If a given bit is blocked, the value stored in that bit of each data latch (one for each plane) is sent to the corresponding screen plane. If a given bit is enabled, the value in that bit position of the CPU data is passed to the ALU, where it can be mixed with latched data via the selected logical function. The data will be rotated (see GDC Indexed Register 3) before it is masked.

4.6 ET4000 ATC Register Description

The CPU interface to the ET4000 internal Attribute Controller (ATC) consists of 23 read/write registers, and a separate flip-flop (1-bit register) which can be toggled between index/data mode. Two I/O addresses are used in conjunction with the index/data mode flip-flop to access the 23 registers as follows: An I/O read to the Input Status 1 register (3BA or 3DA depending on monochrome or color mode respectively, as controlled by bit 0 in the Miscellaneous Output Register) will reset the index/data flip-flop to index mode. Every I/O write with port address 3C0 will also toggle the index/data flip-flop between index and data mode. The index value in the ATC index register can be read with I/O address 3C0. While in index mode, the index value can be written to the ATC index register with I/O address 3C0, with the index/data mode flip-flop toggled to the data mode.

If the 16-bit I/O is enabled, an I/O WORD access to port 3C0 will automatically reset the index/data flip-flop. All of the 22 indexed registers can be read with I/O address 3C1. While in data mode, all of these indexed registers can be written to with I/O address 3C0, with the index/data mode flip-flop toggled to the index mode.

Table 4.6-1 ATC Index Register

Register Name	Port Address	Indexed Address
ATC Index register	R : 3C0 W : 3C0 (INDEX)	

Table 4.6-2 ATC Indexed Registers

Indexed Register Name		
Palette	R : 3C1 W : 3C0 (DATA)	0-F
ATC Mode	R : 3C1 W : 3C0 (DATA)	10
Overscan	R : 3C1 W : 3C0 (DATA)	11
Color Plane Enable	R : 3C1 W : 3C0 (DATA)	12
Horizontal Pixel Panning	R : 3C1 W : 3C0 (DATA)	13
Color Reset	R : 3C1 W : 3C0 (DATA)	14
Miscellaneous	R : 3C1 W : 3C0 (DATA)	16

ATC Index

This is a read/write register.
R : Port address = 3C0
W : Port address = 3C0 (index/data flip-flop in INDEX mode)

Bit	Description
0-4	Current ATC index.
5	Palette RAM address source.
6-7	Reserved.

Bits 0-4 provide the index of the currently selected internally indexed register. A bit 5 value of 0 enables CPU write access to palette RAM, and replaces all video outputs with the contents of the overscan register. A bit 5 value of 1 disables CPU write access to palette RAM and allows ATC access of RAM.

This bit must be set to 0 before the CPU can update any palette RAM location. After the palette RAM is updated, this bit must be set to 1 so the ATC can access the palette RAM for video information.

ATC Indexed Registers

The following registers are the ATC indexed registers. These registers are accessed by writing the index of the desired register to the ATC Index register when the index/data flip-flop is in INDEX mode, and then accessed using the index value in the ATC Index Register. See details under previous paragraphs under ET4000 ATC REGISTER DESCRIPTION.

ATC Indexed Registers 0-F: Palette RAM

This is a read/write register.
R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description
0	Primary blue video.
1	Primary green video.
2	Primary red video.
3	Secondary blue/mono video.
4	Secondary green/intensity video.
5	Secondary red video.
6	Reserved.
7	Reserved.

These 16 internal palette registers define a dynamic remapping between colors as defined by text attributes and graphics bit maps and the colors actually generated by the video circuitry. Each palette register 0-15 corresponds to an attribute, 0-15, in the "PLANE" (16 colors) configuration. Four bits (1 bit from each plane) of video data for a given pixel enters the palette RAM and addresses one of the 16 palette registers, and the 6-bit value stored in the corresponding palette register is transferred to the output latch of the ATC to provide the actual pixel data. In "linear byte" (256 colors) configuration, these registers should be programmed to have contents the same as the indexed address to "pass through" the internal display data.

Bits 0-5, when set to 1, select the appropriate color attribute. When set to 0, indicate the appropriate color is not present.

ATC Indexed Register 10: Mode Control

This is a read/write register.
R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description
0	Graphics/text select.
1	Mono/color select.
2	Line graphics enable.
3	Background intensity/blink.
4	Reserved.
5	Enable pixel panning.
6	PELCLOCK/2.
7	SB/SG select.

Bit 0, when set to 1, enables the ATC to process the pixel data in graphics mode; when set to 0, enables the ATC to process the pixel data in text mode.

Bit 1, when set to 1, selects a monochrome display attribute; when set to 0, enables a color display attribute.

Bit 2, when set to 1, specifies that in the 9 dots/character state (controlled by the CRTC), the ninth (and last) dot produced horizontally per character should replicate the eighth dot for character codes C0 hex through DF hex. The ninth dot of all other character codes is always 0 when line graphics is enabled. This is normally used to allow the text mode line graphics characters supported on the IBM Monochrome Display, which are 8-dot-wide characters in a 9-dot-wide character box, to connect. If this bit is 0 and the CRTC is set to the 9 dots/character state, then the 9th dot will display bit 7 of Intensity Memory plane (plane 3).

Bit 3, when set to 1, enables blinking in both text and graphics modes. When enabled in text mode, blinking occurs whenever bit 7 of the attribute byte for a given character is 1; when enabled in graphics mode, blinking occurs for all bits that have a 1 in the intensity plane. Blinking is performed by toggling the most significant address line (bit 3) into the palette RAM, thus toggling the video data between the lower eight and upper eight palette RAM registers. This means that the effect of the blink (for example, reverse video to video, video to high-intensity video, dark to dark) is completely programmable. Bit-mapped graphics modes can be programmed to support all the attributes of text modes, for instance.

NOTE: The non-blinking bits will use the upper eight palette registers.

Bit 3, when set to 0, disables blinking; in this case bit 3 of the palette RAM address is multiplexed directly from the video data to the palette RAM. When bit 3 is 0, all 16 simultaneous colors are enabled in graphics mode; in text mode, all 16 background colors are available simultaneously.

Bit 5, when set to one (1), disables pixel panning while in split screen, while a 0 will enable the panning.

Bit 6, when set to 1, halves the rate of pixel output to the screen, such that only 4, instead of the usual 8, pixels are output in a character clock time. This is normally used only for the 320x200 256-color graphics mode. For all other 256-color modes, this bit should be set to 0.

Bit 7 is used to select for the SB and SG video bits. When set to 1, SB and SG are bits 0 and 1, respectively, of the Color Select Register; a zero (0) causes them to be bits 4 and 5 of the internal palette register. This is not applicable to linear graphics (256-color) modes, for which SB and SG always come from the memory data.

ATC Indexed Register 11: Overscan Color

This is a read/write register.
R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description
0	Blue border color.
1	Green border color.
2	Red border color.
3	Intensity border color.
4	Secondary Blue border color.
5	Secondary Green border color.
6	Secondary Red border color.
7	Secondary Intensity border color.

This register defines the color to be displayed around the perimeter of the working screen area (the border or overscan color).

Bits 0-7, when set to 1, select the appropriate border color/attribute, each bit corresponding to one of the output pins. This value is a 0 for the monochrome display.

NOTE: When, in plane graphics mode, the high resolution mode is selected (via ATC Indexed Register 16), bits 4-7 should be programmed equal to bits 0-3 and the overscan limited to 16 colors.

ATC Indexed Register 12: Color Plane Enable

This is a read/write register.
R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description
0-3	Enable plane.
4-5	Video status select.
6-7	Reserved.

In "PLANE" (16 colors) configuration, the color plane relative to each of bits 0-3 is enabled when the appropriate individual bits are set to one. Bits 0,1,2,3 control the enabling of planes 0,1,2,3, respectively.

Bits 5 and 4 select two of eight color outputs to be returned by the Status register, as follows:

Input Status Register 1			
Bit		Bit	
5	4	5	4
0	0	PR	PB
0	1	SG	SB
1	0	PI	PG
1	1	SI	SR

ATC Indexed Register 13: Horizontal Pixel Panning

This is a read/write register.
R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description
0-3	Horizontal pixel panning.
4-7	Reserved.

Bits 0-3 specify the number of pixels by which the video data should be shifted to the left. Shifts of up to nine pixels are supported. Note that in 9-dot modes, a value of 8 signifies no shifts, and the values 0-7 signify shifts of 1-8 pixels, respectively.

ATC Indexed Register 14: Color Select

This is a read/write register.
R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description
0	S_color 4.
1	S_color 5.
2	S_color 6.
3	S_color 7.
4-7	Reserved.

Bits 0 and 1 are available for replacement use of bits 4 and 5 of the attribute palette registers, forming an 8-bit value for color to be exported from the chip. When bit 7 of the ATC Mode register is set to 1, bits 0 and 1 are selected as SB and SG outputs of the plane system.

Bits 2 and 3 provide the two high-order bits of the exported digital color value in plane systems. With 256-color graphic modes, the 8-bit attribute value becomes the 8-bit digital value exported from the chip.

ATC Indexed Register 16: Miscellaneous

This is a read/write register (protected by KEY).
R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description
0-3	Reserved.
4-5	Select High Resolution/color mode.
6	2-byte character code (ET4000 Rev. E).
7	Bypass the internal palette.

Bits 4-5, in combination, select high-resolution or high-color modes. When bit 4 is set to a logical 1, the MCLK/2 bit in TS Index 7 should also be set. The available selections are:

See Addendum 6.1 for the description of bit 6 and programming instructions.

Bit 4 5	
0 0	Normal power-up default.
0 1	Reserved.
1 0	High-resolution mode (up to 256 colors).
1 1	High-color 16-bit/pixel.

NOTE: Normally, high-resolution mode never needs to be set.

Bit 7, when set to 1, causes the internal palette to be bypassed (effectively the output equals the input value).

5.0 Programming Interface

The functions that are supported as program calls to the adapter are listed in this section. These calls are made through software interrupt 10H (INT 10H).

Functions are identified by the content of the AH register at the time of the call; in some cases, the AH register identifies a group of similar functions and the AL register identifies the specific function. The primary functions are:

Interrupt 10 Functions

(AH)	Function
00H	Mode Set
01H	Set Cursor Type
02H	Set Cursor Position
03H	Read Cursor Position
04H	Read Light Pen Position (not supported)
05H	Select Active Display Page
06H	Scroll Active Page Up
07H	Scroll Active Page Down
08H	Read Character at Current Cursor Position
09H	Write Character(s) at Current Cursor Position
0AH	Write Character(s) Only at Current Cursor Position
0BH	Set Color Palette
0CH	Write Dot
0DH	Read Dot
0EH	Write Teletypewriter to Active Page
0FH	Return Current Video State
10H	Set Palette Registers
11H	Character Generator Routine
12H	Alternate Select
13H	Write String
1AH	Display Combination Code
1BH	Return Functionality/State Information
1CH	Save/Restore
14H	Reserved
15H	Reserved
16H	Reserved
17H	Reserved
18H	Reserved
19H	Reserved

BIOS FUNCTION CALLS

All values in hexadecimal unless otherwise noted.

AH=0 Set video mode.
Input:
AL=mode to set (see table below).
Output:
none.

Mode	Type	Colors/ Shades	Alpha Format	Buffer Start	Box Size	Max. Pages	Display Size
0	A/N	16/256K	40x25	B8000	8x8	8	320x200
0*	A/N	16/256K	40x25	B8000	8x14	8	320x350
0+	A/N	16/256K	40x25	B8000	9x16	8	360x400
1	A/N	16/256K	40x25	B8000	8x8	8	320x200
1*	A/N	16/256K	40x25	B8000	8x14	8	320x350
1+	A/N	16/256K	40x25	B8000	9x16	8	360x400
2	A/N	16/256K	80x25	B8000	8x8	8	640x200
2*	A/N	16/256K	80x25	B8000	8x14	8	640x350
2+	A/N	16/256K	80x25	B8000	9x16	8	720x400
3	A/N	16/256K	80x25	B8000	8x8	8	640x200
3*	A/N	16/256K	80x25	B8000	8x14	8	640x350
3+	A/N	16/256K	80x25	B8000	9x16	8	720x400
4	APA	4/256K	40x25	B8000	8x8	1	320x200
5	APA	4/256K	40x25	B8000	8x8	1	320x200
6	APA	2/256K	80x25	B8000	8x8	1	640x200
7	A/N	4	80x25	B0000	9x14	8	720x350
7+	A/N	4	80x25	B0000	9x16	8	720x400
D	APA	16/256K	40x25	A0000	8x8	8	320x200
E	APA	16/256K	80x25	A0000	8x8	4	640x200
F	APA	4	80x25	A0000	8x14	2	640x350
10	APA	16/256K	80x25	A0000	8x14	2	640x350
11	APA	2/256K	80x30	A0000	8x16	1	640x480
12	APA	16/256K	80x30	A0000	8x16	1	640x480
13	APA	256/256K	40x25	A0000	8x8	1	320x200
18	A/N	4	132x44	B0000	8x8	2	1056x352
19	A/N	4	132x25	B0000	9x14	4	1188x350
1A	A/N	4	132x28	B0000	9x13	4	1188x364
22	A/N	16/256K	132x44	B8000	8x8	2	1056x352
23	A/N	16/256K	132x25	B8000	8x14	4	1056x350
24	A/N	16/256K	132x28	B8000	8x13	4	1056x364
25	APA	16/256K	80x60	A0000	8x8	1	640x480
26	A/N	16/256K	80x60	B8000	8x8	3	640x480
29	APA	16/256K	100x37	A0000	8x16	1	800x600
2A	A/N	16/256K	100x40	B8000	8x15	4	800x600
2D	APA	256/256K	80x25	A0000	8x14	1	640x350
2E	APA	256/256K	80x30	A0000	8x16	1	640x480
2F	APA	256/256K	80x25	A0000	8x16	1	640x400
30	APA	256/256K	100x37	A0000	8x16	1	800x600
37	APA	16/256K	128x48	A0000	8x16	1	1024x768
38	APA	256/256K	128x48	A0000	8x16	1	1024x768

A/N = Alphanumeric modes (text)
APA = All Points Addressable modes (graphics)
* Extended Graphics Adapter text modes with 350 scan lines.
+ 9x16 character cell enhanced text modes with 400 scan lines.

Note that there are a number of distinct text modes available including 132-column monochrome text modes.

NOTES:

1. AL bit 7 can be 0 or 1. When set to 1, the MODE SET function does not clear the display buffer.

2. Default modes are 3+ for color monitor and 7+ for monochrome monitor.

3. Modes 0 through 6 emulate IBM Color Graphics Adapter support.

4. Modes 0, 2, and 5 are identical to modes 1, 3, and 4 respectively.

5. There is no hardware cursor in graphics (APA) modes. Altering the hardware cursor type has no effect in these modes.

6. Selecting the number of scan lines in alphanumeric modes is detailed under "(BL) = 30H, Select Scan Lines for Alphanumeric Modes".

7. Use of the equipment flags variable at address 0:410 (applicable bits are ⟨5,4⟩:
   * Binary XX11 XXXX = monochrome
   * Binary XX10 XXXX = color

   If there is more than one video adapter in the system, the equipment flag setting at the time of the set mode call determines if the mode should be set in the color or monochrome adapter. If necessary, color modes will be converted to monochrome mode 7 and monochrome modes to color mode 3.

   If there is only one adapter, then in EGA mode, the equipment flag forces a color or monochrome mode to be set, with conversion if necessary.

   In VGA mode, the equipment flag automatically gets changed to agree with the mode being set.

AH = 1 Set cursor type (start and stop scan lines)

Input:

CH = start scan line for cursor.
CL = end scan line for cursor.

Output:

none.

Note: Only bits 0 through 4 should be set.

AH = 2 Set cursor position.
Input:
BH = page for which cursor is to be set.
DH = row position cursor is to be set to.
DL = column position cursor is to be set to.
Output:
none.

Note: (0,0) is upper left of screen.

AH = 3 Read cursor position.
Input:
BH = page for which cursor is to be read.
Output:
CH = current start scan line for cursor.
CL = current stop scan line for cursor.
DH = row position of cursor in selected page.
DL = column position of cursor in selected page.

AH = 4 Read light pen position
Input:
none.
Output:
AH = 0 then light pen switch not activated, return values invalid.
1 then light pen switch activated, valid values returned.
BX = pixel column.
CH = raster line.
CX = raster line (new graphics modes).
DH = row of character light pen position.
DL = column of character light pen position.

AH = 5 Select active page.
Input:
AL = page to select as active page.
Output:
none.

AH=6 Scroll up active page.
Input:
AL=number of lines rows are to move up.
0 means blank window.
BH=attribute used to fill blank line or lines at bottom.
CH=row of upper left corner of scroll window.
CL=column of upper left corner of scroll window.
DH=row of lower right corner of scroll window.
DL=column of lower right corner of scroll window.
Output:
none.

AH=7 Scroll down active page.
Input:
AL=number of lines rows are to move down.
0 means blank window.
BH=attribute used to fill blank line or lines at top.
CH=row of upper left corner of scroll window.
CL=column of upper left corner of scroll window.
DH=row of lower right corner of scroll window.
DL=column of lower right corner of scroll window.
Output:
none.

AH=8 Read character and attribute at cursor position.
Input:
BH=page to read from.
Output:
AH=attribute of character at cursor position.
AL=character read from cursor position.

Note: Attribute valid in text modes only. Only characters drawn in white matched in graphics modes.

AH=9 Write character and attribute at cursor position.
Input:
AL=character to write at cursor position.
BH=page to write character and attribute to.
BL=attribute to write character with in text mode.
=foreground color in graphics mode.
CX=number of times to write character and attribute.
Output:
none.

Note: If bit 7 of BL is 1 in graphics mode, then the character is XOR'd into video memory, else the character displaces the previous contents of video memory. (XOR not valid in 256 color modes.)

Note: In 256 color modes, the value passed in BH is used as the background color.

AH=0A Write character only at cursor position.

Input:
AL=character to write at cursor position.
BH=page to write character and attribute to.
BL=(in graphics modes only) foreground color for character.
CX=number of times to write character and attribute.
Output:
none.

Note: See previous notes for function AH=9.

AH=0B Color select for color/graphics adapter compatible modes.
Input:
BH=0 means set the background color specified by BL.
<>0 means set the palette specified by BL.
BL=color value to be used:
*When setting the background color, BL selects any of the 16 colors with a value of 0-15 with bits 0-3.
*When selecting the palette, BL operates as follows:
bit 0=0 selects palette 0 (green/red/brown).
bit 0=1 selects palette 1 (cyan/magenta/white).

Output:
none.

Note: In text modes, the set background function sets the border color only. In graphics modes, the set background function sets both the border and background colors.

Note: This function is implemented via emulation, since the EGA does not have the same color registers as the color/graphics adapter.

Note: Actual operation is to set palette register 0 for background, palette register 11h for overscan, and palette registers 1-3 for palette colors 1-3. Palette registers are set in any graphics mode, although this was valid only in 320x200 graphics mode on the color/graphics adapter.

AH=0C Draw graphics pixel.
Input:
AL=color (actually attribute that goes to the palette RAM) to draw pixel in.
BH=page to draw pixel in.
CX=screen column to write pixel at.
DX=screen row to write pixel at.
Output:
none.

Note: If bit 7 of AL is 1, then the pixel is XOR'd with the contents of video memory (except in 256 color modes).

AH=0D Read graphics pixel color (actually attribute that goes to the palette RAM).
Input:
BH=page to read pixel from.
CX=screen column to read pixel from.
DX=screen row to read pixel from.
Output:
AL=pixel value read (attribute of pixel).

Note: Interpretation of value returned depends on graphics mode in effect.

AH=0E Write TTY.
Input:
AL=character to write.
BL=color to draw character in graphics mode.
Output:
none.

Note: Carriage return, backspace, line feed, bell are commands, not displayed characters. Cursor is moved to the right after character is displayed, with wrap and scroll at right margin of screen.

AH=0F Return video information.
Input:
none.
Output:
AL=video mode in effect.
AH=text columns supported in current mode.
BH=active display page.

Note: Bit 7 of AL is set to 1 if the regen buffer was not cleared when the mode was set.

AH = 10 Set EGA palette registers.
AL = 0 set color for a single palette register.
Input:
BH = color to set palette register to.
BL = palette register to set color of.
Output:
none.

AL = 1 set color for overscan (border color) register.
Input:
BH = color to set overscan register to.
Output:
none.

AL = 2 set colors for all 16 palette and the overscan registers.
Input:
ES:DX = address of table organized as follows:
bytes 0-15 = colors for palette registers 0-15.
byte 16 = color for overscan register.
Output:
none.

AL = 3 select interpretation of intensity/blink attribute bit.
Input:
BL = 0 select high intensity background.
1 select blinking.
Output:
none.

AL = 4 reserved

AL = 5 reserved

AL = 6 reserved

AL = 7 read individual palette register
Input:
BL = palette register to read (range 0 to 15)
Output:
BH = value read

AL=8 read overscan register
Input:
none
Output:
BH=value read

AL=9 read all palette registers and overscan
Input:
ES:DX points to 17 byte table area
Output:
bytes 0-15 = palette values
byte 16 = overscan value

AL=10h set individual color register (external palette)
Input:
BX=color register to set
DH=red value to set
CH=green value to set
CL=blue value to set
Output:
none

AL=11h reserved

AL=12h set block of color registers
Input:
ES:DX=pointer to table of color values in RGB format
(i.e. 3 bytes for each entry)
BX=starting index
CX=number of color registers to set
Output:
none

AL=13h select color page
BL=00 select paging mode
Input:
BH=paging mode
0—selects 4 register pages of 64 registers
1—selects 16 register pages of 16 registers
Output:
none

BL=01 select page
Input:
BH=page value (0 to nn, where nn = 3 in page mode 0
and nn = 15 in page mode 1)

AL = 14h reserved

AL = 15h read individual color register
Input:
BX = color register to read
Output:
DH = red value read
CH = green value read
CL = blue value read

AL = 16h reserved

AL = 17h read block of color registers
Input:
ES:DX = pointer to destination for RGB table
(3 bytes/entry)
BX = starting index
CX = number of color registers read
Output:
(ES:DX) = table

AL = 18h reserved

AL = 19h reserved

AL = 1Ah read color page state
Input:
none
Output:
BL = current paging mode
BH = current page

AL = 1Bh sum colors to gray shades (VGA only)
(This call reads R, G, and B values found in external palette ram and performs a weighted sum (30% red, 59% green, and 11% blue), then writes the result into each R, G, and B component of color register (original data is overwritten).
Input:
BX = starting index
CX = number of color registers to sum

AH=11 Font interface.
AL=0 load user font into soft font (text mode).
Input:
BH=# of bytes per character.
BL=# of soft font to load font into.
CX=# of characters to store.
DX=offset into table of first character to store.
ES:BP=pointer to font to load.
Output:
none.

AL=1 load ROM monochrome font into soft font (text mode.)
Input:
BL=# of soft font to load font into.
Output:
none.

AL=2 load ROM 8x8 double dot font into soft font (text mode.)
Input:
BL=# of soft font to load font into.
Output:
none.

AL=3 select fonts displayed (text mode).
Input:
BL=specification for high/low attribute bit 3:
bits 4,1,0=soft font # selected when attr bit 3 is 0.
bits 5,3,2=soft font # selected when attr bit 3 is 1.
Output:
none.

AL=4 load ROM 8x16 font into soft font (text mode.)
Input:
BL=# of soft font to load font into.
Output:
none.

Note: The following functions AL=1X are the same as AL=0X, except:

*The active page must be zero.
*The char_height variable will be recalculated.
*The crt_rows variable will be recalculated as:
INT((200 | 350 | 400) / char_height)—1
*regen_length will be recalculated as:
(crt_rows + 1) * crt_columns * 2
* The CRTC will be reprogrammed as:
Max scan line = char_height—1
Cursor start = char_height—2
Cursor end = char_height—1
(cursor_type set via set_cursor_type BIOS function)
Vert disp end =
((crt_rows + 1) * char_height)—1
[char_height*2 above if double scan]
Underline = char_height—1 (mono. modes only)

AL=10 load user font into soft font (text mode).
Input:
BH=# of bytes per character.
BL=# of soft font to load font into.
CX=# of characters to store.
DX=offset into table of first character to store.
ES:BP=pointer to font to load.
Output:
none.

AL=11 load ROM monochrome font into soft font (text mode.)
Input:
BL=# of soft font to load font into.
Output:
none.

AL=12 load ROM 8x8 double dot font into soft font (text mode.)
Input:
BL=# of soft font to load font into.
Output:
none.

AL=14 load ROM 8x16 font into soft font (text mode.)
Input:
BL=# of soft font to load font into.
Output:
none.

AL=20 set user font chars 128-255 for color/graphics adapter compatible modes (graphics).
Input:
ES:BP=pointer to font to load.
Output:
none.

AL=21 set user font (graphics).
Input:
BL=# of rows on screen, as follows:
0 then DL=user specified # rows.
DL=# rows.
1 then 14 rows.
2 then 25 rows.
3 then 43 rows.
CX=character height.
ES:BP=pointer to font to load.
Output:
none.

AL=22 set ROM 8x14 font (graphics).
Input:
BL=# of rows on screen, as follows:
0 then DL=user specified # rows.
DL=# rows.
1 then 14 rows.
2 then 25 rows.
3 then 43 rows.

AL=23 set ROM 8x8 double dot font (graphics).
Input:
BL=# of rows on screen, as follows:
0 then DL=user specified # rows.
DL=# rows.
1 then 14 rows.
2 then 25 rows.
3 then 43 rows.

AL=24 set ROM 8x16 font (graphics)
Input:
BL=# of rows on screen, as follows:
0 then DL=user specified # rows.
DL=# rows.
1 then 14 rows.
2 then 25 rows.
3 then 43 rows.

AL=30 return font information.
Input:
BH=0 return pointer to upper 128 graphics characters
(INT 01Fh pointer-color/graphics adapter compatible modes).
BH=1 return pointer to graphics font
(INT 043h pointer).
BH=2 return pointer to ROM 8x14 font.
BH=3 return pointer to ROM 8x8 double dot font.
BH=4 return pointer to top half of ROM 8x8 double dot font.
BH=5 return pointer to ROM font supplement for 9x14 text.
BH=6 return pointer to ROM 8x16 font.
BH=7 return pointer to ROM font supplement for 9x16 text.
Output:
CX=char_height.
DL=crt_rows -1.
ES:BP=pointer to table selected by BH.

AH=12 Return EGA information or select alternate printscreen handler.
BL=10 return information.
Input:
none.
Output:
BH=0 color mode, addressed at 03DX.
=1 monochrome mode, addressing at 03BX.
BL=installed video memory as follows:
0 = 64K bytes installed.
1 = 128K bytes installed.
2 = 192K bytes installed.
3 = 256K (or more) bytes installed.
CH=feature bits (bits 4-7 of info_1 shifted right).
CL=switches (bits 0-3 of info_1).

BL=20 select this BIOS's print screen routine, which supports all modes of this BIOS.

Input:
none.
Output:
none.

Note: This function selects the print screen routine built into this ROM to replace the standard BIOS print screen routine.

BL=30 select scan lines for text modes

Input:
AL=scan lines to set (takes effect on next mode change)
0 = 200 scan lines
1 = 350 scan lines
2 = 400 scan lines
Output:
AL=12h

BL=31 set default palette load

Input:
AL=# enable/disable palette loading
0=enable palette loading
1=disable palette loading
Output:
AL=12h

BL=32 Enable/disable video

Input:
AL=# enable/disable video
0=enable video
1=disable video
Output:
AL=12h

BL=33 Enable/disable gray scale summing

Input:
AL=# enable/disable gray scale summing
0=enable summing
1=disable summing
Output:
AL=12h

BL = 34 Enable/disable cursor emulation
Input:
AL = # enable/disable cursor emulation
0 = enable emulation
1 = disable emulation
Output:
AL = 12h

BL = 35 Select/deselect display
Input:
Buffers for adapter and planar video are initialized then:
AL = # select/deselect adapter/planar video
0 = initial deselect adapter video
1 = initial select planar video
2 = deselect active display
3 = select inactive display
ES:DX = pointer to 128-byte buffer
Output:
AL = 12h

BL = 36 Enable/disable video output
Input:
AL = # enable/disable video output
0 = enable video output
1 = disable video output
Output:
AL = 12h

AH = 13 Write text string.

Input:

AL = 0 text string is characters only. Cursor not moved from original position.

BL = attribute to write text string with.

1 text string is characters only. Cursor moved to end of text string.

BL = attribute to write text string with.

2 text string is alternating character/attribute sequence. Cursor not moved from original position.

3 text string is alternating character/attribute sequence. Cursor moved to end of text string.

BH = page to write text string to.

CX = count of characters (not bytes) in string to display.

DH = row position at which to start displaying string.

DL = column position at which to begin displaying string.

ES:BP = pointer to text string to be written.

Note: Scroll, backspace, carriage return, if any, will take place in the active page only.

AH = 1A Read/write display code function.

Display combination codes:

00—No display
01—Monochrome with 5151
02—CGA with 5153/4
03—Reserved
04—EGA with 5153/4
05—EGA with 5151
06—Professional Graphics System with 5175
07—VGA with analog BW
08—VGA with analog color
09—Reserved
0A—System 30 with 5153/4
0B—System 30 with analog BW
0C—System 30 with color
0D to FE—Reserved
FF—Unknown

AL = 0 Read display code
Input:
none
Output:
AL = 1Ah
BL = Active display code
BH = Alternate display code

AL = 1 Write display code
Input:
BL = Active display code
BH = Alternate display code
Output:
AL = 1Ah

AH = 1B Return functionality/state information
Input:
BX = implementation type
ES:DI = buffer (40h bytes)
Output:
AL = 1Bh
Buffer, in the following format:

offset	type	description
00	word	Offset to static functionality information
02	word	Segment to static functionality information
04	byte	Video mode
05	word	Number of columns on screen
07	word	Length of regen buffer
09	word	Start address of regen buffer (offset)
0B	8*word	Cursor position for 8 pages (row, column)
1B	word	Cursor mode setting (start, end)
1D	byte	Active page
1E	word	CRTC address
20	byte	Current setting of 3x8 register (mode register)
21	byte	Current setting of 3x9 register
22	byte	Rows on screen
23	word	Character height
25	byte	Active display combination code
26	byte	Alternate display combination code
27	word	Colors supported for current video mode
29	byte	Display pages supported for current video mode

offset	type	description
2A	byte	Scan lines in current video mode 0=200 1=350 2=400 3=480 4=Reserved. 5=600 (Note: IBM reserves this) 6=768 (Note: IBM reserves this) 7-255=reserved
2B	byte	Primary character block 0=block 0 1=block 1 . . . 255=block 255
2C	byte	Secondary character block
2D	byte	Miscellaneous state information 0-1=all modes on all monitors active 1-1=summing active 2-1=monochrome active 3-1=mode set default palette loading disabled 4-1=cursor emulation active 5-0=background intensity / 1=blinking 6-7=reserved
2E	byte	Reserved
2F	byte	Reserved
30	byte	Reserved
31	byte	Video memory available 0=64KB 1=128KB 2=192KB 3=256KB 4-255=reserved
32	byte	Save pointer state information 0 512 character set active 1 dynamic save area active 2 alpha font override active 3 graphics font override active

offset	type	description
		4 palette override active 5 DCC extension active 6-7 = reserved
33-3F	byte	Reserved

Format of static functionality table:

bit	flags:	0 = not supported 1 = supported

offset	type	description
00	byte	Bit Video modes 0 mode 0 1 mode 1 2 mode 2 3 mode 3 4 mode 4 5 mode 5 6 mode 6 7 mode 7
01	byte	Bit Video modes 0 mode 8 1 mode 9 2 mode A 3 mode B 4 mode C 5 mode D 6 mode E 7 mode F
02	byte	Bit Video modes 0 mode 10 1 mode 11 2 mode 12 3 mode 13 4-7 Reserved

offset	type	description
03-06	byte	Reserved.
07	byte	Bit Scan lines available in text mode 0 200 scan lines 1 350 scan lines 2 400 scan lines 3-7 Reserved
08	byte	Character blocks available in text mode
09	byte	Maximum number of active character blocks in text modes
0A	byte	Bit Miscellaneous functions 0 all modes on all monitors 1 summing 2 character font loading 3 mode set default palette loading 4 cursor emulation 5 EGA palette 6 color palette 7 color paging
0B	byte	Bit Miscellaneous functions 0 light pen 1 save/restore 2 background intensity / blinking control 3 DCC 4-7 Reserved.
0C	byte	Reserved.
0D	byte	Reserved.
0E	byte	Bit Save pointer functions 0 512 character set 1 dynamic save area 2 alpha font override 3 graphics font override 4 palette override 5 DCC extension 6-7 Reserved.
0F	byte	Reserved.

AH = 1C Save/restore video state
AL = 0 Return save/restore state buffer size
Input:
CX = requested states
Output:
AL = 1Ch
BX = # of 64 byte blocks needed for save buffer

AL = 1 Save state
Input:
CX = requested states
ES:BX = pointer to save area
Output:
(ES:BX) area modified
AL = 1Ch

AL = 2 Restore state
Input:
CX = requested states
ES:BX = pointer to save area
Output:
AL = 1Ch
Requested states in CX—defined as follows:
bit 0 = 1—save/restore video hardware state
bit 1 = 1—save/restore video BIOS data area
bit 2 = 1—save/restore video external palette
bits 3-F = reserved.

6.0 ADDENDUM

Micro Channel Registers

Programmable Option Select (POS)—To maintain compatibility with the Micro Channel standard, adapter cards used in PS/2 and compatible computers must contain POS registers 100,101, and 102.

POS 100, 101: Card ID

This is a read-only register.
R/O : I/O address 100-101

Bit	Description
0-7	Value derived from DB⟨7:0⟩ when latched.

This register is accessible only when —CD SETUP is active. Values for bits 0-7 are determined during Power-up/Reset. POS 100 is defined as POS I.D. low; POS 101 as POS I.D. high.

Examples: If DB⟨7:0⟩ = 00h-FEh then POS 100 = 000h-0FEh
POS 101 = 080h

If DB⟨7:0⟩ = FFh then POS 100 = 0FFh
POS 101 = 0FFh

POS 102: Card Enable

This is a read/write register.
R/W : 1/O address 102

Bit	Description
0	Card Enable.
1	I/O wait enable.
2	ROM wait enable.
3	RAM wait enable.
4-7	Reserved.

Bits 0-3 are set to 0 during power-up.

Bit 0 is set to 1 by the system during power-up when an adapter is detected in the system.

6.0 ADDENDUM (Continued)

Bit 1, when set to 1, indicates the implementation of a minimum of onee asynchronous extended cycle (wait state) for the ET4000 I/O.

Bit 2, when set to 1, indicates the implementation of a minimum of one asynchronous extended cycle (wait state), for the ROM BIOS.

Bit 3, when set to 1, indicates the implementation of a minimum of one asynchronous extended cycle (wait state), for video memory.

6.1 ET4000 Revision E

The features and/or instructions contained in this section relate to the ET4000AX Revision E.

Attribute Skew (two-byte character code enable)

In order to enable the use of two-byte character sets, one control bit has been added to Rev. E of the ET4000AX. This is located in ATC Indexed Register 16: Miscellaneous, bit 6 (See P.158). A reserved bit in prior versions, this control bit has been added to enable a 2-byte Character Code (CC) feature. The hardware/software design and programming instructions are as follows:

A) Enable the ATSK bit (attribute skew) to a 1—ATC MISC Index 16 bit 6 (See P.158). **NOTE:** KEY should be "ON" (See P.102 for explanation of KEY). The ATSK bit will be used to compensate the attribute (ATT), Display Enable (DE) and Cursor Skew. Therefore, no external hardware circuit is needed for ATT, DE, and Cursor skew compensation.

B) RAS/CAS timing register (CRTC Indexed Register 32) programmed value = 28h.

C) For the first font fetch (i.e.: RASBL and CASL⟨3:2⟩DRAM access cycle) of each scan line, the MD⟨31:16⟩font data are ignored.

D) The first or subsequent Character Codes (CC0 or CC1, CC2, etc.) should be latched by the external circuit and this Character Code should remain latched until the next font fetch cycle.

E) The second, or odd, Character Code (CC1 or CC3, CC5, etc.) and the previously latched even Character Code (CC0 or CC2, CC4, etc.) total of 16-bit Character Codes should be latched at the beginning of every even font fetch cycle via transparent latches.

6.1 ET4000 Revision E (Continued)

F) If the current CCn is not an English character, then the font data (MD⟨31:16⟩) will be fetched according to the 16-bit Character Code (i.e., the external EPROMs are enabled), else the DRAMs font (which contains the VGA's font) are enabled.

G) If the last character font of the scan line is a 24-bit wide font and begins at an odd column, then only half of the font (12-dot) will be displayed.

I/O Decoding

I/O decoding has changed with the ET4000 Rev. E from 10 bits (A⟨9:0⟩) to 16 bits (⟨15:0⟩). The exception is in decoding the Video Subsystem Register, port address 46E8. For this register, I/O decoding is 12 bits (A⟨11:0⟩).

Electrical Specifications—See P.51

Voltages changes are applicable to the following:

Minimum I(OL) for CASL⟨3:0⟩ is 6mA.
Minimum I(OL) for MWAL, MWBL is 8mA.
Minimum I(OL) for MD⟨31:0⟩ is 4mA.

TS Indexed Register 7—See P.143

A new bit, bit 4, is added in Timing Sequencer Indexed Register 7: TS Auxiliary Mode. This bit is used to eliminate possible corruption of video memory when other bits, explained in the register description, are set in certain ways relative to each other.

Timing Specification—See P.56, DRAM/VRAM Memory Timing

The memory data and address set up time has been adjusted from the half-clock to the beginning of SCLK. The improved times are indicated in the following:

No.	Symbol	Description	min.	max.	unit
122	ts(ASR)	AA,AB Address RAS set up time	c+16.5	c+17.5	ns(*5)
123	ts(ASC)	AA,AB Address CAS set up time	c− 8.5	c− 6.0	ns(*5)
124	ts(DS)	Memory Write Data set up time	9.5	14.5	ns(*1)

Timing Specification

ET4000AX Rev. E RAS addresses (No. 130) hold time have been reduced from n=2 to n=1 to improve external font access (Section 2.3.1 Timing Specification P.56)

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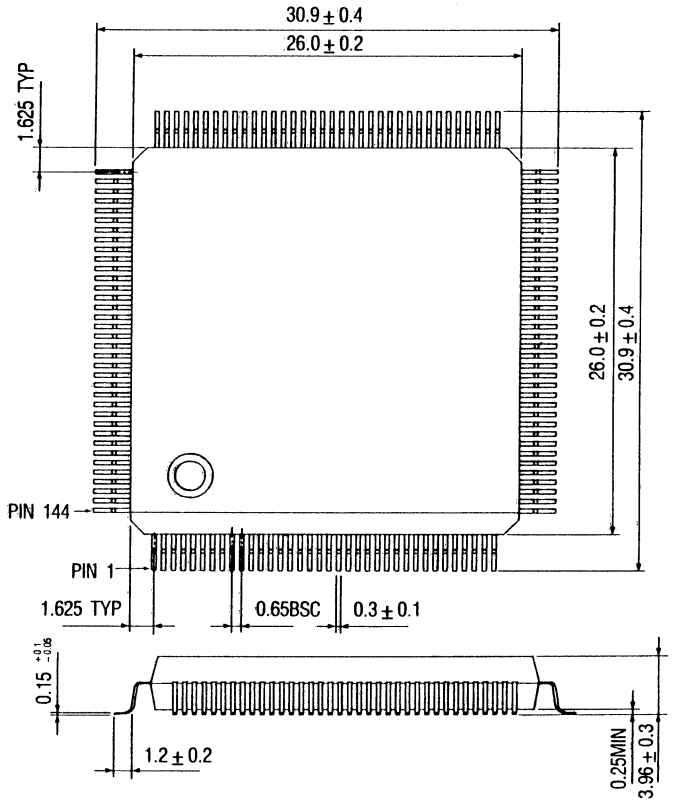
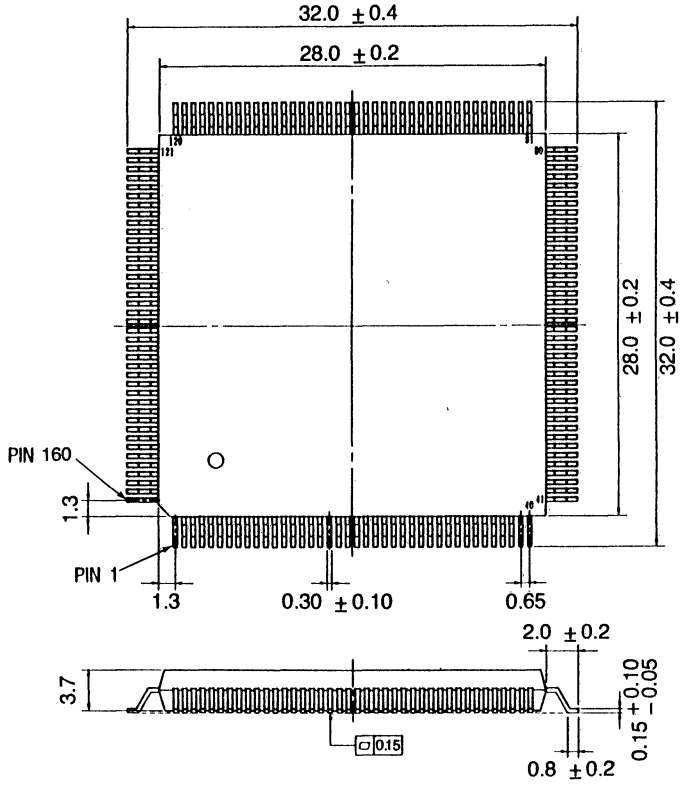
MECHNICAL SPECIFICATIONS

ET4000 - 144-Pin Plastic Flat Package



MECHANICAL SPECIFICATIONS

ET4000 - 160-Pin Plastic Flat Package



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