UMC

UM82C232
Data Buffer

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1. General Description:

The UM 82C232 is a data buffer. It is an interface between CPU data bus, system data bus and peripheral data bus.

2. Features:

- 16-bit data bus buffer
- 16-bit or 8 bit data bus buffer for PC/AT bus
- 8-bit I/O port data bus buffer
- Word swap logic
- Advanced 1.2μ mCMOS Techonoloy
- 100 pin Flat Package

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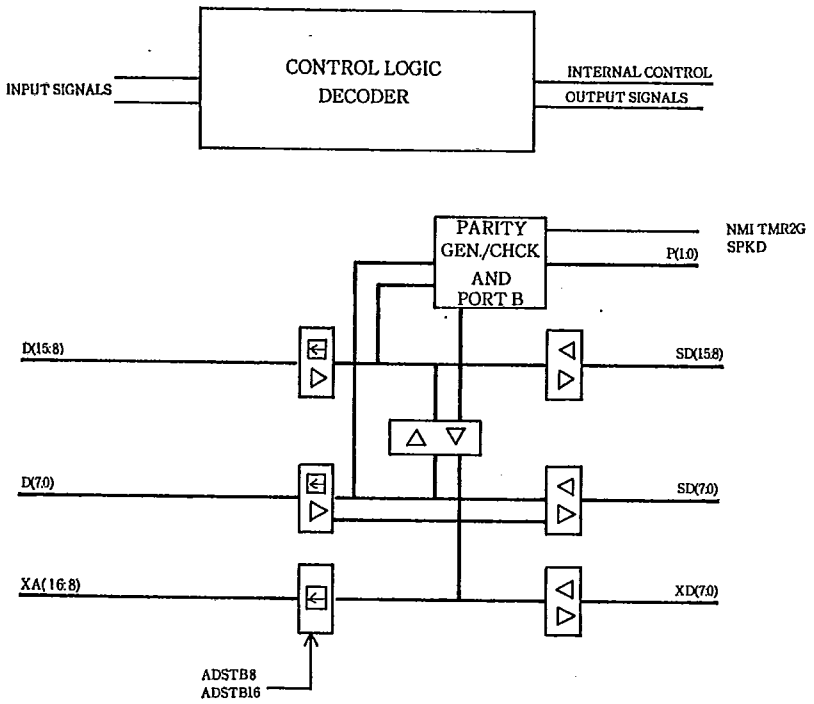
3. UM82C232 Block Diagram



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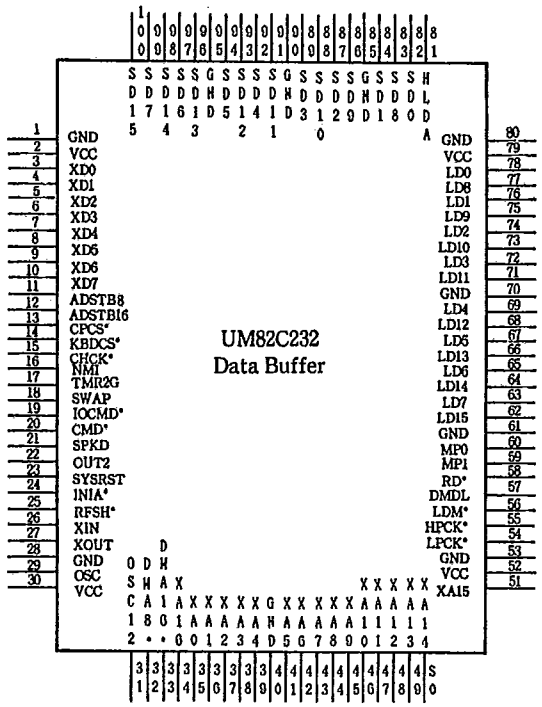
4.UM82C232 Pin Configuration



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5. Functional Description

5.1 Data Buffers and Latches

The UM82C232 provides the buffering between the CPU data bus and the AT data bus. The D(15:0) has 6ma driving capability. The SD(15:0) can drive the AT data bus directly because of 24ma driving capability. The UM82C232 also latches the read data from the SD bus during CPU AT cycles. This causes the bus conversion cycle and READ to command to terminate earlier than the CPU sampling data.

The latch enable signals for read data from SD(15:0) are controlled by the CMD* and SWAP signals.

The direction of the data buffers is determined by the RD*, LDM*, HLDA, DMA8* and DMA16* signals. Also, the D(15:0) are forced to become input when 80287 is accessed.

5.2 Bus Swapping Circuit

The UM82C232 supports data swapping when the 80286 reads from or writes to 8-bit devices. It also supports the high byte and low byte transition between SD bus during 8-bit DMA cycles.

The following table describes the bus transitions:

SWAP	LDM*	CYCLES	OPERATION
0	1	CPU	D(15:0)←→SD(15:0)
1	1	CPU	D(15:8)←→SD(7:0)
x	0	16-bit DMA or MASTER	D(15:0)←→SD(15:0)
0	0	8-bit DMA	D(15:0)←→SD(15:0)
1	0	8-bit DMA	D(15:8)←→SD(7:0)
1	1	8-bit DMA	D(15:8)←→SD(7:0)

5.3 Parity Generation and Checking

The UM82C232 generates an even parity bit for each two bytes during local DRAM write cycles.

During a local DRAM read cycle, the UM82C232 latches the read data and performs parity checking. If a parity error is detected, parity checking function is enabled and if NMI is not being masked, NMI will be activated.

5.4 Port B register

The UM82C232 contains a register as Port B designed for the PC/AT as shown in the following table.

Bit	R/W	Description
7	R	Local DRAM parity error status
6	R	AT bus channel check active status
5	R	Timer 2 out
4	R	Refresh toggle bit
3	R/W	Enable channel check function
2	R/W	Enable Local DRAM parity checking
1	R/W	Enable speaker
0	R/W	Timer 2 gate

5.5 NMI Generation

The NMI generation can be turned on or off through writing IOP 70 with data bit 7 equal to 0 or 1.

If NMI is not masked and parity checking and channel check function are enabled, a parity error or activated CHCK* will initiate NMI.

5.6 DMA address latch

By using ADSTB8 or ADSTB16 to latch XD(7:0), the 8-bit DMA's XA(15:8) or 16-bit DMA's XA(16:9) are latched and driven by the 82C232. The XA14 and XA15 have 24 ma driving capability.

5.7 Miscellaneous decode signals

The UM82C232 provides two decode signals,

- KBDCS* for keyboard controller
- CPCS* for co-processor

6. Pins Description

Pin Name	Pin Type	Pin No.	Description
XIN	I	26	14.3MHZ osc. input
XOUT	O	27	14.3MHZ osc. output
OSC	O	30	14.3818MHZ clock output
OSC/12	O	31	1.19MHZ clock output
D(15:0)	B	62, 64, 66, 68, 71, 73, 75, 77, 63, 65, 67, 69, 72,74,76, 78	Local data bus to/from CPU
SD(15:0)	B	100,98, 96, 93, 91, 88, 86, 83, 99, 97, 94, 92, 98,87, 84,82	AT data bus; these pins have 24 ma current sinking capability which attached to AT data bus directly.
XD(7:0)	B	10,9,8, 7,6, 5, 4,3	System board peripheral data bus.
INTA*	B	24	Interrupt acknowledge signal from 82C231; which is used to direct the interrupt vector data flow from 82C206 to CPU
MP(1:0)	B	59,60	Local DRAM parity bits; they are outputs for write cycle and become inputs during read cycle.
LDM*	I	56	Local memory accessed indication; used by 82C232 to control the data buffers enable.
HPCK*	I	55	High byte parity checking enable; used to determine if high byte parity checking is requited.

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Pin Name	Pin Type	Pin No.	Description
LPCK*	I	54	Low byte parity checking enable; used to determine if Low byte parity checking is required.
DMDL	I	57	Local DRAM read data latch enable; used to latch the read data from DRAM for parity checking.
RD*	I	58	Read cycle status from 82C231; used to control the data flow direction.
SWAP	I	18	High byte data and low byte data control from 82C231; used to control the data flow direction.
CMD*	I	20	Read or write command during CPU AT cycle or MASTER cycle; used to enable the data latches inside the BUFFER.
IOCMD*	I	19	IO read or write command during CPU AT cycle or MASTER cycle ; used with RD* signal to access the IO registers inside the 82C232.
HLDA	I	81	Hold acknowledge signal from CPU to distiquish the CPU cycle and non-CPU cycle.
RFSH*	I	25	Refresh cycle indication.
ADSTB8	I	11	8-bit DMA transfer address strobe; used to latch the XD(7:0) and generate XA(15:8) during 8-bit DMA cycle.
ADSTB16	I	12	16-bit DMA transfer address strobe; used to latch the XD(7: 0) and generate XA(16:9) during 16-bit DMA cycle.
DMA8*	I	32	8-bit DMA cycle indication; used to control the data flow directions.
DMA16*	I	33	16-bit DMA cycle indication; used to control the data flow directions.

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Pin Name	Pin Type	Pin No.	Description
XA16	TO	34	System board peripheral address bus bit 16; this signal is enabled only during 16-bit DMA cycle.
XA(15:8)	B	51,50,49 48, 47,46 45,44	System board peripheral address bus bit 15 - bit 8; normally they are inputs and become outputs during DMA cycle.
XA(7:0)	I	43,42,41 39, 38,37 36,35	System board peripheral address bus bit 7 - bit 0.
CHCK*	I	15	Channel check signal from AT bus; an activated CHCK* monitored by 82C232, NMI will be issued.
NMI	O	16	Non-maskable interrupt to CPU; parity error for the data read from loacl DRAM or CHCK* activated by the channel adaptors will force 82C232 issue NMI if is is programmed to do so.
OUT2	I	22	Timer 2 output from 82C206; used to generate speaker data update IOP 61 contents.
TMR2G	O	17	Timer 2 gate control.
SPKD	O	21	Speaker data; to drive speaker.
KBDCS*	O	14	Keyboard controller chip select; decode through XA bus.
SYSRST	I	23	System reset from 82C231.
CPCS*	O	13	Co-processor chip select; decode through XA bus.
VCC		2,29,52 79	
GND		1,28,40 43, 61,70 80,85, 90 95	
Total pins		100	

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7. Electrical Characteristics (Vcc=4.75~5.25V, TA=0°C-70°C)

7.1 DC Characteristics

Parameters	Symbol	Min.	Max.	Units
Input Low Voltage	Vil	-	0.8	V
Input High Voltage	Vih	2.0	-	V
Output Low Voltage	Vol	-	0.45	V
Output High Voltage	Voh	2.4V	-	V
Input Current	Iil	-	+- 10	ua
Power Supply Current	Icc	-	100-	ma
Output High-Z Current	Ioz	-	+- 10	ua
Standby Power Supply Current	Iccsb	-	1	ma

7.2 AC Characteristics

(Ta = 0 to 70 degree c, Vcc = 5V +- 5%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
t1	D(15:0) to SD(15:0) valid delay	11	21	30	ns	150PF
t2	D(15:0) to XD(7:0) valid delay	10	20	29	ns	75PF
t3	D(15:0) to P(1:0) valid delay	13	22	31	ns	75PF
t4	SD(15:0) to D(15:0) valid delay	9	18	28	ns	75PF
t5	SD(15:0) to XD(7:0) valid delay	9	18	28	ns	75PF
t6	SD(15:0) to P(1:0) valid delay	13	22	31	ns	75PF
t7	D(15: 0) setup time related to DMDL	0	3	5	ns	75PF
t8	D(15: 0) hold time related to DMDL	0	1	2	ns	75PF
t9	SD(15: 0) setup time related to CMD*	0	4	5.5	ns	150PF
t10	SD(15: 0) hold time related to CMD*	0	1	2	ns	150PF
t11	XD(7: 0) setup time related to CMD*	0	4	6	ns	75PF
t12	XD(7: 0) hold time related to CMD*	0	1	2	ns	75PF
t13	SD(7: 0) to SD(15: 8) delay after SWAP active	8	15	25	ns	150PF
t14	SD(7:0) to SD(15:8) invalid delay after SWAP inactive	3	9	18	ns	150PF
t15	P(1: 0) setup time related to DMDL	1	3	5	ns	75PF

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Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
t16	P(1:0) hold time related to DMDL	0	1	2	ns	75PF
t17	CHCK* active to NMI active delay	3	10	18	ns	50PF
t18	HPCK* or LPCK* active to NMI active delay if parity error	8	15	23	ns	50PF
t19	XA valid to DBDCS* valid delay	10	21	32	ns	50PF
t20	XA valid to CPCS* valid delay	9	20	30	ns	50PF
t21	ADSTB8 or ADSTB16 active to XA valid during DMA cycle	10	18	28	ns	75PF
t22	SD, XD buses tri-stated after RD* invalid	5	10	20	ns	75PF
t23	SD, XD buses driven after RD* valid	6	11	15	ns	75PF
t24	D bus driven after RD* valid LDM* invalid	7	11	15	ns	75PF
t25	D bus tri-stated after RD* invalid	7	11	15	ns	75PF
t26	SD(15:8) to SD(7:0) delay after SWAP active	7	15	20	na	150PF
t27	SD(15:8) to SD(7:0) invalid delay after SWAP inactive	3	9	18	ns	150PF

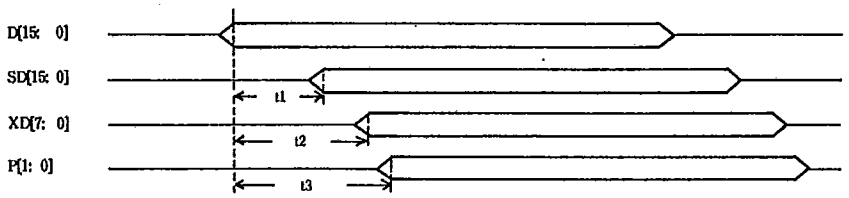

Fig.1 D[15:0] TO SD[15:0] AND P[1:0] DELAY

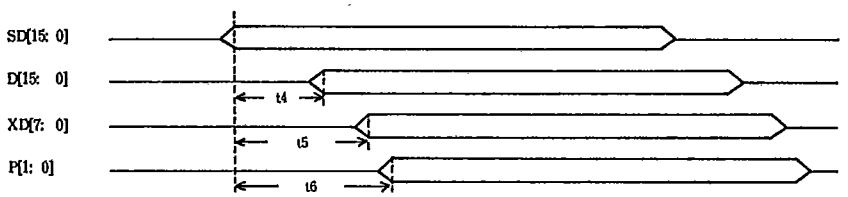

Fig.2 D[15:0] TO SD[15:0] AND P[1:0] DELAY

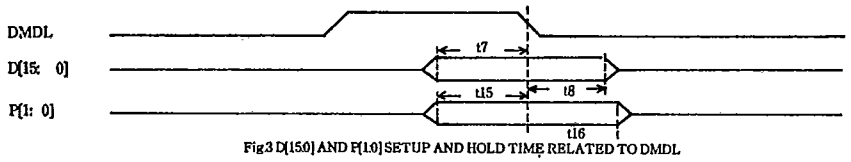

Fig.3 D[15:0] AND P[1:0] SETUP AND HOLD TIME RELATED TO DMDL

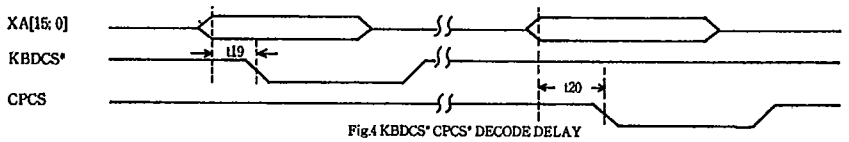

Fig.4 KBDCS* CPCS* DECODE DELAY

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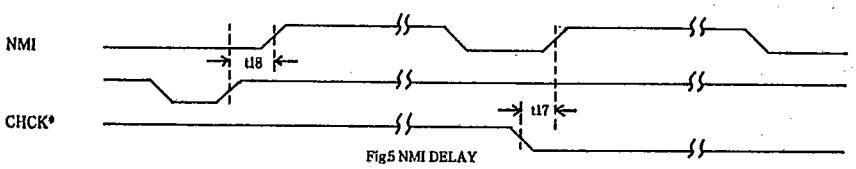

Fig5 NMI DELAY

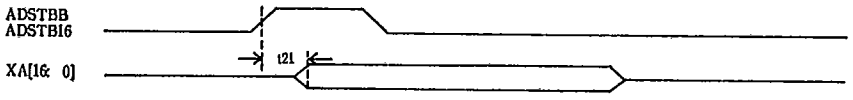

Fig6 XA DELAY DURING DMA

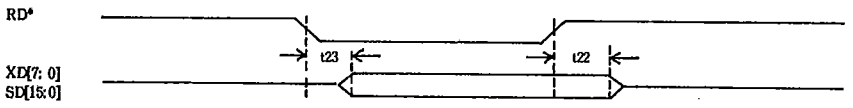

Fig.7

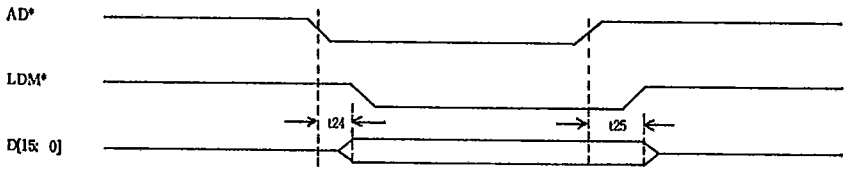

Fig.8

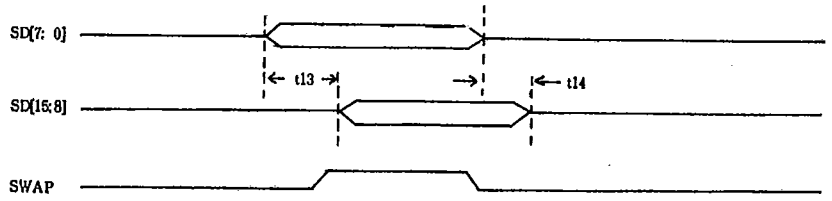

Fig. 9 BUS SWAP

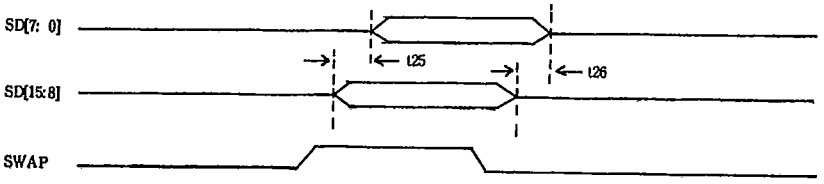

Fig. 10 BUS SWAP

PC Mainboard