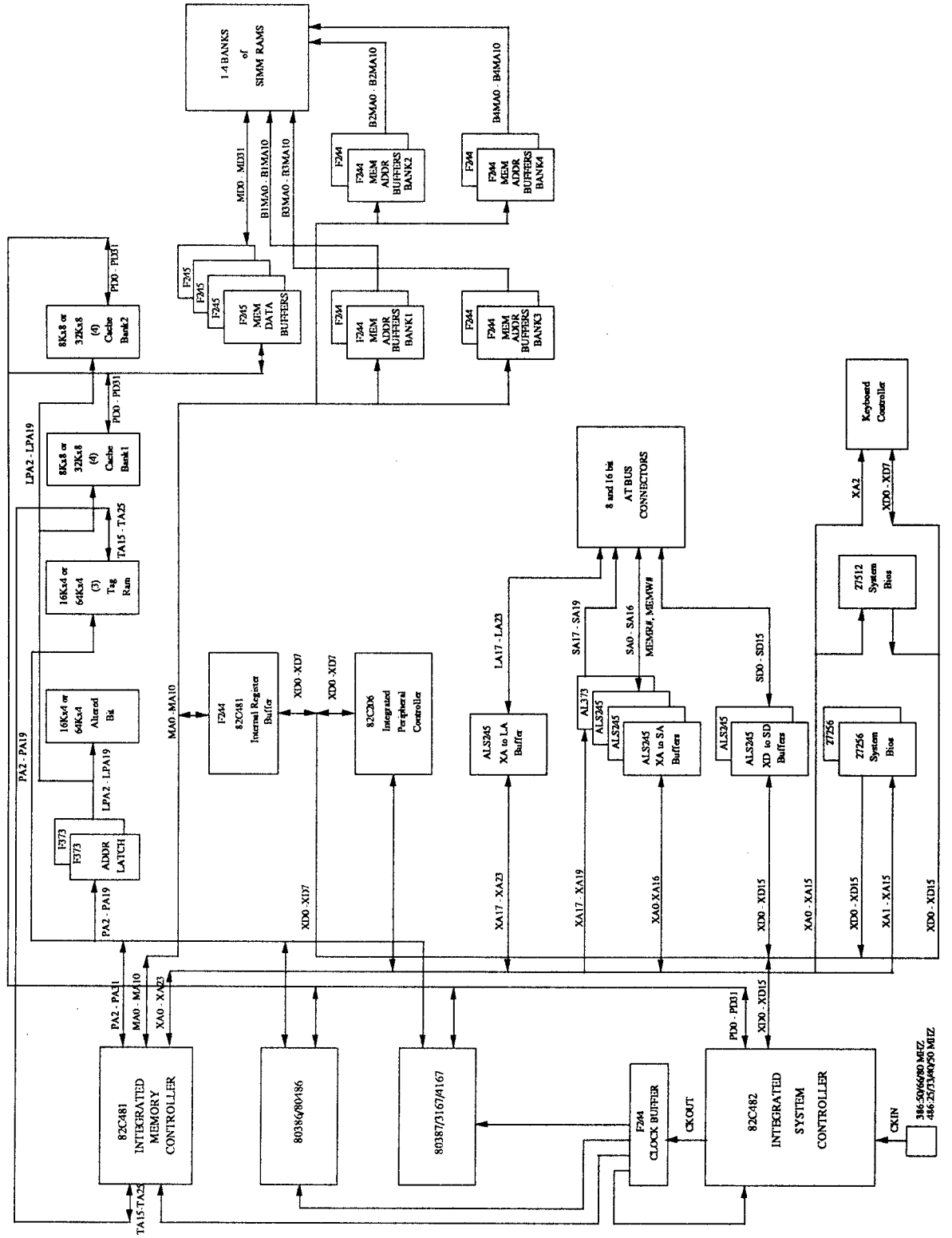
I General Description

The UM82C480 is a highly integrated, IBM PC/AT compatible chip set for high performance 80386/80486 based personal computer systems. Built with exquisite cache controller in advanced 1.0μm CMOS technology, UM82C481 (Integrated Memory Controller, IMC), UM82C482 (Integrated System Controller, ISC), with UM82C206 (Integrated Peripheral Controller, IPC), and limited counts of commercial parts constitute a low cost, highly reliable, full advanced feature personal computer system.

II Features

* 100% IBM PC/AT compatible
* Support 80386 CPU running at 25/33/40 MHz
* Support 80486 CPU running at 25/33/40/50 MHz in 1X clock
* Support Intel 80387 / Weitek 3167 / Weitek 4167 Floating Point Coprocessors
* Built-in cache controller:
  - Direct-mapped organization with write-back operation
  - 0 wait state for cache hit
  - Flexible cache size: 32/64/128/256/512/1024 KB
  - Hidden DRAM refresh to boost system performance
  - Built-in registers to support three independent non-cacheable regions
  - Support cache line fill as well as 80486 burst mode
  - Support Automatic Memory Size Detection
* Sophisticated DRAM controller:
  - Support Fast/Standard page mode
  - Support 4 banks CPU speed DRAM with memory size up to 64MB
  - Support mixable 256Kx9, 1Mx9, 4Mx9 DRAM modules
  - Programmable DRAM wait states
  - Suppport 256KB or 384KB (A to F segments of first 1MB) relocation to the top of DRAM
    memory
* Support sophisticated Shadow RAM for video and system BIOS (C, D, E, F segments)
* Support fast GATE A20 and fast CPU RESET to optimize OS/2 operations
* Synchronous AT bus clock with programmable clock (divided by 2, 3, 4, 5, 6)
* Programmable CPU clock (divided by 1, 2, 3, 4)
* Support 256KB/512KB/1MB EPROMs with single or double EPROM BIOS configura-



SYSTEM BLOCK DIAGRAM FOR UM82C480 386/486 PC/AT CHIPSET

III Required IC List for 64KB cache systems

PART NO.	DESCRIPTIONS	80386-33	80486-33
UM82C481	IMC	1	1
UM82C482	ISC	1	1
UM82C206	IPC	1	1
UM6164K-25L	8K X 8-25 SRAM	8	8
UM61416K-20L	16K X 4-20 SRAM	4	4
27512	BIOS EPROM	1	1
8742	KEYBOARD CONTROLLER	1	1
74F244	TTL	6	6
74F245	TTL	7	7
74F373	TTL	2	2
74ALS245	TTL	4	4
74ALS373	TTL	1	1
74F74	TTL	3	2
74F04	TTL	1	1
74ALS00	TTL	0	1
7406	TTL	1	1
74F32	TTL	1	1
14069A	TTL	1	1
16R6	PAL	0	1
80386-33	CPU	1	0
80486-33	CPU	0	1

IV CHIP SET PERFORMANCE

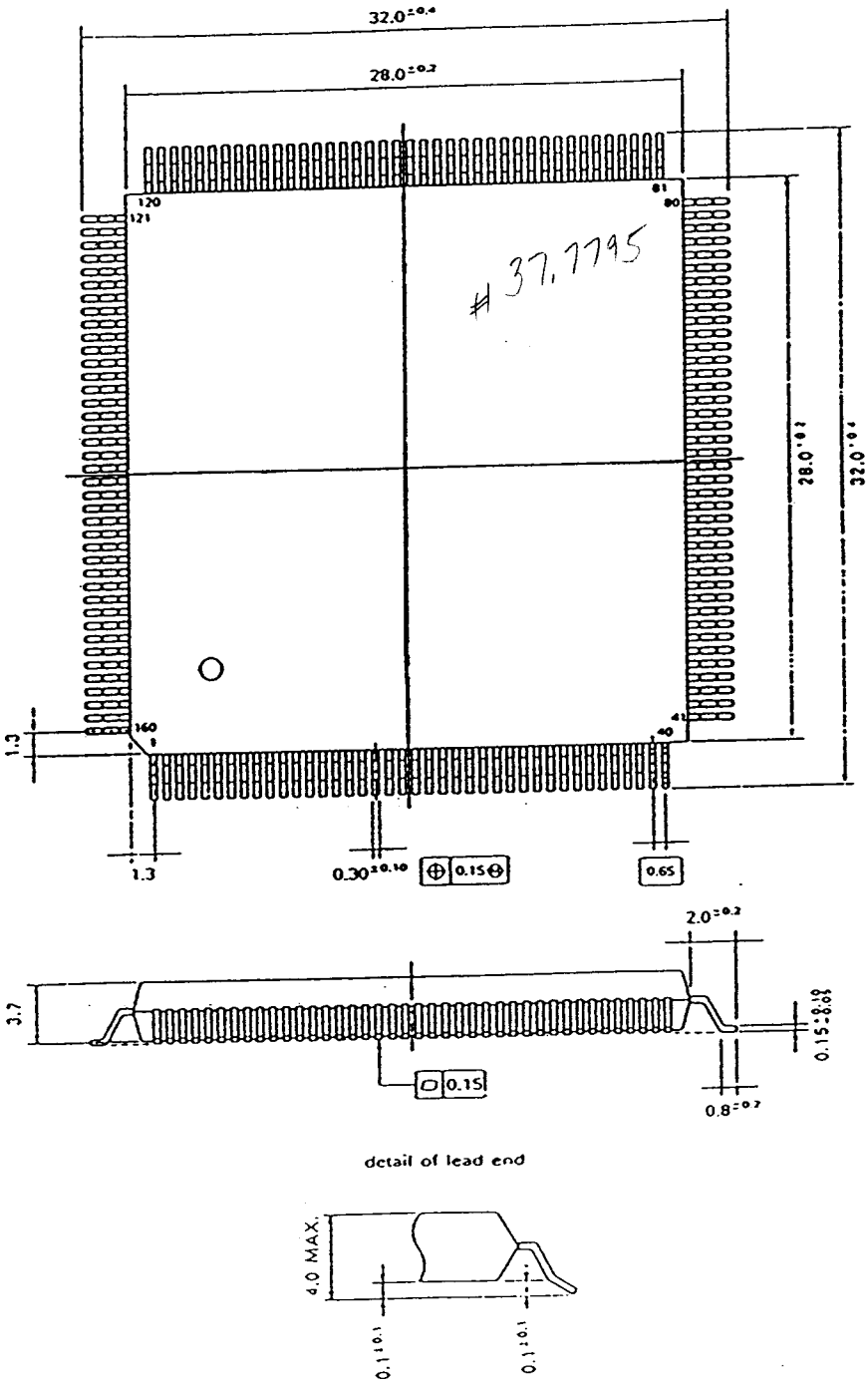
Mode	Landmark (V 1.14)	Power Meter (V 1.5)
386-25	41.0 MHz	6.246 MIPS
386-33	54.3 MHz	8.240 MIPS
386-40**	65.7 MHz	9.842 MIPS
486-25	114.1 MHz	11.232 MIPS
486-33	150.7 MHz	14.849 MIPS
486-40**	182.3 MHz	17.961 MIPS
486-50**	230.0 MHz*	22.399 MIPS

* Estimated value, performance over Landmark measure scale.
** Using 33MHz CPU

PACKAGE INFORMATION (UM82C481 / UM82C482)

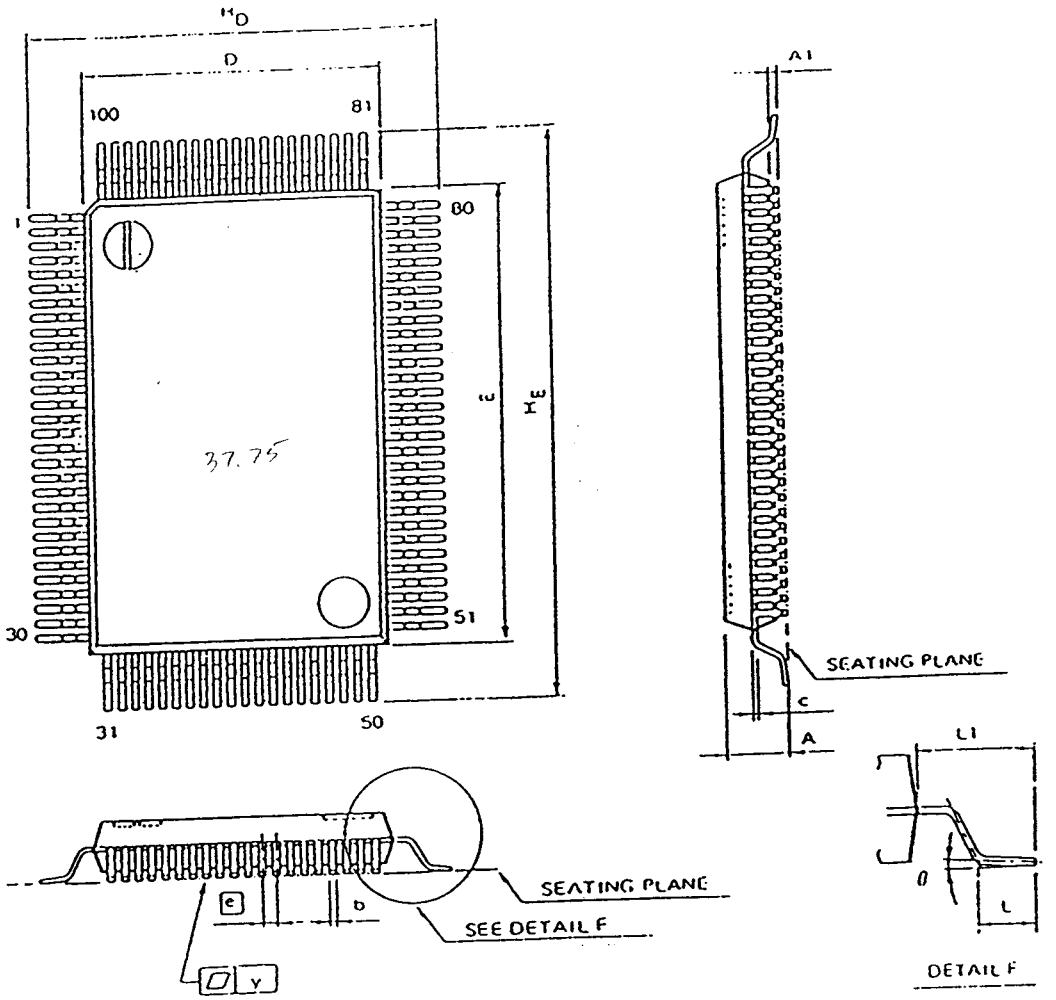
160 pin QFP

unit: mm



PACKAGE INFORMATION (UM82C206)

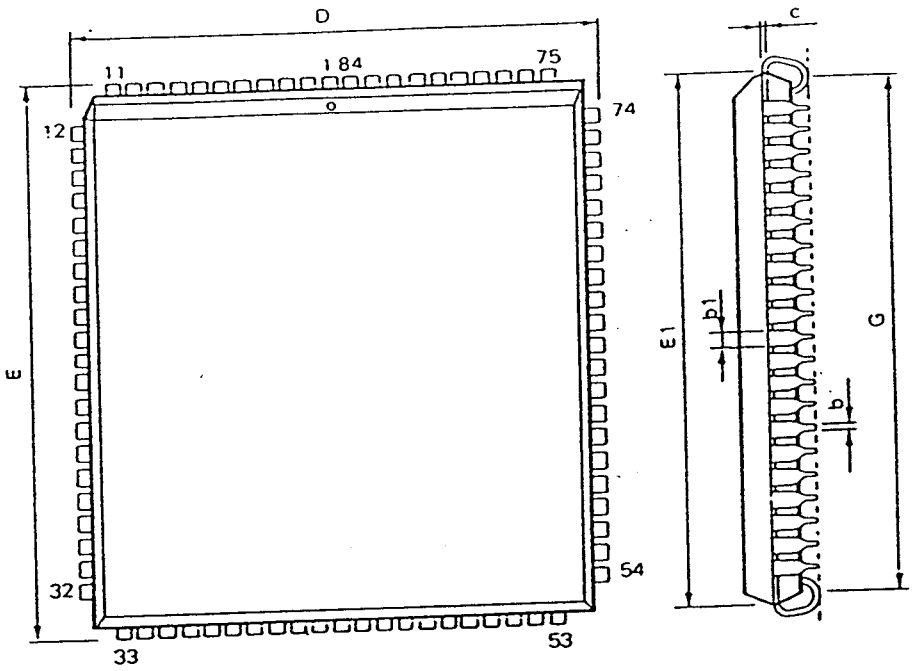
QFP 100L Outline Dimension

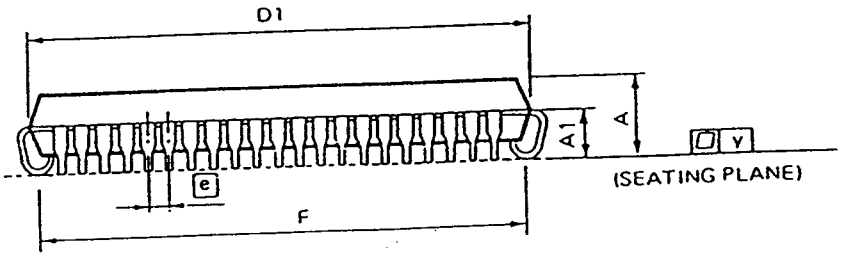


Symbol	Dimensions in inch	Dimensions in mm
A	0.120 ± 0.010	3.048 ± 0.254
A1	0.008 ± 0.004	0.203 ± 0.102
b	$0.012^{+0.004}_{-0.002}$	$0.305^{+0.102}_{-0.051}$
c	$0.006^{+0.004}_{-0.002}$	$0.152^{+0.102}_{-0.051}$
D	0.551 (0.576 Max.)	14.000 (14.630 Max.)
E	0.787 (0.812 Max.)	20.000 (20.625 Max.)
[e]	0.026 ± 0.006	0.650 ± 0.152
H_D	0.740 ± 0.012	18.796 ± 0.305
H_E	0.976 ± 0.012	24.790 ± 0.305
L	0.047 ± 0.012	1.194 ± 0.305
L1	0.095 ± 0.012	2.413 ± 0.305
Y	0.006 Max	0.152 Max.
θ	0° ~ 9°	0° ~ 5°

PACKAGE INFORMATION (UM82C206)

PLCC 84L Outline Dimension





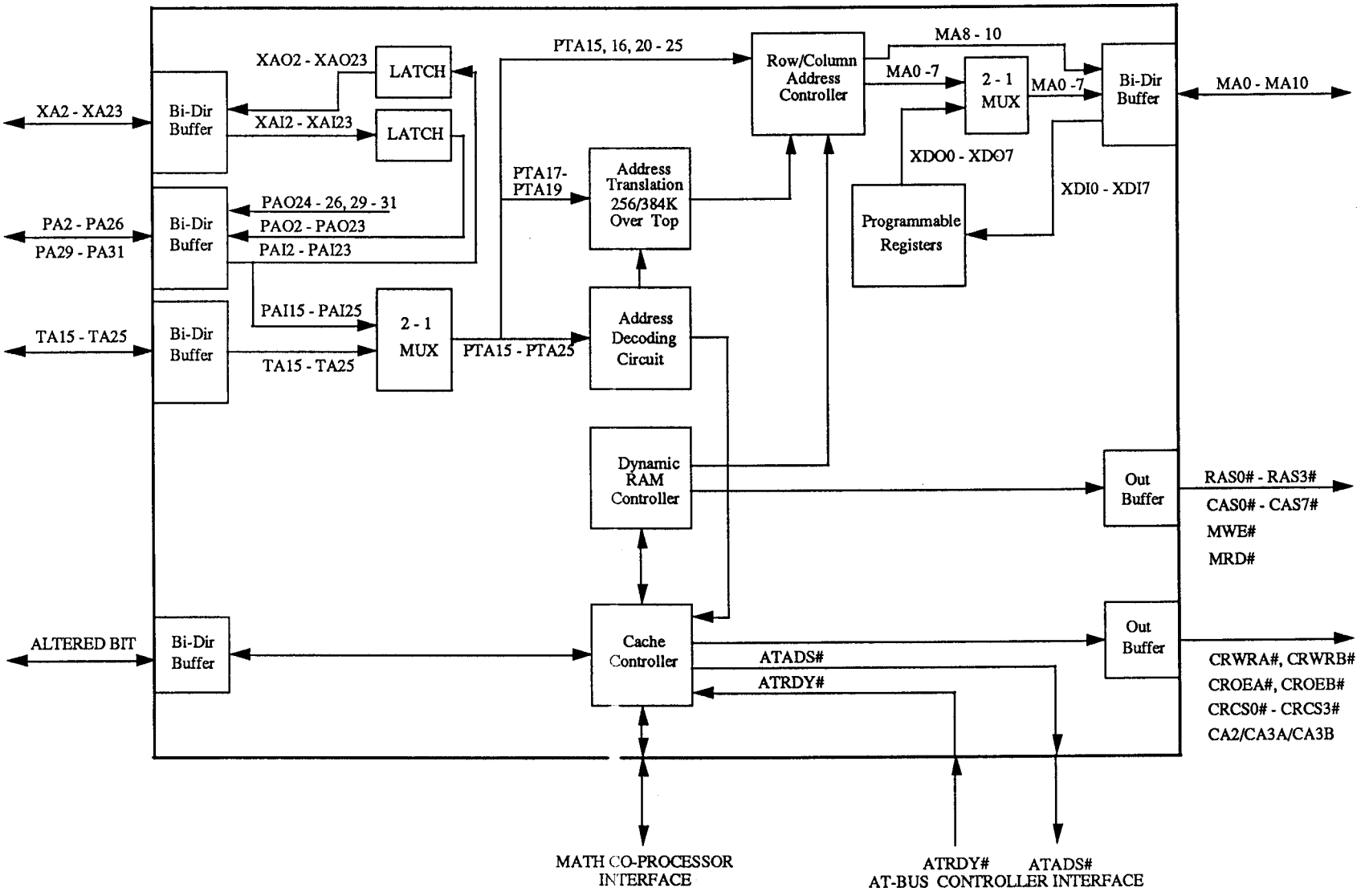
Symbol	Dimensions in inch	Dimensions in mm
A	0.170 ± 0.008	4.318 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
b1	$0.028^{+0.004}_{-0.002}$	$0.711^{+0.102}_{-0.051}$
c	$0.008^{+0.004}_{-0.002}$	$0.203^{+0.102}_{-0.051}$
D	1.190 ± 0.005	30.226 ± 0.127
D1	1.153 (1.185 Max.)	29.286 (30.099 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	1.190 ± 0.005	30.226 ± 0.127
E1	1.163 (1.185 Max.)	29.286 (30.099 Max.)
F	1.117 ± 0.020	28.372 ± 0.508
G	1.117 ± 0.020	28.372 ± 0.508
y	0.006 Max.	0.152 Max.

I General Description

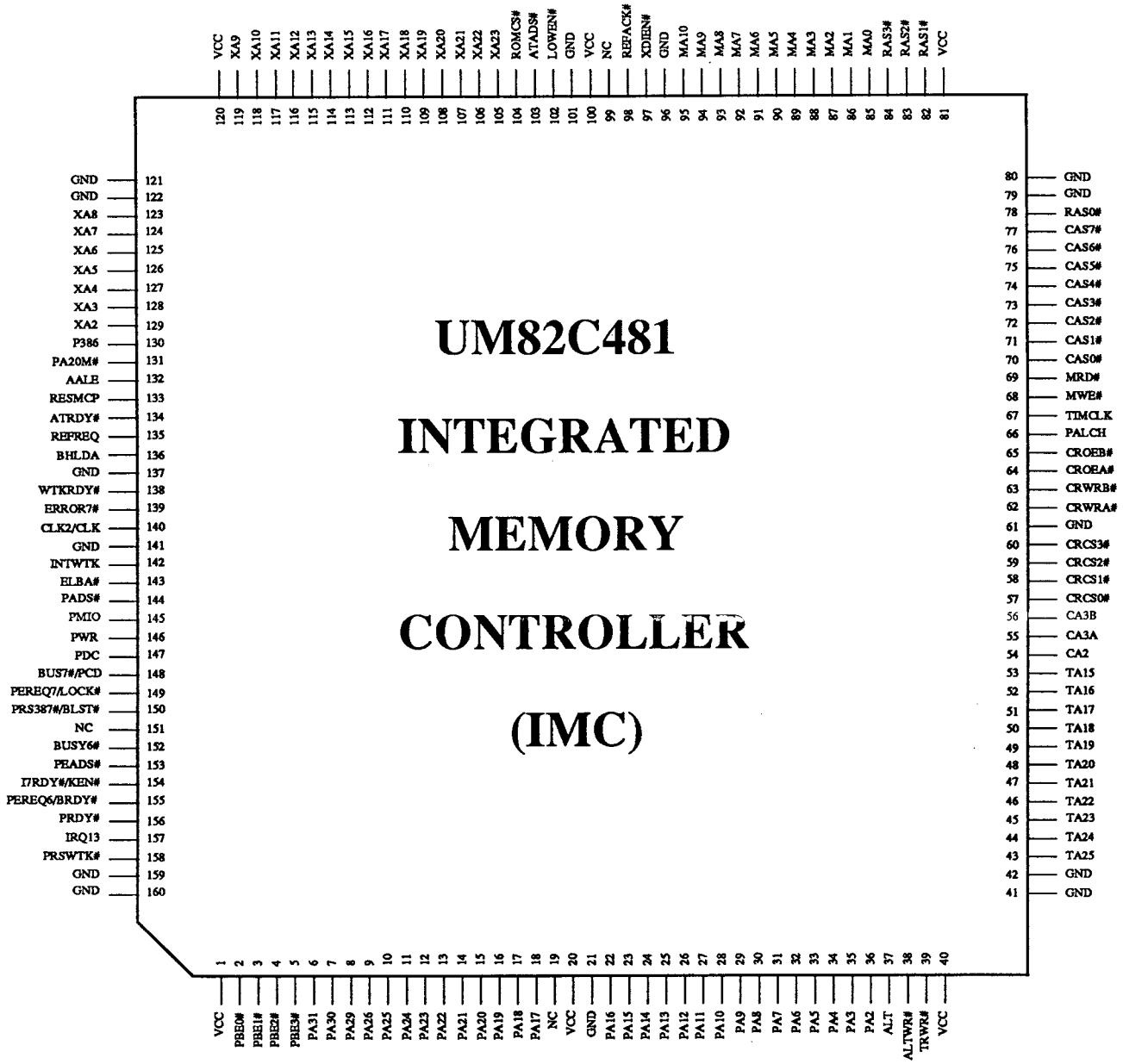
The UM82C481, Integrated Memory Controller (IMC), is part of UMC's high performance 80386/ 80486 PC/AT chip set. It contains sophisticated direct-mapped cache controller with write back operation, and fast page mode DRAM controller. Incorporated with UM82C482, Integrated System Controller (ISC), and UM82C206, Integrated Peripheral Controller (IPC), IMC provides main memory management function for the PC/AT computer system.

II Features

* Built-in cache controller:
  - Direct-mapped organization with write-back operation
  - Cache controller can be enabled/disabled
  - 0 wait state for cache read/write hit if CPU is 80386
  - Programmable 80486 read hit wait state for burst mode
  - Programmable 80486 write hit wait state
  - Programmable cache line size (4/8/16 bytes) if CPU is 80386
  - Flexible cache size: 32/64/128/256/512/1024 KB
  - Support interleaved cache RAM for high speed CPU
  - Hidden DRAM refresh to boost system performance
  - Support Local Bus Access cycles
  - Support three independent non-cacheable regions
  - Video and System BIOS can be cacheable/non-cacheable, write-protected shadow RAM (16 KB resolution for C and D segments)
  - Support fast GATE A20 to optimize OS/2 operations
* Support directly Intel 80387 / Weitek 3167 / Weitek 4167 Floating Point Coprocessors
* Sophisticated DRAM controller:
  - Support Fast/Standard page mode DRAM
  - Support 4 banks of CPU speed DRAM with memory size up to 64 MB
  - Support mixable 256Kx9, 1Mx9, 4Mx9 modules
  - Programmable DRAM wait states
  - Support 256KB or 384KB (A to F segments of first 1MB) relocation to the top of DRAM memory
  - Support Automatic Memory Size Detection
* 1.0μm low-power, high-speed CMOS technology in 160 QFP package



UM82C481 INTEGRATED MEMORY CONTROLLER BLOCK DIAGRAM



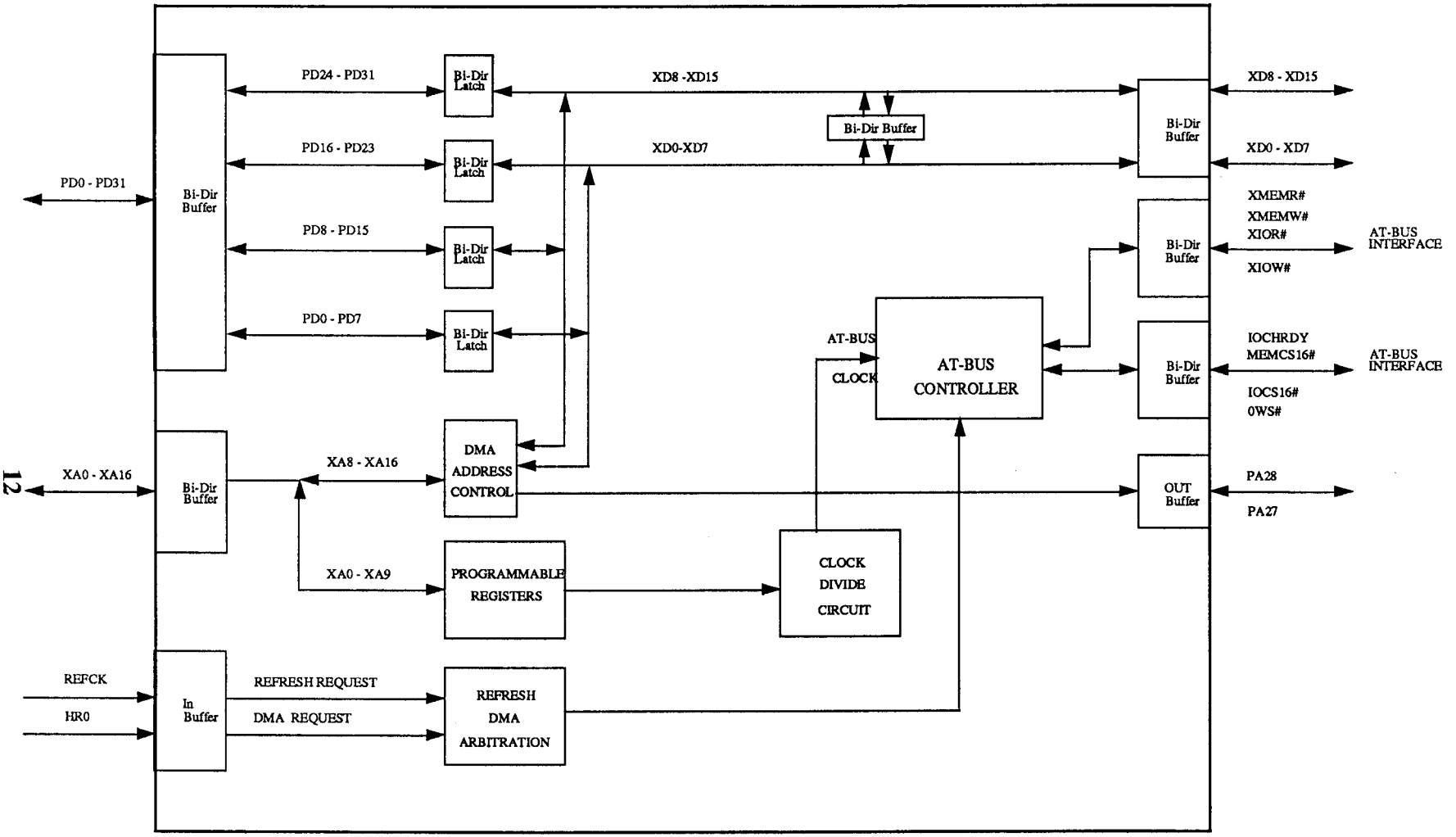
Pin Assignment of UM82C481

I General Description

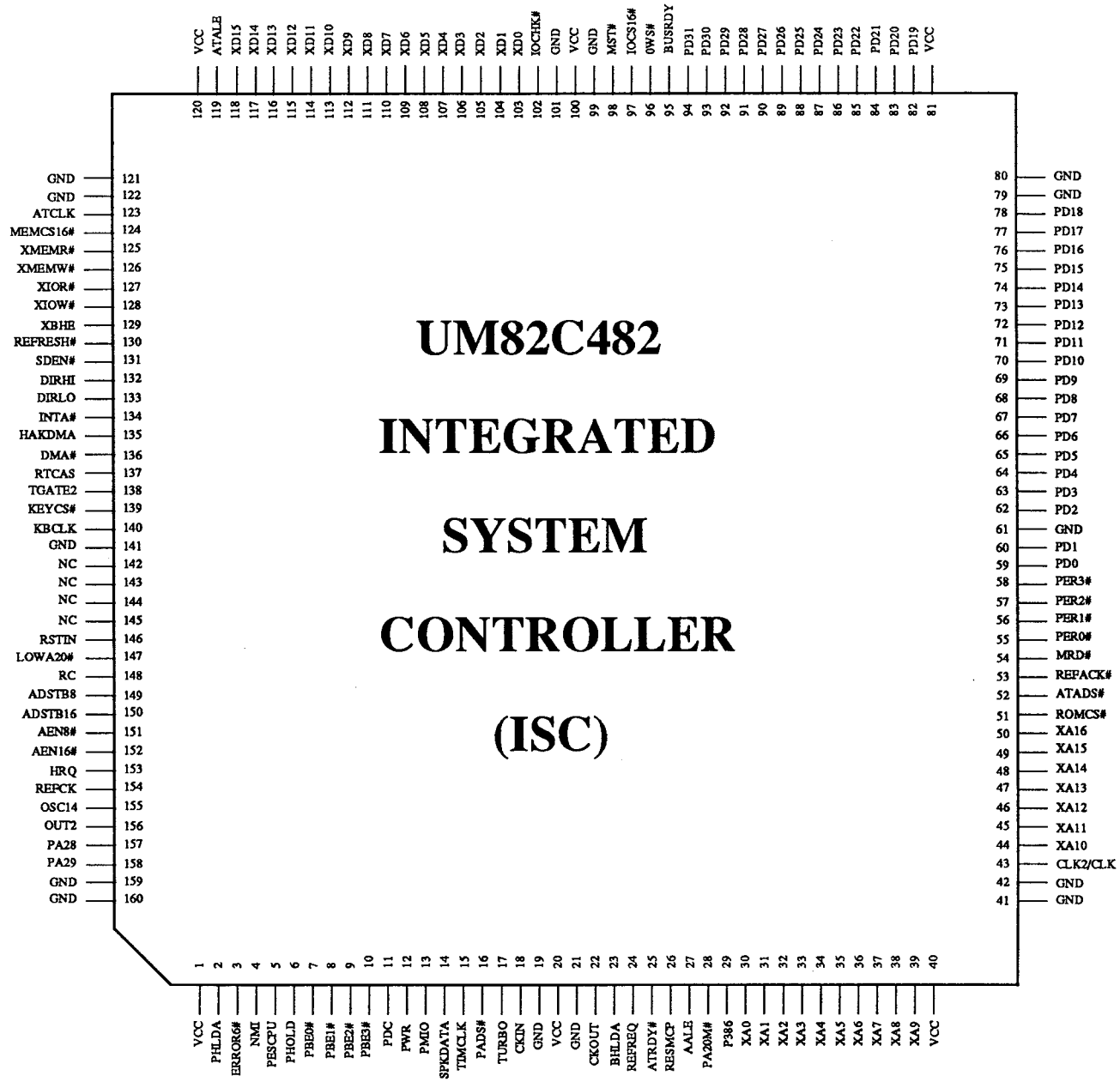
The UM82C482, Integrated System Controller (ISC), is part of UMC's high performance 80386/80486 PC/AT chip set. It contains AT bus control logic, data bus conversion logic, CPU reset logic, clock generation for CPU, keyboard and timer, DMA/refresh logic and peripheral interface logic. Incorporated with UM82C481, Integrated Memory Controller (IMC), and UM82C206, Integraged Peripheral Controller (IPC), ISC provides system control functions for overall PC/AT computer ystem.

II Features

* Interface logic for 80386 and 80486 CPUs
* Feedback CPU clock to reduce clock skew and to increase system stability
* Use 1X clock in 80486 mode to ease system design
* Synchronous AT bus clock with programmable CPU clock (divided by 2, 3, 4, 5, 6)
* Programmable CPU clock (divided by 1, 2, 3, 4)
* Programmable keyboard clock (divided by 1.5, 2)
* Separate DMA and refresh request to perform hidden refresh
* DMA interface logic, refresh address counter and control logic
* Fast CPU reset and GATE A20 to optimize OS/2 operations
* Data bus conversion logic between PD and XD buses
* Parity generation and checking logic
* Support 256KB/512KB/1MB EPROMs with single or double EPROM BIOS configuration
* 1.0μm low-power, high-speed CMOS technology in 160 QFP package



UM82C482 INTERGRATED SYSTEM CONTROLLER BLOCK DIAGRAM



Pin Assignment of UM82C482