SYSTEMS LOGIC/PERIPHERAL

WD6010

DMA and Arbitration Control Device

12

WESTERN DIGITAL

TABLE OF CONTENTS

12

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

As part of the Western Digital® Micro Channel compatible chip sets (WD6500, WD6400SX, WD6400SX/LP), the WD6010 DMA and Arbitration Control Device significantly facilitates the design and implementation of system boards compatible with IBM's Micro Channel architecture. It decreases design complexity and saves space by combining the functions of many discrete arrays and components, while reducing system cost and increasing system reliability.

The Extended Setup Facility is a Western Digital enhancement, designed to allow more functionality such as a Winchester Controller, LAN Adapter or additional serial port to be added onto the system board. It provides product differentiation at the system level and helps hold down costs. Figure 1 illustrates a typical system using Western Digital's Micro Channel compatible chip sets. Devices with bold outlines are available from Western Digital.

1.1 Features

- Completely compatible with the IBM Personal System/2 Models 70 and 80
- Configurable for systems based on the 80386SX, 80386DX, or 80486
- 16, 20, 25, and 33 MHz Clock Speeds to Maximize Flexibility and Performance
- Half-speed 80387/80387SX Operation
- 4-Gigabyte Enhanced Addressing
- Micro Channel Arbitration Control Logic
- Functionality equivalent to two 8237 DMA controllers with Extended Mode Support
- Clock, Resets, and Parity Latch Control
- Extended Setup Facility™ (ESF)™
- Low Power 0.9 Micron CMOS Technology

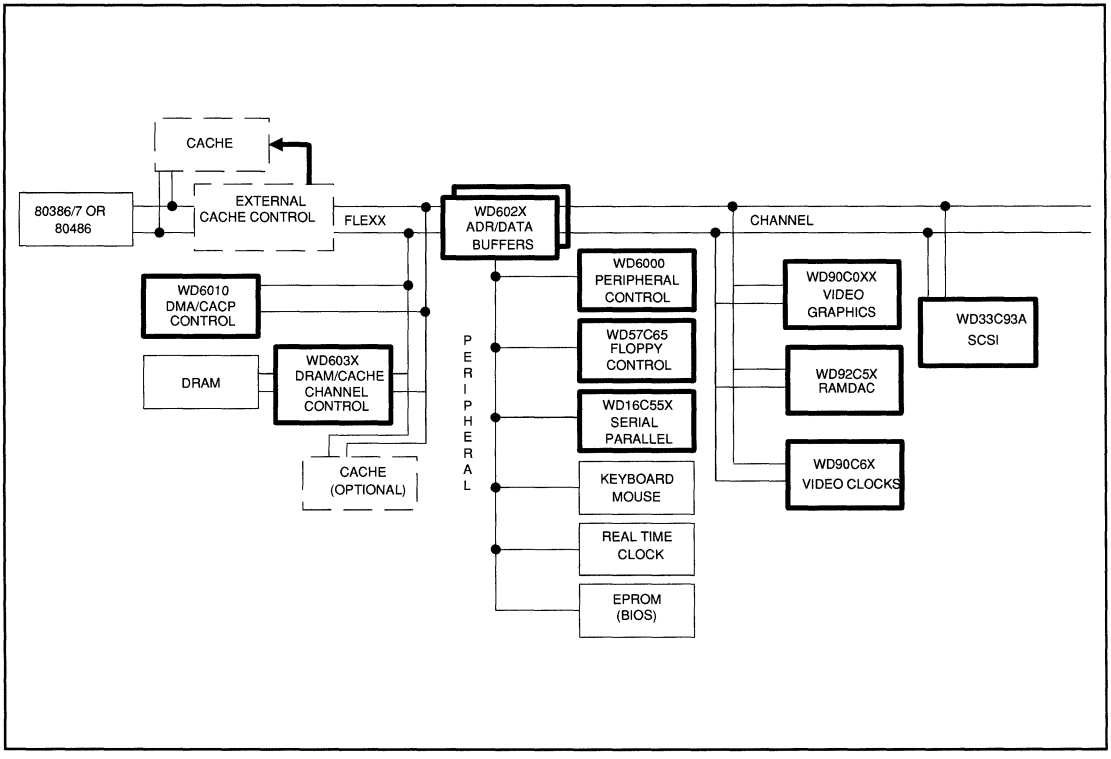


FIGURE 1. SYSTEM DIAGRAM

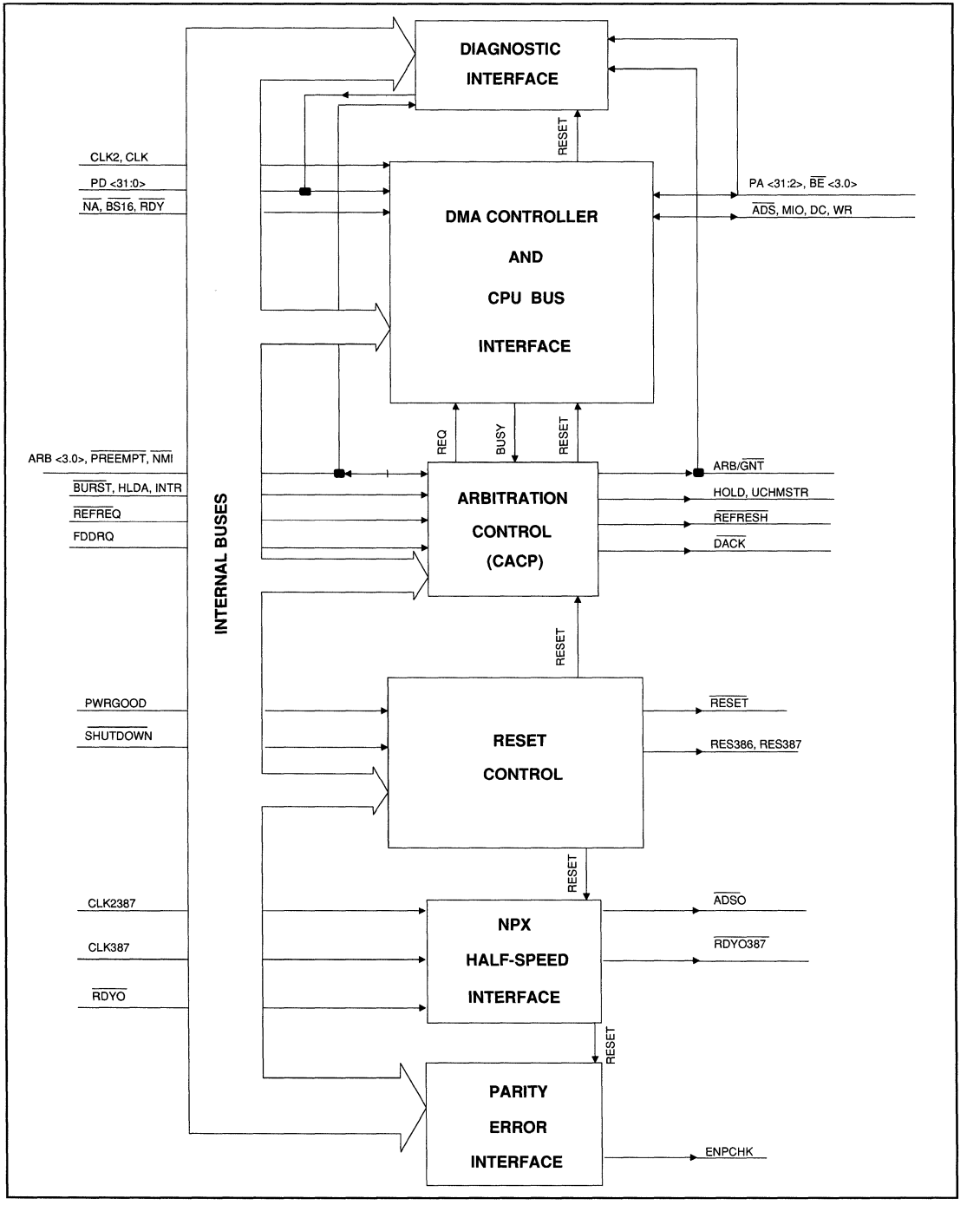


FIGURE 2. WD6010 BLOCK DIAGRAM

2.0 PIN DESCRIPTION

The signals assigned to the different pins are grouped according to their function, and discussed individually in the table on the following pages.

2.1 Diagnostic Interface

This interface is used to diagnose errors in the system. The diagnostic signals recover the state of the bus after an error condition. For more details, see Section 8.6.

2.2 DMA Controller and CPU Bus Interface

The DMA Controller in the WD6010 is fully compatible with the Micro Channel architecture in the basic mode. In addition, the WD6010 provides an enhanced addressing mode, the 4Gig Mode, to enhance the DMA addressing capability.

NOTE: The registers implemented on the WD6010 can only be accessed by the system microprocessor.

2.3 Arbitration Control

The Arbitration Control block in the WD6010 arbitrates between different masters requesting use of the bus at the same time. The Central Arbitration Control Point (CACP) controls the arbitration timing in accordance with Micro Channel specifications.

2.4 Reset Control

The Reset Control block in the WD6010 generates three levels of resets, compatible with the Micro Channel architecture.

A system reset ($\overline{\text{RESET}}$), which resets all the devices in the system.

A CPU reset (RES386), which only resets the microprocessor. The synchronization of this signal to the CPU clock, CLK2, must be done externally.

A numeric coprocessor reset (RES387), which only resets the 80387/80387SX numeric coprocessor. Synchronizing this signal to the numeric coprocessor clock, CLK2387, must be executed externally.

NOTE: The WD6010 is compatible with the 80386SX, 80386DX, and 80486 microprocessors. In the following description, any references to the system microprocessor refer to the 80386SX, 80386DX and 80486, unless specifically stated otherwise. Similarly, any references to the NPX (Numeric coprocessor extension) refer to the 80387SX, and the 80387DX, unless explicitly stated otherwise. Section 10.0 describes the differences in implementation on an 80386SX system versus an 80386DX system.

2.5 Numeric Coprocessor Extension (NPX) Half-speed Interface

The NPX half-speed interface allows the NPX to be operated at half the speed of the CPU. A half-speed NPX interface is useful in systems where the cost-performance requirements dictate an inexpensive coprocessor. In an 80386SX system, the coprocessor used is an 80387SX; on an 80386DX system it is an 80387DX; on an 80486 system, the coprocesser is not required.

2.6 Parity Error Interface

This signal interfaces with external parity latches and provides the capability to latch parity errors.

2.7 Decodes

This block implements the decodes for system-wide functions.

2.8 Miscellaneous

This set of signals include the V_{SS} and V_{DD} signal pins as well as the reserved pins, which should not be connected, but left open in the system.

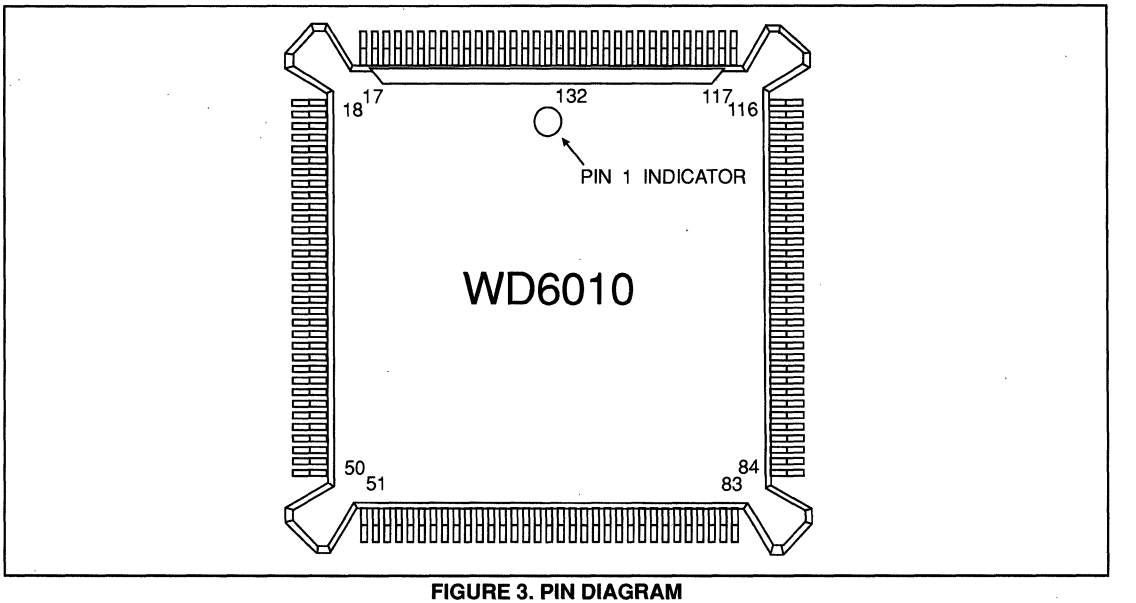


FIGURE 3. PIN DIAGRAM

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	CLK2	34	PD7	67	$\overline{\text{REFRESH}}$	100	V_{DD}
2	V_{SS}	35	V_{SS}	68	$\overline{\text{BE0}}$	101	PA17
3	CLK	36	PD8	69	$\overline{\text{BE1}}$	102	PA16
4	CLK2387	37	PD9	70	$\overline{\text{BE2}}$	103	PA15
5	V_{DD}	38	PD10	71	$\overline{\text{BE3}}$	104	PA14
6	CLK387	39	PD11	71	V_{SS}	105	PA13
7	$\overline{\text{EOT}}$	40	PD12	73	$\overline{\text{ADS}}$	106	PA12
8	$\overline{\text{REFREQ}}$	41	PD13	74	M/$\overline{\text{IO}}$	107	PA11
9	UCHCMD	42	PD14	75	DC	108	V_{SS}
10	A20GATE	43	V_{SS}	76	$\overline{\text{WR}}$	109	PA10
11	N/C	44	PD15	77	$\overline{\text{RESET}}$	110	PA9
12	INTR	45	PD16	78	RES386	111	PA8
13	$\overline{\text{PWRGOOD}}$	46	PD17	79	$\overline{\text{RES387}}$	112	PA7
14	$\overline{\text{SHUTDOWN}}$	47	PD18	80	$\overline{\text{CDSETEN}}$	113	PA6
15	$\overline{\text{BURST}}$	48	PD19	81	$\overline{\text{VGAEN}}$	114	PA5
16	$\overline{\text{TEST}}$	49	PD20	82	$\overline{\text{EDRENA}}$	115	PA4
17	V_{SS}	50	V_{SS}	83	V_{DD}	116	V_{DD}
18	$\overline{\text{PREEMPT}}$	51	PD21	84	PA31	117	PA3
19	ARB0	52	PD22	85	PA30	118	$\overline{\text{PA2}}$
20	ARB1	53	PD23	86	PA29	119	$\overline{\text{NMI}}$
21	ARB2	54	PD24	87	V_{SS}	120	$\overline{\text{ENPCHK}}$
22	ARB3	55	V_{DD}	88	PA28	121	$\overline{\text{DACK}}$
23	V_{SS}	56	PD25	89	PA27	122	$\overline{\text{ADSO}}$
24	$\overline{\text{CHRESET}}$	57	PD26	90	PA26	123	$\overline{\text{RDYO387}}$
24	$\overline{\text{CHCK}}$	58	PD27	91	PA25	124	$\overline{\text{RDYO}}$
26	PD0	59	PD28	92	PA24	125	FDDRQ
27	PD1	60	PD29	93	PA23	126	UCHMSTR
28	PD2	61	PD30	94	PA22	127	A20GTX
29	PD3	62	PD31	95	V_{SS}	128	V_{SS}
30	V_{DD}	63	HOLD	96	PA21	129	$\overline{\text{HLDA}}$
31	PD4	64	V_{SS}	97	PA20	130	$\overline{\text{BS16}}$
32	PD5	65	$\overline{\text{ARB/GNT}}$	98	PA19	131	$\overline{\text{NA}}$
33	PD6	66	$\overline{\text{TC}}$	99	PA18	132	$\overline{\text{RDY}}$

PIN NO.	NAME	TYPE	FUNCTION
			DIAGNOSTIC INTERFACE
127	A20GTX	I/O	ADDRESS BIT 20 GATE – This pin has dual functions. At power-up (trailing edge of RESET), the state of this pin is latched and in conjunction with UCHMSTR, determines the speed at which the system will operate. At all other times, A20GTX, is an output signal acting as a gating signal for address bit 20. This signal is active whenever A20GATE is active or whenever Alternate Gate A20 (port 92H, bit 1) is asserted and the CPU has the bus. **FREQUENCY / UCHMASTER / A20GTX** 16 MHz 0 0 20 MHz 0 1 25 MHz 1 1 33 MHz 1 0
25	CHCK	I	CHANNEL CHECK - This signal which is driven by a master or slave device, indicates that a serious system error has occurred.
24	CHRSET	I	CHANNEL RESET – This signal is generated by the WD6000 to initialize or reset all adapters or on-board peripheral controllers at power-on. The system can also generate this signal through software control (port 96H, bit 7).
10	A20GATE	I	ADDRESS 20 GATE – This signal which is generated by the 8x42 micro-controller activates the A20GTX signal whenever it is active when the CPU generates an address.
9	UCHCMD	I	CHANNEL COMMAND – This signal is the logical OR of the CMD and MMCMD signals, and indicates that a command is present on the Channel.
			DMA CONTROLLER AND CPU BUS INTERFACE
121	DACK	I/O	DMA REQUEST ACKNOWLEDGE – This pin has dual functions. At power-up (trailing edge of RESET), the state of this pin is sampled to determine whether the WD6010 will operate in an 80386SX-compatible or 80386/80486-compatible mode. At all other times, DACK is an output signal to the WD6000 and floppy disk controller. When it is active, it initiates a single I/O read or write transfer. Multiple transfers are initiated only if BURST is also active.

12

PIN NO.	NAME	TYPE	FUNCTION
118 117 115 114 113 112 111 110 109 107 106 105 104 103 102	PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15 PA16	I/O	CPU ADDRESS BUS – This bi-directional address bus between the CPU and DMA controller. During CPU accesses to the WD6010 registers, these are input signals, and during DMA transfers, these are output signals. During DMA transfers in the IBM compatibility mode, which is the power-on default, the WD6010 drives PA (2:31) according to the programmed address. Bits (24:31) are driven to zero. In Enhanced Addressing Mode bits (24:31) are driven according to the programmed address. When the WD6010 is used in an 80386SX system, CPU Address Bus signals (24:31) should be left unconnected.
101 99 98 97 96 94 93 92 91 90 89 88 86 85 84	PA17 PA18 PA19 PA20 PA21 PA22 PA23 PA24 PA25 PA26 PA27 PA28 PA29 PA30 PA31	I/O	CPU ADDRESS BUS – (Cont'd)

PIN NO.	NAME	TYPE	FUNCTION
62	PD31	I/O	CPU DATA BUS – This bi-directional data bus between the CPU and WD6010 is used to transfer data during DMA transfers and CPU accesses to the WD6010 registers.
61	PD30		
60	PD29		
59	PD28		
58	PD27		
57	PD26		The WD6010 has a 32-bit data bus interface compatible with the 80368/80486. However, DMA Transfers are in 8-bit or 16-bit blocks. The WD6010 performs internal swaps and asserts the correct byte enables to put the data in the right location. It handles misaligned transfers by generating the multiple cycles needed to complete the transfer.
56	PD25		
54	PD24		
53	PD23		
52	PD22		
51	PD21		
49	PD20		
48	PD19		
47	PD18		The WD6010 performs dynamic bus sizing to accommodate 16-bit and 32-bit devices on a cycle-by-cycle basis, accomplishing this by sampling the $\overline{BS16}$ input. The combinations of byte enables asserted for different transfers are tabulated below.
46	PD17		
45	PD16		
44	PD15		
42	PD14		
41	PD13		
40	PD12		
39	PD11		
38	PD10		
37	PD9		
36	PD8		
34	PD7		
33	PD6		
32	PD5		
31	PD4		
29	PD3		
28	PD2		
27	PD1		
26	PD0		

	VALID DATA 80386/80486				
Bus Signals	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Byte/Word
PD(0:7)	1	1	1	0	Byte 0
PD(8:15)	1	1	0	1	Byte 1
PD(16:23)	1	0	1	1	Byte 2
PD(24:31)	0	1	1	1	Byte 3
PD(0:15)	1	1	0	0	Word 0
PD(8:23)	1	0	0	1	Word 1
PD(16:31)	0	0	1	1	Word 2

The next table illustrates the way in which the WD6010 splits misaligned transfers into multiple bus cycles. $\overline{BS16}$ is sampled during each cycle to adjust the transfer accordingly.

DATA TRANSFER SIZE (Bytes)					
	1	2			
CPU Address PA (0:1)	xx	00	01	10	11
Transfer Cycles over PD Bus	B	W	LB HB	W	LB H

Legend:
Transfers in **bold** letters indicate that $\overline{BS16}$ was active when sampled.
B – Byte
W – Word
HB –High Order Byes
LB–Low Order Byte
*–The 80386/80486 will first transfer the HB, and then the LB.

12

<table>
<tr><th>PIN NO.</th><th>NAME</th><th>TYPE</th><th>FUNCTION</th></tr>
<tr><td colspan="3">CPU DATA BUS (con't)</td><td>If the $\overline{BS16}$ input is permanently tied low, the WD6010 data bus interface generates a 16-bit interface compatible with the 80386SX. In this mode, the CPU data bus (16:31) should be left unconnected as they each have a weak internal pull-up. The combinations of byte enables asserted for different transfers in an 80386SX system are tabulated below.

<table>
<tr><th colspan="5">VALID DATA 80386SX</th></tr>
<tr><th>Signal</th><th>$\overline{BE3}$</th><th>$\overline{BE2}$
(PA1)</th><th>$\overline{BE1}$
($\overline{BEH}$)</th><th>$\overline{BE0}$
($\overline{BEL}$)</th><th>Byte/Word</th></tr>
<tr><td>PD(0:7)</td><td>x</td><td>0</td><td>1</td><td>0</td><td>Byte 0</td></tr>
<tr><td>PD(8:15)</td><td>x</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>PD(0:7)</td><td>x</td><td>1</td><td>1</td><td>0</td><td>Byte 2</td></tr>
<tr><td>PD(8:15)</td><td>x</td><td>1</td><td>0</td><td>1</td><td>Byte 3</td></tr>
<tr><td>PD(0:15)</td><td>x</td><td>0</td><td>0</td><td>0</td><td>Word 0</td></tr>
<tr><td>PD(0:15)</td><td>x</td><td>1</td><td>0</td><td>0</td><td>Word 1</td></tr>
</table></td></tr>
<tr><td>76</td><td>WR</td><td>I/O</td><td>WRITE/READ – This signal is directly connected to the CPU WR signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. Together with DC and M/$\overline{IO}$, these signals identify the type of bus cycle being executed on the CPU bus.</td></tr>
<tr><td>75</td><td>DC</td><td>I/O</td><td>DATA/CONTROL – This signal is directly connected to the CPU DC signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. Together with WR and M/$\overline{IO}$, these signals identify the type of bus cycle being executed on the CPU bus.</td></tr>
<tr><td>74</td><td>M/$\overline{IO}$</td><td>I/O</td><td>MEMORY $\overline{I/O}$ –This signal is directly connected to the CPU M/$\overline{IO}$ signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. Together with WR and DC, these signals identify the type of bus cycle being executed on the CPU bus.

<table>
<tr><th>M/$\overline{IO}$</th><th>DC</th><th>WR</th><th>WD6010 FUNCTION</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Does not occur</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>I/O Write</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Does not occur</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory Read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Memory Write</td></tr>
</table></td></tr>
</table>

PIN NO.	NAME	TYPE	FUNCTION
73	ADS	I/O	ADDRESS STROBE – This signal is directly connected to the CPU ADS signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. This signal is used to track bus cycles.
71 70 69 68	BE3 BE2 BE1 BE0	I/O	BYTE ENABLE – These signals are used during data transfers to indicate which data bytes are valid on the CPU data bus. During DMA operations these signals are output signals. When the system CPU accesses the WD6010 registers, they are input signals. The definition of these signals changes to match the type of microprocessor (80386SX or (80386/80486), as configured by DACK at power-up.

SIGNAL	80386SX	80386/80486
BE3	BE3	Not connected
BE2	BE2	PA1
BE1	BE1	BEH
BE0	BE0	BEL

132	RDY	I	READ – This signal is directly connected to the CPU READY signal. This signal is used to track bus cycles. It is synchronized with CLK2.
131	NA	I	NEXT ADDRESS – This signal is generated by the WD6030 whenever a pipelined cycle can be supported by the system. If this signal is asserted and the WD6010 has an internal request pending, the WD6010 goes into pipelined mode. For the WD6010 this is an input only signal, that is applicable during DMA transfers. Figure 4 illustrates a non-pipelined transfer and Figure 5 illustrates a typical pipelined transfer.
130	BS16	I	BUS SIZE 16 – This signal is generated by the WD6030 to indicate whether the CPU or WD6010 is accessing a 32-bit or (16-bit or 8-bit) port. The signal is high whenever a 32-bit port is accessed and all the byte enables should be active. BS16 is low whenever a 16-bit port or 8-bit port is accessed. The byte enables are sampled to determine if the access is to a 16-bit or 8-bit port.
3 1	CLK CLK2	I	CLOCKS – CLK is a CMOS-level clock signal which has the same frequency as the CPU. CLK2 is also a CMOS-level clock. CLK2 has a frequency twice that of the CPU clock frequency. The WD6010 shares the CLK2 signal with the CPU.

12

PIN NO.	NAME	TYPE	FUNCTION
66	$\overline{TC}$	O	$\overline{TERMINAL\ COUNT}$ – This signal is generated by the WD6010 DMA controller logic during the last I/O bus cycle of a DMA transfer to indicate that the DMA channel currently servicing the Channel has reached a terminal count condition. This indicates to the DMA slave that this is the last cycle to be performed.
		ARBITRATION CONTROL	
126	UCHMASTR	I/O	CHANNEL MASTER – This pin has dual functions. At power-up (trailing edge of $\overline{RESET}$), the state of this signal is latched and in conjunction with A20GTX, determine the speed at which the system will operate. At all other times, UCHMSTR is an output signal which becomes active whenever a Micro Channel master other than the CPU or the WD6010 DMA controller gets control of the bus. **FREQUENCY / UCHMSTR / A20GTX** 16 MHz / 0 / 0 20 MHz / 0 / 1 25 MHz / 1 / 1 33 MHz / 1 / 0
119	$\overline{NMI}$	I/O	$\overline{NON\text{-}MASKABLE\ INTERRUPT}$ – When driven by the WD6010 to the CPU, $\overline{NMI}$ indicates that the CACP has reached a bus time-out condition while monitoring the bus. When the signal is received from the WD6000, it tells the CACP to initiate an arbitrated cycle to remove any bus masters so that the CPU can service the interrupt.
22 21 20 19	ARB3 ARB2 ARB1 ARB0	I/O	ARBITRATION BUS – These four open collector lines comprise the aribtration bus. These signals are driven by DMA slaves, system master and bus masters when requesting control of the bus during arbitration cycles. When the floppy disk controller requests the bus through FDDRQ, the ARB (0:3) signals are driven by the WD6010.
18	$\overline{PREEMPT}$	I/O	$\overline{PREEMPT}$ – This open collector line signals that an arbitrating device wants to use the bus, and the CACP initiates an arbitration cycle when this line is active. A floppy disk controller request, a refresh cycle request, or the receipt of a $\overline{NMI}$ causes this signal to be driven by the CACP in the WD6010.
129	HLDA	I	HOLD ACKNOWLEDGE – The CPU asserts HLDA in response to a HOLD signal to indicate that it has relinguished the local bus.

PIN NO.	NAME	TYPE	FUNCTION
125	FDDRQ	I	FLOPPY DISK REQUEST – This signal indicates that the floppy disk controller requires the DMA controller to transfer data. The CACP translates this request into a level 2 priority and competes for the bus.
15	$\overline{\text{BURST}}$	I	$\overline{\text{BURST}}$ – This input signals that the current Channel bus owner will continue to hold the bus for more than one transfer. For DMA transfers, $\overline{\text{BURST}}$ is removed during the last I/O bus cycle of the transfer or if a terminal count is reached.
12	INTR	I	INTERRUPT – If bit 4 of the CACP register, port 90H, is set and a master other than the CPU is using the bus, this interrupt signal is used to initiate an arbitration cycle. This allows the CPU to service an interrupt during bus master cycles.
8	$\overline{\text{REFREQ}}$	I	$\overline{\text{REFRESH REQUEST}}$ – This timer output signal is generated by the WD6000 to request a refresh cycle. The WD6010 responds by driving the $\overline{\text{PREEMPT}}$ signal. The CACP enters the ARB state and requests the bus. The refresh cycle is executed and the bus returned to the $\overline{\text{GNT}}$ state. If the CACP is already in the ARB state, the refresh request extends the period by one bus cycle.
7	EOT	I	END OF TRANSFER – This signal from the WD6022 Address Buffer indicates an end of transfer condition. An end of transfer occurs when $\overline{\text{CMD}}$, $\overline{\text{S0}}$ and $\overline{\text{S1}}$ are inactive on the Channel. Internally, EOT is ORed with $\overline{\text{BURST}}$ to show an end of transfer condition.
67	$\overline{\text{REFRESH}}$	O	$\overline{\text{REFRESH}}$ – This Channel signal indicates that the memory read operation on the bus is a refresh cycle. Address lines (2:10) and $\overline{\text{BE}}$(0:3) hold the state of the refresh address counter in the DMA controller. Address lines (11:31) are driven to zero. In response, the WD6030 performs a memory read operation on the Channel and a RAS-only refresh for the motherboard DRAM. On the Channel, any slave can choose to extend the refresh cycle by de-asserting CHRDY.
65	ARB/$\overline{\text{GNT}}$	O	ARBITRATION/$\overline{\text{GRANT}}$ – This signal indicates the state of the CACP. In the arbitration state (high), an arbitration cycle is in progress and all devices wishing to own the bus drive their arbitration levels on the arbitration bus and compete for Channel ownership. At the end of the arbitration cycle (300 ns minimum), ownership of the Channel is given to the owner with the winning arbitration level. The change to a grant cycle is signified by the change in the polarity of the signal to $\overline{\text{GNT}}$ (low).

12

PIN NO.	NAME	TYPE	FUNCTION
63	HOLD	O	HOLD – This signal is synchronous with CLK2. When asserted, it requests the CPU to relinguish the CPU bus for a refresh, DMA, or Channel master transfer.
			RESET CONTROL
14	$\overline{\text{SHUTDOWN}}$	I	$\overline{\text{SHUTDOWN}}$ – This signal initiates a CPU reset and is generated by the 8742 keyboard controller, as commanded by the CPU.
13	PWRGOOD	I	POWERGOOD – This signal originates in the power supply and indicates the state of the power supply voltages. $\overline{\text{RESET}}$ is derived from the state of this line.
79	RES387	O	80387 RESET – This reset signal is generated on a system reset or a NPX soft reset and is an unsynchronized reset for the NPX. It must be externally synchronized with CLK2387 before being sent to the NPX. On a system reset, the pulse width of this signal is determined by the power supply logic. On a NPX soft reset (an I/O write to port F1H), this signal has a pulse width of at least 256 CLK2s. When the NPX is operating at half the frequency of the 80386, the pulse width is 128 CLK2387 periods (CLK2387 period = 2*CLK2 period).
78	RES386	O	80386 RESET – This signal is generated by the WD6010 by the following reset sources; Power-On, Alternate Hot Reset, Keyboard Shutdown or Processor Shutdown. It must be externally synchronized with CLK2 before being sent to the CPU.
77	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ – This signal is derived from the state of the PWRGOOD signal. It is synchronized with CLK2 and resets all the components in the system. While active no memory refreshes take place.
			NUMERIC COPROCESSOR EXTENSION (NPX) HALF-SPEED INTERFACE
124	$\overline{\text{RDYO}}$	I	$\overline{\text{READYOUT}}$ – This signal is the $\overline{\text{READYO}}$ from the NPX. When used in Full Speed Mode, this pin should be connected to VDP. When used in Half-Speed Mode, this signal is used to track bus cycles to the NPX.
6 4	CLK387 CLK2387	I I	80387 CLOCKS – CLK387 is a CMOS-level clock signal which is generated by external circuitry and is synchronized with CLK. CLK2387 is also a CMOS-level clock signal. It is synchronized with CLK2. These two signals should be connected to VDD when the NPX is used in Full-Speed Mode. In Half-Speed Mode, these signals will operate at half the speed of CLK and CLK2 respectively.

PIN NO.	NAME	TYPE	FUNCTION
123	$\overline{\text{RDYO387}}$	O	$\overline{\text{80387 READYOUT}}$ – When the NPX is used in Full-Speed Mode, this signal is left unconnected and the READYO output from the NPX is directly connected to the logic for $\overline{\text{RDY}}$.
122	$\overline{\text{ADSO}}$	O	$\overline{\text{ADDRESS STROBE}}$ – This signal is the address strobe output to the NPX in Half-Speed Mode. In Full-Speed Mode, this pin is a N/C.
			PARITY ERROR INTERFACE
120	ENPCHK	O	ENABLE PARITY CHECK – This signal is a duplication of bit 0 of the Memory Encoding Register 1 (port E1H) in the WD6030. It is used to enable/disable parity checking. The signal directly interfaces with the external parity latches. Refer to the WD6030 Data Sheet for more information.
82	$\overline{\text{EDRENA}}$	O	$\overline{\text{EXTENDED DATA REGISTER ENABLE}}$ – When active, $\overline{\text{EDRENA}}$ enables the selected ESF register to read or write. This signal is generated by comparing the CPU I/O address to the value stored in the ESF Pointer Register (port xxH).
81	VGAEN	O	VIDEO GRAPHICS ADAPTER ENABLE – When enabled by the Video Subsystem Enable Register (port 3C3H, bit 0), this signal decodes the upper address bits (20:31) for the system board video RAM area, A00000H to BFFFFFH.
80	$\overline{\text{CDSETEN}}$	O	$\overline{\text{CARD SETUP ENABLE}}$ – This signal decodes I/O addresses. 100H to 107H with the appropriate timing for the WD6000 for channel setup cycles in the system.
			MISCELLANEOUS
5 30 55 83 100 116	V_{DD}	I	+5 POWER SUPPLY
2 17 23 35 43 50 64 72 87 98 108 128	V_{SS}	I	0V GROUND
11	N/C		Not Connected

12

PIN NO.	NAME	TYPE	FUNCTION
16	$\overline{\text{TEST}}$	I	$\overline{\text{TEST}}$ – This is an active low signal that facilitates board-level testing. When low, this signal tri-states all outputs and bi-directional signal lines, allowing an ATE tester to drive these signals. When high, the outputs and bi-directional lines are enabled by the chip.

Figure 4 illustrates a typical non-pipelined bus cycle for the WD6010, and shows that the bus interface for the WD6010 is identical to the 80386.

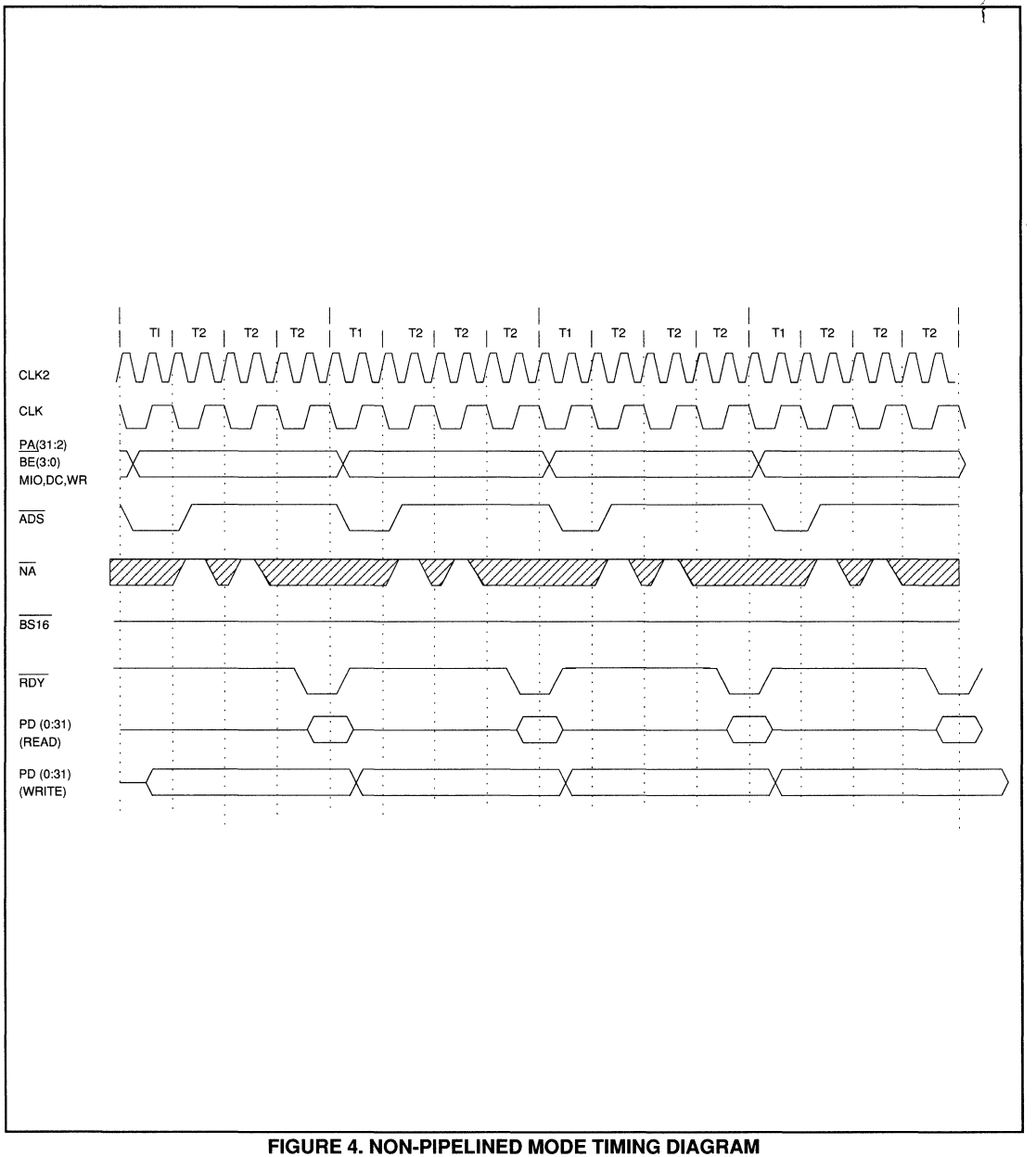


FIGURE 4. NON-PIPELINED MODE TIMING DIAGRAM

Figure 5 illustrates a typical Pipelined bus cycle for the WD6010. The WD6010 generates bus cycles which are identical to the 80386 bus cycles.

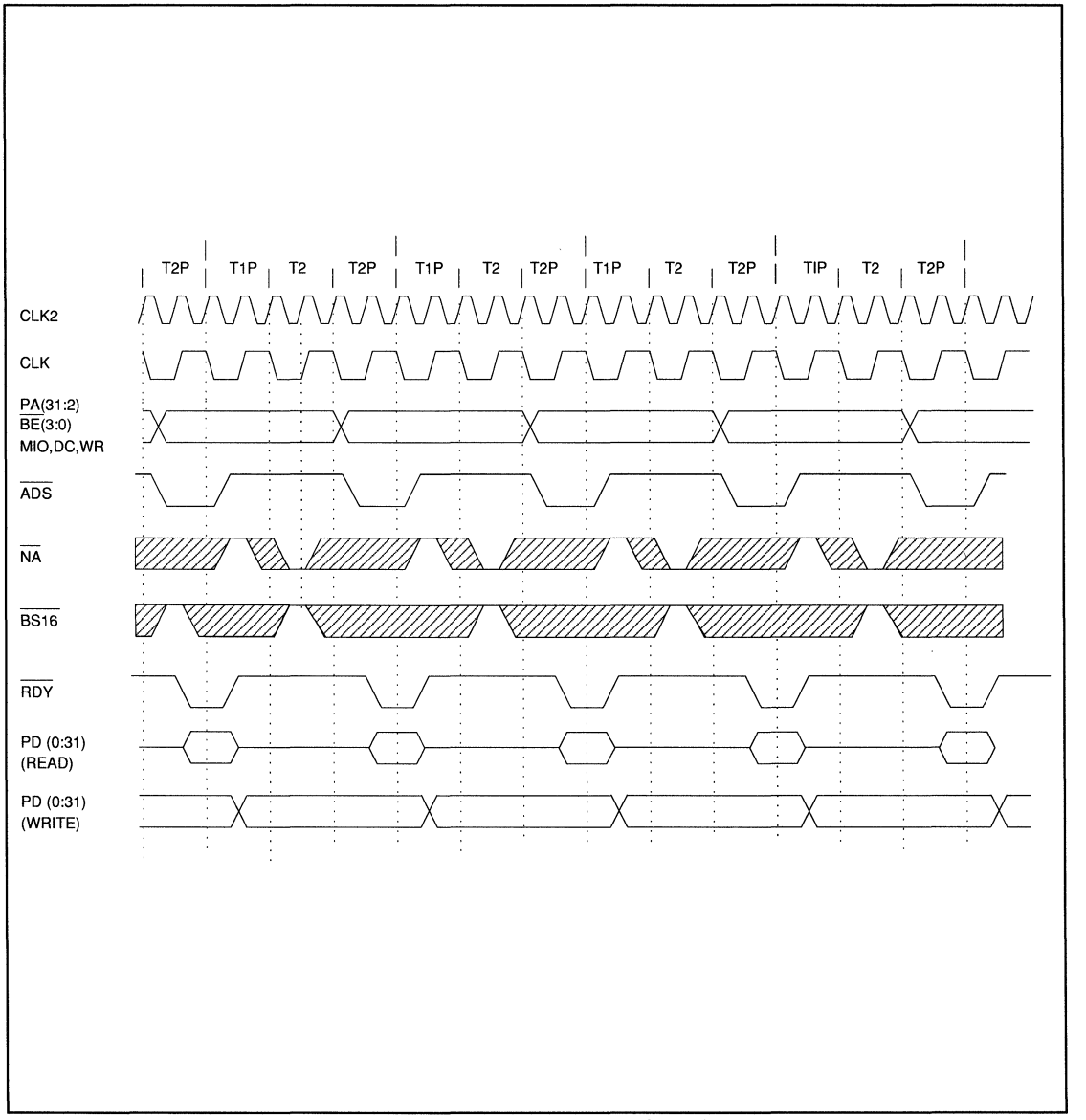


FIGURE 5. PIPLINED MODE TIMING DIAGRAM

ADDRESS RANGE	LOCATION	FUNCTION
0000 to 000FH	WD6010	DMA Controller Chs 0-3*
0018H	WD6010	Extended Function Reg.*
001AH	WD6010	Extended Function Execute*
0020 to 0021H	WD6000	Interrupt Controller 1
0040, 0040-0044, 0047H	WD6000	System Timers
0060H	WD6000	Keyboard Data Port
0061H	WD6000	System Control Port B
0064H	WD6000	Rd - Keyboard Status, Wr –Keyboard Command
0070H	WD6000	RTC/CMOS Address Register, NMI Mask
0071H	WD6000	RTC/CMOS Data Port
0074H	WD6000	EAR0 Extended CMOS RAM, ESF
0075H	WD6000	EAR1 Extended CMOS RAM
0076H	WD6000	Extended CMOS RAM Data Port
0081 to 0083, 0087H	WD6010	DMA Page Registers 0-3*
0089 to 008B, 009FH	WD6010	DMA Page Registers 4-7*
0090H	WD6010	CACP Register*
0091H	WD6000	Card Selected Feedback
0092H	WD6000	System Control Port A
0094H	WD6000	System Board Setup
0096, 0097H	WD6000	POS, Channel Connector Select
00A0, 00A1H	WD6000	Interrupt Controller 2
00C0 to 00DFH	WD6010	DMA Controller (even only)*
00E0 to 00E1H	WD6030	Memory Control Registers
00E2 to 00E7H	WD6010	Diagnostic Registers
00F0H	WD6000	Coprocessor Clear Busy
00F1H	WD6000	Coprocessor Reset
00F8 to 00FFH	NPX	80387/80387SX Coprocessor*
0100, 0101H	WD6000	System ID
0102 to 0107H	WD6000	Board Configuration (POS)
0278 to 027BH	WD6000	Parallel Port 3
02F8 to 02FFH	WD6000	Alternate Serial Port
0378 to 037BH	WD6000	Parallel Port 2
03BC to 03BFH	WD6000	Parallel Port 1
03B4, 03B5, 03BA, 03C0-03C5H	WD90C00	Video Subsystem**
03CE, 03CF, 03D4, 03D5, 03DAH	WD90C00	Video Subsystem
03C6 to 03C9H	WD90C00	Video DAC**
03F0 to 03F7H	WD6000	Diskette Drive Controller
03F8 to 03FFH	WD6000	Primary Serial Port
0700H	WD6010	ESF Data Register (Default)

TABLE 1. SYSTEM LEVEL I/O MAP (WD6500)

* No Channel cycle generated on these addresses.
**The WD90C00 Enable Register (03C3H) is in the WD6010.

3.0 DMA CONTROLLER

The DMA Controller is a serial transfer device compatible with the Intel* 8237, and includes the IBM extended controller interface and functions. Its logic supports eight independent channels, six of which are assigned fixed priorities. The remaining two have programmable priorities.

The WD6010 takes two channel cycles to transfer a word or byte between memory and I/O. Each channel cycle needs two or more CPU clock cycles. Channel and bus arbitration functions are resolved externally.

3.1 DMA Interface

The DMA Controller interfaces to the system on the CPU local bus. As the table in the description of the PD signals shows, it generates and encodes the same control signals as the CPU. The controller may be programmed at any time that Hold Acknowledge (HLDA) from the CPU is inactive. The programming may only be done by the system CPU.

Each of the two transfer bus cycles requires two or more CPU clock cycles. The time taken by the I/O portion of the cycle depends on the response from the system interface: whether it is a local cycle or a Channel cyle. All Channel cycles take at least 200 ns. The time taken by the memory portion of the cycle depends on the response from the system interface, that is, if it is a local cycle versus a Channel cycle, cache hit versus a cache miss, page hit versus a page miss, and so on.

A Channel transfer is established by the CPU setup and initiated from an external slave source through arbitration control in the form of DMAREQ input. The requesting DMA channel is specified on the ARB bus input.

3.2 Internal Architecture

The internal architecture of the DMA Controller in the WD6010 is based on the six basic modules described in the subsections that follow.

3.2.1 Address Translator

This module converts address and data information from the CPU interface that is in PC/AT Compatibility Mode format into the Extended Mode format. This information is then stored for run-time use.

3.2.2 RAM Registers

These RAM locations store the 32-bit base address, the 32-bit current address, the 16-bit base count, the 16-bit current count, and the 16-bit current I/O address, for each channel. The current values are read/write and are written by the CPU at the same time as the base registers. An additional register, the Transfer Holding Register, temporarily stores data between bus cycles of a transfer. This register can not be accessed by the system CPU.

The RAM array is 112 bits x 8 locations, with one location allocated to each channel. The Channel 0 and 4 implement the Virtual DMA feature of the Micro Channel system.

3.2.2.1 Base Memory Address Register

This 32-bit register is initialized by the CPU through byte-wide accesses. This is a write register and can not be read by the CPU. In Compatibility Mode, three writes are executed to program twenty-four address bits, and four writes are executed in Enhanced Addressing Mode to program thirty-two address bits.

3.2.2.2 Current Memory Address Register

The CPU initializes this 32-bit read/write register by byte-wide accesses at the same time that it initializes the Base Memory Address Register. This register can also be read in byte-wide accesses.

During DMA transfers, this register is incremented or decremented after each memory bus cycle. Enabling Auto-Initialize reloads this register at the end of a transfer with the value stored in the Base Memory Address Register. This state is reached when the DMA controller reaches a terminal count condition and the $\overline{TC}$ signal has been generated. Figure 6 illustrates a read cycle with Auto-Initialize, followed by another transfer.

3.2.2.3 Base Transfer Count Register

The CPU initializes this 16-bit register in byte-wide accesses. The number of transfers is the value in the register + 1. The WD6010 does a single transfer when this register is programmed to 0000H.

3.2.2.4 Current Transfer Count Register

The CPU initializes this 16-bit read/write register by byte-wide accesses at the same time that it

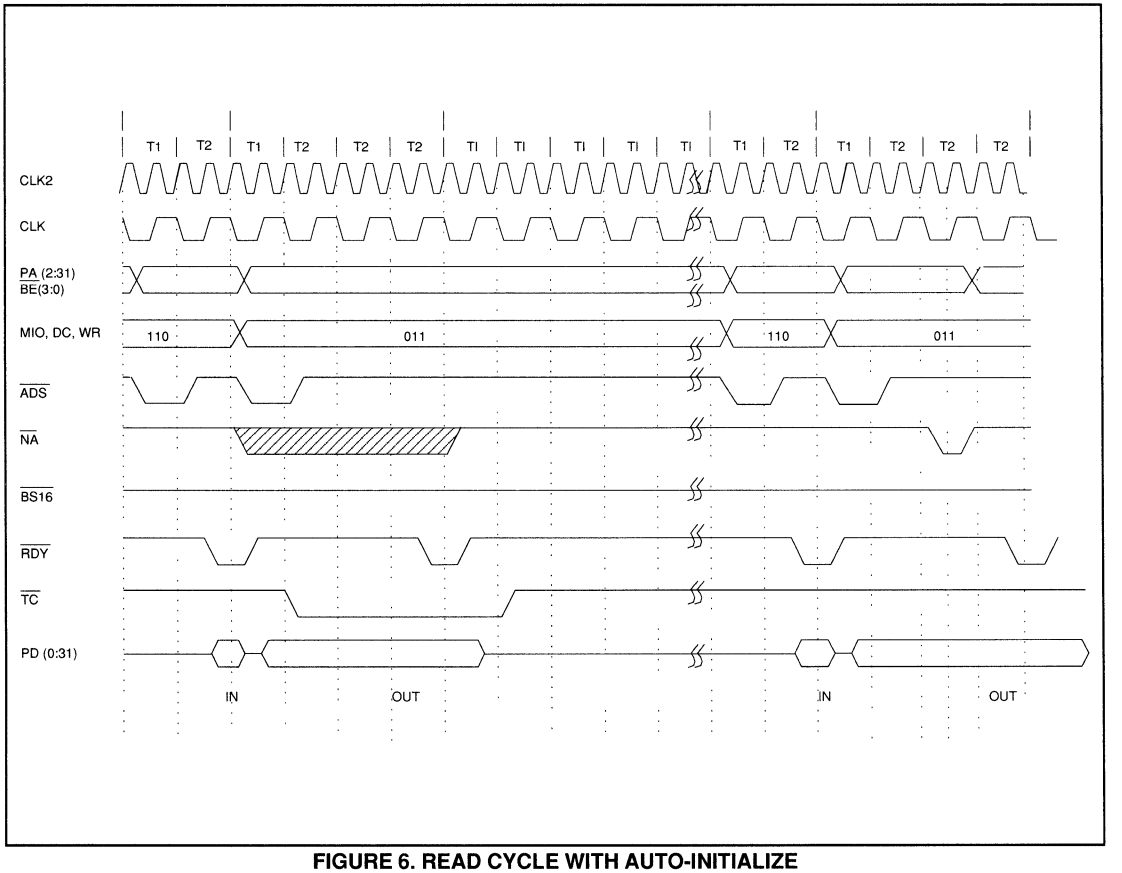


FIGURE 6. READ CYCLE WITH AUTO-INITIALIZE

initializes the Base Transfer Count Register. The CPU can read it in byte-wide accesses.

During DMA transfers, this register is decremented after each memory bus cycle. Enabling Auto-Initialize reloads this register at the End-of-Transfer (EOT) with a value from the Base Transfer Count Register.

3.2.2.5 Current I/O Address Register

This register is initialized by the CPU in Extended Mode only. The value gated to the bus during the I/O bus cycle depends on the state of Bit 0 in the Extended Mode Register. If Programmed I/O Address Mode is set, then the value in the register is used; if not, 0000H is used.

3.2.2.6 Temporary Holding Register

This register temporarily stores data between bus cycles of a transfer. The CPU can not access this register.

3.2.3 DMA Registers

The DMA registers consist of the Mask, Mode, Arbus, and Status registers. Table 2 shows the allocation of these registers.

Figure 7 shows the format for the Mask register, and Figure 8 shows the format for the Mode Register. See Section 3.3 for a description of the various modes and transfer types set in the Mode Register.

REGISTER	SIZE	QTY	ALLOCATION
MASK	8 bits	2	1 for Chs 0-3 1 for Chs 4-7
MODE	8 bits	8	1 per channel
ARBUS	8 bits	2	1 for Ch 0, 1 for Ch 4
STATUS	8 bits	2	1 for Chs 0-31 1 for Chs 4-7

TABLE 2. DMA REGISTER ALLOCATION

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

RESERVED				MASK BIT		CHANNEL SELECT			
0				DIS	ENA	–		–	
						1	0	Channel	
						0	0	0 or 4	
						0	1	1 or 5	
						1	0	2 or 6	
						1	1	3 or 7	
RESERVED		CH 3 OR 7		CH 2 OR 6		CH 1 OR 5		CH 0 OR 4	
0		DIS	ENA	DIS	ENA	DIS	ENA	DIS	ENA

Default = [ ]

FIGURE 7. MASK REGISTER FORMAT

Mode Select		Count Dir		Auto Initial		Transfer Type		Channel Select	
—	—	DEC	INC	ENA	DIS	—	—	—	—

7	6	Mode Select
0	0	Demand
0	1	Single (N)
1	0	Block (N)
1	1	Cascade(N)

3	2	Transfer Type
0	0	Verify
0	1	Write Mem
1	0	Read Mem
1	1	Reserved

1	0	Channel
0	0	0 or 4
0	1	1 or 5
1	0	2 or 6
1	1	3 or 7

PC/AT Compatible Mode

Extended Mode

Reserved	Width		Reserved	Count Dir		Transfer		Transfer		Auto Initial		IO Adr	
0	16 Bit Xfer	8 Bit Xfer	0	DEC	INC	Write Mem	Read Mem	Data	Verify	On	Off	Prog Value	0000H

N=Not Used

FIGURE 8. MODE REGISTER FORMAT

RESERVED				ARBITRATION LEVEL			
–	–	–	–	–	–	–	–

3	2	1	0	Level
0	0	0	0	0 Available
0	0	0	1	1 See Warning
0	0	1	0	2 See Warning
0	0	1	1	3 See Warning
0	1	0	0	4 Available
0	1	0	1	5 See Warning
0	1	1	0	6 See Warning
0	1	1	1	7 See Warning
1	0	0	0	8 Available
1	0	0	1	9 Available
1	0	1	0	A Available
1	0	1	1	B Available
1	1	0	0	C Available
1	1	0	1	D Available
1	1	1	0	E Available
1				F Reserve-System MPU

WARNING:
These levels are assigned to DMA channels 1-3, 5-7. If channel 0 or 4 is assigned to one of these levels, the user must insure that no conflict occurs.

FIGURE 9. ARBUS REGISTER FORMAT

12

Request Status								Terminal Count Status							
Chan 3 or 7		Chan 2 or 6		Chan 1 or 5		Chan 0 or 4		Chan 3 or 7		Chan 2 or 6		Chan 1 or 5		Chan 0 or 4	
Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No
Default =															

FIGURE 10. STATUS REGISTER FORMAT

The two Arbus registers, one each for DMA Channels 0 and 4, implement the "virtual DMA" feature. The software can use these registers to dynamically re-assign the arbitration level to which these channels respond during a DMA operation. This allows Channels 0 and 4 to service devices at any arbitration level. Normally, Channels 0 and 4 are assigned levels 08H to 0EH only, Levels 01-03H and 05-07H are assigned to DMA Channels 1-3 and 5-7. If Channels 0 or 4 are assigned one of these levels, it is up to the user to ensure that there are no conflicts. Figure 9 illustrates the Arbus register format.

In Extended Mode, a status read provides the status of Channels 0-3, and a second read gives the status of Channels 4-7. The byte pointer is initialized when the command is given. Figure 10 shows the format of the Status Register.

3.2.4 Transfer Control

This module provides the interface for the CPU bus. The signals and timings are equivalent to those of the CPU, and are generated from the same CPU clock source.

3.2.5 Register Control

This control function co-ordinates the various modules during a DMA transfer cycle.

3.2.6 Work Registers

These registers are used for the temporary storage of data and parameters during and between DMA transfer bus cycles.

3.3 System CPU Access Modes

The system CPU can access the DMA controller in two modes: PC/AT Compatibility Mode, and PS/2 Extended Mode. At run-time, the mode through which the transfer was set up is not retained.

The WD6010 does not support the Compatibility Mode command, and request and rotating priority functions. The Mode register is only supported to the extent detailed in the following subsections.

3.3.1 Compatibility Mode

Table 3 provides an I/O map of this mode.

I/O ADRS	DESCRIPTION	BIT WIDTH	BYTE PTR
0000H	Ch 0 Memory Adrs. Reg. (R/W)	15-00	yes*
0001H	Ch 0 Transfer Count Reg. (R/W)	15-00	yes*
0002H	Ch 1 Memory Adrs. Reg. (R/W)	15-00	yes*
0003H	Ch 1 Transfer Count Reg. (R/W)	15-00	yes*
0004H	Ch 2 Memory Adrs. Reg. (R/W)	15-00	yes*
0005H	Ch 2 Transfer Count Reg. (R/W)	15-00	yes*
0006H	Ch 3 Memory Adrs. Reg. (R/W)	15-00	yes*
0007H	Ch 3 Transfer Count Reg. (R/W)	15-00	yes*
0008H	Chs 0-3 Status Register	07-00	-
000AH	Chs 0-3 Mask Reg. (Set/Rst)(W)	07-00	-
000BH	Chs 0-3 Mode Register (W)	07-00	-
000CH	Chs 0-3 Clear Byte Pointer (W)	N/A	-
000DH	Chs 0-3 Master Clear (W)	N/A	-
000EH	Chs 0-3 Clear Mask Register (W)	N/A	-
000FH	Chs 0-3 Write Mask Register (W)	07-00	-
0081H	Ch 2 Page Register (R/W)	07-00	-
0082H	Ch 3 Page Register (R/W)	07-00	-
0083H	Ch 1 Page Register (R/W)	07-00	-
0087H	Ch 0 Page Register (R/W)	07-00	-
0089H	Ch 6 Page Register (R/W)	07-00	-
008AH	Ch 7 Page Register (R/W)	07-00	-
008BH	Ch 5 Page Register (R/W)	07-00	-
008FH	Ch 4 Page Register (R/W)	07-00	-
00C0H	Ch 4 Memory Adrs. Reg. (R/W)	15-00	yes*
00C2H	Ch 4 Transfer Count Reg. (R/W)	15-00	yes*
00C4H	Ch 5 Memory Adrs. Reg. (R/W)	15-00	yes*
00C6H	Ch 5 Transfer Count Reg. (R/W)	15-00	yes*
00C8H	Ch 6 Memory Adrs. Reg. (R/W)	15-00	yes*
00CAH	Ch 6 Transfer Count Reg. (R/W)	15-00	yes*
00CCH	Ch 7 Memory Adrs. Reg. (R/W)	15-00	yes*
00CEH	Ch 7 Transfer Count Reg. (R/W)	15-00	yes*
00D0H	Chs 4-7 Status Register	07-00	-
00D4H	Chs 4-7 Mask Reg. (Set/Rst)(W)	07-00	-
00D6H	Chs 4-7 Mode Register (W)	07-00	-
00D8H	Chs 4-7 Clear Byte Pointer (W)	N/A	-
00DAH	Chs 4-7 Master Clear (W)	N/A	-
00DCH	Chs 4-7 Clear Mask Register (W)	N/A	-
00DEH	Chs 4-7 Write Mask Register (W)	07-00	-

TABLE 3. COMPATIBILITY MODE I/O MAP

* Both Memory Address and Transfer Count Registers are loaded on a write operation; only the Current register is readable.

3.3.2 Extended Mode

This mode is accessed through four locations in the I/O space, as Table 4 shows. The format for the Extended Function Register (EFR), 0018H, is shown in Figure 11.

The protocol for Extended Mode is as follows:

1.Write to the EFR (0018H) to set the channel selection and function command. This resets the internal byte pointer to point to least significant byte (LSB). Direct commands only require an I/O write to the EFR. If it is not a direct command, go on to Step 2.

2.Write or read the appropriate number of times to execute the function from the EFE port. The byte pointer increments automatically.

Direct commands written to the EFR include Mask Register Set Bit, Mask Register Reset Bit, and Master Clear. The Mask Register Set Bit command masks or disables all the channels in the Mask Register. The Mask Register Reset Bit command unmasks or enables all the channels in the Mask Register. The Master Clear can be generated by the CPU or by a bus time-out condition. If a Master Clear command is given, the DMA controller must be re-initialized. The Master Clear masks all the channels in the Mask Register, that is, it sets all the bits to one. It also resets all the bits of the Status Register to zero.

I/O ADDRESS	DESCRIPTION
0018H	Extended Function Register (EFR) (W)
0019H	Reserved
001AH	Extended Function Execute (EFE) (W)
001BH	Reserved

TABLE 4. EXTENDED MODE I/O ADDRESS

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Programmed Command (1AH)				Reserved	Channel Selection		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

7	6	5	4	Command	Bit Width	Byte Ptr
0	0	0	0	I/O Adr Reg (R/W)	00–15	yes
0	0	0	1	1 Reserved	—	—
0	0	1	0	2 Mem Adr Reg (R/W)	00–23	yes
0	0	1	1	3 Mem Adr Reg Read	00–23	yes
0	1	0	0	4 Xfer Cnt Reg (R/W)	00–15	yes
0	1	0	1	5 Xfer Cnt Reg Read	00–15	yes
0	1	1	0	6 Status Reg Read	00–07	yes
0	1	1	1	7 Mode Reg (R/W)	00–07	—
1	0	0	0	8 Arbus Reg (R/W)	00–07	—
1	0	0	1	9 Mask Reg Set Bit	Direct	—
1	0	1	0	A Mask Reg Reset Bit	Direct	—
1	0	1	1	B IBM Test DRQ	—	*
1	1	0	0	C IBM Test Clear	—	*
1	1	0	1	D Master Clear	Direct	—
1	1	1	0	E Reserved	—	—
1	1	1	1	F Reserved	—	—

* These functions are not implemented.

2	1	0	Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FIGURE 11. EXTENDED FUNCTION REGISTER (EFR) (0018H)

3.3.3 Enhanced Mode

The DMA Controller Enhanced Mode is a Western Digital innovation implemented on the WD6010 which extends the DMA address space up to 4 Gbytes. A DMA operation can now take place in Memory Addresses 00000000 to FFFFFFFFH.

The WD6010 powers up in a mode compatible with the Model 80, which allows DMA operation in Compatibility Mode or Extended Mode. The memory address space in which a DMA operation can take place extends from 000000 to FFFFFFH. If the addresses exceed FFFFFFH, they roll over to 000000. Address Bits 24 to 31 are always zero in this mode.

Setting the Mode 4 Gig bit in the Enhanced Addressing Register (ESF:018CH) puts the WD6010 in Enhanced Mode. In this mode, the addresses roll over to 00000000 if they exceed FFFFFFFFH, instead of FFFFFFH.

When in this mode, all the channels generate 32-bit addresses. To program the memory addresses for thirty-two bits, four writes to the Memory Address Register should be executed in Extended Mode. To read back the memory addresses, four reads are executed to the same locations. Internally, the bytes are organized as Bytes 0, 1, 2, and 3. If the upper-most byte is not programmed, the old value is used. Therefore, care must be taken to program all the bytes with their proper values. Figure 12 shows the bit assignment for Register ESF:18CH.

3.4 DMA Operation

The state of the HLDA signal from the CPU distinguishes the operaion of the DMA controller. If HLDA is inactive, the operating mode of the DMA controller can be programmed. See Section 5, Arbitration Control, for more information. If HLDA is active, the DMA can only execute transfer cycles that have been set up previously.

To terminate a transfer, the DMA controller examines the state of the BURST signal. As long as this signal is active and the terminal count (TC) has not been reached, transfers continue to be executed. If BURST is inactive at the beginning of a transfer, a single transfer is executed.

3.4.1 Single Transfer Mode

This mode consists of one I/O bus cycle and one memory bus cycle, in either order. A single transfer is executed when BURST is found to be inactive at the beginning of a cycle.

3.4.2 Demand Transfer Mode

Demand transfers are continous transfers carried out as long ast the BURST signal remains active. They may be either slave-terminated or controller-terminated.

A slave-terminated transfer ends under either of two conditions. The transfer ends when the slave has transferred one byte or word and has not asserted the BURST signal, or when the slave has completed a partial transfer and releases BURST during the last I/O cycle.

A controller-terminated transfer can only end when the TC has been reached for that channel. At EOT, the channel is masked from further operation until the CPU interacts with it. Figures 13 to 15 provide timing diagrams of typical DMA operations in Demand Transfer Mode.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Reserved								**Mode**		**Reserved**				**Addressing**	
Bit 7		**Bit 6**		**Bit 5**		**Bit 4**		**Bit 3**		**Bit 2**		**Bit 1**		**Bit 0**	

0	80386 Mode
1	80386SX Mode

0	16 MByte Addressing
1	4 GByte Addressing

FIGURE 12. ENHANCED ADDRESSING REGISTER ESF:018CH

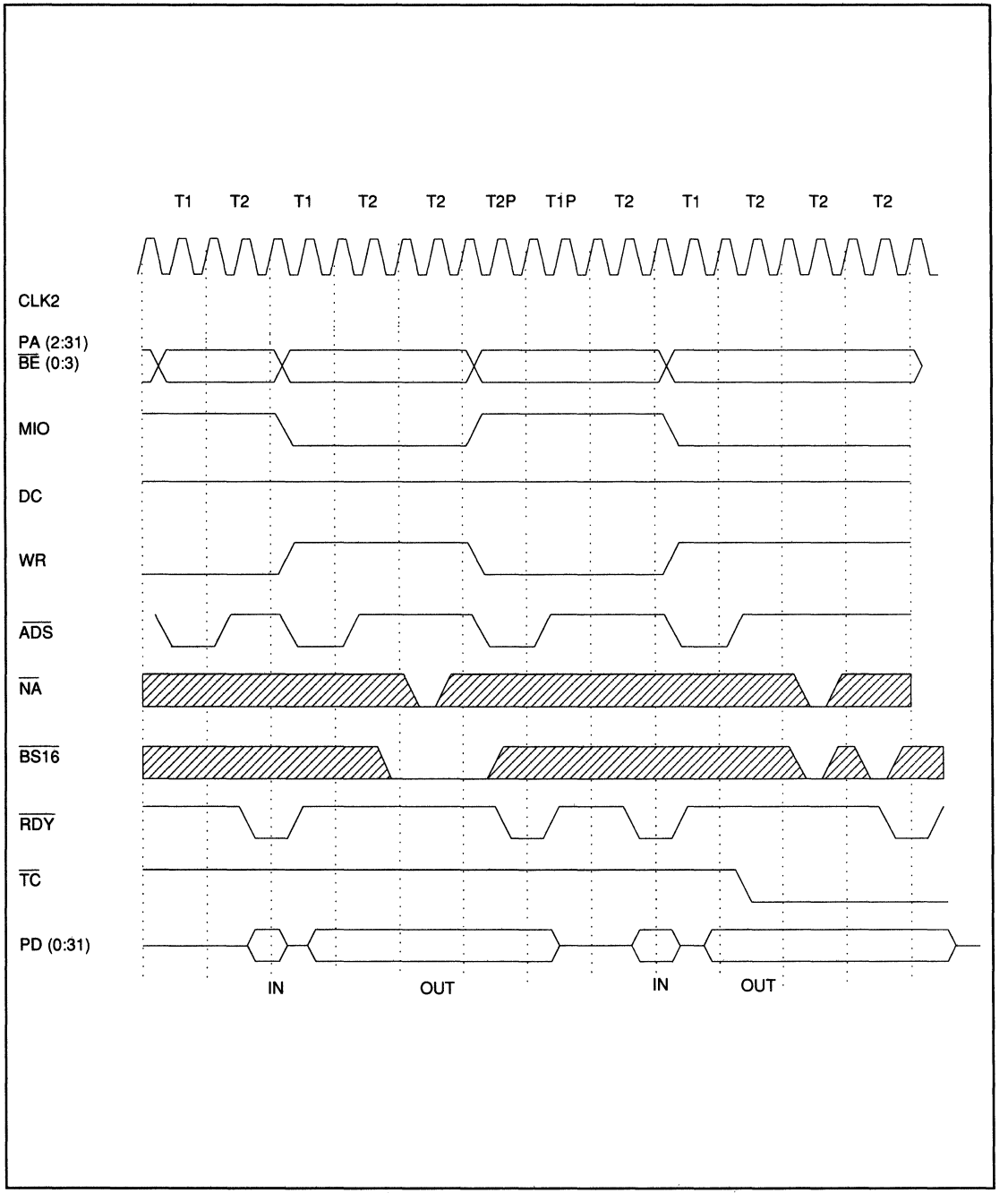


FIGURE 13. 16-BIT READ TRANSFER with COUNT EXPIRATION

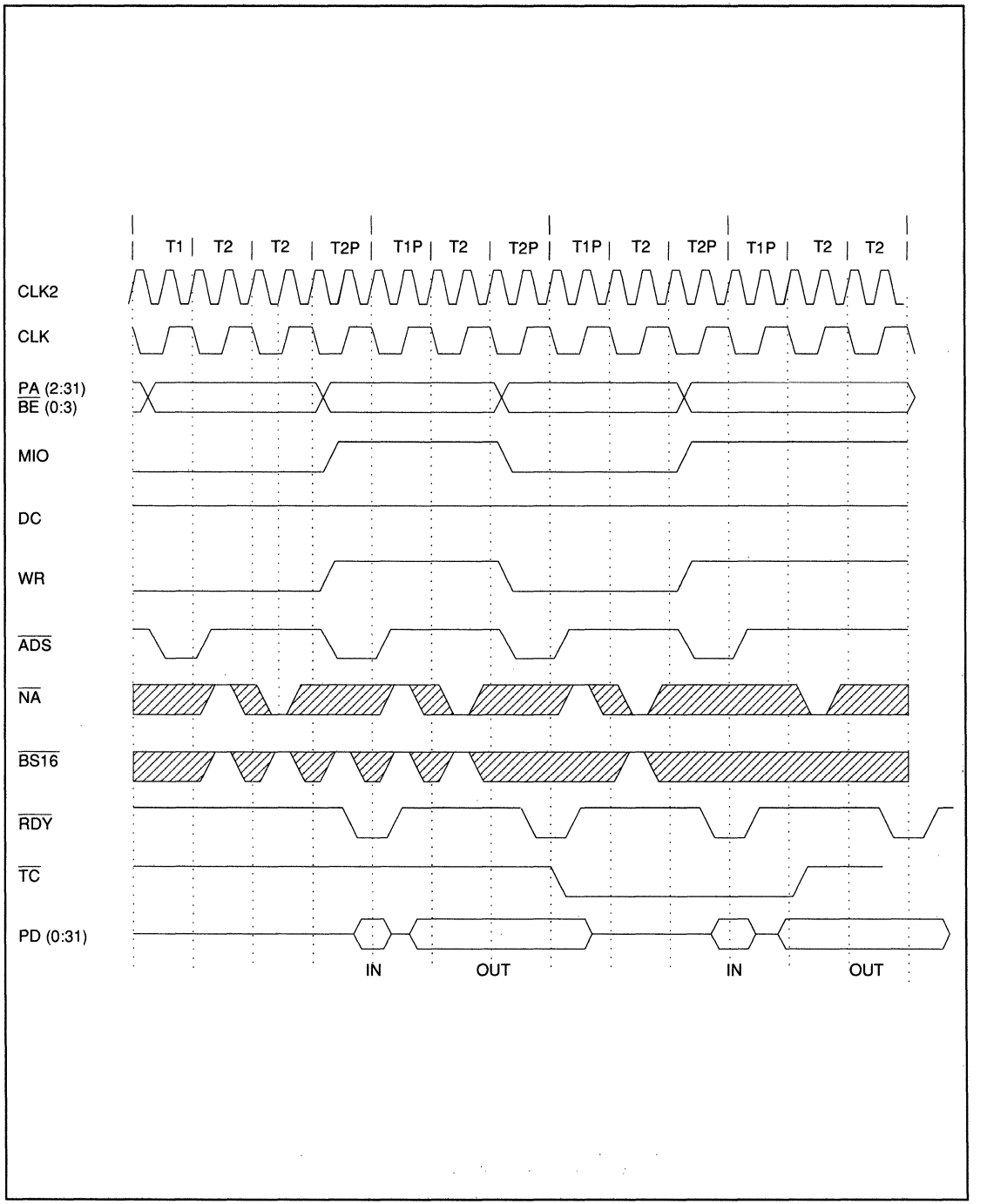


FIGURE 14. 16-BIT WRITE TRANSFER with COUNT EXPIRATION

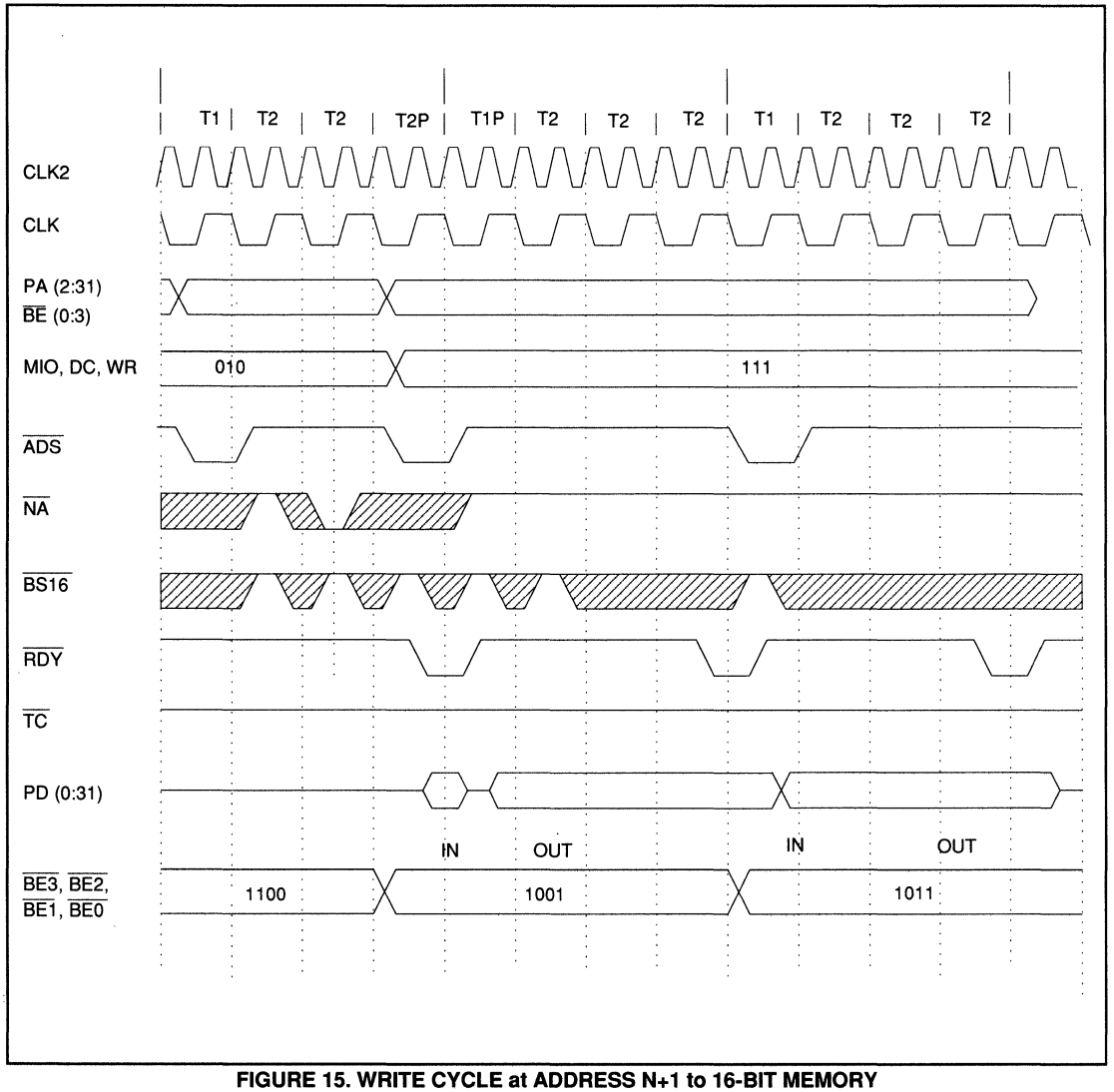


FIGURE 15. WRITE CYCLE at ADDRESS N+1 to 16-BIT MEMORY

3.4.3 Verify Mode

This mode performs address and $\overline{TC}$ generation as in normal transfers, but only initiates memory read commands on the bus. Figures 16 and 17 illustrate this mode through timing diagrams.

3.4.4 Submodes

Auto-initialize Mode allows a channel to operate continuously without interaction from the CPU. At EOT, the values in the Base Memory Address Registers are loaded into the Current Memory Address Registers; the channel remains unmasked.

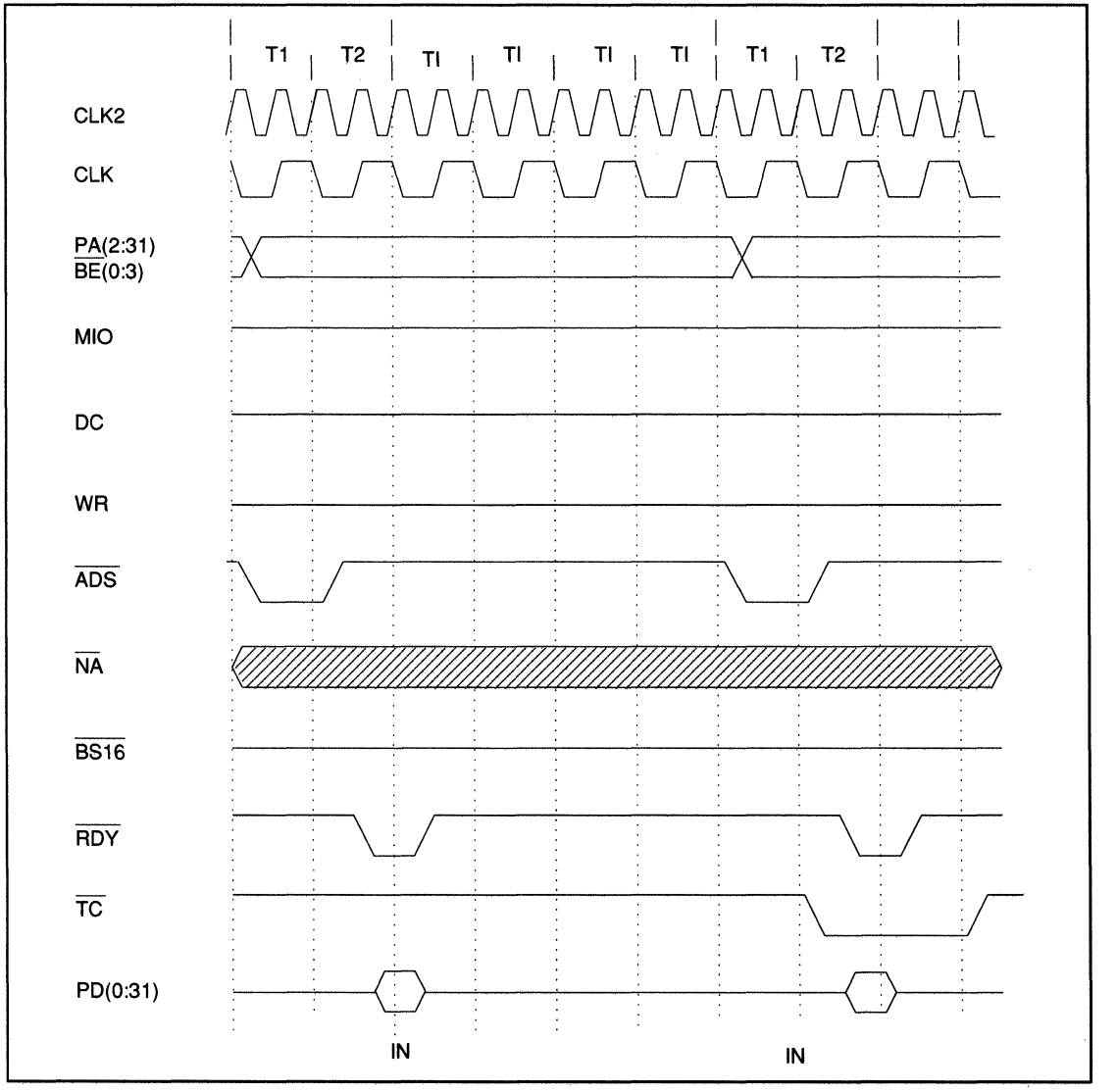


FIGURE 16. VERIFY TRANSFER with TRANSFER COUNT EXPIRATION

The Increment/Decrement submode can set each channel Memory Address Register to increment or decrement.

3.4.5 Boundary and End Conditions

When the Memory Address Register reaches the end of a 64 Kbyte segment of memory, it carries into the upper byte of the counter without indicating this to the CPU.

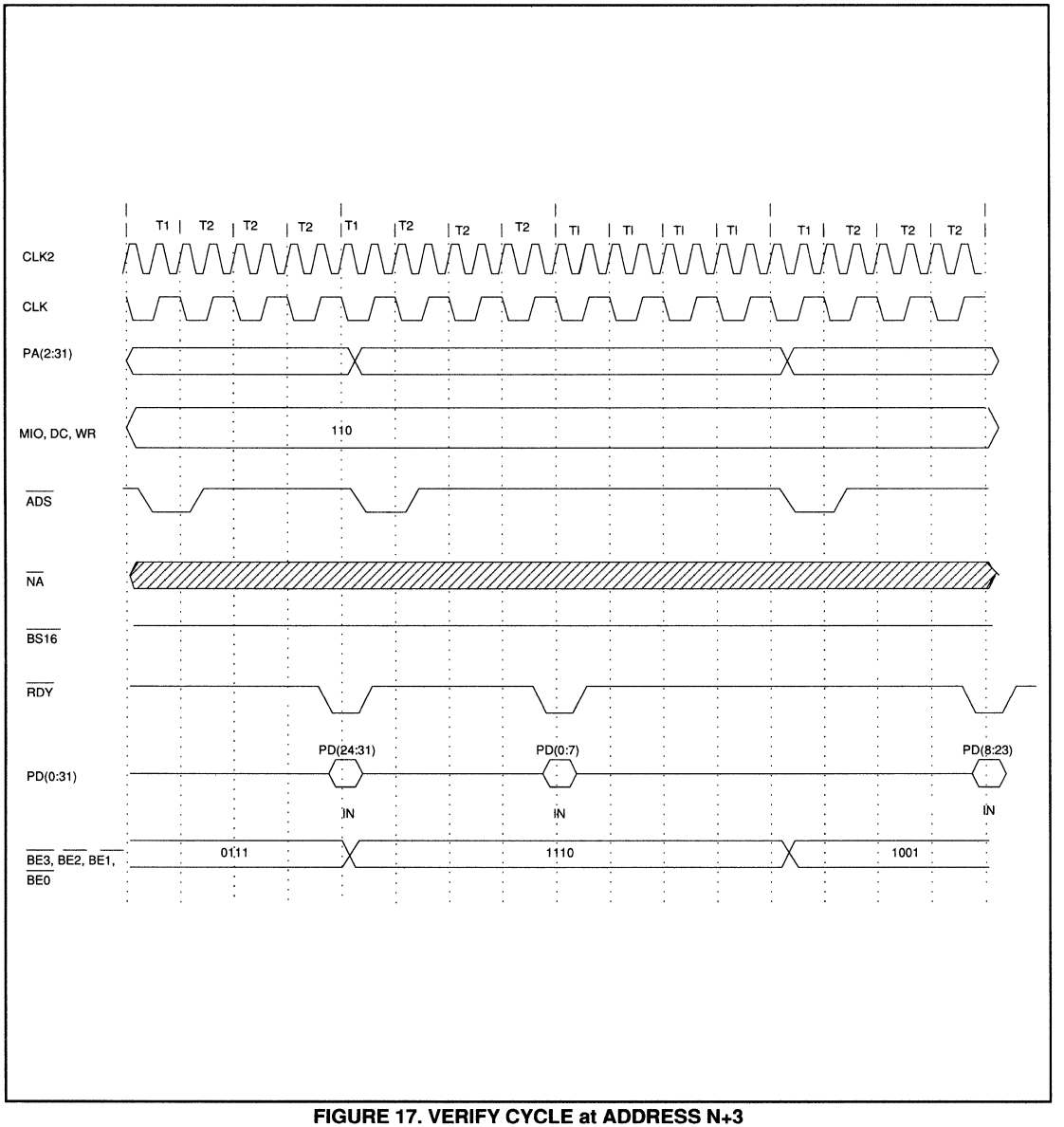


FIGURE 17. VERIFY CYCLE at ADDRESS N+3

With a 16M or 4 GByte physical memory limit, if the Current Transfer Count Register has a valid count remaining and the DMA slave continues to request service, the Current Memory Address Register rolls over to Address 0 and continues. If the transfer is a memory write, no warning is given of the alteration to low memory.

At $\overline{TC}$, the Current Transfer Count Register decrements to FFFFH and stops. If the register was initially set to FFFFH, the counter decrements until it encounters FFFFH again.

At EOT, the mask register bit is not set if Auto-Initialize was selected for that channel, as this would disable the channel.

3.4.6 Direct Commands

The Clear Byte Pointer command initializes the internal byte pointer to point to the least significant byte.

The Master Clear command sets the Mask Register to mask or disable all channels. It also resets all status bits to zeros.

The Clear Mask Register command unmasks or enables all the channels.

The Write All Register Mask Bits command masks or disables all the channels.

3.4.7 Enhanced Mode

Il the DMA operations described in this section are valid when the system is operating in Enhanced Mode. However, it must be remembered that all channels generate 32-bit addresses when in this mode, necessitating four read or write operations to program the memory addresses. See Section 3.3.3 for more information.

4.0 RESET CONTROL

The clock and reset control functions on the WD6010 include the generation of CPU resets, coprocessor resets, and general system resets.

The Alternate Hot Reset Function specified by Control Port A (0092H, Bit 0) is write-only in the WD6010 and read/write on the WD6000. Figure 19 shows the Clock and Reset control function in an WD6010-based system. The block diagram shows an WD6500 system; however, the same architecture applies to any system based on the WD6010.

The generation of different resets is described in the Pin Description Table.

The clock rates and the signal pins are shown in Table 5. The state of three signal pins at power-on reset (POR) determines the clock rates. After POR, the pins revert to their normal functions.

Frequency	UCHMSTR (F_1)	A20GTX (F_0)
16 MHz	0	1
20 MHz	0	0
25 MHz	1	1
33 MHz	1	0

TABLE 5. CLOCK RATE DEFINITIONS

12

5.0 ARBITRATION CONTROL (AC)

Arbitration Control controls and monitors the Channel and local bus arbitration functions. The AC functions are controlled by the bit settings in the Arbitration Register at 0090H. Figure 18 shows the format for the Arbitration Register.

5.1 Arbitration Register

The Arbitration Register (0090H) controls the different functional parameters of the CACP. Figure 18 shows the bit assignments for this register for read and write operations.

5.2 Arbitration Control Functions

The Central Arbitration Control Point (CACP) functions are discussed in more detail in the subsections that follow.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
CPU Cycles		NMI Occurred		Bus Timeout		IRQ Master Preempt		Arbitration Level							
ENA	DIS	Yes	No	Yes	No	ENA	DIS								
Read															
CPU Cycles		ARB State		ARB Cycle		IRQ Master Preempt		Reserved							
ENA	DIS	Arb	Gnt	Extd	Norm	ENA	DIS	—		—		—		—	
Write															
Default=															

FIGURE 18. ARBITRATION REGISTER FORMAT (0090H)

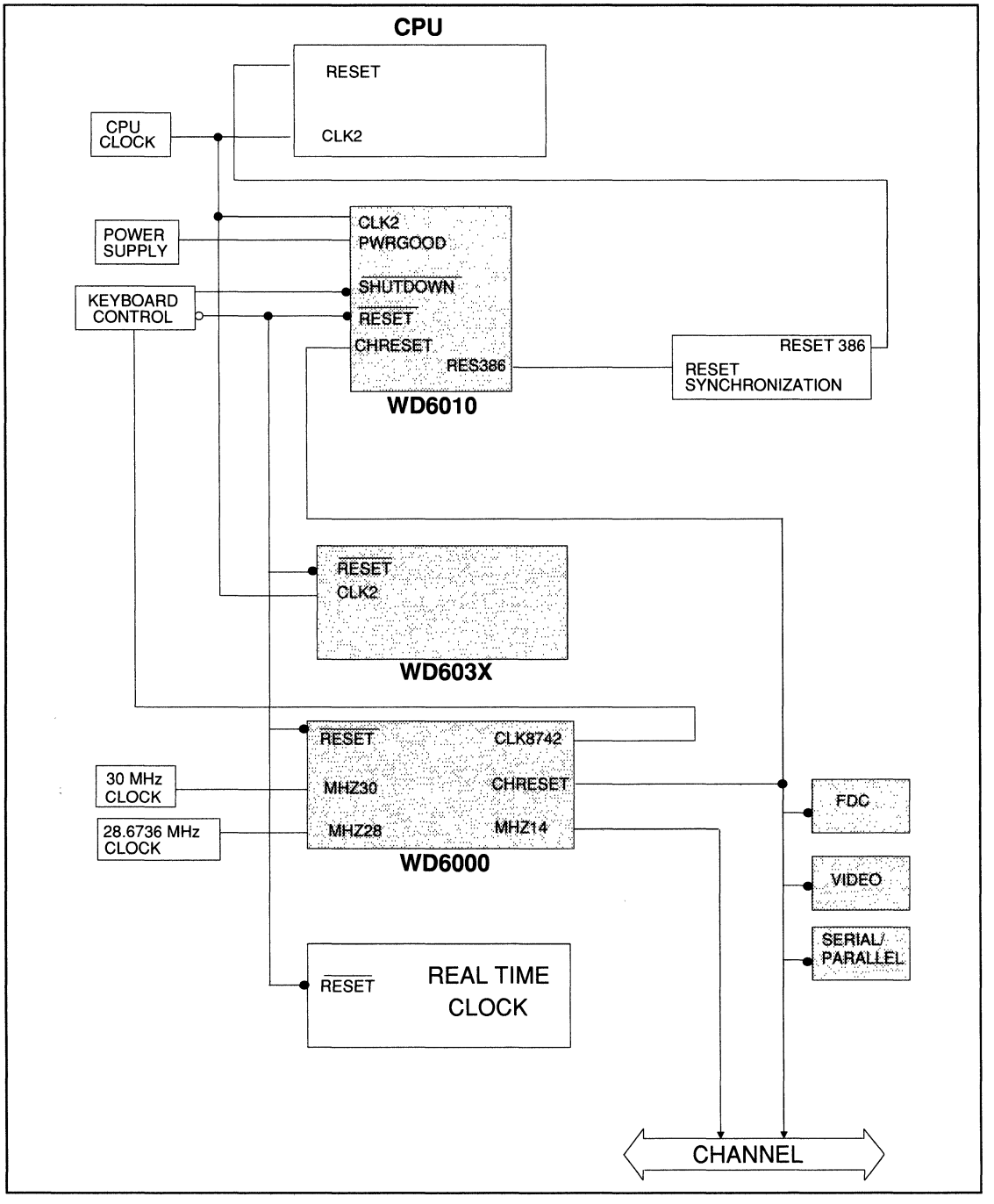


FIGURE 19. SYSTEM CLOCK and RESET CONTROL

5.2.1 Execute Arbitration Cycles

An arbitration cycle is defined as a transition of the ARB/GNT signal from low to high to low, GNT to ARB to GNT. When it is high (ARB), all competing local arbiters may drive ARB (0:3) to determine the new bus owner. Refresh cycles are executed when ARB/GNT is high and extend the arbitration cycle by that amount. An arbitration cycle can be initiated by these external requests:

- Refresh Request
- Bus Time-out
- Competing Bus Master
- Competing DMA Slave
- NMI
- Bus Idle
- Interrupt, When 0090H, Bit 4 is 1

The bus is at an idle state when a Bus Master or DMA slave has been granted the bus, and CMD, and BURST are not active. It indicates a condition when DMA slave or Bus Master transfers have been executed.

5.2.2 Arbitrate the Local CPU Bus

Bus cycles originating from the DMA slave, Channel bus master, or refresh requests require the CPU to give up the local bus. This arbitration request function is performed by the CACP.

5.2.3 Regulate Arbitration Cycle Duration

5.2.3.1 CPU-Programmable

When Bit 5 of the Arbitration Register (0090H) equals one, the default arbitration cycle is extended from a minimum of 300 ns to a maximum of 750 ns, depending on the CPU clock rate. Table 6 defines this relationship.

CPU Clock	Arbitration Control Register	
	Bit 5=0	Bit 5=1
16 MHz	312.5 ns	750 ns
20 MHz	300 ns	750 ns
25 MHz	300 ns	750 ns
33 MHz	300 ns	750 ns

TABLE 6. EXTENDING ARBITRATION

5.2.3.2 ARB (0:3) = 0000 Special Case

If the Arbitration bus changes to 0000 during an arbitration cycle, the arbitration cycle can be shortened to a minimum of 100 ns.

5.2.3.3 Dynamic Extension of Arbitration Time

Arbitration time can be extended by an NMI or Refresh cycle. The NMI sets Bit 6 of the Arbitration Register to one, which forces the ARB/GNT signal to ARB until the CPU resets that bit to zero.

5.2.4 Arbitration Monitor

Since the Channel arbitration mechanism is distributed between the system board and the Micro Channel-based peripherals, a central monitoring point is needed to allow for error recovery. The CACP monitors the Channel bus, and when a bus master does not release the bus as requested by an asserted PREEMPT signal, it hands system control to the CPU, so that the CPU can initiate error recovery.

When a bus time-out occurs, the CACP captures the arbitration level of the device and generates an NMI. The DMA controller is also reset to allow the CPU to attempt error recovery.

The time-out mechanism is based on the refresh timer which cycles approximately every fifteen microseconds. The time-out is armed when a refresh request is pending and when the arbiter is in any state except refresh. If the refresh request is not honored before the next refresh request, a channel time-out condition is said to exist.

The channel time-out and the resulting NMI are held asserted until cleared by a write from the CPU which resets Bit 6 of the Arbitration Register to zero.

5.2.5 Floppy Disk Controller/DMA Interface

On behalf of the floppy disk controller, this function competes for ownership of the system bus by converting DMA requests such as FDDRQ and DACK into the appropriate signals for the CACP.

5.3 PREEEMPT GENERATOR

The WD6010 generates the PREEMPT signal in certain situations, which are described below.

5.3.1 Floppy Disk Controller Request

The CACP generates a $\overline{\text{PREMPT}}$ signal on behalf of the floppy disk controller when the floppy disk controller issues a FDDRQ, and Floppy DMA Controller Channel 2 is not masked. This signal is cleared when a DMA Master Clear command is received or when the bus has been won by Floppy Disk DMA Channel 2 after a bus arbitration cycle.

5.3.2 Refresh Request

A refresh request is made when the $\overline{\text{ARB/GNT}}$ line is in the GNT state will cause a $\overline{\text{PREEMPT}}$ signal to be asserted.

5.3.3 Arbitration Register Bit 6 Set

A $\overline{\text{PREEMPT}}$ is asserted when the ARB/$\overline{\text{GNT}}$ line is in the GNT state and Arbitration Register Bit 6 is set and the ARBUS value is set with any ARB value but a system board value, that is, other than 0FH.

5.3.4 Interrupt Request

A $\overline{\text{PREEMPT}}$ signal is asserted when the ARB/$\overline{\text{GNT}}$ line is in the GNT state, ARB (3:0) $\neq$ 1111B, Arbitration Register Bit 4 is set, and an interrupt request to the CPU is active.

6.0 DECODES

The addresses used by the system control functions are listed below.

1. The ESF Pointer Register (EPR), located at FFFFDH or FFFF, FFFDH, is used to decode the ESF Data Register (EDR).

2. Setup Mode Timing Strobe ($\overline{\text{CDSETEN}}$)

3. The VGA Enable Register (03C3H)

4. Refresh Address Generator (11 bits)

The VGA Enable Register (03C3H) format is defined in Figure 20. When Bit 0 is set to one, an access to an address space below 1 MByte asserts VGAEN, which indicates that the video subsytem is enabled.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Reserved														VGA Subsystem	
—		—		—		—		—		—		—		ENA	DIS

FIGURE 20. PVGA REGISTER FORMAT

7.0 HALF-SPEED INTERFACE

This interface runs the NPX at half the speed of the CPU, permitting the designer to utilize a slower numeric coprocessor to implement a more cost-effective version. For example, when the CPU is running at 25 MHz, it allows the NPX to operate at 12.5 MHz. When used in half-speed mode, the CLK2387 of the NPX has the same frequency as the CLK signal on the WD6010. The reset signal for the NPX (RES387) must be synchronized to the NPX primary clock (CLK2387) with the proper setup and hold times so that CLK387 has the same phase relationship as the internal CLK of the NPX. The phase relationship and clock frequency are set up at power up, and once set, can not be changed.

Figure 21 shows a block diagram of the NPX half-speed interface, and Figure 22 contains a timing diagram of this interface.

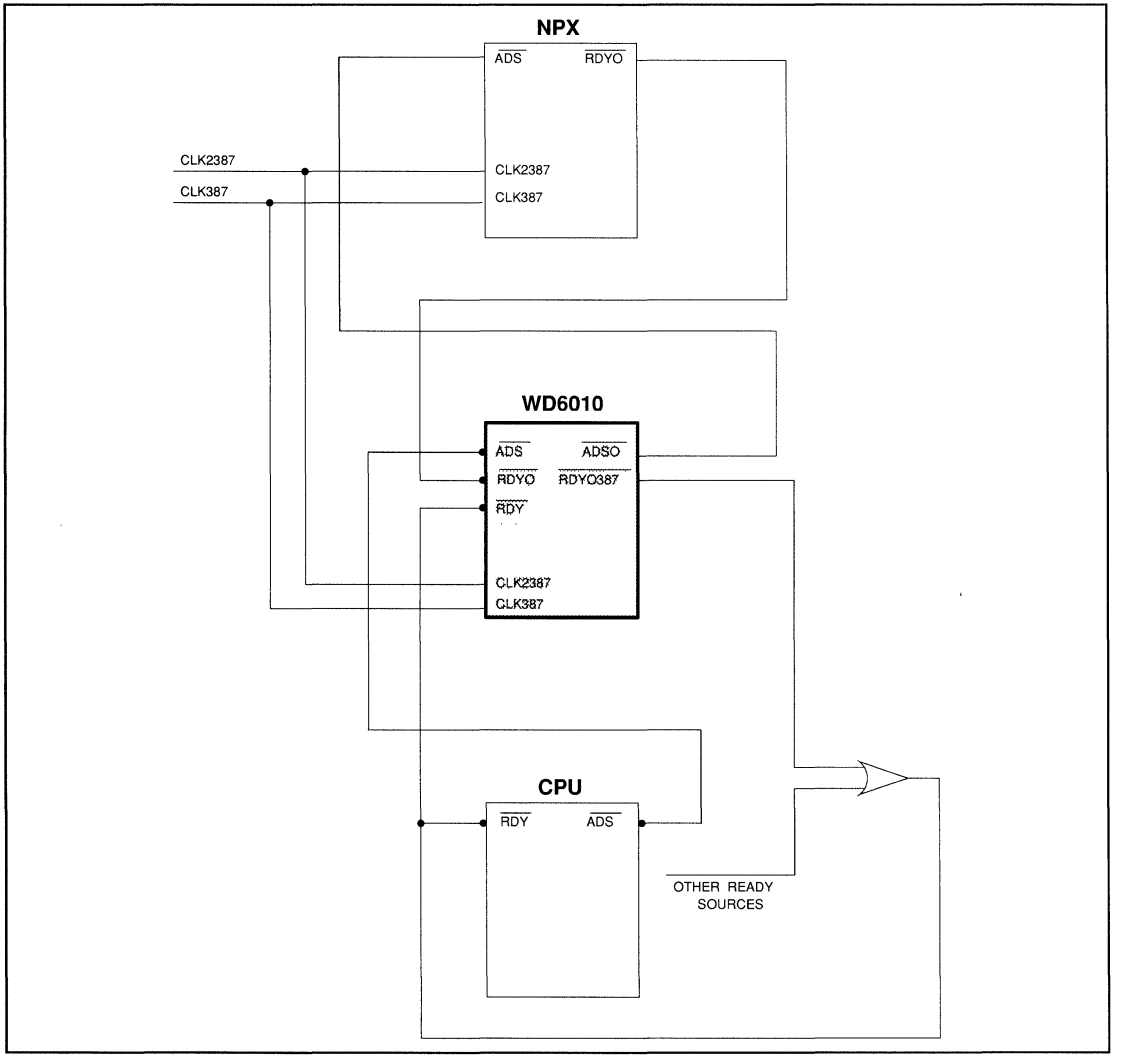


FIGURE 21. NPX HALF-SPEED INTERFACE

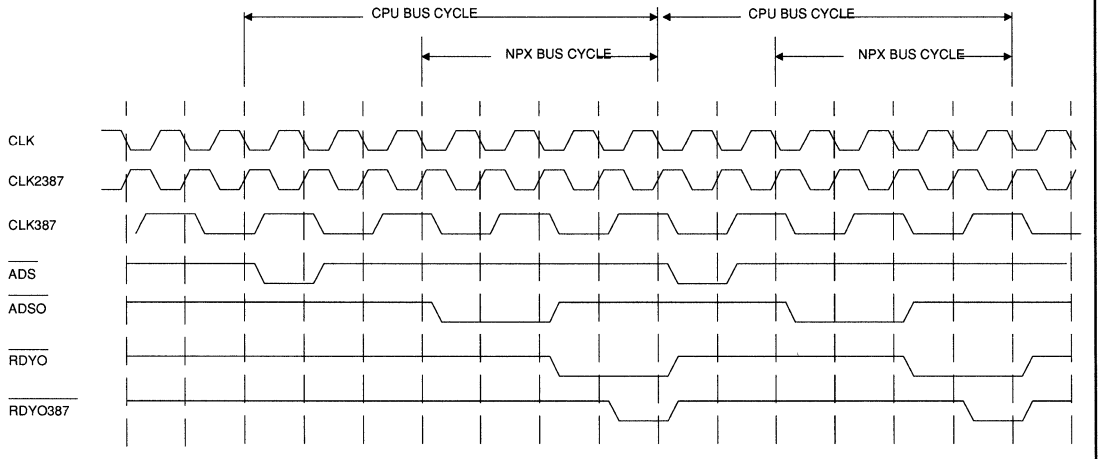


FIGURE 22. NPX HALF-SPEED INTERFACE TIMING DIAGRAM

8.0 DIAGNOSTIC INTERFACE

This logic allows the state of the Micro Channel bus to be latched on a Channel Check condition and is useful to diagnose faults in the system. The error recovery interface is compatible with the Model 80-071.

On a Channel Reset, the latching of the channel state is enabled. At the leading edge of each CMD or MMCMD, the channel state is latched. When a Channel check takes place, the latching is disabled, and the last channel state is retained. The current channel state can be read by the CPU at I/O Locations 00E2H - 00E6H. An I/O Read at 00E7H returns the state of local bus DC pin (Bit 0), and enables the latching again.

The diagnostic signals are described in Section 2. The six read-only diagnostic registers are described here:

- PA (24:31)- 00E2H
- PA (16:23)- 00E3H
- PA (8:15)- 00E4H
- ARB/$\overline{GNT}$, M/$\overline{IO}$, PA (2:7)- 00E5H
- $\overline{BE}$ (0:3), ARB (0:3)- 00E6H
- DC, RESERVED- 00E7H

8.1 Diagnostic Register 1

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA31		PA30		PA29		PA28		PA27		PA26		PA25		PA24	

A Read at this location, 00E2H, gives the last latched state of the bus.

8.2 Diagnostic Register 2

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA23		PA22		PA21		PA20		PA19		PA18		PA17		PA16	

A Read at this location, 00E3H, gives the last latched state of the bus.

8.3 Diagnostic Register 3

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA7		PA6		PA5		PA4		PA3		PA2		M/$\overline{IO}$		ARB/$\overline{GNT}$	

A Read at this location, 00E4H, gives the last latched state of the bus.

8.4 Diagnostic Register 4

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA7		PA6		PA5		PA4		PA3		PA2		M/$\overline{IO}$		ARB/$\overline{GNT}$	

A Read at this location, 00E5H, gives the last latched state of the bus.

8.5 Diagnostic Register 5

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
ARB3		ARB2		ARB1		ARB0		$\overline{BE3}$		$\overline{BE2}$		$\overline{BE1}$		$\overline{BE0}$	

A Read at this location 00E6H, gives the last latched state of the bus.

8.6 Diagnostic Register 6

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	9	1	0	1	0	1	0
Reserved														DC	

A Read at this location, 00E7H, gives the last latched state of the bus. It also enables the relatching of the channel state.

9.0 EXTENDED SETUP FACILITY(ESF)

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable (EDRENA) output from the WD6010 to the WD6000. ESF is designed to extend the configuration architecture established with POS features. See Figures 23 and 24 for an overview of the ESF function. ESF supports:

- Memory Map Control Registers
- Additional Physical Serial Port (SP2)
- Programmable Port Enables A and B
- EMS Control Registers
- External DRAM Control Configuration
- System Board LAN Configuration
- Customer-specified Enhancements that include
- System Identification
- System Version

9.1 ESF Access

ESF is based on an "alternate I/O space" concept similar to the way in which the Extended CMOS RAM feature was implemented by IBM. ESF space, which consists of 128 locations, expandable to 32K, is accessed through a single "real I/O space" window called the ESF Data Register (EDR). ESF space may be implemented as word-wide or byte-wide, at the discretion of the designer.

The write-only ESF Pointer Register (EPR), configurable by the software, points to the EDR. It is loaded by writing to memory location FFFFFDH or FFFF, FFFDH, a PROM location. The power-on default location for the EDR is at I/O Address 0700H.

1. Set the value 8DH in Port 0070H to disable NMI.

2. Read System Control Port B at 0061H, and test for a change in the state of Bit 4 (Refresh Toggle) to synchronize it with the refresh circuitry.

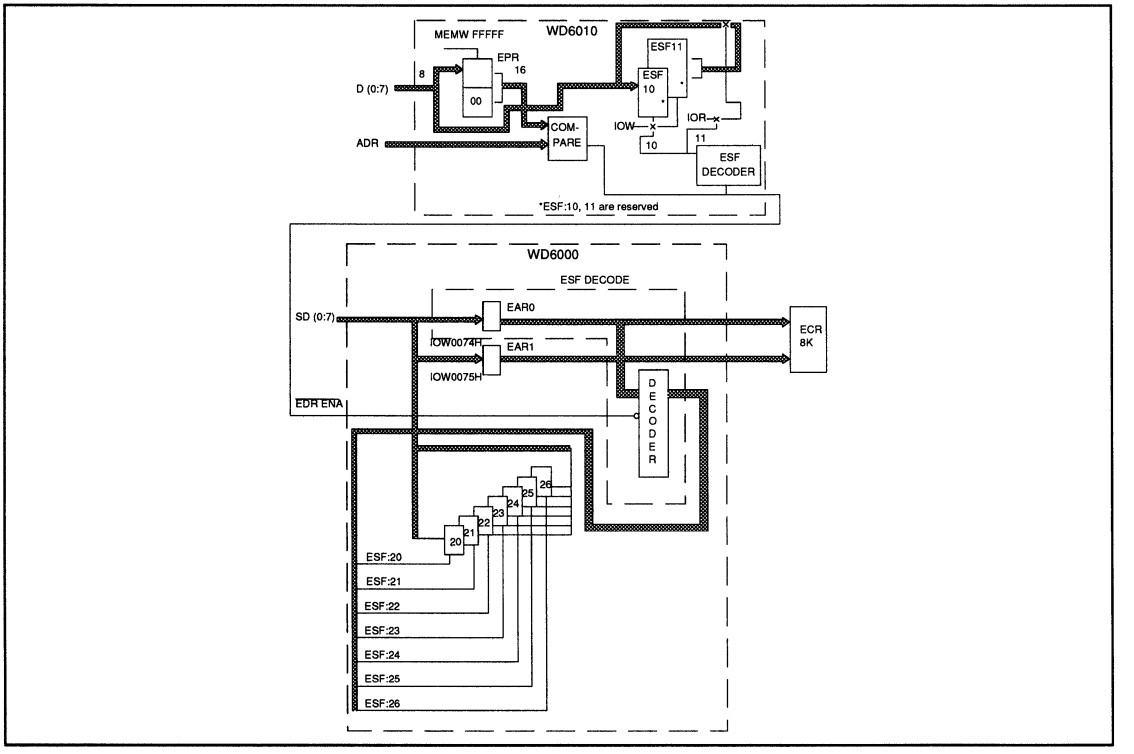


FIGURE 23. ECR & ESF BLOCK DIAGRAM

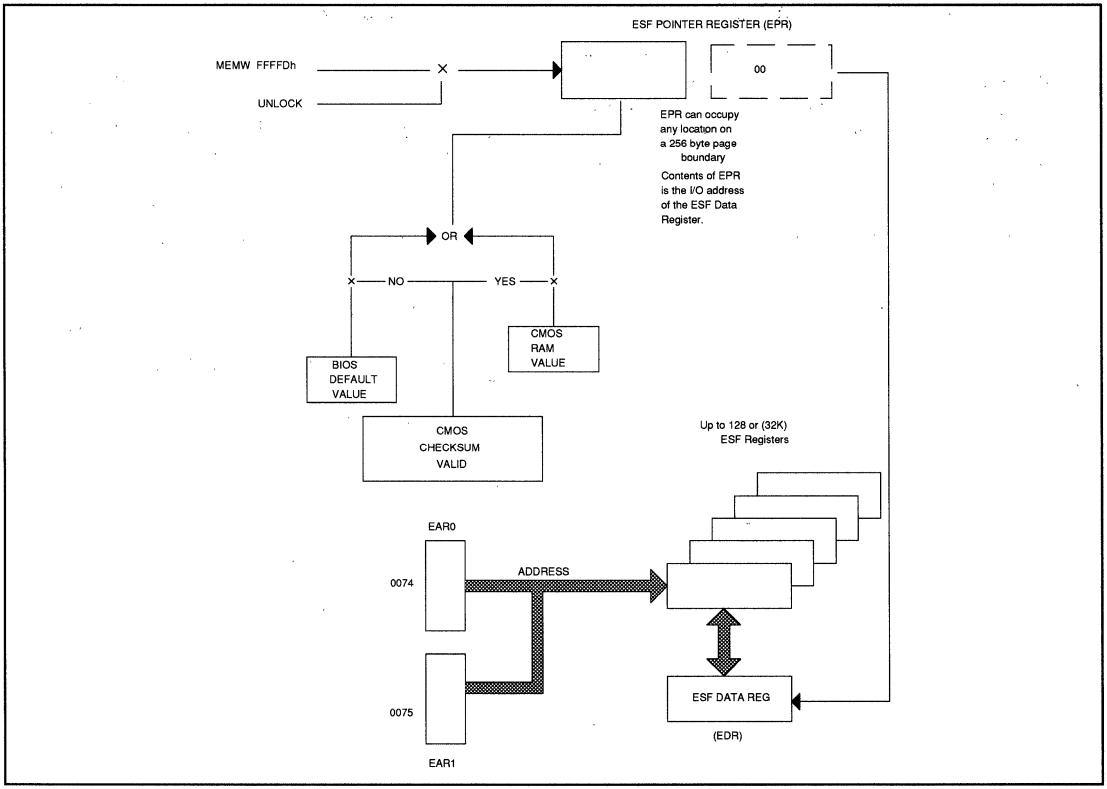


FIGURE 24. EDR and ESF BLOCK DIAGRAM

3. Read EAR0 at 0074H, (normally write-only) to unlock the EPR.

4. Write the new value into the EPR (at FFFFDH). This locks the EPR once again.

5. Enable $\overline{\text{NMI}}$ if required.

Note that the EPR is locked when written, or on the next refresh cycle, whichever occurs first.

The value in EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K I/O space of the CPU from 0400H to FF00H.

To address the ESF I/O space:

1. Write 8DH to Port 0070H to disable $\overline{\text{NMI}}$.

2. Write the address value to EAR0 at 0074H (and EAR1if expanded ESF is being used).

3. Issue an I/O Read or Write command to the EDR address.

The selected ESF register is determined by decoding the EAR0 address value.

9.2 ESF ADDRESS MAPS

The lower 64 bytes (EAR0 = 00H - 3FH) are reserved for Western Digital functions and features. The upper sixty-four bytes (40H -7FH) can be used by the customer. (see Table 7 for details). All functions using ESF must include Bit 7 of EAR0 in the decode. This bit must be 0 when addressing only 128 ESF registers. To expand the ESF to 32,768 location, set EAR0 Bit 7 to 2 and write the second ESF address byte to EAR1.

ESF ADDRESS	FUNCTION
00H-0FH	System reserved
10H-1FH	System board core functions
20H-3FH	System board peripheral functions

ESF ADDRESS	FUNCTION	R/W	WD6500 DEVICE	WD6400SX/(LP) DEVICE
0 - 001FH	Reserved	-	-	-
20H	Peripheral Configuration	R/W	WD6000	WD6000
21, 24H	Port A,B Control	R/W	WD6000	WD6000
22, 25H	Port A,B Address (LSB)	R/W	WD6000	WD6000
23, 26H	Port A,B Address (MSB)	R/W	WD6000	WD6000
30-3FH	Reserved	-	-	-
40 - 7FH	Customer-specified	-	-	-
0180H	Memory Configuration	R/W	WD6030	WD6036SX/(LP)
0181H	Memory Size Register	R/W	WD6030	WD6036SX/(LP)
0182H	Bank Enable Register	R/W	WD6030	WD6036SX/(LP)
0183H	Split Address Extension	R/W	WD6030	N/A
0184H	Memory Window Bank 0	R/W	WD6030	WD6036SX/(LP)
0185H	Memory Window Bank 1	R/W	WD6030	WD6036SX/(LP)
0186H	Memory Window Bank 2	R/W	WD6030	WD6036SX/(LP)
0187H	Memory Window Bank 3	R/W	WD6030	WD6036SX/(LP)
0188H	CAS Pulse Width	R/W	WD6030	WD6036SX/(LP)
0189H	RAS PreCharge Delay	R/W	WD6030	WD6036SX/(LP)
018AH	RAS Pulse Width	R/W	WD6030	WD6036SX/(LP)
018BH	RAS Access Time	R/W	WD6030	WD6036SX/(LP)
018CH	Enhanced Addressing	R/W	WD6010	N/A
018DH	Reserved	-	-	-
018EH	Reserved	-	-	-
18FH	System Control Register[1] System Configuration[2]	R/W ***	WD6030	WD6036SX/(LP)

TABLE 7. MICRO CHANNEL COMPATIBLE ESF REGISTERS

1. WD6500 implementation only.
2. WD6400SX(LP) implementation only.
*** Dependent on the state of the UCHMASTER and A20GTX signals at reset.

10.0 80386/80486 80386SX ENVIRONMENTS

As described before, the WD6010 can be configured to be used in either an 80386/80486-based system or an 80386SX-based system. The differences in usage in these two environments is summarized in this section.

Certain signals, listed below, have been provided with weak internal pull-ups to ease system design:

- PA (24:31)20K internal pull-up
- PD (16:31)20K internal pull-up
- $\overline{\text{DACK}}$20K internal pull-up
- $\overline{\text{BE}}$ (0:3)20K internal pull-up

When using an 80386/80486-based system, the following points should be noted:

- PD (0:31) connect to the 80386/80486 data lines (0:31)
- PA (2:31) connect to the 80386/80486 address lines (2:31)
- $\overline{\text{BE}}$ (0:3) connect to the 80386 byte enables (0:3).
- The WD6010 $\overline{\text{BS16}}$ connect to the 80386 bus size 16.

When using a 80386SX-based system, the following points should be noted:

- PD (0:15) connect to the 80386SX data lines (0:15), PD (16:51) are left unconnected.
- PA (2:23) connect to the 80386SX address lines (2:23), PA (24:31) are left unconnected.
- $\overline{\text{BE}}$ (0:1) connect to the 80386SX $\overline{\text{BEL}}$ and BEH respectively, BE2 connect the 80386SX address line 1. BE3 is left unconnected.
- BS16 is tied to GND.

11.0 TECHNICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

The absolute maximum stress ratings for the WD6010 device are tabulated below. Permanent damage to the device could result from exposing it to conditions exceeding these ratings.

11.2 Normal Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD} - V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Bias on Output Pin	V_{OABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	TS	-40	125	°C

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long-term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD} + 0.3	V
Power Dissipation	PW	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

12

11.3 DC Characteristics (under Normal Operating Conditions)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input Capacitance @ fc = 1 MHz	CI	–	5	pF
*I/O Capacitance	C_{IO}	–	10	pF
Logic High Input Voltage	V_{IH}	2.0	–	V
Logic Low Input Voltage	V_{IL}	–	0.8	V
*Input Leakage	I_{IL}	–	±10	µA
*Tri-state Output Leakage	I_{OL}	–	±30	µA
*I/O Pin Leakage	I_{IOL}	–	±40	µA
OUTPUTS $\overline{BE}$(0:3), M/$\overline{IO}$, DC, WR, $\overline{ADS}$				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	24	µA
OUTPUTS $\overline{TC}$, ARB (0:3), $\overline{PREEMPT}$, ARB/$\overline{GNT}$, $\overline{REFRESH}$				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	24	µA
ALL OTHER OUTPUTS				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	4	µA

NOTES:

Underlined signals are open collector outputs.

Signals PA (24:31), $\overline{BE3}$, PD(16:31), and $\overline{DACK}$ have internal pullups of 20K.

When $\overline{TEST}$ = 0, all outputs and bi-directional signal lines are tristated.

*Pins ARB (0:3) $\overline{NMI}$ and $\overline{PREEMPT}$ are open collector outputs. Source current value does not apply. External pullups are required on these outputs.

11.4 A.C. Test Loads

OUTPUTS	SYMBOL	MIN	MAX	UNITS
$\overline{BE}$(0:3), WR, M/$\overline{IO}$, DC, $\overline{ADS}$*	CL	-	75	pF
PA(2:31), PD(0:31)*	CL	-	120	pF
ARB(0:3), $\overline{PREEMPT}$	CL	-	200	pF
$\overline{TC}$, ARB/$\overline{GNT}$, $\overline{REFRESH}$	CL	-	240	pF
ALL OTHER OUTPUTS	CL	-	50	pF

NOTE

1.PA(2:31), $\overline{BE}$(0:3), PD(0:31), $\overline{ADS}$, M/IO, DC, WR, ARB(0:3), $\overline{PREEMPT}$, and NMI are bi-directional signals.

2.UCHMSTR, A20GTX, and DACK are inputs only at power-up; they are outputs the rest of the time.

3.$\overline{TC}$ is a tristate output signal.

4.ARB(0:3), $\overline{PREEMPT}$, and NMI are open collector signals and require external pullups.

*These signals are tested at 50 pF for the 25 and 33 MHz frequency.

12

12.0 TIMING

The following inputs are asynchronous to CLK2: A20GATE, PREEMPT, BURST, EOT, FDDRQ, REFREQ, CHCK, CHRESET, UCHCMD, NMI, INTR, SHUTDOWN, PWRGOOD, and ARB(0:3).

The following outputs are asynchronous to CLK2: ARB/GNT, ARB(0:3), DACK, REFRESH, UCHMSTR, A20GTX, RES386, RES387, RESET, and ENPCHK.

The timings in the following table are in nanoseconds, except where specified.

PARAMETER	DESCRIPTION	MIN	MAX	NOTE
T1A	PREEMPT on to EOT	0	7.8 µs	–
T2A	ARB/GNT high from EOT	30	–	1
T3A	PREEMPT off from ARB/GNT low	0	50	–
T4A	BURST on from ARB/GNT low	–	50	–
T5A	ARB/GNT high	300	–	–
T6A	Driver turn-on delay from ARB/GNT high	0	50	–
T7A	Driver turn-off delay from ARB/GNT high	0	50	–
T8A	Driver turn-on delay from higher priority line	0	50	–
T9A	ARB [0:3] stable before ARB/GNT low	10	–	–
T10A	Tristate drivers from ARB/GNT high	–	50	–

TABLE 8. ARBITRATION CYCLES

NOTE
1 EOT signifies the End of Transfer on the Channel with Chs[0:1], BURST, and CMD off.

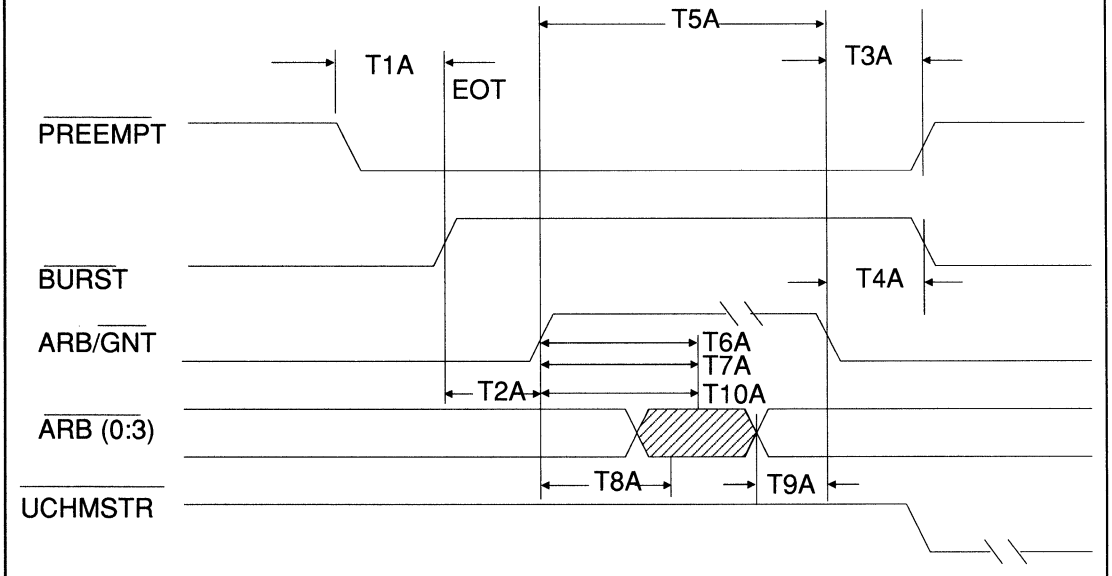


FIGURE 25. ARBITRATION TIMING

Parameter	Description	16 MHz		20 MHz		25 MHz		33 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
T1B	FDDRQ on to $\overline{\text{PREEMPT}}$ on	25	-	20	-	15.6	-	12	-
T2B	ARB/$\overline{\text{GNT}}$ high to $\overline{\text{DACK}}$ off	0	-	0	-	0	-	0	-
T3B	ARB/$\overline{\text{GNT}}$ high to HOLD on	0	-	0	-	0	-	0	-
T4B	ARB/$\overline{\text{GNT}}$ high to HOLD off	0	-	0	-	0	-	0	-
T5B	HLDA to ARB/$\overline{\text{GNT}}$ low	25	-	20	-	15.6	-	12	-

TABLE 9. FLOPPY REQUEST CYCLES (ns)

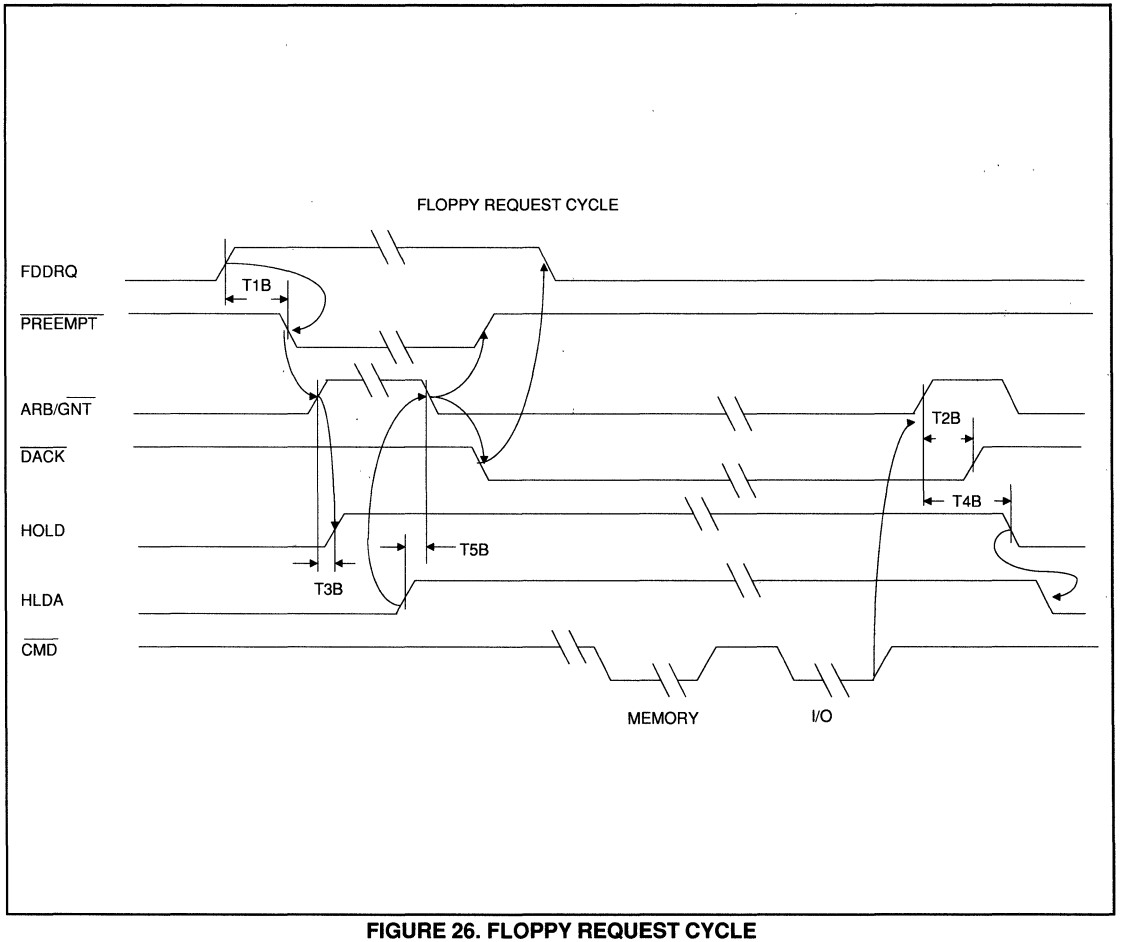


FIGURE 26. FLOPPY REQUEST CYCLE

Parameter	Description	33 M Hz		16 M Hz		20 MHz		25 MHz		Notes
Operating Frequency		8	33	4	16	4	20	4	25	MHz
CLOCKS										
T1C	CLK2 Period	15	62.5	31.25	125	25	125	20	125	@ 2V
T2AC	CLK2 High Time	4.25	-	5	-	5	-	4.5	-	@(V_{DD}-0.8V)
T2BC	CLK2 High Time	6.25	-	9	-	8	-	7	-	@ 2V
T3AC	CLK2 Low Time	4.25	-	7	-	6	-	4.5	-	@ 0.8V
T3BC	CLK2 Low Time	6.25	-	9	-	8	-	7	-	@ 2V
T4C	CLK Period	30	125	62.5	250	50	250	40	250	-
T5C	CLK High Time	8	-	20	-	14	-	10	-	-
T6C	CLK Low Time	8	-	15	-	12	-	10	-	-
T7C	CLK2387 Period	30	12.5	62.5	250	50	250	40	250	-
T8C	CLK2387 HighTime	8	-	-	-	-	-	10	-	-
T9C	CLK2387 Low Time	8	-	-	-	-	-	10	-	-
T10C	CLK387 Period	60	125	12.5	500	100	500	80	-	-
T11C	CLK387 High Time	12	-	-	-	-	-	17	-	-
T12C	CLK387 Low Time	12	-	-	-	-	-	17	-	-

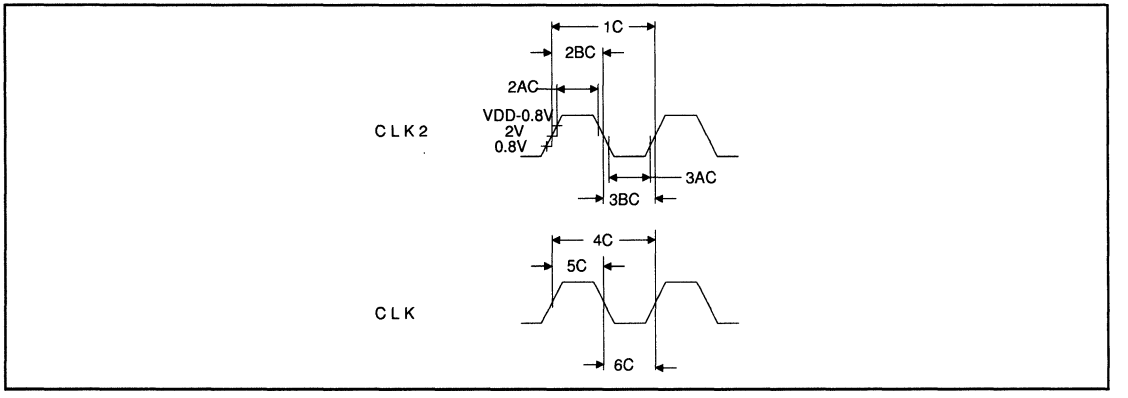


FIGURE 27. INPUT CLOCK TIMING SPECIFICATIONS

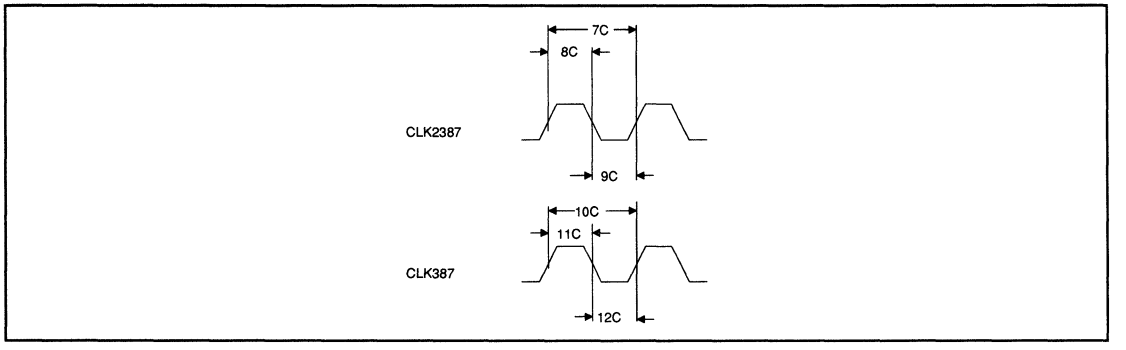


FIGURE 28. INPUT CLOCK SPECIFICATIONS II

DMA OPERATION - OUTPUTS										
Parameter	**Description**	**16 MHz**		**20 MHz**		**25 MHz**		**33 MHz**		**Notes**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
	PA (31:2), $\overline{BE}$ (3:0)									
T1D	VALID	2	38	2	32	2	24	2	15	
T2D	DISABLE	2	38	2	32	2	24	2	15	
	M/$\overline{IO}$, DC, WR, $\overline{ADS}$									
T3D	VALID	4	35	4	30	2	21	2	15	
T4D	DISABLE	4	35	4	30	4	21	2	15	
	REGISTER READ									
T5D	PD (31:0) VALID	2	75	2	75	2	75	2	75	
T6D	PD (31:0) DISABLE	2	75	2	75	2	75	2	75	
	DMA WRITE									
T7D	PD (31:0) VALID	2	50	2	40	2	27	2	24	
T8D	PD (31:0) DISABLE	2	35	2	27	2	22	2	17	
	HOLD									
T9D	VALID	4	35	4	30	4	24	2	19	
T10D	DISABLE	4	35	4	30	4	24	2	19	
	TC									
T11D	VALID	4	25	4	25	4	25	4	25	
T12D	DISABLE	4	25	4	25	4	25	4	25	

NOTE:
1. LOADING CAPACITANCE = 120 Pf for16 and 20 MHz, 50 Pf for 25 and 33 MHz.
2. LOADING CAPACITANCE = 75 Pf for 16 and 20 MHz, 50 Pf for 25 and 33 MHz.

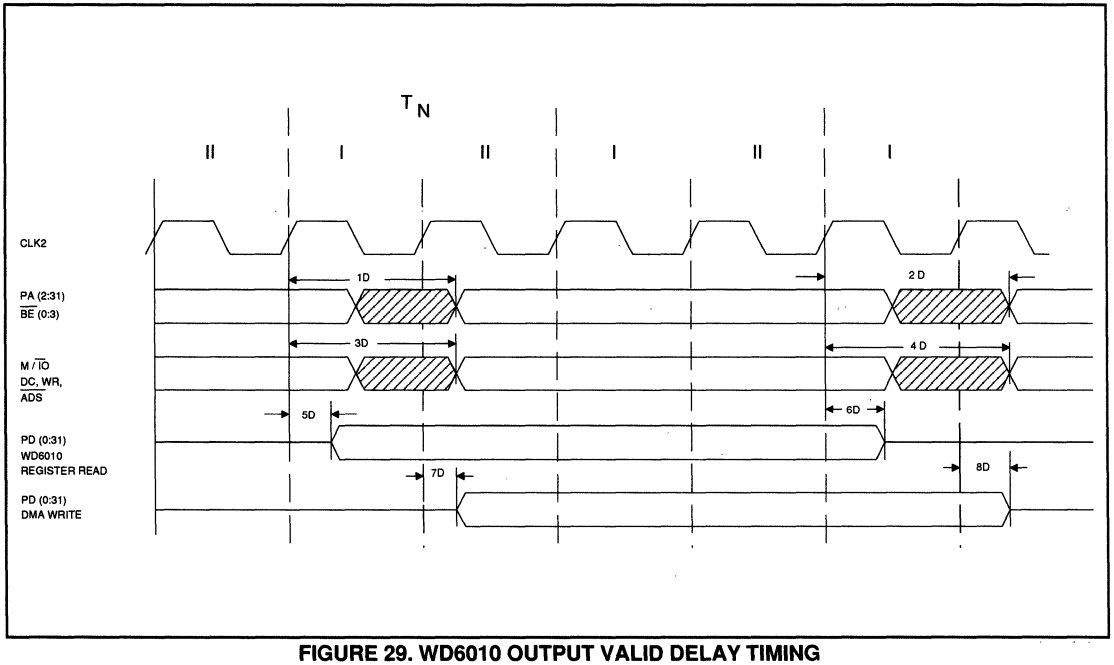


FIGURE 29. WD6010 OUTPUT VALID DELAY TIMING

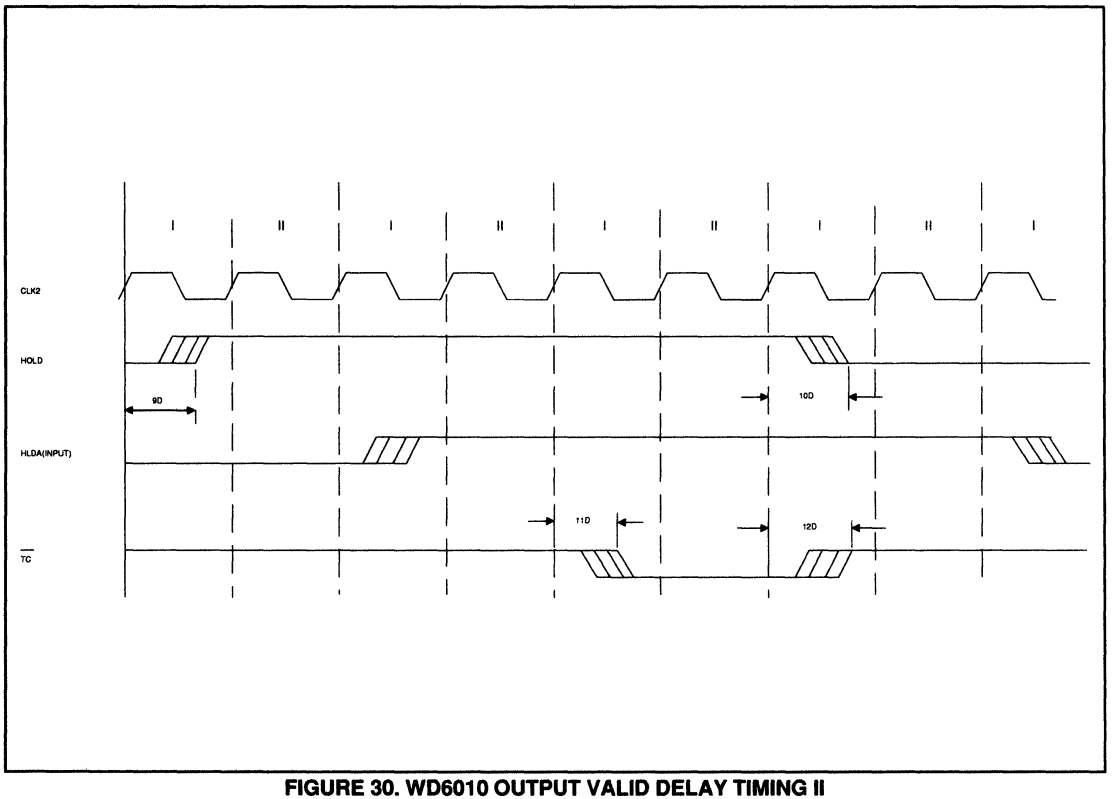


FIGURE 30. WD6010 OUTPUT VALID DELAY TIMING II

DMA OPERATION - INPUTS										
Parameter	**Description**	**16 MHz**		**20 MHz**		**25 MHz**		**33 MHz**		**Notes**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
	RDY									
T13D	SETUP TIME	20	-	11	-	10.5	-	7.5	-	
T14D	HOLD TIME	3	-	3	-	3	-	3	-	
	HLDA									
T15D	SETUP TIME	25	-	18	-	16	-	10	-	
T16D	HOLD TIME	3	-	3	-	3	-	3	-	
	PA (2:31), $\overline{BE}$(0:3)									
T17D	SETUP TIME	22	-	20	-	16	-	15	-	
T18D	HOLD TIME	2	-	2	-	2	-	2	-	
	M/$\overline{IO}$, DC, WR, $\overline{ADS}$,									
T19D	SETUP TIME	22	-	20	-	16	-	15	-	
T20D	HOLD TIME	2	-	2	-	2	-	2	-	
	REGISTER WRITE									
T21D	PD (0:31) SETUP TIME	75	-	75	-	75	-	7.5	-	
T22D	PD (0:31)HOLD TIME	15	-	15	-	15	-	15	-	
	DMA READ									
T23D	PD (0:31) SETUP TIME	10	-	10	-	10	-	10	-	
T24D	PD (0:31)HOLD TIME	5	-	5	-	5	-	5	-	
	NA, $\overline{BS16}$									
T25D	SETUP TIME	20	-	20	-	20	-	15	-	
T26D	HOLD TIME	5	-	5	-	5	-	5	-	
	$\overline{NMI}$, INTR									
T27D	SETUP TIME	15	-	15	-	15	-	15	-	
T28D	HOLD TIME	5	-	5	-	5	-	5	-	

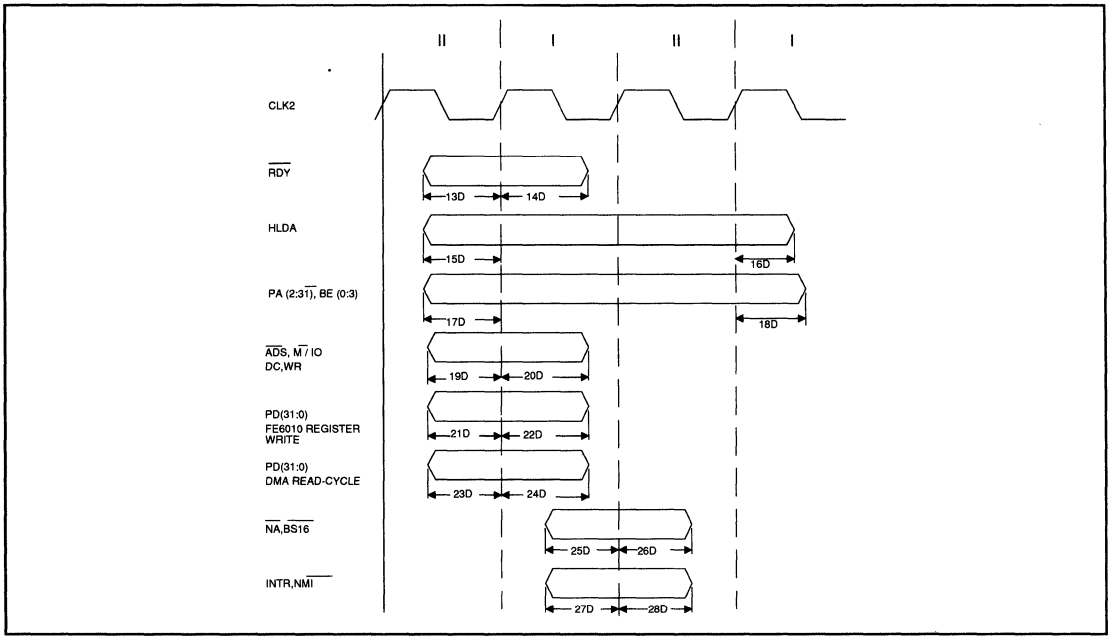


FIGURE 31. INPUT SETUP AND HOLD TIMINGS

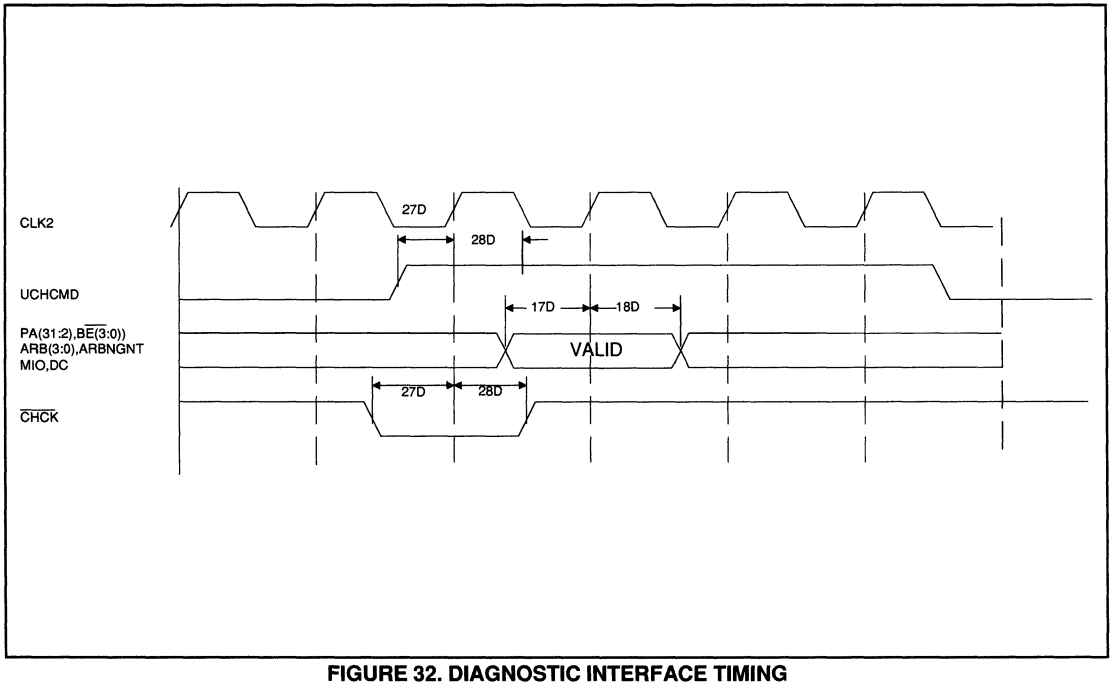


FIGURE 32. DIAGNOSTIC INTERFACE TIMING

12

80387 HALF-SPEED INTERFACE									
Parameter	Description	16 MHz		20 MHz		25 MHz		33 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
T1H	ADSO	6	34	6	28	3	24	-	21
	Valid from CLK2387								
T2H	Setup Time to CLK2387 RDY0 rising edge	20	-	11	-	9	-	-	7
T3H	Hold Time from CLK2387 RDY0 rising edge	4	-	4	-	3	-	-	3
T4H	Valid from CLK2387	2	25	2	25	2	19	2	15
	NRDY0387								
DEVICE ENABLE TIMINGS									
T1E	CDSETEN, VGAEN, EDRENA Valid from CLK2387	-	20	-	20	-	20	-	20

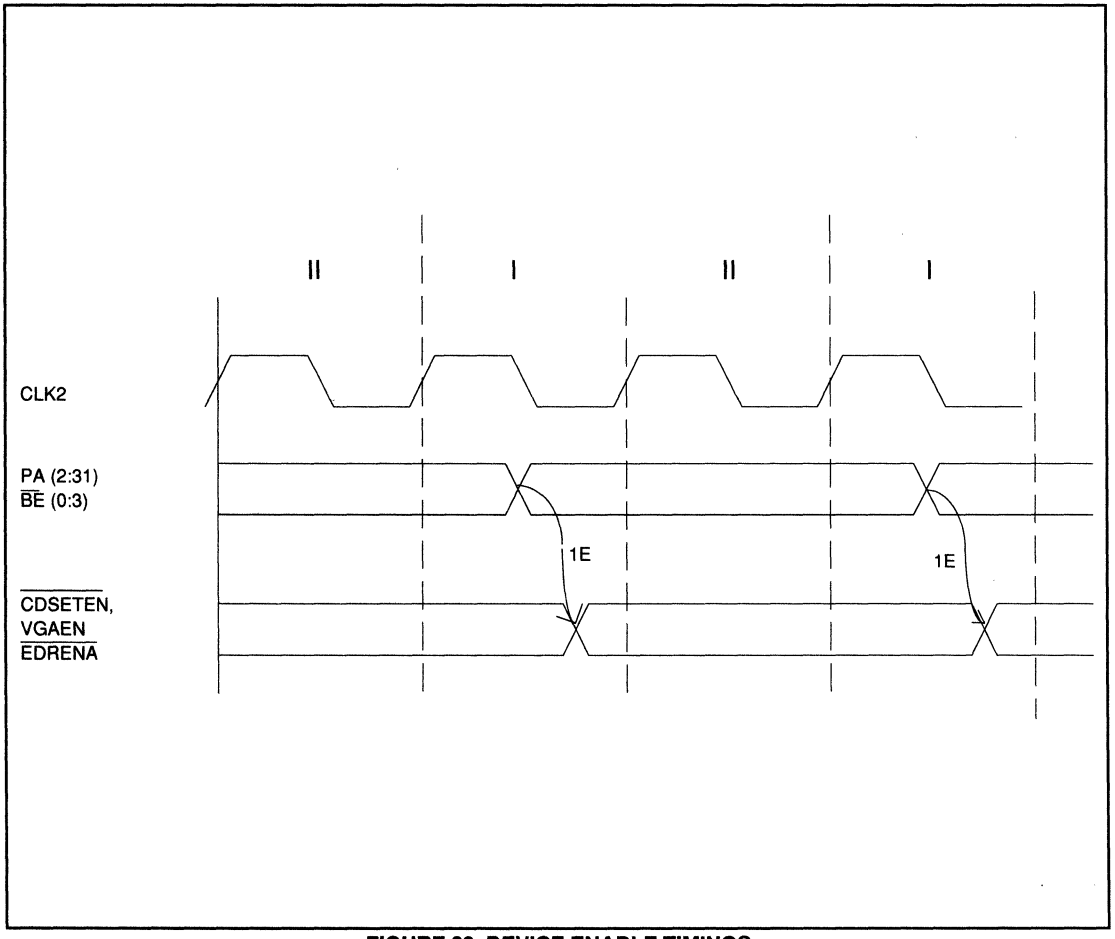


FIGURE 33. DEVICE ENABLE TIMINGS

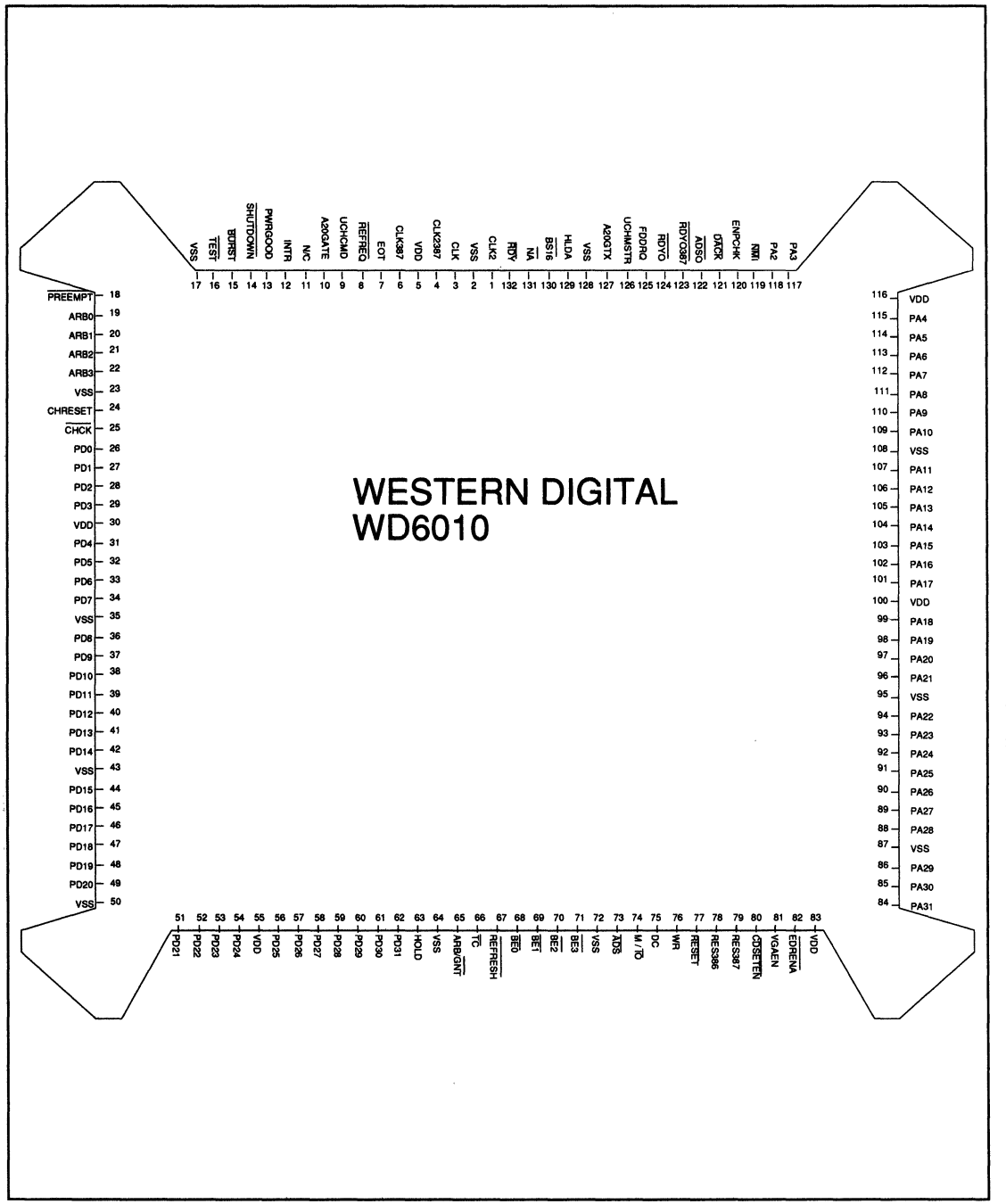


FIGURE 34. PIN LAYOUT DIAGRAM-TOP VIEW

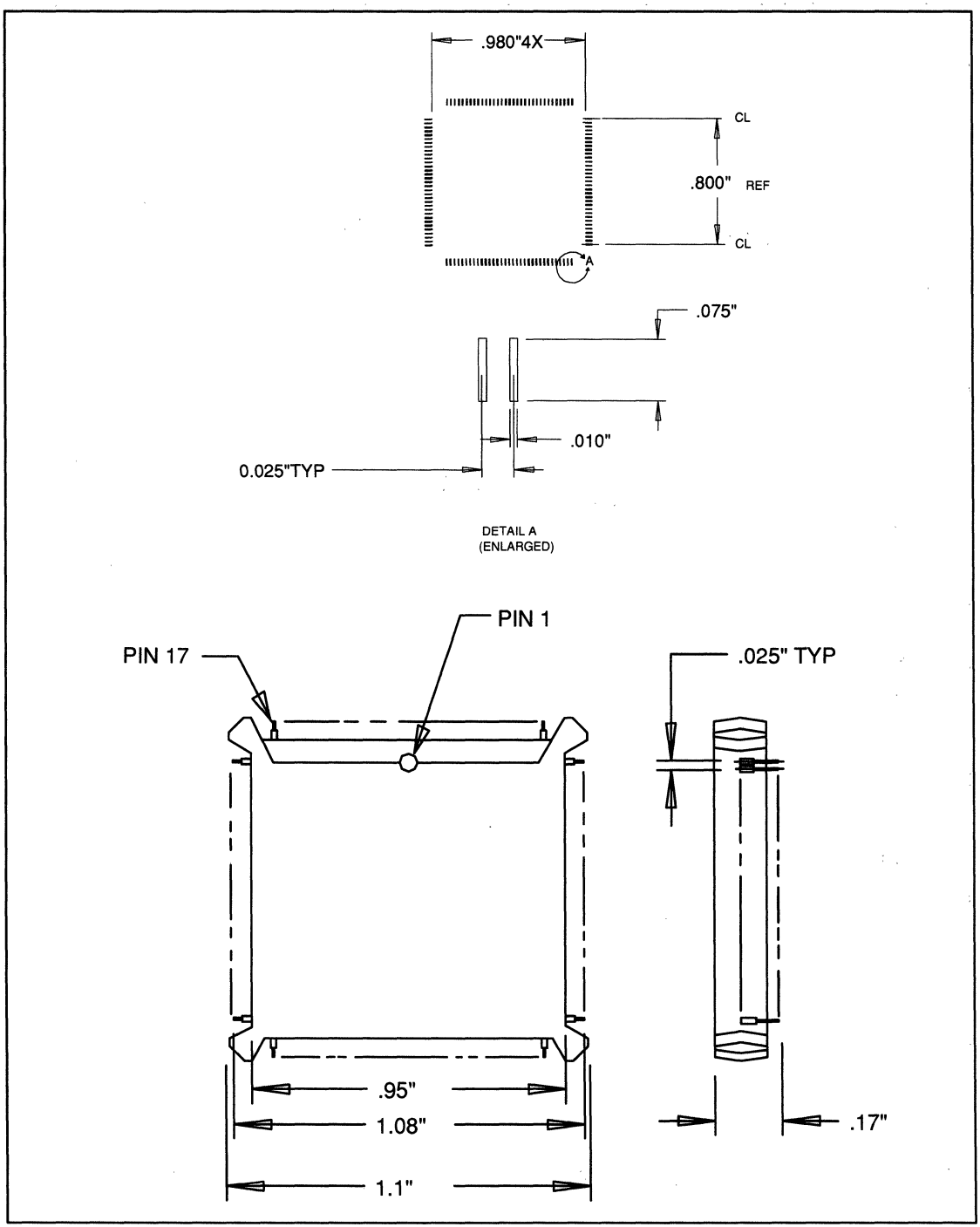
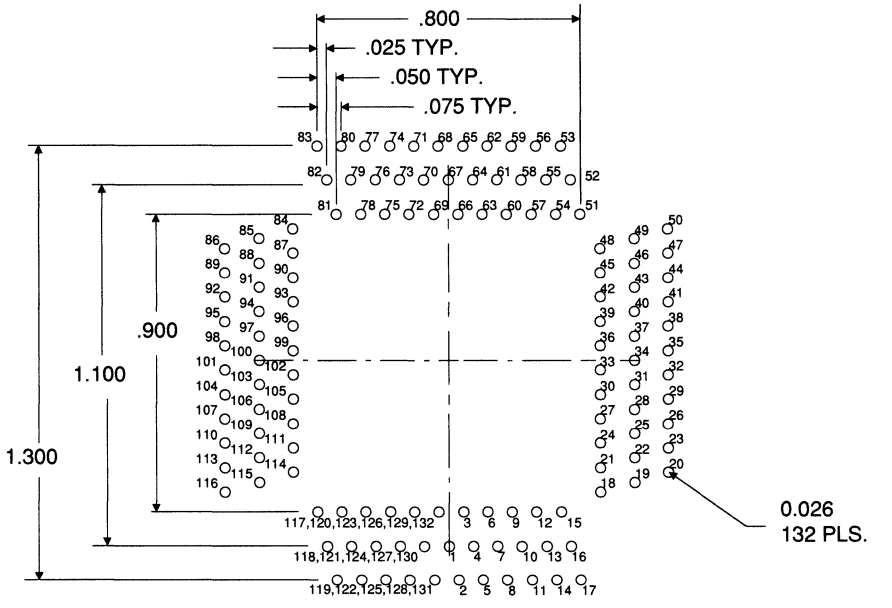


FIGURE 35. 132-PIN JEDEC FLAT PACK PACKAGE DIAGRAM



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

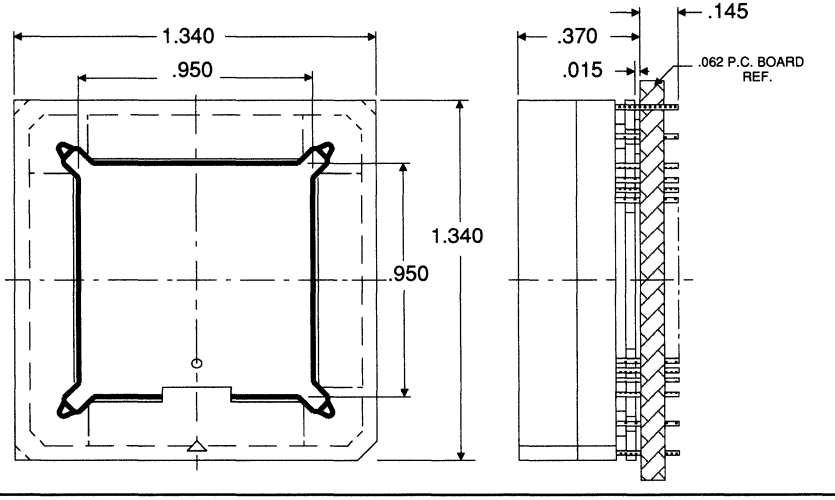


FIGURE 36. SOCKET DIAGRAM