WD60C31B

Optical Disk Drive

Encoder/Decoder

WESTERN DIGITAL

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1.0 INTRODUCTION

The WD60C31B is an encoder/decoder for optical disk drives. The primary functions of this device are the conversion of Non-return to Zero (NRZ) data to Run Length Limited (RLL 2:7) data, the conversion of RLL 2:7 data to NRZ data, the detection of a variety of special identifying marks on the media, and the detection of data error conditions.

This device supports the "Continuous/Composite" data format as proposed to the American National Standards Institute (ANSI X3B11) committee.

1.1 FEATURES

- Supports ANSI X3B11 format (5.25-inch and 3.5-inch formats)
- Converts RLL (2:7) data to NRZ data
- Converts NRZ data to RLL (2:7) data
- Track formatting
- Provides variable threshold voting for data address mark detection
- Sector mark detection (5 3 3 7 3 3 3 5)
- Programmable rotational speed tolerance of ±.5 % and ±1%
- ID address mark detection and generation (16 code bits)
- Data address mark generation and detection (48 code bits)
- Variable threshold voting for data address mark detection
- Resync generation and detection (16 code bits)
- Programmable resync window size
- Supports extended recovery techniques
- Write Only RAM Memory (WORM) flag generation and detection
- WD10C00 interface support
- Supports three on-the-fly Identification (ID) voting
- Automatically increments ID track and sector
- Supports track streaming
- Provides extensive error status

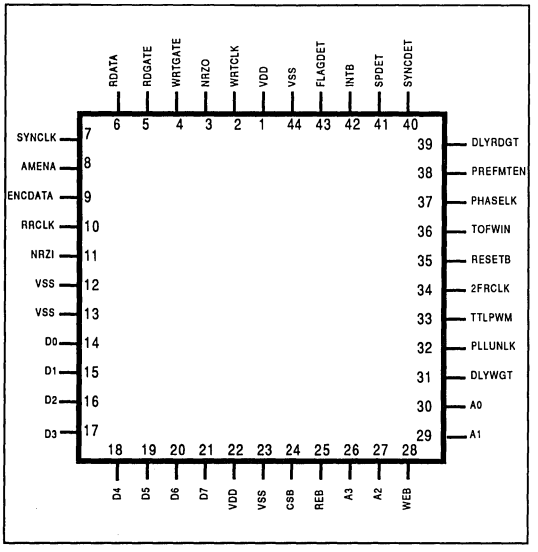

FIGURE 1-1. WD60C31B PIN DIAGRAM

1.2 PIN ASSIGNMENTS

The WD60C31B signals fall into four function groups:

- Disk controller interface (11 pins)
- Phase-locked loop (PLL) interface (11 pins)
- Microprocessor bus interface (17 pins)
- General support (5 pins)

Figure 1-1 is a pin diagram of the WD60C31B. Table 1-1 identifies each pin signal by number, and symbol. See Section 4.0 for a complete pin description.

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PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VDD	16	D2	31	DLYWGT
2	WRTCLK	17	D3	32	PLLUNLK
3	NRZ0	18	D4	33	TTLPWM
4	WRTGATE	19	D5	34	2FRCLK
5	RDGATE	20	D6	35	RESETB
6	RDATA	21	D7	36	TOFWIN
7	SYNCLK	22	VDD	37	PHASELK/PRDETB
8	AMENA	23	VSS	38	PREFMTEN
9	ENCDATA	24	CSB	39	DLYRDGT
10	RRCLK	25	REB	40	SYNCDET
11	NRZI	26	A3	41	SPDET
12	SEQOUT	27	A2	42	INTB
13	VSS	28	WEB	43	FLAGDET
14	D0	29	A1	44	VSS
15	D1	30	A0		

TABLE 1-1. WD60C31B PIN ASSIGNMENTS

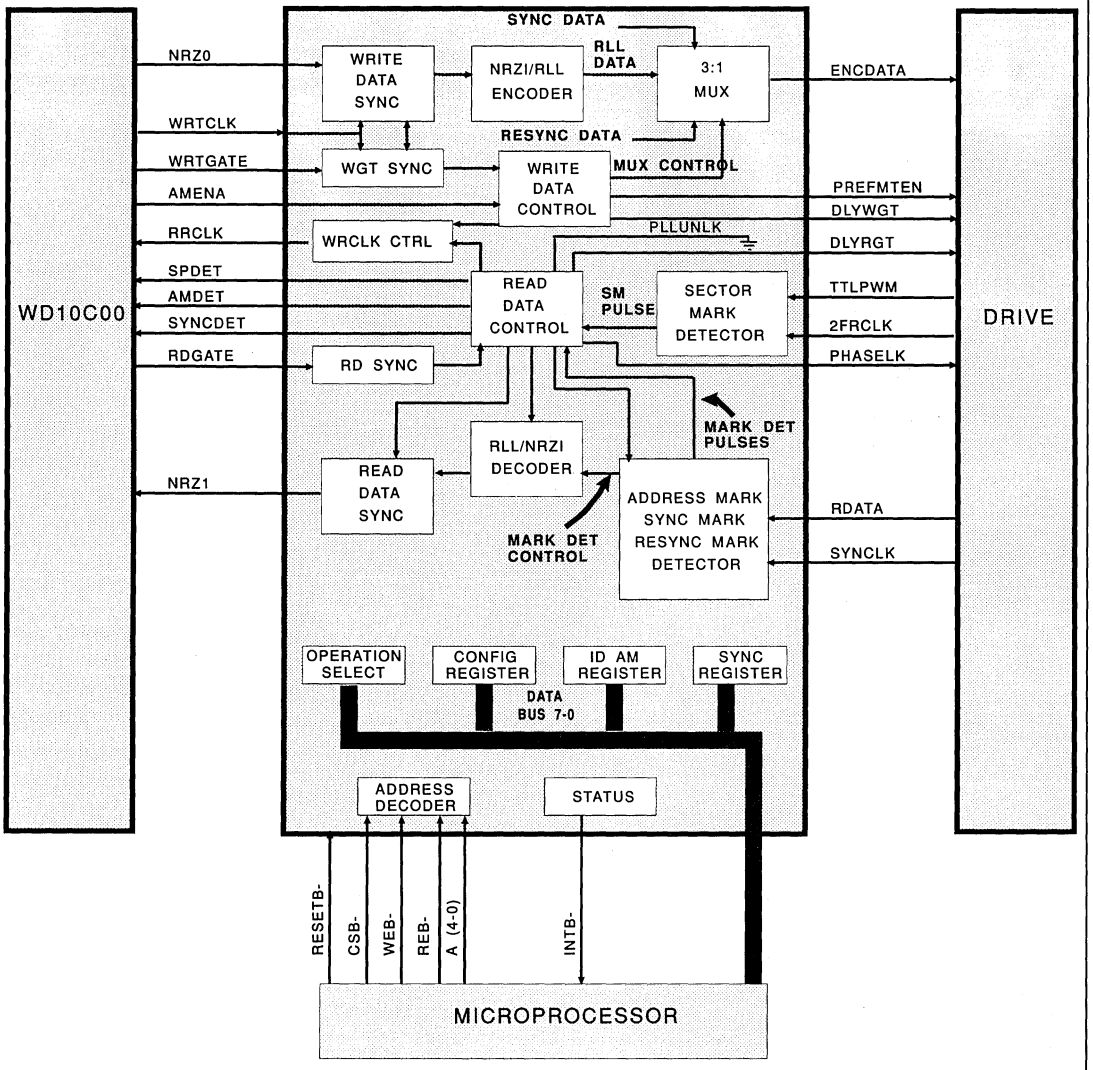

FIGURE 2-2. WD60C31B BLOCK DIAGRAM

2.0 WD60C31B ARCHITECTURE

As shown in Figure 2-1, the major functions within the WD60C31B are:

- Write data synchronization
- Write data encoding
- Write data control
- Read data synchronization
- Read data decoding
- Read data control
- Detection of address marks, sector marks, and sync and resync marks

The WD60C31B acts as a bridge between standard magnetic disk controller products and optical disk drive electronics. During write operations, the WD60C31B accepts serial NRZ data and modifies the code to create an RLL bit pattern for the optical drive. During read operations, the WD60C31B detects fields unique to the optical disk drive environment and by removing or inserting certain bit patterns it is able to decode RLL read data from the optical drive into NRZ serial data that can be handled by a standard magnetic disk controller such as the WD10C00.

The WD10C00 is a Very Large Scale Integration (VLSI), Winchester/optical disk controller device that provides data, status, and control signals for intelligent drive applications.

3.0 WD60C31B INTERFACES

3.1 DISK CONTROLLER INTERFACE

Serial NRZ data passes from the WD10C00 to the WD60C31B at a frequency of 15 Mbits/s along with the respective bit clock (WRCLK). Six control lines are associated with data transfer: three are generated by the disk controller (AMENA, WRTGATE, and RDGATE) and three are generated by the WD60C31B (SPDET, AMDET, and SYNCDET). The WD10C00 controls the direction and type of data transfer. The WD60C31B provides the proper NRZ data (along with its respective clock, RRCLK) to the WD10C00 and converts NRZ data from the WD10C00 to RLL data (ENCDATA) for the optical disk drive.

3.2 PLL INTERFACE

The phase-lock loop interface allows the WD60C31B to transfer serial RLL data to and from the optical dirve. This serial data, ENCDATA and RDATA, each are accompanied by their respective clocks, 2FRCLK and SYNCLK. TLPWM is unsynchronized serial data from the drive that is used to detect the optical media's sector mark. The PLL interface provides four control signals for the optical disk drive:

- Preformat Enable (PREFMTEN) controls the read channel gain.
- Delay Read Gate (DLYRGT) and Delay Write Gate (DLYWGT) are signals from the ADS10C00 that have been processed by the WD60C31B control circuitry.
- The Phase Lock (PHASELK) signal is an optional signal that can be used to change the gain of the phase-lock loop.

3.3 MICROPROCESSOR BUS INTERFACE

The WD60C31B has a generic microprocessor bus interface that allows it to be used with all popular 8-bit microprocessors. The microprocessor interface provides an 8-bit bidirectional data bus for the transfer of status, data and control signals to and from the WD60C31B. The read enable and write enable signals (REB, WEB) allow the microprocessor to access the internal registers selected by the address bus (A3 through A0). After requesting status information, the microprocessor receives an interrupt signal from the WD60C31B. This interrupt capability frees the microprocessor from constant polling of the WD60C31B. The master reset from the microprocessor resets all internal registers and tristates all outputs. The chip select (CSB) is the enable signal for the WD60C31B.

4.0 SIGNAL DESCRIPTION

PIN	SYMBOL	NAME	I/O	CKT TYPE	DESCRIPTION
4	WRTGATE	Write Gate	I	A	Gates write data to the drive
3	NRZO	NRZ Data Input	I	A	NRZ serial data from the disk controller
2	WRTCLK	Write Clock	I	A	Write data input clock from disk controller (inversion of RRCLK)
11	NRZI	NRZ Data Output	O	B	NRZ serial data to disk controller
10	RRCLK	Read Clock	O	B	Multiplexed 2FRCLK / SYNCLK to disk controller
5	RDGATE	Read Gate	I	A	Enables read gate during a read operation
41	SPDET	Sector Pulse Detected	O	B	Indicates detection of a sector mark or the end of a SM window
40	SYNCDET	Sync Detected	O	B	Indicates detection of an address mark
43	FLAGDET	Flag/Gap Detected	O	B	Indicates detection of a flag field
8	AMENA	Address Mark Enable	I	A	Indicates the WD60C31 should write the Data Sync Mark
12	SEQOUT	Window Toggle	I	A	The WD10C00 indicates the location of the data field.

CKT TYP (Refer to Section 5.0 for more detail)
A = Input
B = Output

TABLE 4-1. DISK CONTROLLER INTERFACE

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PIN	SYMBOL	NAME	I/O	CKT TYPE	DESCRIPTION
6	RDATA	Read data	I	A	Data from the PLL which is synchronized to 2XRCLK
7	SYNCLK	PLL clock	I	A	The PLL clock is derived from REFCLK during a write operation.
33	TTLPWM	Input data	I	A	Raw input from the heads
9	ENCDATA	Output data	O	B	Write data from the WD60C31B to the read/write heads
37	PHLK	PLL phase lock	O	B	Places PLL in phase mode
34	2FRCLK	Reference clock	I	A	PLL reference clock
31	DLYWGT	Delayed write gate	O	B	Buffered write gate to heads
39	DLYRDGT	Delayed read gate	O	B	Buffered read gate to PLL
36	TOFWIN	TOF window	O	B	Identifies the location of the mirror mark (1 or 2 byte times)
38	PREFMTEN	Preformat enable	O	B	Programmable signal which selects the gain of the read channel.
32	PLLUNLK	PLL unlock enable	I	C	Indicates when PLL is out of lock
CKT TYP (Refer to Section 5.0 for more detail) A = Input B = Output					

TABLE 4-2. PLL INTERFACE

PIN	SYMBOL	NAME	I/O	CKT TYPE	DESCRIPTION
21-14	D7-D0	Data Bus	I/O	C	Eight-bit bidirectional data bus for transferring status, data and control of the WD60C31B
26, 27 29, 30	A3-A0	Address Bus	I	A	Nonmultiplexed address bus
25	REB	Read Enable	I	C	Read strobe for the internal registers in PIO
28	WEB	Write Enable	I	C	Write strobe for internal registers during PIO
24	CSB	Chip Select	I	A	Master chip enable for the WD60C31B
42	INTB	Interrupt Request	O	B	Output to microprocessor requesting a status transfer
35	RESETB	Master Reset	I	A	Master resets all internal

CKT TYP (Refer to Section 5.0 for more detail)
A = Input
B = Output
C = Bidirectional

TABLE 4-3. MICROPROCESSOR INTERFACE

PIN	NAME	SIGNAL	FUNCTION
1, 22	VDD	+5 Volts	Supply voltage
13, 23, 44	VSS	Ground	Digital ground

TABLE 4-4. GENERAL SUPPORT

5.0 ELECTRICAL SPECIFICATIONS

Non-operational:	
VDD	7.0V
Voltage with respect to VSS	-0.3V (minimum) +0.3V (maximum)
Storage temperature	-55°C to 150°C
Operational:	
VDD	5.0V ±0.5V
IDD (maximum)	150 mA at 30 MHz
Ambient temperature	0°C to 70°C

SYMBOL	PARAMETERS	MIN	MAX	UNITS	TEST CONDITIONS
Vih	High-level input voltage	2.0	V_{DD} +0.3	V	
Vil	Low-level input voltage	-0.3	0.8	V	
Vi	Input clamp voltage (low)	-0.5			
Ilh	Leakage current (high)	-10	+10	µA	$2.0 \leq Vi \leq V_{DD}$
Ill	Leakage current (low)	-10	+10	µA	$0.0 \leq Vi \leq 0.8$
Iluh	Latchup current (high)	-40		µA	
Ilul	Latchup current (low)		40	µA	
Note: Positive current is flow into the pin.					

TABLE 5-1. CIRCUIT A - OPERATING CHARACTERISTICS

SYMBOL	PARAMETERS	MIN	MAX	UNITS	TEST CONDITIONS
Ioh	High-level output current		-400	µA	Vo = 2.8V
Iol	Low-level output current	2.0		mA	Vo = 0.3V
Voh	High-level output voltage	2.8		V	Io = -400 µA
Vol	Low-level output voltage		0.3	V	Io = 2.0 mA
Iozh	Off state, high-level output current	-10	+10	µA	$2.0 \leq Vo \leq VDD$
Iozl	Off state, low-level output current	-10	+10	µA	$0.0 \leq Vo \leq 0.8V$

TABLE 5-2. CIRCUIT B - TRISTATE OUTPUT CHARACTERISTICS

SYMBOL	PARAMETERS	MIN	MAX	UNITS	TEST CONDITIONS
Ioh	High-level output current		-2.5	mA	Vo = 2.8V
Iol	Low-level output current	4.0		mA	Vo = 0.3V
Vih	High-level input voltage	2.4	VDD + 0.3	V	
Vil	Low-level input voltage	-0.3	0.8	V	
Vik	Input clamp voltage (low)		-0.5	V	
Voh	High-level output voltage	2.8		V	Ioh = -2.5 mA
Vol	Low-level output voltage		0.4	V	Iol = 6.0 mA
Iozh	Off state, high-level output current	-10	+10	µA	VCC = Maximum Vih = 2.8V
Iozl	Off state, low-level output current	-10	+10	µA	VCC = Maximum 0.0 ≤ Vo ≤ 0.8
Iluh	Latchup current (high)	-40		mA	
Ilul	Latchup current (low)		40	mA	
Iih	High-level input current	-10	+10	µA	VCC = Maximum Vih = 2.8V
Iil	Low-level input current	-10	+10	µA	VCC = Maximum Vil = .4V
Note: Positive current is current flow to the pin.					

TABLE 5-3. CIRCUIT C - BIDIRECTIONAL CHARACTERISTICS

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6.0 AC OPERATING CHARACTERISTICS

6.1 TIMING CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
t1a	NRZO setup	10	
t1b	NRZO hold	10	
t1c	WRTCLK high	trlo-4.5	
t1d	WRTCLK low	trhi-4.5	
t1e	WRTCLK period	trp-4.5	
t2a	WRTGATE/RDGATE	10	
t2b	WRTGTE/RTGTE hold	10	
t3a	NRZI setup	trhi-4.5	
t3b	NRZI hold	trlo-4.5	
t4a	SYNCDET setup	trlo-4.5	
t4b	SYNCDET hold	trhi-4.5	
t5a	AMENA setup	10	
t5b	AMENA hold	10	
t6a	SPDET pulse width	2 x trp-4.5	
t6b	SPDET high delay	10	
t6c	SPDET low delay	10	
t7a	FLGDET pulse width	4 x trp-4.5	
t7b	FLGDET setup	trlo-4.5	
t7c	FLGDET hold	trhi-4.5	
t8a	Clock high	13	
t8b	Clock low	13	
t8c	Clock period	tclk	
t9a	RDATA setup	7	
t9b	RDATA hold	7	
t10a	DLYRGT low delay	12	40
t10b	DLYRGT high delay	12	40
t10c	PHASELK low delay	12	40
t10d	DLYRGT to PHASELK	0-63 2FRCLK	
t11a	ENCDATA low delay	12	25

TABLE 6-1. DISK CONTROLLER AND PLL TIMING

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
t11b	ENCDATA high delay	12	25
t12a	PREFMTEN low delay	12	30
t13a	TOFWIN high delay	12	30
t13b	TOFWIN low delay	12	30
t13c	TOFWIN pulse width	0-15 2FRCLK	

Note: Unless otherwise specified, all time units are in nanoseconds.
trhi = clock high for the RRCLK output
trlo = clock low for the RRCLK output
trp = clock period of the RRCLK output
tclk = 2FRCLK clock input

TABLE 6-1. DISK CONTROLLER AND PLL TIMING (Continued)

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
t14a	Address valid to REB	20	
t14b	REB high to address change	0	
t14c	REB false to CSB false	0	
t14d	REB pusle width	100	
t14e	REB true to data valid		80
t14f	REB false to data hold	10	
t15a	Address valid to WEB true	20	
t15b	WEB high to address change	0	
t15c	WEB pulse width	100	
t15d	Data setup to WEB false	80	
t15e	WEB false to data hold	00	
t15f	WEB false output change		80
t15g	WEB false to CSB false	10	

TABLE 6-2. MICROPROCESSOR TIMING

6.2 DISK CONTROLLER TIMING

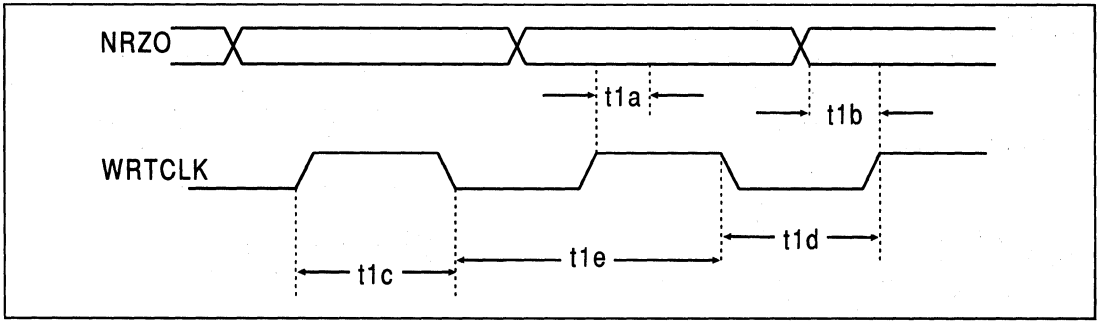

FIGURE 6-1. DISK CONTROLLER TIMING (NRZ0 TO WRTCLK)

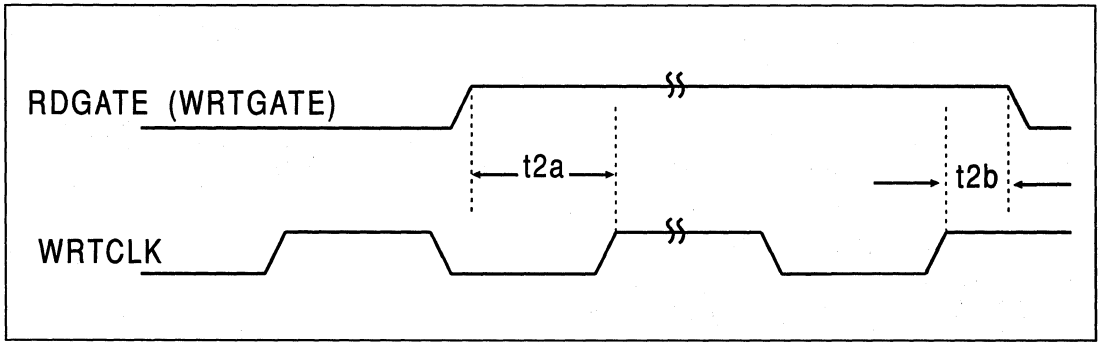

FIGURE 6-2. DISK CONTROLLER TIMING (WRTGATE/RDGATE)

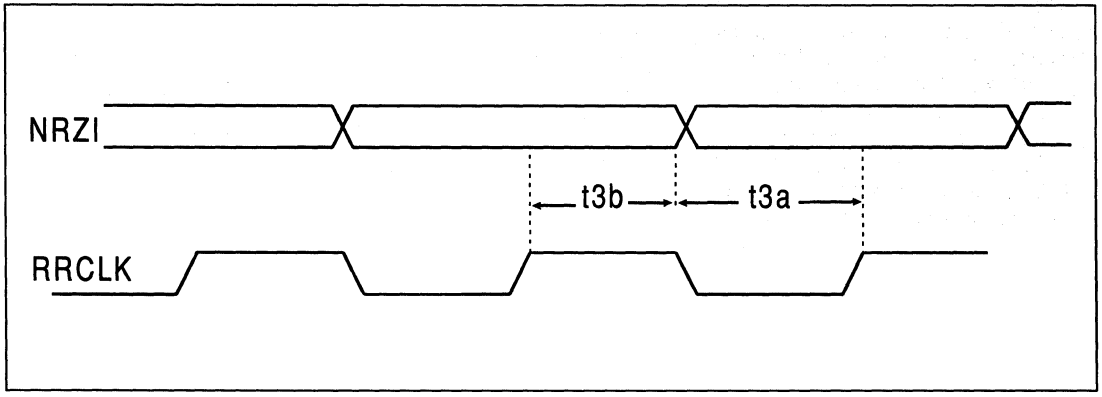

FIGURE 6-3. DISK CONTROLLER TIMING (NRZI TO RRCLK)

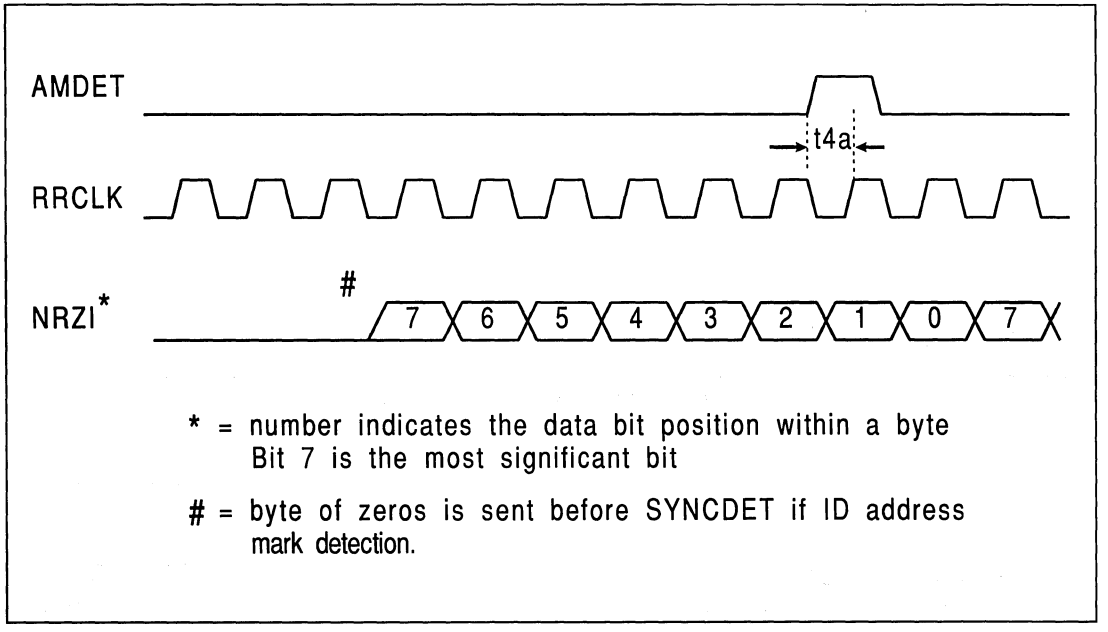

FIGURE 6-4. DISK CONTROLLER TIMING (SYNCDET)

NOTE

Sync Detected (SYNCDET) is generated whenever RDGATE is active and either the ID Address Mark (ID AM) or the Data Address Mark is detected. Whenever an ID Address Mark is detected, the SYNCDET is sent concurrently with the first byte of the 5-byte ID Address field. The 5-byte ID field is preceded by a NRZI byte of zeroes. During ID search, the SYNCDET is sent concurrently with this byte of zeroes. Whenever a Data Address Mark is detected, the SYNCDET is sent one byte before the first byte of the data field. A full byte of zeros is sent concurrently with the SYNCDET. This byte of zeros is handled in the WD10C00 as an address mark. SYNCDET, once active, remains active until RDGATE is dropped.

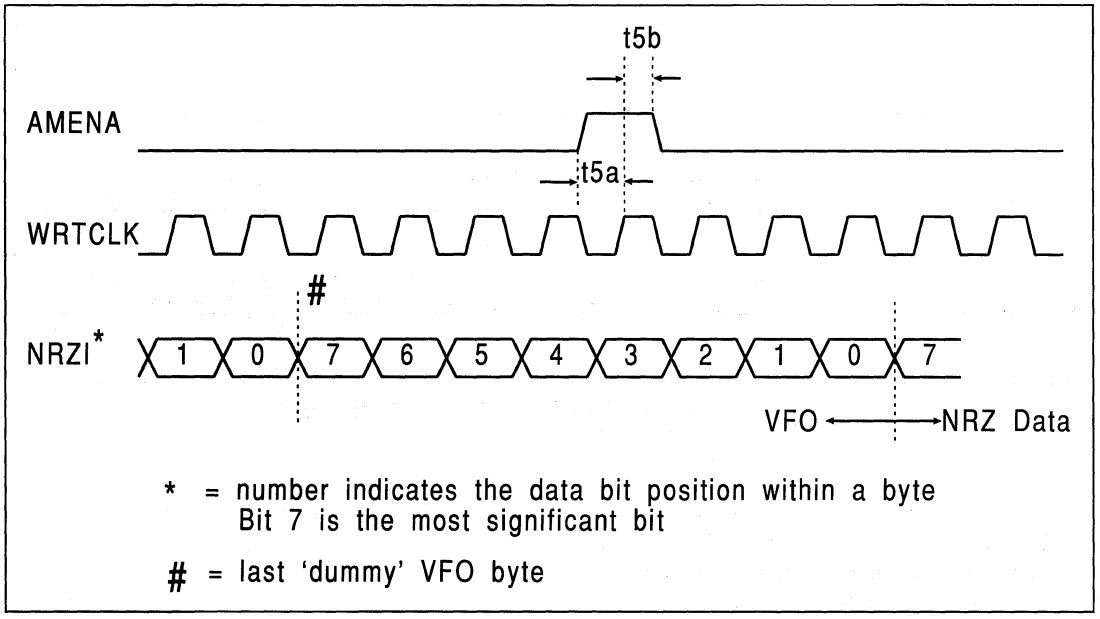

FIGURE 6-5. DISK CONTROLLER TIMING (AMENA)

NOTE

The data field of an optical drive contains four unique types of information. They are : 1) the VFO field, 2) the Data Address Mark, 3) the encoded user data, and 4) the Resync Marks. The WD10C00 and the WD60C31B share the responsibility of defining the type and quantity of information to be written on the media. In the case of the VFO field, the WD10C00 specifies the size of the VFO field, and the WD60C31B creates the unique high-frequency pattern. First, the WD10C00 raises WRTGATE. Then an NRZ data pattern of 1's is sent to the WD60C31B. This specifies the beginning of the VFO field. The WD60C31B writes a fixed RLL pattern on the disk. The WD10C00 must indicate the end of the VFO field. This is performed by sending the Address Mark Enable (AMENA) signal during the last byte. This signal initiates the writing of the previously programmed Data Address Mark (3 bytes). The WD60C31B then encodes the incoming NRZ data from the WD10C00 and injects the Data Resync Mark, another previously programmed pattern, into the encoded write data path. This operation continues for as long as WRTGATE is active or the end of sector is detected.

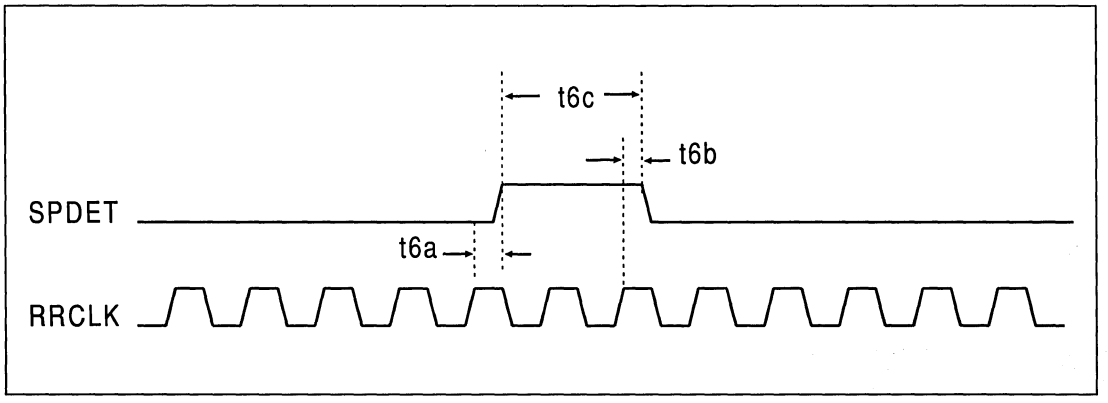

FIGURE 6-6. DISK CONTROLLER TIMING (SPDET)

NOTE

The Sector Pulse Detection (SPDET) signal occurs whenever a sector mark is detected. A SPDET also occurs whenever a sector mark has not been detected by a defined time. (One sector period plus 6 byte times.)

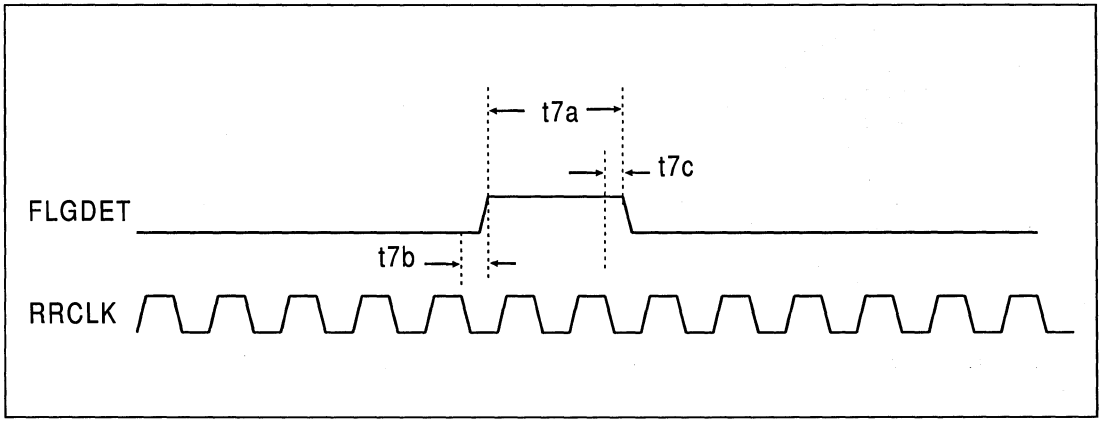

FIGURE 6-7. DISK CONTROLLER TIMING (FLGDET)

NOTE

A Flag Detect (FLGDET) pulse occurs if RDGATE is active and 1-1/2 bytes of the Flag pattern (high frequency '100') is detected.

6.3 PLL TIMING

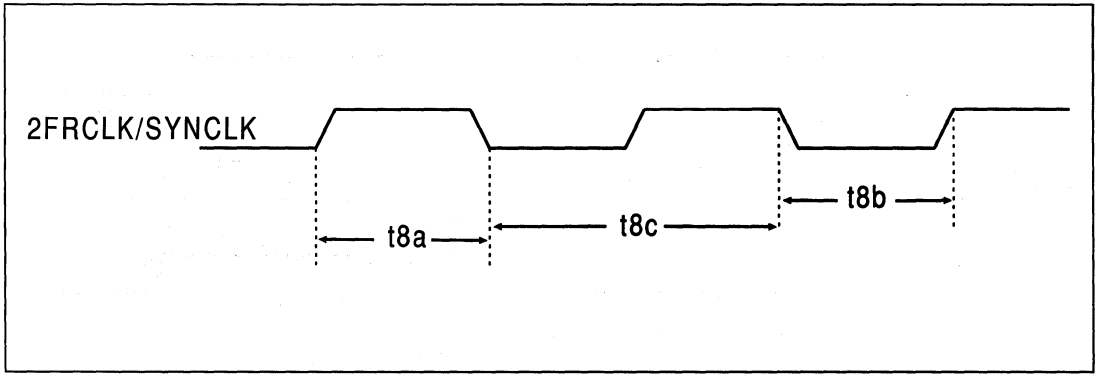

FIGURE 6-8. PLL TIMING (2FRCLK/SYNCLK)

NOTE

Both clocks must be glitch-free. The PLL must deliver a clock which does not violate the above timing. The is especially true of the SYNCLK which changes between the reference clock and the internally generated PLL clock when Read Gate is applied.

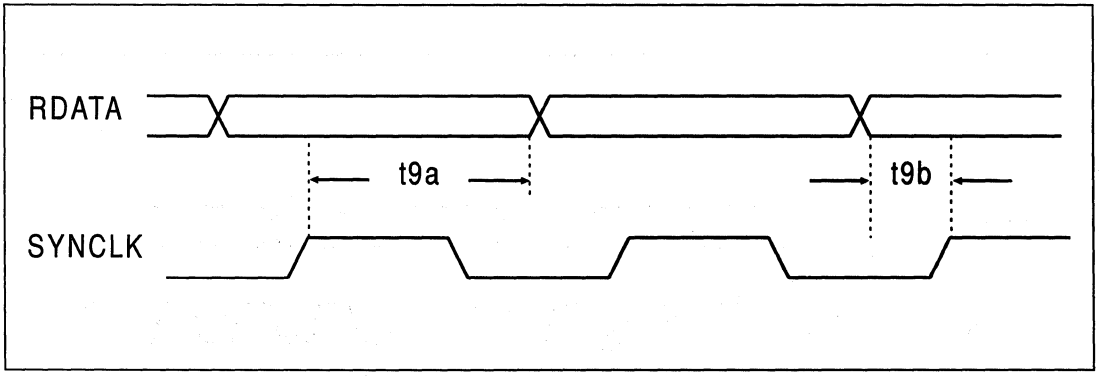

FIGURE 6-9. PLL TIMING (NRZI TO RRCLK)

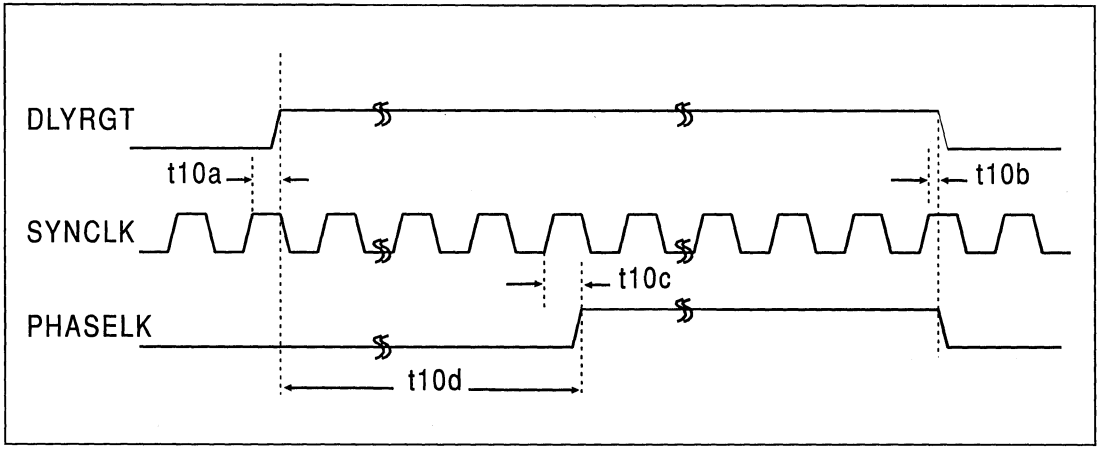

FIGURE 6-10. PLL TIMING (DLYRGT/PHASELK)

NOTE

The PHASELK signal controls the PLL modes. Whenever PHASELK is low, the PLL should be in high gain (or phase/frequency mode). Whenever PHASELK is high, the PLL should be in low gain (or phase mode). There is a delay of 1 to 64 SYNCLKs (+/-1 SYNCLK) from DLYRGT to PHASELK.

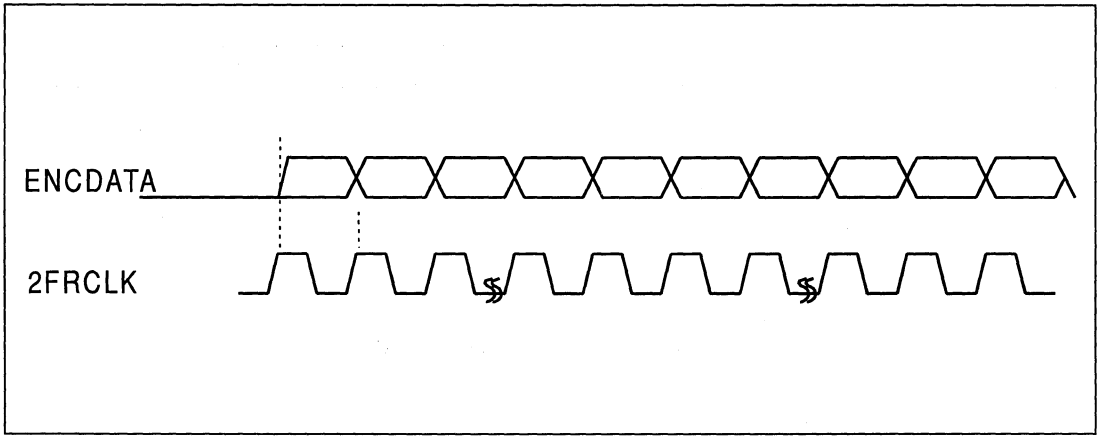

FIGURE 6-11. PLL TIMING (ENCDATA)

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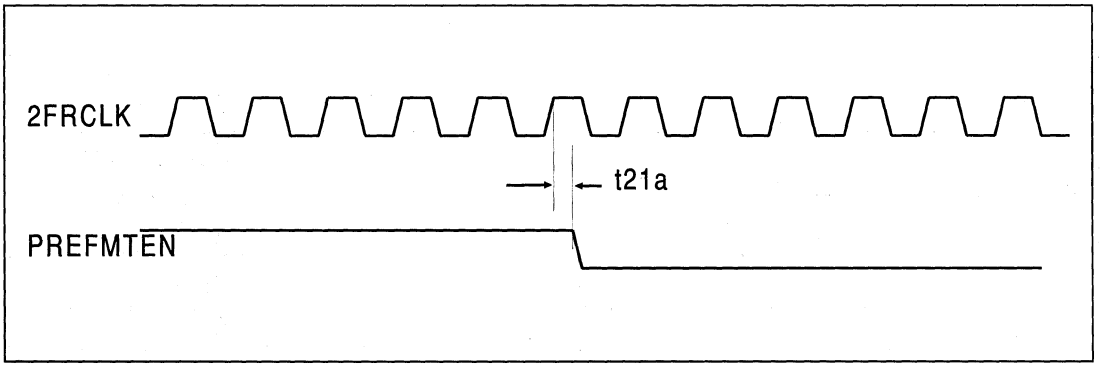

FIGURE 6-12. PLL TIMING (PREFMTEN)

NOTE

When enabled by the microprocessor, the Preformat Enable signal (PREFMTEN) acts as a read channel control line. This signal occurs whenever the drive is expecting to read the preformatted data (ID fields). This signal is continuously high for WORM drive applications. This signal, when enabled, is low 47 bytes after SPDET.

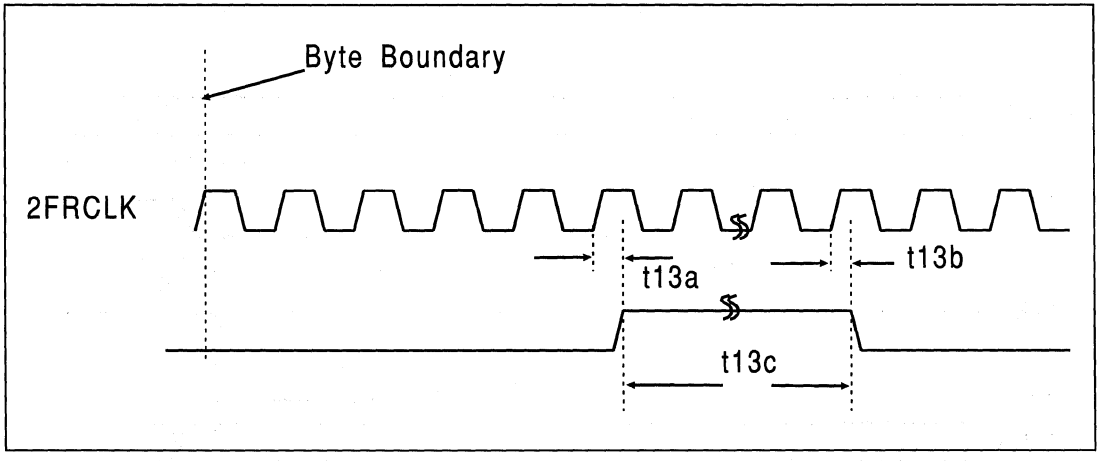

FIGURE 6-13. PLL TIMING (TOFWIN)

NOTE

The TOFWIN signal is used in optical servo systems which utilize the Mirror Mark / TOF Mark for servo alignment. TOFWIN is active 47 bytes after sector mark. This signal is active only if a sector mark is detected.

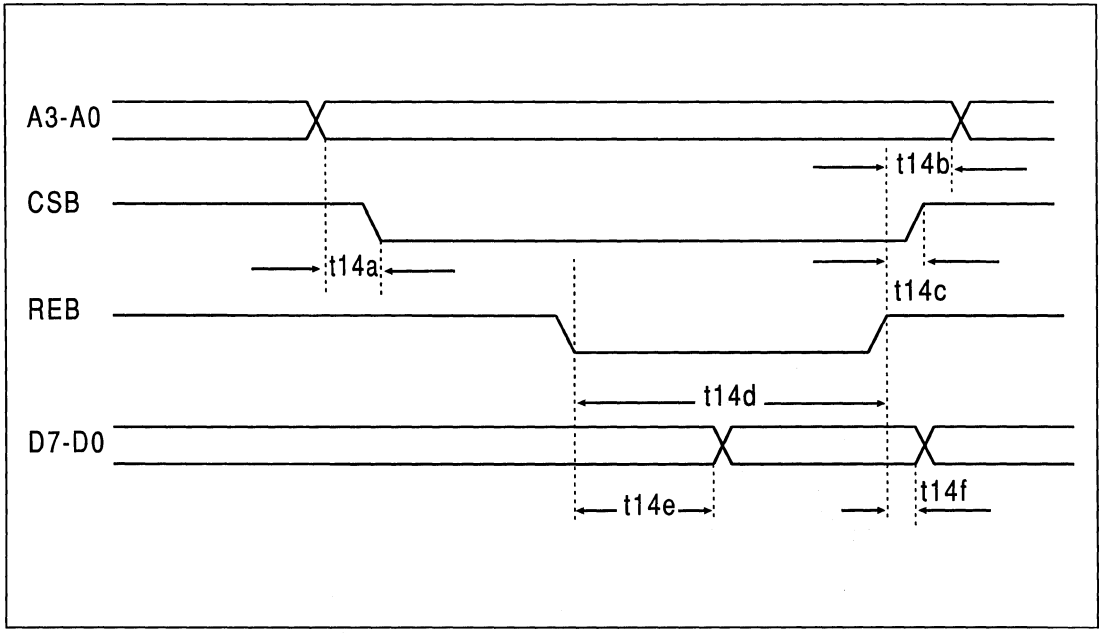

FIGURE 6-14. MICROPROCESSOR READ TIMING

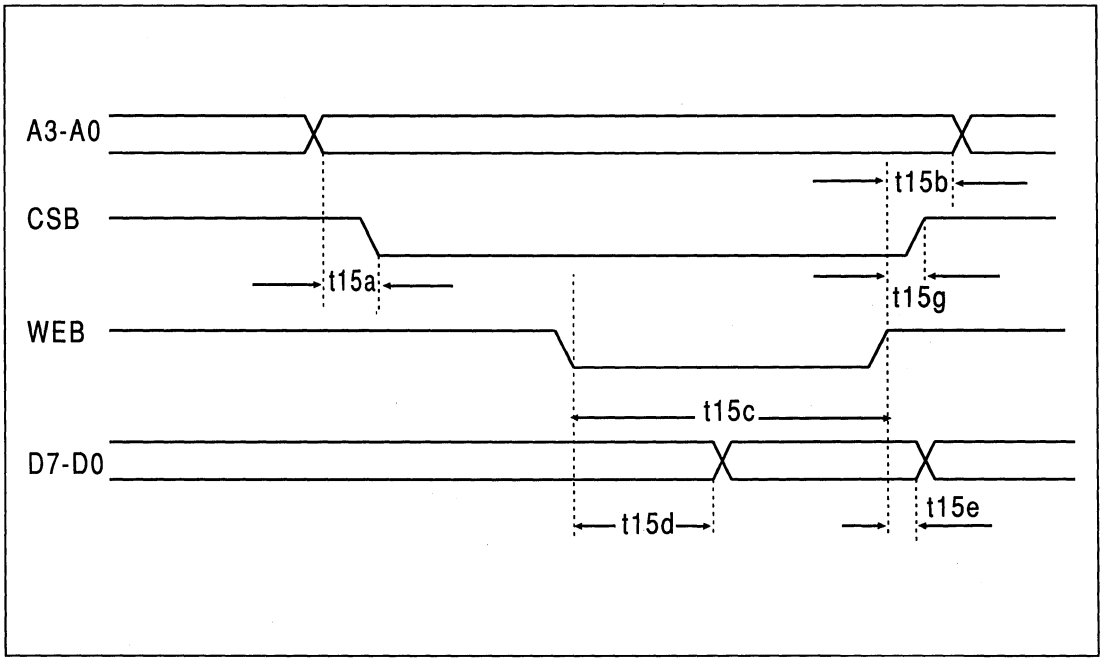

FIGURE 6-15. MICROPROCESSOR WRITE TIMING

7.0 REGISTERS

The WD60C31B has 21 read/write locations.

ADDRESS	WRITE FUNCTION	READ FUNCTION
X'0'	Configuration write	Configuration read
X'1'	Software reset	Operation error status
X'2'	Data resync MSB byte	Data resync MSB byte
X'3'	Data resync LSB byte	Data resync LSB byte
X'4'	ID address mark MSB byte	ID address mark MSB byte
X'5'	ID address mark LSB byte	ID address mark LSB byte
X'6'	Data sync bytes (6 bytes)	Pointer counter status
X'7'	Sync threshold/TOF size	Sync threshold/TOF size
X'8'	Data size/RESYNC limit	Data size/RESYNC error flag
X'9'	Data sync pointer reset	Future ID track/sector (3 bytes)
X'A'	Phase lock delay	Phase lock delay
X'B'	Secondary configuration	Secondary configuration
X'C'	Third configurtion	Third configuration
X'D'	ID preset track/sector (3 bytes)	ID preset track/sector (3 bytes)
X'E'	ID control	ID status (3 bytes)
X'F'	Sector/track	Sector/track

TABLE 7-1. REGISTER ADDRESS ASSIGNMENTS

7.1 CONFIGURATION READ/WRITE REGISTER: ADDRESS X'0'

7	6	5	4	3	2	1	0
FF	ID	SS	IE	WT	PE	M1	M0

FF= Enable Flag Field Detection
(Active state = 1)

This bit enables the flag detection logic. Eight rising edges of TTLPWM during an internally created flag window indicates a flag detection, and FLGDET goes active. In addition, all write operations are disabled until the next sector mark if a flag is detected. An interrupt is also generated if Bit 4 of this register is set.

ID = Enable ID Search Mode
(Active state = 1)

Normally, during a read opertion, the WD60C31B sends an AMDET (in the Bit 1 position) with the first byte of decoded RLL data after an ID address mark is detected. If the controller is trying to read the ID field, the concurrent byte is the Track High Byte. The WD10C00 uses the Track High Byte as an Address Mark byte and stores only the subsequent NRZI bytes in its internal register. If the Track High bytes do not match, the WD10C00 does not store the subsequent ID field. The programmer can activate this bit and perform another ID read operation. The WD60C31B moves the AMDET forward by eight RRCLKs and sends a byte of zeroes. The WD10C00 is then programmed to wait for SYNCDET and expect an Address Mark byte of zeros. This means that the WD10C00 will store the Track High Byte internally along with the subsequent bytes. This mode is

SS	SE35	IDW	BYTES/SECTOR	MODE DEFINITION
0	0	0	746	5.25" - 512 bytes
1	0	0	1360	5.25" - 1024 bytes
0	1	0	725	3.5" - 512 bytes
1	1	0	1394	3.5" - 1024 bytes
0	0	1	746	Auxilliary mode - 512
1	0	1	1360	Auxilliary mode - 1024

TABLE 7-2. SELECTION OF SECTOR SIZE

normally used after a seek operation to determine the head position.

SS = Select Sector Size
(Active state = 1)

When this bit is active, a sector size of 1024 data bytes is selected. When inactive, a sector size of 512 data bytes is selected. The Secondary Configuration Register further defines the total number of bytes per sector. Refer to Table 7-2.

IE = Enable Interrrupt
(Active state = 1)

This is the Master Interrupt Enable bit. An interrupt occurs as a result of any of the following conditions:

- Data Read Complete
  At the end of each data field read operation an interrupt is generated if interrupts are enabled and Bit 5 of of the ID Control/Status Register is set.
- Flag Field/WRTGATE Error
  This bit is set if a flag field is detected and a write operation is attempted in this sector. An interrupt is possible if Bit 7 of this register is set.
- Pseudo SPDET/WRTGATE Error
  This bit is set if a pseudo SPDET is generated and a write operation is attempted. An interrupt is generated if Bit 0 of the Third Configuration Register and Bit 4 of this register are set.
- Resync Threshold Exceeded Error
  If the programmed missing RESYNC counter equals or exceeds the programmed limit, this bit is set. An interrupt is generated if Bit 4 of the ID Control/Status Register and Bit 4 of this register are set.
- RDGATE/SPDET Error
  This bit is set if RDGATE is applied and a SPDET is generated. An interrupt is generated if Bit 4 of the Secondary Configuration Register and Bit 4 of this register are set.
- ID Miscompare Error
  If the on-the-fly ID detection logic is unable to meet the programmed ID threshold, an interrupt is generated concurrent to the transfer of an invalid ID AM byte transfer on the NRZI pin. Bit 4 of this register must be set.
- Read Stop Interrupt
  This bit is set when RDGATE is applied after the next SPDET. An interrupt is generated if Bit 7 of the Sector per Track Register and Bit 4 of this register are set.

WT = Internal Test Mode

This is used for IC testing purposes only.

PE = Preformat Enable Control

When set, this permits the PREFMTEN signal to go low 47 bytes after the sector mark. This is used in erasable media applications.

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M1,M0 = Select Data Recovery Mode

M1	M0	MODE
0	0	Normal data tranasfer
0	1	**Recovery Mode 1: Disable Data Sync Detection** During a data field read, a fixed number of data segments are sent as soon as read gate is active without waiting to detect the Data Sync Mark first. This mode is selected when the Sync Mark can't be detected, regardless of the Sync threshold. The number of data segments are determined by the Third Configuration Register.
1	0	**Recovery Mode 2: Invalid Code Bit Map with sync** The NRZ Data that is sent to the ADS10C00 is not the decoded RLL data. Instead, it is a map of the invalid RLL code bit of the data stream. An NRZI Bit 1 indicates an RLL violation.
1	1	**Recovery Mode 3: Invalid Code Bit Map with resync** This mode performs both RLL code violation mapping (Mode 2) and disabling of Data Sync detection (Mode 1).

The following interrupt functions have individual enables. In order for these interrupt functions to be enabled, both the general enable (Bit 4 of the Primary Configuration Register) and the specified enable must be set:

FUNCTION	INTERRUPT ENABLE
Data Read Complete	ID Control Status Register (Bit 5)
Resync Threshold Exceed Error	ID Control/Status Register (Bit 4)
RDGATE/ SPDET Error	Third Configuration Register (Bit 3)
ID Miscompare Error	ID control/Status Register (Bit 6)

The following functions do not have individual interrupt masks. The only individual control possible is to disable the function:

FUNCTION	FUNCTION ENABLE
Flag Field/ WRTGATE Error	Primary Configuration (Bit 7)
Pseudo SPDET/ WRTGATE Error	Third Configuration Register (Bit 0)
Read Stop Interrupt	Sector per Track Register (Bit 7)

7.2 SOFTWARE RESET/OPERATION ERROR STATUS: ADDRESS X'1'

Write:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

X = not applicable

The following status flags are reset when writing to Address X'1':

- Flag Detect Error Flag
- Read Complete Flag
- Pseudo Sector Mark Error Flag
- Resync Threshold Error Flag
- Missing Resync Error Flag
- RDGATE/SPDET Error Flag
- ID Miscompare Error Flag
- Read Stop Error Flag

Read:

7	6	5	4	3	2	1	0
IV	RDC	FLE	SE	IP	TE	RS	RD

Whenever Address X'1' is read, the following status flags are cleared and reinitialized.

IV = Invalid RLL Code Detected

RDC = Read Complete
(Active state = 1)

The RDC bit is set upon finishing a data field read operation. This bit is cleared at the end of each sector or if the programmer writes to Address 1. Enabling this bit and Bit 5 of the ID Control/Status Register generates an interrupt.

FLE = Flag Detect Error
(Active state = 1)

The FLE bit is set if the flag detection logic has been enabled, a flag has been detected, and WRTGATE is active. An interrupt is also generated if Bit 0 of the Primary Configuration Register is set. The FLE bit is cleared when the programmer writes to Address 1.

SE = Pseudo Sector Mark Error
(Active state = 1)

The SE bit is set when a Sector Mark is not detected, a pseudo SPDET is generated and WRTGATE is active for a given sector. An interrupt is also generated if Bit 0 of the Third Configuration Register is set. Writing to Address 1 clears the SE bit.

IP = Interrupt Pending
(Active state = 1)

TE = Resync Threshold Exceeded
(Active state = 1)

The number of missing resyncs as defined in the Resync Error Threshold Register has been equaled or exceeded in a single sector data field read. An interrupt is generated if TE is enabled and Bit 4 of the ID Control/Status Register is set. TE is cleared when the programmer writes to Address 1.

RS = Missing RESYNC Field Detected
(Active state = 1)

This bit indicates that at least one Resync byte has been missed. The RS bit is cleared by writing to Address 1.

RD = RDGATE/SPDET Error
(Active state = 1)

Read Gate is active when SPDET becomes active. This error flag generates an interrupt if enabled and Bit 3 of the Third Configuration Register is set.

7.3 RESYNC MOST SIGNIFICANT BYTE (MSB): ADDRESS X'2'

Write/read :

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8

This register stores the Resync MSB value. On write data operations this value is injected into the encoded NRZI bit stream. During read operations, this value is used for the detection of the Resync mark within the RLL bit stream.

7.4 RESYNC LEAST SIGNIFICANT BYTE (LSB): ADDRESS X'3'

Write/read :

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

This register stores the Resync LSB value. On write data operations this value is injected into the encoded NRZI bit stream. During read operations, this value is used for the detection of the Resync mark within the RLL bit stream.

7.5 ID ADDRESS MARK MSB: ADDRESS X'4'

Write/read:

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8

The user programs the IDAM MSB by writing to this register.

7.6 ID ADDRESS MARK LSB: ADDRESS X'5'

Write/read:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The user programs the IDAM LSB by writing to this register.

7.7 DATA SYNC BYTES (6): ADDRESS X'6'

Write:

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The microprocessor must write 6 bytes to fully program the data sync field value. The first byte must be the LSB. After each write to this location a counter is incremented. The counter value can be viewed by reading this location. It is important to maintain 2FRCLKs during the writing of this register. The 2FRCLKs should maintain the minimum pulse widths as defined in Section 6.3.

Read :

7	6	5	4	3	2	1	0
RSE	FID1	FID0	PID1	PID0	C4	C2	C1

RSE = Read Stop Interrupt

This bit is set at the next SPDET. RDGATE is blocked to the internal device; DLYRDGT is blocked to the drive electronics.

FID1 through FID0 = Future ID Pointer

This counter is incremented whenever the user reads the Data Sync Pointer/Future ID (Address = X'9'). The next expected Track High, Track Low, and Sector bytes must be read serially from this location. The programmer resets these bits when he writes to Address X'9'.

PID1 through PID0 = Present ID Pointer

This counter is incremented whenever the user r eads the ID Compare Preset Register (Address = X'D'). Writing to Address X'9' resets these bits.

C2 through C0 = Data Sync Counter

Number of bytes written to Data Sync register. This value is reset on soft reset (Address = X'9').

7.8 SYNC THRESHOLD/TOF SIZE: ADDRESS X'7'

Write/read:

7	6	5	4	3	2	1	0
T3	T2	T1	T0	M3	M2	M1	M0

T3 through T0: TOF window size (increment = one 2FRCLK)

M3 through M0: Sync Field Majority vote trigger point (Value range = 0 > 12 base 10)

The user sets the percentage of the Sync Mark that must be found before an AMDET is generated in the Data field. Each incremental value changes the correlation percentage by 8.33%.

7.9 RESYNC ERROR THRESHOLD/ DATA SEGMENT SIZE: ADDRESS X'8'

Write/read:

7	6	5	4	3	2	1	0
DS16	DS8	DS4	DS2	DS1	TD4	TD2	TD1

DS16 through DS1 = Data Segment length
Value range = 0 through 31 base 10

This field sets the quantity of data bytes between RESYNCS within the data field. The present formats define this field to be 14_{10} or 19_{10}. (DS16-DS1 = # of byte between resyncs minus 1)

TD4 through TD1 = Resync Error Threshold
Value range = 1 through 7, base 10

This field determines the number of resyncs that are detected within a single sector. When this value is reached or exceeded, the Resync Error Flag in the Status Register is set.

7.10 DATA SYNC POINTER RESET: ADDRESS X'9'

Write :

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Writing to this address location resets all internal pointers which are used for multiple write operation. The pointers that are affected are the Data Sync Write Pointer, Present ID Write/Read Pointers, and Future ID Read Pointer. The Data Sync Pointer selects which register is to be written when writing to location '06'. The Present ID Write/Read Pointers are two independent counters which determine the location of the initial ID compare values. The Future ID Read Pointer identifies which byte of the expected ID counter is being read. The 2FRCLK should be operating at this time.

Read:

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0

If the autoincrement functions are enabled, the WD60C31B can perform ID compare operations for ID field bytes other than the original bytes. The user reads the internal counter which predicts the next ID field to be verified. To read all three bytes (Sector byte, Track Low byte, and Track High) the user must perform repeated reads of this location. The byte that is read is identified in the Data Sync Status Register (Address X'9').

7.11 PHASE LOCK DELAY: ADDRESS X'A'

Write/read:

7	6	5	4	3	2	1	0
FS	IDS	P5	P4	P3	P2	P1	P0

FS = Flag Window Select

This bit defines the placement of the internal flag window for flag field detection. The flag window, nominally 6 bytes, is placed with reference to the last ID read. This bit is "0" if the last ID read is predicted to be ID number 3. This bit is "1" if the last ID read is predicted to be ID number 2. During the ID read operation, the WD10C00 should generate an AMENA during the last byte of the last ID that is read, normally the second CRC byte. Generally, the AMENA should not be generated unless the ID field passes a bit for bit comparison. The WD60C31B then delays the appropriate number of byte times and opens the flag window.

IDS = ID Window Enable
(Active state = 1)

When active, the detection of the ID Address Marks is limited to three small windows, ± eight 2FRCLKs. This reduces the probability of false ID AM detection.

P5 through P0 = Programmable Phase Lock Delay from DLYRGT (Value range = 0 through 63)

The user can set the time difference between the Delayed Read Gate and the PHASELK output signal.

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7.12 SECONDARY CONFIGURATION: ADDRESS X'B'

Write/read:

7	6	5	4	3	2	1	0
FMT	SE35	IDW	XX	RGH	SP0	RS1	RS0

FMT = Format Enable
(Active state = 1)

If active, the WD60C31B is set for a format track mode when WRTGATE is received.

SE35 = Media Select
(Active state = 1)

When active, the WD60C31B sets the internal operation for 3.5-inch, ANSI continuous composite format sector sizes.

IDW = Disable Internal ID and Data Window Generator (Active State = 1)

Normally, the WD60C31B generates internal windows for predicting the location of the ID and data fields. When this bit is active, the internal window generator for ID and data is defeated. Instead, the WD60C31B relies on an external signal, SEQOUT from the WD10C00. SEQOUT, along with RDGATE, selects the type of field the WD60C31B is expecting to read. (The default sector size is 746 and 1360 bytes). A typical situation is as follows: The WD10C00 waits for a SPDET and then raises a read gate. The WD60C31B searches for an address mark. The WD60C31B then sends the ID field to the WD10C00. When the WD10C00 finds the appropriate number of IDs, read gate is dropped. SEQOUT is sent to the WD60C31B to identify the next read operation as a search for a data sync mark. This feature is primarily used with soft-sectored media.

RGH = Read Gate Hold
(Active state = 1)

When active, the DLYRGT signal is extended to the read channel by nine RRCLKs. This occurs only if READGATE is raised and lowered in the ID field. This is useful when maintaining the PLL phase mode between consecutive ID fields. The Read Gate signal from the WD10C00 must be dropped after each ID field.

SP0 = Speed Tolerance Selection
(5.25-inch only)

The programmer sets the expected spindle motor tolerance. This tolerance changes sector mark detection windows. When this bit is 0, the sector mark window is set for a .5% speed tolerance. When this bit is 1, the window is set to a 1% speed tolerance.

RS1	RS0	MODE
0	0	Fixed Window - 12 clocks, .5% speed tolerance
0	1	Fixed Window - 18 clocks, 1% speed tolerance
1	0	Progressive Windows - The resync window is initially set to a minimum value (six 2FRCLKs). If a resync is not found, the resync window is increased by four clocks for each resync that is not found.
1	1	Progressive Windows - The resync window is initially set to a minimum value (eight 2FRCLKs). Window increases by eight clocks for each resync that is not found. Maximum window = 24 clocks.

7.13 THIRD CONFIGURATION: ADDRESS X'C'

Write/read:

7	6	5	4	3	2	1	0
ID1	ID0	SMS	T4	RDI	DCI	DC0	SME

ID1,0 = ID Status Select Bits

These bits select which status byte of four possible bytes to read from Address E.

ID1	ID0	
0	0	Control Register
0	1	ID Error Status
1	0	Present ID/Data Sync Read
1	1	Reserved

SMS = Small SYNCDET Enable (Active State = 1)

When enabled, this bit reduces the size of the SYNCDET to one NRZI bit. Normally, the SYNCDET signal is set during Bit 1 of the Address Mark byte and remains set until RDGATE is dropped. If this mode is enabled, the SYNCDET is only a pulse. During the reading of the ID fields, the RDGATE can remain on throughout all the ID fields. The SYNCDET is raised for each ID address Mark that is found. However, in both cases RDGATE must be dropped before reading the data field.

T4 = TOFWIN Window Size MSB (Active state = 1)

This bit is used in conjunction with T3 through T0 of the Sync Threshold/Size register. This bit extends the size of TOFWIN byte from 0 to 31 2FRCLKs. This is the MSB of the count value.

RDI = Read Gate/SPDET Interrupt Mask (Active state = 1)

When this bit is set, an interrupt is generated if RDGATE is active when the SPDET is sent.

DC1,0 = Data Segment Transfer Count (used in Mode 2 and Mode 3 operations)

If a Data Sync is not detected for a given minimum threshold, the programmer can select a Resync as the synchronization mark for the data field. DC1 and DC0 define the quantity of data segments that are sent to the WD10C00 before the Resync detection logic is enabled. A data segment is the quantity of data bytes between Resync marks as defined in the Rsync Error Threshold/Data Segment Size Register, Address X'8'.

DC1	DC0	DATA SEGMENTS
0	0	1
0	1	2
1	0	3
1	1	4

SME = Pseudo Sector Mark Error Enable (Active state = 1)

When active, a pseudo sector mark error flag is set and an interrupt is generated (if Bit 4 of the Primary Configuration is set). This error occurs if a sector mark is not detected, an SMDET is generated due to a timeout, and a write operation is attempted. In addition, the DLYWGT signal is disabled to the drive.

7.14 ID COMPARE PRESET REGISTER: ADDRESS X'D'

Write/read:

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

The microprocessor loads the ID field with the Sector byte, Track Low byte, and Track High byte which is used during the ID on-the-fly comparison. The Sector byte must be loaded first, then Track Low and Track High. Repeated reads are necessary to obtain these three values. The ID Status Register, Address E, contains a value that identifies which value is being read.

7.15 ID CONTROL/STATUS REGISTER: ADDRESS X'E'

Write:

7	6	5	4	3	2	1	0
3ID	IDE	RCM	REM	TAE	SAE	IT1	IT0

3ID = 3 ID Enable
(Active state = 1)

When this bit is set, the special 3 ID on-the-fly mode is enabled. In this mode the WD60C31B reads the IDs for the WD10C00 and relays this information to the WD10C00.

IDE = ID Error Interrupt Enable
(Active state = 1)

When this bit is set, an interrupt is generated whenever the ID Compare is completed and an error is detected.

RCM = Read Complete Interrupt Mask
(Active state = 1)

When this bit is set, an interrupt is generated whenever the end of a data field read operation is reached.

REM = Resync Threshold Error Interrupt Mask
(Active state = 1)

When this bit is set, an interrupt is generated whenever the Resync Error Counter is activated.

TAE = Track Autoincrement Enable
(Active state = 1)

When this bit is active the Track High and Track Low bytes can be incremented whenever the maximum sector is detected and the last ID comparison is good.

SAE = Sector Autoincrement Enable
(Active state = 1)

When this bit is active, the expected sector value can be incremented after a good ID comparison.

IT1,0 = ID Compare Threshold Bits

These bits define the quantity of good ID field(s) which must be detected before the WD60C31B flags the WD10C00 of a good operation. IT1 is the MSB.

IT1	IT0	Good IDS Detected
0	0	Not valid
0	1	1
1	0	2
1	1	3

Read:

This address location can contain three possible status bytes. The Third Configuration Register, ID1 (Bit 7) and ID0 (Bit 6) determine which is status byte is to be read.

Control Register (ID1 = 0, ID0 = 0)

7	6	5	4	3	2	1	0
3ID	IDE	RCM	REM	TAE	SAE	IT1	IT0

ID Compare Error Status (ID1 = 0, ID0 = 1)

7	6	5	4	3	2	1	0
SP	C3	C2	C1	I3	I2	I1	ICE

SP = Pseudo Sector Mark Detect
(Active state = 1)

When active, no sector mark is detected within the internal sector mark wihdow. A pseudo SPDET is generated. This bit is cleared when an authentic sector mark is detected.

C3 through C1 = ID Cyclic Redundancy Check (CRC) Error

These error bits occur under the following conditions: ID AM is detected, ID Track and sector bytes are compared and a CRC fault exists. C3 is status for the Third ID; C2 for the second ID.

I3 through I1 = ID AM and ID Field Match

These status bits are active whenever an ID AM is found and the ID field track and sector bytes match. The ID Threshold limit set in the ID Control Register determines the validity of this status.

ICE = ID Compare Error
(Active state = 1)

This bit is set whenever the ID Threshold (set by the Control Register) is not met by the end of the ID zone. An interrupt can also be generated if enabled in the ID control Register.

Present ID/Data Sync Status (ID1 = 1, ID0 = 0)

7	6	5	4	3	2	1	0
DS3	DS2	DS1	DS0	PIR1	PIR0	DR	XX

DS3 through 0 = Reserved

DR = Data RDGATE/SPDET Error
(Active state = 1)

When active, this bit indicates that RDGATE was active when SPDET was generated. RDGATE active is due to an extended data field read operation. This bit is cleared when writing to Address 1.

PIR1,0 = Reserved

7.16 SECTOR PER TRACK: ADDRESS X'F'

Write/read:

7	6	5	4	3	2	1	0
RSP	SC6	SC5	SC4	SC3	SC2	SC1	SC0

RSP = Read Stop Enable (Active State = 1)

SC6 through SC0 = Sector per Track

The user defines the number of sectors per track. This register is important whenever the autoincrement function is enabled in the ID control Register. Whenever the predicted ID field matches the maximum sectors per track, the end of the ID field is reached, and the ID Threshold has been met or exceeded, then the internal sector counter sets the sector byte to zero.

A.0 FORMAT DESCRIPTION

The following section describes the functionality of the WD60C31B as it relates to the ANSI Standard Continuous-composite Format for 5.25-inch and 3.5-inch optical drives. The WD60C31B can perform a track format operation on media which is unformatted. This device also performs ID voting functions that previously were handled by the WD10C00.

A.1 OPTICAL FORMAT

The ANSI specified Continuous-Composite Optical Media format is intended for use in Write Only RAM Memory (WORM) and magneto-optic drive applications. The WD60C31B is tailored for this application. The WD60C31B is programmable in order to accommodate future changes to the present format.

A.2 SECTOR FORMAT DESCRIPTION

The sector format is divided into three primary zones. The first zone is the ID area which contains the Sector Mark and three unique ID fields. The second zone is the drive area which contains the Mirror Mark, Flag, and Aauto Laser Power Control (ALPC) fields. The Mirror Mark and ALPC are for servo use. The Flag field is for WORM applications. Flag and ALPC are not used in 3.5-inch applications. The third zone is the data field which contains data, cyclic redundancy check (CRC) and error correction code (ECC).

A.3 SECTOR MARK

The five-byte sector mark is intended to be detected without recourse to use of the phase-locked loop. The pattern does not exist in data. Sector marks are identified by alternating long marks of three and five NRZ bit times.

A.4 VFO AREAS

There are three different lockup areas designated as VFO1, VFO2, and VFO3. The recorded information for VFO1 and VFO3 is identical in length and pattern. The area for VFO2 has one of two possible patterns and is four bytes shorter than VFO1 and VFO3.

Given that there are three concatenated ID fields and RLL 2,7 modulation coding is used, the conditions leading into each VFO2 area will be different depending on the last byte of CRC recorded in the preceding ID field.

A different VFO pattern prior to ID2 and ID3 is needed in order to allow the last byte of CRC to achieve correct decoding. Note that while the entering pattern is different, the VFO2 fields always end in the same pattern. The choice between the two patterns for VFO2 depends on the content of the last byte of CRC in the ID field immediately preceding the one being read.

A.5 ADDRESS MARK (AM)

The Address Mark is a special pattern, not used in RLL 2,7 data, and is a run-length violation for RLL (2,7) encoding.

A.6 ID AND CRC

The ID field consists of 5 bytes, allocated as follows:

- 2 bytes of track address, MSB/LSB.
- 1 byte of sector address:
  Bits 7,6 = ID number, (specifies one of three ID fields)
  00 = 1st ID
  01 = 2nd ID
  10 = 3rd ID
  Bit 5 = Reserved for future expansion, (S/B 0)
  Bits 4-0 = Sector Number, (binary value, most significant bit = 4)

The CRC consists of 2 bytes derived from the previous 3 bytes of ID information and using the polynomial:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The CRC calculation begins with the registers containing all 1's. (Refer to CCITT CRC standard). Input and output sequence uses MSB first.

NAME	FUNCTION	PATTERN
SM	Sector Mark	Special Redundant Pattern = 5 3 3 7 3 3 3 3 5 Channel code bit pattern following sector mark = 0010010010
VFO1, VFO2, VFO3	Lockup Field	VFO1= 01001001001...010010 VFO2= 10010010010...010010 VFO2= 00010010010...010010 VFO3= 01001001001...010010 *Note that VFO2 varies according to previous CRC pattern.*
AM	Address Mark	(Bit/Byte Sync) 16 code bits, (1 byte) 0100 1000 0000 0100
SYNC	Redundant Sync for data	Triple sync pattern 0100 0010 0100 0010 0010 0010 0100 0100 1000 0010 0100 1000
ID	Track number (2B) Sector number (1B)	High order/low order Bits 7-6 = ID Number (ID 0-2) Bit 5 = Reserved, (S/B 0) Bits 4-0 = Sector Number
CRC	ID field check bytes	CCITT Polynomial =1's
PA	Postamble	Allows last CRC byte closure under RLL (2,7) modulation
ODF	Offset Detection Flag	Unwritten, no grooves
Gap	Gap (Splice)	Unwritten - 3 byte areas
FLAG	Indicates written block continuous pulse	(5-byte area, decision by majority) 1001001001001001001001001001001001.
ALPC	Auto Laser Power Control	Blank 2-byte zone
DATA	User data, control, CRC, ECC and Resync	See Figures A-1 through A-4
BUFFER	Used for RPM timing margins	Unwritten area
RESYNC	Data field byte Sync	16 code bits (1byte) 0010 0000 0010 0100

TABLE A-1. SECTOR FIELD FUNCTIONS

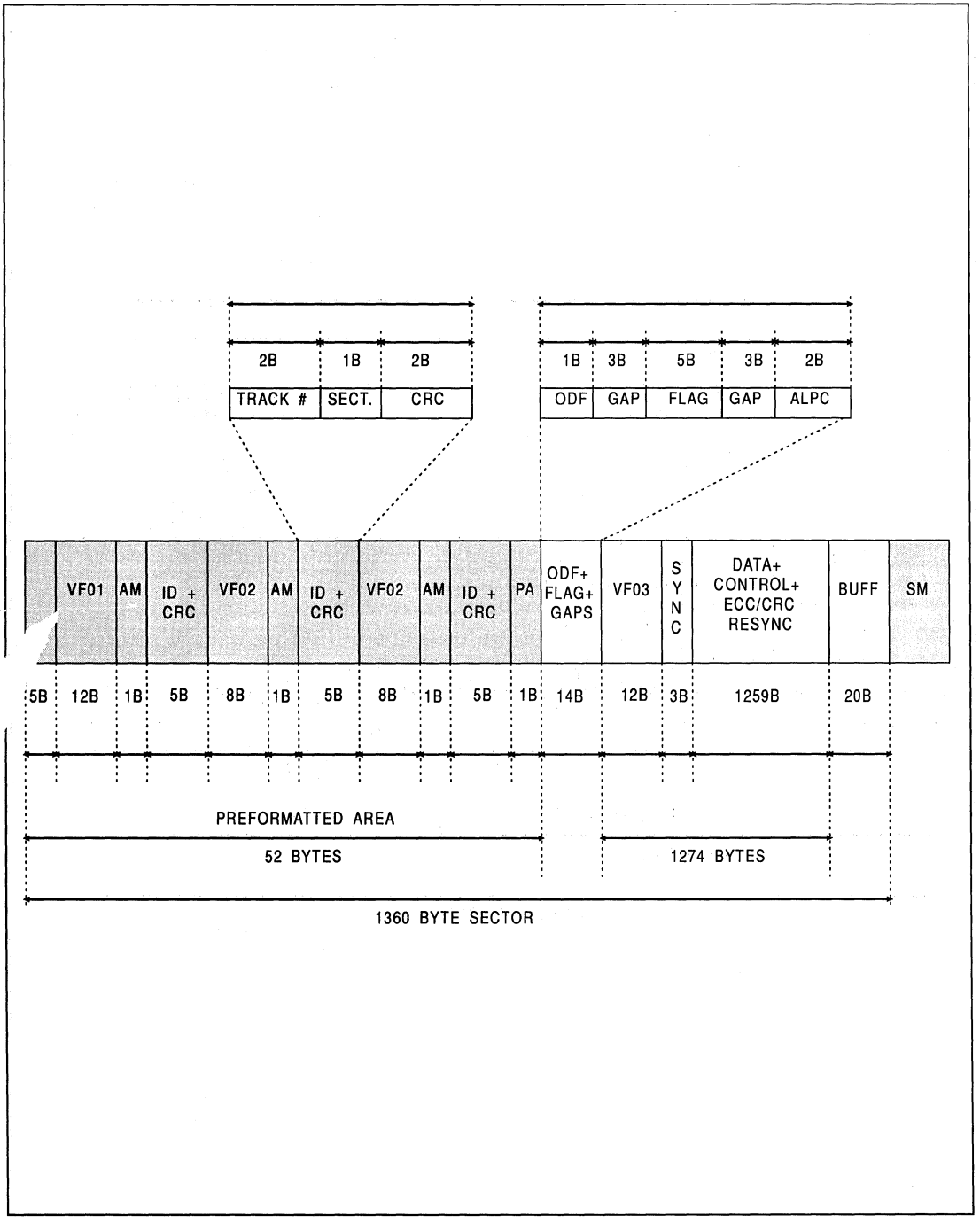

FIGURE A-1. 5.25-INCH, 1024-BYTE FORMAT

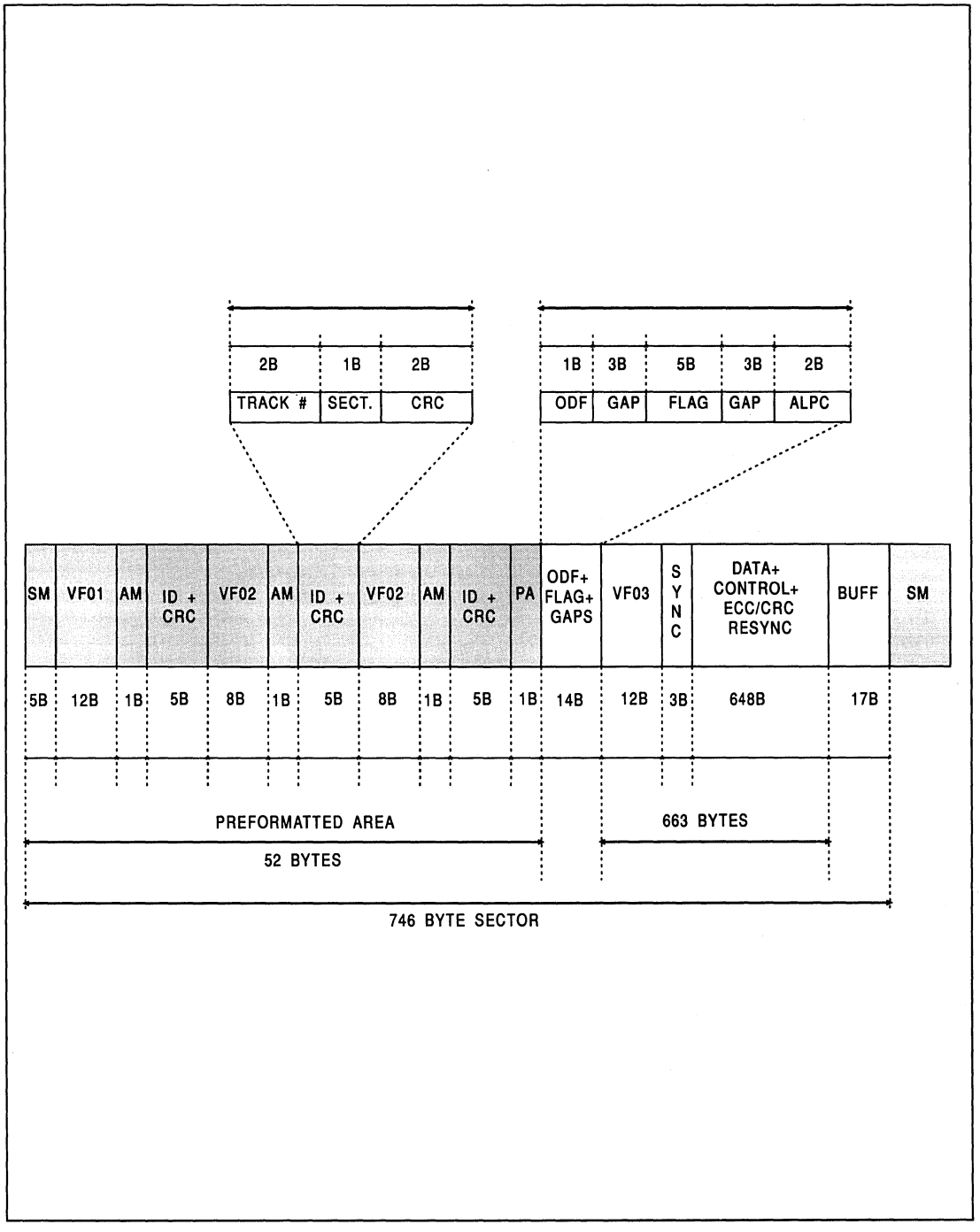

FIGURE A-2. 5.25-INCH, 512-BYTE FORMAT

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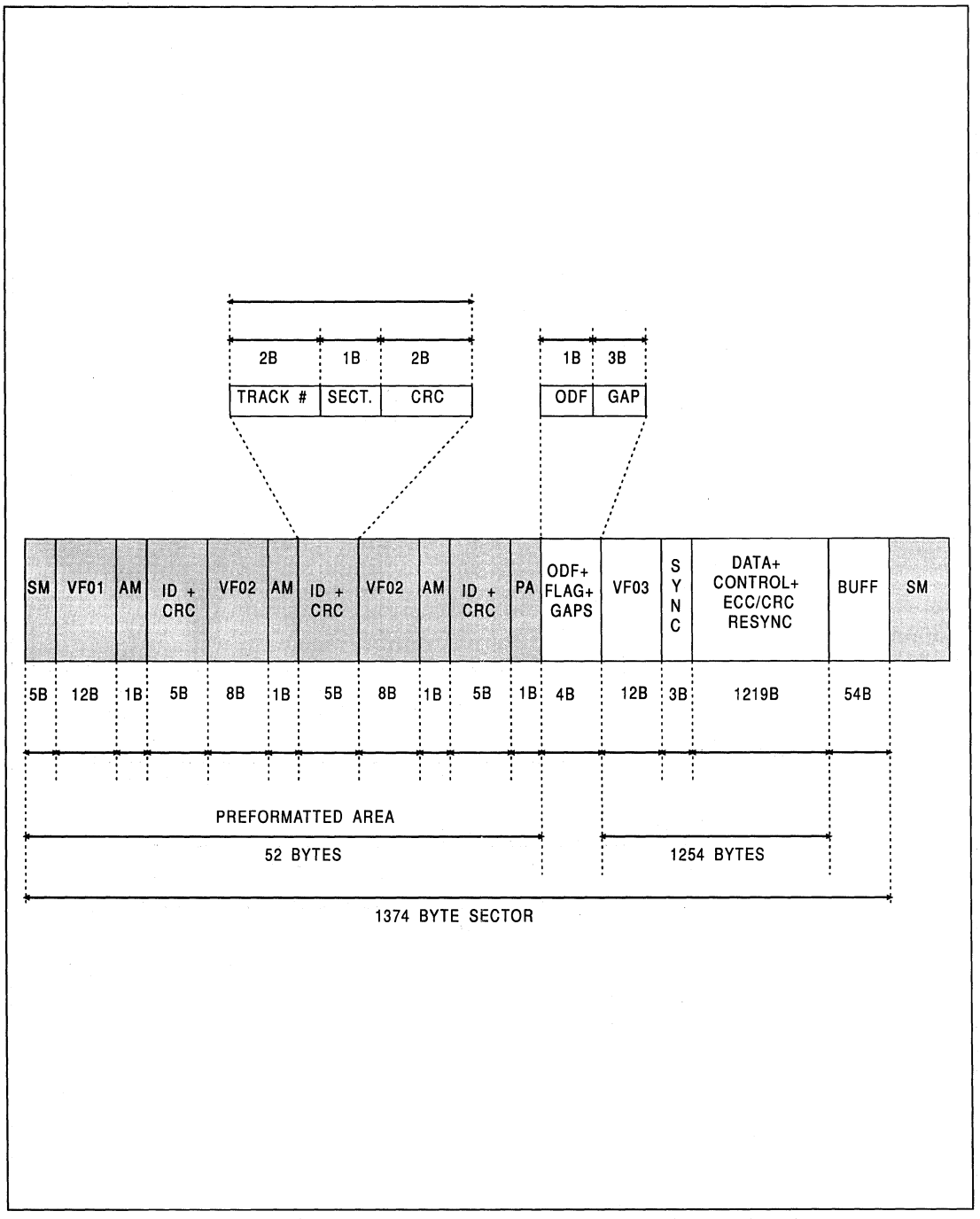

FIGURE A-3. 3.5-INCH, 1024-BYTE FORMAT

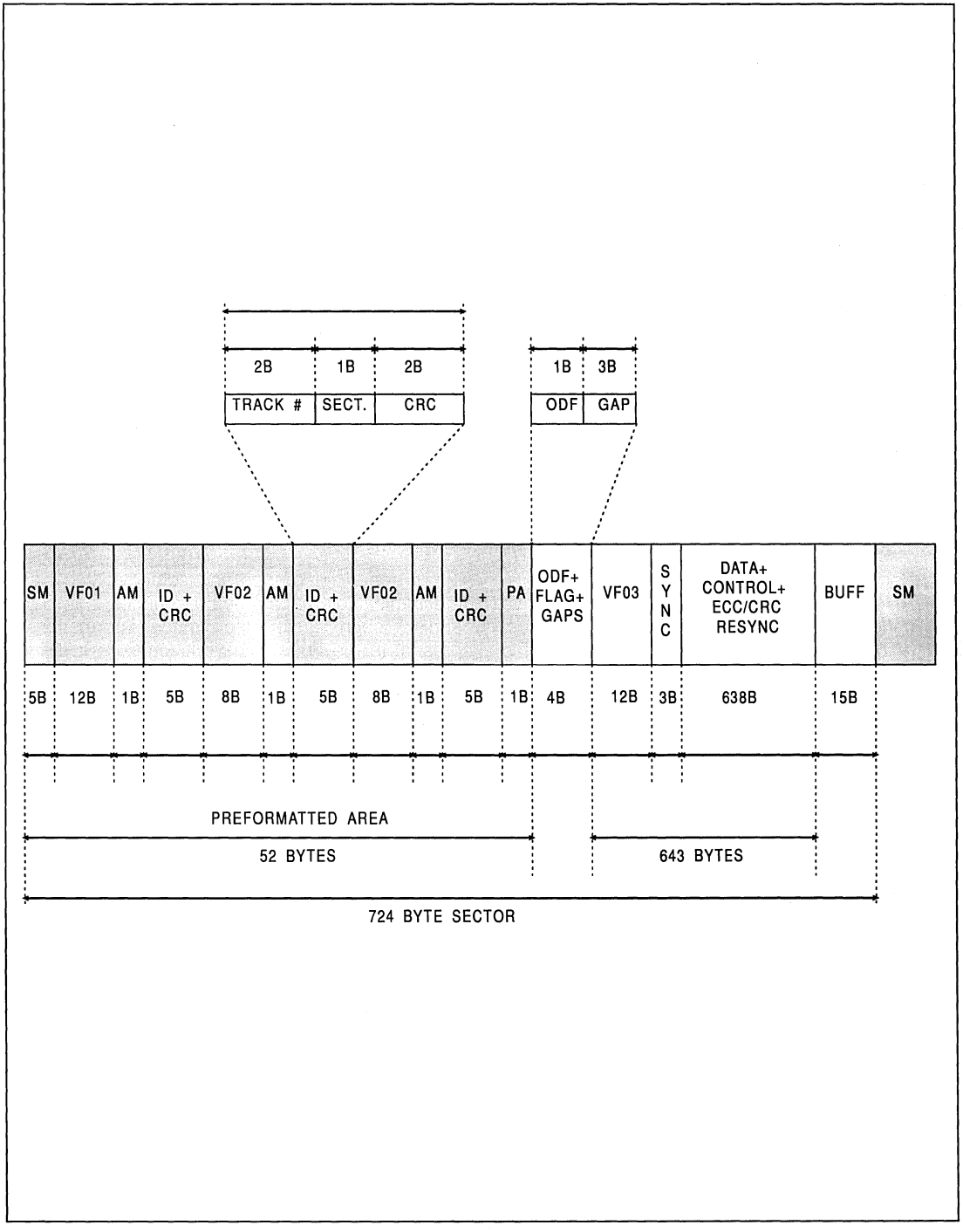

FIGURE A-4. 3.5-INCH, 512-BYTE FORMAT

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A.7 POSTAMBLE (PA)

The last portion of the preformatted area (PA) consists of a one postamble byte on the third ID field. Due to the use of the RLL 2,7 encoding scheme, the framing of the last byte of CRC in the last ID field is uncertain within a few bit times. The postamble allows the last byte of CRC to achieve closure and permits the ID field to always end in a predictable manner.
This is necessary in order to locate the Offset Detection Flag/Mirror Mark in a consistent manner.

A.8 ODF / MIRROR MARK

The Offset Detection Flag (ODF) or Mirror Mark is an area with no grooves or preformatted data. The purpose is to allow track offset detection within the drive.

A.9 FLAG

The flag field prevents inadvertent write operations over previously written data in WORM drive applications. The flag may be written after successful completion of the write operation or during the same pass. The use of this field is optional. It is not used in 3.5-inch format.

A.10 AUTO LASER POWER CONTROL (ALPC)

The Auto Laser Power Control is a grooved test area for calibration of the laser power levels used by the drive. It is not used in 3.5-inch format.

A.11 DATA FIELD

The data field consists of 1024 bytes of user data and 223 bytes of CRC/ECC/Resync information, plus 12 bytes of control information. A 512-byte data field is optional. The 3.5-inch format has reduced the pointer field to xxx bytes for the 512-byte sector.

A.12 RESYNC

The resync mark reestablishs byte synchronization when it is lost during a data segment. (A data segment consists of the bytes of data, usually 15 or 20 bytes, between resync marks.)

Resync marks are used in only the Data/Control/ECC/CRC field. Resync marks are written within the data as shown in Figures A1 through A4.

A.13 BUFFER

Motor speed tolerances and some electrical and mechanical tolerances require a buffer zone at the end of each sector. No written information is present in the buffer. The buffer field is a 1-byte postamble to the data field to allow closure of channel bits in the RLL 2,7 encoding scheme. During format, however, this area is filled with a high-frequency pattern of "100".

B.0 WD60C31 FUNCTIONS

B.1 READ OPERATIONS

The WD60C31B is responsible for the detection of the following special format marks:

B.1.1 SECTOR MARK

The WD60C31B is constantly in a sector mark detection mode. If a sector mark is detected (3 of 5 majority), a (Pseudo Sector Mark Dectect) SPDET pulse goes to the WD10C00. If no sector mark is detected at the end of each sector, the WD60C31B creates a SPDET. The created SPDET is based on a worst case speed tolerance of +/-.5 % or 1%. This mark is detected under a window, .5% or 1%, thereby minimizing misdetection.

B.1.2 ID ADDRESS MARK

The WD60C31B examines the input RLL bit stream whenever an ID field area is expected and RDGATE is active. RDGATE should be applied after a SPDET is sent. The RLL pattern is programmable by the microprocessor. The RRCLKs are paused when RDGATE is raised and NRZI goes from high to low. Once the ID AM is detected, the RRCLKs begin again. The NRZI data stream is a byte of zeros and the ID field (Track High byte, Track Low byte, and sector byte) follows. A SYNCDET pulse is sent along with the first ID address byte. The WD10C00 should be programmed to wait for the SYNCDET signal and expect the Track High byte to be the Address Mark. The WD10C00 then performs a bit-for-bit comparison and CRC verification. The WD60C31B can also be placed in another mode, the ID Search mode. This mode should be used whenever the Track High byte is not predictable. This is used to satisfy WD10C00 requirements. In this mode, the SYNCDET signal is moved forward one byte. This means that this signal becomes active during the byte of zeros preceding the Track High byte. The WD10C00 should be programmed to wait for the SYNCDET and an address mark of zeros. A bit-for-bit comparison over the complete ID field is performed. The WD10C00 stores the full ID field in its internal registers. The Normal mode only stores the Track Low byte, sector byte, and CRC.

B.1.3 DATA ADDRESS MARK

The WD60C31B examines the input RLL bit stream whenever the Data field area is expected and RDGATE is active. The RLL pattern that is expected is microprocessor programmable. In addition, the level of pattern correlation is programmable. A SYNCDET pulse is sent whenever a comparison is made. This pulse is sent along with a psuedo-address mark NRZ byte of '00's. The WD10C00 is programmed to make this comparison.

B.1.4 DATA RESYNC MARKS

The WD60C31B detects and removes the Resync marks from the NRZI data stream. An internal window is generated which predicts the location of the next resync. This window minimizes the probability of misdetection In normal mode, the internal resync window is opened if RDGATE is raised in the data field, the Data Sync has been detected, and a data segment has passed. Four programmabale window sizes are available: two fixed sizes and two variable sizes. The ANSI specification states that the number of bytes in a data segment is 15 or 20. The WD60C31B permits the microprocessor to set the value from 0 to 31 bytes. A value of zero assumes that there are no resyncs. In addition, the Resync mark pattern can also be programmed. In an error recovery mode, RDGATE must be applied in a data field, but the Data Sync Mark need not be detected. Instead, the Resync mark is the first mark to be detected. The first resync window is opened after a preprogrammed number of bytes are sent to the WD10C00. This means that the WD10C00 receives the exact number of data bytes per sector. This mode is used if the data sync is undetectable after lowering the Data Sync Threshold value.

B.2 WRITE FUNCTIONS

During write, the WD10C00 and WD60C31B must write in the Media Data Format the following pattern: 1) VFO field, 2) Data Address Mark, 3) Encoded RLL Data, 4) Data Resync Marks, and 5) Data Postamble. The WD10C00 sends a dummy VFO pattern that contains the exact number of bytes that are written on the disk. The WD60C31B creates the actual high frequency pattern, "100100". The WD60C31B continues writing this pattern until an AMENA signal is sent from the

WD10C00. This AMENA signal is sent with the last byte of the dummy VFO. When AMENA is received, the VFO is completed at a byte boundary and the Data Sync Mark is injected into the RLL data stream pulse which initiates the writing of the Data Sync Mark. When the WD60C31B inserts the Data Sync Mark or the Rsync Marks into the RLL data stream, the RRCLKs are paused. This action halts the data byte transfer through the WD10C00. In effect, the WD10C00 is unaware of this pause. This pausing of the RRCLKs is also performed during a read operation. The WD10C00 sends data bytes, CRC bytes, and ECC bytes. An AMENA is sent with the last byte of the ECC field. This action ends the insertion of the Resync marks into the encoded RLL data stream. In addition, 3 bytes of pad should be sent after the last byte of ECC. These bytes compensate for the WD60C31B internal pipeline structure and closure requirements of the last bit of the last byte of ECC.

B.3 FORMAT OPERATION

The WD60C31B is also capable of performing a track format operation. This allows the WD60C31B to operate with drives that use either prestamped media or nonstamped media. The format must conform to the prestamped format requirements. The task of formatting the media is shared by the WD10C00 and the WD60C31B. In general, the WD10C00 must 1) keep track of the number of bytes that are written on the track; and 2) inform the WD60C31B when the special marks (sector mark, ID address marks, and Data Sync Mark) are to be inserted into the RLL data stream. The WD60C31B is responsible for encoding and decoding the NRZ serial data from the WD10C00; inserting the special marks mentioned above (also Resync Marks), and predicting the next type of special mark to be written.

The general format sequence is as follows:

1) All special marks are programmed in the WD60C31B.
2) The WD60C31B is set for Track Format (Secondary Configuration Register).
3) The drive provides an Index to the WD10C00.
4) The WD10C00 raises Write Gate when Index is received. The NRZ data transfer begins. The first NRZ data bit this sent must be a 1.
5) Upon receiving Write Gate, the WD60C31B begins writing the first Sector Mark. All subsequent sector marks are written when a specific number of AMENAs are received. The NRZ data from the WD10C00 is internally pipelined within the WD60C31B. When the pipeline is full, the RRCLKs are paused. When the writing of the sector mark is complete the RRCLKs start again and NRZ data encoding begins and is merged into the RLL data stream.
6) The WD60C31B continues to encode the NRZ data until it receives an AMENA. This pulse from the WD10C00 defines the concurrent NRZ data byte as the last byte before the next special mark. The special mark is inserted and encoding continues. RRCLKs are restarted. The WD60C31B keeps track of the quantity of AMENAs that are sent. The type of special mark to be inserted is based on the quantity of AMENA signals received.

B.4 MODULATION METHOD

The modulation method used to record all information on the disk in the formatted areas shall be the Run-Length Limiting (RLL) code known as RLL 2,7.

CODE CONVERSION	
NRZ Input Bits	**RLL 2,7 Channel Code Bits**
10	0100
010	100100
0010	00100100
11	1000
011	001000
0011	00001000
000	000100

B.5 ID VOTING (ON-THE-FLY ID VERIFICATION)

In addition to the previously discussed methods of ID read operations, the WD60C31B can perform ID voting. In this mode, the WD60C31B detects and verifies the validity of the three IDs. The IDs undergo the following test.

- Detection of a valid ID Address Mark byte
- A successful bit-for-bit comparison of the track and sector bytes
- A successful match of CRC from the drive to an internally derived CRC

If these parameters are met, a single ID is considered valid. The user can program the number of IDs which must be found to satisfy a write or read operation. When all conditions are met, the WD60C31B sends the WD10C00 a SYNCDET and an address mark byte of F0 on the NRZI line. If all conditions are not met, the WD60C31B sends a SYNCDET and an address mark byte of FF to the WD10C00.

Track streaming is also supported. This means that the internally stored track and sector values can automatically be incremented when the ID threshold is met. The user must set up three conditions. First, the three ID modes must be enabled. Second, the maximum number of sectors per track must be set. Third, the track and/or sector autoincrement function can be independently enabled. This function minimizes the microprocessor overhead between sector IDs.