COMPUTER DESIGN

THE DESIGN AND TS, EQUIPMENT & SYSTEMS

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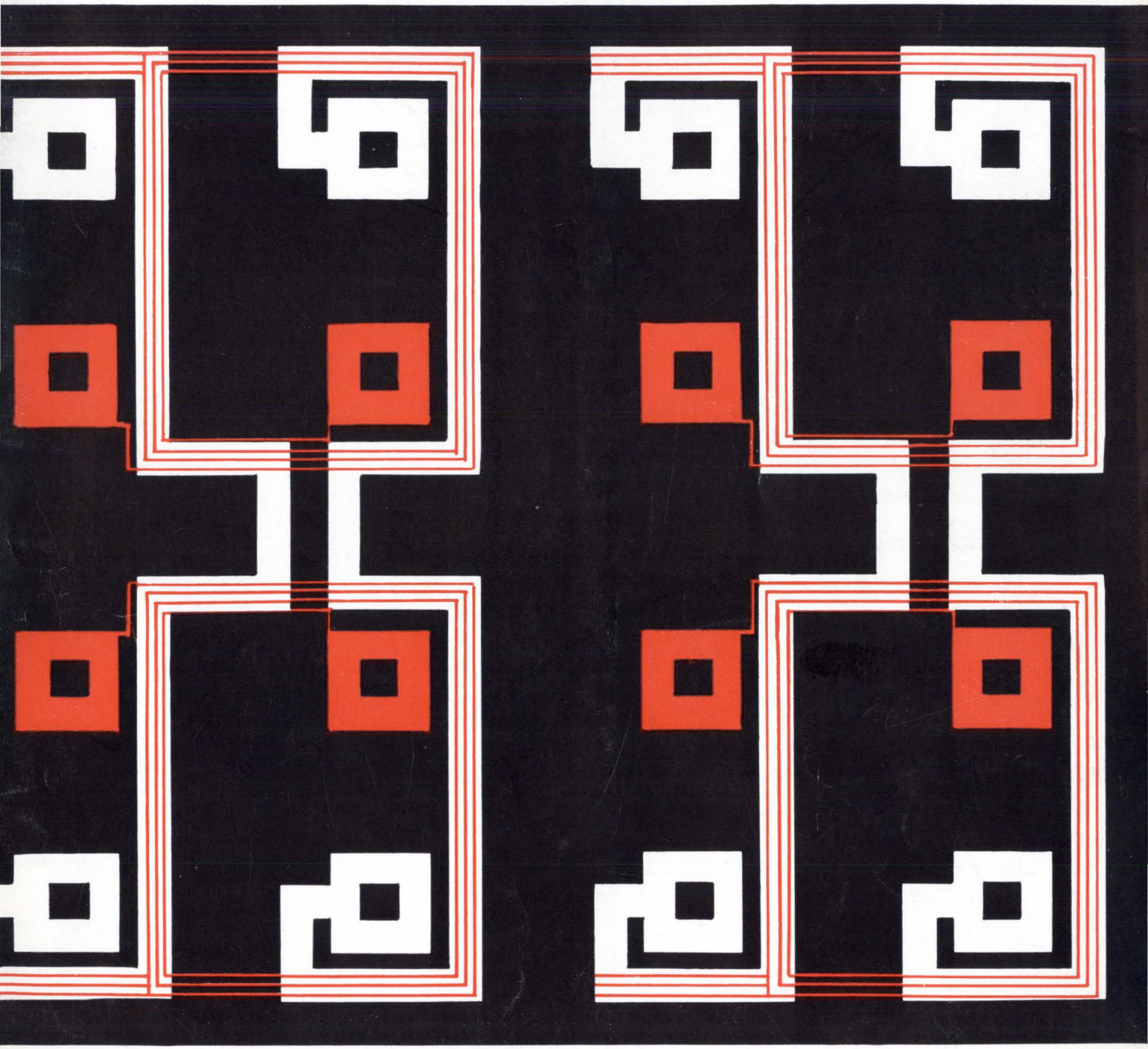
SEPTEMBER 1965



IN THIS ISSUE: DISCUSS-ONLY SESSIONS AT THE 1965 FJCC
What will be discussed and how you can participate.

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24-bit word DDP-124 features monolithic integrated circuit μ-PAC^{tm} construction; fast, reliable, and flexible logic configuration — binary, parallel, sign/magnitude, single address with indexing, powerful command structure. Over 285,000 computations per second. MEMORY: 8192 words (expandable to 32,768) directly addressable; cycle time 1.75 μsecs. INPUT-OUTPUT: Typewriter, paper tape reader and punch. (Strong optional I/O capability and broad range of peripheral equipment.) SOFTWARE: FORTRAN II and IV, assembler, executive, utility and service routines. Fully program compatible with DDP-24 and DDP-224 general purpose computers. Write for complete specifications.

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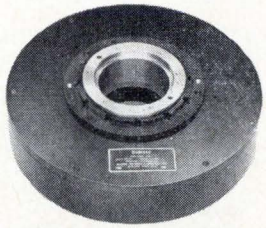

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*For photographs of ARCSEC Encoders see DIGISEC Units of same diameter.

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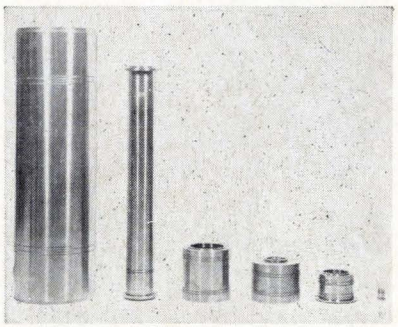
Wayne-George Corporation also offers a line of Air Bearing Sidereal Rate Tables for calibration and testing of gyro and inertial systems as well as encoders in standard and special configurations.

COUPLINGS



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CIRCLE NO. 2 ON INQUIRY CARD

SEPTEMBER 1965 • VOLUME 4 • NUMBER 9

COMPUTER DESIGN

FOR ENGINEERING PERSONNEL RESPONSIBLE FOR THE DESIGN & APPLICATION OF DIGITAL CIRCUITS, EQUIPMENT, AND SYSTEMS IN COMPUTING, DATA PROCESSING, CONTROL AND COMMUNICATIONS.

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BPA

Circulation over 24,000

FEATURES

14 CD READERS' FORUM

Continuing the discussion on logic symbol standards initiated in the recent May issue, CD readers give their opinions as to the necessity for a standard and their preference for a particular proposed standard.

20 DISCUSS-ONLY SESSIONS AT FJCC

The coming 1965 Fall Joint Computer Conference has scheduled some technical sessions as discuss-only sessions. Since the papers for these sessions will not be read at the conference, attendees must study the papers in advance in order to prepare themselves for meaningful discussion periods. Reviews of the papers involved are presented in this issue along with procedures for obtaining the advanced copies. Also, one of the papers, "Design Considerations for a 25 Nsec. Tunnel Diode Memory," is presented in its complete form.

44 REMOTE TIME-SHARING SYSTEM PERMITS ECONOMICAL PROCESSING OF SHORT ENGINEERING PROBLEMS

The "Quiktran" system allows up to 40 remotely-located engineers to enter, check, translate, and execute different programs concurrently on the same processor.

46 THE VARIABLE-THRESHOLD LOGIC CONCEPT

New integrated circuit approach results in outstanding noise-rejection capabilities and high temperature stability.

DEPARTMENTS

4 EDITORIAL NOTES

6 LETTERS TO EDITOR

8 DC OUTPUT

10 INDUSTRY NEWS

17 GOVERNMENT REPORTS

58 NEW PRODUCTS

• Circuit Components • Circuit Packaging • Input-Output Equipment • Console Equipment • Power Supplies • Memories • Test Equipment • Systems • Circuit Modules

78 LITERATURE

80 ADVERTISERS' INDEX

Reader subscription cards ..... opposite page 16
Reader inquiry cards ..... opposite page 64

DATA COMMUNICATIONS

equipment for on-line, real-time processing

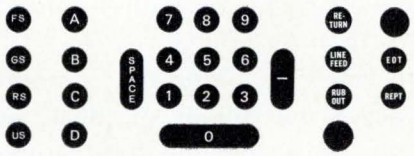
there are keyboards...and there are keyboards

Data communications vary, requiring a variety of different keys and even different keyboards. This is why there are Teletype sets available with 3-row keyboards, 4-row keyboards, and numeric keyboards, having a variety of special purpose keys.

The 3-row keyboard operates on the 5-level Baudot code. The new 4-row keyboard is similar to the standard office typewriter, and operates on an 8-level code that's compatible with the American Standard Code for Information Interchange. It can communicate directly with computers and other business machines in data processing systems. The numeric keyboard consists of 25 keys that are used primarily to speed transmission of coded numeric data such as used to control inventory and delivery in warehouses, supermarkets, etc. Though this Teletype set can send only numeric data, it is capable of receiving and printing all alphanumeric characters.

WHAT ARE THE "KEY" DIFFERENCES?

There are many different special purpose keys on Teletype keyboards. The most commonly used are the function or non-printing keys. On the 3-row keyboard, depressing the LTRS key transmits the letter characters shown on the lower keytops while depressing the FIGS key transmits the figure characters on the upper keytops.



NUMERIC KEYBOARD

On the 4-row keyboard, both the letters and figures are shown on the lower part of the keytops. Thus, the SHIFT key enables the code combinations to be generated for the printing characters shown on the upper keytops, such as "&" and "%". A CONTROL key is used to generate the code combination for the function characters shown on the upper keytops, such as "WRU" (who are you?) and "EOT" (end of transmission).

ERROR DETECTION AID

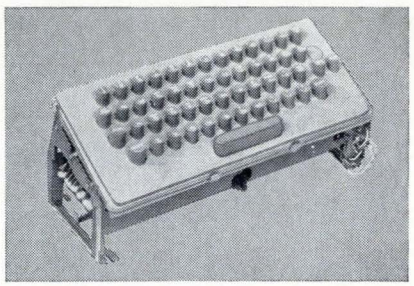
The 4-row keyboard can generate an "even parity" which is used to aid in error detection. Even parity provides for adding a marking pulse whenever the number of marking pulses in a code combination is odd. Thus, if a code having an odd number of marking pulses is received, it indicates an error. The eighth level is used for providing even parity.

machines that make data move

On friction feed typing units, depressing the LINE FEED key causes the paper to advance one line. Sprocket-feed typing units are equipped with both LINE FEED and FORM-OUT keys that cause the platen to advance a printed business form either one line or a sufficient distance to bring the next form to the starting position.

SELF-CONTAINED KEYBOARDS

Self-contained 4-row keyboards are available to provide direct parallel-wire entry of variable data into computers and business machines.



ALPHANUMERIC KEYBOARD

The versatility of Teletype keyboards is another reason why they are made for the Bell System and others who demand reliable communications at the lowest possible cost. If you wish further information on Teletype equipment write: Teletype Corporation, Dept. 71 J, 5555 Touhy Avenue, Skokie, Illinois 60078.

TELETYPE

CIRCLE NO. 3 ON INQUIRY CARD

Editorial Notes

IN SEARCH OF A DIALOGUE

At The 1965 FJCC

Five of the technical sessions at the coming Fall Joint Computer Conference are planned as "discuss-only" sessions. Each of these sessions will be a dialogue between the authors of papers and the attendees. The sessions will be devoted entirely to questions, challenges, rebuttals, and evaluations of the authors' material from the audience. The success of this experimental format depends entirely on the attendees. If they study the pre-printed papers in advance and bring their thoughtfully prepared reactions to the authors' material, then the experience should be exciting for everybody involved.

In cooperation with the FJCC Program Committee, COMPUTER DESIGN is happy to present the details of these sessions in this issue, beginning on page 20. Here you will find reviews of all the papers for the three hardware-oriented discuss-only sessions, one complete paper, and procedures for obtaining the pre-printed volume of all the complete discuss-only papers.

We urge you to read this material carefully so that you can decide to participate in sufficient time to get your advanced copies. Even if only one paper sparks your interest, it will still be worthwhile to send for the pre-prints since the cost will be accredited as part of your conference registration fee.

For CD Readers' Forum

The introduction, in this issue, of a new department called CD Readers' Forum is OUR experiment in promoting the interchange of ideas and opinions. This department is intended for the discussion of any worthy topic or significant facet affecting your professional life and industry.

We will introduce topics that we believe deserve industry-wide discussion but we hope that the content of this department will primarily be determined by our readers. Let us have your opinions, comments, and solutions on what you think are the major problems facing our industry.

S. Henry Sacks

EDITOR

DATA COMMUNICATIONS

equipment for on-line, real-time processing

words for whachamacallits

What is a bit? What does ASCII stand for? What is real-time? These are typical of the jargon of data communications that has become so much a part of data processing.

Listed below are working definitions for terms related to Teletype equipment—the kind made for the Bell System and others who must have the most reliable communications at the lowest possible cost. Additional information on Teletype equipment and its uses is available by writing: Teletype Corporation, Dept. 71J, 5555 Touhy Avenue, Skokie, Illinois 60078.

DATA HANDLING TERMS

Alphanumerics—Characters including letters of the alphabet, numbers, punctuation, and mathematical symbols.

ASCII—American Standard Code for Information Interchange. A 7-level coded character set and recording format approved by the American Standards Association for handling data within processing and communications systems. Teletype Models 33 and 35 equipment use the ASCII code, but add an 8th level for even parity check.

Baudot Code—A 5-level permutation code in which all code elements are of same length. This code is used on Teletype Models 28 and 32 equipment.

Data Communications—The preparation, transmission, and reception of data.

Off-Line—Not connected to a communications network. Paper tapes frequently are punched off-line on a Teletype ASR (automatic send-receive) set and later transmitted on-line using a paper tape reader.

On-Line—Connected to a communications network.

Real-Time—Communications while a process transpires, in order that results be useful in guiding the process.

Total System Concept—Refers to an equipment system providing pertinent information, at the right time and place, and in the right form, so that knowledgeable decisions can be made.

TRANSMISSION TERMS

Baud—Unit of signalling speed. The speed in bauds is the number of code elements per second.

Bit—One impulse, or unit of information represented by a mark or space.

Full-Duplex—A circuit for simultaneous two-way communication.

Half-Duplex—A two-wire circuit for two-way communications, but not simultaneously.

Line Switching—Connecting two terminals through a switching center prior to exchanging information.

Mark—An impulse in a neutral circuit, which causes the loop to be closed; or in a polar circuit, which causes the loop current to flow in a direction opposite to that for a space impulse.

Message Switching—Receiving and storing messages, and retransmitting them on appropriate outgoing circuits.

Parallel—Refers to a system in which the elements defining a character occur simultaneously.

Serial—Refers to a system in which the elements defining a character occurs sequentially.

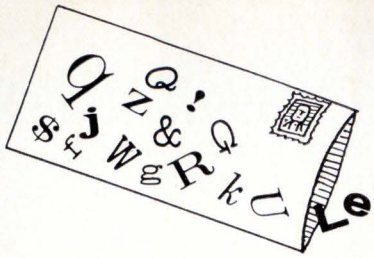
Space—An impulse, which in a neutral circuit, causes the loop to open; or in a polar circuit causes the loop current to flow in a direction opposite to that for a mark impulse.

Start-Stop—A system of operation whereby the start impulse precedes the first impulse of each character and is always a spacing impulse. The stop impulse follows the last impulse of each character and is always a marking impulse.

machines that make data move

TELETYPE

CIRCLE NO. 4 ON INQUIRY CARD



Letters to the editor

ULTRA-HIGH-SPEED TRANSISTORS

To The Editor:

I recently read your article "Ultra-High-Speed Transistors" in the July 1965 issue of your publication COMPUTER DESIGN and found it so amusing, I had wished I had written it myself. My congratulations to its author and your editorial staff.

Since others associated with me found it equally amusing, I have been deluged with requests to reprint it in a monthly publication I edit for a Westinghouse Field Support Department of the Corporation's Defense & Space Center in Baltimore.

If you would grant me permission to reprint the article in my publication, I would be only too happy to reprint it verbatim and with proper credits.

My publication is distributed among engineering personnel of the Westinghouse Electric Corporation scattered throughout the world.

Very truly yours,
George Madoo, Editor
Westinghouse Electric
Baltimore, Md.

Editor's Reply:

Amused? It was a serious article! However, permission granted.

To The Editor:

The article "Ultra-High-Speed Transistors" in July 1965 issue was cute. I have, however, the comment that when we get to the point where the problems are solved before they are coded, and the machines don't need to be designed, built, and debugged, then we engineers are likely to be drawing negative salaries!

Dan M. Bowers,
Contributing Editor

Editor's Reply:

To prepare for such an eventuality, we recommend the book, "The Power of Positive Thinking."

NEW ISSUE July 26, 1965

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Common Stock
(Without Par Value)

Price: $6.25 Per Share

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80 Federal Street, Suite 1410
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DATA COMMUNICATIONS

equipment for on-line, real-time processing

how modular can you get?

Teletype machines are modular by design, as are all the special purpose control and operating functions. As a result, Teletype equipment provides many more opportunities for you to improve on your capability to communicate data. This is also why Teletype sets are the best equipped to prepare data for transmission, as well as transmitting and receiving it.

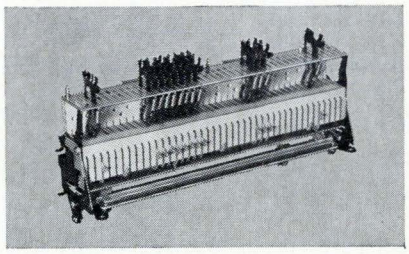
FRICTION OR SPROCKET FEED?

Teletype sets can be equipped with either a friction feed platen that prints on single or multiple copy paper, or a sprocket feed platen that positions multi-copy business forms for printing. Projecting pins engage perforations in the business form to provide for continuous, accurate multi-copy alignment.

Also, horizontal and vertical tabulators can be provided on Teletype Model 35 equipment to speed typing and improve efficiency. Teletype sets can be equipped with a form-out feature that with one key stroke will advance a business form, bringing the next one to the starting position.

NON-PRINTING FUNCTIONS

The stunt box can control many non-printing functions that add to the versatility of Teletype sets. Among these functions are carriage return and line feed, plus the ability to activate other apparatus including paper tape punches, paper tape readers, and business machines.



STUNT BOX

OTHER CONTROL FUNCTIONS

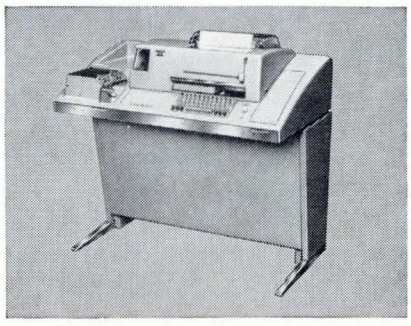
Control circuits for operating auxiliary input and output devices can be utilized, such as on the Teletype Model 35 ACS (Automated Communications Set). This is basically an automatic send-receive set with an additional tape reader for internal programing capabilities.

The auxiliary devices include: push button addresser that automatically calls in a preselected remote receiver, a push button generator that automatically types in repetitive stored data to further simplify the filling-out of business forms, and an auxiliary page printer and tape punch.

ADDITIONAL TIMESAVERS

To further aid the operator in preparing business forms, Teletype machines are equipped with a copy-holder to hold papers for easy, convenient reading and handling. Also, there is a form supply box for storing unused and completed business forms.

We have indicated only a few of the features that are or can be incorporated into Teletype sets. This versatility is one of the reasons why they are made for the Bell System and others who require dependable communications at the lowest possible cost. The new Model 35 ACS is described in an 8-page brochure, which you can obtain by writing: Teletype Corporation, Dept. 71 J, 5555 Touhy Avenue, Skokie, Illinois 60078.



MODEL 35 AUTOMATED COMMUNICATIONS SET

machines that make data move

TELETYPE®

CIRCLE NO. 5 ON INQUIRY CARD

from our man in Washington

Funds have been requested by the National Bureau of Standards to establish a central and major Government resource in the ADP field. NBS would provide the technical base for standardization in the computer field. They would develop new applications for the computer and improve its efficiency in performing older tasks.

Dr. Allen V. Austin, Director, National Bureau of Standards, believes here is "an opportunity to return to the taxpayer, in the form of increased Government efficiency and effectiveness, many times the money invested."

.....

A proposal to permit Federal savings and loan associations to establish electronic data processing facilities has been issued by the Federal Home Loan Bank Board.

The proposal would authorize any Federal association to (1) establish and maintain a special office solely for the purpose of providing EDP services for itself and (2) participate with one or more insured associations in providing EDP services primarily for those associations.

.....

The White House has under study a proposal to send a high level U.S. delegation to Moscow to explore the liberalization of trade. It is doubtful, however, if any relaxation would involve the present restrictions on strategic items such as electronic computers.

The U.S.S.R. and Eastern Europe, it is believed, are interested in buying advanced and specialized machinery, industrial processes, and technology from the U.S. Any relaxation in trade restriction in this area would require Congressional approval.

.....

The U.S. Civil Service Commission is proposing to lump all Government computer positions together into a single specialist series. The Government's hiring agency recently issued new tentative standards for analysts, programmers, and technicians. Agencies are being asked to comment on the proposals.

.....

An increasing number of Congressmen are complaining that the use of automatic data processing equipment by Federal agencies isn't being followed by a decrease in personnel. They say that the machines seem to create more work than they are worth.

.....

During 1963, manufacturers in the computing and related machines industry had total shipments valued at $2,045 million, an increase of 85% over 1958, according to preliminary results obtained from the 1963 Census of Manufactures.

Average employment in this industry showed an increase of 23% from 1958 but a decrease of 1% from 1962 to a total of 99 thousand employees in 1963. Value added by manufacture amounted to $1,127 million in 1963, an increase of 95% from 1958 and 10% from 1962.

Recent Defense Department Contracts .....

SPERRY RAND CORP., Sperry Gyroscope Div., Syosset, Long Island, N.Y., awarded a $7,170,000 fixed-price contract for engineering and data processing services for the Fiscal Year 1966 POLARIS technical assistance program. The Bureau of Ships is the contracting agency.

INTERNATIONAL BUSINESS MACHINES CORP., Washington, D.C., received a $1,639,304 fixed-price contract for procurement of electronic data processing equipment. Work will be done in Poughkeepsie, N.Y. The 2750th Air Base Wing, Wright-Patterson AFB, Ohio, is the contracting agency.

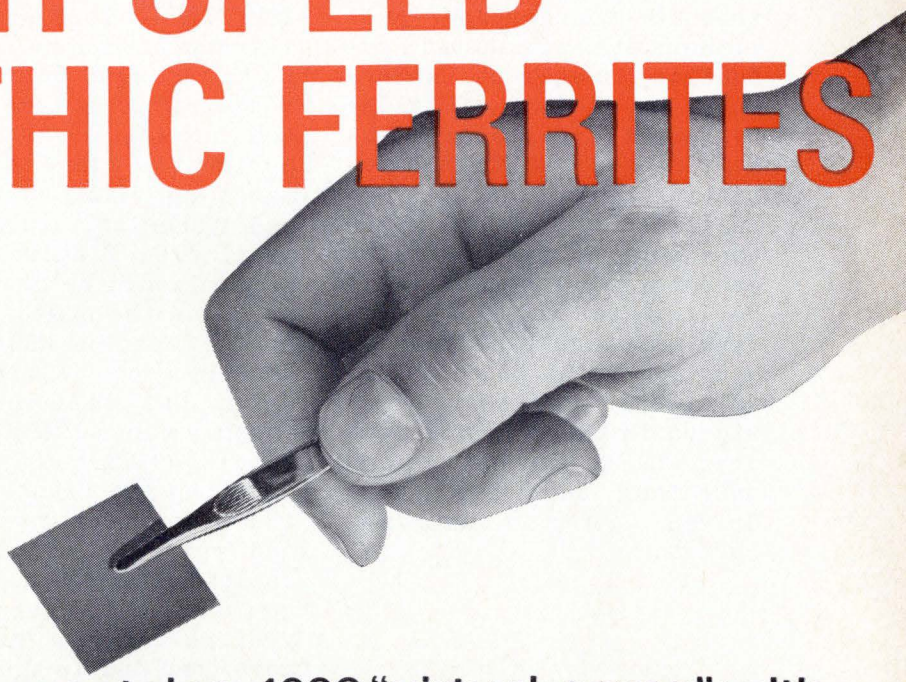
LEAR SIEGLER, INC., Grand Rapids, Mich., is receiving a $1,104,058 modification to an existing contract for bomb computer systems for Navy aircraft. The Bureau of Naval Weapons is the issuing agency.

CONTROL DATA CORP., Minneapolis, Minn., awarded a $1,122,732 fixed-price contract for one data processing set and associated equipment. Work will be done in Minneapolis. The contract is being awarded by the Bureau of Ships.

GENERAL PRECISION, INC., Librascope Group, Glendale, Cal., awarded a $1,270,000 fixed-price contract for data processing programming services. The contract is being issued by the Electronics Systems Division, L. G. Hanscom Field, Mass.

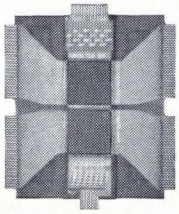
A totally new memory technology from RCA

NEW BATCH-FABRICATED HIGH-SPEED MONOLITHIC FERRITES



Each monolithic array contains 4096 "virtual cores" with an effective diameter of only 5 mils within a single, solid, sintered ferrite wafer only 1 in. by 1 in. by 0.005 in.

RCA monolithic ferrites offer all the proved advantages of ferrite technology plus:



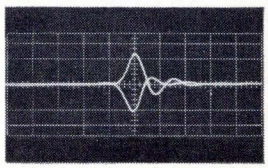
□ **Potentially much lower cost** than wired core-memory planes because RCA monolithic ferrites can be mass-produced with standard ceramic processing techniques.

□ **High-density packaging.** Type MF 2100 unit, as shown, is complete with two monolithic memory wafers, and an integral diode matrix assembly. It requires only 3.75" x 4.5" for a memory capacity of 4096 bits in two -"core"- per bit linear-select operation.

□ **Very high speed.** Full cycle time (read, delay, write), as low as 0.2 usec for 64 x 64 array.

□ **Low drive current requirement.** Less than present small-core memories: only 400 ma read, 120 ma write for 45 mv output and 35 nsec switching time.

□ **High output voltage.** Equal to conventional cores. Trace indicates over 50 mv each for differential 1 and 0 output. Compare this with other bulk-fabricated systems having output voltages of only 1 or 2 mv.



. . . . . and no stringing

TYPICAL PERFORMANCE IN 64 x 64 ARRAYS								
READ CURRENT			WRITE CURRENT		DIGITS		TYPICAL OUTPUTS	T_s
I ma	T_d (50%) ns	T_r T_f ns	I ma	T_d (50%) ns	I ma	T_d (50%) ns	1 & 0 mv	nsec
400	110	45	100	120	30	200	35	60
400	80	30	120	100	30	200	45	35
400	60	30	150	30	30	100	30	35

Available now in developmental 4096-bit arrays for testing and evaluation. Call your local RCA Sales Office or write today for information to: RCA Electronic Components & Devices, Memory Products Operation, 64 "A" Street, Needham Heights, Mass. (617) HI 4-7200.

See RCA Monolithic Ferrites in operation at FJCC — Booth #202-203

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CIRCLE NO. 6 ON INQUIRY CARD

INDUSTRY NEWS

A LOW-COST TYPESETTING SYSTEM WHICH USES AN INTEGRATED CIRCUIT COMPUTER TO PRODUCE 12,000 LINES AN HOUR was introduced to newspaper publishers at their annual Production Management Conference in Chicago. Digital Equipment Corp.'s new system, called the PDP-8 Typesetting System, accepts unjustified and unhyphenated tape punched by perforator operators; justifies according to column width, type size and font; hypenates according to rules and an exception dictionary stored in the computer memory; and generates a clean operating tape for tape-driven linecasting machines.

THE COMPLETION OF THE LAST PHASE OF ESTABLISHING A FULLY-AUTOMATED INTEGRATED CIRCUIT TESTING CAPABILITY was announced by Associated Testing Laboratories, Inc., of Wayne, N. J. This facility is capable of automatically presenting 800 to 1000 individual measurements per day in the form of punched card outputs on a wide variety of flat packaged type integrated circuit modules. Measurements such as base current, output voltage, leakage current, Hfe, all input measurements and sustainer voltage measurements can be performed. In addition new improved techniques are available for performing automatic dc and small signal parameter measurements up to 30 amps on transistors and diodes.

A TASK FORCE HAS RECOMMENDED THE DOUBLING OF THE U. S. DEPARTMENT OF AGRICULTURE'S LIBRARY THROUGH THE USE OF COMPUTERS. Task Force ABLE (Agriculture Biological Literature Exploration) suggested an automated system that would enable the Department's library to make more published scientific and technical information available. Electronic computers would be used in increasing the number of references in the USDA Bibliography of Agriculture, which has been published monthly since 1945. The task force estimates that by adopting the first stage of the system for the storage and retrieval of bibliography information, $52,000 could be saved over a three-year period and they could more than double the present 120,000 citations. In addition, the report presents a complete system of automation for many of the library's clerical functions.

INSTALLATION OF A UNIVAC 1050 CARD SYSTEM HAS BEEN ANNOUNCED BY CAMBRIDGE THERMIONIC CORP., of Cambridge, Mass. Acquisition of the new computer is said to enable the company to better facilitate its "Dial-A-Part" 24-hour a day shipping service and maintain continuous inventory and production control. In addition, the new computer will assist in keeping distributors and representatives constantly abreast with up-to-the-minute marketing data and sales analyses.

SALES OFFICES

BOSTON

Lindsay H. Caldwell
Professional Bldg.
Baker Ave.
W. Concord, Mass.
phone: (617) 369-6660

CHICAGO

Phil Holmes
410 N. Michigan Avenue
Chicago 11, Illinois
phone: (312) 467-6240

DETROIT

Robert T. Barrett
424 Lafayette Building
Detroit 26, Michigan
phone: (313) WO 1-0278

LOS ANGELES

David Barton
672 So. Lafayette Park Pl.
Los Angeles 57, California
phone: (213) 382-1121

NEW YORK

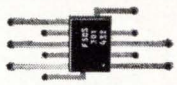
Robert J. Bandini
1 Rockefeller Center
New York 20, N. Y.
phone: (212) CI 6-4712

LONG ISLAND — SO. CONN.

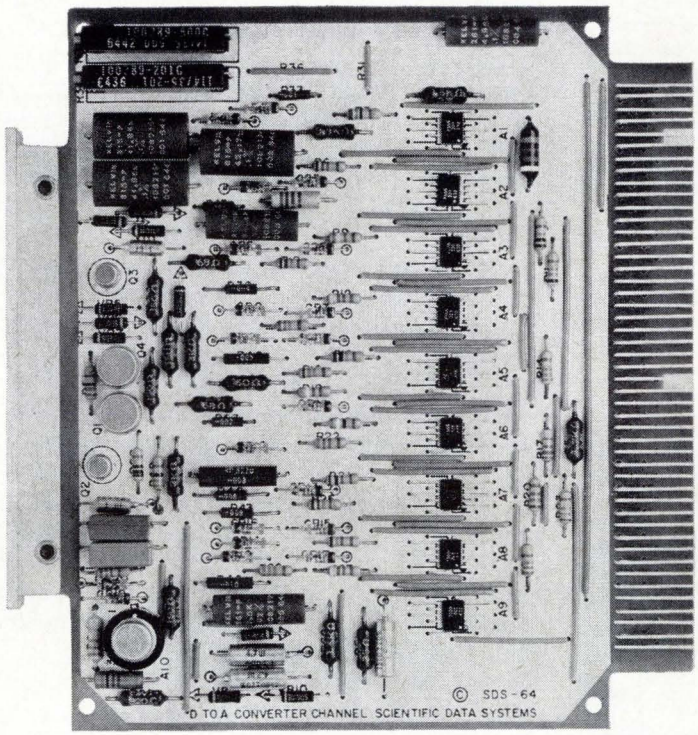
C. Lynn Coy
Robert C. Woodies
155 E. 50th St.
N.Y., N.Y. 10022
phone: (212) 751-2960

SAN FRANCISCO

David Barton
672 So. Lafayette Park Pl.
Los Angeles 57, California
phone: (213) 382-1121



Get this Assembly Register Free



with this $395 D to A Converter

With an SDS D to A Converter, you get two registers per channel: A holding register like everybody else and an assembly register like only us. So what? So now, in addition to sequential conversion, you can simultaneously convert all of your system channels on demand. And it doesn't cost a penny more.

About the register shown above: You're right. It is an integrated circuit. All of our new analog system components utilize them to cram more reliability into less space. They also allow new systems set up flexibility (our 9-bit D to A, for example, is fully contained on a single card).

So add up our D to A converter advantages: both assembly and holding registers; integrated circuits; 5 microsecond speeds; 200 Kc conversion rates; 9, 12 and 15-bit models; off-the-shelf delivery of individual channels or complete multi-channel systems. You'd get more for your money even if our prices weren't so low.

May we send you a brand new brochure on our complete digital and analog component line?

SDS SCIENTIFIC DATA SYSTEMS
1649 Seventeenth Street, Santa Monica, Calif.

Sales offices in: Santa Monica, New York City, Boston, Washington, D.C., Philadelphia, Pittsburgh, Wilmington, Houston, Huntsville, Orlando, Dallas, Chicago, Detroit, Albuquerque, Denver, San Francisco, San Diego, Seattle. Foreign representatives: CECIS, Paris, France, Geneva, Switzerland; Kanematsu, Tokyo, Japan; RACAL, Sydney, Australia; Instronics, Ltd., Stittsville, Ontario, Canada.

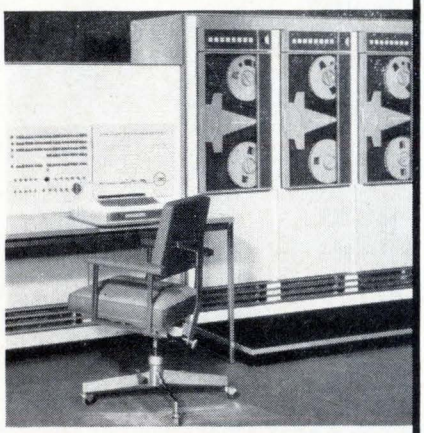
CIRCLE NO. 7 ON INQUIRY CARD

what secret ingredient makes EDP profitable?

EDP system components that do the job **better** for **less money.** That's what. And designers, builders and users bent on cutting the traditionally high cost of computing are specifying that kind of EDP system components. For instance, they specify computer magnetic tape units from Datamec. Either the **D 2020** or the **D 3030.** Both set new standards for the industry in all-around economy: lower initial cost, reduced maintenance expense, greater up-time, higher performance reliability.

The **D 2020** is an attractively-priced unit for computer and off-line applications where moderate speed performance is highly practical (data transfer rates up to 36,000 characters per second).

The **D 3030** offers the same unprecedented **economy** and **reliability** for heavy duty, on-line use with digital computers and other digital EDP systems requiring higher data transfer rates (up to 60,000 characters per second).



Some 80 leading manufacturers already specify Datamec computer magnetic tape units in their data systems. Want to take a look at the list of people who've discovered that "secret ingredient"? Write Tom Tracy at Datamec, 345 Middlefield Road, Mountain View, California.

DATAMEC®
A DIVISION OF HEWLETT-PACKARD
leadership in low-cost/high-reliability digital magnetic tape handling

CIRCLE NO. 8 ON INQUIRY CARD

INDUSTRY NEWS

THE NIPPON ELECTRIC CO., OF JAPAN HAS INTRODUCED ITS DESK-SIZE COMPUTER, THE NEAC-1210, THAT EMPLOYS THE JAPANESE INVENTED PARAMETRONS IN PLACE OF TRANSISTORS FOR ITS LOGIC ELEMENT. The Parametron is a magnetic-electronic logic device invented by the Japanese physicist, Dr. Gotoh. It consists of a ferrite core and a capacitor. This resonant circuit, activated by the external input, oscillates in two-phase modes: "Zero Phase" and "Pi Phase", which correspond to the "1" and "0" of the logic circuits. Thus, the two different states are represented by the different phases of oscillating frequencies. The uniqueness of the Parametron circuit is that it uses majority decision logic. A revised version of the NEAC-1210 will be designed for the American business market and should be available for marketing in the United States early in 1966. Presented for the first time in the USA at the Nippon Electric Company's exhibit at the New York World's Fair, the NEAC-1210 was designed especially for business applications which require high-speed computation combined with descriptive information.

A LABORATORY INSTRUMENT COMPUTER (LINC) RECENTLY CONDUCTED SIMULATED BIOMEDICAL LABORATORY DEMONSTRATIONS at the Federation of American Societies for Experimental Biology Meeting in Atlantic City, N.J. The computer, exhibited by Digital Equipment Corp., used special programs to demonstrate the averaging of physiological signals and plotting of histograms and ECG data. The LINC is designed specifically for biomedical research. Its capabilities, according to DEC, can be brought to bear on virtually any laboratory problem for which the researcher can prepare a program, or set up logical steps corresponding to the experimental procedure of analysis. In the lab, the LINC can generate stimuli, control stimuli/response relationships, and display responses for on-line monitoring. Experiments can be modified by the computer as they are performed. LINC stores data for future reference and displays stored data selectively before or after statistical analysis. The computer also calculates distributions, correlations, histograms, and performs Fourier analysis.

CERTAIN ASSETS OF THE BUSINESS COMPUTER OPERATION OF GENERAL PRECISION INC'S LIBRASCOPE GROUP were acquired by Control Data Corp., in exchange for an undisclosed number of shares of CDC common stock. General Precision is concentrating its activities wholly on the development, manufacture, and sales of computers to the military, space and special-application markets. General Precision will also continue to make and sell its line of drum and disk memories. Involved in the purchase are General Precision's existing business computer rental and service contracts, inventory of business computers, and business computer sales and service organization. Among these computers are over 400 LGP-21, LGP-30 and RPC-4000 computers. Control Data intends to serve past and future customers for these systems.

now! anyone can afford a new "off-line" tape converter

(so why waste the time and cost of using a computer?)

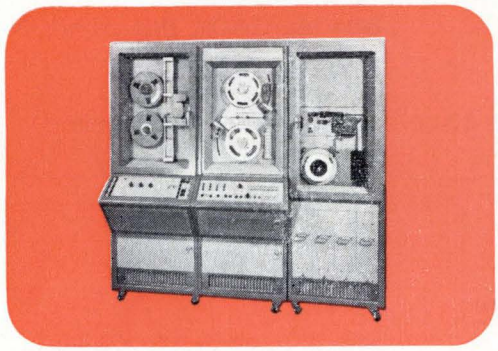
Free your computer. Convert or duplicate magnetic and paper tapes and punched cards faster and more economically, "off line," with one of these new high-speed Versa-Verter* tape converters. Select the bi-directional versatility of the SC-332A unit or the uni-directional economy of a new B, C or D model. Each has a universal code converter with programmable plug board and a standard density magnetic tape transport. Ideal for data translation needs for numerically controlled machine tools, invoice and inventory data control, and business machine tape conversions. Select the one designed for your requirements and write or call for information. Phone (716) 342-8000 or write: Product Mgr., Data Equipment, General Dynamics|Electronics, 1400 N. Goodman St., Rochester, N. Y.

*Trademark applied for

shop here

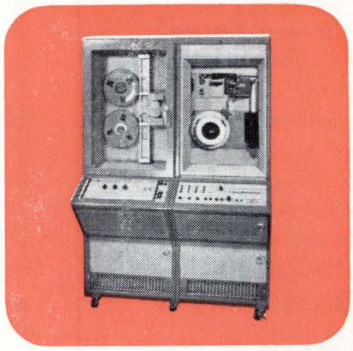
SC-332A VERSA-VERTER
MAGNETIC to PAPER TAPE / PAPER to MAGNETIC TAPE / PAPER to PAPER TAPE

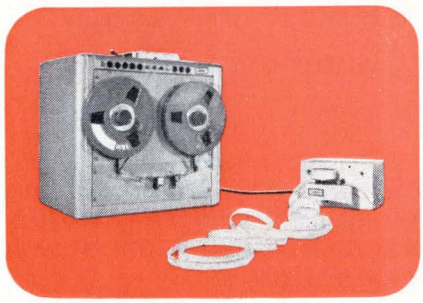
Features up to a 2,048-character buffer, 1000-char/sec. PT reader, 300-char/sec. punch. Operates with standard 5, 6, 7 or 8 level paper tape. Post-punch verification also available.



SC-332C VERSA-VERTER
MAGNETIC to PAPER TAPE

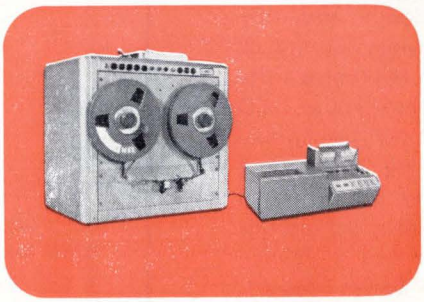
A uni-directional unit with up to 2,048-char. buffer and a 300-char/sec. PT punch that operates with either 5-level $^{11}/_{16}$" tape or 6, 7 and 8 level 1" paper tape. Post-punch verification available.





SC-332B VERSA-VERTER
PAPER to MAGNETIC TAPE

A uni-directional unit with a 100-char/sec. PT reader that operates with standard 5, 6, 7 or 8 level paper tape.



SC-332D VERSA-VERTER
PUNCHED CARD to MAGNETIC TAPE

A uni-directional unit with a 100-card/min. reader that accepts standard 80-column punched cards.

GENERAL DYNAMICS | ELECTRONICS
ROCHESTER, NEW YORK

CIRCLE NO. 9 ON INQUIRY CARD

What do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

Logic Symbols Standard

Considerable interest has been shown in the subject of logic symbology since the lack of standardization was deplored by Harry D. Young in a letter to editor printed in the May 1965 issue of COMPUTER DESIGN.

CD agrees that a universal standard is necessary and desirable for our dynamic industry. CD also agrees that technical journals should pioneer in the use of such a standard if progress toward general acceptance is to be made. As a major medium of communications for the computer industry, CD accepts the responsibility of leading this pioneering effort.

However, the route of the pioneer is never smooth and any available map is always worthy of consideration. To maximize the probability that the route CD chooses is the best for our industry, not only for today but for the future, CD will defer choosing the standard which it will advocate until all readers have had a chance to be heard. This Forum department (which is also intended for the discussion of other worthy topics) will give all viewpoints a fair hearing and then recommend a standard for use in and advocacy by CD.

Let Us Have Your Opinions!

WHERE TO OBTAIN COPIES OF PROPOSED STANDARDS . . .

IEEE STANDARD (ASA Y32.14) — No. 91

Order From:

IEEE ORDER DEPT.
BOX A, LENOX HILL STATION
N.Y., N.Y. 10021

PRICE: $3.00/copy ($1.00 for IEEE members)

MIL-STD-806B

Write To:

STANDARDIZATION DIVISION
DEFENSE SUPPLY AGENCY
WASHINGTON 25, D.C.

NOTE: *Extracts from the IEEE Standard were printed in the May 1965 issue of COMPUTER DESIGN. MIL-STD-806B symbols were given and discussed in the July 1964 issue of COMPUTER DESIGN.*

TWO VOTES FOR MIL-STD-806B

"I would like to add my vote to that of Mr. Young in regard to logic symbology. Although there are two systems in the ASA proposal, we at Union Switch and Signal have adopted the MIL-STD-806B version for three reasons:

1. Personnel with military experi-

CIRCLE NO. 10 ON INQUIRY CARD

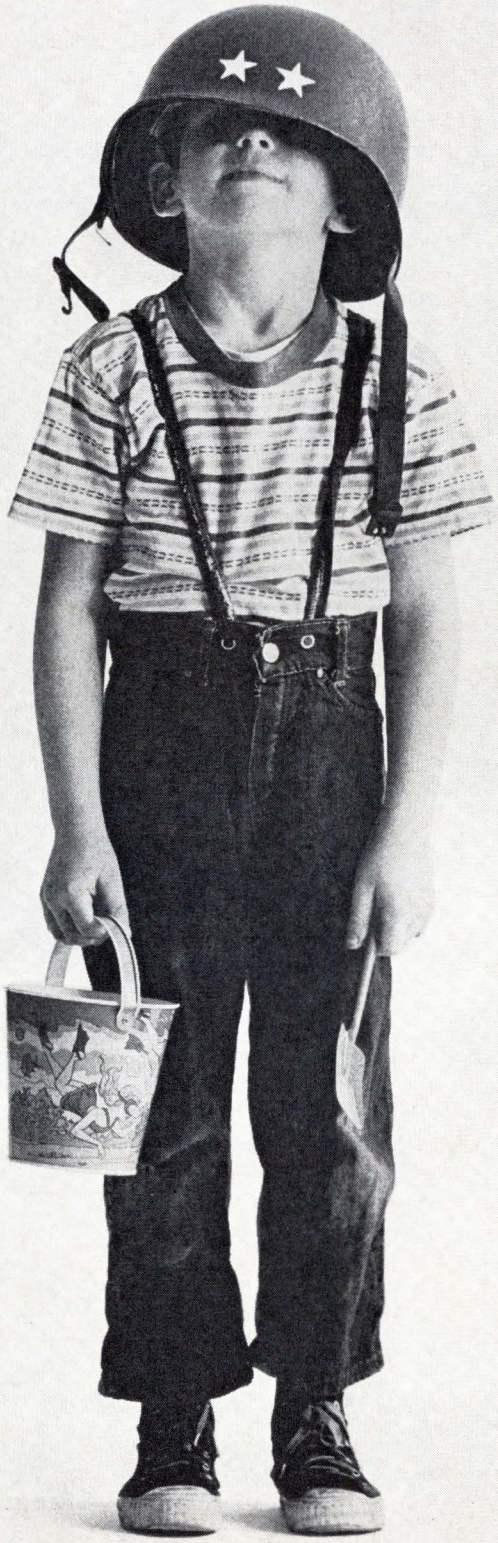
If we don't show our age it's because our ideas keep us looking young. Like the one we patented back in 1948 for the first ferrite memory core. It actually gave the memory business its start. Now, many large computer manufacturers use our patents. Yet, we're still making more of these cores than any of them. Ten million a week. Every one of them fully tested. All at a good price.

We're known for other ideas, too. Like the Microstack,® the first miniaturized and ruggedized memory module. And for our basic research with core materials, multi-aperture devices, and circuitry.

While it's true we're the old man of the memory business, you'll find that Indiana General is still young at the core. Look to us for new ideas backed by experience. The kind you can use. Experience that's yours for the asking. It's all in our technical literature packet on memory products. Write the Indiana General Corporation, Electronics Division/Memory Products, Keasbey, New Jersey.

INDIANA GENERAL

Indiana General. The old man of the memory business.



DIGITAL SYSTEM DESIGNERS

Newly Formed Dept.
of a
Prominent East Coast
Mfr. of EDP Equipment
has

IMMEDIATE

Staffing Requirements
for
Creative & Versatile
Digital Systems Designers

Creative Accomplishment in

- **System Design**
- **Logic Design**
- **Digital Circuitry**
- **Programming**

Multiple Skills Desirable

Excellent Starting Salary
Paid Relocation Expenses
with many Company Paid
Benefits

Send Resume
in Complete Confidence to:

Computer Design

Dept. A

West Concord, Mass. 01781

An Equal Opportunity Employer

CD Readers' Forum (Continued)

ence will find them most familiar.

2. When we do military contract work we will not have to change our standards.

3. The unique shapes for AND and OR circuits are easier to locate on a logic diagram, making the diagram easier to read.

Also, along with Mr. Young, I would like to see COMPUTER DESIGN and other technical publications lead the way to adoption of a uniform standard."

William H. Moore
Engineering Supervisor, Digital Systems
Union Switch and Signal
Westinghouse Air Brake Co.,
Pittsburgh, Pa.

"I read with some interest the Editor's Reply to Mr. H. Young's letter regarding the lack of adherence to approved logic standards by technical publications. The real fault lies with the original technical writers who in many cases feel it is below their professional dignity to follow an approved standard, and must therefore provide innovation, and frequently from one article to the next. Accordingly, it is relatively expensive for a publisher to convert such drawings into an approved symbol system, and also at the risk of introducing errors in the logic.

In this connection, and because I was instrumental in promulgating the MIL-STD-806B and later the ASA (DOUBLE) Standard for Logic Symbols, I have since made the following observations as to trends in logic symbols:

(a) The more advanced manufacturers of integrated solid-state circuits appear to have accepted the "truly symbolic" symbols of the -806B- (as note their one- and two-page ads).

(b) Electronics companies which have adopted the -806B logic symbols for company-wide use realize cost savings.

It has been found that -806B logic drawings pass easily and without change in symbology through the evolutionary cycle starting in engineering and through drafting, production, text, and technical/maintenance manual publication for the field.

In this regard it is a fact that before the military services committed themselves jointly to the MIL-STD-806B, a thorough and practical study was performed by the Air Force whereby the logic symbols of the -806B proved themselves superior in usage, particularly at the level of activity where many people are involved and their time is costly — equipment maintenance. Please find one copy of the A.F. study for your reference and possible further use."

Wm. J. Smith
Arlington, Mass.

EITHER-OR VOTE

"Regarding the letter to the editor in the May 1965 issue, MIL-806 and IEEE are not equivalent. I hope your magazine will rise to this real challenge and get MIL-806B **or** the IEEE Standard accepted as an international civilian and military standard.

I was a correspondent to the subcommittee and consider that delays and lack of **a** standard from 1958 to 1965 are ridiculous in our profession."

R. W. Roberts, Supervisor
Division 2422,
Advanced Data Systems Dev.,
Sandia Corp., Albuquerque, N.M.

INTEGRATED CIRCUITRY

Integrated circuitry has come of age in defense and space electronic systems and will find increasing application in consumer items. Primary reasons for the growing number of uses are the inherent advantages of this technology-improved reliability, reduced-cost, and smaller size and weight. These views are expressed in an information package prepared by the Institute for Applied Technology, National Bureau of Standards. The package reviews Government R&D in circuit design and fabrication as well as applications in electronic systems. The computer field particularly has benefited much from integrated circuitry, the review discloses. Applications in other areas including telemetry and switchboards are also described in the review.

Order from Clearinghouse, U.S. Dept. of Commerce, Springfield, Va. 22151. Order No: OTR 111N. Price: 50 cents.

TRANSISTORS AND DIODES FOR MICROPOWER CIRCUITS

A number of available transistors are well suited to micropower circuits. Tests conducted on the S-4528 and S-4529 transistors show that these high quality planar devices even have the required stability for space applications. Repetition rates as high as a megacycle were obtained at low milliwatt power levels, less for some simple gating circuits. Flip-flops have been constructed which operate at several kilocycles and consume 50 to 100 microwatts. As a test of lower limits of power, a 2 kilocycle free running multivibrator was built that uses less than one microwatt. Researchers expect to reduce the size of the transistors and to improve their speed.

Order from Clearinghouse, U.S. Dept. of Commerce, Springfield, Va. 22151. Order No: N65-14458N. Price: $2.00.

MEDIUM-SPEED MASS MEMORY

Report describes that a batch fabrication technique makes use of toroids etched out of sheet permalloy to fabricate the memory elements, and all drive and sense wiring is provided by a combination of precision etching and plating processes. The resultant memory is inherently low power. Air Force researchers developed system designs which use for the most part integrated circuitry. The resulting mass memory system of 10^8 bits capacity is small, light, economical, low power, medium speed, nonvolatile, and non-destructive in readout. The major accomplishment of the researchers thus far has been successful fabrication of planes having 16 x 16 bits on 25 mil centers with reasonable and steadily improving yield. They have also been successful in fabricating 64 x 64 bit planes on 25 mil centers using mechanical pin registration.

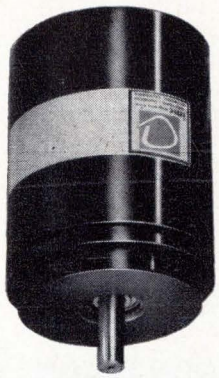
Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. AD614831N. Price: $6.00.

MICROPOWER LOGIC CIRCUITS

NASA has published a new technology utilization report on micropower logic circuits. The 15-page report, prepared by John C. Sturman of NASA's Lewis Research Center, Cleveland, is based on data developed during a continuing series of research studies of ultra-low-power circuits at Lewis.

Order from Clearinghouse for Federal Scientific and Technical Information, Springfield, Va. 22151. Order No. NASA SP-5022. Price: 75 cents.

It's new from IMC



How fast do you need a step servo motor?

1 millisecond fast; day after tomorrow fast? That's what's new from IMC—The first factory stocked broad line of step-servo motors. 18 models including a unit capable of one thousand pulse per second operation—bi-directionally. And all for day after tomorrow delivery. Sizes from 5 to 20. Running torque up to 8 oz. in. Step angles of 15 and 90 degrees. And proven capability on programs such as Polaris, Surveyor, Mariner and LEM. Included in the stock program are units designed for business machine and commercial applications.

Call your nearest IMC Engineering Representative or use the coupon for IMC's latest literature which will include our line of stock step-servo motor electronic controllers. Better still, test us with a fast order!

Check IMC also for: Precision Solenoids—factory stocked!

ENGINEERING REPRESENTATIVES FOR IMC STEP SERVO MOTORS
(Not to mention solenoids,
synchros and resolvers, DC synchro indicators)

Albuquerque: J. F. Quirk & Assoc., 256-0884
Dallas: Hillman Enterprises, Inc., LA 1-2070
Georgetown, Tex.: Hillman Enterprises, Inc., UN 3-3780
Los Altos, Calif.: Richard Strassner Co., 948-334
Portland: Shaffer & Nelson, Inc., 234-7437
Salt Lake City: Oscar Salme & Assoc., Inc., AM 2-2349
Seattle: Shaffer & Nelson, Inc., MU 2-0186
Temple: IMC Magnetics Corp., Ariz. Div., 967-7851
Chicago: Berndt & Klein Assoc., SP 5-3488
Dayton: Bek Assoc., Inc., CR 8-1343
Kansas City: Design & Sales Eng. Co., GR 1-1640
Minneapolis: D. A. Schultz Co., FE 9-7701
St. Louis: Design & Sales Eng. Co., PA 1-6403
Atlanta: Bill Henry Assoc., 255-0920
Charlotte, N. C.: Bill Henry Assoc., 375-8958
Sarasota: Bill Henry Assoc., 955-4637
Binghamton, N.Y.: Engineering Components, RA 3-4197
New Haven: Edcom, Inc., MA 4-7291
Newtonville, Mass.: Edcom, Inc., WO 9-9710
Ottawa, Ontario: M. J. Howard Co., Ltd., PA 8-2991
Philadelphia: Burgin-Kreh Assoc., Inc., OR 7-1646
Syracuse, N.Y.: Engineering Components, HE 7-8181
Towson, Md.: Burgin-Kreh Assoc., Inc., VA 5-3212
Westwood, N. J.: Clarfield-Stollmack Assoc., 666-8989

Manufactured by IMC Western Div., 6058 Walker Ave., Maywood, Calif. 90270. Tel. (213) LU 3-4785, TWX 213-773-5307.

imc **IMC Magnetics Corporation**
Marketing Division: 570 Main Street
Westbury, New York 11591. Telephone:
(516) 334-7070. TWX (516) 333-3319

☐ Send my Step Servo Motor Catalog, fast
☐ Send a Rep, faster
☐ And/or tell me about _____

Name _____

Title or dept. _____

Company _____

Address _____

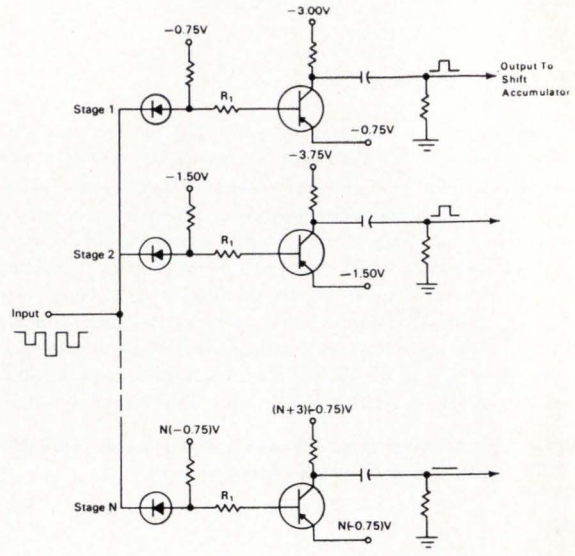
City _____ State _____ Zip Code _____

CIRCLE NO. 11 ON INQUIRY CARD

NASA TECH BRIEF

A SUMMARY OF A SPECIFIC TECHNICAL INNOVATION DERIVED FROM THE SPACE PROGRAM. ISSUED BY THE TECHNOLOGY UTILIZATION DIVISION OF NASA.

Pulse Height Analyzer Operates at High Repetition Rates, Low Power



THE PROBLEM

Providing a pulse height analyzer that operates at pulse repetition rates as high as 10 to 20 megacycles per second. Conventional pulse height analyzers employing digital feedback circuitry cannot be driven at such high pulse rates and waste power when no input pulses are applied.

THE SOLUTION

A simple multistage transistor gating circuit that compares the input pulse heights (voltages) to discrete reference voltages. The number of stages required for this circuit is determined by the range of pulse heights to be measured, and only seven components are needed for each stage.

HOW IT'S DONE

Each pulse in a train of negative pulses is admitted simultaneously to the base of the transistor in each of the stages (1 to **N**). The transistors (base and emitter of each transistor) are biased by a reference voltage so that they produce an output voltage for any pulse height less (i.e., greater in absolute value) than the particular reference level. The reference levels are established in decreasing equal increments. As shown in the circuit diagram, the reference bias voltage for the first stage is −0.75 volt; for the second stage, −1.50 volts; and for the **N**th stage, **N**(−0.75) volts. The voltage references may be chosen so that the circuit measures any desired voltage difference, the minimum difference being determined by the transistor used.

When no input pulse is applied, all the transistors are turned off, because each transistor is biased to the same extent (voltage on base equals voltage on emitter) by the regulated power supplies V1, V2, . . .V**N**. The diodes block interaction between stages, and thus prevent one stage from turning on another stage. When a negative pulse on the input terminal is less than −0.75 volt, for example, the first-stage transistor begins to conduct and an output voltage pulse appears at its collector. This pulse is then stored in the shift accumulator. As the input voltage continues to decrease to lower bias levels, succeeding stages (i.e., stage 2, 3, etc.) turn on, and their outputs are stored in the shift accumulator. The height of each pulse is read from the accumulator position that corresponds to the highest stage for that pulse.

NOTES

1. The collector voltage supplies need not be closely regulated.
2. For operation at low frequencies (less than 300 kc per sec) a single voltage supply with a resistive divider may be satisfactory for the base and emitter bias voltages. At higher frequencies, however, a separate regulated supply will be needed for each of these voltages.
3. The operating speed of the analyzer can be increased by shunting each resistor R_1 with a capacitor.
4. Inquiries concerning this innovation may be directed to: Technology Utilization Officer, Western Operations Office, 150 Pico Boulevard, Santa Monica, California, 90406. Reference: B65-10041.

PATENT STATUS

NASA encourages commercial use of this innovation. No patent action is contemplated. **END**

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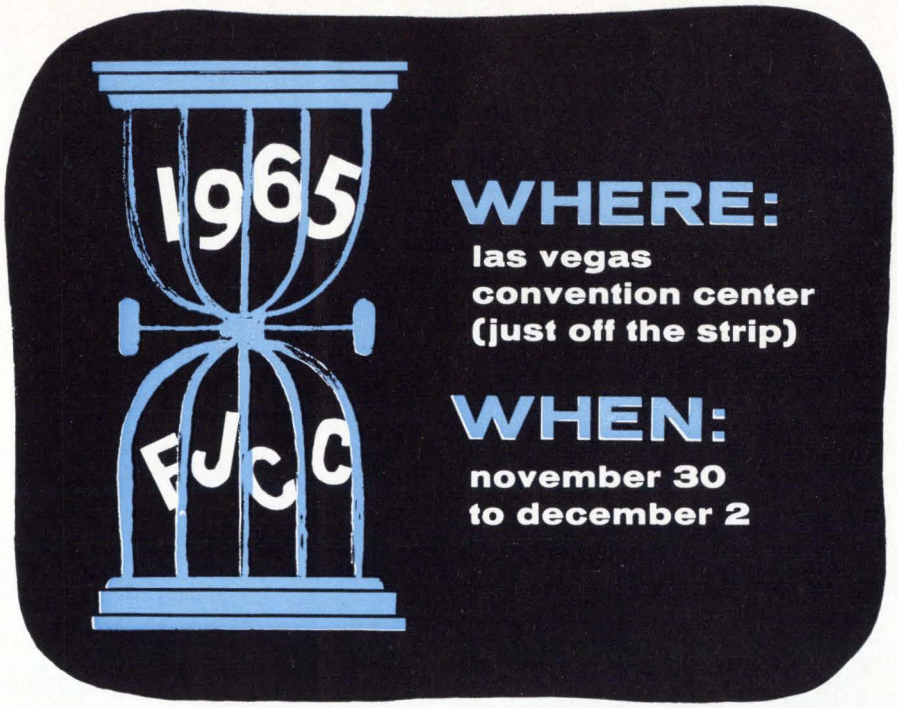
Discuss-Only Sessions at the Coming 1965 Fall Joint Computer Conference

The 1965 FJCC will include 5 "discuss-only" technical sessions — a format used successfully at a recent IEEE Computer Group Conference on the "Impact of Batch-Fabrication on Future Computers." These sessions are designed to provide pre-prints of papers to registrants one month prior to the conference; eliminating the formal presentation of papers during the conference; and devoting the session time primarily to discussion between authors and attendees. It must be emphasized that for the "discuss-only" sessions to succeed, pre-prints of papers must be obtained in advance to permit a critical study and preparation by the attendees. Each participant will benefit from such sessions in proportions directly related to the advance preparation.

The conference on the "Impact of Batch-Fabrication" seemed to be a significant success from both the technical and experimental standpoints. Several people have commented that this was the first conference they had attended in years in which they had sat through and participated in the technical sessions, rather than wandering around the halls and lobbies talking to old cronies. The more pertinent consensus of opinion was that this conference format is a must for special conferences such as the Batch-Fabrication ("the only way to run a conference"). Although the majority felt that it could be applied to a large conference like the FJCC, some experimentation on a smaller scale would be more appropriate. The Program Committee for the 1965 FJCC has decided to commence such an experiment with five technical sessions, covering the areas of Scratchpad Memories; Read-Only Memories; Memories for Future Computers; On-Line Interactive Software Systems; and Time-Shared Computer Systems. In the hardware area the field of memories has been chosen by the Program Committee as a suitable technical arena in which to utilize this approach of conference dialogue for a larger conference such as the FJCC. Its success may permit extension to cover more sessions in future AFIPS and other national conferences.



Pre-prints of all 5 sessions' 24 papers, contained in a single paper-bound volume, will be available about October 21, 1965. This will give participants about a month to study the papers. To obtain a copy of the pre-print, use the order coupon. →

Two types of "discuss-only" session formats will be employed. One type will permit each author about 5 minutes to up-date the pre-print material. A discussion then follows between attendees, authors, and other panelists, specialists in fields of endeavor not covered by papers presented in the proceedings. The second type will employ direct author-attendee exchange of information and ideas. All sessions will permit introduction of new material by both authors and attendees.

In addition to the papers of the three memory sessions described in detail here, the pre-print volume will contain 5 papers for the session entitled, "*On-Line Interactive Software Systems*" and 4 papers for the session "*Time-Shared Computer Systems: Software/Hardware Considerations.*"

procedure for participating in discuss-only sessions

To take part in the discussions on any of the papers scheduled for the discuss-only format, you should order the pre-prints prior to Oct. 21, 1965. The mailing of the papers will commence on that date giving you approximately a month's time to study those papers in which you are interested. The complete papers for all 5 discuss-only sessions will be contained in a single paper-bound volume. The cost of this pre-print volume is $5.00; however, upon presentation of such payment receipt (which you will receive with the volume) at the conference in Las Vegas, you will be charged with only a $5.00 registration fee. Otherwise, the conference registration fee is $10.00.

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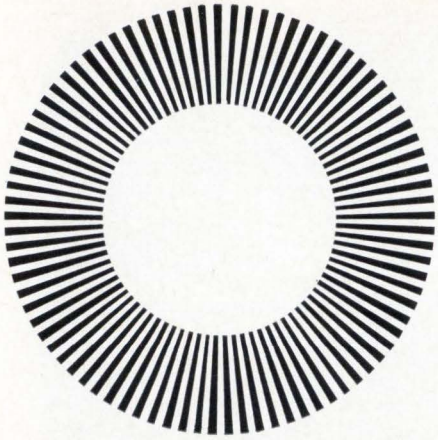

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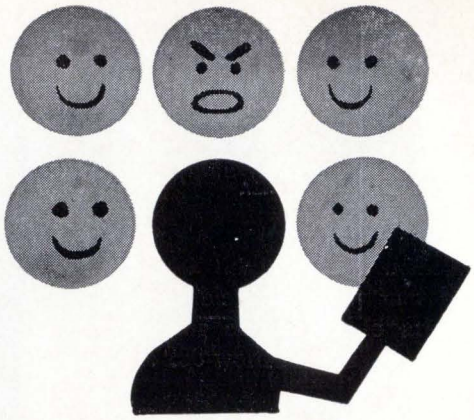
REVIEWS OF DISCUSS-ONLY PAPERS



"Scratchpad Memories" Session

Gordon S. Mitchell of the National Security Agency, Fort Meade, Md., has organized and will chair this discuss-only session on scratchpad memories. Three different storage techniques are described in three of the papers, and the applications of scratchpad memories in two different computer systems are discussed in the other two papers. Here are reviews of four of these papers; the fifth paper, "*Design Considerations for a 25 Nsec. Tunnel Diode Memory*" is presented in its complete form on the pages following these reviews.

"An Experimental 65 Nsec Thin Film Scratchpad Memory System"

G. J. AMMON and C. NEITZERT
RCA, Computer Advanced Product Research, Camden, New Jersey

A 256-word by 25-bit magnetic thin film memory system is described. A partially populated model of 8 words by 6 bits has been operated with a cycle time of 65 nsec and an access time of 30 nsec. Memory storage array is a continuous sheet of magnetic film composed of a nickel-iron-cobalt alloy on an aluminum substrate. Word currents of 500 ma with 9 nsec rise time, and digit currents of 200 ma produce a minimum sense signal of 2 millivolts. The sense amplifier contains 3 capacitively-coupled differential gain stages. The sense amplifier output, after a delay of 5.6 nsec, is 1 volt with a 4 nsec rise time. Basic memory logic circuit is a two-level AND/OR gate consisting of an emitter follower driving a current steering circuit. Information disturb (creep) tests were run with 25-million disturb cycles. Tests indicated that every other word line had to be short-circuited to eliminate large numbers of disturbed bit locations. Assuming circuit speeds can be improved, a memory cycle time of 60 nsecs is predicted. This paper clearly demonstrates the feasibility of thin film memory systems operating in the less than one hundred nsec cycle time range.

During the discuss-only session, the authors should present more data on the bit disturb problems associated with this thin film memory and, if possible, how they can be minimized or eliminated to attain a full size 256-word memory.

SMID — A New Memory Element

R. P. SHIVELY
Litton Systems, Inc.
Guidance and Control Systems Div.,
Woodland Hills, Cal.

A PNPN device is utilized as the basic element in an integrated circuit latch. Because of its simplicity and low power requirements, nine SMID storage elements can be placed on a 40-mil square semiconductor chip. The name SMID is derived from Semiconductor Memory Integrated Device. A read cycle time of 100 nsec over a temperature range of −55C to 125C and a power consumption of 0.55 milliwatts per bit is claimed for the device. A detailed description of a SMID memory array under the control of word and digit drivers is presented by the author. The word and digit drivers have been designed and fabricated in integrated circuit form. They are capable of driving a SMID memory of 512 words (40 bits per word). The sense switch is obtained by remetallizing a standard DTL gate. The memory logic circuits are implemented with standard integrated TTL gates.

The author states that a 64-word, 21 bits per word, SMID memory system has been constructed and is now in the test phase. The total memory system utilizes 194 fourteen-lead flat packs. The inclusion of system block and timing diagrams would lend credence to the stated memory cycle time of 100 nsec. Improved interconnection techniques and a package with more than fourteen leads may enable this 1344-bit memory to be contained on a circuit board as small as 3 square inches.

The results obtained from testing the 64-word memory should be available when the discuss-only session is held and may provide an interesting base for discussion.

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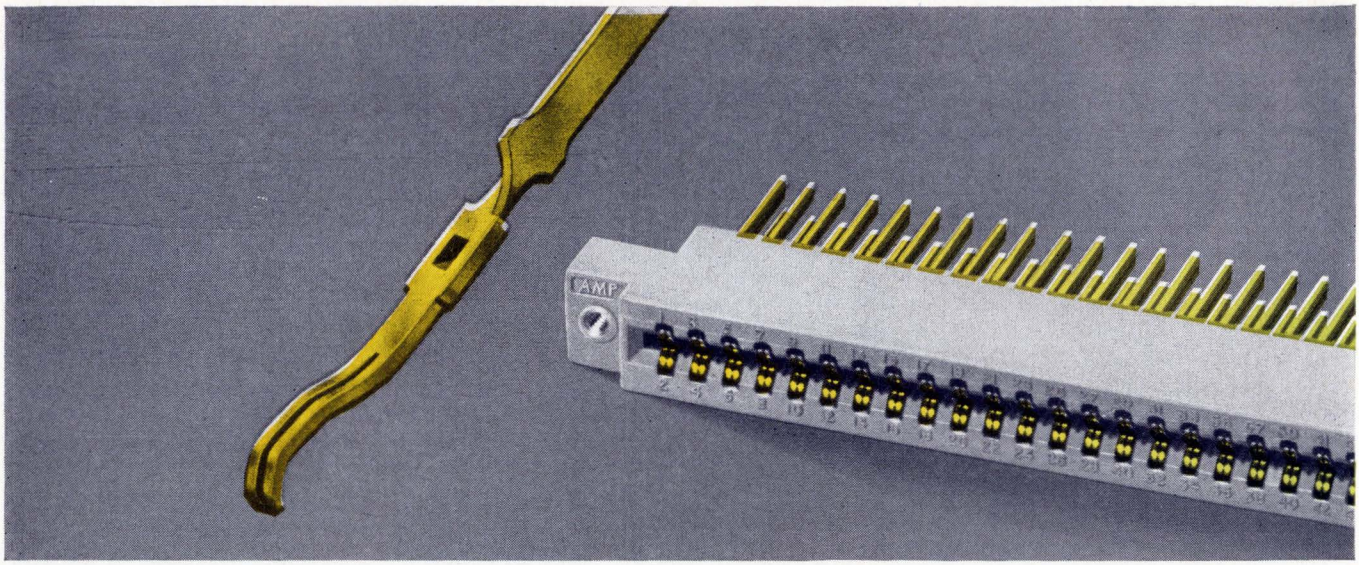

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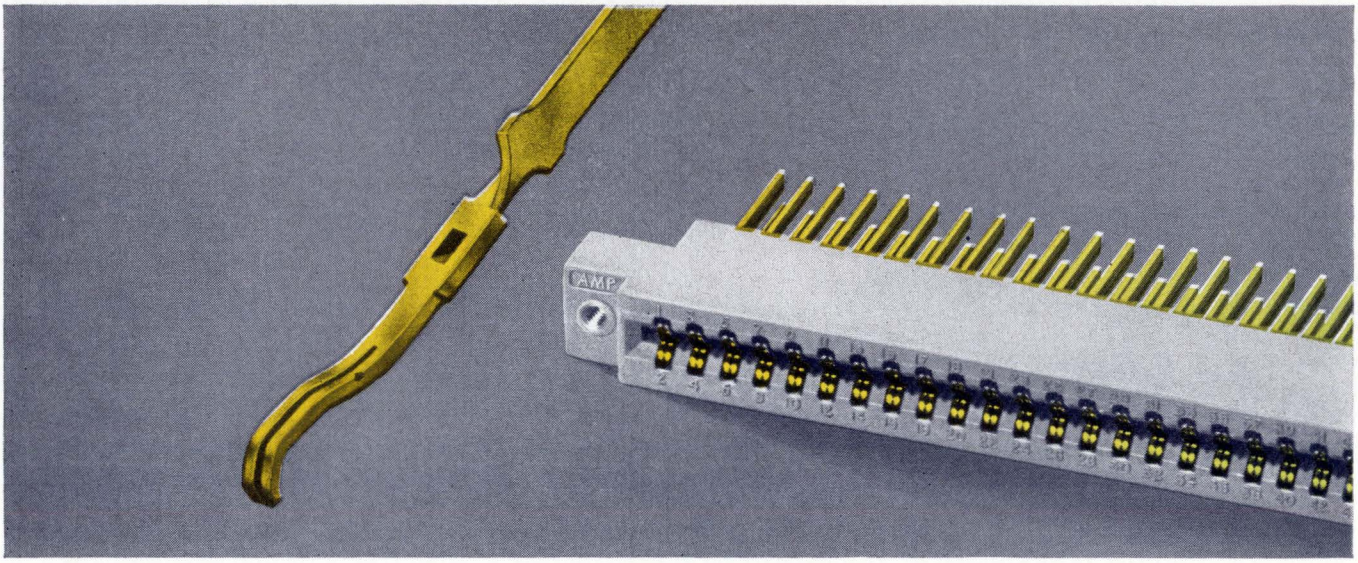

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REVIEWS OF DISCUSS-ONLY PAPERS

(CONTINUED)

Scratchpad-Oriented Designs In The RCA SPECTRA 70

A. T. LING
RCA, Electronic Data Processing,
Camden, New Jersey

A 300 nsec cycle magnetic core scratchpad (128 words, 32 bits each) was chosen for the SPECTRA-70 models 45 and 55. The large number of registers required in these machines makes it more economical to use a ferrite core scratchpad rather than a flip-flop implementation. Continued cost reduction of integrated circuits in the future may change the economic factors dictating this choice.

The scratchpad memory with a processing matrix in its data circulation path, plus two separate hardware utility registers, comprise the basic data flow and processing entities of the central processor. This provides simplicity while retaining flexibility of function. An example of the flexibility is the reduced overhead for interrupt processing. Since all program status is already stored in registers for other than the interrupt states, separate status-saving actions are unnecessary. However, using a single scratchpad leads to a processing speed bottleneck since only one read or write can be done in any one cycle.

The author clearly points out that scratchpads are not a panacea, but are suitable for a certain performance and cost range. Small machines cannot afford to use them, and very high performance machines require greater concurrency of action.

During the discuss-only session, the author should be prepared to answer questions regarding his conclusions on a ferrite core scratchpad vs. a flip-flop scratchpad with respect to cost.

SCRATCHPAD MEMORIES AT HONEYWELL: Past, Present, and Future

NORMAN NISENOFF
Honeywell, EDP,
Wellesley Hills, Mass.

Honeywell introduced the use of a scratchpad memory in 1958 in the design of the H-800. Their machines have continued to use scratchpad memories through the various models of the series 200, to the current design, the H-8200. In these designs a scratchpad provides manipulative storage for "overhead" processes, fast access to selected portion of main memory, and storage for temporary status or intermediate results. The H-800 and H-8200 allow for several (up to 8 and 10, respectively) processor equivalents (control groups), interleaving with the same main memory. Each control group is a set of locations in the scratchpad memory separate from any other control group.

In deciding on the method of implementation for a scratchpad, one must consider trade-offs among speed, capacity, and cost-per-bit. The author presents a simple cost analysis for evaluating the trade-offs between scratchpad media, considering their peripheral support (drivers, decoders, etc.). However, the author does not treat the influence of technical feasibility factors which may be extremely important in the higher speed ranges, or the effect on the rest of the machine design of the choice of a particular scratchpad implementation.

Extrapolation from the characteristics of 208 computers over more than 10 years suggests that main memory cycle time of approximately 300 nsec will be normal in 1970. Scratchpad cycle time in the range of 40 to 75 nsec will be needed. Whatever its speed, scratchpads are expected to be used even more extensively in future designs, primarily due to the increased complexity of computer systems and the economy of using scratchpads to implement these complexities.

In preparation for the discuss-only session, the author should assemble additional data on his cost analysis technique for evaluating scratchpad memory devices and implementation.

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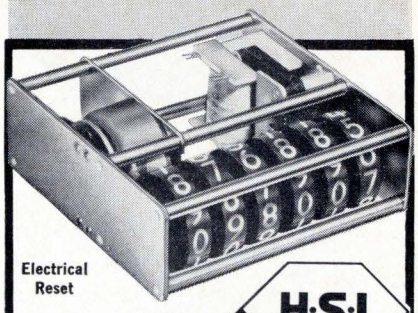

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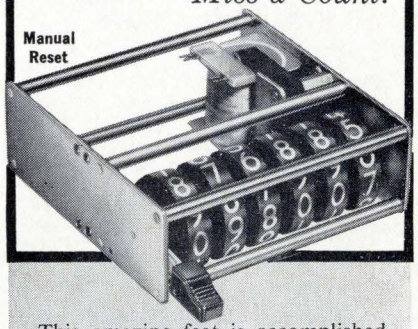

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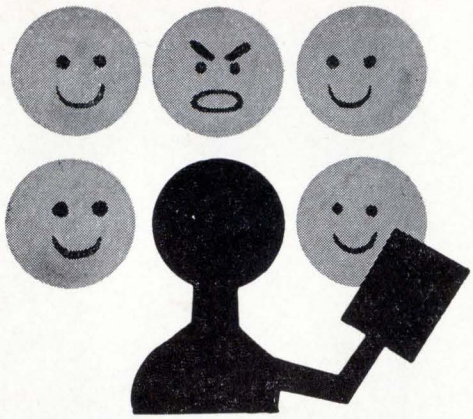

"High-Speed Read-Only Memories" Session

This discuss-only session, organized and scheduled to be chaired by J. Reese Brown, Jr. of Burroughs Corp., Pasadena, Cal., takes a broad look at the hardware aspects of different types of read-only memories. The session will commence with the discussion of a survey paper which reviews the state-of-the-art. Three other papers describe some read-only memory implementations. Here are reviews of the 4 papers.

A Survey of Recent Read-Only Stores

D. M. TAUB
IBM Corp., United Kingdom Labs

The purpose of this paper, according to the author, is to consider developments in read-only stores which have taken place since 1961. Developments prior to that time had already been reported by the author in a paper titled, *"A Short Review of Read-Only Memories,"* which he lists as Reference No. 1 on this paper. The paper does a respectable job of reviewing the current state-of-the-art; however, it falls somewhat short in clearly identifying those developments that are new vs. those that existed prior to 1961. Much of the paper is devoted to a general review, which is largely a duplicate of Mr. Taub's earlier paper.

It is suggested that the discussion at the conference be directed toward highlighting those items which represent the latest developments so that the magnitude of improvements and the trend of developments may be discerned. Suitably augmented by such discussion, this paper should be truly helpful in bringing attendees up to date on the status of read-only stores.

Development of an E-Core Read-Only Memory

P. S. SIDHU
Ampex Corp., Redwood City, Cal. and
PROF. B. BUSSELL
Univ. of Cal., Los Angeles, Cal.

This paper describes a read-only memory in which information is written by linking or by-passing the primary leg of a linear transformer core with a conductor used as the word drive line. A transformer core is used for each bit position of a word, and a multi-turn sense line is wound around the secondary leg of the transformer core. With a single primary leg as just described, the sense circuitry would distinguish a signal output as a binary 1 and the absence of a signal (ideally) as a binary 0. However, to alleviate the signal-to-noise discrimination problem in this system, a 3-legged core is used, with one primary leg being linked for binary 1 and the other for binary 0. Now the sense circuitry need only discriminate against output polarity instead of amplitude. The 3-legged core is actually assembled from two E-shaped cores, hence the name.

A model of 1024 words by 24 bits was built. Electrically, the storage array actually consisted of two banks of 256 48-bit words. Cycle times of 250 nsec were achieved with drive currents of 50 ma. A large table is included which is intended to show how the optimum number of sense winding turns was determined, but it is not obvious how the table was used. Also, another table gives a comparison of cost and performance of different ways of organizing the memory, including multiple-select instead of linear-select organization.

However, the accompanying text does not provide enough supporting detail to make the comparison as effective as it might be.

A Thin Magnetic Film Computer Memory Using A Resonant Absorption Non-Destructive Readout Technique

J. L. ARMSTRONG, W. MAY, and W. W. POWELL
Hughes Aircraft Co.,
Culver City, Cal.

H. A. Toombs and T. E. Hasley described a technique in the *Proc. — IRE, June* 1962, which utilizes ferromagnetic resonance to obtain non-destructive readout in thin permalloy film memories. This paper describes a study made to determine how this technique could best be utilized in medium and large ca-

pacity computer memories. The technique depends on detecting a change in the absorption of RF energy by a magnetic film spot. If an RF field is applied orthogonal to the easy axis, and a plot of RF energy absorption versus frequency is made, the absorption peaks at the resonant (Larmer precession) frequency. If the spot is driven at a frequency below resonance, and a sampling pulse is applied in a direction opposing the static magnetization vector, the resonant frequency is lowered and causes the film spot to absorb more energy. Less energy is absorbed if the sampling pulse is in the same direction. Therefore, if RF is applied to a strip line conductor coupling a row of spots and a sampling field is applied to the column of spots, the latter will modulate the attenuation, and hence amplitude, of the RF signal down the line. An amplitude detector at the output of the RF line can then determine the state of spot at the intersection of the lines. The action of the RF and sampling fields provides coincident-circuit selection capability. However, it also requires that information format be changed in going from writing to reading, in the same sense of "turning the corner" on a punched card.

Apparently the extent of the study to date has been the testing of fifty matrices of 24 by 32 spots driven at a frequency of 550 mc. However, factors concerning feasibility are discussed partly in terms of a hypothetical 4k key 48-bit system.

A High-Speed, Woven Read-Only Memory

H. MAEDA and M. TAKASHIMA
Toko, Inc., Tokyo, Japan and
A. J. KOLK, JR.
General Precision, Inc.,
Librascope Group,
Glendale, Cal.

In earlier conference papers, a technique for weaving DRO and NDRO memory arrays was described. This technique consisted of employing conductors plated with a uniaxial anisotropic permalloy film as the basic storage element. Lengths of these conductors are woven with insulated conductors. The plated conductor serves as both the sense and digit line, and the insulated conductor serves as the word drive line. This paper describes a technique for producing a read-only memory by a variation of the weave. Essentially, this variation consists of arranging the word line to link the plated wire to "write" a binary 1, and to by-pass the plated wire for a binary O.

In the DRO form of the woven memory, the word drive line is arranged so that the region of permalloy encircled by it is driven into the hard (axial) direction by the READ pulse. This induces a positive or negative signal in the sense line depending on the original direction of circumferential magnetization. When the READ current is shut off, the magnetization of the switched material returns to the circumferential direction determined by the polarity of the digit current pulse which must be turned on prior to word drive shut-off. In contrast, in the read-only form of the memory, a READ pulse can switch permalloy only if it links it, and a dc digit current is used to restore the magnetization of all bits to the same direction. The read-only memory, therefore, generates an output pulse for a binary 1 and no pulse, ideally, for a binary 0. The electrical characteristics are such that a memory containing a few thousand 32-bit words with cycle times of 100-150 nsec is "easily obtainable." It is not clear from the paper how much of this memory has actually been built. Graphs of output voltage versus bend and twist angles, shown in the paper, are intended to indicate that the element is insensitive to mechanical stresses encountered in the weaving process. However, it appears from the graphs that considerable sensitivity exists if a 30 degree bend can occur over an 85 mm length. This is not clarified in the paper.

The memory described is attractive because of its high speed and low cost potential. It would be interesting to discuss a more detailed comparison with competing techniques.

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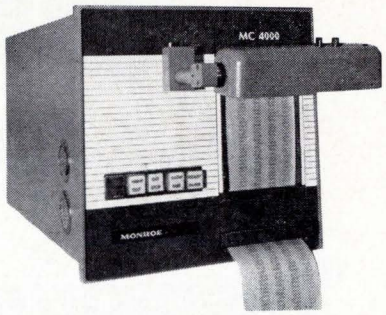

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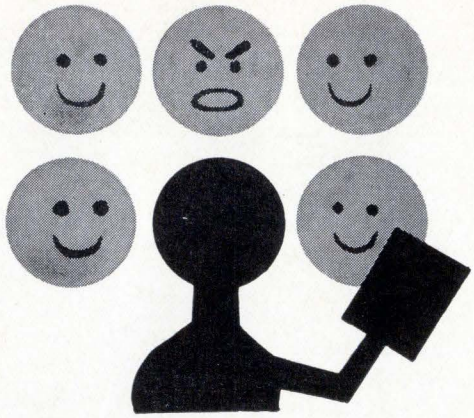

"Memories for Future Computers" Session

Donald A. Meier, of the National Cash Register Co. of Hawthorne, Cal., organized and will chair a discuss-only session that explores many of the latest results in memory element and system organization techniques that are in advanced stages of development. This session was designed to give a good cross-section of advanced memory technology and is complete as time will permit. It is interesting to note that many techniques that will be described in this session were thought to be unobtainable and impractical just a few short years ago. Reviews of the 5 papers for this session are presented below.

High-Speed Ferrite 2½ D Memory

T. J. GILLIGAN and P. B. PERSONS,
Electronic Memories, Inc.,
Hawthorne, Cal.

A 900 nsec cycle time memory system using a 30 mil discrete ferrite core is described in this paper. The 16K memory system is organized in a new 2½ D three-wire technique claimed by the authors to make possible a significant savings in the costs of electronics when compared to a linear-select organization. The authors describe the choices of factoring in both the word and bit direction for this system. The advantages of the 2½ D organization such as in recovery, short drive lines, and a small number of cores on a drive-sense intersection are also described. Details of the system construction, circuit details, and operating margins by schmoo diagrams are covered in good detail.

It is hoped that this paper will provide a platform to air an existing controversy within the industry. Namely, the discrepancies in claims made relative to cost, power dissipation, and speed of operation for a 3-wire system.

Monolithic Ferrite Memories

I. ABEYETER,
M. M. KAUFMAN,
and P. LAWRENCE,
R.C.A. Corp.

This is the first paper to appear on the monolithic ferrites indicating that this technology has moved from the research laboratory into advanced development. It describes the details of construction, electrical characteristics, and system tests of a basic laminated memory stack. Such aspects as the ferrite wafer construction, the stack assembly, and system organization are discussed in considerable detail. Also discussed are the test procedures and results, some material characteristics, and semiconductor requirements. The batch fabricated wafer described in this paper has the following characteristics: 4096 elements per wafer; approximately one inch square; stores 2048 bits per wafer. The monolithic ferrite wafer is described in a test system of 256 words of 64 bits each. When projected into a 4096-word memory, a cycle time of 500 nsecs is anticipated.

Laminated ferrite techniques appear to have made significant progress in recent years. However, reliable batch fabrication techniques have yet to be proved.

Design and Fabrication of a Magnetic, Thin-Film, Integrated Circuit Memory

T. J. MATCOVICH and W. FLANNERY,
Univac, Div. of Sperry Rand Corp.,
Blue Bell, Pa.

The design and fabrication of an integrated circuit thin magnetic film memory system is described in this paper. This system is designed to make effective use of uncased integrated circuits, thin magnetic films, and evaporated aluminum conductors. The concept of the whole memory as composed of integrated circuits and thin magnetic film as an integral unit is the theme of the paper. The design and fabrication of a 250 nsec cycle time 64 word by 24 bits-per-word system is described. Major emphasis is on the fabrication, mounting, and testing of the uncased integrated circuit chips. Equipment for handling these circuits is also described. This memory system is contained in a few square inches of area with a projected price by the authors of only 2 cents per bit.

Although the emphasis placed by the authors in this technology is correct, cost projections in the area of thin-film memories have always lagged with time. It is hoped the prediction given in this paper will not follow suit.

A 375-Nsec Main Memory System Utilizing 7 Mil Cores

G. E. WERNER and R. M. WHALEN,
IBM Corp., Poughkeepsie, New York

This paper demonstrates that the discrete ferrite core is a contender throughout the spectrum of memory technology. The authors accomplish this by demonstrating that the individual core technology can be employed in memories of high speed as well as reasonably large capacity. The discussion emphasizes the techniques necessary to increase the speed of a discrete core memory. Among these are: small high coercivity cores, transmission line construction, and array temperature stabilization. The memory system described has a capacity of 590,000 bits. The 12 mil cores are assembled on 15 mil centers and mounted in two planar configurations on either side of a single continuous ground plane. This geometry provides a bit density of 4000 bits per square inch. The linear select memory organization achieves a 375 nsec cycle time with 2048 words of 288 bits each, logically organized as 8192 words of 72 bits. The authors also comment on the necessary changes to reduce the cycle time to 240 nsec.

Although the authors feel optimistic about the ferrite core, an objective discussion of claims made by the industry at large would be appropriate for this session.

Batch Fabricated Matrix Memories

THOMAS L. McCORMACK,
CLAUDE P. BATTAREL,
and HARRISON W. FULLER,
Solid State Laboratory for Electronics,
Boston, Mass.

This paper describes a method of etching memory elements from a sheet of permalloy material with the accompanying wire of electroplated copper. Various steps in making the main array such as photoetching, evaporation, and electroplating are explained in good detail. These manufacturing methods achieve small size with resulting low power requirements. Extensive tests of many completed 64 × 64 matrix arrays are given with their yields encouraging enough for the authors to contemplate array sizes of 256 × 256. The 64 by 64 array is contained in a square of 1.6 × 1.6 inches. Presently, a linear select memory of 8000 words of 30 bits each is under development having a cycle time of 2 usec and a power dissipation of less than 10 watts. The authors also project the batch fabricated element into a mass memory with a capacity in the 108 bit range. A mock up is shown of this system.

As is true with most batch fabrication techniques, the limiting factor is yield. Reliable fabrication techniques for this technology, however promising it may appear, have yet to be proved.

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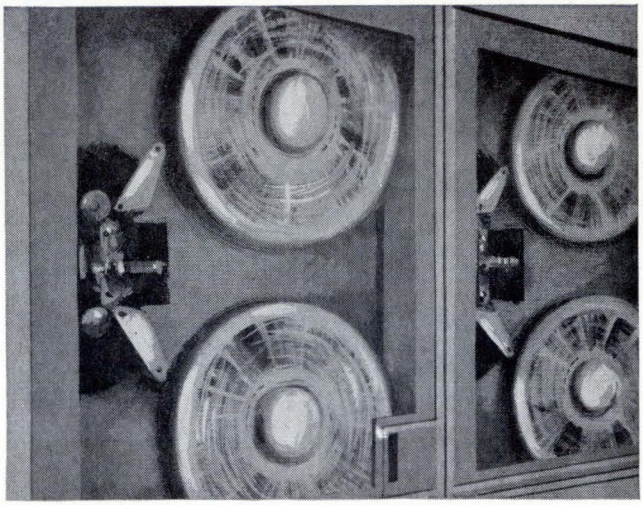

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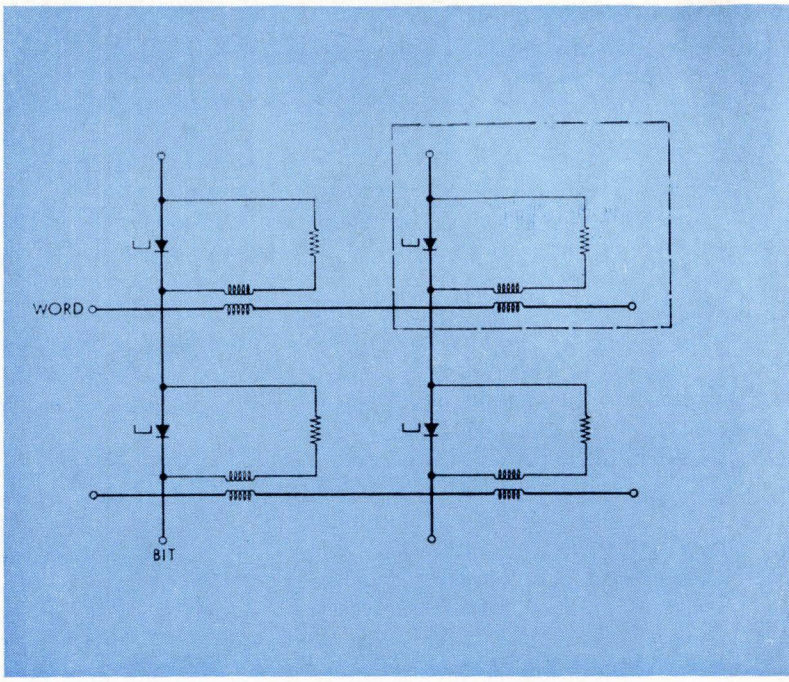
Fig. 1 (near right) Basic storage cell shown in dashed-line box consists of a tunnel diode shunted by a series-connected load resistor and the secondary winding of a transformer.

Fig. 2 (center) Tunnel diode load line diagram.

Fig. 3 (far right) Magnetic field pattern around primary conductor.



COMPLETE PAPER FROM 1965 FJCC DISCUSS-ONLY SESSION ON SCRATCHPAD MEMORIES

Design Considerations

D. J. CRAWFORD, R. L. MOORE, J. A. PARISI, J. K. PICCIANO, and W. D. PRICER,
IBM Corp.,
Poughkeepsie, N.Y.

Editor's Note: This description of the development of a practical 25 nsec. 64 x 48 tunnel diode memory is one of the most interesting papers of the discuss-only sessions. Key design features are the etch circuit transformer construction, high-speed driving techniques, and the rapid regeneration of interrogated information.

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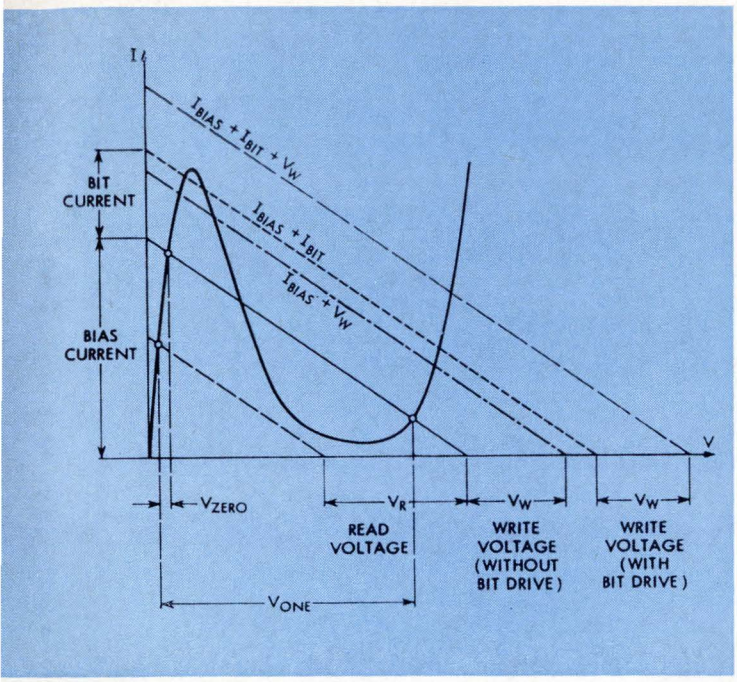
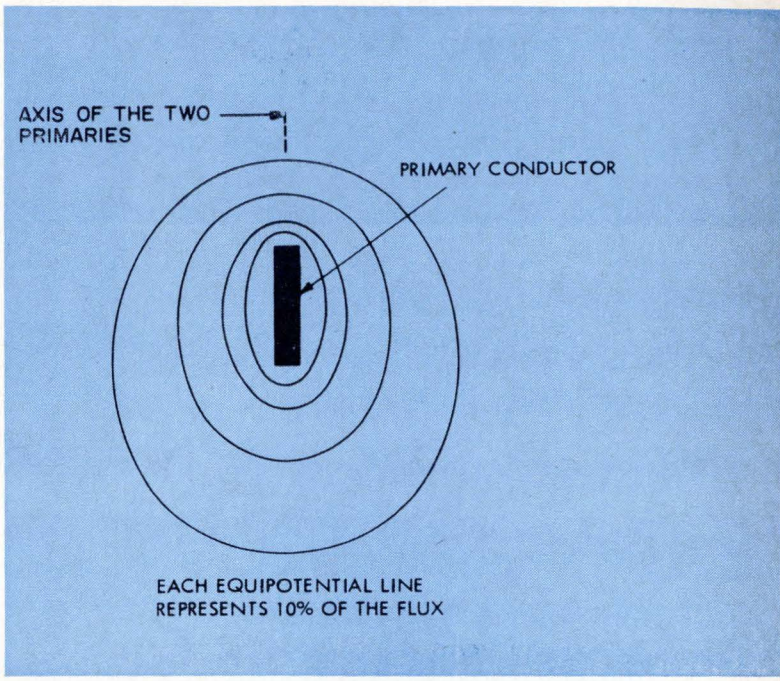
About two years ago a tunnel diode memory system was described which employed substantially different techniques than those previously used.[1] Although earlier systems had tended towards array arrangements that had the storage cells connected in parallel on one or more axes; the new system employed series connections along two axes. This new arrangement has several design and performance advantages compared to previous systems. The original paper described the basic approach and some of the earlier work which included the design of array cross-sections and the associated driving and sensing circuits. Since that time one version of the system has been operational in two IBM 7030 systems,[2] and a 16-word, fully-populated, higher-speed laboratory model was built and reported.[3] This paper describes the engineering considerations used in the design of a larger and faster memory employing these basic techniques.

The new memory system contains 64 words of 48 bits each, and test results from a partially-populated cross-sectional model indicate a complete READ/RESTORE or a CLEAR/WRITE cycle time of less than 25 nsec. A fully-populated complete memory system is in the final stages of construction and assembly.

Cell Operation

The basic storage cell is simple, as shown in the dashed-line box in Fig. 1. It consists of a tunnel diode shunted by a series-connected load resistor and the secondary winding of a transformer. A biasing current is introduced to the tunnel-diode storage cell along the bit axis. During the writing portion of a memory cycle, the biasing current can be increased by the addition of a bit current. The word





or a 25 NSEC Tunnel Diode Memory*

driver introduces voltage excursions within the storage-cell loop by means of the transformer. The normal bias current through the tunnel-diode cell is such that the tunnel diode can be either in a high-voltage region or in a low-voltage region.

The cells are series-connected along two axes (Fig. 1) in order to form the basic memory array configuration. Fig. 2 shows the load-line diagram for the basic storage cell. The current bias and the load resistor are such that the cell normally has two stable states. During the READ operation, if the cell has been storing a ONE, the voltage induced into the secondary winding of the cell transformer shifts the load-line and clears the cell from the high-voltage state to the low-voltage state. The net voltage drop when the cell changes its operating point from the high-voltage to the low-voltage state is transmitted through the series connection of the diodes on the bit line to the end of the bit line, where it can be detected.

On the other hand, if the cell was storing a ZERO, it initially would be in the low-voltage state. The shifting of the load line in this case by the READ voltage, V_r, produces only a very small voltage as the ZERO response. At the conclusion of the READ cycle, all the cells associated with the particular word will have had their information read out and will be left in the low-voltage state.

Array Design Considerations

One of the key items in the design of the system is the cell transformer. The objectives are to achieve a low impedance when looking into the primary loops, and have reasonable inductive coupling but a minimum of capacitive coupling from primary to the secondary loop. In the earliest work, etched circuit construction was tried but the state-of-the art of fine-line etching and the difficulty of making good miniature connections made the approach impractical at that time. The succeeding systems employed transformers with secondary windings made of wire. When the work on this new system was started, it was decided to attempt to solve again the various problems of the etched circuit transformer for the inherent advantages of reproducibility it offered.

The first step in the design process was to study electric field patterns of likely configurations using resistance paper analog techniques. From this work, reasonably accurate predictions of the transformer parameters such as mutual coupling and secondary self-inductance were made. This procedure permitted a quick review and optimiza-

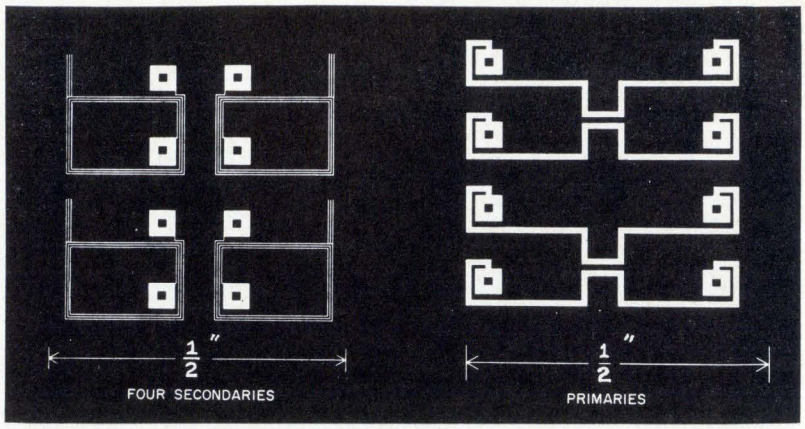


Fig. 6 Final transformer patterns.

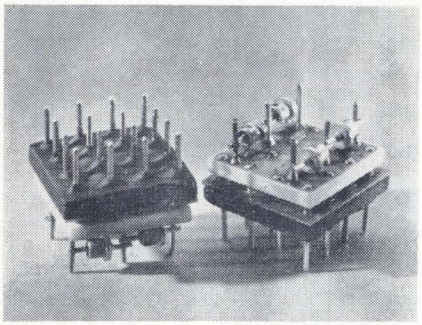
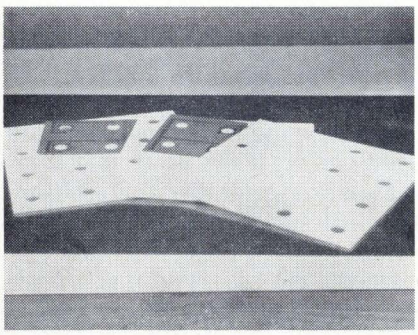


Fig. 4 Assembled memory array modules.



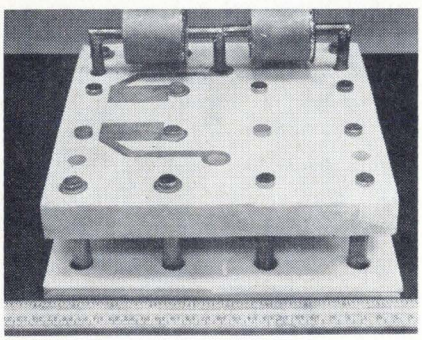


Fig. 5 Top photo — transformer wafer sheets, twenty times normal size; bottom photo — memory module, twenty times normal size.

tion of different transformer patterns. A typical field plot used is shown in Fig. 3. As a result of this work, preliminary decisions were made as to the desired shape and dimensions of the transformer.

At this time different constructional methods and arrangements of the storage cell into arrays were considered from both a mechanical and electrical viewpoint. It was finally decided that an approach which had several cells on a module would simplify manufacturing problems and improve serviceability. Although it offered certain mechanical constraints, the SLT (Solid Logic Technology) type of module employed by IBM was chosen as a starting point for the design.

An alumina ceramic wafer about one-half inch square serves as the main mechanical structure for the module. The ceramic wafer has sixteen swaged pins on 0.125 inch centers for external connections plus six pins in the opposite direction to serve as mounting points for welding the tunnel diodes. One surface of the ceramic has four screened resistors and a solder-coated circuit pattern. The transformers are contained in a separate multilayer etched copper wafer assembly that is slipped over the sixteen pins and dip-soldered. The final assembly operation consists of applying a ferrite powder coating in an organic binder on the primary side of the transformer wafer to increase the mutual coupling from primary to secondary. The assembled modules are shown in Fig. 4.

Early in the project, it was recognized that a large, accurately-scaled mockup of the module assembly was needed for making electrical measurements. These measurements were needed to assist in the transformer design, and were also vital to the determination of the overall array parameters. The normal-size modules were so small that it was virtually impossible to make electrical measurements with any degree of accuracy or precision. Because both capacitance and inductance scale directly proportional to linear dimensions, it was decided to make a module assembly twenty times normal size. One problem was to find a suitable dielectric material substitute for the ceramic substrate because large ceramic pieces were not available. The solution was found by loading an epoxy resin mixture with titanium dioxide powder in a ratio of approximately 1:1 by weight to achieve a dielectric constant of 9.4. Analog field plots showed that thick copper wiring patterns could be simulated by using two thinner patterns appropriately spaced and connected in parallel. Fig. 5 shows photographs of the large module and some of the transformer patterns.

The final transformer patterns are shown in Fig. 6. The solid squares are lands used for connecting points. To cancel capacitive coupling effects from the primary to the secondary wiring, each transformer uses two primary wires which are driven push-pull with respect to ground. The primary wires are

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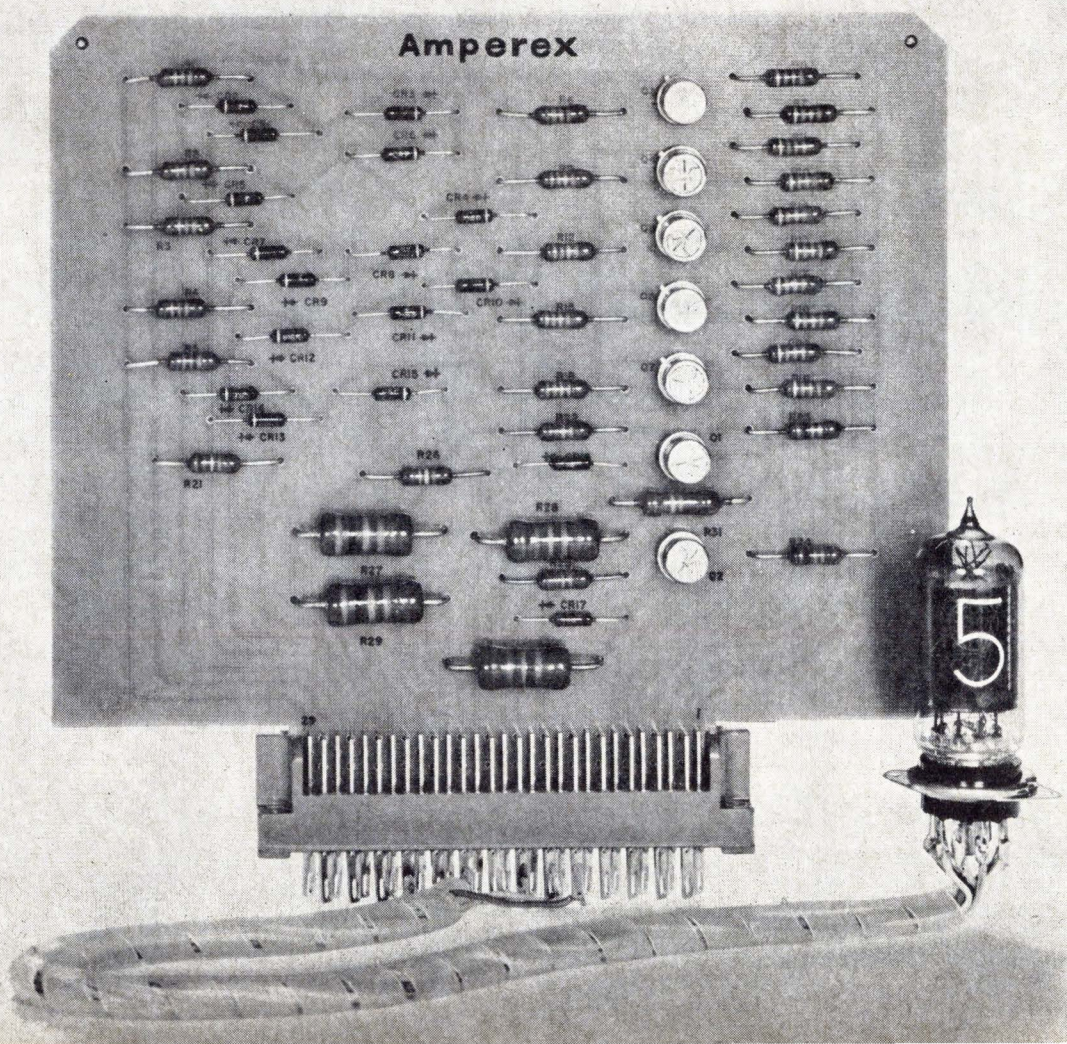

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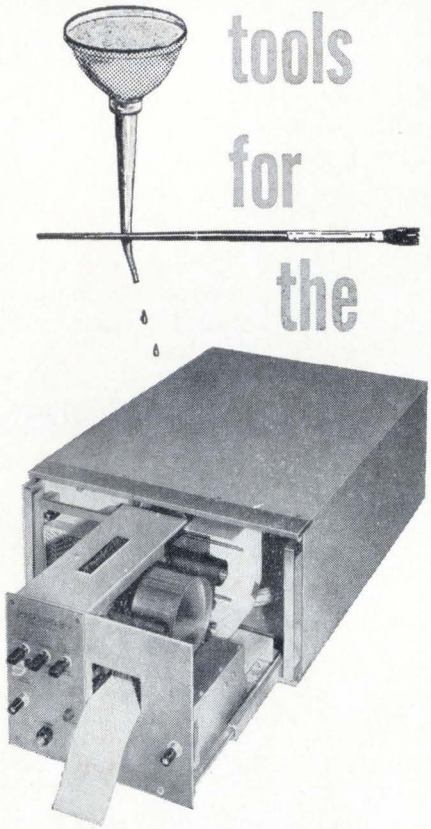

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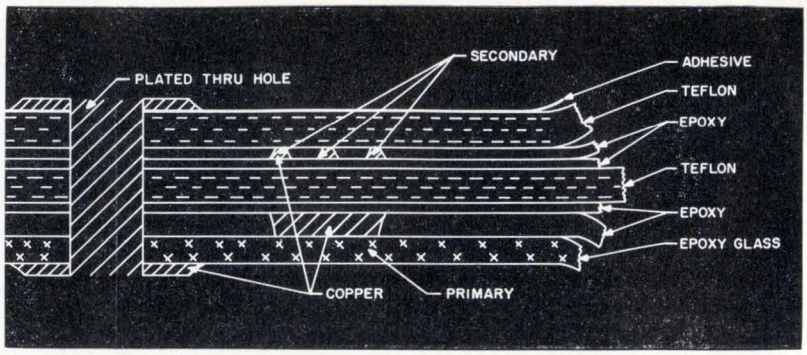

Fig. 7 Cross-section of transformer wafer.

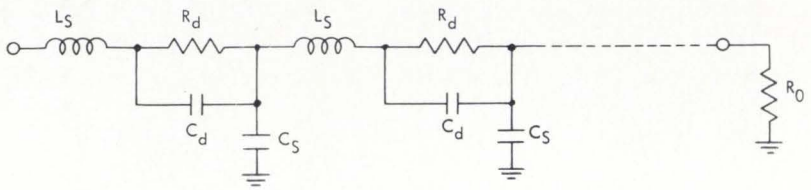

Fig. 8 Bit-line equivalent circuit.

routed in a manner to maximize the mutual coupling to the secondary wires, and the secondary wires are arranged in a mirror image configuration to match the land pattern to obtain uniform characteristics. Capacitance stub "fingers" are included to balance the capacitances between the primary lands and the secondary windings.

A cross-section of a transformer wafer is shown in Fig. 7. To minimize the capacitance, the primary and the secondary wires are separated by Teflon. The outer layers are used as supports for a land pattern for soldering to the pins, and also to protect the transformer pattern. Through-hole plating techniques are used to connect the inner land patterns with the outer lands.

Bit-Line Characteristics

The bit line used in the tunnel-diode memory consists essentially of a number of tunnel diodes connected in series. The inductance of the interconnections is the series inductance of the line, whereas the transformer and module capacitance is the major component of the shunt capacitance. However, the tunnel diodes add a non-linear series resistance component that predominantly affects the response of the line. An equivalent circuit for the line is shown in Fig. 8 where each section represents one bit of the line. The L_S is the series inductance; C_d is the diode junction capacitance; R_d is the non-linear diode resistance; and C_S is the total shunt capacitance. Because each of these parameters is very small and the current rise times desired are very fast, accurate measurements necessary to optimize the line design could not be made.

A program was written to calculate the response of the bit line that utilized this equivalent circuit and took the non-linearities of the tunnel diode characteristics into account. By using this program, the parameters of the lines were varied to find their effect on the response and to find an optimum termination. The range of parameters used was determined by measurements of the twenty-times module model. The results of the investigation led to the following conclusions:

(a) Increasing the series induc-

tance of the line does not improve the response of the line: that is, in spite of the fact that the line becomes less "lossy" as the series inductance is increased, the sum of the rise time plus the delay time increases with increasing inductance.

(b) The parameters that most strongly affect the response of the line are the diode resistance, the shunt capacitance, and the termination resistance, in this order.

(c) The optimum termination resistance, chosen with the criterion of minimum rise time with negligible overshoot, is considerably below the $(L/C)^{1/2}$ for the line. This lower terminating resistance by reflection tends to increase the attenuated bit drive current at the far end of the array.

(d) Because of the non-linearity of the diode resistance, the fastest response times are obtained when the bit drive is toward increased current in the diode.

Actual measurements verified these predictions but could not provide the accurate resolution obtained in calculations.

Two types of crosstalk were investigated. One was the inducement of a false sense signal on a bit line because of a switching tunnel diode on an adjacent bit line. The other type was accidental writing into a tunnel diode receiving full word current by way of mutual inductive coupling between transformer secondaries. The primary source of a false sense signal is the capacitance between cells on adjacent bit lines; these transformers are only 50 mils apart. The value of the capacitance predicted by the twenty-times module (0.31 pf) is slightly high because no ground plane was used in the measurement. In order to find the worst case, it was assumed that the capacitance of eight cells are all lumped together at a point and that the voltage rises in one L/R time constant. Under these conditions, it is predicted that a maximum of 96 mv would be produced from the two adjacent bit lines. However, the actual noise should be much smaller and the detector rejection level is safely above 96 mv.

Calculations were made of the

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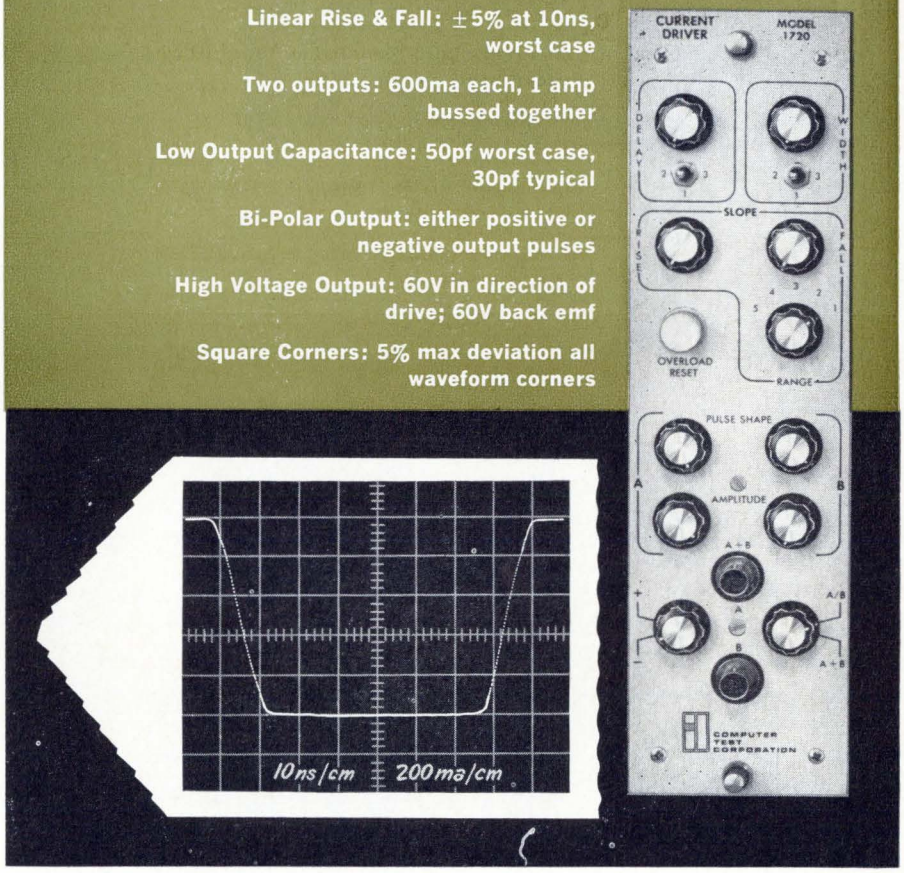

highly linear rise and fall

In practical applications, most magnetic memory devices, such as cores, thin-films and plated wires, switch states as easily with an exponential drive as with a linear drive. Test applications, however, demand better performance from the driving source. Repeatability and correlation of test data can only be achieved if the driving pulse has a well-defined, unambiguous shape. Straight line linearity of the rising and falling edges is the critical factor.

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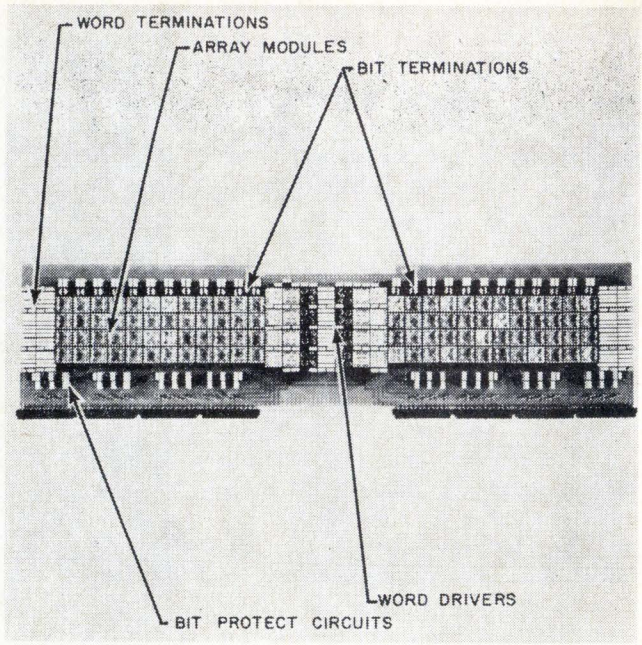

Fig. 10 An assembled array card contains a storage capacity of 8 words, 48 bits per word.

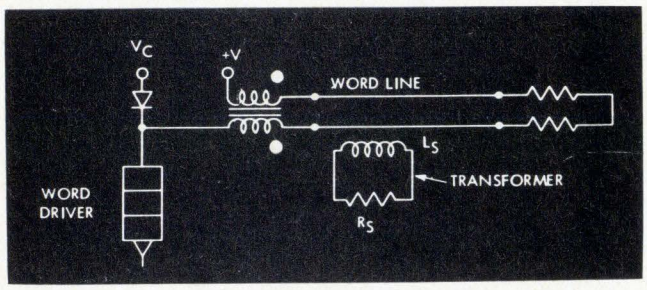

Fig. 9 Word drive system.

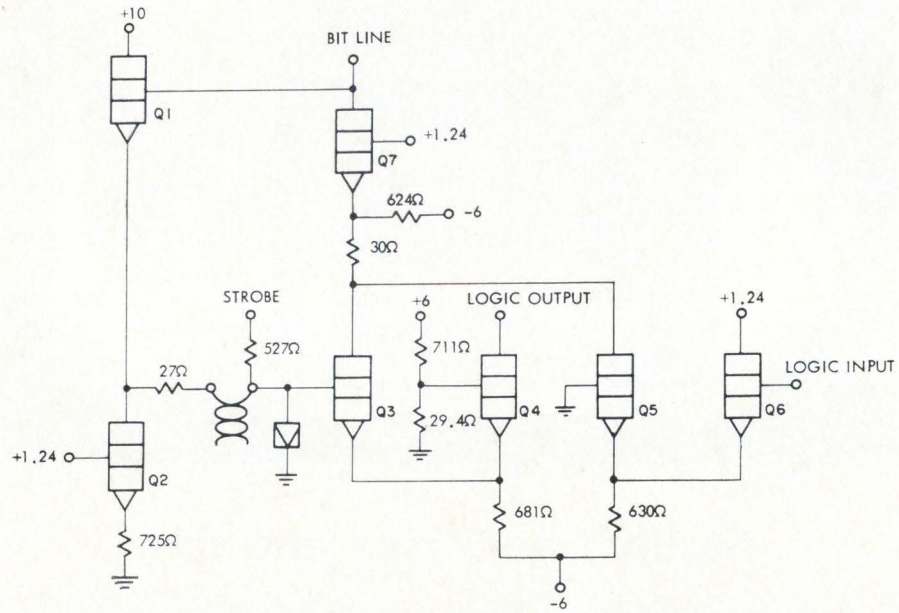

Fig. 11 The Information Control Circuit (ICC) operates as follows: the first transistor, (Q_1) connected as an emitter follower, receives a sense signal as its base and drives a transmission line that is open-circuited at the far end. This passes a pulse of a width of approximately three nsec. If the strobe input is positive at this time, the tunnel diode switches on the first 200 mv of the signal. The detector diode remains in the high state as long as the strobe pulse is present. This drives the current switch ($Q_3 + Q_4$) that supplies the bit current pulse to the bit line. The bit drive may also be actuated by pulsing the logic input terminal negatively (Q_6). The bit-driver collector current increase of the output transistor rises in two nsec or less, and the entire line assumes the full drive amplitude within seven nsec of bit-driver turn-on. No overshoot has been observed. In addition to furnishing the bit pulse, the output transistor also supplies the dc biasing current for the bit line. Throughput time of the ICC from sense-amplifier input to bit-driver turn-on is two to three nsec. The total time elapsed from the resetting of the tunnel diode to its ZERO state until the restoration of that diode to its ONE state is 10 to 11 nsec. During the write noise, the first transistor cuts off, thereby preventing the write noise from influencing the state of the tunnel diode detector.

worst-case noise current induced by mutual inductive coupling between adjacent transformer coils. They showed that the peak induced current would be less than 2.5 per cent of the diode peak current. This value is small enough to have a negligible effect on operating tolerances.

Word Line Study

The ferrite material on the primary winding of the transformer increases the characteristic impedance and delay of the line compared to a similar line without the ferrite. In addition, the ferrite increases the high-frequency losses and results in rise-time deterioration as the word pulse travels down the line. To maintain a reasonable variation in rise time, the word lines are split into 24-bit segments, with two segments being driven by the two output stages of a word driver circuit.

A number of methods of maintaining independence of the secondary output current from primary current rise-time variations were investigated. These involved shorting the word line or inserting a rise time pad in the output of the word driver circuit. An investigation of the response of the transformer itself showed that secondary induc-

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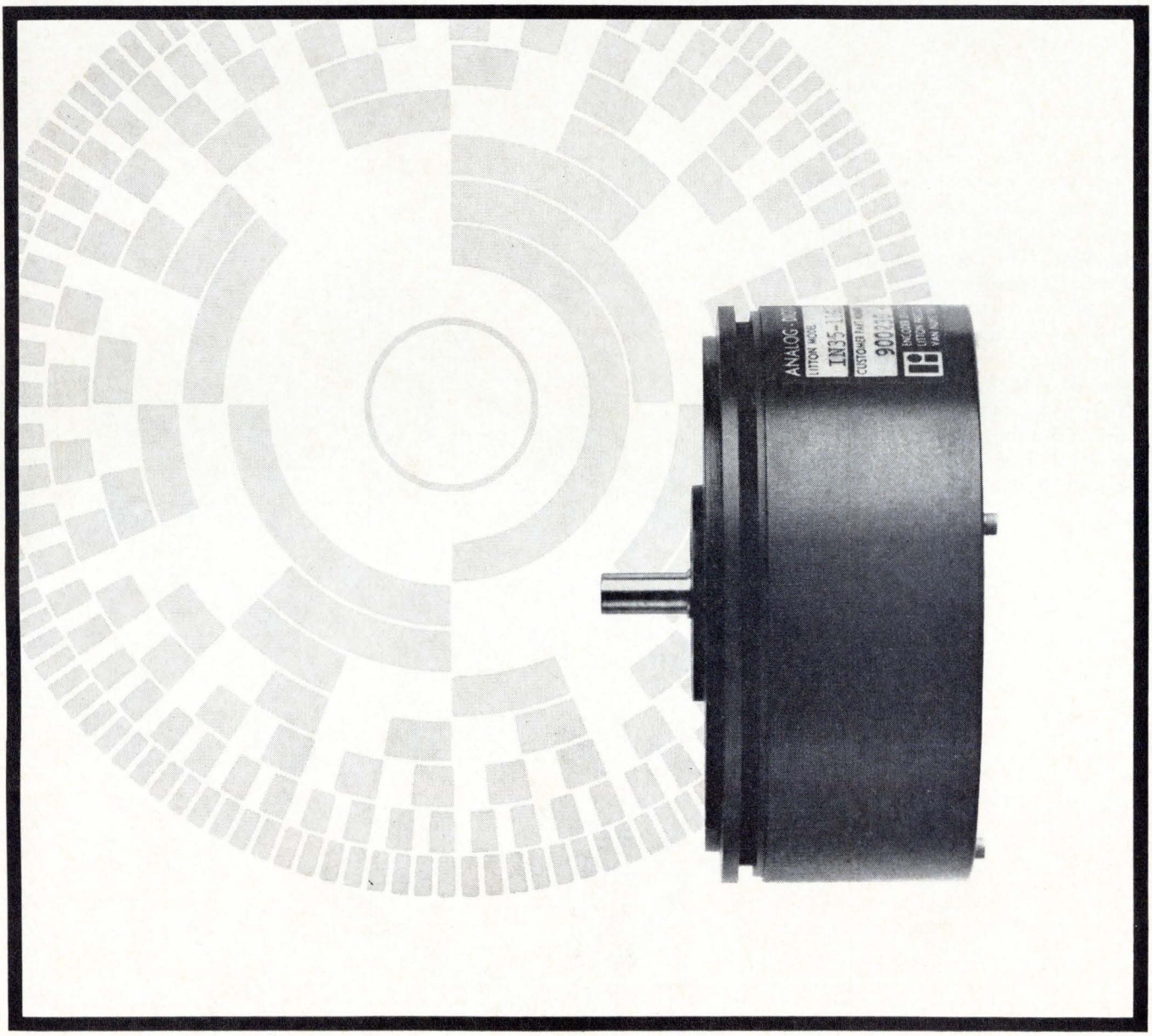


Optical ■ ■ ■ ■ ■ Solid-State Optical ■ ■ ■ ■ ■ Magnetic ■ ■ ■ ■ ■ Contact

CIRCLE NO. 21 ON INQUIRY CARD

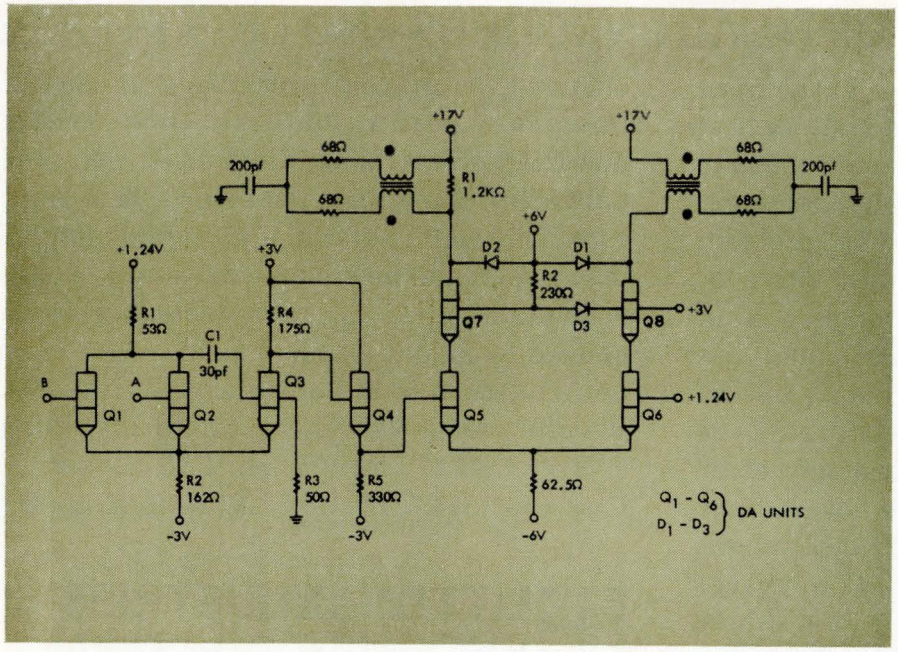


Fig. 12 The word driver circuit operates as follows: the current switch formed by Q_1, Q_2, and Q_3 performs the logical AND function and provides regenerative feedback through C_1 to improve the rise time of the input pulse; Q_4 provides the necessary current gain to drive the output stages. In this circuit, both outputs from the current switch are utilized to drive the word line in two segments. Output stage consists of the current switch formed by Q_5 and Q_6, which drives two 2N2369A (Q_7 + Q_8) transistors for increased voltage gain. Output levels are clamped by the diodes D_1 and D_2 to provide a well-controlled output level. Two wires of each word line segment are driven push-pull with respect to ground by a balun transformer. Because of the relatively light drive power requirements, high-speed current switch techniques can be used. It should be noted that half the driver is left ON all the time because only the changes in drive line current can activate the tunnel diode cells through the transformers.

tance and load resistance caused it to act as a reasonable rise-time pad to a fast word-drive pulse. Fig. 9 shows the method of drive presently employed. The line is terminated in its characteristic impedance, and the pulse is clamped at the driver to control the pulse amplitude. The transformer secondary circuit is used as a rise-time pad so that a 20 per cent change in the primary current rise time results in only a 10 per cent change in the secondary output voltage amplitude.

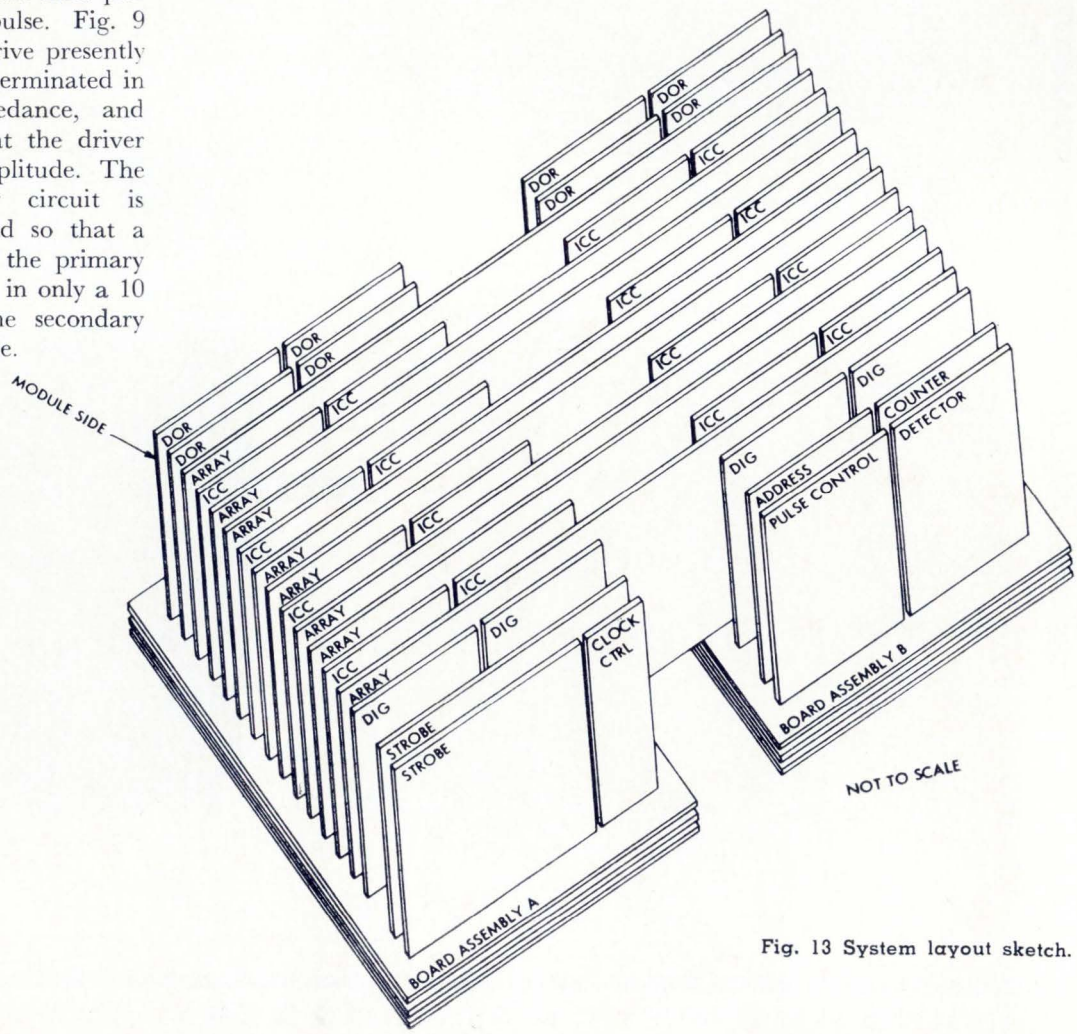
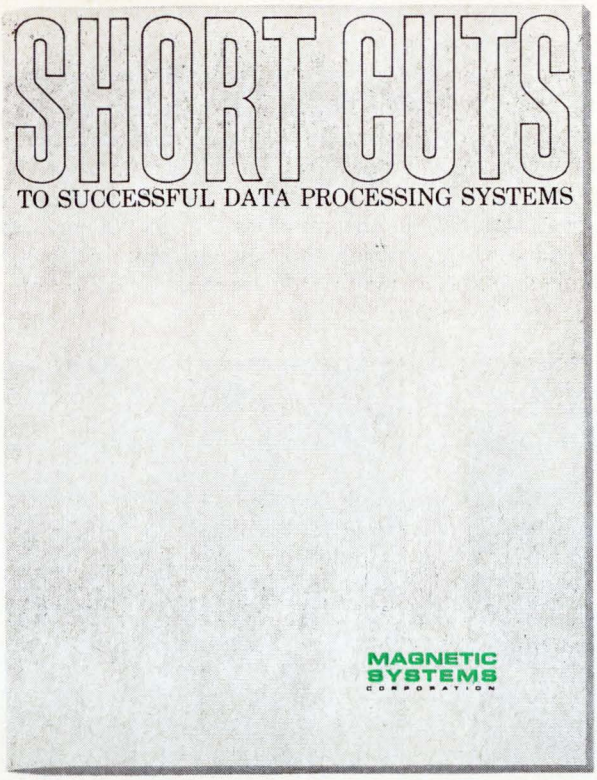


Fig. 13 System layout sketch.



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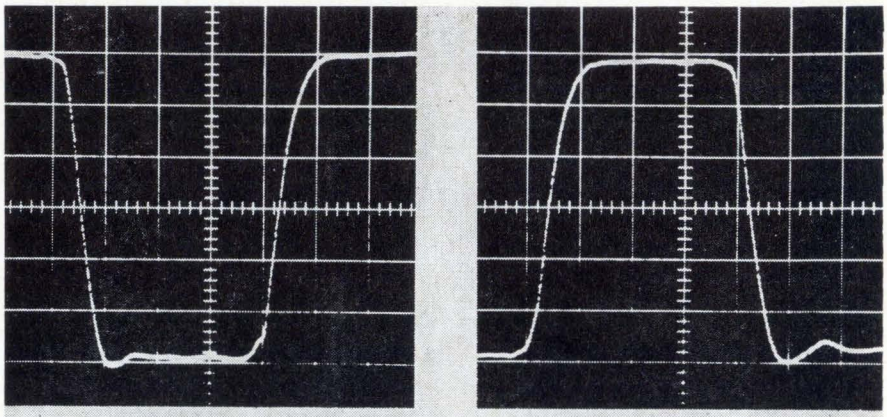
CIRCLE NO. 22 ON INQUIRY CARD

Array Characteristics

The array is formed by mounting the memory cell modules on a pluggable card which contains the interconnection pattern. The card has etched wiring on the two outer surfaces and a ground plane inside the laminate. In addition to the memory cell modules, the array card also contains all the word driver circuits, word line termination networks, bit line termination networks, and miscellaneous power supply decoupling networks associated with the modules. Each card contains eight words; forty-eight bits per word of storage. An assembled array card is shown in Fig. 10.

One of the advantages of the series-type array is that the driving requirements are readily met with high-speed transistors. The array described utilizes a unidirectional current pulse of 88 ma into the word line and presents a load of 136 ohms to the word driver. As previously explained, each word line is split into two 24-bit segments, with a pair of segments driven by one word driver circuit. The propagation delay from the word line input terminals to the far end of each line is about three nsec.

In contrast to the word line, the bit line is much more like a distributed RC-line than a conventional low-loss transmission line and, therefore, exhibits high-phase and frequency distortion. To minimize delay, the bit line is broken into eight-bit segments, with a pair of segments handled by each information control (regeneration) circuit. The bit drive required is only 8.27 ma and is also a unidirectional pulse into a load impedance of about 50 ohms. Output signals for sensing are in the range of 300 to 400 mv, although the detector sensing level is usually set lower to save cycle time.

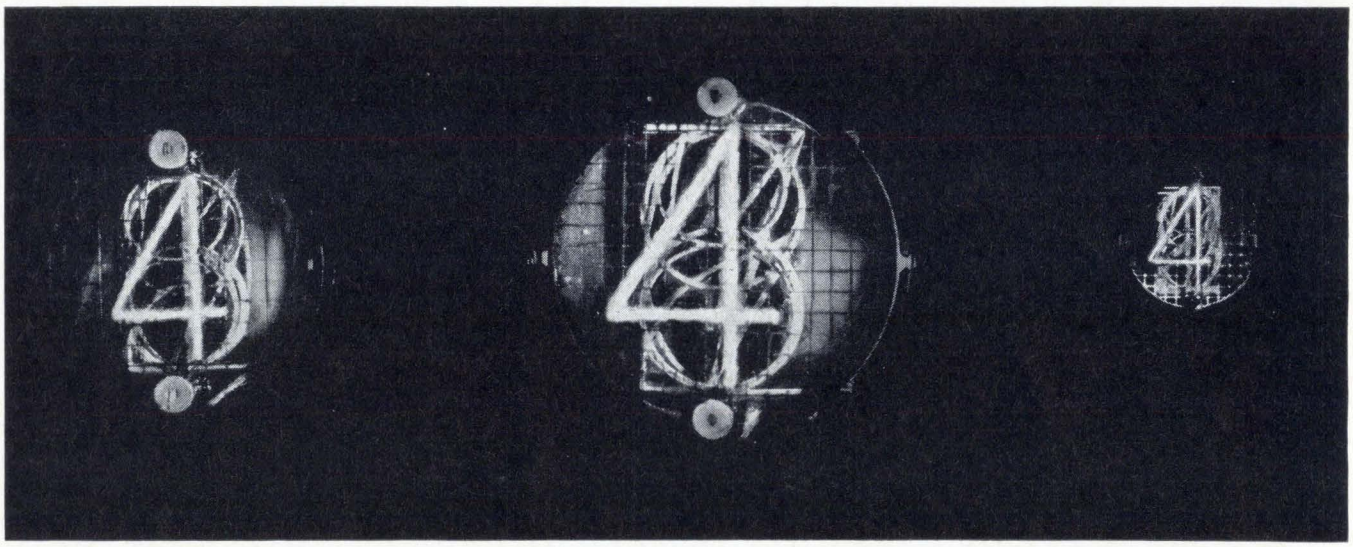


a. In phase output.

b. Out of phase output.

(Horizontal = 5 ns/div and vertical = 2v/div. R_L = 136 ohms.)

Fig. 14 Final word-driver output wave-forms.



Stare at these digits for a few seconds.

CIRCLE NO. 23 ON INQUIRY CARD

Circuit Design

Fig. 11 shows the information control circuit diagram. The sense amplifier, detector, information control logic, bit-line bias current, and bit driver were included in this single circuit to shorten regeneration time and to simplify the circuitry.

The word driver circuit is shown in Fig. 12. The word driver produces an output pulse of 88 ma into a 136-ohm load. The current amplitude stays within a tolerance of ±10 per cent under worst-case conditions. The rise and fall times of the pulse are nominally three nsec, 10 to 90 per cent. The worst-case tolerance on the write transition is within ±15 per cent of nominal value and the read transition is at least as fast. The waveforms of the two outputs of the word driver are shown in Fig. 14.

Overall System Description

In addition to the memory array and the associated driving and sensing circuits, the complete system includes a binary address register with decoding circuits, data input gating circuits, a data output register, and a clock with timing pulse distribution circuits. An address counter, comparing circuits, and manual data input switches permit exercising the memory system without using any external connections. Either the internal clock or an external source of clock pulses may be used. The logic circuits are constructed of an advanced form of IBM solid logic technology, referred to as ACPX in Conference papers presented previously.[4,5]

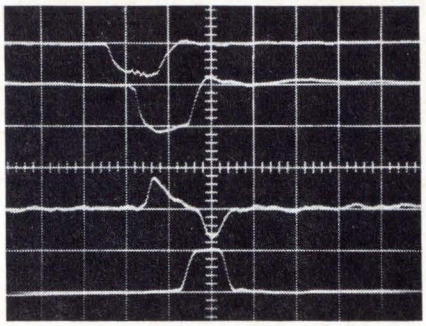
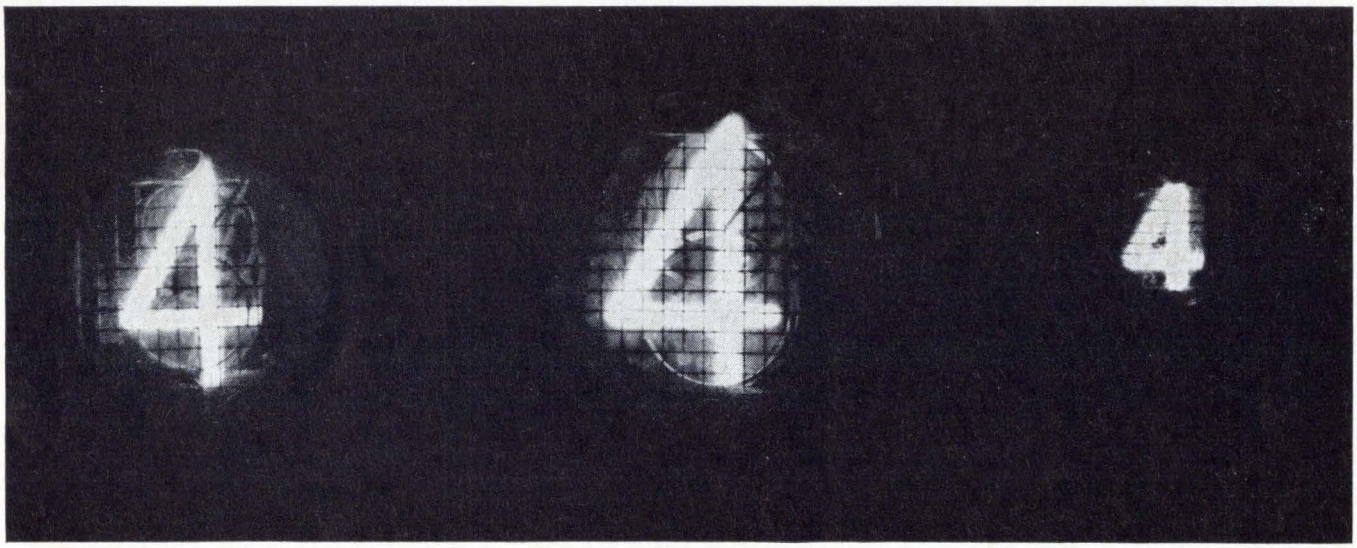


Fig. 15 Cross-sectional model memory circuit timing waveforms (10 ns/cm). The traces from top to bottom are input to word driver; driven end of word line; transformer output of the cell at the far end of the word line; and output of information control circuit.

The system interwiring and voltage distribution is contained in two multiple-layer boards, each about 10 by 14 inches, mounted side by side. These boards have male pins protruding from them which serve as connecting points for external wiring and also receive the sockets mounted on the bottom of each circuit card. The memory array cards are about eighteen inches long and plug into both board assemblies, bridging across the gap between them. Except for one narrower card, all the other circuit cards are about three inches wide and five inches high. About two-thirds of the volume is used by the memory array and the information control circuits; the remainder is used by the various logic circuits. A sketch of the layout is shown in Fig. 13. The card and board assemblies, blower system, power supplies, con-



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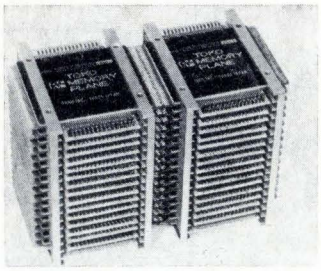
MODEL	TYPE	BITS	WORDS	DIGITS	WORD DRIVE CURRENT	DIGIT DRIVE CURRENT	READ OUT WORD DRIVE CURRENT	OUTPUT (NOTE 1)
MX-W32D40-2RD	DRO	1280	32	40	500 mA	65 mA ± 10%	—	6 mV
MX-W32D64-2RD	DRO	2048	32	64	500 mA	65 mA ± 10%	—	6 mV
MX-W32D40-2GD	DRO	1280	32	40	500 mA	50 mA ± 10%	—	6 mV
MX-W32D64-2GD	DRO	2048	32	64	500 mA	50 mA ± 10%	—	6 mV
MX-W64D64-1TD	DRO	4096	64	64	500 mA	65 mA ± 10%	—	4 mV
MX-W32D40-2RN	NDRO	1280	32	40	500 mA	65 mA ± 10%	160-200 mA	2 mV
MX-W32D64-2RN	NDRO	2048	32	64	500 mA	65 mA ± 10%	160-200 mA	2 mV
MX-W128D40-1TN	NDRO	5120	128	40	500 mA	65 mA ± 10%	160-200 mA	1 mV

NOTE 1 — Current rise time of 50 ns
NOTE 2 — Digit drive current ±15%, ±20% available



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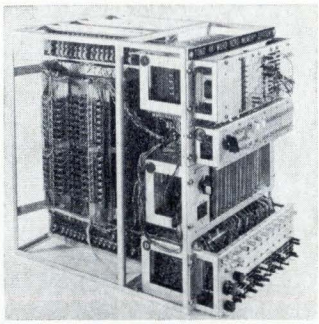
4096 words NDRO
MEMORY SYSTEM

Word Write Current: 500 mA
Word Read Current: 200 mA
Digit Current: 65 mA ± 20%
Sense Output Voltage: 2 mV, min. (t_r of Read Current at 40 ns)
Read Time: 300 ns



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CIRCLE NO. 24 ON INQUIRY CARD

trol panel, and I/O connection panel are contained in a cabinet.

Tests on a cross-sectional model containing two populated word lines and four populated bit lines indicated good operating margins with a cycle time in the range of 22 to 24 nsec. Fig. 15 shows the actual voltage waveforms. Minor improvements have been made since that time. It is expected that the completed system will also have an operating speed in the same range. This represents the first complete memory system, using any type of technology, reported in this size and speed range.

Neither cost, present or projected, nor the amenability of this technique to larger size memories was described in this paper. The authors should be prepared to discuss these particular facets during the discuss-only session at the 1965 FJCC.

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2. *"Series-Coupled Tunnel Diode Memory,"* **COMPUTER DESIGN,** Vol. 2, No. 10, November, 1963, p. 8.

3. **G. Feth,** *"Scratch-pad Tunnel Diode Memory,"* presented at the IEEE Workshop on Computer Memories at UCLA Conference Center, Lake Arrowhead, September 10-12, 1964.

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5. **M. J. Flynn,** *"Engineering Aspects of Large High-Speed Computer Design,"* presented at the ONR Symposium on High-Speed Computer Hardware, Washington, D.C., November, 1964.

GOVERNMENT REPORTS ★★

RELIABILITY OF INTEGRATED CIRCUITS IN MISSILE SYSTEMS

Failure rates for off-the-shelf silicon monolithic integrated circuits have been established by Battelle researchers on the basis of about 68 million part-test hours of data. No failures have been reported for operating-life tests at 25C, so it can be determined only that the failure rate is less than an upper 60 percent confidence limit of 0.067 percent per 1000 hours. The observed failure rate from system and field operational tests is 0.012 percent per 1000 hours (0.022 percent per 1000 hours at 60 percent upper confidence limit). At 125C, the observed operating-life failure rate for laboratory tests is 0.087 percent per 1000 hours. Estimated failure rates for laboratory storage tests range from 0.0055 at 25C (extrapolated) to 0.22 at 150C, and 2.4 at 300C.

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Sponsored by the Army Mathematics Steering Committee, this study includes such topics as algebraic operations with power series on a digital computer, computer curve plotting using the West Point system, use of computer-made decisions in quality evaluation, and real-time operations at White Sands Missile Range. Other papers discuss error analysis for rocket and ballistic trajectories, a dynamic programming solution for a combinatorial problem involving the selection of optimum weapon yields, and work in progress at the Mathematics Research Center on numerical solution of the Navier-Stokes equations.

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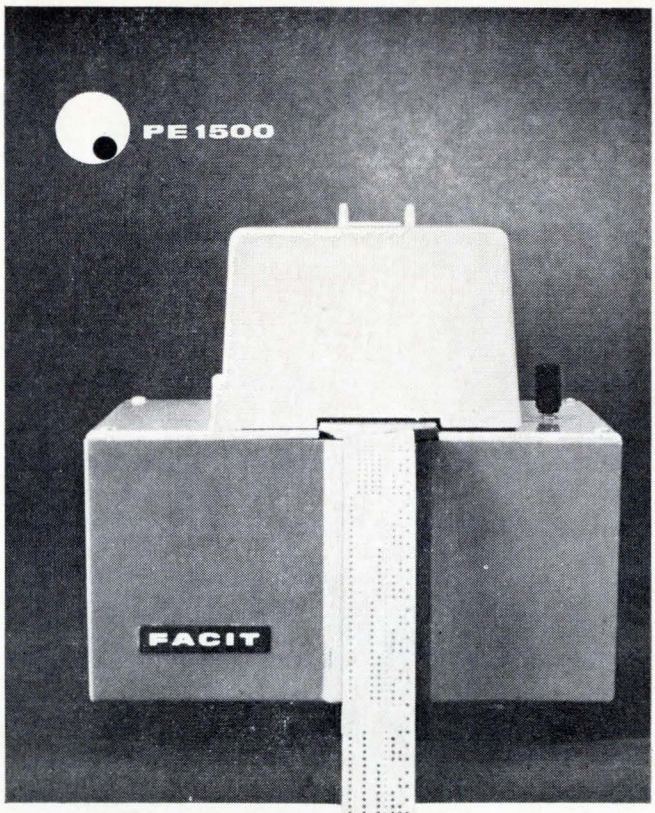

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CIRCLE NO. 48 ON INQUIRY CARD

REMOTE TIME-SHARING SYSTEM PERMITS ECONOMICAL PROCESSING OF SHORT ENGINEERING PROBLEMS

STEPHEN C. PLUMB, *Staff Engineer, Data Systems Div., IBM Corp., Poughkeepsie, N.Y.*

Engineering use of computers has entered a new phase — remote computing. In the developmental and experimental work which preceded the recent announcement of IBM's QUIKTRAN system a great deal of remote computing was accomplished which proved the inherent advantages of this new method.

The Scientific Computation Dept. at IBM had the opportunity of participating in this work, and in the process learned at first hand the advantages to be gained in two specific areas of operations: debugging programs, and handling small calculations which would not normally be put on a computer. The work of this department is essentially to support the design engineers involved in developing advanced electronic components, and in the design of advanced computers. The staff is comprised of engineers, mathematicians, and programmers. In the very nature of our work, we have made heavy conventional use of computers, and have also used desk calculators and manual methods. The availability of QUIKTRAN gave promise of effectively extending our engineering and programming capabilities.

Remote computing has come through the development of appropriate communications equipment and control programs, which enable geographically-distant users to obtain fast, convenient and economical access (via common carrier transmission facilities) to a central computer. The QUIKTRAN system allows up to 40 remotely-located engineers to enter, check, translate, and execute different programs concurrently on the same processor — without leaving their offices or laboratories. Furthermore, because of the rapid computer response time afforded by the system, the engineer can work at his own speed, independent of demands being made on the computer by other personnel.

The engineer, using FORTRAN language, communicates with the central computing system through the keyboard/printer of an IBM 1050 data communications terminal. The 1050, which operates at approximately 15 characters-per-second, has a print span exceeding 120 characters and can be parity-and-longitudinally-checked. The terminal can also be used, if needed, for off-line preparation of data and can be directly attached to a card reader and/or card punch.

The 1050 is connected to the central computer by regular voice-grade telephone lines. In our case, the computer was located at a data center in New York City. Input data flows through a 7740 transmission control unit which acts as the switching center. This unit assembles bits-to-characters, characters-to-messages, performs error detection and correction via retransmission, converts data from communication to computer codes, edits messages, and buffers information while awaiting 7040/7044 processing. These procedures are reversed when the computer sends a response back to the remote inquirer.

QUIKTRAN is organized in two major sub-systems: processor and monitor. The processor consists of a translator that details source language statements into equivalent intermediate representations which can then be executed by an interpreter. The monitor contains a scheduler which coordinates the computer's time-sharing capabilities, and a supervisor which controls I/O and storage allocations.

For the most part, the processor's translator is similar to in-core compilers except that it has the property of being symmetric; that is, it can perform not only source-to-intermediate translations but also intermediate-to-source translations. This is the feature which enables QUIKTRAN to provide a source language debugging function.

Author Stephen C. Plumb checks printout of circuit calculations compiled under control of IBM's QUIKTRAN computer program.

The monitor's scheduler maintains continuous control of jobs being processed, automatically determining the sequence of operations required to meet the terminal response rate and thus optimizes the utilization of all system components. The supervisor in the monitor controls the transmission of information from remote terminals as well as the movement of data between the 7040/7044 and the 7740 transmission control unit.

The major gain afforded the engineer is time. During the approximately 6 months period in which the Scientific Computation Department utilized QUIKTRAN we found we could run small production and debugging programs which previously — due to time and access limitations — had been restricted. The processing of a set of formulae, for example, re-

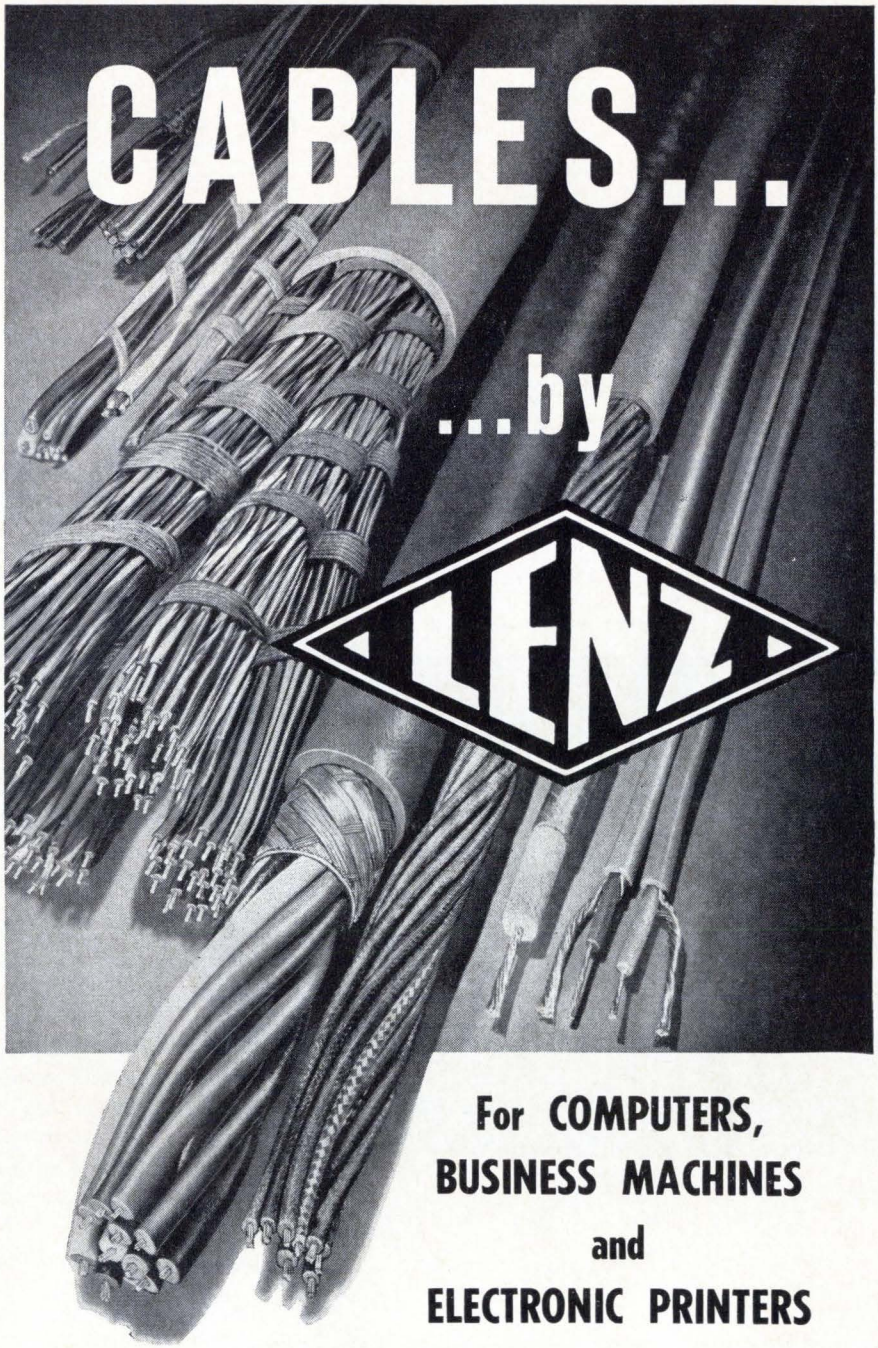
quired about 30 seconds input-to-output time per equation. Comparatively, to compile and calculate the same set of equations using a desk calculator or even a computer that was closely-located (assuming we could gain access to it) often took up to 10 hours of elapsed time.

Since we could quickly process these short programs, we found we could extend computational conditions to determine parameters over a wider range of variables, as one example. The new system also enabled us to spot check large program results; that is, to isolate segments of lengthy equations and recompute them for purposes of accuracy and possible improvement through variation in condition.

QUIKTRAN also incorporates the ability to construct large computational programs in segments. This aids the programmer constructing a program too large, in space or time, to adapt to QUIKTRAN. By using sample rather than actual data initially, the engineer can key in his equations on the 1050, segment by segment, and check each of them for accuracy. Once these segments are completed and checked out, he can then fill in actual operating data and process the whole program in one continuous operation using conventional computer facilities.

When a FORTRAN program such as this includes, perhaps, three or four sub-programs, each of which embodies numerous sub-statements, it can be readily seen how advantageous is the rapid turn-around time afforded by the new system. While building large programs in segments — even with QUIKTRAN — is no simple matter, there are definite advantages over other methods.

A final advantage is the ease with which an engineer can build sets of programs and maintain them on disk file for later use. These are executive routines (not sub-routines) which can be used to perform familiar functions such as plotting. By first building his set of programs, and entering them in a disk file, the engineer can enter applicable operating data at a later date, compute the problem, and see, for example, his finished formula roughly plotted on the 1050 terminal. END



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CIRCLE NO. 26 ON INQUIRY CARD

The Variable-Threshold

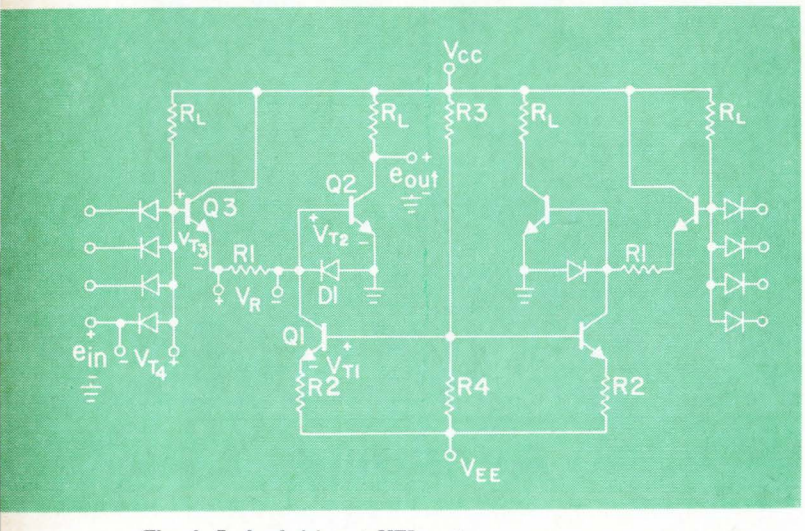

Fig. 1 A dual 4-input VTL gate.

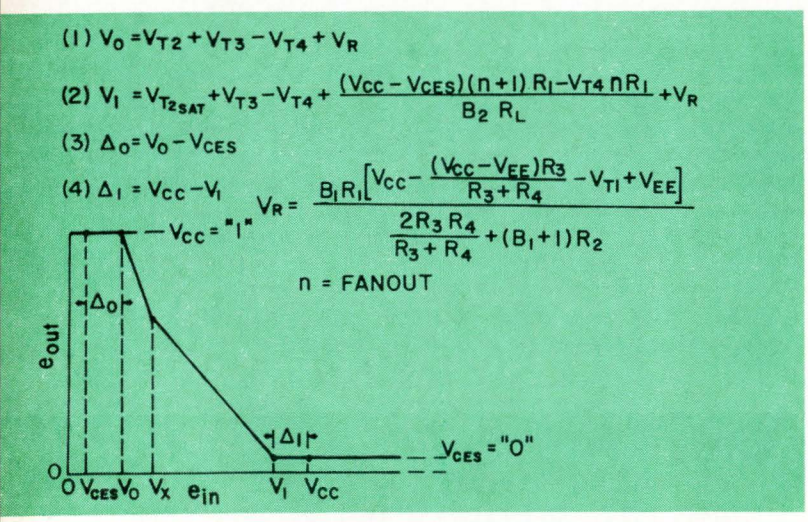

Fig. 2 Voltage-transfer characteristics of the dual 4-input VTL gate.

New Integrated Circuit Approach Results in Outstanding Noise-Rejection Capabilities and High-Temperature Stability

A need for an integrated circuit logic family with greater noise immunity than is presently available has resulted in the conception and development of Variable-Threshold Logic (VTL). This concept is unique in that the input-threshold voltage of the circuit can be adjusted over a wide range (2v to 5v) by adjusting an appropriate external-bias potential. In addition, the threshold of the circuit is relatively insensitive to temperature, a limitation of more conventional DTL circuits.

VTL building blocks can be utilized in peripheral equipment where long signal lines and ground lines are necessary to connect from one piece of equipment to another. These long signal lines and ground lines are very susceptible to noise signals through capacitive coupling and inductive crosstalk. This type of noise makes it necessary to have a considerable amount of filtering and shielding for the presently available integrated-circuit logic families. VTL will greatly alleviate the problems involved with this type of noise. In noisy external environments (such as near-high voltage clicking relays or punch tape readers or writers), VTL building blocks can be utilized because of their extended noise-rejection capabilities.

The VTL Gate

The schematic for a dual 4-input VTL gate which performs a NAND/NOR logic function is shown in Fig. 1. The variable-threshold gate is actually a modified conventional 2-offset diode transistor logic gate. One of the offset diodes and the pull-down resistor for the output inverter in the diode-transistor logic gate have

RICHARD A. GISSELL,
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Logic Concept

been exchanged for a voltage-dropping resistor and a current-source transistor, respectively, in the variable-threshold logic gate. A current-source transistor, Q_1, provides a current through R_1 which establishes a predetermined voltage drop (V_R) across R_1. This current can be adjusted by the use of the external-bias potential supply, V_{EE}. The input-threshold voltage to the gate is equal to the voltage drop across the resistor, R_1, plus one diode voltage drop (V_T). To provide for symmetrical, signal-line, noise immunity the power supplies, V_{CC} and V_{EE}, are made equal to each other. When resistor R_1 is made equal to R_2 the input-threshold voltage to the circuit is relatively insensitive to temperature because all diodes are temperature-compensated.

The diode D_1 is necessary for two reasons: to prevent the current-source transistor from saturating when the input voltage is low when operating with high logic swings; and to prevent the emitter-base junction of the output inverter from breaking down when operating with high logic swings. The diode D_1 is actually the collector — substrate diode for the current-source transistor. By connecting the substrate (P-type) of the monolithic chip to ground, the collector-substrate diode is utilized as a circuit element eliminating the need for including an additional diode plus an additional isolation area in a monolithic chip.

The current-source transistor Q_1 not only provides the current to establish the input-threshold voltage for the gate, but also provides an ample turn-off current for the output inverter when the input voltage is low. When there is symmetrical signal line noise immunity ($V_{CC} = V_{EE}$), the turn-off drive for the output inverter is equal to the turn-on drive.

Transfer Characteristics

To understand fully the noise-rejection capabilities of the VTL gate it is necessary to examine the voltage-transfer characteristics of the gate using piecewise linear-breakpoint analysis. Fig. 2 shows the voltage-transfer characteristics E_{in} vs. E_{out} of the gate. As the input voltage is moved positive, the first breakpoint occurs when the output inverter begins to conduct. This point is defined as V_0. As the input voltage is increased to V_X, the output load gate diodes begin conducting, thereby decreasing the voltage gain of the gate. The last breakpoint occurs when the input voltage reaches V_1; this is the point at which the output inverter goes into hard saturation. Equation 1, in Fig. 2, shows the V_0 input level defined in terms of the circuit parameters. As can be seen from this equation, if $R_1 = R_2$ for all practical purposes, all the diodes will have been temperature-compensated. Input level V_1 is defined in terms of the circuit parameters in Equation 2, shown in Fig. 2. An additional temperature dependent term is associated with the β dependent term of the output inverter Q_2 when the gate is subjected to fan-out loading. This term causes the V_1 voltage to move more positive with decreasing temperature thereby decreasing the logical "1" noise margin.

The dc noise margins of the gate with respect to the logical "0" and the logical "1" levels are defined as $\triangle_0$ and $\triangle_1$, respectively. They are shown in Equations 3 and 4 in Fig. 2.

For the output voltages to be essentially equal to half the power-supply voltage, $\frac{V_{CC}}{2}$, when the input voltage $= \frac{V_{CC}}{2}$, V_0 is designed nominally to be less than $\frac{V_{CC}}{2}$ to compensate for the finite slope of the transfer characteristics while the output inverter is in the active region (voltage-gain region of the gate). V_0 is also designed to insure that the minimum dc noise margins with respect to the logical "1" and "0" levels are essentially equal under worst-case conditions.

Fig. 3 shows the voltage-transfer characteristics of a 4v conventional two offset-diode-transistor logic gate and also the voltage-transfer characteristic of a 4v-logic swing, VTL gate. Both have a fan-out of 5. These characteristics are shown over the entire operating range from −55C to 125C. Note that the

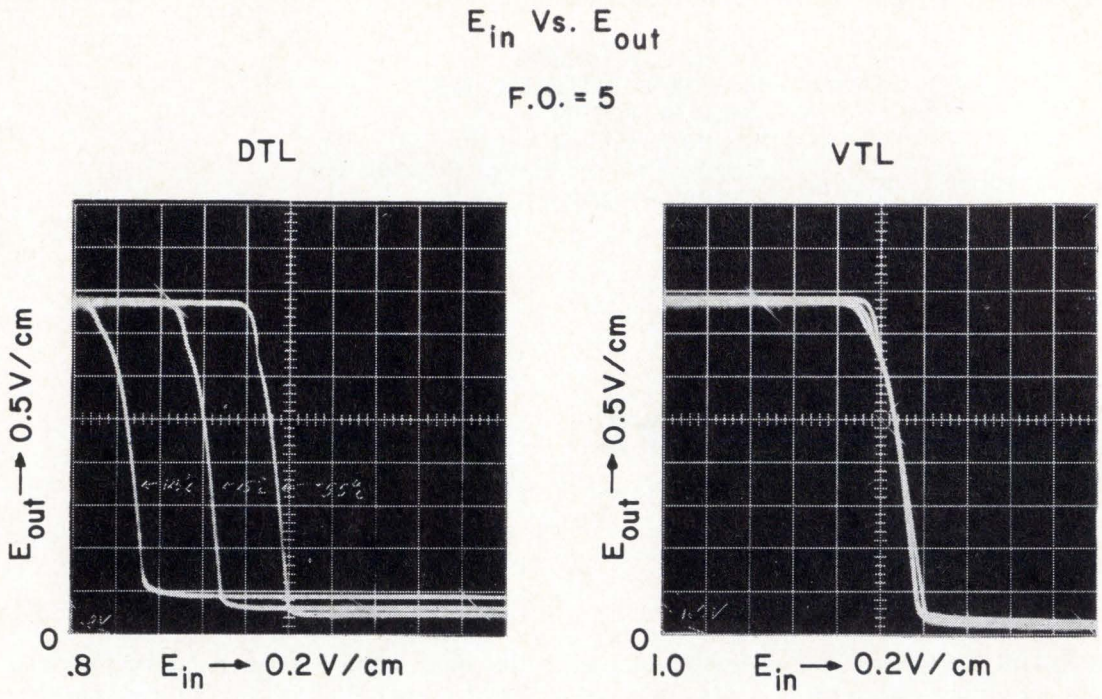

Fig. 3 Comparison of the voltage-transfer characteristics of a 4-volt conventional two-offset DTL gate with those of a 4-volt logic swing VTL gate.

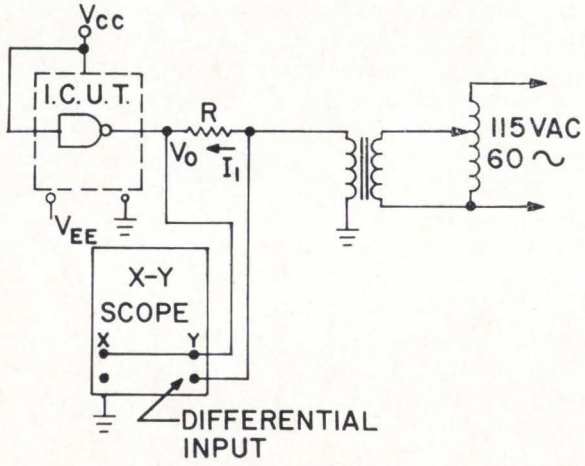

Fig. 4 Test setup for measurement of I_1 vs. V_0.

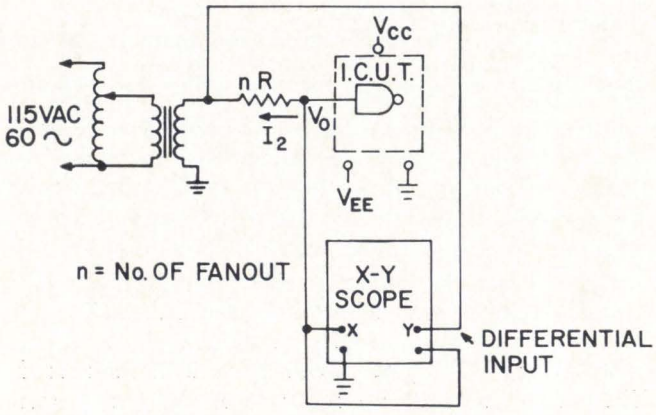

Fig. 5 Test setup for measurement of I_2 vs. V_0.

threshold voltage of the VTL gate has remained insensitive to temperature while that of the DTL gate has moved more positive 3.6 mv per °C with increasing temperature. This is because the DTL gate has two uncompensated diodes.

Signal-Line Noise Margins

The following black-box characteristic approach was used to determine the Δ_0 immunity margin of the VTL gate. First, the output characteristics were measured as shown in Fig. 4. With a logical "1" applied to the input, the output inverter is saturated. With the gate in this stage, the output characteristics show the value of $V_{C(sat)}$ (logical "0" level) as a function of the output sink current. In a logic chain, this sink current is actually the current received from the fan-out gates. Therefore, the input characteristics should be measured with the resistor (Fig. 5) equal to N×R, where N equals the number of fan-outs. If the input characteristics (using negative I_N) are superimposed on the output characteristics, the intersection of the characteristics will determine the operating point (logical "0") of the gate for that particular fan-out. Fig. 5 shows the input-characteristic test setup for determining the logical "0" operating point of the gate. As N is varied from 1 to 5, a family of input characteristics will be generated. This family of characteristics can now be superimposed upon the output characteristics to determine the logical "0" operating point for that particular fan-out condition. These operating points can now be laid off on the voltage transfer characteristics of a gate subjected to the same fan-out condi-

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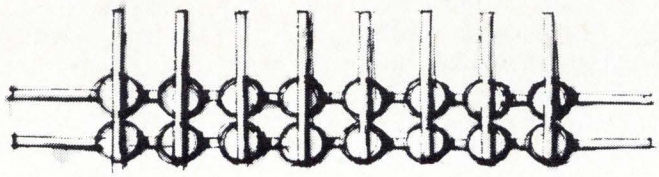

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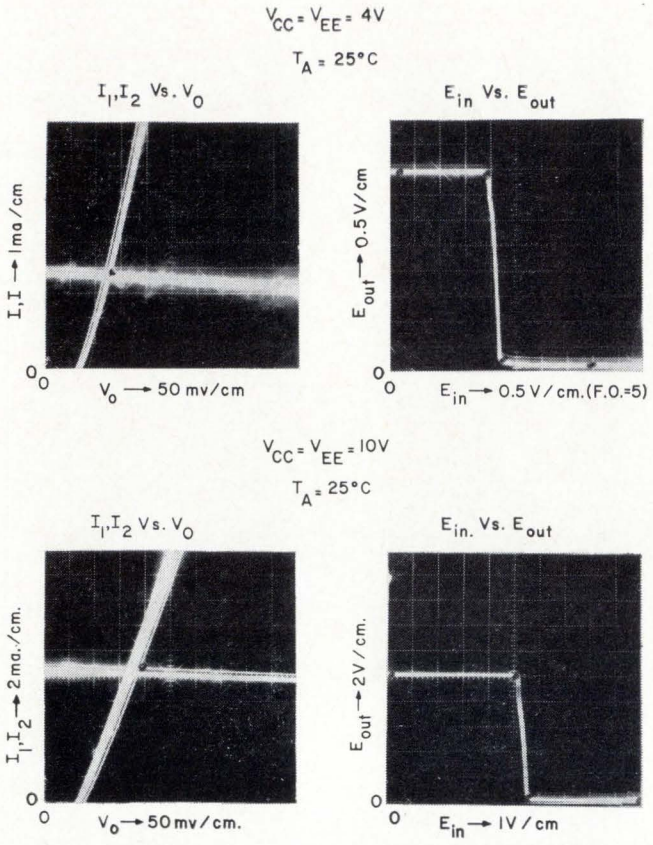

Fig. 6 Black-box characteristics of ten VTL gates subjected to a fan-out of 5 for a 4- and 10-volt logic swing.

tion. By doing this, we can determine the Δ_0 dc noise margin for the gate. The advantage of this technique is the stability to determine the worst Δ_D noise immunity from a distribution of gates with a minimum amount of testing.

Fig. 6 shows the black-box characteristics of ten VTL gates subjected to a fan-out of 5 for a 4 and 10v logic swing. The input characteristics are superimposed on the output characteristics. The intersection of these characteristics are then laid off on the voltage-transfer characteristic curve at the right. Using this technique, the Δ_0 (Fig. 7) and Δ_1 (Fig. 8) dc noise margins of the gate have been determined over the entire operating range for logic swings of 4, 7, and 10 volts. The slight decrease in the Δ_0 noise margin with increasing temperature is because the saturation voltage of the output inverter goes up with increasing temperature. The Δ_1 noise margin decreases with decreasing temperature because the β of the output inverter decreases with decreasing temperature causing V_1 to move more positive with decreasing temperature.

Ground-Line Noise Margins

So far, the signal-line noise margins of the gate have been discussed; however, in a logic system the ground noise margin of the logic blocks has to be considered also. The ground noise margin of the VTL gate was determined with all the inputs tied to a logical "1", and

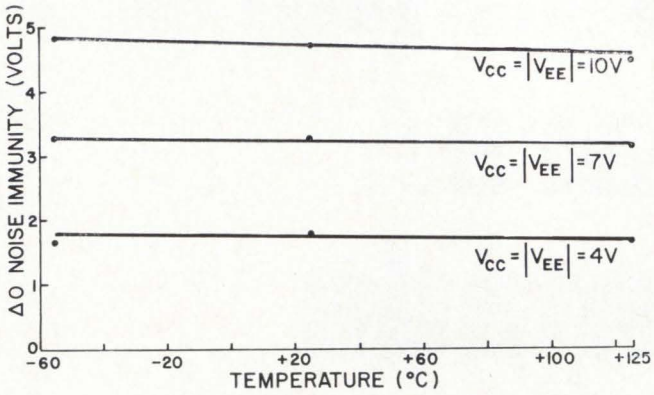

Fig. 7 Typical Δ_0 noise immunity vs. temperature for VTL gate.

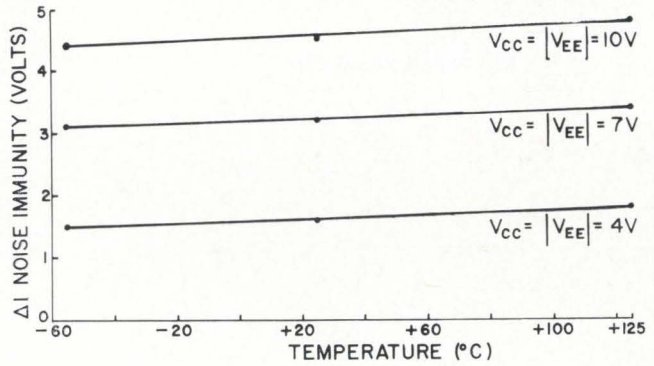

Fig. 8 Typical Δ_1 noise immunity vs. temperature for VTL gate.

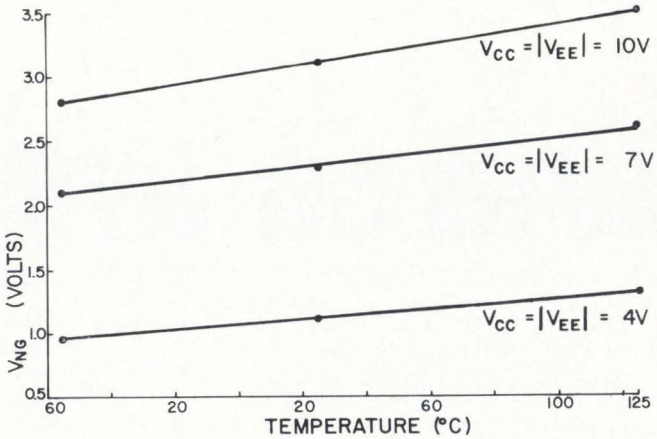

Fig. 9 Ground-line noise margins vs. temperature for VTL gate.

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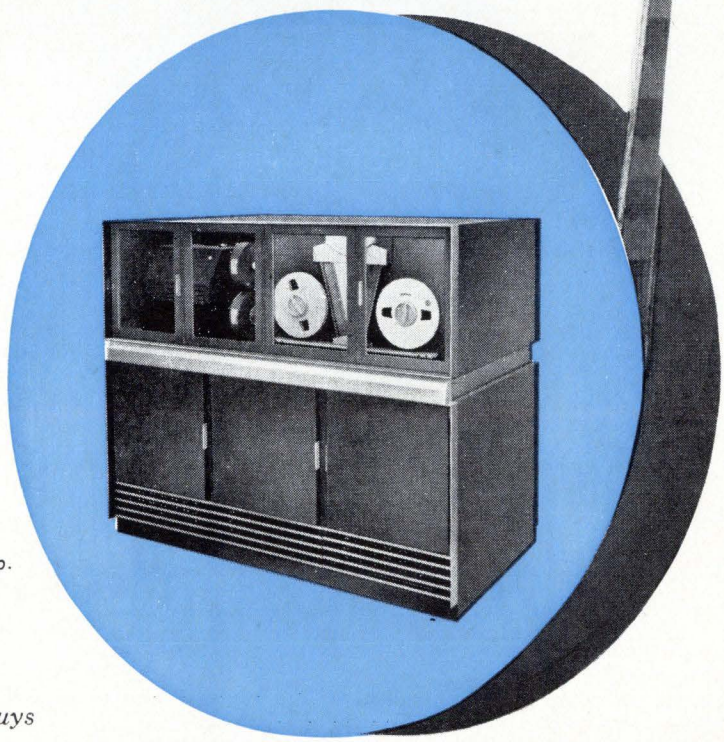

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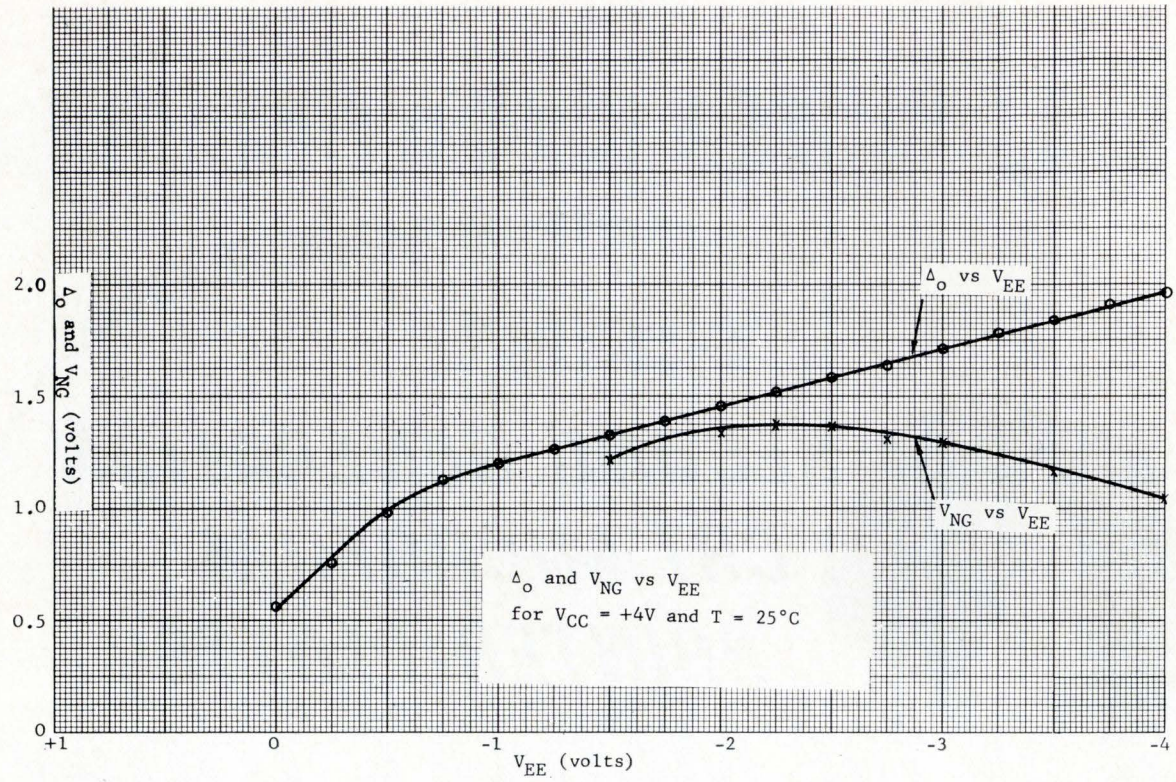

Fig. 10 VTL signal-line noise margin $\triangle_0$ and ground-line noise margin V_{NG} as functions of V_{EE}.

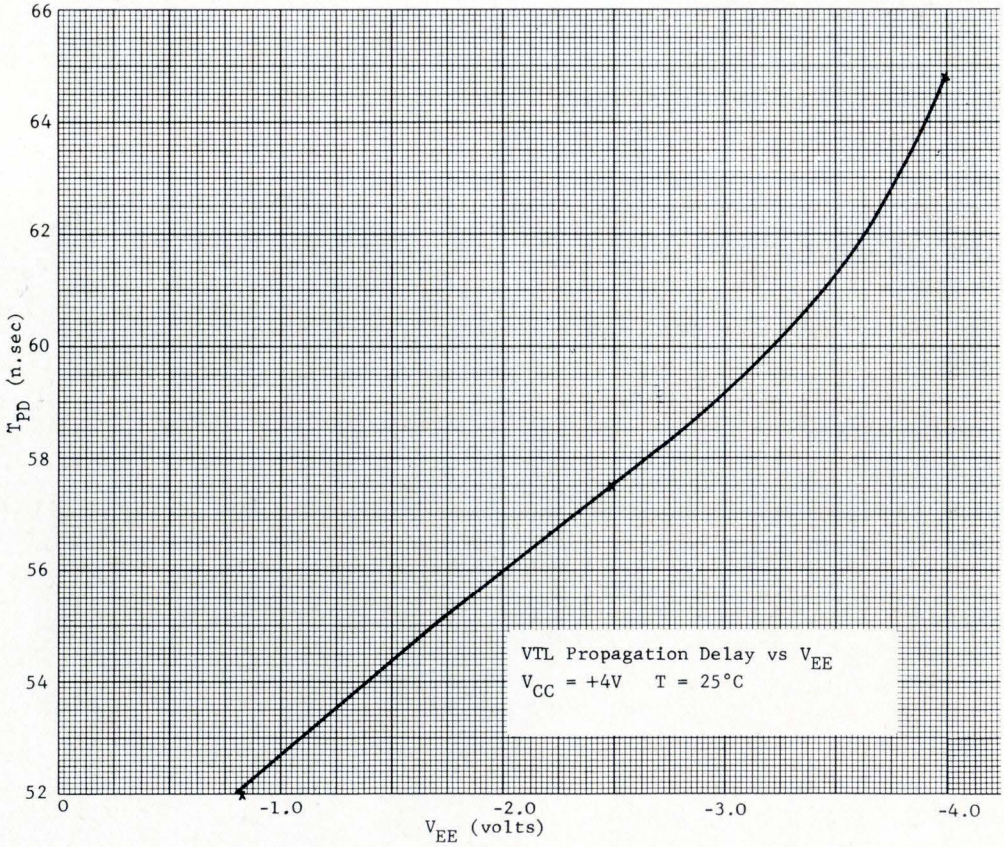

Fig. 11 The effects of bias-supply voltage V_{EE} on VTL propagation delay.

the output level at a logical "0". The ground-line voltage was then varied, and the output voltage monitored on an X-Y oscilloscope. Using this technique the ground-line noise margins of the gate were determined for the entire operating range as shown in Fig. 9. Note that the ground-line noise margins are considerably less than that of either the Δ_0 or Δ_1 signal-line noise margins for the gate. The ground-line noise margins decrease with a decrease in temperature because the β of the output inverter decreases with decreasing temperature.

By driving the bias-supply voltage V_{EE} more positive, the ground-line noise immunity can be improved at the expense of some Δ_0 signal-line noise immunity

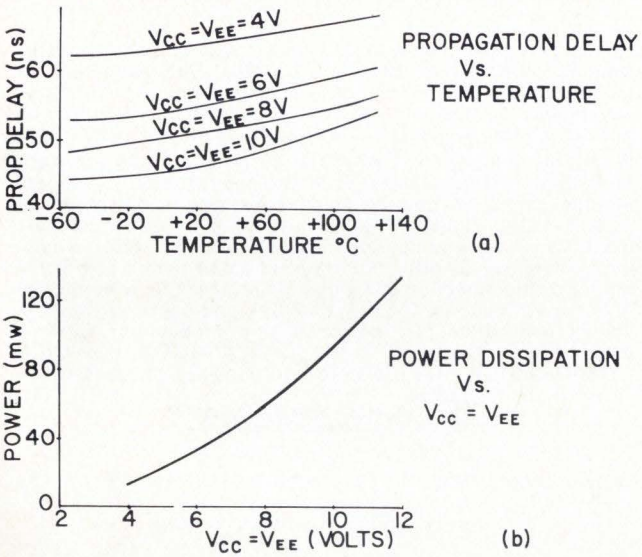

Fig. 12 Average VTL propagation delay vs. temperature and average VTL power dissipation vs. supply voltage.

as the threshold voltage is made closer to the logical "0" level of the gate. By decreasing the V_{EE} supply, the on-drive to the output inverter is increased, thereby increasing the ground noise immunity and fan-out capability.

By decreasing the V_{EE} supply, the power consumption of the gate is decreased because of the lower current drain on the V_{EE} supply. Because the turn-off drive is more than necessary when $V_{CC} = V_{EE}$, an improvement in propagation delay results by decreasing V_{EE} for two reasons.

- Better turn-on time due to increased on-drive.
- A lower threshold voltage resulting in a faster turn-off time because of the slow rising waveform.

Fig. 10 shows the plot of Δ_0 and V_{NG} vs. V_{EE} for $V_{CC} = 4v$, at +25C. V_{EE} is seen to be $-2.5v$ for the maximum ground-noise immunity operating points. Using the same technique, V_{EE} optimum was determined for $V_{CC} = 7$ and 10v as $-5.5v$ and $-7.5v$, respectively.

The effects of the bias-supply voltage V_{EE} on the propagation delay are plotted in Fig. 11. Note that the

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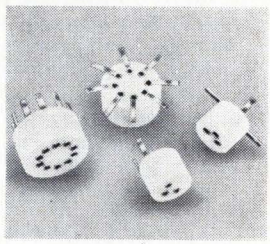

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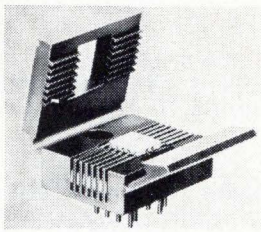

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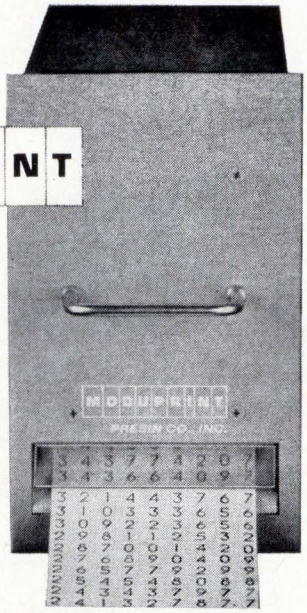

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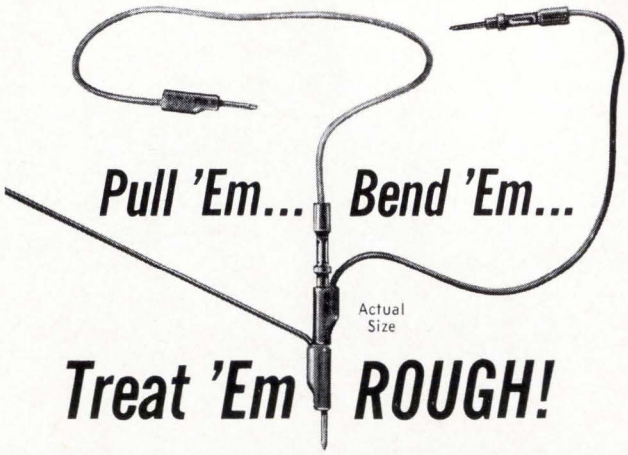

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Noise Immunity: VTL vs. DTL

The noise immunity properties of a 2 offset-diode, DTL gate are compared to those of a VTL gate with 4-volt-logic swing in Table 1. Note that the signal-line noise immunity of the VTL gate is greater than that

Table 1 • Comparison of Noise Immunity

DTL GATE			VTL GATE		
SIGNAL LINE NOISE IMMUNITY					
(VOLTS)			(VOLTS)		
−55°C	+25°C	+125°C	−55°C	+25°C	+125°C
1.4	1.0	0.5	1.9	1.8	1.7
GROUND NOISE IMMUNITY					
0.8	0.9	0.4	0.95	1.1	1.3

of the DTL gate over the entire operating range. Note the decrease in signal-line noise immunity of the DTL gate at high temperature. This is because the input-threshold voltage is moving more negative and the $V_{C(sat)}$ is moving more positive with the increase in temperature. They are, therefore, approaching each other, and the Δ_0 noise margin is decreasing. The only variation in the VTL gate Δ_0 signal-line margin is because the $V_{C(sat)}$ level is moving up with an increase in temperature.

Note that the ground-line margin of the VTL gate is greater than that of the DTL gate at both hot and cold temperature. At −55C, the ground-line noise margin in the DTL gate decreases because the output inverter on-drive has decreased, thereby causing a decrease in the gain of the gate, whereas in the VTL gate the on-drive to the output inverter is essentially constant over the entire operating range. At 125C, the DTL ground-noise margin decreases because the saturation voltage is moving positive and the threshold voltage is moving negative.

Pulse Noise Margins

In a logic system, the pulse noise margins of a gate are of prime importance rather than the dc noise margins. Pulse noise margins have been determined and are greater than the dc noise margins in all cases.

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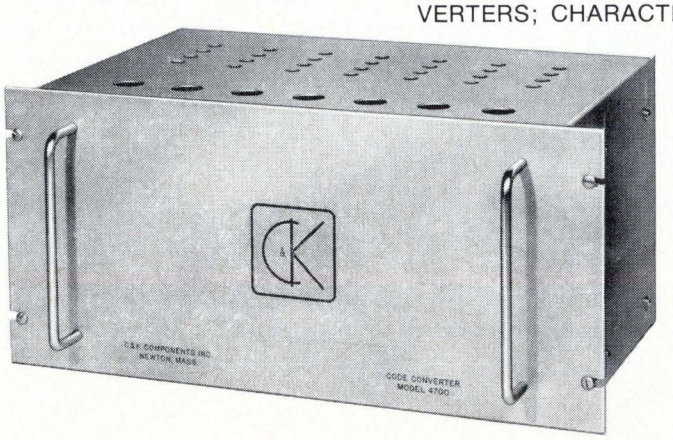

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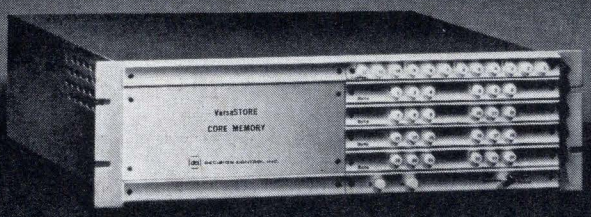

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the VTL gate was measured in a 5-bit ring oscillator for 4v, 7v, and 10v logic swings. These results are shown in Fig 12(a). Shown in Fig. 12(b) is the average power dissipation for a VTL gate as a function of supply voltage $V_{CC} = V_{EE}$.

Other VTL Circuits

Also designed for the VTL family is a gated R-S flip-flop, shown in Fig. 13. The gated R-S flip-flop is essentially the same as that of the dual gate except for the addition of two extra emitter-followers and voltage-dropping resistors and an input-diode cluster for the set and reset inputs. The additional input emitter-followers are necessary to prevent the input

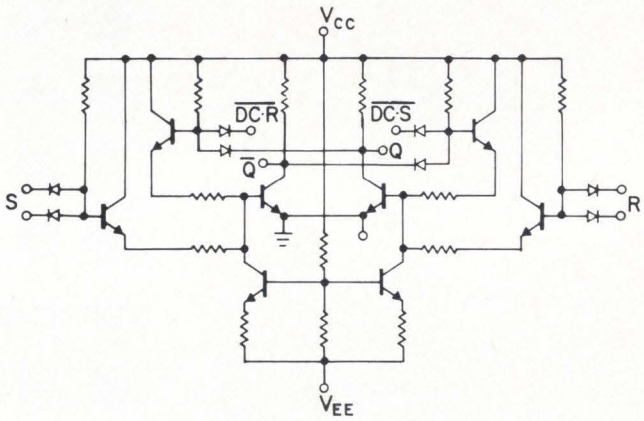


Fig. 13 A VTL R-S flip-flop.

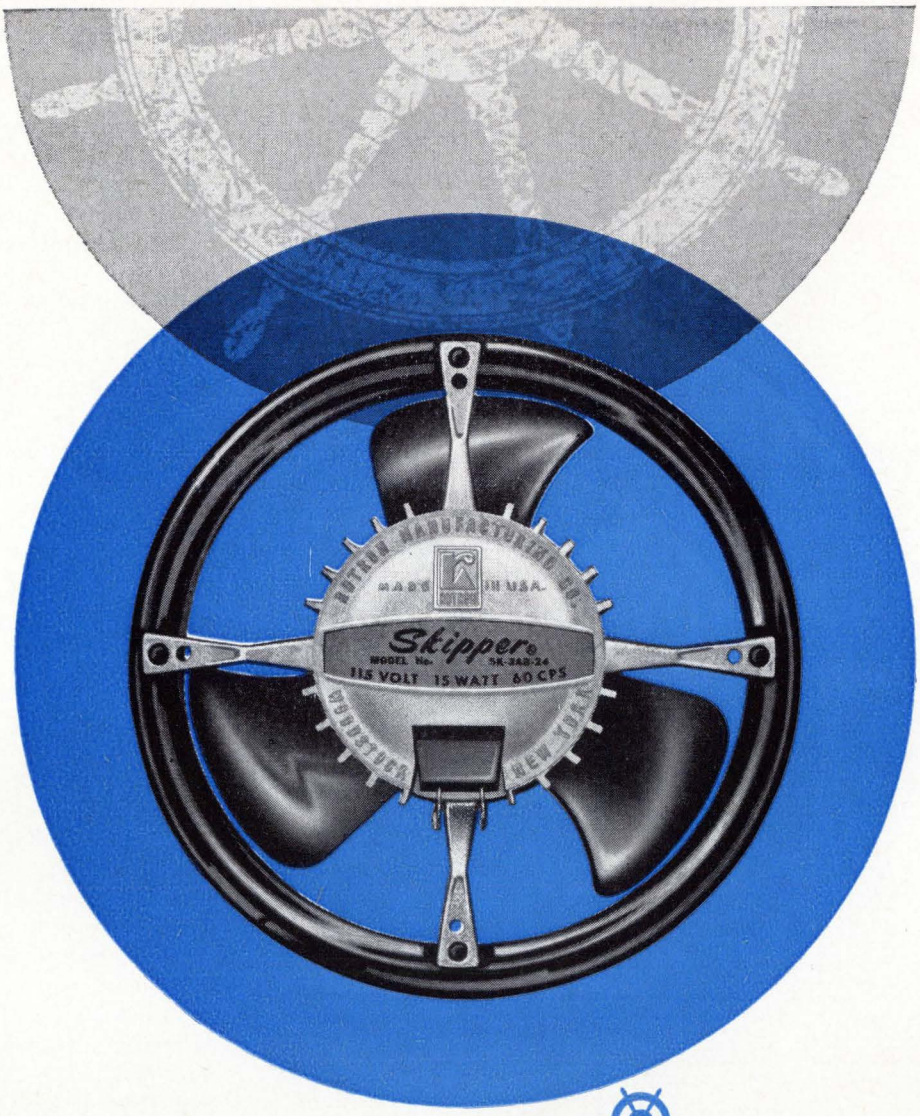
emitter-follower from breaking down if one of the inputs is low and the latch-back is high. The propagation delay of the flip-flop is equal to essentially two gate delays. It will take two of the flip-flops to make a shift-register element. Also designed for the VTL family is a line-driver circuit which exhibits a 10 to 1 decrease in propagation delay over that of the gate when driving a 100 pf output-capacitance; and a power gate with a fan-out capability of 20.

Conclusions

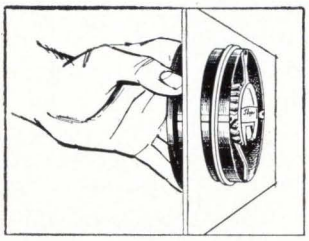
Equipment designs requiring integrated logic circuits to operate in high-noise environments can be better realized by new circuit approaches. While presently available logic circuits can be designed-in by proper packaging and shielding, variable-threshold logic represents probably the first integrated circuit solution to extending the noise-rejection capabilities of logic circuit building blocks.

Three VTL circuits were introduced by Motorola at the recent Wescon Show. They are a dual 3-input gate, a dual 4-input gate, and an R-S flip-flop.

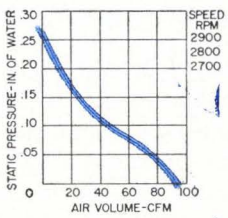
Circle No. 103 on Inquiry Card



You can buy the amazing new *Skipper* for less than $4.00 in quantities!



- Time and money saving installation—just cut out hole for fan and slide neoprene rubber mounting ring over venturi—and the Skipper is instantly secured in position. No mounting holes to drill... no nuts and bolts to handle.
- Complete selection of matching accessories available—line cord and plug, finger guards, etc.
- Styling and reliability—unmistakably ROTRON.
- Designed to meet U.L. Approval.
- Impedance Protected.
- And it's quiet! Only 39 db SIL.
- Constructed of unbreakable polymer and die cast aluminum.
- Built-in heat sink for cool running motor and longer life.
- For operation at ambient temperatures up to 140°F (60°C).
- Measures just 5¼" in diameter by only 1 13/16" in depth.
- Just 5/6 lb.—lightweight.
- Alternate mounting arrangements.
- Mounts easily anywhere—on any panel thickness (even glass).
- Available in 115V—60CPS-1ϕ (other ratings available).



Write, wire or call today for complete details to . . .

ROTRON MANUFACTURING COMPANY, INC.
WOODSTOCK, NEW YORK

West Coast: ROTRON/PACIFIC, Glendale, California
Canada: THE HOOVER CO., LTD., Hamilton, Ontario
Rotron-Vactric Europa (N.V.) Breda, The Netherlands
Export Sales—AURIEMA INTERNATIONAL GROUP

CIRCLE NO. 34 ON INQUIRY CARD

NEW PRODUCTS

PAGE TELEPRINTER

Low-cost page teleprinter in the 3000 word/minute class produces real-time hard copy and is suitable for applications in offices and "decision-making" environments where, up to now, noisy and bulky printers may have precluded such use. The unit utilizes solid-state and integrated circuitry for high reliability, and a new non-burning, current-sensitive paper that requires no processing. Motorola, Inc., Military Electronics Center, Chicago, Ill.

Circle No. 155 on Inquiry Card

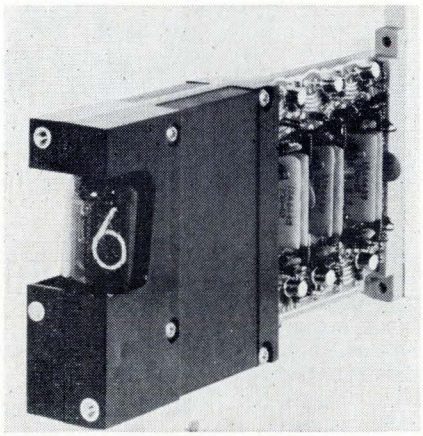
GLASS REED RELAY

Glass reed relay has a 10 watt contact rating (0.5 amp max. and 250 vdc max.) while operating on 28 milliwatts of power. The relay operates in 2 milliseconds, has a contact life of 4 million operations at maximum rating, or 20 million operations at one-quarter maximum rating, and an insulation resistance of 5000 megohms. Dimensions are 1-7/16" long by 29/64" wide by 7/16" high. Lead length is ⅛". Wheelock Signals, Inc., Long Branch, N.J.

Circle No. 170 on Inquiry Card

FORWARD-BACKWARD DECADE COUNTER

High-speed, forward-backward decade counter with latching display counts periodic or aperiodic signals at rates from 0 to 1-mc, in either direction, and provides an indication only after a "latch command" signal has been applied to the input. The unit then displays the decimal count accumulated when the latch command was applied. The display remains unchanged until the next latch command is received. Reversing delay time is less than two microseconds. Typical applications for this building block module include instrumentation systems, machine tool and process control systems, shaft-encoder decoding and many other uses. Either single or dual inputs may be used by simply supplying the proper directional control commands. Since the circuit uses a common, rather than



a ground, the drive signal may have an arbitrary reference level that matches the requirements of a wide variety of standard and non-standard logic control levels. Price is $115.00 in quantities of 55-99. Janus Control Corp., Newton, Mass.

Circle No. 175 on Inquiry Card

HIGH DENSITY CONNECTORS

A new electronic connector with a high density of contacts can be used for center-of-the-board printed circuit applications or panel-mounted. As a panel-mounted plug or receptacle, the unit provides up to 74 contacts in a space 3⅛ by ⅜ inches. For ease of engagement both versions are provided with jackscrews and matching jacksockets. Winchester Electronics, Oakville, Conn.

Circle No. 120 on Inquiry Card

RAPID-ACCESS DISC FILES

Two new rapid-access disc files are said to offer access times and data transfer rates typical of more expensive drum storage units with capacities and costs comparable to conventional disc files. Model RAD 9167 has a maximum storage capacity of 8,388,606 characters, an average access time of 17 milliseconds, and a data transfer rate of 480,000 characters per second. The RAD 9166 has an average access time of 34 milliseconds with a data transfer rate of 60,000 characters per second. Use of fixed read/write heads for every track in the file reduces access time by eliminating the positioning delay associated with conventional movable-arm disc file. Rotational delay is minimized when large blocks of data are transferred through the use of a technique which initiates transfer at the current file location rather than at the beginning of the disc. As an example, this technique reduces the time required to transfer 4096, 24-bit words from computer memory to discs from 50 to 35 milliseconds, a 30 per cent time saving over conventional methods, according to the company. The Model 9166 has a sales price range of $18,500 for 524,288 characters of storage, to $95,000 for 8,388,608 characters; monthly lease prices range from $420 to $2,140 per month. The Model 9167 varies from $23,500 to $100,000, with monthly lease prices from $530 to $2,640. Scientific Data Systems, Los Angeles, Cal.

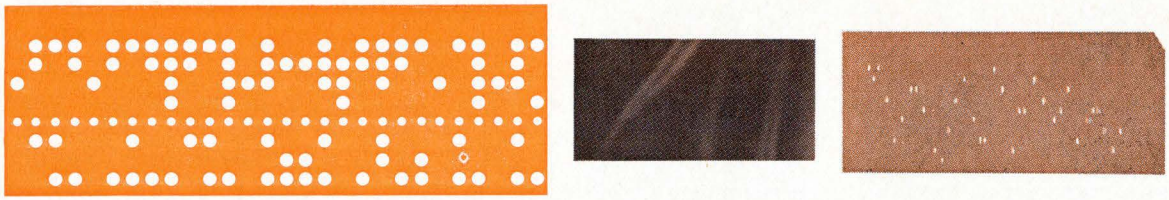
Circle No. 133 on Inquiry Card

THE LOGIC OF IT ALL 5

Fifth in a series of discussions on the advantages of Tally paper tape readers and perforators from the user's point of view.

Topic 5:

Paper tape, magnetic tape or punched cards,



which media should you use?

Choosing the right medium for a given EDP application is primary to optimum data system performance. As the maker of the world's most complete line of perforated tape processing equipment, we wish we could tell you paper tape is the only way to go. However, the problem doesn't lend itself to such a ready solution. In truth, paper tape, magnetic tape, and punched cards all have their place in collecting, storing, and processing data.

Paper tape is the least costly medium, per se. Information is recorded in a non-volatile machine language form on paper, foil, or plastic tape. The message can be of any length. It's visible and will withstand rough handling. Code and formats are compatible with modern computers. Speed range is between cards and mag tape. Cost of equipment for recording, reading, and storage is the lowest of the three media.

Magnetic tape mounted on ordinary reels will handle up to 90,000 characters per second. Information stored on magnetic tape is delicate, volatile, and invisible. Cost of magnetic tape digital data handling equipment is far higher than either paper tape or punched cards. Speed is the big advantage.

Punched cards are the oldest and most widely understood of the three media. Cards have a fixed format which imposes a valuable preparation discipline. Further, they are sortable. These advantages, however, turn out to be a mixed blessing. Sortability is of no advantage in modern computers. Fixed format requires the whole card to be repunched whenever an error occurs.

Fixed record length causes waste in both short and long messages. Short messages fail to use up the card's capacity. Long messages, exceeding 80 character columns, require duplication of indicator information again and again. Cards have a low data density (i.e., they use a lot of space to put the message down). Cards have a low mechanical efficiency in terms of the speed at which they can be processed and the amount of equipment necessary for the task.

Summing up, if your problem is reading data at less than 1,000 characters per second or recording both long and short messages at up to 300 characters per second, paper tape will undoubtedly serve your needs better. If your problem is reading data serially above 1,000 characters per second or writing data serially above 300 characters per second, you should be looking at magnetic tape equipment. If your problem is handling units of recorded data with message lengths less than the capacity of the punched card and you must reorganize data blocks prior to processing, you should consider punched cards.

New Catalog Ready

If you would like to know more about Tally products, we would be pleased to send you our 1965 catalog. Please address Mr. Ken Crawford, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone: (206) MA 4-0760. TWX: (206) 998-0551. In the U.K. and Europe, write our man in London, H. Ulijohn, Manager, Tally Europe Limited, Radnor House, 1272 London Road, London S.W. 16, England.
Phone: POLlards 9199.

TALLY®

CIRCLE NO. 35 ON INQUIRY CARD

NEW PRODUCTS

DISK CAPACITORS

New disk capacitors have "flat bottoms" for manual or automatic insertion in printed circuit boards. They prevent rock or roll on printed circuit boards because they seat perfectly every time and they eliminate electrode exposure. The new configuration permits lower circuit board height without kinked leads as well as complete control of Durez on wire leads. Hi-Q Div., Aerovox Corp., Myrtle Beach, S.C.

Circle No. 176 on Inquiry Card

VACUUM GAUGE DIGITIZER

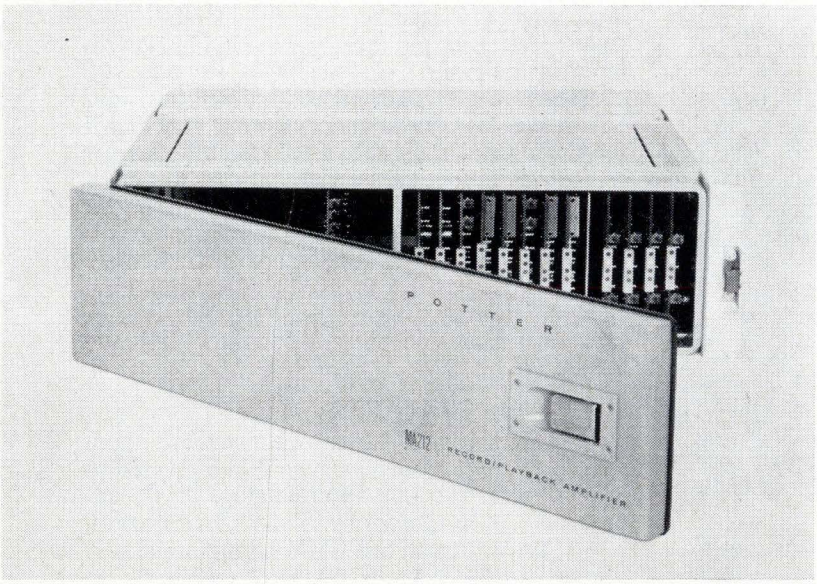
Digital converter repetitively scans and digitizes the read-out of a molecular vacuum gauge. Pressure range is 1 micron to 20 millimeters of mercury. Output format is 2-4-2-1 BCD. These digital converters are similarly applied to all types of dial-pointer instruments, 3 inch to 20 inch diameters. Photo-optic sensing of pointer angular position is accurate to 0.1 degrees of arc. Various outputs available for compatibility with visual display, computer, printer, tape punch, etc. Sampling rates from 1 to 600 per minute. Discon Corp., Ft. Lauderdale, Fla.

Circle No. 129 on Inquiry Card

SYSTEMS COMPUTER

A high-speed, general-purpose stored program machine features bit-oriented logic which greatly simplifies maintenance and provides a variable word size design. Designated the DATA 620, the 4096 word 16 bit machine requires only 21 inches of standard rack space. The front panel displays and provides control for all registers simultaneously. While designed as a system component, the DATA 620 is said to be a very powerful computer in its own right. Memory cycle time is 1.8 microseconds; add time is 3.6 microseconds. The DATA 620 design is highly input/output-oriented, and is designed to be integrated into any system. Virtually any type of peripheral equipment may be used with the computer through the use of standardized interface logic. A wide range of multiplexing and analog/digital interfacing is available for hybrid applications. A 4096 word, 16-bit word size computer is priced at $26,000. Data Machines, Inc., Newport Beach, Cal.

Circle No. 188 on Inquiry Card



READ/WRITE AMPLIFIER

Multi-speed read/write amplifier for use with digital magnetic tape transport systems is IBM 7-9 channel (self-clocking) or 8-channel (center clock) compatible unit and can also be adapted for 9 channels (IBM 360 and ASCII compatible). Eight- and sixteen-channel internally strobed or clocked systems are also available. The MA212 amplifier, offered for 200 bpi and skew compensated for 200/556/800 bpi, is designed to operate with tape transports in speed ranges between 2 and 120 ips (up to 96 kc). Any of four speeds can be selected. Simultaneous write/read can be used above 12 ips. Input circuit drive requirement is 1.5 ma. Output circuits are short-circuit-proof and drive load currents are up to ±20ma. Potter Instr. Co., Inc., Plainview, N.Y.

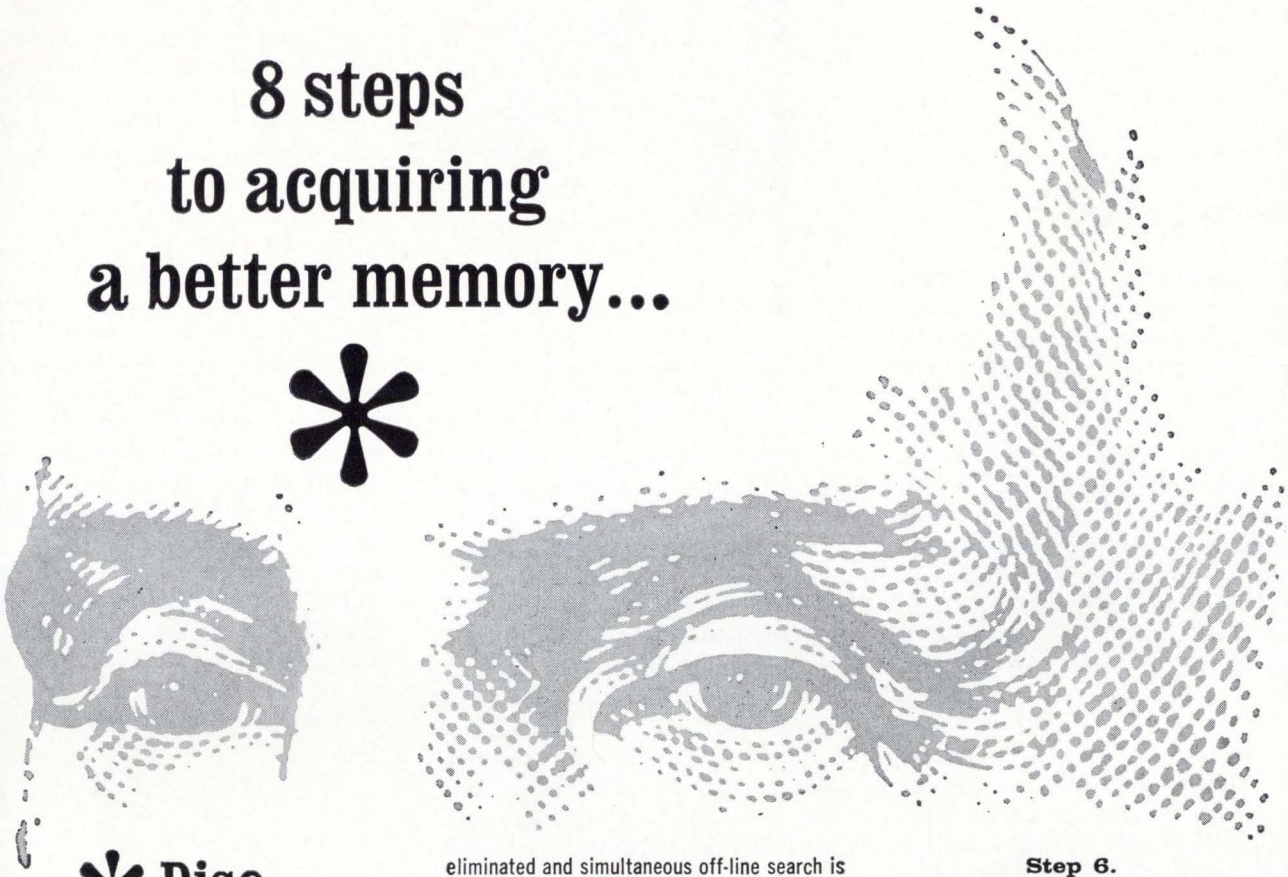
Circle No. 169 on Inquiry Card

HIGH-SPEED SWITCHING TRANSISTOR

A new npn diffused-silicon planar epitaxial device, type 2N3862, has been developed to fill the need for a high-performance, universal saturated switching transistor. The new unit is said to provide a unique combination of characteristics, including a high-speed switching $t_s \leq$ 10 nsec at 10/10/10; a high current switching $t_{off} \leq$ 30 nsec at 200 ma, ckt $\beta = 10$; high current saturation voltages $V_{CE} \leq 0.7V$ at 200 ma/20 ma; high frequency response $f_T \geq 600$ mc; and a high voltage $V_{CEO} \geq 20$ volts at 10 ma. The unit is said to perform effectively as a universal switching transistor, suitable for both logic and high-speed memory applications in a broad variety of computer and data processing systems. Price, in 100-199 quantities, is $4.60. Transitron Electronic Corp., Wakefield, Mass.

Circle No. 154 on Inquiry Card

8 steps to acquiring a better memory...



* Disc mass memory, that is.

For "time-sharing" and other applications where various computer systems must draw upon one large-capacity, central memory file designed for continuous and virtually instantaneous information processing, the LIBRAFILE 4800 mass memory produced by Librascope Group of General Precision, Inc., offers many remarkable new features. Consider the following before you buy or specify:

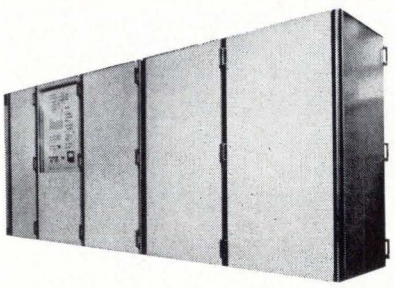
Step 1. Consider Capacity:
Where an extremely large amount of data must be stored, the memory element of the LIBRAFILE 4800 has an initial capacity of 400 million bits of information with expansion capability to 6.4 billion bits on a single trunk line.

Step 2. Inquire About Access and "Time Sharing":
The technique of information retrieval used by the random-access 4800 is either fixed-address or record-content search, depending on the master-control electronics used. Average access time is 35 milliseconds. Search by record-content is an exclusive technique that permits any desired field to be used as the access key so that where the data is stored need not be known; only what information is needed. Costly flagging and table look-up are eliminated and simultaneous off-line search is permitted. The 4800 can be easily incorporated into time-sharing computer networks.

Step 3. Consider Flexibility:
The LIBRAFILE 4800 mass memory can be used with any data processing system, whether already in use or scheduled to be installed in the future to provide faster, more accurate, more reliable operation with greater storage capacity.

Step 4. Inquire About High Transfer Rates:
The Series 4800 disc files can be organized to transfer data at rates from 1 million up to 160 million bits per second. This is accomplished through multiple-head read/write operations. (The 4800 discs have one head for every data track.) Through adaptation of special electronics, data rates approaching 1 billion bits per second are possible for special applications.

Step 5. Ask About The Manufacturer's Experience:
Behind the LIBRAFILE 4800 mass memory is the extensive background and 28-year history of Librascope Group of General Precision, Inc., in computer equipment and components.



Step 6. Check The Equipment's Performance Record:
LIBRAFILE 4800 mass memories are a key part of a General Precision/Librascope data processing system in Headquarters USAF's 473L command-and-control system in the Air Force Command Post at the Pentagon. More than a million headbar hours have been logged without a single head-bar failure. And, a scheduled installation for a scientific laboratory will provide a common data base for eight powerful computers, enabling many scientists and engineers to "share" the system on virtually a simultaneous basis. The 4800, in this instance, will help replace magnetic-tape equipment twelve times more costly and which must now be manually monitored to provide the data base.

Step 7. Request Detailed Information:
Write today for our brochure showing applications, typical configurations, and complete specifications.

Step 8. Call or Write Us:
The quickest and surest way to acquire a better memory (a LIBRAFILE 4800 mass memory) is to contact our Marketing Department. The address is shown below.

SYSTEMS DIVISION
GENERAL PRECISION INC.
LIBRASCOPE GROUP
808 Western Ave Glendale 1, Calif.
Phone: (213) 245-8711

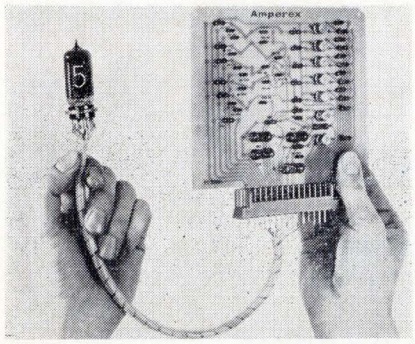
CIRCLE NO. 36 ON INQUIRY CARD

NEW PRODUCTS

TIME CODE GENERATOR

Time code generator unit generates time code formats for use in magnetic tape analog recording systems, telemetry systems, range-timing systems, and other real-time data acquisition systems. Among the time code formats which can be furnished are IRIG-A, B, C, D, and E; NASA-36 and 28-bit; and AMR D-5. Each time code generator provides a modulated carrier time code output, a level-shift time code output, a parallel digital output of the time to 0.1 milliseconds, and pulse rate outputs. Use of the unit allows analog data to be recorded on magnetic tape, oscillographs, or strip chart recorders. Digital data systems can be precisely correlated on a time basis. Internal time base of generators has a stability of one part in 10^8 per day. Chrono-Log, Broomall, Pa.

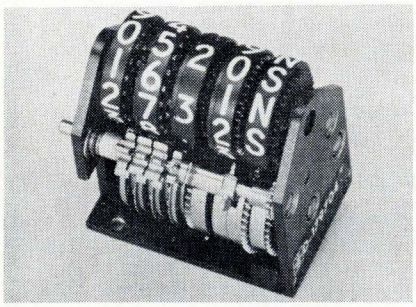
Circle No. 177 on Inquiry Card



DECODING/READOUT SYSTEM

A solid-state conversion matrix for decoding BCD codes and a biquinary numerical indicator tube are combined to provide a decoding/readout system that uses approximately 50% fewer components in the conversion matrix and 30% fewer transistors to drive the tube, according to company reports. The "Bi-Qui" tube itself is said to provide an additional advantage with its built-in error detection capability. Any failure will be visible because two numerals within one tube will simultaneously ignite. The board and tube come ready to use and need only a standard connector and socket. Amperex Electronic Corp., Hicksville, L. I., N. Y.

Circle No. 145 on Inquiry Card



REVERSING COUNTERS

A new reversing counter which functions as two counters in the space of one features a unique rotary reversing mechanism which smoothly reverses the direction of the counter wheels at a predetermined point while input shaft rotation is maintained in one direction. This is accomplished by means of a precision gear-driven differential mechanism which reverses the counter at the exact point desired with no lost counts. This new design is said to permit either a reduction in panel size or increase in figure size in a display system. The new reversing counters are presently used in a number of aerospace navigational computer systems. In addition, the new reversing counter has applications in numerical control systems for machine tools and two-mode direct readout devices for machine tools. Veeder-Root, Hartford, Conn.

Circle No. 192 on Inquiry Card

DATA TERMINAL EQUIPMENT

New solid-state data terminal communications device is expected to be used widely for real-time computer applications, time-sharing systems, and conventional inter-office data networks. The terminal unit has been designed to be compatible with all major computer systems, incorporating the ability to read and punch paper tape and edge-punch cards while simultaneously producing a printed document and data. The equipment also is designed to accommodate many types of systems, including those where print-out only is required, or just pure data from transmitting-to-receiving stations. Speeds up to 175 words per minute are possible on-line or off-line. The system operates on-line via Data Phone or comparable equipment. Dura Business Machines, Madison Hts., Mich.

Circle No. 165 on Inquiry Card

PUSHBUTTON SWITCHES

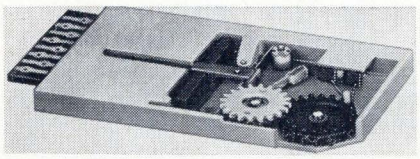
This low-cost, lighted-pushbutton, snap-acting switch is rated at 5 amperes 125 volts a-c or 28 volts d-c. It combines compactness, ease of installation, and wide variety of control and indication, at a cost below that of the separate switch and pilot-light assembly it replaces. Combination of pushbutton switch and indicating lamp mounts in a half-inch-diameter hole and its housing extends less than two inches behind the panel. The ⅜-inch-diameter lighted pushbutton projects 0.291 inch from the panel. Unit is rated at 5 amps, 125 volts ac or 28 volts dc. The switch has single-pole, double-throw contacts, permitting its single pushbutton to control two circuits alternately. The mechanical action is push-on/push-off. The lamp circuit is independent of the switching circuit, hence the lamp can be wired to indicate either ON or OFF, or connected to serve as a warning or indicating signal from other circuits. UNIMAX SWITCH, Wallingford, Conn.

Circle No. 135 on Inquiry Card

QUARTER-RACK SUPPLIES

Quarter-rack power supplies cover three voltage and current ranges — 0-7 vdc at 4 amps, 0-14 vdc at 3 amps, and 0-32 vdc at 1.5 amps. All units feature 0.01% regulation, both load and line, 0.5 mv rms ripple, and 0.05% stability with 0.01% stability optionally available. The supplies include circuits that provide automatic adjustable current limiting to prevent damage to transistors and other circuit components due to inadvertent overloading. In addition, front panel indicator lights signal overload conditions immediately as a secondary precaution. All units are remotely-programmable over their full voltage range without derating and include remote sensing and continuously-adjustable voltage adjustment controls. Price: $189 to $199. Trygon Elect., Inc., Roosevelt, L. I., N. Y.

Circle No. 151 on Inquiry Card

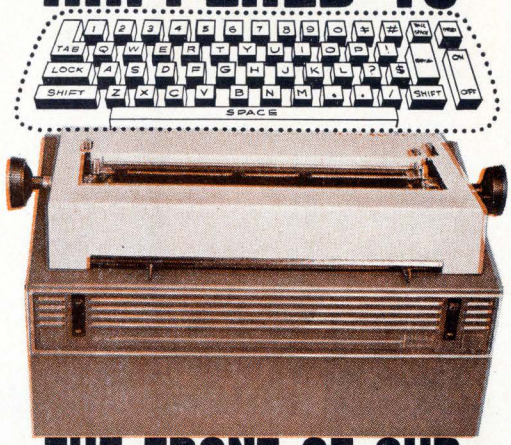


READOUT MODULES

Two new units were designed for count/control systems where a printed readout is necessary. The units are the "Uniprint" module and the "Uniprint" platen. The modules can provide systems with readout combinations of digital numerical data, time data, or manually-advanced calendar designations. The decade build-up permits a maximum of 16 characters on ¼" centers. Count speed for the Uniprint module is 50 counts per second. Printed figure size is 0.14" high by 0.09" wide by 0.015" line thickness. Maximum impact force on the platen is 0.05 lbs. The impact time is 10 msecs. The modules require 24 volt dc ± 10%. A similar module, called "Unicount", provides visual readout where decade build-up is needed without printed or electrical readout. Durant Mfg., Co., Milwaukee, Wisc.

Circle No. 146 on Inquiry Card

LOOK WHAT'S HAPPENED TO



THE FRONT OF OUR DATA PRINTER

(we eliminated the keyboard)

There are now 50% fewer parts. Reliability is increased, operation simplified and maintenance minimized. The Model SP-16 Printer accepts data in six-bit form for printout at a nominal rate of 15.5 characters per second. Carriage remains stationary while the printing element moves across the 13 inch writing line. Printing is accomplished electromechanically using solenoids for selection. Timing disc photoelectrically synchronizes printer to external equipment. Delivery 30 days. Write for SP-16 Printer Bulletin.

Price range $1480 to $1625.

IT'S INVAC FOR ADVANCED PERIPHERAL EQUIPMENT

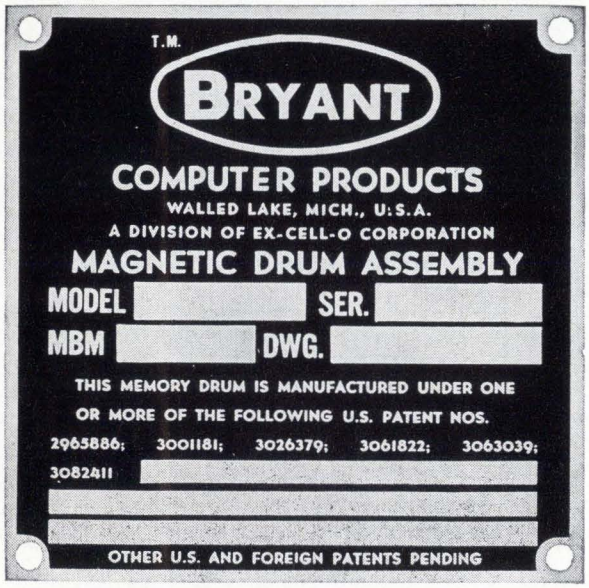
INVAC CORPORATION

26 Fox Road, Waltham, Mass. 02154 Tel. (617) 899-2380

CIRCLE NO. 37 ON INQUIRY CARD

Look for the familiar label.

You'll see it on Bryant Auto-Lift® memory drums being used in all types of E D P systems. Because the unique Auto-Lift fits any computer, it has become commonplace product line equipment with major manufacturers. Just as important, every unit is backed by Bryant's reputation for proven reliability. As the leading independent maker of drum and drum systems, Bryant maintains the best Product Assurance group in the field. It checks equipment from design through production to final acceptance testing. And Bryant's top management makes sure the product meets customer requirements. The whole story is in our free brochure #BCPB-108-5-65. We'll be glad to send it. Meanwhile, keep an eye out for our labels. You won't have to look far.

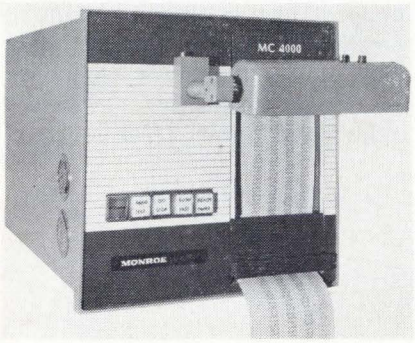


CIRCLE NO. 25 ON INQUIRY CARD

HIGH-SPEED READER/SPOOLER

A new model photocell punched tape reader and matching tape spooler were specifically designed as high-speed input devices. The reader is available in either unidirectional or bidirectional models and operates at speeds to 700 characters per second. The spooler features bidirectional rewind from pushbutton or remote control at 200 inches per second. The unidirectional model RR-702 reader is priced at $1440.00 and the bidirectional model is $1585.00. The model RS-702 spooler is $1495.00. Rheem Electronics, Hawthorne, Cal.

Circle No. 139 on Inquiry Card



DIGITAL PRINTER

High-speed digital printer records 192,000 characters per minute on photo-sensitive paper. It can be used in missile or satellite tracking for a split-second by split-second progress record of the flight path and it can also be tied into the control system of petroleum processing or steel plants to provide continuous or instantaneous recording of processes throughout the facility. Designated the MC 4000, the new unit accepts coded input and converts it to digits or alphabetical characters. These are registered on the head of a cathode ray tube. A fiber optics bundle intensifies this image on the photo-sensitive paper, greatly speeding the printing and creating a clearer copy. It records 100 lines of data per second, without heat, drying, or photo chemicals. Price is $5850. Monroe Data Log Div., Litton Industries, San Francisco, Cal.

Circle No. 140 on Inquiry Card

ELIMINATE PAPER TAPE PROBLEMS WITH
DIGI-STORE® DS-2
MAGNETIC TAPE UNITS

BIDIRECTIONAL . . . ASYNCHRONOUS

- Speeds up to 333 characters per second.
- Operates in either write or read mode—can replace both tape punch and reader.
- Lower initial cost than high-speed punches.
- Handles any code up to 8 levels.
- 8 times more packing density than paper tape—less tape bulk—no chad problems.
- Less tape handling cost — DS-2 tape can be reused **thousands** of times without erasing.
- Compatible with conventional paper tape digital data handling systems.
- Plug-in interface logic available to suit individual requirements.
- High reliability — all-solid-state circuitry — only one main moving part — less downtime — reduced maintenance cost.

WRITE TODAY FOR DS-2 TECHNICAL DATA AND SPECIFICATIONS

TRAK ELECTRONICS COMPANY, INC.
59 Danbury Road • Wilton, Conn.

CIRCLE NO. 38 ON INQUIRY CARD

NEW PRODUCTS

MICROELECTRONIC VOLTAGE CONTROL

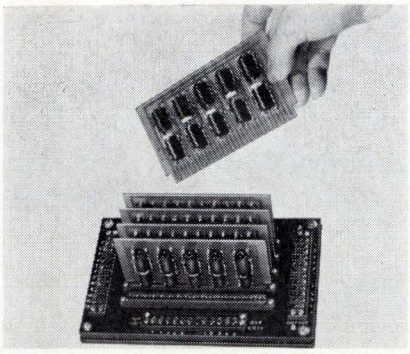
For new microelectronic generation of commercial computers and data processing systems, a unique microelectronic circuit was designed to provide optimum "error-free" performance by rigid control of voltages. The microcircuits precisely regulate, or adjust, the voltages at individual "points of use" throughout the computer and replace bulky and complex conventional systems which control the voltages from a central power source. By "decentralizing" the voltage control, according to the company, the new devices eliminate one of the major causes of "marginal" computer operation — line dropout. While providing smaller and more efficient voltage control, the new microcircuit is also expected to reduce the cost of commercial computers. Prices for the microcircuit range from $18 per unit in quantities of 1000 and up to $30 in quantities of 1 to 99. The voltage regulator circuit contains two high performance silicon epitaxial transistors, a compensated Zener diode reference element and a three-resistor network. Microelectronic Div., General Instrument Corp., Hicksville, L.I., N.Y.

Circle No. 159 on Inquiry Card

GERMANIUM POWER TRANSISTORS

A new family of npn germanium power transistors is said to provide industry with the only available source for 17 units manufactured in standard can Types TO-3, TO-10, and TO-13. The line features complementary pairs for npn applications, and 2N326 for power output and 2N1218 for high gain audio applications. KSC Semiconductor Corp., West Newton, Mass.

Circle No. 172 on Inquiry Card



SWITCHING MATRIX

A new fail-safe reed relay switching matrix was designed for over 100 million operations. It is said to be 50% smaller than comparable equipment and requires a 5 ms pulse to activate the latching magnets. Continuous holding power is not required and power interruption or shock does not disturb the circuit. Designated as Model DK series, the basic plug-in card incorporates 5 sets of switches internally wired and suitably terminated on a sturdy base board. McKee Automation Corp., North Hollywood, Cal.

Circle No. 191 on Inquiry Card

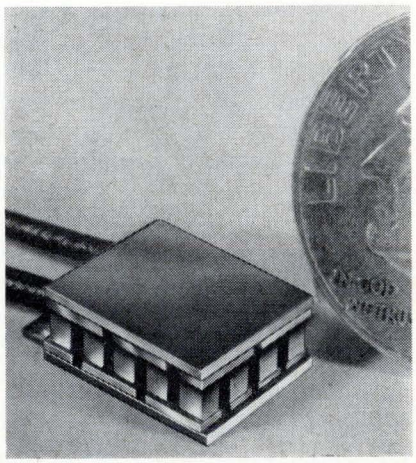
MICROMINIATURE SOCKETS

A series of microminiature sockets was designed for plug-in installation of miniaturized components to PC boards. Permanent mechanical retention and positive electrical connection is maintained between component pin and socket by means of a precision closed-entry contact inside the socket housing. Severe shock and vibration will not affect mechanical or electrical connection, the manufacturer states. Plug-in feature permits easy removal and replacement of components with no damage to pins or leads. Sockets attach to circuit boards by either crimp mounting or dip soldering and may be mounted from the top or bottom of board. Positive electrical contact is maintained without specially prepared holes. Units can be installed individually, or grouped into multipin socket assemblies, and are especially adaptable to automatic component mounting machinery. Patrician Industries, Monrovia, Cal.

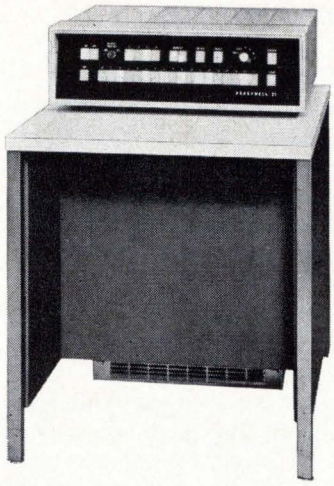
Circle No. 123 on Inquiry Card

IC COOLER

Highly-compact thermoelectric cooler stabilizes the temperature of integrated circuits, transistors, or crystals. The new cooler, Model 4 KA, requires 5 amps input current at approximately one volt. Heat sink capacity is 9 watts. Cold and hot surfaces both measure 0.415 x 320 and the unit's height is 0.15 of an inch. The unit has metalized ceramic plates which can be soldered to the heat sink or soldered to the components to be cooled. The company can provide the basic cooler; the cooler on a base with hermetic seal feed-throughs and enclosure; the cooler on a base with components mounted on the cold surfaces, sealed and evacuated to 1 x 10^{-6} mm Hg vacuum; as well as power supplies and temperature control equipment. Price is $29.50 each in quantities of one to nine. International Energy Conversion, Inc., Garland, Texas.



Circle No. 185 on Inquiry Card



if you can find a better main frame for the price . . . get it!

We're talking about the H21 – central processor for the new Honeywell 20 Digital Control System. The main frame price, starting at $21,000* is one of many features which make it an attractive component for real-time systems.

Some other features are:

Word Length: 18 bits plus parity and memory guard bits. Single word instructions provide 8192 directly addressable core locations.

Priority Interrupts: Up to 16 hardware levels.

Memory: Magnetic core, random access; 2,048 to 16,384 words capacity; prewired for field expansion; non-volatile on power failure.

Memory Guard: Gives "padlocked" protection against accidental modification of guarded core locations.

Direct Memory Access: Independent path to memory for external I/O operations on a fully buffered, cycle-steal basis.

Silicon Hybrid Circuits with low active component count insure reliable system operation from 32 to 120° F.

Indexing may be combined with indirect addressing.

Three-Address Register Commands allow three-address arithmetic and/or logical operations with single word, one cycle instructions.

Double Length Accumulator facilitates 36-bit arithmetic.

Parallel I/O Channels — designed to provide efficient and convenient interface with user's system equipment.

Typical Operating Speeds (in microseconds, including accessing and indexing): register arithmetic/logical operations, 6.0; load/store, 12.0; multiply, 54.0.

Options: Auxiliary drum memory, magnetic tape unit, high speed paper tape punch and tape reader, priority interrupts, DMA.

Software—An extensive software package includes CONTRAN, the new compiler-level programming system for real-time control; FORTRAN IV with linkage capability to executive programs; and CAP assembly system plus arithmetic, utility, and diagnostic programs.

The H22 central processor with a cycle time of 1.75 microseconds is available at a slightly higher price.

For additional information
call or write A. L. Rogers, Systems Sales Manager
Philadelphia Division, Fort Washington, Pa. 19034
Telephone: 215-643-1300

*Basic price of $21,000 includes H21 central processor with 2K core and input/output typewriter with integral tape punch and reader.

Honeywell

CIRCLE NO. 39 ON INQUIRY CARD

NEW PRODUCTS

INCREMENTAL CURVE FOLLOWER

An incremental curve follower provides automatic tracing and digital recording of continuous-graphic data. Curve follower tapes are compatible with characters-oriented and word-oriented computers and may be prepared in either 6 or 8 character-per-word formats. Resolution is ± 0.01 inch at lineal speeds up to 45 inches per minute. In many applications, the computer can be used to process tracer tape data for off-line plotting. California Computer Products, Inc., Anaheim, Cal.

Circle No. 168 on Inquiry Card

A-D CONVERTER

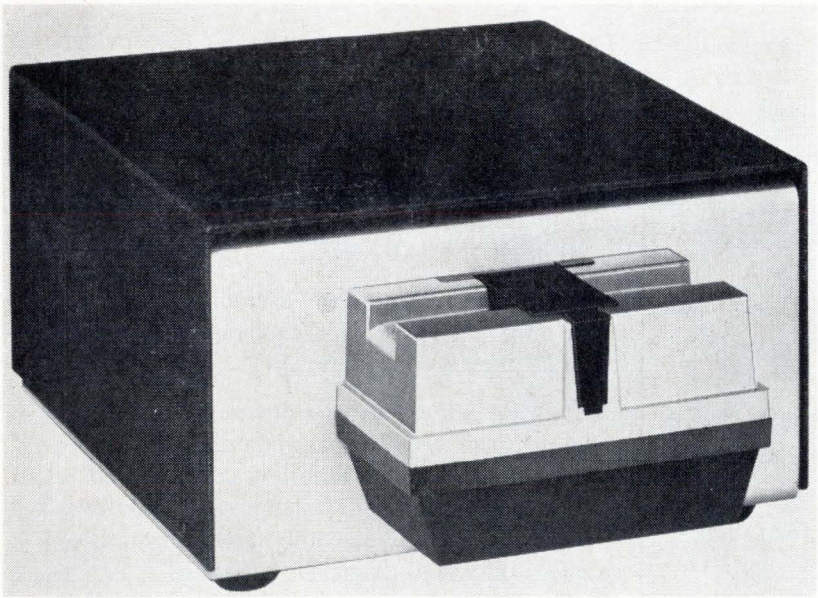
High-speed analog-to-digital converter is capable of 15,000 complete measurements per second. It comes complete with its own internal power supply and reference source. Output code is bipolar 9 bits or 8 bits plus sign and is displayed on the unit's front panel binary indicators. Three ranges of input voltages are provided, ± 1.024, ± 10.24 and ± 102.4 Input impedance is 1000 ohms per volt. Output voltage is + 10 volts at 2ma and accuracy is ± 0.1%, ± ½ least significant bit. The Model 327 is designed for rack mounting and is 19″ by 15″ by 3-½″. It requires standard 115vac, 60cps power and is available at $995.00. Digital Electronics Inc., Westbury, L.I., N.Y.

Circle No. 161 on Inquiry Card

ALPHANUMERIC KEYS

Designed for mounting directly on printed-circuit baseboards, alphanumeric keys contain magnetically-actuated, glass-sealed switches with minimum bounce characteristics and a life expectancy of up to 100 million operations. A protective hysteresis band between the make and break points in the stroke of the key makes the switch immune to microphonic vibrations at the time the contact is first making or breaking. Keys are available either with direct outputs from the glass-switch closures or with a single pulse output from a pulse generating circuit built into the key. Navigation Computer Corp., Norristown, Pa.

Circle No. 181 on Inquiry Card



PERFORATED TAPE READER

Principal feature of a new tape reader is a new read head which reads from the bottom of the tape at 75 characters per second asynchronously and bidirectionally. It reads 5, 6, 7, or 8 level tape without adjustment or modification. Any tape, such as paper, Mylar, or foil, in widths of 7/8″, 11/16″, or 1″ can be used without regard to color, thickness, or opacity. The new reader, Model R-75, operates on the non-return to zero principle and uses the star-wheel method of reading. Form "C" switching provides positive hole/no-hole identification. Tally Corp., Seattle, Wash.

Circle No. 190 on Inquiry Card

QUADRUPLE DTL NAND GATES

A new quadruple DTL NAND gate for military applications incorporates four separate two-input gates packaged in a single ⅛-inch-by-¼-inch "flat-pack." The collectors of the four NAND gates may be connected externally to form an AND-OR-NOT function. Completely compatible with company's DTL logic devices, it provides increased logic density since it has four gate functions per device, and each gate function has the output capability to drive at least eleven other gates. Typical noise margin is one volt, and average switching time is 23 nanoseconds. Price of the quadruple NAND gate is $20.50 each in quantities of 50 through 499. Westinghouse Molecular Electronics Div., Elkridge, Md.

Circle No. 147 on Inquiry Card

DOCUMENT RECORDER

The coding step in microfilm storage and retrieval of documents has been made fully automatic by a document recorder that translates computer language into ordinary words and symbols and records the information directly on 16mm or 35mm microfilm. The system, called the S-C 4400, receives data from a computer or computer-generated magnetic tapes and records it directly on film. At the same time, it codes the film for automatic and semi-automatic storage and retrieval systems. When operating on-line with a computer, the S-C 4400 can eliminate the need to produce magnetic tape. Paper copies need not be produced either, since selected pages can be printed on paper from the microfilm image as required. Stromberg-Carlson Data Products Div., San Diego, Cal.

Circle No. 117 on Inquiry Card

TAPE RECORDING FORMATTER

An instrument called the ADF-4 provides a complete link between the experimental laboratory and a digital computer. Using either on-line experimental analog signals or voltages reproduced from an analog tape recorder, the ADF-4 generates IBM computer compatible digital tapes. It is designed to be used with any of the new incremental tape recorders which operate at data recording rates of about 400 steps per second. Features of the ADF-4 include 1 to 4 channels of time-shared input data 10-bit analog-to-digital converter; manual command-code input; internal or external clocking with counters to determine record length, record count, and to generate the inter-record gaps and automatically stop the system at the end of a run; and output formatting to break up the 10-bit data word and to insert channel identification marks. Price of the complete ADF-4 unit is $6,250.00. Pastoriza Electronics, Inc., Newton Upper Falls, Mass.

Circle No. 118 on Inquiry Card

TELEMETRY DATA PROCESSING LINK

New digital data processing unit functions as a data processor between a decommutation system and a telemetry data processing computer complex. Its functions are threefold: frame sync recognition, in which it recognizes and identifies any two missing channels which could occur in an incoming, non-standard PAM wavetrain, or any one of three subframe sync pulses, thus providing the computer with a time coincident sync signal; displays selected digital data in the form of 8-bit binary words on the front panel; and provides digital data and sync information to a telemetry data processing computer. Decommutation rates range from 1 pps to 5000 pps. Stellarmetrics, Inc., Santa Barbara, Cal.

Circle No. 119 on Inquiry Card

MODULAR
A-D CONVERTERS

GREAT IDEA!

Why modular? Because now you can buy **only** the options you require . . . and all in one package.

By grouping the circuit elements into modular blocks, Navcor Series 2200 A-D Converters are constructed entirely from a family of compatible circuit modules. The basic units are available in ten-bit binary plus sign or three-digit BCD, with absolute value outputs or complement outputs for negative numbers, and operate at rates up to 8,000 complete conversions per second.

The variety and versatility of the plug-in modules assure compatibility with peripheral equipment, and system expansion is quick and easy. Sample and hold circuits, multiplexing, operational amplifiers, remote-output buffers, and other options may be added at any time.

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CIRCLE NO. 40 ON INQUIRY CARD

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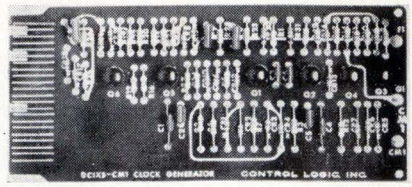


LOGIC CIRCUIT CARDS

New series of 100 kc silicon circuit cards and modules is available in two configurations — welded encapsulated modules and glass epoxy open circuit cards. Operating parameters of the family are from dc to 100 kc. The new series also includes cards which extend the counting range to 1 mc. The low-power, 100mw/circuit units offer a guaranteed noise rejection of 1.2v, 6v logic levels, 1 million hours MTBF, and require only two power supply voltages, ± 12v. Control Logic, Inc., Natick, Mass.

Circle No. 164 on Inquiry Card

MODULAR POWER SUPPLIES

All-silicon modular power supplies have multiple current ratings based on ambient temperatures of 40C, 50C, 60C and 71C. Full ratings apply when these units are mounted on any of three vertical surfaces. The complete series, designated the LM Series, includes 22 models, in four package sizes, with voltages up to 60 vdc, 0.08 amps to 8.3 amps. Units are remotely programmable — 200 ohms/volt over voltage range. All units have ac input voltage and frequency range of 105-132 vac, 45-440 cps. Temperature coefficient is 0.03% per degree C. Line regulation is 0.05% + 4 mv, load regulation 0.03% + 3mv. Ripple is lmv rms, 3mv peak-to-peak. Units are completely protected against short circuit and electrical overload, and excessive ambient temperatures. There are no voltage spikes due to "turn-on, turn-off" or power failure. Adjustable, automatic electronic current limiting circuit limits the output current to the present value upon external overloads including direct short, thereby providing protection for load, as well as for power supply. Prices start at $79.00. Lambda Electronics, Melville, L. I., N. Y.

Circle No. 142 on Inquiry Card

SOLID-STATE MULTIPLEXERS

Miniature solid-state multiplexers, available in 30 to 120 channel sizes, were designed for use in aerospace or ground-based telemetry and data acquisition systems requiring time-sharing of a single conversion and/or transmission device among a number of data points. The units may be operated as straight-through multiposition switches, or with converters to provide PAM, PDM, and PCM data formats and variations. Various types are available for high-level, single-ended, or low-level differential data multiplexing. Features, according to the company, are small size (9.6 cubic inches for 30-channel high-level unit), low power consumption, higher operating speeds, and longer life spans than competitively-priced mechanical devices. The Ralph M. Parsons Electronics Co., Pasadena, Cal.

Circle No. 152 on Inquiry Card

COMPUTER FAN

A new fan delivers 100 cubic feet of cooling air per minute and sells for less than $4.00 in quantity. It requires no holes for mounting hardware because it requires no mounting screws. The fan inserts into the same hole required for the air flow and it is secured by a keeper ring. Called the Skipper, it mounts easily anywhere on any panel thickness or panel material, including glass. The fan was designed for minimum acoustical disturbance. Its 38-decibel (SIL) noise level makes it suitable for computer rooms, test areas, or other areas where silent operation is required. Accessories include plug and cord assembly, guards, boot to protect solder connections, and plates to provide a choice of mounting methods. Rotron Mfg., Co., Woodstock, N.Y.

Circle No. 127 on Inquiry Card

NEW PRODUCTS

LOW-LEVEL MULTIPLEXER

A 32-channel addressable low-level multiplexer provides 3-wire multiplexing at rates as high as 200 samples per second. The Model 9532 can be randomly addressed from a 5-bit binary word or operate in a sequential mode with a serial pulse train input. Completely self-powered, the unit provides less than 1 microvolt channel-to-channel offset, 1 microvolt crosstalk, and 1.5 microvolt peak noise. Molecular Research, W. Palm Beach, Fla.

Circle No. 189 on Inquiry Card

COAXIAL PROGRAMMING SYSTEM

Complex switching is said to be facilitated by a new coaxial programming system. Program changes involving up to 3036 coaxial circuits are rapidly accomplished by changing one or more of the removable front boards in the new system. The procedure normally requires changing a series of individual or multiple coaxial connectors. In addition to removable patchboards, system comprises a lightweight metal frame which houses a molded plastic board containing individual coaxial spring contacts. One-crimp coaxial contacts connect the system with external equipment. Hybrid systems are available with mixtures of coaxial and universal contacts. Redundant contact design, coupled with a special camming action of the frame provides an exclusive double wiping action of patchboard tips and contact springs to assure positive reliable contact. The new system was developed for critical low-level switching applications in equipment designed for testing, data handling and processing, communications, analog computers, and telemetry instrumentation. Amp Inc., Harrisburg, Pa.

Circle No. 174 on Inquiry Card

40-MILLIWATT RELAY

High-sensitivity relay of crystal-can dimensions is actuated by 40-milliwatt input signals and rated to switch 2-amp, 28vdc-resistive loads 100,000 times, or dry circuit loads up to 50 million times. The DPDT Series 35, a magnetically biased polar relay, always closes the same set of contacts when de-energized and switches only in response to signals of proper polarity. Flexure elements that remain stable even under 30 g vibration replace conventional pivots, thereby eliminating a potential source of friction and wear. Direct connection of contact members to the balanced armature without use of pushers provides an integrated switch mechanism. Its low power drain, combined with minimum heat dissipation and small size, are said to make this relay suitable for use in computers and dataprocessing systems. Sigma Instr., Braintree, Mass.

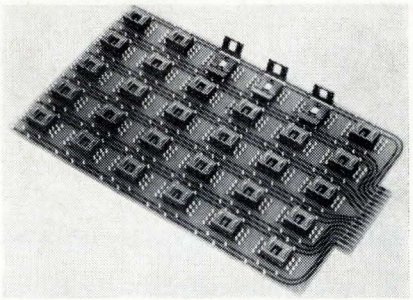
Circle No. 138 on Inquiry Card

MERCURY-WETTED RELAYS

Mercury-wetted contact performance in a very small encapsulated package with printed circuit terminals is featured in a new relay. The assembly construction assures long life operating stability. Rugged, one-piece combination terminal posts and printed circuit pins are staked through an epoxy resin terminal board to assure unfailing conductivity. With the capsule and coil assembly in place contact leads are soldered to the rigid posts, thereby eliminating stresses that transmit to the contacts inside the capsule and affect operating stability, such as occur when contact leads are used for terminals. Contact leads are used or terminals. Contact rating is 28va at 1 amp or 100 volts maximum, resistive load. Operate time and release time are each 1 ms. Life expectancy is 100 million cycles at rated load. Magnecraft Electric Co., Chicago, Ill.

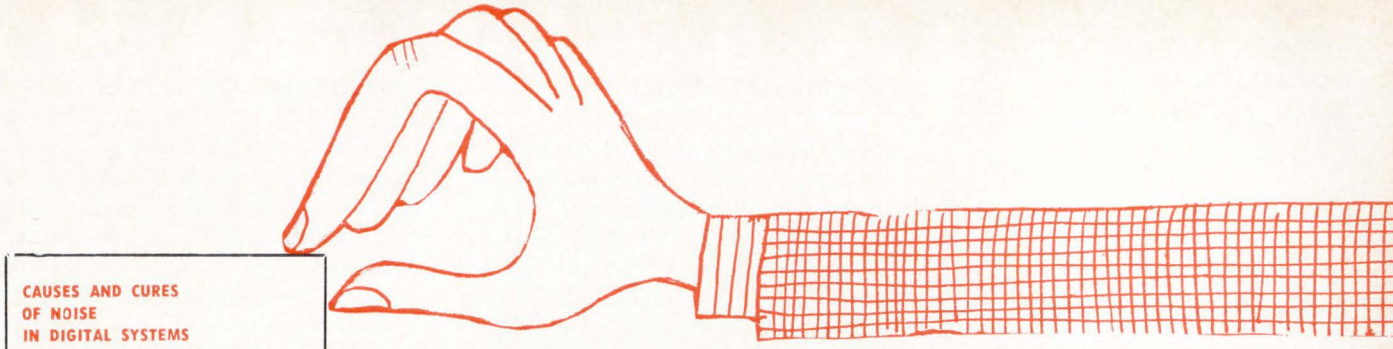
Circle No. 193 on Inquiry Card

INTEGRATED CIRCUIT BOARDS



New integrated circuit board units were designed to simplify the testing, power aging, and breadboarding of integrated circuits in all standard sizes of TO-5 and flat package cases. For specialized applications, the units are available with a variety of the latest sockets available. Sockets are mounted in varying positions of multiples of five. For example, one standard board, the 030-001, has thirty positions of "Quik-Sert" flat-pack sockets terminated in turret lugs with sixteen busses. For easy insertion and optimum protection, all sockets for TO-5's have large pyramidal entrances with polarization marks, and sockets for flat-packs feature a unique flip-top cover and latch assembly with automatic component positioning. Boards are also available with mating connectors for use with interchangeable sockets. The 030-001 type board has the sockets terminated in turret lugs adjacent to each socket position and has busses running the full length of the board, with two interconnection points on each of the sixteen busses per socket position. Interconnections between positions are made by hard wiring techniques, and power inputs and outputs are made to the buss connections. Adequate room is provided for the addition of any discrete components which might be required. Barnes Development Co., Lansdowne, Pa.

Circle No. 125 on Inquiry Card



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By J. Paul Jones, Jr.

A 56-PAGE POCKET-SIZE HANDBOOK

The material in this handbook originally appeared in a 3-part series of articles in the 1964 Fall issues of **COMPUTER DESIGN.** The large number of requests for copies prompted the printing of this handbook.

Excellent design tips and basic guideline rules for eliminating or minimizing noise in digital systems are given. Here is just a partial listing of topics:

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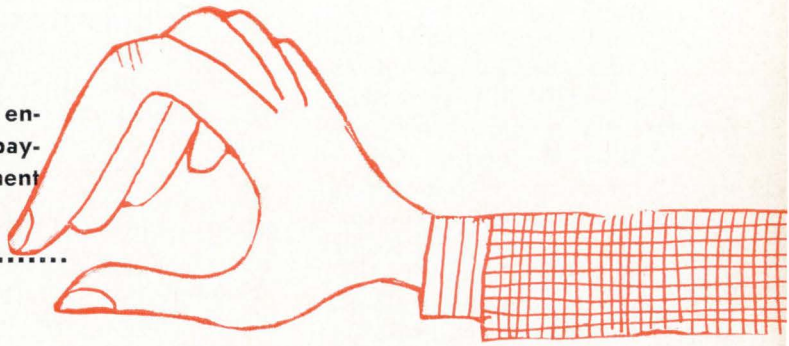

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NEW PRODUCTS

COOLING FAN ASSEMBLIES

Cooling motor-fan assemblies for use in computer and electronic equipment cabinets can be operated as blower or suction units and are rated 500 cfm at approximately 1550 rpm. Models for operation at 3000 rpm also are available for applications where greater air flow capacity is required. The assemblies are designed for all-angle operation and can be mounted in any position inside an equipment cabinet between the air intake and outlet without adversely affecting motor life. Provided with a wire mesh safety screen, units are available for operation at 115 or 230 volts, 50 or 60 cycles. General Electric Co., Spec. Motor Dept., Ft. Wayne, Ind.

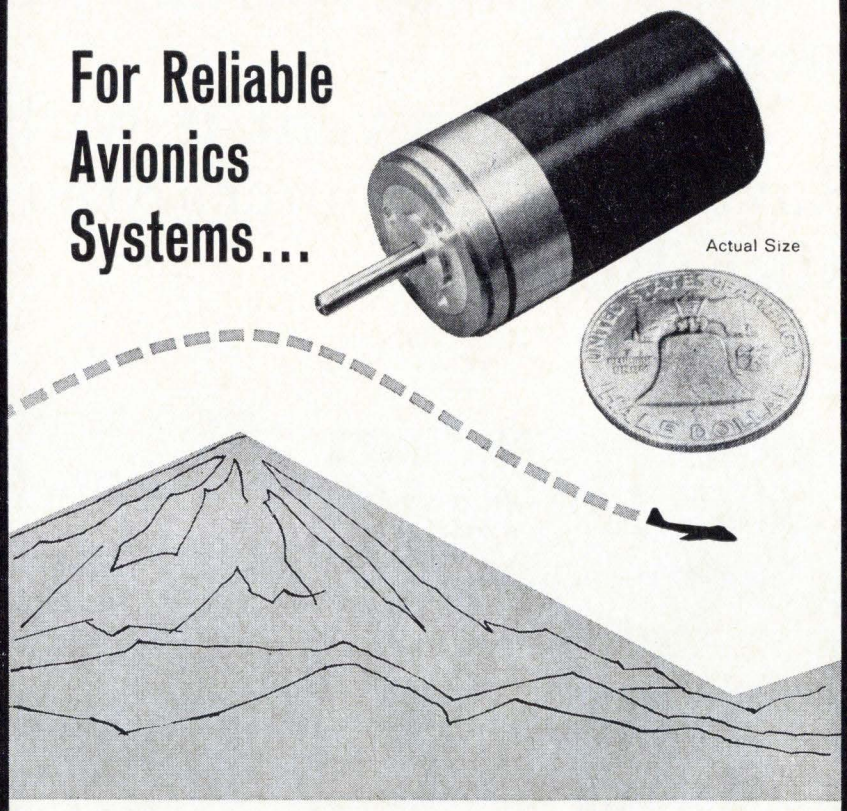
Circle No. 167 on Inquiry Card

LOW-COST DTL CIRCUITS

A complete line of high-speed monolithic DTL integrated circuits priced as low as $2.25 in small quantities make up a logic family of 14 circuits in the DTL mode with operation guaranteed over the temperature range of 0 to 75C. They were designed for low power operation in the range of 7 mw per gate with typical propagation delay time of 30 nanoseconds. Though specifically applicable to commercial equipment, the integrated circuit series is said to be also useful to the military equipment designer because he can use it to breadboard a system at low cost and then upgrade it to meet military specs by replacing each element in turn with a corresponding device from previously introduced integrated circuit series which has a temperature range of −55C to +125C. Packages offered are the 10-lead TO-5 and a 10-lead ¼" x ¼" ceramic flat-pack. Motorola Semicon. Products, Inc., Phoenix, Ariz.

Circle No. 198 on Inquiry Card

For Reliable Avionics Systems...



a NEW Integrated Circuit All-Magnetic Size 11 Encoder

Designed specially for avionics fire control, navigation and computation systems, the EMR Model 508 is the FIRST shaft-angle encoder with integral interrogate/readout electronics in a size 11 case (1.1" diameter). For digital coding of shaft angle the new encoder offers all the reliability advantages of non-contact magnetic encoding and is as simple to apply as a brush encoder. Self selecting logic presents non-ambiguous dc logic-level outputs. Outputs can be binary-code, gray-code, and incremental codes with direction sensing logic available; resolution per turn is eight bits. All logic is performed within five microseconds after receipt of enable pulses. We'll loan operating models for evaluation; just write or phone:

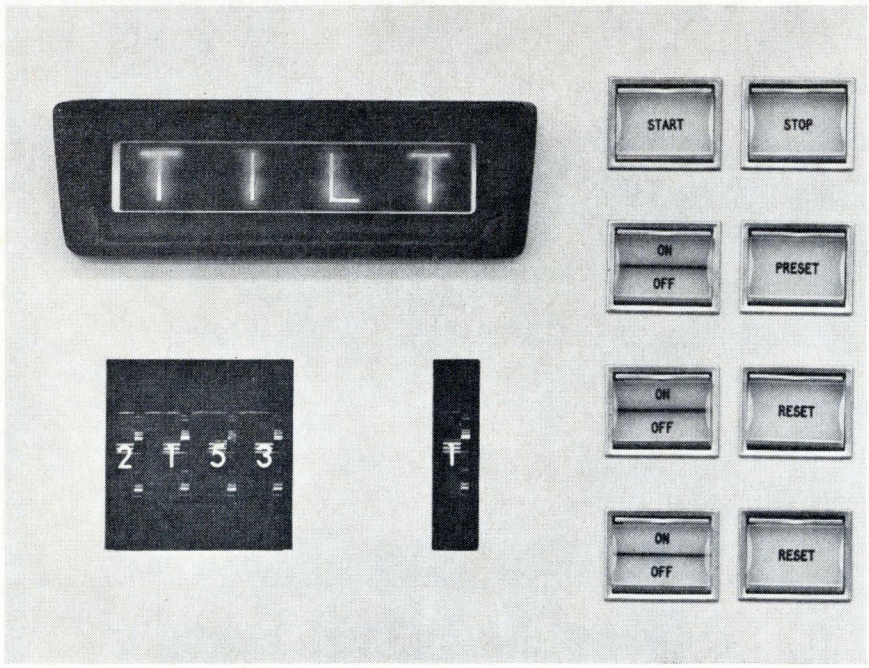
EMR

PRINCETON DIVISION
P. O. BOX 44 PRINCETON, N. J.

ELECTRO-MECHANICAL RESEARCH, INC.

CIRCLE NO. 42 ON INQUIRY CARD

Why chance a scrambled memory?
You can prevent it with Raytheon Computer's NDRO MicroBIAX



Published reports indicate that failure of the on-board computer during the recent flight of Gemini 4 resulted from a "scrambled" memory. Designers of airborne and spaceborne computer and data systems can avoid this hazard by using Raytheon Computer's MicroBIAX memories. Memory systems with MicroBIAX multi-aperture ferrite elements offer true non-destructive readout. No rewrite cycle or priming operation is required after readout.

Even with complete or partial power failure, data is still held in memory, ready for use when power *is* restored. And MicroBIAX is demonstrably more tolerant of wider swings in voltage and current than coincident-current memories.

MicroBIAX stores more than 2000 bits per cubic inch; stacks are available in sizes up to 4096 words by 144 bits. Readout rate can be 1 megacycle or faster over a temperature range of −55°C to +100°C.

For help in making your next airborne or spaceborne data system memory scramble-proof, write for Data File B-116B. Raytheon Computer, 2700 So. Fairview Street, Santa Ana, Calif. 92704.

RAYTHEON

CIRCLE NO. 43 ON INQUIRY CARD

NEW PRODUCTS

DIGITAL CLOCK

An electromechanical digital clock provides visual readout continuously and remote electrical readout on command. The clock was designed for use in data reduction systems; to control batching where timed mixing is important; to aid in computing piece rates in all production processes; and, in all types of data or material handling where a time base is required. Each digit has an isolated 11 line readout that can be made available to computers, printers, and controls. The digital clock is available as a standard model with or without a time base generator, with a cabinet for desk mounting or without cabinet for 19″ relay rack mounting or for 9½″ panel mounting. Durant Mfg. Co., Milwaukee, Wisc.

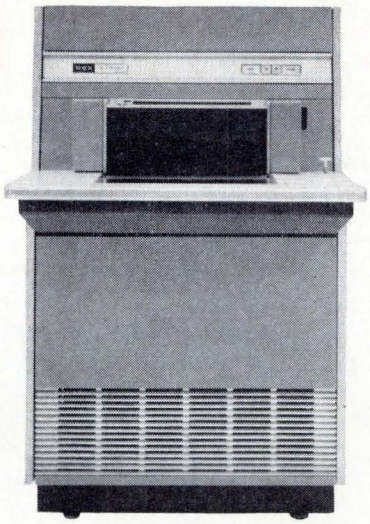
Circle No. 179 on Inquiry Card

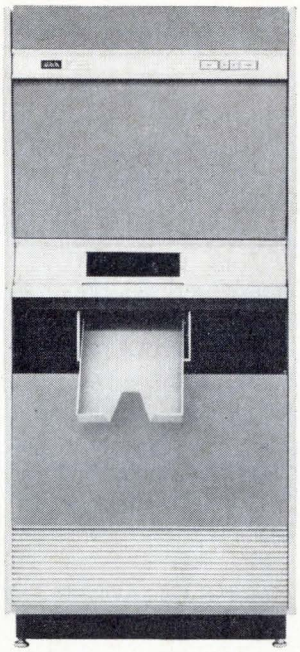
MICROMINIATURE FILM RESISTORS

A new series of microminiature film resistors are said to feature extremely high temperature range, wide resistance range, and optimum size/power ratio. Units are rated from 10 ohms to 10 megohms; from 0.12 to 1.0 watt power; with a maximum operating temperature of +275C. Superior performance is said to be based on the use of resistance films processed from a proprietary formula of complex oxides. Power and precision models are offered in standard resistance tolerances of ±1% with tolerances to 0.1% available on special order. Other specifications include: load life of 1000 hours at rated power, with 0.5% maximum resistance shift; overload 5 times rated power for five seconds, with 0.2% maximum shift; overvoltage 1.5 times maximum voltage, with 0.5% maximum shift. Caddock Electronics, Riverside, Cal.

Circle No. 186 on Inquiry Card

No matter what we start discussing at Xerox... sooner or later we're talking about more new jobs.





Sometimes people are puzzled when we say that Xerox is in the business of graphic communications. Let's try to clarify. (It could be important, especially if you're intrigued with Xerox, but not perfectly sure why.)

We define graphic communications as the entire spectrum of communications in a graphic sense — the formulation, reception, transmission, recording, storing, retrieving, processing, copying, or presentation of any meaningful images. As you can imagine, graphic communications transcends copying equipment, no matter how advanced. LDX (Long Distance Xerography) suggests something of our future. The current system recently sent an 8½" x 11" xerographic image 3,450 miles over broadband telephone lines in 7 seconds. For what LDX implies, reread the definition of graphic communications above. You'll get the picture.

The openings outlined below are abstracts from our current list of immediate vacancies. In most cases they are new, expansion-created spots. In others, the man has been promoted. Isn't this the best way to come on board in any organization?

COMMUNICATIONS SYSTEMS ENGINEERS
To direct a team of Systems Engineers on assigned major projects; evaluate alternative systems concepts; determine cost/performance trade-offs; establish systems requirements; generate concepts leading to future engineering developments and analyze methods for facsimile distribution switching and storage. BS required in EE, Engineering Sciences or Physics (MS preferred) with a minimum of 3 years' experience in circuit and systems design, preferably involving data communications equipment including teletype and/or telephone modem equipment, facsimile, broadband and microwave equipment, and integration of such equipment into larger systems involving network operation. Also, experience with remote input/output equipment, optical character recognition, on-line, real time digital data communication with computers.

ADVANCED CIRCUIT DEVELOPMENT ENGINEERS
For integrated circuit module selection and specification for general purpose logic modules and macro-modules employing microminiature array logic for decoders, code translators, shift registers, multiplexers and D/A converters for computer peripheral and communications products. BS/MSEE with 8 to 10 years' comprehensive experience in general purpose computer products development in areas of circuit design and systems. Must have designed and used standard card configurations in fulfilling system requirements and be familiar with design automation and automatic fabrication, wiring and checking techniques.

ELECTRONIC DEVELOPMENT ENGINEERS
For experimental design, fabrication and testing of advanced CRT display, character generation, and control equipment. Experience in electronic circuit design, solid state logic, display, communications, and/or packaging.

INFORMATION SYSTEMS ENGINEERS
For system configuration study and synthesis leading to detailed specification of information storage and retrieval equipments, computer peripheral equipments and data systems terminals. BS required in EE, ME, or Physics with at least 5 years' experience in design, development and/or systems in digital information processing display, communications, and/or microfilm systems.

Positions are in Rochester, N. Y. Send resume, including salary history, to Mr. R. E. Conboy, Xerox Corporation, Dept. CD-9, P.O. Box 1540, Rochester, New York 14603.

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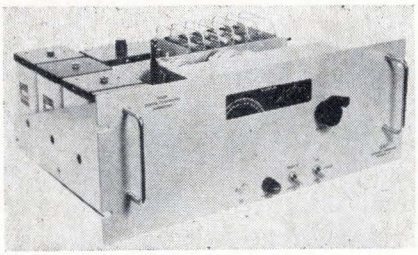
NEW PRODUCTS

PRECISION RESISTORS

New precision metal film resistors are highly stable, low-cost units designed for use in military, computer, and industrial markets. Over two million component hours of preproduction testing with results exceeding MIL-R-10509 have been completed on the new resistor. Production of a complete range of values in the ⅛ watt size with tolerances of ±1% and ±0.5% and temperature coefficient of resistance to ±50 ppm/°C began this July. Other wattages will be added this fall. P. R. Mallory & Co., Inc., Indianapolis, Ind.

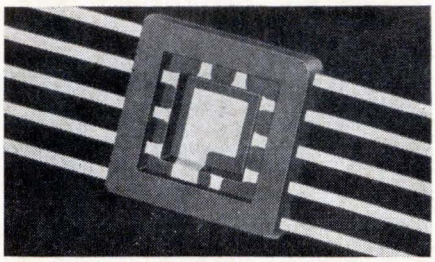
Circle No. 182 on Inquiry Card



DIGITAL-TO-SYNC CONVERTER

A digital-to-synchro converter, Model S3216, converts parallel binary data through a servo loop into two-speed synchro outputs of 36 and 1 or 36 and 2. Synchro outputs can be used to drive a radar antenna, machine table, or any other positioning device using two-speed synchro data. Servo part of the computer uses a unique two-speed potentiometer follow-up section featuring continuous rotation capability through the zero angle point without reversing direction. Model S3216 features 15 bit resolution; dial readouts; manual positioning knob; ± ½ bit accuracy; 12° per second slew rate; 15k to ground input signal load. Logic level for binary one is −6.8v, ± 1.5v; binary zero logic level is 0v, ± 1.0v. Gap Instrument Corp., Westbury, N.Y.

Circle No. 131 on Inquiry Card



IC PACKAGING

A new line of flat packages for integrated circuits is produced with glass-to-metal technology for maximum reliability, ruggedness, hermeticity and economy. Included in the series are ten and fourteen lead flush pad designs, and a new recessed pad 10-lead design. The recessed 10 lead "Flat-Pak" series is the ultimate integrated circuit package, according to Glass-Tite engineers, because it avoids bonding problems when silicon chips are assembled to the pad area. More rapid and reliable assembly of chips is assured by providing more room for the electrode and less chance for lead shorting. Also available is a 14-lead series made with hard glass and gold-plated expansion-matching nickel-iron cobalt. Glass-Tite Mfg., Div. of G.T.I. Corp., Prov., R.I.

Circle No. 148 on Inquiry Card

DTL IC KIT

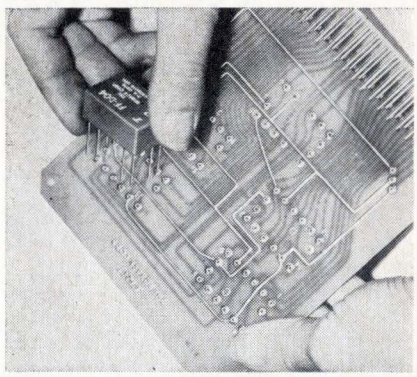
An engineering kit of 10mc DTL integrated circuits includes flip-flops, two and four input NAND gates, gate extenders, line drivers, one shots, a clock source, and interface circuitry. Also included are connectors, a mounting panel, and a convenient storage container. This special kit is intended to assist those considering integrated circuits in new product development programs. The same group of sample cards may be used for hundreds of different experiments without soldering or damaging the flat pack elements. The complete kit including data sheets and application notes is available for $795. Microsystems Components, Woodland Hills, Cal.

Circle No. 141 on Inquiry Card

ZENER DIODES

New "whiskerless" Zener is one-tenth the size of a standard DO-7 package. The glass-body is a true hermetic seal and is designed to meet or exceed environmental requirements of MIL-S-19500B. The first Zeners in the new line will be rated up to 500 mw and are characterized by extremely low dynamic impedance and low leakage (0.01 ua). Transitron Electronic Corp., Wakefield, Mass.

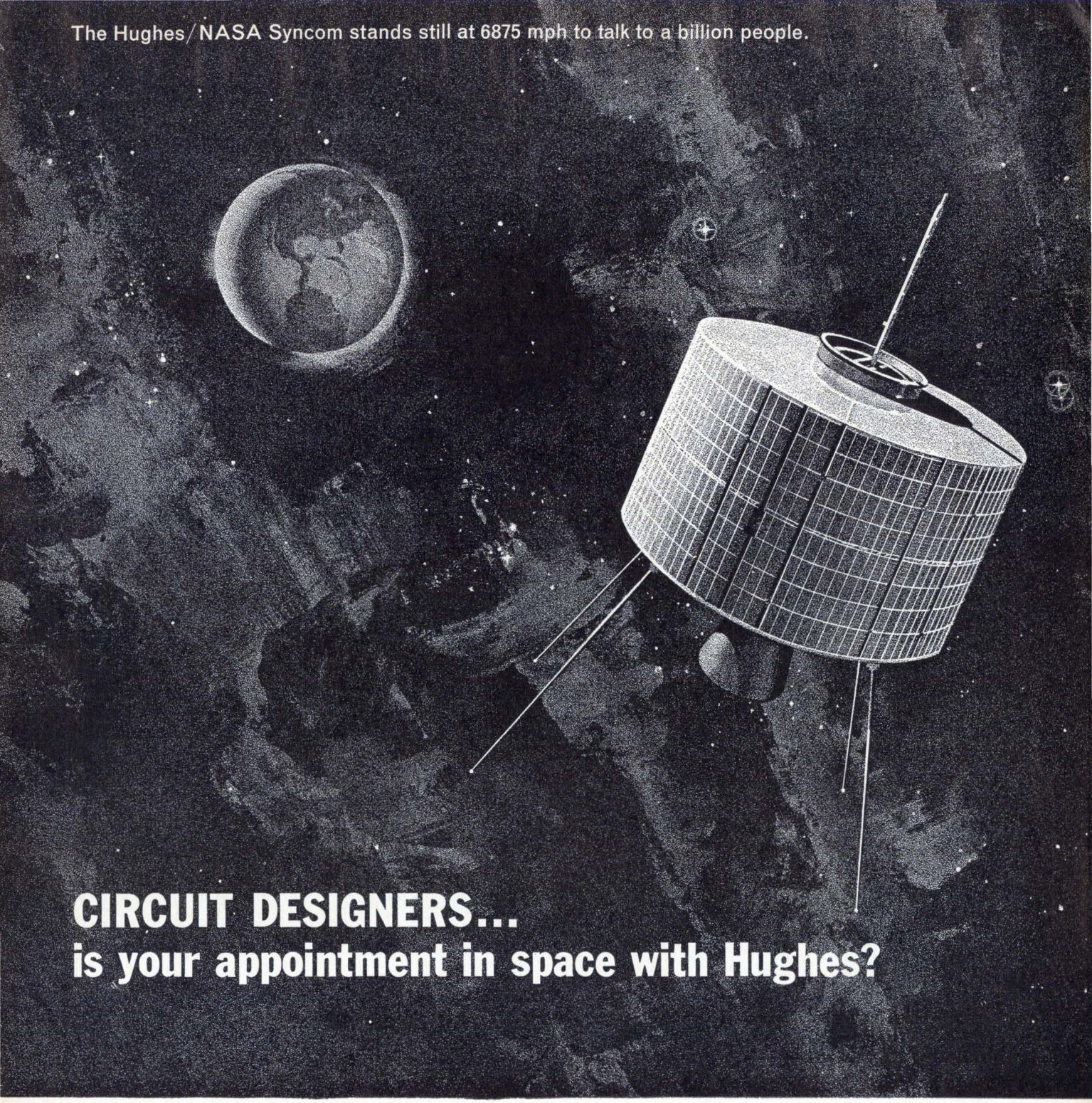
Circle No. 183 on Inquiry Card



ENCAPSULATED FLIP-FLOP

An encapsulated counter register flip-flop is a new 25kc all-silicon digital circuit module which is one of a number of standard, ready-to-use encapsulated circuits. The new flip-flop can be supplied unmounted, premounted on standard or custom-designed circuit cards. Voltage levels, physical characteristics, and power supply voltage of the flip-flop and other circuit modules in the family are completely compatible with those of the manufacturer's higher frequency encapsulated circuit modules. Also module size and pin connections are identical. Thus, selected portions of digital systems can be implemented with high-frequency modules or with the new low-cost modules as required, usually with significant dollar savings, according to the company. Designed especially for heavy duty industrial and commercial applications, the new flip-flop lists at $5.85 each with quantity discounts available. The Roback Corp., Huntingdon Valley, Pa.

Circle No. 158 on Inquiry Card



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CIRCLE NO. 900 ON INQUIRY CARD

LITERATURE

Industrial Counters

Standard, in-stock counters are presented in a 24-page catalog. The publication illustrates and gives specifications for the firms's line of hand-operated, mechanical, electric, predetermining, and photoelectric counters. Veeder-Root Inc., Hartford, Conn.

Circle No. 209 on Inquiry Card

IC Packaging

How flat-pack integrated circuits are being manufactured in high density, low weight, microminiaturized packages through parallel gap welding techniques is described in a new bulletin. The bulletin shows how as many as 10 integrated circuits per square inch can be mounted on a circuit board using the delicate parallel gap welding method. The bulletin points out that parallel gap welding has enabled construction of circuit boards with flat packs mounted on them to be stacked to densities previously unattainable. High Reliability Circuit Systems, Anaheim, Cal.

Circle No. 213 on Inquiry Card

Microminiature Connectors

A 12-page publication contains 57 photographs and drawings of circular, rectangular, strip, and special microminiature connectors, all incorporating twisted pin contacts. New types of plug-in packaging for integrated circuitry are also described and illustrated. ITT Cannon Electric, Los Angeles, Cal.

Circle No. 214 on Inquiry Card

Computer Floors

A 12-page brochure explains how the infinite access floor concept was brought into being as the technical solution for installing automatic data processing equipment. If offers an inexpensive and practical method of providing clear underneath-space to accommodate electrical power and signal cabling and mechanical service lines, and to serve as an air plenum. The brochure supplies all the basic information required by architects and engineers, including detail drawings and architectural specifications. It includes a typical floor plan of a computer room, cross-referenced to the details, and explains the advantages of the unique precision die-cast aluminum panels and pedestals and the rigid, vibration-free assembly of the floating floor. Floating Floors, Inc., New York, N.Y.

Circle No. 202 on Inquiry Card

Core Memory Catalog

More than 2000 different coincident-current core memory stacks can be specified with the help of a new 8-page catalog, covering plane capacities up to 16,384 cores. The catalog is said to provide a selection of components great enough to permit the designer to "build" a memory stack which exactly matches his computer system specifications. The publication describes 16 frame styles, eight core designs, four inhibit wiring patterns, and two plane interconnect methods. Also included are ELR characteristics for any of 24 possible core-frame configurations, as well as the means of calculating electrical properties for plane stacks. Fabri-Tek, Inc., Amery, Wisc.

Circle No. 216 on Inquiry Card

Computer Typesetting System

A 6-page brochure describes a PDP-8 typesetting system based on an integrated circuit computer. The system accepts unjustified, unhyphenated perforated tape and produces a clean operating tape for use in automatic linecasting machines. Production rate is 12,000 lines an hour, keeping 12 linecasting machines busy. Digital Equip. Corp., Maynard, Mass.

Circle No. 207 on Inquiry Card

Telephone-Type Relays

Engineering data sheet covers miniature telephone-type relays which were designed to provide outstanding switching capability and versatility for their size. Coil, contact, and other electrical characteristics, as well as important environmental, mechanical, and dimensional data of the relays are included. C. P. Clare & Co., Chicago, Ill.

Circle No. 224 on Inquiry Card

Plug-In Power Supply

A new 1965 catalog covers a line of dc plug-in power supplies. Line drawings, specifications, and prices are included in the sixteen-page brochure. Both single output and dual output models are described in detail. Acopian Corp., Easton, Pa.

Circle No. 215 on Inquiry Card

A-D Converters

An 8-page catalog contains descriptions of wide-band, floating differential amplifiers, analog-to-digital converters, and a solid-state multiplexer. Data is also presented on rack assemblies available for multiple amplifier installation. Preston Scientific, Inc., Anaheim, Cal.

Circle No. 225 on Inquiry Card

IBM

Space Guidance Center offers a wide range of career openings in Advanced Aerospace Computer Development

At IBM the excitement of growth, the challenge of new problems, the stability of long-range markets—all these add up to outstanding career opportunities for professionals at all degree levels. For example, the Space Guidance Center at Owego, just south of the Finger Lakes vacation region of New York, is significantly expanding its activities in advanced aerospace computer development to give greater support to the nation's aerospace programs. The Center's widening role in space science has created new opportunities for experienced engineers and scientists. The areas listed below represent only a few of the many immediate openings.

Computer Applications Engineers: Aircraft computer applications —synthesis, flow charting and operational debugging of equations for navigation, guidance, flight control, data processing, fire control, system checkout and alignment, track-while-scan systems, correlation techniques for fix taking and other related aircraft functions • Analysis of computation requirements for space-oriented operations, celestial and engineering mechanics, principles of space guidance, navigation and control for earth and cis-lunar space • Digital computer theory and design principles • Detailed digital computer design, aerospace applications • Detailed logic designs of both serial and parallel computers, utilizing integrated circuit technologies • Definition and optimization of computational requirements for advanced aircraft systems. Creative designs for memory, arithmetic and control, and input/output systems • Large-scale data processing systems configuration • Scientific data processing and real-time control functions.

Computer Systems Engineers: Digital computer logic and systems design for aerospace systems environments • Synthesis of detailed aerospace computer requirements • Future computer planning for aircraft/space computer interface problems in aircraft and space systems, requiring state-of-the-art experience in aerospace computer technology and application of technical knowledge toward planning of future aircraft and/or space computer problems.

Computer Design Engineers: Aerospace computer technology, including high-speed random-access memories and integrated circuits • Detailed analysis of computer instruction sets • Detailed design of aerospace computer systems • Machine languages • Programming systems.

Exterior Computer Systems Design Engineers: Detailed exterior computer design • Familiarity with operation of magnetic tape, disc, and drum memory systems and design, utilizing these storage media as slow-access peripheral memories • Utilization of logic and organizational techniques to perform input/output control, formatting and conversion in data processing and control applications.

Logic Design Engineers: Analysis of electronic circuits to determine logic effectiveness • Create new machine organization methods to provide for increased computer reliability • Develop mathematical models of serial and parallel machines • Organization and logic design of advanced space computers.

Logic Systems Engineers: Design large-scale computing and data-handling systems for aerospace environments • Develop computer specifications, functional organization and detailed logic design of systems.

Please Write: Outline your qualifications and interests to: J. R. Raftis, Dept. 540J, IBM Corporation, Owego, New York 13827. IBM is an Equal Opportunity Employer.

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LITERATURE

Copper Welds

Guidelines for designing copper printed circuit boards for best parallel-gap welding results are contained in a new report. Included are discussions of weld schedules, weld strength and consistency data, metallurgical characteristics of kovar-to-copper weldments, board damage, and effect of goldplating. Hughes Aircraft Co., Welder Dept., Oceanside, Cal.

Circle No. 222 on Inquiry Card

Pulse Transformers

Improved molded miniature pulse transformers in a wide variety of sizes, lead styles, volt-microsecond capability, and turns ratios are included in a new series. A complete cross-reference chart on old and new catalog numbers, as well as complete data and outline drawings, and lists of standard transformers is given in a 12-page bulletin. Sprague Electric Co., North Adams, Mass.

Circle No. 205 on Inquiry Card

Binary-Controlled Switch

Product newsletter describes master/slave positioning units for remote airborne rocket launch control and similar applications. Selection of any one of 21 switch positions on master unit is precisely duplicated by the slave unit through rotary printed circuit switches containing binary-coded information. By this means, only 5 wires are required to transmit 21 coded signals between master and slave. A. W. Haydon Co., Waterbury, Conn.

Circle No. 226 on Inquiry Card

ADVERTISERS' INDEX

ALBERT, NELLISSEN, INC.	78
AMP, INC.	24
AMPEREX ELECTRONIC CORP.	33
BARNES DEVELOPMENT CO.	53
BENSON-LEHNER CORP.	51
BRYANT COMPUTER PRODUCTS	64
C&K COMPONENTS, INC.	55
CAMBRIDGE THERMIONIC CORP.	54
COMPUTER CONTROL CO.	Cover 2
COMPUTER TEST CORP.	35
DATAMEC CORP.	12
DECISION CONTROL, INC.	56
DYNAMICS RESEARCH CORP.	22
ENGINEERED ELECTRONICS CO.	23
ELECTRO-MECHANICAL RESEARCH INC.	73
FACIT	43
FAIRCHILD SEMICONDUCTOR	Cover 4
FRANKLIN ELECTRONICS	34
GENERAL DYNAMICS/ELECTRONICS	13
GENERAL PRECISION, INC. Librascope Group	61
HAYDON SWITCH & INSTRUMENT, INC.	25
HONEYWELL EDP	Cover 3
HONEYWELL Special Systems Div.	67
HUGHES AIRCRAFT CO. Aerospace Div.	77
HUGHES AIRCRAFT CO. Microelectronics Div.	49
IBM CORP.	79
IMC MAGNETICS CORP.	17
INDIANA GENERAL CORP.	15
INVAC CORP.	63
LENZ ELECTRIC MFG. CO.	45
LITTON INDUSTRIES Encoder Div.	37
LITTON INDUSTRIES Monroe Data/Log Div.	27
MAGNETIC SYSTEMS CORP.	39
NAVIGATION COMPUTER CORP.	69
POLAROID CORP.	40, 41
PRESIN CO.	54
RAYTHEON COMPUTER	74
RCA	9
RESE ENGINEERING	70
ROTRON MFG. CO.	57
SAFETEE GLASS CO.	29
SCIENTIFIC DATA SYSTEMS, INC.	11
TALLY CORP.	59
TELETYPE CORP.	3, 5, 7
TOKO, INC.	42
TRAK ELECTRONICS	65
WAYNE GEORGE CORP.	1
WINCHESTER ELECTRONICS Div. of Litton Industries, Inc.	19
XEROX CORP.	75

"...I liked my job,

but

I felt
more and more
I was just repeating myself.
Not really learning much.
Not being pushed,
you know?

There was plenty to do.
I was busy.
It's just — I don't know —
it's like that old line
about a specialist
being someone
who knows more and more
about less and less.
That was me.
That was our whole group . . .

Everything was an emergency,
no one seemed to know
what was important —
they were too busy with
"emergencies."

Deciding to leave
wasn't easy.
As I said,
they were a fine group.
But I needed
something different.
More responsibility.
Less red-tape.
And a company that
seemed to be growing
in a planned direction,
not just jumping around,
putting out fires . . .

. . . So I thought about it,
did some reading —
not just the help wanted ads,
but business articles,
financial news,
things like that —
and decided to contact
Honeywell.

At first my wife said
"Boston!"
as if it were Hong Kong.
After,
she saw some of the material
about the schools and towns here.
Now I couldn't
get her to leave
if I wanted to —
and I don't.

It's really amazing —
Honeywell's
figured out
how to keep all the advantages
of working in a small
company
and still be a big
operation.

I don't know how they
do it."

Interested Computer Engineers are invited to forward their resumes to Mr. Edwin Barr, Employment Supervisor.

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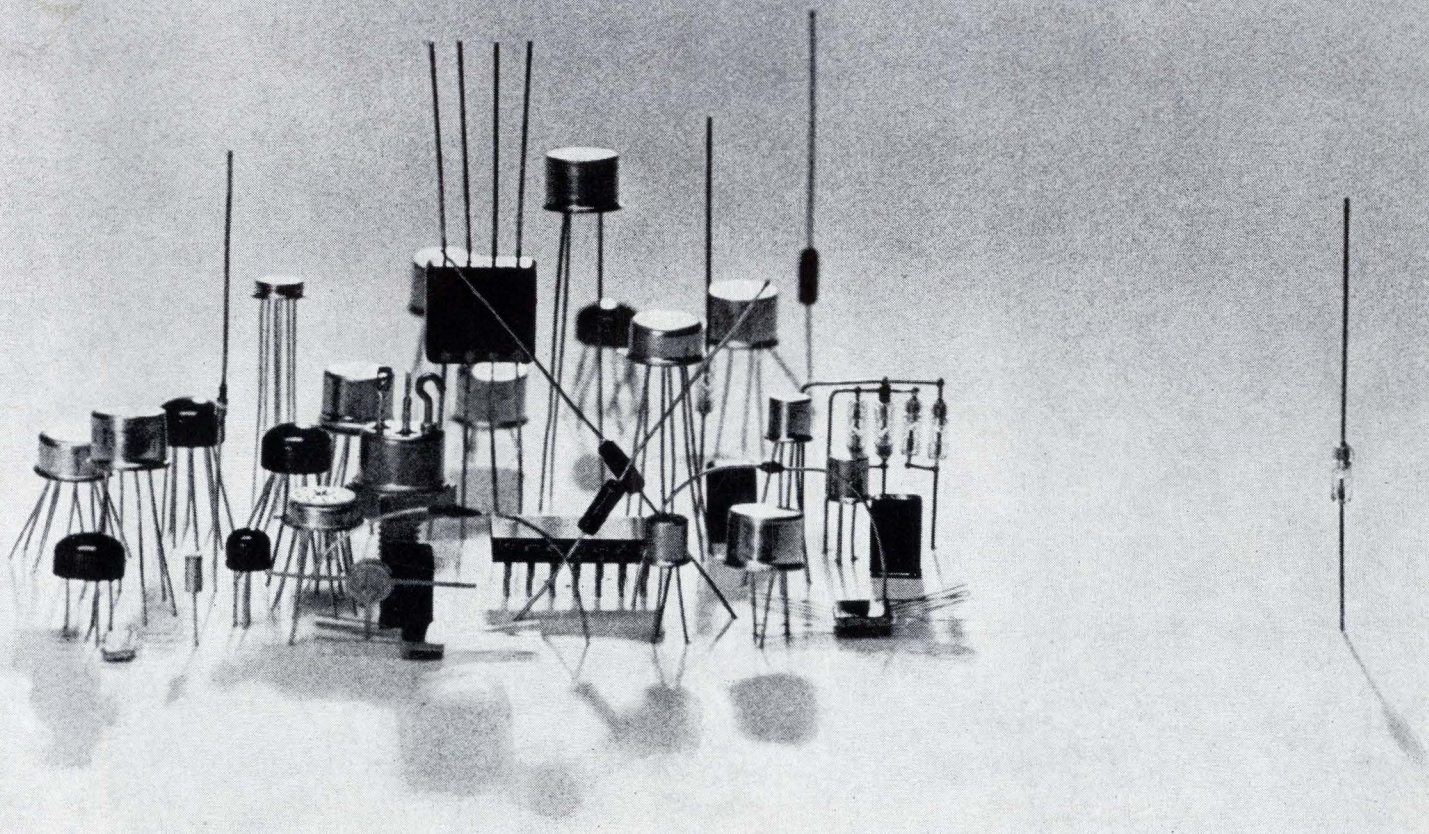

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