November, 1977

Getting Small: Microcomputers

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Digital Design

The Magazine of Digital Systems

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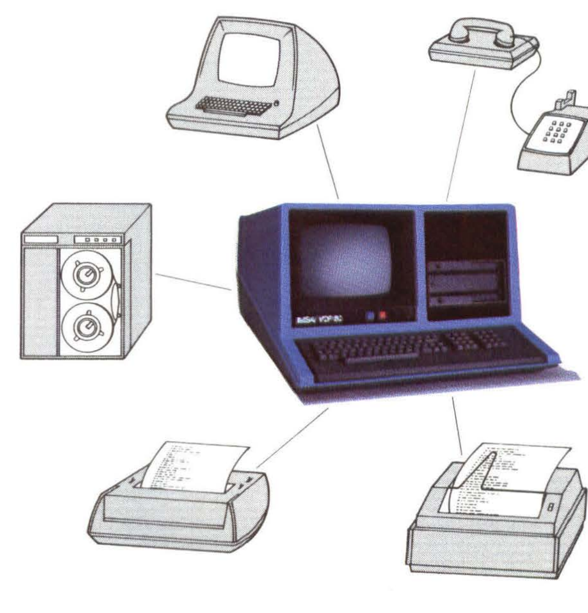

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PCS-80/15 (w/IKB-1)

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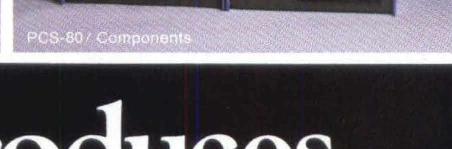

PCS-80/ Components

IMSAI introduces the PCS-80 component system...

Introducing push-button microprocessor system debugging.

HP's 1611A Logic State Analyzer... Dedicated to all 8080 or 6800 based systems.*

View program flow in mnemonics. *With CRT data and addresses selectable in either hexadecimal or octal formats and external lines in 1's and 0's.*

Maintain testing control. *LED indicators show status at all times. You can monitor system operation at normal speed or stop the microprocessor and give control to the 1611A for single or multiple keyed steps.*

Enter data quickly and easily. *The hexadecimal keyboard makes trigger and qualifier data entry as easy as operating a calculator. And the CRT display gives you a quick visual check on your entries.*

Choose your display. *Either mnemonic or absolute (op codes). Roll the display to view any 16-line slice of the 64-byte memory.*

Pinpoint virtually any specific event. *Trigger on address, data, or external signals... or on any combination of the three. You can also qualify the trigger by bracketing the address and opting to trigger on the nth occurrence of the trigger word. TRIGGER ENABLE and DISABLE keys act as arm and disarm circuits providing unparalleled pinpointing flexibility.*

Move the display window. *Delay up to 65,472 qualified clocks or memory transactions from the trigger word. Or, pre-trigger to see up to 63 bytes leading up to the trigger word (negative time).*

Obtain program and timing data. *Qualify the display with TRACE TRIGGER and see only those bytes that match your trigger inputs... all write instructions, for example. Press COUNT TRIGGERS and the 1611A displays the number of trigger occurrences between the TRIGGER ENABLE and TRIGGER DISABLE entries. Push TIME INTERVAL and you get a display of actual elapsed time between selected points in your program on your hardware.*

The 1611A should be on hand when you start up your microprocessor-based system. Imagine the time you'll save with push-button operation and an unparalleled view of your system's operation; viewing things dynamically that you never could see before. And there's more... self test; trigger outputs to drive external equipment; error messages to warn of improper operation or setup; and the choice of two initial "μP personality modules" that let you tailor the 1611A to either 8080 or 6800 based systems.

Let HP's 1611A, priced at $5,000**, help you speed development, production-line testing or service. Ask your local HP field engineer for all the details. Ask him about HP's digital seminars too. He can tell you when one will be held in your area and how you can attend.

*and more modules for other microprocessors to come.

**Domestic U.S.A. price only.

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086/15

CIRCLE 11

At only $1088, you can't offer your customers a better buy.

Our quantity-50 OEM price for the *Silent 700** Model 743 KSR Terminal is now just $1088†. In larger quantities, the price goes below $1000.

And it keeps on costing less because the real payoff is in the cost of ownership. In the long run, it costs less than any other printer terminal with comparable performance.

The reason is easy. Superior design. The 743 KSR is built around a TI microprocessor. So, there are fewer components and circuit boards than in other printer terminals. That means less maintenance and more uptime performance. Plus standard EIA and current loop interfaces in a lighter, desk-top package.

The 743 features the speed, reliability and quietness that made the *Silent 700* terminal family so popular. Incoming data is buffered, so you get true 30 characters-per-second throughput.

TI's Model 743 KSR

Disturbing noises associated with impact printers are eliminated with the 743's non-impact electronic printing.

Use it as a console I/O for software development. Keyboard terminal for inquiry/response. Data entry. Interactive remote computing. Or as a message terminal network. And it's now available with APL.

The 743 is backed by TI's worldwide maintenance and support services.

Find out more about TI's 743 KSR printer terminal. Fill out and mail the coupon today. Or call your nearest TI sales office, or Terminal Marketing, (713) 494-5115, extension 2126.

TEXAS INSTRUMENTS
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Yes! I am interested in the 743 KSR Printer Terminal.

silent 700
electronic data terminals

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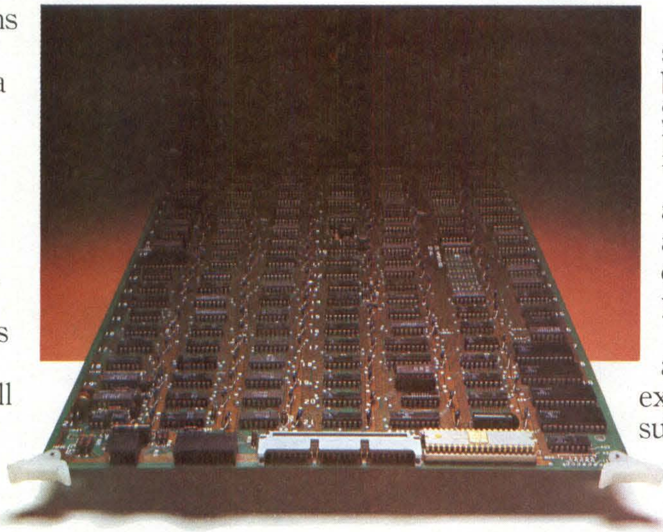
TEXAS INSTRUMENTS.

Sperry Univac's new mainframe-on-a-board: What you do with it is your business.



Whether your systems business is scientific, instrument control, or data communications, know this:

Our new V77-200 delivers more computing power than any other computer-on-a-board you can buy. Handling up to 32K/16-bit words of 660ns MOS memory.

Reason enough to call it the world's first mainframe-on-a-board. But there's more.

Because our new V77-200 comes loaded with "big machine" features. Like 8 programmable registers with byte, word and double word manipulation. Up to 32-bits of arithmetic precision. A powerful set of 187 instructions. Hardware multiply/divide. Direct memory access. Programed I/O. Multi-device automatic program loaders. A real-time clock. And a teletype/CRT controller. All standard. And all on a single 10.8″ x 17″ board.

There's even Virtual Console Logic that eliminates the need for a programmer's console by allowing you to control the V77-200 from a teletype or CRT keyboard.

You get "big machine" performance, too. Example: a microinstruction cycle time of 165ns that allows multiplication functions to be handled in just 4.9 microseconds—divide in just 8.

Plus your choice of OEM-tailored options. Like a variety of connector planes and general purpose interface boards for custom I/O designs. Three different 660ns memory boards (in 8K, 16K, and 32K-word modules). An operator's console. Power-fail detect and data save. Memory parity. Hardware for up to 64 priority vectored interrupts. An integral or modular power supply. And a system chassis. All the "unbundled" pieces you need for quick and easy system integrations.

The new V77-200 also saves you time and money by allowing you to use Sperry Univac's well-established floppy or disk-based VORTEX real-time operating system. In effect, allowing you to concentrate on the development of your application software.

And giving you access to Sperry Univac's extensive library of software subsystems, language processors, and system utilities.

Best of all, the world's first mainframe-on-a-board has a base price of just $1200. Plus a discount plan designed to give even modest-volume OEM buyers a big break. And you can take delivery in a matter of days—not months.

No matter how you configure it, the new V77-200 is the most economical Sperry Univac yet. Delivering the kind of price/performance value that just makes good sense. No matter what business your systems are in.

For more information on the world's first mainframe-on-a-board, please contact: Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, P.O. Box C-19504, Irvine, California 92713, Telephone (714) 833-2400.

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CIRCLE 6

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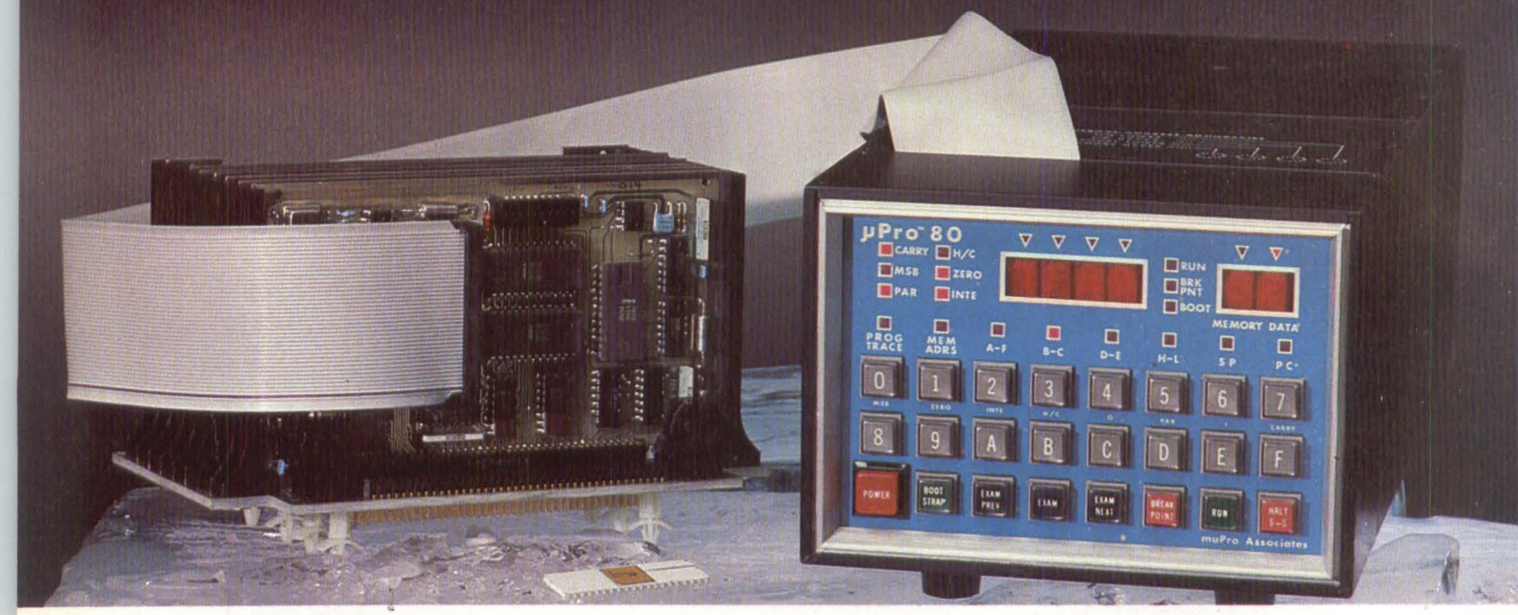

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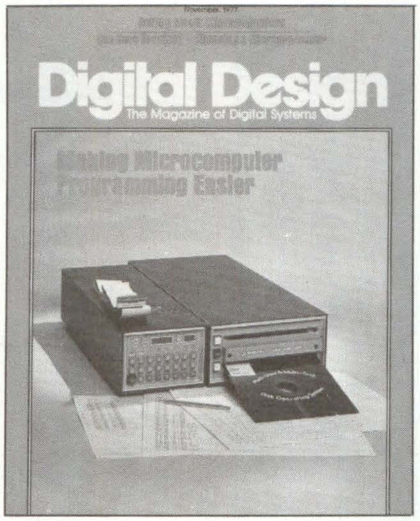
THIS MONTH

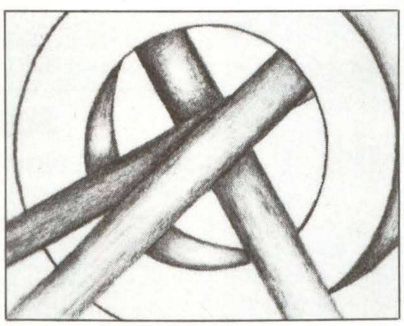
Features

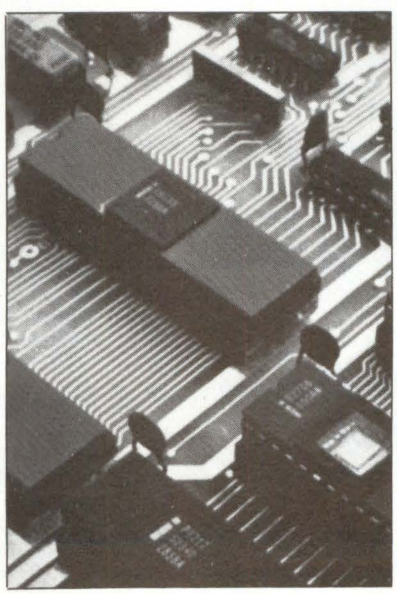


November, 1977

Vol. 7 No. 11

Diskette operating systems can enhance microcomputer capabilities; MuPro's MUTE system gives additional power and flexibility that reduce debug time. Cover design by Mike Barisano.





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Floppy Drive Innovations: Challenging Hard Disks

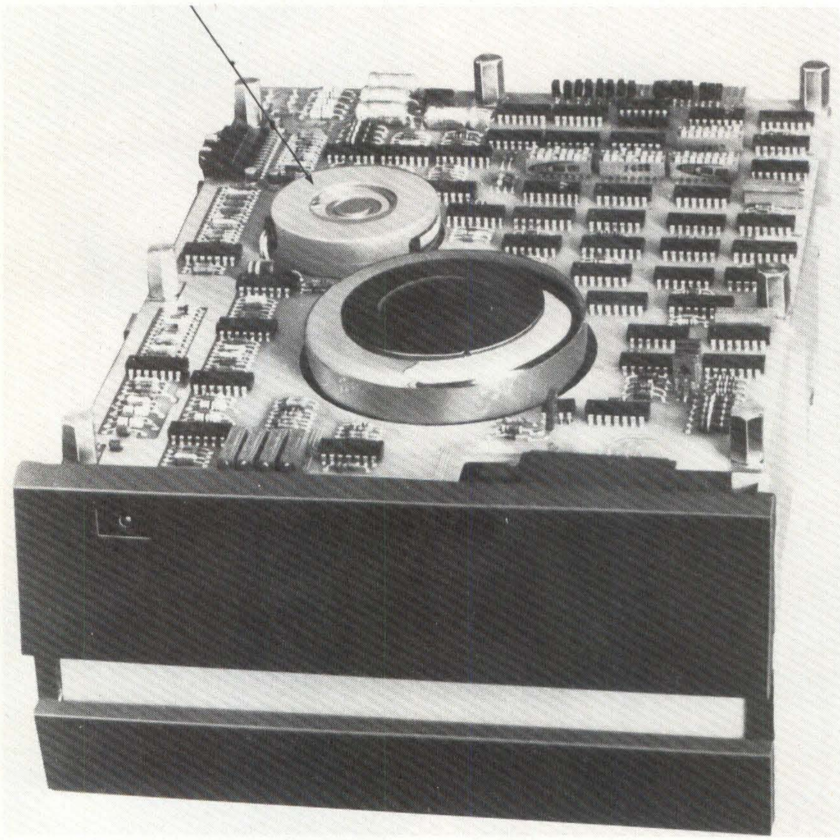


Fig 1 Top view of the 800 diskette drive shows central location of the stepper motor.

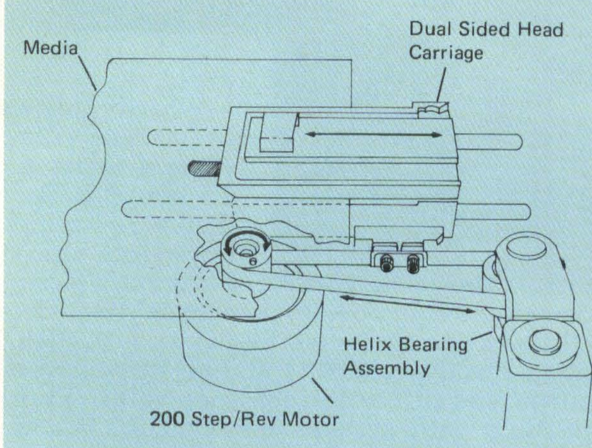


Fig 2 The head positioning mechanism of MFE's 700 Series floppy disk drive uses their Heli-Band™ mechanism to link the stepper motor to the head carriage.

Advances in the state-of-the-art in digital systems components – often thought of only in terms of *electronic* progress – frequently come as a result of *mechanical* innovation. This mechanical innovation does not necessarily mean new technologies or new devices; it can just as easily be the result of a new parts orientation or substitution of one component for another. These types of changes are responsible for much of the progress in peripheral device technology, particularly for printers, plotters, CRT terminals and disk and flexible disk drives.

Flexible disk, or floppy, drives typically house a spindle motor for spinning the disk and a stepper motor-based system that positions the read/write head. MFE Corporation of Salem, New Hampshire, claims that their recently introduced 700 Series double-sided flexible disk drive runs at low power with greater head positioning accuracy and higher MTBF because of mechanical changes they introduced in both the spindle motor and the positioning system.

Most floppy drives use an AC synchronous induction motor that typically consumes about 80 to 100 watts. MFE designers replaced the AC motor with a DC brushless motor that, according to Jim Bartley, Sales Manager for MFE's OEM digital products, operates at higher efficiency than AC motors, thus reducing power consumption. In addition, an electronic circuit automatically drops the voltage supplied to the stepper motor whenever it is not stepping. The resulting power consumption averages 30 watts in typical random operation.

Most floppy drive designers put the stepper motor at the rear of the unit. To increase thermal stability, and to allow the unit to fit in a smaller space, MFE engineers located the stepper motor at the center. Because of this motor relocation, the 700 Series measures 8.7″ x 4.35″ x 12″, making it the

CIRCLE 9 ▶

smallest currently available double-sided flexible disk drive, according to Bartley. This size savings permits rack-mounting four units vertically in the space that two units take up horizontally. The entire package can even fit comfortably in the base of a CRT terminal, thus becoming the mass storage device for an intelligent terminal or desktop computer.

Another mechanical change MFE designers introduced with the 700 Series is what they call the Heli-Band mechanism for head positioning. Flexible disk drives typically use a stepper motor with a lead screw for their positioning system, a method that suffers from high error rates and initial alignment problems. According to MFE, the Heli-Band, which gives a track-to-track access time of 3 ms, has greater accuracy than other band designs. Dave Dunn, Engineering Manager for the 700 Series, says that this accuracy improvement results from locating the stepper motor in the center of the unit, near the spindle itself. Dunn points out that the consequent compression of the positioner reduces expansion, thereby improving thermal stability. He also emphasized that the Heli-Band design offers a significant maintenance advantage: you can easily replace the entire head/carriage mechanism or the band in minutes, whereas in some other designs, to replace the carriage or the band, you must also replace the entire positioning mechanism.

The 700 Series allows double-density, double-sided recording, permitting storage of up to 12.8 megabits per flexible disk. Using double ceramic read/write heads and ceramic load pads in the carriage mechanism eliminates trouble-prone felt pads, and, according to Bartley, extends head life beyond 4×10^7 wear revolutions.

Bartley points out that the 700 drive provides a wide range of factory-installed options, including separated data and separated clock for single density applications, activity lights to indicate unit selected or head loaded, write protect sensor. Among the options that the design allows you to install: daisy chain interface, radial ready allowing each drive to have ready monitor simultaneously, and a power saver for the DC spindle drive.

Can flexible disks challenge hard disks in most applications? Dunn foresees the higher reliability and increased storage capability of newer units like MFE's 700 Series giving "the hard disk a run for the money."

For further information, contact MFE Corporation, Keewaydin Drive, Salem, NH 03079. (603) 893-1921.

Circle 169

Development System Bus-Connects To Prototypes

In the September issue of **Digital Design,** Greg Miller of Tektronix Corp. explored the role of microprocessor development systems in the testing and debugging of prototypes of microprocessor-based products. One such system, developed by Arthur D. Little (ADL) of Cambridge, Massachusetts, was originally conceived and developed to meet the needs of the company's staff. However, the growing use of microprocessors in industrial and consumer products has created a growing need for development systems; because of this, ADL welcomes inquiries about this system and customized versions.

A primary design goal for the system, according to Dr. David Curtis, Manager of ADL's Electronic Systems Section, was to allow testing and debugging of systems that did not have I/O ports. These systems, once designed using the 'random logic' approach, include such special-purpose devices as controllers for washing machines. This type of product poses unique problems for the microprocessor system designer; because there are no ports for peripherals, problems exist in loading applications software, running it, and diagnosing and correcting hardware and software faults.

Also important in the design of ADL's Microprocessor Development Support System (MDSS) is the capability to monitor and control the prototype in real-time. Curtis points out that many development systems that use emulation techniques cannot run in realtime; they incorporate an external processor that may replace a single prototype microprocessor instruction with several emulator instructions. Because the MDSS does not replace the microprocessor, but instead hooks directly into the prototype bus, the test unit does not generate timing problems.

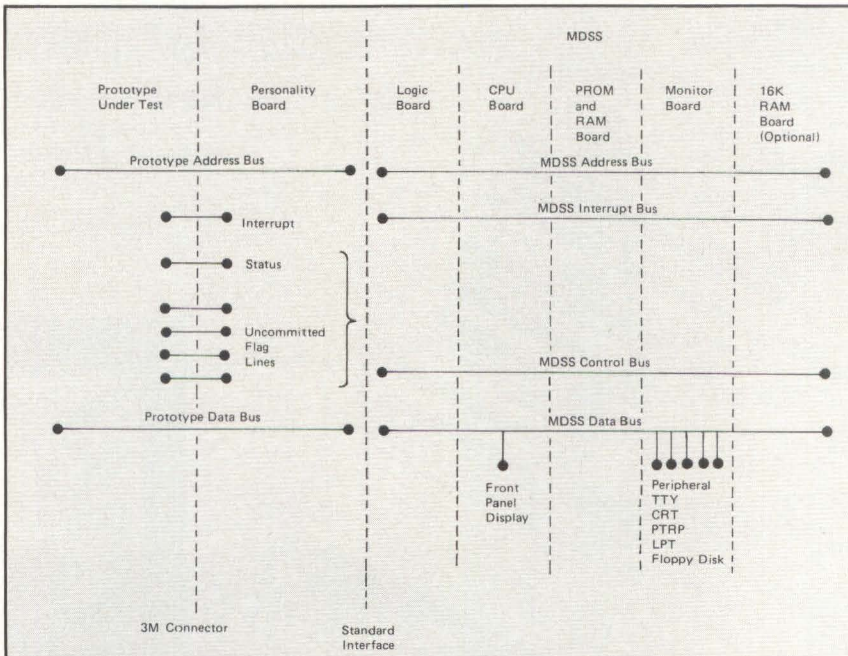
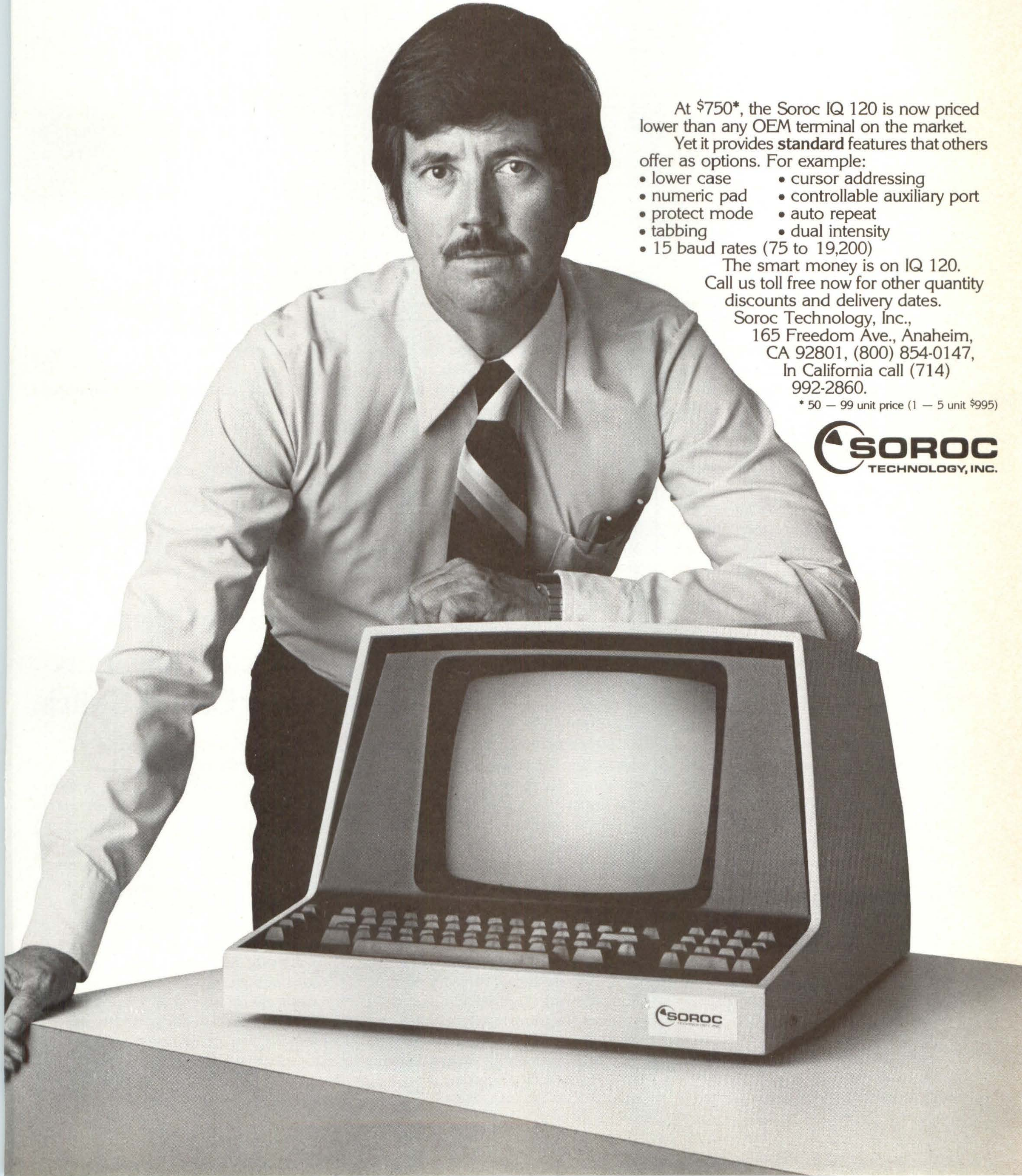


Fig 1 Internal and external bus connections for Arthur D. Little's Microprocessor Development Support System.

Why settle for less when nothing costs less?



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* 50 — 99 unit price (1 — 5 unit $995)

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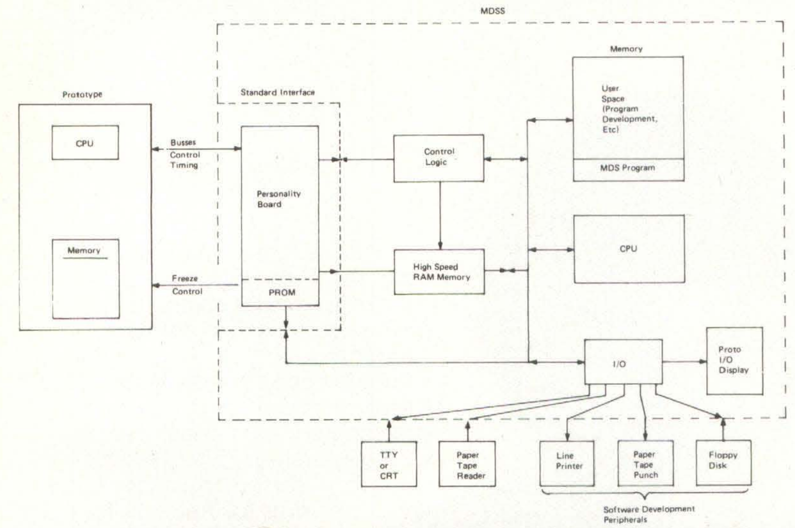

Fig 2 This block diagram shows the basic structure of the development system.

Through the use of personality boards, the MDSS can easily adapt to any microprocessor; boards currently available serve the Intel 8080, National Semiconductor's Pace and the Motorola M6800 series. ADL plans to add additional interface boards to handle other microprocessors.

The MDSS features interactive operation; you can monitor and control the operation of the prototype in real-time using a teletype or CRT terminal connected to the MDSS. Curtis says that this allows rapid determination of the running conditions of the prototype under test. You can alter these conditions via prototype program changes (using MDSS commands) and then re-execute the modified program.

Two types of commands assist you when using the development system. Monitor commands allow you to examine the operation of the prototype in real-time under control of the prototype's internal software. Intercommunication commands, also known as Buswatcher commands, allow you to examine or modify data in the prototype memory and registers.

Typical Operation. The prototype links to the MDSS via a flat cable, connecting the prototype's address bus and data bus to the personality board. Loading the assembled software into the prototype's RAM activates the prototype hardware. The use of RAM rather than PROM permits immediate corrections to the data or program. Loading can most easily be accomplished by reading the object code file, existing on paper tape or in mass storage, into the prototype microprocessor memory through peripherals associated with MDSS.

The PUT command loads the program into prototype RAM; you can then use the EXECUTE command to run the actual applications program. The TRACE command causes the MDSS to store each operation of the prototype in high-speed RAM for later retrieval by the MDSS processor, thus allowing uninterrupted real-time operation of the prototype while providing information on as many as 63 sequential prototype microprocessor bus operations. You can review the program in operation after the fact, even if only one run has taken place.

After recording a desired prototype instruction sequence, the MDSS can automatically print out the data, or else display it on a CRT. The print-out or display operation can be controlled by four variations of the TRACE command. A STEP command, following a FREEZE-at-address command, forces the prototype to execute one instruction at a time, thus providing more detailed analysis. The GET command gives you the capability to examine the prototype memory following execution, allowing you to determine whether the correct program is installed and whether the instructions have been modified by incorrect program operation or which data is present in the prototype. You can investigate I/O problems with the aid of the I/O DISPLAY command; this command causes continuous display of input or output data.

By incorporating suitable electronics, you can also test the prototype while the input ports are exercised, allowing system debugging in a working environment.

Curtis points out the utility of the MDSS: he comments that "with the inevitable proliferation of microprocessor-based products, the MDSS is especially significant and timely. Not only are no two microprocessors of different manufacture alike, but even the same model produced from different sources can diverge in software and hardware performance. For this reason, a universal testing and debugging instrument that accommodates itself to the differences and idiosyncracies of diverse microprocessor systems is a necessity to avoid chaos and the waste of literally thousands of hours of plant and laboratory work. The MDSS was designed, and is offered, with these factors in mind."

For further information about the Microprocessor Development Support System, contact Arthur D. Little, 25 Acorn Park, Cambridge, MA 02140, (617) 864-5770.

Magnetic Circuit Protector Doubles as Power Control Switch

Designers and manufacturers of control and distribution panels for marine and medical equipment, power supplies, data processing, instrumentation and many other systems continually search for smaller, less expensive components that help simplify circuit design, increase packaging density and reduce manufacturing costs, while providing better product life cycle economies for the end user.

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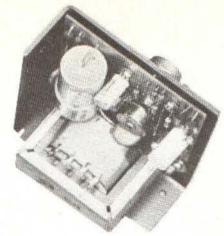

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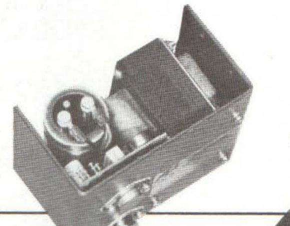
APS 6-2.5	6	2.5	±0.05%	±0.1%	3mV	OV1-63	10-24	32.20	6.70
APS 12-1.6*	12	1.6	±0.05%	±0.1%	3mV	OV1-122	25-49	30.70	6.40
APS 15-1.5*	15	1.5	±0.05%	±0.1%	3mV	OV1-152	50-99	29.20	6.05
APS 20-1	20	1.0	±0.05%	±0.1%	5mV	OV1-201	100-249	27.00	5.70
APS 24-1*	24	1.0	±0.05%	±0.1%	5mV	OV1-241	250-499	25.20	5.25
APS 28-0.8*	28	0.8	±0.05%	±0.1%	5mV	OV1-281			

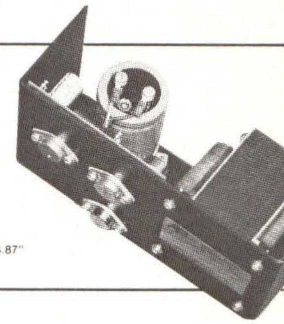


DIMENSIONS: 5.62"x3.40"x4.87"

30 TO 60 WATT "GREEN HORNET" SERIES. †U.L. Recognized (File No. E58512)

MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 48-1	ALL OTHERS	
APS 5-6†	5	6.0	±0.05%	±0.1%	OV2-56	1-9	68.00	55.00	15.00
APS 6-5	6	5.0	±0.05%	±0.1%	OV2-65	10-24	64.75	52.10	14.40
APS 12-4†	12	4.0	±0.05%	±0.1%	OV2-124	25-49	61.75	49.65	13.75
APS 15-3†	15	3.0	±0.05%	±0.1%	OV2-153	50-99	58.75	47.25	13.05
APS 20-2.4*	20	2.4	±0.05%	±0.1%	OV2-203	100-249	55.15	44.35	12.25
APS 24-2.2*†	24	2.2	±0.05%	±0.1%	OV2-245	250-499	50.75	42.00	11.30
APS 28-2*†	28	2.0	±0.05%	±0.1%	OV2-284	500-999	49.60	40.00	11.05
APS 48-1*	48	1.0	±0.05%	±0.1%	OV2-481				

* RIPPLE: (PK/PK) 5mV. All others 3mV.



DIMENSIONS: 9"x3.65"x4.87"
APS 5-18 DIMENSIONS: 14"x3.65"x4.87"

50 TO 120 WATT "BLACK BEAUTY" SERIES. *U.L. Recognized (File No. E58512)

MODEL NUMBER	RATING		OVP MODEL SUFFIX	POWER SUPPLY PRICES					OVP PRICES
	Vdc	Amps		QTY.	APS 5-9	APS 5-12	APS 5-18	ALL OTHERS	
APS 5-9	5	9	OV2-510	1-9	71.00	85.00	108.00	75.20	15.00
APS 5-10*	5	10	OV2-510	10-24	66.74	80.55	101.45	71.30	14.40
APS 5-12	5	12	OV2-512	25-49	63.90	76.80	96.70	67.95	13.75
APS 5-18	5	18	OV2-518	50-99	61.05	73.00	91.95	64.60	13.05
APS 12-7*	12	7	OV2-127	100-249	57.30	68.55	86.35	60.65	12.25
APS 15-6*	15	6	OV2-156	250-499	52.75	65.00	79.45	55.80	11.30
APS 24-5*	24	5	OV2-245	500-999	51.60	57.90	77.70	54.60	11.05
APS 28-4*	28	4	OV2-284						

REGULATION: LINE +0.05% Load +0.1%. RIPPLE (PK/PK): 3mV on 5, 12, 15V models. 5mV on 24, 28V.

DIMENSIONS: 16.72"x4.87"x6.60" Max. APS 5-30 only.
All others 16.72"x4.87"x5.75"

125 TO 250 WATT "BLUE MAX" SERIES.

MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 5-30	ALL OTHERS	
APS 5-25	5	25	±0.05%	±0.0.1%	OV3-525	1-9	163.00	158.00	25.00
APS 5-30	5	30	±0.05%	±0.0.1%	OV3-530	10-24	154.65	149.95	24.25
APS 6-22	6	22	±0.05%	±0.0.1%	OV3-622	25-49	147.45	142.95	23.15
APS 12-17	12	17	±0.05%	±0.0.1%	OV3-1217	50-99	140.20	135.90	22.00
APS 15-15	15	15	±0.05%	±0.0.1%	OV3-1515	100-249	131.65	127.60	20.65
APS 20-11	20	11	±0.05%	±0.0.1%	OV3-2011	250-499	121.10	117.40	19.00
APS 24-10	24	10	±0.05%	±0.0.1%	OV3-2410	500-999	118.50	114.85	18.60
APS 28-9	28	9	±0.05%	±0.0.1%	OV3-289				

RIPPLE (PK/PK): 3mV on 5.6.12.15V models. 5mV on 20.24.28V models.

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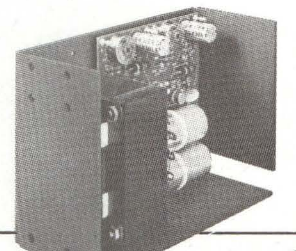
DUAL OUTPUT MICROPROCESSOR SERIES U.L. Recognized (File No. E58512)

MODEL NUMBER	RATING		QUANTITY PRICES					
	Vdc	Amps	1-9	10-24	25-49	50-99	100-249	250-499
DAPS 5.8	±5	0.8	43.00	40.70	39.80	38.00	36.80	33.00
DAPS 9-12.5	±9-12	0.5	43.00	40.70	39.80	38.00	35.80	33.00
DAPS 12-.75	±12	0.75	43.00	40.70	39.80	38.00	35.80	33.00
DAPS 15-.60	±15	0.06	43.00	40.70	39.80	38.00	35.80	33.00
DAPS 5112.5	+5 -12	1.0 0.5	43.00	40.70	39.80	38.00	35.80	33.00
DAPS 12-1.5	±12	1.5	59.00	55.90	53.30	50.65	47.60	43.80
DAPS 15-1.3	±15	1.3	59.00	55.90	53.30	50.65	47.60	43.80
DAPS 53121.5	+5 -12	3.0 1.5	59.00	55.90	53.30	50.65	47.60	43.80

REGULATION: +0.05% Line, +0.1% Load. RIPPLE (PK/PK) 3mV.



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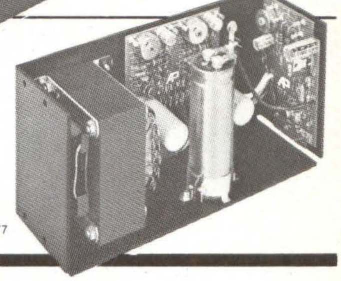
MODEL NUMBER	RATING		QUANTITY PRICES					
	Vdc	Amps	1-9	10-24	25-49	50-99	100-249	250-499
TAPS 1	5V ±9-12*	4.0 0.5	94.15	89.20	85.05	80.85	75.90	71.00
TAPS 2	5V ±9-12*	6.0 1.0	107.00	101.60	96.85	92.10	89.00	87.50
TAPS 3	5V ±9-12*	9.0 1.5	137.00	129.80	127.80	125.00	123.75	113.85
TAPS 4	5V ±9-12*	12.0 3.0	168.00	159.00	151.50	149.00	148.00	147.00

* Also available with +12-15V output. Specify if desired. REGULATION: +0.1% Line, +0.1% Load. RIPPLE (PK/PK): 5mV



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CIRCLE 12

ponents: a fuse, a fuse holder and a separate power control switch, plus the necessary wiring to complete the circuit. According to the firm, T11 has the benefits of magnetic circuit protectors – long life, positive resettable operation, high current switching and tailorable delay-to-operate features.

T11 configuration – single pole, single throw series trip with the load being protected, comes with a choice of paddle handle colors. According to Airpax, it's the smallest magnetic protector available, being about one half the size of devices that handle comparable loads.

How the T11 Works

Through linkage, the paddle handle positions a carrier to initiate both the opening and closing of the switch contacts. In either case, carrier position causes an over center spring to control a movable contact bar.

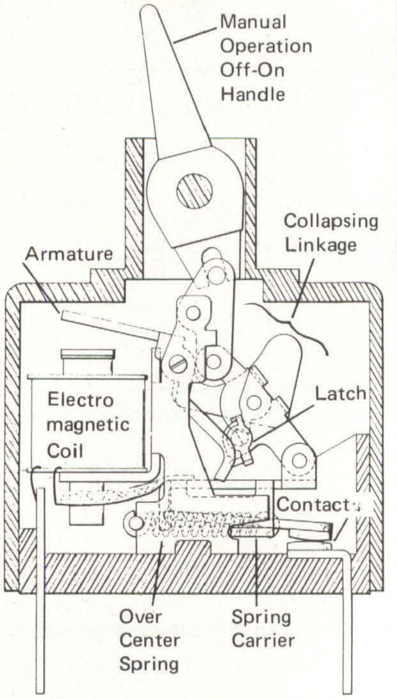


Fig 1 This drawing of the power switch/magnetic protector shows the paddle handle in the ON position, and the contacts closed.

When opening the contacts manually, the paddle handle position causes rotation of the carrier until the over center spring passes through the horizontal line of the contact bar. Instantaneously, the spring opens the contacts

◀CIRCLE 13

with a snapping action. Positioning the paddle handle in the ON position reverses the contact snap action.

In the event of overcurrent, the circuit protector responds to open the contacts. An electromagnetic coil senses overcurrent, and attracts an armature; the movement of the armature trips a latch that unlocks the collapsible linkage. Unlatching the collapsible linkage cancels out the ON position of the paddle handle. A spring initiates carrier movement to duplicate contact opening action as previously described.

To reset, after removing the overcurrent situation, you return the paddle handle to the ON position, and the contacts close. Because of the snap action, the T11 contacts can't be "teased" or "kissed." This helps eliminate the problems of arcing and contact wear and erosion to further increase contact life.

An added benefit, useful where loads are dc or inductive, is the quick, wide opening of the contacts. Normally, open switch contact gap is about 0.010 to 0.015 inch, according to the firm. The T11's open contact gap is 0.280 inch – 20 times as much, permitting the contacts to handle higher currents and increasing contact life.

By selecting specific delays, you can get a choice of trip responses and inrush tolerances. Time delays and therefore the time to trip the latch, brought about by the movement of an iron core in viscous oil, depend on the speed of the iron core movement, which in turn depends on the amount of overcurrent and the oil viscosity (usually silicone oil).

Current rating and trip curves easily adapt for close correlation with the needs of mixed loads, matching them to wiring, PC boards, motors, transformers, lights and other components. The switch/protectors cost under $5.00 each in quantities of one to twenty-four. Similar savings apply for higher quantity purchases. Airpax Electronics, Cambridge Division, Cambridge, MD 21613.

Computer to Speed Production of Braille Literature

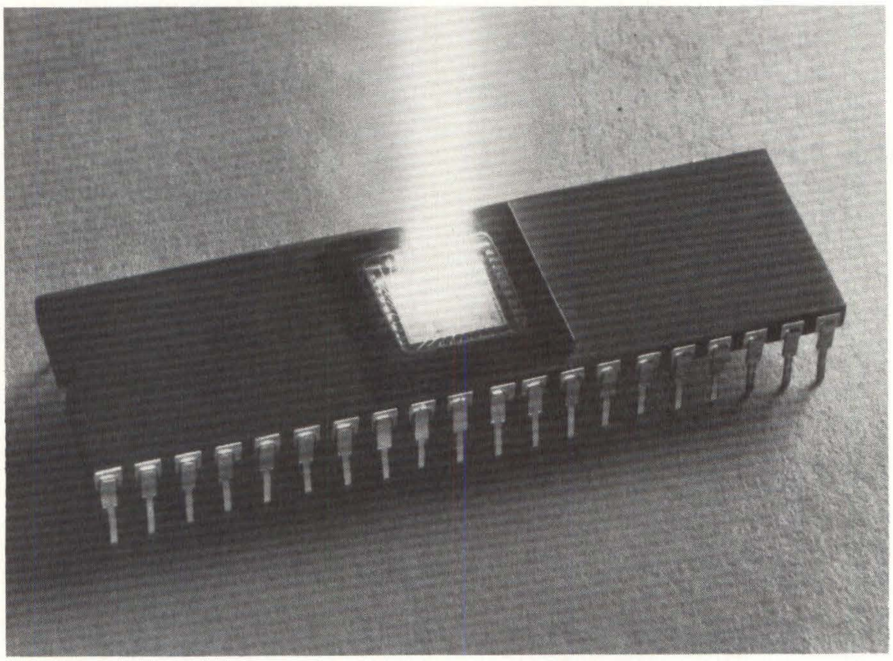
A GEC 4070 computer and related equipment for use in the production of braille literature will be installed by the Royal National Institute for the Blind in London. Part of a plan that will make RNIB's work in this field the most advanced in the world, the computer equipment will be used in a new printing center to speed publication of a greatly increased range of braille books and periodicals for educational, vocational and recreational purposes, according to the firm.

Operators at 16 text-entry visual display terminals will key in text from English originals. The computer system will directly accept these inputs and translate the data into braille output coded onto magnetic tape cassettes. These are used to control embossing machines which automatically punch the braille characters (called cells) onto zinc plates suitable for use on a printing press. Alternatively, for single copies of a document, the computer can itself drive a paper embosser, thus eliminating the need to manufacture a metal printing plate. The use of visual display units as input terminals gives the operators the facility to edit text on entry. Separate purpose-built refresh graphics display terminals are used to edit the braille cells prior to commiting the output to embossed paper or zinc.

The GEC system will replace an existing system which uses punched cards as the text input medium. Contained in the GEC configuration are two GEC 4070 central processors, each with 192 Kbytes of core store, four 4.8/4.8 Mbyte fixed/exchangeable cartridge disks, two 300 1pm line-printers, two 9-track 800 bpi magnetic tape units, four digital input/output devices, two control thermal printers, paper tape station, four cassette decks for braille coded tapes and two cassette decks for maintenance and diagnostic programs.

The GEC system will bring to the RNIB benefits in speed gained through improved editing, economy and throughput.

Choosing Microprocessors For Reduced Parts Counts



by
Frank Lunch
and
Clay Showen

Faced with selecting a microprocessor for a control application, today's designers choose between three alternative devices: a fixed-instruction MOS chip, a bipolar bit-slice chip or a fixed-instruction bipolar chip.

The first alternative, a fixed-instruction MOS microprocessor such as the 8080, was originally developed for low-level applications that do not require high-speed operation. Systems designers have used these chips in controllers, but not without paying the penalty of adding components to overcome the inherent MOS speed limitation.

The second alternative, a bipolar bit-slice microprocessor such as the 2901, was designed to emulate minicomputers. Well suited to preserving existing software, this high-level emulation does little to simplify circuitry for lower-level control applications. To implement the bit-slice device, the designer must not only define a microprocessor architecture, but create an instruction set.

When it comes to high-speed control applications, no microprocessor can match the combination of high-speed performance and ease of implementation offered by the third alternative, the fixed-instruction bipolar chip. While designers recognize more and more the attributes of this single-chip bipolar Schottky device in the controller market, little has been said about the hidden savings its exceptional operation speed (4 million operations/second) brings to overall system development cost.

Significantly, the operating speed allows several critical functions, which might otherwise be handled with external components, to be performed on-chip. Although the need for fewer parts may save money, the lower parts count during the manufacturing stage provides the major cost savings. Fewer components mean less handling and inventory, reduced assembly and testing, low power consumption and improved reliability.

This microprocessor is ideally suited for numerous control applications, including tape/disk controllers, CRT keyboard terminals and communications concentrators/demultiplexers. Whenever the device satisfies the need to move and interpret data at high speeds, it usually provides savings resulting from reduced parts count.

For example, consider a communications controller. In this case, a fixed-instruction bipolar Schottky device, such as the Signetic 8x300, provides an order of magnitude greater throughput over that possible with a typical MOS microprocessor. The higher baud rates achievable with the 8x300 often allow you to completely eliminate the need for UART's

and baud-rate generators – while substantially reducing the number of interface circuits required.

A similar savings results from implementing a CRT controller with the 8x300; in this case the microprocessor eliminates the UART and keyboard encoder because it handles these functions on-chip.

Let's now examine more closely the hidden economics of microprocessor speed by taking a specific example, such as a double-density floppy disk controller. And let's compare an 8x300 implementation with three alternate approaches.

Double-Density Floppy Disk Controller

To evaluate the benefits derived from microprocessor speed, compare an actual 8x300 design of a double-density Floppy Disk Controller (FDC) with three other microprocessor implementations, namely: MOS, bi-polar bit slice and standard bipolar TTL.

As the electronic link between a minicomputer and floppy disk drive, the FDC manages disk mechanics, formats data and frees the minicomputer (host processor) from many tasks, such as copy, search and autoretry. Since the introduction of the IBM 3740, the first industry standard, the FDC has become considerably more powerful – both in control features and recording formats. For example, the Shugart 3800 uses a M^2FM encoding format to double the recording density of the IBM 3740. An advance such as this one places heavy time constraints on FDC design, particularly when you consider that a double-density FDC needs to transfer data at 500 kbits/s, while handling the other routine tasks related to disk subsystem management.

Design Guidelines. There are several major time-critical functions that double-density FDC must perform. The response/resolution times dictate the boundaries of our design implementations.

To create a common base for design comparison, first partition the time-critical functions into blocks of minimum complexity. If a general-purpose LSI device can handle the speed/resolution time requirements, then it is likely to provide the least complicated implementation. And if the LSI device is programmable, it probably offers the greatest design flexibility for subsequent product changes without PC board work. Accordingly, we will use discrete components only for those tasks for which speed requires dedicated hardware. Let's now analyze four implementations of double-density FDC with these common guidelines in mind.

As the central controlling element, the 8x300 provides a 250ns instruction execution time that encompasses accessing data and storing the result. Besides handling logical and arithmetic operations, the chip can rotate, mask, shift and merge data during a single instruction cycle. This capability to quickly move data at the bit level minimizes the number of FDC functions (Fig 1) requiring special-purpose hardware.

The processor contains a 8x300 CPU, a RAM for working store, a ROM for the control program and I/O bus control circuitry. Commands received from the host computer and status sent to the host are first buffered in the processor's RAM. The arithmetic necessary to map addresses between the host memory and the sector buffer takes place in the processor. Counters are maintained in RAM for bytes-per-sector, index marks, track position and autoretries. The processor also performs address mark comparison and generates the timing and control signals for the drive mechanics.

The host interface consists of dedicated hardware elements for each of the functions identified. Two Direct Memory Access (DMA) registers contain the address data for transfer to or from the host computer's memory. The address decoder and time control circuits permit the host computer to access the command and status buffers while occupying the bus for only one processor cycle. The 250ns required for a "cycle-steal" greatly simplifies meeting this requirement.

The drive interface demands the most critical timing in the double-density FDC, because the 500 kbit/s disk transfer rate results in a 2μs bit time and a 16μs byte time. These speed parameters determine the sophistication and amount of hardware needed for the drive interface. Whenever the software loop time exceeds the time allowed for a given function, it limits placing the maximum number of functions in software. For example, the command, clock-shift and data-shift registers are double-buffered. To eliminate this second set of buffers, the loop time must not exceed the byte time, and the response must be handled in a one-bit time. Bit detection for the read function and encoding and pre-compensation for the write function operate at a speed substantially less than the bit cell time of 2μs, because the mechanical drive

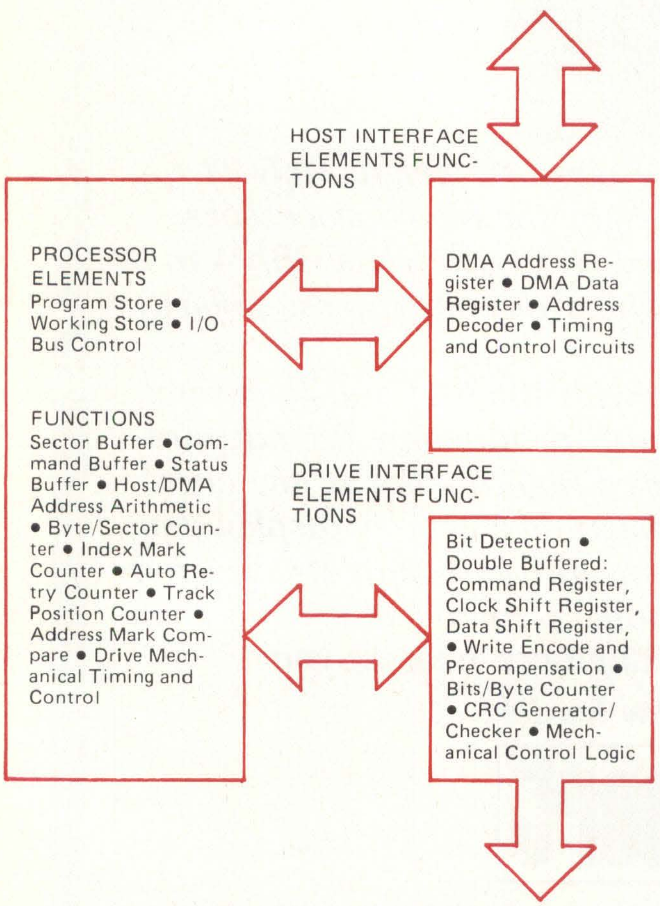


Fig 1 Block diagram of the floppy disk controller shows how the elements and functions for the 8X300 microprocessor are partitioned.

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does not maintain absolutely constant speed; the transitions which read relative to the bit cell move as a result of the recorded ones and zeros pattern. Moreover, special hardware is provided for the bits-per-byte counter and the Cyclic Redundancy Check (CRC) generator and checker. Logic also interfaces the mechanical control of the drive to the timing and control signals from the processor.

Implementing the double-density FDC with an 8x300 satisfies the design criteria. The arrangement accommodates double-density transfer rate and the host computer transfers its data under DMA control. The FDC performs all the system housekeeping functions, such as autoretry on CRC failure, disk formatting, search and seek commands.

This implementation uses only components currently available from production and requires a single +5V power supply. Support for the microcontroller includes an assembler (MCCAP) and a simulator (MCSIM) for simplifying the design process, while maintaining FDC design flexibility.

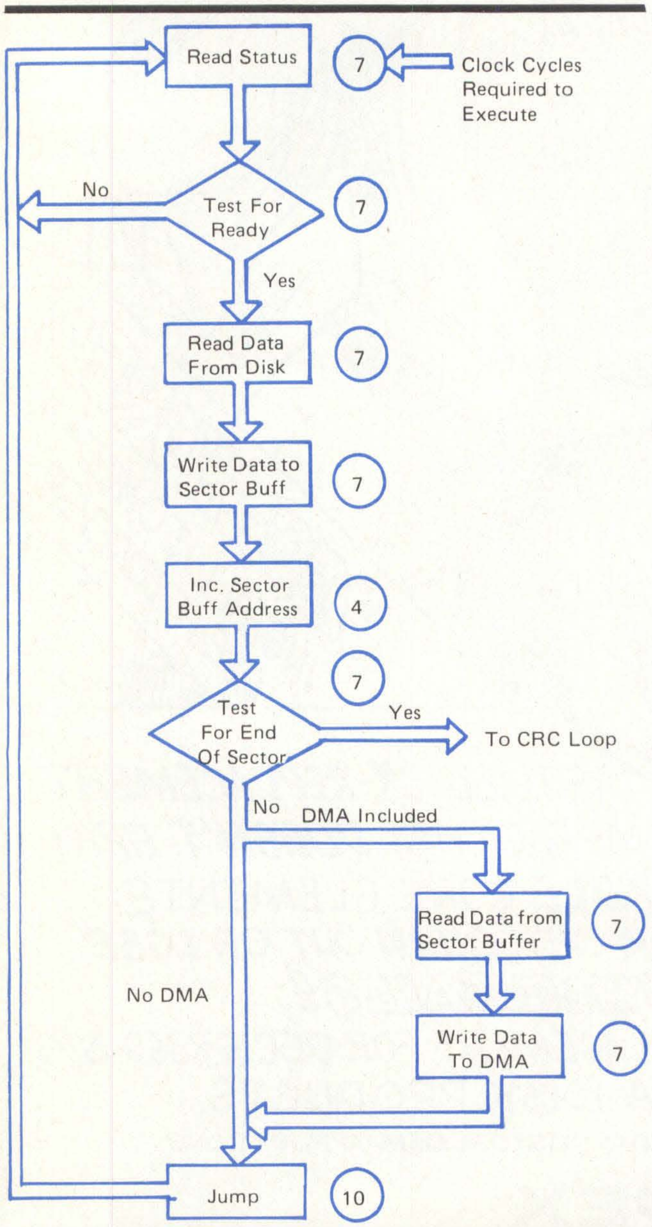

Fig 2 Program loop shows the steps taken by a MOS microprocessor-based FDC in reading data from a disk.

MOS Microprocessor. When designing a double-density FDC with an MOS microprocessor, you must begin by carefully choosing the microprocessor for speed and then using some additional MSI devices. The flow chart in Fig 2 shows some of the difficulty in choosing a MOS microprocessor. In transferring data from the disk to the sector buffer, the basic steps include reading and testing the status, reading the data from the disk, writing the data into the sector buffer, incrementing the address preparatory to the next sector buffer access, and testing the address for the end of the sector. If the sector is incomplete, the next byte is read from the disk.

The flow chart shows the simplest possible DMA transfer at this point. Data is read from the sector buffer and written into DMA logic; successive jumps back to the beginning of the loop repeat the process until completion of the sector. At that time, the test for end-of-sector results in a jump to the CRC loop.

The circled figures indicate the number of clock cycles required for a Z-80A, the fastest currently available MOS microprocessor, to go through the loop. With the DMA operation included, the clock-cycle count totals 63. Allowing for the ±2.5% drive speed variation, the amount of time available to write a byte is 15.2μs. This total requires a 240ns clock period which is lower than the minimum for the Z-80A microprocessor 4 MHz or 250ns clock cycle. Eliminating the 14 clock cycles required for DMA allows the Z-80A to complete the 49 clock-cycle loop.

To implement the DMA function, you must add two address counters for host memory address and internal RAM address, plus some miscellaneous logic to the host interface. The drive interface also requires additional parts to perform the address mark comparison. Other portions of this section are the same as the 8x300 implementation.

For the processor, higher density ROMs and RAMs of the MOS type provide some parts-count economy. In all, the MOS processor implementation requires more dedicated special-purpose logic and therefore results in a higher parts count with reduced flexibility of design. Moreover, a MOS-implemented FDC generally needs additional power supplies beyond the +5V.

Bipolar Bit-Slice Microprocessor. In the bipolar Schottky and MOS micrprocessor FDCs, the most important single design parameter is instruction execution speed. A bit-slice microprocessor could solve this problem, since its execution time is extremely fast and we could add microprogramming tailored to make the processor perform the functions desired.

Referring back to the elements and functions listed in Fig 1, we find that the speed of a bit-slice processor can reduce special-purpose hardware. In the drive interface, for instance, the two preceding implementations require double buffering of the command, clock and data registers. The bit-slice system requires only single buffering. And while it operates on information at the byte rate, it can respond within a one-bit time. It is not, however, fast enough to operate on all of the information at the bit rate. Consequently, we can eliminate only three of the six registers. This parts count reduction, however, is offset by the complex nature of implementing a multi-chip CPU; the support hardware and software for bit-slice systems are far less available than for single

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chip microprocessors like the 8x300. Programming, or more accurately, microprogramming of a bit-slice system is done frequently at the bit level. Accordingly, the system designer must not only program the bit-slice, but must design the opcode structure to be programmed.

Standard Bipolar TTL. An analysis of using standard TTL to implement an FDC leads very quickly to several simple conclusions. First, you can design a very high-speed, special-purpose controller for the floppy disk with TTL, provided that the controller is functionally restricted to simply writing into and reading from the disk drive. It performs functions essential to handling the disk medium – bit detection, serialization/deserialization, address mark comparison, CRC generation/checking and write precompensation/encoding in a manner almost equivalent to that shown in Fig 1.

When the system-oriented functions of DMA transfer begin the task of seeking and searching for data on the disk, disk formatting and autoretry after CRC failure are added to the basic control functions. As a result, the amount of special purpose hardware required to handle these functions approaches some 250 to 300 integrated circuit packages.

The second line of reasoning follows directly from the first. If this mostly special-purpose hardware is unacceptable, then why shouldn't you implement a general-purpose processor using standard TTL to handle all these control functions? Today's available devices can implement these functions most efficiently by using the bit-slice approach just described. And we have already seen that the bit-slice microprocessor is more difficult to implement than the 8x300, because it's a multi-chip CPU that lacks design support.

The Bottom Line

In comparing the four implementations of the double density FDC, the bipolar Schottky microprocessor becomes a clear choice, because its high-operating speed allows several critical control functions to be handled on-chip. Faster than MOS, and far easier to implement than a bipolar bit-slice device, the 8x300 requires fewer parts to implement a typical control task. From these advantages, you could conclude that the 8x300 suits those applications in which the control processor must function in the data path.

Summarizing the parts count for the basic functions of the four implementations just discussed, we find that the 8X300 approach requires 101 parts; the MOS system requires 116 parts; the bit-slice method requires 105 parts; and discrete TTL requires 160 parts. These parts counts, with the exception of the 8X300, arise from paper designs never implemented. The counts represent minimum estimates likely to go higher when they reach the hardware stage. The major savings in reduced parts count reside more in the manufacturing stage than in the parts cost.

Strictly on a parts count basis, a bit-slice approach may appear to be closely competitive with the 8x300. However, a fixed instruction set 8x300 offers complete design support (MCCAP and MCSIM) for a single-chip processor at a power consumption of only 1.5W. The equivalent bit-slice design, by comparison, spreads over three to four chips, consumes 5W.

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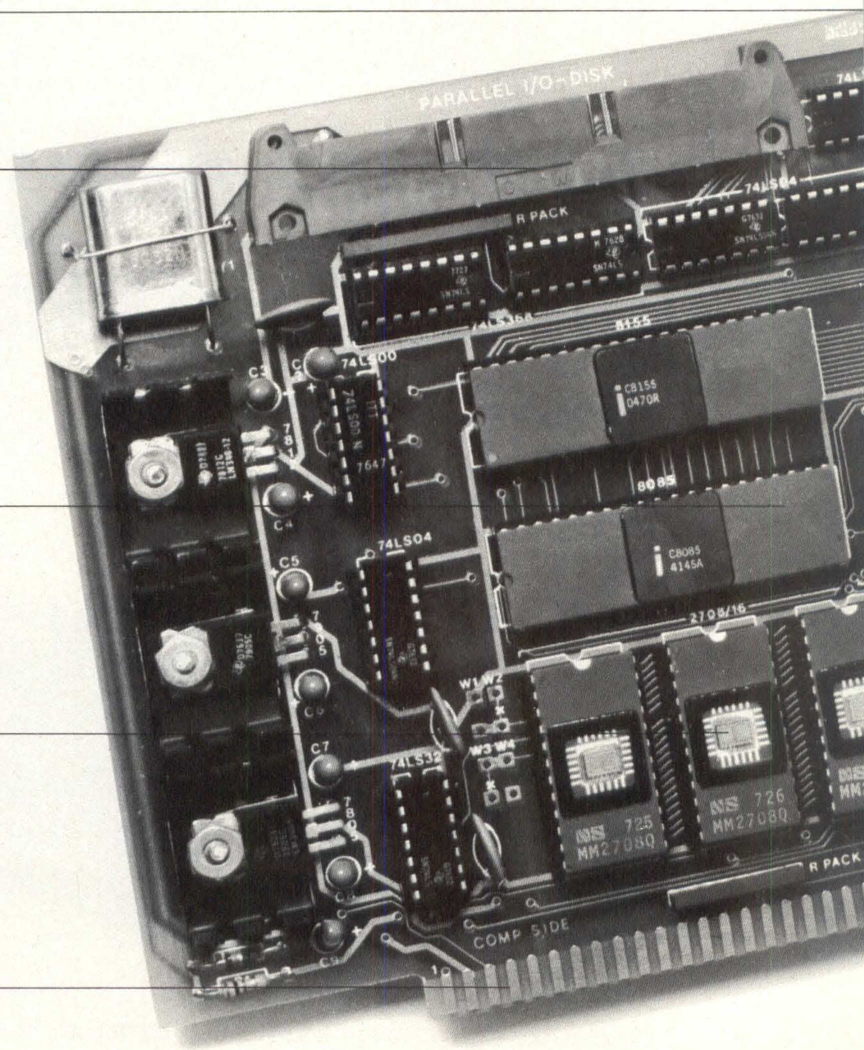

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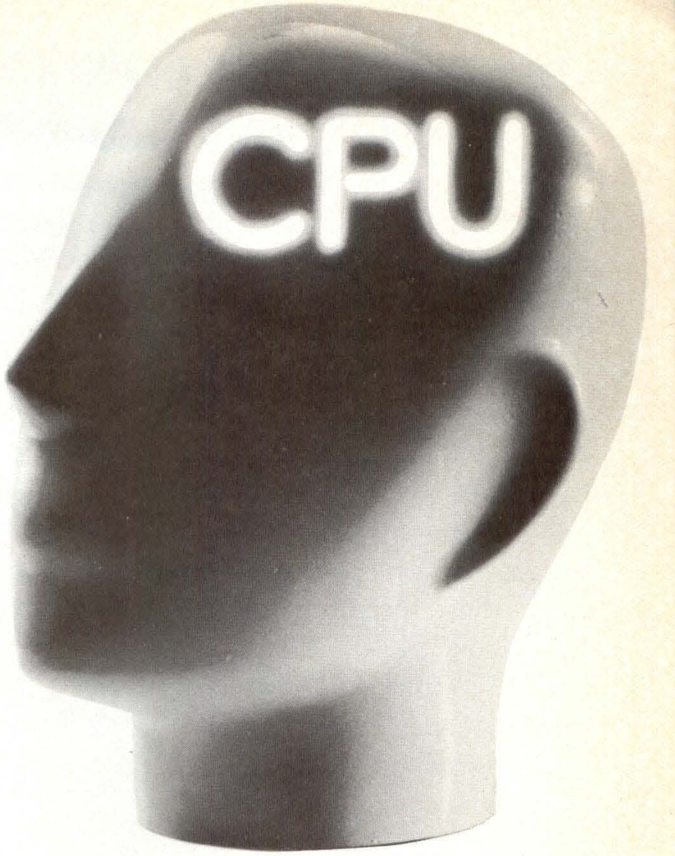

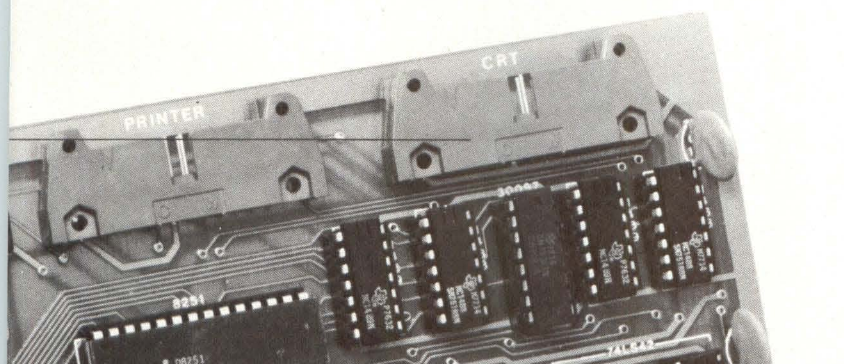

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CIRCLE 21

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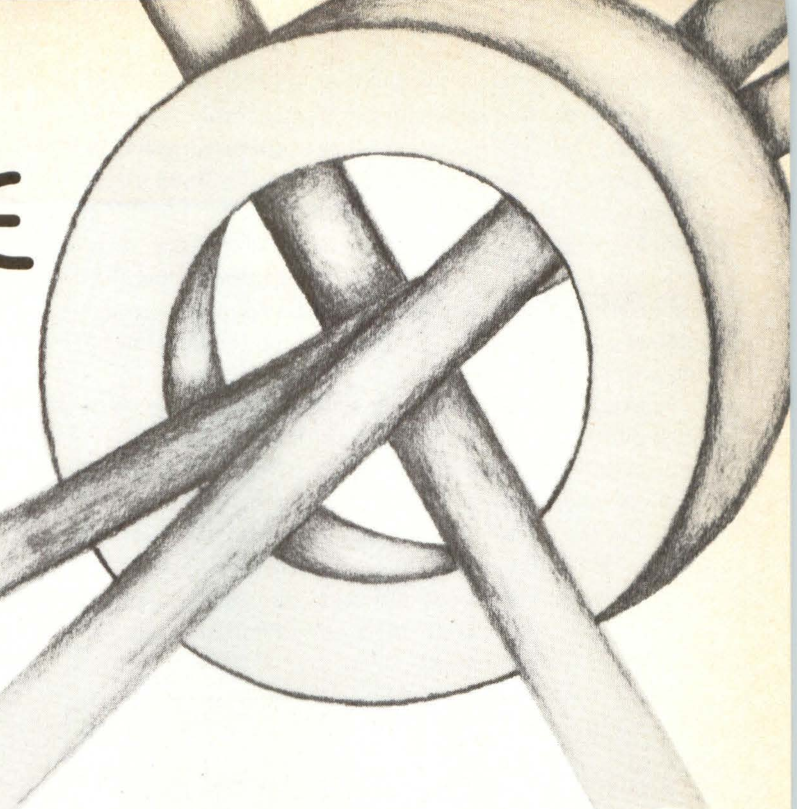
CIRCLE 22

CAN CORE SURVIVE?



by Alton C. Shimp

The core versus semiconductor debate continues. Despite the introduction of a variety of new technologies for semicon memory, core still appears in most minicomputer, and some microcomputer systems. Will core stay with us in the future? We present one perspective in this article: that core memory will remain a viable technology into the 1980's because of improved performance, proven reliability, established production capability and continued cost reductions.

Many comparisons between core and semiconductor memories have skewed performance, reliability and even pricing data. Fortunately, valid comparisons between the two technologies are possible. This article highlights the principal characteristics of core and semiconductor memories as they affect system performance by presenting 'hard' data drawn from the test laboratory and actual field reports. This data demonstrates that when price, performance and reliability comparisons are made between equivalent core and semiconductor memory systems, the competitive edge goes to core. Core memories will remain a viable technology into the 1980's because of continued reductions in cost, improved performance, proven reliability and its established production capability.

Semiconductor memories are inherently volatile. Following a power interrupt, it is often inconvenient and sometimes impossible to reload the information lost from memory. A similar situation would not affect data stored in a core memory because it can be powered down either catastrophically or routinely for an indefinite period without loss of data. In contrast, semiconductor memories must overcome the volatility disadvantage by using internal batteries to back up the primary power source. While operating on back-up power, data protection is limited and the battery power cannot be disconnected for system maintenance purposes.

Battery back-up for a small memory system can add considerable expense. Commonly used low cost lead-acid or high cost nickel-cadmium rechargeable batteries require battery charging circuits; both battery types have high failure rates when compared to other electronic components. Batteries also tend to demonstrate 'charging history' effects.

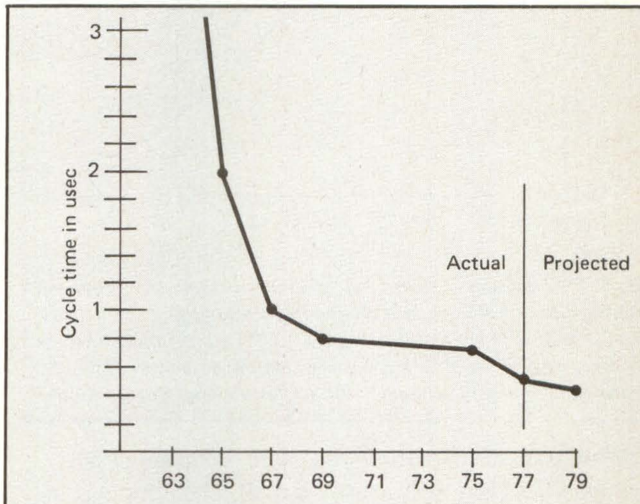


Fig 1 Typical core memory cycle times for production systems.

The cost of a battery back-up option to a user of a typical 16K x 18 memory can range from $200 to $250, providing back-up power over a period of a few hours to a day. However, frequent intermittent power failures can still cause a memory failure by not allowing sufficient time for batteries to recharge. Memories requiring long storage times need larger, more costly, remotely mounted batteries. One alternative to a battery back-up system would be the use of a core memory system to store key data from the semiconductor memory system while it is powered down.

Dynamic semiconductor memories store ones and zeros as a charge or absence of a charge in the cell capacitor. Even when MOS devices with low leakage currents are used, the capacitors must be frequently refreshed, thus requiring additional refresh circuitry. Typically, each cell in a 4K RAM is refreshed every two milliseconds simultaneously at 64 addresses; thus refresh circuitry must perform 64 refresh cycles every two msec. At a cycle time of 470 nsec, 30.08 µsec out of every two msec are required just for the refresh function. For a different ratio of addresses to the refresh rate, the efficiency loss of larger memory chips may be greater. Extra refresh circuitry usually consists of a counter, refresh address register and OR gating to the input address lines of the memory chip.

Leakage current approximately doubles for every 10°C. Most dynamic semiconductor memories have their maximum refresh rates specified at 70°C; at 90°C the refresh rate required for a dynamic RAM is four times the rate of 70°C. Thus, for the typical 4K RAM described above, the refresh rate would be 500 µsec at 90°C instead of two msec. This further reduces the over-all efficiency and greatly limits the use of dynamic semiconductor RAMs in military environment temperature ranges.

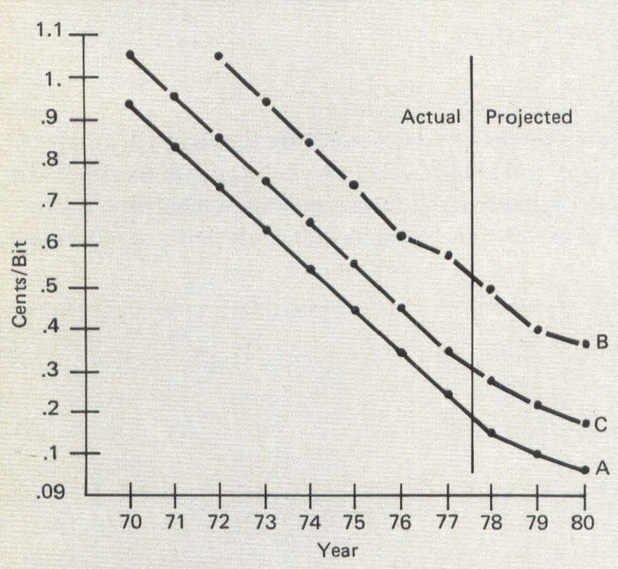


Fig 2 Typical selling prices for memory systems. A: Projected selling price of semiconductor memory cents/bit at chip level; B: Quoted selling price of computer 128K word semiconductor memory system including enclosure and power supply; C: 128K word core memory system with enclosure and power supply.

Reliability. A significant problem with semiconductor memories has been their relative lack of reliability in comparison to core memories. This can best be illustrated by using the data given in MIL-HDBK-217B. For integrated circuits MIL-HDBK-217B takes into consideration such factors as system environment, manufacturing learning factors, junction temperatures, chip complexity, packaging factors and quality factors.

According to MIL-HDBK-217B, the failure rate for integrated circuits is:

$$\lambda = \pi_P \pi_L \pi_Q (C_1 \pi_T + C_2 \pi_E)$$

where π_P is the packaging factor and depends on the number of pins,

π_L is the learning factor,

π_Q is the quality factor,

π_T is the junction temperature factor,

π_E is the system environment factor,

and C_1 and C_2 are the chip complexity factors.

A typical specification for a semiconductor memory might be: operation at 55°C junction temperatures, commercial grade, hermetic packages, system environment of fixed ground equipment (G_F), 24-pin dual-in-line packages and an established chip design (i.e. one which has been in continuous production for more than six months). For this example the failure rate calculation is shown below:

$$\lambda = \pi P\ \pi L\ \pi Q\ (C_1\ \pi T + C_2\ \pi E)$$

$\pi P = 1.1$

$\pi L = 1.0$ (for the chip designs $\pi L = 10$)

$\pi Q = 150$

$C_1 = .3$

$\pi T = 1.2$

$C_2 = .12$

$\pi E = 1.0$

$\lambda = 79.2$ failures $/10^6$ hours

For a typical 16K x 18 dynamic RAM system requiring 72 4K RAMs, the MTBF would be 175.36 hours for the RAM chips alone. (This calculation excludes the refresh circuits, timing, battery back-up, power regulators, and the circuits required to drive the memory chips.) In comparison, a typical core memory system that includes peripheral interface circuitry and a power supply has a calculated MTBF of approximately 600 hours.

Core memories always have the reliability edge when direct comparisons to semiconductor memories are made because the toroid core storage element retains stored information until it is physically damaged. While screening can enhance the quality factor of 4K semiconductor RAMs, screening can also enhance the reliability of the semiconductors used in core memories. For military applications, the choice of fully qualified RAMs is presently limited to the JM38510/23501, 4K RAM.

Unlike core memories, semiconductor memory pattern sensitivity is not well defined. Core memory worst pattern noise, commonly referenced as delta noise, has been well established and is reliably tested. For semiconductor memory, worst case patterns vary from design to design, and even from vendor to vendor on identical designs. Semiconductor memories often approach obsolescence before complete testing information is derived.

To circumvent the semiconductor memory worst pattern identification problem, checking programs have been established that check all combinations and interactions of addresses and read/write sequences. Examples of some of these so called 'N^2' patterns include Galloping Pattern, Ping Pong, Walk Pattern and Galloping Write Recovery. These test programs insure that pattern sensitive memories are eliminated no matter what the pattern may be; however, they are very time consuming. The N^2 dependency indicates that test time is proportional to the square of the number of memory bits, which means a 16K RAM takes 16 times longer to test than a 4K RAM. As an example, using typical 4K and 16K RAM chips with a 0.47 microsecond cycle time, it takes approximately 84 seconds for a 4K RAM and 22.4 minutes for a 16K RAM to run one Galloping Write Recovery pattern.

N^2 testing thus becomes impractical for medium/large scale RAMs except on a sample basis, leaving the 'N' patterns – such as Checker Board, Double Checker Board

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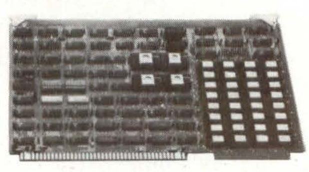

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Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally SBC 80 and Intellec MDS hardware and software compatible.

Limited one year warranty on parts and labor.

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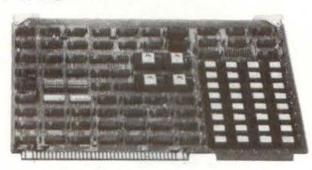

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CIRCLE 23

and Marching – as the only practical production testing modes. Unfortunately, many so called 'soft' errors, i.e. pattern sensitive errors, can pass undetected, yielding an increased failure rate of the basic memory. If you add error correction to the semiconductor memory system to correct these 'soft' errors, the failure rate of the 'hard' errors increases because of the added support electronics required. Hard errors are those catastrophic errors which are detected in all patterns.

As chip size increases, catastrophic defects that cause 'hard' errors become more likely. Current lithographic techniques limit MOS RAM chip size to 40,000 to 50,000 square mils; as design layout features and spacings become smaller, this chip size limit will probably decrease because smaller defects will produce 'hard' errors. The growth of memory size beyond 4K requires new layout techniques, for example, the double poly processing technique used on most 16K RAM designs. Relative reliability comparisons are difficult with these new techniques, although it is unlikely that these new techniques will enhance reliability.

Some defects in semiconductor memories, such as oxide contamination, do not show up immediately, but are time/temperature sensitive. Because latent defects in MOS designs are more prevalent than in bipolar designs, MOS memory has relatively higher failure rates.

Error Correction. To reduce the failure rate of semiconductor memory systems, designers have resorted to error detection and correction techniques that add a 'check bit' word to each memory data word. For single bit error correction, a five-bit check word is required for each 16-bit data word, allowing you to check both the data word as well as the check word for single-bit errors. The formula for the number of required check bits is $2^C - C \geqslant D + 1$, where C is the number of check bits, sometimes called hamming parity bits, and D is the number of data bits. You can see that the shorter the data word, the larger the percentage of required check bits: an eight-bit data word requires 50% redundancy for error correction.

Table 1 Failure Rates in Core Systems

Memory Size / Customer	2K	4K	16K	32K
A	143,000			
B		192,000		
C			93,000	
D				74,000

A = 12,636,000 unit/hours of field operation.
B = 576,000 unit/hours of field operation.
C = 1,861,200 unit/hours of field operation.
D = 1,109,056 unit/hours of field operation.

MTBF (Hours)
CORE MEMORY SYSTEMS

By adding another check bit, you can perform double bit error detection with single bit correction. A 16-bit data word thus requires a total of six check bits; the additional bit sums the parity of the check bit plus the odd parities of the data word bits. The state of this error summing parity bit shows whether the error is a single bit correctable or a double bit non-correctable error. In addition to the extra memory bits required, error correction requires a parity, or hamming code generator for the check bit word, an error code detector and an error logging memory. Error correction can add 40% or more to the hardware costs of the semiconductor memory system.

Users must also review the error log periodically to determine if errors were non-recurrent pattern susceptible, or catastrophic chip defects. You must identify and remove the problem chip; otherwise the probability of multiple bit errors, which are not correctable, increases. This is not required with core memory; error correction is unnecessary.

Error correction causes some degradation in performance. During a read cycle, the check bits generated during a write cycle are checked, the data bits are checked, and then an error code is generated. If there is an error, the error code identifies the erring bit, automatically complements it using an exclusive OR gate, and logs the error in the error logging memory. Typically, read access time increases by 50 nanoseconds when using error correction.

With error correction techniques, the semiconductor memory failure rate is relatively independent of the storage devices themselves. Failure modes occur in the peripheral memory circuitry, refresh, power supply and in the error correction logic itself. This also holds true for core memory systems except that error correction is not required; in core memories, the failure rate is relatively independent of the storage devices themselves; failure modes again consist of failures in the core memory peripheral circuitry and power supply.

Future Trends

According to Electronic Engineering Times, April 4, 1977, present lithographic techniques will not allow RAMs larger than 65K; this may even hold for the 65K RAMs. 'Minor' variations in processing, such as the use of double poly silicon, were employed in making the transition from 4K to 16K to keep chip area within bounds. To go from 16K to 65K and beyond requires major changes.

Electron beam exposing with plasma etch will almost certainly be needed to keep pace with the closer tolerances needed for new smaller cell requirements. The transition to these new techniques will probably take longer than the transition from 1K to 4K. Thus, future price reductions (for the next 3-5 years) in semiconductor RAMs may slow as the learning curve on the 4K and 16K chips flatten, and the 65K RAMs undergo production/engineering problems.

Over the past 25 years, a consistent set of techniques evolved for both the production and the testing of cores and core systems. Nomenclature, test methods, core chemistry and design techniques passed between and among the various core memory suppliers result in industry standardization. Core specification presently allows interchangeability at the stack level and temperature ranges, current compensation, disturb ratios, switching/peaking times and signal outputs are consistent enough to allow the system designer multiple sourcing on the core array. This second sourcing is more independent than that often found in the semiconductor industry with their mask interchanging. If the primary design had faults, the second source will probably have the same faults.

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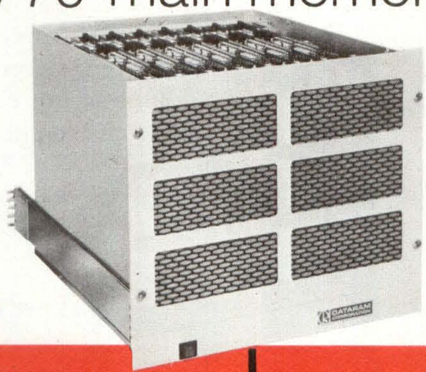

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CIRCLE 24

Core system testing has evolved to where the worst patterns (i.e. the patterns of 'ones' and 'zeros' in the core array that generate maximum noise or minimum operating margins during interrogation) are clearly defined for virtually all configurations and sense winding schemes. Half select read currents (called x/y currents for 3D designs and word/digit for 2½D designs) generate this pattern noise. When any core is coincidently selected in a core array, these half select currents disturb a group of cores along either of the two coincident drive lines. Because the patterns that add the most noise to a 'zero' signal and subtract the most noise from a 'one' signal are identified, you can take steps in the design and production phases of the core element to reduce this effect.

In recent years, reductions in the amount of inherent delta noise (half select output of 'one' cores minus the half select output of 'zero' cores) and full select 'zero' noise, along with tightly controlled compacted packaging techniques, have contributed to the wide current margins of

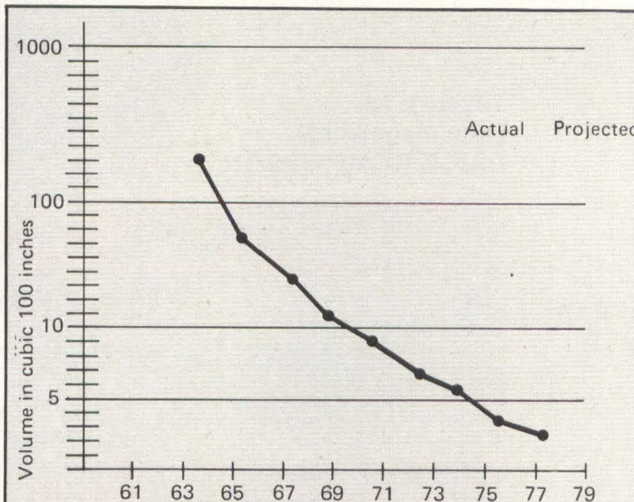

Fig 3 Size comparison by volume of 1096x18 core array assemblies.

present day core memory systems. The reduced delta noise and new packaging techniques make possible the low cost 16K and 32K sense lines in new designs. Development stage testing now includes checking delta noise and minimizing it. A laboratory test that ran nineteen 16K semiconductor memories for 28 days on a 24 hours a day basis, yielded an MTBF of 1160 hours; a concurrent test using eight 16K core memories showed no system failures.

Table 1, based upon documented field data provided by Fabri-Tek customers, shows MTBF's for core memory systems. These systems include core array, sense amps/drives, timing and control circuitry and address and data registers for either 16 or 18-bit memories.

Semiconductor memory selling price projections are easily misinterpreted, unless translated into complete memory system costs to the O.E.M. or user for a specific application. RAM memory pricing, primarily projected at the component or chip level as some fraction of cents per bit, can be misleading until you consider a detailed analysis of associated cost factors at the system level. For example, in a process control application requiring 128K words of memory with an enclosure, power supply and error correction and detection, the projected semiconductor price of .1 cents/bit at the chip level may end up as high as .4 cents/bit. Fig

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CIRCLE 27

3 shows typical semiconductor and core memory prices for 128K word memory systems.

The past twenty years show dramatic improvement in the development of core memory products. The predominant core types in the late 1950's and early 1960's were 80 mil and 50 mil cores. Technological advances and improved manufacturing techniques made during this period laid the groundwork for future core memory designs.

Thirty and 20 mil cores were developed during the mid 1960's; these cores were used primarily in 3D, 4-wire systems. In the late 1960's, the 20 mil core emerged as a predominant core type. System cycle times improved by more than an order of magnitude; 1.0 μsec became a common performance characteristic. Planar arrayed core systems were developed in the early 1970's with the 18 mil core predominant. The 3D, 3-wire organization became the standard memory architecture; sub-1.0 μsec systems now appear on the horizon.

Today's core memories, best characterized as 16K x 18, and 32K x 18, planar arrayed pluggable modules cycle in 550 to 650 nsec and acces 225 to 250 nsec. Containing a single or couble sided planar core array, the electronics within these core modules are highly integrated and feature sophisticated multi-layer circuit boards.

Core memories of tomorrow will use cores made from better materials and manufactured by improved processes; 13 and 14 mil cores will enable designers to further increase the packaging densities of systems and improve performance. Work will continue on the development of 10 mil cores and there will be new types of both low drive temperature stable cores. Additional work will realize the development of partial switching techniques along with further investigation of multi-state cores. Core arrays that package 100,000 bits in a fraction of a cubic inch will be developed, memory system electronics will continue to become more integrated as MSI and LSI technologies mature, and higher performance 16K and 32K modules will become available; slower-speed modules of 65K and 128K are also imminent.

Core memories will remain a viable technology into the 1980's because of continued reductions in cost, improved performance, proven reliability and established production capability. They will continue to thrive in applications where high reliability and nonvolatility are major considerations. The process control marketplace, with its harsh environmental conditions and its need for continuous operations, will use core memories to meet its requirements; point-of-sale systems and other on-line applications requiring a permanent data base will continue to use core memories. Core memories will replace drums and disks, thus improving the cost/performance ratios of both large and small computing systems.

As the applications for microprocessors develop, so will new applications for core. Microprocessor memory will not be the exclusive domain of the semiconductor memory because core memories will be used as the microprocessor memory in those applications where high reliability and nonvolatility are required.

Alton C. Shimp *is Engineering Manager for OEM Memory Products at Fabri-Tek Inc.*

NATIONAL ANTHEM

ALL THE NEWS THAT FITS

A Review of New Products and Literature from National Semiconductor • No.4

65 K static ROM features high speed, low power

We call it the MAXI-ROM™: 8192 × 8 bits of static, fully decoded, read-only memory with an access time of 800 ns maximum. And because our MAXI-ROM has timing requirements identical to those of static RAMs, you need only one clock for both RAM and ROM store.

Officially called the MM4235/MM5235, this new mask programmable metal-gate MOS ROM is an n-channel device and operates from a single 5-V supply. Its inputs are TTL compatible, as are its Tri-State®, OR-tie-compatible outputs. Further, the MAXI-ROM has three programmable chip-select inputs for easy, wire-OR'd memory expansion.

Right now, all of this comes to you in a 28-lead package; shortly, look for another version of the MAXI-ROM in the 24-lead 2316E pin-out.

3½-digit DPM on a single chip

Okay—you've asked for it, now you've got it. We proudly announce our ADD3501/ADD3701 and ADD3511/ADD3711 DPMs-on-a-chip. While the 3501 is intended for instrumentation-type uses, the 3511 is designed to interface with microprocessors. With its addressable BCD outputs, the 3511 is ideal for MPU-based system A/D uses and is the first of its kind available in the industry.

The results of an extensive survey of your DPM needs, the ADD3501 and ADD3511 incorporate just about everything you've told us you want.

To start with, we've put it all on a TTL-compatible, single CMOS chip that runs from a single 5-V supply (45 mW drain) and requires only two external parts—a reference and a digit driver. By switching external resistors you get two scale ranges: ±0.1999 V and ±1.999 V for the ADD3501, or ±0.3999 and ±3.999 for the ADD3701 (ideal for electronic weight scales, azimuth indicators, and so on), and to an accuracy of one count from 0° to +70°C.

And these units are National proprietary designs that use pulse modulation A/D conversion techniques, rather than dual-slope techniques. This method of conversion eliminates precision external components, and lets you use a single reference voltage of the same polarity as the input signal. The use of a single, isolated power supply for the whole DPM, by the way, allows the conversion of positive and negative voltages. The ADD3501/ADD3701 automatically outputs the proper sign and, also automatically, displays +OFL or −OFL in case of an overrange situation.

You can use either an external RC network or an external signal source to control the DPM's on-chip clock (100-640 kHz), which in turn sets the conversion rate to $64{,}256/f_{in}$ conversions per second. The digit multiplexing is synchronized with the A/D conversion timing to eliminate noise from power supply transients.

Other features of the ADD3501/ADD3701 are a FET input circuit, which draws an analog input current of only ±0.5 nA; a Start Conversion input and a Conversion Complete output; and a seven-segment LED drive for jitter-free displays to 0.5 inch. Our NSB5388, described in this issue, is a perfect companion for the 3501; and we've got a 3¾-digit display that's an ideal display-mate for the 3701, too.

Cutting it fine: a 4-bit bipolar MPU slice

The IDM2901A is a 4-bit microprocessor slice intended to be used either alone or cascaded in central processing units, programmable microprocessors, peripheral controllers—in fact, wherever high-speed applications demand economy, software/hardware flexibility, and easy expansion. Its building-block architecture and microinstruction format permit the IDM2901A to emulate most digital-based systems.

A low-power-Schottky part, the 40-pin IDM2901A features a multiple-address architecture, which improves system speed by providing simultaneous yet independent access to two working registers. Its multifunction ALU performs addition, two subtraction operations, and five logic functions on two source operands; for every ALU function, the IDM2901A selects data from five source ports for a total of 203 source operand pairs. And because left/right shifts are independent of the ALU, an arithmetic operation and a left or right shift are obtainable on the same machine cycle.

The IDM2901A has four status functions with carry, overflow, zero, and functional sign available as outputs. And it's microprogrammable, too, with three 3-bit groups for source operand, ALU function, and destination control.

The IDM2901A chip carries a 16-word by 4-bit two-port RAM, a high-speed ALU, and all required shifting, decoding, and multiplexing circuits. And it's *fast.* In fact, our IDM2901A is the fastest 2900-type MPU you can buy. We've proved it, and so can you. Check the IDM2901A's data sheet, then try the part itself. We're sure you'll like it.

Voltage regulators —we have 'em

Innovative technology, quality of the highest order, competitive and better-than-competitive pricing, and minimum-lead-time delivery—these have made National the Number One supplier of linear circuits.

Our voltage regulator family is a good example of our leadership position. Already the most complete three-terminal regulator line in the industry, it's still growing, as this chart shows:

POSITIVE REGULATORS

Fixed

LM123	- 3.0A
LM140	- 1.5A
* LM140A	- 1.5A
LM141	- 0.5A
LM142	- 0.25A
LM140L	- 0.1A
LM78XX	- 1.5A
LM78MXX	- 0.5A
LM78LXX	- 0.1A

Variable

LM117	- 1.5A
* LM150	- 3.0A

NEGATIVE REGULATORS

Fixed

LM145	- 3.0A
LM120	- 1.5A
LM120M	- 0.5A
* LM120ML	- 0.25A
* LM120L	- 0.1A
LM79XX	- 1.5A
LM79MXX	- 0.5A
* LM79LXX	- 0.1A

Variable

* LM137	- 1.5A

The products marked here with an asterisk either have been introduced very recently, or will be available very shortly. Our LM140A/LM340A, for example, has performance unmatched by any other manufacturer, with nearly perfect line (0.06 %/V) and load (0.5 %/A) regulations and is fully spec'd at 1.0 A—not at 0.5 A. The LM340, in fact, has improved specs—right to the military limits—and slips into any 78LXX socket to give superior performance at no increase in cost.

Then there are the LM120ML/LM320ML (0.25 A) and LM120L/LM320L (0.1 A), negative regulators that complement the positive regulator versions, and which offer optimal price performance.

Two other bright new stars in our regulator galaxy are the LM150/LM350—a high power (3 A) version of our LM117/LM317, which was the industry's first adjustable regulator—and the LM137/LM337, which is an adjustable 1.5-A negative regulator that complements the LM117. We've improved reliability by 100 per cent burn-in testing, so these parts will reduce your inventory requirements and standardize packaging, while improving your system's performance.

Finally, there's our LM79LXX—a new regulator for negative, low-current applications, which we test to 100 mA (versus only 40 mA for competitive parts); even with only a 0.1-μF output compensation capacitor, this unit retains its excellent transient response, line regulation (0.07 $\%V_o/V$, max.), and load regulation (0.01 $\%V_o/A$, max.).

New in PACE family: n-channel, 16-bit MPU

Our INS8900 microprocessor is intended for applications which require the efficiency of a 16-bit word length, yet it is priced the same as many 8-bit microprocessors.

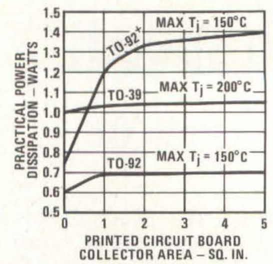
Housed in a standard 40-pin ceramic DIP, the INS8900 is built with n-channel silicon-gate technology. It's a true 16-bit CPU with 16-bit instruction words and 16-bit data words, all handled by a powerful, efficient, and flexible set of 45 instructions.

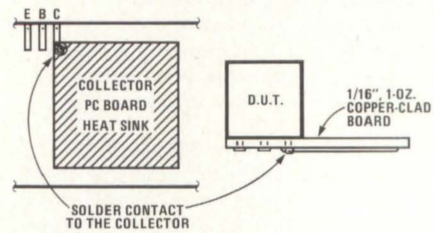
The single-word 16-bit format of the instructions reduces memory accesses and program storage requirements. And because it can operate on both 8-bit and 16-bit data words, the INS8900 extends its efficiency and power to 8-bit applications as well.

Features of the new MPU, for which a full family of peripheral circuits is planned, include multiple addressing modes, four general-purpose accumulators, byte and word processing, common memory and peripheral addressing, six hardware vectored priority interrupts, a ten-word stack, four control flag outputs, three sense inputs, four I/O control strobe signals, a single-phase 2-MHz clock, and low-power-Schottky-compatible outputs. And all of this is yours at a high-volume pricing of less than $10.

TO-92+ dissipation —pinned down

Many of you have been asking to see a comparison of the power dissipation capabilities of three popular packages—the molded TO-92+ and TO-92, and the metal TO-39. In answer to these requests we present the following chart, which shows what you can expect in actual use on a PC board.





We are pleased to point out that our TO-92+ power devices lead the pack; so pleased, in fact that we're adding these curves to the TO-92+ data sheets to complement the SOA and thermal derating curves already present.

Our 80/10: alternate source, lower cost

National has entered the microcomputer marketplace with the introduction of our Series/80 BLC 80/10—a self-contained computer-on-a-board. The central processor, system clock, RAM/ROM store, I/O lines, serial communications interface, bus drivers and logic . . . all on a 6.75 × 12-inch PC board.

Our 80/10 is an alternate source for the Intel product—but at a price lower than Intel's. The lower price results not only from our automated assembly procedures, but also from a major use of our own components—something Intel cannot match.

The CPU, for example, is our own INS8080A; the 1K × 8 static read/write capability, our MM2711 RAMs; up to 4K × 8 read-only memory, our MM2708 PROMs or MM2308 ROMS; two INS8255 programmable interface circuits provide 48 I/O lines; an INS8251 US/ART; Teletypewriter® and RS232 interfaces; provision for up to six interrupt request lines; etc., etc.—you get it all.

And supporting the BLC 80/10 card itself is an army of other Series/80 cards: RAM boards, ROM/PROM boards, DMA boards, I/O boards, memory and I/O expansion boards, prototyping boards; and coming very shortly, full Series/80 systems and firmware.

With National as an alternate source, the 80/10 microcomputer emerges as the *de facto* industry standard. So get on the bandwagon today. Ask for our Series/80 literature. See what you've been missing— and how much you'll be able to save.

Active filters, anyone?

National now has an extensive line of standard active filters. While many of these filters are intended for general purpose use up to 100 kHz, there is also a new family intended specifically for telephone equipment.

In the general purpose line our AF99, for example, is a tunable (60 to 270 Hz) high Q, band pass filter with a user-strappable bandwidth option of 2.5 to 5.0 Hz. Because it is also usable as an oscillator, the AF99 comprises a complete tone generating and receiving system in a single package—excellent for 2-wire tone-activated systems.

Our AF100 is a universal active filter that needs only four external resistors to program it for specific second-order functions. It features simultaneous and separate low pass, band pass, and high pass outputs; and independent Q (to 500), frequency (to 10kHz), and gain adjustments. The AF100 may be cascaded to realize higher-order systems. (In fact, we have a new filter to make that job even easier: our AF151, which combines two AF100s in a single package.) And the AF150—the newest member of our filter family—is a high-frequency version of the AF100, with operation extended to 100 kHz and the Qf_c product increased to 200,000.

Then there's our AF120—a generalized impedance converter. Adding one external capacitor to this device turns it into the gyrator-equivalent of a grounded inductor; paired AF120s form ungrounded inductors or inductor networks. Two external capacitors turn the AF120 into a frequency-dependent negative resistance. In short, with appropriate transformations the AF120 makes it possible to realize any low-frequency ladder filter network.

Finally, we have a group of filters intended specifically for telephone transmission systems. The AF132, for example, combines transmit and receive filters in one package, and is for use in digital PBX equipment. The AF130 (transmit) and AF131 (receive) filters, on the other hand, are high quality, fifth order, elliptic low pass units intended for high-quality PBX and PABX equipment or D3 Channel Bank use. Yet another step up the chain are our premium, central-office quality AF133 (transmit) and AF134 (receive) filters. These allow you to meet all AT&T 2- and 4-wire specifications as well as the CCITT international specs for PCM exchange equipment. All these filters meet the stringent requirements of the telephone industry, and satisy all considerations of size, environment, life, and cost.

APPLICATIONS CORNER

Seven-segment to BCD—the easy way

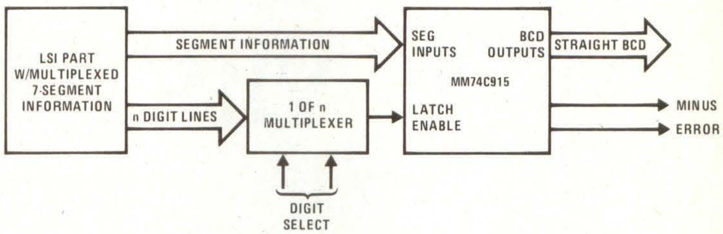
Many popular devices output multiplexed seven-segment information. If you want to analyze such information, or store it, process it or route it, it is more efficient and easier to do if you first convert to a BCD format. Unfortunately, most of the articles that have appeared on this subject in the trade press have presented methods that are expensive, or complicated, or both. Unfortunately, too, the interface problem has aggravated the situation. Thus, the use of calculators, clocks, counters, and A/Ds as number crunchers, real-time clocks, and inexpensive converters has been discouraged. But now, we're pleased to point out, the situation has changed.

It has changed because of our MM74C915—a CMOS seven-segment-to-BCD converter. This part holds, on one chip, all the circuitry you'll need for level shifting, decoding, latching, busing, and even error detection.

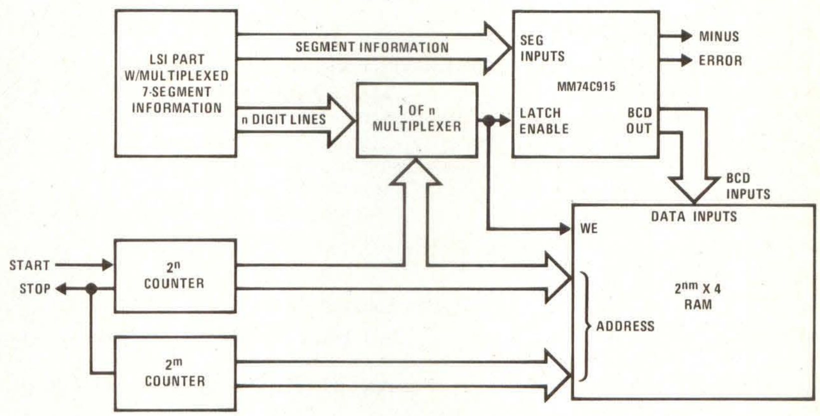
The MM74C915 accepts either positive-true or negative-true inputs. It decodes only legitimate seven-segment characters, allows for variations on the characters one, six, and nine, and gives you an error output when illegitimate characters are present. Its on-chip latch simplifies de-multiplexing a display; the outputs are TTL compatible; and the inputs are MOS compatible without a clamp diode to V_{CC}. And you can use the Tri-State® data outputs for direct data-bus interfacing; there's even a minus-sign output useful in program branching.

With a single MM74C915 you can interface a nine-volt calculator or a watch chip to a five-volt MPU; you can store data in half the memory space, route it with a mux half as wide, process and analyze it twice as efficiently—all without the loss of the price or low parts count of a MOS seven-segment device.

In fact, it's so easy to use and solves so many problems that whenever you think of the seven-segment LSI world, you should also think about the MM74C915.



Multiplex 7-Segment to Straight BCD



Memory Expansion from 7-Segment Outputs

3½-digit, 0.5-in. high LED display

Intended for digital instrumentation applications—power supply readouts, multimeters, panel meters, etc.—the NSB5388 is a common-cathode multiplexed display with separate access to the decimal points and ± signs. It is directly compatible with our ADD3501 DVM chip (story on page 1).

Electrical specifications include a typical light intensity of 1.6 mcd and forward voltage of 1.7 V.

NATIONAL ANTHEM

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Chip set for processor systems

We have a pair of CMOS/LSI circuits that we've dubbed LPCS—which stands for Low-power Programmable Calculator Set. The pair consists of the MM58101 (a Control ROM Element, or CRE), and the MM58102 (a Memory and Processor Element, or MPE). The two chips form a processor with an eight-bit instruction/ four-bit data word architecture.

The LPCS turns out to be ideal for any and all controller/timekeeping applications that demand a low-cost, micropower processor—electronic door locks and security systems in general, toys and games, telephone interconnect devices, battery operated instruments and control systems.

The LPCS directly drives seven-segment, six-digit liquid-crystal displays (with decimal points), and interfaces to 40-position keyboards. An on-chip 32.768-kHz oscillator provides not only all clock and control signals required for the LPCS to operate as a processor, but a 1-Hz program-controlled interrupt function as well.

A key feature of the set is its single-mask programmability: the 2048 × 8 ROM is mask-programmable to your own application requirements, and you talk to it via a set of 39 standard instructions.

Other features of the MM58101/ MM58102 LPCS include operation from a single −3 V supply, an on-chip doubler to drive liquid-crystal displays, a general purpose output port, and three program-controlled I/O ports.

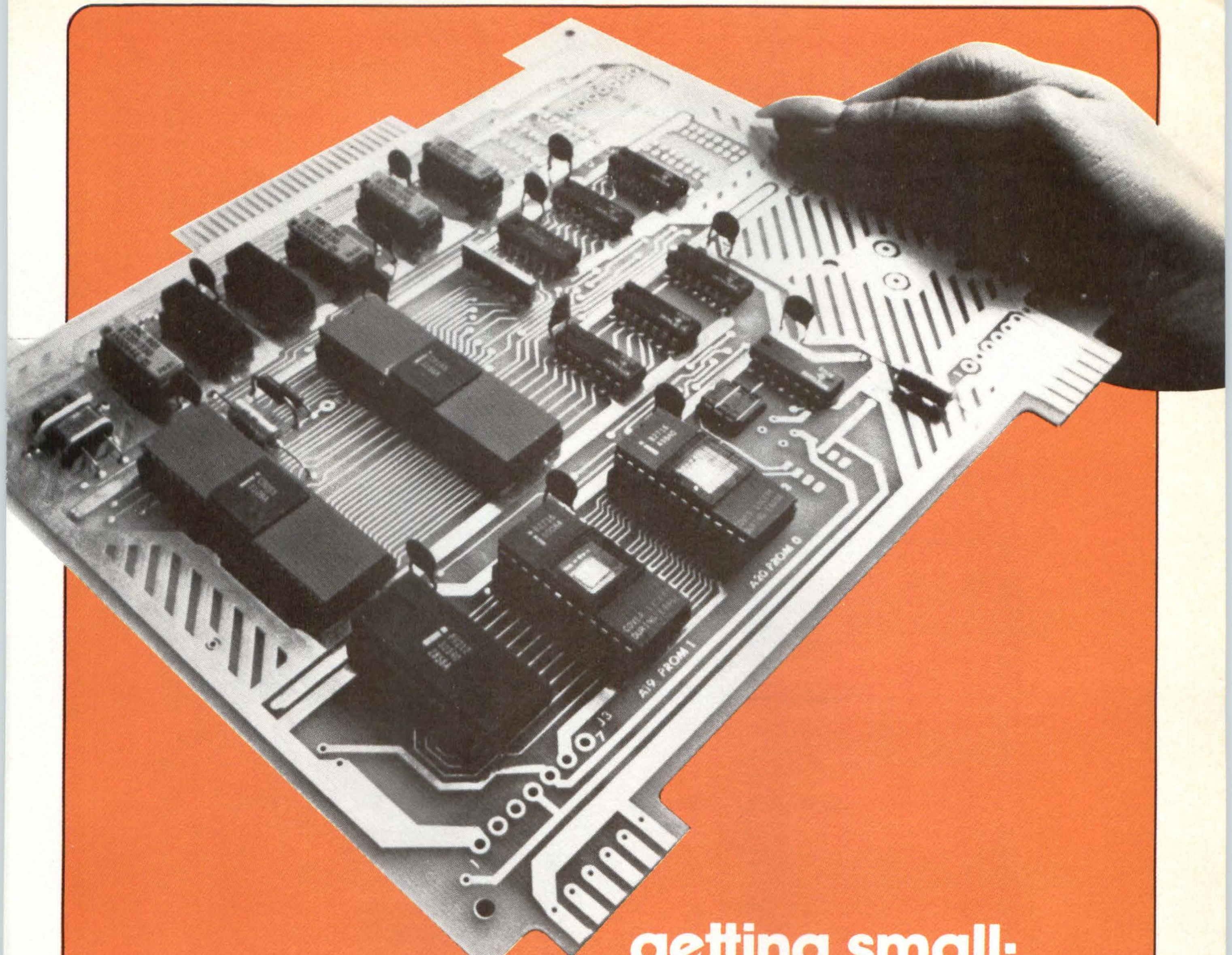
Pressure transducers: what you need when you need it —at the right price

When it comes to pressure transduction we have the devices you need. If you're involved with hydraulic controls, medical instrumentation, machine monitoring, flow control, chemical analysis, etc, in the industrial, automotive, medical, or process control fields—among others—remember this: Our unique transduction method, our manufacturing skills, and our *in-touch* application-oriented designs combine to guarantee you production volumes of the most advanced, reliable, and cost-effective true IC pressure transducers you can buy.

Four years ago we published the first transducer catalog of any usefulness to transducer users. Since then, National has become a world leader in the field. Now we've made this experience available to you in an up-to-date new edition of that catalog. The 142-page mix of detailed specifications and charts and tables, and applications-oriented hard-to-come-by practical information—and some blue sky thoughts, too—is so complete and useful that we call it *The Pressure Transducer Handbook*.

Besides completely characterizing our extensive line of pressure transducers and telling how to install them, the *Handbook* has sections on accuracy, auto-referencing, and signal conditioning; on packaging and environmental considerations; fluid flow; accelerometers and load cells; switch control; temperature measurement; and medical, acoustic, and automotive applications.

From theory to practice, from the here-and-now to the avant-garde—it's all between the covers of *The Pressure Transducer Handbook*. A copy is yours for $3.00; mail your check or money order (no cash) to Marketing Services MS/520, National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, CA 95051. (San Francisco Bay Area residents add 6.5% sales tax, please; other California residents, 6%.)



getting small: microcomputers

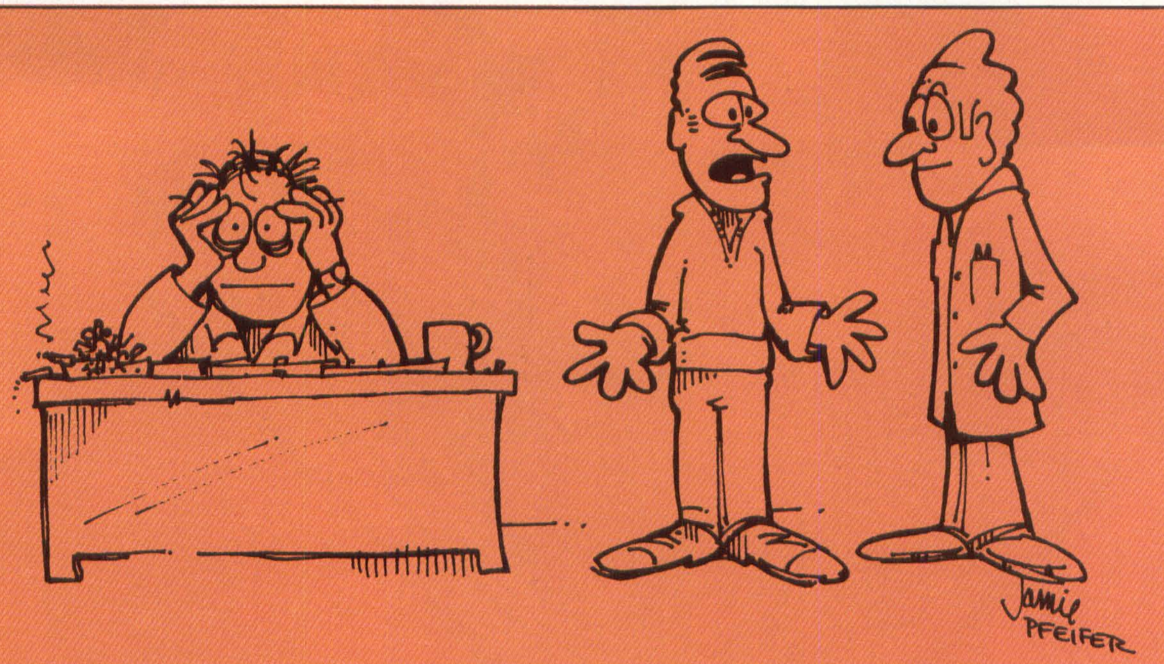
by Henry K. Simpson

No one has yet put a microcomputer onto the head of a pin but it would probably not surprise anyone who follows the industry if it happened the day after tomorrow. No question about it – microcomputers can be amazingly small. This small size, extremely important in some of the earliest applications of microcomputers in the aerospace industry, remains important in many current applications. Increasingly, however, microcomputers find places in industry where their compactness is convenient but not the main reason for their selection. Just as minicomputers in their early days began doing things that larger computers could do, microcomputers are now making inroads into the applications of minicomputers (see page 44).

If littleness is no longer the big thing it once was, then cost may well have taken its place as being of primary importance. Compared to minicomputers or hard-wired logic, methods that compete with microcomputers in many control applications, microcomputers, at least on an initial purchase basis, clearly win the race. But initial cost does not tell the whole story; this is as true of microcomputers as of anything else. Dick Anderson, Product Planning Manager of Rockwell's Microelectronic Device Division, observed that "the trend, if projected, suggests that in the future hardware will be free and all the expense will be in software development." Well, prices may never asymptote to zero, but this comment still makes a significant point – that software or, more specifically, the programming aspect of microcomputers, is a very important cost item. Most microcomputers serve in dedicated, special-purpose applications and are programmed in assembly or machine language. Usually these programs are developed by design engineers who, until recently, knew very little about computer programming. In other words, the advent of microcomputers has changed the design engineer's task and has significantly increased emphasis on programming. We now survey the microcomputer field covering representative products of each major type of microcomputer, and considering how microcomputers affect the designer's task. We will map industrial trends and see what the manufacturers are saying will happen to microcomputers in the next few years.

What is a Microcomputer?

Industry generally classifies a microcomputer as a microprocessor plus memory, with I/O interface (Fig 1). Two types of memories generally are used: ROM (Read Only Memory), which contains the program; and RAM (Random Access Memory, also sometimes referred to as read/write memory), used to store data temporarily. The I/O interface gets data into and out of the microcomputer. The micro-



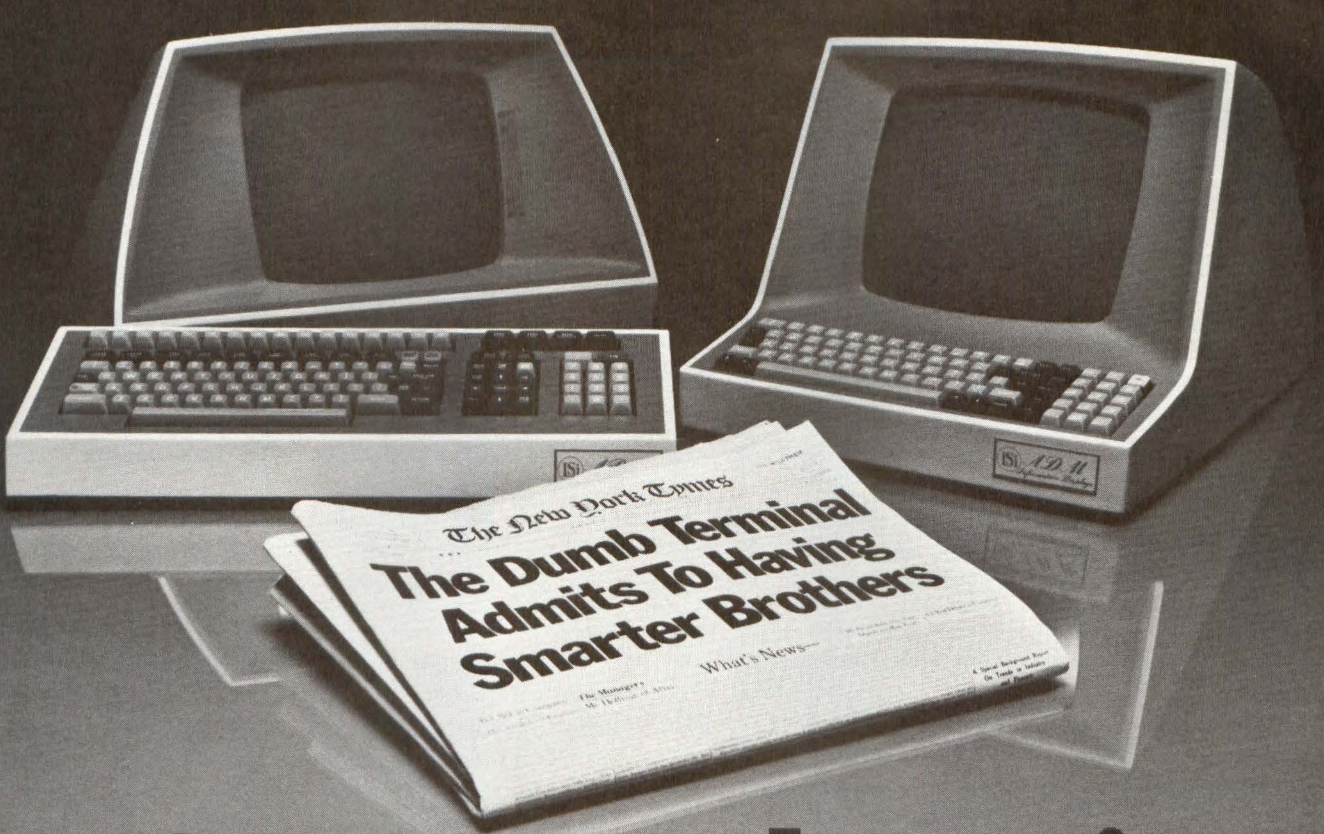
"It began when somebody told him that only microcomputers use LSI and he discovered a mini that uses LSI. Then he figured that minis had bigger memories. That worked okay until he found a micro with half a megabyte. Then he tried to convince everyone that microcomputers were simple-minded and had to be coded in machine language. What finally blew his mind was our new business microcomputer that can be programmed in FORTRAN, has 16-bit addresses, a CRT and a line printer."

Microcomputers and Minicomputers

The distinction between microcomputer and minicomputer becomes increasingly blurred, at least at the boundaries, as time passes. Both got their names because of size – the mini because it was smaller than the larger computers it was compared with, the micro because it was smaller than the mini. At one time you could make a distinction based on technologies employed –micros used large scale integration while minis used discrete components – but many minis now employ LSI also. We used to say that minis were more memory-oriented than micros, but many micros now contain large memories. It used to be true that high-level languages such as BASIC and FORTRAN were available on minis, but not on micros. This is no longer true in many cases, though it is true that such languages are more widely available on minis than on micros. Micros used to be limited to 16-bit or smaller addresses. No longer.

Many of the previous rules still hold, at least in most cases. The problem develops with a class of microcomputers, designed for general-purpose applications, that possess the appearance and all the capabilities of minicomputers. Manufacturers such as Texas Instruments do not help us solve this dilemma when they design both minicomputers and microcomputers around the same TMS 9900 microprocessor chip. Nor does Pacific Cyber/Metrix do much to clarify the situation by designing its PCM-12 microcomputer with a microprocessor that is "essentially an LSI version of the CPU in the PDP-8/E™," making the PCM-12 "perform like a PDP-8/E in nearly every respect."

You may by now see that we do not take this issue too seriously. Names – whether you call something a minicomputer or a microcomputer – are far less important than performance (or, as Shakespeare once had Romeo put it, in a slightly different context, *". . . a rose by any other name would smell as sweet . . ."*). In many cases today, microcomputer performance approaches or equals that of some minicomputers.



Sooner or later it was bound to get out.

Yes, the Dumb Terminal™ really does have two smarter brothers.

At first, they weren't quite as well known, because their Dumb Brother's smashing success was stealing the show. Although they had been selling quite well all along, even without getting constant headlines, like their Brother.

Now, however, Dumb Brother has pulled them into the limelight. And ADM-1 and -2 have decided, after all, that perhaps it's time you knew a little more about how smart they really are.

ADM-2 is the more intelligent of the two, providing you with flexibility of format, security, editing, interface, and transmission. You'll find, among a variety of other outstanding features, up to 8 screen status indicators and a numeric key pad. And a detachable keyboard with 16 function keys. Which give you the ability to access your special program, or form, or instruction.

The ADM-2 is also available in a model compatible with your Burroughs TD-800 Series. The ADM-2B. The ADM-2B adheres to the standard Burroughs poll and address line discipline.

On top of all that, we've made the ADM-2 micro-programmable. And taken all the mystery out of the procedure. Which makes user-micro-programmable simple, quick, and cost-effective. The ADM-2's versatility is limited only by your imagination.

You could call the other Smarter Brother, ADM-1, the "with-or-without" terminal. Starting with some pretty smart standard features, like a standard 24-line display, a field protection feature with dual-intensity and switch-selectable operating modes – block mode and conversation mode – you build up from there. With options like a hardcopy printer interface, and display editing capabilities (line insert, line delete, line erase, character insert, and character delete). Just add the options you need, and leave the rest of the "bells and whistles" for someone else. That way, it's more systems adaptable. And it's up to you just how smart you want it to be.

The Smarter Brothers have it all. Intelligence, appropriate functions, and sensible cost-per-performance.

So, you might as well get used to seeing more of the ADM-1 and -2 in the future. Because we suspect they're going to be in the spotlight from now on.

After all, there's really nothing wrong with exposing your Smarts.

LSi ® **The dumb terminal's smarter brothers.**

Lear Siegler, Inc., E.I.D./Data Products, 714 N. Brookhurst St., Anaheim, CA 92803; (800) 854-3805, In California (714) 774-1010.

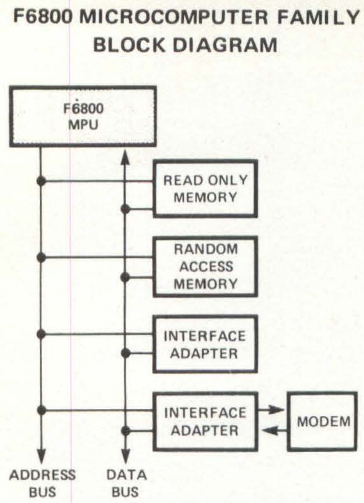


Fig 1 Microcomputer consists of microprocessor (in this case Fairchild 6800), ROM, RAM and I/O.

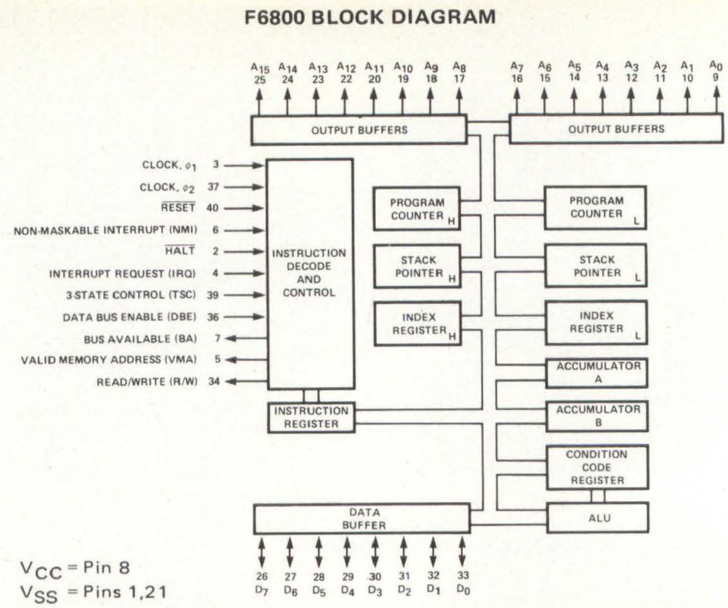
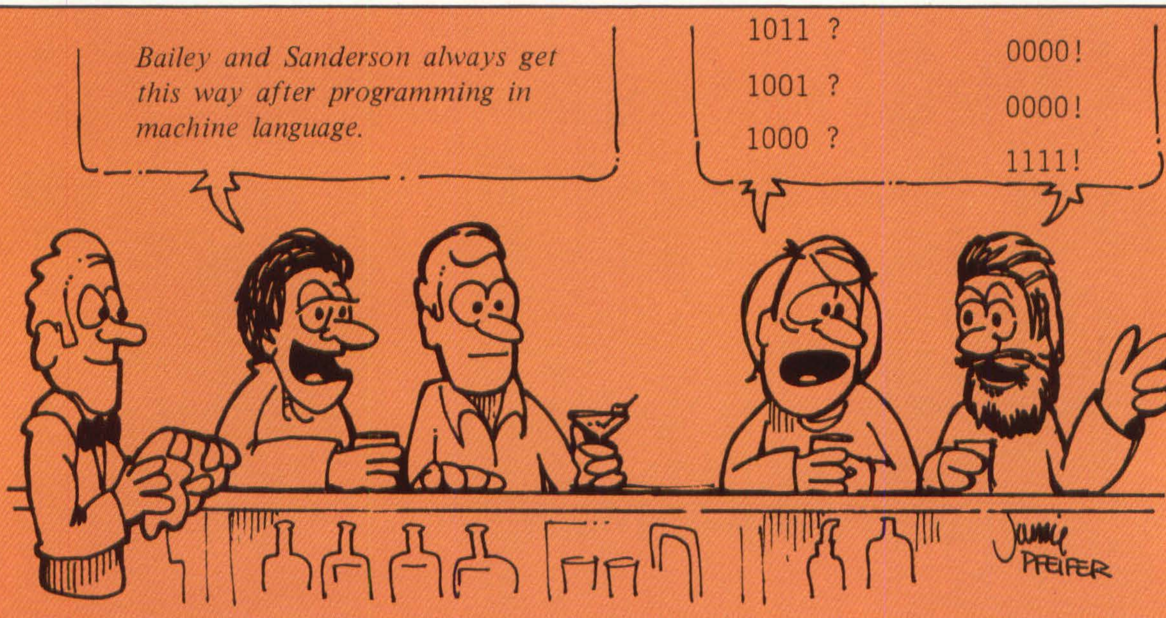


Fig 2 Block diagram of fairly representative 8-bit microprocessor chip, the Fairchild 6800.

processor, heart of the microcomputer, contains an arithmetic logic unit, accumulators, registers, address buffers, instruction decoding and control, and the various other functional entities found in larger computers. Fig 2 shows a block diagram of the F6800 microprocessor.

Microcomputers use a fairly limited set of microprocessors. Most common of the 8-bit processors are the 8080 and its variants, Z-80, 6800 and F-8; the 4040 is a widely used 4-bit processor. Sixteen-bit processors, now becoming quite common, include the IMS 9900 and 1M6100 I. The

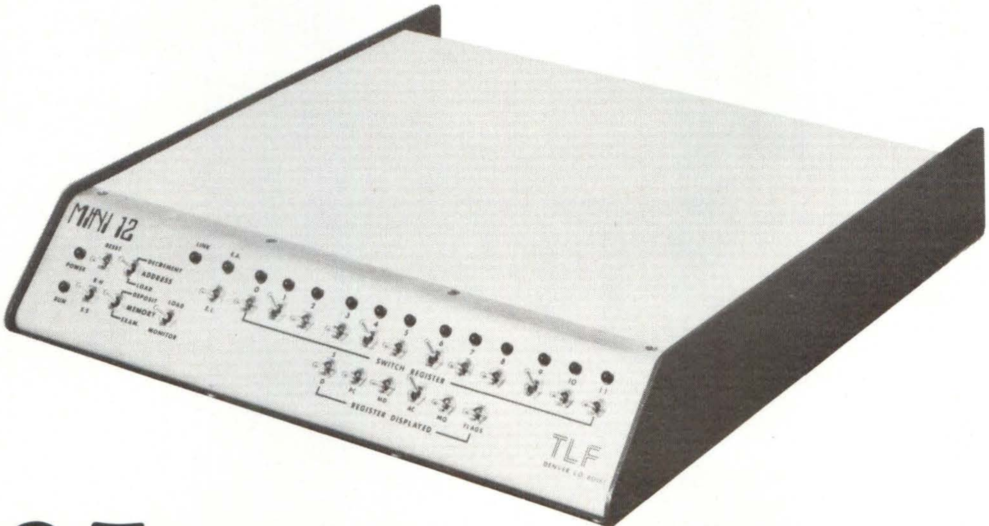


What Programming Language Should You Use?

Programming is easiest with high-level languages, more difficult with assembly-level languages, most difficult with machine languages. [For a more complete discussion of this topic, see page 66 of this issue.] The easier the language, the more rapidly the program can be written and the more money saved in programming time. On the other hand, high-level languages must be compiled and the machine instructions thus constructed are not generally as efficient in terms of number of instructions or memory requirements as programs originally written in machine language. In other words, you may save yourself time by programming with a high-level language but you will pay for this time-saving by getting a program that has more steps (and runs slower) and that requires more memory.

If you do decide to use a high level or assembly level language for programming, you choice of microcomputers becomes more limited, because cross compilers and assemblers are not available for all microcomputers.

THE FIRST AFFORDABLE MINICOMPUTER



$895

ASSEMBLED

READY TO COMPUTE, CALCULATE, CONTROL, OR . . . . ? . . . . ? . . .

STANDARD FEATURES:

Word Length	12 Bits
Instruction Set	PDP-8E Compatible
Memory Size	8K, Expandable to 32K
Extended Memory Control	DEC Compatible
Serial I/O Port	DEC Compatible, current loop
Parallel I/O Port	Compatible with DEC DR-8 - EA
Programmable Real Time Clock	Compatible with DEC DK8 - EP
Full Function Programmer's Front Panel	
Binary Load and Punch Routines in ROM	

TLF CORPORATION

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CIRCLE 31

Fig 3 Texas Instruments model 990/4 16-bit microcomputer, based on TMS 9900 microprocessor, with 24K x 16 words of memory, floppy-disk ROM loader, video terminal and floppy disk, can be programmed in several high-level languages such as FORTRAN IV, COBOL and Multiuser BASIC.

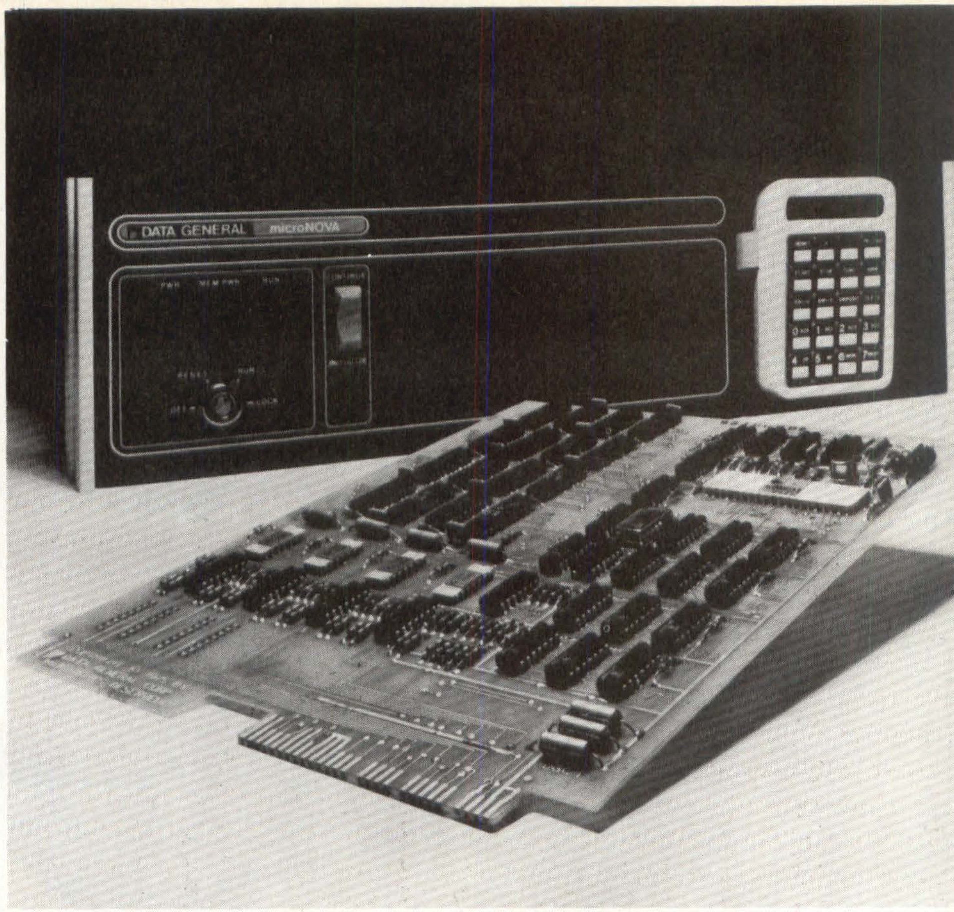


Fig 4 Data General microNOVA 16-bit computer, available in board or cabinet configuration, uses mN601 CPU chip, can provide up to 315 K word memory with optional dual diskette.

microprocessor alone is not a microcomputer, because it lacks the requisite memory and I/O. However, single-chip microcomputers do exist and are becoming commonplace.

Given a particular microprocessor, it is difficult to predict all possible applications, because, in the words of one industry spokesman, "we see no clear mapping from microprocessor to end product." Four-bit processors are more commonly used in control applications than 8-bit devices because they perform adequately at lower cost. High speed data processing microcomputers generally use 16-bit processors. A popular processor such as the 8080 turns up in microcomputers designed for such varied applications as dedicated control, data processing and hobby systems.

Some Typical Microcomputers

Microcomputers come in many shapes and sizes, suitable for an enormous range of applications. They may be general- or special-purpose (dedicated) machines, operating in real or non-real time. Since the field is so diverse, one of the problems is to get a handle on the different kinds of microcomputers available. Let's look at some classification schemes.

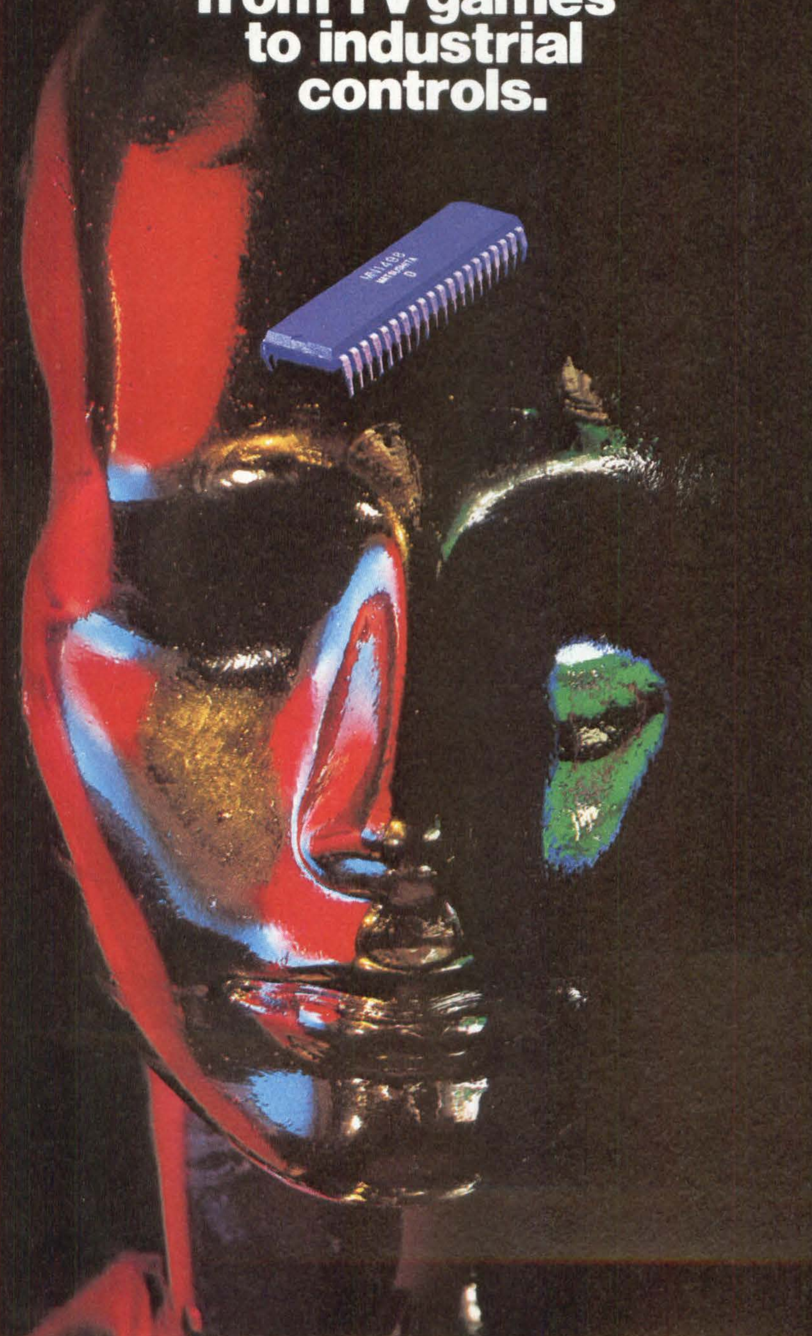
One way industry commonly classifies microcmputers is by product application. The commonly accepted categories include control, data acquisition, data processing, scientific computing, intelligent terminal, hobby and development systems. Most microcomputer-based products belong to at least one of these categories. The last category, development systems, contains machines used in the process of designing, testing, prototyping, programming and debugging new microprocessor- or microcomputer-based systems. Development systems are extremely important to the designer who is working with microcomputers and for this reason we are going to treat development systems separately and at length in the January issue.

Another way to classify microcomputers is by how they are physically structured when sold. Industry produces microcomputers in four different basic structural forms: single chip, board, cabinet and modular component system (like a minicomputer). Actually, this classification scheme proves very useful, because it relates directly to what the engineer must do to get a microcomputer to work in the system being designed. Going from chip to board to cabinet and then to component system, the designer's task becomes progressively simpler. At the same time, as microcomputers are acquired in progressively more finished states, the computers generally become more specialized, thereby reducing the designer's options.

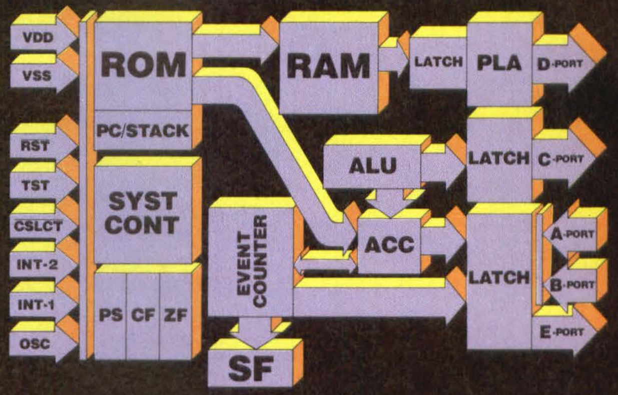
Single-Chip Microcomputers. Intel introduced the first single-chip microcomputers late in 1976. Three related chips – 8048, 8748, 8035 – contain the same processing and control subsystems, with 8-bit CPU, 64-byte read/write data memory, three programmable 8-bit I/O ports and eight other control and timing lines, programmable interval timer/event counter, priority interrupt controls, system clock generator and a set of system controls and utilities. Various expansion peripherals are available with these microcomputers, as with most other single-chip microcomputers, to increase memory,

4-bit, one-chip micro-computers

Brainy enough for anything from TV games to industrial controls.



Block diagram of MN1400 with on-chip, 1024x8-bit ROM.



Now Panasonic offers you a whole family of TTL compatible, one-chip microcomputers. So you can choose the combination of features and capabilities that are most cost-effective for your application. From appliances to gas pumps and electronic scales, to copiers, POS and intelligent terminals, tractor controls and countless others.

Why pay for costly I/O interfacing when Panasonic puts it all on the chip?

Our MN1400 family is ideally suited for control functions with its extensive array of on-chip I/O facilities. There's an 8-bit presettable counter/timer, a clock generator, an arithmetic logic unit, and several input and output ports. Units are available with a self-contained 1024x8-bit ROM and a 64x4-bit RAM memory.

Still more flexibility and efficiency from Panasonic.

For flexibility, our instruction set contains up to 75 instructions. To give you TTL compatibility, all our family members operate on +5V. And for extra computing speed, we've utilized N-channel E/D MOS construction.

Panasonic can help you cut development time and costs.

Our Evaluator, the MN1499, can help you design, evaluate and debug programs quickly. In addition, software is available for a number of applications.

The Panasonic family of one-chip microcomputers.

Package		MN1400 40-Pin Plastic DIP	MN1402 28-Pin Plastic DIP	MN1498 40-Pin Plastic DIP	MN1499 64-Pin Ceramic DIP
Power Supply		+5V	+5V	+5V	+5V
Instruction Cycle Time		10μs	10μs	10μs	10μs
Instruction Set		75	57	68	75
Instruction Memory	Instruction ROM	Internal 1024 x 8 bits (8192 bits)	Internal 768 x 8 bits (6144 bits)	External 1024 x 8 bits (8192 bits)	External 2048 x 8 bits (16384 bits)
Total on Chip RAM		64 x 4 bits (256 bits)	32 x 4 bits (128 bits)	64 x 4 bits (256 bits)	64 x 4 bits (256 bits)

16-bit microprocessors, too.

They're ideally suited for a wide variety of computer peripheral and business machine applications. Designed with minicomputer architecture LOCOS MOS N-channel construction for optimum speed and thruput efficiency.

For complete information and prices, write to Panasonic Electronic Components, One Panasonic Way, Secaucus, N.J. 07094; or call (201) 348-7269.

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Introducing the 920-D logic analyzer. Nine channels, 20 MHz and much, much more.

Don't let the low price mislead you. Biomation's new 920-D stands up to logic analyzers costing twice, even three times as much. It includes the functional features design engineers ask for most. And combines them with 9½ pound portability, making the 920-D an ideal field troubleshooting tool.

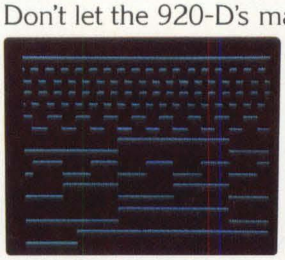
Nine channels — not just eight — give you added capability for more applications. Use the extra channel for recording data, or to mark a trigger location. And select between trigger or clock qualifier. Attach the optional Biomation 10-TC probe pod and you can select up to a 19-bit combinational trigger word.

The 920-D enables you to set a precise interval between the actual trigger and the start of recording, using either clock periods or number of trigger events. Or the pre-trigger recording mode can be selected to capture data from before the actual trigger. The logic threshold level is selectable — TTL, ECL or variable. And you can record at rates from DC to 20 MHz.

Captured data, at 256 bits per channel, can then be displayed on any single channel scope or CRT display in timing diagram format.

Compare the 920-D with other logic analyzers, for both price and performance. Then ask yourself if you can afford to settle for less.

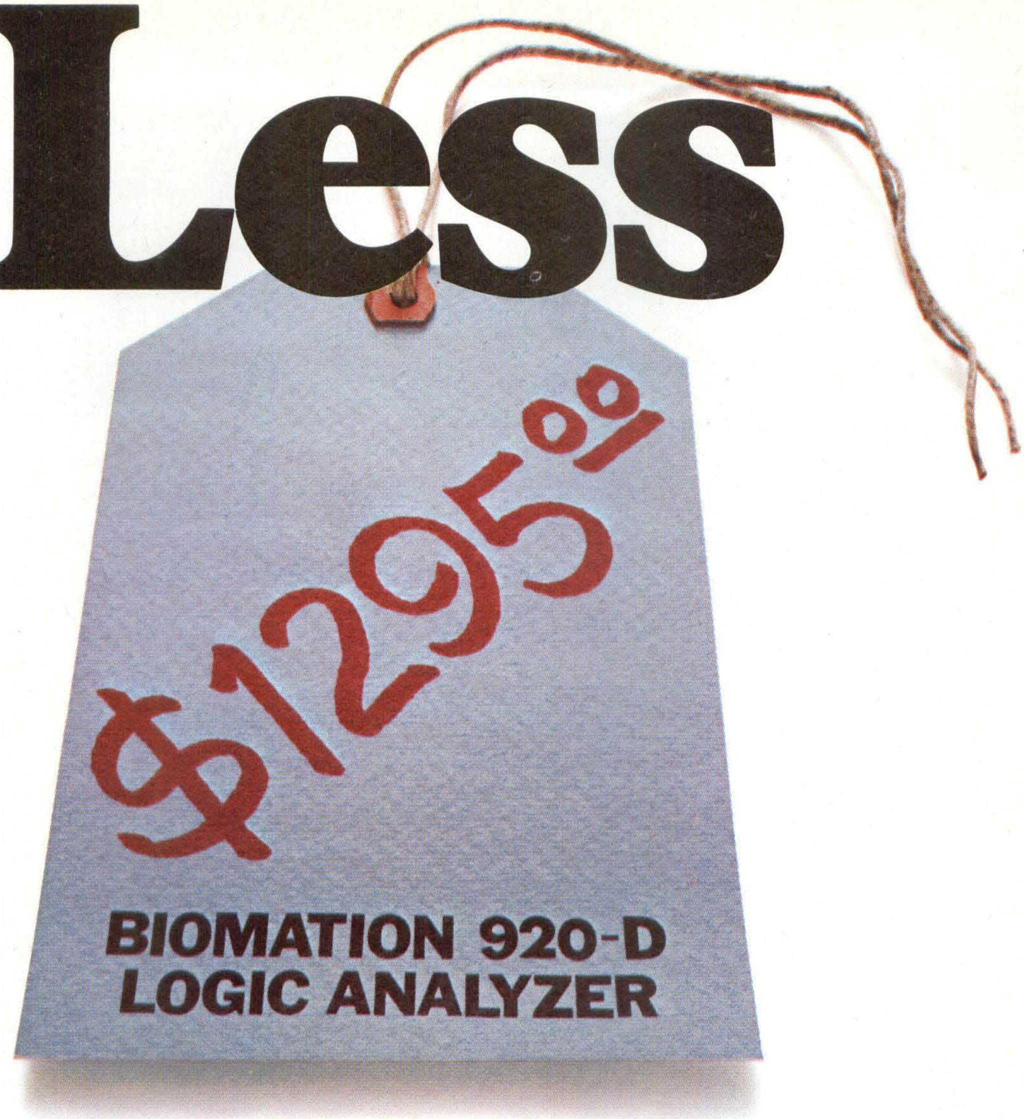
Don't let the 920-D's many features and high performance mislead you. It's priced less — far less — than any comparable logic analyzer.



In fact, the 920-D's $1295* price tag makes it practical to put its extensive capabilities to work wherever you design, debug or troubleshoot TTL logic.

The 920-D is a cost-effective first logic analyzer for most applications. Years of experience providing

Less



thousands of engineers and technicians with the industry's leading family of logic analyzers has helped us design the 920-D with proven real-world features you can put to good use.

Low price makes the 920-D a great choice for your second... or third or fourth logic analyzer. You won't need to stand in line or share your company's only logic analyzer when you have a 920-D of your own.

We built the 920-D for lightweight portability. It weighs in at under 10 pounds and connects to the nearest oscilloscope or CRT. That makes the 920-D the newest tool for field service.

Biomation has led the way in logic analyzer developments. Today there are seven Biomation analyzers, offering from 8 to 16 channels, 10 to 200 MHz capture rate, memory lengths from 256 bits to 2048 bits per channel and operating in both time and data domains.

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Fig 5 Tektronix 8001 development system provides software and hardware emulation, software development support and hardware debug capability for 8080, 6800, Z-80, 9900 and 8085 microprocessors.

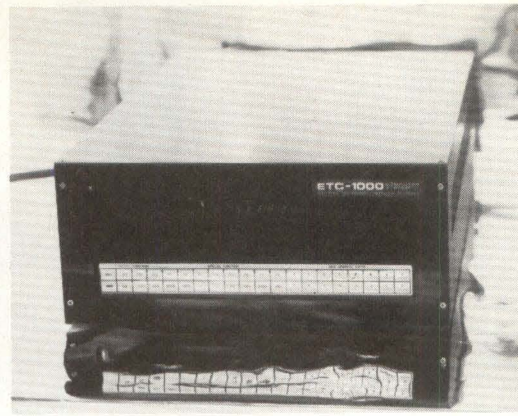

Fig 6 Electronic Tool Company ETC-1000 microcomputer, based on 8-bit 6502 microprocessor, available in several configurations, can have up to 32 K of RAM and dual floppy disks.

I/O and programming capabilities. Intel supports the designer with its Intellec™ development system. Other single-chip microcomputer manufacturers support their product with similar special-purpose development systems. The 8748 contains a 1-Kbyte EPROM (erasable and electrically reprogrammable ROM) which can be programmed in assembly language with the Intellec development system, or in machine language with the less expensive Intellec PROMPT 48 personal programming tool. The CPU in these microcomputers has 96 instructions. Possible applications, according to the manufacturer, include home appliances, electronic games, automotive equipment, small business machines, instruments, data terminals, vending machines and controllers.

Fairchild produces the F3870 MicroMachine™, another 8-bit single-chip microcomputer, with 70 instructions, 2048 bytes of PROM, 64 bytes of RAM, a programmable binary timer and 32 bits of I/O. Software for the F3870 is compatible with the F8, a widely-used microprocessor.

Rockwell produces a line of PPS-4/1 single-chip microcomputers; its most recent addition, the model MM76C, incorporates a programmable high-speed counter-timer. Instruction set size is 53 instructions and it contains a 48x4 RAM and a 640x8 ROM. You can automatically reload the counter with a preset value; serial 8-bit mode with start-pulse detection is possible. The counter functions as a single 16-bit reference or as two independent 8-bit counters. It can count inputs ranging from 2 MHz to days-long frequencies. Two input counting modes are provided: in "event" mode, discrete inputs are counted up or down; in "quadrature sensing" mode, motion and direction can be sensed. PPS-4/1 microcomputers are supported by various design aids, including a PC board development microcomputer, XPO-1, a special MM76C development circuit internally wired to permit real-time operation directed by a program contained in external memory.

American Microsystems recently introduced the S2000, an 8-bit microcomputer with 1Kx8 ROM, 256 bit RAM and 51 element instruction set. AMI supports development of the S2000 with its microcomputer development center, which enables text editing, assembly, simulation, real-time debugging and PROM programming. Various other support options are available.

Microcomputers on a Board

Intel makes a wide range of microcomputer boards and recently introduced two low-cost single-board microcomputers, based on the 8085 8-bit microprocessor. The 80/04, selling for under $100 in OEM quantities, consists of a CPU with system clock generator, system controller and 4-level vectored priority interrupt control, 256 bytes of RAM, up to 4 Kbytes of program storage in ROM or PROM and 22 programmable parallel I/O lines. Selling for under $200 in OEM quantities, the 80/05 offers more RAM storage than the 80/04 and a system interface bus, which the 80/04 lacks. Intel supports their microcomputers with development systems and extensive documentation.

Zilog builds a series of Z-80 based microcomputer boards that fit together in modules. The basic board, designated Z80-MCB, can operate as a single-board computer and contains 4 Kbytes of dynamic RAM, up to 4 Kbytes of ROM. PROM or EPROM and serial/parallel I/O ports. Z80-MCB can be expanded to include greater I/O or memory.

Motorola produces a series of modular microcomputer boards, referred to as Micromodules™, based on the 6800 microprocessor. The M68MM01 computer board has 1K static RAM, Peripheral Interface Adapters (PIA's) to provide programmable I/O and sockets for installing up to 4 Kbytes of ROM. Motorola also produces modules to increase memory and I/O capabilities of the system being designed. Motorola manufactures a "kit" for use in designing with

Tandberg's TDC 3000 Digital Cartridge Recorder.

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Communication. With every computer.

Begin with the industry-proven Tandberg TDC 3000 Digital Cartridge Recorder. Add our new RS-232 I/O controller/interface. And you have a highly cost-effective recording system compatible with *every* computer.

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With *total* communications compatibility, the microprocessor-based RS-232 controller/interface from Tandberg Data is engineered according to EIA Standard RS-232-C, type D and E, and a "teletype-compatible current loop," recording in ANSI/ECMA/ISO-compatible format.

And from the substantial savings in line charges alone, the TDC 3000 with the RS-232 controller/interface will recoup its modest cost in a matter of months. It's hard to beat that kind of cost-effectiveness.

Conceived in the rugged Norse heritage, the Tandberg TDC 3000 is no wilting lily when it comes to tough environments. Put it to work in subzero snow country or under a desert sun and don't worry about the bad vibes or emissions from nearby equipment. The TDC 3000 is engineered to roll with environmental punches.

Modular construction of the TDC 3000 enables the user to configure a system to individual needs. Applications include minicomputer input/output, minicomputer peripheral storage, terminal peripheral storage, software distribution, data entry via keyboard, local data collection, data transmission, and text editing. And a few other things yet to be dreamed up.

Besides RS-232, Tandberg Data provides TDC 3000 interfaces for HP 21MX, PDP 11, 8080 Microprocessor, AN/UYK-20 and 8-bit parallel general purpose. All give up to 48K bits transfer rate.

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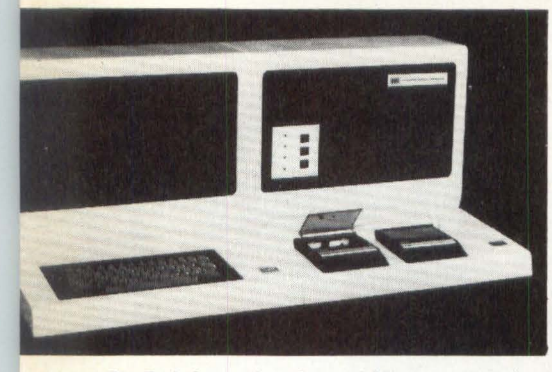

Fig 7 Information Control Microcommand System™ supports development of 8080 and Z-80 microprocessor-based systems with light pen, editor, assembler, monitor, up to 64K RAM and up to 2 Kbytes ROM, dual floppy disks, EPROM programmer, keyboard, CRT and optional In-Circuit Debugger.™

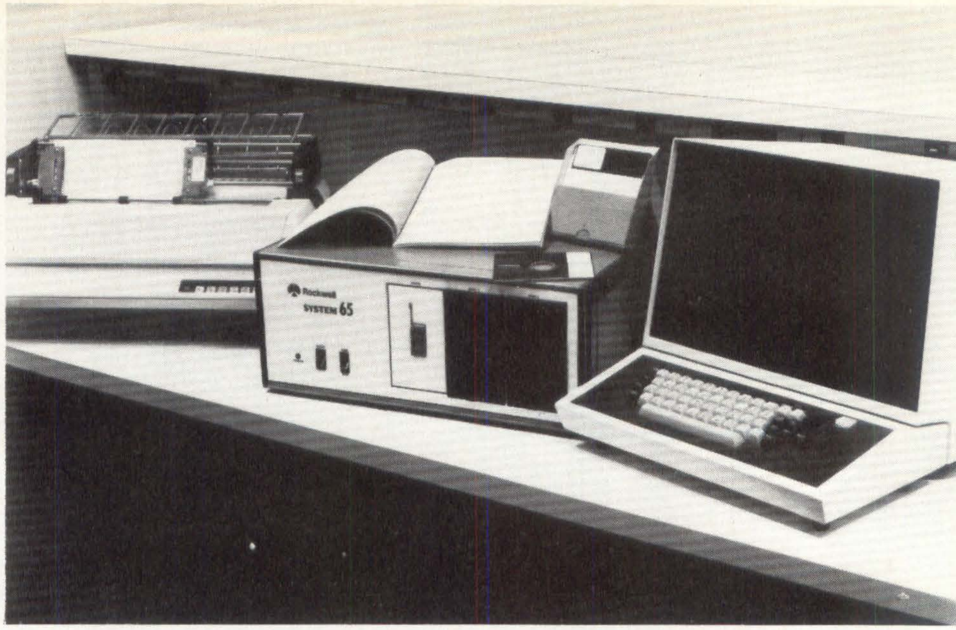

Fig 8 Rockwell System 65 development system supports R6500 microcomputer system development with dual minifloppy disk drives, 16K bytes of static RAM plus ROM-based resident system software, monitor, text editor and assembler.

6800 series microprocessors that includes documentation and simple hardware for programming and debugging 6800-based systems at relatively low cost.

Microcomputers in a Cabinet. Most microcomputers in this category, while packaged, do not come with extensive peripherals. Generally used in industrial control applications, they vary somewhat in the degree in which their manufacturers have tailored them for specialized applications.

Warner & Swasey produces System 4 and RT-4 4-bit microcomputers, both of which use 4040 microprocessors, for special-purpose industrial control applications. The RT-4, with 1Kx8-bit words of PROM and 320x4-bits of RAM, is a modular system in which the CPU and various I/O modules are plugged into a motherboard housed in an oil-tight industrial enclosure. With greater memory capacity than the RT-4, the System 4 suits many of the same applications, such as machine tool control, remote monitoring and control, material handling control, data entry and retrieval, traffic control and energy management. The company also produces a System 8, based on the 8080 microprocessor, suitable for complex industrial measurement and control applications. Warner & Swasey supports its microcomputers with FORTRAN compilers, available on timesharing systems or able to run on the user's computer. A microcode assembler is available for users wanting to define their own microcoded instruction set. System tester and program analyzer are available, as is a programmer's console to provide online control and diagnostic capability.

Wyle produces a series of microcomputer modules, based on the 8080A microprocessor, that you can assemble in various configurations, depending upon user requirements. Wyle provides separate modules for CPU, memory (1K and 4K RAM, 256 word RAM/1K ERPROM, 4K ERPROM), I/O, priority interrupt, timing, operator/programmer's panel, PROM programmer, direct memory access and paper tape reader. Wyle can provide the customer with resident assembler or cross-assembler (using a PDP-11), a relatively simple and inexpensive development system and various software packages. Primary applications of these microcomputers are process control and monitoring and data collection.

Data Numerics manufactures the DL-8A microcomputer, 8080-based, with 4K RAM, 2K PROM, four 8-bit I/O registers, Universal Asynchronous Receiver-Transmitter (UART) for teletype or any RS-232 terminal operation and an interrupt system with priority resolution and self-identifying vectors. Users can expand memory to 64K. Edit and assembly programs are available resident with the DL-8A and as programs which execute on a PDP-8, PDP-11 or from timesharing services.

Process Computer Systems offers its PCS SuperPac 180 microcomputer, an 8080A-based machine designed primarily for on-line direct control in industrial automation applications. The 180 comes with a 64 character ASCII keyboard and CRT with character generator capable of presenting 7x9 dot matrix characters. You can customize the system with various modules – memory, keyboard interface, I/O, A/D and D/A conversion. Real-time operating system and FORTRAN compiler are available.

Fabri-Tek manufacturers the MP12 microcomputer, a 12-bit modular machine designed for industrial control, laboratory automation, data communications and data acquisition. The MP12 provides a 4Kx12 magnetic core RAM, direct memory access, hardware interrupt capability and a PDP-8-compatible instruction set. Additional modules increase memory and provide I/O and D/A or A/D conversion.

Data General supplies microNOVA 16-bit computers, using the mN601 CPU chip, in board or cabinet configuration, for use in instrumentation, industrial automation, communications and data acquisition system (Fig 4). The cabinet version of the computer, referred to by its manufacturer as a minicomputer, contains a 4K word RAM, optional RAM and PROM to 32 K, single or dual diskette subsystems providing up to 315 K words and I/O and other boards. The manufacturer provides a software library and makes available a disk operating system, assembler and FORTRAN IV compiler. Data General also provides a devel-

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opment system for use with mN601-based microcomputers.

Plessey Corp. manufactures the Miproc 16-bit microcomputer, a high-speed machine for special military and commercial applications such as signal processing, multiplexing, weapon control systems and industrial control . Miproc 16 can process up to 4 million instructions per second, with a maximum data throughput of 20 Mbytes per second. The system has 83 basic instructions, expandable to 170, and various memory options – up to 8Kx16 RAM and 8Kx16 PROM. Cross-assemblers are available for various computers and timesharing. Plessey also manufactures a supporting development system.

Modular Component System Microcomputers. Microcomputers in this category may remind you of minicomputers – they can be programmed in a high-level language, and some of them were designed for people who don't know very much about computers. A wide range of easily interfaced optional peripherals is usually available.

Texas Instruments manufactures general-purpose 16-bit minicomputers and microcomputers, based on the TMS9900 microprocessor. The microcomputer, designated model 990/4 (Fig 3) consists of 24Kx16 word memory, floppy-disk ROM loader, video display terminal and dual FD 800 floppy disk. Hard copy devices can be interfaced directly. Available high-level languages include FORTRAN IV, COBOL and Multiuser BASIC. Texas Instruments provides software support and a disk-based development system.

The Components Group of Digital Equipment Corp. offers the 16-bit LSI-11 microcomputer system, used mainly in specialized process and control applications such as remittance processing systems, ultrasonic scanning systems, distributed process control, voice input terminals and computer numerical control. The LSI-11, using the same 400-instruction set as the PDP-11 minicomputer (also manufactured by Digital), fits many of the same applications. LSI-11 contains a 4Kx16 RAM, expandable up to 64 Kbytes, and various I/O interfaces and peripherals. Digital claims that over 30,000 PDP-11s are in use and the extensive library of programs for these computers is compatible with the LSI-11.

Who's Programming?

Increasingly, designers are doing their own programming. In the "old days," with larger computers, the designer would generally assign programming to programmers and stick with hardware. Most designers now feel that they must do their programming to stay on top of the product they are developing. If that product eventually requires changes, then the designer will make them, and more likely than not, the program modifications will land in his lap. An argument can be made in favor of farming programming out to "experts" if the program is a one-time only exercise and the designer is never going to be called upon again to change or update the product.

Also compatible are assembly and higher-level languages available for PDP-11. Digital provides documentation and training services for the user.

General Automation offers 16-bit GA-16/110 and GA-16/220 microcomputers. The GA-16/110 is designed as a "load and go" worker computer for dedicated applications, rather than as a software development system; the more expensive GA-116/220 contains hardware needed for program generation. Both computers are compatible with software and I/O of GA-16 and SPC-16 series computers. Memory can be expanded to 64 Kbytes. Program assembly tools enable using assembly and high-level languages such as FORTRAN, COBOL and BASIC.

Pacific Cyber/Metrix manufactures the PCM-12 microcomputer, using a 12-bit IM6100 microprocessor that is "essentially an LSI version of the PDP-8 CPU," according to PC/M. The PCM-12 is therefore compatible with PDP-8 series minicomputers software. You may purchase PCM-12 as a kit or fully-constructed. A wide range of peripherals is available, as are various memory and I/O options.

Electronic Tool Company offers its ETC-1000 (Fig 6) 8-bit, 6502 microprocessor-based microcomputer in various configurations, depending upon user requirements – from hobby to scientific computing and data processing. Software consists of three levels of operating systems plus language processors and other software aids. The ETC-1000 can be configured with up to 32K of RAM and dual floppy disks. CRT display with integral keyboard and buffered interfaces are standard.

Electronic Memories & Magnetics Corp. manufactures the System 800 microcomputer, which uses a high-speed bipolar 8080 emulator. It is compatible with the 8080 instruction set and widely available software for the 8080, but runs at higher speed. The system offers 32 Kbytes of RAM, expandable to 1 Mbyte and optional nonvolatile core memories. Intending the system to compete with minicomputers, the manufacturer also offers disk drives, CRT display and line printer and delivers System 800 with an operating system and Enhanced BASIC.

MITS Corp., a Pertec subsidiary, manufactures the Altair™ 8800b microcomputer, an 8080A-based general-purpose machine used in home, business, scientific and educational applications. Available software includes Altair BASIC, a disk operating system and an assembly language development system. Memory can be expanded up to 64K of directly addressable memory and up to 256 separate input and output devices can be addressed. The manufacturer provides various peripheral options, including floppy disk, printer and CRT terminals.

Processor Technology Corp. makes the Sol-20, an 8080-based microcomputer that its manufacturer says is the "first small computer designed as a complete system," and which is operable "without any prior computer experience." Sol-20 comes with an 85-key keyboard, video display circuitry (for a TV monitor or standard TV), 1K word RAM, 1K word ROM, cassette interface, parallel and serial I/O interfaces and software including preprogrammed PROM personality module and cassette with BASIC-5 and two "sophisti-

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  1600 CPI Phase Encoded Model—$19,950

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cated" video games. The computer will find application with hobbyists and and in home, office and laboratories, according to Processor Technology.

Where Microcomputers Are Going

We asked manufacturers who submitted product information to us to predict how microcomputer technology would evolve by 1980. There seems to be a general consensus among them that certain well-established trends in the industry toward lower cost, greater miniaturization and faster speeds will continue. These trends, widely read about and in many cases their results directly experienced by people in the industry such as the readers of this magazine, are not exactly news. A few of the specific comments made by the manufacturers may raise an eyebrow, however. Shay Adams, a marketing executive with Pro-Log, for example, suggests that by 1980 the microprocessor industry will address itself more to "real-world" designs, improve low-end CPU technology, limit attempts to emulate minicomputers and instead advance dedicated control-type architecture. John Staller, manager of marketing services with Warner & Swasey, a manufacturer of industrial control microcomputers, foresees that by 1980 the only type of industrial machinery available will be that controlled by microcomputer-based systems.

Dick Anderson and Roger Helmick of Rockwell, addressing the issue of the effect the evolving technology will have on designers, foresee continued change in the engineer's job. Increasingly they see software becoming an off-the-shelf item, just as hardware is now. This idea is echoed by many in the industry and we have already seen changes in this direction. Higher-level languages are becoming increasingly available on microcomputers – it may be that soon the only people who need to worry about machine language will be those who manufacture microprocessors.

In the January Issue of *Digital Design,* we will continue our coverage of the microcomputer revolution with a report on the role of the development system.

BUYER'S GUIDE

This buyer's guide lists manufacturers of microcomputers and of development systems. A word of caution, however: we only indicate what a manufacturer makes if we have first-hand information. In some cases, manufacturers did not respond to our request for information, and in other cases the manufacturer may not have told us about its entire product line. As noted in the text, most microcomputer manufacturers also make development-related products – hardware and software – to assist designers using their systems in the product development process. This means that, even if a particular manufacturer is not in the business of making development systems, it may still provide tools to aid the designer. Contact manufacturers directly for information or circle the appropriate number on the reader service card.

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Applied Data Communications 1509 East McFadden Ave. Santa Ana, CA 92705 (714) 547-6954 **Circle 227**	•	
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While others promise to improve 2901 Bit-Slice performance, Signetics delivers the promise.

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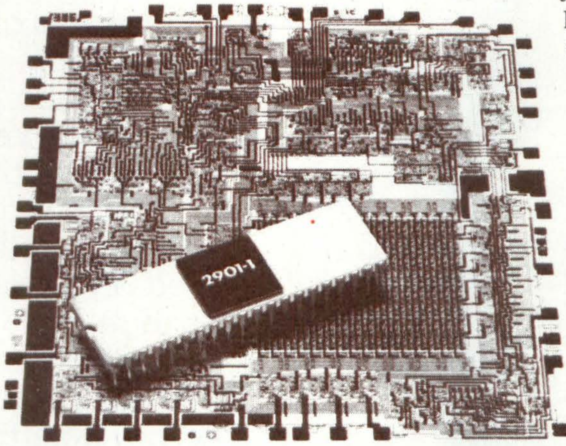

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CIRCLE 36

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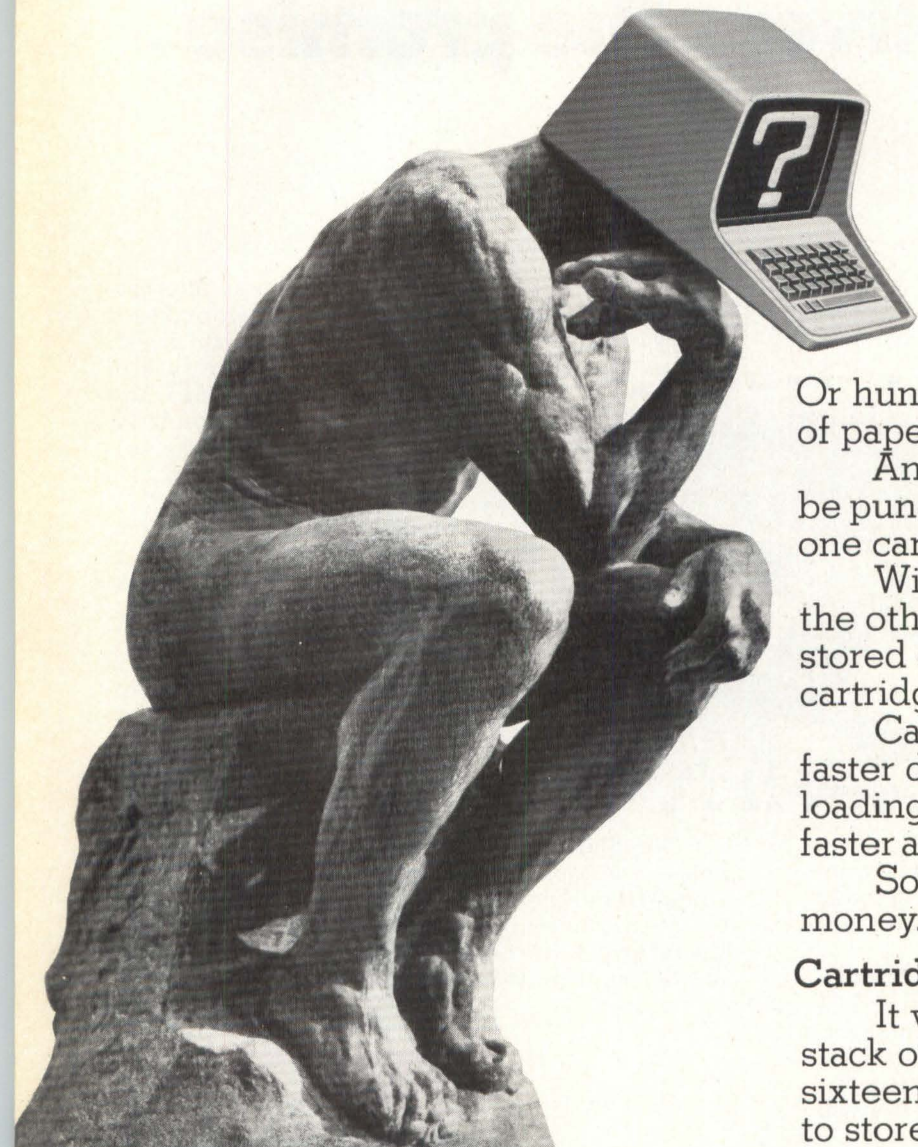

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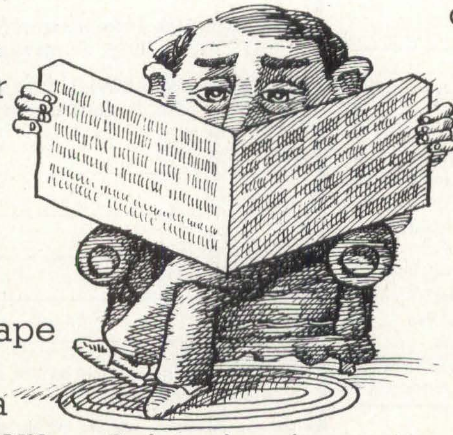

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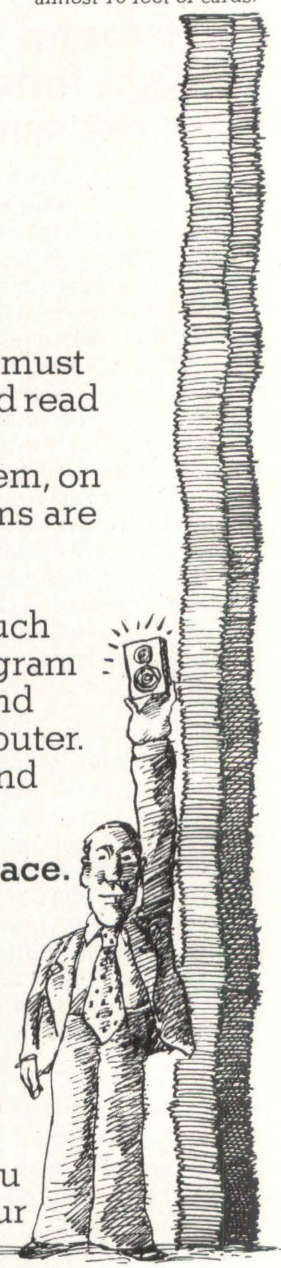

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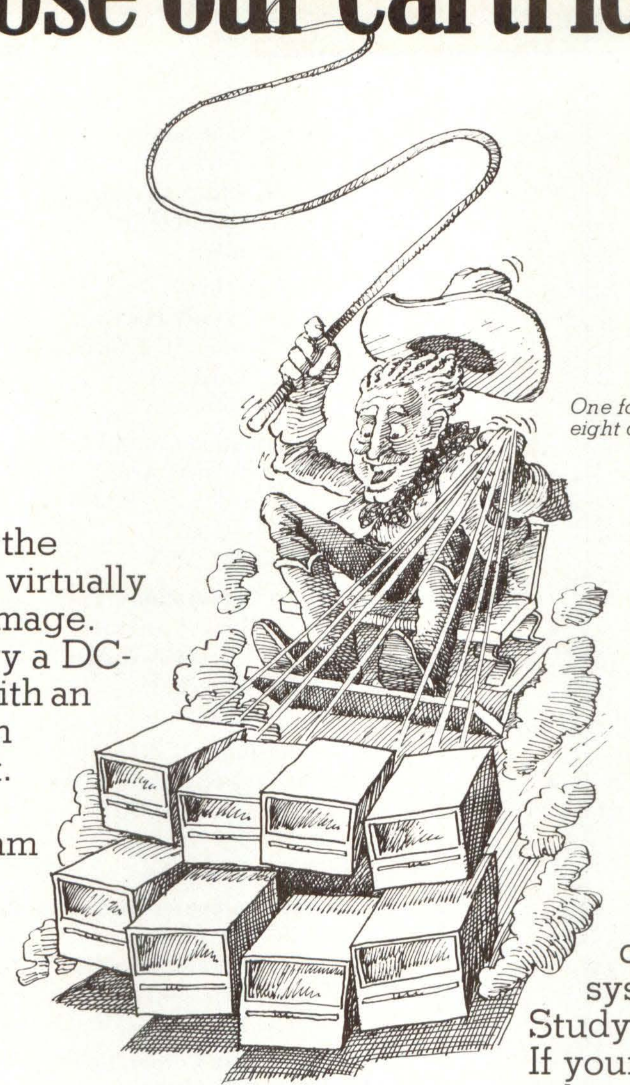

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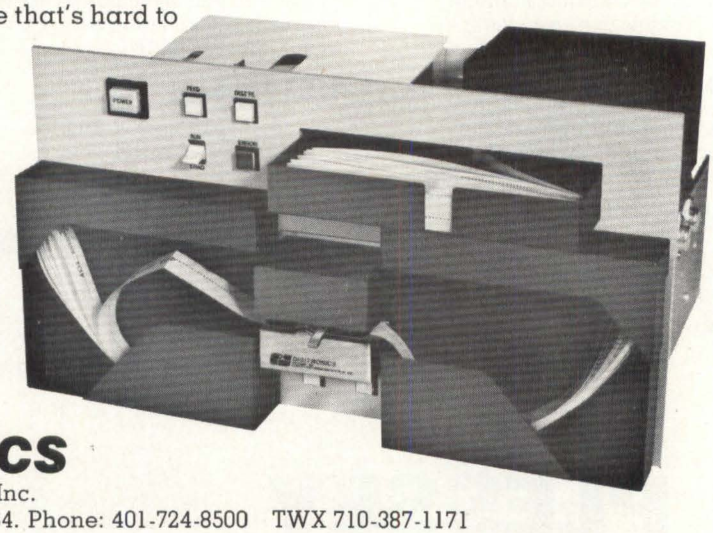

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making microcomputer programming easier

by Carol B. Shaw

When an engineering team designs a microcomputer-based piece of equipment, it can develop the software quicker with a Diskette Operating System (DOS). In addition, software packages for such functions as text editing, compiling and debugging, currently available from many microprocessor/microcomputer suppliers, also make programming easier and faster. Both types of programming tools cut debugging time significantly.

Here's how microcomputer programming evolved. When microcomputers first became available, software development facilities virtually did not exist. Users had to translate programs into machine code by hand and then toggle them into the machine through the front panel. Soon, the industry developed cross-assemblers to run on minicomputers or large computers and produce punched tape or other outputs to be read into the microcomputer memory. When addressable memory sizes increased, assemblers became available to run directly on the microcomputers. Now, a microcomputer with a DOS can provide complete editing, assembling, compiling, linking, loading, debugging and file management facilities, and eliminate the need for costly large computers in micro software development.

What factors should you use to compare microcomputer system software? To help you make your choice we shall provide basic operating system definitions and features, and describe the types of support programs available with microcomputer DOS development systems.

Know Your Application

When choosing a microcomputer system, you must consider hardware and software. A unit with a sophisticated operating system (OS) and diskette drives costs more than one without, but usually saves money in the long run, because the DOS greatly reduces development and maintenance time.

Since your system must satisfy the requirement of your application, you must consider the following factors:
• Are you going to integrate the operating system into the final product? If you are, can you use it for software development or do you need a separate development system?
• How fast is the operating system? How much memory space does it require? • If you expect to purchase optional software packages for the system, how much memory do they require? • Is the application single or multiple task; that is, will several programs run concurrently? • Will the system have one user or multiple concurrent users? • Does the system need to operate in real time? • Which peripheral devices are standard on the system? Will the system require special interrupt handlers for nonstandard devices? • Does the application require file management capabilities? • Is the system easy to use, well-documented and reliable?

You can answer these questions by defining your application and then comparing your needs with the specifications of currently available operating systems.

Diskette Operating System Definitions

An OS is a collection of programs that manages the resources of a computer. These resources include allocation of the CPU, main memory (RAM, ROM, PROM) and peripheral devices such as diskettes, lineprinters and terminals. An OS can be thought of as a group of "tasks" or "processes" running concurrently. Fig 1 shows how a task interacts with the rest of the system. When a user program is run, a new task is created. If several user programs can be run simultaneously, then the system is said to be multiprogrammed.

In reality, since only one task can run at a time, a multitask OS must provide a mechanism for switching from one task to another. Several methods exist for deciding when to switch and which task to run next. One method uses a time-sliced system; that is, each task runs for a small, fixed amount of CPU time, then is suspended and the next task in line is started up. In an event-driven system, such as MuPro's Multi-User/Multi-Task Executive (MUTE) DOS, switching occurs only when a significant event such as a completion interrupt from a peripheral device or a task completion occurs (Fig 2).

In most systems, tasks are assigned different priorities so that the most important things are done first. For example, let's consider a system with a lineprinter. This peripheral is often the bottleneck because it is relatively slow and in high demand. Giving the lineprinter's I/O driver a high priority keeps the printer busy as much of the time as possible. The driver is suspended while it waits for each line to be printed. The ordered-according-to-priority task queue contains information on all of the tasks. The task scheduler starts up the highest priority task which is ready to run.

Interactive capability is a key DOS feature. In an interactive system, a prompting message appears on the user's terminal; the user enters a command and receives a response. The time between the command entry and reply is called the response time and is proportional to the difficulty of the requested task and the load on the system. If this wait time is too long, the user becomes frustrated. An interactive system allows the user to send data to a program from the terminal during execution, whereas a batch system does not.

Some interactive systems allow the user to put several

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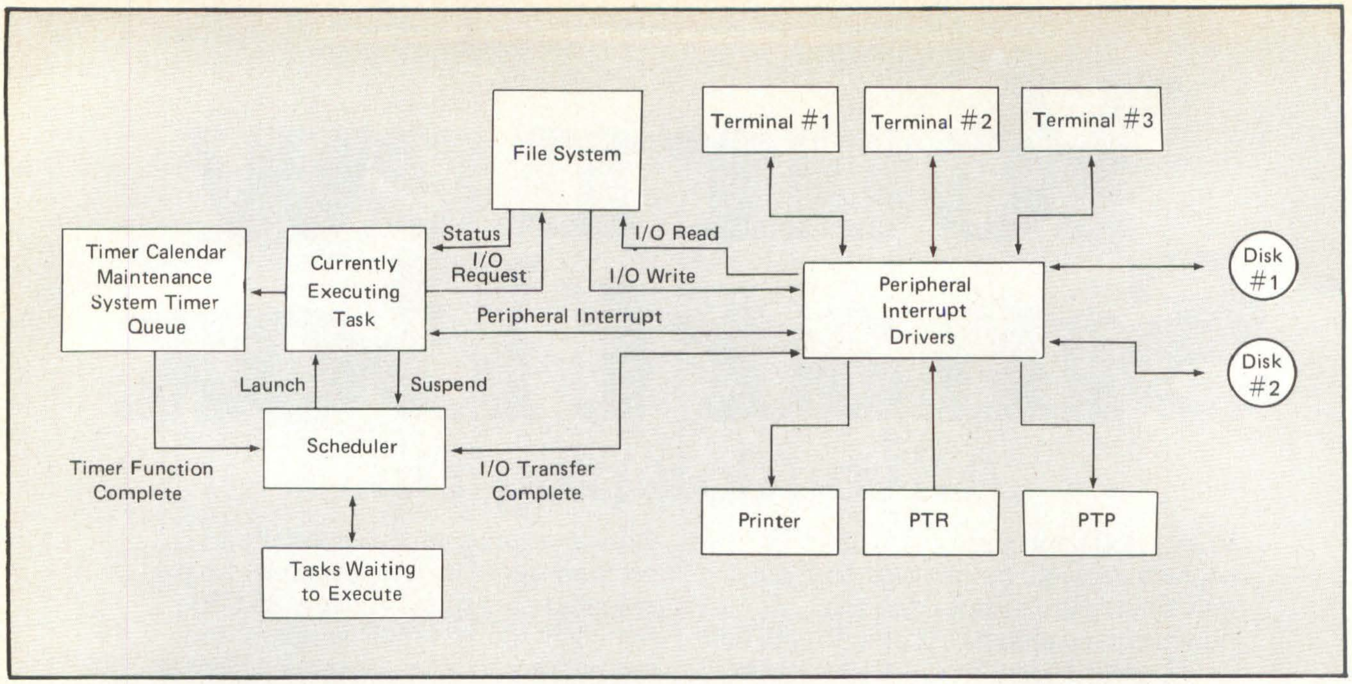

Fig 1 Simplified multitask operating system block diagram shows how the currently executing task interacts with peripherals through the file system: It is launched and suspended by the task scheduler.

commands on the same line to be executed sequentially before the next prompt appears. A few systems have a read-ahead feature which allows the user to enter new commands or program input before the previous input line has been processed. In a multi-user system, several people on separate terminals can use the system at the same time.

Some operating systems are called "executives." Usually these are real-time systems which must be reconfigured for each application. An example is Intel's RMX/80, which is supplied as a collection of relocatable program modules. After the software has been developed on the Intellec Development System, it is linked with the desired system modules and stored in ROM, PROM or RAM. RMX/80 has an optional diskette driver that gives the system a file management capability.

Memory protection, which prevents one user from destroying another user's programs and data, is generally found on large computers. When a user's program tries to access memory outside its allocated area or do I/O, an interrupt is generated which starts up an OS routine. The OS can terminate the user program with an error message or execute privileged instructions, such as I/O, that are not available to the user.

The average microcomputer, on the other hand, lacks privileged instructions and hardware memory protection. The OS can allocate a different part of memory to each program, but it cannot prevent a program from branching outside its own area. Since an undebugged program may destroy the OS programs, it may force you to reboot the system. Thus, a multi-user microcomputer system without protection features must be a cooperative effort. Several people can edit and assemble at the same time, but they may want to restrict the system to one user at a time when debugging an untested program. Fig 4 shows where each system program resides in memory in one microcomputer system.

The file system, a part of the OS, manages information storage and retrieval. In some systems, all peripheral devices, including lineprinters, readers, punches, terminals and diskette drives are treated as files. This arrangement means that user programs treat all I/O in a similar fashion, without wor-

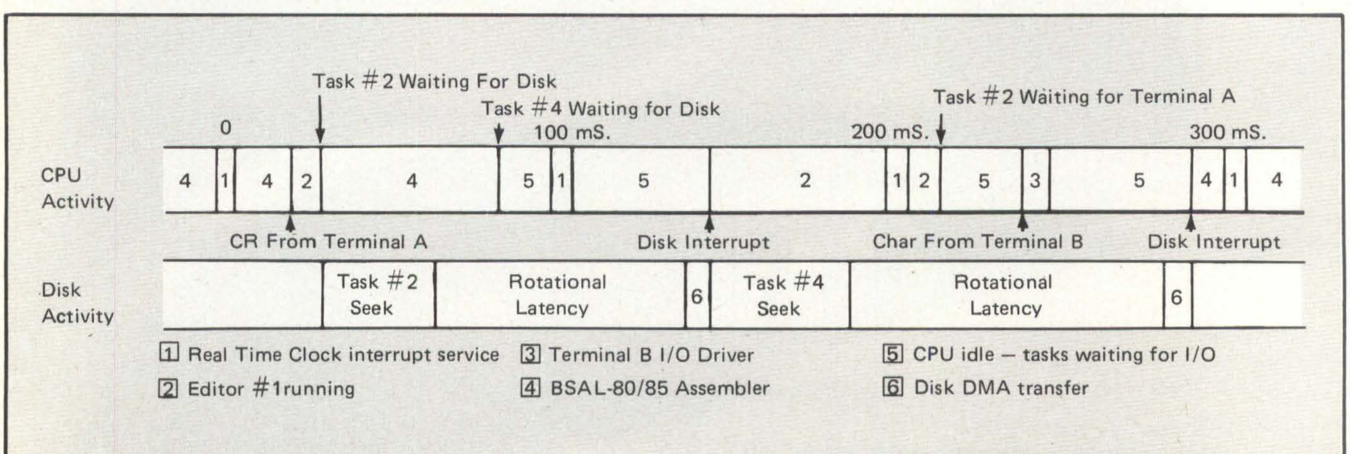

Fig 2 In an execution sequence of an event-driven OS, an editor (task # 2) is interacting with terminal A user. The lower priority assembler (task # 4) executes while the editor waits for terminal or diskette I/O.

rying about the particular characteristics of a peripheral. There are many file management routines that a user program may call. Disk program and data files are accessed with the same system routines.

A good file system allocates diskette space so that the user does not need to know the physical location of his/her file. Files are accessed by specifying the file name and record number. Deleting and creating files can cause diskette fragmentation – the division of available space into many small pieces, none of which is big enough to hold a new file. In some systems, the diskette must be compacted or pushed together periodically to create one large free area.

Some file systems offer techniques for minimizing fragmentation. For example, in MuPro's DOS, a file can be broken up into pieces called "extents". The file can fill in several small holes with extents, instead of occupying one large contiguous set of sectors on the diskette.

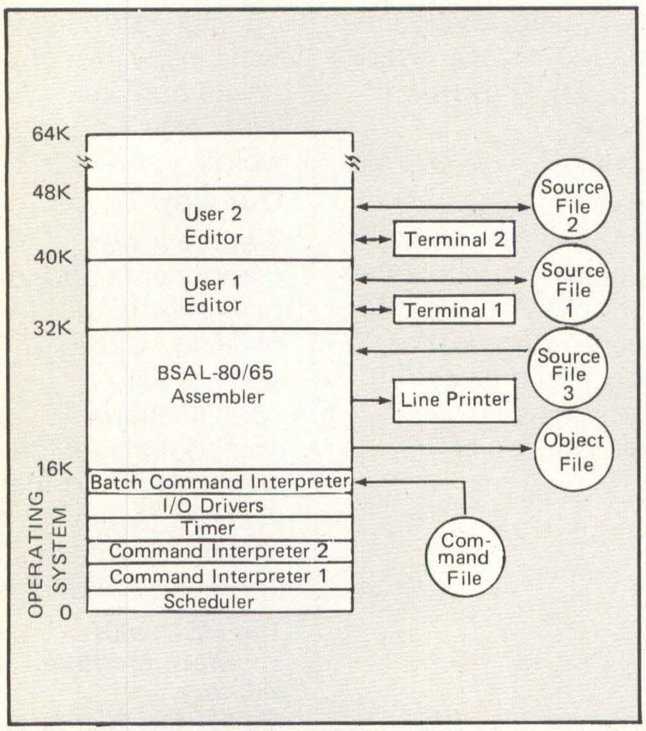

Fig 3 In this two-terminal system, the lower 48K of memory is allocated to the system tasks and the rest of the memory, to user tasks.

Another useful file system feature is the user directory. The file system allows the user to group files on each diskette into several user directories. A separate directory can separate the files for various programming projects. When referring to a file, the user may specify the diskette drive number, directory name and filename. If only the filename is specified, then the OS will use the default directory name which was set up at the time for setting the default disk and user name for searching the files.

Associated Program Packages

Most microcomputer development systems include a variety of programs that are not technically part of the OS, such as editors, assemblers, compilers, linkers, loaders, debuggers and utilities. Some of these are written as subroutines linked in with user programs. Others are run as separate programs, with user programs as inputs.

Text Editors. An interactive text editor can greatly facilitate software development. With the editor, the operator enters into the system through the terminal keyboard. A diskette file stores them. The user can make changes in a file quickly and easily with such editor commands as ADD, DELETE, COPY, GATHER, FIND, MODIFY, LIST and REPLACE. Usually the commands can be abbreviated (for example, A for ADD) to save keystrokes, once the commands have been learned.

The lines of text in a file are numbered so that individual lines can be identified and accessed. In some editors, all of the lines are renumbered every time new lines are added or deleted, so that the numbers always run consecutively, starting with 1, 2, 3, etc. In other editors, new incremental line numbers are inserted. For example, lines added between lines 100 and 101 could be numbered 100.1, 100.2, 100.3. In this scheme, since text lines retain their original line numbers, it is easy to determine where changes have been made.

Programming Languages. Since machine language is no longer used extensively, languages can be divided into two basic categories: assembly (or assembler) and high level. Assembly language is the most efficient in terms of speed and memory use, because each instruction corresponds one for one with a hardware machine instruction. The programmer must manipulate registers and allocate memory space for all variables. Assembler opcode mnemonics are sometimes hard to understand and each computer uses a different set of mnemonics. To make a program intelligible, a comment is needed on nearly every line.

High level languages include ALGOL, FORTRAN, BASIC and many others. When using these languages, the programmer does not have to worry about register or memory allocations, because the compiler or interpreter takes care of such details. Consequently, programs in these languages can be machine-independent. However, the programs usually run slower and less efficiently than they would in assembler, because the code is not optimal. High-level programs require fewer lines of source code and less detailed comments than assembler language programs, and usually require less time to code, debug and maintain.

Some languages, such as ALGOL, contain control structures that make it easier to follow the flow of control within a program. Such constructs as "IF condition THEN BEGIN . . . END ELSE BEGIN . . . END"(Fig 5) and "DO . . . WHILE condition" encourage structured programming. Languages similar to ALGOL are available on some microcomputers. FORTRAN, the first high-level language, lacks such control structures, but benefits from being standardized and widely used.

An interesting compromise between assembler and high level languages, MUPRO's BSAL-80 (Block Structured Assembly Language), uses a statement syntax similar to ALGOL's, but is just as efficient as assembly language, because most statements correspond directly to machine instructions. BSAL-80 has the "IF condition THEN BEGIN . . . END ELSE BEGIN. . . END" construct that makes block structured programs possible.

Assemblers/Compilers/Interpreters. Programs for converting source statements into executable object code are called assemblers for assembly language and compilers for high level languages. Interpreters perform source code analysis as a program is being executed, so that no object code is needed.

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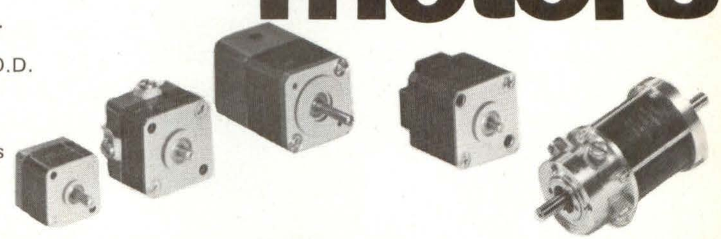
MINIATURE DC PM INSTRUMENT motors

APPLICATIONS

- DAISY WHEEL DRIVES
- PRINT HEAD DRIVES
- INSTRUMENT RECORDERS
- LABORATORY INSTRUMENTS

FEATURES

- Torques from 2 to 50 oz-in.
- .75 inch cube to 1.25 inch O.D.
- Cartridge brushes
- Alnico or rare earth magnets



PM STEPPER motors

APPLICATIONS

- PRINTER RIBBON DRIVES
- PRINTER PLATTEN DRIVES
- CARD SORTERS
- OFFICE COPIERS

FEATURES

- Step angles 7.5°, 15°, 30°, 45°, 90°
- 1.1 inch to 2.8 inch O.D.
- Ceramic or rare earth magnets

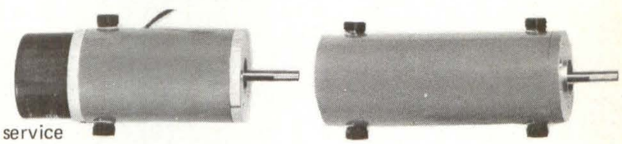
INTEGRAL ENCODER AND motors MOTOR-TACHOMETER ASSEMBLIES

APPLICATIONS

- PRINTER CARRIAGE DRIVES
- COPYING MACHINES
- SPEED CONTROLS
- MACHINE TOOL CONTROLS

FEATURES

- Optical encoder resolution to 1000 cycles
- Solid state gallium arsenide light source
- Integral assemblies – no assembly or alignment necessary
- Single source for motor/encoders eliminates costly assembly & simplifies service



DC PM HOLLOW SHAFT TORQUE motors

APPLICATIONS

- INERTIAL NAVIGATION PLATFORMS
- AIRCRAFT INSTRUMENTS
- AIRCRAFT CONTROLS

FEATURES

- Torques from 6 to 500 oz-in.
- 1.1 inch to 5.2 inch O.D.
- Precision tolerances
- Gold commutators
- High reliability

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CIRCLE 43

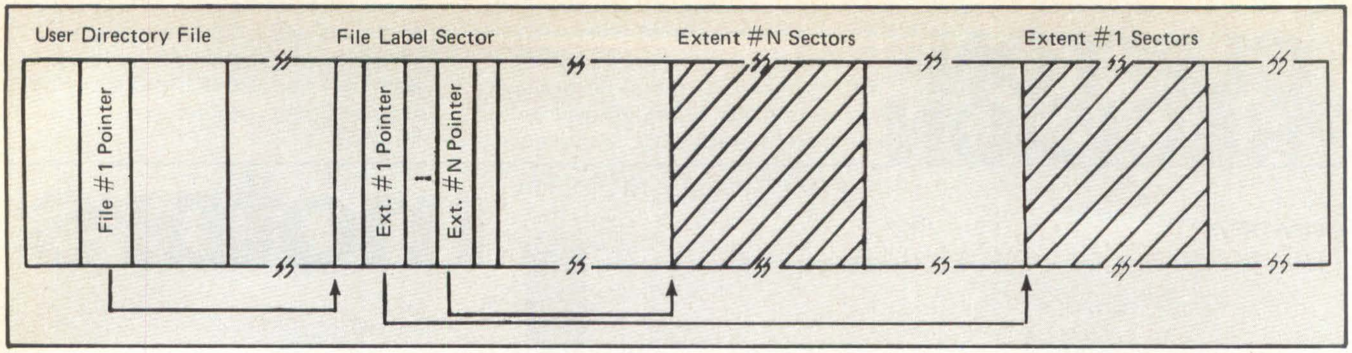

Fig 4 Each disk file in this type of organization can consist of up to 8 separate extents.

Assemblers produce absolute or relocatable code. Absolute code must be loaded into a fixed location in memory, whereas relocatable code can be loaded anywhere. Relocatability is advantageous, because several program modules can be developed independently without worrying about the location of the other modules, then linked together into one program module. Some assemblers possess a macro capability that allows a user to associate an identifier with a block of text which is substituted every time the macro is invoked. Parametric macros allow a different parameter value to be used each time a macro is invoked.

The listing produced by an assembler/compiler should be easy to follow with line numbers, address, source and object code all shown on the same line. Error messages should be easy to find and understand. A symbol table and cross-references are extremely useful in locating variables and labels and the statements that refer to them (Fig 10).

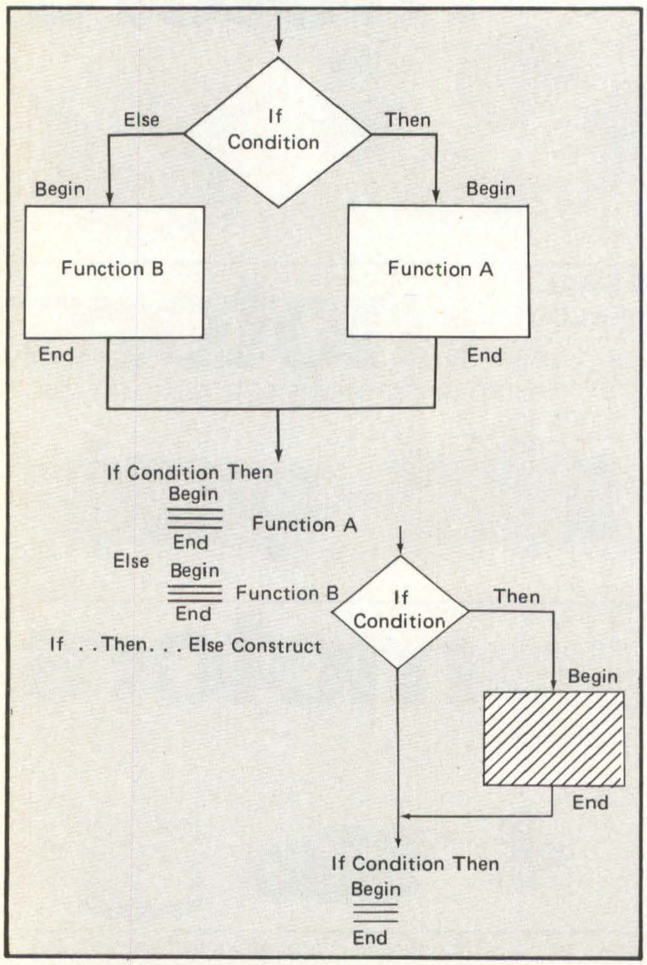

Fig 5 Flowcharts and equivalent program statements are given for ALGOL "If . . . Then" control structures.

Linkers/Loaders. A linker combines relocatable object modules into one absolute or relocatable program module and produces a load map giving the address of each symbol that has been declared as an entry point. MUPRO's linker also provides a cross-reference table telling which modules reference each symbol.

A loader transfers the program file from diskette to main memory so that the program can be executed. Some systems have a single combination linking loader program.

Debuggers. A debugger allows one or more breakpoints to be set so that the user program can run until a specific memory location is accessed. The break may occur at memory read and write or just at instruction execution. Memory locations and registers may be examined and changed. The program can be stepped through by executing one instruction at a time. A program trace facility allows the user to follow the order of instruction execution.

In some systems, the debugger must be specified during the linking process and becomes part of the program module. In others, the debugger is run as a separate program. The front panels of some microcomputers have switches, LEDs and hardware debugging circuitry.

Utilities. Provided with the system, utilities perform general-purpose functions. Examples include multiplication/division subroutines for computers which do not possess these functions in hardware, and conversion routines such as binary to ASCII and binary to BCD.

The Bottom Line

Choosing a DOS requires careful consideration of the support it can provide for each application. Today's microcomputers provide features previously found only on larger systems such as multi-user, multi-programming and random access file systems. Program packages are available for text editing, compiling, debugging and other facilities to aid program development.

Microcomputer applications in which recurring production costs or execution speed are important factors demand efficient use of the machine architecture and instruction set. Software design and maintenance costs are also important considerations, and often far exceed the hardware engineering costs. An operating system and its associated editor and programming languages must take these factors into account.

Carol B. Shaw *is a systems programmer at MuPro, Inc., 424 Oakmead Parkway, Sunnyvale, CA.*

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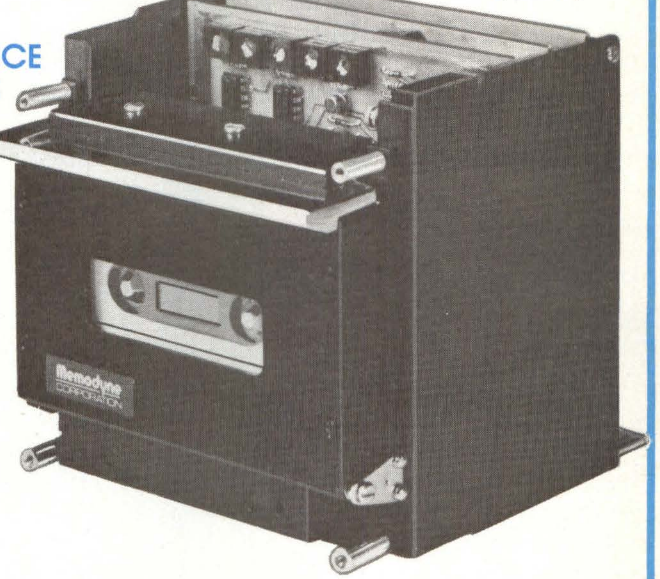

FEATURES

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Control Signals:
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Start Distance to ±5% of 20 Inches Per Second:
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CIRCLE 44

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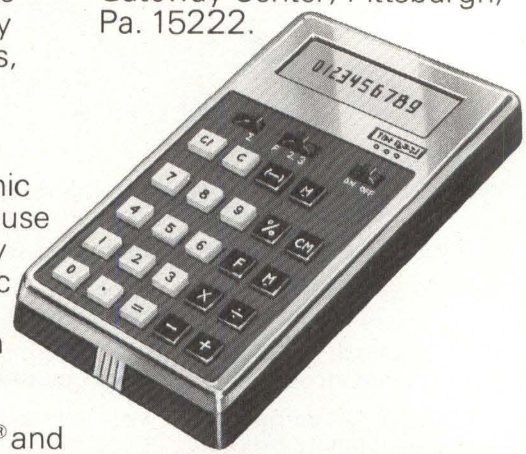

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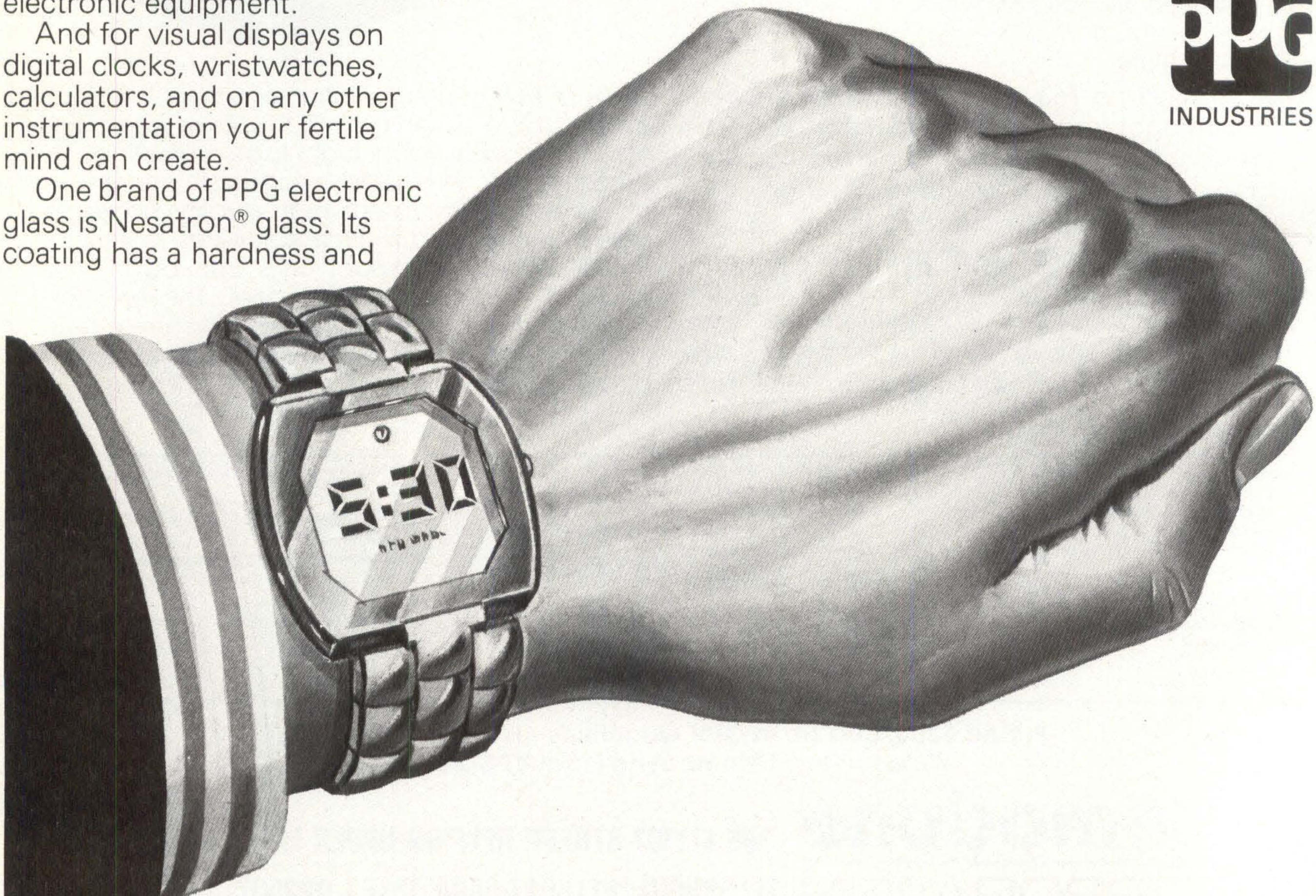


CIRCLE 45

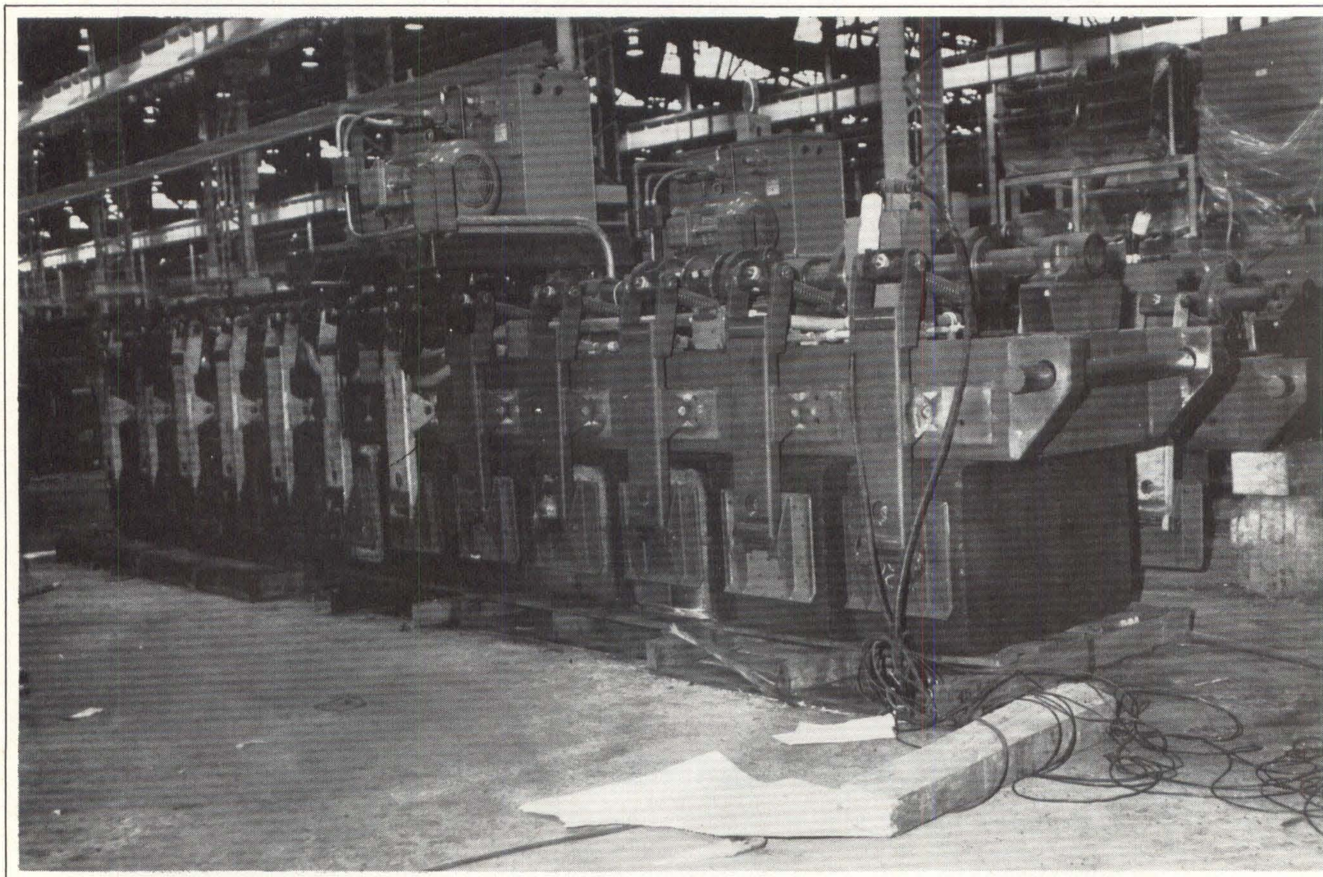
Microprocessor Control Of A Bridge Crane

by Sharon Pellerin

Last winter, after accepting the task to replace five miles of gravity conveyor with a computer-controlled bridge crane system, Control Logic, Natick, MA and their parent company, Harnischfeger Corp., began work. Their customer, a major aluminum manufacturer, requested the crane system for storing carbon blocks. The aluminum maker carries an inventory of as many as 12,528 carbon blocks, each measuring 1.5 by 1 by 3 feet. Half of these blocks, in a green state, occupy the east storage area waiting to be baked. The other half are baked and ready for use.

For discussion purposes, only a portion of the project receives treatment here. Control Logic engineers designed and built the crane system electronics which includes two 8080-based systems. The first system is called the ground console (GC) and the second the on-board controller (OB). Control Logic programmer Ted Knowlton wrote the software to control both systems. The ensuing article delves into Knowlton's six-month development effort in an attempt to shed light on the time and effort involved in programming microprocessors for control applications.

Fig 1 Pictured here is the crane used by a major aluminum manufacturer to load and unload carbon blocks from a storage area. The crane has its hoist lowered to the bottom point and its twelve grabs closed around the carbon blocks.



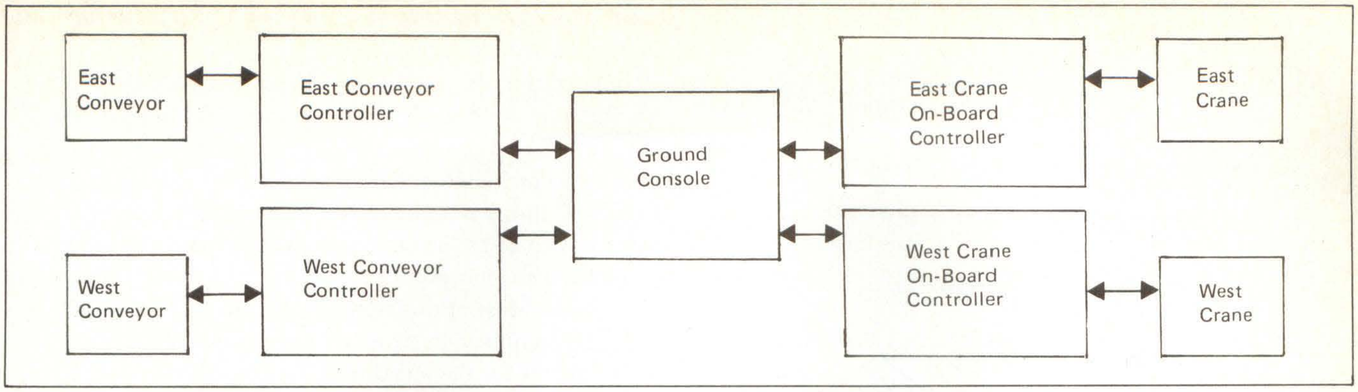


Fig 2 This block diagram shows the overall crane control system.

system overview

The system specifications are as follows. Each storage area holds 6,264 carbon blocks arranged in 87 rows of 72 blocks each. Within a row, the blocks are stored 12 across and six high. Three conveyors split each storage area into two sections – north and south. The north section contains 27 rows and the south 60 rows. The distance between the first and last rows is 306 feet. Both cranes lift twelve carbons at once with each block weighing up to 710 pounds.

Of the three floor-mounted roller conveyors that feed and drain the storage areas, only the north and south conveyors do both. The center conveyor feeds only. A conveyor controller commands each crane to either load carbon onto a conveyor from storage or to unload carbon from a conveyor into storage. Communication with the cranes occurs via wiring to the ground console which serves as a command multiplexer to the crane controllers. The ground console talks to the crane only when the crane is stationary.

Storage areas fill up either in layers or tiers. Starting from the farthest point, the crane works its way back to the conveyor either a row per command for layers or a row every six commands for tiers. When a section fills, ground console flashes a message on the CRT to alert the operator. Furthermore, on system initialization, the operator can specify any rows to be excluded from the stacking process.

Normally, the crane waits for instructions in an idle state positioned above the conveyor serviced in the last command. When an unload command issues, the crane bridges to the selected conveyor – if required. It then lowers its grab, picks up the carbon blocks and hoists them to a 10'-6" level. The bridge travels to its destination at maximum speed, slows down and stops at the proper stacking positon. The hoist then lowers the grab to the proper level and the grab opens to release the twelve carbon blocks. The hoist returns to maximum height and the crane returns to the selected conveyor.

Conversely, receipt of a load command from the ground console reverses the process and the crane brings carbon blocks from the last stacking position to the selected conveyor. The grab opens, releasing the carbon, and the hoist rises to the highest position to await the next command.

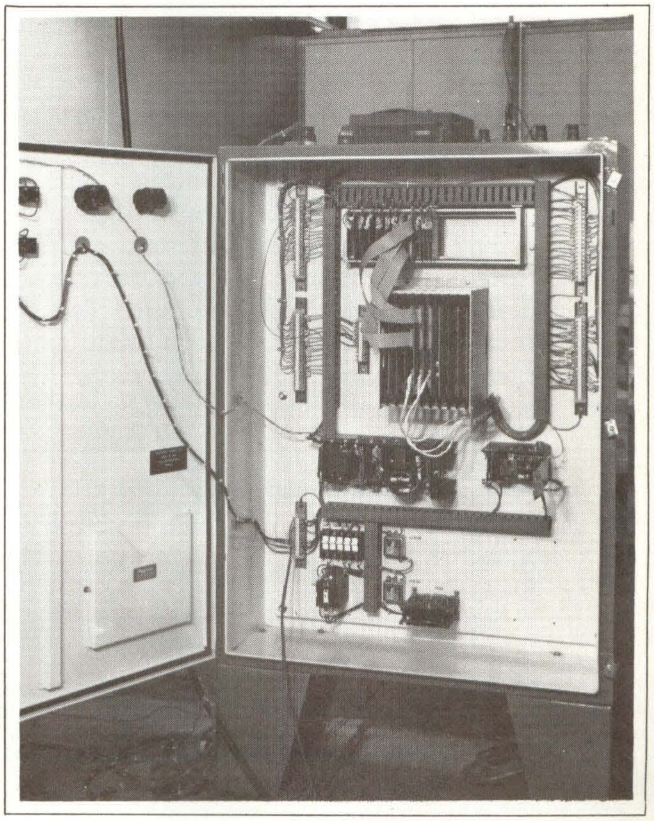
The ground console monitors crane operation and uses this information to update the operator display. The operator display includes information on the contents of each storage area (east and west) as well as associated sections (north and south). Any faults in either the GC or the OB are reported on the display. In addition, the ground console regularly transmits crane status to the conveyor controller.

ground console

The ground console serves as a command multiplexer between the conveyors and the cranes. It accepts commands from the conveyors' controller and updates them as to crane status. Further, it delivers commands to the cranes as well as requesting and accepting each crane's status. The ground console must also support two-way communications with a CRT terminal which provides an interface for the operator.

The GC program treats both cranes equally. After each pass through the main loop, a turnaround routine forces the program to use variables for the other crane in its next pass. Two 120-byte read/write memory sections

Fig 3 The ground console is shown here with its front panel swung open. This station will sit in the air conditioned room in the aluminum manufacturer's facility.



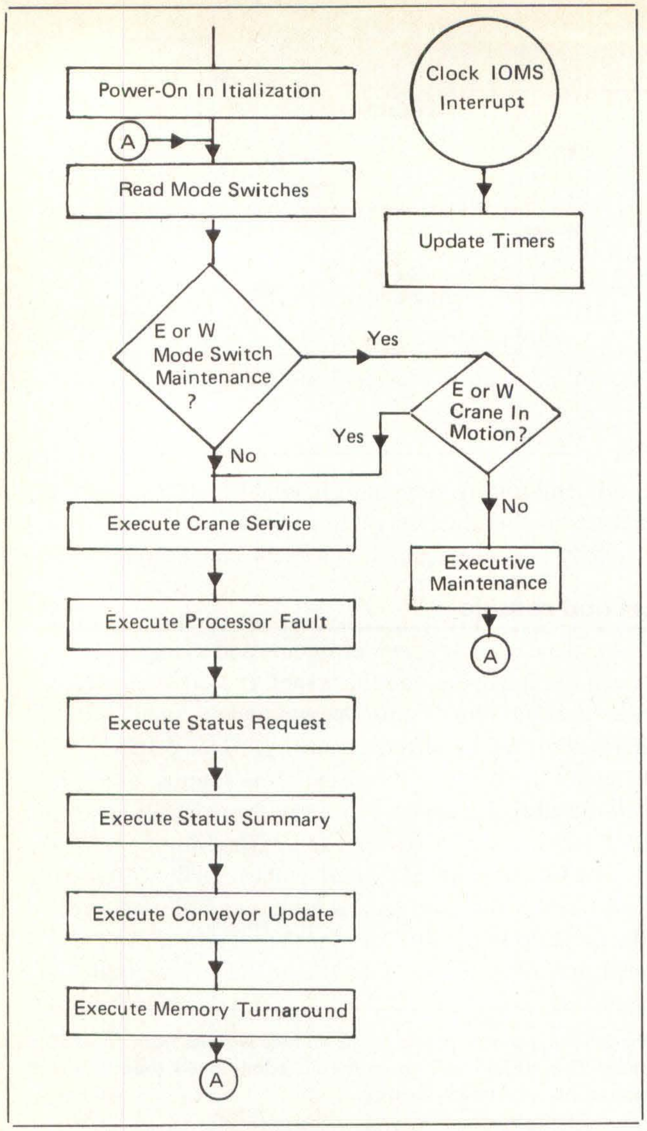


Fig 4 This flow chart shows the operation of the ground console program.

house the variable data for each crane and a third 120-byte workspace section is loaded alternately from the other crane during each execution of the turnaround routine.

The ground console program operates in two modes: maintenance and normal. During the maintenance mode, the operator enters stack limits and exclusions, start stacking positions and stacking method (layers or tiers). To enter the maintenance mode, both manual switches on the front panel of the ground console station must be positioned in the maintenance state.

In normal mode, the GC first executes crane service. This routine waits for a single character transmission from the OB controller. This character indicates the present activity of the OB controller; either idle and ready, waiting to send status, executing a command or faulty. All exits from crane service go to the fault processor routine – even for no faults. The fault processor routine occupies 2106 bytes of memory. Most of this storage is for text; 75 message segments combined in twos and threes form 68 possible fault displays for the operator.

After processing faults, the ground console program enters the status request routine. Here, the GC obtains the crane's status and displays it on the CRT, if requested. Then, the summary status routine updates the bottom line of the CRT which maintains by section a running tally of the contents of east and west storage areas. This bottom line on the CRT also posts the operation being performed by each crane.

Finally, the GC updates the conveyor controller as to the crane's status and then executes memory turnaround to service the alternate storage area. The GC program, also stored in PROM, requires 10.8K bytes of memory.

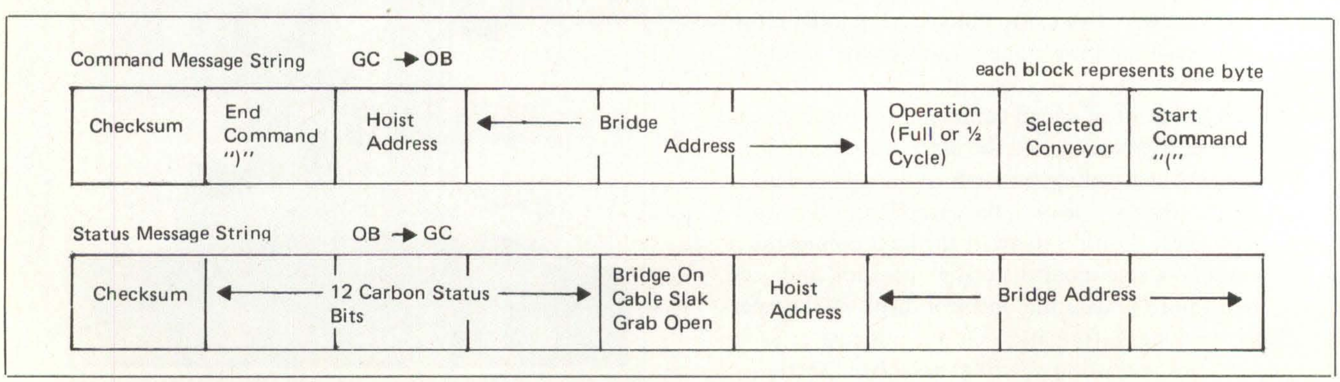
When the GC sends commands to the OB controller, it informs the crane of its bridge and hoist destination and the selected conveyor. It also commands either full or half cycle sequences. For half cycle sequences, the crane either picks up or deposits carbon blocks. It does not perform an entire load or unload operation. These half cycle commands are operator initiated and serve manual fault recovery.

On the other hand, when the OB transmits the crane's status to the GC, it informs the GC of its present hoist and bridge address, the condition of the bridge, cable and grab and the status of the twelve carbon blocks within the grab. Thus the GC keeps itself up to date on the crane's activities.

on-board controller

The on-board controller manages the movements of its associated crane. It accepts as input bridge and hoist positions and sensor readings for cable state (slack or taut). In turn the OB outputs speed and direction signals to the crane's motors. The bridge moves at four speeds – creep, slow, medium and full – and the hoist at three speeds, creep, slow and full. Further, the OB issues commands to open and close the grab.

Fig 5 These message strings command the crane and provide crane status.



Once commanded by the GC, the crane performs tasks on its own. After determining both destination and task, the crane executes the task, stops and waits for another command from GC. The GC communicates with the OB in either single characters or message strings.

The two message strings shown in Figure 5 command the crane and provide crane status.

The OB controller program requires 3.8K bytes of memory. Control Logic chose to implement this on PROM. In addition, the program uses 93 bytes of read/write memory for variables and workspace. After power-on initialization, where the program initializes pointers and checks out memory and clocks, the program enters the main loop called the idle loop. Once in the idle loop, the program scans all status bits for any faults. If any errors prevail, the program enters the fault processing loop and reports the fault type to the GC. If no faults exist, the crane controller searches for a status request or a new command from the GC.

Both the OB controller and the GC contain a clock interrupt routine. Every ten milliseconds, the interrupt causes all the status bits to be updated as well as all the critical timers for system operation. Figure 6 shows a flow chart of the OB controller program. According to Knowlton, about half the program or 1703 bytes are used by the crane to perform its tasks. The other half handles GC communications, faults, initialization and clock updates.

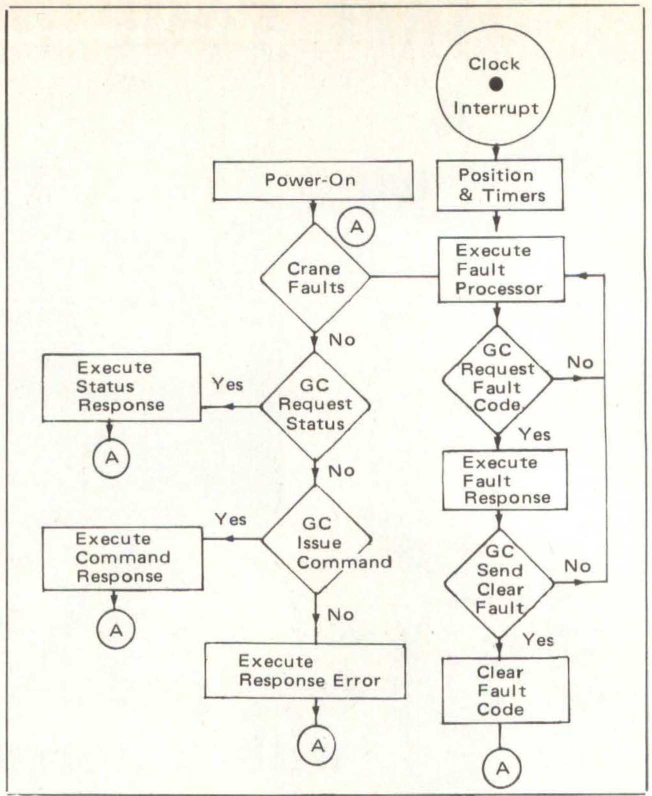


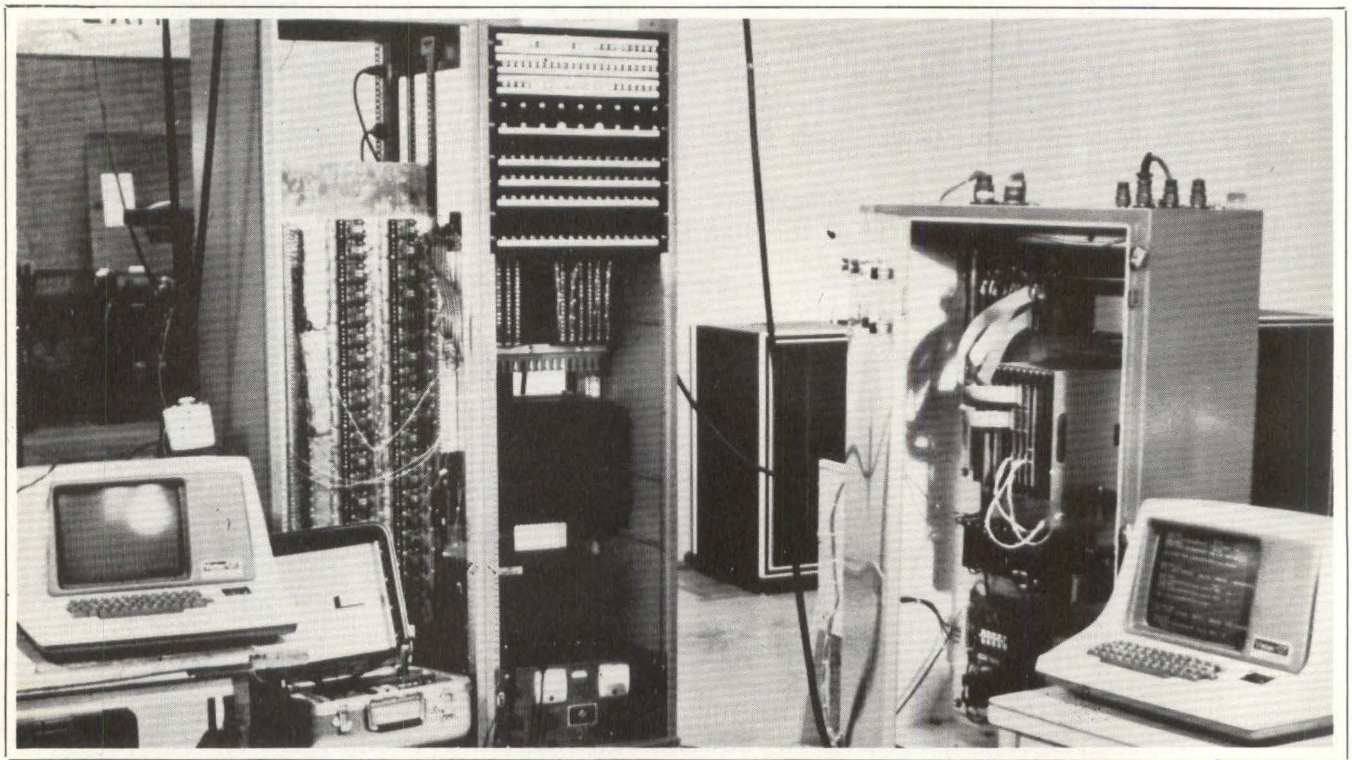
Fig 6 This flow chart shows how the OB controller program operates.

program development

Knowlton spent 26 weeks developing the software for this system. He went through four phases to complete the project – program organization, flow chart, coding, and debug. In the first five weeks, he produced the program organization document. Here, the tasks to be performed by each 8080 were written down in plain language following an outline format. In total, Knowlton's program organization document required 29 typewritten pages. He used the specifications set down by the negotiating team as input.

The next phase, flow chart, took eight weeks to complete. Here Knowlton developed pages and pages of sequences and branches in an effort to link together all the concep-

Fig 7 Pictured below from left to right are the CRT used to debug the OB controller, the crane simulator, the ground console and the ground console's CRT.



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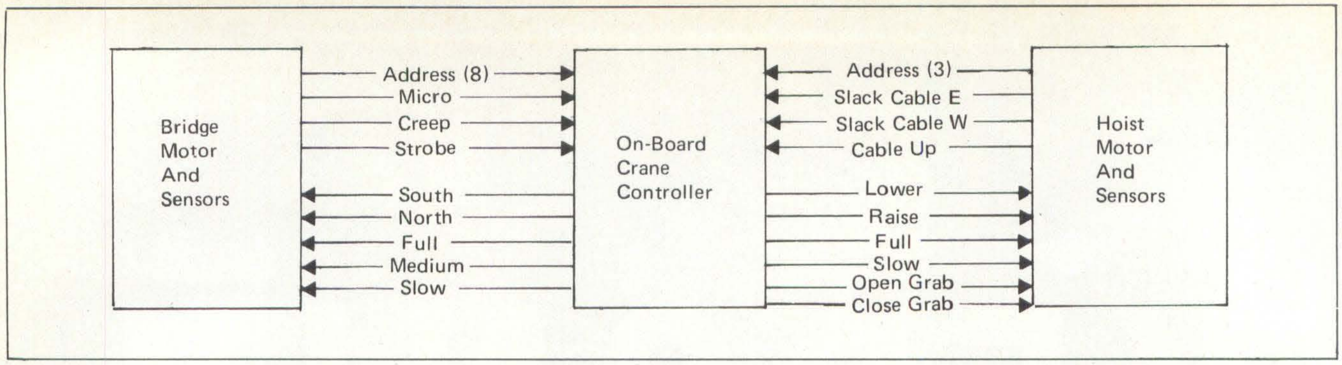

Fig 8 This diagram show signal flow for OB bridge, hoist.

tual tasks set down in the program organization document. Status and control bits were assigned abbreviated symbols and placed in flow chart format. The GC program alone required 46 pages of flow chart information.

After the flow chart, Knowlton dived into coding. Converting the flow charts into 8080 mnemonics took five weeks. According to Knowlton, portions of the program were coded directly from the program organization document, skipping the flow chart phase all together. As a result, time requirements for these two phases may vary slightly from those quoted.

The last phase, debug, went for eight weeks. Knowlton encountered no major problems during this stage and believed the program fairly strong after six weeks. He used the remaining two weeks to develop a maintenance routine which outputs a time chart of the input and output signals between the OB controller and the bridge and hoist. At 160 millisecond intervals, the status of each crane I/O bit is stored. Then for every active bit (high) the printer outputs a "SPACE" and then an "I". For each inactive bit (low) the printer outputs an "I" and then the SPACE". After a given time limit, the printer paper is removed from the unit, rotated 90 degrees and each "I" connected with a pencil to create a time chart.

For the coding phase, Knowlton used a Control Logic MM1 microcomputer development system. The OB controller, connected to a factory tester to simulate actual crane responses, was debugged first. A CRT played the part of the GC. For GC debug, he used the true ground console with CRT, both OB controllers connected to the simulator and a black box for the conveyor controller with switches for output signals and lights for input signals.

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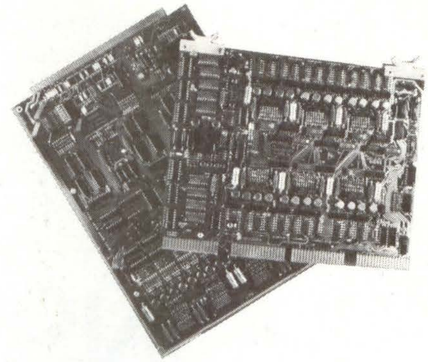

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- D SERIES . FULLY COMPATIBLE WITH PDP-11™ s
- J-1 SERIES . . . FULLY COMPATIBLE WITH MICRODATA™ 800 AND CIP™ 2000
- J-2 SERIES . . . FULLY COMPATIBLE WITH MICRODATA™ 1600
- G SERIES . . . FULLY COMPATIBLE WITH PRIME™ 100, 200, & 300
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IN ADDITION TO THE ABOVE, KERONIX MANUFACTURES ADD-ON MEMORIES, OEM MEMORIES, AND CUSTOM MEMORIES

ONE-YEAR WARRANTY WITH ALL KERONIX MEMORIES

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WE HAVE REPRESENTATIVES AND DISTRIBUTORS WORLDWIDE

George Foldvary

250 E. Emerson St. • Orange, California 92662 • (714) 974-0800

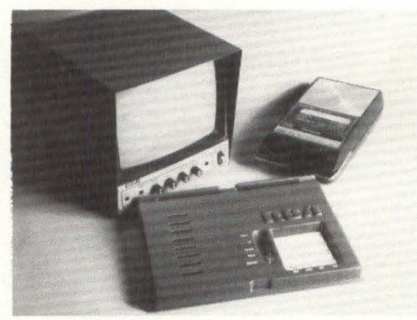
TWX 910-593-1344

FIELD-PROGRAMMABLE LOGIC ARRAYS AVAILABLE

Two Schottky TTL field programmable logic arrays (FPLA) provide new dimensions in logic design, coupling innovative control options with increased cost effectiveness to produce a practical LSI alternative for random logic designs. Designated the SN54S/74S330 and SN54S/74S331, these FPLAs have a built-in capability for multidimensional expansion of their basic 12 input X 50 product term X 6 output organization. A special circuit can decode true product terms to automatically enable the FPLA outputs. The S330/S331 can be programmed to stand alone; that is, the outputs are constantly enabled when system power is applied. Time consuming reduction of complicated Boolean functions can be eliminated or reduced significantly by directly writing compound/multiple gating functions into the S330/S331. Virtually any combination of AND, NAND, OR, NOR logic functions can be programmed to replace random logic gates, reducing design time, PC board area, package count and soldered connections – all of which enhances system cost-effectiveness. Texas Instruments, P.O. Box 5012, Dallas, TX 75222. (713) 494-5115. **Circle 172**

EXPANDABLE HOBBY COMPUTER COMES IN A KIT

An expandable, low-cost hobbyist computer kit, called COSMAC VIP – Video Interface Processor, permits the hobbyist to assemble a microcomputer with which he or she can create and play video games, generate graphics and develop microprocessor control functions. The VIP is a computer on a printed circuit card, offering a complete operating system in 4K bits of ROM. VIP's output directly interfaces with a monochrome CRT display or



to a TV receiver through a modulator. Programs can be generated and then stored in an audio cassette tape recorder for easy retrieval and use. The VIP incorporates a single 8-1/2 x 11" PC card with the CDP1802 microprocessor, 2,048 byte RAM using 4K-bit static RAMs, single-chip graphic video display interface, built-in hexadecimal keyboard, 100-byte per second audio tape cassette interface, simple wall-plug regulated power supply, and expandability for both memory and I/O interfaces. The included hobbyist's manual contains detailed information on kit assembly, VIP operating procedures, CHIP-8 interpreter programming technique, machine language programming, logic description, test programs and trouble shooting guides and VIP system expansion instructions. Price: $275.00 in kit form. RCA Solid State Division, Box 3200, Somerville, New Jersey 08876. (201) 685-6423. **Circle 158**

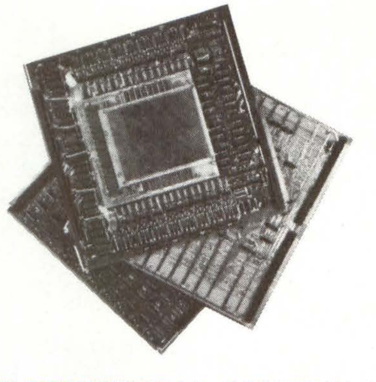
CIRCLE 55▶

A Total Systems Capability

VIDEO DISPLAY TERMINAL
KERONIX MODEL K-4000

- FULL KEYBOARD (Optional 10-Key Pad Available)
- HIGH RESOLUTION, NON-REFLECTING SCREEN; 9" X 7" (12" Diagonal); SWIVEL BASE; EASY VIEWING UP TO 10 FEET; BRIGHTNESS CONTROL; REVERSE VIDEO (Black Characters on White Background, Selectable)
- 80 CHARACTERS PER LINE, 25 LINES, 2000 CHARACTER DISPLAY; STORE UP TO 51 LINES & 4080 CHARACTERS; BLINKING CHARACTERS AT 3Hz RATE
- CURSOR CONTROL (Non-Destructive)
- INTERCHANGEABLE WITH TELETYPE USES STANDARD ASCII CODE
- INTERNAL POWER SUPPLY; RUNS OFF A SINGLE 15" X 15" P.C. BOARD
- VARIABLE BAUD RATE (75 to 9600 Bits Per Second); 10 OR 11 BIT CODE
- ODD OR EVEN OR MARK PARITY
- EITHER EIA OR 20 MA CURRENT LOOP

LOOK FOR OUR COMPLETELY INTELLIGENT



I/0 AND PERIPHERAL CONTROLLERS
FOR KERONIX IDS 16 COMPUTERS AND NOVA TM SERIES OF COMPUTERS

- 1007 I/0 BOARDS
- 1008 REAL TIME CLOCK
- 1010 TTY INTERFACE
- 1011 PAPER TAPE READER CONTROL
- 1012 PAPER TAPE PUNCH CONTROL
- 1016 CARD READER CONTROLLER
- 1023 EIA INTERFACE
- 1034 LINE PRINTER CONTROLLER
- 1038 MULTI-PROCESSOR COMMUNICATIONS ADAPTER
- 1046 DISK CONTROLLER
- 1146 FLEXIBLE DISK CONTROLLER
- 1054 EXTENDER BOARDS
- 1060-4 FOUR LINE ASYNCHRONOUS MULTIPLEXER FOR FOUR EIA STANDARD LEVEL LINES (MUX)
- 1060-8 MUX FOR EIGHT EIA STANDARD LEVEL LINES

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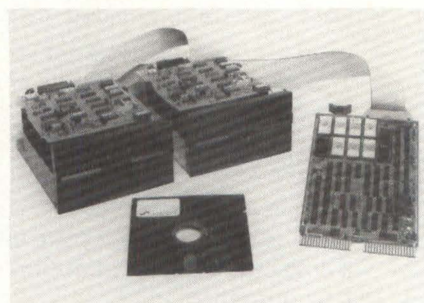
SINGLE-BOARD PE/NRZ TAPE CONTROLLER

A single-board magnetic tape controller software compatible with existing Interdata operating systems, the TC-140 is a complete dual density controller with all interface and formatting electronics for both Phase Encoding (PE) and NRZ. Fully embedded, the controller requires no separate chassis or power supply, and operates via the selector channel or multiplexer bus. The TG 140 handles up to four drives in any combination of seven-track NRZ, nine-track NRZ, nine-track PE or nine-track PE/NRZ, at any two speeds in the range of 12.5 to 125 ips. The TC-140 also includes an extended command register and an enhanced status register allowing higher level of control than previously available. Diagnostic software comes with all TC-140's. Western Peripherals, Inc., 1100 Claudina Place, Anaheim, CA 92805. (714) 991-8700. **Circle 174**

LSI-11 COMPATIBLE MINIDISK CONTROLLER

An interface board allows up to three Shugart SA-400 minidisk drives (5-1/4" format) to be controlled by an LSI-11 computer system. This multifunction controller, designated the MDC11, also provides a DMA Dynamic Memory Refresh Controller and sockets for up to 4096 sixteen bit words of EPROM. All of the functions are contained on a single dual width card that plugs directly into the LSI-11 Q-Bus and uses the standard voltages +5 & +12. The controller performs several functions automatically, including track seek and verify, 16 bit CRCC generation and checking and drive motor timeout shutoff. The EPROM section of the



MDC11 permits critical software and data to reside in a non-volatile memory, thus giving the system some 'resident' intelligence. The EPROM area will accommodate up to 4K words of 2708-type memory chips or up to 8K words of 2716-type chips. Andromeda Systems, 14701 Arminta St. #J, Panorama City, CA 91402. (213) 781-6000.
Circle 201

SERIAL PRINTER GENERATES 120 LINES/MINUTE

In the MP 580 serial printer, the mobile head with 7 printing electrodes prints characters from left to right in a dot matrix generated by the control logic. The non-impact recorder prints the characters on metallized, electrosensitive paper. Input and output are TTL/CMOS compatible, and the printer accepts 6 bit parallel column serial in ASCII code. The MP 580 generates 2 lines per second on paper isolated from the input; the printer has the capability for 63 ASCII characters. Available in 19" rack mount version, in a case or as an OEM version from Gertsch and Brutsch Ag, CH-8304 Wallisellen, Hertistrasse 25, Switzerland. Telefon 01 830 12 55.

DOUBLE-SIZE CHARACTERS SEEN ON CRT TERMINAL

Model 400D Terminals now come with a double-size character option for applications where readability at greater distances is desired. The terminal's refresh memory stores 2000 characters in a 50 line by 40 character format. Twelve lines show on the monitor at one time, with the remaining 38 lines

accessible in either Roll or Scroll modes. On a 15-inch monitor, the characters are approximately one-half inch high. Standard character accents include blink, dim and reverse-video. The cursor appears as a blinking field. An RS232 data interface and RS170 video output for driving auxiliary monitors come as standard equipment. The desktop version incorporates a 15-inch nonglare screen; the KSR-version has a detachable 72-key keyboard, including cursor control keys, TTY lock, and a separate numeric pad. The user can select baud rate (110-9600), keyboard mode (TTY or full-ASCII), I/O mode (local, full or half-duplex), and display mode (page, roll, or scroll). Ann Arbor Terminals Inc., 6107 Jackson Rd., Ann Arbor, MI 48103. (313) 769-0926.

Circle 151

COMPACT ELECTRONIC DIGITAL PRINTER

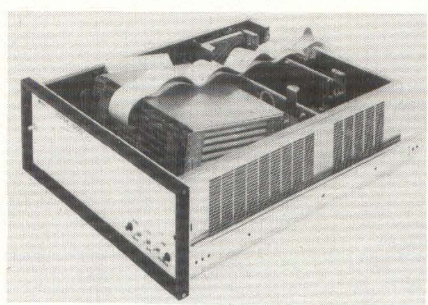
Electro-sensitive Model TCM-101B "Panaprinter" was designed for use in electronic calculators, instrumentation, cash registers and computer equipment. A low level of power consumption in the unit allows battery operation. In addition, its compact size makes it suitable for small printing electronic calculators. Design of the printer eliminates all solenoids providing silent operation. Eliminating the need for inks, ribbons or chemicals, the "Panaprinter" prints both alphanumerals and arithmetic symbols in a permanent dry process. A mechanical horizontal scanning operation of a 7-row-by-one-column head prints characters based on the 7-row-by-5-column dots matrix structure. The unit prints 20 characters per line, at a rate of 2 lines per second. The "Panaprinter" weighs 11.7 oz. and has a voltage supply of -24Vdc. Panasonic Co., One Panasonic Way, Secaucus, NJ 07094. (201) 348-7000. **Circle 203**

DESK-TOP COMPUTER

A desk-top microcomputer turnkey system, based on the MOS technology 6502 processor, incorporates a 20x64 character CRT and a full-ASCII keyboard with a numeric keypad. The system also includes a 4K RAM (expandable to 64K), 4K system monitor EROM, 16-level priority interrupt, modem and TTY interfaces. Price: $3449. Mohr Labs Inc., Madison, WI 53711. (608) 271-5380. **Circle 202**

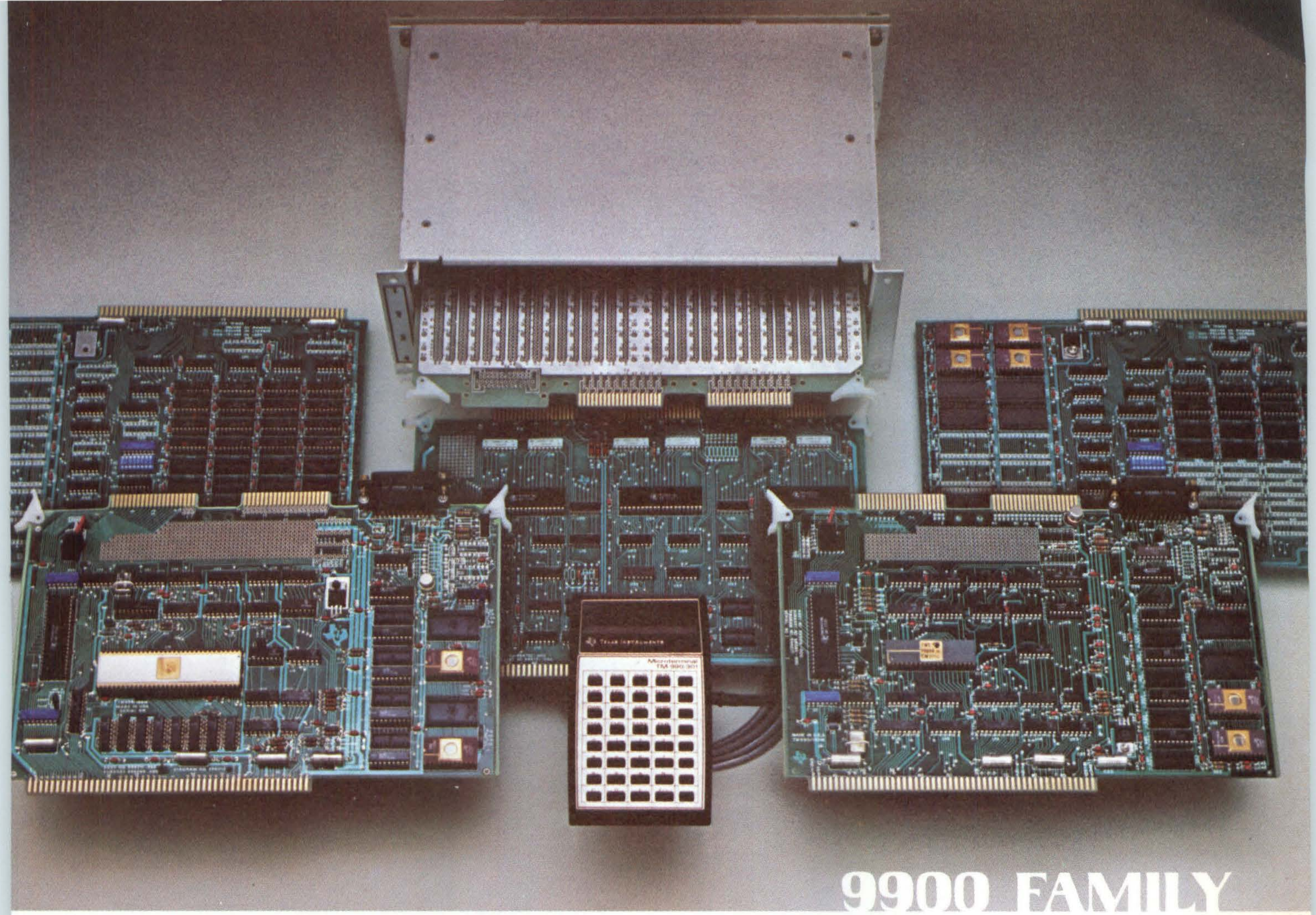
LSI-11 COMPATIBLE DATA ACQUISITION SYSTEM

The System 1000 data acquisition system for industrial and scientific applications, in the stand-alone configuration comes with a DEC LSI-11 microcomputer and a minimum of 4K of RAM memory. Up to 24K of additional memory can be supplied in both ROM and RAM. The LSI-11 can communicate with any of the ADAC library of analog I/O modules for digitizing outputs of thermocouples, strain gages, isolation amplifiers, LVDT, RTD and photomultipliers. With the digital I/O



modules, inputs from Digi-switches, shaft encoders, motor controls, and relay contacts can be sensed with outputs to printers, cassettes, lamps, relays and solenoids. The System 1000 enclosure consists of three major components, the rack drawer, card cage/backplane assembly and power supply. The card cage/backplane can accommodate up to eleven 8½"x10" or twenty-two 8½"x5" or any mixture of LSI-11 bus compatible printed circuit cards. Adac Corp., 15 Cummings Park, Woburn, MA 01801. (617) 935-6668.

Circle 144



Now–more OEM μP modules from TI: 16-bit performance at 8-bit prices.

Compare TI's series of TM 990 microcomputer modules. Here's 16-bit performance at a cost less than 8 bits.

And 16-bit performance means increased throughput. Programming ease. Improved memory efficiency. All leading to greater system savings.

Use these new modules for μP evaluation. And as a production alternative. To speed your microprocessor-based design to market. To minimize design costs.

Leadership series

Included in the TM 990 Series are:

• TM 990/100M – TI's TMS 9900 μP, I/O circuits, and memory – all on a single board. $450.00*.

• TM 990/180M – 16-bit TMS 9980 μP offers 2 MHz operation with 8-bit data bus. $435.00*.

• TM 990/201 – Memory expansion board: 8K bytes of EPROM, 4K bytes of static RAM. Expandable to 32K bytes of EPROM and 16K bytes of RAM. $595.00*.

• TM 990/206 – Memory expansion board with 8K bytes of RAM. Expandable to 16K bytes. $585.00*.

• TM 990/301 – Microterminal for data entry and display. $125.00*.

• TM 990/310 – a 48-bit input/output expansion module. $295.00*.

• TM 990/401 – Interactive debug monitor (TIBUG™) preprogrammed into CPU EPROM. $100.00*.

• TM 990/402 – Line-by-line assembler preprogrammed into the EPROM. $100.00*.

• TM 990/510 – Four-slot OEM chassis on 1″ spacing. $190.00*.

• Cables, connectors, extender and prototyping boards are also available.

And even more modules will be available soon.

All are preassembled. Pretested. Ready to go. Supported by easy-to-use software.

9900 First Family compatibility.

The TM 990 modules are also supported by the advanced AMPL™ software development system. And all are instruction-set compatible with other members of TI's 9900 First Family.

For more details, call your authorized TI distributor. Or write Texas Instruments Incorporated, P. O. Box 1443, M/S 653, Houston, Texas 77001.

*One to nine quantity

TEXAS INSTRUMENTS
INCORPORATED

93330

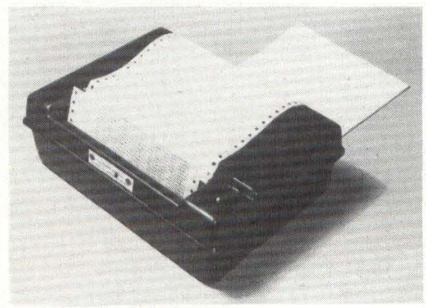
KIT AIDS FIBEROPTIC CONNECTION EVALUATION

A kit for engineering evaluation of fiberoptic interconnections offers a complete interconnect system rather than connectors only. The electro-fiberoptic system operates from DC to 5 MBPS over a temperature range of 0-55°C without drifts or inadvertent comparator switching. The complete fiberoptic kit, Part No. 698-OK-002, consists of emitter assembly, 5-meter fiberoptic cable assembly, temperature-referenced photodetector assembly, TTL-compatible preamplifier and TTL-compatible emitter driver. A second kit, Part No. 698-OK-001, comes without the preamplifier and driver for applications not requiring the electronics package. Price: Kit No. 698-OK-001 $99.50, and Kit No. 698-OK-002 $190.00. Augat Inc., 33 Perry Ave., P.O. Box 779, Attleboro, MA 02703. (617) 222-2202.

Circle 145

BLACK BOX PRINTER USES PRINT CYLINDER

The Black Box Printer, a fully assembled, 80 column, 10 character per second impact printer, uses a print cylinder (not a dot matrix) containing a 64 ASCII character set. It can make up to three copies on tractor (or pressure) fed 8½" wide paper. Shipped ready to connect to (almost) any microprocessor parallel port, the printer has a parallel



interface requiring 7 data bits, a ready and a strobe. Documentation supplied with the printer includes trouble shooting guides, installation and maintenance instructions, printer and interface schematics, plus instructions on how to wire up to the I-O parallel port. The Black Box Printer measures 4.5"H, 13"W, & 10"D, and weighs 11 lbs. Expandor Inc., 612 Beatty Rd., Monroeville, PA 15146. (412) 373-0300.

Circle 147

DISK CARRYING CASE MAGNETICALLY SHIELDED

Magnetically shielded floppy disk preservers protect your flexible disks from magnetic degradation, erasure or physical damage and also protect 9" diameter tape reels. Cases, designed for storage, shipment and hand carrying, come in a wide choice of models and capacities for standard reels, disks, disk packs and standard cassettes. Perfection Mica Co., 740 North Thomas Dr., Bensenville, IL 60106. (312) 766-7800.

Circle 169

/ability.

It Comes Naturally With The Altair™ 8800b

The Altair 8800b from MITS: the second generation design of the microcomputer that started it all. The mainframe that has the abilities everyone is demanding from microcomputers today:

Expand-ability:

The Altair 8800b power supply and one-piece, 18-slot motherboard allow efficient and easy expandability for memory and I/O options. All Altair PC boards are designed to give you maximum capability/lowest power usage possible per board. This means that for each slot used you get more features and require less power, than with any of the "off-brand" Altair-bus-compatible boards.

Whether you buy an entire system up front or choose to expand gradually, it's easy to get the configuration you need with the complete family of Altair peripheral equipment, including floppy disk, line printer, audio cassette record interface, A/D converter, PROM programmer, serial and parallel I/O boards, choice of four different memory boards and many others.

Reli-ability:

The unique design features of the Altair 8800b, which have set the standard for the microcomputer industry, make it the most reliable unit of its kind. The Altair 100-pin bus, the now-standard design used by many imitators, has been "standard" all along at MITS. The unique Front Panel Interface Board on the Altair 8800b isolates and filters front panel noise before it can be transmitted to the bus. The all-new CPU board utilizes the 8080A microprocessor, Intel 8224 clock generator and 8216 bus drivers.

Flex-ability:

Meeting the diversified demands of an ever-increasing microprocessor market requires flexibility: not just hardware flexibility but software flexibility as well. MITS software, including the innovative Altair BASIC language, allows the full potential of the Altair 8800b computer to be realized.

8K ALTAIR BASIC has facilities for variable length strings with LEFT$, RIGHT$, and MID$ functions, a concatenation operator, and VAL AND STR$ functions to convert between strings and numbers.

Extended ALTAIR BASIC allows integer, single and double precision variables, automatic line numbering and renumbering, user-defined string functions, PRINT USING for formatted output and a powerful EDIT command for editing program files during or after entry. Extended statements and commands include IF . . . THEN . . . ELSE, LIST and DELETE program lines, SWAP variables and Trace On and Off for debugging.

Disk ALTAIR BASIC has all the features of Extended BASIC with the additional capability to maintain sequential and random access disk files. Utilities are provided for formatting disks and printing directories.

In all versions of ALTAIR BASIC you get the ease and efficiency of BASIC for the solution of real world problems.

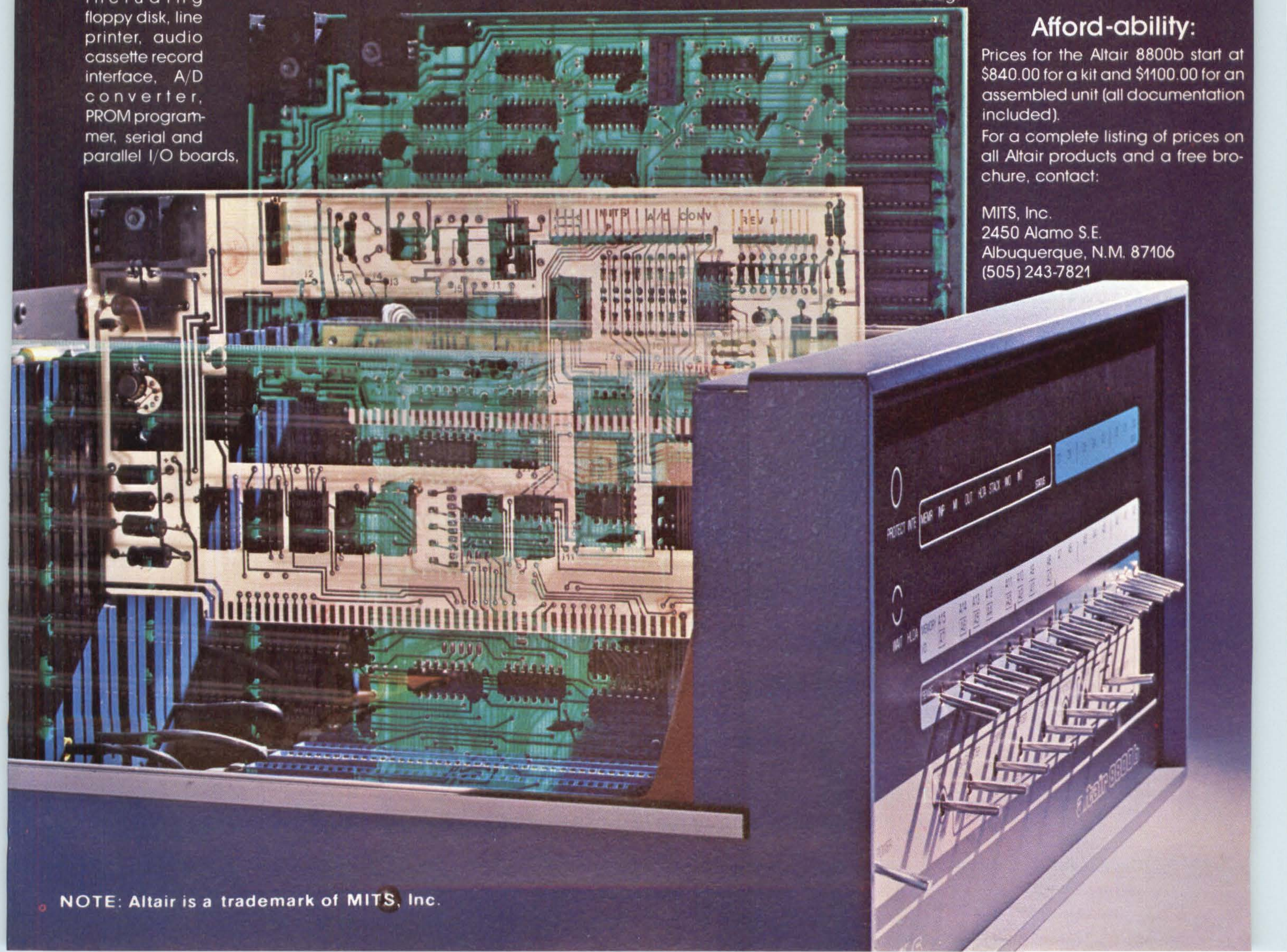
Package II, an assembly language development system for the Altair 8800b, includes system monitor, text editor, assembler and debug.

Afford-ability:

Prices for the Altair 8800b start at $840.00 for a kit and $1100.00 for an assembled unit (all documentation included).

For a complete listing of prices on all Altair products and a free brochure, contact:

MITS, Inc.
2450 Alamo S.E.
Albuquerque, N.M. 87106
(505) 243-7821



We're Moving Up

As of October 24, 1977, Benwill Publishing's Headquarters and Editorial Offices move from the 1st floor at 167 Corey Rd. to the 2nd floor at 1050 Commonwealth Ave., Boston, MA 02215.

Moving to 1050 Commonwealth not only raises our sights, it also triples our work space. Thus expanded and uplifted, we hope to serve you better. Call us. Come up to visit. Our phone number stays the same: (617) 232-5470.

MONOLITHIC 8-BIT DAC SETTLES IN 85 ns

Model DAC-08BC DAC comes in a 16 pin plastic DIP and operates over the 0°C to 70°C temperature range; model DAC-08BM DAC, packaged in a 16 pin ceramic DIP, operates over the -55°C to +125°C military temperature range. The DAC-08 consists of 8 fast switching current sources, a diffused R-2R ladder network, a bias circuit and a reference control amplifier. An external reference current programs the scale factor for the DAC-08. This current can be varied resulting in one or two quadrant multiplying operations. Output current has a high voltage compliance of -10 to +18 volts, allowing direct current to voltage conversion with just an output resistor. Power supply requirement: +4.5V to +18V at 3.8 mA and -4.5V to -18V at 7.8 mA. The DAC-08 interfaces directly to a variety of logic families such as TTL, DTL, CMOS and HNIL. Datel Systems, 1020 Turnpike St., Canton, MA 02021. (617) 828-8000. **Circle 166**

EPROM PROGRAMMER WITH HEX DISPLAY

Model 7608, a low cost, self-contained programmer for type 2704 & 2708 EPROMs, has program entry via panel keyboard and true hexadecimal display of addresses and data. Model 7608 may also be used to copy master EPROMs and to read preprogrammed EPROMs, and an accessory emulator unit permits loading from an external keyboard or computer. Type 2716, 2K x 8 EPROMs may be programmed in two passes using the optional adapter board. Extensive editing capabilities in Model 7608 allow insertion and deletion of data with resequencing prior to programming. Provision for operating the internal memory on battery backup is included. SMR Electronics, 3 Haven Rd., Medfield, MA 02052. (617) 359-4043. **Circle 204**

EIA INTERFACE MONITOR AND BREAKOUT PANEL

A pocket-size rechargeable version of the Model 60 EIA Interface Monitor and Breakout Panel uses two long-life size AA rechargeable Nickel-Cadmium batteries that allow the unit to operate directly from 110Vac while charging the batteries. Model 60 provides access to all 25 conductors of the EIA RS232 interface; twelve LED's monitor twelve key signals and two LED's sense whether signals meet EIA specs. Twenty-four switches with test points on each side allow all interface conductors except frame ground to be individually interrupted permitting isolated testing and observation of terminal and modem signals. The Model 60 weighs 13 oz including batteries and measures 3-3/4" W x 5" H x 1-3/4"D. International Data Sciences, Inc., 100 Nashua St., Providence, RI 02904. (401) 274-5100. **Circle 177**

PAGE PRINTER FORMS 100 CPS FROM CRT

This solid state thermal CRT Page Printer can print full 1920-character screens from any CRT terminal in less than 20 seconds using only one moving part. The fully buffered, microprocessor-controlled Model 650 accepts data as fast as it can be transferred from any CRT having the RS232 interface. Normal interactive CRT dialogues can continue while printing the previous screen. The terminal prints noiselessly at 100 cps on a standard size sheet of paper, in a 24-line by 80-column format using a full 96-character ASCII set. The 9 by 12 dot matrix format provides for descenders on lower case characters. Printing heads, fixed in position, consist of thick film thermal dot arrays. The printer has switch-selectable baud rates up to 9600. It measures 4" x 12" x 12" and weighs 15 pounds. Perkin-Elmer Data Systems, Rte. 10 and Emery Ave., Randolph, NJ 07801. (201) 366-5550. **Circle 168**

40 COLUMN INTELLIGENT DOT MATRIX PRINTER

Model SP-302 5 x 7 impact dot matrix 40 column intelligent printer uses a microprocessor controller to perform such functions as double width printing and double and triple spacing. Inputs include RS-232; a 20mA current loop as standard and a rear panel EIA connector that handles RS-232 'busy' signals; and TTL 'on-line' signals. Internally programmable jumpers allow selectable print intensity. Input baud rate of 110 is standard; other input rates can be internally set. The unit prints at 50 cps with multiple copy capability. Syntest, 169 Millham St., Marlboro, MA 01752. (617) 481-7827. **Circle 176**

Mini/Micro77

THE MINICOMPUTER/MICROCOMPUTER CONFERENCE AND EXPOSITION

DECEMBER 6–7–8 • CONVENTION CENTER • ANAHEIM, CALIFORNIA

CONFERENCE SESSIONS

TUESDAY

MORNING

Small Business Systems
Organizer: Don Schnitter, Basic Four Corp.

Trends in CRT Terminals
Organizer: To be announced

AFTERNOON

Small Disk Memory Trends
Organizer: Henry T. Meyer, CalComp

Buyer Be Aware: How Reliable and Flexible will Future Systems Be?
Organizer: Edward J. Bride, The Conference Co.

Low Cost Microcomputers in Business Applications
Organizer: Adam Osborne, Osborne & Assoc.

WEDNESDAY

Trends in Printer Development
Organizer: Neil Kleinman, International Data Corp.

Intelligent Applications of Minis in the Small Business Environment
Organizer: John Kirkley, Datamation Magazine

Criteria Used in Selecting & Evaluating a Minicomputer
Organizer: Joe Baker, Robert W. Baird Co.

How to Keep an On-Line System from Crashing
Organizer: Neil Kelley, Infosystems Magazine

Application of Microcomputers to Military Avionics
Organizer: Joe Genna, Delco Electronics

Trends in Mini/Micro Software
Organizer: Joe DeVita, Computer Automation

THURSDAY

OEM Peripherals in End-User Systems: The Current View
Organizer: George King, Benwill Pub. Co.

Distributed Data Processing
Organizer: Roger Billings, Billings Computer

Getting Into the Microcomputer Business
Organizer: Robert S. Jones, Interface Age Mag.

Computer Law
Organizer: Richard L. Bernocchi, Irell & Manella

Transaction Processing with Networks
Organizer: Elton Sherman, General Automation

NOTES:
1. **Morning Session – 9:30 - 12:00 noon**
   Afternoon Session – 1:30 - 4:00 p.m.
2. **All Sessions will be held in the Anaheim Convention Center**
3. **Monday, December 5 is IEEE Career Day. Contact: Vincent J. Giardina (201) 981-0060**

LIST OF EXHIBITORS (as of October 1)

E & L Instruments
MuPRO
Micro Computer Systems
Optical Electornics
AMPEX
Data I/O
Applied Computer Systems
Okidata
Artec Electronics Corp.
Qantex
Cahners Publishers
Telefile Computer Products
American Microsystems
Newman Computer Exchange
Computer Magazine (IEEE)
Monolithic Systems Corp.
Electronic Representatives Assoc.
Anderson Jacobson
Digital Systems
Logical Services
Computerworld
Micro Communications
Publishers for Conventions
Alpha Data
Shugart Assoc.
Sola Electric
Matrix Publishers
Wyle Distribution Group/ Liberty Elmar (Intel, Motorola, Fairchild, Signetics, Standard Power, Allen Bradley, Corning, Sprague, ITT Cannon)
Biomation Corp
Sord Computer Systems
Dataflux Corp.
Hughes Aircraft Co.
Pro-Log Corp
Zilog
Digital Equipment Corp.
Mini Micro Systems
Teletype Corp
Applied Digital Data (ADDS)
Printronix
MDB Systems
Systems Furniture
Data Systems Design
Basic/Four Corp.
Ball Brothers Research Corp.
Lear Siegler Inc./EID
Minicomputer Accessories
Ex-Cell-O Corp/Remex Div.
Sybex, Inc.
Memorex
Avnet Electronics
Terminal Rentals
Interdyne
Intermec
Intel Corp
Addmaster Corp
Megatek Corp
The Digital Group
Infosystems Magazine
Calex
Parsons Mfg. Corp.
Ai Electronics Corp.
Triple I
Hamilton Electro Sales (Motorola, National, Intel, Burr-Brown, Shugart Assoc., Ryan-McFarland)
General Robotics Corp.
Computer Automation
Tally Corp.
EECO
First Data Corp.
Calcomp
Microdata Corp.
Electronic Memories & Magnetics (EM&M)
Wangco
Applied Data Communications
Tandberg Data
PCC Pertec
Datamation
Computer Roomers
Computer Decisions
Interface Magazine
Elmatex International
Raymond Engineering
Trimm Enclosure Prod.
Pfystar Microcomputer Products
Diva
Educational Data Systems
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Computer Design
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Centronics
Cherry Electrical
Benwill Publishing Corp.
Sybex
Iasis
Cipher Data Products
Commodore Bus. Machines
International Microsystems
Texas Instruments
Pacific Telephone Co.
Newport Data Systems
Problem Solver Systems

(More companies are being added on a daily basis)

Conference Program Chairman: Dr. L.A. Lotito (Computer Automation)

Exhibits Committee Chairman: William Handel (Nigbert Corporation)

To: MINI/MICRO COMPUTER CONFERENCE AND EXPOSITION
5528 E. La Palma Avenue, Suite I, Anaheim, CA 92807, Phone: (714) 528-2400

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☐ **Exhibiting.** Please send a copy of the Exhibit Prospectus.

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ALPHA BITS

Detecting Digital Signals

Written primarily for practicing and student engineers involved in the design and development of future data-transmission systems, **Advanced Data-Transmission Systems** by A.P. Clark presents an account of the theory and techniques involved in the generation and detection of digital signals, where these are sampled prior to processing at the receiver. The book concentrates on the application of computer-like techniques to the detection of a sampled digital data signal. First studying the discrete Fourier transform and its application to the analysis of linear distortion in a sampled digital signal, the book proceeds through some theory development and accounts of principles, then presents studies of new detection processes and at the end, an analysis of various parallel systems using code-division multiplexing. 420 pages. $27.50 from Halsted Press, Division of John Wiley & Sons, 605 Third Avenue, NY 10016.

Questions Answered

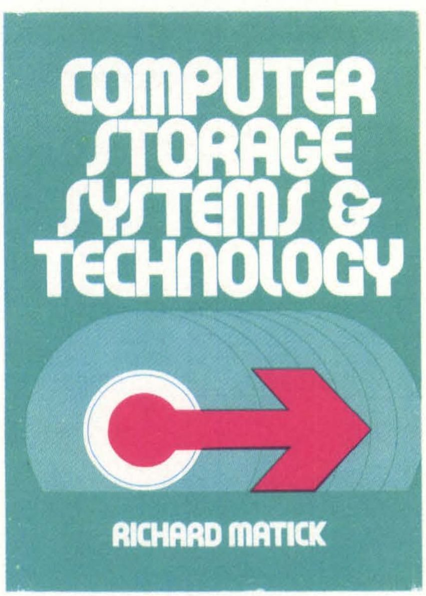
Intended for people new to computing, **Home Computers: 2^{10} Questions and Answers, Volume 1: Hardware** supplies hardware related information. Based on fictional conversations between a person who knows little about computers and a person very knowledgable about the field, author Rich Didday says the book should give people who want to buy a home computer enough of a feel for the hardware so they don't make any purchasing mistakes.

In keeping with the book's dialog format, it is organized by days: Volume 1 includes the first five days of talks and Volume 2 the next five days. As the days progress, the topics become complex.

Volume 2; Software deals exclusively with two models, the Intel 8080 and the Motorola 6800. For these, Didday's chapters cover specific microprocessors' organization, memory access instructions and stack handling; machine and assembly-language programming; basic language programming, including random number generators, arrays, and games; and generalities on programming. Volume 2 also includes a detailed index of both Volumes 1 and 2. Illustrated, Vol. 1 225 pp., $7.95 paper; Vol. 2 225 pp., $6.95 paper. dilithium Press, P.O. Box 92, Forest Grove, OR 97116.

How to Store Your Data

Describing and examining the available storage devices, their technologies and architectures, **Computer Storage Systems & Technology** gives a modern perspective for making the best decisions. Each type of storage device is examined by author Richard Matick for its speed of access, required size, relative cost, necessary organization, as well as other crucial advantages and



disadvantages. The more sophisticated topics related to memory, such as file structuring, virtual memory systems and hardware restrictions are also considered, and typical application examples are given to show how each type of memory can best be implemented and how it functions within the digital system. This 667 page book can be ordered for $29.95 from John Wiley & Sons, Inc., One Wiley Drive, Somerset, NJ 08873. (201) 479-4400.

Learn About Emulation

An introductory "how-to" book that treats microprogramming and emulation topics, **A Microprogramming Primer** by Harry Katzan, Jr., discusses complex relationships between programs, computers and modern methods of implementation. The book presents microprogramming concepts and shows how they relate to the organization of modern computer systems, then discusses the concept of emulation; a microprogramming language; and a microprogrammable computer. The author states the principles of emulation so that students can apply the concepts to the design and development of practical systems. The text uses translator and simulator systems to enable students to write programs that can be executed on any computer system with FORTRAN facilities. Hardcover, 254 pages. $17.95 from McGraw-Hill Book Company, 1221 Avenue of the Americas, New York, NY 10020. (212) 997-2485.

Shopping for Computers, Peripherals

Billing itself as "The Affordable Computer Catalog," **Byte Shopper**, created by The Phoenix Group, Inc., represents over 50 manufacturers of microcomputers, video terminals, floppy discs, I/O boards, memory systems, printers, magnetic tape and books. The catalog includes a glossary of terms for the novice computer user/buyer and begins with a basic description of microcomputers and what they can do. After explaining 4 typical microcomputer systems, **Byte Shopper** continues with descriptions of other microcomputer systems, micro training aids, display, storage and printing peripherals and software. The Phoenix Group has included an up-to-date price list and indicates in the catalog which systems or components are the best buys for hobbyists and small businesses. 41 pages in 11″ x 14½″ format, for $2.50. Order from Byte Shopper, P.O. Box 28106, Tempe, AZ 85282. (602) 894-1193.

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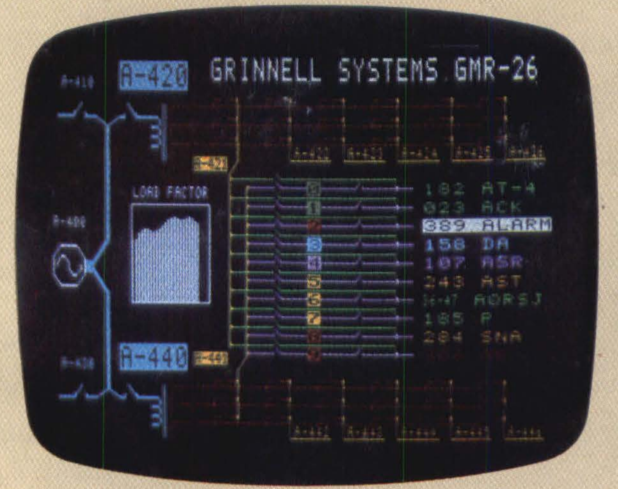

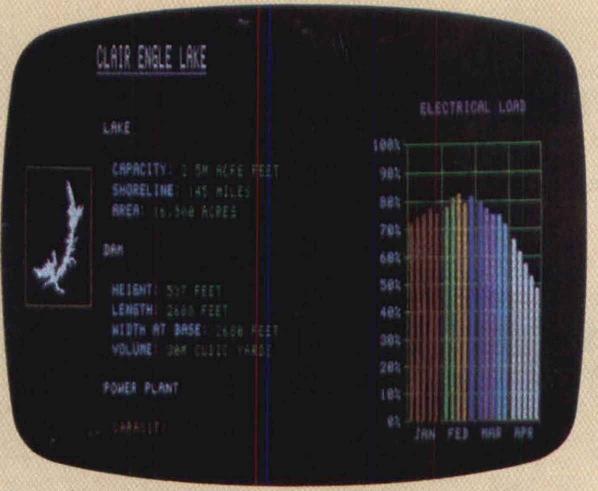

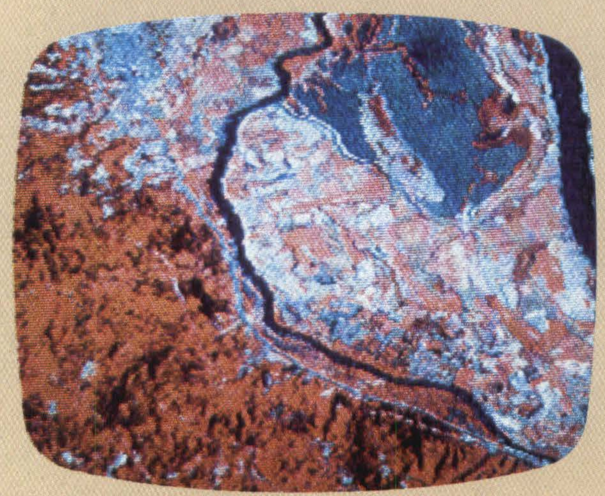

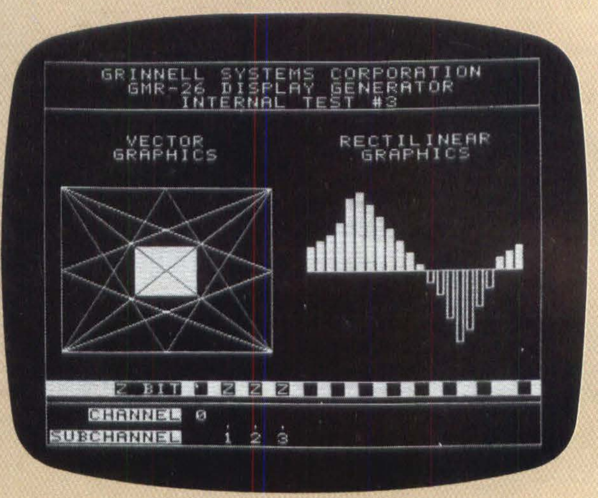

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