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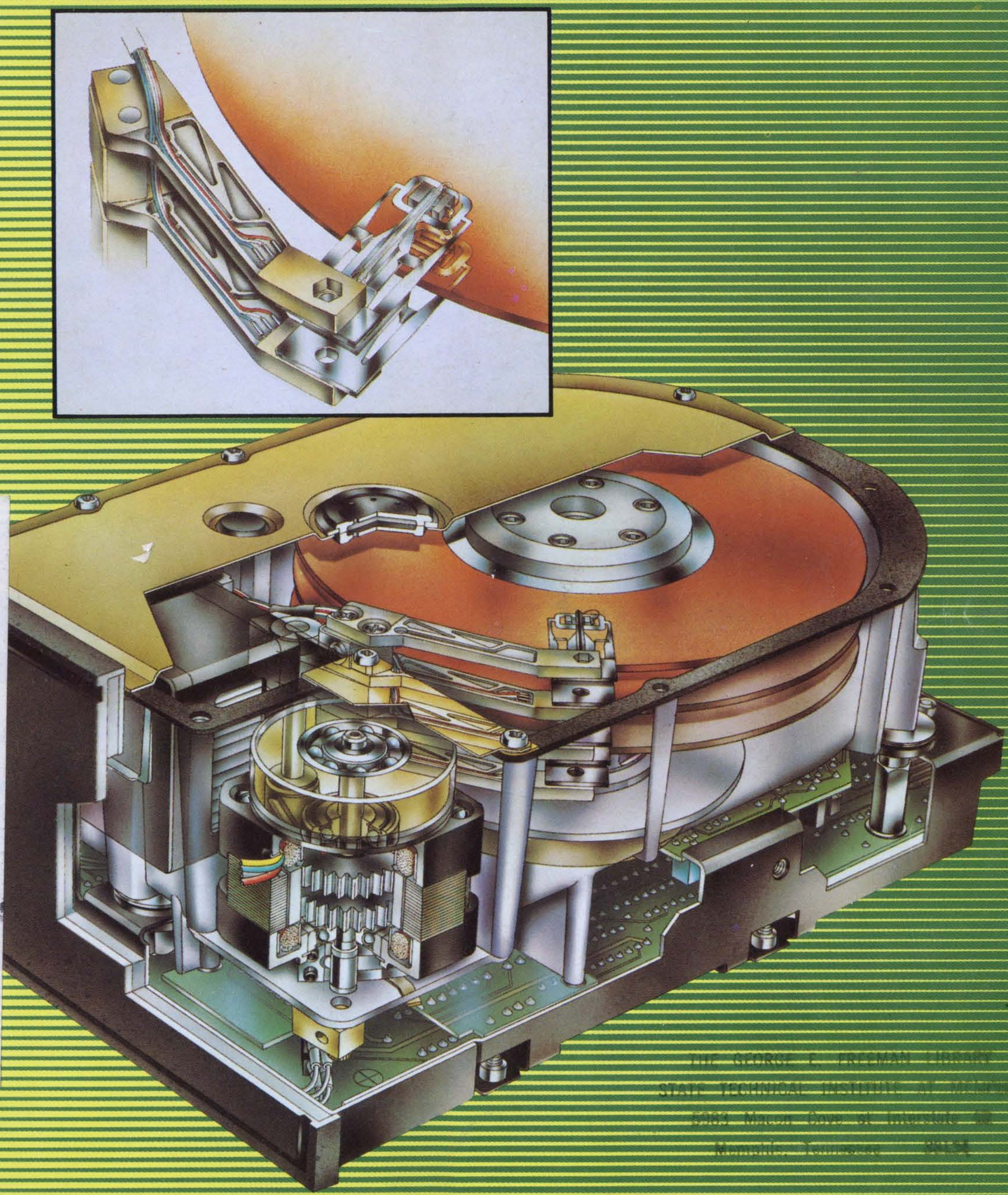
Digital Design

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 4/82



Winchesters—Buying Them And Backing Them Up

- Switchers Gain Sophistication
- GCR For Minis
- STD Bus • NSC800 • Electro '82

VOL 12
NO. 4

REACHING BEYOND

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Vincent van Gogh would have given his left ear for an AED512 graphics terminal.

To impress his young paramour, van Gogh cut off a piece of his right ear. He simply couldn't live without love. Nor could he live without the vibrant colors of his craft—which is why he'd have given his *left ear* for the powerful graphics and imaging capabilities of the AED512.

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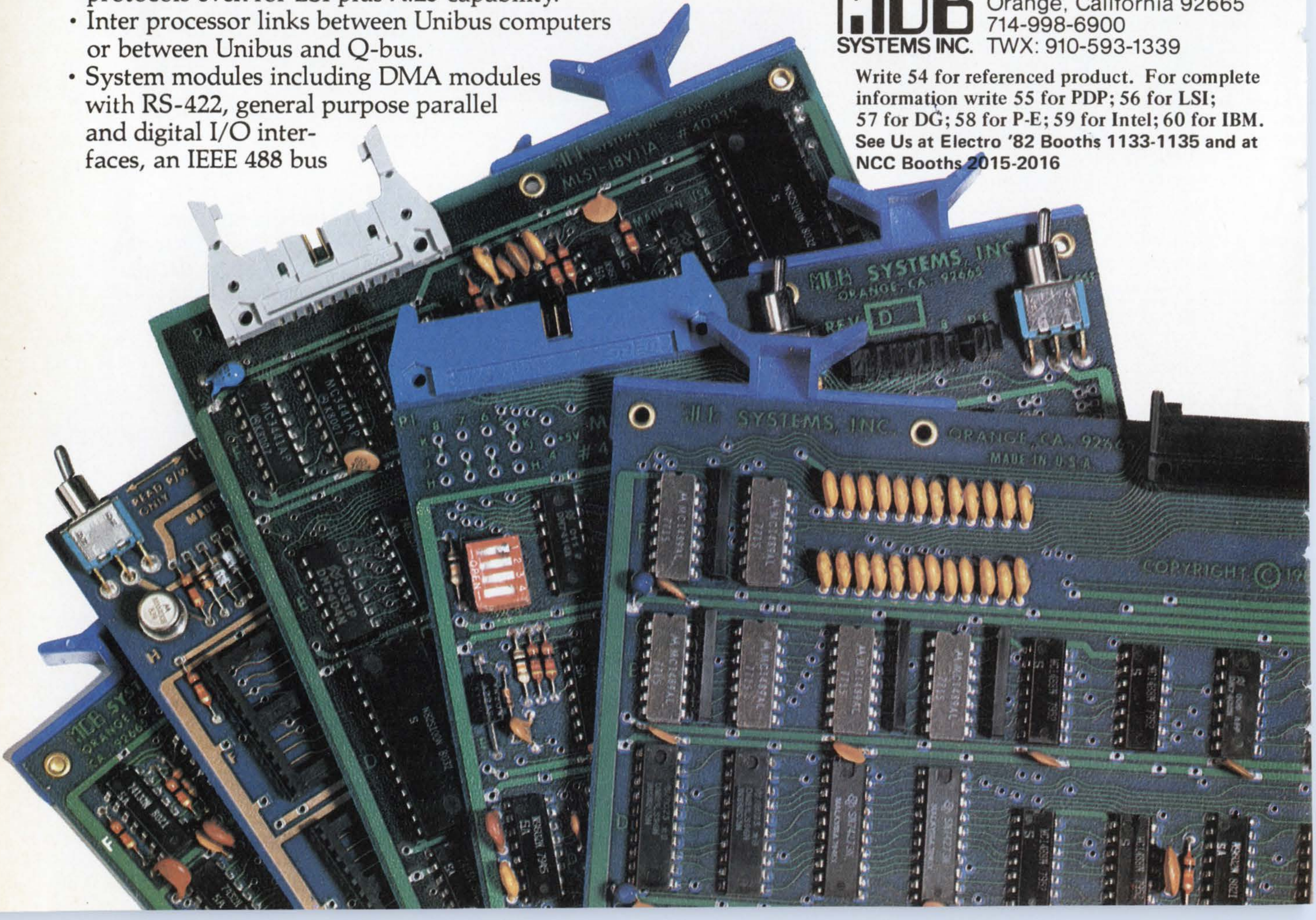
Write 54 for referenced product. For complete information write 55 for PDP; 56 for LSI; 57 for DG; 58 for P-E; 59 for Intel; 60 for IBM.
See Us at Electro '82 Booths 1133-1135 and at NCC Booths 2015-2016



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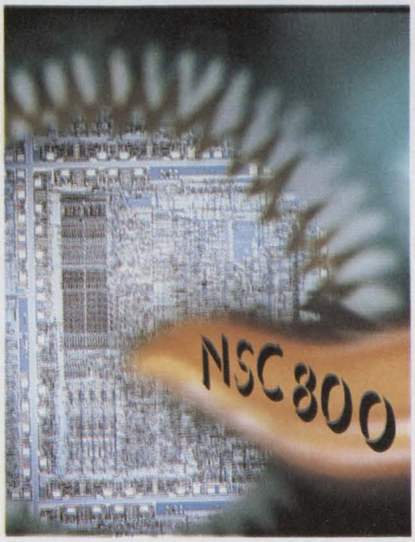

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This month's cover, submitted by Tandon, of Chatsworth, CA, takes a look inside Winchester disk drives--as does our feature material on pages 46-60.

COMPUTERS / SYSTEMS

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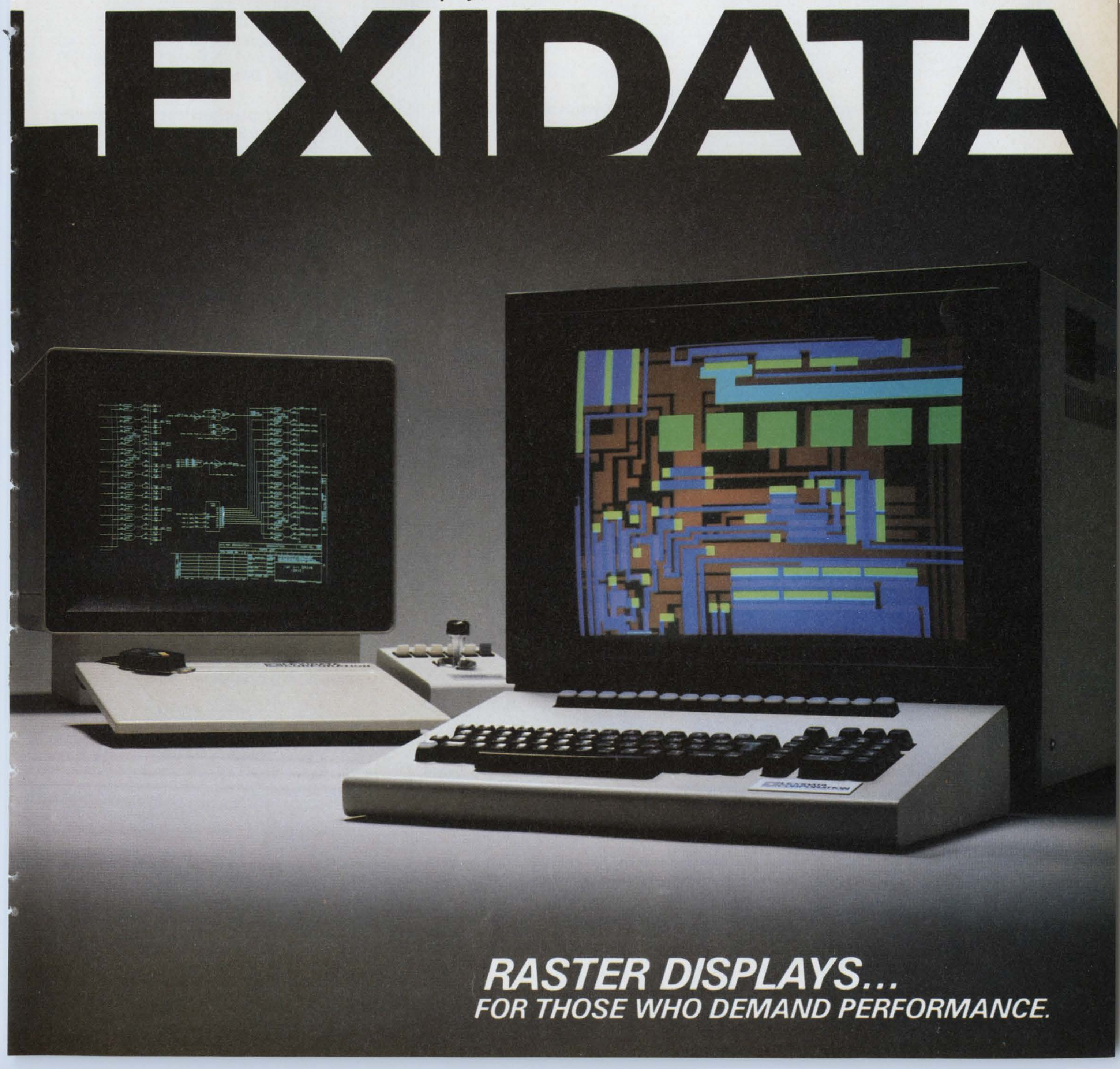

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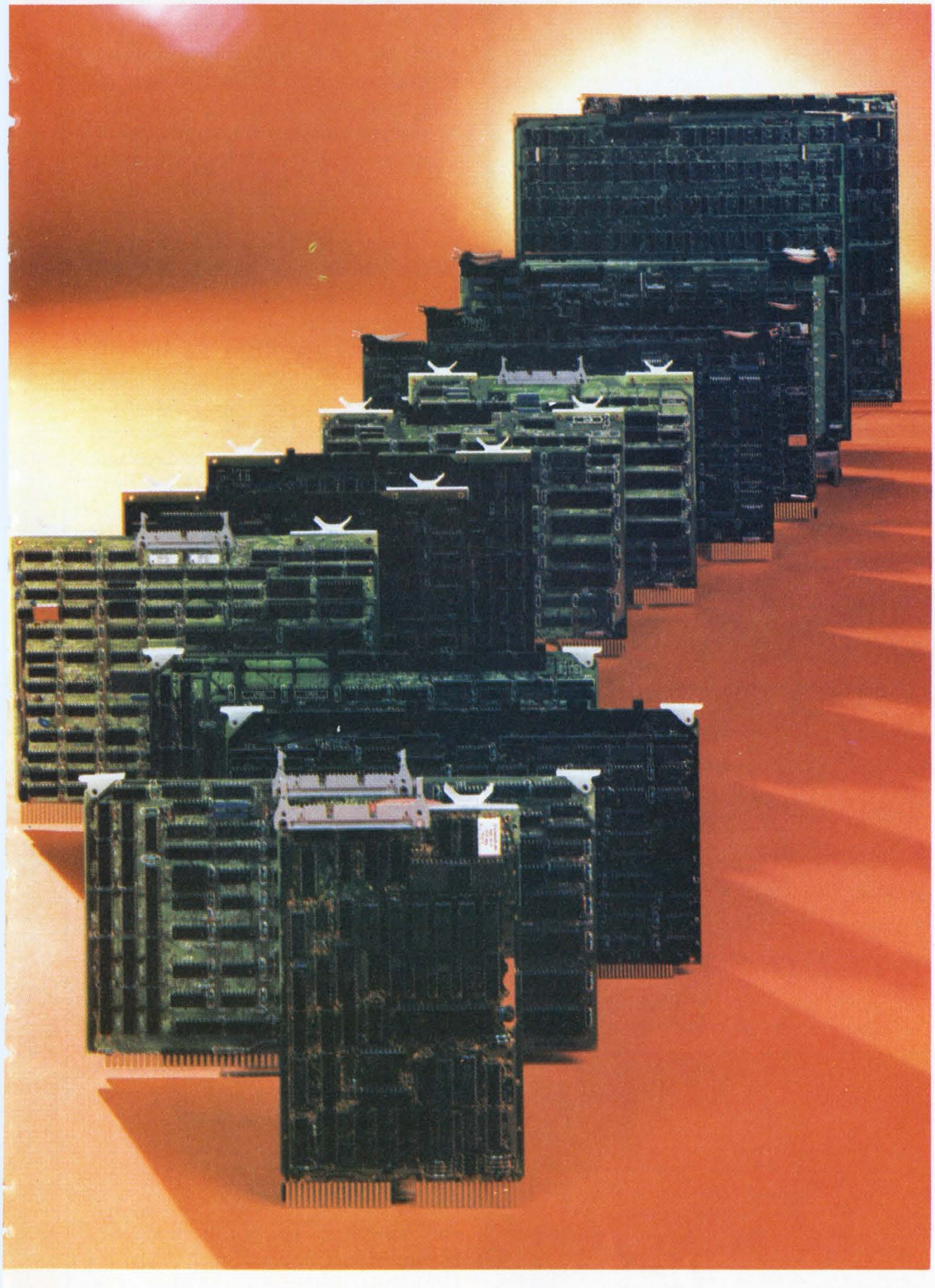

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Letters

Electrotopography Introduced

Dear Editor:

The article by you and William Sniger ("Medical Applications For System Design," P. Snigier and W. Sniger, *Digital Design*, Feb, 1982) was simply outstanding and you are both to be congratulated. It's a pleasure to read something (I read 12 hours a day) which is truly a genuine contribution.

Perhaps your readers would like to learn about some of our work that has very important potential applications in the field of diagnostic medicine and research. We have discovered and developed a new technology that we refer to as Electrotopography (ETG). It has been in the exploratory R&D phase for 14 years, there are issued US and foreign patents, and it's about to go commercial.

ETG is a new form of electrode and, among other things, it permits you to map the electrical fields that exist on the surface of the human body. The result is like a fishnet or contour map employed and developed by geologists, or like the common 3-D maps one sees these days associated with computer graphics. The mappings can be made quickly, are inexpensive (or soon will be) and are a means of doing a systems analysis on human beings.

Minas Ensanian
Lab For Robot
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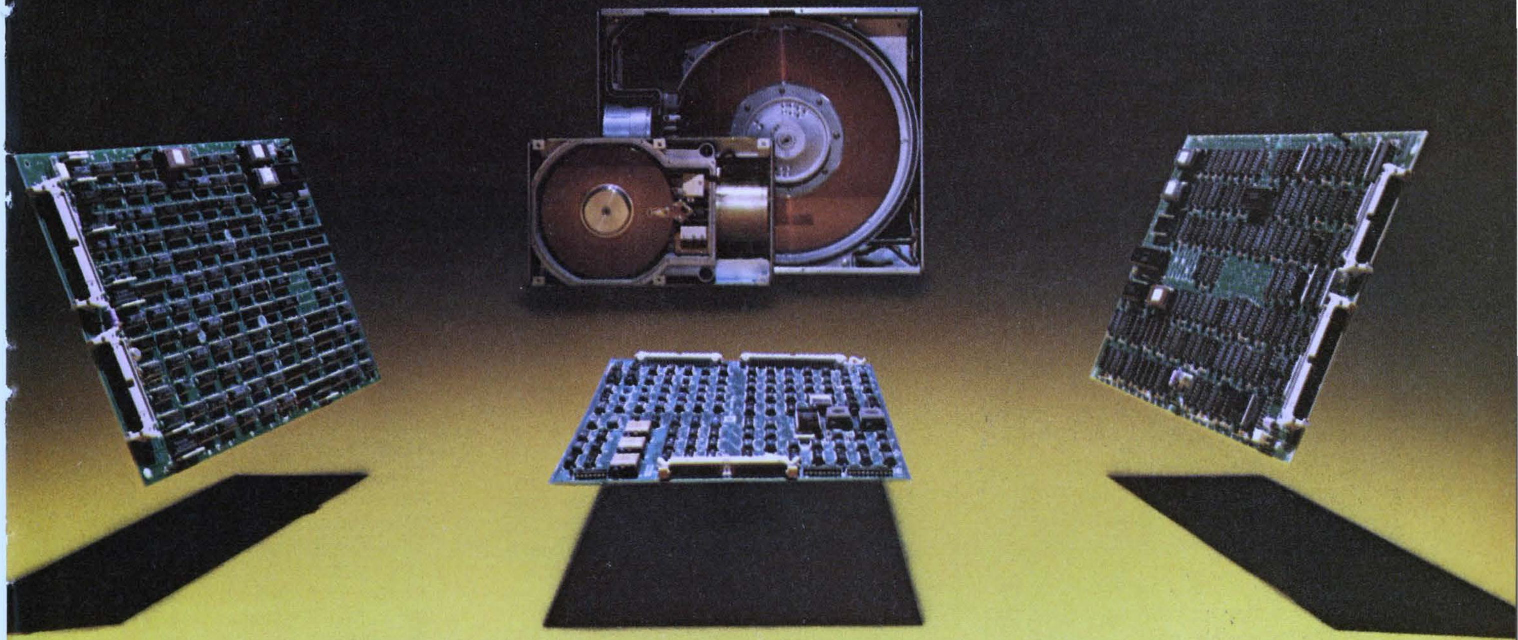
Editor's Note

Our January directory of Forth software companies drew an unexpectedly large and very favorable response. Since the directory was based solely on companies responding to our Forth questionnaire, some companies—those who didn't respond—weren't included. One of these that deserves special mention, as the major supplier of public domain Forth, is the Forth Interest Group (PO Box 1105, San Carlos, CA 94070).

SMART BACKUP!



PRIAM's Intelligent Interfaces For Winchester Discs And Tape Drives

Save time and money by using PRIAM's intelligent interfaces. PRIAM has expanded the SMART family to support *backup* to your Winchester disc systems. Take your pick from 1/4-inch streaming cartridge tape or 1/2-inch tape. PRIAM SMART Interfaces can be mounted on PRIAM drives or separately, and they can be powered from PRIAM's disc drive power supplies.

SMART

Lowest in cost of PRIAM's three intelligent interfaces, the SMART Interface is smart indeed. It includes error checking, disc formatting, selectable sector sizes, full-sector buffering, defect mapping, self-test, and power-down data protection.

SMART-E

Also low in cost, the SMART-E provides all the SMART functions, plus ECC with error correction transparent to the host and high-performance hardware/firmware. Backup is provided by daisy-chaining the EPI STR-Stream* 17-megabyte 1/4-inch cartridge drive or the Pragma DAC 2080* 80-megabyte 1/2-inch cartridge drive.

SMART-T

Compatible with the SMART and SMART-E, the SMART-T provides off-line streaming backup with host access to the database during backup. The SMART-T controls Archive Sidewinder*, DEI Streamer* and Cipher Quarterback* 1/4-inch streaming cartridge tape drives.

In addition to the SMART series, a complete list of disc controllers for popular host busses is available from PRIAM.

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*STR-Stream is a trademark of Electronic Processors, Inc.; DAC 2080 is a trademark of Pragma Data Systems, Inc.; Sidewinder is a trademark of Archive Corporation; Streamer is a trademark of Data Electronics, Inc.; Quarterback is a trademark of Cipher Data Products, Inc.

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Thank you.

The Circulation Department

Calendar

May 3–4
Basic Computer Security Conference, Anaheim, CA. Also, Advanced Computer Security, May 5–7. Contact: ASIS, 2000 K St, NW, Suite 651, Washington, DC 20006; (202) 331-7887.

May 3–5
Cryptography and Data Security, Washington, DC. Also August 2–4 in Palo Alto, CA. Contact: Hellman Assoc, Dept. R, 299 California Ave, Palo Alto, CA 94306; (415) 328-4091.

Automatic and Digital Control, Palo Alto, CA. Also June 16–18, Washington, DC. Contact: Hellman Assoc, Dept. R, 299 California Ave, Palo Alto, CA 94306; (415) 328-4091.

May 3–7
EMC-Design and Measurement for Control of EMI, Los Angeles, CA. Contact: DWCI, State Rte 625, PO Box D, Gainesville, VA 22065; (703) 347-0030.

May 4–6
Eighth Annual Computer Graphics Conference, Detroit, MI. Contact: Carol Lynn, Engineering Society of Detroit, 100 Farnsworth Ave., Detroit, MI 48202; (313) 832-5400.

May 5–7
14th ACM Symposium on Theory of Computing, San Francisco, CA. Contact: Barbara Simons, IBM Research, Bldg. K52/282, 5600 Cottle Rd., San Jose, CA 95193.

May 5–8
1982 Annual Independent Computer Consultants Association Conference, Arlington, VA. Contact: Fran Abernathy, Abernathy Business Consultants, Inc. 414 Hungerford Dr., Suite 358, Rockville, MD 20850; (301) 340-7270.

May 6–8
Information Systems Forum, Tampa, FL. Focus is on key issues affecting information systems users and suppliers over the next decade, IBM's changing systems architecture and the impact of the Plug Compatibles. Contact: Enterprise, Box 1154, Greenwich, CT 06830; (203) 629-1080.

May 9–12
Phoenix Conference on Computers and Communications, Phoenix, AZ. Contact: Leroy N. Templeton, Jr., Honeywell, 16404 North Black Canyon Hwy., Phoenix, AZ 85023; (602) 997-3924.

May 10–12
32nd Electronic Components Conference, San Diego, CA. Contact: D.J. Bendz, IBM Corp., Dept. 649/014-4, 1701 North St., Endicott, NY 13760.

1982 IEEE International Symposium on Circuits and Systems, Rome, Italy. Contact: Prof. Ernest S. Kuh, Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720.

May 10–14
SID 1982 International Symposium, San Diego, CA. Contact: Ifay Chang, IBM Research Center, Box 218, Yorktown Hgts., NY 10598; (914) 945-1234.

May 11–13
DEC Compatible Show, Compatible products and subsystems for PDP-11 and LSI-11 computers, sponsored by MDB. May 11 at Omni International Hotel, Atlanta, GA. May 13 at Sheraton Denver Tech Center, Denver, CO. Contact: Stan Margulis, MDB Systems, Orange, CA; (714) 998-6900.

May 11–14
Computacion '82, Computer And Peripherals Equipment Exhibition, Mexico City, Mexico. Contact: Charles B. Crowley, US Trade Center, Liverpool No. 31, Mexico, D.F. 06600; (905) 591-0155.

May 17–19
Error Correcting and Detecting Codes Seminar, Washington, DC. Also held July 12–14 in Palo Alto, CA; and October 25–27 in Boston, MA. Contact: Hellman Assoc, Dept. R, 299 California Ave, Palo Alto, CA 94306; (415) 328-4091.

May 17–20
Workshop on Logical Data Base Design, Ft Lauderdale, FL. Contact: Robert M. Curtice, Acorn Park, Cambridge, MA 02140; (617) 864-5770.

May 17–21
Graphics Interface 82, Toronto, Canada. Contact: Rich MacKay, DataPlotting Services, 160 Duncan Mills Rd., Don Mills, Ontario, Canada M3B 1Z5; (416) 447-8518.

TEMPEST-Design, Control and Testing, Washington, DC. Contact: DWCI, State Rte 625, PO Box D, Gainesville, VA 22065; (703) 347-0030.

May 18–20
Control Expo '82, Rosemont, IL. Will emphasize both discrete product manufacturing and continuous flow process environments. Contact: Tower Conference Management, 143 N. Hale St, Wheaton, IL 60187; (312) 668-8100.

Northcon (IEEE et al.), Seattle, WA. Contact: Robert Myers, Electronic Conventions, Inc., 999 N. Sepulveda Blvd., El Segundo, CA 90245; (213) 772-2965.

May 19–21
Computer Hong Kong 82, Hong Kong. Contact: Kallman Assoc, 5 Maple Court, Ridgewood, NJ 07450; (201) 652-7070.

Gate Arrays, Boston, MA. Also July 12–14 in Los Angeles, CA. Hands-on experience in custom gate array design. Contact: Hellman Assoc, Dept. R, 299 California Ave, Palo Alto, CA 94306; (415) 328-4091.

May 20–21
Second Annual VLSI Debug And Diagnosis Workshop, New York, NY. Contact: W. Rosenbluth, IBM Corporation FSD, 9500 Godwin Dr., Manassas, VA 22110; (703) 367-3206.

May 25–27
International Symposium On Multiple Valued Logic, Paris, France. Contact: Jon Butler, Northwestern University, Dept. of E.E. & C.S., Evanston, IL 60201; (408) 646-2638.

Electro/82 Show and Convention (IEEE et al.), Boston, MA. Contact: Robert Myers, Electronic Conventions, Inc., 999 No. Sepulveda Blvd., El Segundo, CA 90245; (213) 772-2965.

May 27
Trends and Applications 1982: Advances in Information Technology, Gaithersburg, MD. Contact: Leon Scharff, ADPESO, Dept. of Navy, Washington, DC 20376; (301) 443-2547.

May 31–June 4
Personal Microcomputer Interfacing and Scientific Instrument Automation. Hands-on workshop designing interfaces for personal computers. Contact: Dr. Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061; (703) 961-4848.

Tell us your thoughts

Digital Design is your forum — your inputs help keep the magazine interesting and vital to the design community. So let us know how we're doing and how we can serve you better in the future. We want to know what you like or dislike about *Digital Design,* the subjects you'd like to see us address, how you feel about the problems you face every day as design professionals.

If you have thoughts your peers should know about, put them in a letter in *Digital Design.* Have your say in *your* magazine! Send letters and comments to: Editor, *Digital Design,* 1050 Commonwealth Ave., Boston, MA 02215.

News Update

OAK Industries Forms Satellite Communications Subsidiary

Oak Industries Inc. announced today it has formed a new subsidiary, Oak Satellite Corporation, to consolidate and develop the company's activities in satellite communications.

In announcing the new company, E. A. Carter, chairman and chief executive officer of Oak Industries, said "Oak Satellite Corporation has one purpose: to make Oak a major entity in the business of satellite communications. By consolidating our current satellite operations into a unified, integrated unit and providing experienced senior management, we expect to accelerate the establishment of Oak as a leading participant in an activity with exciting potential."

RCA To Make And Market Color Data Display Tubes

RCA has announced plans to enter the color data display tube business. A 13" (diagonal) color display tube, designed for use in high-volume electronic office applications, will be the company's initial product in this field. Samples of the tube are now available to equipment manufacturers for engineering evaluation.

CSI Expands Short Run Wafer Service

Comdial Semiconductor, Inc. (CSI) today announced expansion of its quick turnaround short-run wafer fabrication services to accommodate a sharp upturn in low volume, custom circuit requirements. Gary P. Kennedy, Vice President, Operations, said CSI is adding another full shift of process personnel and expanding resources to meet the demand of clients with limited quantity, time-dependent projects.

"Increased short-run activity apparently reflects a proliferation of custom circuit development," said Kennedy, "most of which is for preproduction or limited production use under critical deadlines." Short run fabrication of wafer lots up to 125 per month per client are up 70 percent from last quarter, Kennedy said, noting that in contrast major semiconductor mass manufacturing houses have shown less activity in volume runs of standard products.

Europe Plans Joint Computer Research

Philips is among several major European electronic companies which are now holding talks with officials of the European Commission about a program to increase long-term research into computer technologies. If the Community's member states agree, the program will start towards the end of 1983.

Five areas of computer technology that could benefit from extra research have been identified: office technology, factory automation, software, advanced microelectronic chips and new ways of processing information in the computers of the future.

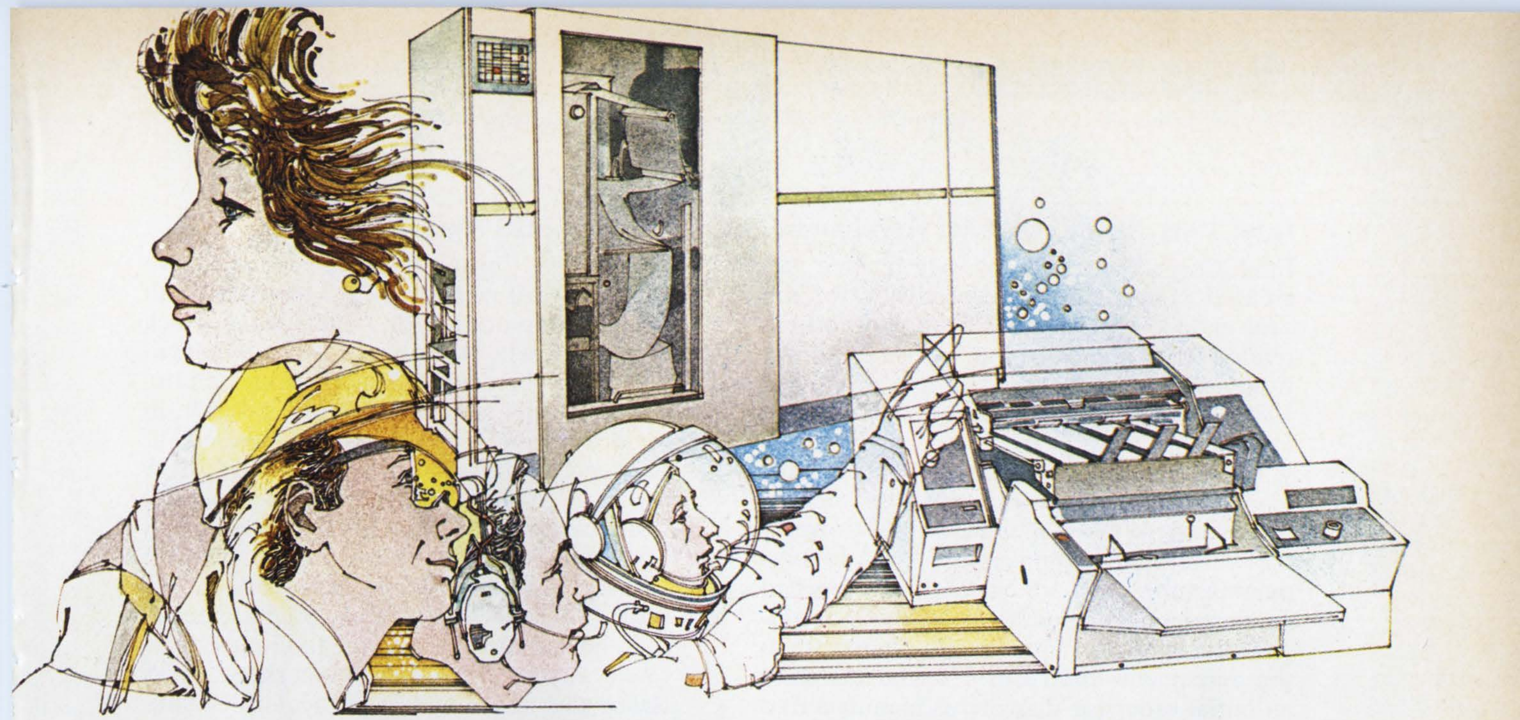
The plan is that the money should be spent over ten years. It would finance research groups in existing institutions in Europe, private laboratories and universities for instance. Approximately half the money would come from European Community funds; the rest from industry and other sources.

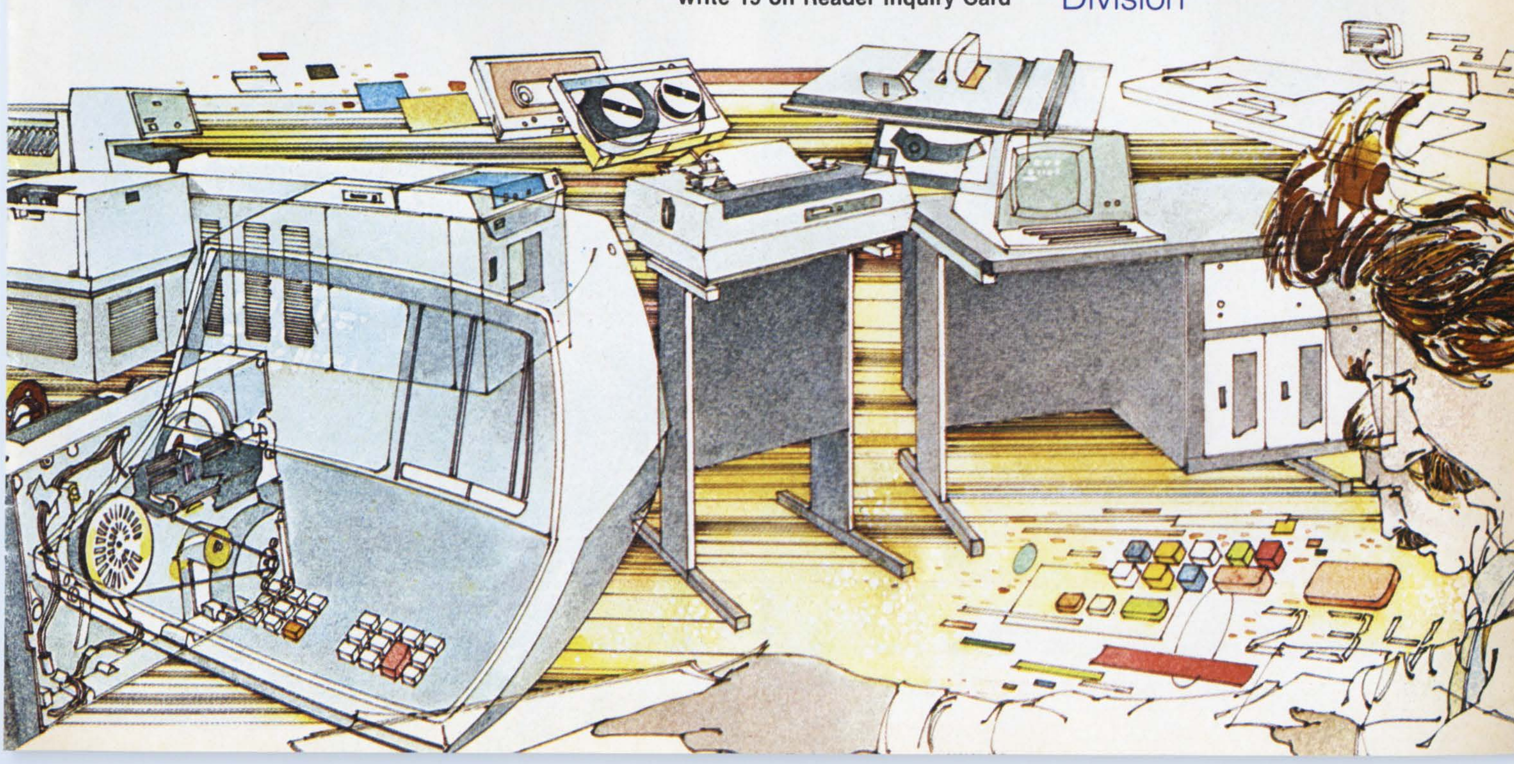
APh Forms Subsidiary

APh Corporation, a Pasadena, CA prototyping and software firm, announced today the formation of a wholly-owned subsidiary—Octothorpe—to market its in-house development tools. These tools include DEC-compatible Ethernet boards and software, the MX family of cross-assemblers for various μPs, and the Datawidget line of μC development systems.

RAIR Computer Announces Joint Venture With ICL

RAIR Computer Corp., which opened its US headquarters last June, has announced a major joint venture with Europe's largest computer manufacturer, International Computers Limited (ICL) of the United Kingdom. The RAIR/ICL agreement calls for the European computer giant to manufacture RAIR's popular Black Box 3/30 μC under ICL's own trade name, "The ICL Personal Computer." ICL will also manufacture a certain number of Black Box 3/30s for RAIR, and will retain the RAIR technical staff as the design authority on this and future μC products.





Intel 1981 Revenues, CMI Agreement

Intel Corp. revenues and net income decreased 8% and 72%, respectively, for the year ended December 31, 1981. Net income totaled $27.4 million or $.61 per share, down from $96.7 million or $2.21 per share for 1980. Revenues decreased from $885 million in 1980 to $789 million.

In other Intel news, Irwin Rubin, Chairman of the Board of Computer Memories, Incorporated (CMI) identified Intel Corp. as the electronics components and systems manufacturer with whom CMI had reached an agreement in principle which was originally disclosed on February 9th. Pursuant to the agreement, Intel Corp. would (1) place an initial order for disk drives manufactured by CMI, (2) be licensed as a manufacturer for CMI's disk drives, and (3) purchase an approximately 20% interest in CMI from CMI and its non-public shareholders for approximately $4.8 million.

Toshiba–SGS Agreement

SGS–ATES Corporation has signed a five year technical collaboration agreement with Toshiba Corporation of Japan. SGS, which describes itself as "a broad range semiconductor supplier, world leader in linear integrated circuits and with a strong position in MOS devices," entered into this agreement to strengthen its position in advanced CMOS products. SGS will receive two high density CMOS processes and will gain access to all Toshiba products made using these very advanced technologies. The key products are static CMOS memories, CMOS μPs, gate arrays, advanced logic circuits and many dedicated circuits for special markets. SGS claims this agreement is particularly significant because it is the first one signed between a leading Japanese semiconductor company and one of the most important European manufacturers in this field.

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Write 48 on Reader Inquiry Card

#1 **DATARAM M23**
See it first at NCC '82

Dataram M23
The Useable 4.0MB LSI-11®

A dramatic innovation unlocks the power of the LSI-11/23

The M23: The answer to your high-performance LSI-11/23 needs

What controllers can be used?
The key to the M23 System, Dataram's proprietary memory management Q-MAP enables you to use the full 4.0MB power of the LSI-11/23. It provides I/O mapping, which supports a wide range of existing peripheral controllers on an 18-bit bus (Q18). While still maintaining the 22-bit bus (Q22) for 4.0MB main memory addressing.

DEC® software compatibility?
The M23's Q-MAP emulates DEC's KT24 memory management, which means it operates with RSX11-M, RSX11-M PLUS, RSTS, UNIX, and all other DEC operating systems which support the KT24.

Memory?
A 1.0MB quad board is contained in the basic M23 configuration. Think of it, a full 4.0MB on only four DEC quad boards! And each additional 1.0MB is only $3400.

System configurability?
The 5¼" M23 provides an incredible 27 DEC dual slots. And since the basic configuration (LSI-11/23, OCU, two SLUs, Q-MAP, bootstrap/diagnostic PROMs, and 1.0MB memory) occupies only six of those 27 slots, that leaves you 21 slots to configure a high-performance LSI-11 system.

5.0 volt current?
36 amps.

Price?
$9400 for the basic configuration, with 1.0MB, in single quantity. Yes, only $9400...and considerably lower in OEM quantities.

More information?
Circle the reader service number below, or better yet, call Dataram now at 609-799-0071, or write to Dataram, Princeton Road, Cranbury, New Jersey 08512. Telex: 510-685-2542.

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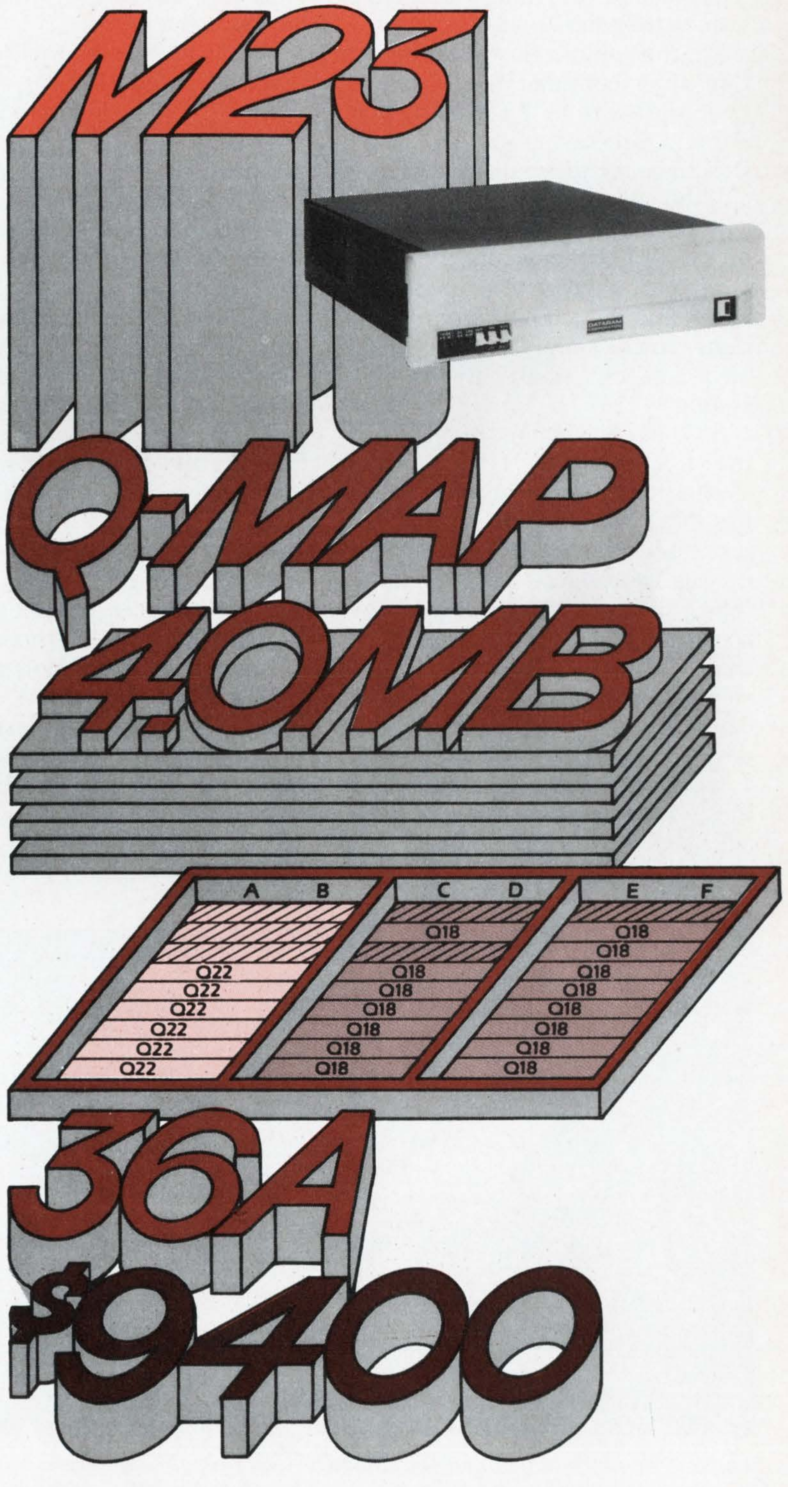

DATARAM CORPORATION

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32-Bit Processors: Can They Be Called "Micro" Much Longer?

At the International Solid State Circuits Conference in February, two of the most prominent 32-bit micros from Bell Labs and Hewlett-Packard received a lot of attention, and they may well arrive sooner than anticipated.

At this point, the question is: Can they continue to be called "microprocessors"? HP calls their effort a processing system, while Bell Labs identifies their device as a 32-bit micro. Perhaps the 32-bit μPs should be called "maxi-μPs" or by some other extension term until a new label is coined. For now, HP appears to be on the right track simply calling their chip set a "32-bit processor system."

S. Dana Seccombe, manager of the R&D lab at HP's System Technology Operation in Ft. Collins, CO, referred to the 32-bit processor as a "super-chip" when it was introduced at the 1981 ISSCC meeting. As a single logic control device, it contains 450,000 transistors. This year, HP previewed the system RAM, its most dense device, containing 660,000 devices in a 128,000-bit memory.

It is interesting to note that these two devices are produced using 1.5 μ-wide lines with 1μ line spacing. With smaller line sizes, complexities could get even more impressive—perhaps closer to one million transistors on a chip in this decade. What's really interesting is that logic and memory in this case are not very far apart in component count.

HP is not willing to disclose any specific application for the 32-bit processor, but it has said that it hopes to introduce a product in about a year (possibly a desktop 32-bit machine). The entire chip set consists of a 32-bit processor, memory controller, RAM, ROM, I/O processor and clock generator. The CPU has a 55ns microcycle time; control store ROM; 32-bit address/data bus with pipelined data transfers at a 36MB/s transfer rate; and a 230 instructor repertoire, including special instructions for byte, half word and word formats, IEEE standard math formats, multiprocessing, and multiple processors.

The 128Kbit RAM, the most dense with 660,000 transistors, is unique in its component count alone. This 128K RAM chip uses a four-transistor cell design making it ideal for synchronous operation at high speed. HP claims that over 0.5V internal signal levels provide good margin and reliability. The ratio of correctable area to uncorrectable area is high, contributing to high yield. HP also claims that the four transistor cell design permits faster design than single transistor cell implementations.

To produce this 32-bit processor, HP not only developed the individual devices as a total system, but has also designed a special board and interconnect package. Chips are mounted directly to a copper core or board with four layers of interconnects (two on each side of the core), separated by Teflon dielectrics with 5mil minimum trace lines and spaces. Substrates are connected to a backplane with conventional PC sockets. The air cooled substrate dissipates 18W at 35°C worst-case junction temperature rise over ambient.

H-P claims that by developing the processor system chips and the interconnect technology at the same time they have been able to reduce speed problems resulting from limited MOS drive capacity and to improve propagation delays and timing skews resulting from varying path lengths and loading. Heat dissipation problems also appear to be minimized with the chip/board/system design approach.

It is interesting to see the direction HP is taking today, pointing to larger capacity, yet more compact computer systems. While the chip technology is extremely interesting, it represents more evolution than breakthrough.

The combination with the packaging technology is, however, more of a technology trend. It represents a different approach to processor design beyond the chips. In fact, it is a design refinement that will see more application in the future. The total system design approach for a processor is the type of design improvement that steps beyond the board level processors currently being offered by the semiconductor producers. —*Groves*

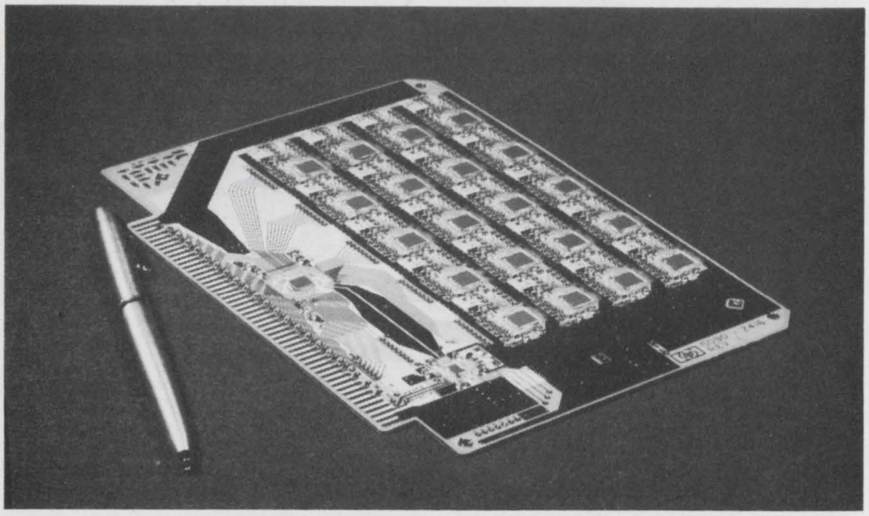

Figure 1: Tiny computer chips are bonded to a special copper-core substrate for higher-performance connections and to aid cooling in a 32-bit processing system.

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Eaton's line of alphanumeric dot matrix impact printers give you printer power plus. You get performance, exclusive product features, attractive prices—all designed and backed by Eaton—one of the great names in American industry.

Eaton printers feature a 100 million character life printhead, easy interfacing and a simple, low maintenance design.

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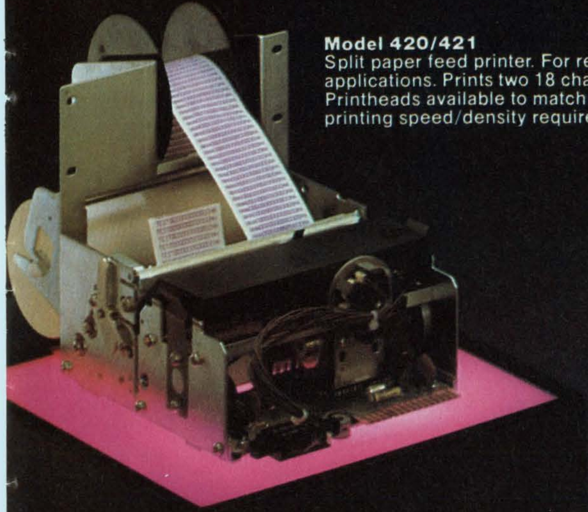
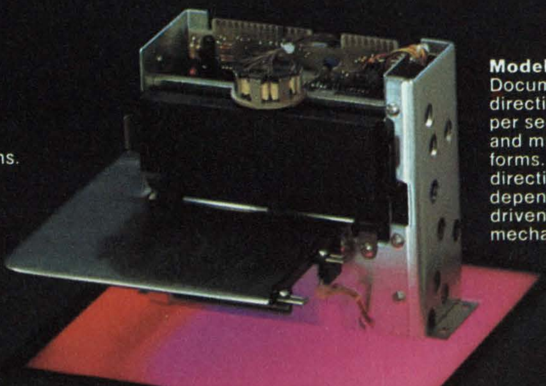
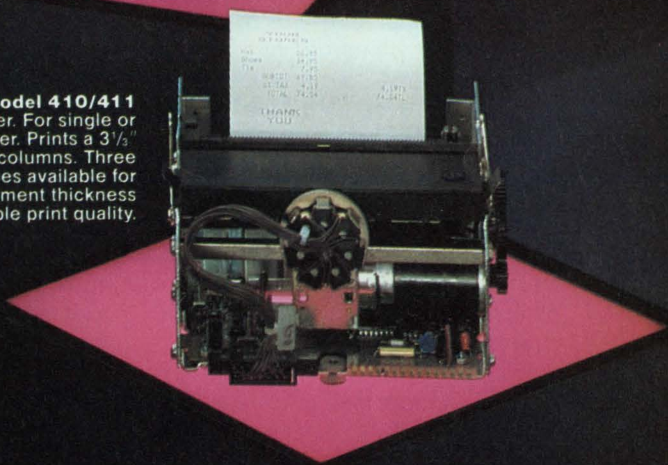


Model 420/421
Split paper feed printer. For receipt/audit applications. Prints two 18 character columns. Printheads available to match paper and printing speed/density requirements.



Model M-400
Document printer. Prints bi-directionally up to 3 lines per second. Handles single and multi-ply tickets and forms. Speed 3 lps bi-directionally. Has a quiet, dependable stepper motor driven paper advance mechanism.



Model 410/411
Single roll printer. For single or multi-ply paper. Prints a 3⅓" line up to 40 columns. Three printhead types available for various document thickness and dependable print quality.

Model 7000+
Designed for commercial and industrial needs. Simple design, no special paper needed. Attractive case. 40 or 64 character capacity.

Printheads
Choose from 3 printhead models for integration with your own equipment. All with a minimum of 100 million characters and lifetime, low maintenance reliability. Short, medium, and long stroke models. Available in either 40 or 24 VDC.

EATON Printer Products

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128K-Bit ROM for Speech Applications

National Semiconductor has introduced a 128K-bit (16,348 × 8) Maxi-ROM for use with the company's Digitalker I speech synthesizer.

The new MM52128 is the largest-ever ROM from National, designed to hold very large vocabularies of up to 140 words. It is specifically intended for applications requiring large storage volume, minimal circuitry and low-power operation. Power dissipation is 20mA in the active mode; 5mA in the power-down mode. The device features single-supply operation of 4.5-11V, and provides complete DTL/TTL compatibility on all input/output lines.

Because speech is a relatively slow process as compared to computer speeds, fast access times are not required. The chip size can be significantly reduced, thereby reducing the cost of the device. The new MM52128 Maxi-ROM has a typical access time of 3μs.

Priced at $25 each in 1000-piece quantity, the single ROM device takes the place of two high-speed, 64K-bit ROMs in a system, thereby reducing system size and lowering costs. User-designed vocabularies in either male or female voices are encoded at National's factory, and are implemented onto one single-layer mask of the MM52128.

National offers the user a standard vocabulary list, and can custom encode any words a user may require.

Fast CMOS Challenges Low Power TTL

Philips/Signetics and RCA have announced that they will be introducing more than 180 high-speed low power CMOS circuits, beginning in the second half of 1982. This new family of CMOS logic will have the same pinouts and logic/functions as series 74/54 TTL with speeds equivalent to low power Schottky TTL. They will be able to serve as drop-in replacements for LSTTL in current equipment designs.

With speeds 20 times faster than CMOS metal gate devices, the basic family designated 74/54HCXXXX will operate at CMOS logic levels with supply voltages ranging from 3 to 6V and power dissipation about 0.001 times that of normal LSTTL devices.

RCA and Philips will follow common design rules (a 3μ oxide isolated silicon-gate process with low threshold voltage) and will exchange tapes for computerized mask generation. The companies will also be able to alternate-source each other's products.

Signetics, a wholly-owned subsidiary of Philips, will provide both Philips and RCA with the basic LSTTL designs that they now produce in bipolar. Signetics will act as a marketing organization for the new 74/54HC CMOS line in the US for Philips in Holland. US production by Signetics is likely at some future date.

The 74/54HC CMOS logic family will include 17 gate types, 14 buffers, 32 flip-flop/latches, 17 transceivers, 15 registers, 20 counters, 26 encoders/decoders/multiplexers, 8 level connecters, 9 switches and 22 assorted functions. Clock rates will be 50 MHz, and typical gate delays will be 10 ns with a 50-pF load. Output drive current will be 4mA, equivalent to driving 10 LSTTL devices. Bus driver types with a 6mA output current should drive 15 LSTTL inputs.

Another group of circuits which will be designated 74/75HCTXXXX will operate at standard TTL levels. The companies foresee the use of these circuits in replacing LSTTL in existing equipment which requires a lower performance. Several useful 4000 series circuits, currently without LSTTL equivalents, will also be included within this new family.

Circuits developed by either RCA or Philips will be produced in either company's production facilities in the US and Europe.

—Groves

Media Questions Challenge Optical Disk Development

At least a dozen development efforts are underway to find a suitable medium for optical storage systems. But system designers have placed two fundamental—and apparently conflicting—demands on media: a high sensitivity to laser light, and the ability to keep recorded data intact long-term. Other key considerations are the amount of information that can be packed onto a disk, the ability to read the data immediately after recording it, and raw bit error rate—as well as cost and availability factors.

One of the most controversial issues has been archivability; a medium generally is defined as archivable when it can store data for 10 years without degradation. However, since none of the existing media has been around for 10 years, efforts to prove archivability for any are inconclusive.

The major approaches to optical media thus far have been photographic film, ablative techniques, bubble media, and erasable media.

Ordinary silver-halide film, similar to that used in cameras, has been explored as one alternative. This extremely sensitive material has demonstrated long-term stability; in fact, it's the only medium presently accepted as archival by the US National Archives. It's also inexpensive and readily available in large quantities. A major problem, however, is that exposed film must be processed chemically before it can be read. This precludes the use of error-correcting schemes that rely on the ability to read data shortly after it has been written. Similar problems have been found with electrophotographic films and dye films.

A second approach—and one that has met with more success—is the "ablative" technique. This involves the burning of holes in one of a number of thin-metal films, the most common of which is tellurium. A laser beam is focused to a spot on the film, melting a small area. At the center of the spot, where the beam is most intense, an even smaller hole opens. Surface tension then causes the surrounding molten metal to curl back onto itself, forming a rim.

Tellurium, whose use is being pioneered by RCA and Philips, is a good ablative medium because of its extremely fine resolution and highly dense data storage capability. But this very sensitive medium is also subject to rapid oxidation and degradation by humidity; and its thin, brittle layers may flake off of the substrate after vacuum deposition.

The bubble media approach has shown the most promise. In this technique, gas is produced by the thermal decomposition of a sensitive polymer under laser illumination; this gas pushes upward against a metallic surface to create a tiny bubble, or blister, instead of a hole. The chief advantage here is lifetime. Because the metal layer is not vaporized, it can have a high melting point. Therefore it is inherently more stable than low-melting-point, more reactive materials such as tellurium.

At less advanced stages of development are various erasable media. Like magnetic media, these can be used repeatedly, with new data displacing the old whenever desired. Present erasable optical media cannot compete with magnetic media on a price/performance basis, but developments later in this decade will likely allow them to displace magnetic media as the latter approach their technical limits.

Optimem Div.
Shugart Assoc.
San Jose, CA

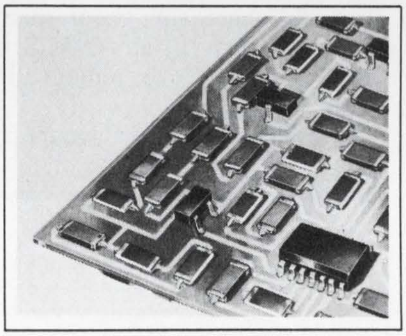
Unpackaged Capacitors For ICs And Boards

To produce high density device packaging on both sides of a printed circuit board has long been one of the problems faced by the designer.

Recently, passive device manufacturers, such as AVX and Philips, have discussed a new product aimed at solving these problems: the surface mounted device or SMD. These devices include ceramic capacitors, thick film resistors, transistors/diodes and integrated circuits.

Many SMD devices are leadless and hence fewer solder connectors are required per device, as well as fewer connections, resulting in higher reliability. Integral to the development of the SMD devices themselves is the packaging of these devices for use by automatic placement equipment.

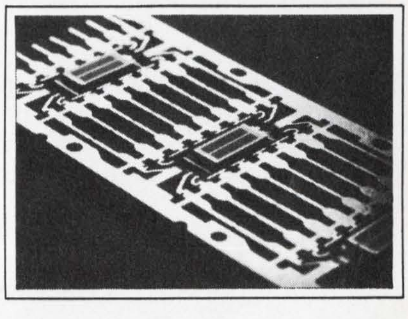
There are several packaging systems in use. The basic require-



ments are: locate and orient the device, identify and protect the device during shipment and storage, and feed the device into a standardized production machine for placement on the board.

At the present time the tape and reel system is the most commonly used. Devices are positioned into pockets in an 8mm wide carrier tape and retained by transparent tape. This ensures full pockets and positive identification right up to the positioning of the device on the board. **Figure 1** shows a typical printed circuit board layout utilizing SMD technology.

The system designer and manufacturer benefit from the elimination of the decoupling capacitor through increased PC board densities, fewer components and easier PC board layouts, according to AVX. **Figure 2** shows the AVX BitGuard product designed into its working environment.



Military CMOS Gets Tougher

In 1970, the military/aerospace industry probably consumed 40% to 50% of the integrated circuit production. By 1979, that number had decreased to estimates as low as 7% to 10% of the IC market. As the most dominant consumer of semiconductors a decade ago, the government could get anything it wanted, but by the end of the decade it had trouble finding semiconductor manufacturers willing to produce and test devices to their specifications. For the semiconductor companies to actively pursue government/contractor business, they had to set aside dedicated production, test, packaging and quality facilities tying up people and scarce capital. A few firms like TI, Motorola, National and Signetics produced a broad range of Mil 883 devices. Other companies were much more selective in the range of products produced and qualified for this market. At the same time, many of the major military prime contractors developed inhouse design and production capability. A few like Hughes Aircraft, Rockwell, and TRW have also entered the merchant semiconductor market with capabilities and products originally developed for the military.

This leads to an increasing market place for military quality components at the same time that the military/aerospace world appears to be changing its technology directions. The Very High Speed Integrated Circuits (VHSIC) program is a tri-service R & D program aiming at 0.5-micron circuit geometry and device complexities exceeding 100,000 active components on a ¼-inch chip. Among the major technologies being used in this program, the two dominant technologies are CMOS and bipolar. The major funding, however, to be directed to CMOS. Why CMOS?

CMOS is changing from a low performance (7 ns/gate av.) to a very high performance technology (under 2 ns/gate). Its complexity can be comparable to or approach NMOS, and it consumes less power than other types of devices. It has one very weak point—radiation hardness. Bipolar structures have greater natural rad hard properties. CMOS and the other MOS technologies are pale in comparison. One of the chief objectives of the VHSIC program is to change these characteristics of CMOS. A goal of 10^{12} rads has been set for CMOS hardness or better than double current CMOS offerings.

Meanwhile, there are military systems trade-offs that make CMOS viable. Its low power consumption (several orders of magnitude less than equivalent bipolar) is of particular significance in avionics systems, and the Cruise missiles in particular. Shielding can be added to the circuit boards or an entire system. The weight savings in power supplies and cooling alone can accommodate the shielding with weight to spare compared to the same system in bipolar. Low power consumption also saves cooling and power supply bulk where equipment space is very limited. In all, CMOS is the military IC technology to watch.

Complexity increases sought in the VHSIC program should begin to appear in the mid-1980s. The Pentagon is also aware of its relatively small consumption of components. Even if military consumption increases, commercial consumption will continue to increase as well, taxing industry capacity even more. This should lead to more inhouse production by the primes. However, transportability of the process techniques and software (a key design goal of VHSIC) will permit moving production from producer to producer as requirements change. It will also mean greater dependence on gate array technology rather than dedicated chip function designs. Arrays or glue chips of 2000 to 6000 gates in complexity are among the VHSIC design objectives. We may see the production of a particular type of IC move from prime contractor, to semiconductor manufacturer and finally back to the prime as volume decreases near the end of the program. It is essentially a silicon foundry concept, with ownership of the technology, design, and software being retained by the Pentagon, but available to all systems contractors requiring that type of technology.

Short term forecasts for the military market (through 1985)

Motorola Cancels Wyle Distribution

As of February this year, Wyle Distribution will no longer distribute Motorola's line of semiconductors. This move follows last November's termination of Wyle's Los Angeles division by Motorola. At that time, Wyle management strongly requested the reinstatement of this division and additional distribution facilities in Portland and Salt Lake City. Motorola, who had expressed public concern about the addition of TI to Wyle's line, also asserted that Wyle's market performance in Santa Clara had slipped. According to Wyle, this was because Motorola had expanded its number of authorized dealers in this area from three to five. The distribution company will now concentrate on its other suppliers which include Intel, National Semiconductor, TI and Signetics.

look like procurement will be for an operational system or systems ready to go into volume production. This market is presently a bipolar IC market because of the speed and radiation specs. In 1980, sales of military ICs showed some dramatic increases, but because of the recession there was price erosion. Unit sales were up across the board but sales for the IC producers remained flat or up only slightly. In 1982, both units and dollars should increase rapidly. The major limiting factors will be the IC production capacity able to produce fully Mil-qualified devices.

New designs appear to show an interesting trend toward newer unqualified products. Many primes are more willing to begin new hardware designs using ICs that have yet to be Mil qualified, if they get a guarantee from the semiconductor producer that the device will be qualified. In the past, the primes were very reluctant to design a hardware system with unqualified components. This meant designing new systems with 3 to 5 year old component technology. Many have been forced to qualify devices on their own or pay excessive premiums, because the semiconductor producers refused because of the small number required.

It is a changing world, yet bipolar remains on top at least for the next few years. CMOS, and the fall out from the VHSIC program, can be expected to cause more important changes.

The designer in the military systems house today should keep his eye on CMOS. Its geometries are shrinking fast, its speed is up, and its power and cooling requirements are down. The bipolar world will not give up easily, especially for real time processing applications. A technology war is entirely likely, but the big money seems to go with CMOS. Once CMOS achieves the 10^{12} rads hardness goal of the VHSIC program the war may be won in the power supply. Today, bipolar ICs sell at a rate of 4 to 1 CMOS device. By 1990, that should be reversed. CMOS with much lower power still has a speed gap to close with bipolar, but that too is getting smaller every day as the circuit geometries decrease.

Energy Related Computer Services To Hit $5 Billion

Expenditures by energy companies for computer services will reach $5 billion in 1985, up nearly 40% per year from $1 billion in 1980 according to a recent report by Input.

Exploration and production companies spent approximately $700 million on computer services in 1980 which made up 75% of the total market (**Figure 1**). Spurred by sharply increased expenditures by petroleum companies, the exploration subsector alone will rise to nearly 80% of total computer service revenue by 1985, Input claims.

SUBSECTOR	USER EXPENDITURES ($ millions) 1980	1985	AAGR 1980–1985 (percent)
Exploration	$578	$3,900	46%
Production	145	510	29
Processing	73	170	18
Transportation	79	180	18
Marketing	90	240	22
Total	$965	$5,000	39%

Figure 1: Forecast of computer services expenditures in energy markets by subsector, 1980–1985 (source: Input).

Processing services revenues, nearly 73% of the total market at $700 million in 1980 reflect the volume of geophysical data processing in energy markets. Facilities management (FM) opportunities will increase as energy companies expand exploration budgets, but have a decreasing ability to hire and retain qualified personnel. Batch processing, currently the major delivery mode for processing services, will give way to RCS as multitasking operating systems with user friendly interface software increase remote batch and interactive operation.

Shortages of qualified geophysicists and computer analysts coupled with escalating exploration activity is forcing the top 20 petroleum companies to shift major portions of their seismic data processing to services vendors.

The large number of consulting, specialist, engineering, and construction firms offering services in energy markets results in a significant market for computer software products and professional services. These companies form a rich source of licensing software products to RCS vendors, and of sale of block time and network services.

The report entitled Computer Services Opportunities in Energy Markets, analyzes both present and future computer services markets, provides a basic technical background and recommendations for energy market entry and expansion.

For more information write to Nancy Hill, INPUT, 2471 East Bayshore Road, Suite 600, Palo Alto, CA.

Multiplexed LCD Display Driver With On-Board RAM Frees Up Host Processor

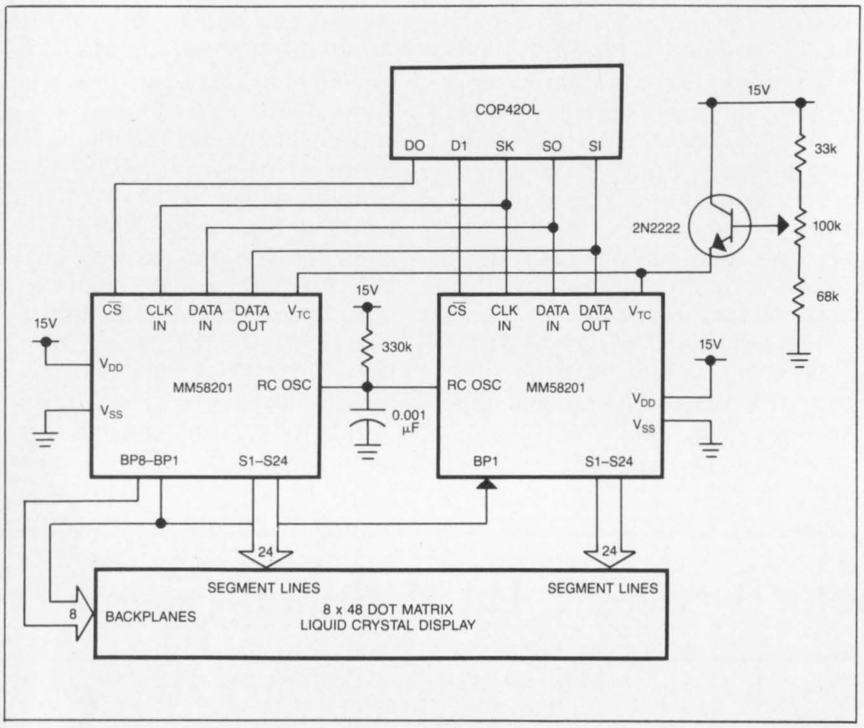


Figure 1: A typical application of the MM58201 LCD display driver from National Semiconductor.

An "intelligent" multiplexed LCD driver, the MM58201, that utilizes 192-bits of on-board RAM to maintain displays is currently available from National Semiconductor.

To minimize the interconnect between the system and the MM58201, serial data input and output pins interface directly with the controller.

The part can drive up to 8 backplanes and 24 segments for a total of 192 segments. Four additional bits of RAM allow the user to program the number of backplanes being driven, and to designate the driver as either a master or slave for cascading purposes. When two or more drivers are cascaded, the master chip drives the backplane lines, and the master and each slave chip drive 24 segment lines, amounting to 384 or more respectively.

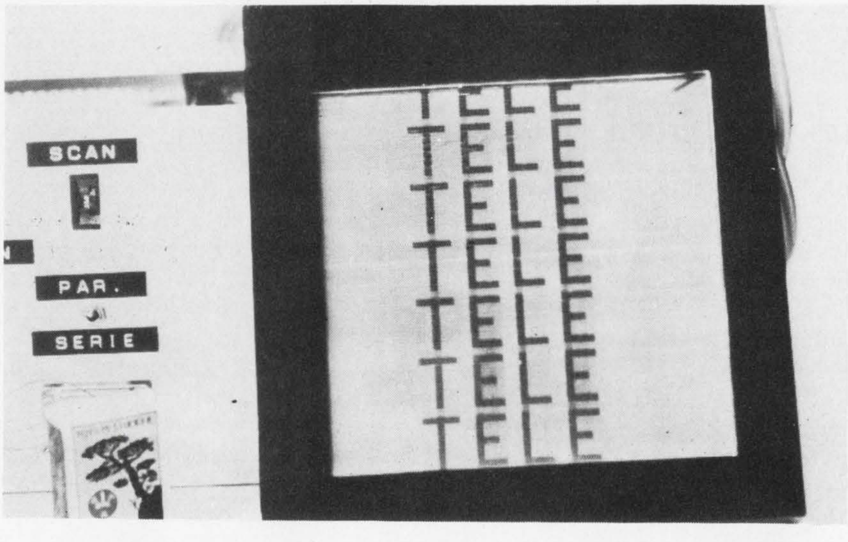
An on-board RC oscillator generates the timing required for multiplexing the LCD. The oscillator works at a frequency that is 4n times the refresh rate of the display, where "n" is the number of backplanes programmed.

The V_{tc} pin (**Figure 1**) is an analog input that controls the contrast of segments on the LCD. If 8 backplanes are being driven ($n = 8$) a voltage of typically 8V is required at 25°C. The voltage for optimum contrast will vary from display to display.

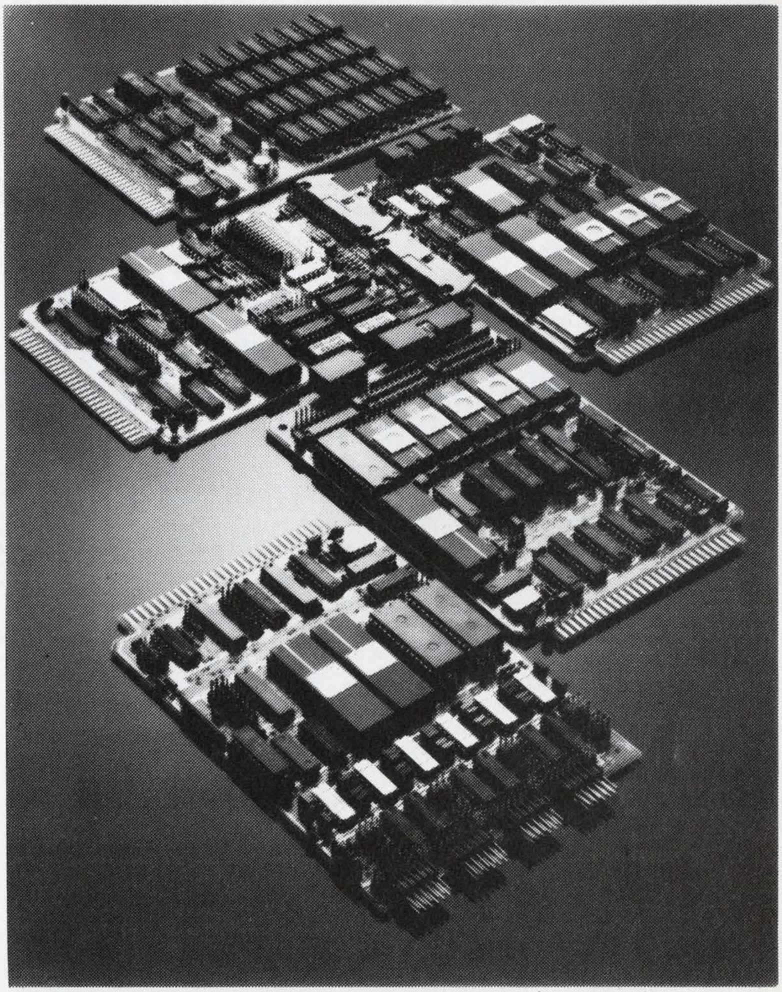
LCDs Break Size Barrier

Claiming to be the first company in the world to make large LCDs commercially, Norsk LCD A/S of Drammen near Oslo currently produces cells measuring from 20 x 15 cm up to 30 x 30 cm.

A first contract has already been secured by the new firm to supply a railway station indicator board measuring 3 square meters. Norsk LCD is currently looking to produce flat computer display screens, which are currently at the experimental stage. Some of these screens have already been supplied to the Research Establishment of Norway's Telecommunications Administration.



THE DY-4 SYSTEMS STD BUS PRODUCT LINE



DSTD-101 Z80(A) CPU with 1K RAM, 4 Counter/Timer Channels and 2-8 Bit Parallel I/O PORTS, 5-28 Pin Sockets for Byte wide ROM/RAM/EPROM.

DSTD-102 Z80(A) CPU with 1K RAM, 4 Counter/Timer Channels and 2-RS232C Serial Ports — 3-28 Pin Sockets for Byte wide ROM/EPROM/RAM.

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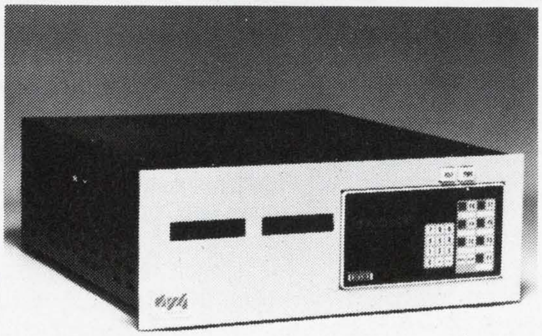

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GCR And Its Applications For Minicomputers

by Haim Brill

Group Code Recording (GCR) is the most current and practical method of storing large amounts of data on ½" magnetic tape. It provides high storage capacity of data and high data integrity. High data throughput is the direct result of the two above issues.

The method of recording which is described below was first introduced by IBM in 1973, and is currently widely used by all mainframe manufacturers. In the last three years, GCR has become increasingly popular on minicomputers. GCR meets the increasing need for storage of large data files and for recording high-speed events in real time.

Recording Methods

Data is stored on magnetic media, whether it be disk or tape, by flux reversals which are detected by the read head as the medium moves over it. The differences between the various schemes are in the interpretation of the transitions. Only the actual encoding of individual bits is being considered here. The earliest method used was Non-Return to Zero (NRZI), where a transition was considered to be a logical one and no transition within the bit cell was interpreted as a logical zero. The bit cell was defined as the area within a defined distance after the first transition within a character. The next encoding method used was Phase-Encoding (PE) of the bits. A positive transition in the middle of a bit cell is interpreted as a logical one and a negative transition as a logical zero. A transition at the bit cell boundary may or may not occur depending on whether the previous bit was the same or different: two consecutive logical ones will have a transition at the bit cell boundary separating them. Several other encoding methods are presently popular, but are being mostly used for disks. These include Frequency Modulation (FM) and Modified Frequency Modulation (MFM).

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When storing large amounts of data on tape, Group Code Recording (GCR) provides high data throughput.

NRZI is not self-clocking and, therefore, the density is limited by the skew in the data due to misalignment of the head and due to bit crowding, where a transition moves due to neighboring transitions. PE overcomes this problem by having each track self-clocking and decoded independently of the other tracks. But PE gains density at a great cost in efficiency—up to two flux reversals are required for each bit stored, making it the least efficient of the encoding schemes above.

With Group Code Recording, the actual encoding method is NRZI, but the data is first encoded so as to guarantee that there will not be more than two zeros in a row in any track; therefore each track is self-clocking. This encoding is done by taking the data pattern which always has at least one logical zero. Since only 16 of the possible 32 combinations are used for data encoding, some of the remaining patterns are used for formatting records on the tape.

Error Correction Improves Throughput

The tape medium is imperfect and subject to errors due to non-uniformity of the magnetic material and dirt between the tape and the read head. To increase confidence in the integrity of the data, check characters are appended to the data. In 9-track NRZI recording, each character always has odd parity. A cyclical redundancy check character (CRCC) is added for further checking the data. In addition to CRCC, a longitudinal redundancy check character (LRCC), which is simply generating a character so that each track has even parity over each record, is also appended.

Although it is possible to correct some errors using the three different character checks, this is generally not done in NRZI recording systems. In PE recording, the characters are recorded in odd parity, but the other check characters are not used. Since each bit cell always has a transition in the middle of it, it is possible to do some error correction. If one track goes dead—

	Data Integrity	Capacity Per 2400′	Relative Throughput
NRZI	10^8	20 Mbyte	1.0
PE	10^9	46 Mbyte	1.8
GCR	10^{11}	180 Mbyte	7.0

Figure 1: A comparison of the merits of PE, GCR, and NRZI recording methods.

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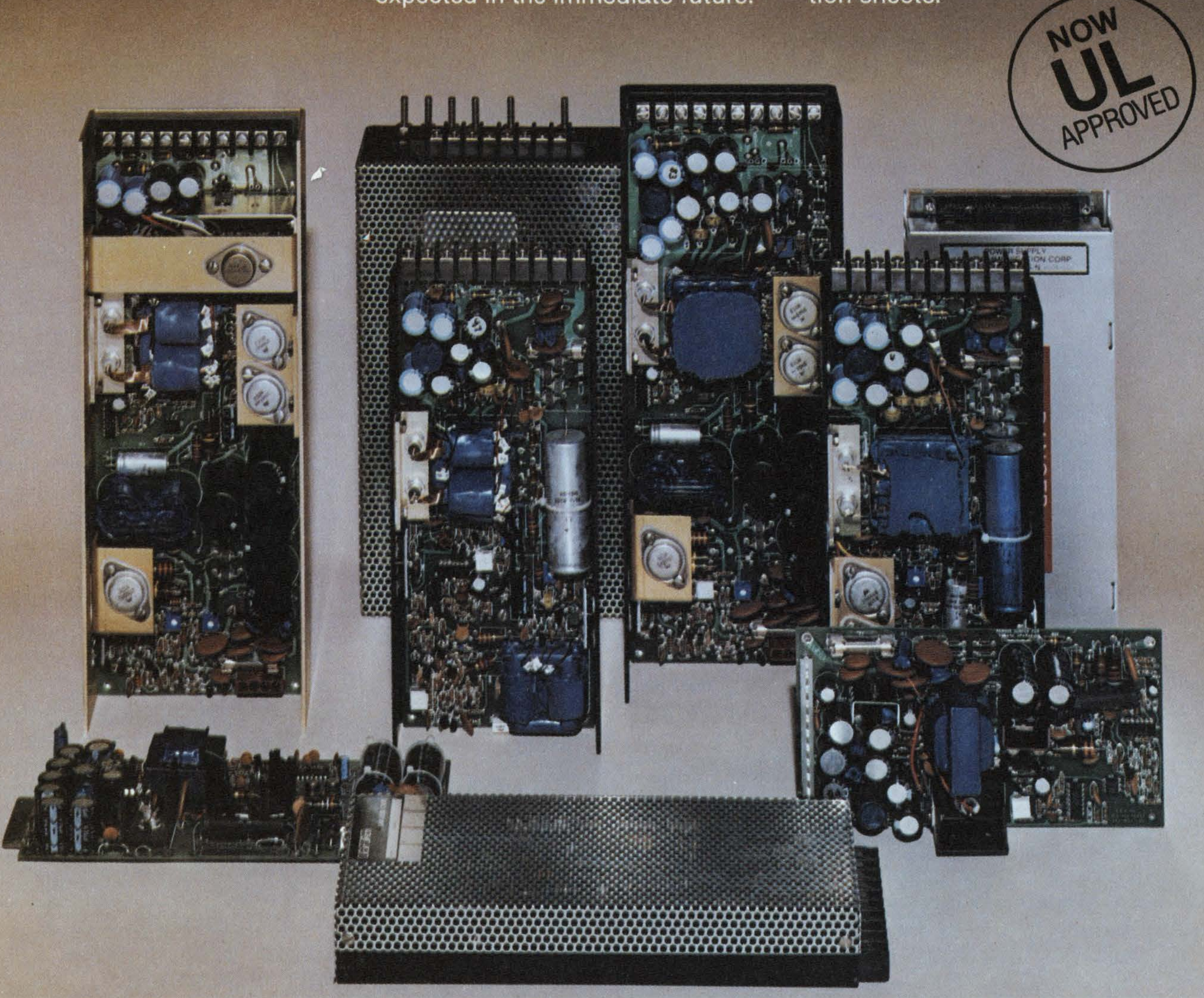

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The Pros And Cons of GCR

There is some question today about slower speed GCR tape transports. This question concerns whether it is presently possible to do GCR below 50 ips, and maybe even 75 ips, due to the required tape velocity over the heads in order to achieve an acceptable signal-to-noise ratio. If this is true then streaming GCR transports may be impractical since the existing disk technology cannot supply data fast enough to maintain the tape transport's required data rate.

The encoding method used in GCR is NRZI. To make it self-clocking the data is encoded so as to guarantee that there will not be more than two consecutive zeros in the data stream of any one track. This allows PLL circuits to be used to separate the data. This encoding is accomplished by taking 4 data bits and encoding them into 5 serial bits. Within this set of 32 combinations there resides a subset of 17 combinations that when assembled serially will never have more than two consecutive zeroes. This supplies the 16 combinations which, when properly assembled serially, are used for unique flag characters (see Table 1).

Data Group/Record Group Translation

DATA	STORAGE/RECORD
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

When using the NRZI recording method the bit cell boundry is referenced across all nine data tracks; therefore the maximum density that can be achieved is limited by the skew of the tape path across the nine data tracks. Since any track can have an infinite number of zeroes (no transitions), a PLL data separator cannot be used, therefore NRZI is not self-clocking.

PE overcomes some of these problems by each track's bit cell boundry not being referenced to the other tracks. It is self-clocking. In actual practice the industry standard allows up to 4 bits of skew by providing 4 bits of buffering for each track. Since NRZI is recorded at 800 bpi, with allowance for less than one bit cell of skew, and PE is recorded at 1600 bpi with allowance of up to 4 bits of skew, PE can tolerate twice the skew distance of NRZI. PE normally can correct for one dead track, giving PE a higher data integrity than NRZI, plus twice the packing density.

—Allan Krosner, Executive Vice President, Distributed Logic Corp. (DILOG), Garden Grove, CA.

that is, if there is no transition when there should be—the data can be filled in by assuming the parity is correct and using the data in the other tracks. It should be noted that this is only usable in the case where one of the tracks definitely does not have transitions within the prescribed bit cell window. Parity errors due to problems other than dead tracks are not correctable. Also, a dead track can obscure the actual position of the postamble, and characters in the postamble can be read as data, giving incorrect results.

GCR formatting has added more error detection and correction than has been available before. Within the formatting of the records, two CRC characters and an Error Correction Character (ECC) are used. The ECC character, 8 bits long for every 7-character data group, can correct any single error within the data group. All two bit errors are detected and can be corrected with the aid of data from amplitude and phase error detectors in the formatter. The CRC characters add additional checks on the data after correction in order to increase confidence in the integrity of the data. The ECC scheme decreases the number of tries necessary to read marginal tapes and, therefore, increases the overall throughput of the system.

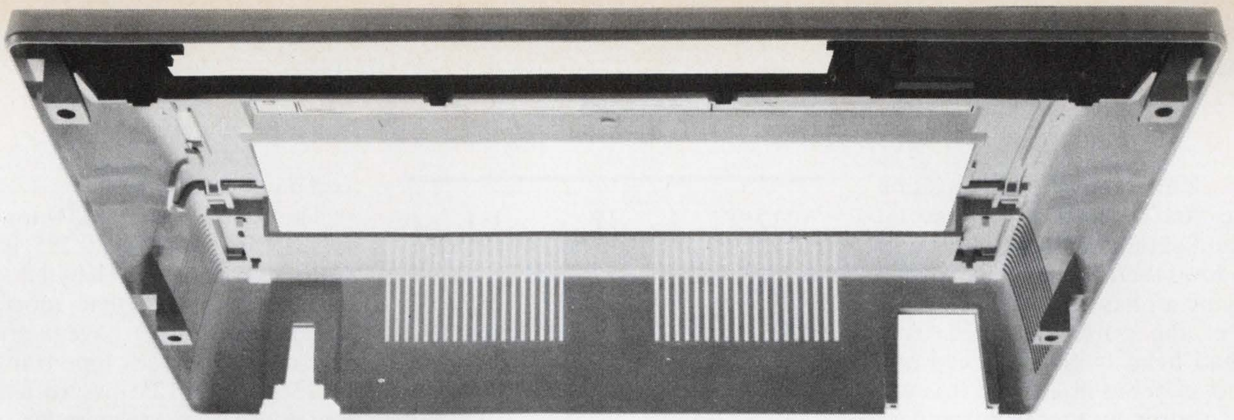
Resynch Characters Reduce Errors

PE recording only has formatting characters at the beginning and the end of the data record. Should a channel become dead in the middle of the record, there is no way to resynchronize the decoding circuitry for that channel until the next record. This limits the length of the records used, as the probability of an error within a record increases with the length of the record. Yet to take advantage of PE with its overhead of 0.6″ interrecord gaps and the characters in the preamble and postamble, the records should be long.

GCR has overcome this problem by imbedding resynch patterns in the middle of the data in the records so that the individual track decoders can resynch during the record, minimizing the probability of uncorrectable errors. GCR can, therefore, be used with high reliability for very long records, which is the most efficient way of utilizing tape.

Amplitude Calibration Improves Tape Interchangeability

In GCR, flux reversals occur only at the center of the bit cell and there are no other flux reversals.



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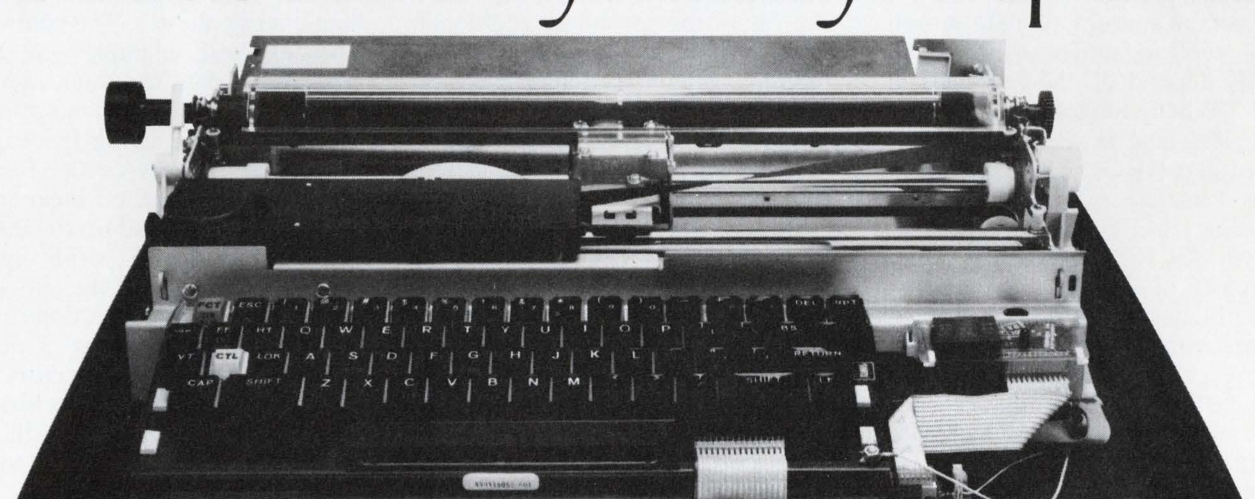

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The formatter checks the position of the flux reversal within the bit cell, and should it occur outside of a window, then the track is flagged as having a phase error. The amplitude of the pulses received from the read head is also checked and flagged as being in error if it is too low. To compensate for differences in tapes and read/write circuitry, each tape has an area at the beginning of the tape with a series of flux reversals in each channel so that the drive can calibrate its read circuitry before reading the data on the tape.

GCR Versus PE

NRZI is the oldest and the least efficient recording standard, and PE is the most popular recording method currently found on minicomputers. Therefore, a comparison between the most promising and the most popular, namely GCR versus PE, is in order.

Capacity. GCR holds 180 Mbyte of unformatted data versus 46 Mbyte for PE per 2400 ft. of tape. The actual amount of data stored on a reel in either density will greatly depend on the records size used. When longer records are used, less tape is wasted on inter-record gap (IRG). This is referred to as "storage efficiency." When recording in PE the IRG is 0.6″ and in GCR the IRG is 0.3″. Therefore, the "storage efficiency" is also higher in GCR.

Data throughput. Due to higher density of data and smaller IRG for tape transport at equal speed, GCR will provide a higher data throughput. Numerically, improved throughput is similar to improvements in capacity and is about 3.5–4 times higher.

Data integrity. Error rates are much lower in GCR than with PE: improvement by a factor of four in the rate of temporary errors per Mbyte of processed data can be realized. A 30% improvement in the rate of permanent errors can be attained in spite of the increased density of flux reversals.

Overall system improvement. All of the above advantages provide the computer with a high performance storage mechanism. Manipulation of large data files is now manageable with GCR systems. The time needed to read or write tape data is now decreased by at least a factor of 4. In the original introduction of GCR, IBM kept the PE as the second or additional density. Thus, it provided media interchangeability via 1600 bpi with older archival data, and a strong performance advantage via 6250 bpi, linking both the past and the future.

NRZI is the oldest and least efficient recording standard, and PE is the most popular recording method currently found on Minicomputers. Therefore, a comparison between GCR vs. PE is in order.

Price/performance. It is generally agreed that GCR has a 4:1 performance improvement over PE. Using Digital Equipment's price list as a guide for price comparison between GCR tape systems and NRZI/PE tape systems, one observes a ratio of close to 2:1. Therefore, one can conclude that price/performance shows a 2:1 improvement.

Mini GCR Tape Transports

GCR tape transports used on IBM and other mainframes operate at 200 ips and are large free standing boxes. The GCR tape transports currently connected to minicomputers are rack mountable and operate at speeds of 75 or 125 ips. The introduction of the mini transports by Storage Technology Corp. in 1977 and by Telex in 1978 at lower speed and lower cost made the attachment of GCR to minicomputers feasible.

The transfer rate at 200 ips GCR is 1.3 Mbyte/s and at 125 ips the transfer rate is 781 Kbyte/s. Considering the fact that most high performance disks have a transfer rate of 1.2 Mbyte/s, tape transports at 75 ips and 125 ips are a better match for most popular minicomputers.

Applications Of GCR

High data capacity per reel of tape—which in turn leads to high data throughput—makes GCR very useful in the following applications for minicomputers:

- High Speed Real Time Data Collection (RTDC)
- Data interchangeability with mainframes and with minis employed in RTDC
- Large disk backup
- Storage of large amounts of archival data.

Real time data collection. Examples of RTDC are data gathering in oil exploration, monitoring moving targets, and experimentation in high energy physics. The characteristics of these examples are large amounts of data at a high rate, often in cases where regeneration of the data, by repeating the experiment, may be very costly. For example, in the era of inexpensive oil, drilling was done up to 6000′ in depth. Today we drill up to 20,000′. Therefore, the information gathering must be done more accurately. This means a larger number of acoustic detectors and closer spacing of the detectors—in other words, more data. Gathering of such data is often done with a minicomputer.

Data interchangeability. Once the data is collected in the field and recorded in the GCR format, the data is often analyzed by minicomputers in a different location. Therefore, the minicomputer used in preprocessing must have GCR equipment. The other important aspect of interchangeability is with mainframe computers. This application of GCR is a direct outcome of acceptance of GCR on large mainframes and growth of minicomputers into the arena of mainframes.

Large disk backup. Today minicomputers have 1.2 to 2.4 Gbyte of disk storage. The trend is toward 600 Mbyte/spindle of fixed media. The only practical way to backup 1.2 Gbyte of storage is via GCR tape. In addition to previously mentioned reasons for using GCR, such as high data capacity and high throughput, long records of approximately 50 Kbytes of data are possible with GCR. Large records increase the tape storage efficiency, which is required for large disk backup.

Tape is the least expensive storage media. It should be mentioned that tapes are not only used in the disk backup as protection from head crashes; they are also used as a means of removal of inactive files for archival purposes and removal of data for transfer to other locations.

Large amounts of archival data. Two applications fall into this classification: First, when large data files are stored for archival purposes, the time to copy the data is much shorter and the amount of tape (as well as shelf space) is much smaller when GCR is used. Second, some "pre GCR" era archives are so large (millions of tapes) that users are adding GCR equipment to their minicomputers to convert the old 800/1600 bpi to the new 6250 bpi.

Future Developments In GCR

In the next 12–18 months we will see slower speed GCR transports designed to operate at 45 ips. The expected cost of these transports is about 35% lower than current equipment. These tape transports probably will be operating in Start/Stop mode. Another parallel development will be streaming GCR transports. This product is also about 1 year away.

A third progress is in the development of VLSI chips primarily for GCR formatters. This development, in my opinion, is the most significant one because it will increase the reliability and lower the cost without sacrificing any performance/throughput. All of these events are currently in progress at different companies. □

System Modeling For Thermal Design Of Supplies And Systems

by Edward A. Wilson

This modeling approach examines chip packaging effects on power supply integration and design.

More careful design, selection and application of power supplies and systems is necessary. This is particularly true with respect to system modeling for thermal design. It was the introduction of and growing use of control ICs in switching power supplies and improved, discretely-mounted components in both linear and switching supplies that made these thermal considerations more critical. Principles discussed in this article can be applied to any temperature-critical situation by analogy.

The Temperature Chain

When addressing the overall cooling of power supply ICs or discretely-mounted power supply components, it is convenient to break down the ultimate concern (junction or heat source temperature) into a set of links in a chain: $T_j = T_a + \Delta T_a + \Delta T_{c-a} + \Delta T_{j-c}$. In this formula, T_j is junction temperature, T_a is ambient air (or even water if that is the coolant), ΔT_a is temperature rise of the air as it passes over heat sources preceding the item of interest, ΔT_{c-a} is case-to-air temperature drop and ΔT_{j-c} is junction-to-case temperature drop.

Although there is an interaction between ΔT_{c-a} and ΔT_{j-c}, for air cooling the interdependence is weak (Reference 1) and the advantage of using the temperature chain in defining and developing system cooling makes it desirable to treat each link as reasonably autonomous. Therefore, we will divide our discussion into two sections, plus a section showing how the temperature chain is used.

Edward A. Wilson is a recognized authority on thermal design at Honeywell, Box 6000, Phoenix, AZ 85005.

Junction Temperature

From the viewpoint of the cooling designer, this is a sacred quantity. Mystical gurus make a pronouncement that a given temperature may not be exceeded, and the designer must see that the requirement is met.

Even though the temperature is set by outside forces, it is worth-

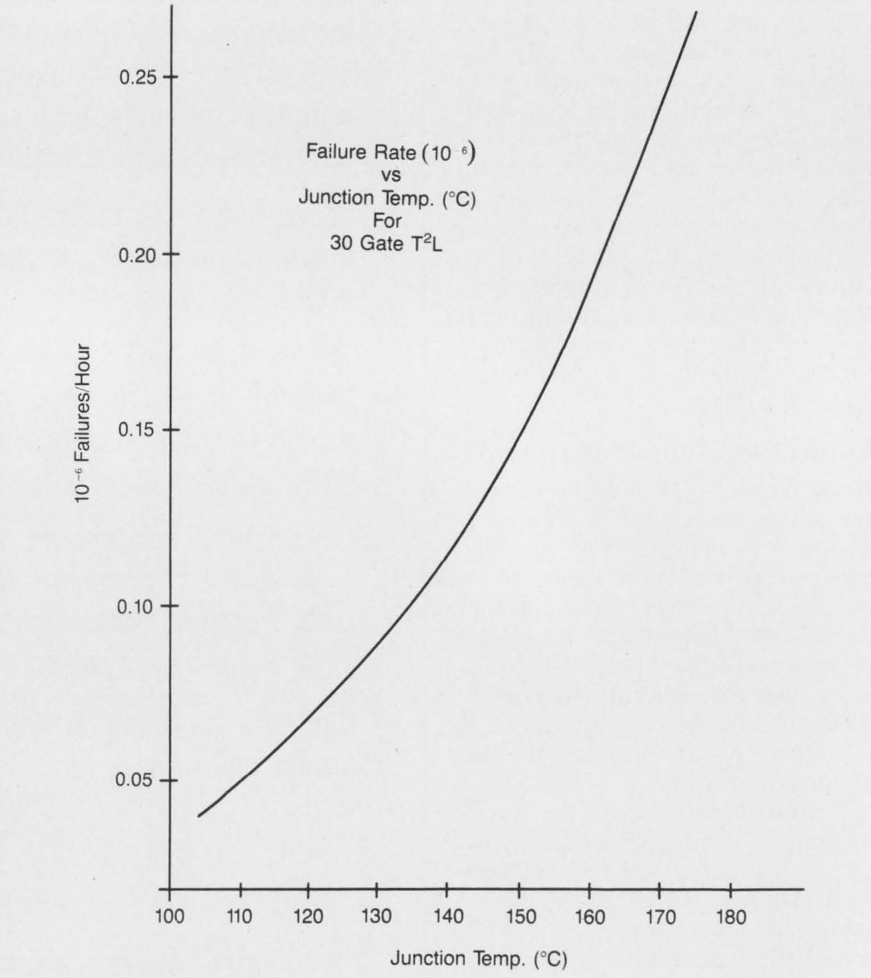

Figure 1: For devices with a high saturation temperature, long term life becomes a deciding factor in setting the allowable junction temperature. The curve above indicates how failure rates accelerate with junction temperature.

while to understand why various values are chosen. The most frequent criterion is lifetime: how long a type of component may sustain a given temperature without a certain percentage of that type falling. If the wording of the preceding sentence sounds awkward, it is because it is intended to convey the fuzziness of the number. Under this criterion, a clear, sharp distinction between good and bad does not exist. In frequent cycles of hysteria, with engineers running the halls crying that the sky is falling because a junction temperature will be 126°C instead of 125°C (under worst case conditions), one gets the impression that everything will fail. Rather, the situation is that the frequency of that type of component failing will probably have increased.

Unfortunately, the lack of the sharp edge of pass/fail places an unwarranted burden on the cooling designer. From one side, the pressure is to keep up the reliability by holding firm on junction temperature. From another side, the pressure is to use less expensive and/or more available parts and not be so strict on the junction temperature (after all, what difference does a few degrees make?). From the top comes the pressure to get a product out the door and to the customer.

Since many aspects of the design will be imposed from outside sources (cost, component availability, and junction temperature limit) the designer should base the pass/fail condition on the technical input only and not bow to the political pressure. That should become someone else's headache, and the burden to overrule technical data must be passed upward to the appropriate management level.

As an example of the influence of temperature on lifetime, **Figure 1** is presented. This figure is for a 30– gate TTL IC chip. Below about 100°C, the curve is relatively horizontal and above 170°C, it becomes relatively vertical. If the design limit is 125°C, the failure rate will be 7.6×10^{-8} chip failures per hour. A change of 1°C will have an imperceptible effect on the failure rate while a 10°C increase will increase the failure rate by about 70%. If an orderly design process with some semblance of control is to prevail, a design limit must be defined and once defined it must be observed if the projected failure rate goal is to be met.

A second criteria for junction temperature limits is poor performance. The Honeywell CML circuit set is a good example of this. The circuit design is such that if the chip gets too hot, transistors will "saturate" with charge and not switch fast enough. In this case, the computer does not compute. But, if the temperature is reduced, the machine will work again. This type of temperature limit is more satisfying from the standpoint of a pass/fail condition although it must be recognized that the junction temperature during a test will not always produce such a failure.

In any case, whatever the criteria, the junction temperature will be treated here as a number provided by "experts" and not subject to challenge by the designer.

Ambient Temperature

As with the junction temperature, this is another given number. It should be specified by a design standard as an envelope on a psychrometric chart as in **Figure 2.**

The exception to T_a being the ambient air would be if pre-chilled air or another coolant were used. In such a case, T_a would be the coolant temperature preceding any heat source and not governed by the class of room. However, the room conditions must still be considered from the standpoint of the entire system. For example, if pre-chilled air is used, the cooling coil should not operate at a temperature which would permit condensation to take place under the specified design conditions. If the room in **Figure 2** is required, then the dry bulb temperature of 28°C and wet bulb temperature of 26°C yields a dew point of 25.5°C. From this example, unless other means are employed to solve the condensation problem, even pre-chilling the air can only help by about 6°C over the worst case dry bulb temperature of 32°C.

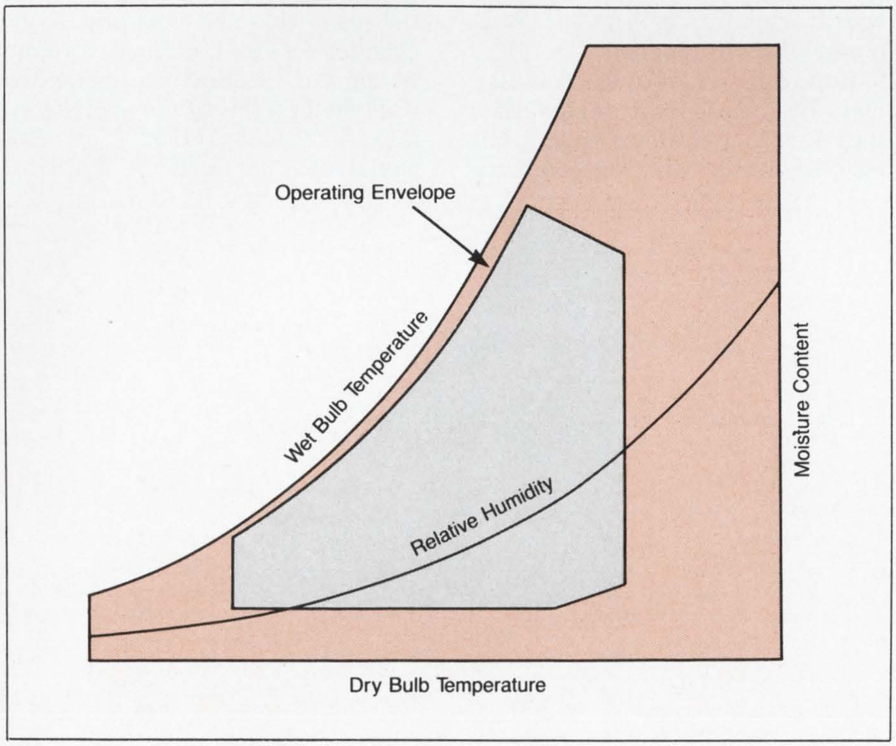

Figure 2: Just specifying an operating temperature is not adequate, the total description should be an envelope on a psychrometric chart.

Air Temperature Rise

The fundamental equation is: $\Delta T = W/c_pM$. In this equation, W is heat input (actually, power is used), c is specific heat of air, ρ is density of air and M is flow rate.

At sea level, the density of air at a typical room temperature is about 0.0725 pounds per cubic foot. The specific heat is 0.24 BTU per pound–°F. Both density and specific heat vary with temperature, but the range of air temperature used in typical computer cooling is small enough to use these values. For ease of use, the specific heat needs to be converted to units which are more consistant with computer designs. Also, the density is altitude-dependent, and with the resulting data: c is 7.6 W minute/lb°C, ρ is 0.0725 lb/ft^3 (sea level) or 0.7861 x .0725 = 0.057 (8000′). Then, at these two altitudes ΔT is 1.81 W/M (sea level) and ΔT is 2.31 W/M (8000′). The 8000′ altitude is representative of a high-altitude ground installation.

It is worth noting the influence of air flow on the design (the effect of velocity is covered in the section dealing with ΔT_{c-a}). Since ΔT_a is simply inversely proportional to the air flow, if a problem exists in which a component is 20°C too hot then just increasing the air flow will probably not solve the problem. For example, assume that ΔT_a is already 20°C; obviously a doubling of the air flow (achieved by opening the space between the boards and maintaining the same velocity and pressure drop) will only account for a 10°C improvement. By this very simple example an important, yet frequently overlooked point is to be made. In most of the problems encountered in computer cooling, the solution lies in the proper design of ΔT_{c-a} and ΔT_{j-c} with the total air flow (as related to ΔT_a above) becoming important only as ΔT_{c-a} and ΔT_{j-c} are reduced to levels comparable to ΔT_a. An auxiliary point is that the cost (in size, money, noise, etc.) of doubling the air flow would not yield a very worthwhile payback (10°C or so).

Recognition of the limited gains which can be achieved by an air flow increase can direct otherwise wasted efforts into areas of the cooling problem which could yield more fruitful results.

Recognition of the limited gains which can be achieved by an air-flow increase can more fruitfully redirect otherwise wasted efforts.

Case-To-Air Resistance

For both ΔT_{c-a} and ΔT_{j-c}, it is useful to consider the product of power and resistance as the appropriate ΔT. This allows studying various factors affecting the resistance and then just scaling by the power to consider the overall system cooling problem. Using the information in the preceding section with an assumed requirement of operating at 8000′ allows writing the temperature chain as: $T_j = T_a + 2.31 (\Sigma W/M) + W (R_{c-a} + R_{j-c})$. Here, ΣW is power input into air stream from preceding heat sources, M is flow rate of air stream (not full board of entire cabinet) and W is power of the component.

If the interaction of R_{c-a} and R_{j-c} may be considered insignificant, then the factors affecting R_{c-a} are associated only with the geometry of the package and the properties of the air stream. In the simplest form, the resistance is the reciprocal of the product of h (coefficient of convection) and A (surface area of the package and/or heat sink).

First, the factors affecting h under forced convection cooling will be considered. The curve in **Figure 3** is typical for the range of velocities encountered in computer cooling and is useful for estimates prior to the always-required experimental determination of R_{c-a} (there is no adequate substitute for real numbers). The factor G is simply ρV (density times velocity), but for more frequency used units and at sea level: G = 4.3V, where V is in fpm. The convection coefficient obtained from the ordinate of the graph may be expressed in more familiar units by multiplying: (h/G) × G × .00366 = h (W/in^{2}°C).

As an example of how to use this curve, consider a package one inch long (in the direction of air flow) and a velocity of 500 fpm. G is 2150 or GL (since L = 1), h/G is 0.0032 (from curve) and h is .025 W/in^{2}°C.

Of more general interest, however, is the relationship of the ordinate to the abscissa. The slope of the plane curve is –0.48 and of the cylinder is –0.41. Using a round fraction of ½ allows expressing the ordinate in terms of the abscissa as: $h/G = 0.1485 (GL)^{-0.5}$, or (for familiar units): h = 0.00112

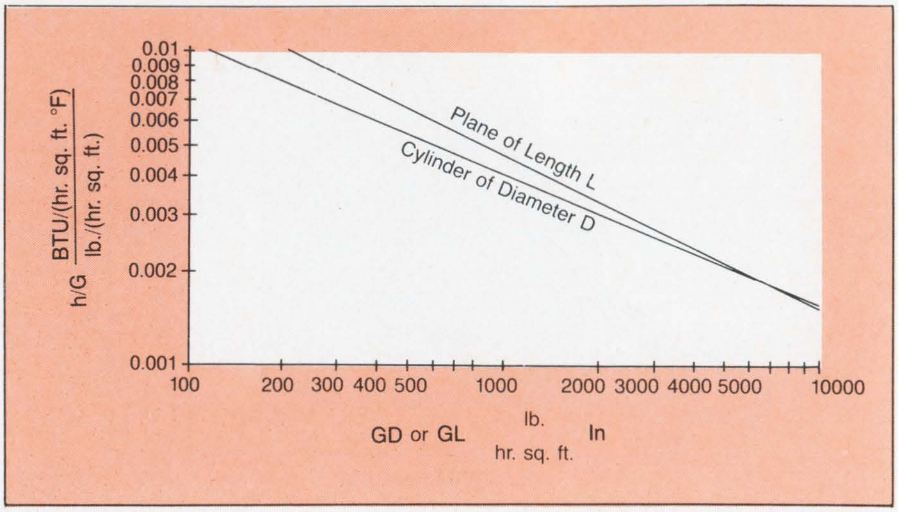

Figure 3: For both pins and planes, the heat transfer coefficient of convection has almost the same relationship with velocity. Based on the figure above, h αSQRT (V) is adequate for modeling purposes.

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$\sqrt{\rho V/L}$ (W/in^2 − °C).

This relationship will generally provide conservative values of h in the absence of other factors such as obstructions, pin fins, and other items which will affect the stream line. Of more importance to this development is the character of the equation rather than the values obtained. In terms of R_{c-a}: $R_{c-a} \propto \sqrt{L/\rho V}$ is the relationship.

The maximum effect altitude will have on the case-to-air resistance will be the square root of the relative density between sea level and 8000′. This is $\sqrt{0.7861}$, or 89% of the sea level determined h. Depending upon the absolute value of R_{c-a} as experimentally determined, this 12% reduction may or may not be of importance. For example, if R_{c-a} is 20°C/W, then the correction of 2.4°C/W for 8000′ is probably within the experimental accuracy.

The R_{c-a} dependence upon velocity is also approximated by the inverse of the square root. But because the range of velocities is greater, the importance of the relationship is greater. Possible velocities range from 200 fpm to 2000 fpm with 1000 fpm as a more likely maximum at component locations (ignoring the localized "jets" at the metering plate). Over this ten to one range, the theoretical decrease in case to air resistance would be about 68% if there were no other influencing factors.

Now notice that as GL or GD increases (due to increasing velocity) the curves merge and the extremely high velocity represented by GL = 10,000 will yield for the practical limiting velocity of 2000 fpm: GL is 10,000, G is 8600 (V = 2000 fpm, h/G is 0.0015 and h is 0.047 W/in^2°C.

Quite simply put, get enough area and the payback will be worthwhile.

In actual practice, 0.04 to 0.05 is about the best which could be achieved by any heat sink design which also has a useful area. For example, a very short fin (0.1″ in the air flow direction) may yield a high h, but there will not be enough surface area to make use of the high h.

A word of caution about the use of **Figure 3.** As long as the bodies are far enough apart to avoid affecting the air stream of each other, **Figure 3** is reasonable for early design estimates. However, as the fins, pins, or whatever form an interfering pattern, other correlations must be used.

These may be developed experimentally, or sometimes found in reference sources such as the General Electric Heat Transfer Data Book. In any case, an h between 0.04 to 0.05 will still be found to be the practically achievable limit.

In the preceeding example the subject of area was touched upon briefly.

Recall that: $R_{c-a} = 1/hA$. In the foregoing discussion on the factors affecting h, it was discovered that they all have a square root (or inverse square root) influence on h. In view of this relative (to a linear relationship) insensitivity and the practical limitations of significantly changing velocity, length, etc., the inverse linear relationship of R_{c-a} to area makes that an attractive candidate for design effort.

Quite simply put, get as much area as possible and the payback will be worthwhile. Consider what has been discussed so far in the temperature chain. Since T_j and T_a are prescribed, the only variables which the designer may manipulate are ΔT_a and ΔT_{c-a} (or R_{c-a}). If a situation exists where both ΔT_a and ΔT_{c-a} are near the same value (say 20°C), then a doubling of heat sink area could reduce the required air flow by the following approximation: $R = \Delta T_a + \Delta T_{c-a}$. Then, double the area and keep R constant, so: $R = \Delta T_a (V_1/V_2) + (\Delta T_{c-a})(\sqrt{V_1/V_2})$; and, since $\Delta T_a \sim \Delta T_{c-a}$, the velocity (hence air flow) ratio becomes 1:4. This means that the original heat sink would have required 40% more air than the new heat sink with doubled area. This reduction in air flow could be important from the total system cooling standpoint. Of course, the payback in terms of air flow, noise, size of blower, etc., is dependent on the relationship of the links in the chain and proportion of the machine air flow affected by the change in area (i.e., is it one isolated location or is it replicated many times?).

In the case of power supply components which are discretely mounted, increases in area can usually be achieved as long as the effect of tight gaps on reducing h is recognized and compensation (such as even larger increase then the first order approximation would suggest) is made.

Unfortunately, off-the-shelf DIPs present a problem. The area is defined by the standard part. If a particular chip is too hot, it might be tempting to add a heat sink to that package alone since it would be too expensive to add a heat sink to every package. But this will adversely affect the air stream and cooling of packages downstream from the package of interest.

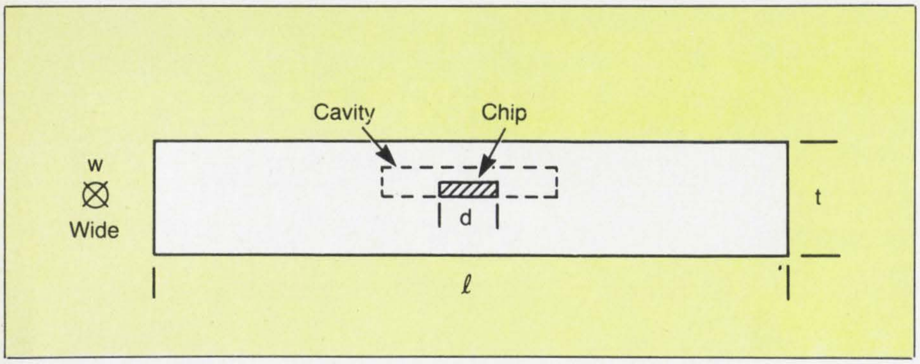

Figure 4: Simplified model to show the important factors in junction-to-case resistance.

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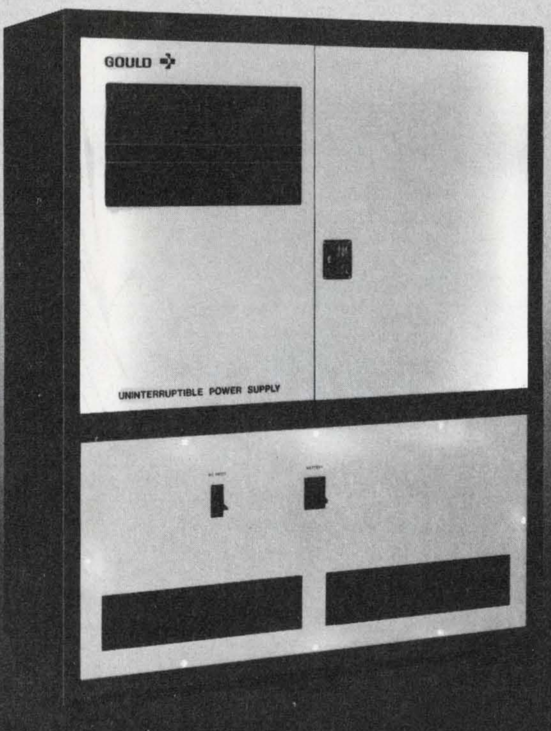

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Alas, the possible cure-all is foiled by the real world. In fact, the surface area is usually dictated by manufacturing considerations. By mounting a DIP close to (but not touching) the printed circuit board, the bottom surface is for all practical purposes lost as convective area. Even locating a low profile package behind an obstruction such as a capacitor will adversely affect the local velocity and may be viewed as effectively losing area that can not have the design point coefficient of convection applied to it. However, in new packaging designs, and non-DIP situations (such as power supply components) the principle of designing for maximum area consistent with the relative values of the links in the chain and cost and space is still valid.

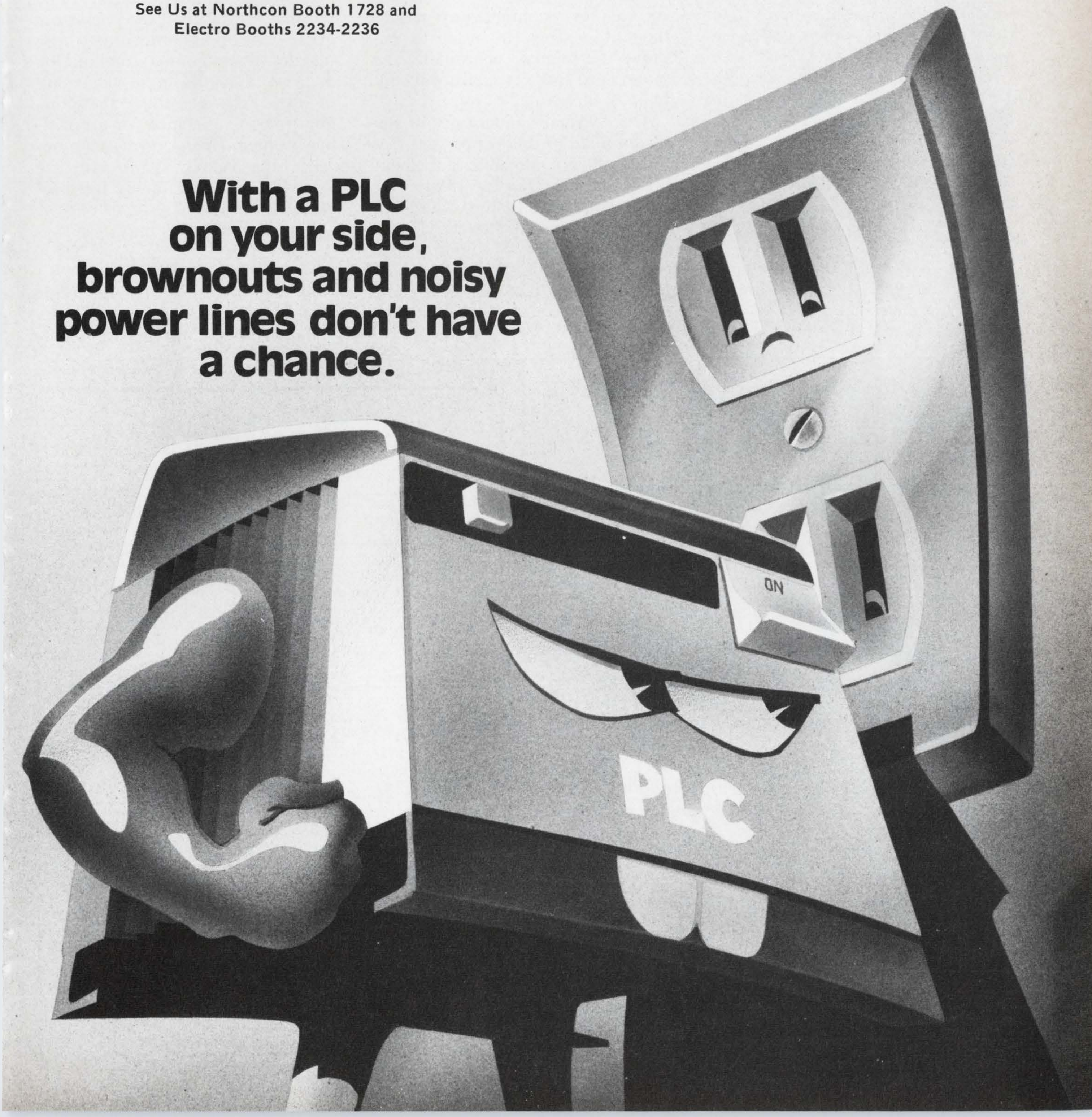
Junction-To-Case Resistance

For components such as power diodes, SCRs, etc., the vendors' specification will hopefully provide either the junction-to-case resistance or the maximum allowable case temperature. The cooling designer has no control over the internal design of such components and therefore, this becomes another given value.

The same situation (no control) exists for off-the-shelf DIPs. However, with the variety of possible vendors and their packaging methods, it is sometimes possible at least to specify acceptable and unacceptable sources and/or package design/materials. With this in mind, it is worth considering the major factors affecting R_{j-c}.

The over-simplified model in **Figure 4** may be used for this purpose. The heat transfer from the chip to the convection surface may be roughly divided into two steps. First the heat must leave the chip and spread downward and outward into the package. If the chip is encapsulated by the package material (as in most plastic packages), it may also spread upward and outward. Then, the heat will travel down the length of the package as it is also convected away.

This series resistance may be approximated by: $R_{j-c} = t/[2k(d+t)] + l/(4ktw)$. This shows that the fol-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lowing are the major factors in R_{j-c}: k is thermal conductivity of the package material, d is edge dimension of the chip, t is thickness of the package, l is length of the package and w is width of the package.

This equation for R_{j-c} should not be used to calculate values for design purposes because of the gross approximations made in the model. However, it may be used to demonstrate the relative influence of the major factors.

Consider a 14-pin DIP and a 40-pin DIP. Typical dimensions in inches for 14- and 40-pin DIPs are: d (0.1″, 0.15″), t (0.15″, 0.15″), l (0.8″, 2.1″) and w (0.3″, 0.6″). Substituting into R_{j-c} yields the following: For a 14-pin DIP, $R_{j-c} = \frac{1}{k}(3 + 4.4)$; for a 40-pin DIP, $R_{j-c} = \frac{1}{k}(1.7 + 5.8)$.

Notice that while the term containing the chip size contributes less to the resistance than the second term, it is still of importance.

Vendors' values are of little help in finding the junction-to-case resistance for high power chips.

As vendors continue to reduce their chip sizes (in order to improve the number per wafer), the junction-to-case resistance will continue to increase.

The thermal conductivity of the material is the most important factor of all. For alumina, k is about 0.7 W/in °C. But for plastics, it may vary from 0.01 to 0.1 and still not be confined by that range. Obviously, using a 1 W chip in a very poor plastic package could yield a 125°C junction temperature even if the package were frozen in an ice cube.

For this reason, limitations must be placed on the vendors and application rules for chips must be disseminated to logic designers. Also, a quality control test program is mandatory for both qualifying the vendors for each chip type and then checking for compliance on each shipment of parts which could cause a problem.

In some vendors' catalogs, the thermal resistance of the package is given either as junction-to-air, junction-to-case, or a combination of these. Usually, these values are of little help in finding the junction-to-case resistance for a potential problem (high power) chip because the values are worst case values. Hence an in-house test program is mandatory.

The Noise Relationship

Due to the restricted length of this article, the development and detailed discussion of the noise prediction equation below cannot be presented. It is treated in detail in **Reference 2.** For a given cabinet configuration and blower type (centrifugal, tubeaxial, etc.) the noise power emission level may be predicted by: $L_{NPE} = K_C + \log M + 2 \log P + K_B (1-R)$, where: M = airflow in cfm and P = pressure drop in inches of ratio. K_c, K_B, and R are associated with the cabinet and blower performance and are beyond the scope of this article.

In the comparison example below, it will be assumed that the same cabinet will be used and that for both air flows the same type of blower is used but in both cases the size and speed are changed to have the same efficiency (called merit ratio in **Reference 2**). This reduces the prediction equation to a relative equation of: $\Delta L = \log (M_2/M_1) + 2 \log (P_2/P_1)$.

Comparative Example

Consider a hypothetical design in which the junction temperature of a set of 2 W chips must be kept below 100°C for an inlet air of 30°C at 8000′. For simplicity, all chips will be assumed to have the same power. Furthermore, test results for a proposed package have shown that the junction-to-case resistance is 5°C/W and at 1000 fpm the case-to-air resistance is 20°C/W at the last package in a row of ten packages (pressure drop of 0.05″ of water). The temperature chain becomes: $T_j = T_a + \Delta T_a + \Delta T_{c\text{-}a} + \Delta T_{j-c}$; or, $100 = 30 + 2.3\ (2 \times 9)/M + (R_c/\sqrt{M} + 5)$ W, and: $R_c = 45$ for an assumed flow area of 0.005 square feet. Then, $100 = 30 + 41/M + 90/\sqrt{M} + 10$ yields: M = 3.5 cfm or V = 700 fpm.

Now, assume that the package design is changed to increase the connective surface area (add a heat sink) such that at 1000 fpm, R_{c-a} = 4°C/W (pressure drop now 0.5″ of water). This leads to $R_c = 9$ and if the rest of the data remains the same, M = 1 cfm or V = 200 fpm.

The next step is to find the total cabinet pressure drop. If the cabinet ducts, exclusive of boards, have a pressure drop of 0.2″ of water at 500 cfm, then the characteristic may be approximated by: $P_c = 8 \times 10^{-7} M_t^2$, where M_t is the total air flow.

Since the cabinet duct pressure drop will be due to mainly momentum change and the board pressure drop due mainly to viscous effects, the total pressure drop may be represented by: $P_t = 8 \times 10^{-7} M_t^2 + 0.01M$ (first design) $= 8 \times 10^{-7} m_t^2 + 0.1M$ (second design).

If there are 25 boards with 8 rows of packages on each board, then the respective pressure drops are 0.43″ of water and 0.13″ of water. The noise difference is: $\Delta L = \log (200/700) + 2 \log (0.13/0.43) = -1.6$ bels. This means that the second design is 16 dB quieter than the first design. It is worth noting that of the 1.6 bel improvement, two thirds is due to the pressure drop decrease, which of course is the result of so much less air moving through the cabinet.

Conclusion

The modeling approach described permits examining the impact of chip packaging on total system design, including blower requirements, relative noise levels, etc. Our example showed that the addition of a heat sink (extra cost) to a package design had a significant payback in noise reduction, which may only otherwise have been able to be later solved at a much greater cost.

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Select Conditioning Devices To Protect Your Systems

by John J. Waterman, Jr.

Balancing cost and protection to select the best trade-off requires that designers consider many factors.

Although today's computers, systems and peripherals use less power than their predecessors, this newer equipment is still very sensitive to power line disturbances. In fact, much of it appears more sensitive than the older equipment it replaces.

For the sake of comparison, the most typical configuration of IBM's Model 3081 uses an average of one-third the electrical power of the older 3033 mainframe. This is a 6-to-1 improvement in power-to-performance ratio, yielding annual electric power savings of up to $70,000. And, while the 3081 is the most visible of the newer computers, and one of the more effective in terms of energy savings, there are other mainframes, minicomputers and many new peripherals on the market which use significantly less power than earlier units.

For many years, most major computer manufacturers forced users to pre-condition power supplied to the larger mainframes by designing their power supplies to operate on 400-Hz power. This mandates use of an Uninterruptible Power System (UPS) or Motor Generator (MG) type device to convert the 60-Hz utility power to 400-Hz. In the process, the power is filtered, regulated and some "ride-through" of outages is provided by the batteries in the UPS or the MG's flywheel effect.

But no such protection was forced on all the peripherals, now increasingly power-sensitive due to more energy-efficient designs and more μCs and sensitive logic.

Thus, while only highly critical DP applications or very large computer centers installed power conditioning equipment in the past, such devices are rapidly becoming the rule, not the exception, for computer installations of all sizes and types.

While UPS and MGs have been the best known and remain the favorite devices employed, there are now many power conditioning devices of varying effectiveness. Before describing them, let's examine disturbances on power lines and the possible impact on computer installations. **Figure 1** presents a summary of occurrences detected on power lines in several studies. The weighted impact, while subjective, is intended to reflect the relative impact of the disturbance-type on a computer center. This column is more significant for selecting conditioning equipment than is the mere number of occurrences.

The most common devices available to eliminate these problems are:

Power Centers: Called Computer Power Centers, Portable Power Centers or Power Distribution Centers, these devices typically combine a high-quality shielded transformer with protective devices and flexible cables tailored to the users' equipment, all in a convenient portable package. These devices normally eliminate over half the common mode noise and some transverse mode noise. Many Power Centers also have high-voltage suppression built in. They provide no regulation or ride-through capability. They are usually installed because of their convenience, but do a little power conditioning.

Disturbance Category	Number of Occurrences	Weighted Impact	Type of Effect On Computers
Common Mode Noise Impulse	94	94	Possible Errors
Transverse Mode Noise Impulse	31	31	Possible Errors
Undervoltages	29	116	Errors/Shutdown
Very High Voltage Impulse	5	40	Damage
Overvoltages	14	84	Damage/Shutdown
Distortion (over 8%)	2	10	Errors/Damage
Frequency Shifts	2	16	Damage/Shutdown
Outages under 0.5 sec.	8	120	Damage/Shutdown
Outages under 1 sec.	7	105	Damage/Shutdown
Outages under 30 sec.	5	75	Damage/Shutdown
Outages over 30 sec.	3	45	Damage/Shutdown
Totals	200	736	Errors/Damage/Shutdown

Figure 1: Occurrence on power lines in industrial/commercial facilities shows number of and effect of each category.

John J. Waterman, Jr. is vice president of Marketing at the Programmed Power Div. of Franklin Electric, 995 Benicia Ave., Sunnyvale, CA 94086.

Power Conditioning Device	% Effectiveness*	Installed Cost**	Operating Cost†	Cost of Unresolved Power Problems‡	Total Cost ($1,000s)
High-Isolation Transformer	18%	13	9	364	386
Line Voltage Regulator (CVT)	38%	19	117	274	410
Power Load Conditioner	37%	20	21	277	318
Magnetic Synthesis	43%	24	74	250	348
Motor Generator	79%	37	88	94	219
UPS	100%	73	47	0	120

*Based upon the percentage of "weighted impact" (see **Figure 1**) reduction.
**For a 100-kVA system ($1,000s)
†Takes relative efficiency assuming a load which is 64% of rating (assumes 25% expansion capability and 80% usage factor) plus a 33% adder for heat removal, all at a forecast 10.5 cents/kW-hr/avg. for the next 5 years. Adds maintenance costs based upon quoted Mean Time Between Failures and maintenance fees.
‡Based upon remaining "weighted impact" occurrences at the ratio of 0.2 hours DP time/error (one weighted point), thus 3 hours for an outage-induced shutdown.

Figure 2: Effectiveness and cost of each power conditioning device varies considerably.

High Isolation Transformers: These are more exotic, triple-shielded devices specifically designed to eliminate all common mode noise. Again, no regulation or ride-through is provided.

Line Voltage Regulators: Most often constant voltage or ferroresonant transformers, these devices provide good steady state regulation, good transverse-mode noise elimination and fair common mode noise rejection.

Power Line Conditioners: Combine voltage regulation with a high quality or high isolation transformer to provide the benefits of both devices.

Magnetic Synthesis: Essentially a constant voltage transformer type of regulator with additional capacitors to provide more noise filtering and added dynamic range.

Motor Generator: A motor with a regulated AC Alternator providing both good voltage regulation and excellent noise elimination. MGs also provide some ride-through of outages (up to several seconds) due to the flywheel's inertia effect.

UPS: Combines a battery charger, battery bank and solid state inverter to provide precisely regulated and filtered power to the computer regardless of power line conditions.

Figure 2 compares these devices in terms of cost and effectiveness. The Power Center is not included, as it is usually required in any event. Effectiveness is added in by putting a value on the power problems which are not resolved. Clearly, the power environment varies for every data center, just as computer sensitivity to power problems varies between manufacturer and model. If you can't afford problems or downtime, a UPS may be your only choice. If you can't afford a UPS, consider a Power Line Disturbance Monitor to determine what kind of power problems you have. Then you can select a lower cost device to meet your specific needs. □

The power environment varies for every data center, just as computer sensitivity to power problems varies between manufacturer and model.

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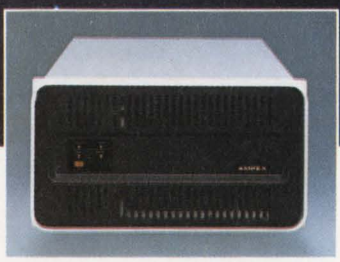

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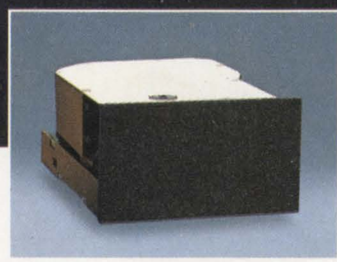

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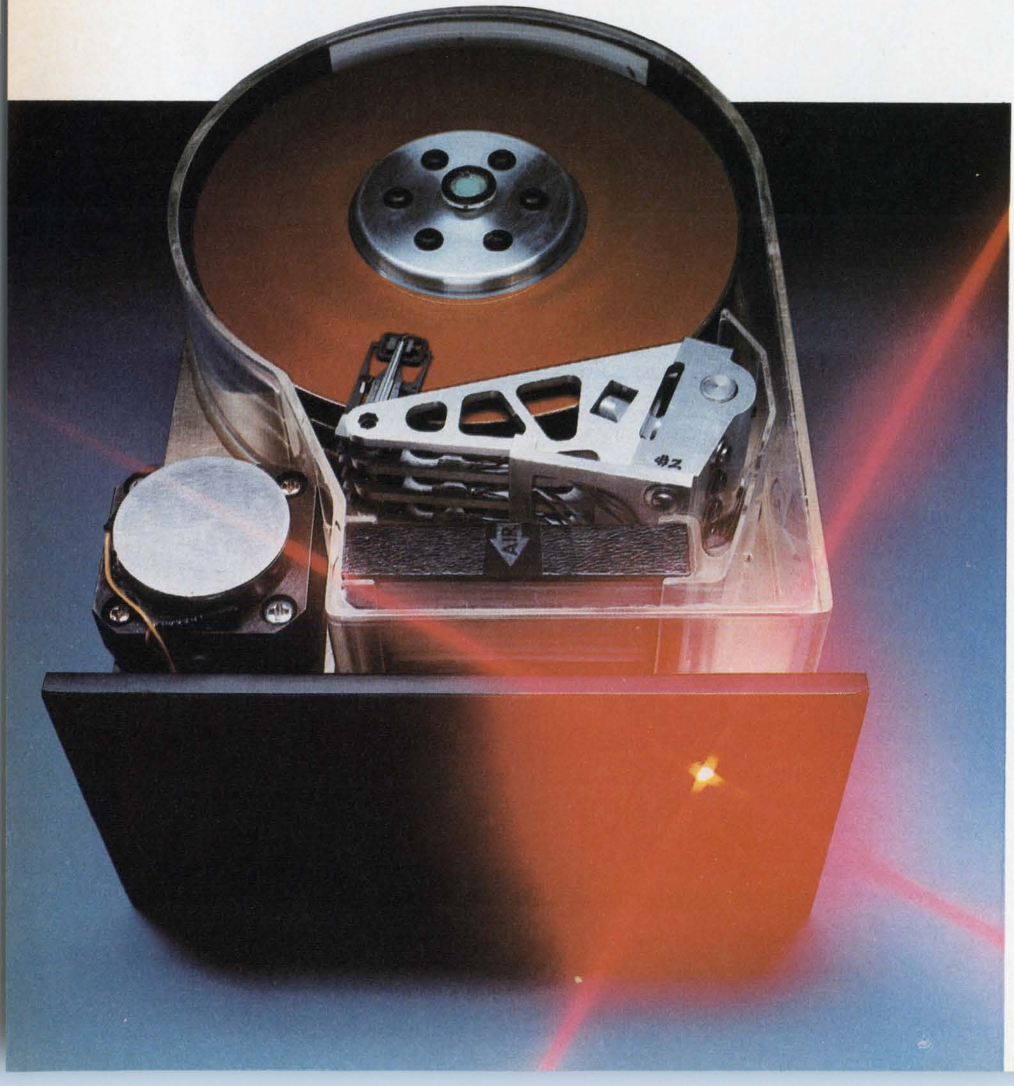
Disk Drive Advances Broaden Winchester Market

Increased capacity and performance are giving small Winchesters big-drive applications; simultaneously, significant price reductions are making large Winchesters suitable for smaller systems.



by Bob Hirshon

When product innovation accelerates to a certain level, product understanding and terminology take a beating. For example, small computers once could be defined "mini" and "micro." But as the technology grew, so too did kluges of Latin and Greek prefixes ("super-mini," "mini-micro," et al) to define it more precisely—until ultimately nearly everyone agreed the terminology defined nothing at all. With Winchester disk drives, rapidly increasing storage densities have made it impossible to pigeonhole a drive's application merely by its platter size. But just as buyers have been unwilling to abandon the concept of small computer categories, they cling to a neat heirarchy of disk drives based on platter diameter—even as technology advances turn that heirarchy upside-down.

Big Drives For Smaller Systems

Designers generally put 14" Winchesters at the top of that pyramid.

But high capacity 14″ drives are turning up in smaller packages with higher access times and, most importantly, lower prices. This puts them in the small system realm, where one multi-platter 14″ Winchester can replace several 8″ drives. A new drive from Alpha Data Inc (Chatsworth, CA) uses three platters to provide 80 to 100 Mbytes of storage, allowing average access times of under 20ms, and permitting access of contiguous 1 Mbyte sections of data (**Figure 1**). This 1 Mbyte access results from the logical cylinders being organized in 1 Mbyte increments.

The new drive, which Alpha Data calls the "Atlas," uses 72 heads (six surfaces, each with three moving head bars with four heads per bar) that are sealed, along with the platters, within a chamber. The company claims the sealed platters and heads require no periodic or preventive maintenance. Packaged in a standard 19″ rack mount, 7″ high and 24″ deep, the company's Atlas disk drive is expected to sell at $6K.

Winchesters vs. Floppies

8″ Winchesters similarly are finding themselves in unfamiliar markets, and now compete across the board, not only with 14″ drives, but with floppies as well. When 20 to 30 Mbytes of storage became available on low-cost 8″ Winchesters—compared to the 1.6 Mbytes available on floppies—many OEMs found Winchester upgrading irresistable. This is now the high-growth niche for 8″ Winchesters, and this is where at least three companies—Shugart, Memorex

Figure 1: Alpha Data's Atlas 14″ Winchester uses three platters and 72 heads in a sealed, maintenance-free chamber. Storage capacity for the $6K drive is 80 Mbytes to 100 Mbytes, with average access times of under 20ms.

and Quantum—are aligning their efforts. Floppy-compatible Winchesters offer an easy upgrade for systems currently using floppy drives for main storage. For systems using multiple drives, systems designers can replace a single floppy with a Winchester drive, thereby boosting capacity, and use the remaining floppy drives for Winchester backup. To make such upgrading simple, manufacturers are making their Winchester disk drives resemble the floppies they're intended to replace in physical, interface, and power supply characteristics. There is cause for "caveat

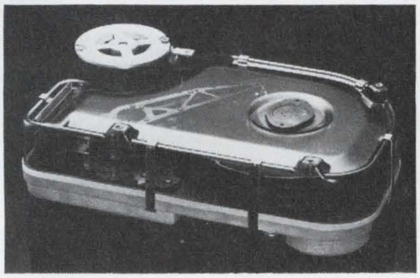


Figure 2: Quantum Corp. announced the Q2040, a 40-Mbyte version of its Q2000 series of 8″ fixed disk drives. The Quantum family, available in 10-, 20-, and 30-Mbyte versions, as well as the new 40-Mbyte Q2040, is fully compatible with the industry-standard Shugart Associates SA1000.

emptor" here: according to a *Digital Design* reader survey, at least one manufacturer sells drives designed to fit into the mounting space of an 8″ floppy drive, but which require external shock mounts, completely negating the original design concept.

Capacity Key Consideration

Capacity is a key factor in the selection of Winchesters; in fact, among the readers we surveyed, capacity was second only to reliability as a reason for selecting a particular drive. Capacity is the key feature of a drive recently introduced by Quantum (**Figure 2**). Their latest entry provides up to 40 Mbytes of storage in an 8″ floppy-sized case. It uses a rotary moving coil actuator to boost track density and lower access times (60ms for the 30 Mbyte model). The actuator has an optical encoder for referencing track locations which, the com-

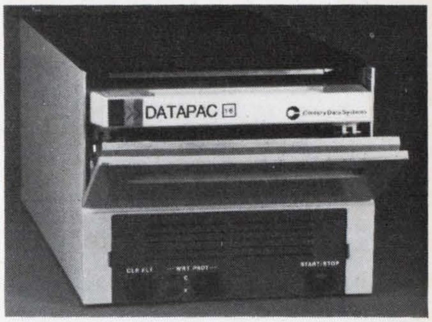


Figure 3: Century Data Systems' entry into the 8″ Winchester market, designated the C2048, has 16 Mbytes of removable and 32 Mbytes fixed storage. The C2048 offers high performance and capacity and low physical space requirements, power consumption and cost.

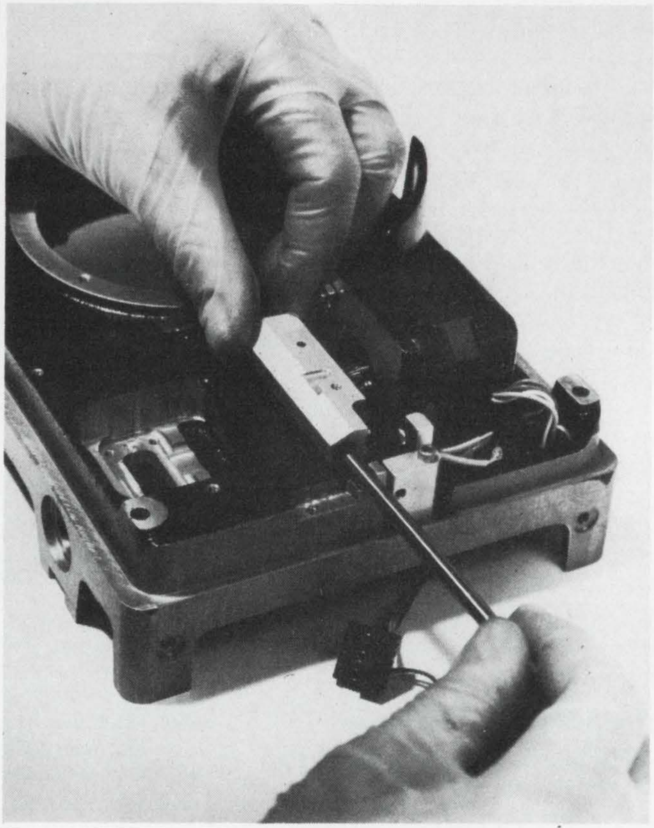
pany claims, is accurate to over ten times the track density of Quantum's present line, "leaving considerable room for growth of the family to higher track densities." To keep positioning accurate under varying temperature conditions, an on-board μP reads track location information encoded on the disk surface and compares it with positioning data from the optical encoder.

Backup Problems

For small systems, Winchester backup remains a key problem. Tape cartridges are probably the most cost effective media, but the user has to pay for the extra drive devoted solely to backup. Floppies are common backup choices, simply because they're familiar and have a huge customer base already. But in many applications, they become awkward, limited as they are by their lower capacity.

One alternative is the removable Winchester cartridge. Century Data Systems (Anaheim, CA) have recently introduced a removable 8″ cartridge drive (**Figure 3**) and Western Dynex and DMA both offer 5¼″, 5 Mbyte removable cartridge Winchester disk drives (**Figure 4**). One problem with these drives is high media cost ($85 per cartridge); the cartridges aren't, nor are they likely to become, cheap enough for applications with large storage requirements. Lack of cartridge standardization is another potential problem, but this could be averted if industry sup-

5-¼″ Winchester Employs Rack and Pinion Actuator



Small Winchesters, as they mature, are benefitting from the technologies used in 14″ drives. Rack and pinion actuators, for instance, have been used for years with large disk drives, providing numerous benefits. The rack and pinion permits multiple resolutions of the stepper motor, presents no problem in designing for compactness, is easy to assemble, inexpensive to produce and sturdy enough to be relatively immune to damage during assembly and shipping.

Miniscribe used aluminum and steel rack and pinion actuators on their latest 5¼″ drives for several reasons. Because the rack is made of aluminum, it does not contribute to any thermal off-track. The pinion gear is hobbed directly into the stainless steel stepper motor shaft; since the pinion contacts the rack on a plane perpendicular to the movement of the carriage, it also does not contribute to thermal off-track. In addition, the use of aluminum and stainless steel reduces the wear factor to the point at which none is discernable well beyond the expected life of the drive, according to Miniscribe. The dependability of rack and pinion positioning accuracy, repeatability, durability and longevity has been previously established by IBM in their 1311, 2311, and 2314 drives.

The drive's high-track density capability (402 tpi) was achieved by making the pitch diameter of the pinion gear relatively small (0.158″). This technique also contributed certain side benefits: because the pinion diameter is so small, the stepper-motor holding force is multiplied (12 ounce/inch of stepper motor holding force translates to 9.5 pounds of holding force in the direction of the carriage movement). This factor enhances both the accuracy and repeatability of the drive, and also makes it resistant to external shock and vibration while in operation.

ports the proposed ANSI cartridge standard now under consideration.

Early Intros

Because Winchester technology advances so rapidly, manufacturers are under considerable pressure to be first with their product, lest they miss the boat. The inevitable result of this pressure is early product announcements—and disgruntled OEMs who can't get delivery on the new drives they've ordered. This hurt the early growth of 5¼″ drives, and it's likely that the same will occur with upcoming 3″ drives.

When questioned about his company's 3″ hard disk drive program, one spokesman with a major disk manufacturer would say only, "When our 3″ hard disk drive enters the marketplace, it will create a sensation." Plainly, manufacturers are unready to reveal anything except their high expectations with regard to their 3″ disk programs.

Despite the lack of hard data, it's only natural that speculation should be widespread about a technology whose impact could be "sensational." One key question concerning OEMs who design small systems is "How will 3″ Winchesters impact 5¼″ Winchesters?" This is being asked even as the question "How will 5¼″ Winchesters impact 8″ Winchesters?" is waiting for an answer. Market indicators point to a large demand for the drives, as small systems demand increases, especially for business applications. Additionally, hikes in disk capacity may put 3″ Winchesters squarely into the performance slot originally intended for 5¼″ drives. Active research and development by the major manufacturers is the most telling indicator, and suggests that 3″ drives may become the small system standard, kicking 5¼″ Winchesters into a higher capacity niche just as they're getting a firm foothold in the small system marketplace.

Reliability Chief Concern

Because of the many bad experiences caused by the introduction of products that weren't ready for the marketplace, reliability has become the chief concern of OEMs specifying disk drives. Our survey of disk drive purchasers revealed

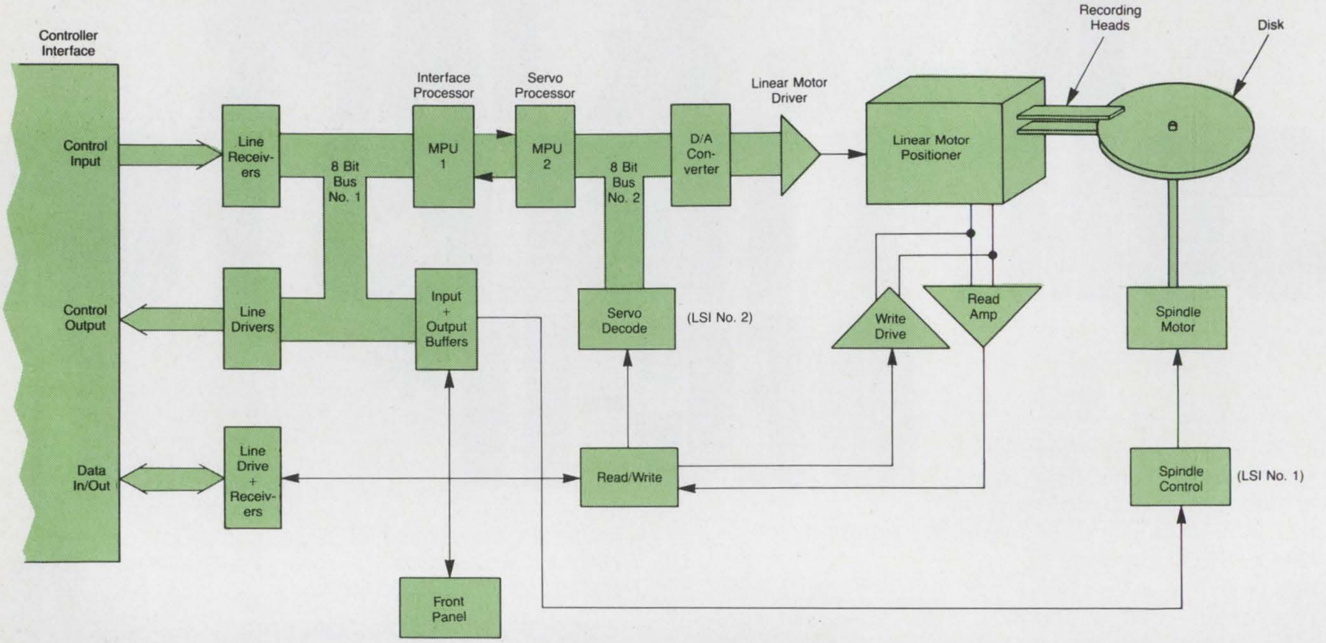
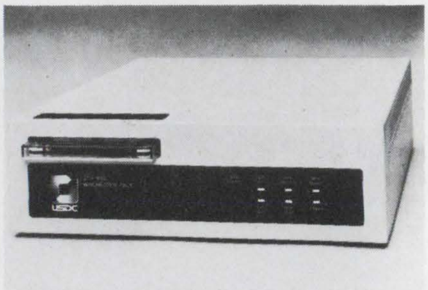


Figure 4: Removable 5¼" Winchester disk cartridges have applications in small computer systems for business, local area networks and word processing.

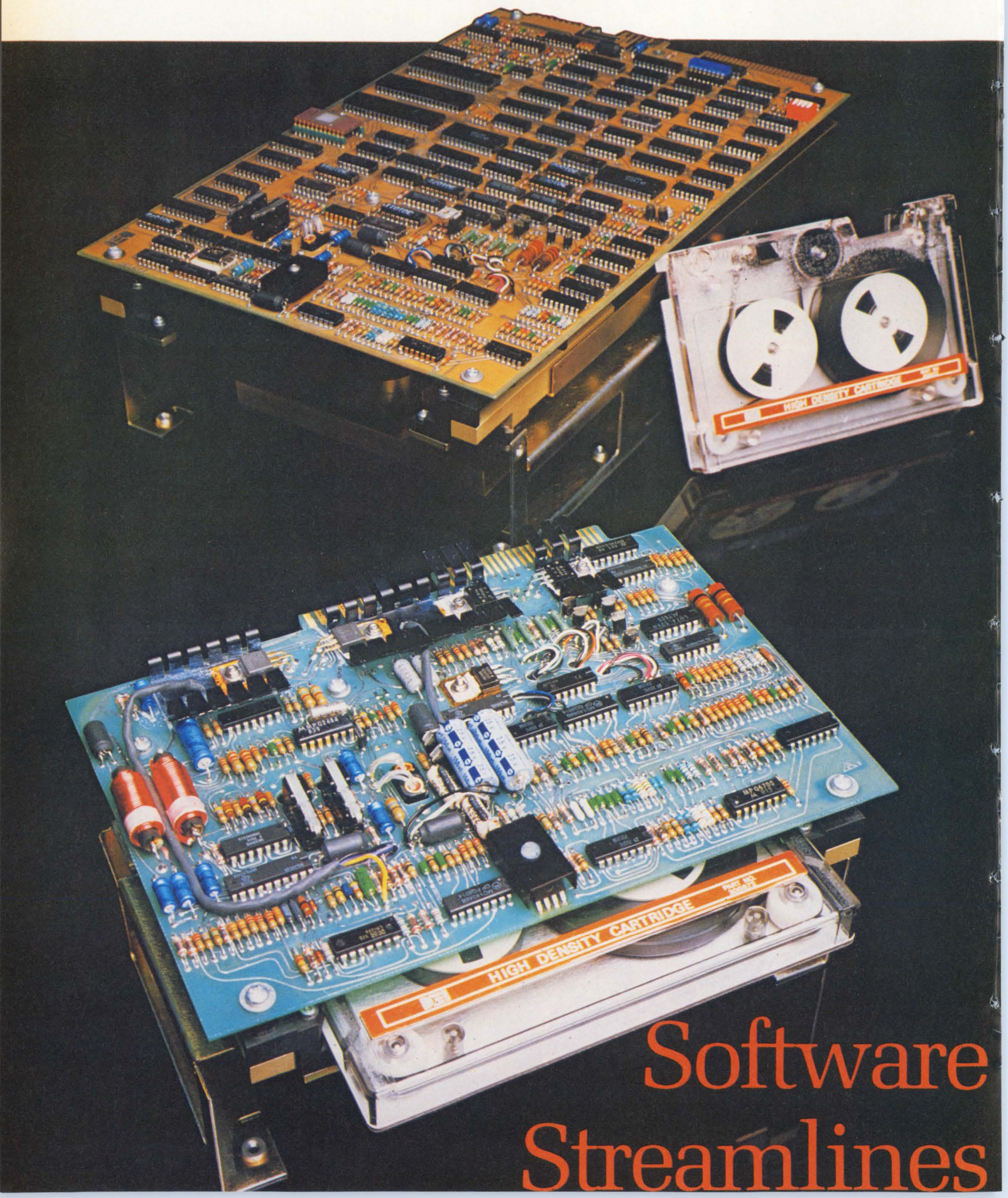
Figure 5: U.S. Design Corp (Lanham, MD) has introduced the CSS-800 Mass Storage System. It contains a 35 or 70 Mbyte Winchester disk drive with a 17 Mbyte cartridge tape drive for backup. The CSS-800 includes two integral controllers with multiported memory that allow simultaneous disk and tape operation, and is configured with a compatible host interface for the Q-bus, Unibus or Multibus.



that 16% of the buyers were currently having problems with their drives. Problems included alignment difficulties, "periodic oddball read errors," dropped bits, difficulty in servicing, and dirt getting in the mechanism ("The media may be sealed," wrote one respondent, "but the belt and drive mechanism collects too much dust.")

Temperature changes also seem to cause serious problems with Winchesters. One respondent decided not to purchase a particular Winchester because he discovered that the drive's injection-molded plastic case became so physically deformed by a 20°F temperature change that the read/write heads couldn't function properly.

After reliability, the most important factors in selecting a drive were, in order, capacity, manufacturer's reputation, price, compatibility, data access time and speed in delivery. The three things drive buyers would most like to see in the future are, in order, greater capacity, lower cost and faster access times. This summer's NCC show, which traditionally would be incomplete without at least one innovative new disk drive introduction, should show the extent to which manufacturers are able to meet these customer demands. □



Software Streamlines

Simulator Back-Up Performance

Use this simulator to test if streaming tape is the best back-up bet for you—before you commit to hardware.

by Henry L. Alioth and Rick Hackworth

Streaming ¼-inch digital cartridge tape drives are proving to be a very effective tool for backing up small Winchester disk drives. However, streaming tape is only efficient if the system parameters are chosen properly for continuous data transfer. If a streaming tape drive runs out of data, it stops. A software simulator has been developed that allows the system designer to try out a streaming back-up system before committing it to hardware.

Real Time Simulation

The software simulator monitors system events on a timed basis, and yields data in several formats. The major output format is a listing of system events with the times during which they occur. Effects of varying key design parameters can be presented in graphical form. The simulator takes into account specifications of the disk drive, the streaming tape drive and the host controller.

Disk specifications that are required for the simulator include: disk speed in rpm; number of heads per cylinder; number of sectors per track; interleave factor; header in bytes per sector; data record in bytes per sector; and number of bytes in an unformatted track. Tape drive specifications that can be varied include: tape speed in ips; time to start from BOT indication; time to stop the tape when data stops; time to reposition the tape for resumption of data flow; record size in bytes; distance between records in bytes; data density in bytes per inch; and the gap-to-gap distance between the write and the read-after-write recording heads in inches.

Optimization of buffer design parameters for the host controller are the primary objectives of the simulation. The key parameters are: buffer size in bytes; transfer rate in bytes per second; and whether the buffer can provide simultaneous input and output transfer. **Figure 1** gives a typical printout of simulator specifications for a system including a Winchester disk drive with a 90 ips streaming tape drive as the back-up.

System scenarios for this simulator require that three buffer memories exist in the system: a sector buffer that stores the data in the disk drive prior to transfer; a host buffer serving as a "byte-reservoir" that accepts the data from the sector buffer before transferring it to the back-up tape drive; and a dual tape drive buffer that accepts data from the host buffer prior to storing the data on tape, and is also used for read-after-write verification.

Key Design Variables

Since most of the disk and tape specifications are fixed for a given product selected, the system designer's most useful tools are those that can be readily varied: the host buffer size and the interleave fac-

```
1240 !    ----------------------------------------HOST-BUFFER-SPECIFICATIONS:
1250        Cap=3072                            ! HOST-RAM (BYTES)
1260        Rate=1.E+6                          ! BYTES/SECOND
1270        Sbt=1                               ! SIMULTANEOUS BUFFER INPUT AND
                                                   OUTPUT TRANSFER
1280                                            ! 1 = YES        0 = NO
1290 !    ----------------------------------------DISC-SPECIFICATIONS:
1300        Rpm=3125                            ! DISC-REVOLUTIONS/MINUTE
1310        Hpc=4                               ! HEADS/CYLINDER
1320        Spt=32                              ! SECTORS/TRACK
1330        Int=3                               ! INTERLEAVE-FACTOR
1340        Hps=58                              ! HEADER-BYTES/SECTOR
1350        Dps=256                             ! DATA-BYTES/SECTOR
1360        Bpt=10416                           ! BYTES/UNFORMATTED TRACK
1370 !    ----------------------------------------TAPE-SPECIFICATIONS:
1380        Ips=90                              ! INCHES/SECOND
1390        Tst=.550                            ! TIME TO START FROM B.O.T.
1400        Ts=.080                             ! TIME TO STOP THE TAPE
1410        Tr=.520                             ! TIME TO REPOSITION THE TAPE
1420        Rs=952                              ! RECORD-SIZE (BYTES)
1430        Dbr=990                             ! DISTANCE BETWEEN RECORDS
                                                   (BYTES)
1440        Dns=1000                            ! DENSITY (BYTES/INCH)
1450        Gtg=.3                              ! GAP TO GAP DISTANCE (INCHES)
```

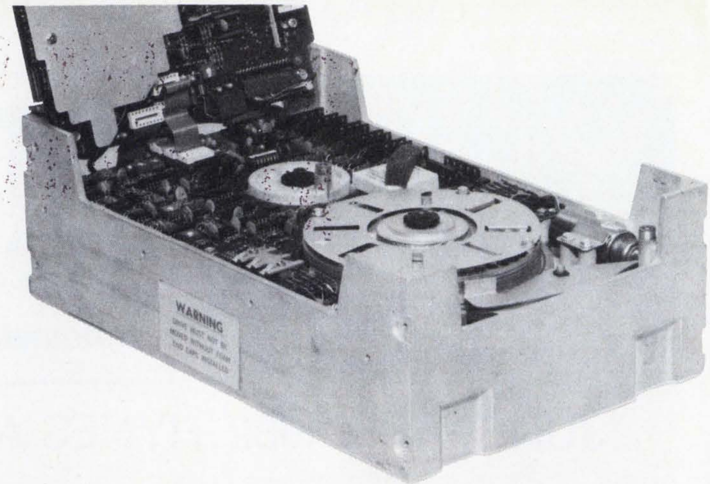
Figure 1: When setting up the simulator, the host, disk and tape specifications are entered into the computer. This is an example of the format used.

Henry L. Alioth is Director of Engineering for Advance Product Development at Data Electronics, Inc. in San Diego, CA. Rick Hackworth is President of Data Automation, also of San Diego.

```
100 ! START:
105 ! ----------------------------------------------------------------
110 ! ENTER THE GIVEN VARIABLES FOR
115 !   — THE HOST-BUFFER
120 !   — THE DISK-DRIVE
125 !   — THE TAPE-DRIVE
130 ! COMPUTE THE DEPENDENT VARIABLES
135 ! RESET THE REAL-TIME
140 ! INITIALIZE
145 !   — THE HOST-BUFFER
150 !   — THE DISK-DRIVE
155 !   — THE TAPE-DRIVE
160 !
165 !
170 !
175 ! SUPERVISOR:
180 ! ----------------------------------------------------------------
185 ! FIND THE NEAREST EVENT
190 ! UPDATE THE REAL-TIME
195 ! BRANCH TO
200 !   — THE DISK SUB-PROGRAM
205 !   — THE HOST-SUB-PROGRAM
210 !   — THE TAPE-SUB-PROGRAM
215 ! DISK-SUB-PROGRAM:
220 ! ----------------------------------------------------------------
225 !   WAS THE DISK-DRIVE
230 !     — READING?
235 !     — SEEKING?
240 ! SECTOR-READ-OPERATION COMPLETED:
245 !   LOG SECTOR ON TRACK-MAP
250 !   SECTOR-BUFFER = FULL
255 !   FIND THE NEXT SECTOR:
260 !     — END OF CYLINDER?
265 !     — END OF TRACK?
270 !     — SAME TRACK?
275 ! -END OF CYLINDER:
280 !   STEP HEADS TO NEXT CYLINDER
285 !   POSTPONE NEXT EVENT FOR 1 REVOLUTION
290 !   SWITCH TO FIRST HEAD -1
295 ! -END OF TRACK:
300 !   SWITCH TO NEXT HEAD
305 !   INITIALIZE SECTORS ON TRACK-MAP
310 ! -SAME TRACK:
315 !   LOCATE NEXT AVAILABLE SECTOR
320 !     ON THE TRACK-MAP
325 !     (RESPECTING INTERLEAVE)
330 !   COMPUTE NEXT DISK-EVENT-TIME
335 !   BEGIN SEEK-OPERATION
340 !   RETURN TO SUPERVISOR
345 !
350 ! SEEK COMPLETED:
355 !   IS THE SECTOR-BUFFER
360 !     — EMPTY?
365 !     — NOT EMPTY?
370 ! -SECTOR-BUFFER = EMPTY;
375 !   COMPUTE NEXT DISK-EVENT-TIME
380 !   BEGIN TO READ 1 SECTOR
385 !   RETURN TO SUPERVISOR
390 !
395 ! -SECTOR-BUFFER NOT EMPTY:
400 !   WAIT FOR 1 REVOLUTION
405 !   POSTPONE NEXT EVENT FOR 1 REVOLUTION
410 !   BEGIN SEEK-OPERATION
415 !   RETURN TO SUPERVISOR
420 ! HOST-SUBPROGRAM:
425 ! ----------------------------------------------------------------
430 !   UPDATE THE CONTENTS OF
435 !     — THE DISK-SECTOR-BUFFER
440 !     — THE HOST-RAM-BUFFER
445 !     — THE TAPE-RECORD-BUFFERS
450 !   IS THE HOST REQUIRED TO SERVICE
455 !     — THE DISK-SECTOR-BUFFER?
460 !     — THE TAPE-RECORD-BUFFER?
465 !     — BOTH (SIMULTANEOUSLY)?
470 !     — NEITHER (IDLE)?
475 ! DISK: NEXT EVENT WHEN SECTOR-BUFFER = EMPTY
480 !         OR WHEN HOST-RAM = FULL
485 !   RETURN TO SUPERVISOR
490 !
495 ! TAPE: NEXT EVENT WHEN RECORD-BUFFERS = FULL
500 !         OR WHEN HOST-RAM = EMPTY
505 !   RETURN TO SUPERVISOR
510 !
515 ! BOTH: NEXT EVENT = EARLIER OF THE ABOVE
520 !   RETURN TO SUPERVISOR
525 !
530 ! IDLE: NEXT EVENT = EARLIEST DISK-EVENT
535 !     OR TAPE-EVENT
540 !   RETURN TO SUPERVISOR
545 !     TAPE — SUB-PROGRAM:
550 !     ----------------------------------------------------------------
555 !       HAS THE TAPE-DRIVE
560 !         — STOPPED?
565 !         — ACCELERATED FROM B.O.T.
570 !           OR REPOSITIONED FROM A STOP?
575 !         —- WRITTEN A RECORD?
580 !         — VERIFIED A RECORD?
585 !         — DECELERATED?
590 !     STOPPED:
595 !       ARE THE TAPE-RECORD-BUFFERS
600 !         — FULL?
605 !         — NOT FULL?
610 !     — FULL:
615 !       START THE TAPE
620 !       SET MOTION-INDICATOR
625 !       NEXT EVENT WHEN PAST LOAD-POINT
630 !         OR AFTER REPOSITIONING
635 !       RETURN TO SUPERVISOR
640 !
645 !     — NOT FULL: WAIT
650 !       NEXT EVENT = EARLIEST HOST-EVENT
655 !         OR DISK-EVENT
660 !       RETURN TO SUPERVISOR
665 !
670 !     ACCELERATED OR REPOSITIONED:
675 !       BEGIN TO WRITE 1 RECORD
680 !       NEXT EVENT AT END OF RECORD
685 !       RETURN TO SUPERVISOR
690 !
695 !     WRITTEN A RECORD:
700 !       COUNT THE RECORD
705 !       CLEAR FLAG
710 !       IF UNDERFLOW, SET FLAG
715 !       VERIFICATION IS IN PROGRESS
720 !       NEXT EVENT AFTER 1 GAP TO GAP DELAY
725 !       RETURN TO SUPERVISOR
730 !
735 !     VERIFIED A RECORD:
740 !       RELEASE THE RECORD-BUFFER
745 !       CHECK FLAG FOR
750 !         — STREAMING?
755 !         — UNDERFLOW?
760 !     — STREAMING:
765 !       WRITE-OPERATION IS IN PROGRESS
770 !       NEXT EVENT AT END OF RECORD
775 !       RETURN TO SUPERVISOR
780 !
785 !     — UNDERFLOW:
790 !       DECELERATE THE TAPE
795 !       NEXT EVENT WHEN STOPPED
800 !       RETURN TO SUPERVISOR
805 !
810 !     DECELERATED:
815 !       SET STOP-INDICATOR
820 !       NEXT EVENT = EARLIEST HOST-EVENT
825 !         OR DISK-EVENT
830 !       RETURN TO SUPERVISOR
```

Figure 2: The basic program flow of the supervisor and the three sub-programs, host, disk and tape are shown here. The basic programs can be implemented in the code of the particular computer used for the simulation. Dashes in the program flow indicate branches in the program.

WHY WAIT FOR THE FUTURE OF DISC STORAGE TECHNOLOGY TO REACH DEC SYSTEMS?



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FSV06JJ

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Because the disc platters, read/write heads and positioners are sealed in a contamination-free environment, you eliminate the risk of head crashes.

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In addition, the clean recording environment allows closer tolerances in the positioning of the read/write heads. Yields greater recording densities. Higher transfer rates.

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FSV06ZJ

28 Mbyte fixed, Winchester storage and 1.2 Mbyte, double-sided, double density floppy for backup. Includes quad-wide Winchester controller. Dual-wide floppy disc controller. 5-1/4" chassis includes power supply

The same backup requirement stalled the use of Winchester technology in small minicomputer systems. Start-stop magnetic tape transports were too expensive for the small systems user. Floppy disc too slow.

Widespread use of 8-inch Winchester technology had to wait until someone solved the backup problem.

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PLESSEY SOLVES THE BACKUP PROBLEM

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The perfect solution would be simple to use. Fast. Inexpensive.

Two and a half years later, Plessey introduced its 1/4-inch streaming cartridge tape backup device — the PM-CSV11A.

It's simple to use
Fast
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So simple to use, in fact, a first-time user can perform backup routines within minutes. Effortlessly. Flawlessly.

ADD A WINCHESTER WITH FAST, EASY TO USE BACKUP

FSV06TJ
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FSV06TJ

Combines 28 Mbyte 8″ Winchester with 1/4″ streaming tape. Fast. Easy to use. True tape streamer — completes backup in 5 minutes. Operates at 90ips. NOT a TM11 or TU11 emulation. Unique. Convenient. Easy to handle tape cartridges cut media cost drastically. And store easily too.

Subsystem includes Winchester, tape streamer, power supply, chassis, controllers, and Cartridge Image Backup utility software.

Backup your new Winchester without interrupting your processor.

New on-line backup under RSX-11M allows file(s) transfer from fixed-media Winchester to ¼″ tape or complete disc backup to tape online (non-streaming). Only available from Plessey Peripheral Systems.

TRUE TAPE STREAMER

So fast you can backup an entire 28 Mbyte Winchester in 5 minutes.

Simply insert a tape cartridge. Type in a command and the tape drive does the rest. At 90 IPS you can backup an entire 28 Mbyte Winchester in 5 minutes. Each drive is partitioned into 14 Mbyte RK06 units for simple archival storage. Use your CSV11A to copy RK05s. RL02 packs. Supports TM11 mag tape.

Economical, too. Save on media costs. Load software and diagnostics. All for less than half the cost of a 1/2-inch tape transport.

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23VTJ-320
$15,080
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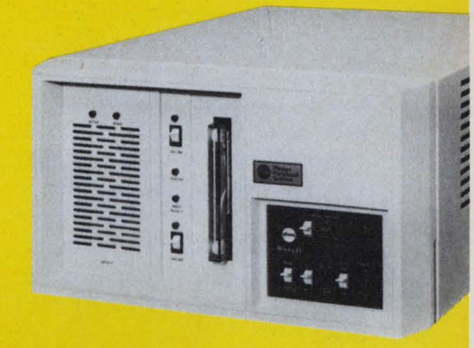

At 20% off, the most advanced LSI-11/23 based computer system just became the best priced. 28 Mbyte Winchester, 1/4-inch tape streamer, LSI-11/23 CPU with 128 Kbyte memory, serial line interface, 9-slot quad backplane in one desktop cabinet.

Enough computing power for eight users. Reliable Winchester storage. Easy to use streaming tape backup device that provides archival storage and software distribution.

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tor. The larger the host buffer, the longer the system can maintain streaming as the data from the disk becomes intermittent. Carefully selecting the interleave factor allows for matching of data transfer rates between disk and tape. Interleave factor is defined for this simulation program as the increment of the disk sector address that establishes the periodicity of sector reading. For example, an interleave factor of 3 means that the disk will read sectors 0, 3, 6, 9, 12, etc. In cases where the number of sectors per track is a multiple of the interleave factor, additional sectors may have to be skipped at the end of a track. A track/sector map is used in the program to establish correct sequence.

In the simulation, data is read from disk to sector buffer, sector buffer to host buffer, host buffer to tape buffer, and tape buffer to tape. Read-after-write verification is taken into account. Tape buffers are filled first; then the host buffer. Until both are filled, data is not written on the tape. **Figure 2** illustrates the program flow, in simplified form. There is a Supervisor program and Disk, Tape and Host sub-programs. The Supervisor links the sub-programs into a proper sequence of events. The simulation program is coded in Basic.

If data isn't provided from disk to the tape and host buffers as fast as it is written onto the tape, the tape drive will stop.

Underflow Disrupts Streaming

If data is not provided from the disk to the tape and host buffers as fast as it is written onto the tape, the buffers will eventually run out of data and the tape drive will stop. This condition is called buffer underflow in the simulator. Ideally, underflow should be avoided, since streaming tape drives take a relatively long time to reposition and start. To avoid start/stop gaps on the tape, the restart algorithm is as follows: after a stop command, the drive decelerates to a stop; to continue, the tape backs up to a point before the end of the previous record and then ramps up to speed in the forward direction to resume recording immediately following the last written data. This repositioning takes about 600 ms.

As a general rule of thumb, you need enough host buffer to last at least through two disk revolutions without new data coming from the disk to the host, while still providing data to the tape.

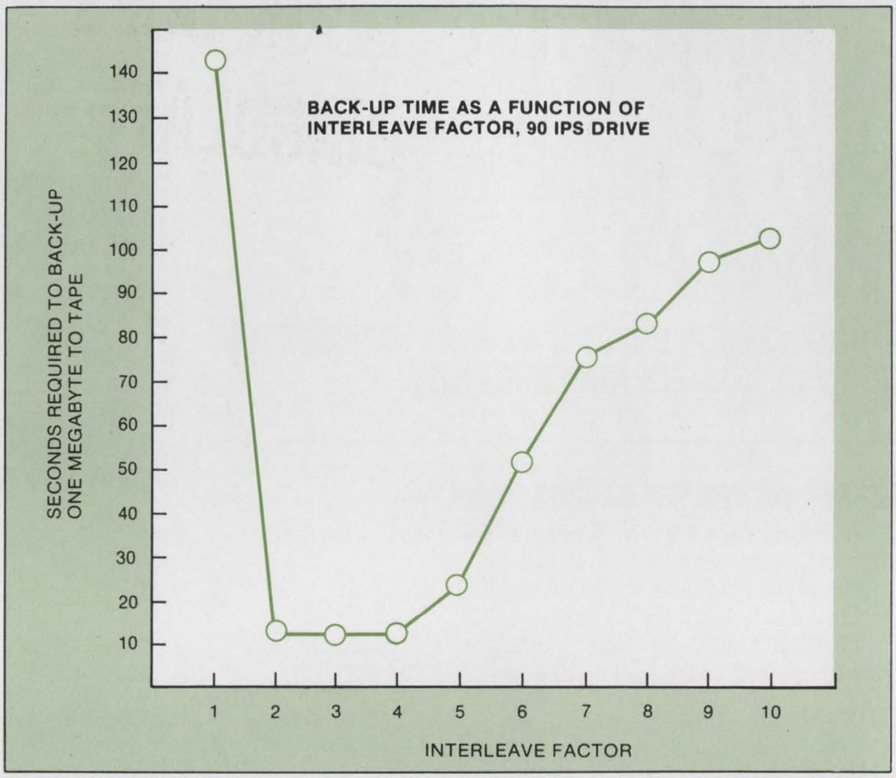


Figure 3: The time required to back-up 1 MB of data and transfer it to tape is shown as a function of interleave factor. For this particular case, the flat section of the curve indicates that streaming is maintained when the interleave factor is either 2, 3 or 4.

Graphic Simulation Results

Two useful curves that can be plotted by the simulation program are: back-up time as a function of interleave factor for a given host buffer size; and the effect of host buffer size on records written before the first underflow. **Figure 3** gives an example of a system using a Winchester with a 90 ips streaming tape drive and assumes a 3 Kbyte host buffer.

In **Figure 3,** the time required to back-up 1MB of data and transfer it to tape is shown as a function of interleave factor. At factor one there is no time for the host to unload the sector buffer between sectors and only one sector can be transferred per revolution of the disk. The flat section of the curve indicates that streaming is maintained when the interleave factor is either 2, 3 or 4. The back-up time for 1MB is then only 15 seconds. This would be equivalent to backing up 20 MB of data in 5 minutes. As the interleave factor goes higher, the effective transfer rate decreases, resulting in an increasing frequency of underflow conditions. The more often underflow occurs, the more tape repositionings occur, and the longer it takes to back-up the disk.

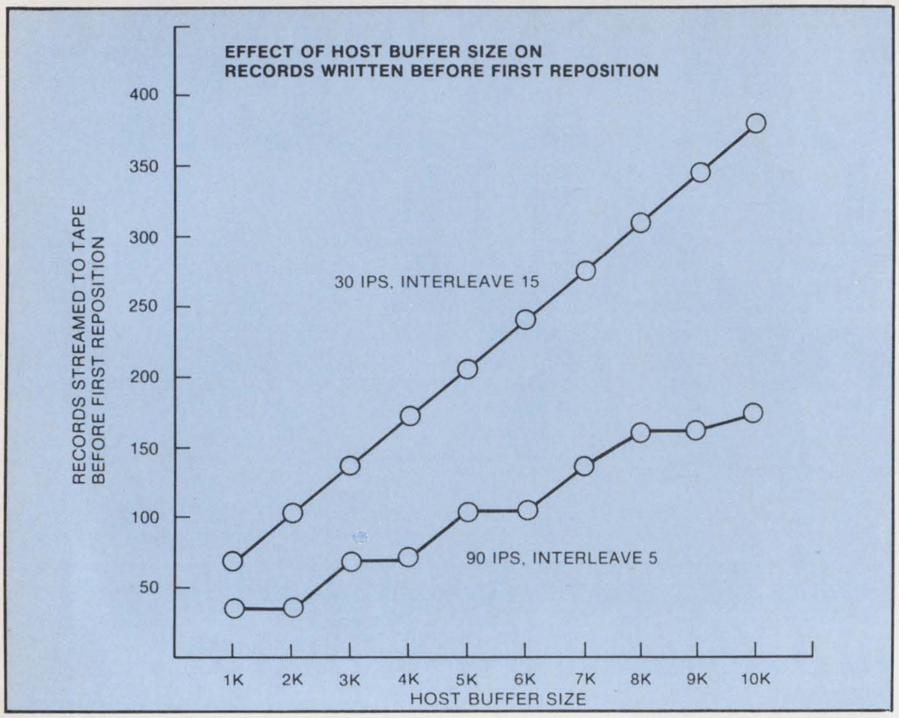


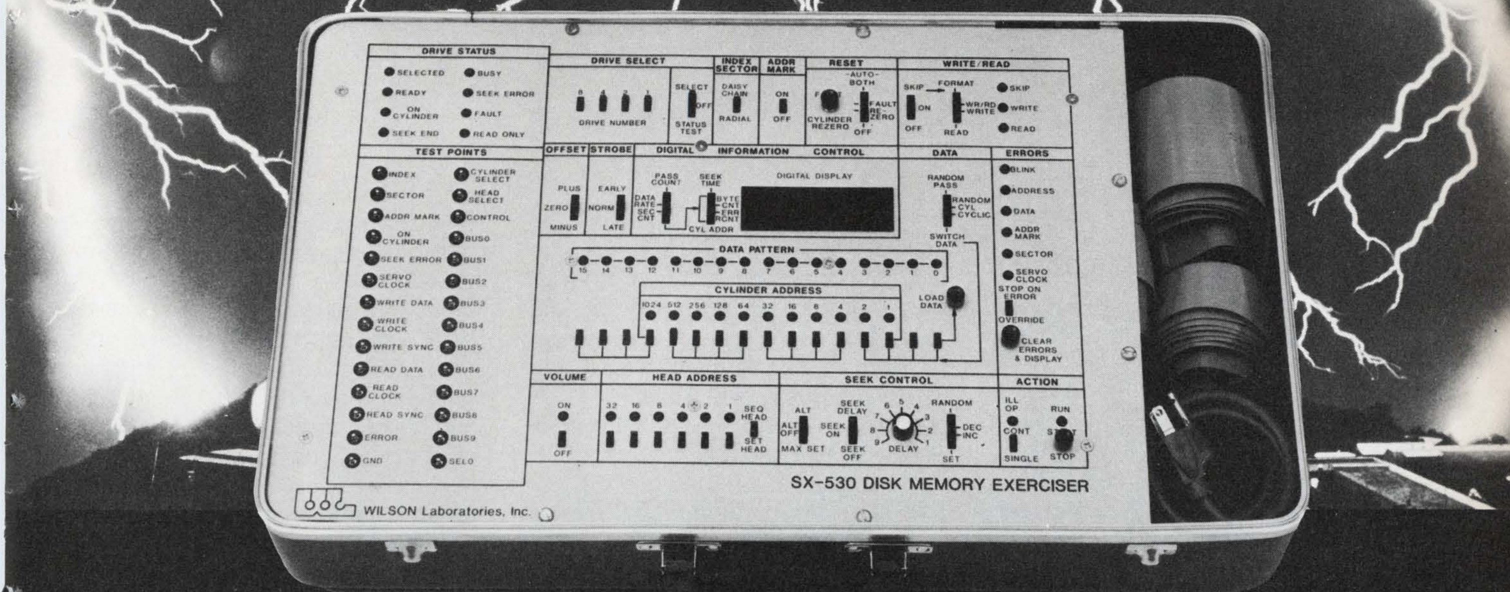
Figure 4: In a case where the interleave factor is just beyond perfect streaming, this curve shows the number of records that will be streamed to tape before the first repositioning, or between underflow conditions.

Figure 4 illustrates what happens when the system is just beyond a perfect streaming scenario. It shows the number of records streamed to the tape before the first underflow condition (first tape reposition), or alternatively, the number of records that will be streamed between tape repositionings, as a function of host buffer size. Since the 90 ips tape drive will stream below an interleave factor of 5, and a 30 ips tape drive will stream below an interleave factor of 15 (in this example), the benefit of increasing host buffer size can be clearly seen. The greater slope of the 30 ips curve indicates that a small increase in host buffer size buys more advantage than the 90 ips case. This curve is of particular importance if system requirements do not allow a selection of an interleave factor that will guarantee constant streaming.

If your application generates a small number of underflows, then streaming tape may be the fastest and most economical back-up technology available.

When the number of underflows becomes large, such as in a file reorganization application, streaming may become an inappropriate means of back-up. In this case, a start/stop cartridge tape drive becomes the logical choice. However, if the application allows for streaming, this is the fastest and most economical back-up technology available. □

WILSON SX-530



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Designer's Guide To The STD Bus

A number of factors make the STD bus, now with over 70 manufacturers, one of the fastest growing buses of the past ten years.

by Paul Snigier, *Editor*

Born in mid-1978 out of a joint agreement between Pro-Log and Mostek, and developed by Matt Biewer (of Pro-Log), the STD or Standard Bus gained rapid acceptance among designers. There are now over 70 manufacturers, the majority being board makers. The easy-to-use modular board approach, lower design and manufacturing costs, initial dual-sourcing and being in the public domain (not patented, copyrighted nor trademarked) contributed to the spectacular rise of the STD Bus, helping to make it one of the fastest-growing buses of the past ten years. In this article, we will look at these characteristics and examine some STD Bus concepts so that you can more accurately assess its suitability to your specific product concepts in terms of designability, manufacturability and maintainability.

Modularity Cuts Costs

The high degree of modularity is a crucial advantage of the STD Bus concept. You choose and pay only for those features that you need. This is in contrast to other buses, which may force you to settle for more than what you need, and incorporate this as added cost buried in the overall system or subsystem price. Ultimately, this added cost for "overkill" must be paid by the end user, who will in turn pass the added cost along to his customers or clients. The simplicity of the STD Bus can eliminate this waste.

First we will begin with a capsule overview of the STD Bus.

The bus is a 56-pin synchronous bus with five sections:

- six data lines
- eight bidirectional data lines
- 16 address lines
- 22 control lines (three bidirectional)
- four auxiliary power lines.

All data and address lines are tristate buffered, as in most buses. Control lines contain controls for memory, I/O, bus access, interrupts and lines for CPU action. Power distribution has ±5V for logic and ±12Vdc auxiliary power, with the option of using it for ±15Vdc or adapting to it with dc-dc adapter cards. Although it has only 16 address lines capable of directly addressing 64K of memory, memory expansion permits addressing far more.

Most STD edge-connected cards are small, almost tiny, compared to other bus boards, measuring only 4.5″ wide by 6.5″ long, regardless of function. The bus is 56-lines wide, using a 56-pin (dual 28-pin) edge connector. Pins are spaced 0.125″. The system, constructed around a standard bused motherboard, allows any card to be inserted in any slot.

With STD card sets, irrespective of the manufacturer, the bus will handle all internal communications, facilitating an orderly signal flow between cards. For the most part, you can alter system functions, memory type and even CPU type by merely replacing cards. With existing STD Bus card makers, and new card makers entering or switching to the STD Bus CPU's and other functions available in card sets have more than doubled in the past two years. The Pro-Log/Mostek gamble paid off handsomely, for STD Bus makers, for OEMs and for end users.

STD Brings Consistency

Unlike many other μP buses in wide use that are tied to the quirks of particular μPs, the STD Bus is universal. It can handle any of the popular 8-bit μPs and some others. It avoids ambiguities so common on other μP buses because all STD bus lines are already defined.

System controls exist for memory and I/O. The bus can enable operations like memory expansion, memory-mapped I/O, DRAM refresh, DMA, multiprocessing, single-stepping, slow devices, power fail, fixed priority and daisy-chain interrupts.

The simplicity of the bus almost eliminates—and in some cases totally eliminates—considerations of handshake and protocol. By selecting and designing around this totally-defined bus, you are almost completely freed from worrying about bus considerations. You cannot change this bus. If this results in a loss of some flexibility, it is more than offset by its remaining constant, no matter how many system additions or modifications are

STD CARD DIMENSIONS	INCHES		MILLIMETERS	
	NOMINAL	TOLERANCE	NOMINAL	TOLERANCE
Card Length	6.500	±0.025	165.10	±0.64
Card Height	4.500	+0.005, −0.025	114.30	+0.13, −0.64
Plated Board Thickness	0.062	±0.003	1.58	±0.08
Card Spacing	0.500	MIN	12.70	MIN

Figure 1: STD card dimensions exclude the card ejector and I/O interface connections, which may or may not be on the card.

made, and no matter who makes them or when. No one else can change the bus, even if they wanted to. This is what a bus standard is supposed to do. It is also why the STD Bus is called the "Standard Bus."

All this does not mean that if your system uses one bus standard that you cannot use another. It is possible to adapt one bus to another, often without a major redesign, if this greater flexibility is worth some system degradation.

On a related vein, if your investment in existing software routines for one given processor is significant, this does not preclude you from discarding your library to use the STD Bus. There are a wide and rapidly-growing variety of CPU cards built around different μPs. You may choose a CPU card, memory, I/O and other functions for virtually any application.

RECOMMENDED MINIMUM CARD SPACING	INCHES		MILLIMETERS	
	MAXIMUM	MINIMUM	MAXIMUM	MINIMUM
Component Height	0.375	—	9.52	—
Component Lead Protrusion	0.040	—	1.02	—
Adjacent Card Clearance	—	0.010	—	0.25

Figure 2: Minimum card spacing depends upon card clearance and thickness, which is fixed, plus a tradeoff between component height and lead protrusion. Cards unable to meet these specs require multiple card slots. An (optional) card ejector occupies the top 1.4" (35.6mm) of the card, protruding 0.1" (2.54mm) out on each side.

STD Mechanics

From a mechanical point of view, the small STD Bus cards are well-suited for harsh environments, have high reliability and make system support easier. The 4.5" wide by 6.5" long cards, which are supported along their vertical and horizontal axes, withstand rough environments easier than larger boards. Larger boards are weaker, as are their enclosures, and so cannot tolerate as much vibration—particularly at low frequency—and impact shock. These larger enclosures are also more expensive.

Higher reliabilities (MTBFs) are not only due to the more rugged STD Bus enclosures and cards, but also to other parameters such as thermal considerations. With increasing heat due to the greater number of components, it is inherently more difficult to cool larger boards than smaller ones, such as the STD Bus cards. Cooling of STD cards will require either a lower CFM-capacity and smaller fan or permit natural air convection cooling in cases where equivalent larger boards would require more costly, higher CFM cooling. Even if cards are mounted vertically, the STD cage allows convection

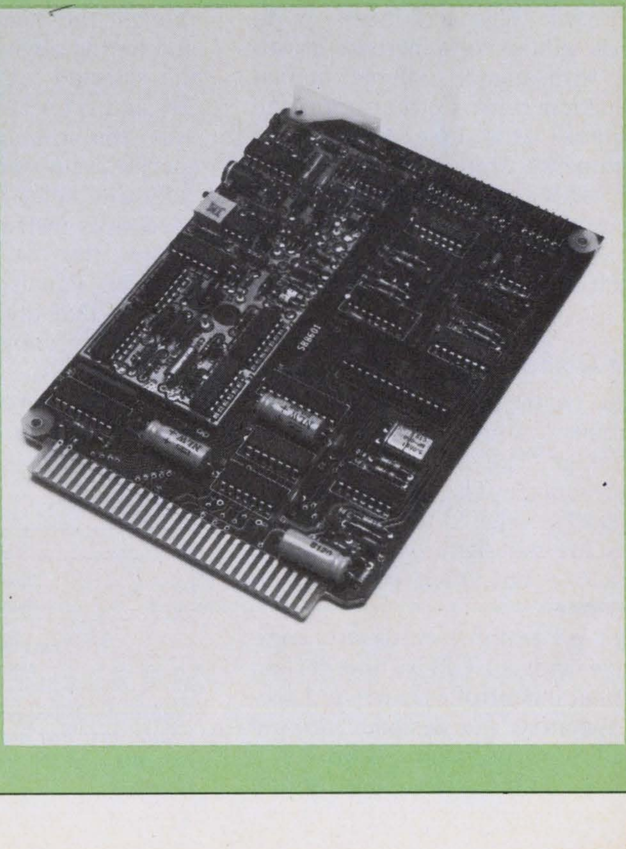
STD Bus Modem Boards Permit Low-Cost LANs

STD Bus Local Area Network (LAN) gateways and network controllers can now be achieved through use of Micro/sys's SB8601 and SB8602 coaxial cable-driven modem boards. Availability of these two boards brings the STD Bus into the field of multiple-node data acquisition networks for factory automation, automatic test, and process monitoring applications.

The SB8601 contains an asynchronous/synchronous serial interface port to drive its on-board modem; it operates up to 19,200 baud. Only the modem is included on the SB8602, which is intended as an add-on to other Micro/sys communication products. Both boards provide a coaxial cable interface.

When driven by a Micro/sys SB8451 Synchronous Data Link Controller (SDLC), the SB8602 can operate at 1 Mbaud and transfer a 2 Kbyte data block in 17ms. This allows block-oriented transmissions (in the standard IBM format) between STD Bus systems, or from STD Bus systems to minicomputers or mainframes.

Both modem boards use FSK modulation and provide typical error rates of less than 10^{-12} for installations with a 20 dB signal-to-noise ratio. Standard RG-59 coaxial cable can be used for links of nearly one mile, and other cable types can extend the range to five miles. A 30 dB dynamic range allows modems to be attached to the cable at any point without gain adjustment or adjacent modem overload. Receivers employ single-ended, 50 kΩ inputs and exhibit a normal mode rejection of 10V at 60 Hz.



cooling in 55°C ambients. From a reliability viewpoint, if the forced air cooling is impaired by fan or blower failure or by aperture blockage, the larger cards of another bus would have much greater difficulty in operating in a reduced mode. The STD system keeps fully-populated RAM cards below 70°C.

System maintenance of large, complex, multi-function boards is difficult. Since many functions exist on these larger boards, failure of any one board is likely to result in total system failure; this means longer MTTRs, as these boards encourage longer trouble-shooting. It is also more necessary to maintain a large spare parts inventory, as the tradeoff point between a larger board's throwaway-repair crossover tends more to the repair side. These economics are inherent in the nature of the larger boards. On the other hand, one- or two-function STD cards encourage trouble-shooting by board-swapping. Also, repair can be inherently faster (lower MTTR) and can require less skilled field repair engineers.

As an initial cost, larger boards require that their systems attempt to fully utilize all the functions on the board. This is difficult to do and the added costs increase drastically with higher volume annual production runs. Furthermore, the argument that larger-than-spec components cannot be fitted onto STD cards is not often a problem; and even when it is, it can be solved by tradeoffs between component height and lead protrusion.

STD Disadvantages

Some characteristics like lack of flexibility, described earlier as an advantage, can also be seen as a disadvantage. The STD Bus was purposely designed to be inflexible; if you are a designer who must add lines to a bus, then consider another one.

Not all support cards are compatible with all CPUs, and certain peripheral controller cards and special functions are designed around a dedicated peripheral chip for a given μP. Operation compatibility must be your foremost concern when evaluating boards from different STD Bus card makers. If based on peripheral ICs that must work with a specified CPU, take care to see that when you do combine boards from different CPU families they will work.

The reason for your concern has to do with four STD Control Bus lines: pins 37 ($\overline{\text{REFRESH}}$), 38 ($\overline{\text{MCSYNC}}$), 39 ($\overline{\text{STATUS 1}}$) and 40 ($\overline{\text{STATUS 0}}$). These are, respectively, Refresh Timing, CPU Machine Cycle Synchronization, CPU Status and CPU Status. Signal flow is out for all four. Pins 37 and 39 are on the card's component side; pins 38 and 40, on the circuit side. More specifically, $\overline{\text{REFRESH}}$ (pin 37) provides refresh timing for DRAMs.

Only a couple of μPs, such as the Z80, have an on-chip refresh register, while others have the refresh address counter on either the CPU or auxiliary card.

The $\overline{\text{MCSYNC}}$ (pin 38) is a tristate, active low-output signal. This signal is outputted once per CPU machine cycle. A machine cycle is the sequence of addressing, data transfer and execution. $\overline{\text{MCSYNC}}$ defines the start of this cycle, although the signal's exact nature and timing obviously depends upon the selected μP. $\overline{\text{STATUS 1}}$ (pin 39) and $\overline{\text{STATUS 0}}$ (pin 40) provide this timing information for special cycle operations. If specifically available, $\overline{\text{STATUS 1}}$ is used to identify instruction fetch.

Now that we know what these four bus signals do, we must keep in mind that they are implemented slightly differently. This will depend upon the CPU selected. If you are a newcomer to the STD Bus, be alert to this potential trouble spot.

Some CPU-peripheral combinations on the STD Bus may be incompatible because the interface board is I/O-mapped while the CPU supports only memory mapping. Memory-mapped I/O treats each I/O peripheral—whether it be a Winchester drive, printer, VDT, or even another μP or μC—like any memory location. It is possible to use memory transfer instructions for I/Oing the data. Memory-mapped I/O is superior and is common in μP systems possessing a unified bus structure. With it, no separate I/O instructions (such as OUT and IN) are used, as the memory data transfer instructions are also used to transfer data between the I/O device(s) by assigning a block of unused memory address as device addresses. By way of comparison, in memory-mapped I/O, the 8080A-derived μPs allow data transfer not just to the A-register (accumulator), as with accumulator I/Oing, but between the memory I/O device and any of the seven general-purpose registers.

Memory-mapped I/O can address far more peripheral devices than can accumulator I/O techniques. The advantages come with greater risk. The lack of absolute decoding of the complete address bus can trip careless designers, unlike accumulator I/Oing, where absolute decoding is done (where all eight lower or eight higher bits should designate or decode a given I/O peripheral device). It is essential to decode the higher address bits, particularly A13–15. With memory-mapped I/O, AO-14 address line inputs to memory, while A15 identifies it as an I/O operation. Thus, the far more powerful memory instructions will be used. For instance, it is unnecessary to transfer contents in and out of tem-

PARAMETER	LIMIT	REFERENCE
Positive voltage applied to logic input or disabled 3-state output	+5.5V	GND pins 3,4
Negative DC voltage applied to a logic input or disabled 3-state output	−0.4	

Figure 3: Maximum ratings for the pins certainly are not recommended operating conditions, but are absolute ratings. Exceeding these ratings can damage card components. Never remove cards or components while voltage is applied, unless specified.

porary registers when arithmetic can be performed directly on an input or output latch.

Like all good things, there is a price. In addition to those mentioned, the loss of one bit means that only 32K of directly-addressable memory now exists, not 64K. One bit less can be a disaster, and there is no way out. When A15 on the STD/CPU address bus is ONE, memory-mapped I/O exists; otherwise (logic ZERO), it does not. When A15 is logic ONE, bits AO-7 decode a selected I/O peripheral device, which looks like an 8-bit memory location, so that MRIs are used to R/W from/to that selected peripheral device. Using these MRIs is a great strength. Although in a small system, this is fine, in a larger one it may rule out use of memory-mapped I/O. Depending upon the peripheral-CPU incompatibility and your system memory needs, this could pose a serious problem.

Fortunately, in industrial control, robot, control automation and process control applications—for which the STD Bus hardware/module software approach is well-suited—there is rarely the need for great quantities of memory, as there often is in data processing applications.

MRIs generally need three bytes to address a port location, to define it out of the possible 64K locations. This is a disadvantage. Special I/O instructions, on the other hand, require only eight bits, not 16 bits of address. The need for extra address bytes means that memory-mapped I/O instructions can take longer to execute, although using two-byte memory instructions (short addressing) can solve this problem.

By way of contrast, the special accumulator I/O instructions just mentioned above are not easily confused with MRIs. For programmers, this helps prevent errors. Then, the instructions are shorter. Also, due to shorter addressing, decoding requires less hardware. Once again, advantages exact a price. Aside from losing the CPU power of memory-mapped I/O (which we have discussed), two control pins are "wasted" for IOR and IOW.

CARD PIN	SUPPLY VOLTAGE	TOLERANCE	REFERENCE
1,2	VCC (+5V)	±0.25V	GND pins 3, 4
5	VBB #1 (−5V)	±0.25V	GND pins 3, 4
6	VBB #2 (−5V)	±0.25V	GND pins 3, 4
55	AUX +V (+12V)	±0.5V	AUX GND pins 53, 54
56	AUX −V (−12V)	±0.5V	AUX GND pins 53, 54

Figure 4: Power bus voltage tolerances. The voltages are specified at the card pins, not backplane traces. 7400 logic has a ±0.5Vdc tolerance; logic, ±0.25Vdc. Most STD cards require +5Vdc for logic. With upcoming lower-power all-CMOS systems, some of the logic power level pins may be opened up for some applications.

Analog Devices

Many analog devices require a ±15 Vdc power supply, and are being incorporated into more STD Bus cards now. Unfortunately, the STD Power Buses only supply ±12Vdc (pins 55 and 56 respectively) for the Power Bus and ±5Vdc (pins 1,2 and 5,6, respectively) for the logic Power Bus. If you must use ±15 Vdc analog components, then there are several choices. You could modify auxiliary power pins 55 and 56 (normally a 24Vdc differential) up to ±15Vdc. Then, by regulating the ±15Vdc down to ±12Vdc on the cards needing ±12Vdc, you can have both. Or, you can specify only those analog ICs that use ±12Vdc.

Another approach is to specify dc-to-dc power converter cards that plug directly into the STD Bus backplane and operate from the STD supply to provide noise-free bipolar ±15 Vdc output. Such power converter cards eliminate ground loop problems on the STD Bus return. These cards are isolated to withstand 500-V common-mode voltages and are EMI/RFI shielded to minimize transients from entering the power lines and passing on to the analog devices, which are sensitive to spurious emissions. Prices depend upon maximum output current and typically would sell for under $200 to over $250 for 150-mA and 300-mA current outputs. Those firms making analog I/O STD Bus cards are going to offer dc-dc power converter cards to round out their families.

Warnings in the past have been voiced about inserting cards the wrong way—that is, swapping component and circuit (trace) sides. If space allows, ejector tabs help pull stubborn cards out of their card cage. In addition, certain cages use ejector tabs to prevent the accidental backward reinsertion of removed cards. An insertion card-slot priority key (notched between pins 25 and 27, and 26 and 28) prevents backward reinsertion of cards. Cards keyed with this single, offset key slot must not use the slot between pins 27 and 29 or between 28 and 30 or this will invalidate the polarity keying.

Wire-wrap pins can scrape adjacent boards if care is not taken. Although the minimum interboard spacing is 0.5″, 0.75″ is commonly used, as the added 0.25″ minimizes this. Wire-wrap prototype boards can be messy, and some cages have a few slots with 2″ spacing just for this.

Other mechanical problems exist. Cards may be too thin and the edges unsmoothed or unrounded. Look for power and ground traces wider than the others, as well as wire-wrap wires soldered to the card's underside ("worms"). Silk-screened component labels and other identifiers make trouble-shooting and servicing easier, and will cut your long-term costs.

The Future

A number of trends are affecting STD Bus use. One key trend is greater support and variety of cards coming from a growing (70-plus) list of STD product vendors. More 64-K RAMs, and even 256-K RAMs (next year), will show up on STD cards. Another factor at work is the volume of STD Bus cards.

STD-Bus Compatible SBC

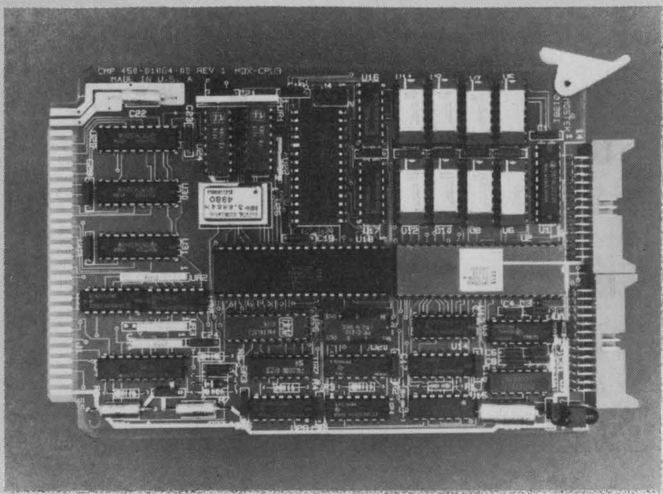
Mostek Corp has expanded its line of STD-Z80-Bus compatible microcomputer boards with the addition of a single-board computer called the MDX-CPU3.

The card features an RS232 serial port and an 8-bit output port with a handshake for connection to a printer. Using 64K dynamic RAMs, it has 64 Kbytes of dynamic memory and up to 32K of ROM or EPROM memory using a single 28-pin memory socket.

The CPU3 supports a flexible memory map configuration, allowing the user to map ROM anywhere on 2K boundaries in the 64K memory map. This feature permits up to 16 different configurations selectable from software.

Using only 18 of the possible 256 port addresses, the CPU3 leaves 238 port addresses for user expansion.

The CPU3 also generates all address and control signals necessary to refresh external dynamic RAM modules to support multiple memory banks. All signals are fully buffered for system expandability, and the CPU3 has a bi-directional reset capability which allows operation with a power-fail-detect module, such as the Mostek MDX-PFD.



Sales have grown explosively, especially considering that the STD Bus is a newcomer, compared to older buses such as the staid Multibus, which came on the scene in 1974. The growing sales of STD Bus products, and the force of the learning curve, mean that prices will continue falling until there is no replace-and-discard-versus-repair decision to be made. Every field-serviceable STD card will be so low-cost it will be automatically discarded and replaced with a new one, thus lowering support and inventory stocking costs, not to mention delays. The more complicated buses cannot follow suit.

The 0°C to 55°C cards we see now will still exist in the next few years, although they will be joined by newer, higher-rated cards in the 0°C to 70°C or better range. Upcoming, all-CMOS STD cards will help here, and will also provide the added benefits of higher voltages, lower power consumption and greater noise immunity. Since in smaller STD Bus microsystems, the CPU often consumes a greater ratio of total power, the newer CMOS μPs will help cut power consumption. Despite few presently-existing CMOS support cards and CMOS card incompatibility with many existing STD cards, numerous STD product makers have or are about to introduce entire CMOS STD-Bus card families. When this stampede really gets under way, perhaps by late this year, we will see sealed STD-Bus, all-CMOS card cages enter the tough environments of factories, machine shops, garages (in dynamometers and wheel aligners, etc), bakeries, chemical plants, construction (cranes, etc) and in thousands of yet-untapped commercial and industrial applications that no other μP systems nor buses were tough enough to enter until now. I suspect that the STD Bus makers and their OEMs are poised on the edge of an explosive growth, perhaps unequalled by any other bus.

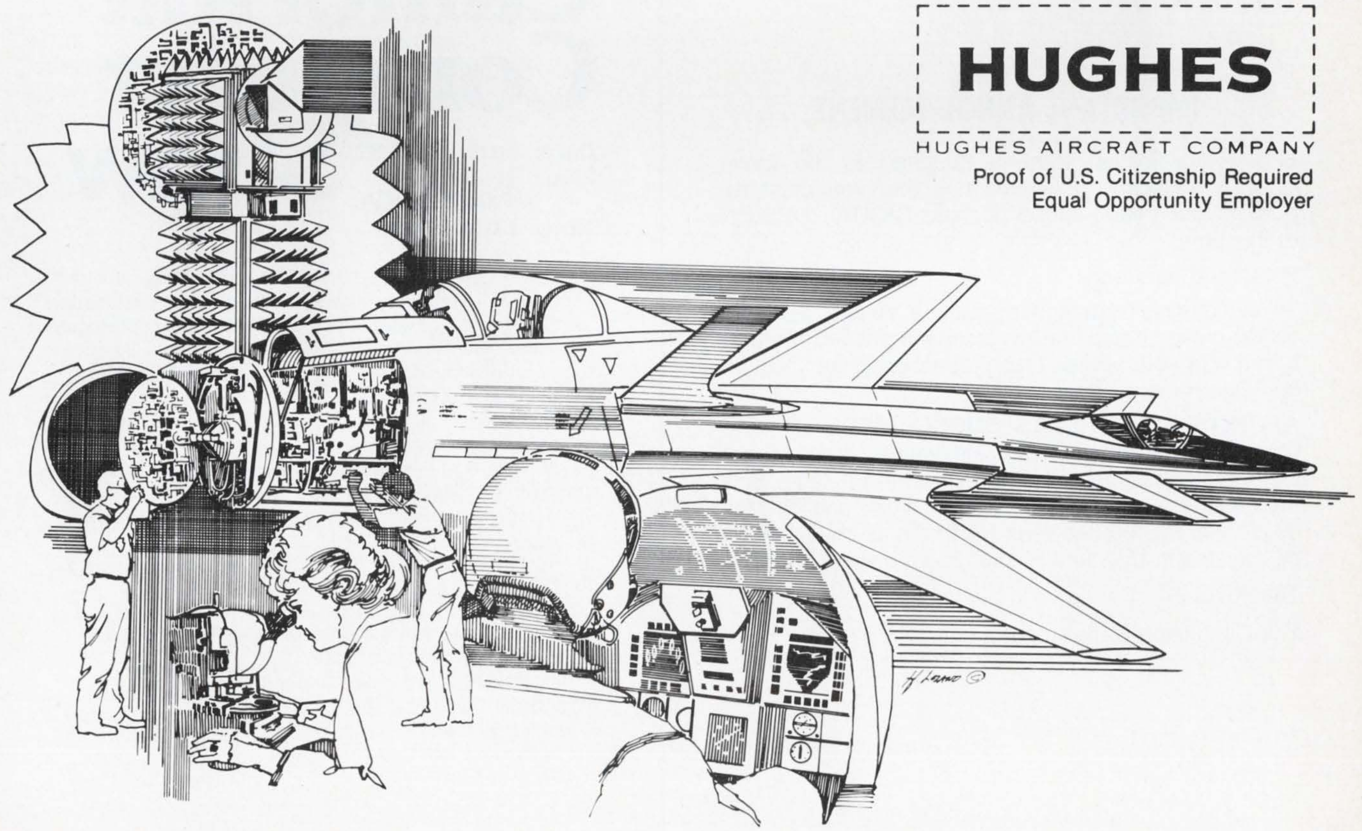
There is a problem in the lack of CMOS bus-driver chips. It is possible that a CMOS STD Bus will emerge as a STD Bus spec subset. This seems likely, and it is a development worth watching. With an all-CMOS STD system, it is possible that the low power requirements will permit opening up more lines for other needs, such as memory expansion.

Another exciting development is the expansion of the 16-bit μPs into the STD Bus, as well as system memories that will be well in excess of the 64-Kbyte maximum directly addressable with the 16-address bus pins. With more common availability of 64-Kbit chips, these over-64-Kbyte STD Bus systems will become fairly common. As chip capabilities and capacities rise, the smaller size and form factor of the STD card is becoming less of an objection, but is becoming a liability for the bigger bus boards.

The trend is toward larger

STD BUS CARD PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OH} (high-state output voltage)	V_{CC} = MIN I_{OH} = -15mA V_{IL} = 0.8V V_{IH} = 2V	2.4	—	V
V_{OH} (high-state output voltage)	V_{CC} = MIN I_{OH} = 24 mA V_{IL} = 0.8V V_{IL} = 0.2V	—	0.5	V
V_{IH} (high-state input voltage)		2.0	—	V
V_{IL} (low-state input voltage)		—	0.8	V
T_R, T_F (rise time, fall time)		4	100	NS

Figure 5: Logic signal characteristics. The STD Bus is TTL-compatible. Input loading/output drive is specified (under worst case conditions) in unit loads, defined as 20μA for max. high-level input-current, and -400μA for max. low-level input-current. Thus, a 50-unit output can drive 50 cards with one-unit load inputs.



	REFRESH*	MCSYNC*	STATUS 1*	STATUS 0*
	PIN 37	PIN 38	PIN 39	PIN 40
8080	–	SYNC*	M1*	–
8085	–	ALE*	S1*	SO*
NSC800	REFRESH*	ALE*	S1*	SO*
8088	–	ALE*	DT/R*	SSO*
Z80	REFRESH*	(RD* + WR* + INTAK*)	M1*	–
6800	–	02*	VMA*	R/W*
6809	–	EOUT* (02*)	–	R/W*
6809E	–	EOUT* (02*)	LIC*	R/W*
6502	–	02*	SYNC*	R/W*

* Low-level active
— Not used
R/W* Read high, write low
DT/R* Data transmit high, receive low

Figure 6: 8-bit μP peripheral timing control lines. Pins 37–40 are defined differently depending upon the μP. Here are nine popular micros. For others contact the individual card makers.

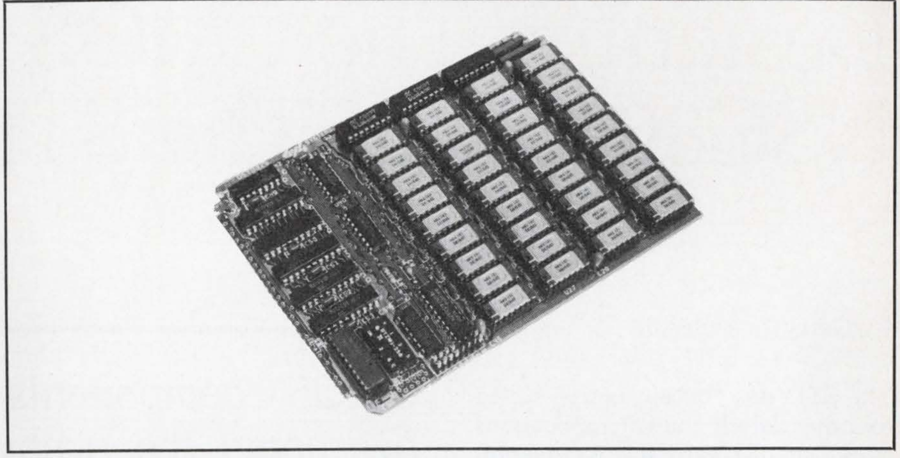
memories with larger word size and word number. The semiconductor makers obviously strongly support this trend, for good accounting reasons. Since memory device costs are falling, semi makers must make more profits from selling greater quantities of memory devices, boards and subsystems, as well as μP development systems, in-circuit emulators and other aids. Larger word sizes help provide the impetus to sell more memory, and they make more money.

The problem is that the data processing-related markets require lots of memory that many control automation, process control and other commercial and industrial applications simply do not need. Nor do these applications require costly development aids in many instances. Semi makers are interested in what they can make more money at; and, consequently, anything that might hinder this would not receive their blessings. This has not always helped designers and OEMs in control automation, process control, industrial engineering, and related design areas. Since these designers do not represent as great a relative market as the data processing-type applications, their best interests (when they conflict with dp-types) obviously will not receive first priority.

Standard Standards

As for IEEE STD Bus standards, the IEEE authorized a working group (No. P961) last October to draft an STD Bus standard in one

Various CPU types and their varying speeds can make it difficult to select interchangeable cards that will work together.



Providing 256K of dynamic RAM, the DSTD-325 card from dy-4 systems, Ontario, Canada is available in 4.0 and 2.5 MHz versions. A single Z80 instruction is used to place any one of 32 8K pages in a processor's 64K address space.

year. The group chairman is the STD Bus creator, Matt Biewer. The group is separate from the non-profit STD Bus Users Group (Bill Shields, Chairman) STDUSR (8697 Frobisher St, San Diego, CA 92126). The P961 draft proposals include STDMG specs and a central timing spec to cover I/O handling and memory. As mentioned earlier, various CPU types and their varying speeds can make it difficult to select interchangeable cards that will work together. The control timing spec approach defines key bus timing, making intercard selection easier.

For those looking for STD-Bus literature, we suggest you contact either STDUSR or a local group that by joint agreement can provide literature: J2 LTD, Technical Publications, 1368 Gertrude St, San Diego, CA 92110. The extra reading could be well worth your while, since, in many applications, STD Bus components are unequalled as low-cost, modular, computer building blocks. □

Designing The CMOS NSC800 Onto The STD Bus

by Garry J. Anderson

The STD bus concept is well suited to industrial μP control applications where smaller card size is advantageous. However, three major problems exist at most industrial sites and they conflict directly with currently available STD systems. These problems are electrical noise, wide temperature fluctuations and power outages necessitating a battery backup system. All of these problems are overcome by using an STD Bus system designed with CMOS components.

To be useful, a CMOS STD Bus system must be designed to be compatible with the existing Bus. In addition, it must be entirely CMOS since one LSTTL or NMOS chip would prevent the system from attaining full CMOS temperature range, noise immunity and low power performance.

Design Requirements

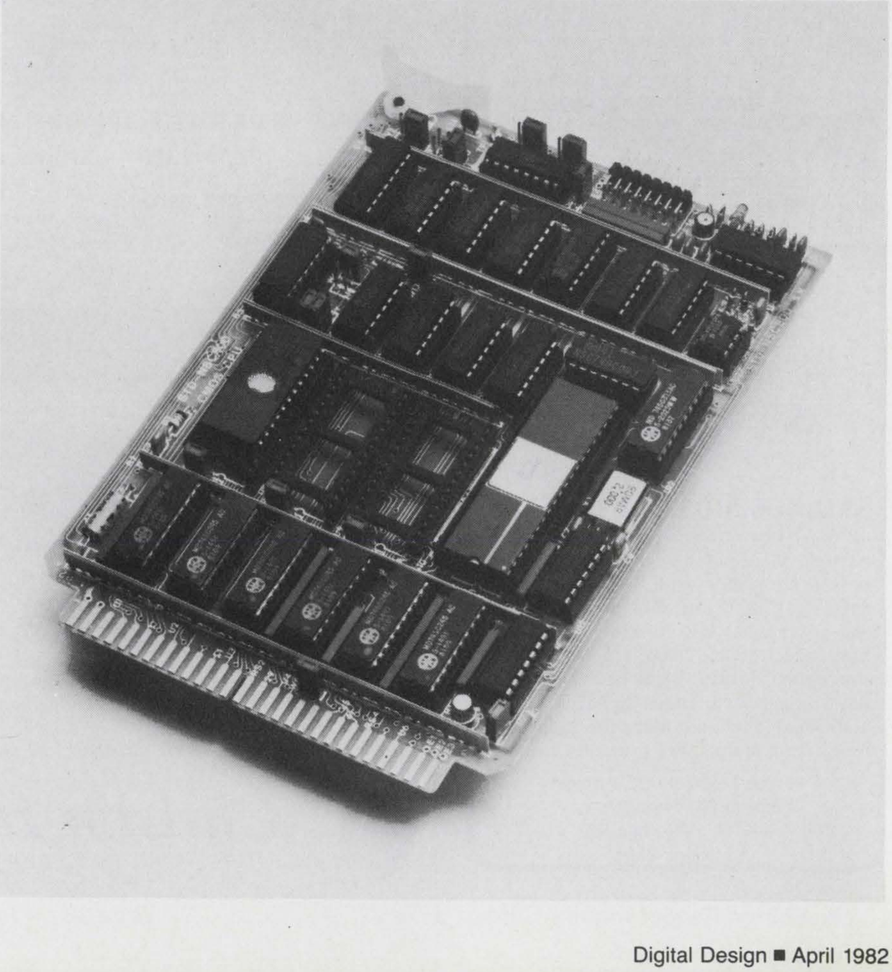
To design an STD-NSC800 CPU card, we must first establish some design requirements. Having established these, we can then proceed to implement them if possible. The design goals are:

1. Compatibility with existing STD Bus specifications.
2. Bus timing signals generated to be compatible with existing 8080/8085 and Z80 peripheral chips.
3. Use of the NSC800 to maximum potential.
4. At least three byte-wide (28-pin) memory sockets on-board for either ROM or RAM.

Garry J. Anderson is Product Engineer at Baradine Products Limited, PO Box 86757, North Vancouver, B.C., Canada V7L 4L3.

CMOS components overcome the problems inherent in using the STD bus for μP control applications.

5. Memory Map Decoder PROM for flexible addressing of the onboard memory sockets.
6. Use of the NMC27C16 CMOS UV EPROM and TC5516 CMOS RAM for best memory performance.
7. On-board Jump-on-Reset address capability and Memory Expansion (MEMEX) port for bootstrap operation with a CP/M operating system.
8. On-board power-fail detector to stop the processor on power-fail.
9. On-board interrupt flip-flops for the three built-in restart interrupts. External access via the user's edge of the card.
10. All components to be CMOS with the possible exception of some MIL-SPEC linear devices.



PARAMETER	STD BUS (74LS245 Drivers)	CMOS BUS (74SC245 Drivers)
Sink Current at V_{OL} = 0.5 volt	24mA	12mA
Source Current at V_{OH} = 2.4 volt	– 15mA	– 14mA

Figure 1: Bus Drive. Trade-offs resulting from existing bus driver chips determine the CMOS BUS properties.

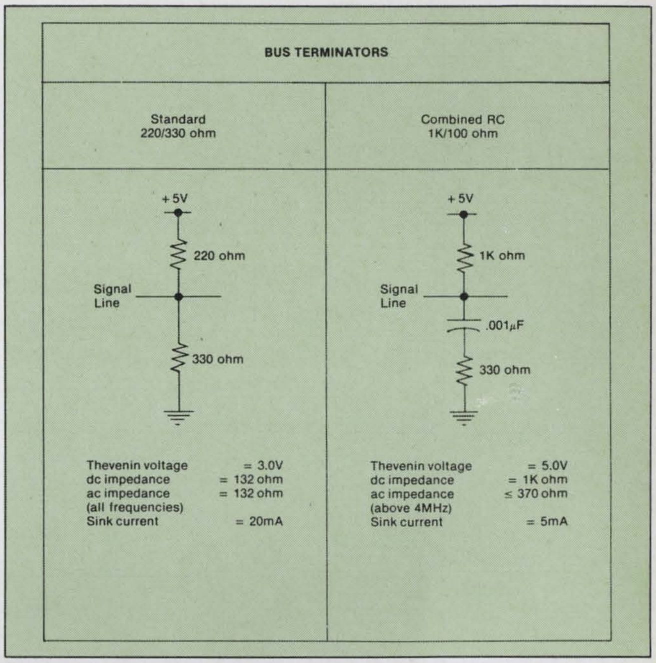


Figure 2: Bus Terminators. A low power, high performance RC bus terminator eases CMOS drive requirements.

The STD Bus

The existing STD Bus specifies mechanical card size as well as the electrical properties of the Bus (see STD Bus Specification and Practice available from Pro-Log Corporation). **Figure 1** summarizes the bus drive requirements. Existing 74LS245 bus drivers are more powerful than their CMOS counterparts. Hence, a trade-off is necessary to reduce the bus drive requirements to that obtainable from existing CMOS chips.

At present, only RCA and Mitel make CMOS bus driver chips with respectable speed (30 ns) and drive current (12-30mA). Unfortunately, the powerful CD40115/40116 (30mA) is only available as an inverting driver and RCA has no plans to make a non-inverting version. Fortunately, Mitel has both inverting (MD74SC545) and non-inverting (MD74SC245) bus drivers available. Therefore, the first design decision is established: Mitel (or equivalent) bus drivers must be used for driving all bus lines in order to achieve the performance shown in Figure 1.

At present, no specification exists for terminating or shielding the STD Bus. In order to minimize the generation of cross-talk noise and bus "ringing", it is essential to terminate every signal line with a low impedance. This has traditionally been accomplished by using a 220/330 ohm terminator network or more recently, by using active termination techniques. These terminators provide an ac/dc impedance of approximately 132 ohms and require a sink current of 20mA.

A better terminator is shown in **Figure 2** which has two advantages

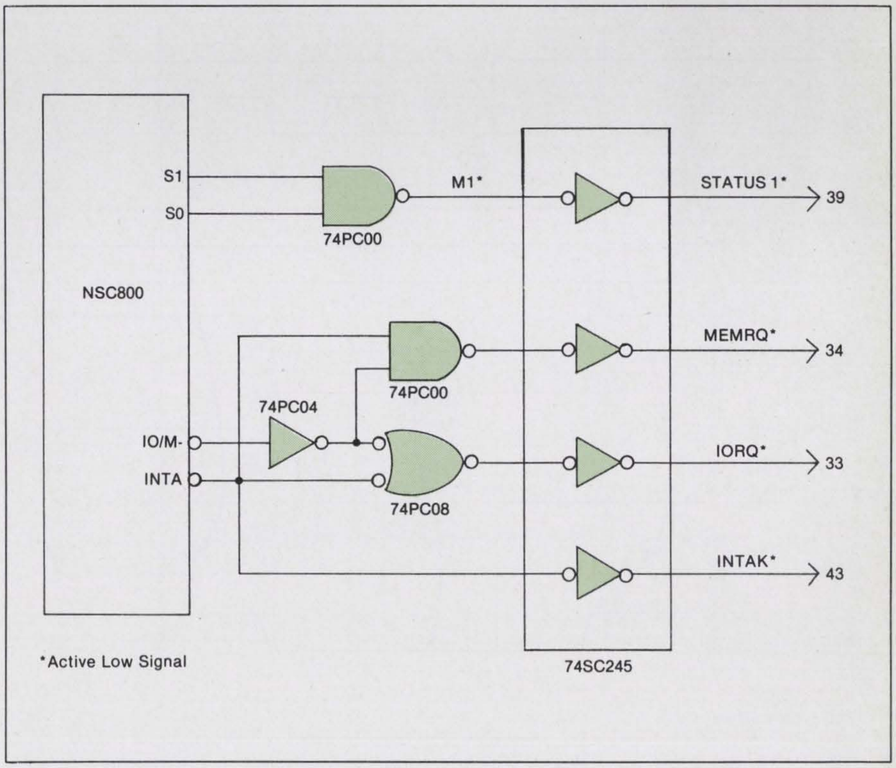


Figure 3: Bus Timing. Compatibility with 8080/8085 and Z80 peripherals is achieved by on-board logic to generate the correct timing.

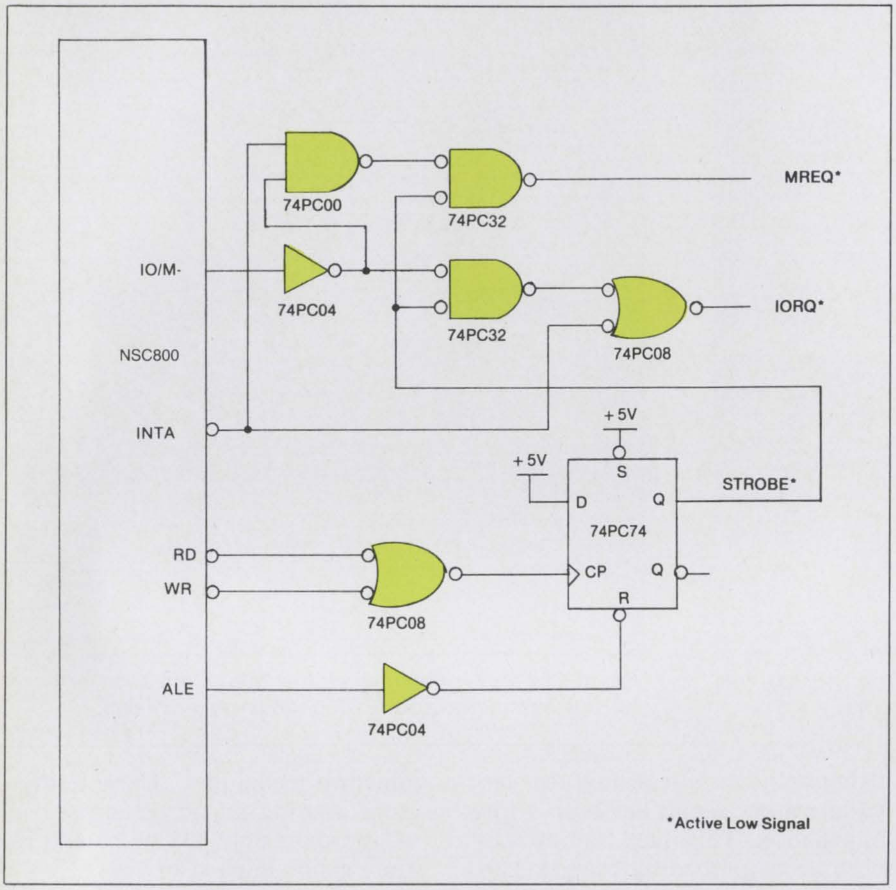


Figure 4: Memory Timing. A valid memory address strobe must be generated to permit the use of synchronous and dynamic memories in a system.

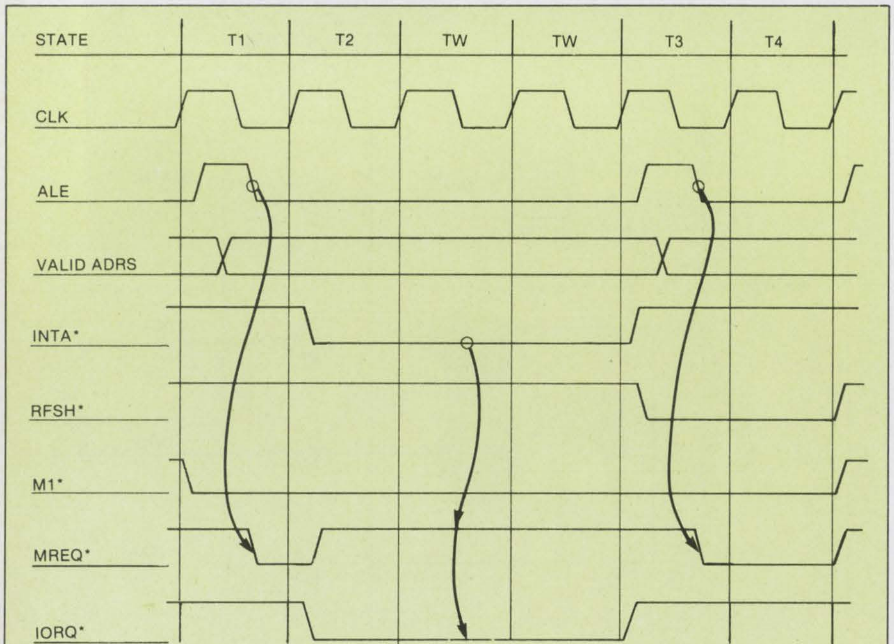


Figure 5: Timing Diagram. The NSC800's Mode 2 Interrupt Acknowledge/Refresh Cycle is complemented by a strobed MREQ and IORQ* line in an attempt to be compatible with existing peripherals and memory systems.*

over the standard terminator: it requires a dc sink current of only 5mA, and it pulls up the signals to 5 volts instead of 3 volts providing slightly better noise immunity in the high state. For signal frequencies above 2MHz the impedance of the .001μF capacitor is low enough such that the 330 ohm ac impedance becomes effective.

The lower power drive requirements of this terminator make more sense for the CMOS bus drivers available. The existing CMOS drivers will not drive the standard 220/330 ohm terminators and remain within specification.

In order to maintain TTL voltage level compatibility, Mitel has compromised on the inherent noise immunity of CMOS logic by reducing their threshold levels to that of TTL. What could have been 1.5 volts of noise immunity has been reduced to 0.8 volts, a 50% sacrifice. National Semiconductor has done the same thing with the NSC800 input thresholds. Unfortunately, these compromises tend to negate the noise immunity afforded by the rest of the CMOS logic in the system.

Bus Timing

Since the NSC800 has the instruction set and features of the Z80, it should be able to work with existing Z80 peripheral chips for maximum utilization of the CPU's features. This would include Mode 2 vectored interrupts and transparent refresh cycles for dynamic memory systems. However, since it is packaged like an 8085 which did not support either Mode 2 interrupts or dynamic memory refresh, an incompatibility exists between the NSC800's pin-out and timing signals and the requirements of the Z80 peripheral chips. It is therefore necessary to generate additional timing signals on-board to approximate the Z80 timing.

Figure 3 shows some of the logic necessary to generate the correct interrupt timing signals for the Z80 peripherals. The op-code fetch (M1) signal is easily generated from the state codes (SØ, S1). The Z80 interrupt acknowledge cycle requires both M1 and IORQ to be active simultaneously. This is achieved by

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ORing the NSC800's INTA signal onto the IORQ line. If this timing is not generated it may not be possible to use Mode 2 interrupts with some Z80 peripheral cards already in existence.

A problem also exists with memory timing if either synchronous or dynamic memories are to be used. Both types of memory require a strobe pulse which occurs after a valid memory address (AØ... A15) has been established. The Z80 MREQ signal performs this function since it is pulsed during every memory cycle including refresh. It can therefore be used directly to strobe synchronous memory chips and generate RAS-only refresh cycles whenever the RFSH status line is active.

Unfortunately, the NSC800 does not directly have such strobed signals due to the 8085 style pin-out. The status signals IO/M- and RFSH cannot be used as a strobe since the full 16-bit memory address is not valid when they first occur. Therefore, external logic must be used to generate a strobe signal which begins after the memory address is valid (after ALE has latched the address). The strobe ends after the current cycle (RD or WR) is finished. **Figure 4** shows the logic required to generate suitable memory timing signals. Note that an address latch (not register) must be used by ALE in order to establish some finite memory set-up time before the strobe is generated.

Another problem exists with the NSC800 timing during interrupt acknowledge cycles. During the first half of the cycle the IO/M- status should be high indicating an I/O Fetch Cycle (like the 8085) and during the last half it should be low indicating a memory refresh. However, since IO/M- cannot change state in the middle of a machine cycle, the NSC800's IO/M- line stays low throughout the entire cycle, creating a slight departure from 8085 compatibility.

Figure 5 shows the NSC800's timing waveforms during the critical Mode 2 interrupt acknowledge/ memory refresh cycle. The strobe signals MREQ* and IORQ* generated by the logic in Figure 4 are also shown. Note that the NSC800 automatically inserts two wait states while INTA* is active. This timing diagram demonstrates that MREQ* is pulsed correctly during refresh but is unwanted before INTA*. Hopefully, this will not cause a problem with existing cards.

Memory Option	Socket 0	Socket 1	Socket 2
0: Standard Configuration	0000-07FF (2K ROM)	0800-OFFF 2K ROM)	1000-17FF 2K RAM)
1: More RAM	0000-OFFF (4K ROM)	1000-17FF (2K RAM)	1800-1FFF (2K RAM)
2: More ROM	0000-OFFF (4K ROM)	1000-1FFF (4K ROM)	2000-27FF (2K RAM)
3: Bootstrap Jump-on-Reset	E000-E7FF (2K ROM)	E800-EFFF (2K ROM)	F000-F7FF (2K RAM)
4: MEMEX Active	Disable all on-board memory		

Figure 6: Memory Map. On-board CMOS Memory Address Decoder PROM provides the address map shown here. Mapping PROM can be modified to achieve different memory maps.

Users of the NSC800 should be aware that they may experience problems making the NSC800 work with existing Z80 peripheral cards and dynamic memory systems unless additional logic is added.

Memory Addressing

Byte-Wide (28-pin) memory sockets are required to maintain compatibility with future memory chips. Sockets must be designed to accept either RAM or ROM via jumper options. A CMOS memory map decoder PROM should be used to provide memory address flexibility. The Harris HM-6611-9 CMOS 256 x 4 PROM works nicely as a map decoder since all parts appear to be faster than specified. Five address lines A15 through A11 are used by the PROM to provide addressing capabilities on 2K boundaries.

Figure 6 shows the on-board memory mapping options available. These options are jumper selectable using two of the remaining three inputs to the decoder PROM. The third input is used for memory expansion and disables all the on-board memory.

In order to achieve proper bootstrap operation, an on-board I/O port is provided containing two control bits. One bit controls the alternate address logic (0000 or E000) and the other bit controls the memory expansion (MEMEX) line on the STD Bus. The initial jump-on-reset to E000 is jumper selectable as well as software controllable. For a full 64K CP/M system to be obtainable,

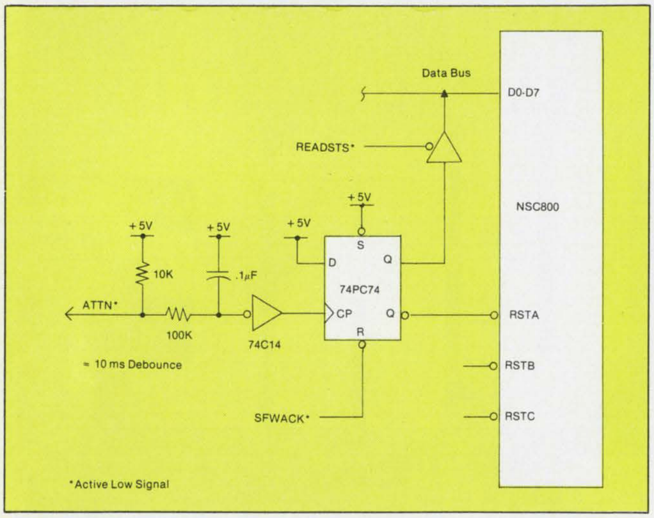

Figure 7: Restart Interrupts. Each of the three NSC800 restart interrupts has logic similar to that shown here. A software acknowledge allows interrupts to be cleared.

the MEMEX control bit allows the bootstrap EPROM to shadow out upper RAM during loading from disk and then disappear completely after loading.

An on-board wait-state generator is required for memory access from EPROM since the NMC27C16 is very slow (650 ns). Jumper selectable control of the generator allows wait states to be inserted during all Op-Code Fetch cycles (M1 only). All I/O cycles have one wait state automatically inserted by the NSC800. Mode 0 and 2 interrupt acknowledge cycles have two wait states automatically inserted. Additional wait states are obtainable via the STD Bus WAIT* input.

Interrupts

Since the NSC800 has plenty of interrupt features, the CPU board should be designed to make the maximum use of them. The Non-Maskable (NMI) and regular interrupt (INTR) are available on the STD Bus, hence this is where they should be used.

These built in level-sensitive restart interrupts are available in the NSC800. The most convenient method of accessing these is via a connector on the User's Edge of the card. The inputs should be debounced using a 74C14 Schmitt trigger and should set individual flip-flops. Each flip-flop must be software resetable via the on-board I/O port. Sensing of these flip-flops should be available for non-interrupt driven applications. Interrupt enable masks are already provided within the NSC800 via I/O port 'BB'. **Figure 7** shows the typical restart interrupt input flip-flop design.

Conclusions

Figure 8 shows a block diagram of the CMOS STD-NSC800 card design. All of the design goals have been attained and the result is a fully CMOS microcomputer card compatible with the STD Bus (with relaxed drive requirements). The performance of the card should be measured in terms of the original design objectives as follows:

The noise immunity of CMOS logic is typically 1.5 volts (at 5V Vcc) in either high or low state which is a two-fold improvement over the TTL noise immunity in the low state (0.8 volts). Unfortunately, the CMOS bus drivers and the NSC800 itself reduce the system noise immunity to that of TTL.

The operating temperature range of the card is typically $-40°C$ to $+85°C$ limited in part by the NMC27C16 EPROM. Industrial grade components are needed to achieve this temperature range.

The power consumption of the card with full memory is a mere 50mA at 5 volts and 1MHz. Battery back-up systems are feasible at these power levels.

No problems have been experienced driving the RC terminated STD bus as discussed earlier. When the STD-NSC800 CPU card is combined with the companion CMOS STD cards, a low power, moderate noise immunity, battery backed-up industrial control system is obtainable. □

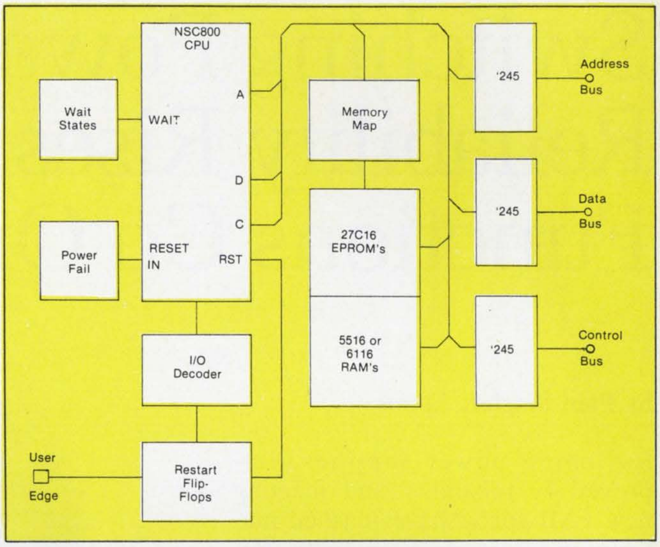

Figure 8: Block Diagram. The STD-NSC 800 card includes mapped bytewide ROM/ RAM and on-board restart flip-flops. Entire board is CMOS.

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Switching Power Supplies: Reliability Rises As More Functions Go On-Chip

by **Paul Snigier**, *Editor*

Switching power supplies, improved in reliability and meeting new EMI specs, have reached maturity in terms of designability. Future improvements will be less in materials and higher frequencies than in more sophisticated control ICs and associated chips. By integrating more switcher functions into silicon, MTBFs will drop further and MTTRs will rise. But, perhaps the greatest development beginning to take place is that of growing added-intelligence in switchers.

A switching power supply contains a bridge rectifier, switching transistors, pulse-width modulation control circuits, feedback network, high-frequency transformer, output rectifiers and filtering network. All compare output voltage to a reference with a control circuit to vary the series switching transistor on-to-off ratio at about 20 to 45 kHz. This chopped current passes through to an output filter.

Saturated transistors are not lossy, so efficiency is 60 to 90% or so, producing higher power, density, compactness and less heat dissipation and forced air or fan cooling. Faster pulse-rep rates mean inductors, filter caps and transformers are smaller and lighter, consuming less raw materials, like iron and copper, and thus lowering costs. They ride through temporary line-voltage drops or brownouts and sustain output levels for 20 to 40 ms.

Switcher specs differ from linear specs. Though not all supplies fall into the following ranges, they do provide a general comparison. Typical specs are: Size (W/in^3) is 0.5 (for linears) and 2 (for switchers); efficiency (%) is respectively 40–55 and 60–85; power density (W/lb) is 10 and 50; ripple noise (mV-pk-to-pk) is 30 and 50; line cycle carryover (ms) is 2 and 25–50; transient recovery time (μs) is 25 and 500; and input voltage tolerance (%) is ±10 and greater than ±20; and regulation (%) is 0.1 and 0.1.

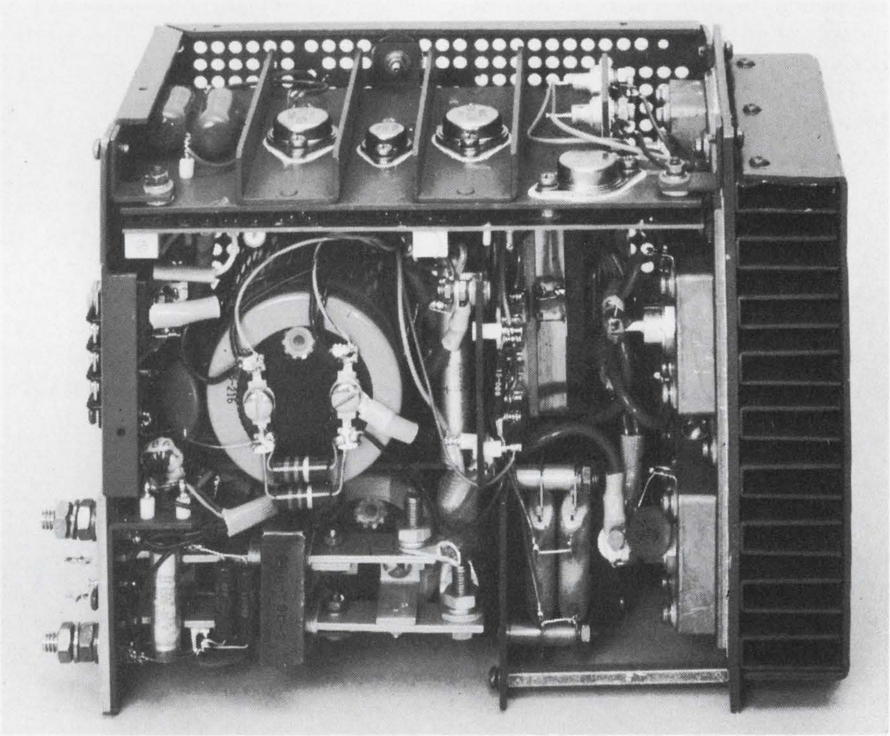

Figure 1: The trend is to optimized cooling and higher efficiency switchers, such as this 120-A Lamda open-frame convection-cooled switcher (5V to 128VDC).

Switchers have a lower degree of stabilization, inrush current woes, higher noise, switching spikes and higher prices for lower-power applications. Transformer imbalance in high-power push-pull switchers can cause failures (although twin-pulse PWM circuits alleviated this). In multiple-output switchers, getting desired outputs simultaneously isn't always easy, although better designs and new components have lowered costs, reduced noise and spikes, increased efficiency and raised reliabilities.

Switching Supply Groups

Categories into which switchers fall include: forward, flyback, half- and full-bridge push-pull converters, and also combinations of these types. The simplest, with least parts, is the one-transistor flyback converter or blocking oscillator. Lowest in cost, it was used for switchers up to a few hundred watts. It's simple and the regulator's clean waveform (in terms of the transformer field or line currents over time) provides superior suppression of RFI. This means that less high-harmonic energy exists. Flybacks are in multiple-output switchers because each output needs only one capacitor and diode, making it simple. Smoothing, however, can be trouble when ripple is bad.

You don't get something for nothing in life, and the same goes for switchers. As with all low-cost circuits, there's a tradeoff of high ripple and poor regulation. Flyback transformers give a large inductive kick that doubles primary voltage, although the switching transistor is only partially off. It must withstand peak currents four times exceeding average at double the voltage for several tenths of a μs. Flyback converters often destroy bipolars, and over-specing is done. Power MOS transistors can handle it; they turn off in tens of nsecs and are more thermally insensitive than bipolars.

Flyback transformers possess tens of μH; and, the core's B-field ($B = \mu H$) is not intense, so there must be more volume to store energy. This is retained during half cycles and not passed from primary to secondary. Some flybacks circumvent this with higher frequencies and lower ferrite permeability or use a medium-permeability core with an air gap for storing magnetic energy.

But, despite problems, the flyback regulator has advantages. The transistor series impedance means that collector-current rise-time is well-controlled and relatively slow, so it is possible to turn off the transistor before the core saturates. Also, during the charge cycle, the secondary completely disconnects from the primary; if a secondary fault occurs, it's not directly reflected back to the primary.

More problems exist: the flyback regulator operates at duty cycles wider than under the clock period, giving this regulator a very large dynamic range. Multiple regulated outputs are possible using a flyback regulator, with regulation from two of these secondaries by regulation of the third. Conversely, transformer regulation is under a conventional DC-to-DC converter because the core material provides worse coupling. However, some vendors tighten regulation by using multifolor and parallel-windings.

For greater power increases in the output, paralleling of stages is done. Since stages are essentially unlimited, output power is (within reason) unlimited. This inherency is due to these transformers being current sources, not voltage sources. By timing the parallel stages so their transformers dump stored energy onto the load on a staggered basis, ripple is reduced. Obviously, reliability will be high, as we said earlier, but can be increased if enough stages exist so any one failure will not affect the load. This is done by fusing the secondary diodes and primary transformers. When one fails, it is removed from the primary and load.

Forward converters use one switching transistor, offering low output ripple, and are for lower-voltage, higher-power uses (more so than flybacks), although most outputs are not above several hundred watts. As inductor cores are driven unidirectionally, power flywheel diode and a series inductor with the load make for a steady current in spite of switching transistor switching.

Adding more critical functions on-chip is improving switcher reliability and repairability. Added intelligence is the next step.

Duty cycle limits of many forward converters at a time saturate the main power transformer. This causes switcher failure. Although this once was a problem, it no longer is.

Push-pull converters, though using two or more power transistors and two flywheel diodes, do provide higher power output, lower ripple and more efficient bidirectional use of transformer cores. Ripple is lower because of doubled frequency, which makes the filtering easier. Naturally, push-pull switchers, though more costly, are popular for these reasons.

With single-ended or half-bridge circuits—the latter withstand double line voltage, being suited for low- to medium-power switchers—then push-pull regulators must use two or more switching transistors. If using a full bridge for more power, then four are used. Paralleling up to eight or so power transistors boosts overall current capacity.

As for push-pull problems, although they create the lowest output ripple, they do have the most complex base drive of all. The converter, if excessive positive feedback saturates the transformer core, may latch or hang up in one state no matter what the driving circuit does. Core saturation, caused by cross-current saturation, takes place when all switching transistors conduct simultaneously. Core saturation occurs from DC imbalance. Push-pull converters are limited in input range. This is overcome by a switching regulator before the push-pull. A tradeoff exists: a noisy switcher-push-pull combination that is inefficient, degrades isolation and recovers slowly from line transients.

Control ICs eliminate push-pull troubles, especially for high-power units, where the problems and their effects can be worse and more costly. Pulse amplitude and pulse width imbalances were the cause of push-pull switcher destruction, although transformer imbalance was largely solved by the twin-pulse circuit without the cost and other problems of overspecifying the transistors. As one pulse is wider than the other due to load variations, one push-pull transistor is driven harder. Its transformer flux is going to be greater, leading to lower diode PIVs (peak inverse voltages). Conventional push-pulls drive the transistors directly with a narrower pulse for a rising output to shorten on-time to provide negative feedback and lower the output.

Conversely, the twin-pulse,

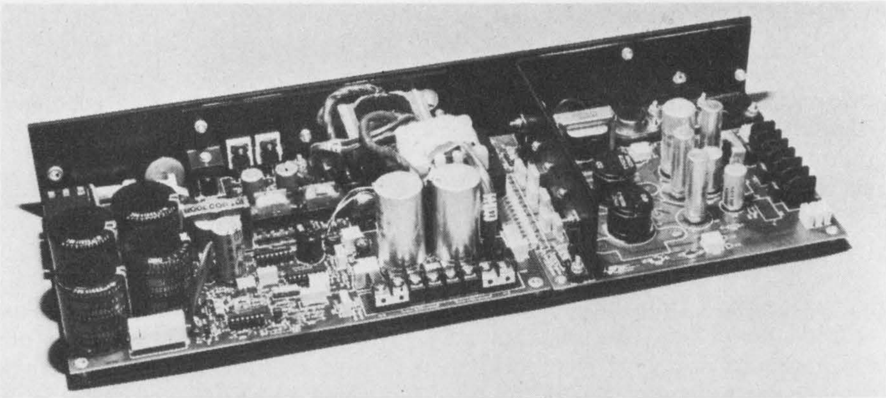

Figure 2: Increased functions built into power supplies, such as this National Power Technology 400W open frame switcher, include built-in line filtering and soft start circuitry, LSI control circuitry, built-in remote sense and OV output main and auxiliary protection, power-fail detect, remote inhibit and other options and features.

pulse-width modulation control IC applies one output to one transistor. A flip-flop is set by the other PWM pulse to provide an identical pulse delayed by T/2 to the second switching transistor, thus circumventing the trouble neatly.

ICs Improve MTBFs And Reduce MTTRs

Most switcher failures are traceable to a small percentage of their components. These are usually things like electrolytic capacitors, pots, power diodes and transistors. Integrating more housekeeping functions onto a chip, particularly if these are the failure-causing functions, can greatly raise MTBFs. Which functions are they? If these functions involve capacitance, inductance and transformers, pot cores and the like, then if they are lowered or minimized by the new control ICs, reliability will be raised. In addition, by reducing high-power and high-voltage components, newer control ICs not only reduce stress, but also reduce internally-generated heat. This, in itself, raises MTBFs. But control ICs help in other ways. PCB links are reduced and (hopefully) greater care can then be taken in partitioning functional sections. This results in improved reliability and cross-talk variations, as they are all assembly-dependent factors.

Although military grade components provide a 350% increase in MTBF reliabilities, and can be well worth the added cost in the long run, some switcher manufacturers raise reliabilities in a different way, and it doesn't cost an extra cent. They juggle statistics. Many OEM's are well aware of the power supply specsmanship game, but still select an initially lower-cost switcher. Some OEMs know very well the long term costs of these certain switchers, but couldn't care less. Smaller OEMs often may not care, as they may be startups, or struggling to survive, and either have no choice or may not be around in five years. Or, the individuals within the firm may not anticipate being with the firm in five years when the tradeoff point on field repair costs cross savings from the initial buy. Many other OEMs try to avoid this situation.

Specsmanship has soured many users; and, one power supply maker told us that he himself wouldn't trust anybody's specs in this business! Certainly, traditional MTBF calculations are more meaningless for switchers than for linears: they often don't account for real-life applications. For power supply design and selection criteria see, "Principles Of Designing And Specifying Power Supplies," P. Snigier, *Digital Design,* Nov. 1981, pp. 52–57.

How to raise MTBFs and lower MTTRs is well-known by every supply maker. An MTBF improvement of 800% is possible with only a 50% increase in critical component cost. This means better screening, system burn-ins and so on. This would make a $500 switcher into one priced at $750 or so, and certainly an unappetizing design choice. But, look at it this way, it saves in overall cost over five years. In your cost estimating, remember that your n-year cost includes initial cost plus repair cost/failure and space allowance (possibly 10% of initial cost) times the ratio of switcher life to MTBF. Cost of failure also includes cost of outage or revenue for users that buy your system or subsystem, not to mention ill will. If MTTR is not low (half an hour), repair expenses involve field visits, shipping costs, aggravation and delays from out-of-stock items, etc. A repair cost can easily exceed $150.

Traditional MTBF calculations may be meaningless for switchers; they often don't account for real-life applications.

Keep in mind that a two or three-year MTBF switcher costs less than a ten-year MTBF unit for the first four to five years, but that after seven years, that initially-cheaper switcher costs you twice as much. In ten years, it's going to cost up to three times more for your company. Some OEMs claim that the break even point is closer to four or five years, as many factors are involved in each individual case.

Control Circuits

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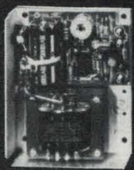

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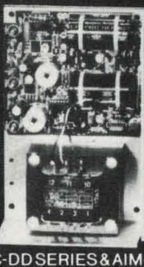

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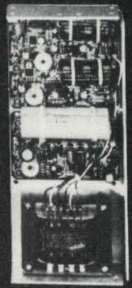

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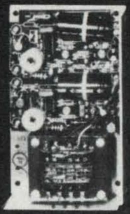

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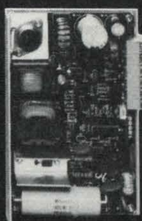

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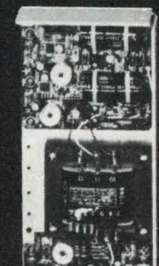

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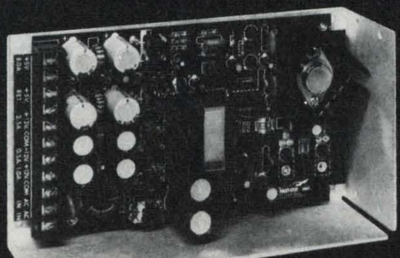

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Creating less confusion among designers, including many supply designers, newer control ICs are easier to design with and provide more functions than earlier circuits. The earlier chips were worse; industry wits two years ago claimed that many of the semi makers manufacturing these control ICs didn't even understand their own product, since they didn't really understand the switching supply business and design problems. This has changed, and more proficient designers exist with up-to-date experience with these recent control ICs. Recent control ICs are growing more sophisticated, with more control and protective housekeeping functions on-chip, thus making switchers a silicon-dependent technology. Instead of designing a cageful of PCBs, today's designer uses a few ICs and modules to take care of conditioning, control and drive functions. The result is smaller size, increased reliability and savings in assembly time, testing and inventory control.

The newer single chip ICs provide more control functions, compactness, reproducibility and accuracy, and offer increased reliability.

New and superior chips, many with improved versions or new families, are being introduced by older-line firms established in the field or by new firms entering it. These newer control ICs provide more functions, such as more accurate references, dual output drives that source and sink more, oscillator synchronization, on-chip power driving, error amplifier, adjustable current-limit amplifier, spare output transistors, wider frequency ranges, independent sensing and overvoltage and multi-level current limiting, stop-start latch for fast switch-offs or slow starts, remote on-off controls, adjustable dead time, limited self-test and line monitoring, and other functions. Improvements in materials may be slower in coming now that 80% of these improvements have been already made. The switcher's future is that of adding functions into silicon and increased intelligence. □

ELECTRO '82 Preview

By Nicolas Mokhoff and Dave Wilson

Technical sessions addressing the leading edge of computer design highlight the Electro '82 conference.

At least ten technical sessions of this year's Electro '82 Professional Program address issues that are of interest to the computer designer. Topics range from Object-Oriented Systems and Languages to Logic Designs for Interfacing Systems in the 1980's.

Electro organizers expect a record 45,000 to attend this annual event that will be dispersed between the Hynes Auditorium and the Sheraton Boston Hotel in Boston, MA. The three day show and professional program is sponsored by the Institute of Electrical and Electronics Engineers and will be held Tuesday, May 25 to Thursday May 27.

Highlighting the show will be keynote speaker Ray Stata, chairman of Analog Devices, Wilmington, MA. Mr. Stata's talk will cover the economic aspects of high-technology companies and the future of electronics in the Northeast. In light of the competition from Japanese and European electronics companies, Mr. Stata will state that "U.S. high technology companies must stand up to the economic challenges posed by their aggressive Japanese counterparts by developing more long-term research and development programs." Analog Devices is meeting the challenge by manufacturing some parts in Japan. Mr. Stata has recently returned from Japan where he formally opened the company's first manufacturing facility.

CMOS For Interfacing Logic

CMOS technology has taken a giant leap forward by adding the benefit of bipolar TTL speed to its list of other features. CMOS's versatility has made it a very popular designers' choice, and a new dimension—that of speed—delivers unbeatable benefits to the user. In the years since the initial products were introduced in the late 1960's, CMOS technology and its manufacturing process have evolved from the initial SSI and MSI functions to LSI, VLSI, memory and μP products, and to high density gate arrays. An ever-growing list of manufacturers have addressed the needs of future systems using the CMOS approach to achieve that technology. Designers have in the past been required to apply the traditional operating characteristics of two basic families—(1) low power dissipation, good noise immunity but relatively slow switching speeds of CMOS, or (2) the higher operating frequencies, faster progagation delays, good fanout or drive capability of TTL, but with a bigger penalty in power. These traditional characteristics are now complemented by those of "High Speed Logic."

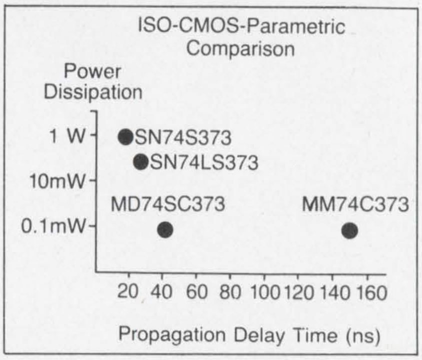

Figure 1: Comparing the performance of Mitel's octal latch with other products.

In this session, four papers will be delivered from leading semiconductor producers of CMOS chips: National Semiconductor, Mitel Semiconductor, Motorola and Texas Instruments.

Larry Wakeman, National Semiconductor, will discuss the company's 54HC/74HC silicon-gate CMOS logic family. He will emphasize their low-power and fast speed, performance features that make the new family comparable with the low-power Schottky speeds of the standard TTL line of ICs.

"To fill the gap between high-speed CMOS μP's and the desire for low-power devices, both National Semiconductor and Motorola are offering the 54HC/74HC CMOS logic family which provides speeds comparable to low-power Schottky TTL circuits, while retaining the DC electrical characteristics of CD4000 and 54C/74C metal-gate CMOS logic families," says Mr. Wakeman. As with standard metal-gate CMOS, these circuits are ideal for battery operated equipment, portable equipment, or any system where low power consumption is critical. The designer can thus achieve higher throughput systems with little increase in overall system power consumption. Since a 54HC/74HC device has about the same speed performance as an LS-TTL chip, it is also ideal for use in systems which require these speeds, but where power is not a primary concern. In these cases, the lower power dissipation

Nicolas Mokhoff is East Coast Technical Editor and Dave Wilson is Senior Technical Editor for Digital Design.

of CMOS can reduce overall system costs by enabling use of smaller power supplies, and reducing cooling requirements, i.e., eliminating fans and heat sinks.

Mitel Corp., a telecommunications system manufacturer, will be touting ISO-CMOS technology, a new generation of CMOS that combines packing density and high-speed. This is important for interfacing 16-bit μP's with high-speed logic on circuit boards that can fit only a certain device density.

Peter Richmond, director of digital product management at Mitel, will elaborate on the characteristics of ISO-CMOS and discuss typical applications. Using the MD74SC373 octal latch as an example of an ISO-CMOS component, **Figure 1** shows process performance compared to other technologies. As shown, the MD74SC373 lies on the same power dissipation axis as a metal gate CMOS, MM74C373. However, the advantage in propagation delays is evident with an almost 375% increase in speed—40ns compared to 150ns. This short delay time is in the same region as that of a low power Schottky SN74LS373 device having around 30ns propagation delay time.

In this comparison, the superiority over a low power Schottky device may be seen as a 3 to 4 order of magnitude reduction in quiescent power dissipation. During operation, the ISO-CMOS device will dissipate increasing power in proportion to increasing frequency of data transfers and bit pattern changes, but not until in the 10MHz region will its power dissipation approach that of TTL.

Gate Arrays For Circuit Design

Mr. Richmond has also organized Session 9: The Gate Array Approach to Circuit Design. "The session will have speakers from gate-array manufacturers as well as established standard IC producers who will discuss the choices that both the user and the IC supplier have to successfully negotiate for a worthwhile business relationship," says Mr. Richmond.

Table of Activity Choices for Suppliers of Standard ICs and Logic Arrays

Activity	Typical Standard IC Supplier	Array Supplier
Logic Function	Supplier Defines	User Defines
Pins	Typically 40 or less	Determined by Requirements
Package	Limited Choices	Determined by Requirements
Interface	Catalog	Computer Terminal
Production Control System	Batch, Inventory Oriented	Real Time, Throughput Oriented
Purchase Criteria	Volume	Service
Corporate Orientation	Efficiency Inflexible Product Oriented	Effectiveness Flexible Customer Oriented
Product Orientation	Lowest Cost Per Function	Lowest System Cost

Table 1: Comparing the organization and methodology of an array supplier to that of a standard IC supplier.

The successful application of a semi-custom IC design may be traced back to the initial definition of the gate array. A supplier chooses the technology for his device based upon his strengths in technology and semiconductor processing, and the particular market he wishes to enter. He could choose among array techniques that include a logic array, a gate array or a transistor array structure. The choice for each array technique depends on the eventual application. Which structure suits what application, and what the proper CAD tools and interconnect techniques, efficient testing routines and programs should be will be discussed in ensuing papers.

In his paper on "Systems Approach To Logic Arrays," Rob Walker of LSI Logic Corp. of Milpitas, Calif., will discuss his company's system approach to their logic array design and production. He will compare the organization and methodology of an array supplier to that of a standard IC supplier as illustrated in **Table 1.**

According to Mr. Walker, the scaled HCMOS technology will be the principal general-purpose logic array technology of the future. While ECL will remain dominant for very high performance applications, chips made with bipolar technologies such as TTL, I^2L, ISL

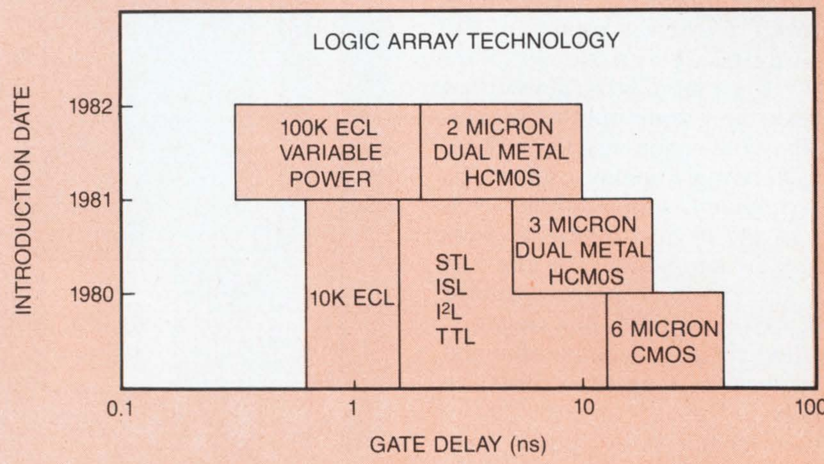

Figure 2: The scaled HCMOS technology will be the principal general-purpose logic array technology of the future according to LSI Logic Corp.

and STL are being outperformed by chips produced with HCMOS. (**Figure 2**).

Analog to Digital Converters

Many unique design features will be highlighted for the engineer who attends the A/D converter sessions.

Brian Gillings, Application Manager at AMD, will outline the use of the Am6112, an industry first 12-bit monolithic ADC that performs accurate conversions in 3μs. According to Mr. Gillings, the resolution (0.024%) and conversion rate of the device will create a whole new range of applications. The Am6112 was designed so that the device would interface to many different μP's, with a variety of conversion initialization, and output data read modes. **Figure 3** shows the AM6112 as it would be interfaced to an Am8085 μP with a 4MHz external clock, the conversion time is 3.3μs. The $\overline{RD}$ and $\overline{WR}$ lines are directly tied to the system's $\overline{IOR}$ and $\overline{IOW}$ control lines. In a minimal system, $\overline{CS}$ could be a dedicated address line. The upper/lower byte pointer C/$\overline{D}$ is tied directly to address line A_0. The only constraint on the data location is that A_0 should alternately be a zero and a one.

Interfacing with μP's will also be discussed by Jerry Whitmore and Mike Hynes from the Analog Devices plant in Ireland. They will describe a 10-bit A/D converter with easy 8-bit interfacing and a minimum of external components among its design goals. The AD7571 is a monolithic device that features three state outputs providing the conversion result in 70μs. A differential analog input has been provided, adding to the versatility of the device. **Figure 4** shows the main components of the device. It consists of a 10-bit voltage mode DAC with thin film resistors, switched capacitor comparator and a successive-approximation register.

Also included are input level shifters to give TTL-compatible logic levels and three state output drives that can drive a low power TTL load. The device normally uses three power supplies, V_{DD} = + 15V, V_{SS} = − 15V and V_{CE} = +5V.

Design Tools for the 80's

The key to engineering success during the 1980's will be the availability of more powerful and sophisticated Computer Aided Engineering (CAE) tools. Session 5, organized by Tektronix's Sharon Van Sickle, addresses this issue. "This session will explore some of the emerging processes, tools, and techniques that will alter the design and development environment of the next decade," says Ms. Van Sickle. The need for CAE is being driven by several discouraging trends which decrease the effectiveness of engineers: the number of design engineers vs. industry needs, technological changes, product life cycles, product development cycles, product quality issues, and expense burden vs. capital equipment trade-offs.

Computer Aided Design (CAD) tools have greatly enhanced development and manufacturing of complex electronic devices. However, most of these tools are directed at subsequent activities to design—with few exceptions, design engineers don't benefit extensively from these CAD tools in their primary job functions.

Tomorrow's designers will need an integrated set of CAE tools which address a wide variety of design tasks. These tools must be flexible enough to remain applicable as technology changes, and powerful enough to significantly improve the engineer's ability to do his job. Fortunately many of the same technological advances which have contributed to the need for new tools have also set the stage for solutions. In his paper, Thomas H. Bruggere, President of Mentor Graphics Corp., Portland, Ore., discusses the nature of these tools for the 1980's and which of the de-

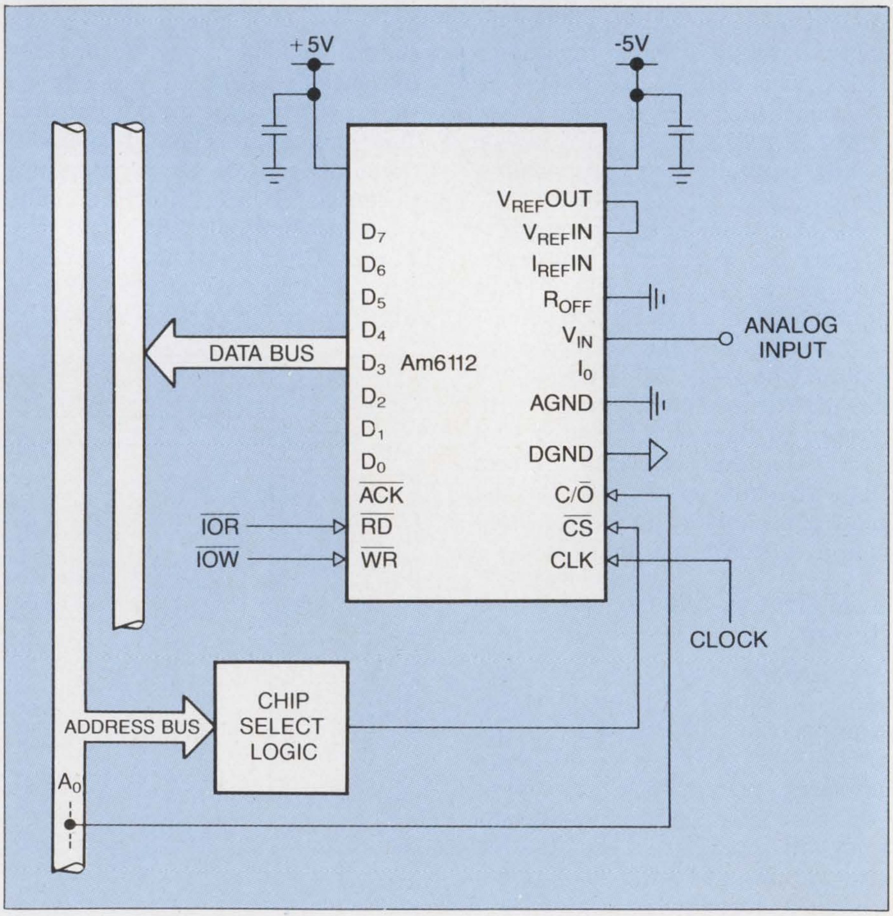

Figure 3: Interfacing the Am6112 to an 8085 will bring conversion times down to as low as 3.3 μs.

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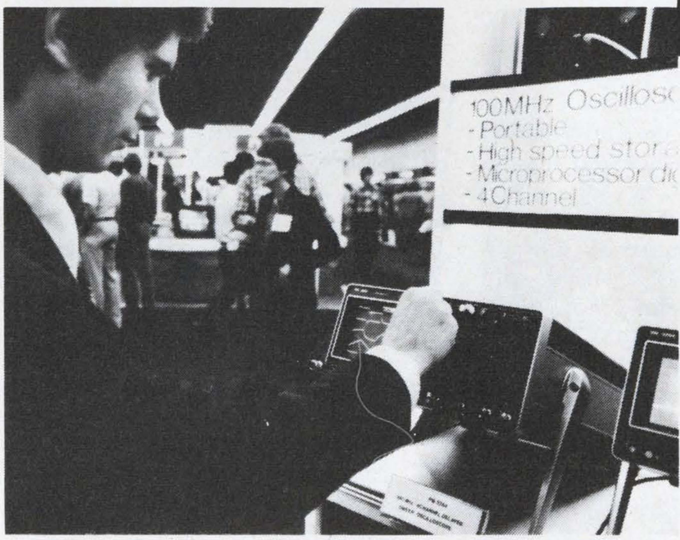

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sign engineering tasks are most likely to benefit.

Other papers in this session include: "Recent Developments in Standard Cells for VLSI Design," by William Loesch of Zymos Corp., Sunnyvale, Calif; "The Impact of Gate Arrays on the Design Process," by Tim Chambers of TI's Houston division; and "Creatively Managing the Future Design Environment," by Messrs. Yesenofski and Lemke of Tektronix Inc., Beaverton, Ore.

The latter paper discusses the impact of a changing technical and business environment on the management of an engineering function. More design creativity and shorter time-to-market is needed, while the human resource requirements both change and become more scarce.

Local Area Data Networks

On Wednesday, May 26, two consecutive sessions will be devoted to the timely and lively topic of local area data networks. The sessions will be roughly divided between papers on the CSMA/CD protocols used in such networks as Ethernet—for which Intel, Digital and Xerox are contributing their components and their expertise—and papers on the token access protocols supported by such computer giants as IBM and Honeywell.

Studies done by Xerox have shown that the flow of information between professionals, managers, and technologists is primarily within the local organization. For example, 93% of the information transactions are inside the organization while only 7% are outside (e.g. customers and suppliers). The geographic boundaries of information transfer are also local with 94% being within an office, floor, building, or campus and 6% within city, country or international boundaries.

Already Intel and Mostek are participating in the distributed computing and Local Area Networks (LANs) market by developing VLSI components for local networking. The result of this effort and others like it will be the full realization of the potential of LANs made possible by the availability of low cost VLSI semiconductor products for LAN interface implementation. Participants from Mostek will discuss the company's contribution to this end.

The originator of Ethernet, Xerox, will have its representative discuss Ethernet's application to various "office" environments. Xerox introduced the concept of interconnecting a broad variety of devices within a moderate geographical area; thus Ethernet is one of the major access methods currently being used. Terminals, hosts, personal computer workstations, gateways, and various types of servers have all found their way onto the Ethernet. The number of devices

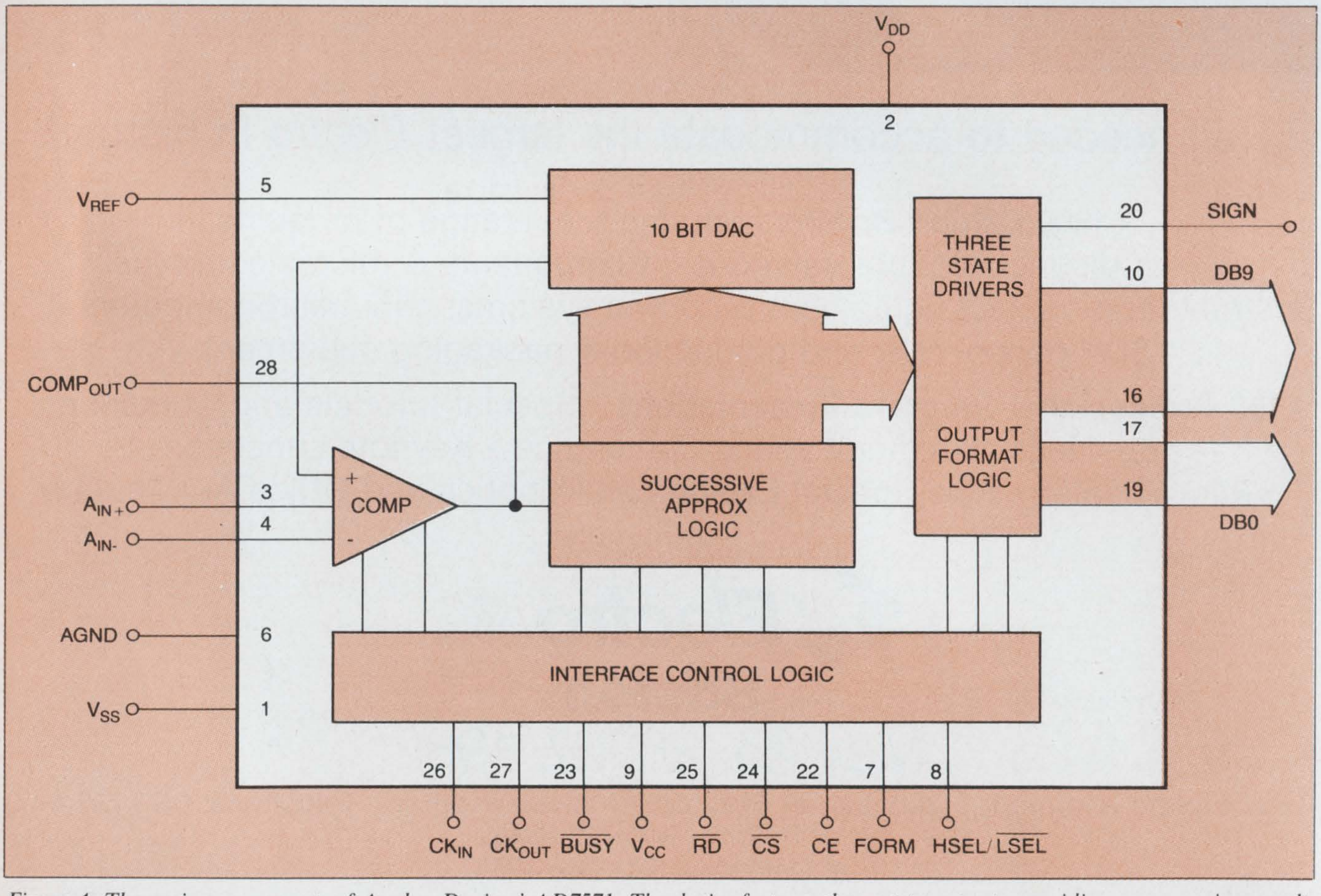


Figure 4: The main components of Analog Devices' AD7571. The device features three state outputs providing a conversion result in 70μs.

that one may attach to the channel is limited by several factors: finite bandwidth, limitations of the contention resolution algorithm, physical constraints, etc. The number of users that may use those stations or "taps" for communication is also limited by these and other factors such as the layered protocol architecture, the physical system architecture, the user workload, etc. The Xerox paper will examine the limits imposed on the number of users due to the finite bandwidth of the channel. This study is performed for users in a time-sharing environment.

Speech Synthesis

A most interesting session should be "Speech Recognition and Synthesis", (Session 11). It will deal with advances in electronic speech generation and recognition.Organized and chaired by James J. Farell III of Motorola in Austin, Texas, the sessions will have presentations from Interstate Electronics, National Semiconductor, General Instrument and Motorola. The papers will discuss the latest speech techniques from both the system and chip point-of-view.

On the chip level, Fred Wickersham of National Semiconductor will expound on the second generation chip that incorporates a time domain algorithm. He will recount the advantages that time-domain synthesis has over synthesizing speech in the frequency domain.

Mr. S. Viglione, Interstate Electronics Corporation, Anaheim, Calif., will reveal a high-performance discrete word, speaker dependent word recognition module, capable of recognizing 100 word vocabularies. The module itself is a single printed-circuit board, automatic speech recognizer consisting of a CPU, 4K bytes of ROM, up to 4K bytes of RAM for reference pattern storage, analog circuitry for speech spectrum analysis, interfacing to a controlling host processor and provisions for optional serial interfaces. **Figure 5** is a simplified block diagram of the word recognition procedures showing the analog processor front end and the digital processor.

David Gilblom, Telesensory Speech Systems, Palo Alto, Calif., will describe the merits of the PROSE 2000 text-to-speech converter, a single Multibus board that accepts plain English text in a serial ASCII format and converts it into high-quality spoken English in real time. Independent tests, says Mr. Gilblom, have shown that listeners will understand paragraph-length passages spoken by the board as well as they would understand human speech. Concluding, he will invite the audience to a live interactive demonstration by calling (415)856-0225.

Single-Chip Micros

One of the many papers presented

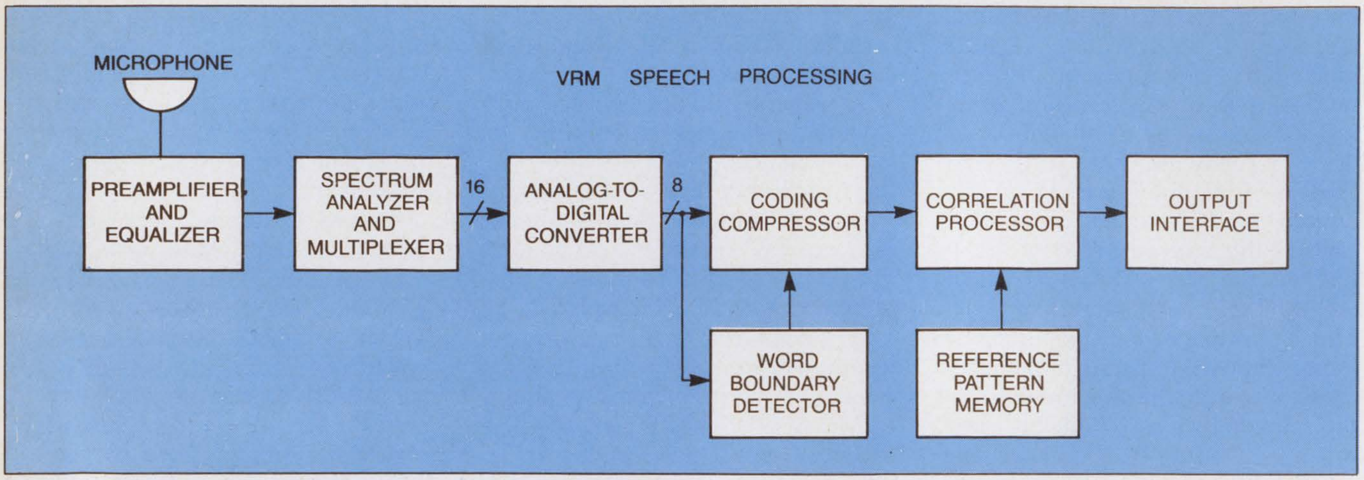


Figure 5: Interstate Electronics' word recognition module showing the analog processor front end and the digital processor.

in the single-chip μC session will demonstrate an application for the INS8073. A member of the 70-series μP family from National Semiconductor, the device has a 2.5K on-chip ROM that is capable of executing NSC Tiny Basic programs directly from stored ASCII as they would be written into memory. Two levels of internal decoding are employed to translate a Tiny Basic program into 70-series machine code and then into a microcode. This gives the user versatility in programming and causes programs to be easier to write than their assembly language counterparts.

Jim Chiang, National Semiconductor, Santa Clara, will outline a simple application for this data logging device (**Figure 6**). Once every ten seconds, the processor is interrupted, it checks the temperature of a sensor and prints it out on a Teletype or CRT terminal. The program is stored in a ROM, so in case of a power failure, operation will resume when power is restored. The following program was used.

```
 10  REM TURN ON
     INTERRUPT B.
 20  ON, 260
 30  STAT=STAT OR 1
 40  REM WATI FOR 10
     SECOND TIMER
 50  GO TO 40
 60  REM INTERRUPT
     ROUTINE
 70  REM GET THE
     TEMPERATURE
 80  A= @#E000.
 90  REM SCALE IT
100  B=(A*40)+15
110  REM PRINT IT
120  PRINT "THE TEMP. IS",
     B.
130  REM GO BANK AND
     IDLE
140  STAT=STAT OR 1
150  RETURN
```

When ROM is limited, the program can be compressed by eliminating all the remarks and space. The compressed program code may look like this:

```
1 ON 2, 3: STAT=STAT OR 1
2 GOTO 1
3 PRINT "THE TEMP. IS",
((@#E000*40) + 15)
4 STAT=STAT OR 1: RETURN
```

Linear in the '80s

"Linear in the '80s" is the title of Session 10. Les Hadley and Ed Ritter of Signetics will describe a linear position servo-loop control system which uses a small amount of specialized IC's and electromechanical hardware to control the position of a cutting blade or other machine tool to within 0.01 in. over an effective range of several inches. Up to now, the electronic package used to perform this electromechanical function was large, cumbersome and expensive. With the system

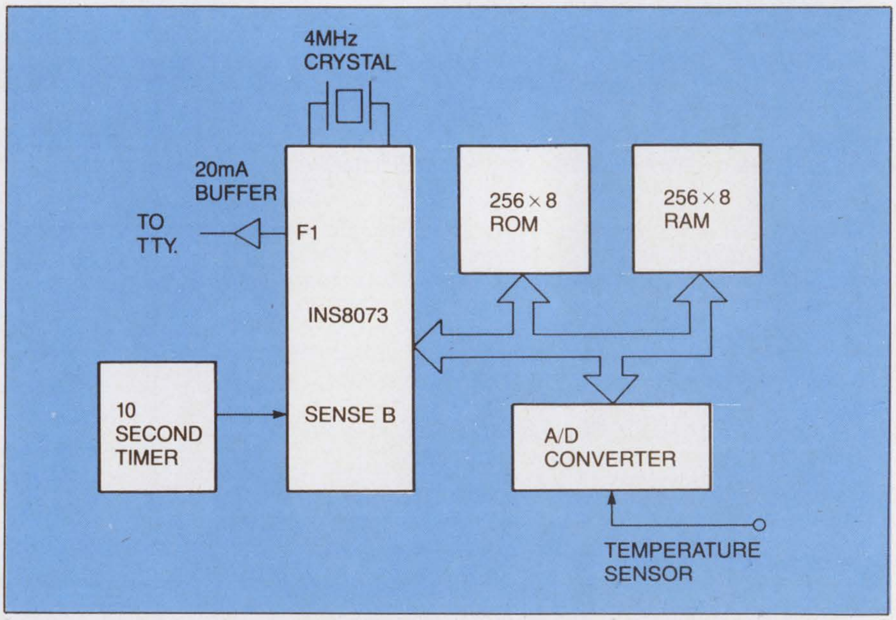


Figure 6: Using the INS8073 in a data logging application. The device is capable of executing Tiny Basic programs directly from stored ASCII.

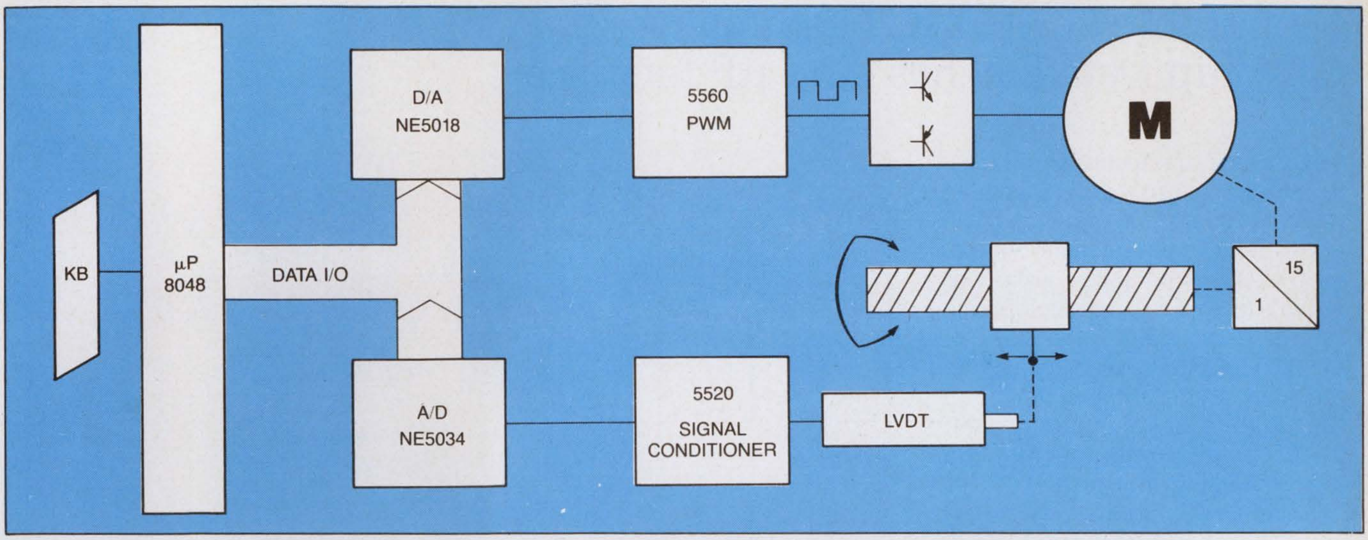


Figure 7: Functional design of a linear position servo-loop control system. Actual circuit diagram is available from Signetics.

Hadley and Ritter will describe, the parts count, and consequently the expense, is kept to a minimum. Apart from the electromechanical ends of the servo-control loop, the entire electronics package can fit comfortably into a 12"x8"x6" enclosure with room left over.

The system (**Figure 7**) uses a Signetics NE5520 specialized LVDT signal conditioner, NE5034 8-bit high speed ADC, NE5018 8-bit DAC system and a NE5560 switching regulator circuit which performs the motor control functions in conjunction with a matched pair of complimentary transistors. □

Monolithic 8-Bit DAC Features On-Chip Data Latches And μP Interface

Many DAC applications previously shelved due to device matching package count or cost considerations will now become viable, particularly in such areas as audio, graphics, and telephone systems, according to Analog Devices. The company has recently introduced what they claim to be the first dual monolithic 8-bit DAC complete with on-chip data latches and μP interface.

Each DAC has its own reference input and the input resistance is matched to within ±1.0% maximum. This feature eliminates the need to test and select DACs in most applications where precise matching is required. Such applications include digitally programmable window comparators and function generators for automatic test equipment.

The AD7528 has a load cycle similar to the write cycle of a RAM and is compatible with most 8-bit μPs, including the 6800 (**Figure 1**), 8080, 8085 (**Figure 2**) and Z80. Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input DAC A/DAC B determines which DAC is to be loaded while separate reference inputs allow each DAC to perform four quadrant analog/digital multiplication independently.

In the state variable or universal filter configuration (**Figure 3**) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cut-off frequency, fc. DACs A2 and B2 must track accurately for the simple expression for fc to hold. This is readily accomplished by the AD7528. Op amps are 2 × AD644. C3 compensates for the effects of op amp gain-bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where μP control of filter parameters is required, e.g. in equalizers and tone controls.

Programmable range for component values shown is fc = 0 to 15kHz and Q = 0.3 to 4.5.

Relative accuracy is guaranteed over the devices' full temperature range: ±1LSB, maximum, for A and S grades and ±1/2LSB, maximum, for B, C, T and U grades. All grades also guarantee monotonicity over temperature. Maximum initial gain error is guaranteed at ±4LSBs for A and S grades, ±2LSBs for B and T grades and ±1LSB for C and U grades. The AD7528 is available in either a Cerdip package for operation over the −25°C to +85°C temperature range (AQ, BQ and CQ grades) or a ceramic package for the −55°C to +125°C range (SD, TD and UD grades). The

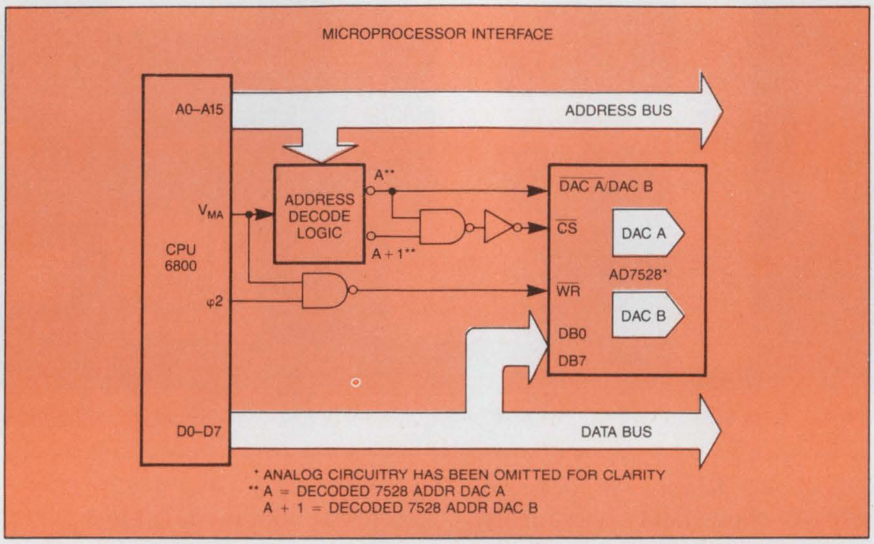


Figure 1: AD7528 Dual DAC to 6800 CPU Interface.

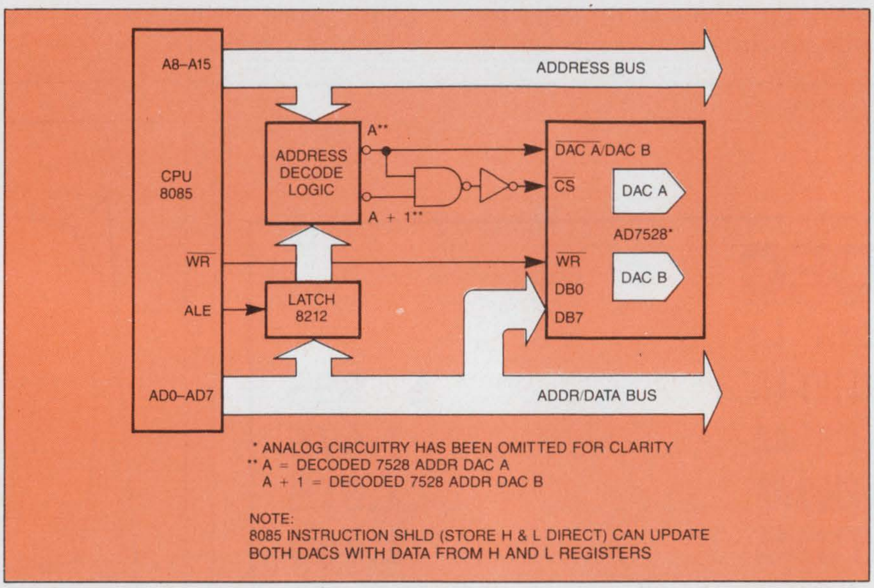


Figure 2: AD7528 Dual DAC to 8085 CPU Interface.

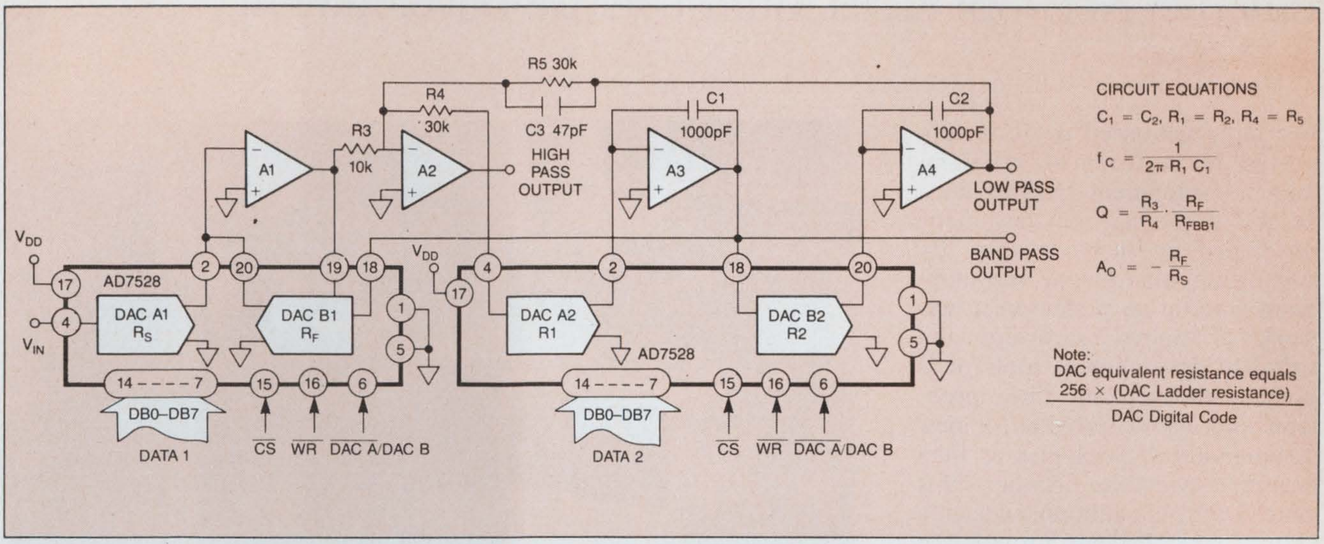


Figure 3: Digitally controlled state variable filter.

AD7528 is also available in leadless chip carriers (E suffix) and in MIL-STD-883B versions.

Other features include operation with a single +5V to +15V power supply and maximum power consumption of 5mW (V_{DD} = +5V). Maximum AC reference feedthrough is guaranteed at −70dB at 100kHz. Typical specifications include total harmonic distortion of −85dB, channel-to-channel isolation of −77dB (V_{REF}A to OUT B), and digital crosstalk of 30 nV-sec.

Ethernet Network Eases Multi-User μP Development

For large μP-based projects supported by a team of programmers, development stations must be able to manage software being developed by many people. By supporting stand-alone development stations as nodes on a network of shared hardware and software development tools, it is possible to overcome these problems and also to provide for new systems and technologies as they become available. Earlier this year, Tektronix announced such a system—the 8560—to provide the user with real-time transparent emulators and assemblers for the Z8000, Z80A and 6809 processors.

Now, Intel Corp. has brought together its expertise with the Ethernet local area network to introduce the NDS-II, a system which will permit all of the company's Intellec systems to become network stations. Both companies feel that with the increasing use of 16-bit μPs and the inherently greater software they demand, the development team approach will become increasingly important.

Figure 1: Up to eight Intellec development systems (two are shown) can be connected to the new, Ethernet-based network development system (NDS-II). On it, they may share a large common data base and expensive, high-speed peripherals, such as disk drives and printers. Programmers can also communicate with one another using electronic mail facilities. At left, the network resources manager oversees all work station activity.

Intel's NDS-II system provides important advantages toward managing this development process. Where several programmers are concurrently developing various portions of a system's program, it is crucial that software status and revision information be continuously available and up to date. With the Intel system, this is done in several ways. First, it provides a single integrated environment with consistent physical, logical and language interfaces throughout. For example, keyboard sequences and access commands are the same for all development tools including editors, compilers and in-circuit emulation modules.

The system also manages other levels of support such as a distributed hierarchical file structure, a software version control sytem and a software generation system. The physical location of these files is based on the frequency of access. Actual file location, however, is kept transparent to the user, who only needs to be concerned with the file name and its contents. In addition, file security can be defined by the file's originator in terms of the rights to "read," "read and write," or "read, write and delete" file data. A suite of project management tools is also available.

The system program controls and documents changes to source and object files. It manages storage and retrieval of different versions, controlling update privileges and keeping a record of when and why the user made which changes.

Automated software generation is supported by a "Make" software program, which automatically merges the latest versions of source or object modules into larger programs, ready for assembly or compilation. Thus, a user need only specify which modules he wishes to combine and "Make" fulfills modular dependency requirements, and the modules are combined.

Another function of this system is distributed job control. With it, users can export one task, such as compilation, while they work on another, such as source code editing. The exported task is automatically routed to any available work station equipped to handle it. Consequently, several tasks may be handled simultaneously by taking maximum advantage of the network's facilities at any time. In this way, overall development time is considerably shortened.

Existing Intellec systems may be upgraded for use as NDS-II resources via the NDS-II communication controller board set. The two-board set plugs into the Multibus chassis and provides the physical and data-link network requirements. **Write 197**

CP/M Programs For The IBM Personal Computer

A printed circuit board that is plugged into the IBM personal computer and allows its users to operate CP/M-80 based programs has been introduced by Xedex, a newly established computer firm.

The combination circuit board and software package allows 20,000 existing CP/M-80 based programs to be used by owners of the IBM personal computer. This eliminates the user's need to convert existing software for operation on the IBM machine. Baby Blue, as the board is called, also expands IBM's computer memory from 64 Kbytes to 128 Kbytes.

When the Baby Blue CPU Plus is plugged into the IBM system it becomes a computer within a computer. However, the board's Z80B μP requires no peripherals directly, such as screen, disk or printer, connected to it. Baby Blue runs the program and passes off the task of communicating with the outside world to the IBM computer.

At the time IBM introduced its personal computer last year, the company specified that outside software vendors were welcomed to write compatible programs for the machine. It allowed these vendors to design boards specified by IBM that could plug into the computer without voiding the guarantee. Xedex is the first company to do just that. Xedex hopes to achieve a 30% market penetration of all IBM personal computers. The Baby Blue board will be available in April and will sell for $600. As Mr. Landgarten, Xedex's President, pointed out: "This is only $60 more than what a user must pay for an IBM memory expansion board that gives the IBM machine an extra 64 Kbytes of memory. With our board the user also gets CP/M compatibility."

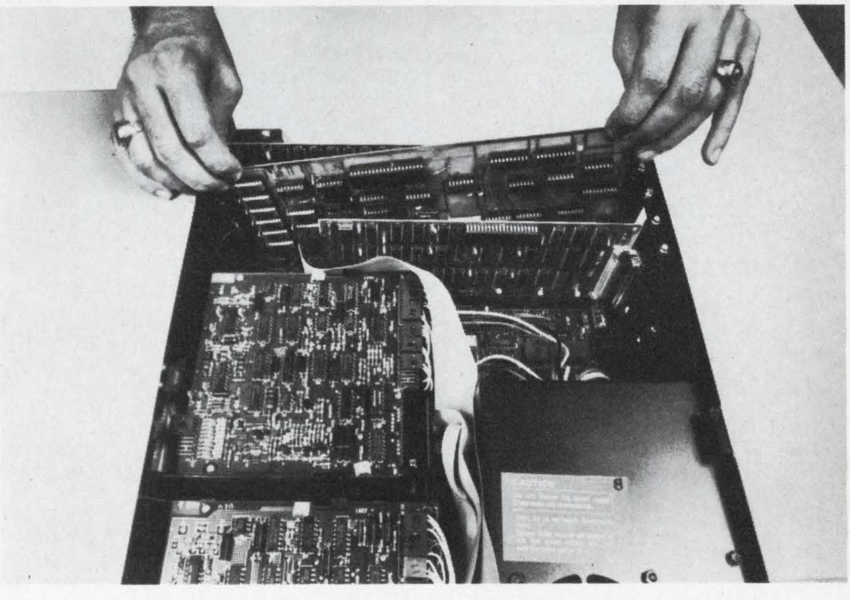
Operation is achieved by the addition of a header—a special preface—to the CP/M program that the board processes. The header consists of two parts: instructions to be executed by the personal computer's 8088 and the translator that Xedex's Z80B uses. Execution begins with the header's 8088 instructions, which tell the native CPU to move the translator and the CP/M program from the personal computer's native memory into Baby Blue's 64 Kbyte memory, and then turn on the Z80B. While the Z80B starts running the CP/M program, the 8088 remains available to the system peripheral I/O routines. When a CP/M function is to be generated, the Z80B converts the function in the translator into the proper form for the resident operating system in the personal computer (PC DOS) and sends the translated function call to the 8088 and then resumes program execution. The 8088 then handles the request and deals directly with the appropriate peripheral device. When the CP/M program is finished, the Z80B returns to its dormant state and normal operation under the PC DOS resumes.

Explaining the phenomena of the Baby Blue, Mr. Landgarten said: "This is the result of something that occurs over and over again in the computer industry. The initial hardware appears and users assume that software will soon follow. But users usually miscalculate the rate at which software is introduced. In the case of the IBM personal computer, many people in the industry assumed that when IBM came out with their computer, hundreds of programmers would start working furiously to convert the existing software.

While many computer experts predicted that a large amount of software programs would appear three to six months after IBM's personal computer introduction, in fact, it might take more like two years."

Mr. Landgarten cited an example showing how Xedex's board could prove cost-effective: "A user writes a program on his computer for a specific application. He then wants to upgrade his operation to an IBM personal computer. Rather than going to an outside consultant and possibly paying him $20,000 or $30,000 for converting the program, the user can instead use his original program for only $600, the cost of Baby Blue." *—Mokhoff*

Write 200



The Baby Blue board can be plugged into the IBM personal computer without the need for special equipment or assistance. While not using the CP/M feature, the board by itself doubles the memory capacity of the machine to 128 Kbytes.

IMPORTANT ANNOUNCEMENT

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Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

DEVELOPMENT SYSTEMS

With Growing Series Of Advanced Emulators

The μP's supported initially are those currently produced by SGS — the Z80, Z8000 and M3870 families — with real time emulation capability extending to 6 MHz operation for the Z80B. Emulators will be available for all new micros produced by SGS. The Z8000-based UX16 is a multi-user host handling up

to 8 users developing hardware and software simultaneously. The UNIX operating system was chosen to maintain compatibility with existing UNIX application software. This operating system will be upgraded to the Systems III version, offering all the advantages of UNIX OS. The UX8 is a compact, Z80-based development system that can be used on its own or as an intelligent workstation for the UX16. For the UX8, a new multitasking operating system, SDOS-II, provides time saving features such as printer spooling and real time debugging. A common language, the C compiler will be offered for both UX8 and UX16. **SGS Systems Div**, 7070 E. Third Ave, Scottsdale, AZ 85251. **Write 186**

OPERATING SYSTEM

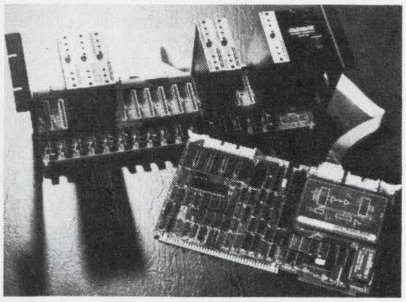
Time-Sharing OS For DEC LSI-11/23 & PDP-11 Family

VENIX is a superset of Bell Lab's UNIX operating system with new features of async I/O, shared data segments, locking semaphores and a resource pre-empting program priority. The standard VENIX distribution includes C and Fortran 77 compilers, word processing tools, full screen editors, plotting subroutines and programs, over 100 commands, drivers for standard DEC interfaces (including A/D, D/A, digital I/O, etc.), a Western Electric UNIX binary license, documentation consisting of a 4 manual set, and support. $2400. **Ventur-Com Inc**, 139 Main St, Cambridge, MA 02142. **Write 210**

SIGNAL CONDITIONING

All Solid-State System

This solid-state isolated signal conditioning system combines a rugged industrial chassis/backplane (the DT750,



suitable for rack or surface mounting) with a broad selection of interchangeable plug-in I/O modules (the DT6700 Series) that simultaneously isolate and condition a wide variety of analog signals. It is a compatible front end to A/D, D/A boards, data loggers, programmable controllers and many other industrial measurement and control systems. All modules utilize a proprietary solid state implementation of the flying capacitor technique to achieve 0.01% non-linearity for full 12-bit accuracy, along with continuous isolation of ±250 VDC and pulsed isolation of 1500V for 0.2ms. A variety of configurations are available from $231 to $273. **Data Translation**, 100 Locke Dr, Marlboro, MA 01752. **Write 187**

GRAPHICS SOFTWARE

Computer-Aided System Increases Individual Productivity

Created for electronic circuit and printed-circuit board designers, HP Engineering Graphics System/45 (EGS/45) is compatible with the HP9845 family of desktop computer systems. It is available either as a complete package or as individual modules: a general drawing core, a schematic drawing module, or a PC board layout module. With general drawing code the designer can create engineering drawings with primitive elements — lines, circles, rectangles, polygons, arcs and text via user-definable screen menus. Groups of primitives can be named, added to the menu and stored on mass media as recallable library parts. These parts then can be scaled, rotated or mirrored when being added to a subsequent drawing. The PC Board Layout Module supports interactive layout or digitizing of multilayer boards up to 32 by 32 inches with one mil resolution. It then automatically generates tooling outputs used in PC board manufacturing. The user can obtain plots to verify layout accuracy, paper tapes to feed numerically controlled, board-drilling machines and magnetic tapes to drive photo plotters. The Schematic Drawing Module combined with the general drawing code, produces electronic schematics and automatically generates material lists. Common electronic symbols are supplied as library parts. Users also can write their own routines in BASIC to process drawings created by the general drawing code or either of the modules. Complete EGS/45 software package (HP 98300A), is $10,000. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303. **Write 189**

DIGITIZING OPTION

Supports IBM Personal Computer

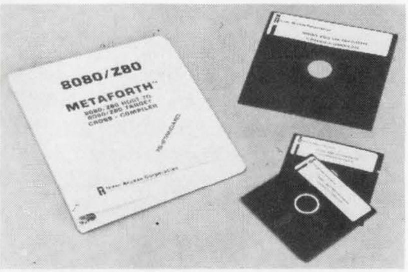
The Graphic Analysis Package #1 is designed so that one can start digitizing immediately, even without prior experience. The hardware includes a digitizer with 0.001″ resolution (sizes of 11″ x 11″ to 42″ x 60″ active area are available), a digitizing stylus, a power supply, a communications interface cable, and an operator's manual. The software, which is supplied on disk,

can be used for various kinds of measurements, including: material usage; material cost; length, distance, and perimeter; area of irregular polygon; display XY coordinates to 0.001″. The software is conveniently controlled by a 22 function block menu attached to the tablet. Eleven functions are predefined, the remaining blank 11 functions may be user defined. $1419 with an 11″ x 11″ digitizer, $2606 with an 11″ x 7″ digitizer, or $3025 with a 20″ x 20″ translucent digitizer. **GTCO Corp**, 1055 First St, Rockville, MD 20850. **Write 188**

CROSS COMPILER

For Creating ROMable 8080/Z80 Programs

The METAFORTH cross compiler is written in 79 Standard Forth. This system allows the user on a CP/M or



Cromemco CDOS 8080/Z80 based system to create 79 Standard Forth and assembly language routines for any target 8080/Z80 machine. This enables one to use currently available inexpensive equipment to design a wide variety of products. This 8080/Z80 system also produces Forth without header and link works for up to 30% space savings. The system includes a 8080 and a Z80 assembler, a Tektronix format downloader and other utilities. Complete source code is also included. $450, available on 5″ or 8″ diskette. **Inner Access Corp**, 517-K Marine View, Belmont, CA 94002. **Write 190**

MULTI-CARD SYSTEM

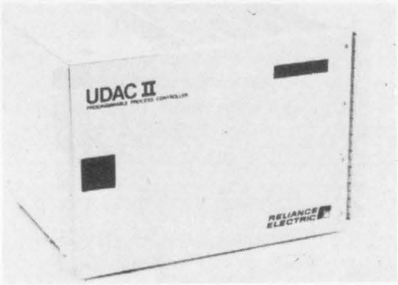
For Modular Remote Data Acquisition And Control

This family of microcomputer-based cards, each oriented toward a specific task, can link up to 256 remote data acquisition and control stations with a central computer over a single twisted pair of wires. REMDACS II employs preprogrammed remote cards close to sensor or control points; in operation, the cards are interrogated by a receiver/transmitter card at the host computer. This modular approach requires that only the cards necessary for a particular application be purchased; current-loop digital communications are carried out on a multi-drop party line basis, dramatically reducing wiring installation costs. Cards include: Receiver/Transmitter cards handle all communications; Analog Remote Cards match specific signals; and Digital Remote Cards for convenient I/O. They offer configuration flexibility with various power supply options. From $429 to $669, qty discounts avail. **Intersil Inc**, 10710 N. Tantau Ave, Cupertino, CA 95014. **Write 195**

μC PROCESS CONTROLLER

Uses Plain English Programming Language

UDAC II, user's digital and analog controller, is a stand alone, microcomputer-based, multi-loop process controller. Designed for use in an industrial environment, 0° to 60°C, it includes microcomputer and memory, high-level process control software and a complete process I/O interface. The unit can monitor and control up to 160 analog process variables and can perform logic and sequence control with up to 320 digital inputs and outputs. Its microcomputer card contains the 16-bit μP, real time clock, 3 peripheral communications ports (RS-232C and 20mA current loop) and 4K of PROM memory for the SPEAK EASY loader and UDAC II system diagnostics. Memory cards hold 16K words of semiconductor or 8K words of core memory. Cards can be added to give the machine direct access of up to 40K of memory. SPEAK EASY is a multitasking computer language utilizing a simple vocabulary of about 100 English words or abbreviations and has a complete selection of process control



functions. An optional communications multiplexer card expands the number of peripheral devices serviced by the UDAC II from 3 to 10. **Reliance Electric Co**, 4900 Lewis Rd, Stone Mountain, GA 30083. **Write 203**

PDP-11 SOFTWARE

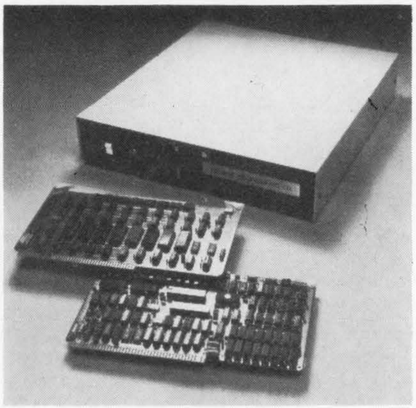
Performance And Capacity Monitor

For PDP-11 computers with RSX-11M and RSX-11M Plus, SRF Version 2 gives managers complete control over the data collection process and also allows them to select the type and amount of information they want reported so the data is tailored to meet their specific needs. When SRF is activated, all the information needed on CPU utilization, pool usage and fragmentation, check-point activity, overlay requests, I/O, task loader, shuffler activity, device usage and memory is printed onto easily read detailed, summary and graphic reports. It aids managers in identifying and correcting bottlenecks, finding where problems exist, and determine user activity so maximum use of resources is guaranteed. **Gejac Inc**, Box 188, Riverdale, MD 20737. **Write 206**

μP-BASED COMPUTER

For Use As A Communications And WP/Small Business Computer

The MZ-80 system is intended for users who want compatible computers for use as terminal concentrators and protocol converters as well as local processors. It uses Intel Multibus architecture



and is configured around 4 basic boards. The processor board contains a 6MHz Z80B μP, 32kB of 150ns dynamic RAM, 4 kB of ROM or EPROM control memory, and a 30 ms watchdog timer. It also includes one serial I/O port for connection to a host computer and another for system maintenance functions. Additional memory boards provide 32 kB each of 150ns static RAM. They allow bank switching, and the entire board may occupy only 2kB of address space, with sixteen 2k banks individually switchable. The I/O boards each contain 8 independent RS232 serial channels. Board design includes an onboard crystal-controlled clock to assure proper timing reference. The channels may be memory mapped or used in I/O mode, and used for async or sync communications or terminal applications. The fourth board is a DMA disk controller. Up to 4 standard 8″ or two 3-½″ micro-floppy drives, single or double-density, can be attached. For applications not requiring disk storage, the system is available in a ROM-based version. $7330 to $7435. **Thomas Engineering Co**, 1040 Oak Grove Rd, Suite 106, Concord, CA 94518 **Write 193**

DEVELOPMENT SYSTEM

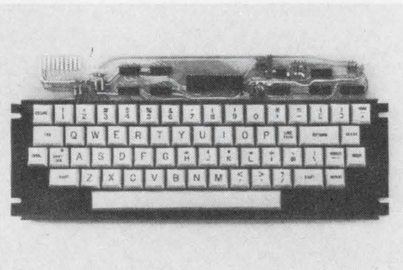
Complete Disk-Based Microcomputer System

The system includes EPROM/EEPROM programming, Z-80 in-circuit emulation, 48K RAM and two double density diskette drives. Software is the Allen Ashley package and includes editor, macro assembler, debugger/disassembler, interactive assembler, linker, relocator, spooler, and enhanced TRSDOS. Programs for programming and reading PROMs and in-circuit testing of RAM and ROM are also included. Compatible cross assemblers are available for Z8, F8/3870, 8048, 1802, COP400 and S2000 at $150 each. The EPROM programmer comes with a universal personality module which can program a variety of EPROMs. Since the zero-insertion force EPROM socket has 28 pins, larger PROMs of the future can be accommodated. The emulator essentially extends the TRS-80 bus into your target system via the Z-80 socket. The software allows interactive checkout of programs in small modules which can later be linked together into a large system. For users who already have a TRS-80 model I or III, the EPROM programmer/Z-80 Emulator is $329. **Orion Instruments**, 172 Otis Ave, Woodside, CA 94062. **Write 150**

INTELLIGENT KEYBOARD

New Concept In Pulse Transformer Technology

The IDK series of ergonomic, μP-based, low profile intelligent keyboards offer a high signal to noise ratio as a result of this new concept in the use of ferrite cores. The closed key coupling produces a peak output and minimizes the effects of contaminants. Also, the low impedence of the IDK series solid state switches traps and



squelches stray static and RF signals, and renders them insensitive to electrical noise and other EMI. The keyboards feature standard encoding in the 7-bit USASCII code (all 128 characters). Outputs are available in both serial and latched parallel formats. Simultaneous TTL serial and parallel outputs are standard, RS-232C is optional. Special character sets or special outputs are easily programmable and custom key layouts are also available. Standard keyboard (59 keys) is $90 in 1000 qty. **TEC Inc**, 2727 N. Fairview Ave, Box 5646, Tucson, AZ 85703. **Write 127**

COLOR TERMINAL

For Demanding Industrial And Commercial Applications

The 9701 features all metal construction, high resolution permanently converged CRT monitor, totally indepen-

dent monitor and display generator power supplies, and a detachable solid state keyboard. Display format is 80 char/line by 48 lines/page; 64 special characters are provided for diagram, plot and forms generation. Individual character attributes include: 8 foreground and background colors, selective blink, character protect and size select. Editing features include: dual cursors, horizontal and vertical writing modes, tabulator, character insert and delete, erase line and page, roll and scroll, and transmit full or partial pages. Onboard diagnostics aid in program development and debugging. Communication is ASCII RS-232C or 20mA compatible at 110 to 9.6K baud full or half duplex. Options include dual computer ports and a terminal supported light pen. $3995; 19″ high resolution version is $4995. **HMW Enterprises Inc**, 604 Salem Rd, Etters, PA 17319. **Write 126**

TEST SYSTEM

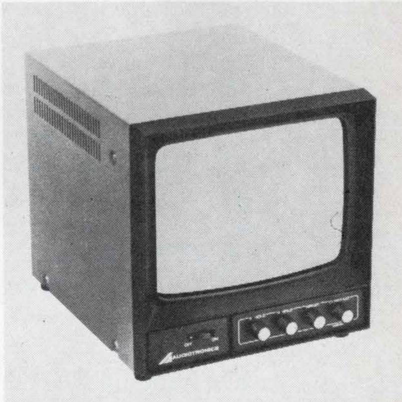
Programs, Verifies, Copies EPROMs

The system can program up to 8 EPROMs at a time and can be used with most industry standard 24 and 28 pin EPROMs. The Inspector-100 is a complete general purpose microcomputer controller containing a 4 MHz Z-80 μP, dual 8″ floppy disks with up to 512k of data storage, 32k of RAM and a full size computer terminal. It runs the industry standard CP/M operating system. The systems are designed to be modular and expandable. The controller of the Inspector 100/8 can also be used with other Pragmatic Design test heads. For higher performance applications the Inspector 200 with a dual 8085/8088 CPU is also available for use with all test heads. The TM-8 test head can program a wide variety of industry standard EPROMs in either ganged or serial modes and can also program 16 bit wide data into the EPROMs. It is totally modular and can be added to any existing Inspector-100, -200 systems. The I-100/8 is $10,950; the TM-8 and monitor software for existing systems is $3450 **Pragmatic Designs Inc**, 950 Benicia Ave, Sunnyvale, CA 94086. **Write 151**

VIDEO MONITOR

Off-The-Shelf 9″ Monochrome Unit

The 9VM967 general purpose monitor features silicon transistorized circuitry,



heavy duty single chassis construction and is designed to insure high reliability and easy maintenance. Front-panel controls include brightness, contrast, vertical hold, horizontal hold, and On/Off switch. Bandwidth is in excess of 10 MHz and horizontal resolution is 700 lines at center. Geometric distortion is less than ±5% of display height. The unit's power input is 30W at 120VAC, and all performance specifications are met with line voltage between 105 and 132VAC. A 240VAC, 50Hz model is also available. **Audiotronics Corp**, 7428 Bellaire Ave, North Hollywood, CA 91605. **Write 128**

COMMUNICATIONS PROCESSOR

Improved Communication/Expansion Of NCR Networks

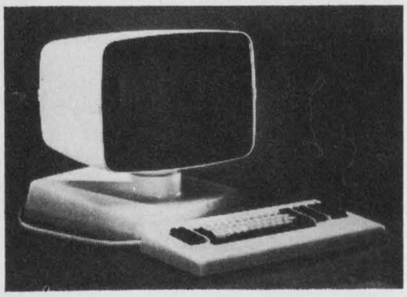
The OSI obsoletes the use of expensive line concentrators and multiplexors

and allows the use of low cost conversational terminals for data input. It uses an MC68000 μP and sophisticated load leveling and software to allow full front-end flow control. This means an almost unlimited mix of workstations and remote printers able to operate at various and differing transmission speeds. A 256K memory stores and forwards programs for local execution within the intelligent terminal network. A single OSI can support up to 20 full-time, multi-function workstations. More stations can be added by interconnecting two or more OSI units. A remote option permits the OSI to service clusters of up to 7 remote stations on a single modem line. **Century Analysis Inc**, 114 Center Ave, Pacheco, CA 94553. **Write 132**

COLOR TERMINAL

Meets New Human Engineering Standards

The desktop color terminal, the MVI-100, has several features not previously offered in color CRT terminals. The display rotates 180 degrees

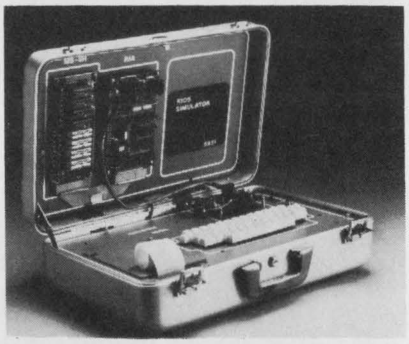


and has a tilting arc of 30 degrees. The compact 14" by 16" base fits any desk, leaving work area for the user. Six monochrome emulators allow for use with most application software previously written for displaying data on standard ASCII terminals. Color highlighting is available through the MVI-100 Color Enhancement Emulation. Full screen editing functions are standard along with cursor addressing on 4 split screens that can be scrolled vertically and horizontally. The MVI-100 includes as standard the DEC VT100 line drawing graphic set plus double high, double wide characters. A detachable keyboard contains a typewriter style keyboard, a 12-key numeric keypad, 15 editing keys and 24 programmable function keys. $2750, qty discounts avail. **Colorgraphic Communications Corp**, Suite 105, 2379 John Glenn Dr, Atlanta, GA 30341. **Write 133**

REMOTE I/O SYSTEM

Continued Life As Debugging Tool, Troubleshooter

This industrial controls and data acquisition system, the Remote Input/Output System (RIOS), includes a single-board microcomputer, ASCII keyboard and thermal printer enclosed in a portable, high-impact case. Model 8851 is an actual RIOS system implemented with an AIM 65 microcom-



puter (simulating or substituting as the system CPU normally supplied by the RIOS user). It allows the user to immediately program and observe RIOS operation, and is useful as a continued-support device for installed RIOS systems as a software debugging tool and troubleshooter. Working either downstream from the user CPU, or as a stand-alone system, the RIOS master station (CPU interface or intelligent controller) communicates with up to 127 individually addressable, intelligent remote stations. Each remote interface adapter (RIA) station can be configured to support an almost unlimited number of analog and digital sensing inputs and outputs, and provides fully isolated switch closures to accomplish command functions. RIOS applications include plant security, production line control, process control, material handling, and other uses where μP-based hierarchies interface with programmable functions. $1399.50. **International Rectifier Crydom**, 1521 E. Grand Ave, El Segundo, CA 90245. **Write 135**

DISPLAY MONITOR

High Resolution 26" Color Display

For computer graphic applications, the CDCT 3 x 66 offers a color raster scan display. It features a .37mm pitch delta

gun tube and is available in three horizontal rates up to 33KHz. Video bandwidth is 25 or 50MHz. From $7600. **Elector**, 5128 Calle Del Sol, Santa Clara, CA 95050. **Write 134**

TERMINAL

Self-Contained Text Editing/Communications Terminal

SCRIB is a truly portable terminal operating on AC power or rechargeable NICAD battery. It provides a built-in, 7" video display of 64 char/line, 18 lines of text plus the capability of a split screen mode allowing two different files to be displayed at the same time. It employs a 68-position typewriter-like keyboard, 27,000-character text memory and R/W mini-cassettes for additional storage. The text memory can be organized into 10 independent files that can be used for reference information, format storage and various other applications. Along with the standard editing features of most stand-alone word processors, the SCRIB also offers various search and replace features, automatic insertion and word wrap, 7 different display modes and scrolling in the forward or reverse directions. **Autologic Inc,** 1727 Veterans Memorial Hwy, Suite 203, Central Islip, NY 11722. **Write 129**

DG MULTIPLEXER

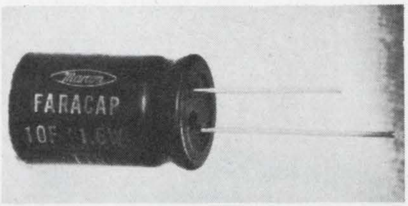
16 Line Async Unit

This multi-line communications controller interfaces up to 16 CRTs, serial printers or manual answer Bell 103 modems to any DG Nova or Eclipse computer. It can also be used in DG communications chassis. The SLAM is a direct replacement for the DG ALM16 or ATI16. It is RDOS, AOS, and DTOS software compatible. In addition, the clear-to-send signal is supported to allow slow printers to operate at higher baud rates. All 16 lines are provided with RS-232C signal levels eliminating the requirement for daughter boards. $2100 to $2250. **Interface Electronics Inc**, 21134 Bridge St, Southfield, MI 48034. **Write 153**

MEMORY CAPACITOR

For High Capacity Applications

The electrolytic capacitor, FARACAP, is extremely high in capacity, ranging from one farad to 100 farad at 1.6 VDC and .1 farad to 3.3 farad at 5.5 VDC. They are ideal for use as a battery for applications requiring low cur-

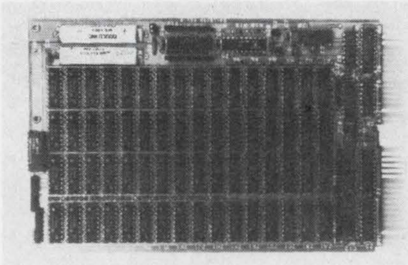


rent drain. They are excellent for retaining memory backup in case of power failure, or can be applied to portable products where power is not available. Application for high impedance design is recommended. **Marcon America Corp**, (Toshiba Group), 700 Landwehr Rd, Northbrook, IL 60062. **Write 154**

CMOS RAM BOARDS

Maintain Data Storage For 30 Days

The 1816CMOS battery backup boards are half-quad size and occupy a single slot when plugged into an LSI-11 Bus backplane. There are 4 models. The 1816CMOS-16S is a 16K word version with standard, 168-hour, retention capability. The -16L model offers 16K words with long retention, 30-day, capability; -8S, 8K words and standard retention; -8L, 8K words with long retention. They are suited for industrial applications where it is desirable to retain data during temporary power outages or equipment shut-down periods. When normal power is applied, onboard automatic switching and re-

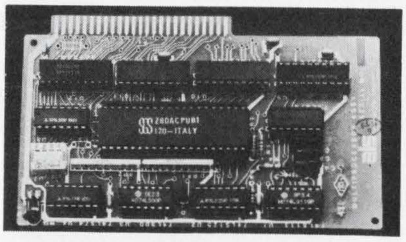


charging circuitry keeps the two self-contained nickel cadmium batteries charged to peak efficiency. On-board 18-bit address decoding circuitry and write protect dip switches, that are accessible while the memory board is positioned in the backplane, permit memory access to start at any 4K word boundry and write protect of 4K, 8K, 12K or 16K word segments. Full operating temperature range is 0° to 55°C. From $695 to $1295, qty discounts avail. **ADAC Corp**, 70 Tower Office Park, Woburn, MA 01801. **Write 155**

PLUG-IN MODULE

Gives Apple II/III Users CP/M Capabilities

Z-Card contains its own Z-80A μP allowing the Apple to run virtually any software designed for CP/M-based microcomputers. It is easily installed with no hardware or software modification so users can switch back and forth between CP/M and DOS or SOS using simple software commands. Synergizer Software, the CP/M operating system delivered with the Z-Card, includes an enhanced directory command, format and copy in one pass, and use of a full 60K of system RAM. Allows Apple owners to take advan-

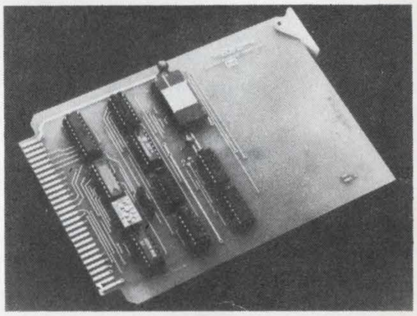


tage of the benefits of using CP/M and run many popular software packages including Wordstar, CBASIC, VTS/80, Accounting Plus, and SuperCalc. **ALS Inc**, 1195 E. Arques Ave, Sunnyvale, CA 94086 **Write 156**

ARITHMETIC PROCESSORS

Available With 2, 3, And 4 MHz Speeds

The ST4402 Fixed/Floating Point Arithmetic Processor is based upon the AM9511 APU and allows the STD BUS user to perform addition, subtraction, multiplication and division, plus a full complement of transcendental derived functions. An onboard jumper option allows the user to select any speed of operation within the Z80 STD BUS environment up to the speed of the board chosen. Able to convert from one format to another with single commands, the processor accepts commands for manipulation of 16- or 32-bit fixed point or 32-bit floating point values. Also featured is switch selectable addressing which allows the processor to occupy a range of I/O addresses from 00H to F8H. $325, 2 MHz; $385, 3MHz; $445 4MHz; OEM



and qty discounts avail. **Applied Micro Technology Inc**, Box 3042, Tucson, AZ 85702. **Write 157**

PLOTTER CONTROLLER

Boosts System Throughput

The electrostatic plotter controller/interface (EPC) is a hardware-firmware package which completely offloads the CPU of the IGS-500 or IGS-400 stand alone systems. The device sorts and generates plots on up to two electrostatic plotter/printers of varying widths, resolutions and manufacture. The IGS-500 supports up to 4 independently operating workstations which incorporate raster refreshed graphics displays. The IGS-400 supports single task, foreground operation. When not operating as a controller, the EPC can be used to analyze drawing files, i.e., extracting data for reports, packing drawings (condensing plot data to conserve storage), and performing network analysis. With basic memory capacity of 48K words, the EPC is $19,500. **California Computer Products Inc**, 2411 W. La Palma Ave, Anaheim, CA 92801. **Write 158**

8 BIT A/D CONVERTER

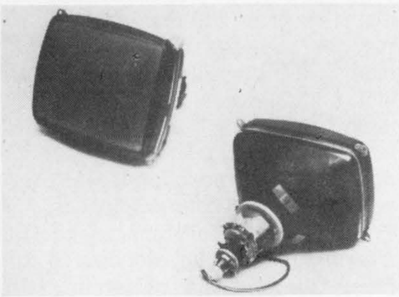
Features ± ½ LSB Total Adjusted Error

ADC-830 8 bit, CMOS A/D converter operates directly with the standard control bus of 8080-μP derivatives via 3-state outputs. The converter appears as a memory location or I/O port to the μP without interfacing logic. Its digital control inputs, $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$, are active low, and are available in all μP memory systems. Using the successive approximation technique and a modified potentiometric resistor ladder, the ADC-830 achieves an 8 bit conversion in 100 μsec with a maximum total adjusted error of only ± ½ LSB. No zero adjust is required. Also, the differential analog input allows the user to increase the common mode rejection and offset the zero value of the analog input. Packaged in a 20 pin plastic DIP it operates over the 0°C to +70°C commercial temperature range. Power requirement is +5 VDC. $7.95 (1-24). **Datel Intersil**, 11 Cabot Blvd, Mansfield, MA 02048. **Write 159**

IN-LINE COLOR CRTs

Available In 5 Sizes

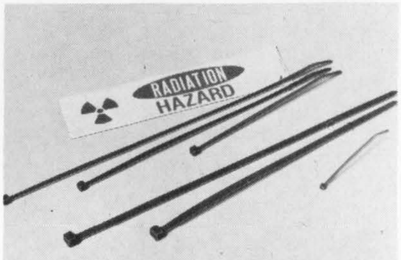
The 9, 12, 13, 15 and 19 inch CRTs offer high resolution (900 x 675 pixels for the 19" tube) due to an innovative electron gun design: the Overlapping Field Lens (OFL) that decreases the separation between the three electron beams in the gun, thus increasing the effective resolution. Features include a pre-converged CRT/deflection yoke, which saves costs by eliminating the need for convergence circuitry; an internal magnetic shield for high immunity against extraneous magnetic fields; a black matrix screen for high brightness and contrast; a high-density shadow mask for sharp and clear graphic and/or alphanumeric display; and the availability of custom phosphors to meet special display color requirements. From $300 to $600 in 10 qty. **Panasonic**, One Panasonic Way, Secaucus, NJ 07094. **Write 162**



CABLE TIES

For Harsh Environments

The ties are designed to fasten cables, hoses and wires in environments having radiation exposure, temperatures up to 302°F, or harsh chemicals. Six PAN-TY TEFZEL cable ties are now available for use on bundle diameters up to 4" and with minimum loop tensile strengths up to 120 lbs. They are offered in miniature, standard and heavy cross-sections and may be installed by hand or with Panduit cable tie installation tools. TEFZEL provides radiation resistance up to 200 megarads and meets the requirements of IEEE 383. Their continuous temperature range is −50°F (−46°C) to 302°F (150°C). The cable ties also provide resistance to ultra-violet light and weathering in outdoor use. **Panduit Corp**, 17301 Ridgeland Ave, Tinley Park, IL 60477. **Write 163**



FIBER OPTIC CONNECTORS

Satisfy Stringent Military Requirements

The new connectors feature superior alignment characteristics with ultra low insertion losses and excellent repeatability. A unique coupling uses a combination of a split tube and special bushing for precise axial and angular alignment as well as interface gap control. Following reliability testing of 500 mating/unmating cycles, no significant degradation of insertion loss resulted. Protection from adverse environments is provided by strategically placed seals. A variety of fibers ranging from 100 microns to 1.16 mm can be accommodated in a single connector. Several types of standard connectors are available: multi-channel circulars in 2, 4 and 6-channel hermaphroditic designs; multi-channel rectangulars which permit the mixing of fiber optic, coaxial and power contacts; specials designed for mounting to printed circuit boards, and single channel types. **Hughes Connecting Devices**, 17150 Von Karman Ave, Irvine, CA 92714. **Write 160**

PHOTODETECTORS

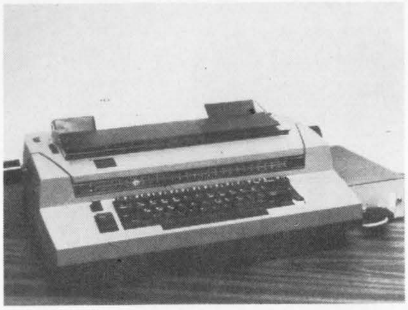
For High Speed Wide Bandwidth Applications

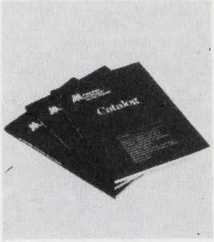
The two new high-speed silicon p-i-n photodiodes provide high responsivity between 400 and 1000 nanometers as well as extremely fast rise and fall times (typically 0.5ns). Responsivity is independent of modulation frequency up to 800 MHz due to their fall time characteristic. The C30971E is supplied with a flat glass window in a hermetically sealed modified TO-18 package. The C30971EL contains a light pipe which is an integral part of the package. They are useful in a variety of applications requiring high speed and/or high sensitivity. Optional user price in quantity 1-24 is $67 each for the C30971E and $75 each for the C30971EL. **RCA**, Box 3200, Somerville, NJ 08876. **Write 164**

PRINTER INTERFACE

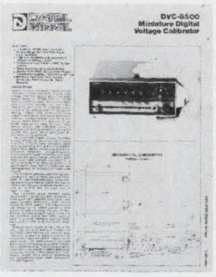
Converts IBM Typewriter Into Letter Quality Printer

The ELF 2 interface allows the use of IBM Electronic typewriter Models 50, 60 or 75 as a letter quality printer by providing an RS-232C serial or a Centronics-compatible parallel printer interface which can be connected to the user's computer. Print speed is 16 cps and the converted typewriter retains its original appearance and can also be used in the normal typewriter manner. The interface accepts any standard ASCII data from the computer. Special typewriter functions normally controlled from the typewriter keyboard can also be commanded from the computer. These include continuous or word underlining, and tab set or clear. The interface is fully compatible with all software, including WP programs, and no modifications to the user's computer or software is needed. The ELF 2 interface is $495, qty discounts avail. **iPEX International Inc**, 5115 Douglas Fir Rd, Calabasas, CA 91302. **Write 161**

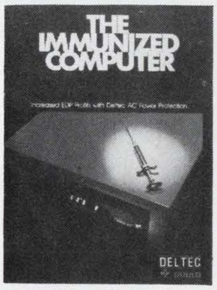




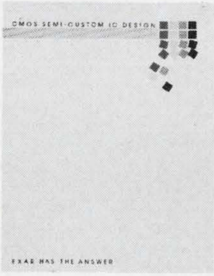
Power Systems. 1982 standard products catalog containing all the company's catalogs and current and new products. Sections include: D/A & A/D Converters, Precision Operational Amplifiers, Precision Voltage References, Analog Switches and Multiplexers, and Dual Transistors, plus bonding diagrams and packaging information. Detailed specs are provided. 200 pp.
Micro Power Systems **Write 275**



Miniature Digital Voltage Calibrator. Details all the electrical and mechanical specs on the DVC-8500, 4-1/2 digit voltage reference source with a full scale output range of −19.999V to +19.999V in 1 μV steps. Includes block diagrams, technical notes and describes applications for calibrating A/D and D/A converters, DPM's, Op Amps, V/F converters and DVM's. Brochure, 6 pp.
Datel-Intersil **Write 277**

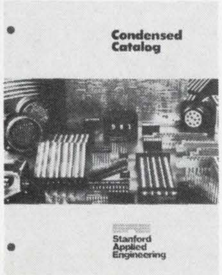


Power Conditioning. "The Immunized Computer" discusses AC power line problems and the ways to correct them to insure stable AC power. A brief discussion on problems, causes and solutions along with an estimator on the total cost for the solution is addressed. Brochure, 4 pp.
Gould **Write 278**

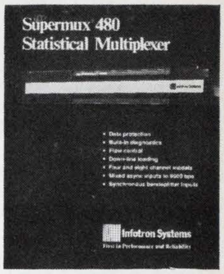


CMOS Semi-Custom IC Design. The brochure explains Exar's CMOS Master-Chip semi-custom IC's, and the Design Kit and Manual, which assists the customer with bread-boarding and development of a schematic. It also delineates the services to the semi-custom client. Specs for their 4 CMOS Master-Chip semi-custom IC's are included. 5 pp.
Exar Integrated Systems **Write 279**

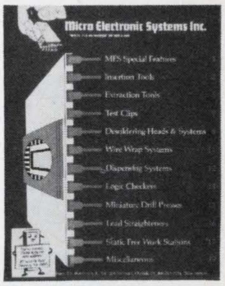
Quick Guide to Overcurrent Protection. Condenses into tabular form the data needed to make an informed selection of the proper circuit protectors for applications ranging from 0.01 to 250A continuous current, AC or DC. Standard and special internal circuit diagrams are shown, giving a wide choice of optional control functions in addition to equipment and branch-circuit protection. 7 pp.
Heinemann Electric **Write 280**



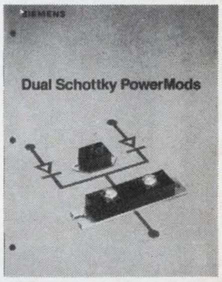
Electronic Components. Describes the company's complete line of electronic packaging hardware, components and systems. Included are particulars on edge-board/PC connectors, connector hood assemblies, Multi-Term IDC connectors and cable, switches, cylindrical connectors, IC sockets, component mounting boards, EMI filters, card files, logic panels and backpanels. Catalog, 6 pp.
Stanford Applied Engineering **Write 281**



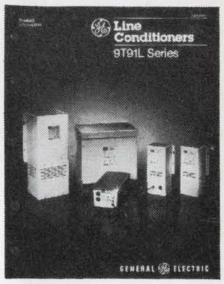
Statistical Multiplexer. Describing the Supermux 480 Statistical Multiplexer, the brochure illustrates the differences between conventional and statistical multiplexing. Before/after type diagrams are used to show a simple system without multiplexing, with conventional multiplexing and with statistical multiplexing. It also describes the features and benefits of the μP-controlled Supermux 480. 12 pp.
Infotron Systems **Write 282**



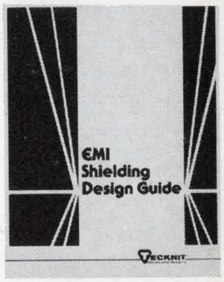
IC Insertion & Extraction Tools. Also featured are a large variety of IC and PCB Handling Systems. Products include wire wrap guns with 650' spools of different colored wire for daisy chain wrapping, a digital rapid IC removal/replacement system, drill and accessories, and soldering iron tip temperature measuring systems. Catalog, 20 pp.
Micro Electronic Systems **Write 283**



Dual Schottky PowerMods. Lists electrical, thermal and mechanical characteristics of the company's 200, 120, 85 and 50 amp PowerMods which are designed for the new, extended frequency power supply designs. Brochure, 4 pp.
Siemens **Write 284**



Line Conditioners. Explains how variations in supply voltage and the presence of electromagnetic noise can lead to malfunctions in sensitive electronic equipment such as electronic cash registers, μP's and computers, Line Conditioners eliminate these problems. The GE Line Conditioner family includes portable and hard-wired models in ratings from .250-15 KVA. Brochure GEA 10931, 8 pp.
General Electric **Write 285**

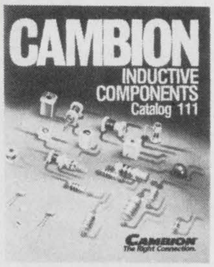


EMI Shielding Design Guide. Assisting in the design, selection and application of EMI shielding materials, this design guide provides the engineering community with an up-to-date reference source. Subsequent material developed from this ongoing project will be directed to the recipient. It takes a step in making EMI Shielding more understandable and easier to include in design, specifying and application. $10.00, 78 pp.
Tecknit **Write 287**

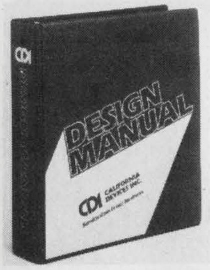
Fiber Optic System. Described is the SL-2000 fiber optic video/audio/data transmission system, and its applications. It explains how fiber optics solve video/audio transmission problems faced in television broadcasting, CATV, military and industrial applications. Brochure, 6 pp.
Artel Communications **Write 250**

New Literature

Molded-On Cable Assemblies. These data sheets and brochures describe Molded-On Cable Assemblies to meet RS-232 and RS-449 as well as forthcoming FCC shielding requirements. Additional literature describes complete cable assembly facilities.
Aura Manufacturing **Write 251**



Inductive Components. This updated 34 pp. Catalog 111 features comprehensive listings of Cambion's Variable Coils (shielded and unshielded), RF Chokes (including military types), Coil Forms (both PC board and panel mount), Micro-Inductors, Testing Fixtures, and selected Capacitors. It contains full documentation, dimensioned line drawings and tabulated specs.
Cambion **Write 252**



Silicon Gate CMOS Gate Array. This design manual provides detailed information regarding silicon gate CMOS gate array applications, technology, logic, layout, CAD, testing and packaging. Included is a listing of common cell layouts for both core logic cells and periphery cells for the HC series. $50.
California Devices **Write 253**

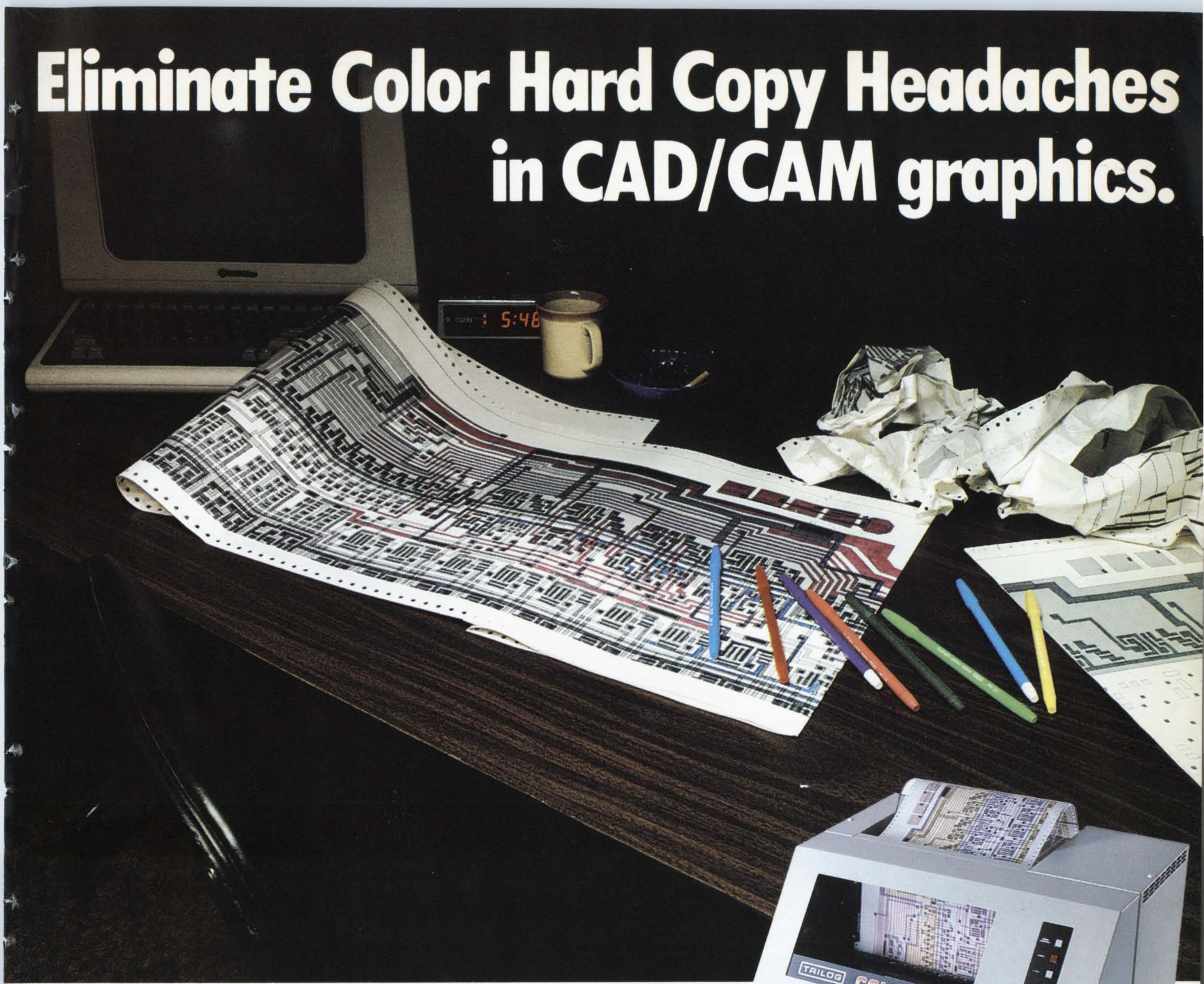
High-Torque Stepper Motors. Fully illustrated with specification charts, engineering drawings, schematics, and performance curves, the literature describes the Size 15 stepper motor's high torque, high speed, small size design. The stepper offers standard accuracy of ±5 % ±3 % accuracy is available.
Clifton Precision **Write 255**

CDS V.22 Modem. This technical brochure describes the CDS V.22, a 1200 bps full duplex modem with an automatic and adaptive equalizer. This feature self-adjusts the modem's receiver to correct for distortion and drift introduced by telephone lines.
Concord Data Systems **Write 254**

Note: To include your literature in this section, send a press release to New Literature Editor, **Digital Design,** 1050 Commonwealth Ave., Boston, MA 02215. All submissions *must* include a cover photo.

Advertiser Index

Eliminate Color Hard Copy Headaches in CAD/CAM graphics.



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Now you can interpret your CAD/CAM graphics quickly and accurately — in full color hard copy. It's simple with the Trilog COLORPLOT.

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IMAGE PROCESSING: MUSIC TO YOUR EYES.

The right side of the human brain interprets music. The left side, language. And a DeAnza image processor maps the brain's metabolic changes right before your eyes.

Research scientists at UCLA School of Medicine's Biophysics and Nuclear Medicine Divisions are mapping new territory. Utilizing an EG&G Ortec ECAT Scanner, a DeAnza IP6400 Image Processing System, and a technique called positron computed tomography, the UCLA team can produce quantitative images of metabolic functions in the human heart and brain. Used in research today, this technique one day may be an important diagnostic tool.

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Your application and budget may call for the intermediate capabilities and price of an Image Processing System, like the IP6400. Or perhaps you need the large memory and state-of-the-art performance of our powerful IP8500 Image Array Processor. Or the stand-alone convenience of our VISACOM/23 Visual Display/Computer System.

Call Today for Answers. But to provide the system that's right for you, we'll gladly analyze your application and requirements. So call or write the DeAnza office nearest you, tell us what you need, and we'll go to work for you.

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