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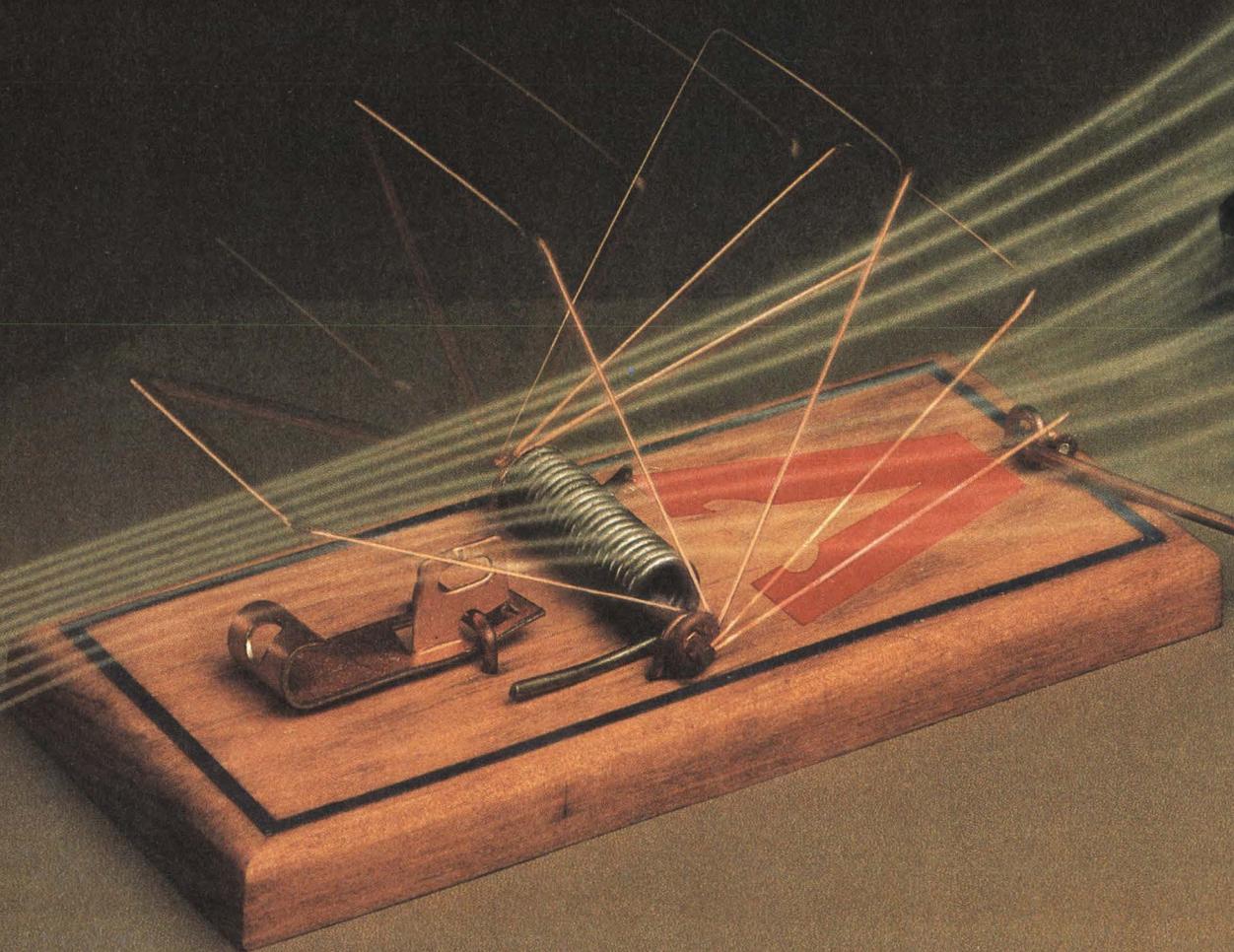


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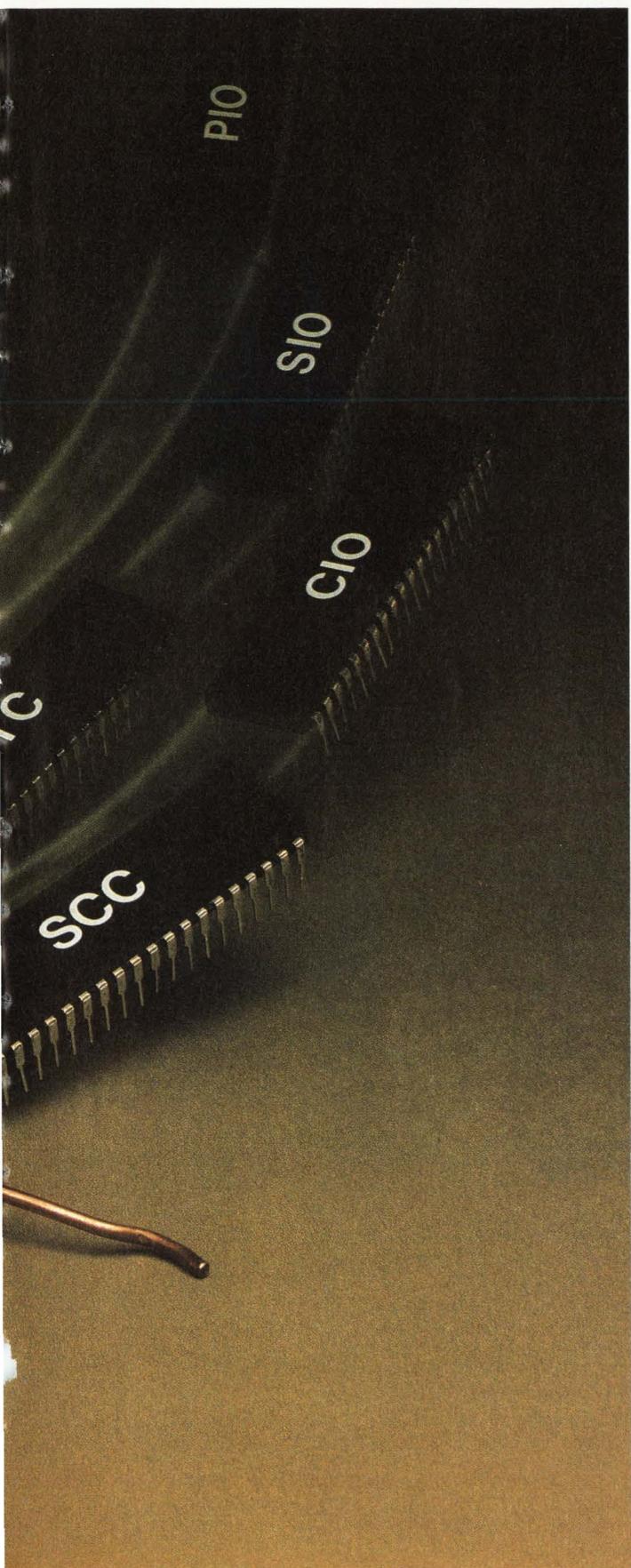
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using either phase-encoded or inverted-nonreturn-to-zero (NRZI) recording standards.

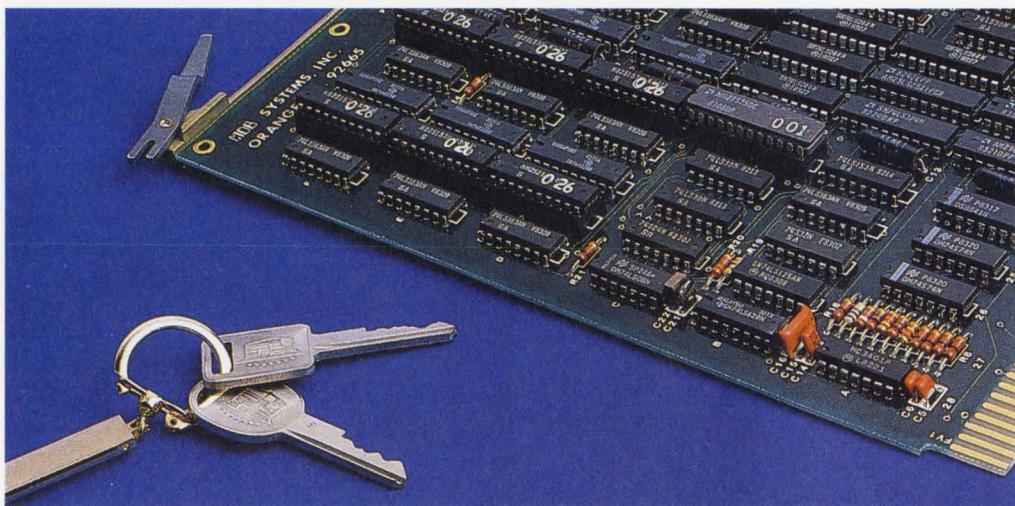
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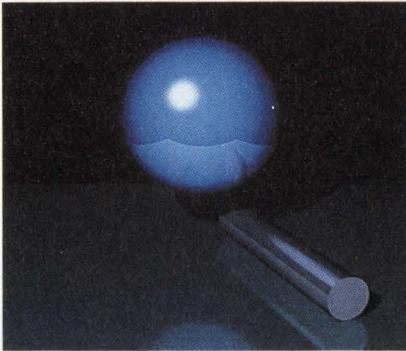
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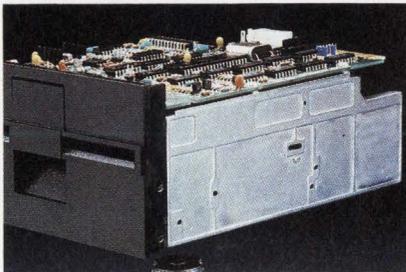
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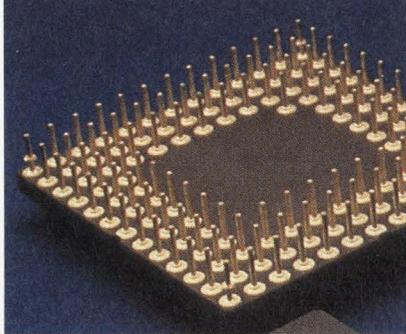
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p. 42 (Photo courtesy M. Wozny, RPI)



p. 57 (Photo courtesy Micropolis)



p. 90 (Courtesy National Semiconductor)

Cover:

Shown on the cover is Apollo Computer Inc.'s DN660 Computational Node running IDEA 1000 C, an Electrical Computer Aided Design (ECAD) package from Mentor Graphics Corp. Apollo's DN660, a general-purpose color workstation, features 1024 x 1024 resolution bit-mapped raster graphics with up to 2 Mbytes of dedicated display memory. The fully integrated graphics capabilities of the DN660 allow users enough power to handle the entire design, simulation, and layout process for ICs and PCBs. In addition, the DN660's graphics capabilities support a wide range of CAD and engineering applications. Cover photograph by Steve Grohe, Boston, MA.

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COMPUTERS/SYSTEMS

Industry Review: Graphics Terminals 42

Describing the design changes in graphics terminals is challenging due to the great diversity of performance and functionality.

Integrating Hardware and Software for VLSI Design 72

Many CAE vendors prefer to remain software houses and leave the hardware development to those companies with the resources necessary to remain competitive.

The Expanding Realm Of The IBM PC 80

The IBM Personal line is invading a range of markets formerly the territory of specifically designed and dedicated machines.

UNIX Standards Move To The Forefront 122

UNIX developments in 1984 have implications for the entire computer industry, including OEM's, users, value-added resellers, and manufacturers.

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Dual Processor Viewstation Provides 3D Shaded Surfaces

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Advances both in flexible media and drives have kept pace with advances in small computer systems, and floppies have prospered.

Peripheral Interfaces Lower Cost And Boost OEM Performance . . 98

The decreasing cost of VLSI devices has resulted in the ability of peripheral manufacturers to add increasing intelligence to their equipment.

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Design decisions relating to choice of technology may become less clear over the next year.

High-Performance Event Interface For A Microcomputer 110

As silicon technology advances to provide denser geometries, timer structures have become more elegant and powerful.

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(Them)



(Us)

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Heurikon presents Minibox – a multiuser UNIX workstation based on its powerful HK68™ single board microcomputer and Uniplus+™ UNIX System III or System V operating system with Berkeley enhancements.

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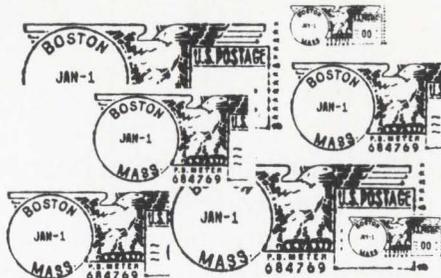
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Our 5480 Series of color raster terminals and workstations aren't the only ones with 4096 colors. But the colors have never looked so good. Because resolution has never been higher.

New standards.

The 1536 × 1024 pixels set a new standard for displayable resolution. Raster staircasing is significantly reduced without the complexity of anti-aliasing.

But new standards don't stop with highest resolution. Areas are filled virtually instantaneously so the 5480 Series also sets a new standard for polygon fill.

Vector generation sets a new standard, too. The time lapse between the moment you draw until the picture is generated is as much as 50 percent faster than many others.

Enemy of obsolescence.

You shouldn't be forced to ditch programs in place when you buy a new terminal. For that reason, standard with all 5000 Series models is a Tektronix



Lundy's 5484 color raster design workstation.

4010 or 4014 Emulator with mixed-mode software switch for enhancing existing programs with color-native protocol.

Currently, our terminals can be driven by many of the leading software products. And the list is growing rapidly. Because Lundy is committed to an aggressive third-party software develop-

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Lundy will help you see more in graphics.

When you look at our 5480 Series, take a close look at Lundy, too. We're a company that's as good as its products.

A company that balances high tech with solid business sense.

A company as proud of its service (one of the largest service organizations in the industry—39 locations nationwide) as its engineering expertise.

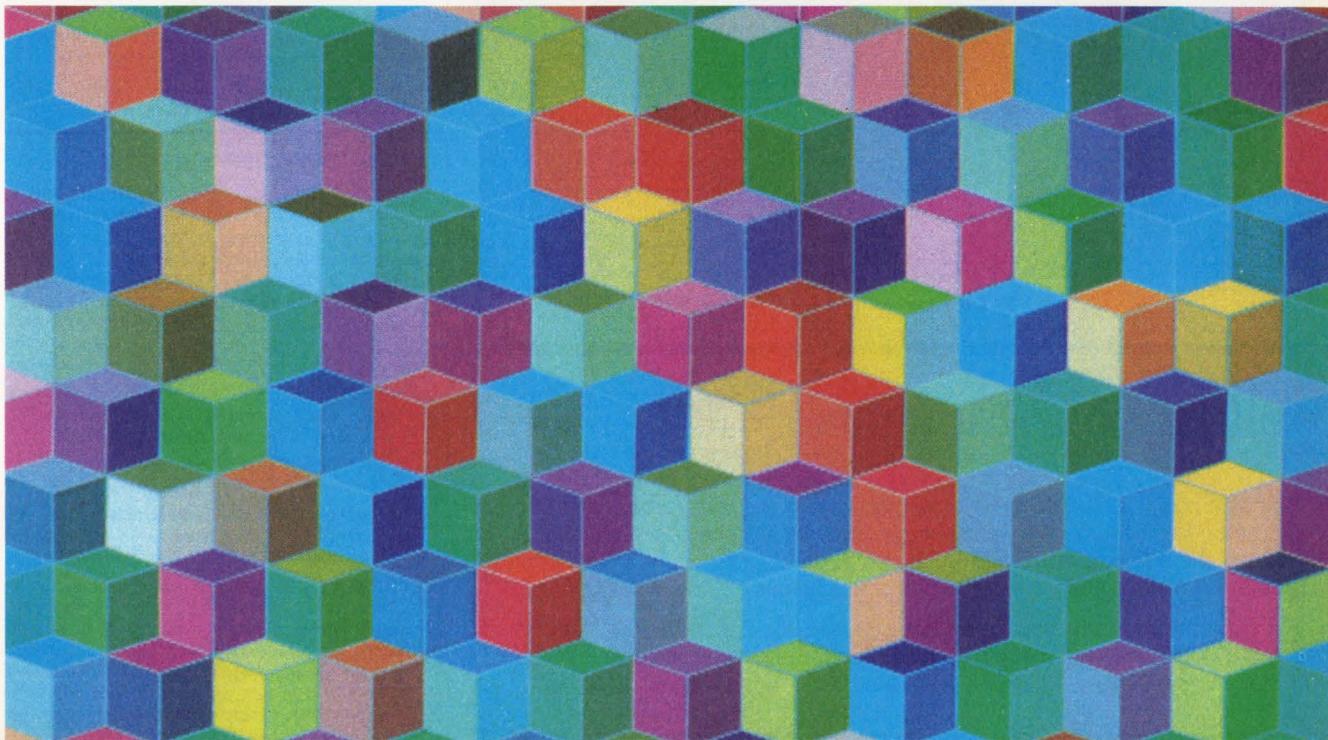
A company you can count on to help you see more in graphics—and get more out of graphics—both now and in the long term.

For more information, write Lundy, Glen Head, New York 11545, or call: (516) 671-9000.



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The two for one buy of the Century.

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- Optional plug-in 128K RAM.

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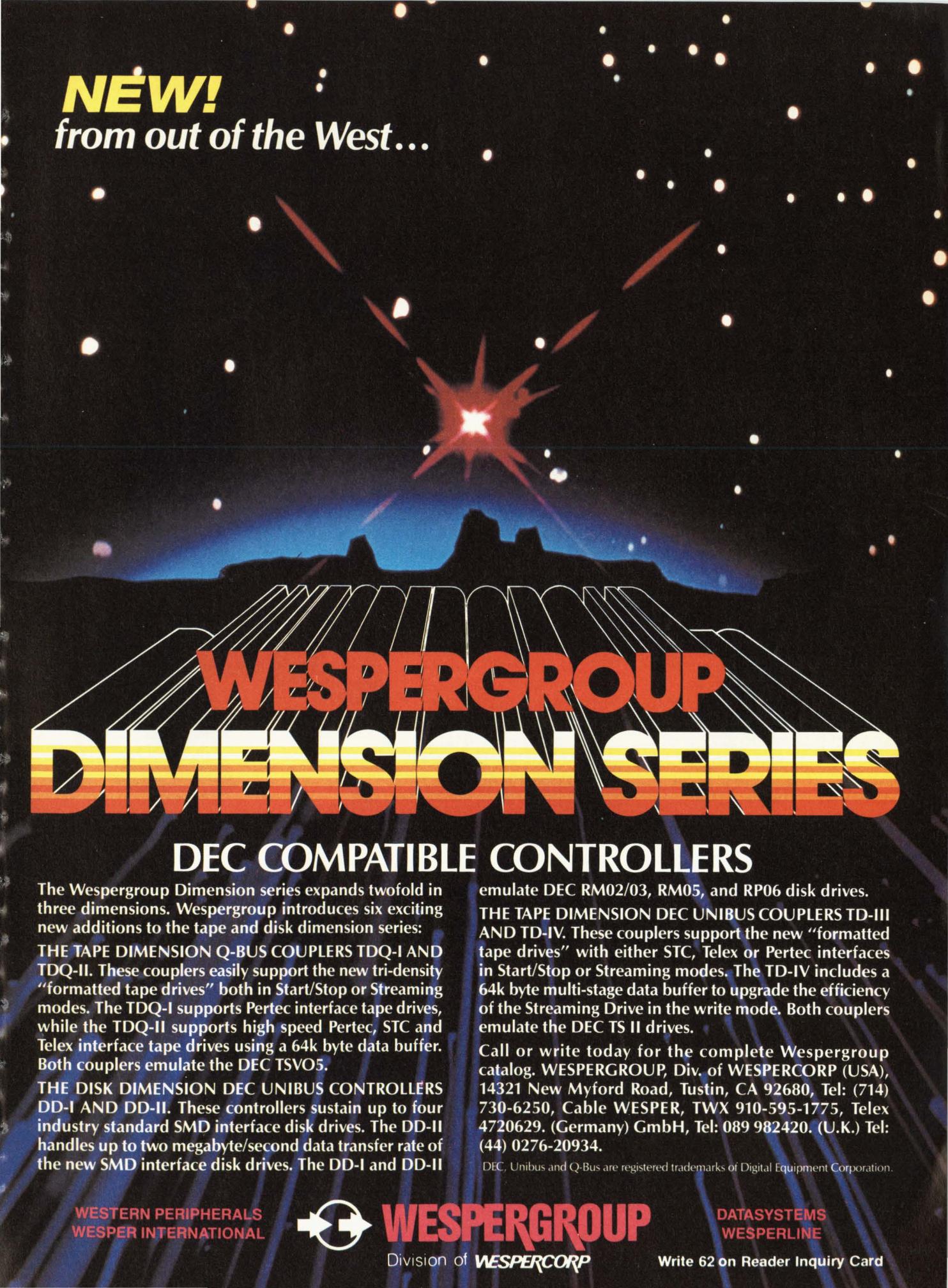
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THE TAPE DIMENSION DEC UNIBUS COUPLERS TD-III AND TD-IV. These couplers support the new "formatted tape drives" with either STC, Telex or Pertec interfaces in Start/Stop or Streaming modes. The TD-IV includes a 64k byte multi-stage data buffer to upgrade the efficiency of the Streaming Drive in the write mode. Both couplers emulate the DEC TS II drives.

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Floating Point Systems array processor to break

The FPS-5000 Series from Floating Point Systems

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words is available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the

Typical performance examples of geophysical, medical imaging and signal/image processing applications.

Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation/Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 msec.

Based upon specifications subject to change.

FPS-5000 Series sets a new standard for cost-effective computing, breaking the \$2,000 per MFLOP* barrier—the first time this has been achieved in any floating-point computing system.

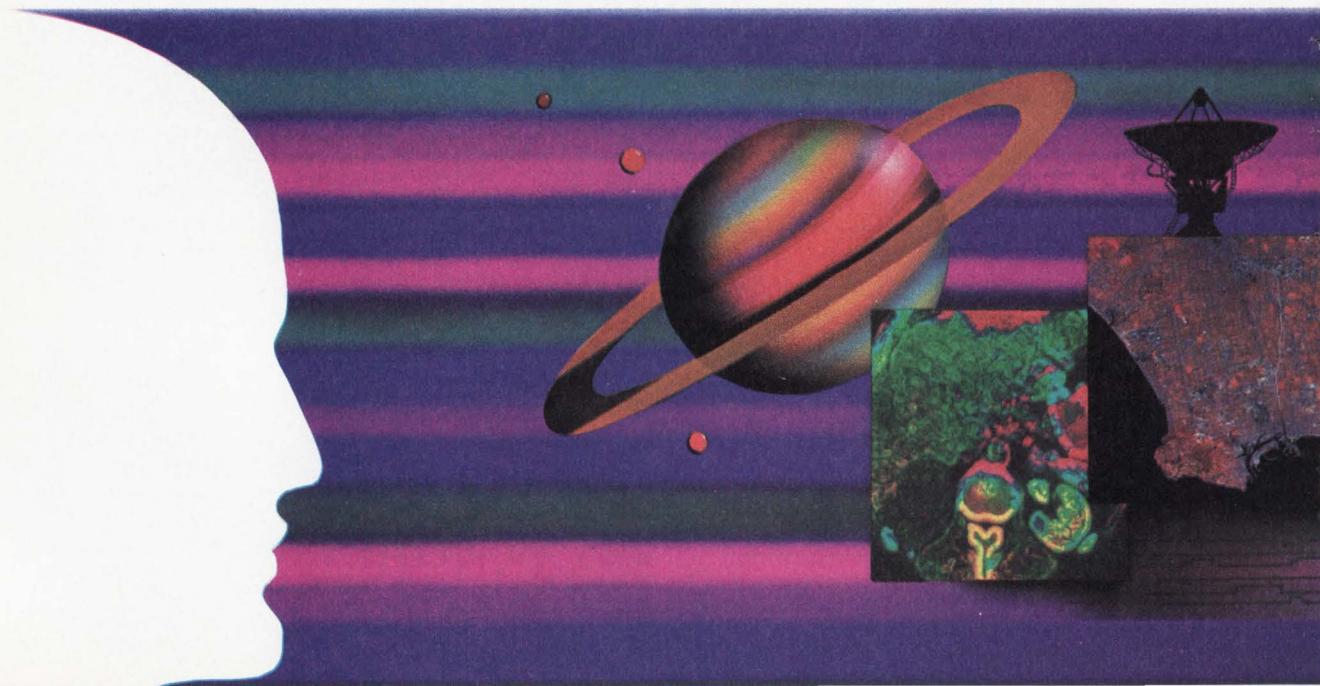
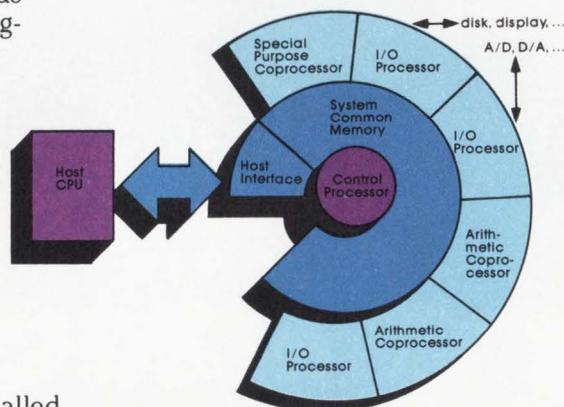
*Based on U.S. Domestic Prices

Distributed processing architecture

The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called

Arithmetic Coprocessors. Data flow is simultaneously managed

FPS-5000 Series Architecture



introduces the first the \$2,000/MFLOP barrier.

by a combination of independent I/O Processors and the central Control Processor.

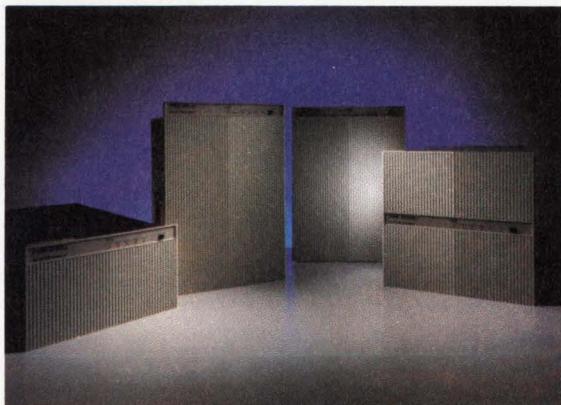
Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

The new Multiple Array Processor Execution Language (MAXL), based upon FORTRAN 77, allows the user to construct an integrated system environment which can be tuned to application requirements.

Increased performance can be achieved by adding Arithmetic Coprocessors as a field-installable upgrade as the user's requirements evolve.

Compatibility

The FPS-5000 Series maintains software compatibility with previous FPS 38-bit processors and is supported on a range of host computers. Thus, the extensive



software support developed for FPS-100 and AP-120B products is maintained and users are able to move existing applications onto the FPS-5000 Series with minimal effort.

Quality and Reliability

The FPS-5000 Series was designed and built with the same quality standards inherent in all of the previous Floating Point Systems products—standards that have earned those products a reputation for unprecedented reliability and one of the best

meantime between failure (MTBF) rates in the industry.

The Series is backed by the same outstanding worldwide support services that distinguish Floating Point Systems from other manufacturers.

For more information about how the FPS-5000 can be used in your specific application, call (800) 547-1445 or your local sales office.

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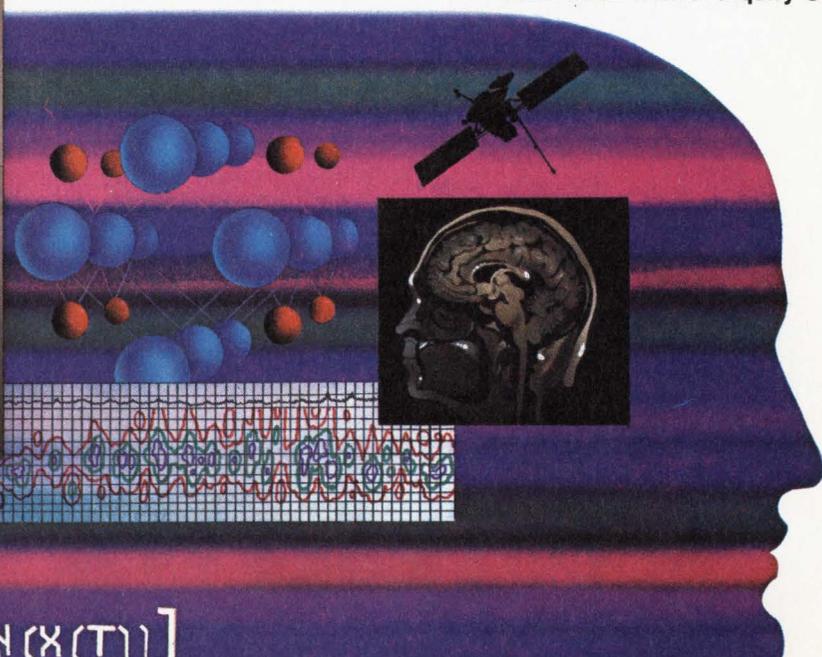
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FFT [HANN(X(T))]

EDITOR'S COMMENT

Traditionally, winter is when the computer industry takes a respite from the rush of the trade conference circuit. The Softcon Conference, the National Software Conference, and the annual meeting of the UNIX user group, UniForum, have changed this. Softcon has become the third largest trade show after the National Computer Conference and the fall Comdex even before its first meeting! The UniForum, attended by as many as 10,000 people overflowed the halls and exhibit space of the Washington Hilton Hotel. The Interface Group, sponsors of the bi-annual Comdex events have also announced a "Winter" Comdex to take place this April in Anaheim which will ostensibly feature both hardware and software, with the emphasis on the latter. This flurry of activity is in stark contrast to the annual "Software Expo" held in September of last year in Chicago which was all but ignored. To be certain, the program and the exhibitors represented a significant portion of the developers and marketers of software, but the emphasis of the event was tacitly that of mainframe computers. Co-sponsorship of the event by ADAPSO, which is made up of the Data Processing Service Organizations, tended to affirm this orientation. The recent Softcon earns recognition for the breadth of developers that were present, even though the majority produce products that support the IBM PC.

While many of us in the computer industry will miss the quiet time winter afforded in the past, we have long needed meetings that address the software industry and its developments. The UniForum show was highly unusual for a trade conference that has as its announced aim the meeting of "users" of one product. Hopefully, other conferences can be as substantive for attendees. UniForum was, as one manufacturer said, "not the sort of show where the attendees give you much room to tap dance." The organizations represented and the tenor of the meetings made it clear that those present were there to obtain information and resolve problems related to the purpose of the conference. The conference attracted equal representation from both hardware and software vendors, as well as those vendors in both areas. Motorola, Zilog, and National Semiconductor were there from the semiconductor industry while IBM, Gould, Hewlett-Packard, Data General, and Digital Equipment attended from the systems world. The producers of workstations were surprisingly well represented: Sun, Apollo, Cadmus, Masscomp, and Methus, as well as the producers of single chassis, multi-user systems such as Victory, Fortune, Momentum, Callan, Codata, Plexus, and Naked Mini. Software vendors were led by the venerable Western Electric discussing Systems Five UNIX. Many designers in attendance from the UNIX community feel that Western Electric's announcement, tentatively slated for the spring Comdex show, will provide not only the company's first commercial computer, but an impatiently awaited release of a new UNIX generation. The news that IBM chose the UniForum Conference as the venue for the release of its UNIX implementation of the IBM PC/IX was no surprise, although there was sufficient criticism of the product to question its potential impact on the marketplace. Typically, the release broke no technical ground, based upon System III and the PC expansion chassis, but added weight to the already wide acceptance of UNIX.

The directions evident at the conference ranged from the

vendors working to provide systems manufacturers with working implementations of UNIX to companies working on enhancements to UNIX for their systems. Cambridge Digital, for example, offered no less than six licensed implementations. Gould continued with its intensive development of UNIX for its recently formed Systems Division. The body of "UNIX like" operating systems, among them UNOS (from Charles River Data) and DEC's new ULTRIX, also continue to show strength. The body of UNIX emulators, however, such as Venix, and the enhancements, such as the Berkeley 4.2 appear to be giving some of their most advantageous characteristics to the mainstream of UNIX software. The revisions offered to UNIX by companies such as Sun Microsystems tend to lend weight to a single stream of development for the software. As developers incorporate the best of other vendors software, the overall distinctions lessen. This trend is further encouraged by the selection of Motorola's 68000 product family as the processor of choice in design.

There is a good deal of support from engineers and designers for a common operating system that would afford both efficient use on multi-user systems, system portability, and all of the lauded programming support tools of UNIX. The exhibitors at UniForum had diverse views on the potential represented by UNIX, among them the idea that UNIX is rapidly becoming the equivalent of CP/M for the universe of multi-user systems. Some feel that it is the operating system for the growing number of 16/32 and 32 bit processors. There are others that have a substantial interest in real time applications, such as Sky Computer. Hewlett-Packard sees UNIX as a tool in its expanding business systems, but also for its engineering and scientific systems.

UniForum was in part a reflection of the success of the Comdex exhibits which are the largest gathering of desktop/multi-users systems. The reflection, to this attendee, is that the needs of users are dependent upon the ability of programmers to provide applications specific software. Furthermore, the reality of the marketplace for the next year is that the production of processors upon which much UNIX work is being performed, is limited by the availability of devices from Intel. Given the limited number of vendors with microcomputers that will play a role in multi-user system, the workstation product design, the body of UNIX developers will have a major influence on the market for systems during the next several years. Of more importance is the determination of who will supply systems for the 32 bit generation of microcomputers.

On another note: you may have noticed our new cover. As part of our ongoing effort to improve *Digital Design*, and as a first step to a more comprehensive graphic redesign, we have selected a format more in keeping with our editorial coverage. The spine of each issue now carries the topics found in a given month, and in January we provided the first comprehensive subject index for the calendar years, 1982 and 1983. In coming months, we will continue to introduce changes that will make *Digital Design* one of the most informative and enjoyable magazines in this industry. Please let us know if you like our changes, we believe that our readers are our best critics.

Jerry Borrell
Editor-in-Chief

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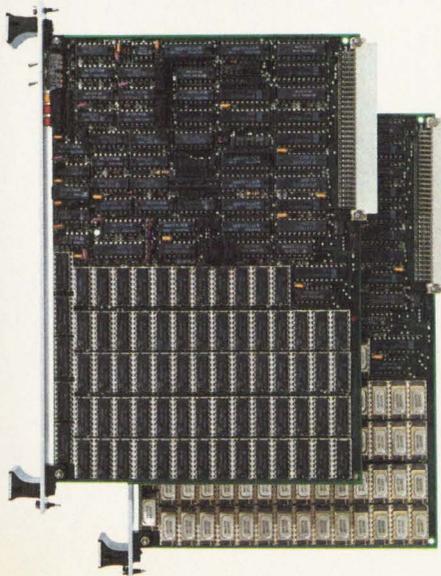
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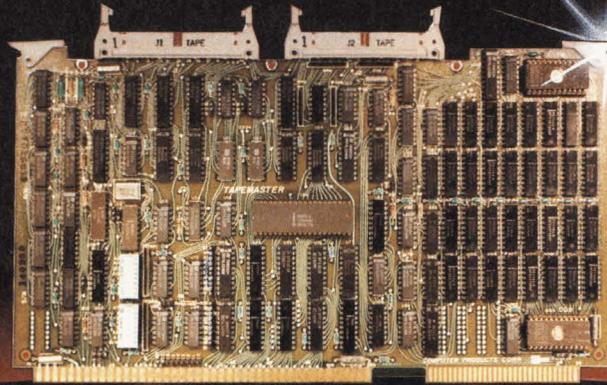
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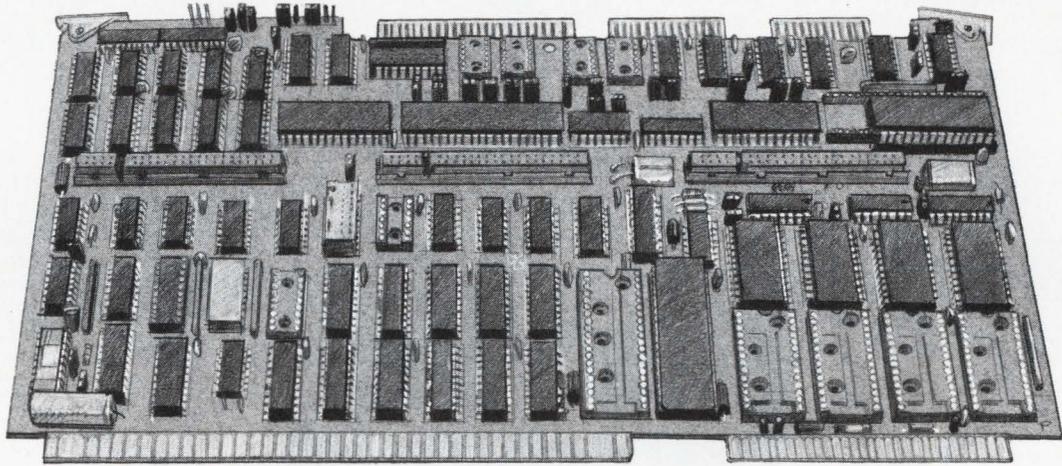
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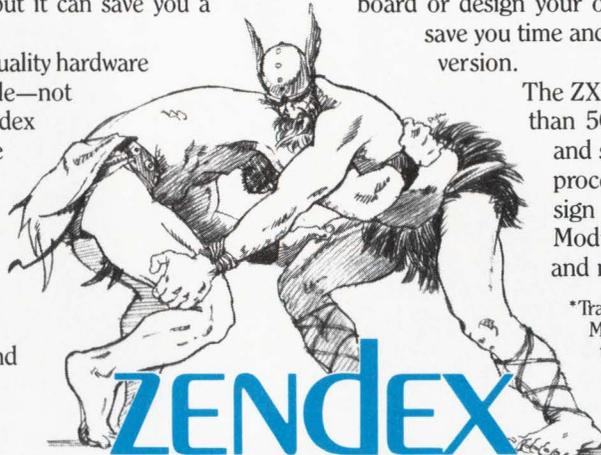
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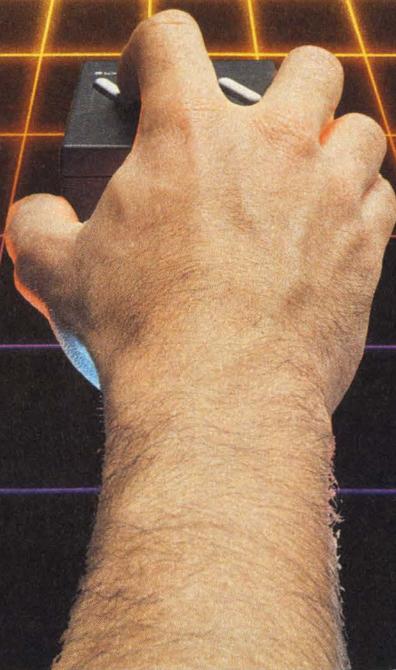
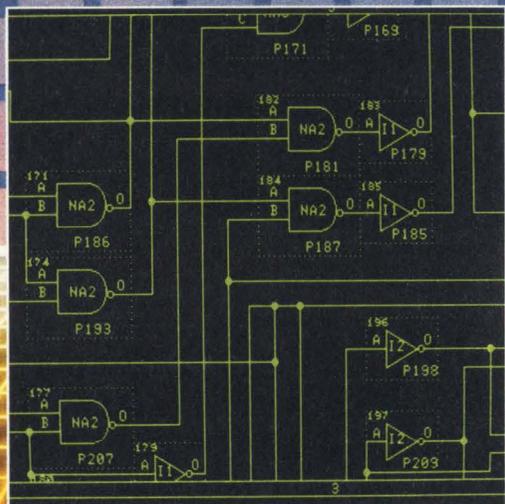


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SuperMinifloppy Pact

Drivetec, Inc., announced an OEM contract with Kaypro Corp., Solana Beach, CA, for an undisclosed number of disk drives with an initial value of over \$6.0 million.

Drivetec's Model 320 SuperMinifloppy is a 5.25-inch flexible disk drive with 3.33 Mbytes of capacity in a half-height size. Kaypro will incorporate two drives in their new Robie™ desktop computer. In addition to its capacity and size, the Model 320 SuperMinifloppy offers a 3-millisecond track-to-track access time and 500 Kbit/second data transfer rate.

Mixed Packages

Digital Equipment Corporation announced availability of new system packages combining its 36-bit mainframe computers and its 32-bit superminicomputers. The offering is the first time Digital has offered DECsystem-10 and DECsystem-20 computers in combination with VAX-11/780 superminicomputers in standard configurations. The arrangement enables users to obtain maximum benefit from both mainframe and VAX resources. The new mainframe/VAX packages are connected through Digital's DECnet networking software to interchange data and files. By using appropriate software packages, including the FTS-20 file transfer spooler and DIL data interchange library, the mainframes and VAX computers have access to each other's data bases.

Intel, Inmos CHMOS RAMs

Intel Corp. and Inmos announced an agreement to develop methods for consistent complementary high-speed, metal-oxide semiconductor (CHMOS) dynamic random-access memory (RAM) products. The effect of the agreement is to provide potential users of either company's CHMOS dynamic RAMs with a second source of supply. Second sourcing often is an important consideration in dynamic RAM purchase decisions.

Intel and Inmos intend to work separately on dynamic RAM designs and CHMOS technologies, but will keep key specifications consistent. The agreement between Intel and Inmos

applies only to CHMOS dynamic RAM specifications. Each company plans to independently develop and introduce 64Kbyte and higher-density products.

New JEDEC Standard

The Electronic Industries Association announced the availability of JEDEC Standard No. 7 which includes industry specifications for 3 series of new high speed silicon gate digital ICs. The 54/74HCXXXX series includes buffered CMOS logic devices with the primary characteristic of v_{IL} and v_{IH} ratings for good noise immunity in all-CMOS system designs. The 74/74HCXXXX series includes a limited number of unbuffered (1 active logic circuit) inverters or gates where v_{IL} and v_{IH} ratings are less than those of the HC series. The third series is designated 54/74HCTXXXX having v_{IL} and v_{IH} ratings of .8V and 2V respectively for direct interfacing with TTL logic ICs.

True 32-bit Machine For Multibus II

The Logical Computer Company, Chicago, IL, may be first out to market with the Multibus II system based on the National Semiconductor's 32032. The company has already gained experience with National's product line by debugging first samples of the 16032. The new product is expected to support memory access with no wait states using Intel's iLBX II bus running at 10MHz as well as the Multichannel II bus specs Intel released at Comdex '83.

California-Japan Trade Exposition

The State of California has been invited by the Japanese government's Manufactured Imports Promotion Organization (MIPRO) to co-sponsor the first "Greater California Exposition" to be held March 30 through April 3, 1984 in Tokyo, Japan. This is the first time MIPRO has chosen an individual state to promote its products and services in the Japanese marketplace. California companies interested in tapping business opportunities in Japan are encouraged to participate in this event.

IBM-Compatible Communications

Communications Solutions, Inc. (CSI), of San Jose, CA, announced that several computer and communications vendors have chosen its ACCESS/SNA™ software as their standard for IBM-compatible communications. The companies are Texas Instruments, NCR, AT&T Information Services, 3Com, AST Research and NBI. Integration of ACCESS/SNA into their products allows these vendors to sell into the IBM market, communicating with IBM host computers and coexisting with IBM equipment in a user's network. Applications range from NBI's office automation systems to 3Com's local area networking products.

Personal Instrument Users Society

Northwest Instrument Systems Inc. and FutureNet have formed PICUS, the Personal Instrument Computer Users Society, to stimulate the exchange of information among the growing numbers of personal instrument users. Personal instruments are personal computer controlled tools used for a variety of application-specific tasks from logic analysis to computer-aided engineering. The personal instrument market base is projected to grow to \$400 million within the next five years.

A major focus of PICUS will be the exchange of software applications programs between vendors and customers.

Three-Way CP/M Agreement

Digital Research Inc. has reached an agreement with American Microsystems Inc. (AMI), a subsidiary of Gould Inc., and Zilog Corp. to embed Digital Research's Personal CP/M operating system into a single-chip, integrated, operating-system processor based on the Z80® microprocessor. Under terms of the three-way agreement, Digital Research will provide Personal CP/M to AMI and Zilog for inclusion in a single-chip operating-system processor that AMI will design, using its ACT™ computerized chip design software. The two semiconductor companies will manufacture, market and distribute the CP/M operating-system processor.

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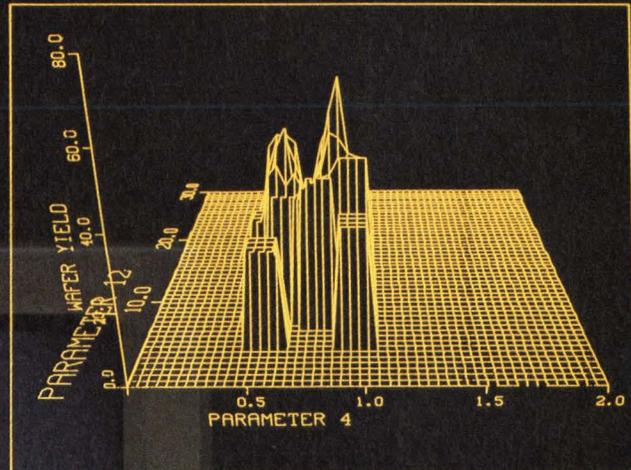
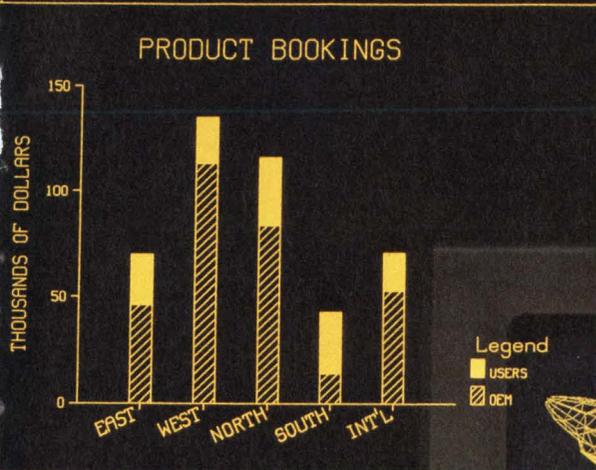
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Congress Supports Biotechnology Research

by Anne A. Armstrong

The idea of using organic molecules such as proteins to create computer circuits instead of silicon or gallium arsenide is mostly theory. But it is an idea that is attracting more and more interest in the research community. The National Science Foundation has recently sponsored a conference to discuss the possibilities of a chemical computer. Companies such as Genex Corp. in Gaithersburg, Md., and Gentrionix Laboratories in Rockville, Md. are trying to establish commercial businesses based on the new technology, but the key to the success of any new research venture is money, and some of the new companies capitalizing on biotechnology have had trouble generating financial support.

However, the possibilities the new research offers for building faster, smaller computers have attracted the attention of Congressmen. Representative Ike Skelton (D-Mo.) became interested in what is sometimes called "biochip" research out of a dual concern that the United States should not lose its dominance in the computer field and as a possible solution to problem of electromagnetic pulse following a nuclear blast. Current theory says that all conventional machinery would be knocked out of service following such a disaster. A biological computer might not be affected in the same way, Skelton was told.

After meetings with small businessmen and university researchers, Skelton proposed an amendment to the Defense Joint Authorization Bill which would set aside \$10 million for research into biotechnology. The amendment was defeated and did not make it into the final bill, but the language and intent of the amendment was retained in the report accompanying the legislation. As part of the legislative history, it shows that Congress approves of as much as \$10 million of the Defense Advanced

Research Projects Agency's (DARPA) budget going for research in this area.

"What happened was the stipulation was changed from a legal requirement to a Congressional suggestion," said a staff aide on the appropriations committee. One reason for the change, according to the program manager at (DARPA), is that the agency does not have enough well-defined technical proposals in this area to justify that kind of money.

Currently, as part of the \$600 million supercomputer program, DARPA is funding \$3.5 million in research in fiscal 1984 for biotechnology projects — which include some work on how to engineer analog computers. But, DARPA scientists have serious reservations about the claims that a 3-dimensional organic structure can be built with switching properties. Although they are interested in serious projects in biotechnology, DARPA officials cannot see \$10 million going into chemical computer research any time soon.

DOD: Buy Or Lease?

As Congress was rushing to end its session, the Department of Defense narrowly escaped having its right to lease automatic data processing equipment taken away. Presented with tales of waste and abuse in leases of computing equipment, the U.S. House of Representatives wrote into the 1984 DOD appropriations bill a prohibition on any further leasing and directed DOD to buy all computers currently under lease.

Cries of alarm from the computer industry and from the Defense Department plus heavy lobbying from all sides persuaded the Senate not to include the lease ban in its version of the money bill. At a House-Senate conference committee meeting to reconcile the differences in the two bills, the House was finally convinced to eliminate the no-lease language when serious questions were raised about the amount of money needed to buy out all the leased computers and about the advisability of an all-out ban on leasing.

The lease issue started when studies by the General Accounting Office and

the investigative staff of the House Committee on Appropriations stated that DOD spent \$900 million on general purpose ADP equipment in 1982 and that hundreds of millions of it was wasted. Examples of uneconomical leasing arrangements were catalogued. The Air Force Manpower and Personnel Center at Randolph AFB began leasing a Burroughs B-6700 system in 1973. By September 1982, the center had paid more than \$29 million in rent for a system which could have been purchased for \$10.7 million. The Automation Management Office at Fort Lee, Va. began leasing an IBM optical page reader in October 1971 and by September 1982 had paid rent totaling more than \$67,000 for equipment which could have been purchased for \$21,890. In addition, the same office has been leasing card punch equipment for 16 years, paying out enough to buy the machines four times over.

Based on its findings, the appropriations committee recommended cutting \$680 million out of the DOD ADP acquisitions budget. The committee staff said that amount could be saved by terminating leases and buying computing equipment outright. The House-Senate conference reduced the estimate of savings each year to \$150 million and set that aside to purchase leases.

As it turned out, no one was exactly sure how many computers the remaining money would buy out. "There has been no study at all to determine how much that sum will buy," said Vico E. Henriques, president of the Computer and Business Equipment Manufacturers Association (CBEMA). "It's an arbitrary number, and probably completely inadequate to buy out the leases on all of Defense's equipment. What will happen to national security if suddenly hundreds of computers are disconnected?" he said. "Our quarrel is not with the decision itself, which is a management decision, but with the precipitousness of the action and its probable consequences."

One industry spokesman described the whole issue as an overreaction. "Sure, there are problems, but look at

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Extensive applications libraries include math, signal processing, and image processing.

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the 25 cases they have documented compared to the 480,000 leases DOD currently administers with no abuses."

In the end, CBEMA's view prevailed. The conferees retained the House's figure of \$150 million set aside to buy existing leases, but admitted that the funds would only support "a modest buy-out program."

Another important feature retained in the final bill is a very critical evaluation of DOD'S use of General Service Administration "schedules." These open-ended contracts have prices already negotiated by the government; however, the committee said Congress does not consider buying computers from GSA schedules as competitive purchasing.

High-Tech Republicans Endorse Chip Protection

Although almost everyone in Washington agrees that some sort of protection must be offered to the designers of semiconductor chips, the town is

split on the best way to do that. The Reagan administration and the Patent Office back extending the copyright law to cover the "mask works" used to etch the chips. The Copyright Office, intellectual property experts, and some Congressmen think a special ornamental design bill is the right answer. (*Washington Report, August, 1983.*)

However, the copyright contingent got a big boost recently when the Republican Task Force on High Technology Initiatives, a group of 140 members headed by Rep. Ed Zschau, decided to support the Semiconductor Chip Protection Act (H.R. 1028). More hearings and meetings with concerned parties are expected after Congress reconvenes in January.

DP Standards Unit Escape Budget Cuts

Early in 1983, the Reagan administration announced a plan to end the government's involvement in estab-

lishing data processing standards. As part of the new approach, the private sector would have to take over developing standards for the industry and the organization which previously had the job would concentrate on research and development.

From the start the plan to reduce the budget of the Institute for Computer Sciences and Technology by 70% and transfer its function to the private sector was in real trouble. The private sector wasn't clamouring for the job, and opponents said there were serious doubts about whether the private sector could handle such a task.

As a result of the criticism from the industry and from scientific circles, the White House changed its mind and restored the money for establishing standards to the budget. In late November, after nearly a year of uncertainty, President Reagan signed the Department of Commerce appropriations bill containing funding for the standards unit.

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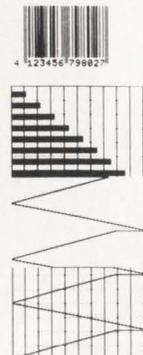
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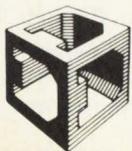
The single board VG-124 interfaces directly to a wide variety of monochrome/RGB cameras, video tape recorders, and video disks. It also provides a software selectable sync source as well as an enhanced DUAL-PHASE-LOCK LOOP.

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Advances In Data Acquisition For PCs

Both industrial process control and laboratory research applications can benefit from the speed, reliability, and ease-of-use provided by a computerized data acquisition system. Some of the personal computer-specific applications in which data acquisition systems (A/D and D/A) are used include automatic test, data logging, materials testing, chromatography/spectroscopy, and energy management.

The DT2808, from Data Translation (Marlboro, MA) is a low cost, multifunction data acquisition system compatible with the IBM Personal Computer. Analog input, analog output, and digital I/O functions are provided on a single printed circuit board which fits in one of the host computer's expansion slots.

The DT2808 includes a high level 10-bit A/D converter system for 16 single-ended analog input channels, as well as two 8-bit D/A converters which can be operated independently or changed simultaneously. In addition, the DT2808 features two 8-line digital I/O ports which may be used separately, to read or write 8-bit data, or changed simultaneously for up to 16-bit data transfers.

An on-board microprocessor controls all on-board operations and simplifies program control by the host computer. Routine tasks, such as analog-to-digital converter se-

quencing and error checking are carried out by the DT2808 microprocessor and need not be handled by the host CPU.

Another control feature of the DT2808 is the external trigger. An external trigger is a user-supplied electrical pulse used to specify the exact time at which an A/D, D/A, or digital I/O command begins execution. The external trigger allows the user to synchronize a DT2808 I/O event with some outside event.

Two screw terminal/signal conditioning panels are optionally available for use with the DT2808. The DT707 screw terminal panel provides ease of connection, via screw terminals, for all analog and digital signals, as well as trigger inputs to the I/O board.

Depending on the amount of analog or digital data the board must process, data transfers to the host CPU can occur in programmed I/O (PIO) or direct memory access (DMA) modes. The DT2808 can be programmed in any language that can access the I/O registers of the IBM Personal Computer. Microcoding within the on-board microprocessor greatly simplifies user access to the board's functions.

All functions on the DT2808 are controlled by writing command bytes, command parameters, and data to



Figure 1: The DT2808 brings low cost analog and digital I/O functions to the IBM PC. This single board peripheral fits in one of the host computer's expansion slots.

the command, Data In, and Data Out Registers. Monitoring is accomplished by reading the board status and data from the status register. The user can write his own subroutines for controlling the various board functions or can make use of the optionally available PCLAB, a library of BASIC-CALLable macro-routines.

—Hanrahan

Write 233

Proximity Computer Takes A Step Towards Artificial Intelligence

The retrieval of information based on inexact, incomplete or inaccurate data has been a difficult problem for computers to handle. Many tasks, such as looking up a name, correcting spelling errors or searching a natural language database, demand that the computer be able to perform pattern matching on strings, that is to be able to recognize and retrieve strings that are similar or approximately equal to a query string.

In the past, systems have typically used special purpose algorithms which are limited in their capability. Most schemes for the automatic correction of spelling errors require that the misspelling be incorrect by no more than three deletions, insertions and substitutions. These systems are software implementations constrained by the requirement to rapidly locate a few words within a data base of many tens of thousands of words.

Now, with the introduction of the PF474, from Proximity Devices, there is VLSI solution to the problem of approximate string matching.

In most applications, one string is chosen as a search string or query string. This query string is compared with each string in a large database by the PF474, which computes a Proximity Value for each of the database strings. The highest Proximity Values (corresponding to the best values) are

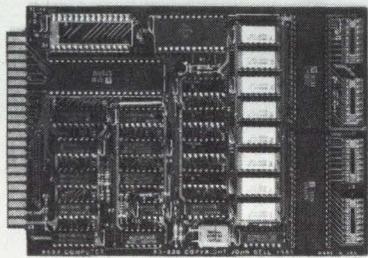
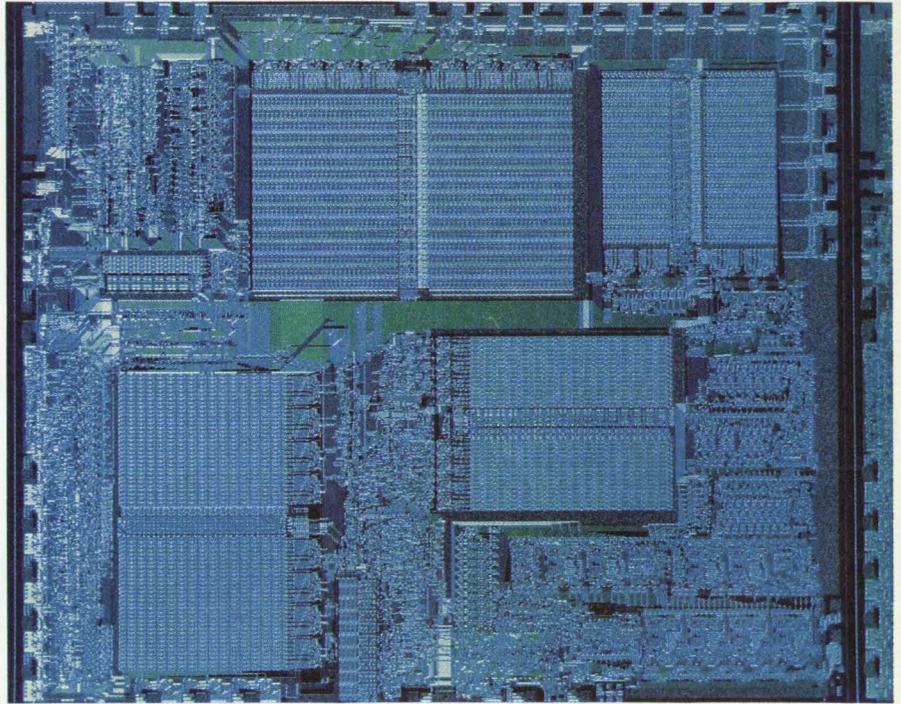
Figure 1: Photomicrograph of the PF474 Chip.

stored in a ranked list in the PF474 for reference at the end of the search.

A natural application area for the PF474 is that of speech recognition. Here, the device might be used at several levels. Its capacity for strings up to 127 characters in length permits a fairly detailed representation of an utterance's phonetic structure to be directly compared against a library. In order to support application development, Proximity has developed standard interface boards for the IBM PC and the Apple II. The IBM PC board uses the hosts' DMA capability and includes a FIFO to couple the data streaming in from the bus with the PF474. It also includes an auto chaining capability that allows it to search multiple strings terminated by a double null, independent of the operation of the CPU.

—Wilson

Write 240



6502 64K COMPUTER-CONTROLLER

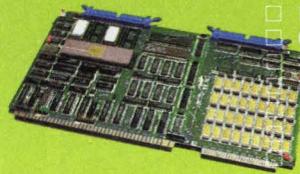
The model 83-230 single board computer has 55K of dynamic RAM, up to 8K of EPROM, four parallel ports, 1 serial RS232 port, and four timers. This 4.5" X 6.5" computer uses the 44 pin AIM bus. This computer was designed to be used as an industrial controller. A 2716 monitor EPROM is available for \$19.95. Bare board for \$49.95 or assembled and tested for \$299.95.

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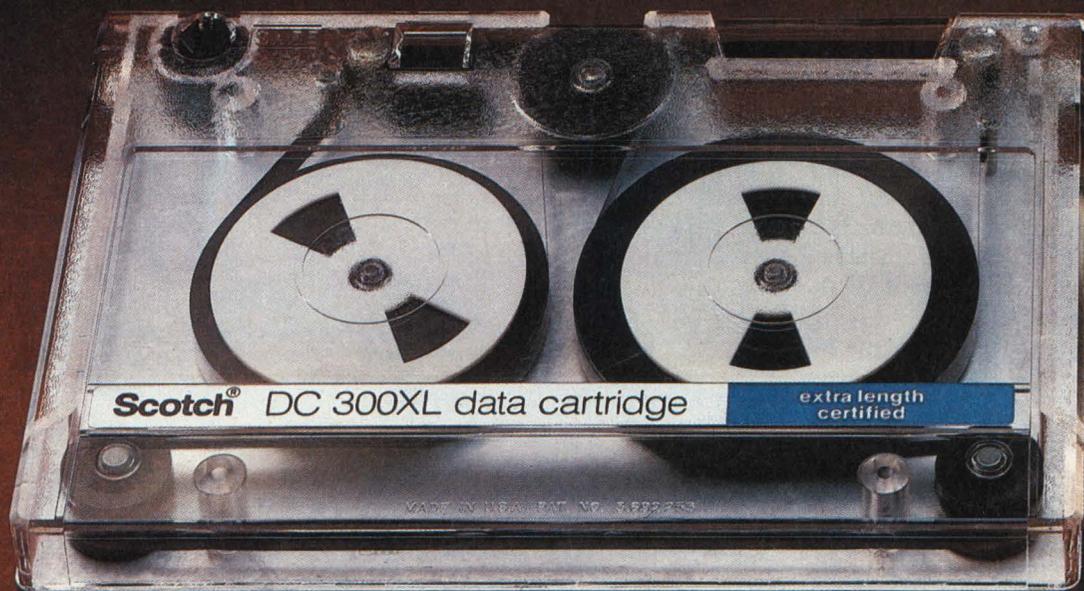
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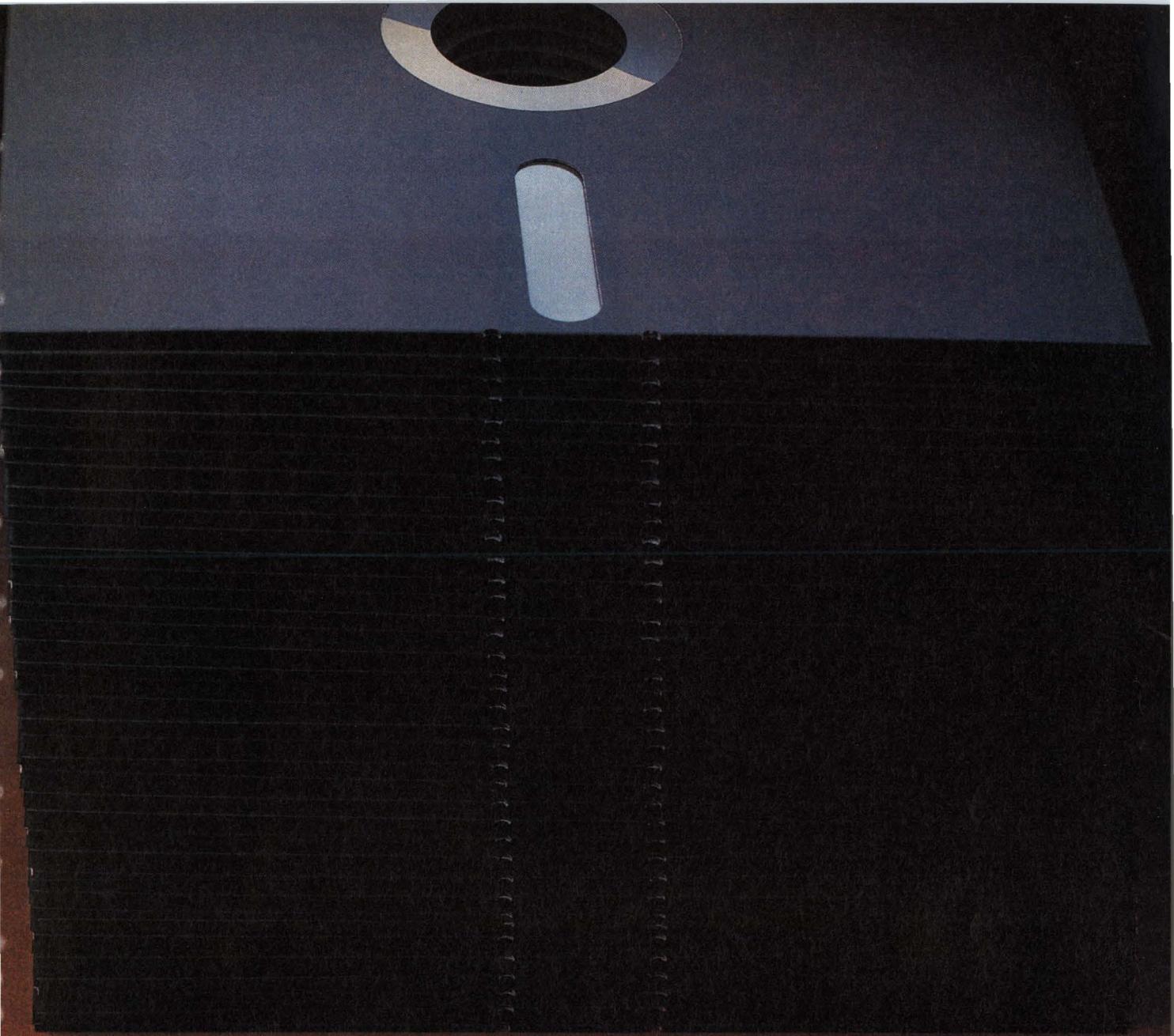
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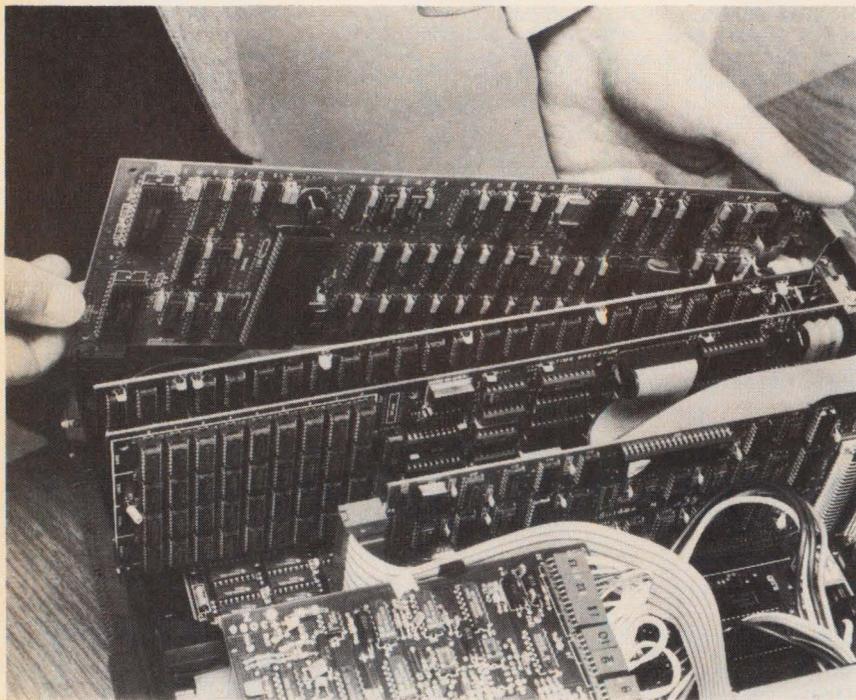
For more information on how 3M $\frac{1}{4}$ " data cartridges can save your customers time, space, and money, write to Chris Binner, National Sales Manager — OEM Market, Data Recording Products Division, Building 223-5N, 3M Center, St. Paul, MN 55144.

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Wang Links To IBM World With 3279 Emulation Board



The 3278 Emulation Board for the Wang Professional Computer, a combined hardware and software package, allows the PC or the Wang PIC professional image computer to access instantly an IBM Mainframe database when attached to a 3270 terminal network. Equipped with the 3278 Emulation board, a Wang PC or Wang PIC becomes an intelligent workstation replacement for a 3278 terminal while maintaining the ability to operate concurrently and independently of host programs. Wang hopes to meet what they see as two important market needs: a Wang-to-IBM and IBM-to-Wang communications interface and a micro-to-CPU link.

Forte Data Systems, Inc. (Santa Clara, CA) supplied Wang with the custom version of its PC 3278/79

microcomputer-to-mainframe communications package. Forte's communication products allow microcomputers to communicate with IBM host computers by emulating the IBM 3278/3279 family of display terminals.

The emulation product's place in the multi-vendor environment enhances the Wang Professional Computers' position as a universal workstation. The 3278 Emulation Board allows the PC to replace the 3278 terminal with the PC's powerful computing capabilities.

Once the 3278 Emulation Board is installed, a Wang PC or Wang PIC can attach in native mode to a 3270 terminal network. No modems, telephone lines, or special cabling are required. Both Binary Synchronous Communications (BSC) and Systems

The combined hardware/software package from Forte Data Systems will provide Wang PC users instant access to IBM mainframe databases.

Network Architecture/Synchronous Data Link Control (SNA/SDLC) protocols are supported.

A Wang PC or Wang PIC with the 3278 Emulation Board has total display symbol compatibility with all 3278 terminals on the network. A single keyed command allows a user to make instant and transparent operating mode transfers between 3278 emulation mode and the current PC program.

The 3278 Emulation Board occupies only one I/O slot on the Wang PC's chassis and doesn't reduce the amount of memory available to the user. Because local processing at the PC does not affect host sessions, the 3278 Emulation Board reduces costs by making the central computer more available to other users. Other marketing features of the emulation package which emphasize its adaptability include menu access to full-screen host applications; verification of line activity and condition; and an independent, on-board serial RS-232 interface that alleviates the need for an IBM asynchronous communications adapter board and frees an I/O slot normally required for such an interface. The 3278 Emulation Board is available as a standalone product or as an attachment to the WangNet CMUX0-3270 Cable Multiplexer, an interface device linking IBM 3270 peripherals with an IBM 3274 Control Unit over the WangNet local area network. Priced at \$1,095, the 3278 will be available in March of 1984.

—Wang Laboratories **Write 238**

Telephone/Display Terminal Market Takes Shape

After a slow start, the U.S. market for integrated telephone/display terminals is beginning to materialize. In 1983 shipments in this market amounted

to over 32,000 units at a value exceeding \$43 million. Expected to provide a further source of growth for this market are the newly announced

entries of such firms as Televideo, Rolm, AT&TIS, Sydis, and Digital Transactions.

At present, the bulk of the market



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consists of low end, non intelligent terminals such as Northern Telecom's Displayphone, Tymshare's Scanset XL, and GTE's ActionStation. According to a market report by Advanced Resources Development (Medfield, MA), these devices are marketed through two primary channels: as devices for access to public data bases and communications networks; and as high end telephone devices in voice/data PBX communications networks. As new participants such as Televideo, Rolm and AT&TIS begin marketing their products, new target markets and applications are expected to develop for the low end.

The second largest segment of the integrated telephone/display market is the multifunction workstation segment. Currently this segment is dominated by Mitel, with its Kontakt workstation, and Davox, with its Series 921 workstation. These devices will be particularly attractive to managers and executives who require both fully featured telephone devices and standalone data processing devices.

A very small segment at present consists of word processing stations with integrated telephones. There is only one current participant in this segment, Basic Telecommunications,

but Mitel is expected to announce a product in this segment in the near future. Although voice/display products have a tremendous potential for growth, much of this potential will be hampered by unclear target markets and applications. As these problems are overcome, shipments could skyrocket, until then, the major source of growth in this market will be application-specific sales, for data base access or along with voice/data communication networks. ARD predicts shipment levels to reach over 200,000 units annually by 1986, with most of the growth attributable to the efforts of new market participants.

Write 239

U.S., Japanese Collaboration Provides IC Products For The Total System

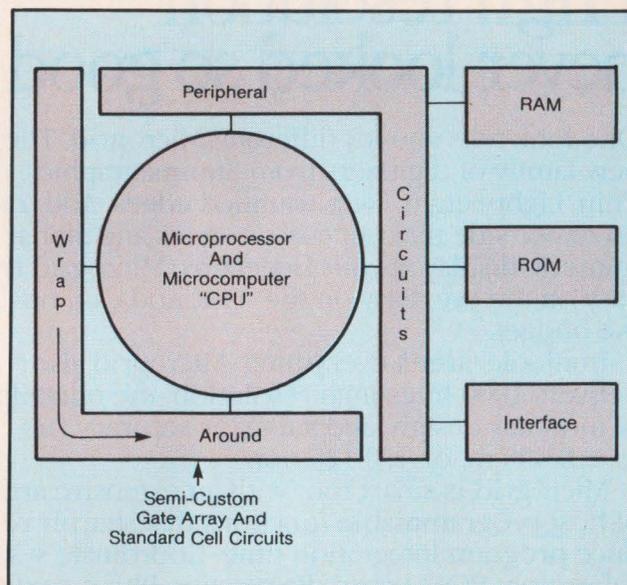
Computer systems and telecommunications manufacturers have created a market need for advanced large scale and very large scale integration (LSI and VLSI) CMOS products. Total systems requirements for CMOS include products such as μ Ps, RAMs, ROMs, logic arrays, interfaces, and single chip microcomputers. A company formed to meet these varied manufacturing needs is S MOS Systems, Inc. of San Jose, CA, which operates in conjunction with the Suwa Seikosha wafer fabrication facility in Fujimi, Japan.

S MOS has been allocated captive capacity scheduled to grow to approximately one-third of Suwa Seikosha's current production, consisting of more than 35,000 4" CMOS wafers per month. This will be increased by an additional four to five thousand 5" two-micron wafers once an additional plant comes into production early this year.

Suwa Seikosha, also manufacturer of Seiko watches, consists of a group of companies, including Epson Corporation, with a workforce of 10,000 people and sales of \$1.3 billion during the last fiscal year.

S MOS has absorbed the backlog, inventory, and sales network of

Figure 1: S MOS Systems will provide IC products for the total system.



Epson's Semiconductor Division, hoping to combine "U.S. strengths in marketing and creative engineering with Japanese efficiency in production" according to S MOS president, Dan Hauer.

S MOS intends to provide all the components needed for a 100% CMOS system. The first S MOS products are 16 K-bit static RAMs and 64 K-bit and 256 K-bit masked ROMs. These memories are available in various configurations, totaling nine different products. The first VLSI product for S MOS will be a 64

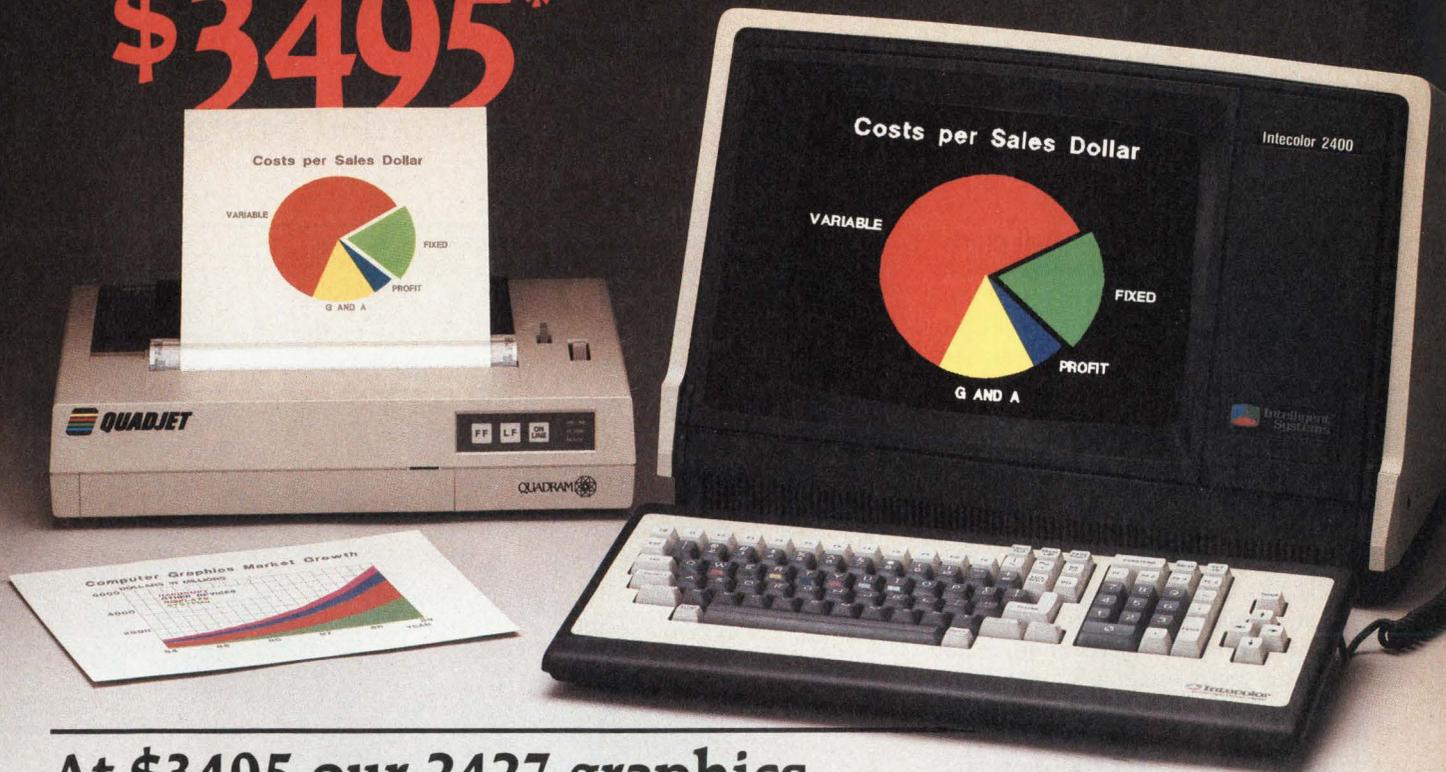
K-bit static RAM, to be announced sometime in 1984.

The Suwa Seikosha facility, where S MOS's product line will be built, is a state-of-the-art CMOS factory currently producing over 35,000 4" wafers per month. The Suwa Seikosha plant will soon begin producing an additional 5,000 to 6,000 5" two micron wafers per month.

As part of the company's policy to provide the IC products for the total system, S MOS will be offering semi-custom gate arrays and cell designs.

—S MOS Systems **Write 236**

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The 2427 has dual processing power—a 16-bit Z8002 to drive graphics and an 8-bit 8085 for terminal functions. It has all the VT52 and VT100[†] features you'll ever need, so it works well with DEC editors. And it's compatible with TEK 4010, 4027 and PLOT 10[†]. Plus it's ANSI X3.64 compatible, so your code is easily portable. To speed up programming, you get 12 function keys (normally optional) at no charge.

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Dual Processor Viewstation Provides 3D Shaded Surfaces

GEOVIEW, Lexidata's dual processor viewstation, is currently used by exploration geophysicists to locate oil and to determine the most effective methods for its retrieval. Advanced surface modeling software allows the user to visualize complicated functions and interpret the data interactively. Because a large amount of two dimensional and three dimensional graphics data processing is required in seismic analysis, GEOVIEW's dual processor architecture distributes the workload between a general purpose microcomputer and a high-speed imaging/graphics processor.

Featuring a special surface modeling software package, Lexidata's GEOVIEW imaging and graphics workstation enables the seismic interpreter to display contour maps and regular gridded data as 3D shaded surfaces for analysis. GEOVIEW is based on the Lexidata ViewStation which can operate as a remote viewing station or satellite processor to a large host computer. The Surface Modeler, a complete surface modeling software package, allows the user to display multiple geological horizons, making it possible to compare both structural relationships and interval thicknesses between various horizons. The Surface Modeler incorporates Lexidata's SOLIDVIEW display technology in which surfaces are constructed incrementally to form a complete 3D display. The user may select a vertical plane in the model and then remove a section to allow closer inspection of the interior of a group of surfaces. Cross-sections are easily displayed and the operator may apply translucency to any arbitrary surface so that areas inside or behind can be studied. All of these capabilities are under the control of the user and all are performed locally in the GEOVIEW system without host computer intervention.

The large display memory allows the interpreter to store up to seven full resolution views, simultaneously, and alternate between them as desired. More views may be stored at lower

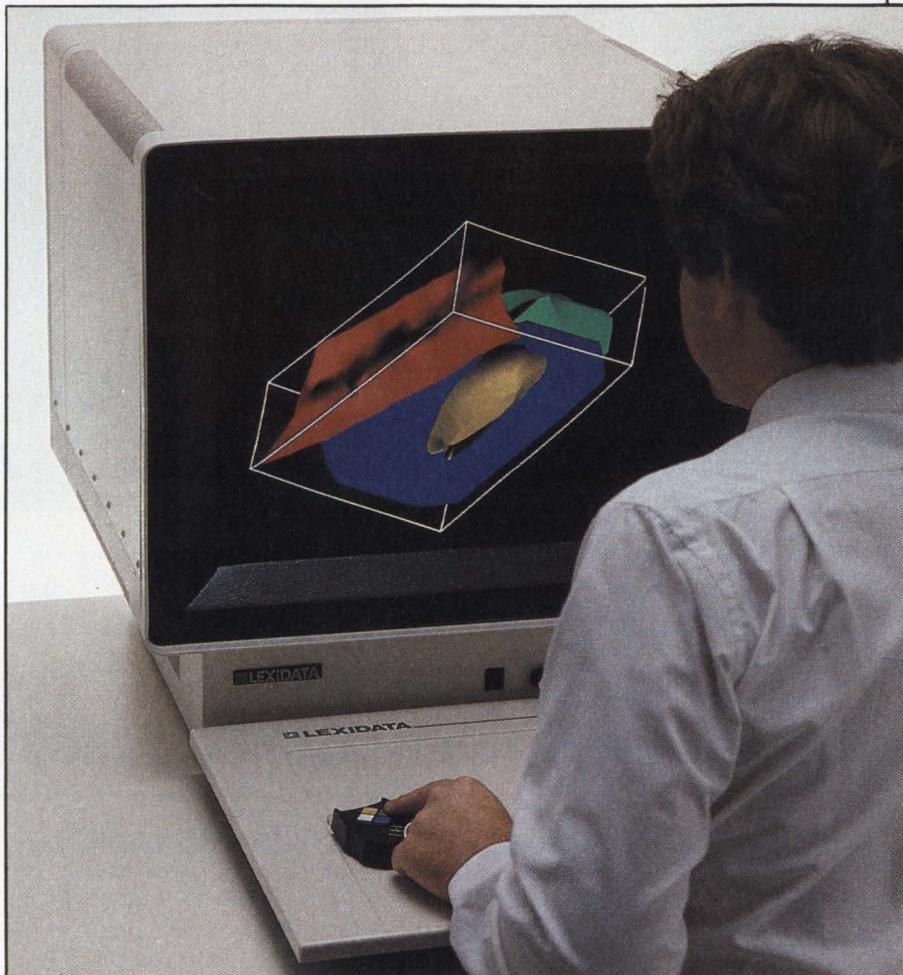


Figure 1: A geological solid model displayed on Lexidata's GEOVIEW.

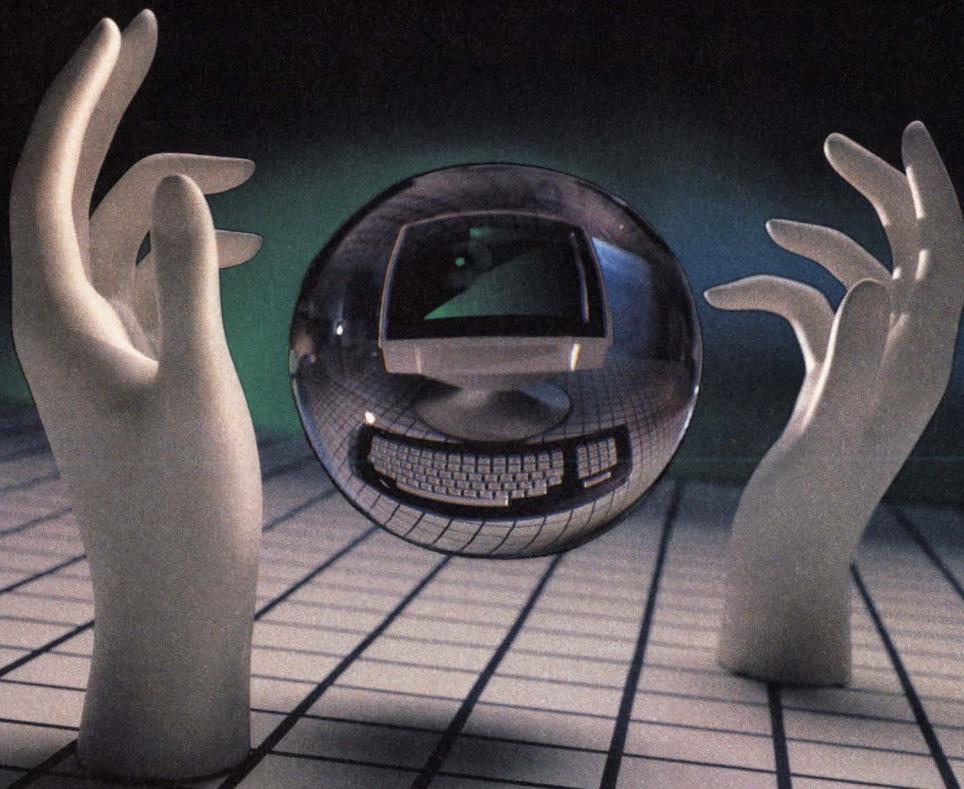
display resolutions for longer cinematic sequences.

GEOVIEW's system controller, the Motorola MC68000 processor, can execute the Surface Modeler package or the user's own application software (Figure 2). The UNIX-based system can be programmed in FORTRAN 77 or C languages, and interacts with up to 1.75 Mbytes of RAM; a 156 Mbyte Winchester disk; and a 10 Mbyte cartridge tape drive. The large disk enables the user to store significant amounts of raw and processed data locally in the workstation for quick access.

GEOVIEW has a high-performance display processor which per-

forms all primitive generation and pixel processing. The display processor is based on Lexidata's own proprietary 3700 System Processor. The display processor operates at writing speeds of up to nearly 10 million pixels per second (in block mode). When not writing in blocks, the 3700 writes vectors at 750 ns. per pixel. Vector writing is done at a continuous drawing speed, not just in bursts or during retrace time. These high speeds become critical when displaying complicated contour maps, well log data, wiggle traces, or other graphical data. A variety of operations can be performed, including 2D vectors, 3D shaded polygons, and

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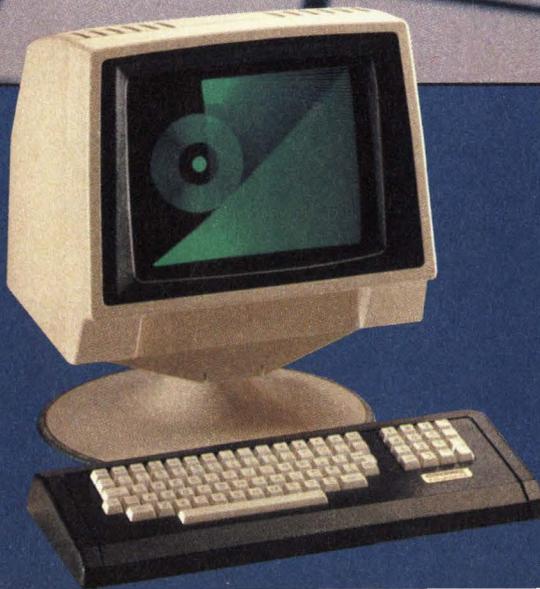
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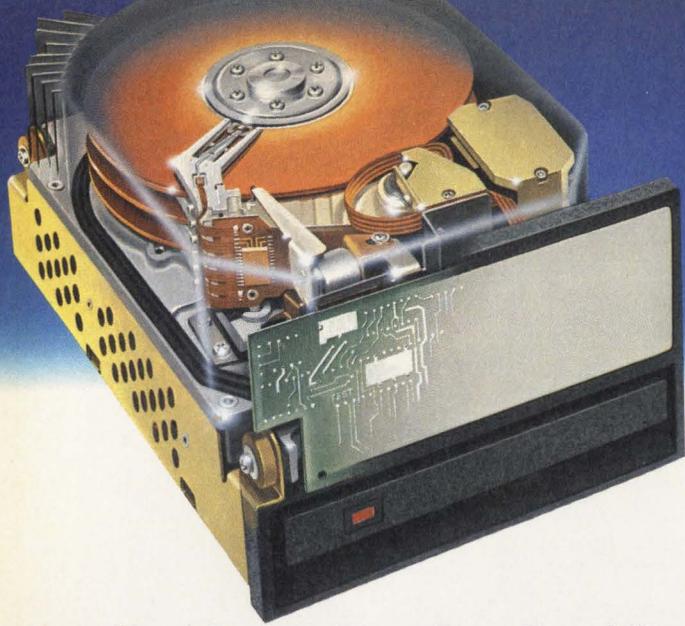
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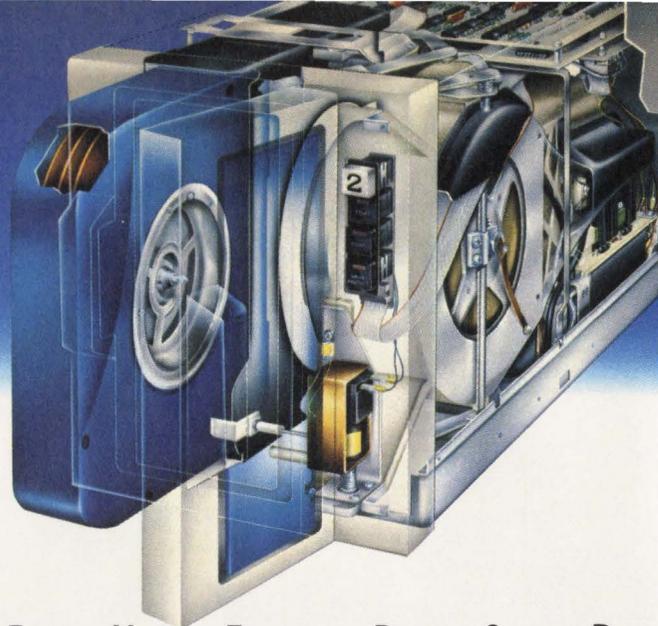
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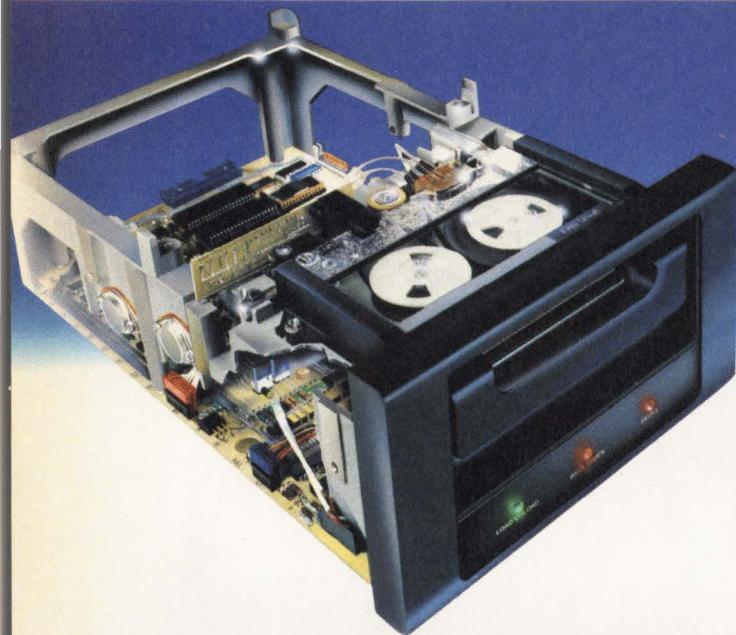
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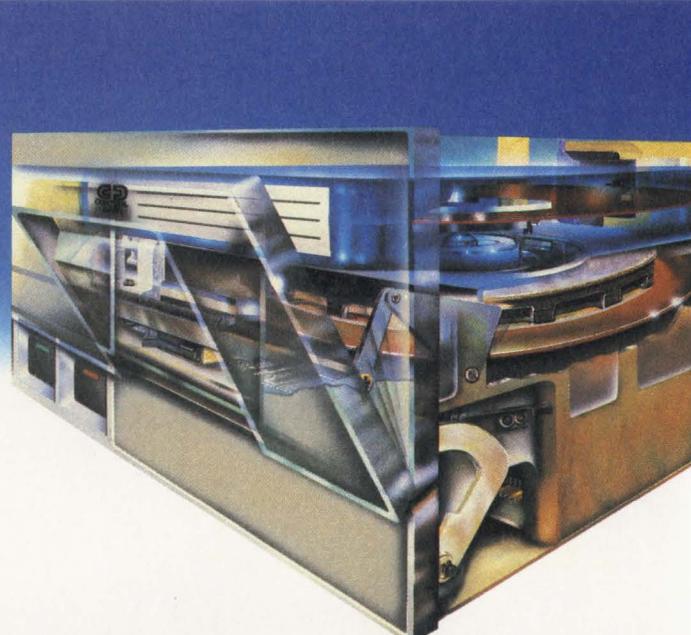
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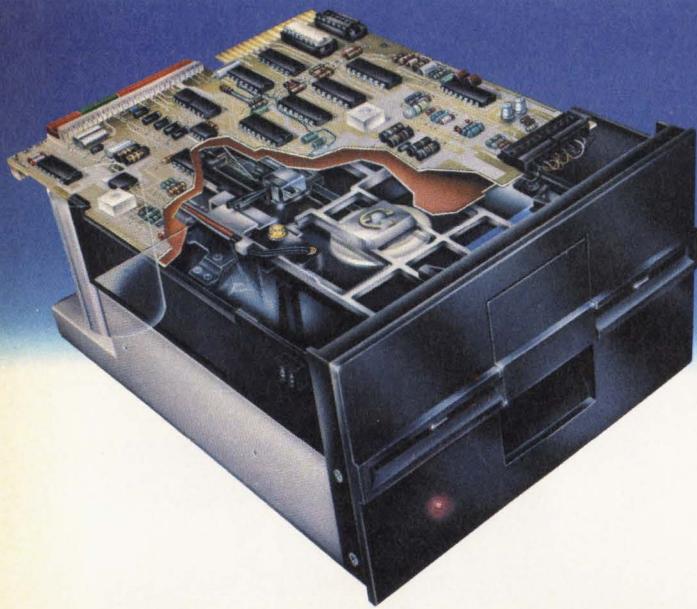
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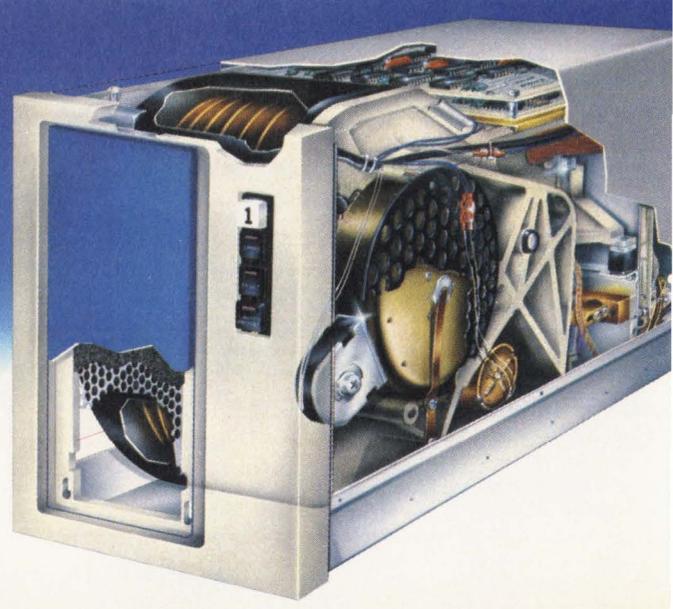
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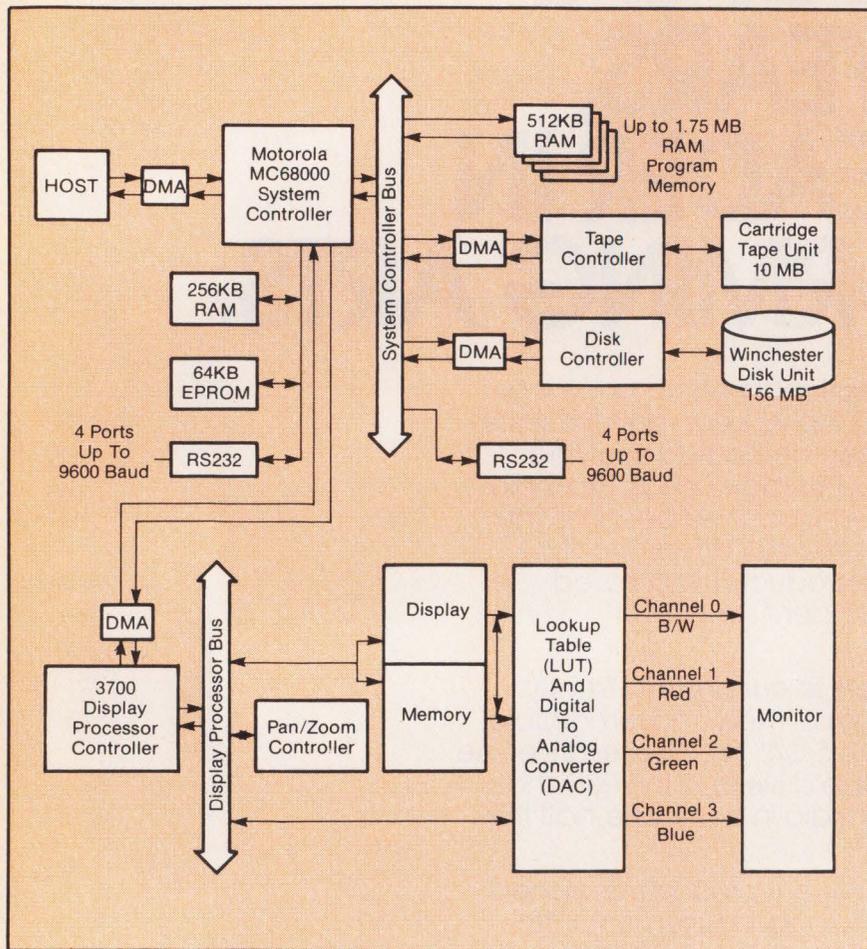


Figure 2: Viewstation functional block diagram.

image processing. A separate memory is provided in the display processor for storing user-defined characters and symbols. The viewstation features a flicker-free raster display with a 640×512 pixel resolution. Up to 5 Mbytes of addressable display memory can be included so that the operator may keep several images in memory.

The imaging and graphics functions are divided into three command libraries: EGOS3, IMAGEVIEW, and SOLIDVIEW. These high-level commands enable GEOVIEW to distribute the processing load evenly over the two available processors for fast response. All functions are performed in the display processor, off-loading the system controller and freeing it to perform other tasks. The user may access any of these commands, even if they are from different libraries. This allows graphics to be combined with imaging, a capability that is critical when tracing and identifying particular horizons on a seismic section.

— Lexidata
Write 232

Color Graphic Board Digitizes TV Images

A new full color digitizer board, the SDD, has been developed by Cromemco, Inc. (Mountain View, CA) which digitizes images from a television camera or other video source. With the SDD interface and a standard television camera, images with up to 754×484 point resolution can be digitized and stored in memory or on disk. Images can then be recalled and displayed on a color monitor.

Varied applications exist for the SDD board including graphics which incorporate color photographs or combinations of photographs, graphics, and data. In industrial or scien-

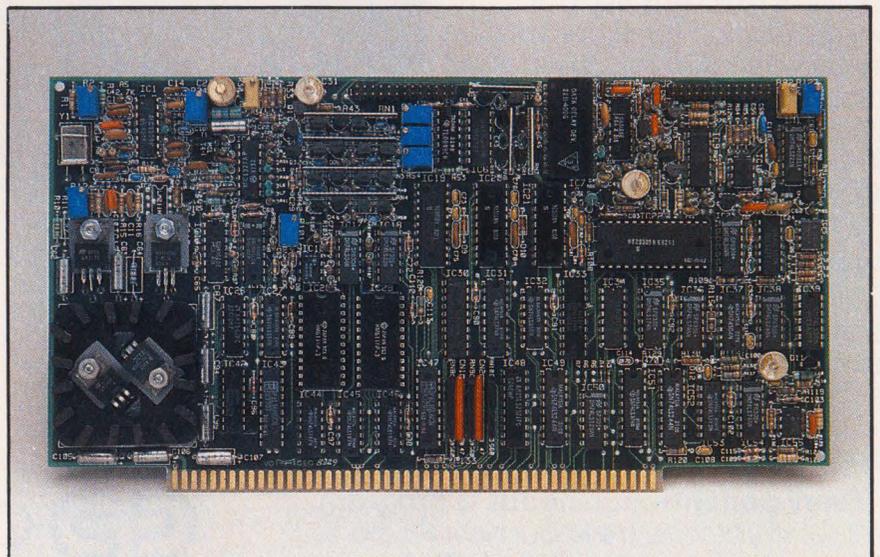


Figure 1: The SDD Digitizer Board.

Figure 2: The SDD Block Diagram.

tific environments, the SDD can be used for automated factory inspection and monitoring systems, and data analysis, including digitized storage of instrument outputs. Image-oriented archives can be developed to implement personnel security systems or image-displaying inventory systems.

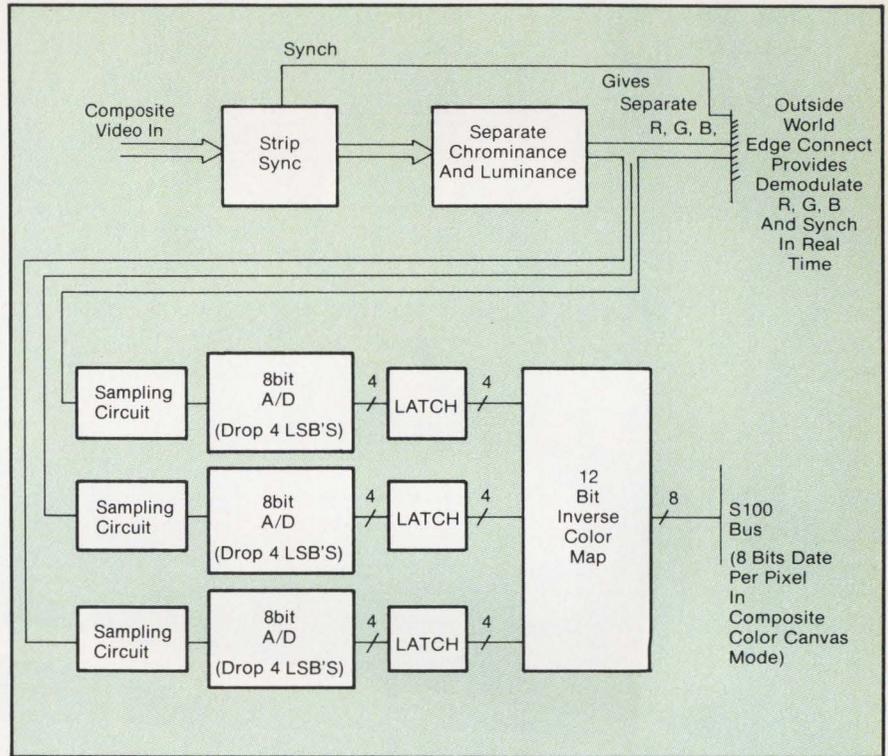
The SDD meets performance demands of image processing environments through generating 8 bits of information for each pixel that is digitized. This translates into 256 shades of grey or 256 colors mapped by the SDD's inverse color map from a palette of 4096 colors.

A digital phase locked loop is used for timing all video sampling and dividing the horizontal line time into 910 pixel locations. This is the same pixel rate as the high resolution mode of Cromemco's Model SDI Color Graphics Interface. Thus 754 samples may be taken during the unblanked line time. With the SDD, 1, 3, 6, or 12 samples may be taken per horizontal image line.

The five different operating modes in the SDD are under software command, for conditions such as grey scale, inverse color mapping, and waveform analysis. The SDD also provides extensive video performance control such as settings for input gain, luminance, chrominance, automatic level control (ALC), flesh-tone compensation and DC restoration level.

The SDD provides real-time demodulation of NTSC composite video into separated RGB. Built-in keying circuitry simplifies the process of mixing the SDD output with other RGB signals. The keyer and demodulator capabilities allow systems based on the SDD to be used in video training or on-the-air studio graphics, where it is desirable to overlay computer graphics on top of real-time video. The SDD is currently priced at \$995.

Write 231



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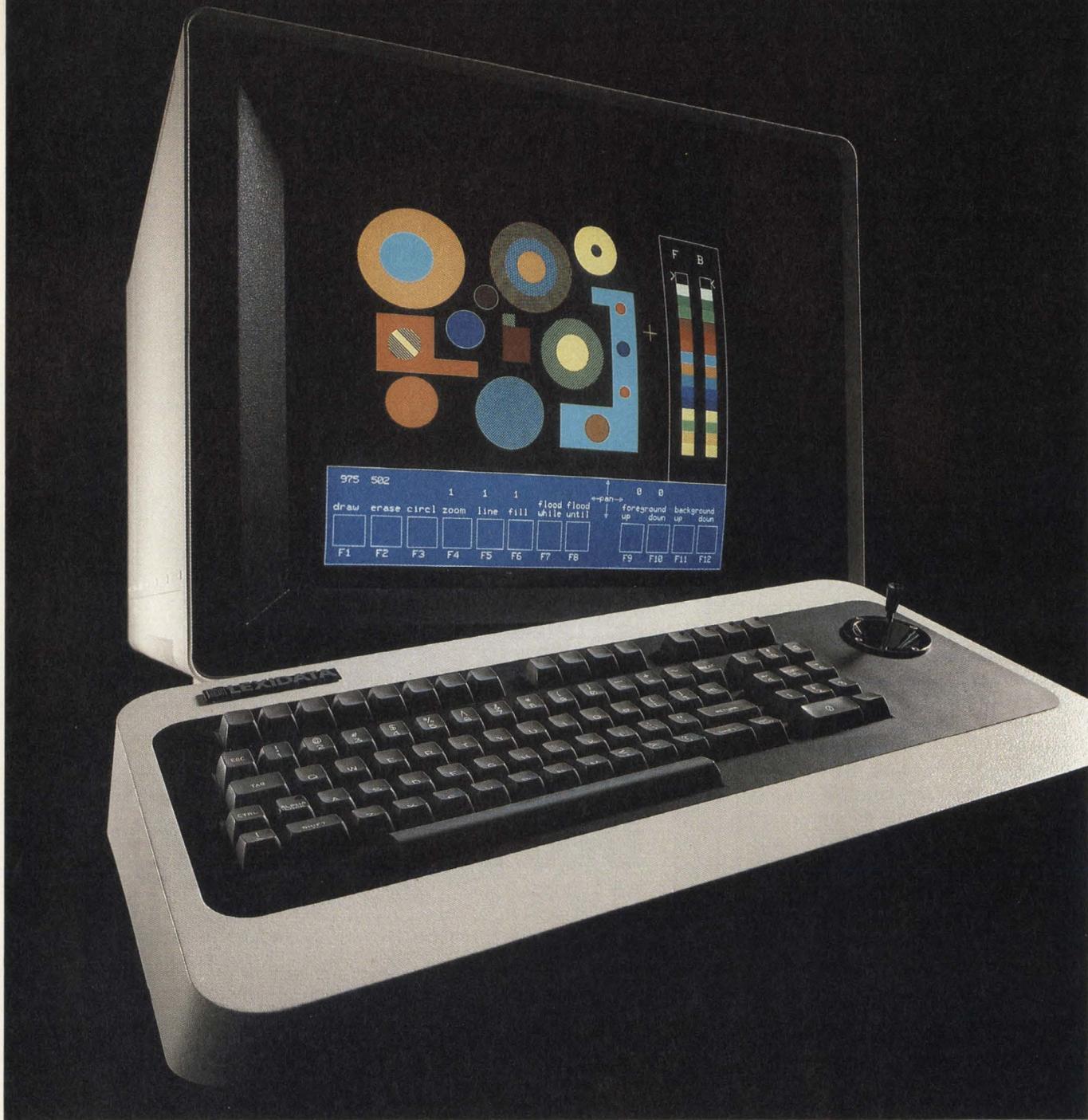
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Industry Review: Graphics Terminals

By Jerry Borrell, Editor-In-Chief

The design and manufacture of graphics terminals has become a primary interest for the computer industry. Users increasingly demand graphics, and new components allow more ingenious methods of providing devices. It is

tacitly recognized that in the near term, the majority of terminals manufactured will have some graphics capability.

Describing the design changes in graphics terminals is difficult because of the great diversity of performance and functionality. For example, in industrial graphics terminals, graphics

Lexidata's 2410 intelligent graphics terminal provides 16 simultaneous colors at 1280 X 1024 resolution. Its firmware allows user-defined application tasks to run on the terminal's 68000 microprocessor.

functionality may be relatively low, however the device may have to be hardened for a harsh environment. Terminals for graphics systems with applications such as flight simulation, on the other hand, may be at the leading edge of performance. Prices range from under \$500.00 to well over

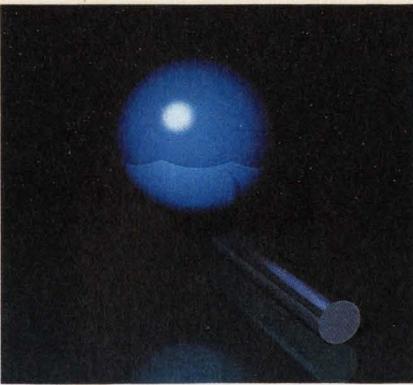


Image produced by Barr-Edward's Ray Tracer, computed on PRIME 500 and displayed on RTI Model 1/20, photographed on Dunn Instruments Model 631.

The designer of a microcomputer system now has options not only in using graphics, but also about performance and price.

\$100,000 in military or Computer Aided Design systems. Terminal, then, becomes a term not dependent upon application or price, rather an indicator that a device may operate under the control or with the assistance of some host computer.

This latter distinction of a terminal has also become less of a clear definition, however, as devices are built that allow operation either as a terminal or as a standalone computer. The distinction remains for graphics terminals, because even those with very powerful architectures are infrequently used for generalized computing tasks. However, as 8 and 16 bit graphics terminals are replaced with 32 bit architectures, more consideration is given to allowing the user to access the computer for tasks other than graphics.

An issue somewhat related is that the distinction between hardware and software is becoming vague as well. Particularly in the field of graphics, where fast processing of both algorithms and data is crucial, there are special advantages in microcoding operating procedures into the system. With each new generation of graphics terminals, more of what we formerly knew as software is loaded into ROM and EEPROM devices, and the trend towards downloading instruction sets into RAM is also on the increase. Thus, many tasks formerly handled by a host system are now carried out locally.

Finally, many designers must be able to provide graphics capabilities in applications traditionally served by minicomputer supported terminals. Today, 16 bit, 32 bit and custom processors for small systems are often able to compete effectively with minicomputer levels of performance. The price of today's processors means that they

can be implemented in systems formerly served by computers. Newer graphics processors or graphics chip sets increase the impetus of this trend. The designer of a microcomputer system now has options not only in using graphics, but also about performance and prices.

Issues Defining Terminal Design

Three major groups of factors shape the design and manufacture of graphics terminals: hardware, software, and performance requirements. Of those, new hardware and changing demand of users for graphics are most influential. Software plays a less important role, due in part to a lack of standards which causes it to be open to less immediate resolution. While each generation or sub-generation change within microprocessors brings increased performance at decreasing cost to designers, graphics functions remain problematic. Many firms, notably those producing monochrome terminals, minimize cost by requiring a host to supply graphics algorithms via software to general processors such as the Motorola 68000 or the Intel 8086. At higher levels of terminal performance

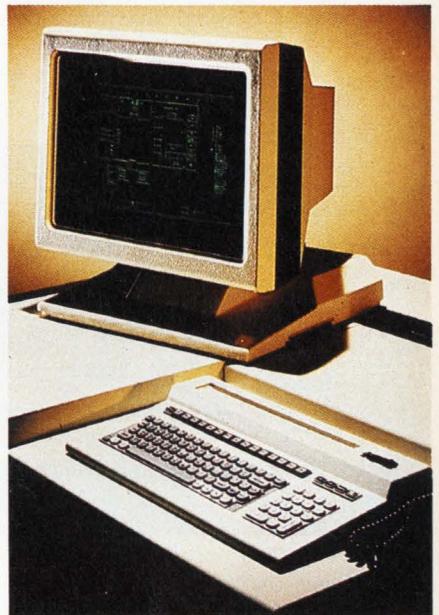
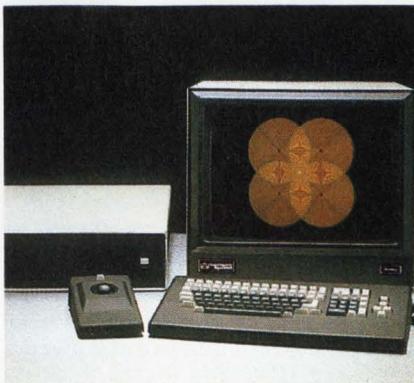
and cost, the manufacturer may utilize more than one processor and additional high speed logic such as bit slice technology to provide floating point calculations.

However, the bulk of new color graphics terminals designed today select a graphics chip, most often the NEC 7220. This device has become so cost-effective that many manufacturers including Genisco (Costa Mesa, CA), Seiko (Mipitas, CA), and Seillac (Tokyo, Japan) can afford to use several of the chips.

Manufacturers at both extremes of the cost performance spectrum have created custom chip sets. There are also more "chip sets" becoming available, as well as supplementary logic devices such as digital to analog converters and CRT controller chips. Those favoring the full custom graphics chip approach were disappointed by the decision of Silicon Graphics (Moun-

The S6100 from Lundy in monochrome or color is said to be the first terminal with full GKS capability.

Intelligent Systems' Intercolor VHR-19 Color Graphics Terminal at 1024² is one of the lowest priced high resolution terminals available.



tain View, CA) to maintain proprietary control of the "geometry engine" developed by the founder, Jim Clark. There was good news during the past year as Weitek (San Jose, CA) made available first its "tiling engine" board set and more recently, a combination of its tiling engine and floating point chip set as "graphics engine". These are solutions for real time or very high performance cost terminal applications.

Performance— One of the principal shaping factors for performance has been the recent reemphasis of traditional graphics markets in computer aided design, process control, SCADA, and simulation applications. The rapid growth of small computer systems such as the IBM PC has significantly changed perceptions regarding business graphics, once thought to be a large portion of potential graphics terminals sales. Much of this market is now thought a good target for small business and personal computers due to its relatively unsophisticated graphics demands.

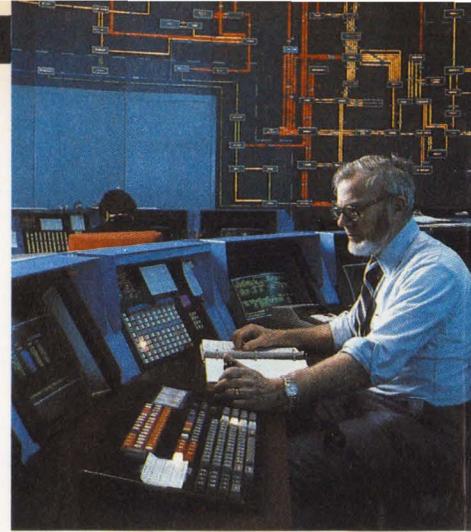
Within the traditional CAD and industrial markets, the demand is for two ends of the performance range. While recent trends for CAD have demonstrated a steadily growing demand for color and interactivity, industry needs less color and interaction, but has specialized performance requirements such as ruggedization, reliability, and long terminal life. While the latter market can be seen as having a relatively stable growth over the long term, the higher performance marketplace shows a marked increase, espe-

cially in light of the use of graphic simulations for flight, technical, scientific, cinematic/ video uses, and graphic arts. While these areas do not share common processing needs for display refresh requirements, they show an increasing demand for the number of colors, display resolution, communications, device interaction (cursor control) and software functionality such as windowing.

Within the above markets, manufacturers must choose performance capacity. Staying within the business graphics market can only bring increased competition with the manufacturers of consumer microcomputer systems. Seeking a higher cost market demands either increased performance or specialized instruction sets for narrower applications.

Monochrome graphics terminals have retained a larger market share than might have been expected. Single color graphics are very attractive in large terminal populations in which a central color terminal or a central color output peripheral may serve several graphics users. Monochrome graphics have also received a boost from those producers of generalized workstations such as Apple's Lisa, Sun, Apollo, Symbolics, and Three Rivers.

A common characteristic among these terminals has been the support of windows. In the past, graphics terminals have supported windows primarily to allow the system user to work with some portion of a display, or to provide different views of a display. More recently, "virtual" windows have become popular. This allows the user



Aydin, traditionally in industrial and military markets, has broadened its terminal line to include high performance offerings. The company supplies builders such as Foxboro, which have critical demands for graphics terminals in industry.

to perform not only separate viewing, but several simultaneous processing tasks. This should not be confused with so called "screen memory" demands in which a terminal may store more than a single page or screen of data for faster local viewing or processing. The latter retains its importance in many uses including animation and programming.

Software Issues— All of these underlie software constraints that are becoming more closely bound with hardware. The most problematic factor for terminal designers may be the need to provide standard operating characteristics for a device. In the past, this has caused manufacturers to build terminals to meet the needs of a system compatible market; Tektronix and Digital Equipment Corporation have been the most important examples. These designs are based upon the need for common instruction sets to direct the electron gun in rendering displays, and because the software is limited to the display constraints (such as resolution) of any specific device and techniques for encoding drawing instructions.

Two recent efforts have ameliorated some of these problems. First of all the virtual device interface, a standard being promoted within ANSI by manufacturers and software developers, would insure common instruction sets to allow terminals to be used with any type of host and the converse. A second important area of growth is that supported by Digital Research (Pacific Grove, CA) in providing a



Once the supplier of component graphics, Matrox Electronics has grown to a full terminal manufacturer. The company supports open systems architectures to give users a wide selection of capabilities.

common set of programming tools under certain of its operating systems that would allow a programmer to develop instructions for several types of terminals with knowledge of common program macros to invoke common graphic functions.

Other important standards, GKS, the European-developed graphic Kernel System, which has recently become a draft ANSI standard and the older SIGGRAPH Core standard provide for common types of functionality on the level of software interaction and system use. There are said to be custom graphic chips under development that will incorporate the functionality of these standards, but they remain beyond the reach of system designers today.

Finally, the manufacturer must decide what amount of software will be programmed into the device as firmware. For higher levels of performance, the designer must be able to use RAM and ROM memory for display list functionality. Megatek (San Diego, CA), Genisco, Ramtek (Santa Clara, CA), Lundy (Glen Head, NY), and Evans and Sutherland (Salt Lake City, UT), for example, do this. Aydin (Fort Washington, PA), Lexidata (Billerica, MA), and Raster (North Billerica, MA) also provide firmware functionality as speed/performance enhancements.

Response to Design Issues

As might be expected, there is a broad range of design solutions to meet these needs. While there is certainly a growing demand for color, the monochrome manufacturers such as Qume (San Jose, CA), Modgraph (Waltham, MA), Telvideo (Sunnyvale, CA), CIE (Irvine, CA), Liberty (San Francisco, CA), Datatype (Mountain View, CA), Visual (Tewksbury, MA) and Digital Engineering (Sacramento, CA) have wide acceptance. Typically, these terminals may provide preview capability for graphics or be used in combination with graphics hardcopy devices. There are also many scientific and technical applications, in which Tektronix systems have been traditionally used, in which monochrome is preferred over color. While some market research firms indicate that this market is diminishing, the number of suppliers is growing. The trend, however, demonstrated by MODGRAPH, is for these same manufacturers to also incorporate color



Megatek, producer of high performance graphics terminal systems, has moved to broaden its product line for low to high cost within the interactive marketplace.

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capability in newer product lines.

In the lower price/performance range of color graphics terminals, manufacturers have to offer resolution in the range of 640x480 while keeping the price below about \$6000. The trade-off here is to limit the number of colors displayable and the number of colors within the color selection to eight or 16. Design efforts have a common theme: the addition of capabilities such as polygon fill, macro instruction sets and local pan or zoom operations, with internal processing. At even lower prices, under \$2000, functionality becomes much more limited, but even these manufacturers, such as Intelligent Systems Corporation (Norcross, GA), are adding functionality in a race to supplant the producers of more expensive devices.

There are several primary areas in which design competition is taking place across all ranges of performance and cost. One of the most evident is that of increasing intelligence.

Processors— Considering only those manufacturers who wish to continue supplying host supported devices, and not those with dual terminal/stand-alone microcomputer capabilities in mind, one can pick out three main efforts: those in the Intel 8086 family, those making use of discrete TTL, ECL, or full custom logic, and those using the Motorola 6800 family or its

predecessors. Not surprisingly, at the highest ranges of performance, designers use bit slice architectures. The one exception to all of this is the group of manufacturers who have retained the Z-80A - Z8000 family of processors; but increasingly such devices are shown in terminals which also incorporate other processors: Matrox (Quebec, Canada), Intelligent Systems Corporation, and Seiko, are examples.

Graphics Chips— To support graphics functions, most manufacturers are either using software for graphics on a generalized processor or implementing a chip or chip set designed with graphics as their primary function. For 1983 the outstanding chip of choice was the NEC 7220. Manufacturers make use of multiple NEC chips including: Seiko, The Nippon Computer Company (Tokyo, Japan), and Genisco. Manufacturers of monochrome terminals are also beginning to embrace the device, and Zentec (Santa Clara, CA) and Televideo have made use of a single 7220 for basic graphics function. A very select group of manufacturers have begun to use PLA/PAL logic, or in some cases gate arrays, for high speed graphics operations: Megatek, Ramtek, Genisco, Seillac, Lexidata, and Raster Technologies are representative here.

Emulation— The emulation of other manufacturers' terminals remains the

mid and low range criterion of acceptability for most manufacturers. The list of Tektronix compatible manufacturers: Genisco, Lundy, Matrox, Digital Equipment, Intelligent Systems Corp., Seiko, ID Systems (Hilliard, OH), Tab (Palo Alto, CA), psiTech, Lear Siegler (Anaheim, CA), and CIE Terminals, is evidence of the large influence Tektronix has had and continues to exhibit in the marketplace for terminals. While the majority of the systems are 4010 series emulators, others match each new generation such as 4014 and 4027, with similar functionality. This emulation has established a de facto terminal standard interface and offers terminal users competitive purchase advantages in the large market for graphics display devices. No manufacturer is alone in this, witnessed by Qume's ability to successfully produce Televideo compatible terminals at a competitive price.

Firmware— The use of microcoded instructions to increase capability in the terminal has become the arena for competition in functionality. The ability to make one's terminal a Tektronix emulator is a typical example at the systems level. There are three other areas of firmware development that determine a terminal's functionality: graphics, text and fonts, and window/screen commands. Graphics instructions begin with the ability to generate geometric primitives locally (lines, arcs, circles) and extend to functionality such as incorporating the algorithms used to fill polygons or to allow new instruction sets to be downloaded. At higher cost, the terminal may incorporate the instruction sets of the ISO draft standard GKS or the long used SIGGRAPH CORE standard. Again, there is a small group of manufacturers that incorporate the highest levels of functionality. In this case, their terminals have display lists of graphics functions that are entire graphics subroutines that allow for premium levels of operation.

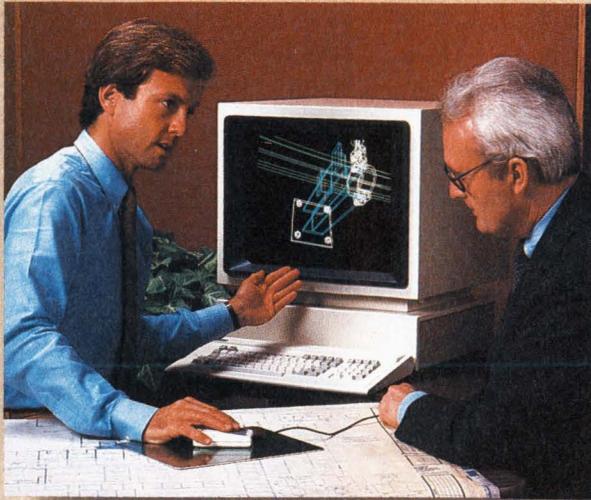
The text and font firmware are less glamorous but offer crucial features at lower cost ranges. These capabilities begin with the ability of a terminal to offer more than one text font, double high characters and to attribute functions for the font such as blinking, blanking or protected fields.

Finally, there are the all-important



Verticom's NAPLPS videotex screen creation/editing, color graphics terminal is the first terminal widely available in the US to bridge the graphics/videotex market.

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The Florida Computer Graphics Beacon terminal line was one of the first to incorporate both 16/32 bit processors and second generation bit slice devices.

functions relating to windowing and screen interaction. Windows have become the rage in terminal design, but it remains to be seen whether the approach will significantly enhance user operation of a device. The near term effect is no doubt going to be that windows, like increasing resolution, will become one of the factors that the market will demand of a device.

The more basic operations of screen interaction for graphics operations include positioning or picking functions in 2D and 3D operations, such as scaling, rotation, rubber-banding, dragging, clipping, and pan/zoom. As in the case of all other functions, the most capability is found in higher priced and performance terminals. However, even office applications for graphics terminals are becoming more sophisticated, as witnessed by the monochrome revolution in windowed terminals begun by Xerox and developed most successfully by Apollo Computers. Apollo, of course, crosses the lines today at all applications levels for both monochrome and color, setting standards of graphics interaction expectations.

The Big Two—The two design criterion that have remained at the top of the graphics forum for the longest and tend to provide the broad classifications within which some users select a terminal are color and resolution. While the number of colors and screen resolution have simple conversion factors for the designer in terms of cost, amount of memory required, and the hardware required (monitor), the conversion into performance for any given number of colors and resolution is not so straightforward. The classic example is that increasing resolution from 512 squared to 1024 squared demands the processing of four times the amount of

data. Memory and processing further increase with each bit of memory required by the use of a color or grey scale. As the amount of data grows, however, related problems do not merely demand greater amounts processing, but are expressed in the inability to transfer data across RAM or hard disk interfaces designed for serial processing. Other requirements such as bandwidth, monitor and drive electronics, and floating point math also make "clean" designs an arduous process.

In determining resolution, the manufacturer/designer has to know the intended market/application and the price range that the manager intends because, while techniques such as the logical display area or color look up tables that may be used to lower cost, some applications will not be amenable to these. The logical display area allows the terminal manufacturer to hold additional display available for users. At low cost/performance, this is developed as additional pages of screen memory. For high performance devices, this is implemented as a viewable display into a larger memory of 1024 squared or more. Color look up tables similarly allow the developer to minimize the amount of RAM used by setting aside a portion of the bit plane of memory for interpolations to numeric values that are assigned as chroma, hue, or value. In this case, more colors are assigned at the cost of the processing time required for the interpolations.

Broad categories of resolution are recognizable, with consumer or small business computers retaining the lowest levels of under 500 squared. However systems for several business applications overlap with the low end of industrial and design systems, at 640 by 480 to 1024 squared. At 1024 squared and above, performance rates tend to increase dramatically, yet systems are widely available under \$20,000 and some anomalies, such as the Intelligent Systems Corporation terminal for under \$4000, show that the trend is to decreasing cost even at this level. Both terminal manufacturers like Lundy and Seillac and monitor producers are pushing for higher levels of resolution, but both are limited by physical aspects of monitor design and by the need to increase the sophistication of logic and control electronics within the terminal itself.

As for color, the demand for more is the driving theme for designers; however, manufacturers directed at specific markets such as Process Control, SCADA, and Command and Control such as Aydin and Intelligent Systems Corporation have great success with eight to 16 colors because of the well-defined needs of their markets. Consumer and business applications have similar bounds for many manufacturers at present, but the demand for a greater selection is pushing these performance levels.

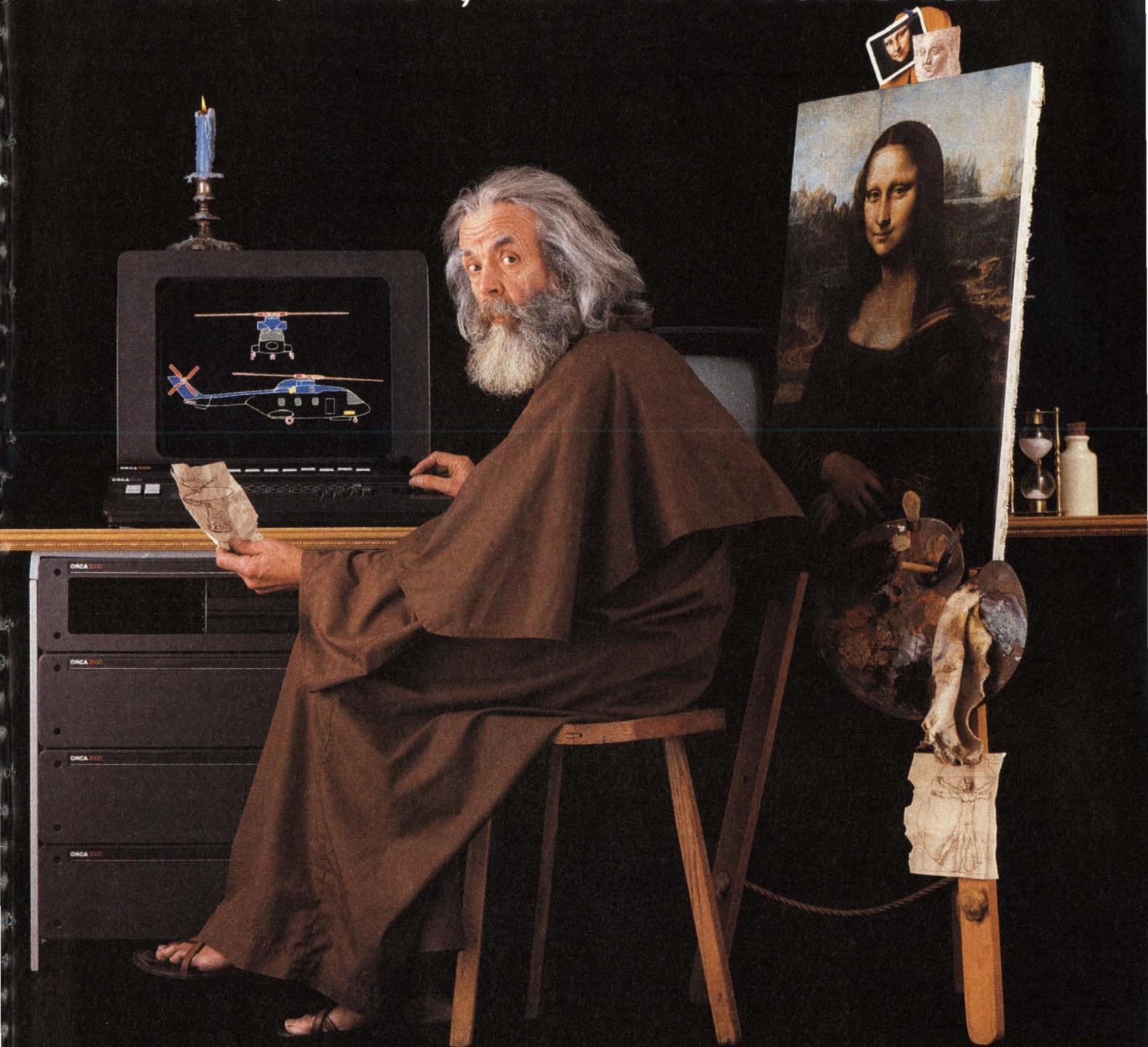
Communications—Communications is one of the growing design considerations for terminal manufacturers because the basis of terminal implementation is, after all, in host-supported environments. For most terminals in non-graphics use, the RS-232 data channel has been sufficient, with multi-ports common. However, in graphics environments, the RS-422 port with its better defined standards and higher data rates is becoming important, especially in light of local area networking. The GPIB, formerly IEEE-488 channel, is important, as is the 8 bit parallel Centronics port. The newest entry is fiber optics links, such as those supported by Artel Communications for graphics links. Seillac terminals are provided with a fiber link for their high bandwidth color-rendered images. For the present, and for low to medium performance communications uses of terminals, the RS-232 with up to 19.2 kilobaud is the most often used.

Specialized Terminal Designs

Beyond the generalized design environments in which the cost/price/performance trade-offs are the guiding principles, there are several markets that require special design consideration. Among these are the military, industrial, IBM, and retrofit markets.

Military—The market for Military Specification terminals is perhaps best represented by manufacturers such as Aydin, Ramtek, and Genisco. Factors such as reliability, tempest hardening, ruggedization, and electromagnetic emission/hardening combine with the extraordinary procurement procedures of the military to make this a highly specialized marketplace which does not correspond to the high levels of performance or lowering costs discussed here.

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Industrial — A related application is that of industrial or harsh environment uses, where terminals must be able to withstand extreme temperatures, vibration, chemicals, and long hours of use. The products of Industrial Data Terminals (Westerville, OH) and Interstate Electronics Corp. (Anaheim, CA) for example, are designed for this market. Reliability in applications such as nuclear or fossil fuel plant monitoring, becomes as important as in military use, and the designer must be aware of long life, power consumption, and distance from a central computer in structuring the plan for a terminal line. Issues such as phosphor capability for displays that remain static over long periods become important, rather than issues of speed of refresh or processing.

Retrofit — One of the specialized areas of terminal design is that of modification for standard ASCII terminals. The ability to retrofit older alphanumeric terminals for graphic capability as predicted to decline long ago, yet new product lines continue to be introduced. One interesting change has been the introduction of products such as those of Digital Engineering which not merely retrofit graphics, but Tektronix 4010/4014 emulation. CIE Terminals has entered the market with not only graphics retrofit cards for its own products but with cards giving Tektronix, ISSCO (San Diego, CA), and DEC capability. The older manufacturers of retrofit capability, Selenar (Sacramento, CA), Datatype, and others who have produced cards aimed at the DEC VT-100 market may do the same, and show continuing strength in their existing markets.

IBM Compatibility — It is perhaps early to measure the results of manufacturers response to IBM's 5081 color terminal. A separate article will evalu-

ate this later in 1984. Most manufacturers had built IBM color compatible terminals for the older 3250 compatible use, but the programs for the 3250 do not transfer readily onto the 5081 which is said to be at a performance level higher than all but the 1500 range products from Spectragraphics and the new CGX product. It is to the credit of all these manufacturers that they have developed additional products during the wait for the release of the color IBM product. The IBM terminal offers performance advantages of the high end Megatek, Spectragraphics, Ramtek, Adage terminals at a lower cost, but is tied to the higher cost processing environment of IBM mainframes.

Videotex — A long awaited entry in graphics terminals came this year from Verticom (Sunnyvale, CA), which has produced the first US graphics terminal that is compatible with the North American Presentation Level Protocol (NAPLPS) for videotex applications. The NAPLPS draft standard is the first and strongest proposed standard for the communication of text and graphics. The Verticom terminal has bridged several markets by also allowing for Tektronix and DEC compatibility.

Summary

The most obvious trend for manufacturers has been to offer a broad range of performance and cost devices. Apollo, Megatek, Ramtek, Lundy, Seiko, Adage, and Orcatech (Ottawa, Canada) remain within the high performance end while CIE Terminals, PsiTech and Intelligent systems seek a similarly broad range within the lower performance range. At the higher end it is probably unfair to merely classify these systems as terminals, rather they should be called display systems, for

despite their being host dependent, they may have open systems architectures such as Multibus or VME bus and provide expansion capability.

The traditional distinctions between the "high performance" system builders are eroding, as the medium and low range producers implement newer generations of processors, graphics chips, or make the investment of incorporating firmware for graphics functions that makes their end products less distinguishable from much higher cost systems. The high performance producers respond by addressing the developing marketplace for new applications requiring picture refresh rates, color or rendering times formerly found only in military or image processing systems. Comtal (Altadena, CA) notes the decreasing distinction between the image processing and computer graphics markets for systems, and incorporates more general graphics functions into its highly specialized terminals.

The most potent change for the graphics terminal market will probably come during the next 12 to 24 months as new graphics chips and chip sets become available to terminal manufacturers and are incorporated into terminal products. These new products will insure that the small computer systems being designed will incorporate more graphics capabilities creating even larger demand for distributed uses of graphics as the user population becomes educated to its use. □

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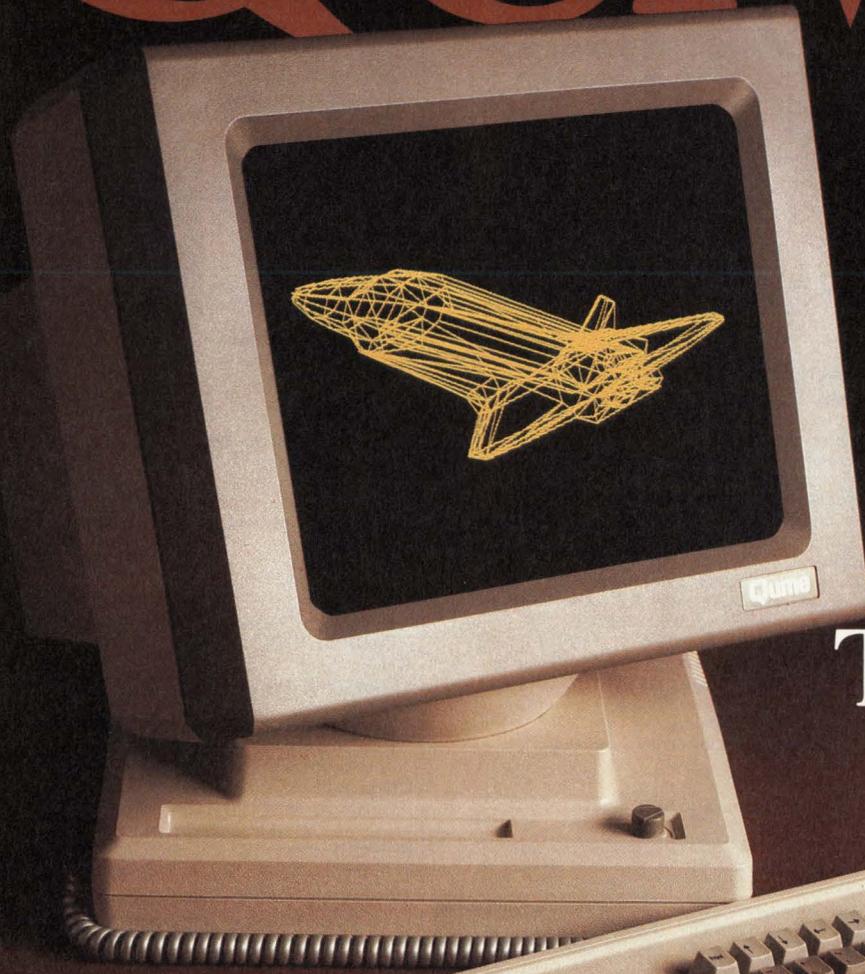
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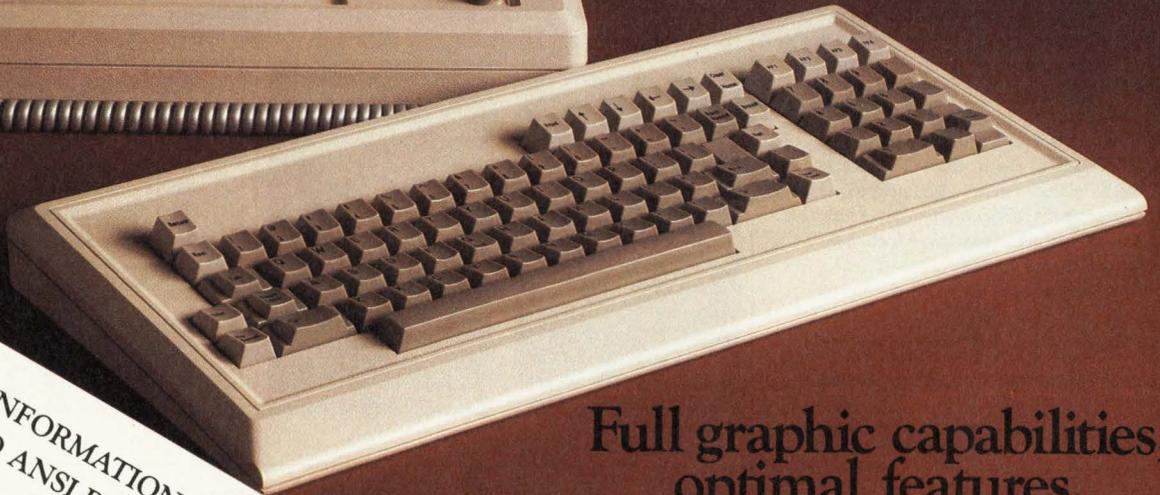
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Now you can get all of the features and ergonomic design of the high performance QVT 102™ — plus full graphics capabilities!

The QVT 211 GX features a 14-inch green display as standard (amber optional). The completely independent graphics memory can be displayed simultaneously with the alphanumeric memory.

The QVT 211 GX is compatible with the Tektronix™ 4010* and 4014* command sets, which makes it ideal as a preview terminal for CAD/CAM and Tektronix PLOT-10 applications. Also, in its native graphics mode, microprocessor-based vector generation greatly simplifies programming. Specify the endpoints and the QVT 211 GX creates the line! Arcs, circles, boxes, and fill can be quickly generated with single commands. These powerful features bring a full spectrum of business graphics within the reach of micro and mini-computer users. Image size and location, as well as additional features—such as variable display windows, relocatable origin and area fill—are easily programmed by the user.

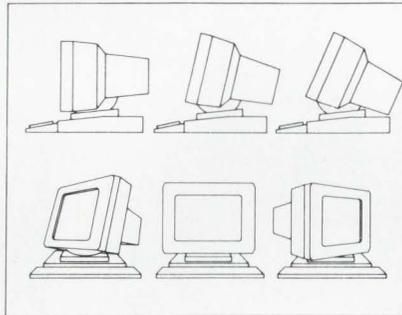
In the Qume tradition, the QVT 211 GX delivers a powerful array of graphics capabilities, at a cost well within reach.

Graphics Features

- Full, interactive vector graphics
- Separate display memory for graphics
- Switchable video
- Absolute and relative addressing
- Variable gain and relocatable origin
- Draws lines, boxes, and arcs (including circles)
- Area fill
- Selectable power-up option
- Graphics memory dump to host
- Cross hair cursor
- **Native Command Mode**
- Large addressable area (65Kx65K)
- Addressable screen area 2500x2000
- Vector generated line, box, arc and circle
- Area fill
- Relocatable origin
- Variable gain
- **Tektronix Emulation Mode**
- 4010 and 4014 software compatibility—PLOT-10
- Addressable plot area 4096x4096
- Vector variation (dot, dash, and lines)
- Incremental plot
- Write through plot
- Resolution 644x288.

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Alphanumeric Features

Display Format

24 lines x 80 characters

25th status/set-up line

Character Formation

7 x 9 matrix in a 9 x 12 cell

Displayed Character Set

96 ASCII characters, 15 line-drawing symbols, and

32 control character symbols

Editing

Cursor: up, down, left, right, and home. Character/line insert and delete, erase to end of line/field/page, tab, back tab, field tab, field back tab.

Communications Interface

EIA RS232-C with optional 20 mA current loop

Communication Protocols

DTR and/or X-ON/X-OFF

Communication Modes

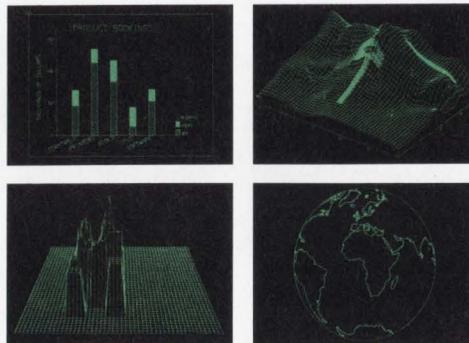
Full or half duplex, block/line, block/page; 7 or 8 data bits

Baud Rates

16 selections from 50 to 19.2K

Auxiliary Port

Bidirectional EIA RS232-C, partial/full screen copy, transparent print.



Screen

Tilt/swivel 14-inch diagonal standard non-glare green (optional non-glare amber)

Character Attributes

Blink, blank, normal video, reverse video, underline, half intensity

Keyboard

Detached, adjustable-tilt, low-profile (home row 30mm from work surface), alphanumeric keys, 14-key numeric pad, 12 function keys (8 user programmable), defeatable autorepeat and key click. Print, setup, and no-scroll keys.

Fields

Protected and unprotected fields

Parity

Odd, even, mark, space

Screen-saver

Screen shut off after 15 minutes of inactivity with no data loss

Emulations

Hazeltine 1500, Lear Siegler ADM-3A/5, TeleVideo 910

Set-Up Mode

Menu style, preserved in non-volatile memory

Power Requirements

95-125 VAC
200-264 VAC
50/60 Hz, 40 W

Dimensions

Keyboard 1.5"(H) X 18"(W) X 8"(D)
Display 14"(H) X 13"(W) X 12"(D)

Weight

Display 20 lbs, keyboard 3 lbs

Options

Amber phosphor screen
Foreign character sets
20 mA current loop (passive or active)

Character Sets

USASCII and APL

Software

A library of PLOT-10 compatible subroutines which speeds the development of graphics applications programs is available from Tektronix Corporation. The library is available under RT-11, RSK-11M, and VMS. The subroutines are written in FORTRAN, but any higher level language which supports a FORTRAN-style call can be linked to the package. Business graphics package for personal computers is available from Digital Research.**

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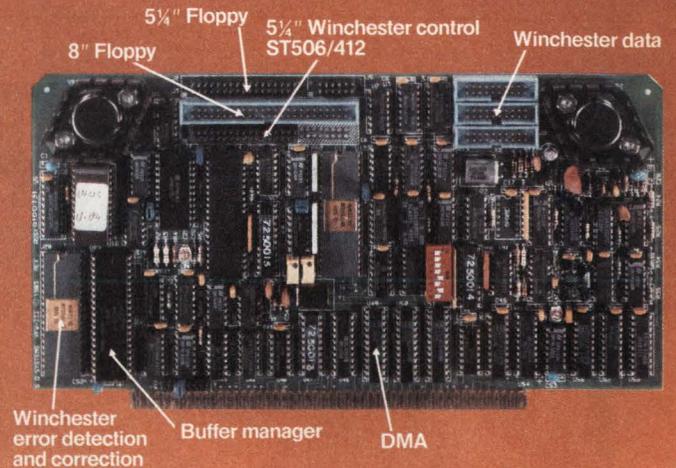
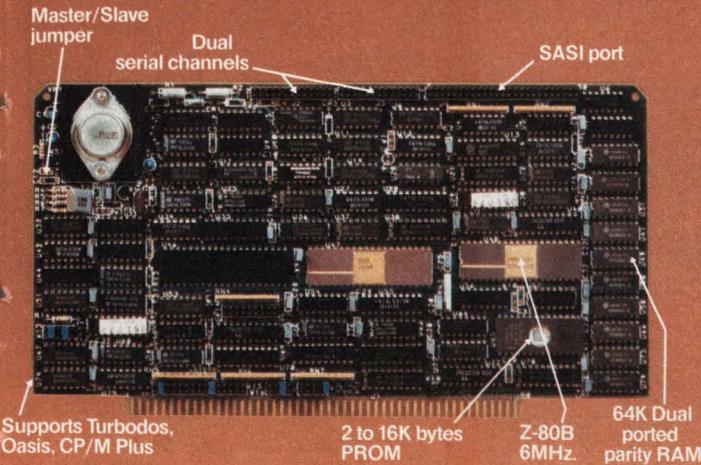
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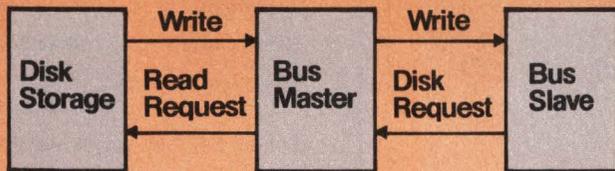
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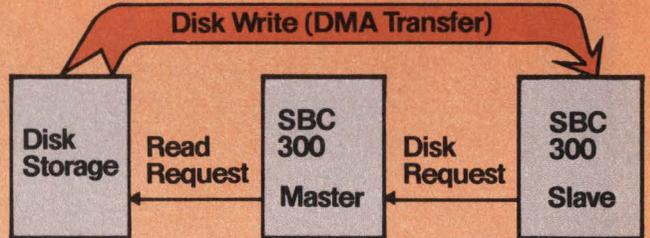


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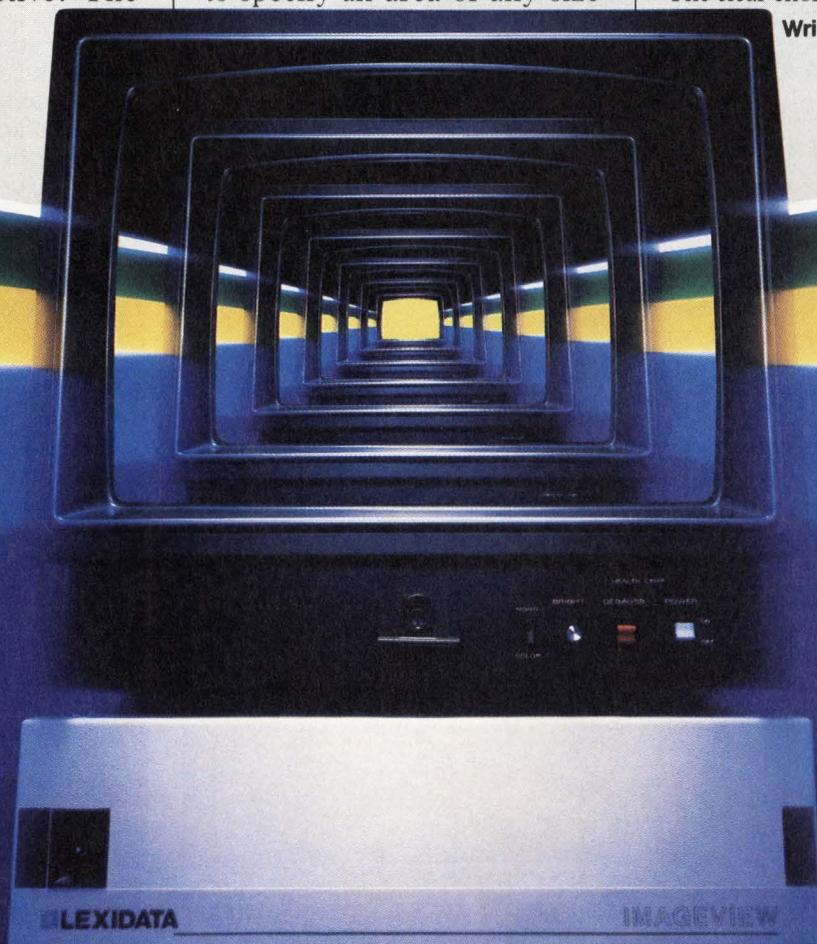
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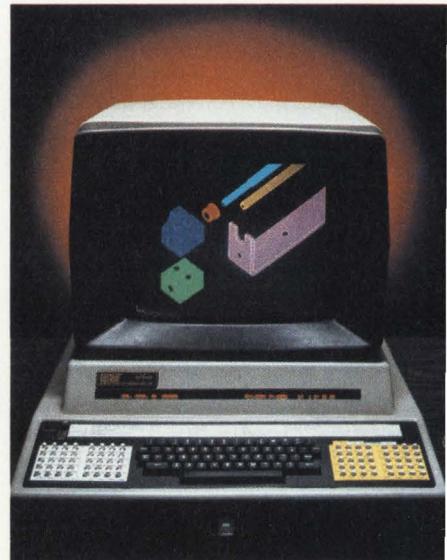
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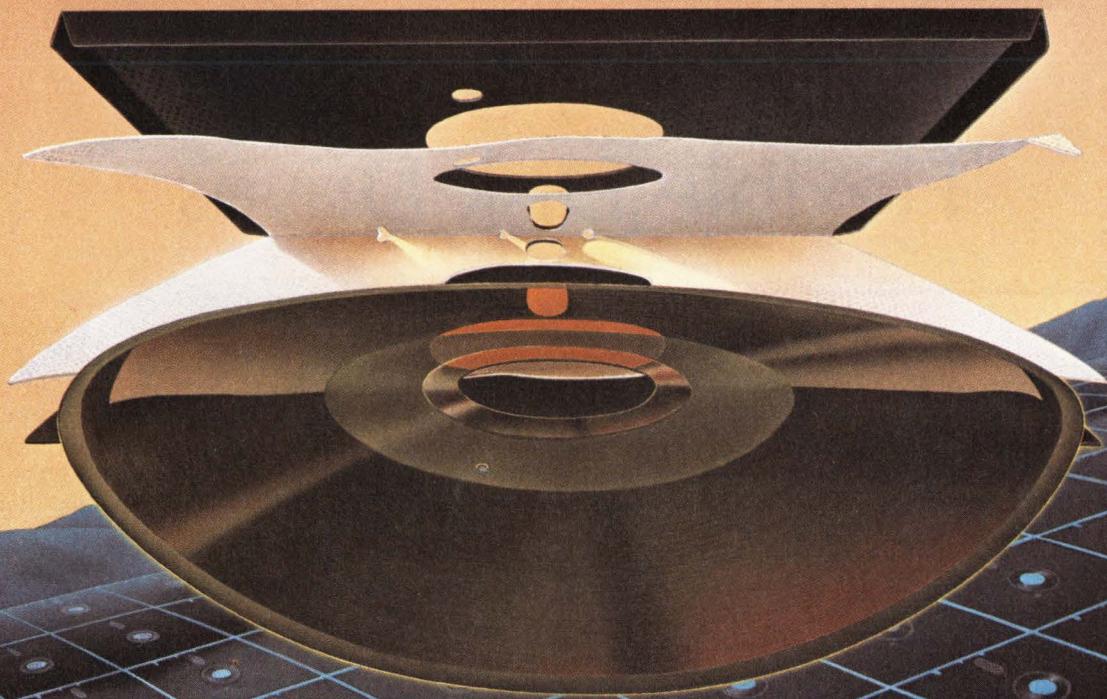
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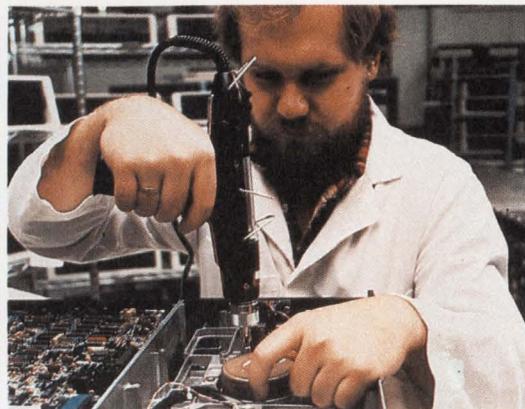
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Designer's Guide Series



FLEXIBLE DISK DRIVES

(Cover photo courtesy Memorex)

Designer's Guide To Flexible Disk Drives

Floppy drive manufacturers report that rumors of their demise are greatly exaggerated.

by **Bob Hirshon, Contributing Editor**

Looking back over the fourteen-year history of the flexible disk drive is like reading one long obituary. Almost from its birth, detractors have predicted the imminent demise of the technology. Alternative technologies, such as bubble memories and removable Winchester, were predicted to replace floppies in most applications, relegating flexible disk drives to a few specialized, low-capacity applications. Even today, one removable Winchester manufacturer runs ads suggesting several suitable applications for flexible disk drives. According to the ad, "obsolete" floppy drives make great book-ends, planters, and targets for rifle practice.

Despite the pot-shots, however, it is the alternative technologies that remain limited to narrow, specialized applications, while floppy disk drives have maintained their popularity. When they were first introduced by IBM in 1970, floppy

drives were intended as program loaders. But coincident with the introduction of the floppies was the introduction of the desk-top computer. For small computers, hard disk drives were then too big and expensive, and tape drives were too slow. Floppies instantly found a home as on-line mass memory devices for small computers. Since then, advances both in flexible media and drives have kept pace with advances in small computer systems, and floppies have prospered.

Boosting Performance

Keeping pace with the demands of small computer systems users hasn't been easy, however. Typically, these systems start with floppy disk drives and upgrade to fixed hard disk drives with a floppy drive as back up to the hard disk as user requirements increase.

When used as back-up devices, flexible disk drives require a capacity of at least one-tenth the capacity of the drive they are backing up (one-third is optimal). Otherwise, swapping floppy diskettes becomes too much of a chore. For a 5-Mbyte rigid disk drive, then, .5- 1.0- Mbyte minifloppy drives are adequate. But the latest generation of high capacity Winchester, packing from 10 to 40 Mbytes (and, in some cases, over a 100 Mbytes) requires back up drives with proportionately higher capacities. To address this market, and also the increasing demands of users who rely on floppy drives for on-line memory, flexible drive and media manufacturers have had to match Winchester manufacturers' capacity gains.

But boosting capacity in flexible disk drives is more difficult than increasing capacity in Winchester, for two main reasons. First, environmental pressures for removable media such as floppy diskettes are far greater than are those of fixed, sealed disks. As data density increases, problems with thermal expansion and contraction of the Mylar substrate also increase, as do contamination and wear problems.

Bob Hirshon is Contributing Editor, Peripherals for Digital Design, and Editor-in-Chief of Memory Update (78 Oldham St., Pembroke, MA 02359), a bi-weekly news journal of memory technology.



Figure 1: High performance flexible disk drives are finally taking hold in the marketplace. Omega, at their manufacturing facility in Ogden, UT (opposite) produce drives with up to 10.5 Mbytes of formatted capacity.

Secondly, flexible disk drives cost less than fixed disk drives. Techniques for increasing capacity that work for Winchester often are not cost effective for floppies.

Despite these difficulties, flexible disk drives have made substantial performance gains, especially over the last year. One reason is the efforts of the media manufacturers to not only improve the flexible media itself, but to help develop new, higher performance technologies.

3M's Keystone

One method of boosting flexible disk drive performance is modifying the diskette media by encasing it in a cartridge, or mounting it on a secondary substrate. This technique has the disadvantage of abandoning one of floppy drives' chief features: standard, interchangeable media. But it also leaves behind a host of problems, such as media contamination and thermal expansion, which can be minimized by innovative media and drive design.

A development effort code-named "Keystone" that uses this approach was unveiled recently by 3M. Targeted at both fixed-disk and removable-disk applications, the technology uses standard flexible disk media stretched over a circular rim, much as a drum skin is stretched over a drum (Figure 2).

Keystone drives use Winchester-type R/W heads that fly over the media surface at approximately 5 μ inches. The media itself spins rapidly, at about 3400 RPM. The pressure of the air-bearing upon which the heads fly causes a dimpling effect on the resilient media immediately under the heads (Figure 3). This dimpling effect, according to 3M, clears away surface contaminants under the R/W heads.

Although the technology is not yet ready for introduction, prototypes using 5.25" media and storing 5 Mbytes of data per side have been demonstrated. These prototypes, says 3M, endured "environmental hazards not normally tolerated by conventional disks."

The first products to use this technology will be fixed disk drives, which 3M hopes to introduce at NCC. Soon thereafter, they plan on developing removable media drives based on the technology. Using servo track positioning, these early products will have track densities of 345 tracks per inch (tpi) in

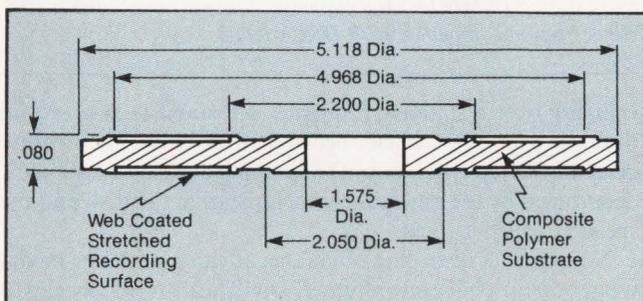


Figure 2: 3M's new Keystone technology, designed for use in either fixed or removable disk drives, uses media consisting of a rigid polymer composite substrate with 10-mil raised rims at the periphery and center hole. Flexible diskette media is then stretched between these rims.

fixed disk models, and 200 tpi in removable disks. Linear densities will be 9795 flux changes per inch (fcpi).

Prototype drives upon which these early products will be based use a polymer composite substrate that serves as a base for a stretched 600-oersted, 60- μ inch thick flexible media substrate. Using particulate oxides, 3M believes it can increase track density to 728 tpi (fixed) and 580 tpi (removable), with linear densities of 20,400 fcpi. This would result in capacities of 48 Mbytes (fixed) and 37 Mbytes (removable).

Beyond that, 3M claims that future generation products using the technology could incorporate thin film media and/or perpendicular recording to attain 728 tpi and 70K fcpi. "We believe we can see 100 Mbytes on a 5.25" disk sometime down the road," says Richard Fleming, marketing manager for the Keystone project.

The stretched media is less susceptible to instability due to environmental changes, and this is one of its key advantages, according to 3M. Media used in current prototypes displays anisotropy of 200 μ inches, which 3M claims is one sixth that of standard diskettes and one third that of the highest density diskettes. In addition, error rates of one soft error in 10^{10} bits compare favorably with rigid oxide or rigid thin-film disks.

For Keystone media to find market acceptance, it will have to be assimilated into mainstream flexible disk drive design, using available or easily modified components. According to Fleming, hardware and electronic modifications to existing drives and components are minimal. "In development activities, manganese-zinc heads were physically contoured slightly, and the track width reduced. Data band dimensions are slightly different, as are the record current and amplifier gain."

3M is co-developing the technology with drive manufacturers whose names they are not yet willing to disclose. Early media testing by these manufacturers has resulted in media life of about 4000 hours, or 20K start/stops over data.

With introduction of a product based on the technology at least months away, it should be remembered that project Keystone is just one of numerous research efforts going on at all of the flexible media and drive companies. Its ultimate impact on the disk drive market, if indeed it even has one, won't be for at least another year. But the technology does serve to illustrate that flexible media in disk drives is not a stagnating technology.

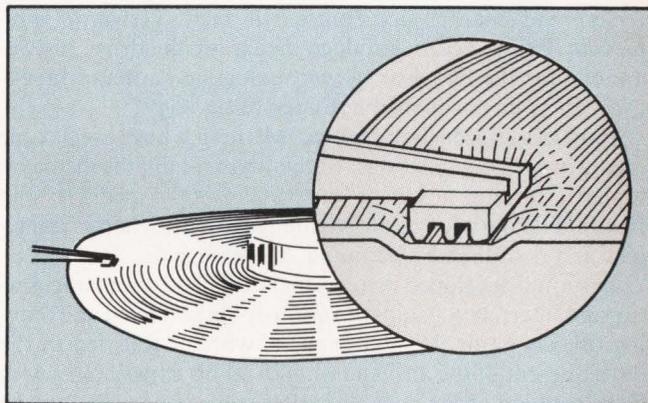


Figure 3: The stretched flexible media of 3M's experimental Keystone drives dimples immediately beneath the R/W heads. This dimpling, 3M claims, disperses particulate contaminants.

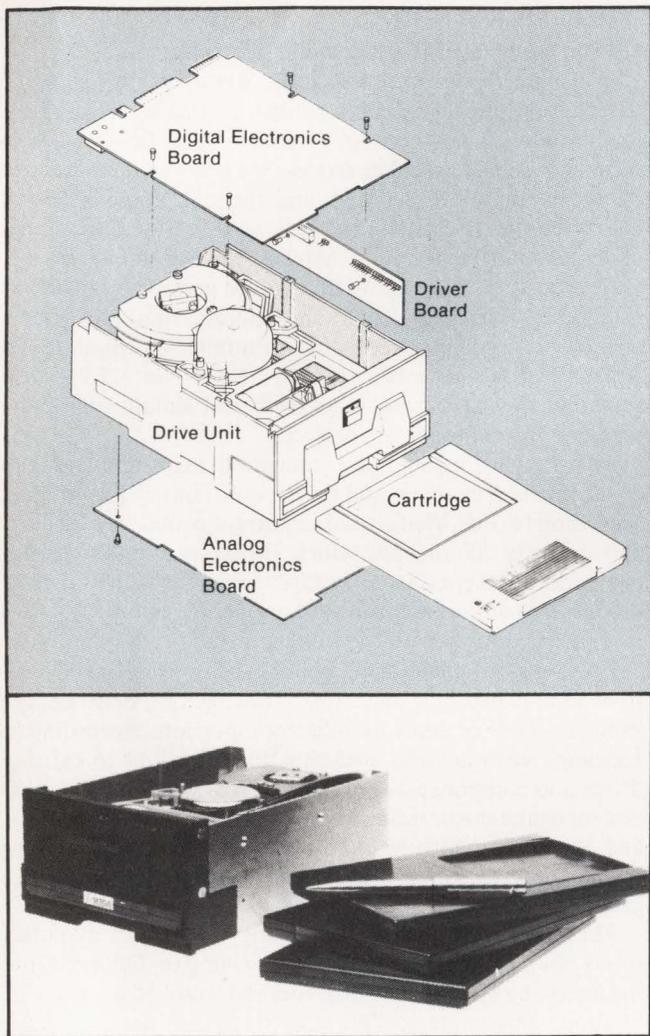


Figure 4: Iomega's Beta-5 uses a floppy disk cartridge to pack 5 Mbytes into a 5 1/4" format drive.

Bernoulli Revisited

Iomega knows how long it can take for a good idea to catch on. Although the basic technology used in their high capacity drives hasn't changed in two years, it is only now getting widespread market acceptance. In fact, Verbatim, who recently contracted to produce media for the drive, just re-announced the two-year old technology as "a major breakthrough in magnetic media storage technology."

Iomega's approach resembles 3M's in that both use flexible media in a unique cartridge. Rather than mount the media on a plastic surface, however, Iomega allows the media to spin free, stabilizing it by taking advantage of aerodynamic principles first described by Bernoulli 200 years ago.

Bernoulli developed theories that explained the characteristics and interrelationships of variously-shaped fixed and moving objects in air. His experiments with air foils led to the development of the airplane wing. And his experiments with disks rotating above a stable surface gave rise to the Iomega disk drive.

A freely spinning floppy disk exhibits considerable instability, making accurate tracking of data difficult. But a disk

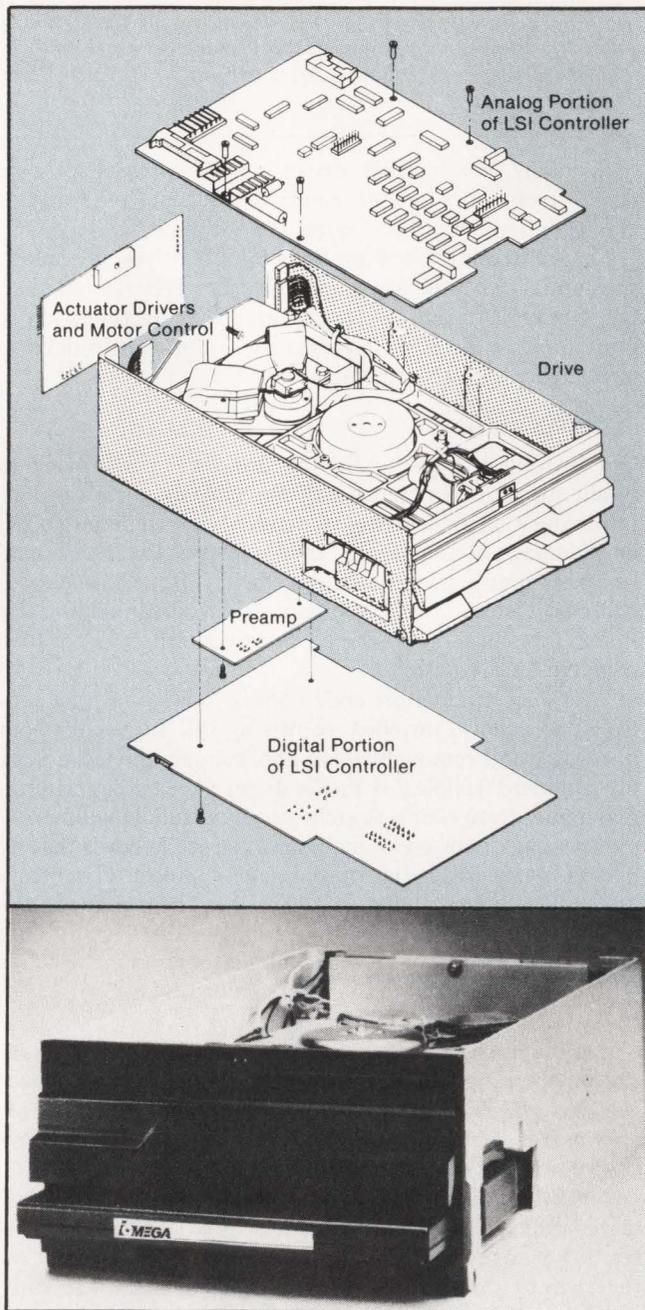
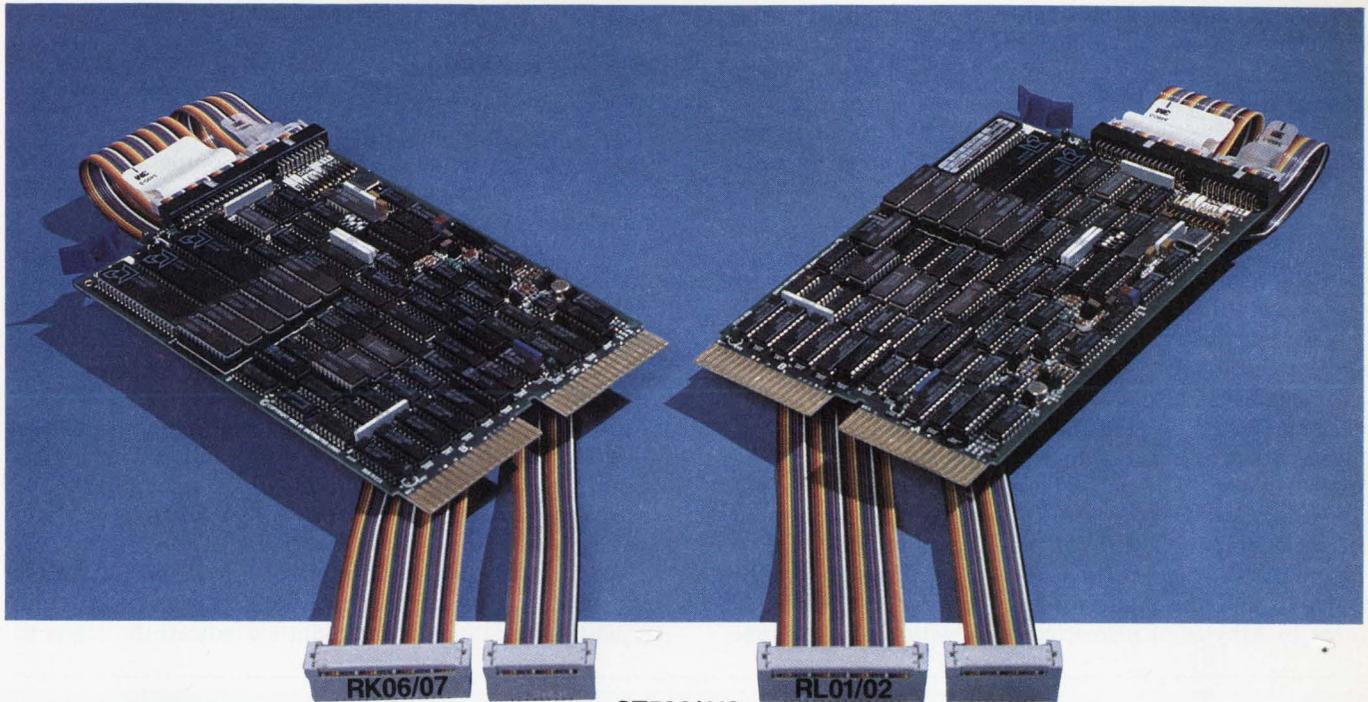


Figure 5: In addition to their standard Alpha-10 8" flexible disk drive, storing 10 Mbytes on a cartridge, Iomega now builds a 10.5 Mbyte version compatible with DEC's RL02.

spinning over a stationary surface will stabilize at a certain distance from the surface, because of negative air pressure generated in the interface by the spinning disk. This distance is determined by the physical characteristics of the disk and the speed at which it spins.

Non-contact recording offers the advantage of low media wear, but must have an extremely small head-to-media gap to achieve high density with an acceptable signal-to-noise ratio. The stable, rotating media of the Iomega drive allows this narrow gap. The media rotates at less than 100 μ inches above the stationary plate. A coupler/head assembly protrudes through an access slot in the plate. Air rushing in through the

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hub opening and the access slot prevents the head from contacting the media. Aerodynamic design of the coupler/head assembly defines a head-to-media gap of 10μ inches. This is narrow enough to allow linear densities of 10K to 20K fcpi.

Head-to-media gaps this small often result in head crashes caused by particular contaminants. But the Iomega design combines a rigid head design with a compliant media that deforms to accommodate particles should they pass between head and media. As a result, particulate contamination may cause soft errors, but no hard errors or damage to media or heads.

In addition, the sweeping motion of the air rushing in through the hub and access slot clears contaminants away from the media. To augment this, recent iterations of the media incorporate a pressure pad to wipe away contaminants. This adds media wear, but was found necessary to keep error rates low, especially in unfavorable environments.

Iomega offers both 8" and 5.25" drives. The 5.25" drive, called the Beta-5 (**Figure 4**), stores 5 Mbytes per cartridge, and has an average access time (seek time, plus settling and latency) of approximately 65 msec. Data transfer rate is 5 Mbits/sec. The drive is both form factor compatible and interface-compatible with the industry standard ST506.

Iomega makes two drives in the 8" form factor: the Alpha-10 and the Alpha-10.5 (**Figure 5**). The Alpha-10 stores 10 Mbytes of formatted data, with a total average

access time of approximately 55 msec. Data transfer rate is 1.13 Mbytes/sec, and the drive is compatible with SCSI hardware, protocol and command set definitions. The Alpha-10.5 is identical, except that it boosts capacity to 10.5 Mbytes and is sector and capacity compatible with the DEC RL02 drive.

Servo-Positioning

While Iomega uses a cartridge media combined with servo-controlled positioning to achieve high capacity, other manufacturers found that servo-positioning alone could provide high capacity, while retaining the advantages of standard-type media. Minifloppy drives from Amlyn and Drivetec store over 3 Mbytes on a diskette—less than Iomega's Beta-5, but double the capacity of standard high-density minifloppies. Although these drives use standard high-density media, the diskettes must be pre-embedded at the factory with positioning information to allow this high capacity.

The two companies use two different methods of head positioning. Amlyn's 170 tpi drive uses media with a reference track pre-written around the disk's outer edge by the media manufacturer. The reference track is 12 mils wide and has eight windows (**Figures 9, 10**).

When a diskette is inserted into the drive, the head reads the amplitude of the reference track at each of the eight windows. Variations in the amplitude indicate the degree to

Artel casts new light on an old problem:





which the diskette varies from being perfectly round. The microprocessor controlled system compensates for these inaccuracies.

To access the data tracks, the drives use a stepper motor combined with an optical sensor. The optical sensor reads a mylar strip coded with 1700 lines per inch, and steps the heads ten times for each track. The idea behind the optical system is that any expansion or contraction affecting the mylar diskette will also affect the mylar strip. Positioning based on the mylar strip should therefore automatically compensate for thermal changes.

Drivetec's 192-tpi drive (**Figure 5**) uses two stepper motors, one for coarse positioning, and the other for fine positioning based on servo burst signals pre-recorded between every sector of every track. The advantage of this system over the Amlyn system is that it actually follows the data track, compensating for eccentricities continuously. The disadvantage is that it fixes the disk configuration at the factory; the Amlyn drive media is user-configurable.

Amlyn's drive (**Figure 5**) is standard minifloppy size, and is second-sourced by MPI. Shugart is considering the technology, but hasn't licensed it yet. Remex licensed the technology, and then discontinued it to concentrate on a half-

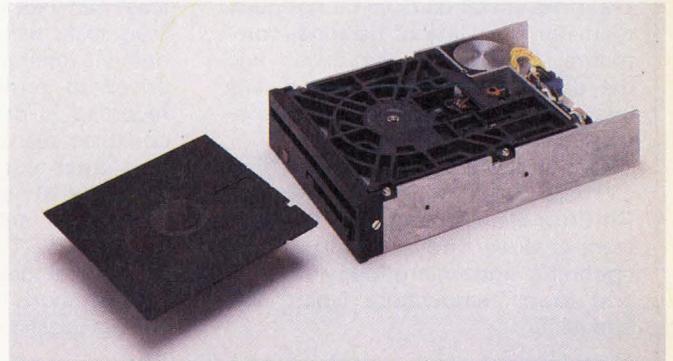
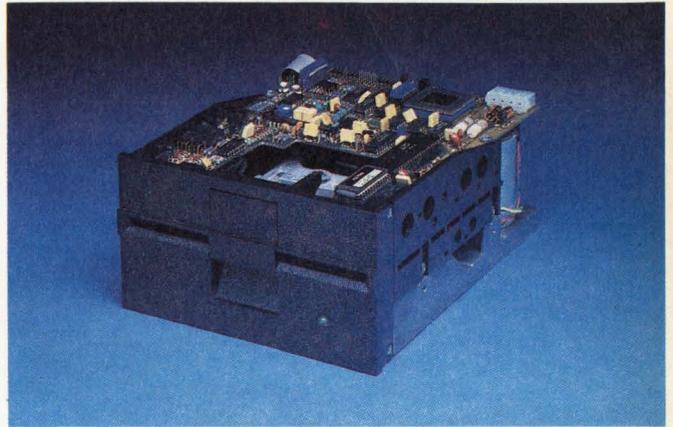


Figure 6: Flexible disk drives from Amlyn (top) and Drivetec (bottom) use closed-loop positioning systems to pack over 3 Mbytes on 5 1/4" diskettes.

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Insuring Microfloppy Reliability

Mass memory subsystems are the leading cause of malfunction in computer systems. Consequently, manufacturers of computer systems, such as Hewlett-Packard, put disk drives through especially rigorous testing before selecting them for their systems. Over the last 18 months HP has shipped more than 100,000 3 1/2" drives making them the leading user of 3 1/2" microflopies. Before they adopted Sony's 3 1/2" drive as standard operating equipment for their line of personal computers, they tested the drives and the diskettes for reliability and data integrity under a variety of environmental conditions.

One of the first tests was the "Five Corners Test." In it, HP performed Bit Error Rate Testing (BERT) in five temperature/humidity situations, spanning the microfloppy's upper and lower temperature limits: 5°C and 45°C.

The Five Corners Test

Temperature (degrees centigrade)	Relative Humidity
5	20%
5	80%
32	80%
45	30%
45	20%

Using eight Sony drives to pass at least 10^{10} bits on each test diskette, read tests were performed by randomly exchanging diskettes between drives to prove that microfloppy's recorded in drives at each "corner" could be read correctly in drives at any other corner. The result was BERTs of 10^{-9} or better.

HP then subjected Sony's diskettes to BERT at room temperature for several days, passing 10^{12} bits. Still, no more than one soft error in 10^9 bits passed was uncovered.

HP then began "strife" tests on the first HP product containing the Sony dual-drive mechanism. Twenty dual-drive devices (without diskettes) were placed in test chambers and subjected to temperature variation cycles ranging from a low of -15°C to a high of $+65^{\circ}\text{C}$ for seven days. Turning the power off and on increased the stress.

"The idea was to make the device malfunction," says HP production engineer Ray Franklin. "As a result, we discovered problems with the HP controller and power supply that were solved prior to production and formal Class B tests."

The next stage involved tests for humidity, condensation, vibration, drop testing, electrostatic shock, and magnetic susceptibility.

•**Humidity.** Extended bouts with temperatures of up to 65°C and humidities ranging from 6% to 96%.

•**Condensation.** Tests in which the drive functioned 15 minutes after being subjected to condensation.

•**Vibration.** A test where the peri-

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peripheral is shaken for 30 minutes at the following frequency ranges and amplitudes:

- 5-10 Hz at 3.17 mm
- 10-25 Hz at 1.52 mm
- 25-55 Hz at .38 mm

•**Drop Tests.** Each drive received 18 blows (3 each on 6 surfaces) at a force of 30 Gs.

•**ElectroStatic Shock.** Testing with electrostatic discharges showed that the Sony drive tolerates 10 KV on its front face. It operates error-free in an electric field of 5 Volts/meter from 14 KHz to 1000 MHz (HP's requirement is 1 Volt/meter).

•**Magnetic Susceptibility.** The diskette was shown to operate error-free in magnetic fields of 4 Gauss (peak-to-peak) from 47.5 Nz to 198 Hz.

While these tests define the drive and media operational parameters, individual drive reliability depends on quality assurance controls. At HP's Greeley, Colorado division, where the devices are assembled, all units must pass a final test, consisting of five procedures:

•**Testing the Write-Protect Tab.** The

test simply involves placing the diskette in the drive and making sure the machine will not write over saved information on a diskette where the tab has been removed by the user.

•**Head Alignment Testing.** HP tests a peripheral's ability to decipher data by using a special diskette with off-center data that's passed through a drive. If the device can't read the data, it's rejected.

•**Motor Speed.** This test measures the consistency of a drive's motor speed with the R/W head both on and off the diskette. On the diskette, the drive is tested at the media's extremes — tracks 0, 35 and 70.

•**Phase Lock Loop.** The free-running frequency of the phase lock loop is measured to assure that it is within specifications allowing lockup to data patterns and low error rates.

•**Read/Write.** Each unit is tested to assure that read/write work correctly.

In addition to the final test, five drives from each shift are selected for "production audits." These combine the above tests with two more:

•**Bit Error Rate Test (BERT).** Drives

are linked to a computer that records the read head's attempts to decipher data written on a diskette. Each attempt or re-try is a "soft error." Ten of them at HP are considered a "hard error." In these tests (also referred to as read-after-write) the 3 1/2" microfloppy exhibited less than one soft error per 10⁹ bits.

•**Interchange Test.** Diskettes recorded on one drive are passed to another to see if they can be read correctly.

HP reports that the Sony 3 1/2" microfloppy drive has proven to be four times more reliable than HP's comparable 5 1/4" product. It has a 1% warranty failure rate, and a cost of ownership that's 33% to 55% below that of the 5 1/4" drive.

To increase data reliability even after the drive is sold, HP drives feature a "media monitor." This feature counts diskette revolutions and records them on the media. When the number of revolutions reaches the maximum recommended, an LED lights up on the drive, suggesting that the user should transfer the data to a new diskette.

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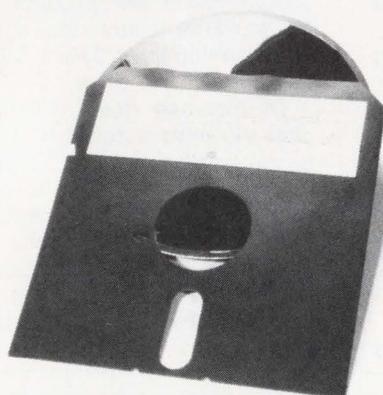
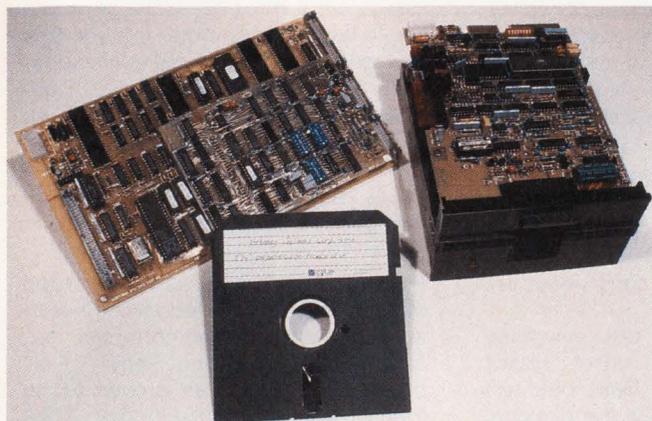


Figure 7: Vertimag's VSC530 (top) looks like a standard Shugart drive, but uses perpendicular recording techniques to store 5 Mbytes on a dual-sided 5 1/4" diskette. Their media (bottom) is a sputtered cobalt-chromium alloy.



Figure 8: A cross-section view shows how cobalt-chromium forms crystals perpendicular to the diskettes surface.

height drive. They may try to forge an agreement allowing them to develop the technology for use in a half-height model.

Drivetec's drive is half-height minifloppy size, and is currently second sourced by Kodak. Both drives sell for between \$300 and \$400 in OEM quantities.

Vertical Recording

To the casual observer, Vertimag's VSC530 5-Mbyte perpendicular recording flexible disk drive looks like a standard Shugart drive. This isn't surprising, considering the fact that Vertimag uses the Shugart drives as the basis for their vertical recording drives. "It's like putting a race car engine in the body of a Volkswagon," says Vertimag President Clark Johnson, Jr.

The drive achieves its high performance without need of servo positioning or cartridge-type media. It increases linear bit density by using vertical recording.

Horizontally-recorded bit densities are limited by two factors. First, magnetized regions defining each bit must be much longer than they are wide. Therefore, as more bits are squeezed into a track, each region must be made narrower, to maintain the length to width ratio. This results in less and less magnetic material per bit and weaker signals as linear densities increase.

Furthermore, horizontal recording aligns like poles that repel each other. As bit densities increase, these repulsions cause physical deformities and demagnetization.

Perpendicular recording solves these problems by arrang-

ing the magnetic regions perpendicular to the disk surface, standing down into the track. With this arrangement, increasing bit density decreases the width of each magnetic region, while leaving the length intact. As a result, boosting density increases the regions' length to width ratio, and actually improves the recording characteristics of the regions. In addition, with vertical recording, areas of opposite, rather than like, charge are adjacent. Consequently, mutual repulsion is replaced by mutual attraction, eliminating demagnetization and physical deformation.

As a result, linear bit densities of 30K fpci are achieved on Vertimag's drive. Although the drive records at a relatively modest 96 tpi, this still allows capacities of 3.46 Mbytes (unformatted), or 2.51 Mbytes (formatted) per disk surface, or over 5 Mbytes per disk. Vertimag claims that capacities three times higher are already being achieved in their lab. Cost for the 5-Mbyte drives, when they are introduced, should be about \$500 each.

The main drawback to the technology is the media. It consists of a polyethylene terephthalate base onto which is sputtered a permalloy keeper layer that acts as a flux return path to minimize record current and maximize playback voltage. Onto this is sputtered a cobalt/chromium alloy that crystallizes with magnetizable axes perpendicular to the substrate.

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The PET base for the diskettes must be perfectly smooth and free of defects, as must be the sputtered surfaces. Contaminants, too, must be eliminated — even the fine silica slip agents often used to coat the polyester film substrate. Furthermore, sputtering, although the most precise method of diskette coating, is also the slowest, most power-intensive, and most expensive method. And because the Vertimag drive is thus far unique, they must supply all of their own media.

To keep up with expected demand for the media, Vertimag recently purchased a 350-ton, 1-Mwatt sputtering unit capable of producing 15 million diskettes per year, according to Johnson. The diskettes are expected to sell for about \$10 each.

Because of their unique data transfer rate of 2 Mbits/sec, Vertimag also designed their own controller. Designed with Winchester disk backup applications in mind, the controller uses the SCSI interface, and supports two ST506-compatible Winchesters and two Vertimag VSC530 floppies. Expected price of the controller is \$1500.

Micros Face Uncertain Future

While boosting capacity is the chief concern of many flexible disk manufacturers, decreasing size is another goal. The sub-4" floppy drives, or microflopies, are the result of efforts by a number of manufacturers (see "The Micro-Floppy Race Tightens," *Digital Design*, Dec. 83).

Microflopies are undergoing a curious evolution. All three formats (3", 3.25" and 3.5") have recently received boosts in support from their proponents. But simultaneously, the confident forecasts for the future of microflopies have suddenly been replaced by a wary conservatism.

Spokesmen for each of the three formats have remarkably similar statements regarding the technology: "We'll let the market decide which format is best." So far, the market seems unwilling to make a quick decision. A boost came for the 3.5" format when Gavilan decided to incorporate it into their portable computer. Together with Hewlett-Packard's use of the 3.5" hard shell design (albeit with different coating and functional specs), this lends substantial support to the format. In addition, a number of drive manufacturers have recently announced double-sided 3.5" microflopie drives that store 1 Mbyte without requiring that the disk be flipped.

Hitachi has stepped up both production and support for its 3" media and drives. By one report, they are now producing 15K drives per month, mostly for use within Japan, but also part of what could be an aggressive entry into the U.S. market.

Meanwhile, thanks largely to the efforts of media-maker Dyan, the 3.25" soft-jacket microflopie continues to make inroads. Original drive designer Tabor has been joined by MPI and Seiko as manufacturers of the drives, with Seagate prepared to enter the market should demand warrant.

Dyan has spun off a division devoted specifically to selling IBM and Apple software for the 3.25" microflopies, to give market acceptance of the drives a shot in the arm. "They're crazy," says one rival media manufacturer, "they're competing with their own customers." But to Dyan, the most important aspect of the microflopie competition is that 3.25" must gain a sizeable share of the total market early enough to make production of the media profitable. The availability of software for the 3.25" drives early on gives designers more incentive to specify them for portable computer systems.

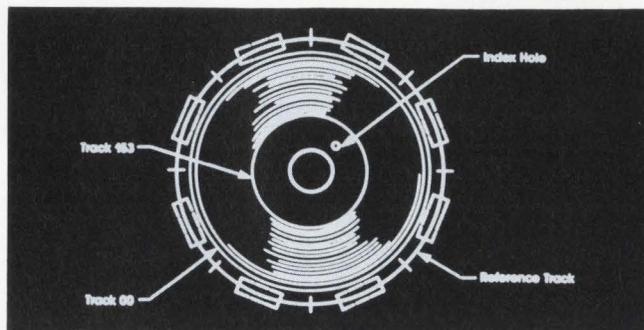


Figure 9: Amlyn's 170 tpi flexible disk drive uses a reference track with 8 windows for accurate R/W head positioning.

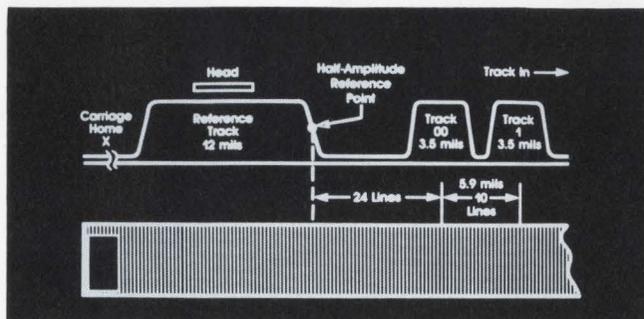


Figure 10: The 12-mil reference track on the edge of Amlyn diskettes allows the R/W head positioning system to compensate for physical eccentricities.

As far as desk-top computer systems are concerned, Jim DeStefano, Dyan Business Strategist, thinks that microflopies will be eclipsed by high capacity miniflopies. "In Japan they are putting together a 2-Mbyte miniflopie-compatible standard on the 5.25" disk. So you can expect half-height disks with 2 Mbytes to come flowing into the U.S. sometime during the year and they will fit into a desktop very nicely. When those products become available, who's really going to want to buy a half-Mbyte or even a 1-Mbyte microflopie?"

DeStefano thinks that the microflopie's niche will be in low-cost, notebook-size portable computers, and low-cost home computers. "There are a lot of home computers out there that don't have disk drives. Those people want to go out and buy an add-on, but they're thinking tape cassette price range. We intend to get the price of media and drives down so that it competes with tape cassettes."

Enter The Film Makers

One factor that will help drive down media costs is competition from a new source: photographic film companies. Kodak, Polaroid and Fuji have all entered the flexible diskette media market within the past year. Kodak's Spin Physics division manufactures Isomax diskettes that use smaller, improved magnetic particles. According to Kodak, Isomax diskettes allow linear bit densities up to 40K bpi.

Fuji Photo Film U.S.A. recently introduced 3", 3.5", 5.25", and 8" diskettes through their new Magnetic Products Div. Although they have been marketing flexible media in Japan since 1977, Fuji states that they were reluctant to enter the U.S. market because of "market instability" in the U.S. Recent "trends towards stability" have now made entering the

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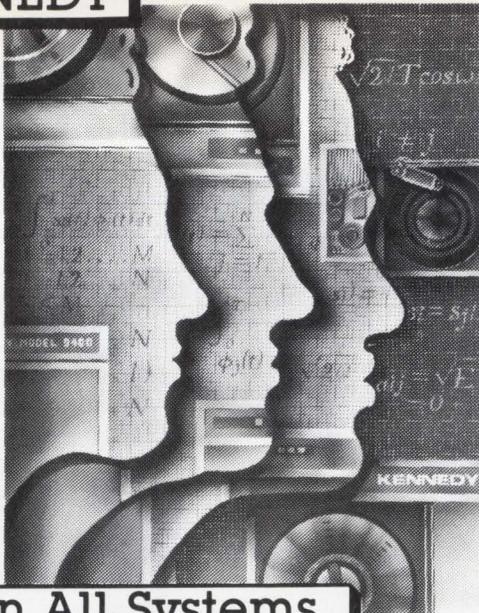


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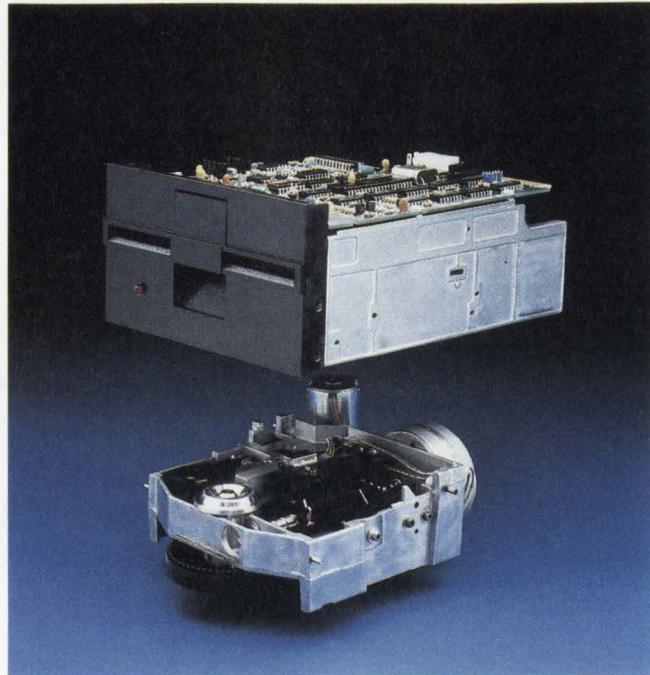
Floppy Drives

Figure 11: Micropolis' minifloppy drive uses a chassis-within-a-chassis construction to increase durability.

market more desirable.

Polaroid, too, has decided to enter the market. They will supply Permabyte Magnetics (Chatsworth, CA) with "premium quality 8", 5.25" and sub-4" floppy media." Permabyte will then convert that media into a finished disk. The diskettes will then be distributed by Polaroid and Perfect Data (Chatsworth, CA). Availability of the diskettes is scheduled for early this year.

Death Throes Continue

Despite rapidly increasing media sales, and significant advances in drive price/performance, rumors of the floppies demise continue. One recent article went so far as to refer to the "death throes" of flexible media. If flexible media sales are any indication (with a compound annual growth rate in excess of 40%), floppy technology is certainly undergoing some of the most profitable death throes in the computer industry.

In the near term, strong media sales are expected to be accompanied by strong sales of standard and especially half-height minifloppy drives, slow but steady increases in microfloppy drive sales, and the ramping up of high-capacity drive production. Consequently, there would seem to be no foreseeable end to flexible disk technology's death throes and, in all likelihood, hapless floppy disk companies will suffer even greater profits in 1984.

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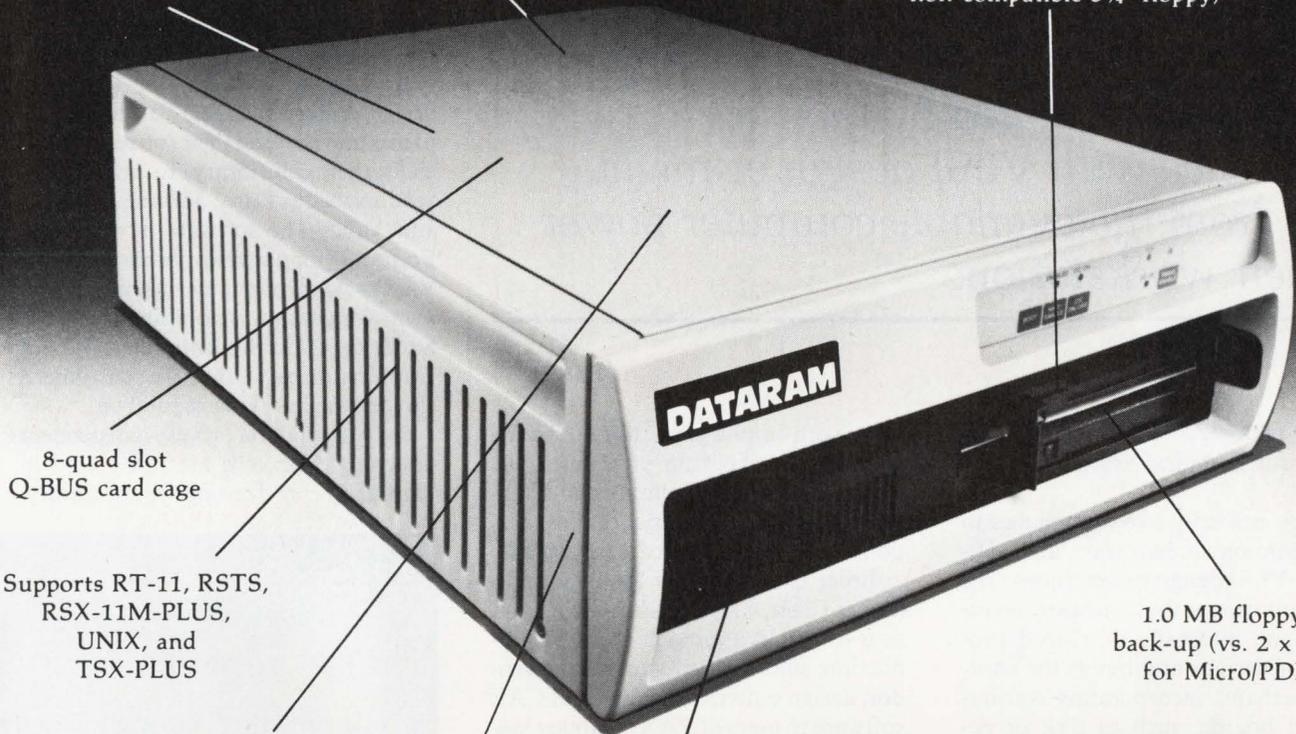
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Integrating Hardware And Software For VLSI Design

The philosophy of the CAE company might be determined by their own experience with VLSI design or might stem from the available computer power in their workstation.

by Tom Inglesby,
West Coast Technical Editor

There are basically two approaches to the integration of hardware and software for VLSI design workstations. The vendor purchases the hardware necessary to run internally developed programs, or designs and builds the hardware, perhaps incorporating various standard boards, such as disk or peripheral controllers. Many CAE vendors prefer to remain software houses and leave the hardware development to those companies with the resources necessary to remain competitive. This can present a problem of compatibility between generations of workstations if the hardware company fails to keep up with the CAE vendor's needs. Some companies have hedged that bet by utilizing standard buses, such as the Multibus, in creating their own hardware. Others have approached the problem by merging resources with a hardware company for a larger say in the development of the computer.

Foundry/CAE Vendor

Most of the CAE workstation developers started as software houses. A few started as silicon foundries, and this is still their main profit center with the design systems being released either to the marketplace directly or through controlled design centers.

By selling the necessary design sta-

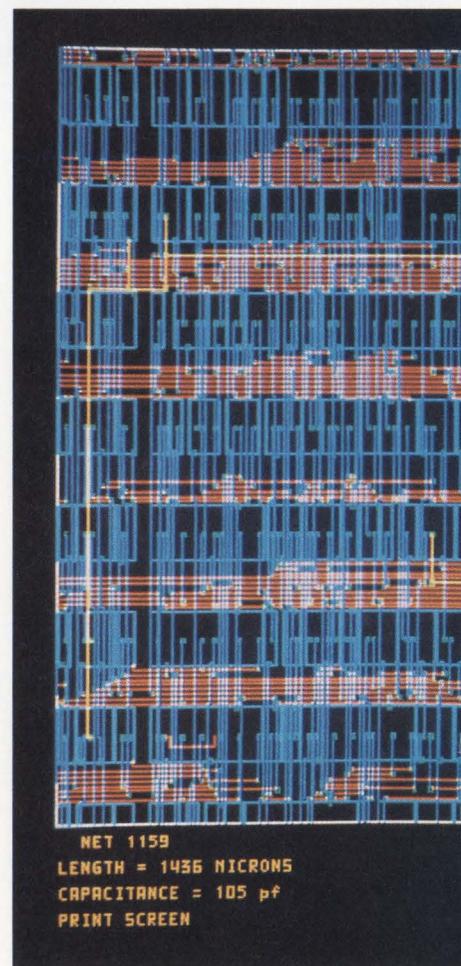
tions, with emphasis on their cell libraries and rule checking procedures, the silicon companies can insure that a substantial part of the output of those stations will be channeled to their facilities.

Bruce Christopher of Matra Systems (Santa Clara, CA) explains the situation as a four-fold approach to VLSI production: silicon seller, workstation vendor, design center, and supplier of CAE software to users of VAX computer systems. Matra builds their own hardware based on the Multibus with dual processors, the 8086 and 8087. By using Intel products the hardware is supported and serviced by Intel. This configuration isn't unique in the industry but then Matra isn't a hardware vendor, depending on their specialized software to set them apart. In this area, they offer an 18 state logic simulator to test the circuit according to the timing specifications and to do a fault test generation right on the system. Matra also have a program that converts a bipolar programmable array logic (PAL) into a CMOS gate array by using the Boolean equation derived from the PAL. They claim that a CMOS gate array can be developed in approximately ten minutes through this method.

Another systems integrator with roots in the silicon foundry is International Microelectronic Products (IMP) of San Jose, CA. A complete IMP workstation can be purchased or the design software is available on a time-shared basis via

dial-up from the customer's location or can be installed on the customer's computer system. In addition, IMP has design centers available to client companies and they sell their software, especially their cell library, to other CAE vendors such as Daisy, Mentor, Metheus, and Valid. The software is written in Fortran 77 for portability between Prime, VAX or Apollo computer systems. IMP's own workstation is composed of a 32-bit Prime 2250 minicomputer, Jupiter graphics display and the customer's choice of networking capabilities.

IMP depends on process-independent designing. The cells are not stored in hard geometry drawings in the library.



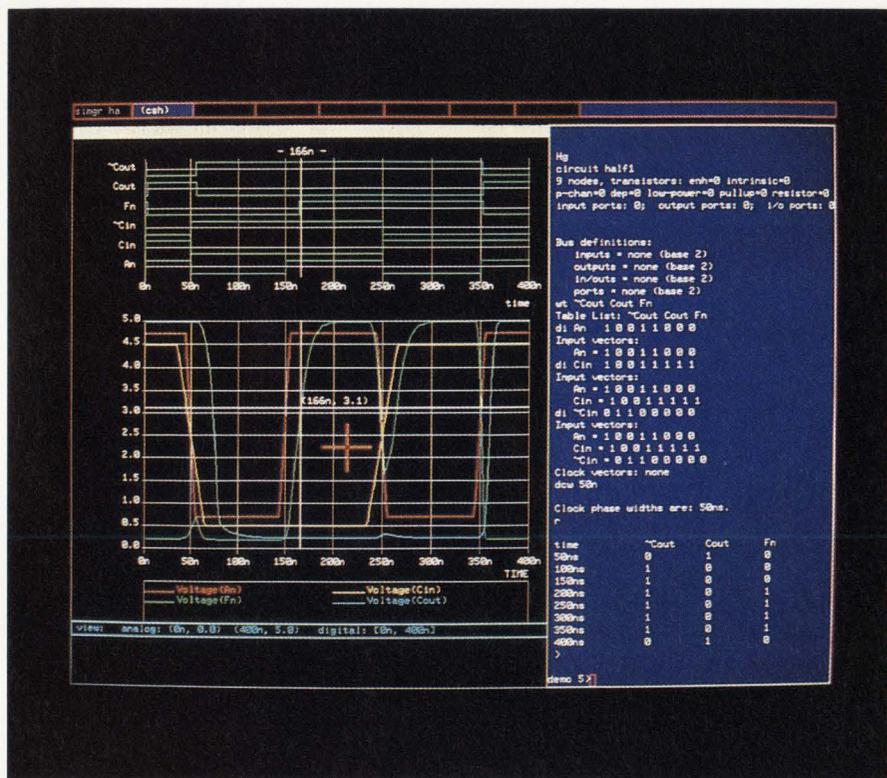


Figure 2: Using a split screen or windowing effect to allow menus on screen with the design or, as in this photo from Metheus, logic simulation patterns, can increase designer productivity by making choices readily visible.

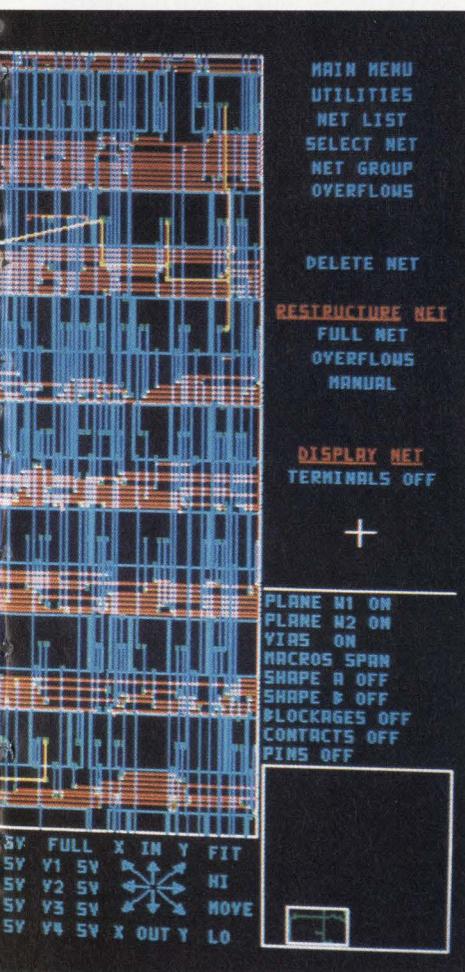
built into the native operating system. The programs are written in Pascal, FORTRAN and a structured language precompiler called Mortran which outputs FORTRAN. Some of the programs provide methods for entering the description of the chip into the system through schematic capture, text editing or translating a previous design made on another vendor's system. Other programs are a version of UC-Berkeley's SPICE circuit simulator containing the CSIM compact short channel IGFET model and three classes of AMI enhancements, the SIMAD MOS/VLSI logic simulator which verifies logic designs and develops test patterns, and PATH, a timing verifier which works on worst-case propagation delays through each path of the chip.

AMI software layout tools and design testing programs lead the designer all the way to the verifying of mask layouts, biasing of mask layers for manufacture and conversion to formats required by pattern generators and EB machines.

Hardware/Software Integrators

A firm with origins in West Germany, Kontron Electronics (Redwood City, CA) took the approach of combining their European designed hardware with American developed CAE software. The software was developed by Mikron Integrated Microelectronics (Redwood City, CA) for use on the Kontron Design Station (KDS) which was developed in Munich. Kontron markets the system for the personalization of gate arrays, not for developing silicon VLSI designs.

Dr. John Adam of Kontron defines the gate array personalization design stages as system schematic entry (using the library of symbols), on-line checking of the schematic, netlist extraction, logic simulation to check logic operation, and timing verification. As do AMI, IMP and Matra, Kontron will accept the output of their workstations from customers and provide prototype silicon, only they are acting as a broker not as a foundry. They have a supply agreement

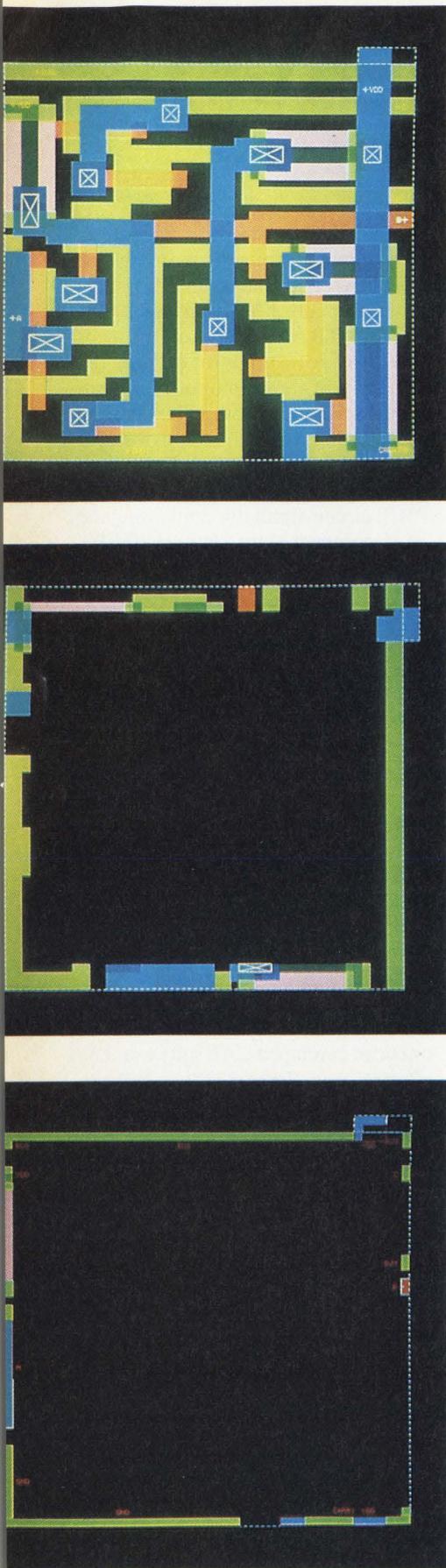


Instead, they are in the form of a "recipe" which can be easily modified if the rules or processes change. This means that the library won't become obsolete; the designer simply has to go back to the "recipe" and make the changes. Then the hard drawings of the geometry in the already proven circuit are changed accordingly.

As with Matra and IMP, AMI's interest was in getting more business for their silicon foundry. This meant that portability of their software to a variety of hardware systems was necessary to give both AMI and its customers the freedom to choose from several computer, display and peripheral vendors, allowing them to take advantage of price/performance improvements in the future.

The ACT system incorporates more than 50 programs and supports 25 MOS circuit fabrication processes. Porting ACT to various computer systems is made easier by providing "hooks"

Figure 1: A color display can improve operator accuracy in determining the various layers of a design. In this illustration from Mentor Graphics, the blue and red traces represent two layers of an array while the yellow lines indicate a missed connection.



Figures 3-4-5: Design rule checking requires significant computer power, especially when chips exceed 10,000 components. Valid Logic Systems developed their SCALDstar with a hierarchical verification program that checks each low level cell as it is created and then generates two representations of the cell without the internal geometry. Since the cell has been proven correct, the outer boundaries are where future errors can occur. The bounded cell with external connections and the "donut" of the cell with all boundary geometry shown are used in rule checking to reduce time and power requirements.

with AMI for fabrication from a supply of Kontron owned wafers. All they have to do is send accurate masks developed from the client's data to AMI and have the final metal layers put on and etched.

A company integrating outside computer hardware with outside CAE software is Mentor Graphics of Oregon. They use the Apollo computer and Domain networking features to run software developed by California Automated Design, Inc. (CADI) of Santa Clara, CA. To do this, they merged Mentor with CADI and the combined companies, operating under both names, provide complete CAE stations (Mentor) or just the software (CADISYS). The Mentor/CADISYS layout tools, for instance, run on the Mentor IDEA 1000 workstation when working with gate array designs up to several thousand gates; if the design calls for more than 10,000 gates, CADISYS operates on a mainframe networked to the Mentor.

CADISYS incorporates automatic placement and routing as well as graphic representation of the design on a color raster screen. Mentor integrates this software with several combinations of Apollo hardware to provide the designer with a variety of CAE systems meant to carry the VLSI process from idea to PG tape.

The Apollo computer hardware is popular among CAE systems integrators as is Prime and, for larger systems, DEC's VAX. Major companies such as Calma use Apollo systems for both mechanical and CAE workstations. As Calma product manager, Phil Arana, puts it, "If we decided to make our own computers, we'd have a difficult time keeping up with the technology that companies like Apollo, IBM and others are incorporating in their system archi-

ture. We think that we can keep up in the area of display quality and interfacing the software with the display. There is a much closer dependency on the interaction of the hardware and software and it is here that we can increase the acceptability of the system by providing some hardware assists in the display mechanism."

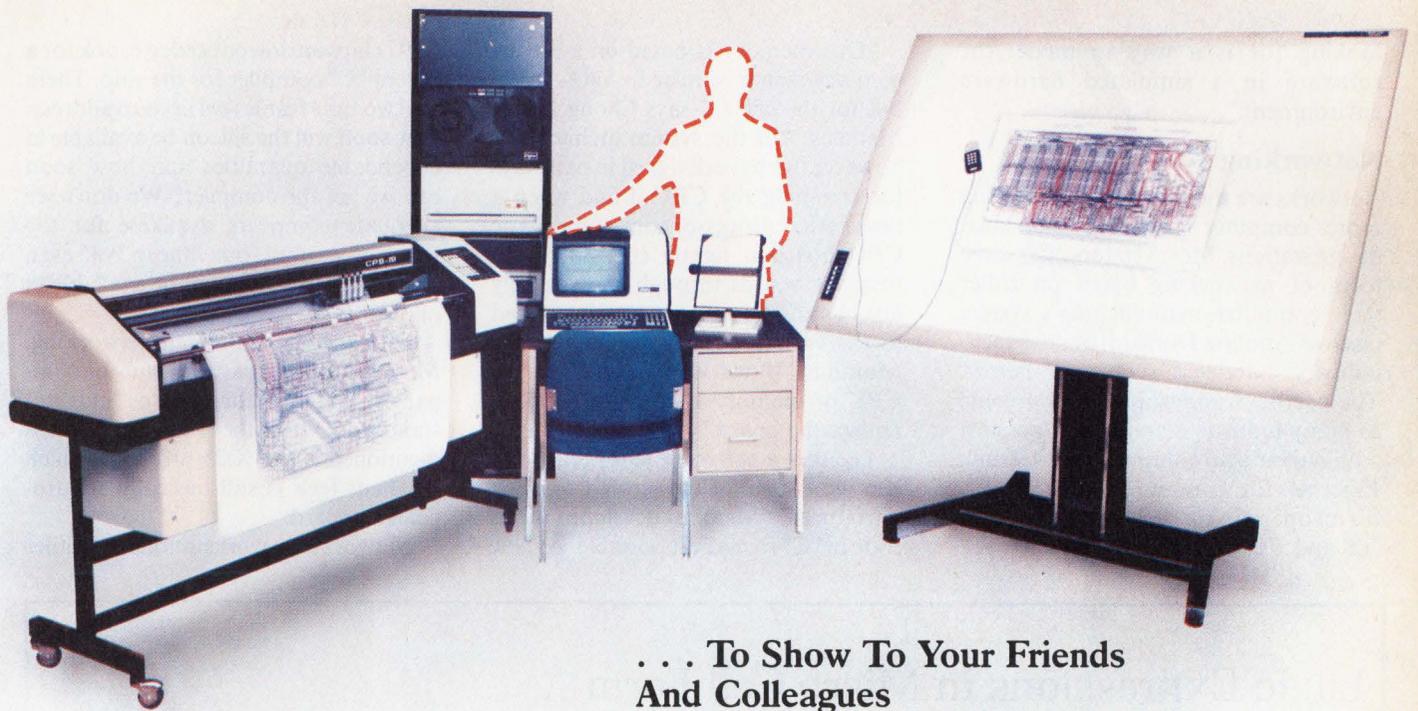
Calma's marketing approach is to provide modular systems with a defined growth path in both hardware and software. Calma supplies software modules for schematic capture, layout, simulation, and design verification. Using logic libraries from AMI, IMP and other vendors, the customer can take the design from idea to PG tape output. One Calma Program, STICKS, can be used with cell libraries as a general, technology-independent design tool that includes mechanisms for automatically compacting design data according to specific rules.

Arana and Malcom White of Calma see increasing research in the area of silicon compilers which will take high level language inputs from the designer and translate them into schematic drawings. The user will be able to "talk" through a design (actually talking with the incorporation of voice recognition systems!) with the schematic being entered without the operator's knowledge of the process being used.

In terms of a designer specifying the parameters of a chip and having it designed automatically, they feel we are a long way off. But the system isn't too far off that will allow certain sections of a chip to be specified and then designed without human involvement.

General Electric is going into the development of macro cell libraries, too. Macro cells are like standard cells but of arbitrary size and shape. Working with them is like using building blocks with each complex segment of the IC represented by a cell. Once the cells are determined, they can be used with current or future fabrication processes by changing the descriptions within the cell.

Arana adds, "Microprocessor-based designs have a very tight coupling between hardware, software and firmware that drives the system. It is becoming a very difficult job to model the end performance of the system. It isn't just a case of simulating the hardware but it is also dependent on the software, which in most cases is not written. What we are



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looking for is a way to model the software in a simulated hardware environment."

Networking

Networks are the next step in providing more computer power to individual design stations. Most vendors offer some form of networking based on either their computer manufacturer's system (such as Apollo's Domain) or on defacto industry standards such as Ethernet. The Metheus philosophy is to provide as many industry standards as possible within their own computer architecture; Ethernet for communications, UNIX for an operating system and support for "C" and FORTRAN languages.

"Our memory is based on a virtual memory system similar to VAX/VMS but for the 68000," says Chong Lee of Metheus. "In the system architecture, however, we have designed in pathways for changing the CPU if and when a better microprocessor comes along. The CPU board is tightly coupled to the memory boards through an extremely fast bus and this subsystem is interfaced to the various controllers through the Multibus. If we want to change the CPU or memory all we have to do is replace the board."

Lee sees a software/hardware problem with some of the new chips being introduced. "Metheus developed all its code in "C" to make it portable. As new

CPU chips are introduced, we look for a decent "C" compiler for the chip. There are two time frames we need to address: how soon will the silicon be available in dependable quantities and how soon can we get the compiler? We don't see adequate compilers available for the newer chips until sometime in 1985 even though the silicon might be available in mid-1984."

By choosing Ethernet networking, Metheus joins a growing club of companies that are turning to "industry standards". Another standard often mentioned is the X.25 protocol, which Metheus feels is still basically a European standard.

Networking workstations together

Logic Expressions in Micro Cell Form

A recent start-up company in Scottsdale, AZ, Cademic, Inc., is marketing a microcomputer-based CAE workstation called "CLYDE." While the hardware, utilizing the Motorola 68000 processor, isn't novel, the approach they use for logic development represents a break with traditional methods of schematic capture.

The \$10,000 workstation package includes logic design, logic simulation, timing simulation, chip external hook-up, a macro cell library, and supporting technology data.

The CADEMIC approach uses entry of logic expressions in micro cell form on a matrix instead of the more common electronic schematic diagram. The design system supports all forms of hierarchy through the use of these micro cells. Micro cells can be used to develop macro structures such as flip-flops and counters which, in turn, can be used to produce larger cells such as registers and multipliers. The designer interprets these cells as "AND" and "OR" gates or as truth tables.

The designer can insert cells one at a time, from left to right in a row and from top to bottom in a column. To connect the micro cells, paths are entered with the cursor. Vertical paths are shown in magenta and represent "OR" functions while horizontal paths are in yellow and indicate "AND" functions. Macro cells are inserted from the cell library with the origin of the cell at the location of the cursor on the matrix. Cells can be moved, named, and customized through keyboard commands.

Besides the provided cell library, the customer can construct and add proprietary cells to the library. These are developed from scratch or by modifying existing macro cells. The technology files include information on NMOS, CMOS, IIL and other processes to provide the designer with data in a technology independent manner for timing and other simulations.

The illustration shows a 4x4 multiplier with yellow paths (AND/NAND gates) with 1 and 0 as inputs and + and - as outputs. The vertical magenta paths (OR/NOR gates) follow the same rules where 1 and + are true, high,

positive, etc. for inputs and outputs and 0 and - are false, low, negative, etc. The truth table minterm expressions are on the yellow paths with 1, 0, and blank indicating true (1), false (0), and don't care (blank).

The use of truth tables to input logic into the system is said to improve first time user's productivity because the system is familiar to engineers even right out of college. This integration of ease of use with ease of learning might be the direction for entry level workstations of the future.

—Cademic
Write 301

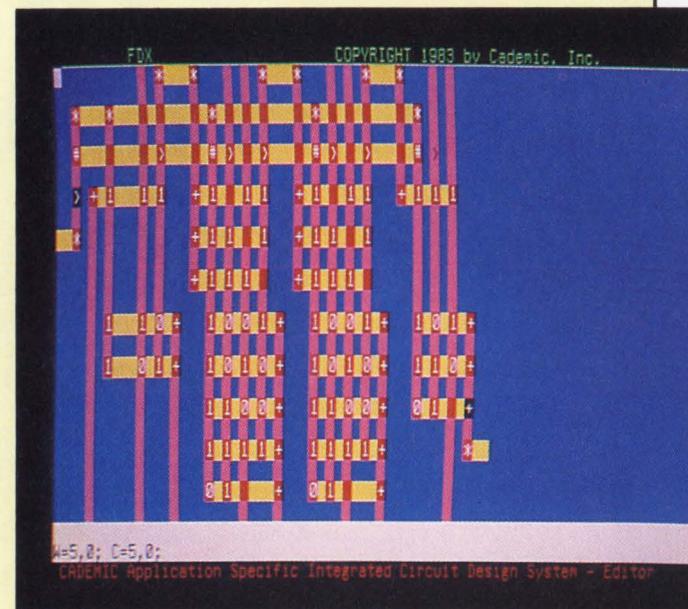


Figure 1: The Cademic approach uses entry of logic expressions in micro cell form on a matrix instead of the more common schematic diagram.

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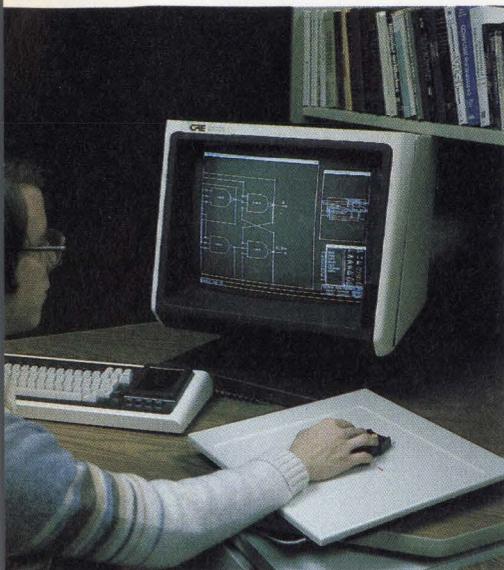


Figure 6: CAE 2000/420 used in logical design for VLSI.

requires more than cable and protocols. The important database access between stations must be included to increase the data transfer among designers. With more LSI chips being designed by groups of engineers, each working on a particular segment of the whole, the interchange of data is vital. Working from the common database the designer can not only be assured that the information is up-to-date but also that each engineer knows where the others are in the process. Even such peripheral but important functions as documentation and archival drawings can be generated accurately only if the information that they draw upon is current.

With the Apollo Domain network, the access to other workstation's power is transparent to the individual. The user can multiply the power of each workstation by the number of stations on the network, according to Calma's White. "That transparency is the key to efficient use of the network because the operator doesn't have to do anything that will distract from the design process."

The Human Operator

One development that Calma has been experimenting with for more than a year is voice recognition for the design station. "We haven't had many requests for it because of the high price tag," responded Arana, "but as the cost comes down, the idea will start to catch on in some areas. We had one piece of equip-

ment that actually demanded voice recognition because otherwise the operator couldn't keep up with it. That may have been the first use of VR in CAD!"

Chong Lee of Metheus agrees that the operator needs special attention in the overall integration of VLSI systems. "If you're doing a lot of waveform analysis or complex ICs, you need a color display. With a monochrome unit it takes months to train a designer to recognize the layers and the traces accurately. Even with a color display, there must be controls for the designer to tailor the color choices to match personal work methods. We have had at least one designer in our training classes who was color blind in the red spectrum. Without a way to alter the color choices in the design, this person would have lost a lot of information."

Other Approaches

A major silicon house, Fujitsu in San Jose, CA, uses VLSI workstations with their own software but depends on mainframes in Japan for the computer-hungry complex stages of the design process. With both Daisy and Valid systems in-house, Jim Coe, VP for custom products, explains, "We create a data file of the logic here and edit it. Then it is transmitted by satellite link to the Fujitsu mainframes in Kawasaki. We have written, in cooperation with Daisy and

Networking workstations together requires more than cable and protocols.

Valid, the conversion routines necessary to take their format and make it usable on the mainframes. Once we get the netlist and test data, we treat the in-house developed designs the same as those submitted from outside customers. "Our system is built to be mainly a design verification system rather than an interactive design system. It will take a logic design and a set of test vectors and tell whether the circuit will work that way, and exactly how the silicon will work. We guarantee that we can give the customer a specification that will work in CMOS before we start on silicon."

Since Fujitsu depends on mainframes Coe has some strong opinions on the capabilities of workstations in VLSI design. "The present state of the art in workstations deals adequately with schematic capture, the drawing of a schematic on the screen and building logic. They can be interactive, flag design

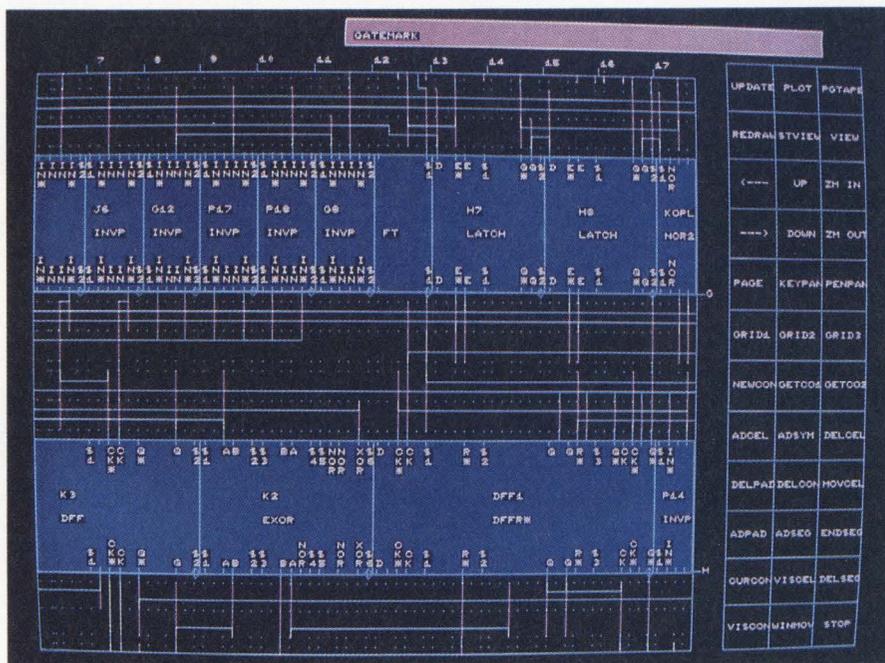


Figure 7: The GATEMARK system from Matra Design Systems provides schematic entry, fault test generation, automatic layout and PG/Calma art layout.

rule violations, and do timing verification where you can build a model of each gate with timing parameters on it and use that model for the path analysis. But the simulation systems being sold don't really simulate the device. There are two problems we see in this area. One is the lack of CPU power and the other is the lack of a dynamic load equation. If you take a 2000 gate array with several thousand test vectors, a fairly normal piece for Fujitsu," says Coe, "then you'll tie up a workstation for two or three days to run a simulation that we can complete in 25 minutes."

Microcomputer-based Systems

Several vendors are offering CAE systems based on the ubiquitous IBM Personal Computer (PC). One of the major forces in this revolution is Chancellor Computers of Palo Alto, CA. They are bundling the IBM PC/XT (hard disk version) with software from CADI including CADIGRAPH, SKIMCAP schematic capture and netlist generation, and SIMULOG interactive logic simulator. Because of the limited computer power in the basic PC, such systems are still aimed at the area of smaller, less complex designs. However, as entry level systems for designers who will turn the more complex stages of development over to the silicon suppliers, these systems might prove adequate.

A familiar name among workstation developers is Daisy Systems of Sunnyvale, CA. One of the earliest designers of free-standing systems, Daisy has moved one giant step toward total software/hardware integration with the release of their MegaLOGICIAN. Called a third generation workstation, the MegaLOGICIAN takes several simulation functions that were formerly handled by software programs . . . gate level simulation, functional level simulation, and behavioral level simulation . . . and incorporates them into a new hardware simulation engine. As a result of this integration of functions into hardware, they claim a 100 times increase in simulation speed over previous Daisy systems.

Summary

Newer workstations are integrating the software necessary to design advanced VLSI with faster and higher powered computers, both in-house and outside developed. There are still limitations

imposed by the available CPU's and the extent of software development, especially in the area of logic simulation. A long overlooked factor in the integration equation, the human operator, is being addressed by many companies. In the near future, VLSI design may take a turn toward the integration of actual Artificial Intelligence concepts with the

addition of voice recognition and silicon compilers capable of designing a chip from high level language inputs. □

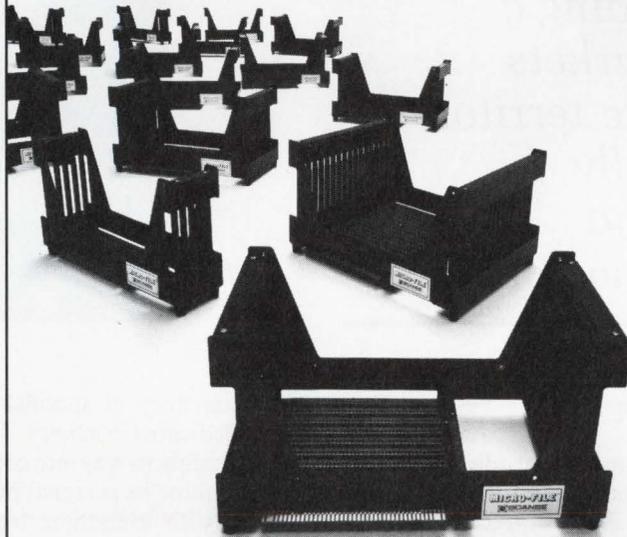
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The Expanding Realm of the IBM PC

The IBM Personal line is invading a range of markets formerly the territory of specifically designed and dedicated machines.

by Julie Pingry, Editor

Ubiquitous seems *the* most used adjective for IBM's Personal Computer. And if it's everywhere now, recent announcements from IBM and the rest of the industry will allow the PC far wider applications. Not content to have the ascendant personal computer on the market, IBM has introduced both higher and lower end models, the PC/XT, XT/370 and 3270-PC and, at long last, the PCjr, to provide a family of microcomputers.

The basic PC was the first personal computer to use the Intel 8088 processor — now becoming standard (and nearly impossible to purchase because of that fact). The 16-bit processor has been a great advantage for the IBM PC over older 8-bit micros. The XT adds hard disk storage for higher-end business and industrial use. And the PCjr uses a smaller keyboard (no function keys), maximum 128K memory and no expansion slots, for home use.

Although these are not terribly innovative computers, the IBM Personal line is invading a range of markets

formerly the territory of specifically designed and dedicated machines. The PC is already finding its way into companies who combine its personal processing power with everything from data acquisition to word processing, to remote data entry and access. This move for PCs was sparked not only by the IBM name, but also by the availability and reliability of its parts and software and the standardization springing up around it.

One of the biggest advances for IBM in the PC family is the encouragement of third parties. Besides the basic IBM memory expansion unit, displays and printers, the PC catalog includes NEC and Epson printers, Hayes modems, a Versa Graphics tablet, INMAC hardware and Kraft game controls, as well as a variety of software offerings. The once isolated giant of mainframe computers has flung its doors open to others in this PC market, and with good effects. The flexibility of adding this range of hardware and software to the PC will no doubt be as large and essential an asset for IBM as it has been for Apple in the PC market.

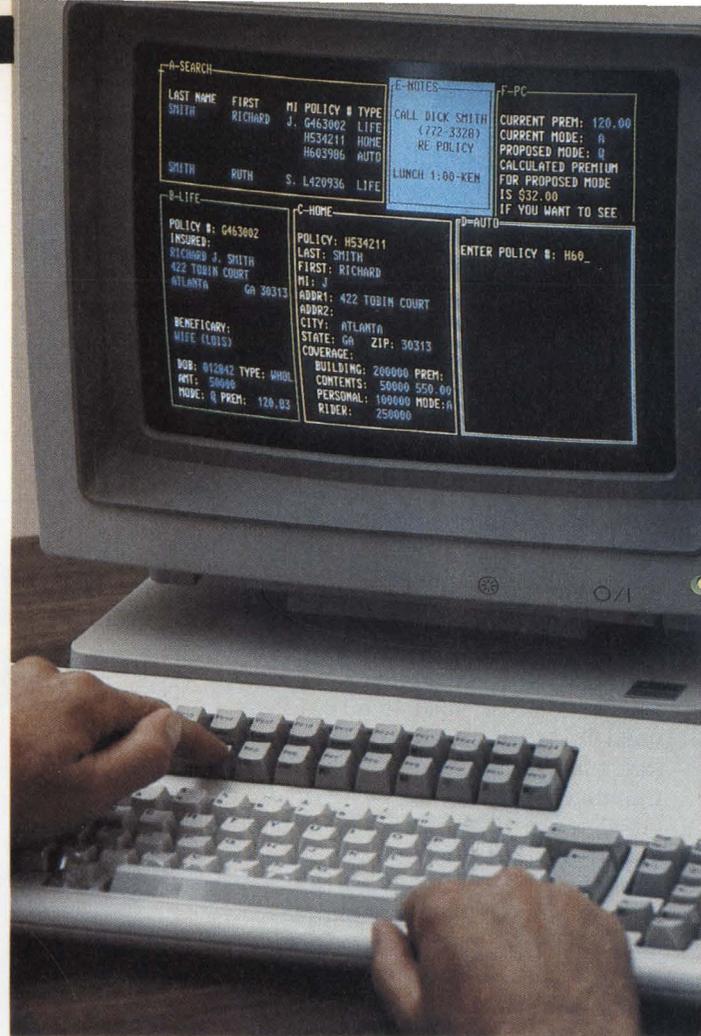


Figure 1: The IBM 3270-PC uses windowing to display up to four host applications and two notepads simultaneously with the PC program.

High-End PCs

The expansion of the PC into sophisticated industrial and design applications, however, will often require a direct connection into IBM mainframe systems. IBM's October announcements, the XT/370 and the 3270 PC, are designed for personal computer access to IBM's mainframes.

The 3270-PC, available with 256K to 640K of main memory and optional 10 Mbyte hard disk, will run up to seven simultaneous applications, with as many user-definable windows (**Figure 1**). Four of the seven programs are used on IBM mainframe hosts, two are "notepads" and one, for the PC program, giving users access to both mainframe files and PC processing. This capability for accessing files and development work will be invaluable to users

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in large networked environments. Anyone who is experienced with the 3270 display can learn to use this PC easily, since the keyboard combines the 3270s and PC's.

A direct enhancement to the PC/XT, the XT/370 includes three boards that allow an XT to run programs under VM/CMS, as the IBM System/370. Called three workstations in one, the XT/370 can act as a 3277 display terminal connected to a host or as a 370, as well as functioning as a PC/XT. To get mainframe power for running VM/CMS programs, the added boards have dual 68000s, one standard and one customized for System/370 fixed point data and control instructions. A custom 8087 is used for floating point operations. The boards have 512K of added memory, 4 Mbytes of virtual memory to accommodate VM/CMS operation; and a coax attachment to connect to a 3274 display controller for use as a 3277 Model 2 terminal.

The multiple character of these PCs, with both processing for an individual and access to corporate files through IBM hosts, will make them attractive for both desktop use and replacements for terminals. Naturally, with the enormous IBM mainframe base, corporate users will value access to existing systems. Even before these announcements, a study showed that over half of the personal computers going into the corporate market were IBM's.

Simultaneously with the two high-end PC announcements, IBM brought out a board product for the PC or XT for 3278 or 3279 display unit emulation, and an attachment to the 3279 color display to allow it to act as a PC. To further integrate the PC into the traditional IBM line, the XT can be attached to System/38, /36 or /34 through the 5250 terminal emulation program, and a utility from IBM allows PC DOS 2.0 to run on these same systems.

PC Communications

Others have also realized the huge potential of PC links to mainframes and other computers. Recent product

announcements for the PC, XT and even the PC jr will allow communications and file/database access between personal computers and between PCs and main computing power. The variety and number of products in the PC communication field are both testament to the IBM PC's popularity and a boost to its flexibility (and thus, no doubt, its marketability).

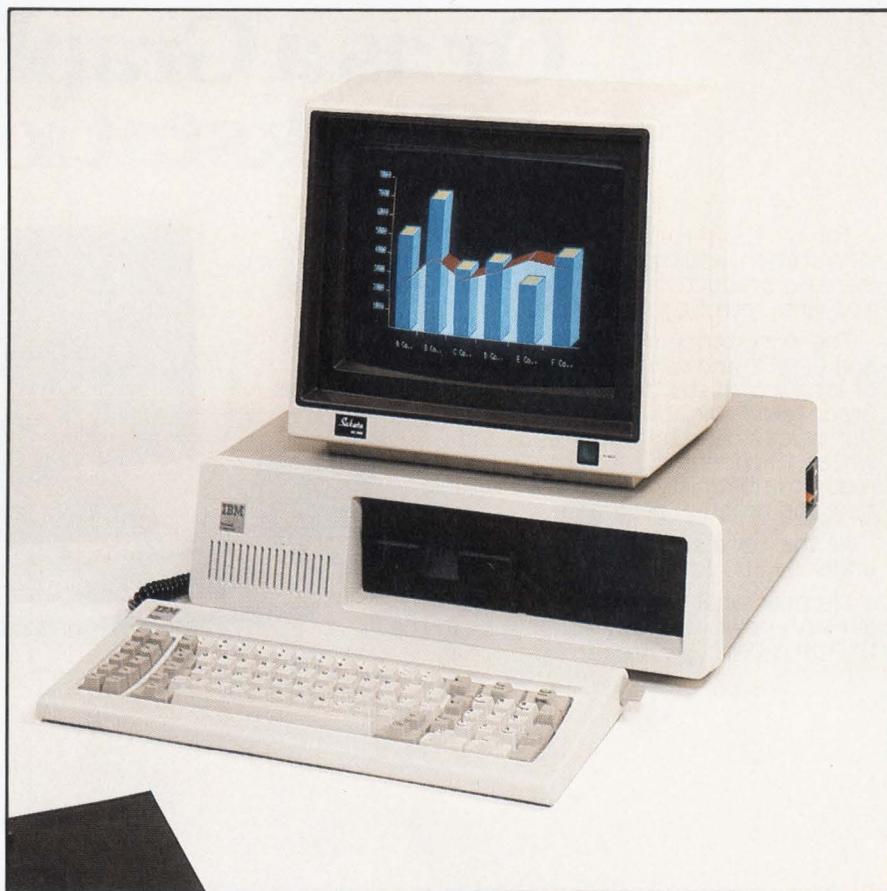
Several products that make the PC or XT emulate IBM terminals were announced at Comdex; emulations of the 3270 and 3278 are available from several sources. These allow the PC to hook into IBM networks as a terminal for database and file access in addition to getting information for the PC to work on locally. Some products, such as the 8-way PC cluster controller from Lantech Systems (Dallas, TX), allow the PC or XT to hook into a network in clusters. This sort of arrangement can economize on cabling and hardware.

The success of products such as Technical Analysis Corp.'s (TAC) Irma and Irmaline products could be indicative of the importance of integrating PCs into IBM networks. TAC merged

with Digital Communications Associates (DCA) this fall, offering a combination of DCA's switched network approach with TAC's hardware and software for IBM PC interface to 3270 controllers for database access.

In a twist on communications for PCs, Intelligent Technologies International (Palo Alto, CA) offers DEC VT 100 or 52 emulation for the PC, with optional SNA. Protocol converters for SNA allow bypassing IBM 3274 cluster controllers or other IBM network interfaces altogether. Even Apple has announced SNA capabilities, in the Lisa SNA; this IBM network compatibility may help Lisa remain popular in the face of the IBM PCs.

No less than nine local area networks that let IBM PCs and XTs share facilities were shown at this fall's Comdex. Orchid Technology (Fremont, CA) was founded in 1982 with a charter to network IBM PCs, with their PCnet. PCnet has also been licensed to three other companies, and enhanced to allow more memory, combined network and floppy controllers on one board, and floppyless operation.



Color monitors for the IBM PC like Sakata's SC-200 allow PC users enhanced display options.

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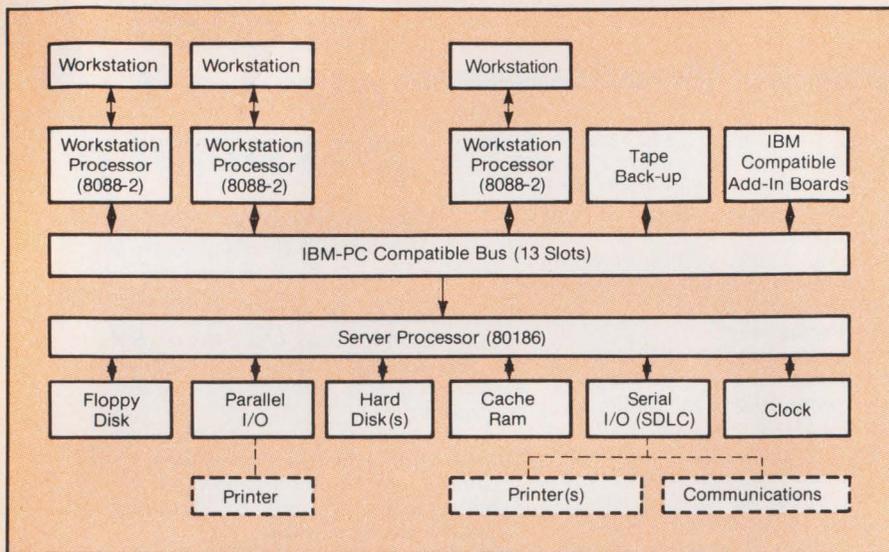


Figure 2: PC/XT compatible Dimension from North Star allows multi-user application without networking through multiple 8088-2 processors on the PC bus and an 80186 server processor for memory, clock and I/O.

LANs for the PC and XT are varied, to allow many configurations and price ranges. Several use the CSMA/CD scheme, from a digitized voice/data Ethernet system from Tecmar (Cleveland, OH) and 3Com's thin coax Ethernet to an Orchid-compatible IDEAnet from IDE Associates (Bedford, MA) to G/NET from Gateway Communications, Inc. (Irvine, CA), that also provides access to SNA networks over shared SDLC links. Prices dropped recently on X-Net, a twisted-pair PC LAN from XComp (San Diego, CA), from \$650 to \$490 per node. Alloy Computer Products (Framingham, MA) and Fox Research (Dayton, OH) also offer networking of PCs over inexpensive twisted pair cable. Should IBM really come forward with the token passing LAN protocol, PerCom (Dallas, TX) and Nestar (Palo Alto, CA), will be in place. PerComNet also has an encryption feature, and Nestar has adapted the popular Datapoint ARCnet system for the PC.

Networking will allow PC users not only to communicate, but also to share resources. With the relatively low price of a personal computer in its unadorned state, a LAN to connect mass memory and a printer to many PCs can provide a good bit of working room to individuals in their offices at minimal cost. As this plethora of network offerings matures, costs will, no doubt, drop, and further gateways into SNA and

other network schemes will make the PC an extremely powerful tool.

Software Expansion

As Apple has proven over the past few years, software availability and variety can make a personal computer. And IBM's openness to third parties' software has helped the PC in the market. With other makers' machines often outperforming the basic PC, software availability is carrying the day in some applications.

For the networking and communications flexibility promised in hardware, software has been developed both for use alone or with these additions. File servers for networks, links to mainframes and to various networking systems have been announced. In the field of IBM terminal emulation, 3270 cluster emulation from vendors such as Polygon (St. Louis, MO) allows networking, and many others offer links and emulation packages. More limited connection is provided by a resource sharing package for four PCs or XT's from IDE.

Networking on all levels has become a most desired feature. Software from Connections, Inc. (W. Bridgewater, MA) for network design now runs on the PC, for low cost modeling and optimizing of network design.

Within a few weeks of the PCjr announcement, several vendors were offering programs for the jr. Programs like the Vanpak from Software Strate-

gies (Eden Prairie, MN) allow the jr to use an XT library, and could expand the range of applications for jr, to make IBM's vision of the executive who uses a PC or XT at work and finishes up on his jr at home, a reality. And since the jr's features are more limited than some of the competition's, with only 128K memory and no display included for a none-too-low price, the jr can surely benefit from all of the compatibility IBM and third parties can offer.

Other software announcements run the gamut from DBMS like GMS' (New York, NY) 10-Base, to word processing, accounting and financial packages to integrated packages like those from Innovative Software (Overland Park, KS), Intelligence (UK) and Excalibur (Albuquerque, NM). Integrated packages, of course, allow ease and flexibility for PC users. META-FILE has been adapted for the PC and XT, from Sensor-Based Systems (Glenview, IL), and like the other integrated software packages, it includes DBMS to make the other functions more powerful.

An indication of how much impact the PC is having on spreading computing to the general public is the success of Cdex Corp. (Los Altos, CA). Cdex boasts of \$5 million in annual sales of *training packages* on how to use the IBM and Apple personal computers. The VisuALL program that allows data entry via USI's OptoMouse is also aimed at the inexperienced user. Maker Trillian Computer Corp. (Los Gatos, CA) feels that using a mouse and windowing techniques, users who cannot type or have no prior experience will have an easier time with computing.

Such considerations are foreign to IBM, the mainframe giant. And that is the reason why their encouragement of outside software development will probably allow the PC to stay on top.

Memory Expansion

Naturally, one of the crucial additions to make a micro powerful enough to perform tasks once reserved for mini or mainframe processing is adding memory. And this business looks large — DILOG (Garden Grove, CA) has even started a manufacturing group, DILOG PC Products, just to make PC peripherals. Their first product was a board-level "Electronic Disk" that

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replaces the PC's floppy with RAM, for faster access especially for multi-user and multi-tasking on PCs.

A variety of 8", 5-1/4" and 3.9" Winchester drives are available externally or to the PC or XT form factor for internal devices. Several compatible drives use caching and many offer faster access times than the standard XT drive. Whether fixed or cartridge, the speed and capacity of Winchester drives on the PC can make it a powerful tool for many applications. Even Control Data is offering a hard drive for the PC.

Many of the networking programs for PCs and XTs are designed so that if one micro in the system has a hard disk and acts as file server for the net, the others can operate in a basic configuration without even floppy storage. So one of the many available drives can be shared, keeping memory costs lower than the main PC hardware.

Adding drives requires adding controllers, as well. And since IBM was out to make reliable machines in very large quantities, neither the controller nor the drive in the XT is "state-of-the-art." This has left room for others to produce faster and more efficient storage equipment. At the very high end, Interphase has introduced Maverick, for 8" SMD interface Winchesters and their controller will allow two 8" or larger disks per PC.

The PC has also attracted a bubble memory board. Helix Laboratories' (San Diego, CA) Bubble Disk emu-

lates a half megabyte Winchester. With bubble technology, memory is nonvolatile and requires no external power. And this sort of sophisticated add-in will expand the range of the "low-tech" IBM PC.

PC Add-Ins/Add-Ons

A host of multi-function boards are available for the PC that combine extra memory with a variety of the functions a basic IBM configuration is short on: parallel printer and serial ports clock/calendar and PAL are available on a few from Tecmar (Solon, OH). Gateway has added an 80186 and RAM in its Supercharger, making the PC a far more powerful machine; Winterhalter uses a Z-80A to let the PC or XT act as a terminal.

A variety of graphics boards are also available to extend the display capabilities of the PC. Although many personal uses do not require more than monochrome displays, the advantages of color are making sweeping changes in the number of color monitors sold. IBM offers a 4-color display, and the XT uses a 16-color monitor as well as monochrome and color adapter boards.

The boards from third parties for 16 colors abound, but the Discortex (Hicksville, NY) color transformer lets the user choose which 16 colors to use from a palette of 262,144. IDE uses the popular NEC 7220 chip for the standard PC monitor. And Quadram's color graphics board provides as many as

136 colors. These color capabilities open up the PC to applications from designing presentation graphics to CAD/CAM, when used with the memory and processor modules coming out.

Better monitors than the standard IBM offerings are also available especially for the PC. And since the PCjr is offered without monitor in its basic package, opportunities for display makers should open up in the home/low-end market, as well.

High resolution (690 x 480 on a 12" screen) monitors, large monitors and non-glare screens are the expected offerings, available from vendors such as Princeton Graphics Systems (Princeton, NJ), Quadram and Sakata (Elk Grove Village, IL). The CIE-7800 is a terminal emulator for the PC from ACM, Inc. (Newport Beach, CA) that provides emulation of five IBM terminals on a PC. And for ease of use and special applications, a sensitive touch-screen monitor is available from start-up Micro-Touch. (Woburn, MA).

The multiple user voice response system from Vynet (Los Gatos, CA) has been adapted for the IBM PC (it was on Apple already). This product should bring the PC into banking and inventory or order entry applications.

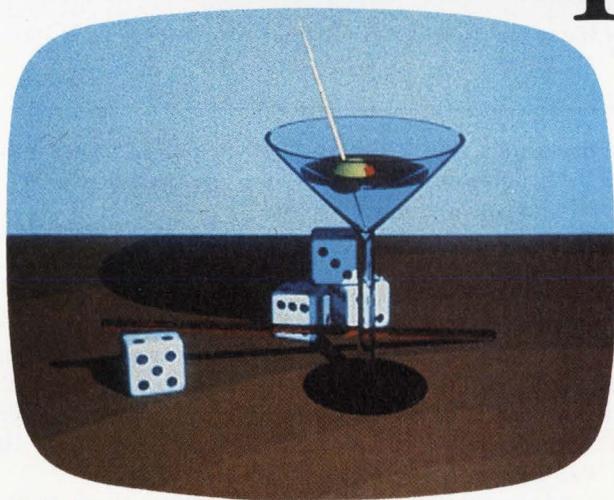
Other peripherals are true powerhouse additions for a personal computer. With a Winchester disk and power supply in addition to 8 expansion slots, the Dynaframe (Santa Ana, CA) allows PC users to reconfigure their system to almost any size; combining several of the board offerings would need not only the extra slots, but also the extra memory of a Winchester.

Comdex was also the first public showing of the first product from PC Technologies (Ann Arbor, MI), the XTender. This package makes the PC/XT into a multi-user computer. Intel 80186 and 80286 processors act as host CPU in the XT for up to five concurrent PCs, terminals or keyboards.

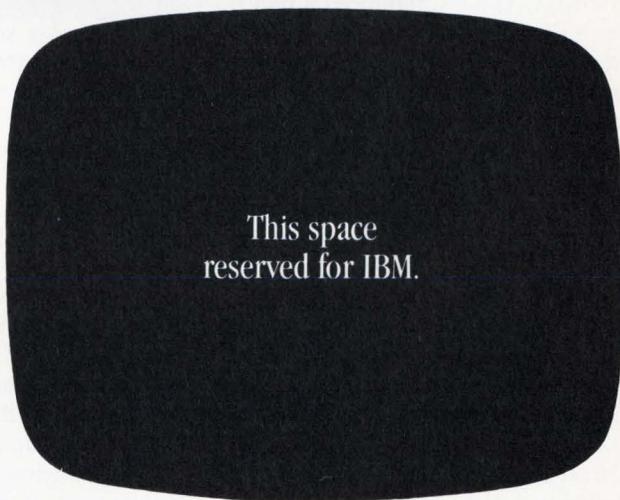


The first SMD rigid disk interface controller board for the PC is Interphase's Maverick SMD PC-80, shown here being inserted into an IBM system.

We were going to compare Vectrix graphics to IBM's. Unfortunately, there is no comparison.



Vectrix VX/XT Graphics

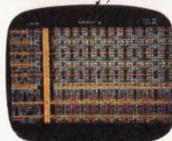


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IBM Compatibility

All of these third party offerings are more or less in the traditional line of IBM-compatible products. Bigger, faster, more sophisticated or newer-technology products have always been available to add into or onto IBM machines. But the giant's entry into personal computers has given "IBM-compatible" a whole new meaning. Now, entire computers claim to be IBM-compatible.

And everyone is getting into the act. In addition to Compaq, Columbia, Eagle, Corona, Chameleon and Hyperion, Tandy, the established personal computer market leader, Apple, is going IBM-compatible. With this sort of variety in compatibles, the PC market can truly be said to have found a standard in the IBM PC.

Fall announcements show that, as with most standards in this industry, many will conform. North Star (San Leandro, CA) has announced a multi-user XT-compatible, the Dimension. Based on the Intel 80186, the system can support 12 users in a cluster, with the attached workstations using an 8088-2 CPU (Figure 2).

Santa Clara Systems (San Jose, CA) is offering a PC with built-in networking capabilities over the Orchid-developed PCnet. And another networking PC compatible is available from Digital Microsystems (Oakland, CA). Their DMS-816 workstation uses 8088 and Z80A processors and hooks into their HiNet LAN. OSMs proprietary Zeus-Net now has an OSM (Mt. View, CA) PC to support.

Other newer PC compatibles include a system from Leading Edge Products (Canton, MA) that operates faster than the IBM, at 7.16 MHz compared to 4.77 MHz and is lower in price, at \$2895. STM Electronics (Menlo Park, CA) uses the Intel 80186 to speed up processing, and their PC includes an integrated 16-line LCD, printer and modem. Panasonic's portable Senior Partner is also made for MS-DOS 2.0 and other IBM software and hardware.

PC Infiltration

The much-feared and inevitable shake-out in personal computers is happening, and introducing IBM-compatible machines or capabilities for existing PCs is probably the best insurance against it. Not only will more IBM-compatible



Winchester disk StorageMaster™ subsystems from Control Data provide 18 or 30 Mbytes of storage to the IBM PC.

micros probably hit the market, but those that claim to be IBM-compatible may have to increase real compatibility. PC DOS and MS DOS programs are now so numerous and varied that personal users will no doubt demand similar choice on their computers.

And the software and hardware enhancements that will put the IBM PC into new, more demanding applications are strengthening that driving force. The PC is now being used as an engineer not only for office functions and networking between executive offices, but for data acquisition, database access and even CAD/CAM applications. The strength of a PC with third-party and IBM additions and upgrades in nearly unlimited.

Especially important to remember is that the cost of a PC, especially when used in a resource sharing environment of clustered or networked micros with common mass storage and other peripherals, is not high. Distribution of computing power is now possible on a scale ranging from tiny enterprises to the very largest corporations. Firms entering into computerization for the first time will almost certainly see the great flexibility that having personal processing power affords. And all of the products now on the market to link PCs

to each other and to more powerful processors gives the PC a new dimension.

Accessing more powerful machines will, no doubt, always be a big priority for microcomputers in industrial and office environments. Once the realm of minis or mainframes and the terminals and workstations powered by them, industrial automation control and design are now hot areas for PCs —IBMs, compatibles and others.

The trend for larger firms to choose the IBM model may well continue. But the wealth of features and advantages of the compatibles, especially with additions, should keep many of them healthy on the market. Further standardization to IBM specs may take place in the compatibles, to take full advantage of the overwhelming third-party support and enhancement products. □

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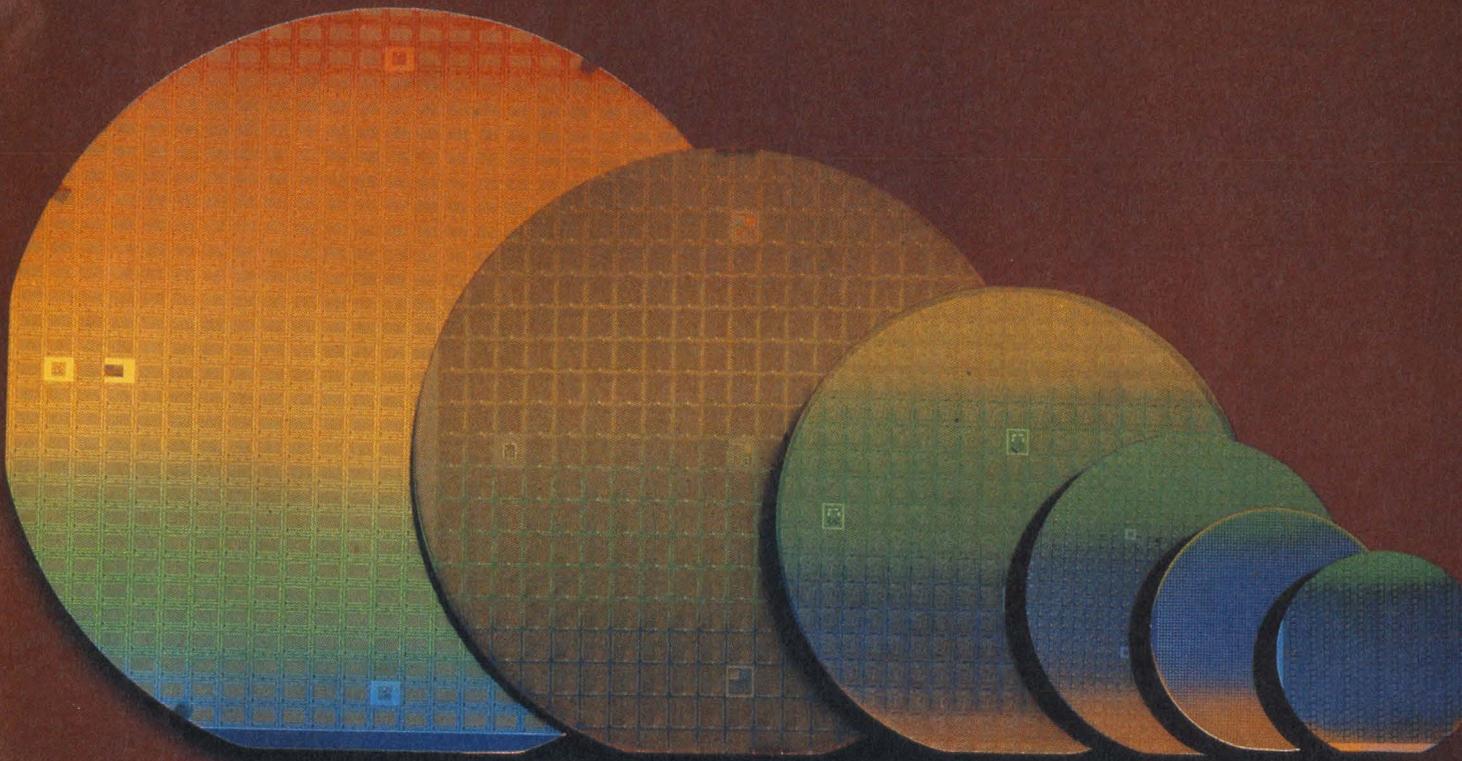
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Integrated Circuits: Advanced μ P Designs Will Rely On OS Support

(Photo courtesy National Semiconductor)

by **Dave Wilson,**
Senior Technical Editor

Today's computer designer can choose from three basic categories of products to implement his system. These consist of dedicated general purpose devices, fuse programmable logic, and full custom Integrated Circuits. Each of these alternatives offers distinct advantages and disadvantages in terms of cost, availability and architectural flexibility. Many designs incorporate all three of the design approaches to some degree. One, Data Systems Design's Multibus board, uses PAL for a state machine, a gate array for error correction, and standard products, such as a DMA controller and an 8085 μ P.

Design decisions relating to choice of technology, however, may become less clear over the next year. At the present time, PAL is widely used to implement control functions, such as state machines, whereas the gate array may be used for data path applications such as EDC, that call for a larger number of gates.

But in the PAL arena, this year will see a whole range of new products, some of which may challenge the gate array for some sockets. Monolithic Memories, who currently hold about 70% of the market share, plans to introduce CMOS and ECL parts, as well as two SUPERPALs — a 40- and an 84-pin part.

As more functions go on chips, the problem of test becomes greater. Sys-

tem diagnostics on a chip is another area that MMI has pioneered with its 16K registered PROMs with on-chip diagnostics in most minicomputers, disk drives, terminals, I/O parts, and μ P-based systems.

For its part, Advanced Micro Devices is promoting the concept of variable output architecture. The AmPAL 22VIO incorporates the unique capability of defining and programming the architecture of each output on an individual basis. Each output is user programmable for either registered or combinational operation, allowing the designer to optimize the device design by having only as many registers as necessary. Upon an increased volume demand, the system designer may find it advantageous to

*The role of
programmable,
semi-custom and
custom logic will
find increasing use
in the design of
advanced computer
systems.*

switch to HAL (Hard Array Logic), which is a metal mask option of the PAL, but lower in price for larger volumes. If future design alterations are necessary, the internal structure of the PAL can be changed while maintaining identical pin-outs, thus being immune to PC board alterations. Designing using PAL has been greatly simplified by the use of two software tools, PALASM and PLEASM. PALASM is the key software tool for designing with PALs and PLEASM is its counterpart for designing with PROMs as Programmable Logic Elements. Using Boolean equations to simplify logic definition, PALASM and PLEASM translate the Boolean equations into working prototypes. Together with a PROM programmer, the software programs and a computer become a logic development workstation for breadboarding of PAL and PLE designs.

Inevitably, the idea of using the IBM PC as the basic computer for μ P-based design tools has become a reality. At Wescon last year, Valley Data Sciences announced its I60 series programmable logic workstation that provides user support for designing with programmable logic devices. The personal computer provides an environment for the execution of development software that is available to run on I60-series systems.

Placing more tools in the designer's hands is also a plan of George Stephan's at Universal Semiconductor. Conventionally, a gate array designer may have gone through several procedures

(such as circuit design, verification, and specification) before the design was passed off to USI for schematic conversion and capture. By use of an IBM PC, the engineer can now work on circuit design, schematic capture and specification documentation at his desk, downloading the design information via modem to the gate array manufacturers VAX where logic and circuit simulation, test vector generation and fault simulation can be carried out. Eliminating the breadboarding phase may cause some consternation among many designers at first, but the right software will help immeasurably to overcome the worry.

As in the PAL business, the density of gate arrays continues to climb. Applied Micro Circuits, for example, recently announced that it has expanded its family of bipolar gate arrays to give system designers an increased density of as many as 1500 gates and increased I/O capacity. AMCC's Q1500 arrays are second sourced by Signetics and are included in the technology exchange agreement

the two companies announced in September. Many designers today are currently using gate array technology to reduce the number of standard TTL parts in their product. Interestingly, the huge demand for TTL (with delivery dates being quoted up to 50 weeks) has pushed some manufacturers into gate array technology, where the design time and turnaround on a product may be less than the delivery times for TTL. Functional cell design is a more recent development in the semi-custom area. A cell library of RAM, ROM, μ P, and I/O cells are stored in a design system, and mixed and matched to the designers requirements. This area has already attracted interest from keyboard, mice, and cable decoder manufacturers — users of high volumes of μ Ps that can risk the up-front design costs that may be in the order of \$100,000 on the chance that they may save millions.

American Microcircuits Inc. was one of the first IC houses to promote the concept several years back, but their choice of the unpopular TI 9900 family of 16-bit machines, coupled with their

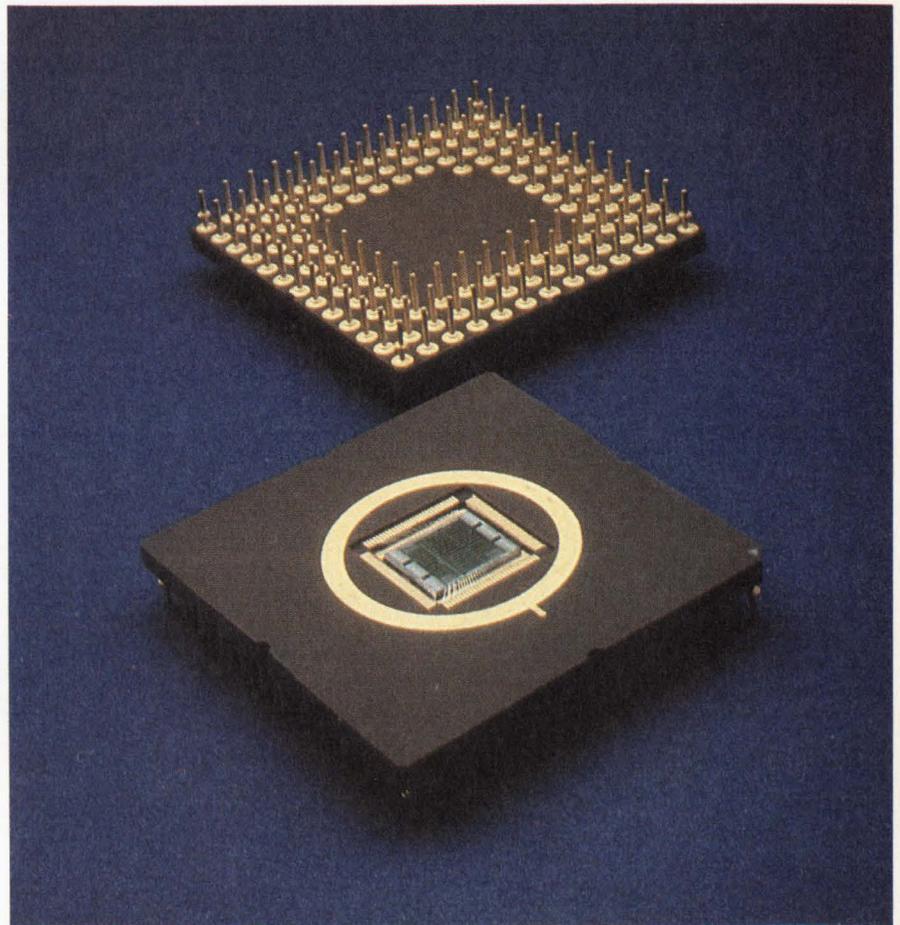


Photo courtesy National Semiconductor.

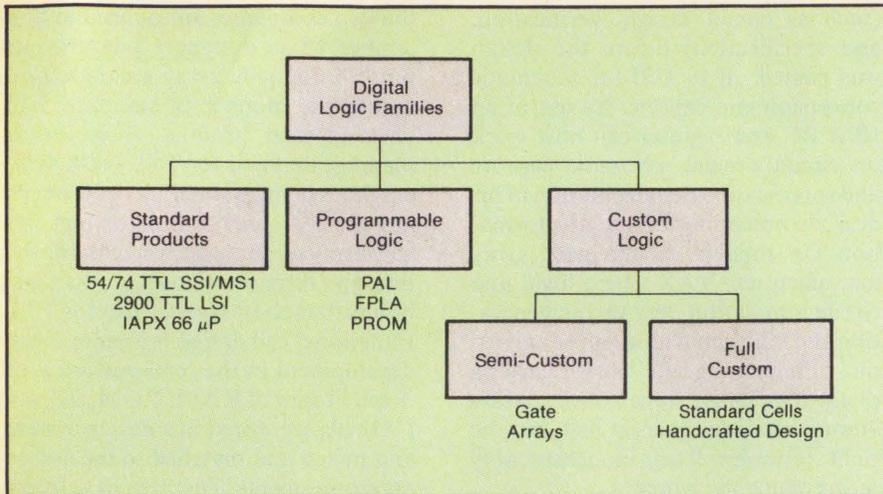


Figure 1: Basic categories of digital logic.

n-channel technology, was (to say the least) not what most designers were looking for. Today, they are currently working on an agreement with Zilog for the use of the Z80 8-bit μ P as a core building block. Since Intel and Motorola dominate the 8-bit μ P market it is hardly surprising that both companies also are in the standard cell business. Intel's 8049 and 8051 and Motorola's 6805 family are two very popular μ Ps in the industry today; in fact, getting hold of an 8049 from a distributor is almost an impossible task. Originally faced with the same problem as AMD, Zymos

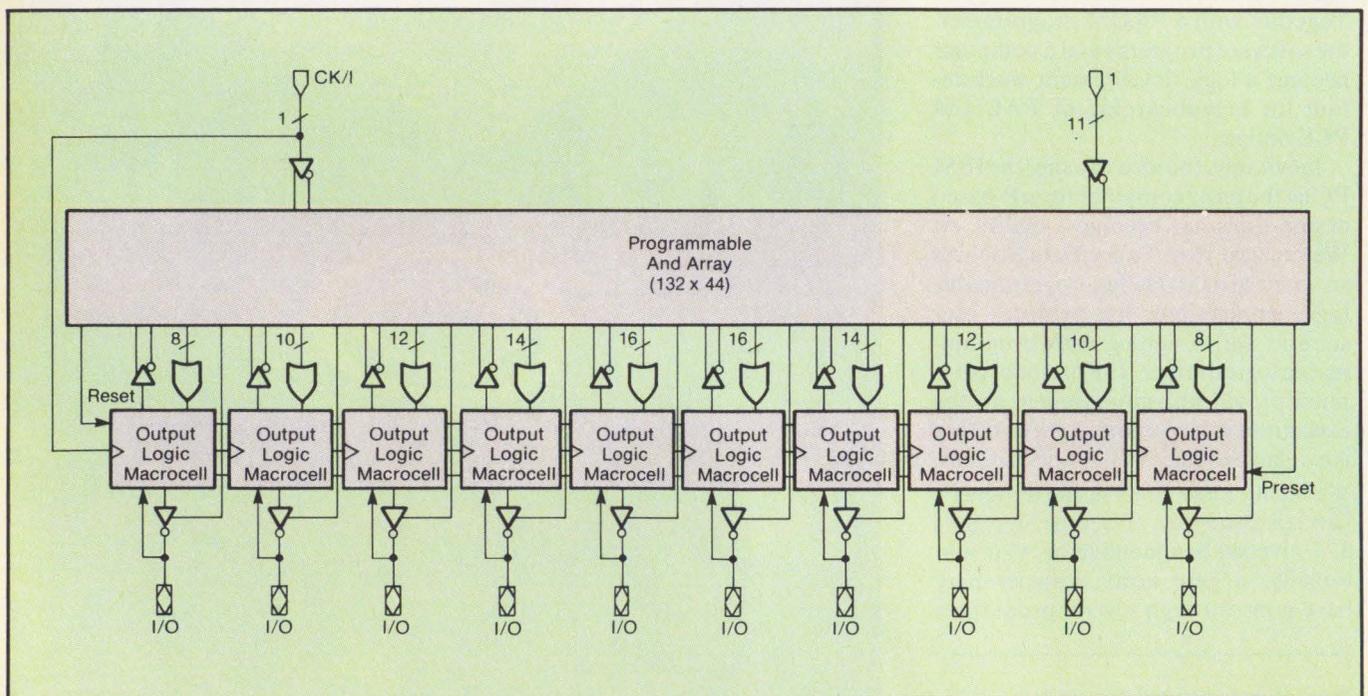
started out with their own ZyCOMP-4 μ P that proved unpopular due to its unfamiliar instruction set. Today, the company offers the Intel 80C49 as a core with a 3μ process which Intel second sources.

One of the problems faced by standard cell vendors is that, although their cell libraries may be large, inevitably many designers will find some functions missing, and resort to designing their own. Gate array designs will complement, rather than compete with the standard cell industry. LSI Logic is one company that has recognized that as devices increase in density, the designer will need both LSI building blocks like RAM, ROM, PLAs and a gate array

section. "We'll probably have something to talk about in that area," says Will Corrigan, President of the company, "It will be close to fully automated full custom and the silicon usage penalty will be minor." In the past, a full custom approach with all its benefits of smaller chip size, increased reliability and less power consumption, may have appeared too complicated, and too risky, and system level designers may have restricted themselves to gate arrays or standard cells. However, a new design methodology called "cell compilers" may offer a simple solution to the design approach and short design cycle together with incorporating the flexibility and other benefits associated with the full custom approach.

According to Robert Duyn, at VLSI Technology (San Jose, CA), cell compilers are similar to standard cells in that each cell represents a pre-designed function, and the user selects a function from a cell library. Each cell compiler represents a generic, user configurable function. However, since it is software that describes the function, parameters can be specified to alter what the software ultimately generates. Cells can be changed in terms of performance, number of inputs and outputs, I/O locations and in some cases even the basic func-

Figure 2: AMD's PAL 22V10.



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LL5000	880-6000	3 micron double layer	2.5	YES	YES
LL7000	970-10,000	2 micron double layer	1.4	YES	YES

*2 input NAND, FO = 2, T_A = 25°C, V_{DD} = 5V

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LSI LOGIC CORPORATION

Transputer Eliminates Von Neumann Bottlenecks

In the past, system performance has increased regularly by a factor of ten each decade. This improvement has been achieved by advances in circuit technology and by increasingly complex systems. For the future, VLSI offers the potential of much greater circuit complexity but only modest increases in circuit performance.

The economics of current systems are based on the historical perspective that processing is expensive in comparison with memory. This has led to the von Neumann bottleneck where a single processor is connected to vast amounts of memory. The economics of VLSI are different. Today, a single wafer of silicon can contain 2 Mbytes of memory or 256 conventional microprocessors.

To exploit this potential it will be necessary to build systems with a much higher degree of concurrency than is currently possible. The Inmos (Colorado Springs, CO) transputer is designed as a programmable component to implement such systems. The term 'transputer' reflects this new device's ability to be used as a system building block. The word is derived from 'transistor' and 'computer', since the transputer is both a computer on a chip and a silicon component like a transistor.

The power of the transputer is that it creates a new level of abstraction. Just as the use of logic gates and Boolean algebra provides the design methodology for present electronic systems, so the transputer, together with the formal rules of occam, provides the design methodology for future concurrent systems.

In their proposals to achieve intelligent interaction between people and computers, the Japanese have projected the need for computers with one thousand times the performance of present day systems. These will only be possible using concurrency, and the transputer has been designed to make such fifth generation systems a reality.

Pipelines and arrays of transputers can be used to pro-

vide greatly increased performance by exploiting the concurrency inherent in many applications. Two examples which require high performance are signal processing and database searching. Networks of transputers can provide the performance needed for both applications.

Signal processing, such as the fast fourier transform (FFT) algorithm, maps easily onto a pipeline. The pipeline can accept input samples at up to 100kHz, which more than covers the full audio spectrum. A 64 point FFT requires six transputers in the pipeline, a 256 point FFT require eight and a 1024 point FFT requires ten transputers. A pair of pipelines, interlinked at each stage, is able to accept input samples at up to 200 kHz. Higher frequencies can be handled by using more transputers in parallel.

A pipeline or an array can also be used for searching. Provided that the search request can diffuse through the network, and the answers converge, the shape of the network does not matter—it can even contain faulty devices. The full internal memory of each transputer can be searched 1000 times per second. With external memory attached to each transputer the search rate is slower, but 64 Kbytes per transputer can be searched at least 30 times per second.

Other applications, such as image processing, finite element analysis (as used in weather forecasting), matrix manipulation, telephone switching systems, fault tolerant systems and artificial intelligence naturally lend themselves to arrays or networks of transputers.

Applications apparently less directly suitable have also been found to benefit from multi transputer systems. As an example of a compiler, an occam compiler, written in occam, can use a pipeline of processes. As an example of a large scientific program, the INMOS logic simulator can achieve performance proportional to the number of transputers used.

Write 300

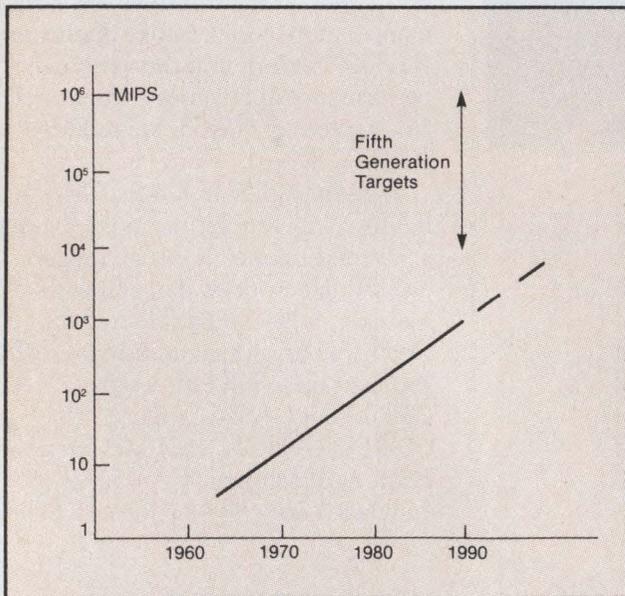


Figure 1: Conventional system throughput.

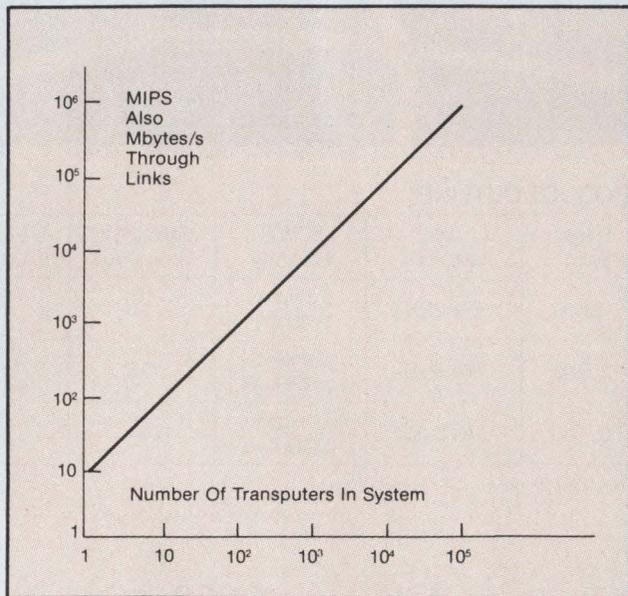
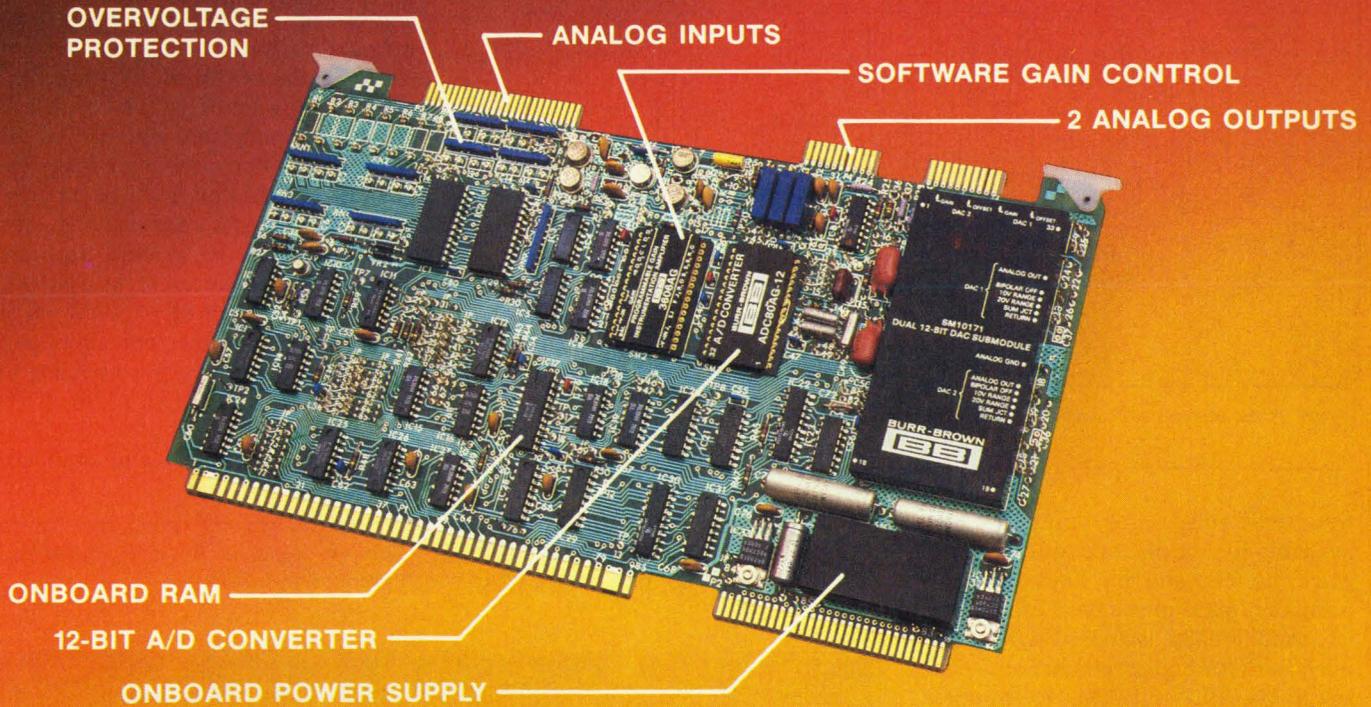


Figure 2: Transputer system throughput.

How To Handle 127 Channels of 10mV to 10V Analog Inputs With Minimum Space/Cost!



If your analog input signals range from 10mV to 10V; if you have to input up to 127 channels; if you must isolate some of those channels—the MP8418 family of Multibus™-compatible analog I/O peripherals offers a cost effective solution!

MP8418 is the basic I/O board: it's 12-bit accurate and provides resistor or eleven software programmable gains ranging from 1 to 1024 V/V. When your host converts a channel by reading a memory location, the MP8418's onboard RAM sets the amplifier gain for that channel—transparent to host and operator! Analog inputs have overvoltage protection to 26VDC and up to fifteen 4–20mA inputs can be accepted. The input section has MUX, amplifier, S/H and 12-bit ADC. Optional analog output adds two DACs and control logic. DC/DC converters are included in all models.

MP8418-EXP: Used with the basic MP8418; differential input capacity is increased from 15 to 63 channels; single-ended input capacity from 31 to 127 channels.

MP8418-ISOE: Use up to three with MP8418 to gain an additional 48 *isolated* analog channels. The basic MP8418's 15 channels are non-isolated CMOS multiplexed inputs.

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For specifications on these three I/O peripherals call or write:

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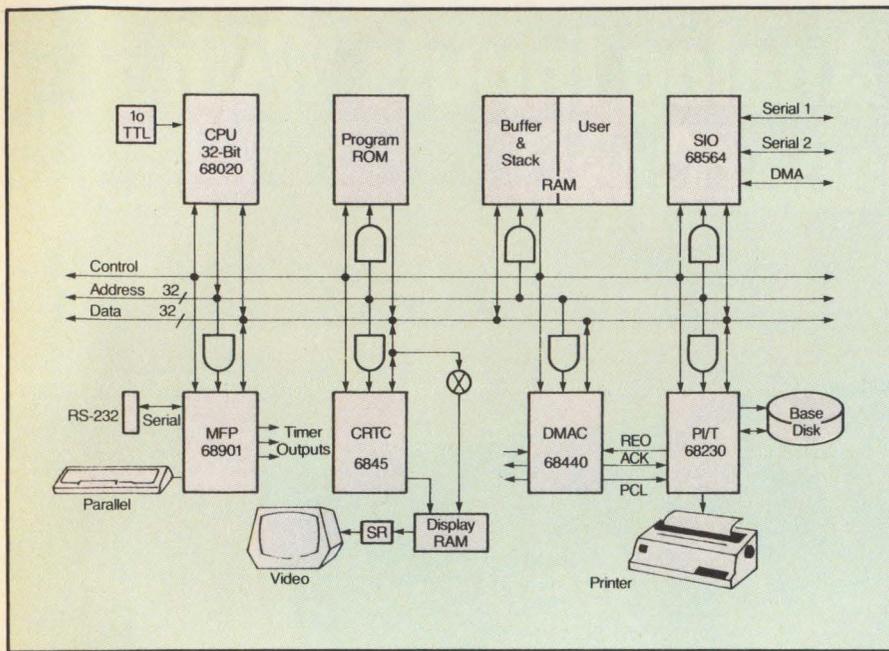


Figure 3: An engineering workstation using the 68020.

tion represented. Cell compilers are available for simple functions, such as gates, buffers, and flip-flops that are normally found in standard cell libraries. Additionally, standard cell compilers exist for high level functions such as ALUs, PLAs, RAM, ROM and comparators.

The added flexibility that the previous design solutions provide will become increasingly important over the next few years as designers are faced with implementing what many are calling "fifth generation" machines. The end of the fourth generation may arrive with the implementation of full 32-bit machines, such as National Semiconductor's NS32032, Motorola's 68020, Intel's iAPx386 and Zilog's Z80,000. It is extremely unlikely that these manufacturers will see the need to go to a 64-bit μ P since the exceptionally large addressing range of 4 Gbytes will prove enough for the majority of market needs. Already in the 16-bit computer marketplace, many OEMs like Charles River Data are touting their product against DEC's VAX line. The arrival of 32-bit μ Ps will heat up that market even more, and the next step seems evident - 32-bit workstations networked to a shared database.

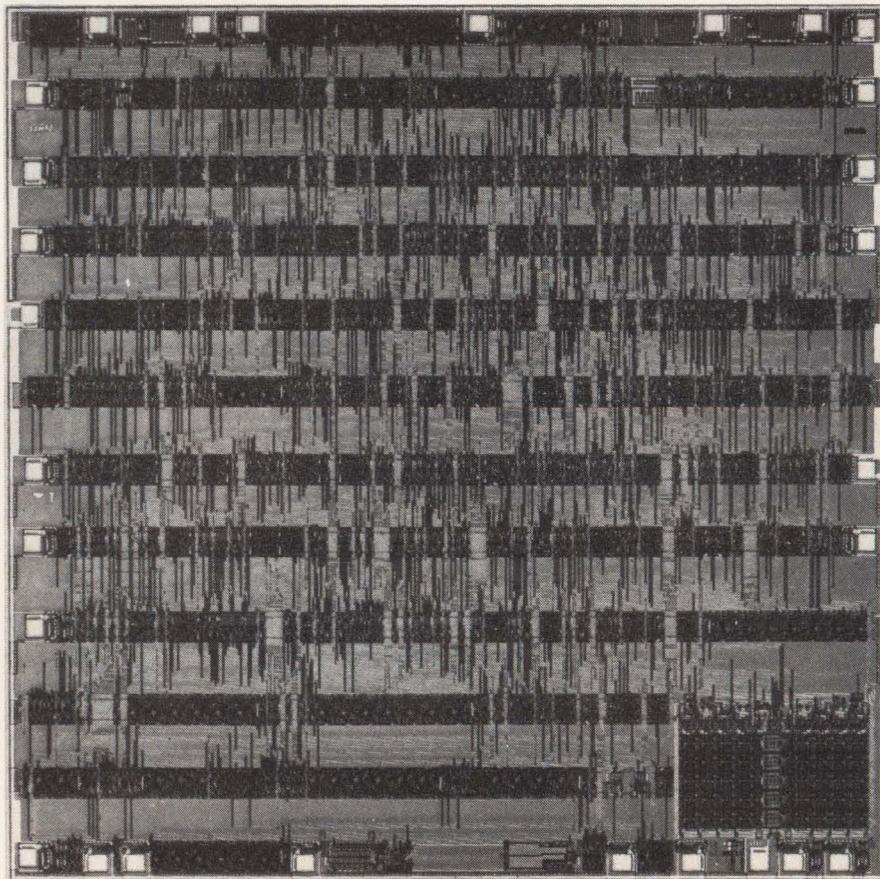
One question that is often asked about 32-bit, μ Ps relates to the portability of software. According to Thomas

Starnes, Product Manager at Motorola, the new 68020 has no such problems. Code written for any of the other

68000 μ Ps will run identically on the 68020. Some of the original 68000 instructions have additional flexibility but all of the original capabilities are maintained. New addressing modes, for instance, fit some of the unused bit patterns of the original instructions. This has the additional benefit of extending the concept of universal application of addressing modes to categories of instructions. National's approach is similar to Motorola's, their 08/016 and 032 are also software compatible with one another. Coming this year will be the NS16C032. With the speed of the XMOS part, the power will be cut drastically. A single chip version, the NS16010, will arrive in 1985. Software compatible with the rest of the NS16000 family, it will include 8K of ROM, 1K of RAM and many interrupt, timer and I/O oriented features. Also coming in 1985 will be the NS32132, a 32-bit CPU with on-board MMU.

Software portability and on-board

Figure 4: Custom IC with imbedded RAM (courtesy Zymos).



MMU is also a feature of the Z80,000 μ P from Zilog, providing significant performance increases over current 16-bit designs. A migration path to Zilog's 32-bit machine is today available with the Z8003 and Z8015 PMMU system components.

By use of other specialized ICs, like floating-point units, the designer may increase the speed of his system even further. These units usually fall into two categories, the co-processor or the slave processor unit. The co-processor method was the first to be used. Here, the main CPU and the co-processor operate independently and in parallel. With the slave processor approach the CPU does the decoding and sends out the required information to the slave processor. It then waits for the result. To the programmer, the slave processor instructions look part of the regular instruction set—in National's part, all regular addressing modes, sources, destinations can be used.

With MMU's already on-board 32-bit machines, it is only a matter of time

before floating point units are integrated on-chip as well. At present, the Z80,000 can support up to 4 8070 co-processors. All FPU instructions have a tag field associated with them that indicate which FPU they are to be executed on. This sort of approach is extremely useful when building fail safe systems, where 2 FPUs may be instructed to execute the same instruction and the result compared. It may be that the next generation 32-bit CPU's incorporate not only one but many FPU's.

Extending this concept further, it is possible to envision four 16-bit μ Ps on a single die tailored to handle concurrent processing. Unfortunately, many IC houses are at present caught between a rock and a hard place due to the non-availability of operating systems and compilers that will support such advanced processing schemes.

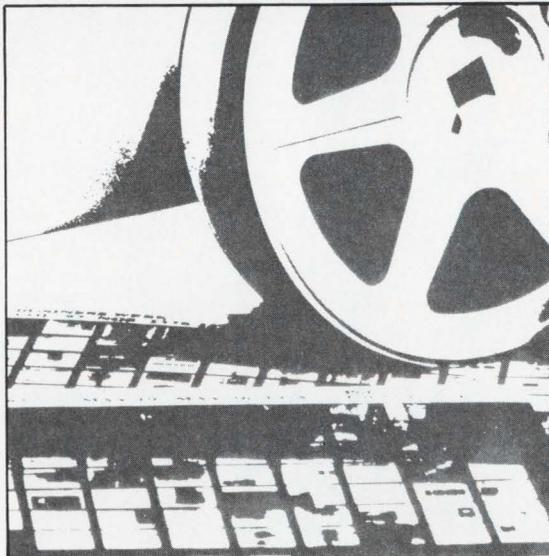
According to Col. Rada at National Semiconductor, the software will now dictate what the hardware will look like and not the other way around. In one respect he may be right. The supermicro-

computer market today appears to be making UNIX the standard O/S. The UNIX supporters strongly endorse the movement to standard operating systems, the use of high-level languages wherever possible, and the flexibility that this will offer to the marketplace. UNIX opponents rightly criticize the age of the O/S, its inability to support concurrent processing, and its suitability to the μ P world at all. Those vendors, such as Inmos (Colorado Springs, CO) with its Transputer and Occam programming language and Multisolutions (Lawrenceville, NJ) with its S1 operating system are two companies that are doing something about the situation.

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Peripheral Interfaces Lower Cost And Boost OEM Performance

by Dave Wison, Sr. Technical Editor

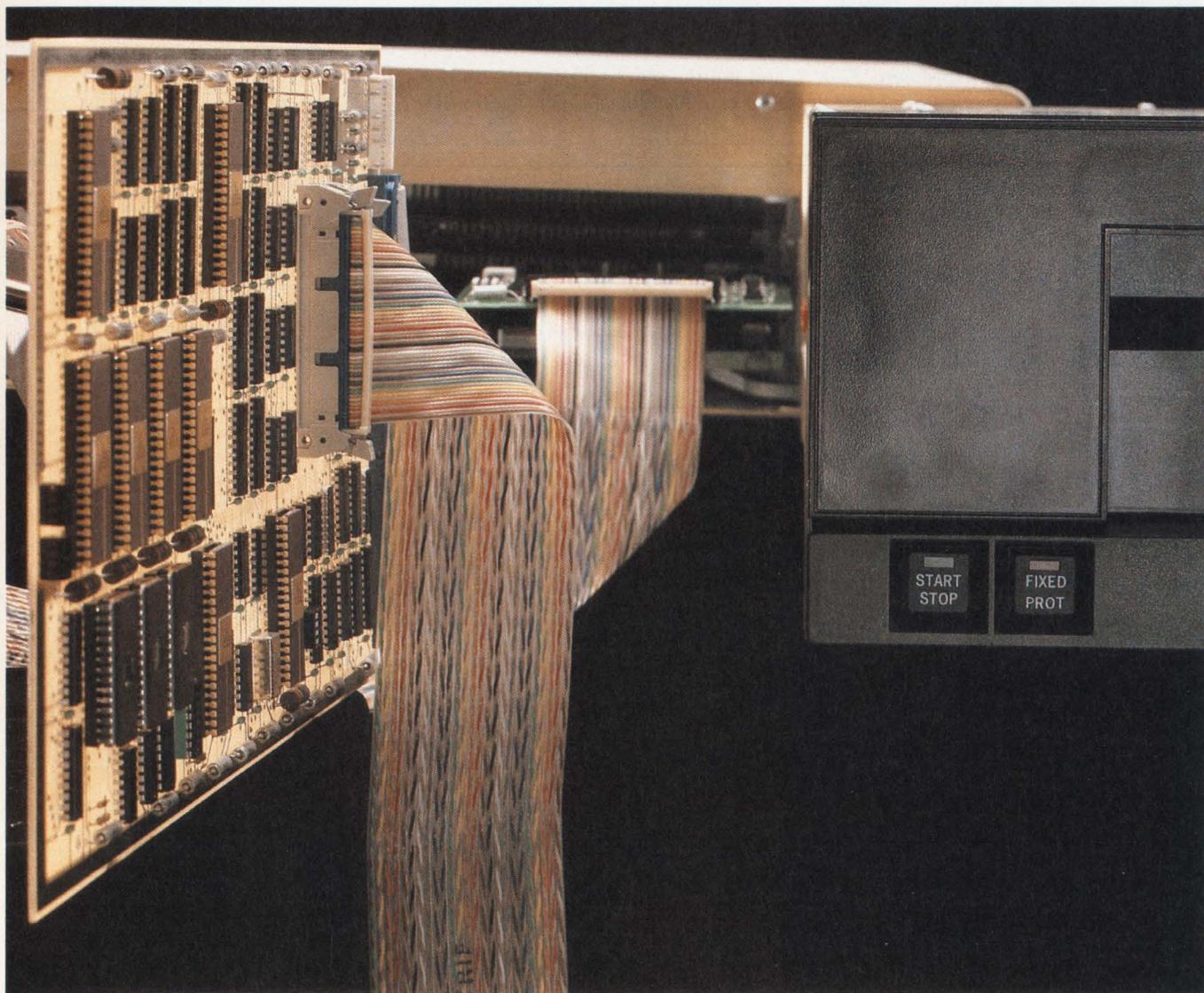
The decreasing cost of VLSI devices has resulted in the ability of peripheral manufacturers to add increasing intelligence to their equipment.

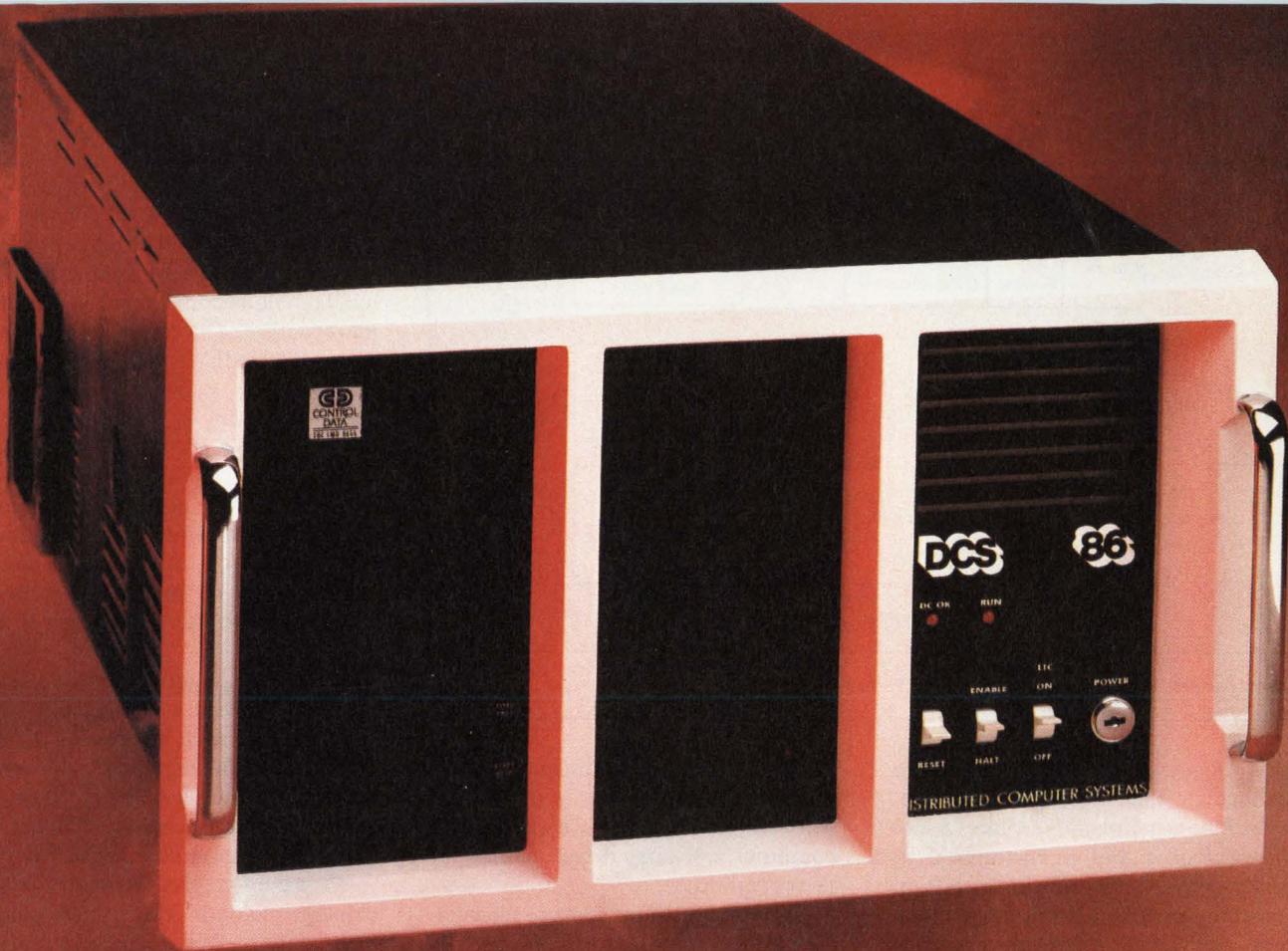
In the days of discrete transistors, the only functions that were contained within the disk were the basic functions of seek and read/write. Today's disks, however, now include addressing and data recovery functions. The controllers contain all the other functions.

As more intelligence moves onto peripherals, the role of the controller is one of a simple CPU adaptor.

In the future, even more functionality will move onto the disk, leaving the role of the controller as one of a simple CPU adaptor (**Figure 1**).

High performance disk drives typically use the SMD interface supported by a disk controller specifically designed to support these kinds of drives. Sim-





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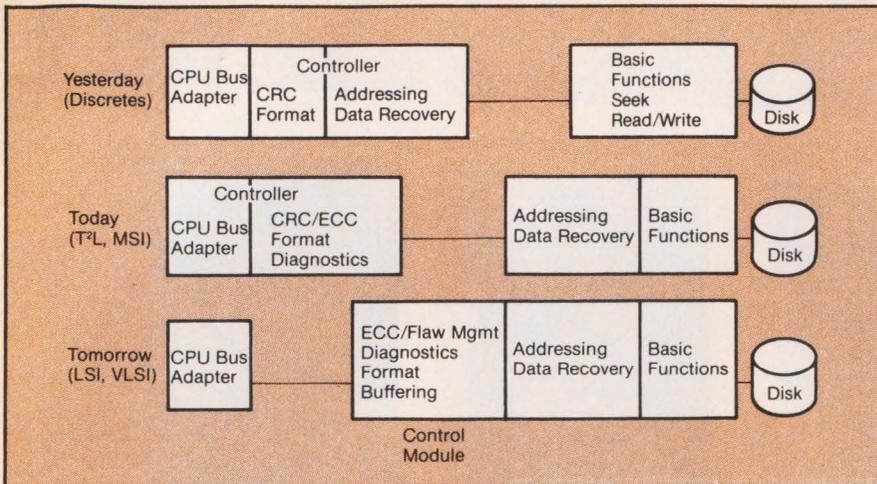


Figure 1: Disk control functions—a history of packaging.

ilarly, mag-tape drives use a Pertec interface or the Centronics interface. Each of these peripherals requires a specific controller that is customized to handle the peripheral in question. Upcoming peripherals will move much of the intelligence into various peripherals as shown (Figure 2). The host adaptor then becomes common to all the peripherals. Each of the four host adaptors shown are identical to each other, and the four peripherals shown can be supported by a single host adaptor.

Looking one step further into the host computer itself, a common set of peripheral software supports all of these

intelligent peripherals. Instead of having disk driver software, mag tape driver software, etc., the interface will permit a common software driver called the peripheral driver.

Figure 3 illustrates some of the interface terminology involved in interconnecting a peripheral with the host bus or backplane. In the middle is the systems interface, that may be the ISI, IPI or other system level interfaces. Note that the system level interface is independent of both the host and the peripheral. This is important because as systems continue to be designed with faster microprocessors, disk vendors are driving up the areal density of their product to provide more cost effective peripherals. These two developments need to occur independent of each other so that product improvements in both areas in the

future do not obsolete interfaces and give the designer cause for concern with the changing geometry of disk products.

As areal densities increase, flaw-free media will become more difficult to manufacture. The control module analyses the media, finds the flaws and manages the string of data around them. The aim is to make the disk appear to the CPU as perfect media.

In addition, the control module can perform effective correction if an error occurs in the reading of data through some transient problem. The control module converts many soft errors to good data and the CPU receives only correct data.

Advanced diagnostics ensure that a peripheral device is functioning properly. Should a fault be detected the control module can diagnose and localize it, reducing the time and cost of repair. The ISI also offers predictive maintenance. The control module analyses the performance of a peripheral device and catalogs the data. The control module also catalogs all error correction operations it performs. The data can then be analysed and used to predict potential failures before they happen, even though the peripheral may be functioning within its design specifications. The ISI is a high performance interface that can support up to eight control modules in a daisy chain. Each control module can address up to four slave devices (Figure 4).

The host electrical interface is common, and all communications with the control module are done by exchanging blocks of information. All control

Photo page 98: Control Data's 9050 Control Module for the ISI interface.

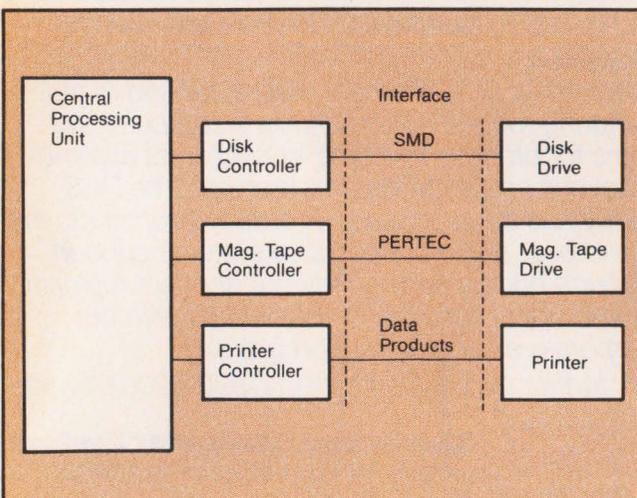


Figure 2a: Today's peripheral interfaces.

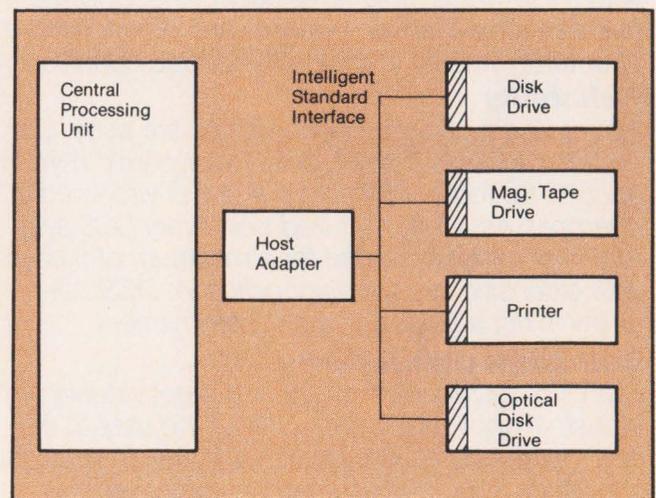


Figure 2b: Tomorrow's common interface.

A man in a dark pinstriped suit and glasses is leaning over a black briefcase. The briefcase is open and overflowing with US dollar bills. He is looking towards a large sign that reads "ON ALLOCATION". In the background, a large sign for "LS INC" is visible, with the letters "LS" being significantly larger than "INC".

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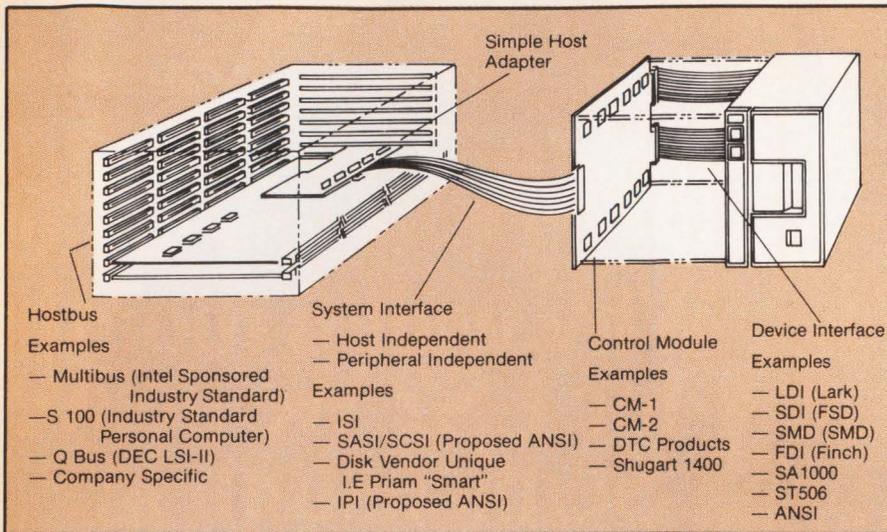


Figure 3: Interface terminology.

modules support the command and status block protocols. Although differences in performance occur in the con-

trol modules, they can all connect to the same adaptor and perform the same basic seek, write, read and format com-

mands with minimum changes to the host adaptor or the host software. The differences that occur affect the functionality of the control modules and allow variances in the level of performance in the users subsystem to fit the application. Drive operations start with a control module selection process. The host adaptor activates the select-hold line (**Figure 5**) and sends a unit select address over the bus (using sync-in and sync-out exchanges for handshaking). The selected control module then responds to the select sequence by activating the select-active line. Both control lines then remain active throughout the entire selection process to ensure

Burst Error Correction Made Easy

Mass store systems based on magnetic media are getting larger, denser, and faster and burst error processors such as the AM9521 are pushing the limits of these media yet retaining acceptable levels of performance.

Usually, the controller in a mass store subsystem will contain enough workspace, buffers and computational power to perform error correction. With the AM9521, the hardware interface is simple, but the software and micro-

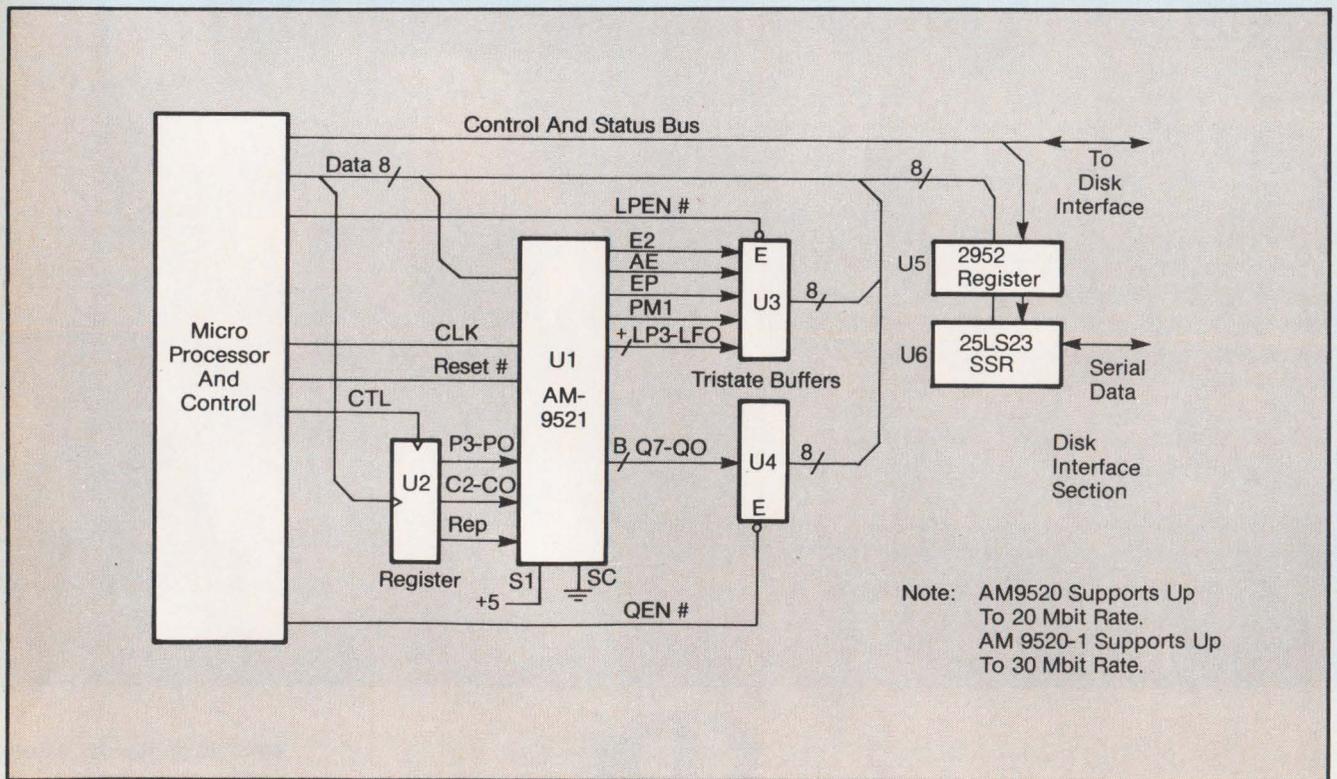


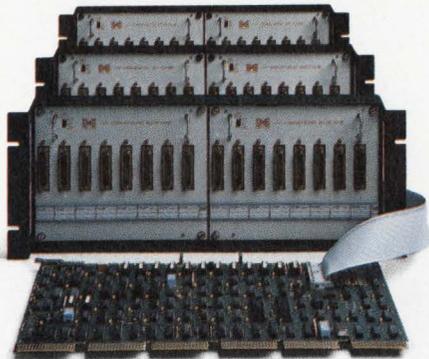
Figure 1: AM 9521 application diagram.

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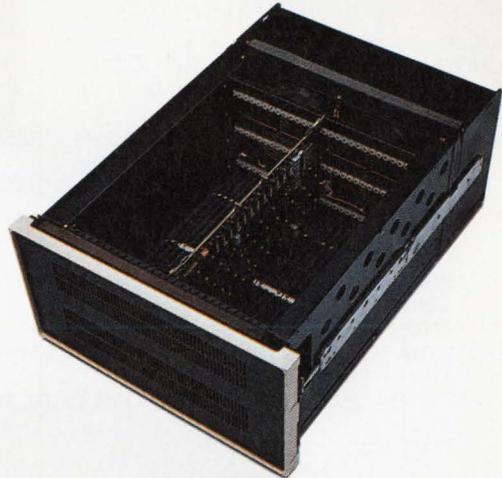
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Emulex's new DMF-32 emulation is typical. One controller board handles up to 64 lines, vs. only eight per DEC module. And Emulex offers *all* lines with modem control, not just two. For even more lines, Emulex's Statcon Series is the answer. We simply add a low-cost port concentrator, so that with one controller board you can connect up to 256 remote *and* local terminals.



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For instance, a DEC DH11 controller lists at \$8,950 per 16 lines, with expansion chassis costing \$3,000 or more. Compare that to Emulex's CS11/H at \$4,500 for the first 16 lines and \$3,000 for each additional 16 lines. At 64 lines, you suddenly have savings of about \$23,000 and a lot of extra slots to boot.



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```

VAR
  I:INTEGER; (* 16 BIT COUNTER *)
  D:ARRAY [0..255] OF BYTE; (* DATA *)
(* PSEUDO OP_WAIT (ARG1) IS SHOWN FOR TIMING. DELAY
ARG1 NANOSECONDS MINIMUM *)
(* NUMBERS DECIMAL UNLESS APPENDED B FOR
BINARY *)
BEGIN
  CLK:=1;
  FUNCTION SELECT:=000B; (* C2,C1, C0 *)
  POLY_SHIFT:=000 0B; (* PC, P2, P1, P0 *)
  REP:=0B;
  RESET:=0; WAIT (800); RESET:=1; WAIT (250); (*RESET
CHIP *)
  FOR I:=0 TO 511 DO BEGIN (*WRITE DATA TO DISK *)
    DATA:=D[I] (ENABLE D[I] TO DATA *)
    WAIT (200);
    CLK:=0;
    WAIT (200); (* ALSO CLOCK DATA INTO U5 *)
    CLK:=1
    END;
  FUNCTION_SELECT:=001B; (* WRITE CHECK BITS *)
  QEN*:=0; (* ENABLE Q TO DATA *)
  FOR I:= 0 TO 4 DO BEGIN (* WRITE CORR. CODE TO
DISK *)
    WAIT (200)

    CLK:=0;
    WAIT (200); (* ALSO CLOCK DATA INTO U5 *)
    CLK:=1
    END
  END; (* BLOCK IS NOW ON DISK *)

```

Table 1: PROCEDURE WRITE BLOCK

```

PROCEDURE READ BLOCK
VAR
  I: INTEGER;
  D: ARRAY [0..516] OF BYTE
BEGIN
  CLK:=1;
  POLY_SHIFT:=000B; REP:=0B;
  FUNCTION_SELECT:=011B; (* READ HIGH
SPEED *)
  RESET:=0; WAIT(800); RESET:=1; WAIT(250);
  ENABLE_2952_TO_DATA BUS;
  FOR I:=0 to 516 DO BEGIN
    LATCH_DATA; (* DATA FROM DISK *)
    WAIT (180);
    CLK:=0; (* ALSO WRITE DATA TO D [I] *)
    WAIT (180);
    CLK:=1;
    END;
  (* NOW DATA AND ERROR CODE ARE IN
MEMORY *)
  DISABLE_2952_TO_DATABUS;
  WAIT(200);
  IF ER=0 THEN EXIT (READ_BLOCK) (* NO
ERROR *)
  ELSE CORRECT_BURST_ERROR
  END; (* PROCEDURE READ_BLOCK *)

```

Table 2: THE READ PROCESS

sequence control is more complicated.

In this note, we give the algorithms for reading, writing,

```

VAR
  R1,R2,R3: 1 BYTE INTEGERS;
  M1,M2: 2 BYTE INTEGERS;
  K,F1,F2: 5 BYTE INTEGERS;
  DATA_BIT:ARRAY[0..(517*8) OF BITS;
BEGIN
  FUNCTION_CODE:=111B; (* CORRECT HIGH
SPEED *)
  POLY_SHIFT:=0001B;
  REP:=0B;
  R1:=R2:=0;
  WHILE (EP=0) DO BEGIN
    IF AE=0 THEN R1:=R1+1
      ELSE R2:=R2+1;

    CLK:=0;
    WAIT (450);
    CLK:=1;
    IF ((R1+R2)>23) THEN ABORT
      (NON_CORRECTABLE)
    END
    (* WE NOW HAVE R1,R2 *)
    M1:=(8*R1)+R2;
    F1:=M1*4095;
    POLY_SHIFT:=0010B;
    M2:=0;
    WHILE (PM2=0) DO BEGIN
      M2:=M2+1;
      IF (M2>4095) THEN ABORT
        (NON_CORRECTABLE);
      CLK:=0;
      WAIT (450);
      CLK:=1;
      WAIT (450);
      END
    (* WE NOW HAVE M2 *)
    F2:=M2*720,728;
    F1:=F1+F2+5;
    WHILE (F1>94185) DO BEGIN
      K:=K+1;
      F1:=F1-94185
      END
    (* F1 NOW POINTS TO FIRST BIT IN ERROR —
BIT # IS ((517*8)-6)-F1 *)

    REP:=1;
    WAIT (150);
    R1:=(Q7.Q0);
    R2:=(LP3..LP0); (* LEFT JUSTIFIED IN REGISTER *)
    BURST_START:=517*8-6-F1;
    FOR I:=0 TO 11 DO BEGIN
      DATA_BIT[BURST_START +I]:=
      DATA_BIT[BURST_START +I] XOR (BIT7(R1));
      R1:=R1+R1; (* SHIFT LEFT *)
      IF (I=7) THEN R1:=R2;
      END
    END; (* PROCEDURE CORRECT BURST_ERROR *)

```

Table 3: PROCEDURE CORRECT_BURST_ERROR

and correcting data. The algorithms have been tested in an actual design. What is given here would suffice for an engineer to implement burst error correction in a disk controller. In this example, 12 bit correction is used with a 35 bit polynomial over 512 bytes of data. Twelve bit correction is the longest burst length supported by the 9521. The process descriptions are given in pseudo code and include timing details.

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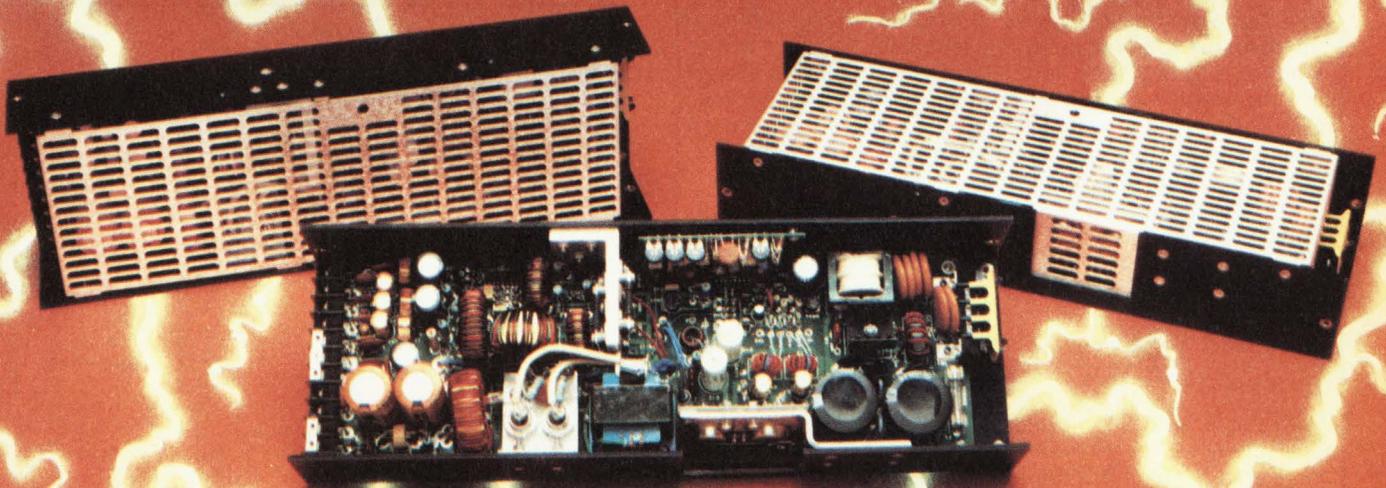
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MASS 300-3	5V,25A (30A PK)	15V,4A (6A PK)	-15V,4A (6A PK)	24V,4A (6A PK)	—
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MASS 300-5	5V,25A (30A PK)	12V,4A (6A PK)	-12V,4A (6A PK)	28V,4A (6A PK)	—
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Hardware Design

The hardware implementation is the easy part of the overall design (**Figure 1**). Register U2 is required for controlling the AM9521. Tri-State buffers (U3, U4) are used to read status information or output correction code bytes for writing to the disk. The procedures to read, write, and correct data follow. Usually a microprocessor will initiate these procedures. The engineer may use PAL microsequencers to perform tight loops or form short pulses where the microprocessor is not fast enough.

The Write Process

When writing a data block, first the 512 byte block is clocked into the AM9521 as it is being written to the disk, then 5 correction code bytes from the outputs of the 9521 (Q7-Q0) are written to the disk. The 5 Bytes can later be used to correct read errors. The algorithm used in this example can correct up to 12 bit errors.

Table 1 is a Pseudocode procedure for writing out a block with a block check code appended. Procedure WRITE BLOCK shows how to program all pins of the 9521. Timing information is specified in the argument field of Pseudo-operation WAIT().

The Read Process

To read data and check for errors, (**Table 2**) first the 9521 is setup and reset. Then 517 bytes are read in and clocked into the 9521. Each byte is latched from the incoming shift register, written to RAM and clocked into the 9521. The FOR loop in the pseudocode example illustrates this.

After reading all of the data, the ER lead on the 9521 is checked. If this is low (=0) then there is no error. If ER is high, an error has occurred and the CORRECT BURST ERROR procedure is used to perform error correction.

The Correction Procedure

The correction procedure is only invoked if there is an error detected while reading data (ER = 1 in the read procedure). Variables are required of varying lengths as is shown in the Var area of Procedure Correct Burst Error. (**Table 3**) These are the maximum lengths required for signed integers. Determining the error position and forming the error pattern requires two loops which monitor EP and PM2 respectively, while clocking the device.

The bit position is determined for the first bit in error in a burst, then the error mask which is read out of the device is exclusive, -or'ed with the burst to form corrected data. If the error is non-correctable, as will be determined when attempting to refine the error in the two loops monitoring EP and PM2, a re-read may be attempted.

Conclusion

With the AM9521 it is possible to implement burst error correction with a minimum amount of effort. The tables have shown how this is done in a practical design. Pseudocode is useful in describing procedures such as reading, writing, and error correction. Pseudocode covers software, firmware and hardware sequencing and brings the benefits of structure to this type of design.

—Robert E. Anderson
Advanced Micro Devices
Ottawa, Canada

—Barry Pelley
Mitel Corporation
Ottawa, Canada

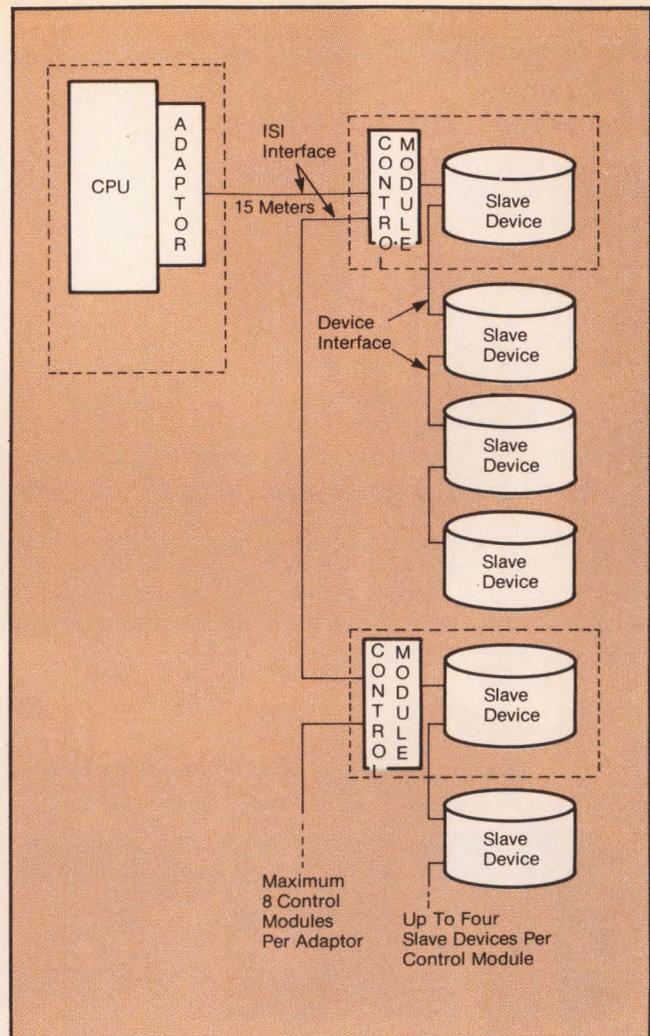


Figure 4: Configuring the ISI.

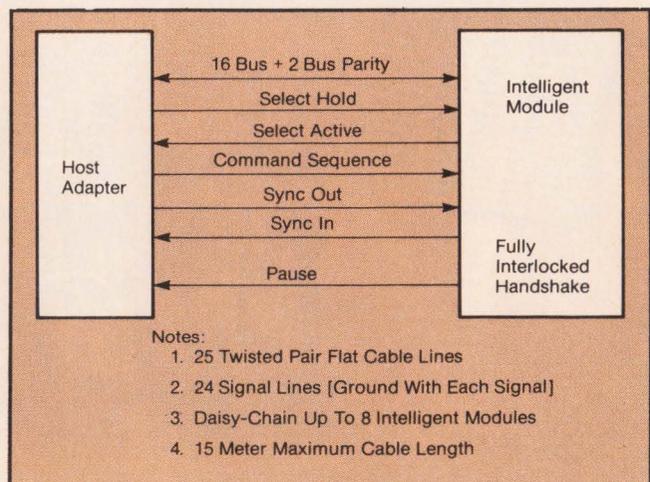
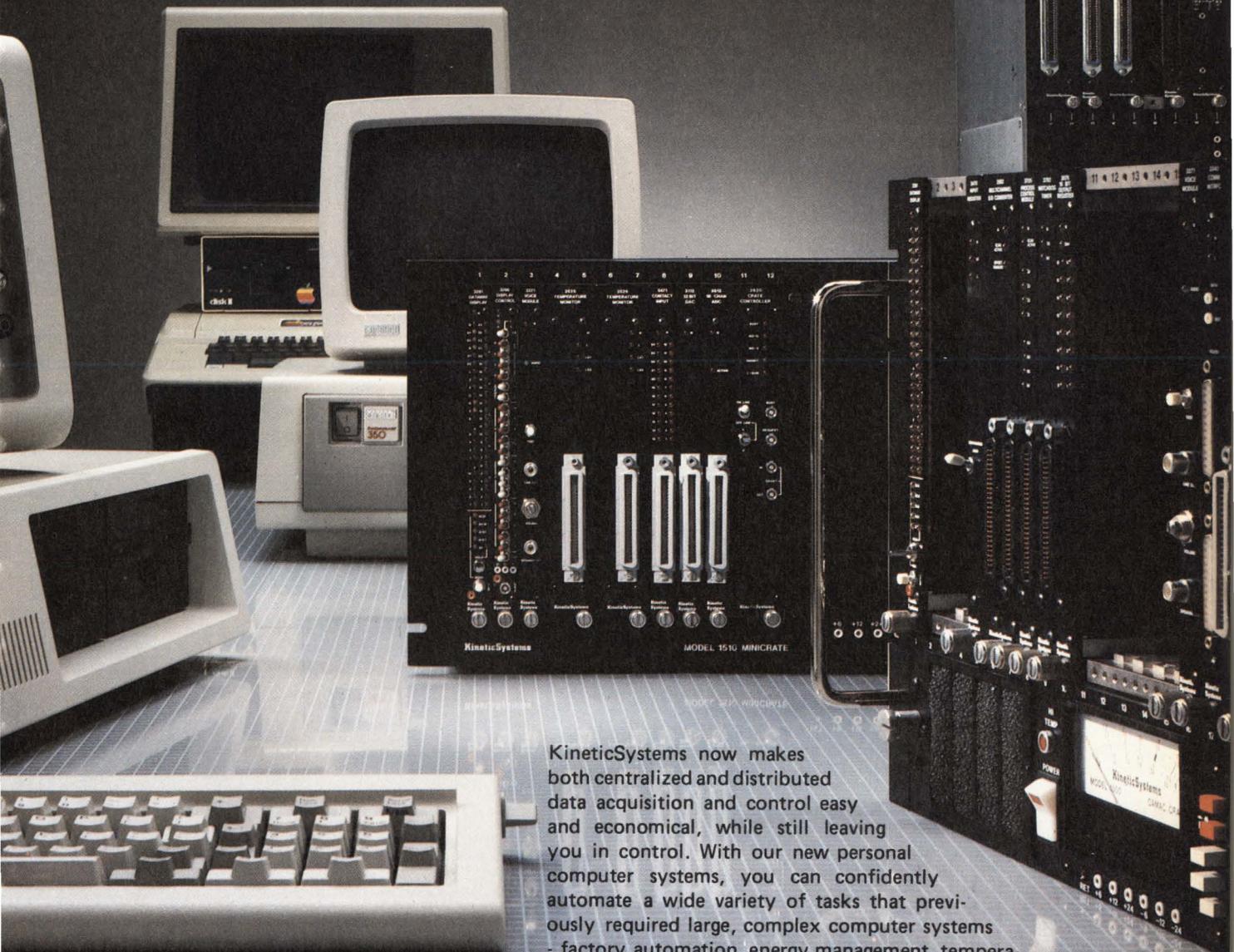


Figure 5: ISI I/O interface signals.

interface integrity. As part of the select sequence, an optional bit-significant responds to verify that unit selected is possible.

When the ISI is otherwise idle, con-

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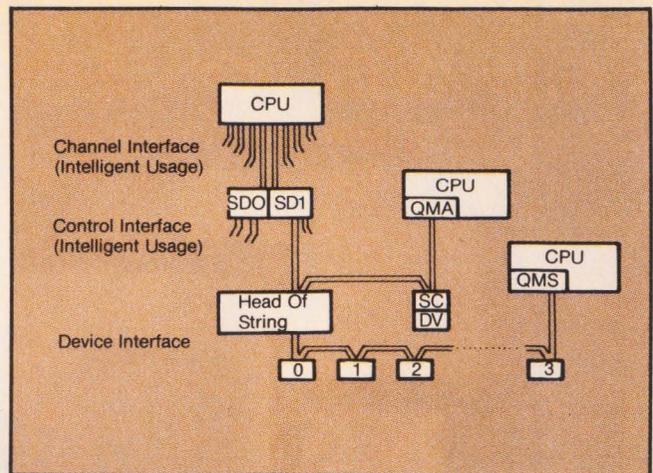
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trol modules may enable bit-significant bus or attention bus lines enabling the host to determine the activity of all control modules without running polling routines. The host activates the command-sequence line to define the beginning of a new function and de-activates the line when that function should cease, either temporarily or permanently.

ISI protocol defines the first bus transfer after command-sequence activation to be a single 16-bit function word. The function code specifies bus direction and the type of information to be transferred. Messages include command, status or data block transfers. They may be as small as one 16-bit word or as large as the total storage capacity of a logical disk drive. After the message block is specified by the function word, each sync-in or sync-out exchange will transfer one word of the message across

Figure 6: Configuration flexibility of the IPI.



the bus. To minimize the hardware needed to support these transfers, the command and status blocks are designed so that the adaptor can use the host computers DMA channel for transfers

between the ISI bus and the main memory. Eight command blocks can be sent to a control module, one at a time, or all at once. ISI allows commands to address up to eight logical slaves on

Interface	Max Data Rate (Mbit/sec)	Max Distance (ft.) Control Data	# Cables	Daisy Chaining Supported (Yes/No)	# Drives	# Hosts	Data Path Width (Bits)	# Conductors Control Data	Data Recovery in Drive (Yes/No)	Dagnostic Support (Yes/No)	Comments		
System Interfaces													
SCSI (4)	10	20 50 (OPT)	NA	1	Y	8 TOT	8	50	NA	Y	Y	Proposed ANSI STD	
ISI	20	50	NA	1	Y	8	1	16	50	NA	Y	Y	
IPI	20(1)	10 (OPT) 15 (OPT) 50 (OPT) 400 (OPT)	NA	1	Y	8	1	8/16	50	NA	Y	Y	Proposed ANSI STD Command Structure not Defined
LDDI (5)	50	3000	NA	1	Y	16 (3)	16 (3)	1	2	NA	Y	Y	Proposed ANSI STD For Local Distribution
Device Interfaces													
SMD	9.67(1)	75	50	2	Control Only (6)	8	1	1	56	26	Y	N (2)	
SDI (Long)	24	100	100	2	Y	8	1	1	50	20	Y	Y	Planned Product
SDI (Short)	16	25	25	2	Y	8	1	1	40	24	Y	Y	Not Planned
LDI	16	10	10	2	Y	2	1	1	40	26	Y	Y	
FDI	16	25	10	2	Y	4	1	1	50		Y	N	
SA 4000	5	25	10	2	Y	4	1	1	50		Y/N	N	
SA 1000	5	25	10	2	Y	4	1	1	50		N	N	
ST 506	5	10	10	2	Y	4	1	1	34		N	N	
ANSI 1226	10	10	NA	1	Y	8	1	1	50	NA	Y	Y	ANSI STD

(1) 40 with synchronous transfer
 (2) Supported on SMD-1 I/O
 (3) Higher at shorter distances logically 256
 (4) SCSI—small computer systems interface—Formerly SASI
 (5) LDDI—local data distribution interface

Figure 7: Characteristics of various interfaces.

each control module. Multiple blocks can be used, for example, to queue disk commands and to overlap seeks.

The command block defines the command to be executed, the device number and address. To verify a control module's receipt of a command block, the host may perform a wrap operation; that is, immediately read back the control module's command blocks. This function is used for detecting programming errors and operating system faults. The control module uses the device status block to make device specific information available to the host. Like command blocks, device status blocks can be sent in sequences of up to eight blocks. There are also smaller blocks that can report attention delay status, revision level status and device operating mode status.

In the years since the ISI concept was launched, several companies have offered products that use the adaptor/control function concept. Peripheral manufacturers included Micropolis, Priam, Shugart and Kennedy. The best known application of the concept has evolved from the products Shugart and Data Technology Corporation offered for the SA1000 in 1980. Shugart has promoted the original interface and several proposed generations of it as the Shugart Associates System Interface (SASI). ANSI has a version of SASI called the Small Computer System Interface (SCSI). This interface will seriously challenge proposed SASI changes in the battle to replace the original interface found on DTC and Shugart 1400 series controllers.

All of these alternatives utilize an 8-bit bus type protocol over a ribbon-type cable. The original version was designed to use one adaptor for each controller—no daisy-chaining of controllers on an adaptor was provided. Newer versions of the original protocol have added features like multiple controllers daisy-chained on the cable and even multiple CPUs daisy-chained on the cable. There is even some talk of a 16-bit bus version. Whichever interface finally wins the race to replace the original SASI will probably control a major portion of the lower performance market for systems based on 8-bit microprocessors. The American National Standards Institute has for over two years struggled with selecting one of the proposed interfaces as their standard. Currently, ANSI is working on its own 16-bit version called IPI.

The SCSI can coexist with the IPI because both use a structured, modular approach to implementation and are oriented for use in new systems applications where there is no need for compatibility with existing software and hardware. Equivalence between SCSI and IPI configurations can be obtained by using an SCSI-like logical interface command repertoire.

An SCSI complex could be configured with one node dedicated to high performance disk activity that uses IPI interfaces to the disks. The operating system software in such a complex would be almost totally unaware that it was operating with two different physical interfaces except at the I/O dispatcher level. When a vendor has to configure systems where multiple levels of interface must be supported, it is possible to use the same physical interface as device, control and channel (Figure 6) with the only difference being the command repertoires at each. It is even more likely that the same physical interface will be used with more than one level of logical interface capability. As

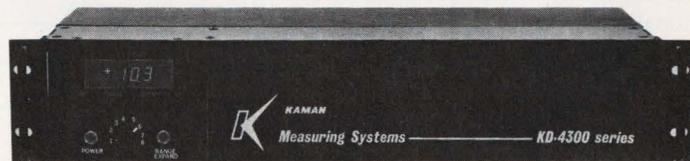
new peripherals and software are introduced, the command repertoire can grow to suit higher levels of functionality. Figure 7 highlights the characteristics of various interfaces that are available or currently being standardized by the ANSI committee.

Realistically, the adoption of a 'standard' is more often than not governed by the availability of product in the commercial environment than by esoteric technical nuances between different proposals. If this is the case, then Control Data's ISI has gotten off to a good start over the IPI. Control Data already produces two Control modules for the bus, the 9050 and the 9056 and will be announcing two more (for tape and optical disk) in the near future. □

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High-Performance Event Interface For A Microcomputer

As silicon technology advances to provide denser geometries, timer structures have become more elegant and powerful.

by Lionel Smith, Intel Corp.

Microcontrollers are microprocessors specially configured to monitor and control mechanisms and processes rather than manipulate data. The systems they are imbedded in are often called real time control systems; microcontrollers always incorporate some form of timer structure to allow synchronization with the outside or 'real' world. As silicon technology advances to provide denser geometries, these structures have become more elegant and powerful.

This trend can be seen in the Intel 8048, the Motorola 6801, and the Intel 8051 which were introduced at approximately two and a half year intervals starting in 1976. The 8048 has a single 8-bit timer; the 6801 has a 16-bit timer, and the 8051 has two 16-bit timers. The new 16-bit microcontroller from Intel, the 8096, has an independent High Speed I/O subsystem which provides the functionality of four to eight 16-bit timers. While this subsystem is designed to provide an integrated approach to measuring and controlling time modulated signals, it is easier to describe as separate input and output units.

Lionel Smith is a Staff Applications Engineer in the Microcontroller Operations Division of Intel Corporation, Chandler, Arizona. During his eight years with Intel Corp., Mr. Smith participated in the definition of the Intel 8051 and 8096 microcontroller architectures. He is also the author of several application notes on microcontrollers.

High Speed Input Unit

The purpose of the High Speed Input unit is to allow the measurement of the periods of incoming pulse or frequency modulated inputs with high resolution and minimal software overhead. A block diagram of the hardware used to accomplish this goal is shown in **Figure 1**. The heart of this unit is a programmable change detector which monitors the four I/O pins of the 8096 which are designated as "High Speed Inputs" (HSI.0-HSI.3).

The operating mode of the change detector is controlled by a byte register which can be written as register 3 of the onboard register file. This register has the predeclared name HSLMODE in the 8096 assembly language. The register contains a separate field for each of

the four HSI pins. There are two bits in each of these fields and they are encoded as follows:

- 00 Capture every eighth positive transition
- 01 Capture positive transitions only
- 10 Capture negative transitions only
- 11 Capture both positive and negative transitions

It is also possible to disconnect one or more of the HSI pins from the change detector by writing into one of the two I/O control registers. This register, known to the assembly language as IOCO is addressed as register 15H of the on-board register file. HSI pins that

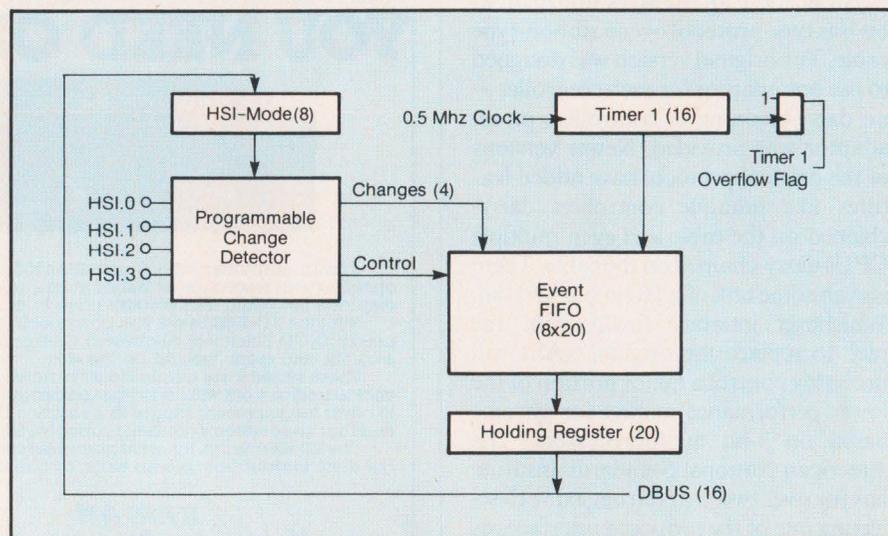
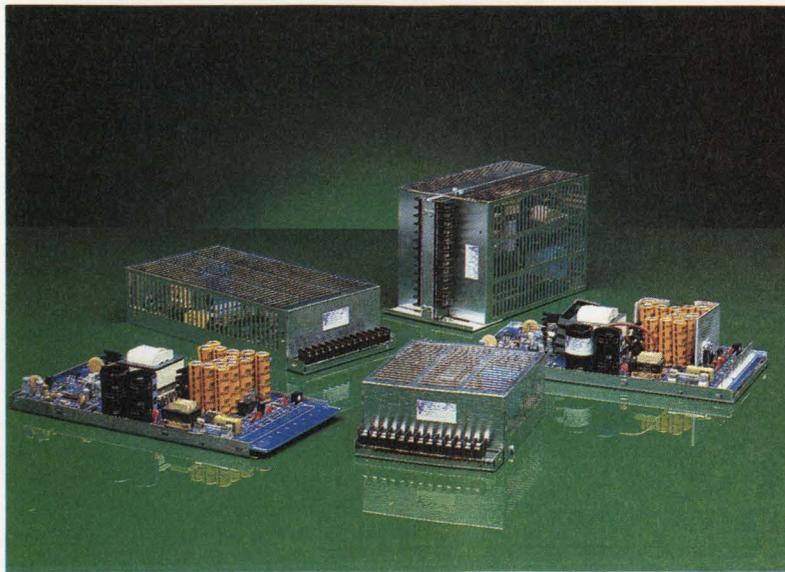


Figure 1: Diagram shows the High-Speed Input Unit which is used to measure incoming pulse or frequency modulated inputs.

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Rx FOR HEALTH

INSTALLMENT THREE



By Lawrence Lee, MD

Dr. Lee is a leading Southern California Internist, specializing in cardiology. He is a co-founder and board chairman of LH Research, Inc. This column is presented as a public service for better understanding of topical medical problems and possible solutions.

HERPES!

SIMPLEX TYPE 2 VIRUS

In our last column we discussed HERPES SIMPLEX 1, which occurs primarily above the waist.

HERPES SIMPLEX 2 (HSV-2) infects people primarily below the waist, usually in the genital areas (penus, vulva, cervix). HSV-2 is frequently acquired during close contact between infected and susceptible individuals during the sexually active periods of life. The incubation period is the same as for HSV-1; from as little as two days to two weeks. The pathogenic mechanisms are the same for HSV-1 and HSV-2. There are three basic phases:

- (1) **Primary Initial Infection**—Virus enters through the mucocutaneous surface (skin or mucous membrane), giving rise to characteristic clusters of vesicles (small blisters), and commonly associated with fever, local lymph node enlargement, pain on urination, tired feeling and local and/or radiating pain to thigh or buttock area. The vesicles will normally remain up to two weeks.
- (2) **Latent Infection**—After initial healing, the virus enters the sensory nerve and is harbored in the body of that sensory nerve in a dormant stage until . . .
- (3) **Reactivation of Latent Virus**—This occurs when some trigger mechanism, such as menstruation, skin trauma, sexual activity, fever, anxiety or other unknown mechanisms come into play to reactivate the virus in the sensory nerve. The virus then migrates down the nerve to produce the typical cluster of vesicles. Prior to the outbreak of these vesicles, the person usually experiences some itching, burning or pain at the site. The frequency and intensity of these recurring lesions are highly variable from individual to individual. Once latent infection is established, the virus persists for a prolonged period of time—and in some individuals for life.

The most serious complication of HSV-2 is infection of the newborn, who lacks immune defense mechanisms. Thus, the passage of a child through an infected birth canal can cause a massive viral infection and possibly death.

In our next column, we shall discuss diagnosis and latest treatment of HSV-2.



The Power Supplier.

This is the third in a series of columns by Dr. Lee on medical subjects of current interest, although perhaps not fully understood, by the public. If you have a question, please write Dr. Lee at LH Research, Tustin, CA 92680.

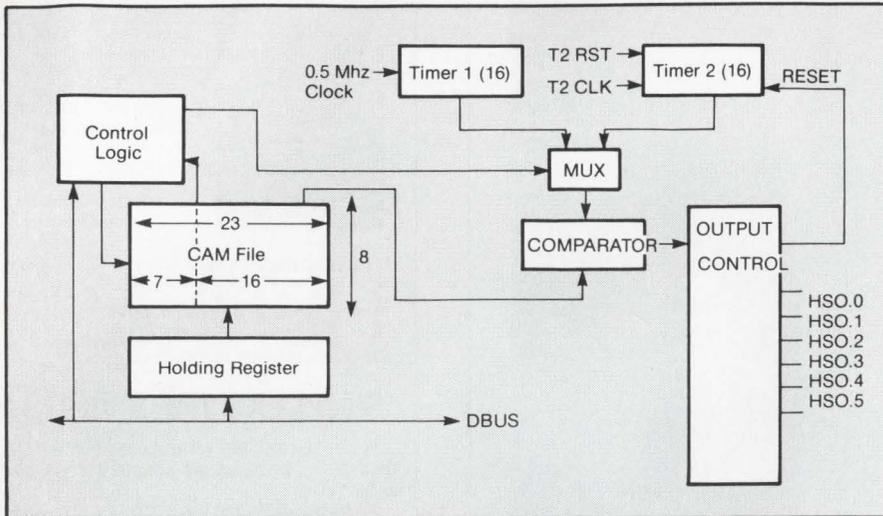


Figure 2: Block diagram of the High Speed Output hardware.

have to be disconnected from the change detector are available for use as normal digital inputs and two of them (HSI.2 and HSI.3) can be used by the High Speed Output unit.

When a change (or changes) of the required type occurs, four bits of change information, along with the current value of TIMER1, are loaded into a FIFO (first-in, first-out memory). Each set bit in this field indicates that a change occurred on the corresponding input pin.

The time reference for the HSI unit is TIMER1, a sixteen bit counter which is incremented every eight state times by the CPU clock. With a 12 MHz crystal this gives a resolution of 2.0 microsec-

onds. TIMER1 is cleared by reset and then starts incrementing. It cannot be written to by the software but can be read as a sixteen bit word at any time. When its count goes from all ones to zero a flag is set and an interrupt generated. The software can use this flag and/or interrupt to extend the measurement range of the HSI unit.

The FIFO that is used to store the change and time information is eight levels deep (including the holding register) and 20 bits wide. The oldest entry in the FIFO is placed in the holding register. When the holding register is read then the next oldest entry will drop into it and another cell of the FIFO will become available for input data. An

interrupt can be generated either when one or more entries exist in the FIFO or when seven or more entries exist. The choice is made by the software by setting a bit in I/O control register 1 (IOC1).

The 8096 only supports byte and word operands for most operations. The holding register is 20 bits wide hence the holding register is broken down into two registers. The 16-bit time field is read as a word register and is known as HSLTIME to the assembler. The change information is read as an eight-bit byte known as HSLSTATUS. The four extra bits in this byte are used to report the state of the HSI pins at the time the register is read (not at the time the reported change occurred). The holding register is cleared after the HSLTIME is read so that HSLSTATUS can be read at any time to monitor the actual state of the HSI pins without losing data from the FIFO.

High Speed Output Unit

The High Speed Output unit serves the output requirements of the system in the same way as the HSI unit serves the input. It allows the generation of pulse and frequency modulated signals with high resolution and minimal software overhead. It can also be used to generate time delays for the operating software and to trigger the A/D converter at precise time intervals for signal processing algorithms. A block diagram of the HSO hardware is shown in Figure 2.

The HSO unit is driven by a Content Addressable Memory (CAM) which is 23 bits wide and eight levels deep. The

(continued on page 120)

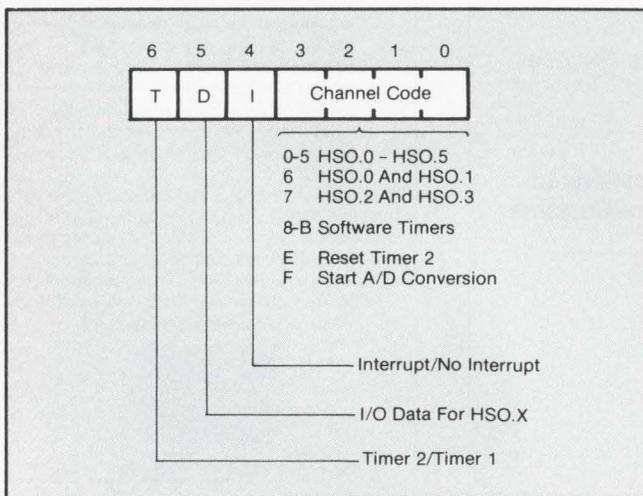


Figure 3: Diagram shows format of Command Tag. The lower four bits specify the basic operation and the remaining three bits are options to the basic operation.

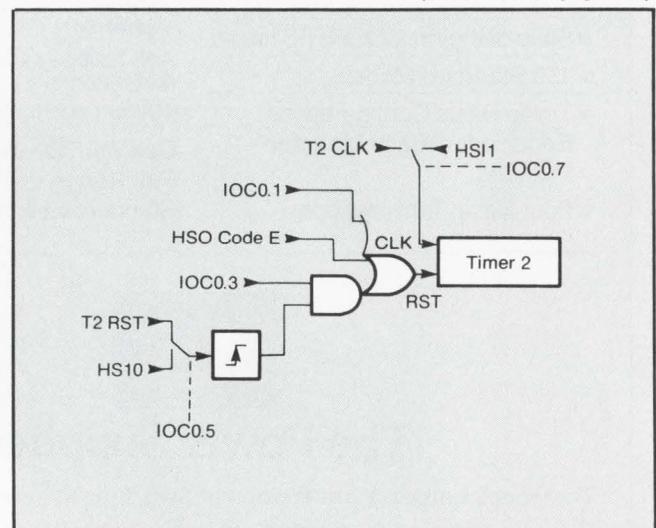


Figure 4: Figure shows the clock and reset options of TIMER2 used by the High Speed Output unit.

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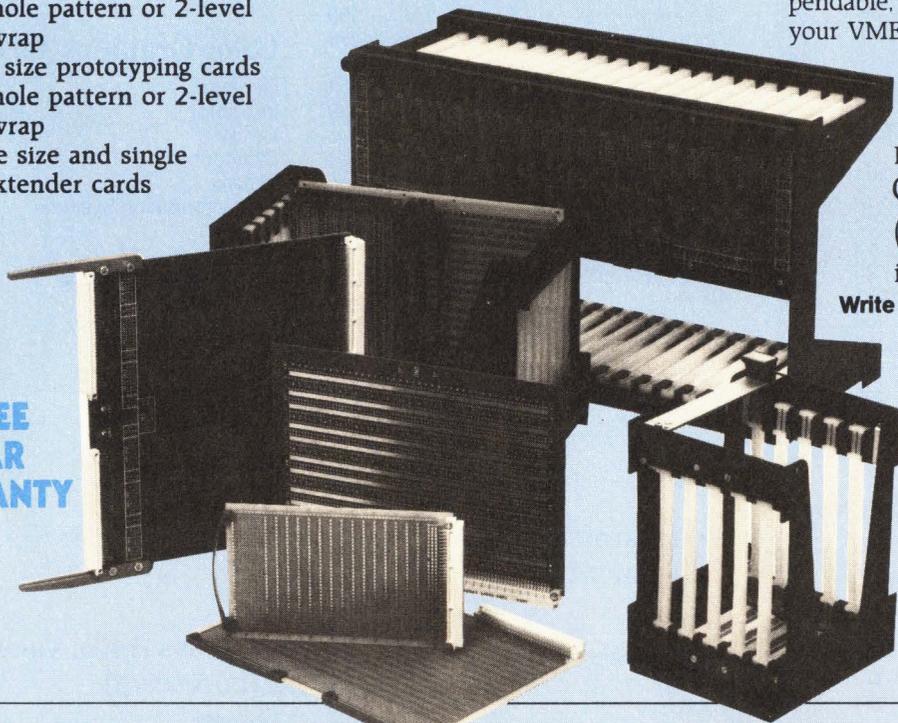
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(continued from page 112)

23 bits are broken into a 16 bit time tag and a seven bit command tag. The command tag tells it when to do it. The format of the command tag is shown in **Figure 3**. The lower four bits of the tag specify the basic operation and the remaining three bits specify options to the basic operation. The basic operations supported are:

- Write to one of the six pins controlled by the HSO unit (HSO.0-HSO.5).
- Write to HSO.0 and HSO.1 with a single command.
- Write to HSO.2 and HSO.3 with a single command.
- Set one of four software timer flags.
- Reset Timer 2.
- Trigger an A/D conversion.

If an operation on an HSO pin is specified, then the value to be written to the pin is taken from bit five of the command tag. Note that if two HSO pins are to be modified with the same command then both will be set to the same state. Bit five of the command tag is ignored for the other HSO operations. Bit four of the command tag enables the generation of an interrupt which occurs when the command is executed.

There are two interrupts generated by the HSO unit. One of them indicates that an operation involving a HSO pin has occurred, and the other is used to signal that one of the internal HSO functions (such as setting a software timer flag) has been completed. Bit six of the command tag controls which one of the two timers available to the HSO unit will be used as a time base for the command. If bit six is a zero then the command tag will be executed when **TIMER1** becomes equal to the time tag stored in the CAM. If bit six is a one then the command tag is executed based on **TIMER2**. In either case the command is flushed from the CAM as soon as it is executed.

One of the timers (**TIMER1**) used by the HSO unit is the same timer that is used by the HSI unit. The other (**TIMER2**) is used only by the HSO unit. **TIMER2** allows HSO events to be generated on a time base that is different from that of the CPU. Like **TIMER1** it is a 16 bit counter that can be read but not written to by the software. It also

has an overflow flag and interrupt to indicate that it has incremented from a source external to the 8096 and can be reset by a number of paths in addition to system reset. The options available are shown in **Figure 4**.

The clock input can come either from a specific pin designated as the **T2CLK** or it can come from **HSI.1** depending on the state of **IOC0.7** which is set by the software. In either case the counter is incremented on both edges of the clock signal. **TIMER2** can be reset by a specific pin designated as **T2RST** or it can be reset by **HSO.0**. It is also possible for the software to lock out external sources of reset (by clearing **IOC0.3**) and/or reset **TIMER2** directly (via **IOC0.1**) or indirectly via a command stored in the CAM. Note that this last possibility allows **TIMER2** to be configured as a modulation counter since the software can command the HSO unit to clear **TIMER2** when it reaches a given value.

Commands are loaded into the CAM from the 23 bit wide holding register which, like the holding register for the HSI unit, is actually made up of a byte register (**HSO_COMMAND**) which stores the command tag and a word register is considered loaded after **HSO_TIME** is loaded so the software must always load **HSO_COMMAND** and then load **HSO_TIME**.

The software must also ensure that the loading of the two registers is not interrupted by an interrupt service routine which uses the HSO unit. If such an interrupt occurs immediately following the loading of **HSO_COMMAND** then the subsequent loading of **HSO_TIME** will reload the command tag written into the holding register by the interrupt service routine. The safest procedure is to lockout interrupts during the loading of the holding registers, however a care-

ful examination of the control flow of the program may show this to be unnecessary.

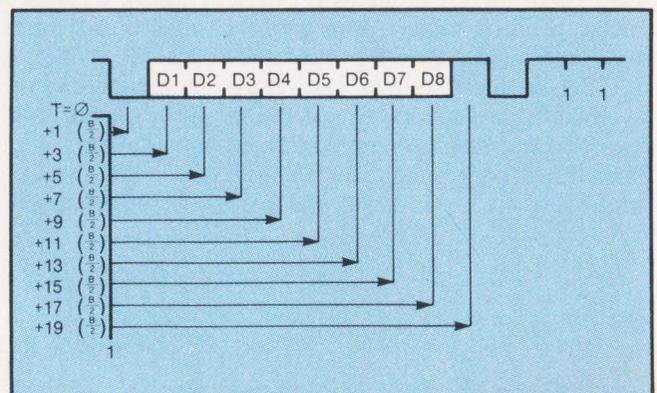
If there is an empty cell in the CAM when the holding register is loaded then the command and its time tag will be loaded into the CAM within seven state times (1.75 microseconds at 12 MHz). It is important to note that a command will not execute from the holding register, it must be loaded into the CAM. If the CAM is full then the command will remain in the holding register until one of the commands already in the CAM is executed and flushed.

Two status flags are available to help the software manage the CAM. One of them indicates that the holding register is full or the CAM is full. Once a command is loaded into the CAM it cannot be read or overwritten, it can only be flushed after it is executed. To support those situations where the software wishes to cancel a command after it has been loaded, the HSO unit is configured so that two operations to a HSO pin which cancel each other will not effect the setting of the pin if they are executed with identical time tags.

Application Example

Since the 8096 incorporates a full duplex asynchronous serial port in its hardware it may seem strange that one would want to implement a software driven serial port using the high speed I/O features. There are, however, many useful configurations of microcontroller systems which in fact require more than a single serial port. An obvious example would be a network of 8096 controllers which use the hardware serial port for interprocessor communications. One (or more) of these controllers might also be required to communicate with a CRT terminal used to supervise or monitor

Figure 5: Figure shows standard 10-bit asynchronous frame.



The serial output process is simpler than the receive process because there is no need to synchronize with the outside world.

the system. Another example would be a simple CRT terminal design based on an 8096 which needs one serial port for communication and another for driving a slave printer. It may also be true that this is, in fact, a strange requirement. In any case it is an excellent example to show how the high speed I/O features of the 8096 might be used.

The objective is to add a software driven asynchronous serial port to the 8096 that provides full duplex serial communication at 2400 baud. A standard frame consisting of a START bit, eight data bits and a STOP bit will be assumed. A high speed input pin (HSI.0) will be used for received data and a high speed output pin (HSI.0) for transmit data.

A standard 10-bit asynchronous frame is shown in **Figure 5**. The figure also shows the points in time where the receive process must sample the incoming data stream and take some action. The first timing point (labeled T=0) is the leading edge of the start bit, the accurate sensing of this edge is important because all subsequent sample times are relative to this edge. This event also places the highest burden on the sampling algorithm because it can occur at any point in time. The rest of the sampling events occur at some multiple of one-half a bit period relative to the edge of the start bit. The diagram uses the symbol B to represent a bit period.

At the second sample, which occurs half way through the start bit, the data must be checked to make sure it is still a SPACE. If it is not, a noise pulse has caused a false start and the receive process must be reinitialized. The next eight samples are used to shift in the serial data stream. The last sample, which occurs 19 one-half bit times after the leading edge of the start bit, is used to

verify that the stop bit is valid (i.e. it is in the MARK state). If it is not the a framing error must be reported since it is likely that the receiver is not properly synchronized with the transmitter.

The HSI unit is an ideal mechanism for detecting the leading edge of the start bit. All that needs to be done is to set the mode register to detect negative going edges on HSI.0.

The software timer interrupt service routine implements a simple state machine based on the variable count. The routine also arranges for the next sample by issuing a command to the HSO unit to generate another software timer interrupt at the appropriate time. This is done in all states unless the reception of the character is complete or a false START bit has been detected. Under these conditions the receive process must be reinitialized by enabling HSI.0 into the event FIFO (by setting IOC0.0) instead of retriggering the software timer.

The serial output process is simpler than the receive process because there is no need to synchronize with the outside world. A transmission can be started at any time by setting the TxD line to a space for one bit time to form the START bit. Following the START bit are the eight data bits and the STOP bit. The HSO interrupt service routine can be used to transmit the data and the stop bit but the transmit process must be initialized.

The only real complication in the HSO interrupt service routine is that there are no flags available in the 8096 which indicate which of the HSO outputs caused the interrupt. In many systems this does not represent a problem because the HSO unit can be treated as a write only device. It is given commands which are to be executed at the proper time but no feedback is required to indicate when the proper time has been reached. In this case, however, the feedback is required since the CAM isn't deep enough to hold all of the transitions required for a character. Even if it were big enough it is unlikely that so many CAM locations would be dedicated to serial output. □

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UNIX Standards Move To The Forefront

Will the first volleys fired between IBM and AT&T center around UNIX in 1984?

by Mike Cashman, West Coast
Technical Editor

The year of 1984 promises to be the most significant year in the history of the UNIX operating system since its creation in 1969. This has implications of various degrees for the entire computer industry, including OEM's, users, value-added resellers, and manufacturers.

For those not intimately familiar with the churning UNIX marketplace, the prediction for 1984 may seem overstated. After all, UNIX has been in existence for 15 years, virtually everyone in the industry has at least heard of it, and many if not most, directly affected by its existence have opted to either support it or use it. It is significant that Western Electric, the entity that actually licenses the operating system, acknowledged at Comdex in Las Vegas that licensees would top the 100,000 mark by year-end 1983.

Still, the consensus of people interviewed seems to be that up until 1983, UNIX has been a comer; in 1984 it will arrive. Here is why.

- 1984 will be the year that AT&T officially invades the computer industry. The first two products which will be announced (the 3B5 and 3B20) will of course, be Unix-based and very likely Unix-optimized.
- It was considered at Comdex that IBM would announce Unix support probably for the 4300 level machines extending downward toward the desktop products. Some thought this move might be made prior to AT&T's entrance into the computer marketplace, or immediately after in order to steal some

of AT&T's thunder.

• A proposed technical standard for Unix-compatible systems is slated for review during January, 1984. Additionally, the IEEE Society has agreed to use this document as a basis for proposing a UNIX standard.

UNIX Origins

During the primitive batch processing world of the Sixties, there were seers who envisioned that the computing "futureworld" would be markedly different. This new world would involve continual interaction by users working from terminals to computers supporting much larger data bases than existed then. One of the first suitable designs for a computer operating system that would operate in this mode was developed at the Massachusetts Institute of Technology. It was called MULTICS, and if the IBM 370 series hadn't been introduced in 1970, but 1971 or 1972, General Electric might still be a factor in the computer industry. General Electric offered MULTICS on its last large-scale computer system announcement, the GE-645.

As luck would have it, one of the few places where a GE-645 was installed before the company exited the business in 1970 was Bell Laboratories. There, Ken Thompson borrowed on many of the MULTICS concepts to create a multiuser, interactive operating system for the Digital Equipment Corporation PDP-7. It is important to bear in mind that to solve was essentially one of programmer productivity. But like so many other developments in this industry, the UNIX system would come to be some-

thing of a significance unforeseen by its developers. The bright idea of a time-shared operating system for minicomputers was followed up by another good idea: coding the system in a high-level language that would make the operating system somewhat machine independent, or transportable. So Thompson created a new language for that purpose called simply "B". The "B" language was modified by Dennis Ritchie to become "C", and he then rewrote UNIX in "C".

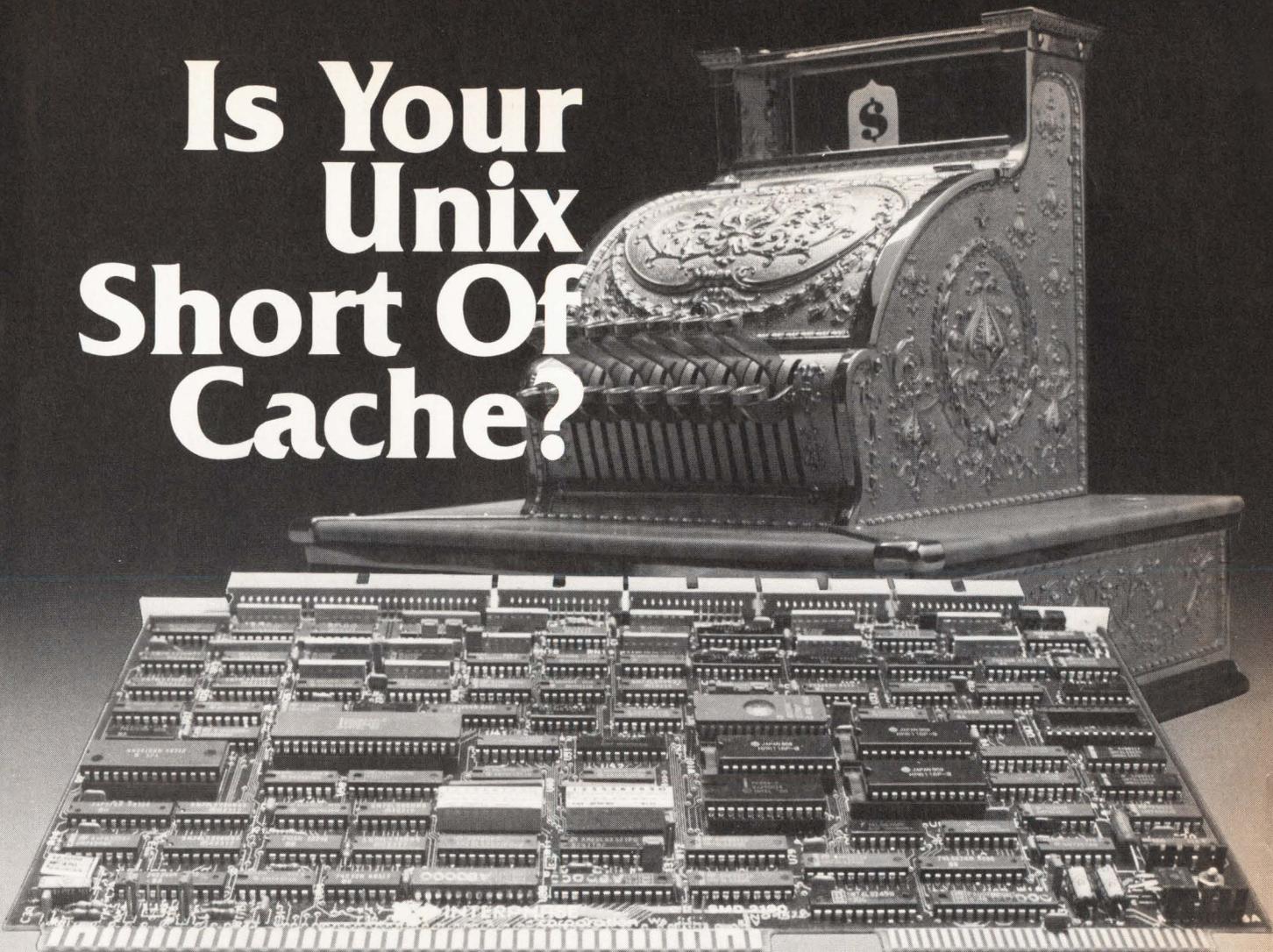
UNIX was a distinct watershed in the history of operating system development. Until this time, operating systems were created by vendors, not users, and users had to operate within the confines of whatever type of system a vendor chose to support. Users were very much locked-in: hundreds, thousands, and even tens of thousands of man years would be involved in converting operational programs from one vendor's way of operating to another's.

But UNIX had the potential to change the rules of the game. If users could get their hands on a common operating system, one which would run across even a few assorted manufacturers' machines, users would be a lot less dependent on their hardware vendors for their software. In addition, software houses would find it much easier to develop programs for a wider variety of machines.

This was the potential and promise of UNIX. Because UNIX was created on a minicomputer supplied by DEC, UNIX readily caught on with other DEC users. And because relatively low-cost DEC minicomputers were in evidence among universities, UNIX popularity increased enormously. A whole new generation of programmers and computer science majors were exposed to the concepts of a richly endowed, reasonably portable operating system that ran on, of all things, a small system.

Still, UNIX came out of a technician's world and was largely focused on the programming productivity problem and has been described as being "user

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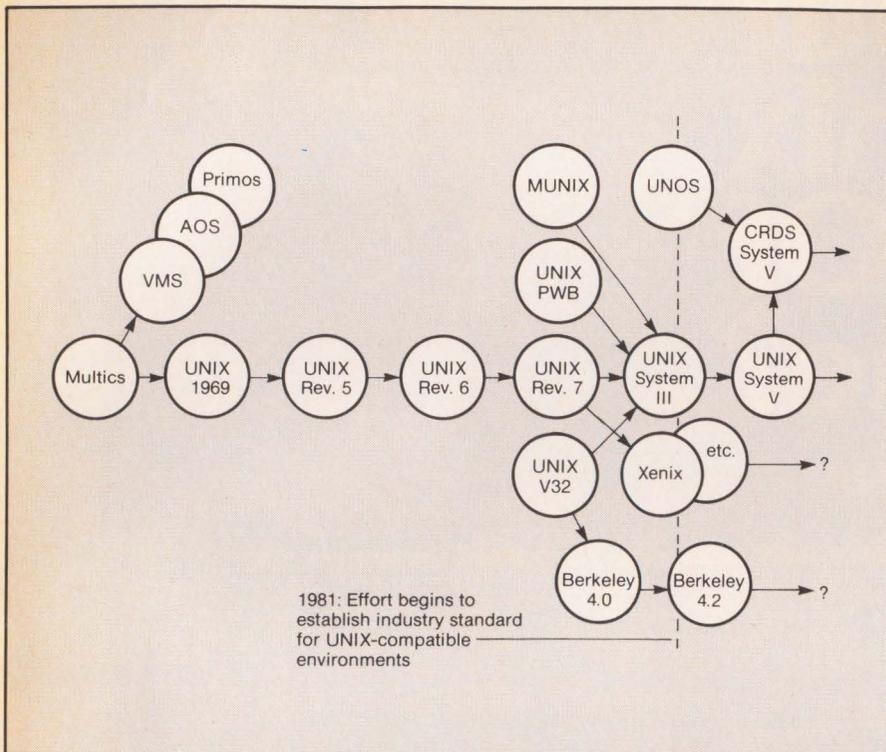


Figure 1: The evolution of UNIX: The UNIX operating system has its roots in Multics, a multi-user, multi-tasking operating system developed in the late 1960s at the Massachusetts Institute of Technology. UNIX was created as a software development system by Bell Laboratories in 1969, and underwent a number of revisions by Bell, and was modified and enhanced by others. UNIX System III has served as the basis for many of the proprietary UNIX-derived operating systems available today, and many are compatible with it. The new UNIX System V is the latest Bell revision. Charles River Data Systems announced their UNOS operating system in 1981 with Revision 7 compatibility as well as CRDS System V, which is derived from UNIX System V.

hostile in a user friendly world." UNIX was still a giant step forward in freeing up software packages to run on a greater variety of equipment. But there were no English language commands and user friendly interfacing.

Because of this, users, especially the universities that began to use UNIX as a basis for an even better operating system. UNIX gradually became a nucleus, or kernel, inside of programming shells

that were added to take care of the lack of user friendliness and system capabilities such as virtual memory management.

As an entire sub-industry that specialized in improving UNIX evolved, Bell began to lose control over its creation. For example, for use in business applications, it was absolutely necessary to have file and record locking, and virtual memory features were advantageous too. Today, 15 years after the birth of

UNIX, these capabilities are not present in Bell's latest system version. They are, however, available from other sources, most notably the University of California at Berkeley's computing center. (There are strong rumors that Bell will finally include these features this year as a response to the popularity of systems that offer them.)

This is one of UNIX' principal problems. Equipment suppliers and users

UNIX In Europe

"The entire perspective is different for UNIX in Europe. In the U.S., a vendor is apt to say it supplies AT&T's UNIX. Over here the response to the same query would be along the lines of "we use UNIX from some American company called AT&T."

Emrys Jones is Chairman of EUUG, The European UNIX Systems User Group, an entity that clearly sees things UNIX in a different light. "There is a strong steady UNIX push here. Users want the system for the same reasons as everyone else; relative independence from traumatic hardware and software changes. Vendors see it as a useful tool for approaching multi-national markets."

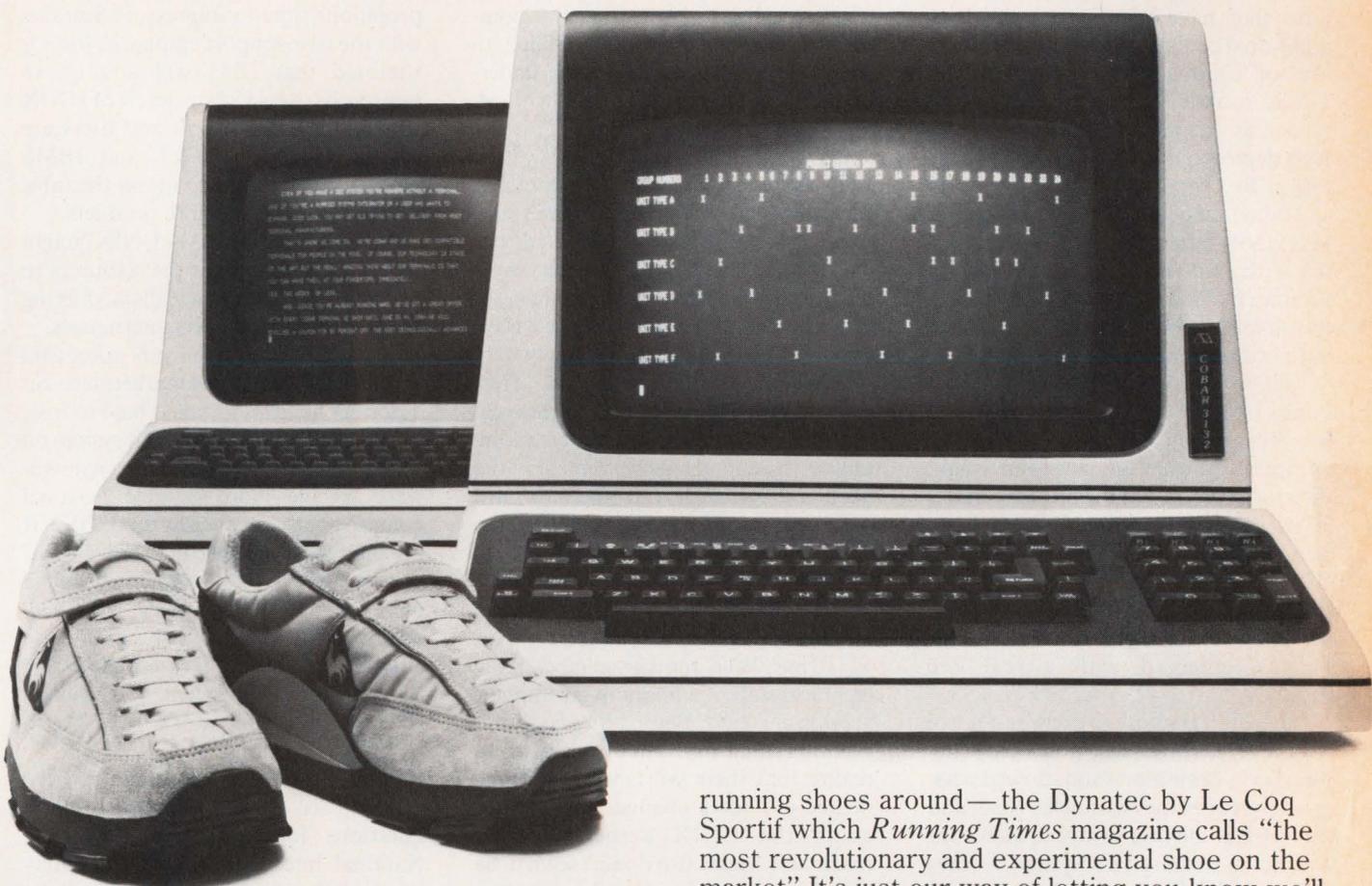
Many major European vendors offer UNIX. This set includes Siemens, Kontron, Thomson-CSF, Philips, NCR and others. The set excludes, for the time being, ICL and Olivetti, with strong rumors that this situation

will be addressed this year.

The degree of UNIX support has varied widely, according to Jones. "Some UNIX suppliers have fallen down in support; IBM does well in these situations," he observes. Another development of interest is that of UNIX being used by vendors of newer hardware against the hardware UNIX was born on, the Digital Equipment product line. "VAX hardware is seen as overpriced now, and that market is being picked over by other suppliers.

"The level of communication and documentation from AT&T isn't what one would expect. In fact, not every announcement coming out of AT&T is fully understood; the company doesn't do a great job of spelling things out." This attribute, cited by domestic UNIX users, may endure during the time AT&T finds its own computer industry style.

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alike feel frustrated at Bell's development pace. Together with other factors (not the least of which is the amount of the license from Bell) has given rise to a three-tiered market. Today there are stock UNIX systems, UNIX-based systems that have been augmented with additional coding (and thus in Bell's eyes are not legitimate UNIX systems), and UNIX look-alike systems. These systems may resemble UNIX systems to a high degree and yet contain not a single line of Bell code.

Today, one vendor's UNIX is not necessarily (and probably isn't) compatible with another's. To a degree, Bell has lost much of the control of the destiny of its offspring, but this may only be a temporary situation.

"Three years ago, AT&T really didn't appreciate the value of UNIX. Now it perceives it as crucial to its future in the computing business," says Jim Isaak, director of product marketing for Charles River Data Systems, a Framingham, MA supplier of UNOS. UNOS is a UNIX-like system that contains approximately two-thirds of the complete set of system calls of UNIX, but has been augmented with a real-time monitor.

"Bell didn't choose to exercise control over UNIX for a long time. Then the enhancers came along and showed what great potential the Bell nucleus had, and now Bell is moving swiftly to gain control again, starting with System V," says Robert V. Dickinson, vice president and general manager of the systems division of Zilog, Campbell, California.

This is the situation that is holding off the growth of UNIX today. Licensees either stay within Bell's guidelines and stay compatible with future Bell developments, or they opt for augmented systems. The arguments in favor of basing systems on Bell are balanced by the relatively high license fees, lack of important features, and insecurity regarding the Bell UNIX development pace. While it hasn't been clear how much involved with UNIX Bell was going to become, it is somewhat clearer after the Comdex exposition in December in Las Vegas.

"It's clear that the industry is waiting for two developments. One is the official AT&T entry into the computer marketplace, and the other is to see what IBM is going to do about that and UNIX," says Charles River Data System's Isaak.

So, as the UNIX name and popular-

ity have spread, AT&T is moving to reassert control, perhaps to get everyone thinking the same way in preparation for its hardware announcement. At Comdex, Western Electric, the UNIX license people held a meeting on a non-disclosure basis with its System V licensees. Some attendees were willing to share their impressions on the understanding that they wouldn't be identified.

The Xerox/Thermos Problem

"The meeting was a review of the state of the union, given by Tom Crowley and Otis Wilson of Bell. They solicited user comments on issues like whether we'd want to see updated system releases more or less often, what the revision cycle should be, what key features were needed, etc.," said one attendee. "They also made it very clear that the lawyers aren't happy regarding trademarking abuses. It reminds me very much of the problems XEROX and Thermos have with their names not becoming generic. They carefully explained that there are only two authorized versions, or ports, of UNIX, and that those are for the Digital Equipment VAX and PDP-11/70 line," said another member of the technical staff of a major minicomputer vendor. "I find Bell's attitude disappointing in all this. They don't seem to realize that there will always be some degree of coding changes necessary to adapt the UNIX kernel to other machines. And it also doesn't seem to be perceived that we're all in this together. We, as licensee, can put money in Bell's pocket, and I feel they are too quick to draw the line between what is a true UNIX system and what is not," said this user. "Maybe these are the hallmarks of a company that has had a more technical than business/marketing bias, at least concerning this particular product. I think their attitudes will mature, but it's going to be frustrating for a while."

On the plus side of the matter, users reported that Bell estimated the number of object code licenses would reach 100,000 by the end of calendar 1983, a number almost double what some outside consultants had been claiming. Also, object code licenses are in the process of dropping "showing Bell's sensitivity to the low-end marketplace" by perhaps 50%.

Also, Bell is thinking of unbundling the system to a greater degree. This would involve separating the operating

system kernel from programming languages, programming workbench features and other capabilities says a source.

So steps are being taken to shore up UNIX support by Bell prior to the AT&T announcement. It seems like a propitious time to impress its licensees with the new support emphasis, for it is rumored that IBM will attempt to impress its users with its levels of UNIX support. Clearly buyers and users are waiting for both AT&T and IBM's UNIX cards to be face up on the table before moving to acquire products.

No matter what "IBM's UNIX" might look like, it clearly has the resources to build a UNIX-like critical mass, offering both suppliers and users alternatives.

"IBM has never been very successful in that DEC VAX-type marketplace. So it doesn't have an installed base to lose. By bringing up a quasi-UNIX system on the 4300 and perhaps extending it downward to the more capable personal computer variants such as the 3270/XT, it would have a powerful product strategy to use on both AT&T's fledgling computer industry efforts and also against DEC. All this with virtually no effect on itself. IBM likes situations like that," says the president of a Silicon Valley systems integrator who wished to remain anonymous.

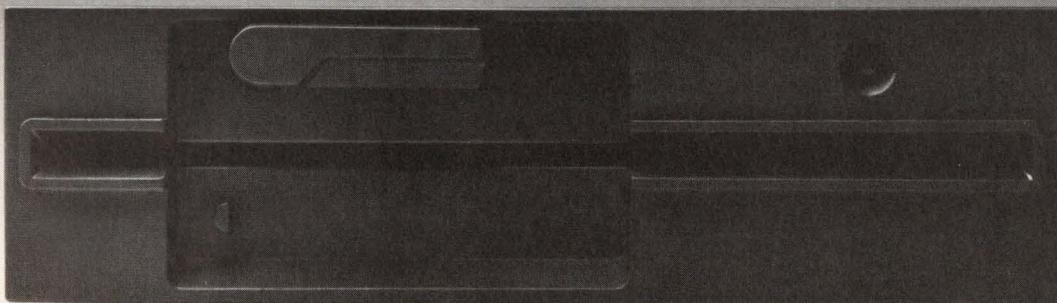
"I think AT&T's entrance into the marketplace alone will create a lot of questions for buyers of Motorola, National, Intel and other micros. It may be that the AT&T offerings will be highly optimized to run the relatively large UNIX system measurably more efficiently," according to Charles River Data Systems' Isaak.

One other interesting aspect of AT&T's entry into the marketplace is that the company will be entering a market filled with competition. In general, users have been critical of the quality of the documentation supplied for UNIX. With a technical standard for UNIX-like systems put for review, AT&T's early moves getting closer, and IBM's responses all due in 1984, it figures to be an interesting year for all concerned. □

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WE'VE TAKEN MASS STORAGE TO A NEW LOW.



C Itoh's YD-380 Floppy Disk Drive is half the size of an ordinary 5¼" drive and measures a low 1.6". It also offers an incredible 1.6 megabytes of storage and full 8" double-sided, double-density performance—a new high. And when you realize that two such drives fit easily into one conventional 5¼" drive slot, it's no wonder the YD-380 Floppy Disk Drive is fast becoming a new favorite.

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C. ITOH ELECTRONICS

A World of Quality

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Digital Optical Disks Store 1 Billion Bytes

GIGADISC is the first of a family of laser optical storage devices to be developed by Thomson-CSF Communications of France. The GIGADISC will store one billion bytes of formatted data on a single sided 12" optical disk, and will be produced in both a 19" RETMA rack mount version and a stand-alone table top unit.

The GD 1001 drive is easily adapted to mini or micro computers via the SCSI (1) interface. The optional internal controller, which can host up to 8 disk drive units, features a powerful real-time error detect and correct scheme which boasts a 10^{-12} non-recoverable error rate for normal data reliability in the EDP environment.

Low cost, non-erasable data and extended storage life assures GIGADISC much success in traditional mass storage applications such as archives, database libraries, facsimile storage (including medical applications) and electronic filing systems requiring audit trails.

As with any magnetic disk peripheral, GIGADISC allows for direct access to each information record, while guaranteeing the same level of data integrity. GIGADISC's large storage capacity does not interfere with easy connection to a computer, including microcomputers. The disk can be removed without imposing any constraints on its operating environment. A dedicated archival feature is included because each sector in the disk can be recorded only once. There is a ten year storage life for archival and an even longer life when utilizing metallic disks.

The GIGADISC read-write unit requires no adjustment as a result of environmental changes or after replacement of any one of its subassemblies. The disk format includes an optical unit, with a semiconductor laser module and a photodetector. An optical head is actuated for both radial and vertical positioning of the laser beam. A linear motor moves the optical head in order to focus it on the target track area, and a rotation motor which, on its axis, includes the disk seating and clamping device. A set of logic boards controls the power

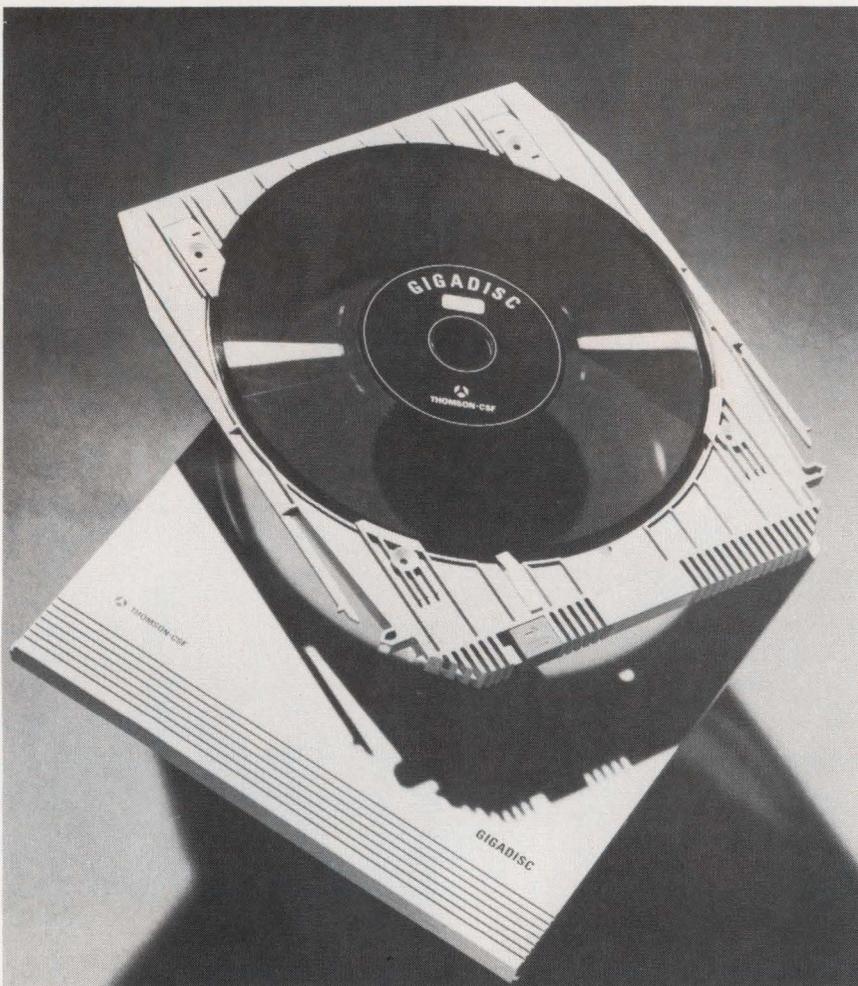


Figure 1: GIGADISC allows for direct access to each information record, while guaranteeing the same level of data integrity.

of the laser output, the servomechanisms and the disk accesses.

Data Integrity

While developing GIGADISC, it appeared that real-time error detection techniques would not allow for optimized use of the entire disk capability. Thomson-CSF decided to develop a highly powerful and automatic error detection and correction feature which guarantees the effective user's capacity of the disk and maintains records at a level of quality even after numerous years in archival storage. The disk is preformatted in tracks and sectors. Each sector can be directly accessed by its logical address

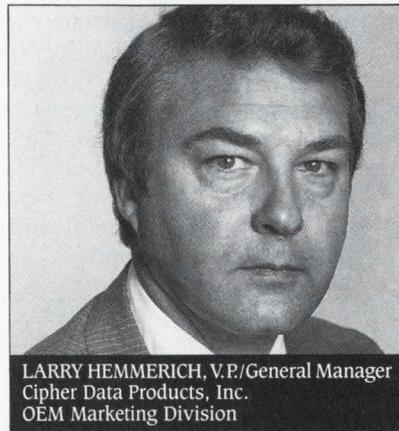
and the spiral organization of the tracks allows for continuous writing and reading of streams of information. Once recorded, a disk can be entirely replicated in one step by a physiochemical process (plastic copies). Metallic copies of a disk can also be made when the need arises for extra long archival life.

In comparing GIGADISC to other recording technologies, it features a very high recording density: 210 Mbits/inch² (33 Mbits/cm²); non-reversible writing capability (automatic archiving); removable disks; direct access to any sector in the read or write mode; three methods of access (random, optimized random and sequential). The quality of data

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integrity required by data processing allows a capability for recording and archiving of data, very high levels of

data compression, compatibility with the existing data management softwares, and preservation of stored

data on recorded disks over a minimum of 10 years.

—Thomson-CSF

Write 235

Stand-Alone Array Processor Runs APL Software

The APL Machine, a stand-alone, general-purpose computer system from Analogic Corp. (Wakefield, MA), uses array architecture to deliver mainframe APL performance. Featuring the interaction of an IBM PC, the APL Machine is designed to replace traditional methods of processing APL software. The APL Machine is targeted toward financial and actuarial markets, but will also find applications in graphics animation and laboratory research.

A typical configuration consists of a 4 Mbyte array processor, an IBM PC as the programmer's workstation, a 124 Mbyte hard disk, a dual mode tape drive, an I/O processor supporting up to 8 terminals, and the Analogic software system. System archi-

ture supports several levels of overlapped and parallel processing.

Analogic's version of APL software is the first implementation conforming to the ISO standard of APL and emphasizes its strong portability. The APL machine's APL interpreter runs in the 12.5 Mhz 16/32-bit super micro control processor handling all the aspects of syntax and conformance checking. Concurrently, the array portion of the machine executes arithmetic and logical expressions, while providing several high-speed processing elements executing additions, multiplications, and logical operations at the same time. The APL Machine's array processor can execute up to 10 million full floating point operations per second.

The Analogic 32-bit floating point array processor (**Figure 1**) used in the APL Machine is also programmed directly in APL. Since the primitive functions and operators of APL reside in pipeline microcode (**Figure 2**), high-speed execution in most applications is achieved directly from APL. For applications using different software such as compiled or assembled code, Analogic's APL implementation provides incorporation of the non-APL code. These "shells" are similar to UNIX shells and handle non-APL code in the same manner as if it were written in APL.

Analogic has designed an operating environment for the PC workstation called InSight, which allows the user to display up to ten concu-

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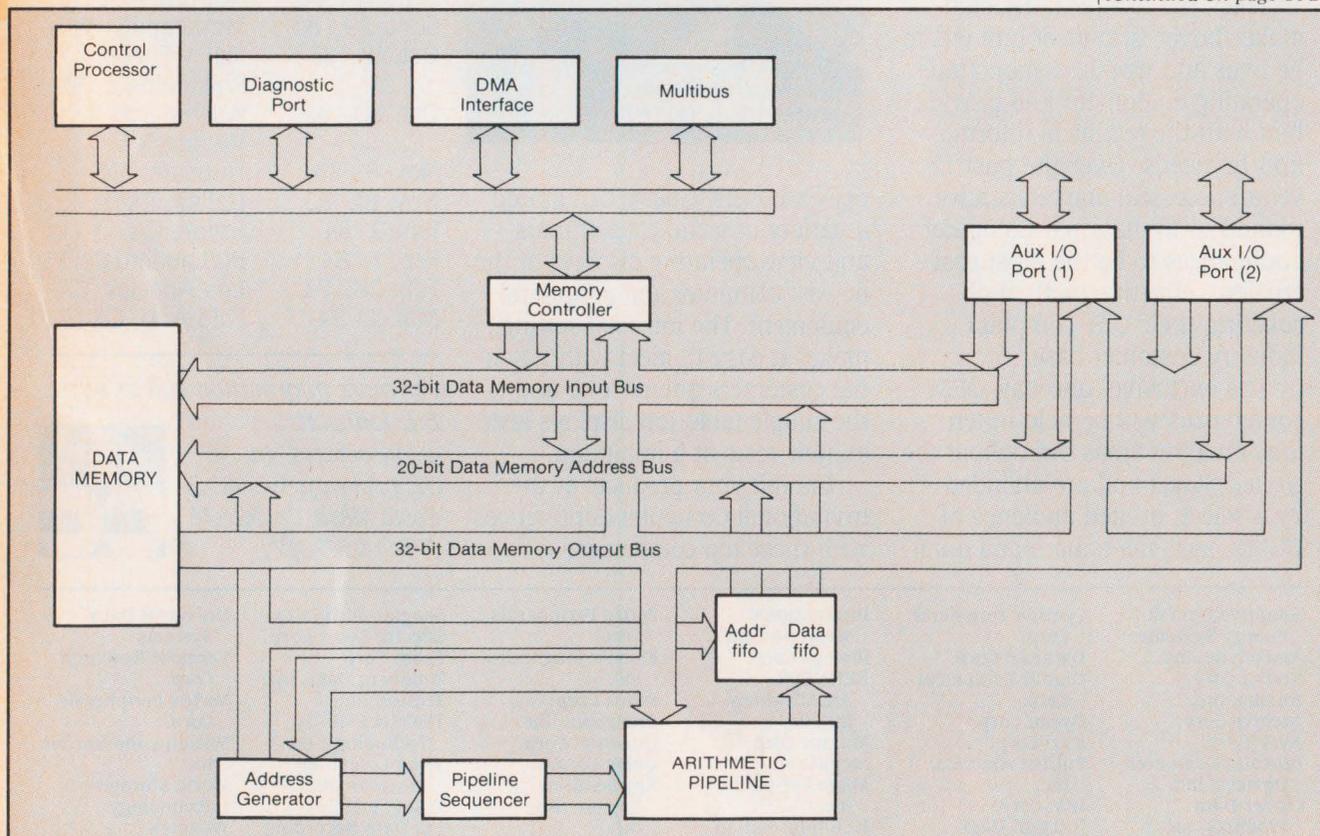


Figure 1: Array Processor Architecture.

Coprocessor And I/O Port ICs Offer Solution To Real-Time Processing Needs

Significant interrupt control and input/output capability are crucial in high speed controller and communications link designs. Two new integrated circuit devices from Signetics Corp.'s Bipolar LSI Division are the 8X310 Interrupt Control Coprocessor and the 8X374 Addressable I/O Port with Parity. Both products support the 8X305 MicroController, a control-oriented solution to real-time processing needs in robotics, industrial, space and military applications.

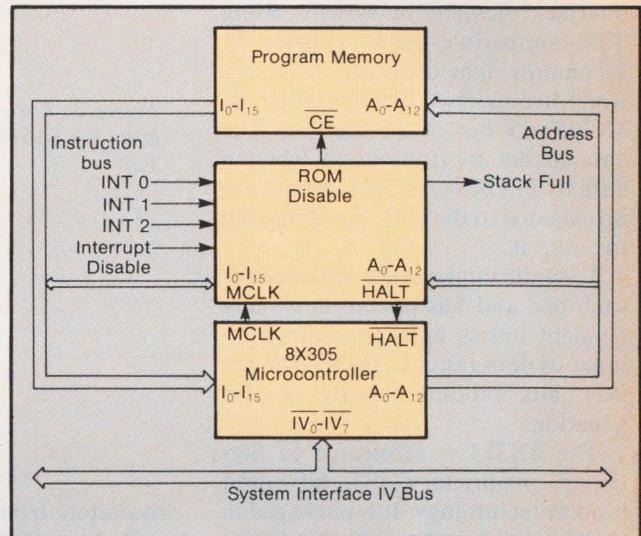
Used in combination with the 200ns 8X305, the new 8X310 Interrupt Control Coprocessor adds hardware interrupt and subroutine handling for interrupt-driven real-time control systems. Since the benchmark of 8X305 applications is throughput speed, the 8X310 unburdens the host by operating synchronously on the system's instruction and address buses. It functions by monitoring the binary flow on these buses to capture, decode and process interrupt and subroutine call requests.

The 8X310 can interrupt the 8X305 in as little as 400ns, or two machine instruction cycles. The 8X310 features three maskable, prioritized interrupts (handles up to four simultaneous interrupts and/or subroutine calls), interrupt disable, 4-level LIFO stack and Stack Full flag.

Fabricated in Signetics' proprietary ISL (Integrated Schottky Logic) high-performance bipolar technology, the 8X310 is packaged in a 40-pin 0.6-inch wide plastic or ceramic DIP. It operates from a single +5 volt supply and is available immediately in sample quantities. For 100 — 999 pieces, the 8X310 is priced at \$15.00 (plastic) or \$23.50 (ceramic), for commercial (0 to 70°C) operation. Samples rated for more hostile space, military, automotive and industrial environments (-55 to 125°C) will be available in Q3 1984.

As shown in **Figure 1**, the Interrupt Control Coprocessor provides three prioritized interrupt request lines, INT 0 (Highest priority), INT 1 and INT 2. A low-to-high transition applied to any of these input lines latches in

Figure 1: Typical system connection using ICC.



an interrupt request which may be serviced when sampled by the ICC once each instruction cycle of the MicroController. When an interrupt request is serviced, the ICC forces the MicroController to jump to one of three fixed locations in program memory.

The ICC performs three general functions. It provides a means for the 8X305 MicroController to respond to interrupt requests by diverting the program flow of the 8X305 MicroController to the proper interrupt

service routine or, in the case of subroutine, the ICC stores the return address in the 4-level LIFO stack (**Figure 2**). The ICC also returns the user to the proper point in the main program for both interrupt and subroutine activities. Both automatic and programmed masking capabilities are provided by the ICC.

The new 8X374 Addressable I/O Port with Parity marries the 8X305's 8-bit IV (Interface Vector) data bus to its system application. Unlike prior family I/O ports, the 8X374 features

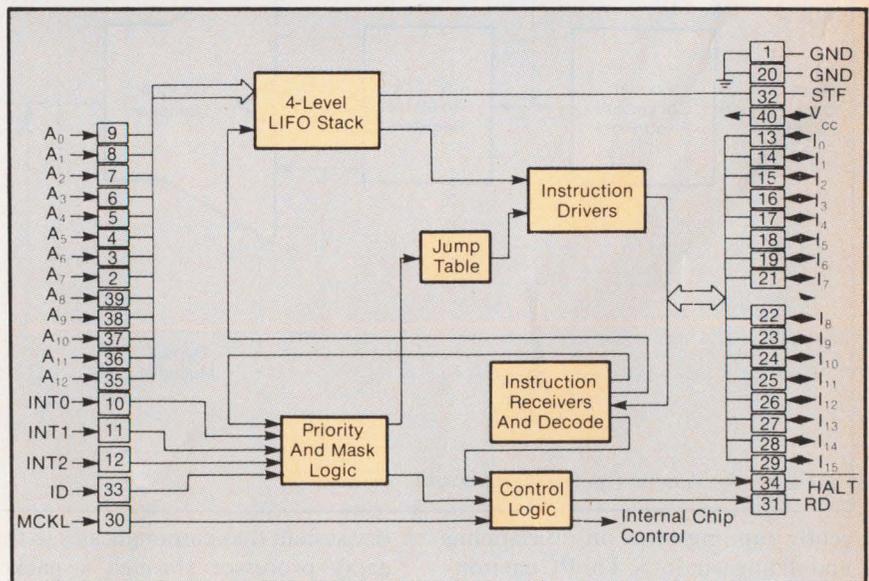


Figure 2: 8X310 Interrupt/Control Coprocessor functional block diagram.

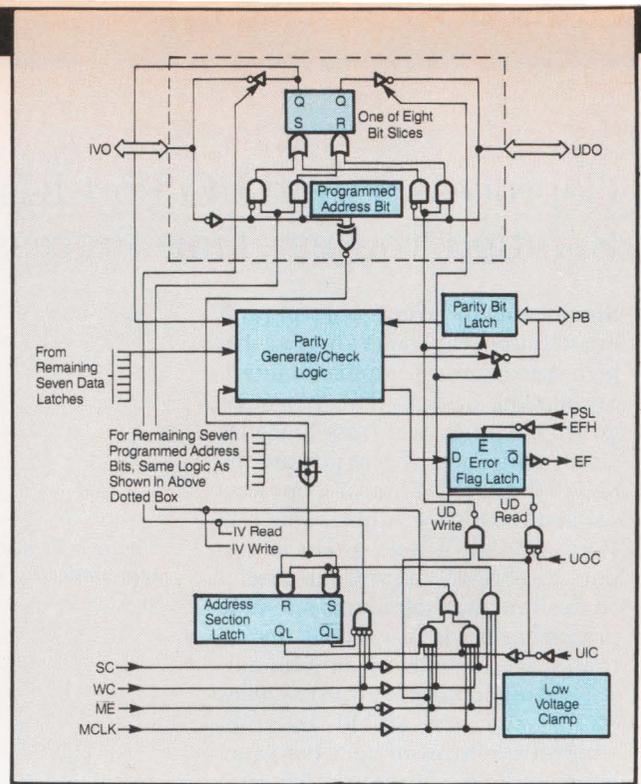
parity generation/checking logic, making it valuable in applications where low error rates are mandatory.

Like its sister I/O ports, the 8X374 is designed for use as a bi-directional interface element in systems using TTL-compatible buses. (Figure 3). It contains eight identical data latches which are accessed through either the 8X305's IV bus or the user bus. The data latches are transparent, wherein data from a bus enabled for input are propagated to the other bus if enabled for output.

Separate controls are provided for each bus and bus operation is independent unless both attempt simultaneous data input to the 8X374; the user bus retains priority in this situation.

The 8X374 is fabricated in Signetics' proprietary ISL advanced bipolar technology. It is packaged in a 28-pin 0.6-inch wide plastic or ceramic DIP and operates from a single +5 volt supply. Available im-

Figure 3: Logic diagram for 8X374 I/O Port.



mediately from stock, the 8X374 is priced at \$5.75 (plastic) or \$8.75 (ceramic) for commercial (0 to 70°C) operation. Samples rated for more

hostile space, military, automotive and industrial environments (-55 to 125°C) will be available Q2 1984.

—Signetics Corp.

Write 234

Innovative Design

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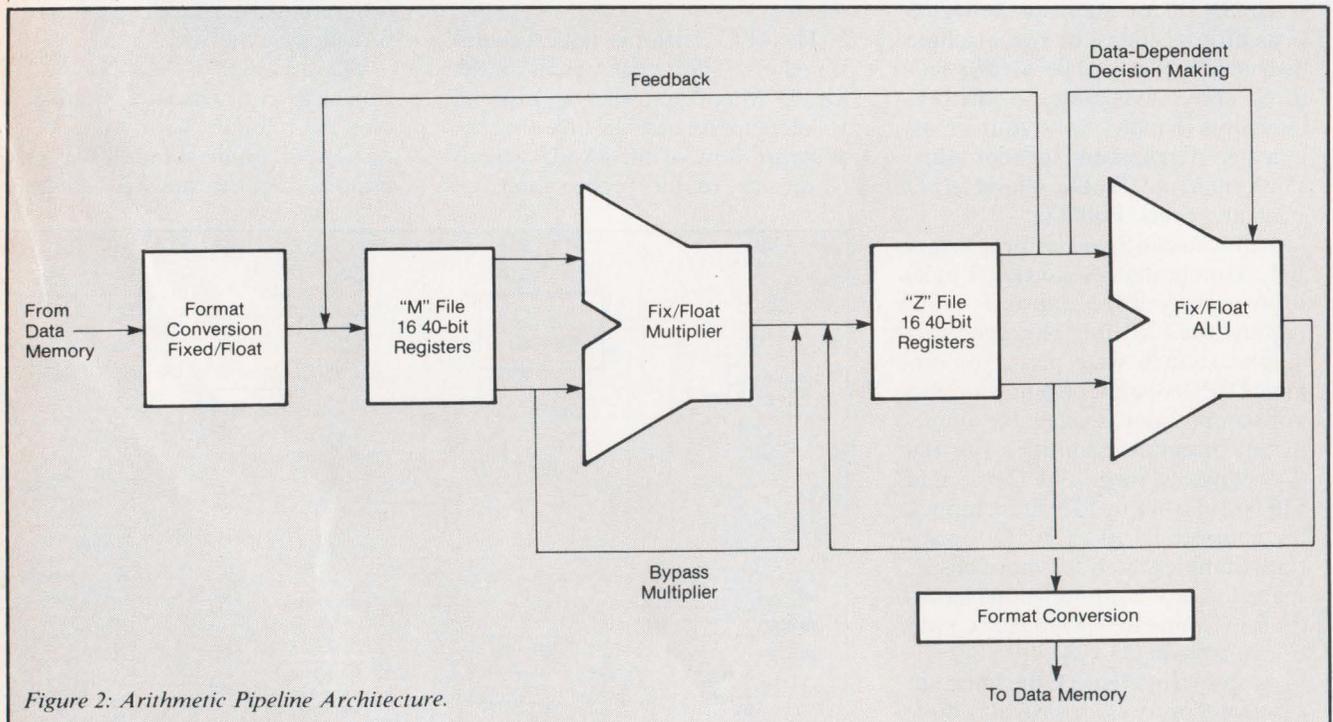


Figure 2: Arithmetic Pipeline Architecture.

rently running tasks on overlapping and sliding windows. The PC environment is a multitasking, virtual mem-

ory system that communicates to the array processor through a packet protocol, extending the PC for con-

current interaction with the multiple processes on multiple systems.

—Analogic Corp.

Write 237

OPERATING SYSTEM EXTENSION

Programs Can Be Viewed Simultaneously

Microsoft Windows are an extension to the MS-DOS operating system, for use with the Polo System I microcomputer. Microsoft Windows provides a common operating environment for applications programs that utilize a bit-mapped display and a mouse cursor control device. Windows feature a window management capability that allows a person to view unrelated applications programs simultaneously. It also provides application portability between computers and can transfer data from one application program to another. Data can be exchanged among word processing, spreadsheet and graphics packages. The programs that are activated by Microsoft Windows will appear as one or more windows on the display. Any number of application programs can be displayed on the screen and the user can alternate between unrelated application programs without restarting



the system. The minimum hardware requirements for Microsoft windows on the Polo computer are 192K of RAM and a mouse. The Polo System includes 128K of RAM, color monitor, two 360 Kbyte floppy disk drives and an auto dial/auto answer modem. **Polo Microsystems**, Mountain View, CA **Write 126**

PORTABLE COMPUTER

In Color Or Monochrome



The TI portable computer is available with either a 9" color or monochrome display. The computer features graphics, color capability, memory expansion up to 768 Kbytes and internal modems. All software programs available for the Texas Instruments Professional Computer are compatible with the TI Portable Professional Computer. Features include a 16-bit 8088 central processor, a 64K RAM expandable to 768 Kbytes, five expansion slots, and a 5 1/4" half-high floppy diskette drive with space for an additional built-in disk drive option. Storage capacity of an individual floppy diskette is 320 Kbytes under MS-DOS 1.1 and 360 Kbytes with MS-DOS 2.1. The portable version will support all communication products currently available for the TI Professional Computer including TTY, 3270 and the Ether-Series of local area network products. Prices are \$2,395 (monochrome) and \$2,965 (color). **Texas Instruments**, Dallas, TX **Write 129**

GRAPHICS SOFTWARE

Scientific/Engineering Applications

Frame editor is a color graphics software package which runs on Verticom's PLP200 color graphics

terminal, and IBM PC XT, DEC VAXes, Plexus, and Onyx microcomputers. Frame editor is designed for use with a digitizing tablet or optical mouse allowing non-programmers to interactively create free-form graphic designs. The designs utilize squares, circles, rectangles, and other geometric forms in 16 colors, which are selected from a palette of 4,096. Frame Editor has applications in scientific/engineering, education, and videotex markets. Price ranges from \$500. to \$2,000. **Verticom**, Sunnyvale, CA **Write 131**

COLOR MONITOR

720 x 420 Resolution



The Color IV is a high-resolution color monitor compatible with the IBM Personal Computer and DEC Rainbow computers. It is available in two versions with either RGB analog or digital input. The monitor, using a separate interface, will display 16 colors and will accept the RS 170A, RGB signal of the DEC Rainbow. The monitor has 720 x 420 resolution and a .31mm dot pitch CRT. The unit has a 96 x 24 character display. Price is \$995. **Amdek Corp.** Elk Grove Village, IL **Write 128**

MICROCOMPUTER

256 Kbytes Memory



The Apricot is an 8086-based IBM-compatible 16-bit microcomputer. It has 256 Kbytes of main memory, three operating systems (MS-DOS, CP/M-86 and concurrent CP/M-86) and 3.5" Sony MicroDrives, each with 315 Kbytes of storage. The Apricot also includes an integral calculator and bundled executive software. An 80-character MicroScreen is built into the keyboard and displays two 40-character lines. Price is \$2,495., **ACT**, Santa Clara, CA **Write 132**

CRT DISPLAYS

With Video ICs

Models SD-U6020, SD-H2114 and GD-H3014 are color CRT displays which have regular to ultrahigh-resolution formats. They all include a MX chassis, a PCS deflection yoke, and video integrated circuits. The SD-H2114 has scanning frequency ranges of 14.75 to 25.5 kHz and is switchable to 15.75 or 24 kHz. The SD-U6020 has a horizontal frequency of 64 kHz. **US JVC Corp.**, Elmwood Pk, NJ **Write 133**

PORTABLE COMPUTERS

256 Kbyte Memory



The T-4000 and T-5000 are two portable computers which are battery-operated and have 256 Kbyte non-volatile bubble memories. The T-4000 has an 8-line x 80 character LCD and weighs nine pounds. The T-5000 has a 16 line x 80 character LCD and weighs ten pounds. Both models fit into a briefcase and have alphanumeric keyboards

COMPUTERS/SYSTEMS

with 16 programmable function keys. The computers are based on the Zilog Z80L microprocessor and use CP/M 80 or UCSD P-system operating systems. They include 64K RAM and 4K ROM. Prices are \$1,995. (T-4000) and \$2,495. (T-5000). **Teleram**, White Plains, NY **Write 130**

PERSONAL COMPUTER

With 256K RAM

The M68 is a dual CPU 8/16 bit desktop computer which utilizes a 256K chip. The M68 has 1 Mbyte memory and expansion slots for three optional memory boards of 1 Mbyte each. Its dual CPU system bases the 16 bit performance on the MC68000 (10MHz) and in 8 bit on the Z80A. It utilizes CP/M80 software and languages such as C, FORTRAN, COBOL and APL on CP/M68K. **Sord**, New York, NY **Write 134**

WORD PROCESSING TERMINAL

With Horizontal Scrolling

The CIT-500 word processing terminal is designed for use with all CIES 680 multi-user computer systems. The CIT-500 has a 64-line x 80-column screen and horizontal scrolling from 81 to 120 columns. It can create, edit and display standard text and ledger-sized documents. It has a 15" screen, and detachable keyboard. **CIE Systems**, Irvine, CA **Write 135**

MICROCOMPUTER

Based On 8088



The T300 Computing System includes a 192K computer with Intel 8088 microprocessor, 640K 5-1/4" floppy disk drive and a 12" green screen display. The system includes a 10 Mbyte hard disk, a memory expansion to 512K, a clock/calendar, and a 16 color palette. The 12" monochrome display has a resolution of 640 x 500 and the same feature is included on the optional 14" color display. Price is \$2,495. **Toshiba**, Tustin, CA **Write 136**

DESKTOP

256K RAM

The Seequa/XT desktop computer has a dual processor design (8088 and Z80) which allows it to run 16-bit IBM software. The Seequa/XT has 256K of RAM expandable to 640K, 8K bytes of ROM expandable to 48K and a 10 Mbyte hard disk in addition to a 320K 5 1/4" disk drive. Color and black and white graphics are included in resolutions of 320 x 200 and 640 x 200 respec-

tively. Other features include 5 expansion slots, a parallel printer port and a serial communications port. Price is \$3,995. **Seequa**, Odenton, MD **Write 137**

PORTABLE COMPUTER

64K RAM



The MD3 is a CP/M-based portable computer which includes two floppy disk drives and eight software packages. Features of the MD3 include 64 Kbytes of RAM, two double-sided, double-density, 5.25" floppy disk drives (400 Kbytes each), a 5 x 9" monitor with an 80-character by 24-line display, two ports, a detachable keyboard, and character-map graphics. **Morrow**, San Leandro, CA **Write 138**

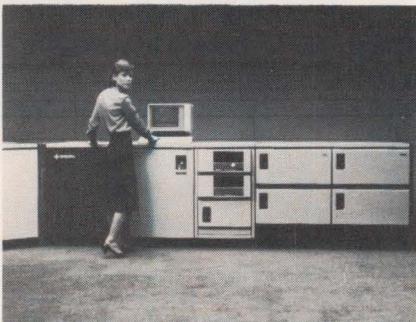
DISPLAY TERMINAL

DEC Compatible

The Ann Arbor Guru display terminal features a 15" CRT housed vertically to give the display the appearance of an 8 1/2 x 11 page, making it well suited to word-processing applications that involve lengthy documents. Memory and display formats are user-definable with a display of 66 lines of 170 columns and memory of 250 lines to 255 columns. Editing commands include erase character/area/field/line/display, insert/delete character/line, push/pop line, insertion/replacement mode, and set editing extent. A RS232 printer output can be configured for local, remote, or page print operations. A DEC mode option is available which permits the Guru to be used with standard VT100/VT52 software. Price is \$2395. **Ann Arbor Terminals**, Ann Arbor, MI **Write 139**

SYSTEM PROCESSOR

460 Mbyte Storage Capacity



The Mapper 10 is a solutions-oriented processor with 4th generation, interactive software. The Mapper 10 system configuration consists of a CPU with 524K words of memory, two fixed disk drives with a total storage capacity of 460 Mbytes, a streaming tape, one 0789 printer and a console. The system will be available in April, 1984. **Sperry**, Blue Bell, PA **Write 143**

WORKSTATION

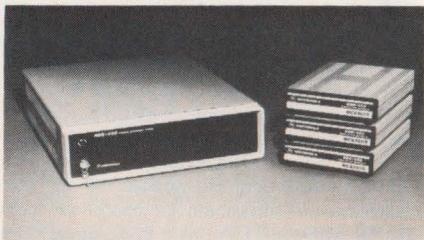
Supports One Gbyte Memory



The MegaLogician is a CAE design system which has a simulation capacity of one million gates and a performance level of 100,000 evaluations/second. The MegaLogician incorporates a multi-processor architecture which includes three micro-coded KIPS that serve as hardware accelerators and perform local high speed logic simulation. The MegaLogician incorporates Intel's iAPX80286 microprocessor and supports one Gbyte of virtual memory. It uses the Ethernet standard as its LAN protocol. The system features one to six Mbytes of main memory, four to eight Mbytes of KIPS memory, monochrome or color graphics, a 40 or 80 Mbyte Winchester disk and one Mbyte of floppy disk storage. Price is \$120,000. **Daisy Systems**, Sunnyvale, CA **Write 140**

MICROPROCESSOR DEVELOPMENT STATION

For Hardware/Software



The HDS-400 Control Station (M68K HDS400A) has been configured to operate with the Motorola VME/10 Microcomputer System and DEC VAX hosts. The emulator allows microprocessor system engineers to debug their hardware and software in the latter stages of the development cycle. The development station operates with a Motorola EXORmacs host over a 56K baud synchronous RS-422 serial link as well as with a control station which interfaces to a VME/10 host through a 19.2K baud asynchronous RS-232C serial link, or to a VAX host over a 9600 baud asynchronous RS-232C link. Two emulator modules operate with any of the four HDS-400/Host/Operating System configurations. The modules provide 8.0 MHz emulation with no user target restrictions and support 16 program breakpoints, which can be set in RAM or ROM. **Motorola**, Phoenix, AZ **Write 141**

DESKTOP COMPUTERS

IBM Compatible

The Eagle Plus XL, Eagle Plus, and Eagle Spirit, are three 16-bit computers which are IBM compatible. The Eagle Spirit is a 16-bit portable computer which includes built-in graphics and a 9" screen. The Eagle PC Plus XL desktop computer has an integrated 10 Mbytes of hard disk storage. The Eagle PC Plus is also a desktop and features one or two floppy disk drives. Monochrome and color graphics adapter boards and monitors are available as options to both Eagle PC Plus XL and Eagle PC Plus. The computers are powered by Intel 8088 microprocessor and feature 5-1/4" floppy disk and Winchester hard disk drives. The standard 128 Kbytes of RAM is expandable to 640K on the main CPU board. The design accommodates either 64K or 256K dynamic RAMs. All models have four IBM PC compatible option slots. Integrated onto the main board of each system are two serial ports and one parallel port for printer, modem or mouse connections. Prices are \$3,295. (Eagle Spirit), \$4,295. (Eagle PC Plus XL), and \$2,795. (Eagle PC Plus). **Eagle Computer, Los Gatos, CA Write 142**

COLOR MONITOR

RGB Composite

The MJ-22 16-color monitor is switchable between RGB and NTSC composite video, and compatible with the IBM PC and PCjr. The MJ-22 displays 2,000 characters (5x7) on a 80 column x 25 line screen with resolution of 506 x 240. The RGB operates at a bandwidth of 18MHz, composite at 3MHz and separated video at 5MHz. Price is \$499.95. **Teknika, New York, NY Write 146**

COLOR OPERATOR STATION

640 x 400 Resolution

The Astra 4045 color operator station features a 14", 25-line x 80-column color monitor with 640 x 400 pixel resolution. The Model 4045 is an NEC 8086-driven intelligent terminal. Text display is controlled by NEC's 7220 graphics control LSI. Eight screen colors can be displayed including red, green, yellow, blue, magenta, cyan, black and white. A graphics expansion option consists of 96 Kbyte VRAM memory and an additional 7220 controller allows pixel addressable graphics. Price is \$3,000. Graphics expansion option is \$375. **NEC Information Systems, Boxborough, MA Write 147**

MULTIFUNCTION WORKSTATION

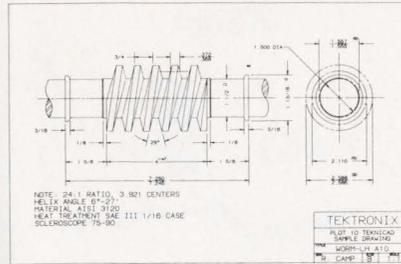
Available In Three Configurations

The 7350 Professional Computer multifunction workstation is based on the M68000 microprocessor. The 7350 features a CPU, memory, video display unit, detached keyboard, 15 Mbyte Winchester disk and two double-density, double-aided floppy diskette drives. It is available in three configurations; a single user workstation, color graphics workstation, or cluster controller console. The single user workstation comes with a graphics display, 320 Kbyte of user memory and 15 Mbyte of hard disk storage. The color graphics workstation features a 27 color palette and has 448 Kbytes of user memory. The cluster console version includes an additional 1 Mbyte of memory and allows attachment of three terminals to pro-

vide a four user cluster configuration. **Perkin-Elmer, Oceanport, NJ Write 148**

CAD SOFTWARE

Locally Stores And Redraws Sketches



PLOT 10 CAD software gives Tektronix 4100 display terminal users drafting functions for engineering drawings, illustrations, and presentation overheads. The software runs locally under the CP/M-86 OS on most Tektronix models. Drawings can be locally stored and redrawn with changes. Local zoom/pan is included. Plotting utilities support Tektronix, CalComp, Benson and Hewlett-Packard plotters. Text and geometry can be entered using the thumbwheels and a crosshair cursor. 250 levels can be specified on a drawing. PLOT 10 CAD can be configured with different sized terminals to permit more or less of a drawing to be entered and viewed at one time. Price is \$1,600. **Tektronix, Beaverton, OR Write 149**

CAD WORKSTATION

For ETP Applications



The Qubix workstation makes use of CAD input for technical publishing through interactive capabilities of both art and text. The workstation interfaces with CAD systems by IGES and Versaplot and allows CAD input database to be converted through data processing and reprocessing capabilities. Operations include object placement, scaling, enhancement of detail, and sizing. The workstation has a screen, 2240 x 1680 viewable elements, and a digitizing pen for manually drawing art. Geometrical construction of graphic entities for display and storage in a model database are supported. The Qubix configuration includes four graphic workstations for art and text. **Qubix Graphic Systems, Saratoga, CA Write 150**

STANDALONE COMPUTER

Can Be Configured As Workstation



The 16/8 Professional Computer was designed for use as a standalone computer or as a workstation in an office communications network. It includes a 16-bit processor, 128 Kbytes to 256 Kbytes of memory and an 8-bit processor with 64 Kbytes standard memory. The two processors have separate memories so operations under separate applications programs can be executed simultaneously. The 16/8 has a 12", 24-line, 80-character display screen, with high/low intensity, inverse video and graphics. An optional anti glare screen filter is available. The 16/8 includes two daisywheel printers, which operate at 20 and 40 CPS and users can choose single- or double-sided 5-1/4" or 8" disks. Price ranges from \$3,395. to \$5,295. **Xerox, Stamford, CT Write 145**

Errata

In the Technology Trend on page 20 of the November issue of *Digital Design*, we mistakenly labeled Figure 1 Calma's STICKS software on Apollo; the package actually runs on the Data General Eclipse. Calma also points out that the DDM, a mechanical design system, runs on either Apollo or DEC equipment. Several TEGAS products, developed by CGIS, now a part of Calma, run on Apollo hardware, but TEGAS 5 does not.

In the December, 1983 issue of *Digital Design*, in the article "Looking Ahead: A Forecast for the '80s" the photo on page 60 was credited incorrectly. The photo is actually courtesy Megatek Corporation, not Lexidata.

Also in the December, 1983 issue of *Digital Design*, in the article, "Engineering Workstations Meet Demands For Individual Design Needs," Figure 2 on page 88 was incorrectly identified. The photo was of AED's new Model 1024 color graphics terminal with 1024 x 768 resolution not of AED's S11 workstation.

PERIPHERALS

TABLETOP LASER PRINTER

Prints 12 Pages/Minute

The LP 4120 from Ricoh is a tabletop laser printer capable of printing 12 pages per minute. The printer employs the Ricoh LP Controller 120, which has two 128-character internal fonts. The controller also provides the printer with overlay and portrait/landscape conversion capability. A variety of interfaces are available for connecting the LP 4120 to word and data processors, electronic mail devices, local area network systems and personal computers. **Ricoh, Fairfield, NJ. Write 166**



WINCHESTER DISK DRIVES

Stores 60-80 Mbyte



The CM7000 Series are Winchester disk drives which provide mass storage in a 5.25" floppy drive package. The three-platter Model CM7660 has an unformatted capacity of 60 Mbytes and the four-platter Model CM7880 stores 80 Mbyte. Both drives have a rated MTBF of 12,000 power-on hours with an MTTR of 30 minutes. Average access times are 40 msec. Features include a preamplifier in the HDA and a track density of 1173 tpi. The drives have swing-arm head-positioning actuators, manganese-zinc heads, and a data writing density of 9275 bpi. **Computer Memories, Chatsworth, CA. Write 161**

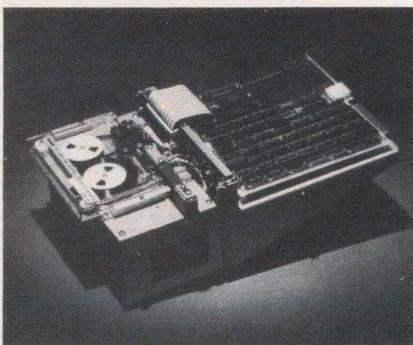
PRINTER

Seven Color Capability

The VersaPrint Model 530 is a serial dot matrix printer which has color printing and cut-sheet capabilities. Features include seven color printing, friction-feed cut-sheet and tractor-feed continuous-form paper handling. It has three print modes (draft quality at 180 cps, memo quality at 90 cps and NLQ at 45 cps). The 530 has dot addressable graphics, 10, 12, or 16.5 character pitch to print up to 224 characters per line, 55 dB operation, and a 1.5 billion character print-head. Price is \$2,495. **Lear Siegler, Anaheim, CA. Write 156**

STREAMING TAPE SYSTEM

99 Mbyte Capacity



The JetStream 16 is a streaming cartridge tape system that reads and writes as a 9 or 16 track tape with a 99 Mbyte capacity when used with 555 foot cartridge tapes. The Jet Stream 16 provides 80 Mbytes of formatted data on a DC 300XL data cartridge. The streamer also writes and reads the QIC 24 format, which provides a capacity of 45 Mbytes on a DC 300XL cartridge. It has burst transfers of 400 Kbytes/sec and an average transfer rate of 72 Kbytes/sec. The Jet-Stream 16 has a separate erase bar and utilizes a two-channel bi-directional tape head to record data on 9- or 16-tracks. It has an intelligent controller with two separate microprocessors; one for the tape drive, the other for the controller. The interface is electrically compatible with the QIC 02 interface specification. It features five buffers and block lengths of 512 bytes. Price is \$1,450. **North Atlantic Industries, Hauppauge, N.Y. Write 158**

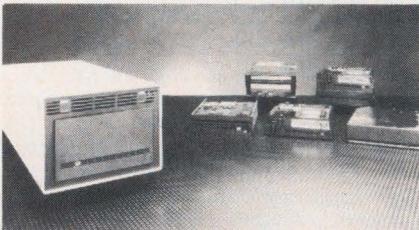
STREAMING TAPE DRIVE

330 Mbyte

The MT-1220 330 Mbyte streaming tape drive has an 8.5 by 10.2" panel footprint which is compatible with Control Data's 9715 FSD disk drive. It has a Pertec microformatter interface and the data cartridge has an unformatted capacity of 330 Mbytes. It operates in a 200 or 50 ips streaming mode or a 50 ips start-stop mode. When operating at 200 ips, it is capable of backing up a 300 Mbyte disk in 24 minutes. The 24-track, bit-serial, serpentine format is employed in the MT-1220 half-wide drive along with a packing density of 9,600 bpi (12,000 frpi). Data is encoded into a 4/5 GCR format. Price is \$4,950. **MegaTape, Duarte, CA. Write 157**

DATA STORAGE SUBSYSTEMS

10 To 40 Mbyte Capacities



The fourteen data storage subsystems from Data Technology are designed for OEMs, retailers, and other system integrators. The subsystems include standard and half-height 5.25" Winchester disks with 10, 20 or 40 Mbyte capacities, streaming tape backups with 20 or 45 Mbytes, half-height floppy disks with 2.62 Mbytes, and fixed/removable hard disk combinations with each disk carrying 5 Mbytes. All subsystems include chassis, controller, power supply, and cables. System integrators may specify data storage peripherals for integration. Using supplied peripherals, DTC will assemble, test and certify the completed subsystem. **Data Technology Corp. Santa Clara, CA. Write 162**

WINCHESTER DISK DRIVE

For Multi-User Networking

The ST8100 is a 8" Winchester disk drive, designed for multi-user networking, graphics and shared-resource systems based on super-microcomputers. The ST8100 stores 102.10 Mbytes of unformatted data. Average access time is 30 msec and the transfer rate is 10 Mbits/sec. The ST8100 drive uses three 8" oxide-coated disks, a DC spindle motor, and manganese-zinc ferrite minislidder read/write heads. A linear voice-coil motor is used for head positioning in conjunction with servo data stored on a dedicated disk surface. Price is \$1,500. **Seagate, Scotts Valley, CA. Write 160**

FLOPPY DISK DRIVE

130 Mbyte Capacity

The Model 1110 is a 130-Mbyte dual-mode, half-inch floppy disk drive. The drive is designed to provide backup for high-capacity Winchester disk drives and provides both start/stop and streaming modes of operation. Drive capacity is 130 Mbytes formatted in streaming mode at 75 ips and 83 Mbyte in start/stop mode at 50 ips. The unit searches and rewinds at 150 ips, and transfers data at the rate of 225 Kbytes/sec in the streaming mode. Price is \$1,000. **Memorex, Santa Clara, CA. Write 159**

MODEM

Features LSI

The 9629 synchronous modem features LSI and can be used as a stand-alone unit. The 9629 offers adaptive equalization, which tracks changes in line characteristics and eliminates the effect of

large variations in delay and amplitude distortion, assuring a lower error rate over unconditioned lines. The unit is available with fallback rates of 7200 and 4800 bps to accommodate deteriorated line conditions. The 9629 has a diagnostics feature which allows network monitoring by means of front-panel indicators. Price is \$2,650. **Prentice Corp.** Sunnyvale, CA.

Write 163

EXPANSION CHASSIS

LSI-11/23 Compatible

The Plessey Series 670 memory expansion chassis is compatible with LSI-11/23 computer systems, including the company's Series 6000 computers. The 670 is designed to support two Mbytes of internal memory and contains a multifunction board, memory mapping module, 25 amp power supply and cooling fan. Price is \$5,850. **Plessey Peripheral Systems**, Irvine, CA.

Write 164

PRINTER

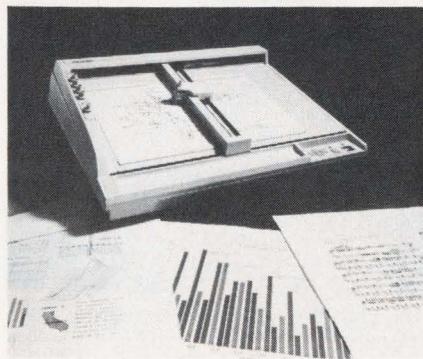
200 CPS

The LQ-1500 is a multi-function serial dot matrix printer with applications in letter quality correspondence, high speed drafts, and graphics. The LQ-1500 has a 24-pin head and printing speeds from 200 cps for high volume drafts to 60 cps for letter quality. The LQ-1500 is a 136-column printer and has 96 ASCII characters, 13 international sets and 96 italic characters as well as 128 downloadable characters. Printing is bidirectional with logic seeking. Available interfaces are Centronics 8-bit parallel and additional 2K buffers are provided with RS-232C and IEEE 488/GPIB interfaces. **Epson OEM Products Division**, Torrance, CA.

Write 165

SIX PEN PLOTTER

With Windowing Software



The Lotus 1-2-3 software driver directly drives the Amplot II, six-color, X-Y coordinate plotter. The Amplot II is a microprocessor intelligent plotter accepting ASCII commands. It has built-in software for arc and circle generation, windowing and other functions. The plotter has RS-232-C and 8-bit parallel interface. It has a 10" x 14" plotting range and automatic pen selection and is designed for business graphics or engineering applications. **Amdek Corp.** Elk Grove Village, IL.

Write 170

WINCHESTER DISK DRIVES

315-517 Mbytes Storage

The AMS571 is a 571 Mbyte Winchester disk drive with an additional 100 Mbytes of storage capacity. The 513 Mbyte SMD-compatible has eight Gbytes of on-line storage capacity. The C2075 is an operational 80 Mbyte, 8" fixed/removable disk drive. It features 53.5 Mbytes fixed storage and 26.8 Mbytes removable cartridge storage. **Century Data Systems**, Anaheim, CA.

Write 171

KEYBOARD

Twin Bifurcated Contacts

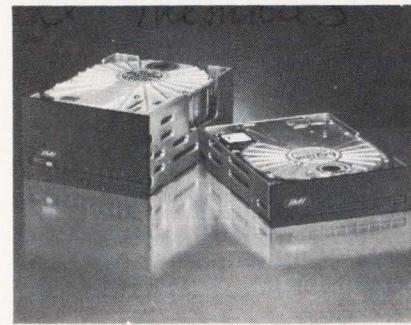


The KS-200E keyboard is designed with patented twin bifurcated contacts and has a rated life of 50 million cycles. The KS-200E is available with tactile or linear feel. Keys have a .120" stroke and typical bounce is less than one msec, with a five msec bounce over the switch life. The KS-200E is available as discrete switches or arrays assembled with or without keycaps, or assembled and soldered to a PC board with or without electronic encoding. **Stackpole Components**, Farmville, VA.

Write 172

WINCHESTER DISK DRIVES

In Full And Half-Height Models



Models 2306H and 2312H are 5 1/4" half-height Winchester drives with capacities of 6 and 12 Mbytes, and full-height models 5612H, 5624H, 5636H and 5650H have capacities ranging from 12 to 51 Mbytes. The 1.6" half-height drives have an average access time of 85 Msecs, including settling time. The 5600H series has an average access time of 49 msecs and a 51 Mbyte unformatted storage capacity and 40 Mbytes of formatted storage. **International Memories**, Cupertino, CA.

Write 173

DAISYWHEEL PRINTER

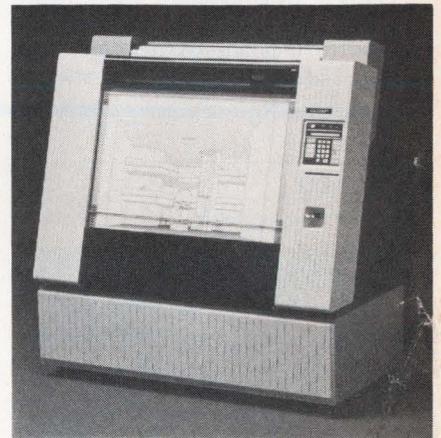
Bi-Directional Printout

The M20 is a daisywheel printer which has several interface control codes, making it compatible with other printers, including those manufactured by Diablo, Qume and NEC. It interacts with all computer/software combinations. Horizontal formats include 10, 12, 15 pitch and proportional spacing, with a line printing width of 15.7". In plotting applications its resolution is 23,000 dots/inch. The M20 is designed for bi-directional printout, at 20 cps. **Daisy Systems Holland BV**, Torrance, CA.

Write 167

DUAL-MODE PLOTTERS

21 To 52 IPS Plotting Speed



The 107X family features three plotters, models 1073, 1075 and 1077, with diagonal plotting speeds ranging from 21 to 52 ips. The plotters feature a 36" wide continuous-roll feed as well as the ability to provide 34"x30" cut sheet plots. The plotters are designed for manufacturing, engineering and design applications centered on CAD/CAM, analysis and presentation, and mapping. The 107X plotters are equipped with MC68000 microprocessors with abilities that include scaling techniques, rotation, mirroring and form alignment. Prices range from \$14,950 to \$24,500. **CalComp**, Anaheim, CA.

Write 174

FLOPPY DISK DRIVES

1.6 Mbytes To 125 Kbytes Storage

The H596-16 floppy disk drives have storage capacities which range from 1.6 Mbytes unformatted for the double-sided, double-density 96 tpi model to 125 Kbytes unformatted for the single-sided, single-density 48 tpi model. Features include a self-centering clutch, a continuous band positioner for track to track access time, a servo-controlled direct drive brushless spindle motor, and an automatic disk eject mechanism. The H596-16 is a double-sided 96 tpi drive with a memory capacity of 1.6 Mbytes and a track to track access time of 3ms. The H596-10 is a double-sided 96 tpi drive with memory capacity of 1.0 Mbyte and a track to track access time of 3ms. The H596-05 model is a single-sided 96 tpi drive with 500 Kbytes of memory and a 3ms access time. **Hi-Tech Peripherals**, Huntington Beach, CA.

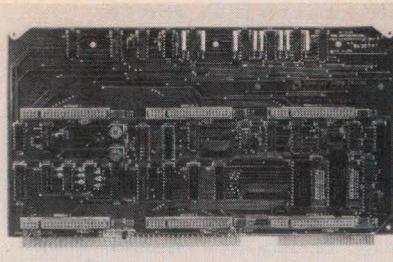
Write 175

COMPONENTS

SBX MODULES

With Dual Channel Controller

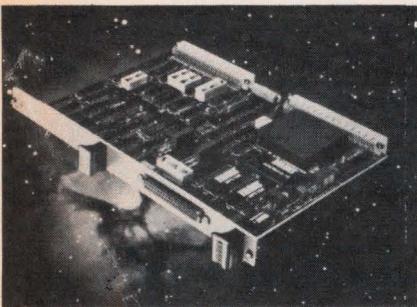
The Am94/2000 Motherboard has six SBX connectors and two SBX modules, a stepper-motor controller and a dual channel serial communications controller. The motherboard includes on-board Multibus address decoding and data buffering and Multibus/SBX timing reconciliation. The on-board SBX connectors can handle any 8- or 16-bit SBX modules and provide for six single-width modules, one double-width and four single-width modules, and two double-width and two single-width modules. The Am94/1530 is a programmable dual-channel serial communications module. The Am94/1530 handles asynchronous formats, and synchronous byte-oriented



protocols. The Am94/1541 is a programmable, single-width SBX module with an on-board 8-bit microcontroller IC. Prices in quantities of 1-9 are Am94/2000 SBX Motherboard, \$495, Am94/1530 Dual-Channel Serial Communications module, \$395, Am94/1531 Stepper Motor Controller, \$395. **Advanced Micro Devices**, Sunnyvale, CA. **Write 187**

I/O BOARD

VMEbus Compatible



The MPV901 is a 12-bit resolution 32-channel analog input, 2-channel analog output system which is compatible with - and directly interfaces to the VMEbus. The MPV901's analog input section includes; an analog multiplexer for 32 single-ended or 16 differential channels, a PGA resistor, a sample/hold amplifier, and a 12-bit A/D converter. Gains of 1 to 1000 V/V are software selectable and can be stored in on-board RAM. When instructed by the MPV901's control logic, it will set the proper gain for the channel addressed. Price in quantities of 1-9 is \$1495. **Burr-Brown**, Tucson, AZ. **Write 188**

TERMINAL CONTROLLERS

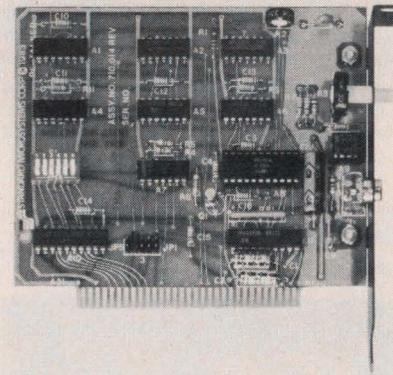
8048-Based

The NS455 series Terminal Management Processor is a family of single chip microcontrollers which include a NS456 masked-ROM version intended for high-volume applications. A ROM-less version, the NS405, is designed for use with external memory, and a pre-programmed version, the NS455, is intended for use in standard character-oriented terminals or as an evaluation tool for the series. The integrated controllers allow a 48-pin integrated circuit to replace seven separate devices usually required for terminal control. The controllers are based on an enhanced 8048 8-bit microprocessor architecture and instruction

set. The NS456 can be programmed to operate in either a character mode or graphics mode. The character font can be programmed with a character width from 6 to 10 dots and 16 scan lines per character. Graphics resolution is 640 x 325 dots. **National Semiconductor**, Santa Clara, CA. **Write 186**

SPEECH SYNTHESIZER MODULE

For IBM PC



The PC-Talker Speech Synthesizer Module provides speech capability for the IBM Personal Computer. When plugged into a spare slot in an IBM Personal Computer and connected to an external speaker, the PC-TALKER provides an unlimited speaking vocabulary by combining phonemes in the appropriate sequences. Features include fine pitch adjustment, on-board audio amplifier with volume control, and a phono connector for connecting an external speaker. Price is \$199. **Standard Microsystems**, Hauppauge, NY. **Write 190**

PROTOCOL CONVERTERS

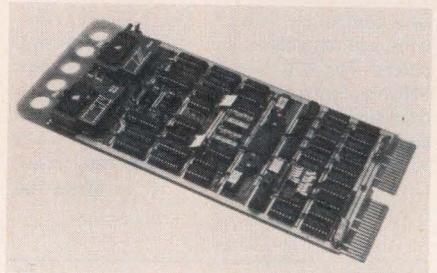
On-Board Diagnostics

The Series II Plus line of protocol converters feature on-board diagnostics. The Series II Plus 3770 allows the attachment of one to eight serial asynchronous and byte parallel devices

to an IBM SNA/SDLC network. The Series II Plus HASP attaches one to eight devices to an IBM synchronous network via IBM binary synchronous protocol. The Series II Plus 2780/3780 can connect one to three asynchronous or byte parallel devices to an IBM synchronous network via IBM binary synchronous protocol. All three Series II Plus protocol converters communicate with the host locally or via a modem utilizing EIA RS-232-C interface. **KMW Systems**, Austin, TX. **Write 191**

EPROM PROGRAMMING SYSTEM

For DEC LSI-11 Microcomputers



The System PR77EX is an EPROM programming system for the DEC LSI-11 microcomputer. It includes a PC board, software, user manual and two pairs of EPROM adaptor plugs. When configured as two independent channels, the PC board will permit programming of two EPROMs with identical data, or with alternating address bytes simultaneously. The board provides user access to 24/28 pin ZIF sockets with the board operational in the LSI-11 card cage. The PR77EX will program all 24 and 28 pin EPROMs requiring a single 5v supply voltage. The PR77EX includes 30 bits of latched TTL output, 16 bits of latched TTL output, two programmable DC converters ported offboard via switching and hardware timer pulse output. Price is \$880. **Interplex**, Mountain View, CA. **Write 189**

6-BIT CMOS CONVERTER

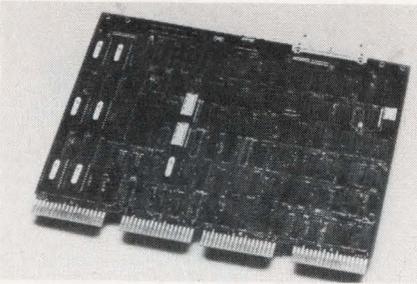
20 nsec Aperture Time



The TML1060 6-bit converter utilizes a flash technique which results in a sample aperture time of 20ns. +3.2 and -3.2 volt references set the converters full scale range and drive an internal 20 KΩ typical resistor network with 64 taps. Applications include; A/D conversion, transient signal analysis, optical character recognition, ultrasound signature analysis, high-energy physics research, motion signature analysis, and general-purpose hybrid ADCs. The converter has separate analog and digital grounds and operates from ±5V supplies. Price in quantities of 100 is \$16.00. **Telmos**, Sunnyvale, CA. **Write 205**

TAPE COUPLERS

For 1/4" Streamer

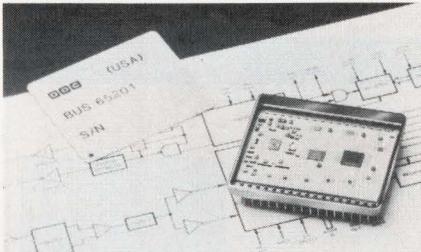


The TC05 and TC15 tape couplers provide software transparent storage and backup using a 1/4" cartridge tape drive with any of DEC/s LSI-11, PDP-11, MICRO/PDP-11, or VAX-11 series CPU's. The TC05 tape coupler supports 22-bit addressing and provides 4 Mbyte memory on the LSI-11/23 Plus and Micro-PDP. 16-bit NPR data transfers are handled by both couplers. Internal self-test diagnostics are performed automatically during power-up and errors are flagged with a fault-indicator LED. Both controllers incorporate a 3.5 KByte data buffer. Prices are \$1,300. (TC05) and \$1,400. (TC15). **Emulex**, Costa Mesa, CA.

Write 203

RTU HYBRID

With Encoder/Decoder



The BUS-65201 Data Bus Dumb RTU hybrid contains a transceiver, encoder/decoder, control logic, dual rank I/O registers and an internal clock generator. The BUS-65201 provides flags to the subsystem when Broadcast, Mode Code and Own Address commands are decoded. Features include 8-, or 16-bit, 3-state parallel or serial I/O and controls for single or dual redundant data bus configurations. Price is \$801. **ILC Data Device Corp.** Bohemia, N.Y.

Write 202

SYNCH TO SYNCH CONVERTERS

Supports IBM 2780/3780

The 3770 Synch-Synch and the Hasp Synch-Synch are two protocol converters which allow the communication of batch data between synchronous protocol devices and synchronous host computers. The 3770 communicates via standard synchronous protocols to IBM/SNA/SDLC host computers. Protocols supported by the 3770 include IBM HASP, 2780/3780, and 2770, Honeywell GRTS, Univac 1004, and CDC 200 UT. The HASP Synch-Synch converter communicates with IBM, CDC or Univac hosts which utilize HASP protocol. The HASP Synch-Synch converter supports the same devices as the 3770. **Datagraph**, Austin, TX.

Write 200

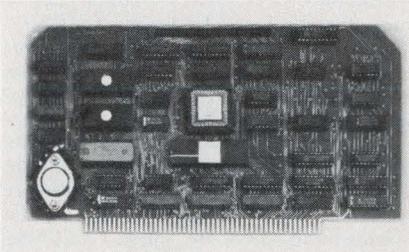
INTERFACE**Connects IBM Mainframe To Ethernet LAN**

The Model 8911A interface connects IBM and plug compatible mainframes to an Ethernet LAN. The 8911A connects directly to the programmable channel interface and emulates an IBM control unit, (such as a 3803/2803 Mag Tape Controller of a 3272 Terminal Controller). Software is available for a variety of Ethernet protocols including a version that achieves speeds of 200 Kbytes/sec. Standard protocols and customized packages can be obtained through Auscom. **Auscom**, Austin, TX.

Write 199

PROCESSOR BOARD

1 Gbyte Virtual Address



The Lightning 286 processor board utilizes an Intel 80286 micro processor to provide compatibility with 8088 and 8086 software. The Lightning 286 has as an option, a 5 Mhz 80287, which provides IEEE standard floating point math which can be used for programs having a mix of floating point operations and control structures. The 80286 operates at a clock rate of 6 Mhz and the Lightning can run at rate of 10 Mhz. It has 16 Mbyte physical address space and a 1 Gbyte virtual address space. Four operating systems are available; MS-DOS, CP/M-86, and MP/M-86. Price is \$1,395. **Lomas Data Products**, Westborough, MA.

Write 198

GRAPHIC UPGRADES

For Dec VT100

The SG480, SG481, and SG482 are graphic upgrades for the DEC VT100, VT101, and VT102. Features include 800 x 480 resolution and Tektronix 4010 and 4014 emulation with enhanced graphics module. All models have 4096 addressability, variable character sizes, variable line types, point plot, incremental plot, write thru mode, and crosshair cursor.

Selanar Corp., Santa Clara, CA. Write 204**SWITCHING REGULATORS**

10-100V Input

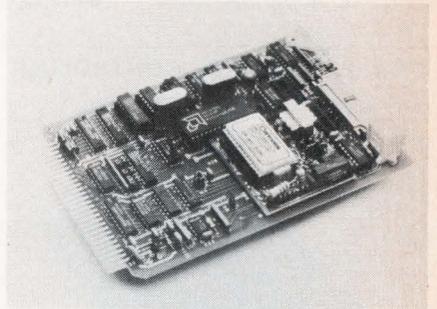
The HS7067 and HS7107 are hybrid switching regulators designed for use in floppy and hard disk drives, robotics, computer and display terminals, data acquisition systems, industrial control systems, portable instrumentation and printers. The devices are housed in a TO-3 package containing a temperature compensated voltage reference, a pulse-width modulator with programmable oscillator frequency, error amplifier, high current, high voltage output switch and steering diode. The HS7067 has 10V to 60V input, is output adjustable from 3V

to 55V, and frequency adjustable to 300KHz. The HS7107 has 35V to 100V input, is output adjustable from 5V to 95V, and frequency adjustable to 150KHz. **National Semiconductor**, Santa Clara, CA.

Write 197

MODEM BOARD

Bell 103/202 Compatible

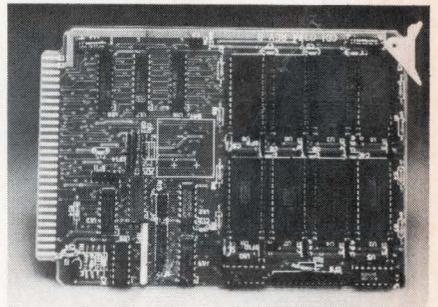


The SB8630 is a Bell-compatible modem board that allows STD Bus systems to use telephone lines for data communication. The SB8630 can be used full-duplex at 300 baud, or half-duplex at 1200 baud. Features include auto-answer, auto-dial, and auto-originate for both pulse and touch-tone dialing. An RS-232C or RS-422 serial I/O port is used by the SB8630 to interface with STD Bus systems. An analog loopback test performs diagnostics for checking system readiness, and a buffered audio output provides line monitoring. Price, in quantities of ten, is \$540 each. **Micro/sys**, La Canada, CA.

Write 209

MEMORY CARD

64K RAM



The SRAM-64 static memory card contains 64K of static RAM. It is compatible with STD Bus systems and CPU types, and requires no refresh hardware. On-board RAM may be placed in the 64K memory map, and multiple cards provide 128 Kbytes using the memory expand line. The SRAM-64 will accommodate standard byte-wide memory devices, such as EPROMs and EEPROMs. Features include static operation, 6 MHz operation, buffered STD Bus lines, and user selectable card address. Prices start at \$240. **Computer Dynamics**, Greer, SC.

Write 196

8-BIT MCU

4144 Bytes ROM

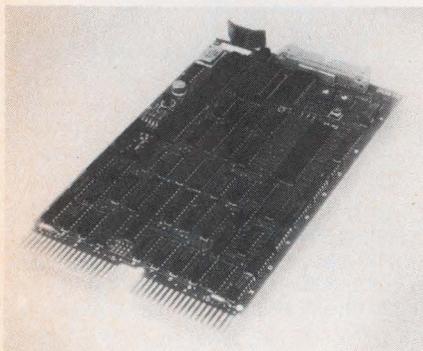
The MC68HC05C4 is an 8-Bit single-chip MCU fabricated in high-density, silicon gate CMOS (HCMOS). The MC68HC05C4 operates at frequencies of 2.1 MHz (5V operation)

COMPONENTS

and 1.0 MHz (3V operation) down to D.C. It utilizes a M6805 instruction set and includes a 6801 type, 3-function, 16-bit free-running timer. Two serial message systems are supported on the MC68HC05C4. Other features include 4144 Bytes ROM, 176 Bytes RAM, 24 bidirectional I/O lines, a serial communications interface, a serial peripheral interface and self check. Price in quantities of 1,000 is \$9.50. **Motorola**, Austin, TX. **Write 195**

5 1/4" FLOPPY DISK CONTROLLER

Interfaces Q-Bus To SA450 Drives



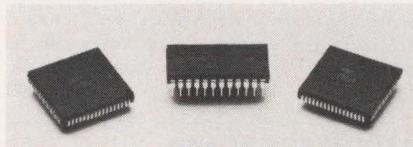
The DQ619 5 1/4" Floppy Disk Controller interfaces LSI-11-11/23PLUS, MICRO/PDP-11 computers to one or two 96TPI double sided, double density 5 1/4" floppy drives having a SA450 interface. The controller is con-

tained on a dual height PCB that includes control and interface electronics for RX02 emulation supported by DEC RT-11, RSX-11 and RSTS. The DQ619 has 22-bit addressing, a media present monitor, data buffer, 16-bit CRCC and on board self test. Price is \$595 in quantities of 50. **Dilog**, Garden Grove, CA.

Write 201

VLSI CHIP SET

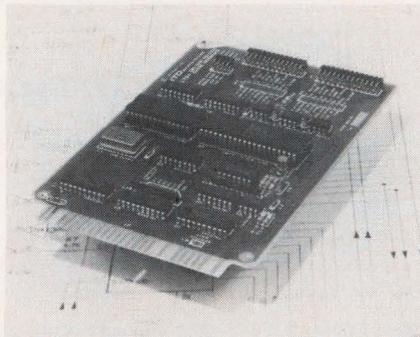
For Custom Design



The PFM 5000 Controller Chip Set is a third generation CMOS/VLSI for custom and/or multi-function controller designs. The set features consecutive sector transfers, ECC error detection and correction, 2.0 Mbyte data transfer rates, and intelligent buffer management. It includes a data sequencer, four channel memory controller, and a MFM data separator. Buffer memory is provided with 16 bit DMA (65K) and programmable memory cycle times. The Data Separator chip has rate control to 10 Mbits/sec, internal VCO and phased lock loop, address mark detection and generation, and write precompensation. Prices in quantities of 10,000 are \$5.75-30.51. **Omti**, Campbell, CA. **Write 206**

SERIAL INTERFACE

STD Bus Compatible

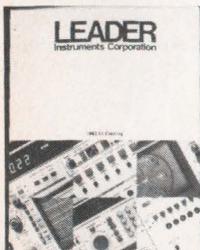


The Model 5370A is a dual RS-232C serial interface which is STD Bus compatible. It contains two software programmable asynchronous or synchronous (SIO/O option) RS-232C serial channels. The serial channels have software baud rate selection and an optional crystal referenced baud rate oscillator. The external RS-232C interface is DCE or DTE configurable. Both serial channels can operate with an external bus master (DMA), with the DMA trigger outputs connected at the top of the module. The remaining two (2) counter/timer channels may be used for external interrupts, event counting, or time tick generation. Price is \$175 (2.5 MHz), \$200 (4.0MHz), and \$235 (6.0 MHz.) **STD Microsystems**, Palo Alto, CA. **Write 194**

New Literature



M-12 memory and logic board test system



Test System Brochure. This brochure describes the M-12 board test system from Micro Control Company. The system evaluates boards containing memories such as RAMs, ROMs and PROMs. The M12 can also test boards with a mixture of logic and memory devices, microprocessor based boards and boards with buried memory. Applications for the test system include engineering characterization, production testing and failure analysis. **Micro Control Company** **Write 254**

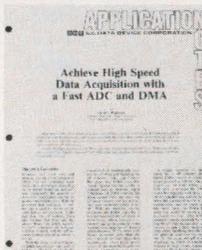
Capacitor Data Sheet. This data sheet from the Capacitor Div. of TRW offers engineering specifications for its laser-produced gauge 80 Series capacitor. The sheet includes performance, applications, packaging, dimensions and testing specifications for the 2 pin-DIP capacitor. The TRW 80 Series capacitor is designed for use in coupling, decoupling and bypass applications in digital and analog circuitry. **TRW** **Write 255**

Test and Measurement Catalog. This catalog from Leader Instruments Corp. describes their line of test and measurement instruments. Featured are two oscilloscopes in a 100 MHz and 50 MHz versions. Calibrators included are four frequency counters ranging from 80 MHz to 1 GHz as well as a dual channel auto-ranging AC millivoltmeter. **Leader Instruments** **Write 256**

Graphic Plotter Brochure. This brochure from Nicolet Test & Measurement group describes precision digital instruments used for problem solving in science and industry. Graphics plotters, logic analyzers and digital oscilloscopes are included, as well as photographs and summaries of the products. **Nicolet** **Write 266**

Data Acquisition Application Note. This four page application note from DDC describes using a DMA Controller for transferring high speed ADC output directly into memory without microprocessor intervention. The note outlines the role of the DMA Controller as a dedicated high speed circuit and covers the ADC to microprocessor interface and the software required for this task. The note contains descriptions of five additional data conversion devices available from DDC. **DDC** **Write 252**

Graphics Terminal Brochure. This four color brochure describes the graphics and display capabilities of the GVT Graphic Display Terminal from Human Designed Systems. Features of the terminal, including its ANSI X3.64 functionality, Tektronix 4010/4013 compatibility, DEC VT100 software compatibility, and switchable 80/132 column capability are also described. **Human Designed Systems** **Write 267**

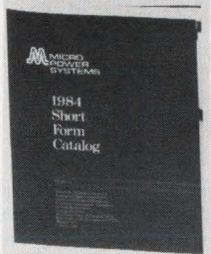




Product Catalog. This 1983 20-page product selection guide is available from General Instrument Microelectronics. The guide features specs. and brief descriptions of ROM, EEPROM, Microcomputer, Audio, Video, Data Communications, Telephony, and Semiconductor microcircuits.

General Instrument

Write 262



Power Systems Catalog. This B/W, 12-page catalog lists all of the current and new products from Micro Power Systems for 1984. Five product areas are covered: military ICs, voltage references, dual transistors, op amps and DACs. The DACs range from 6- to 18-bits, and op amps from OP-01 to OP-227. The parts are tabulated for reference, including electrical characteristics. All devices listed come in dice form and with 883B processing.

Micro Power Systems

Write 258



Communications Report. This technical report entitled "Communications Between Programmable Controllers in the Industrial Environment" from Reliance Electric discusses applications for communications networks, known as LANS. Performance criteria are analyzed, such as speed, distance and node, and reliability requirements. Alternatives for implementing communications networks are offered. Topology alternatives are analyzed, and available software protocols are compared.

Reliance Electric

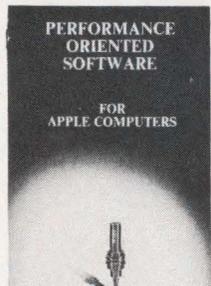
Write 264



Logic Device Catalog. This short form catalog from SGS Technology describes the HS-C2 MOS family of logic devices. The products are pin compatible with LSTTL and 4000B industry standard types. Features such as speed, power, fanout and noise immunity are covered. Fourteen tables list the specifications and technical characteristics of the entire HS-C2MOS line.

SGS

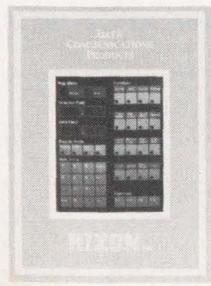
Write 253



Software Brochure. Brochure lists HI-compatible software for Apple™ users. This brochure from Houston Instrument provides Apple computer users with a list of compatible vendor-supplied software to drive HI plotters. The listings include information about applications, system configurations, and minimum plotter language and cost. The brochure is one in a series of folders for users of micro, mini and mainframe computers who are researching software to drive HI plotters.

Houston Instrument

Write 250



Data Communications Catalog. This catalog from Data Communications Products describes their line of communications products. Each product includes a description and photograph. The catalog covers multiplexers, high and low speed modems and auxiliary equipment.

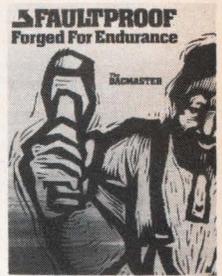
Rixon

Write 263

Fault-Tolerance Brochure. This brochure from Autech Corp. describes the Faultproof extension of fault-tolerance for hostile industrial automation applications. The brochure includes information on the company's Dacmaster data acquisition and control system which is designed to operate on the production floor without benefit of a control room. Also covered are a process control software system, and a dual active, high-speed local area network, called Masterlink.

Autech

Write 251



Data Sheet. This 16-page, four-color data sheet contains specifications for the Model 6000 Instrumentation Computer from Wavetek. The Model 6000 features multi-tasking, memory with parity check, extended BASIC with I/O instructions, and structured programming. It includes an A/D converter and a built-in clock with internal and external interrupt. Included are six pages of hardware and software specifications, and a list of options such as cables, accessories, peripherals, software and manuals.

Wavetek

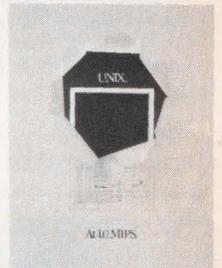
Write 259



Operating System Brochure. This four-page brochure describes Computer Automation's implementation of the UNIX System III operating system on the company's dataCASE/5 super minicomputer system. The dataCASE/5 has 1.0 MIPS of processing speed, 560 Mbytes of data storage with a 30 ms average access time and a 5.0 Mbits/sec data transfer rate with plated media 5.25" disk drives.

Computer Automation

Write 260



Acquisition Systems Journal. This technical journal from Analog Devices discusses data acquisition systems and components. Covered in this issue is a single-board data acquisition system offering industrial signal conditioning and a BASIC programming language. Other application articles cover software for industrial measurement and control, a data acquisition information system and ground rules for high-speed circuits.

Analog Devices

Write 261



Drafting System Brochure. This brochure includes specifications and a price list for the IBM XT/PC 68000 two-dimensional drafting system with three-dimensional modeling. For CAD purposes, the system has color graphics, a display with 1024x1024 resolution, and 3-D modeling capabilities.

Summit CAD Corp.

Write 265



Test Equipment Catalog. This catalog from LDJ Inc. describes their line of magnetic testing equipment. The publication provides a brief description of each product, including those used in microprocessor controlled instrumentation. The catalog is intended as a reference for magnetic instrumentation and applications support.

LDJ

Write 257



February 28 - March 2

State-of-the-Art Robot Systems Course. Boston, MA. Contact: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Place, Los Angeles, CA 90045. (213) 417-8888.

March 6 - 9

Designing Effective Man/Machine Interfaces Course. Boston, MA. Contact: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Place, Los Angeles, CA 90045. (213) 417-8888.

March 13 - 15

CIMCOM Conference. Washington, D.C. Contact: Computer and Automated Assoc. of SME, One SME Dr., PO Box 930, Dearborn, MI 48121.

March 19 - 21

Third Annual Phoenix Conference on Computers and Communications. Phoenix, AZ. Contact: Susan C. Brewer, Honeywell, LCPD, MS/Z22, PO Box 8000 F, Phoenix, AZ 85066.

March 19 - 21

1984 IEEE International Conference on Acoustics, Speech, and Signal Processing. San Diego, CA. Contact: Stanley A. White, Rockwell International (BB85), PO Box 4192, Anaheim, CA 92803.

March 20 - 22

Fifth Annual AFCEA Intelligence Sympo-

sium. San Diego, CA. Contact: Nancy Clancy, (619) 225-8401.

March 20 - 23

Computer Graphics Course. Baltimore, MA. Contact: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Place, Los Angeles, CA 90045. (213) 417-8888.

March 21 - 22

1984 IEEE VLSI Test Conference. Atlantic City, NJ. Contact: Dr. Ned Kornfield, Widener College, 14th and Chestnut Sts., Chester, PA 19013. (215) 499-4055.

March 21 - 23

International Symposium on the Performance of Computer-Communications Systems. Aurick, Switzerland. Contact: Harry Rudin, IBM Aurick Research Laboratory, Sautmerstrasse 4, CH-8803 Rushchlikon, Switzerland.

March 25 - 30

Seventh International Conference on Software Engineering. Orlando, Florida. Contact: 71CSE, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

March 26 - 28

GI/NTG Conference on Architecture and Operation in Computer Systems. Karlsruhe, W. Germany. Contact: H. Wettstein, Institute für Informatik, III, Univ., of Karlsruhe, Karlsruhe, W. Germany.

March 26 - 30

EDA 84, European Conference on Electronic Design Automation. Warwick Univ., England. Contact: IEE Conference Dept., Savoy Pl., London WC2R OBL, UK.

March 28 - 30

Frost & Sullivan's Sixth Annual Computer Graphic's Conference: Forecast and Assessments. Miami Beach, FL. Contact: Carol Sapchin, Frost & Sullivan, Inc., 106 Fulton St., New York, NY 10038.

March 30

International Workshop on Models and Languages for Software Specification Design. Orlando, Florida, UK. Contact: Robert Babb, Dept. of Computer Science & Engineering, Oregon Graduate Center, 19600 NW Walker Rd. Beaverton, OR 97006.

April 2 - 4

CAD '84 6th International Conference and Exhibition on Computer in Design Engineering. Brighton, UK. Contact: Ms. Joanna Wexler, Butterworth Scientific Ltd., PO Box 63, Guildford, GU2, 5BH, UK. Tele. 0483-31261.

April 3 - 5

International Teleconference Symposium. Philadelphia, PA. Contact: Conference Administrator, ITS, c/o COMSAT, 950 L'Enfant Plaza, S.W., Washington, D.C. 20024.

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