

# DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

OCTOBER 1984

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- MICROFLOPPIES SQUEEZE THEIR WAY INTO THE MARKETPLACE
- DEC CONTROLLER DESIGNS IMPLEMENT DIGITAL STORAGE ARCHITECTURE
- ARTIFICIAL INTELLIGENCE
- WORKSTATIONS ■ PRINTERS



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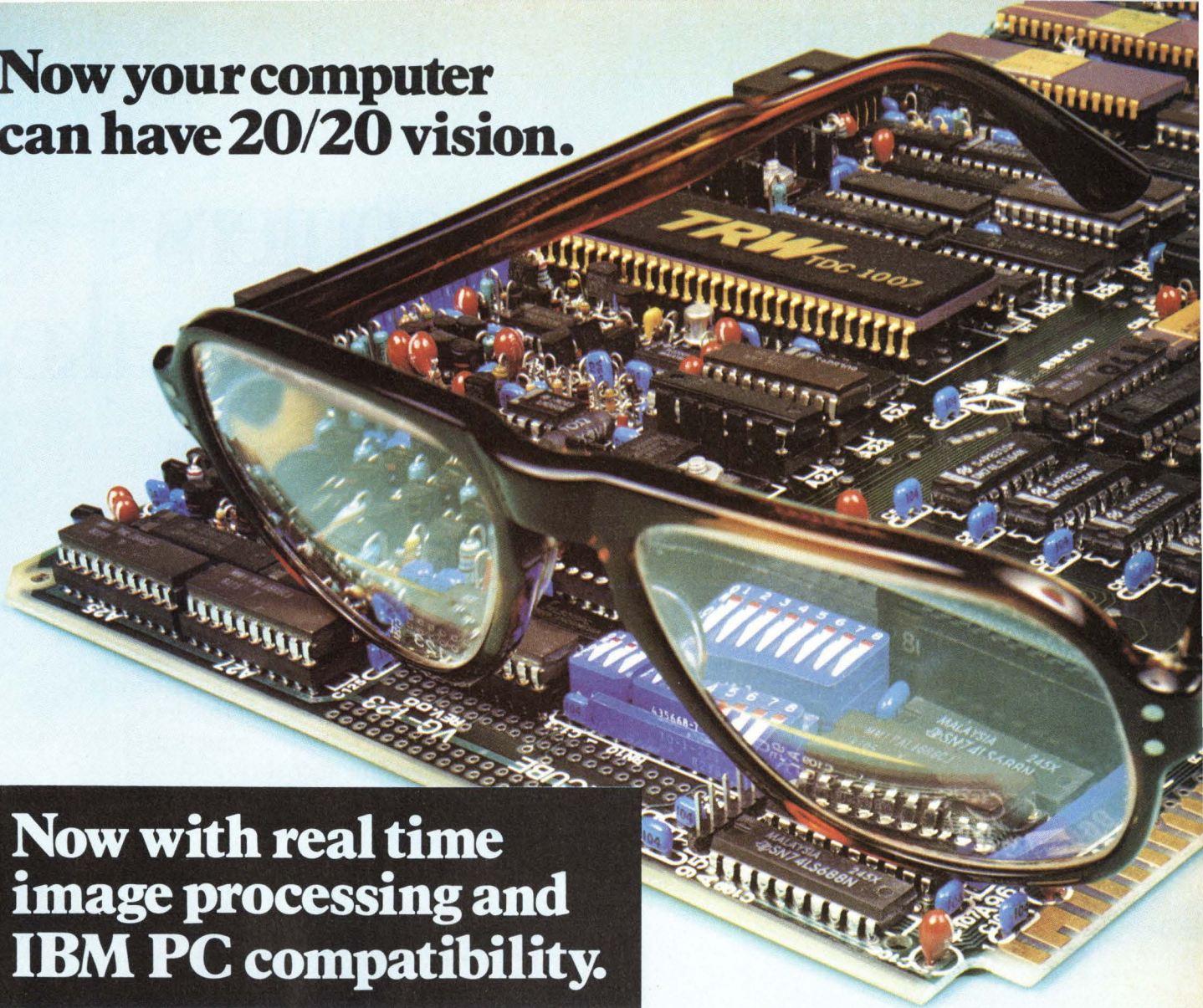
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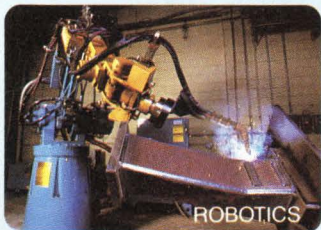
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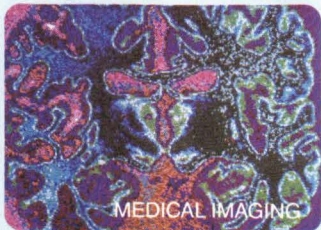
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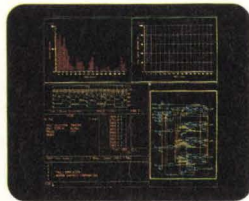
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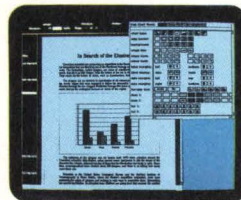
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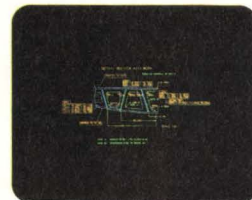
From left to right  
application software from:  
Mentor Graphics Corp.,  
Interleaf,  
Auto-Trol,  
Swanson Analysis  
Systems, Inc.,  
Racal-Redac,  
Automated Impact,  
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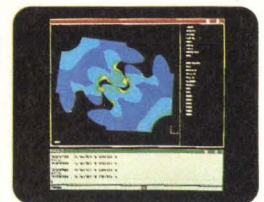
Logic design  
simulation.



Documentation  
with  
integrated  
graphics and  
text.



Design  
drawing of a  
bulkhead.



Finite  
element  
analysis of  
gear cluster.





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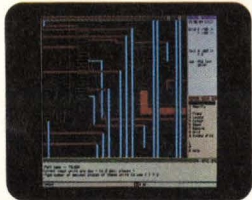
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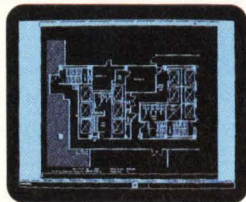
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# apollo



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circuit board  
layout.*



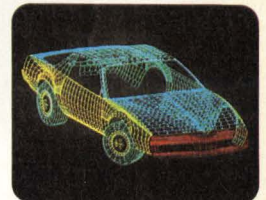
*Space plan  
of a  
facility.*



*Exploded  
solid model  
of an  
automobile.*



*Relational  
database  
management  
system.*

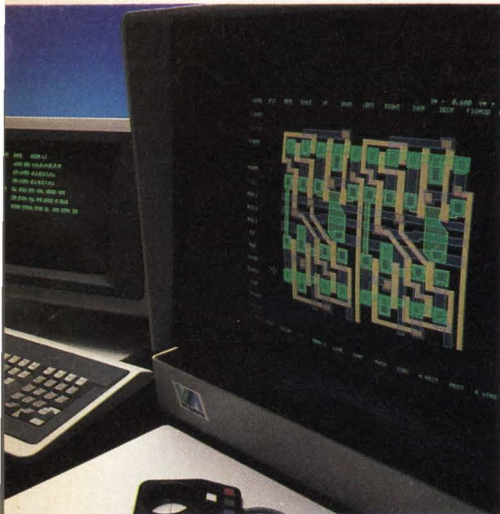


*3D surface  
model.*



Write 6 on Reader Inquiry Card





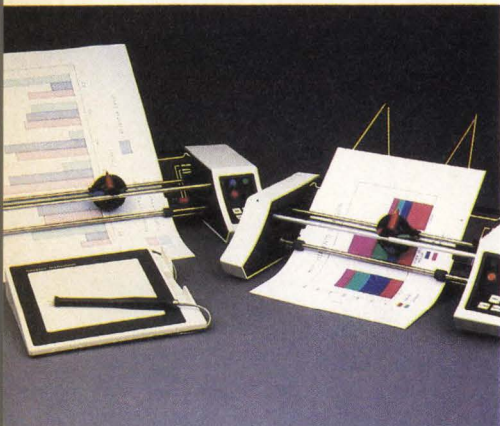
COURTESY VIA SYSTEMS

54 Engineering workstations



COURTESY GE

88 Microflops move ahead



COURTESY HOUSTON INSTRUMENT

104 Plotters for PCs

## DEPARTMENTS

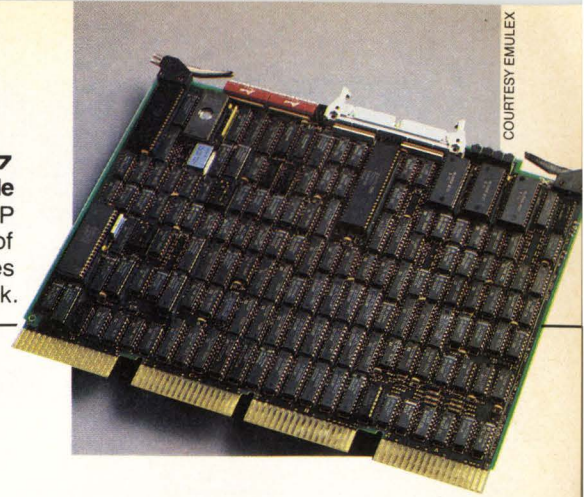
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DECs DSA MSCP  
supports all types of  
storage technologies  
including tape and disk.



## FEATURES

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by Ronald Collett

With an abundance of CAD/CAE tools on the market, the question arises of whether a particular workstation is superior to another. According to present CAD/CAE users, fully integrated systems, portable software and a full line of engineering application programs are the characteristics most frequently demanded.

### **67** **Designer's Guide To The Q-bus/Unibus**

by Dave Wilson

Introduced two years ago, the Digital Storage Architecture and Mass Storage Control Protocols are aimed at increasing performance by partitioning system functionality. This may present some thorny problems for third parties trying to emulate DEC designs.

### **78** **AI Makes The Transition From Theory To Practice**

by Gregory MacNicol

AI is being utilized in pattern recognition, robotics, speech recognition, simulation, and not surprisingly, in theoretical computer model building. Though some of the promising work is many years away from substantial rewards, some of the results are being witnessed now in small but effective ways.

### **88** **Microflops Squeeze Their Way Into The Market**

by Julie Pingry

Microflops must provide specific benefits to win over the established 5¼" products. The end-user considerations around which microflops were conceived must be what users truly want.

### **96** **Dot Matrix Printers Approach Letter Quality**

by Andrea Coville

With the implementation of sophisticated electronics, ribbonless ink systems and printheads with high pin counts, dot matrix printers have emerged as intelligent devices for the high speed, color graphics and near letter quality applications, making them the most popular computer hardcopy output devices.

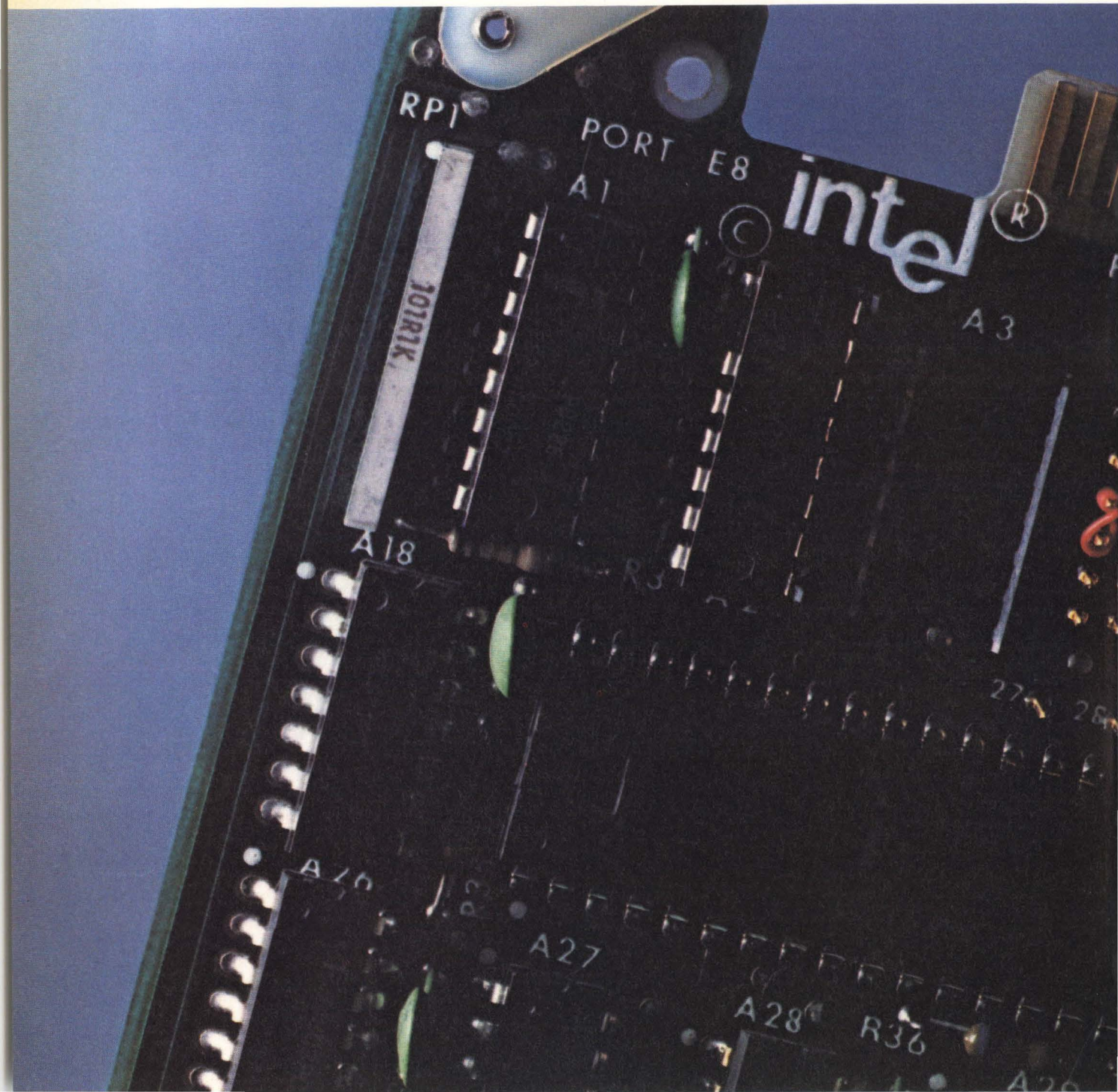
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## ON THE COVER

The capacity of floppy disks may increase dramatically with the combination of flexible ferric oxide magnetic media and a rigid plastic substrate. Stretch Surface Recording (SSR) disks from 3M have flexible recording media stretched between hub and rim. The technology of the hard substrate could allow recording density rivaling Winchester with easy removability for disks from 8" down to 3½"-3" microflops. Photo courtesy 3M.



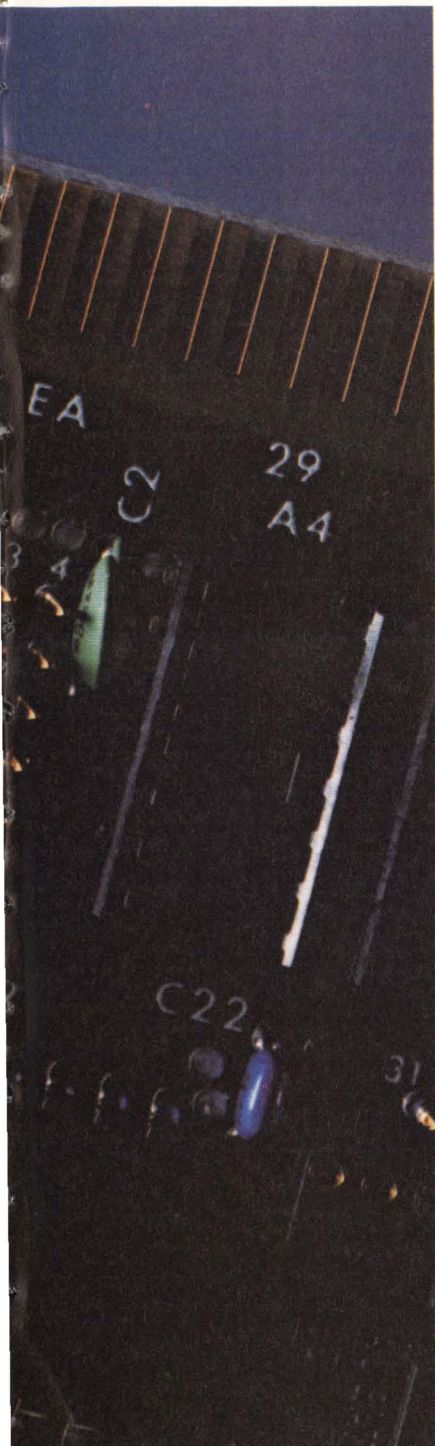
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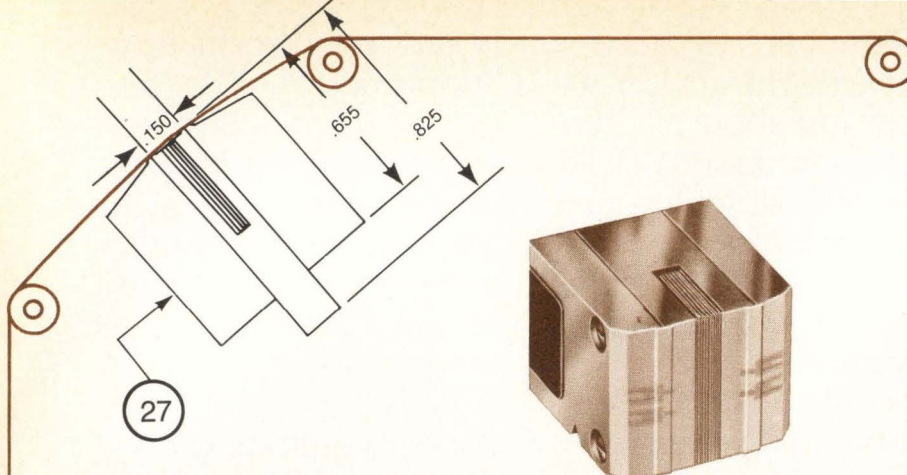
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Write 51 on Reader Inquiry Card

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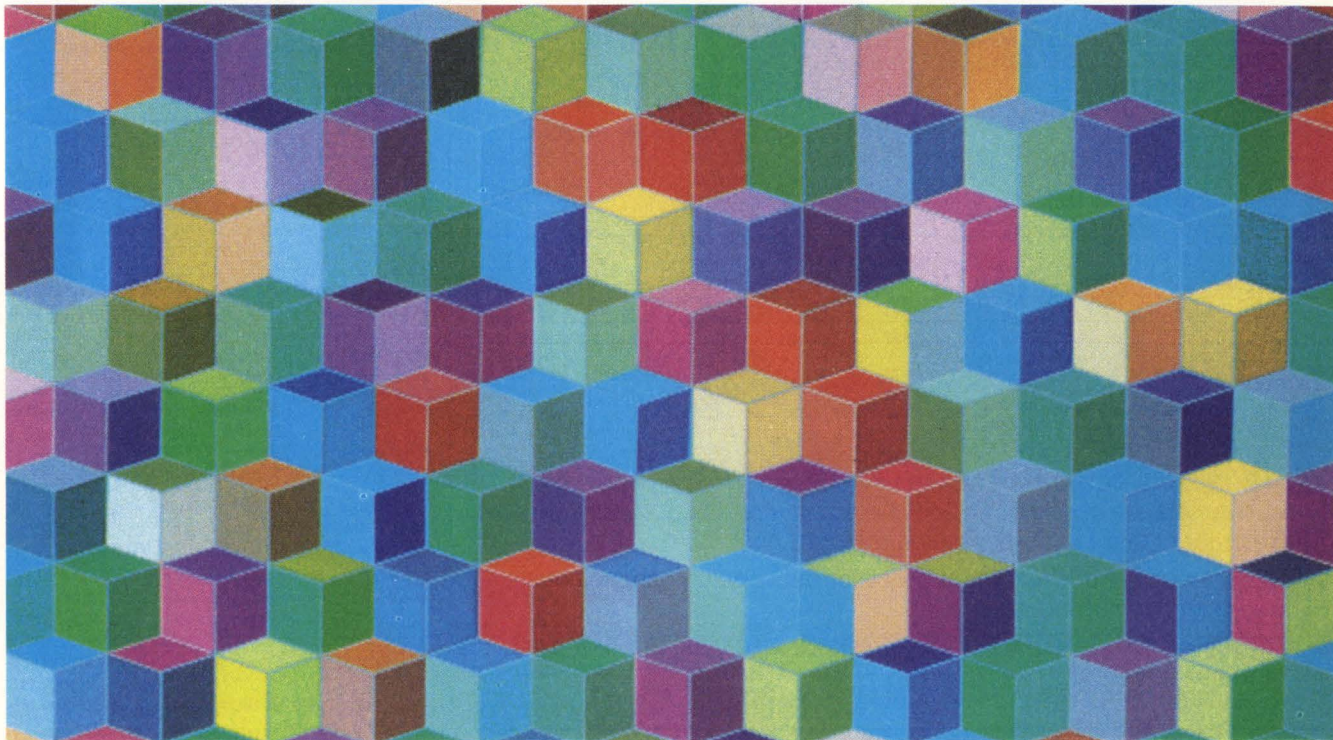
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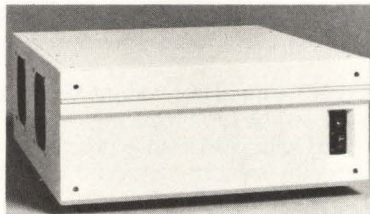
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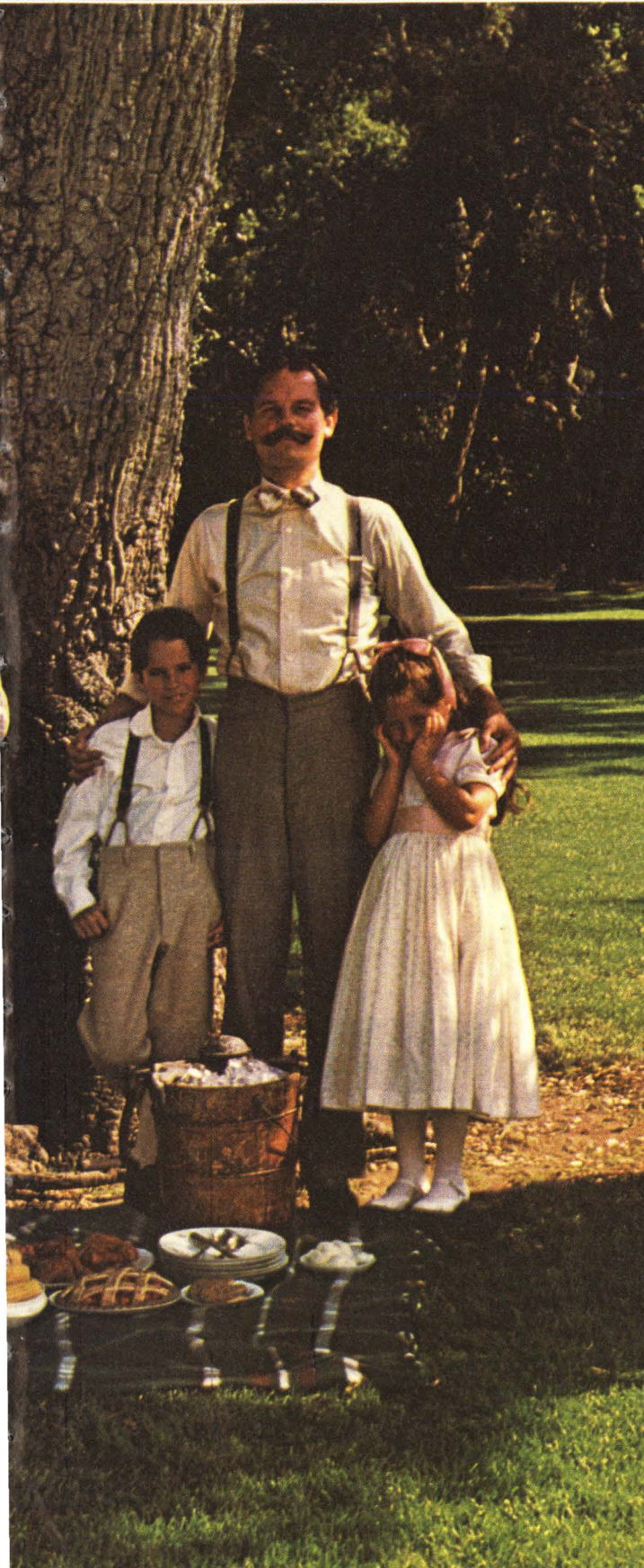


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‘With the introduction of workstations from the large vendors, smaller vendors must look hard at ways to improve the performance of their next generation products.’

## EDITOR'S COMMENT

**A**lthough still in its infancy, the workstation marketplace is maturing at a rapid pace. Early entries were primarily from small startups, however, recent announcements have been made from industry heavyweights, such as Tektronix, Data General and Prime Computer.

The distinctions between many of these workstations have become a blur. Most manufacturers today claim 16/32-bit  $\mu$ P-based machines that run the UNIX operating system, offer Ethernet local communications and allow OEM system enhancements through the provision of a standard bus adapter to Multibus or other standards.

With the introduction of machines from the larger vendors, smaller vendors must look hard at ways to improve the performance of their next generation products. Because color graphics is an important factor in workstation design, one enhancement many vendors are currently investigating is the use of custom graphics devices, such as those offered by Weitek. Others are taking advantage of modern computer architectures, such as RISC (Reduced Instruction Set Computer). This concept, developed at UC Berkeley, is based on a computer having very few instructions that execute very fast, one instruction per machine cycle.

Other companies are looking at ways of implementing advanced techniques such as dynamic load balancing, and allowing for off-the-shelf CPUs to be added incrementally into a system, linearly increasing their processing power.

In this issue, Ron Collett, Technical Editor, takes a look at some of the workstations available in the market today, and Gregory MacNicol, West Coast Technical Editor, examines the implementation of the RISC architecture, on which Ridge Computers (Santa Clara, CA) has based its new workstation. Although Digital Equipment Corporation has not offered a workstation product *per se*, the MicroVAX 1 and, subsequently, the MicroVAX 2 and 3, will offer an environment many systems OEMs will find attractive, primarily due to the large installed base of application software written under VMS for the design environment.

One area of workstation performance addressed by DEC relates to the design of high performance disk and tape controller interfaces and subsystems. In the workstation environment, disk access times are critical, especially when designing hardware to work with operating systems that fragment data like UNIX. DEC addressed this issue for its VAX line over two years ago when it announced its Digital Storage Architecture, building intelligent controller products and partitioning system functionality between the CPU and the disk drive. This, in turn, has presented some opportunities for third parties who are



building products to conform to the architecture

In the "Designer's Guide to the Q/Unibus," many of the leading controller houses were approached and asked to predict where they think DEC may take their architecture next, and describe some of the problems they faced when designing around the DEC specification. The trend toward providing more intelligence within a disk drive is evident industry wide — not just at DEC.

One problem facing the disk drive manufacturers is what route to take in implementing an imbedded controller — whether to use an existing design, to use off-the-shelf parts or to go the custom route. In this month's issue, Erik Walberg from Priam discusses the trade-offs used in the design of a SCSI product for his company.

One direction all workstation vendors will undoubtedly be moving towards will be the field of artificial intelligence. According to Gregory MacNicol, who prepared this month's Advanced Technology Series on the subject, much of the more promising work is many years away from substantial rewards, even though some of the results are being witnessed in the marketplace today. Most of the larger computer companies are already in the field, some with associated workstations. IBM, DEC and Data General have all announced products specifically aimed at AI and expert system development at the last Artificial Intelligence Conference in August. Interest in the field is increasing at a remarkable rate and soon there will be a growing number of tools, languages and methods provided by new start-ups entering the field.

AI, itself, is often thought of in connection with so-called fifth generation computers. The November and December issues of *Digital Design* will include a special two-part report on computer architectures. Prepared by Ron Collett, Part 1 will examine the limitations of the von Neumann architecture, and Part 2 will look at alternatives that may be implemented in the near future, including data flow architectures.

Advanced workstation designs, coupled with developments in graphics and artificial intelligence, will provide ever-increasing sophistication of tools to meet the design needs and narrowing market windows over the next few years.

**Dave Wilson, Executive Editor**



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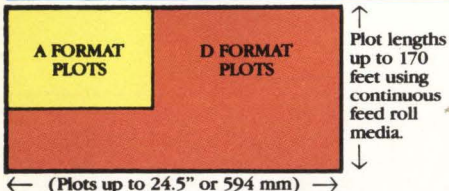
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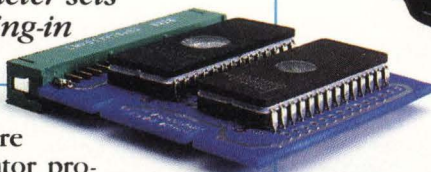


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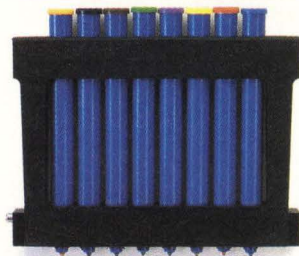


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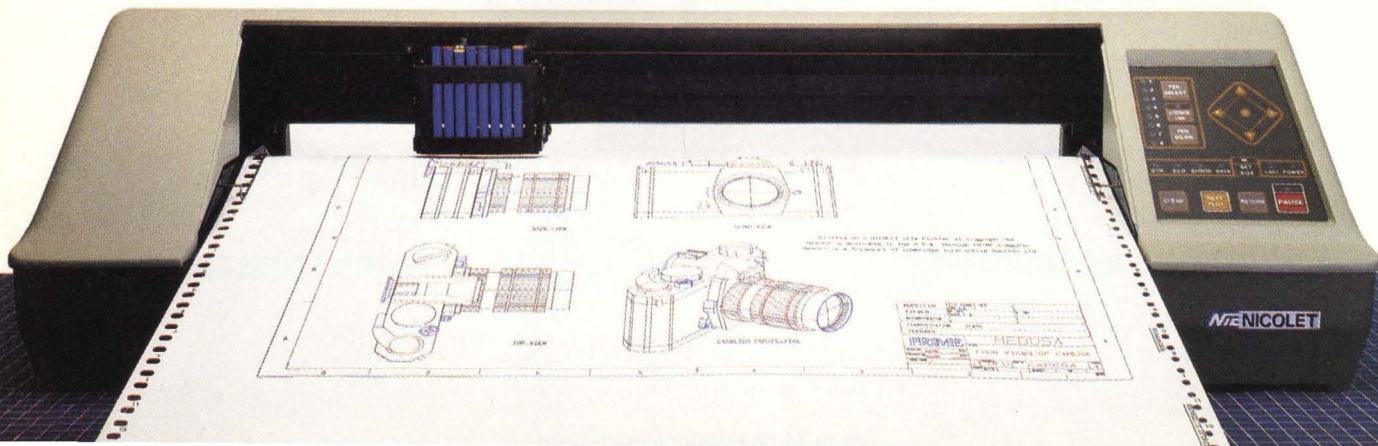
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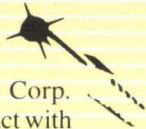
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## Product Technology Collaboration

Western Digital (WD) will grant VLSI Technology, Inc. (VTI) second source rights on the WD2123 (DUAL UART), WD1933/1935 (SDLC), WD9216 (DATA SEPARATOR) and selected disk controller products. The companies will also jointly develop key Megacell building blocks based on WD's product architectures for use in custom IC designs. VTI will implement several WD disk controller products in a mutually agreed upon CMOS technology with VTI and WD having co-ownership rights to the CMOS version.

## Fiber Optics On GSA Schedule

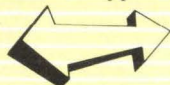


Artel Communications Corp. signed a one-year contract with the Government Services Administration (GSA) allowing US Government and military organizations to directly purchase Artel fiber optic video, audio and data communications systems from GSA's Authorized Communications Schedule Price List. Artel's fiber optic transmission systems are used for tactical and fixed military applications, including mobile teleconferencing and weapons range testing by the Army, Navy and Air Force.

## Knowledge Engineering

IntelliCorp and Symbolics, Inc., will cooperate in the enhancement of product design and marketing for IntelliCorp's Knowledge Engineering Environment (KEE) system and the Symbolics 3600 family of computers. Each company will assist each other in increasing product sales and licenses through product demonstrations, development and distribution of sales literature and cooperative customer support.

## MMG Multibus Standard



The Multibus Manufacturers Group (MMG) announced plans for promotion of the Multibus standard in the computer industry. The MMG members decided to form "action teams" to plan and implement group activities in six areas: Trade shows; Advertising, Public Relations & Collateral; Multibus Literature Kits; Market Research; Technology; and Sales Aids.

## Programmable Controllers For China



Gould Inc. signed a 10-year licensing agreement with the China National Machinery and Equipment Import and Export Corp., Beijing, People's Republic of China, for the manufacture and assembly of programmable controllers for industrial computers. The programmable controllers will be distributed and sold in the Chinese industrial markets for factory automation applications.

## INMOS, Racal-Redac Marketing Agreement

Under an agreement between Racal-Redac and INMOS, Racal-Redac will market a complete hardware/software package which INMOS developed for designing its transputer and other complex VLSI products. The INMOS VLSI design system uses a special-purpose graphics workstation that allows hierarchical design management, logic and circuit design through a high-level hardware description language, mixed-mode simulation, and mask layout with interactive design rule checking. The package will form a part of Racal-Redac's recently introduced CIEE (Computer Integrated Electronic Engineering) capability.

## D/CAS Votes on 40MB Drives



The decision to draft product standards for 40 Mbyte data cassette drives was adopted unanimously by member companies of the Working Group for Data Cassette Drive Compatibility (D/CAS). The members also agreed to define modifications for downsizing products to 3½" form factor, to study requirements for selective file overwrite, and to explore use of ¼" tape in a cassette package.

## Sony Enters OEM Market

Sony Corp. of America has announced the formation of Sony Component Products Div. Sony currently markets components and professional equipment including 3.5" microfloppy disk drives, computer memory devices and audio and video equipment for the OEM market.

## Supercomputers Available to Researchers

The National Science Foundation (NSF) has selected Boeing Computer Services to supply accredited scientific and engineering researchers with up to \$2.6 million in CRAY-based supercomputer processing services during the next 12 months. NSF is funding the program to facilitate access to large-scale computers by researchers and enhance progress in several areas of scientific and engineering education and research.

## Disk Backup for NCR



NCR Corp. will purchase from Cipher Data Products Inc. its Microstreamer dual-density 1600/3200 bpi ½" streaming tape drive for high-capacity disk backup on a wide range of NCR computers. The 3200 bpi provides 92 Mbytes of unformatted data storage and reduces storage costs compared to other peripheral packages with similar capabilities.

## Alternate-Sourcing For High-End Linear Circuits

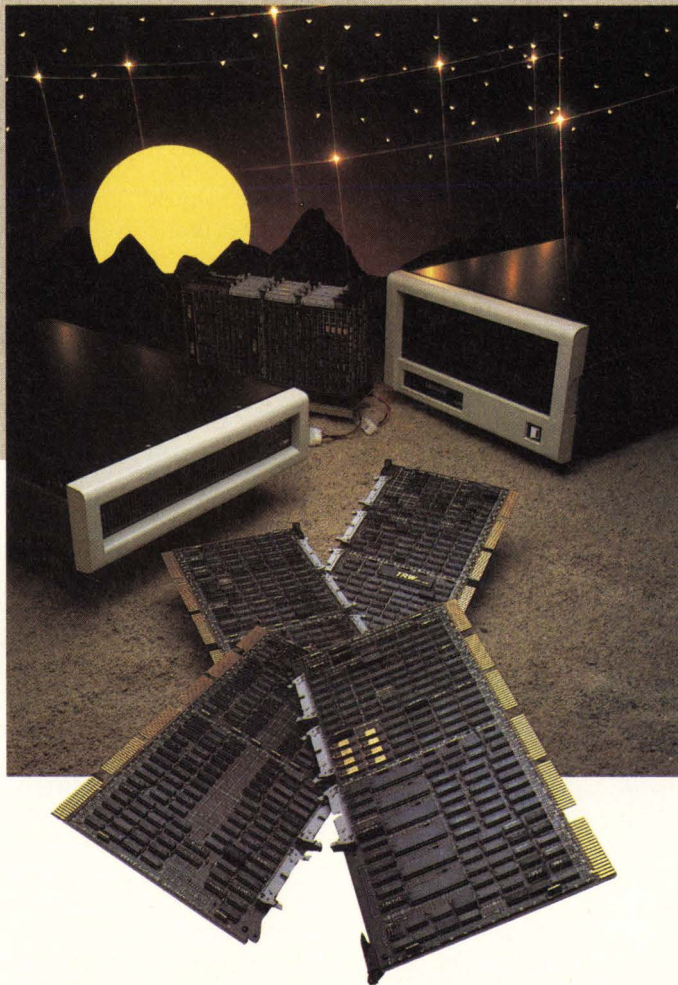
Linear Technology Corp. and Signetics Corp. signed a worldwide alternate-sourcing agreement covering Linear's high-performance ICs and Signetics' small-outline (SO) packaging technology. Under the agreement, Linear Technology will provide tooling, design and test procedures covering two previously announced low-noise, high-speed, precision operational amplifiers, the LT-1012 and the LT-1037. This enables Signetics to become an alternate supplier of these high-end linear circuits.

## Software Development

MDB Systems, Inc. and American International Communications announced an agreement for AIC to provide data communications software for MDB communications peripheral hardware products. Under the terms of the agreement, AIC will provide ongoing DCS (Data Communications System) products supporting MDB JFEP11 and DMF32 communications peripheral controllers. AIC will provide products including electronic mail interfaces, IBM interfaces and microcomputer to mainframe interfaces.



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# WASHINGTON REPORT

by Anne A. Armstrong

## Guidelines For Computer Shipments To Soviet Bloc

In the first large-scale revision since 1976 of the Military Technologies List, the 15 nations that make up the Coordinating Committee for National Strategic Embargoes (CoCom) have drafted new rules for selling to Soviet bloc countries that make it easier to ship 8- and 16-bit micros, forbid shipments of most superminis and mainframes, and require licenses for everything else.

Machines that cannot be shipped under any circumstances include those with .5 Gbyte of virtual memory, any computers with a processing data rate of 48 million bits per sec or faster, any equipment which could be used to upgrade an existing Soviet computer, any large bubble memory storage device, and computers used for microelectronic manufacturing or design.

Eight- and 16-bit off-the-shelf micros that have not been "ruggedized" or modified for combat can now be shipped without any special license. Most 32-bit microcomputers will require individual unit licenses; however, the precise regulations will not be completed and published until fall.

Originally, US officials had been pushing to require even 16-bit micros to get licenses for export. While trade associations were lobbying hard to get current export regulations eased. The 32-bit level for licensing is a compromise US officials agreed to in order to get approval from CoCom countries on other issues.

Also included for the first time in the controls is a large body of software including programs for online transaction processing, distributed database management systems, various CAD/CAM packages, artificial intelligence, and a variety of others.

Added to telecommunications controls were digital switched communications systems and terminal and transit switches used in networks.

## Navy Bars Personnel From Non-DOD Conferences

In an attempt to further restrict leakage of "sensitive" technical information, Navy Vice Admiral R. A. Miller said that the Navy "does not want Navy Material Command personnel actively participating in non-Department of

Defense sponsored symposia, conferences, or other similar forums on weapons and associated technologies and related subjects."

The instruction was included in a memo, written in the spring, but brought to light later as some civilian personnel from the Naval Research Laboratory were required to give up teaching engineering courses at night at George Washington University in Washington, D.C.

A Navy spokesman told *Digital Design* that although there is no specific Navy policy concerning participation in commercial or professional seminars that OP NAV instruction 5510.IG discusses in general terms, the necessity of clearing topics and appearances in advance and warns personnel to be alert that no sensitive material is disclosed. He said the Navy was not aware of any other command instituting a similar policy, but there was no requirement to notify the Navy headquarters with such information.

"We tend to hear about such things from the press because a person affected is unhappy and talks to the media," he said.

A broad interpretation of Adm. Miller's memo could preclude participation by a large number of scientists in professional meetings. How strictly the directive will be enforced is not yet clear.

## RTCA Undecided On Portable Device Interference

The Radio Technical Commission for Aeronautics (RTCA) has been wrestling for almost a year with reports that computers and other portable electronic devices used in flight have interfered with plane navigation and control systems. Reports of incidents in flight led several airlines to ban the use of computers in flight.

After nine months of testing and investigation, the RTCA committee has not been able to build a conclusive case for barring the devices, nor has it been able to give them an absolutely clean bill of health.

A compromise plan, currently under discussion, would recommend to the airlines that passengers not be permitted to use any portable electronic device during takeoff or landing, and would

propose to the Federal Communications Commission that the spectrum used by aircraft be protected by a higher radiation limit than the rest of the spectrum. This would permit passengers to use devices certified as within the FCC limits during the major portion of the flight.

## Congress Must OK Laser Printer Purchases

Although the prices for laser printers have fallen dramatically in recent months, approval procedures in the federal government make laser printers more difficult to purchase than daisy wheel printers and may affect the future market for both.

Daisy wheel printers are considered computer peripherals and are available freely in the government computer store or from a General Services Administration approved list of vendors. An office that has the budget can buy whatever machine it wants.

Laser printers are another matter. Because they have "font capability," they are considered printing devices and must be approved by the Joint Committee on Printing. Some government officials say this distinction is a holdover from the days when laser printers cost \$100,000 and were indeed designed for large scale printing.

Thomas J. Kleis, staff director for the JCP, says the approval process is part of an attempt to make certain that offices purchase the right equipment for the job. JCP is currently seeking approval of a plan that would require all government offices to submit printing management plans. Once the plan is approved, he said, a request for a piece of equipment can be issued very quickly. "We are trying to get away from a lot of ad hoc equipment requests," he said.

In the meantime, the perception in many government offices is that it is much easier to get a daisy wheel printer than a laser one.

## C3 Wins GSA Contract

C3 Inc. of Reston, Va., has received a \$73 million contract from the General Services Administration to provide up to 4,299 Convergent Technologies workstations to various government offices over the next nine years. The contract calls for installation, software, training and system maintenance.



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# DISPELLING THE MYTH ABOUT SINGLE CHIP MICROCOMPUTERS.

This is the first in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors — what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.



Single chip microcomputers are marvels of advanced electronic technology. Going beyond even the tiny architectures of today's general-purpose microprocessors, they combine the functions of multiple chips to form a single-device solution. Indeed, they are awesome machines.

But after their introduction, myths grew up around MCU's. Designers believed that they were difficult to design with; that there wasn't sufficient hardware and software support for them; that those who selected them would get a Sisyphus Complex. Sisyphus, you remember, is the character in ancient Greek mythology who was condemned forever to push a rock up a hill. Just as the rock reached the top, it escaped Sisyphus and rolled back to the bottom.

Some MCU's, no doubt, deserve the stigma of this myth. But one definitely does not. Zilog's Z8<sup>®</sup> MCU Family. For there is more than enough evidence to prove that the Z8 chip is not only the fastest MCU around, but it's the easiest to work with, too. In fact, it should be the chip of choice for any dedicated control applications that must get to market

on time — even if you need large quantities of them to fill your needs. Because the Z8 device is available now for off-the-shelf delivery.

But what does ease of design mean to you? What do you look for when you select a chip? What do you need to make your job easier? Whatever it is, you'll find Zilog provides everything you need, and more:

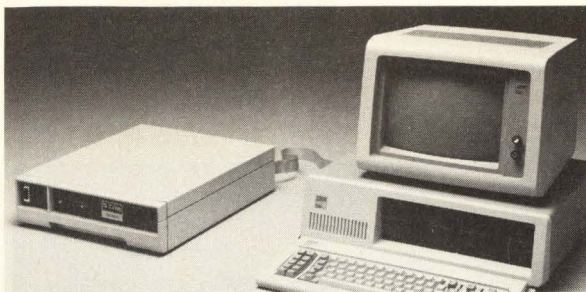
- Hardware and software development tools
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Zilog's Z-SCAN 8 is an in-circuit Emulator with a combination of hardware and sophisticated software that gives you efficient, interactive emulation of the entire family of Z8 microcomputers. By the simple exchange of target devices, the selected Z8 MCU can be emulated in a real-time mode that gives you the ability to inspect and control the



tested environment. It also gives you real-time trace speed up to 12 MHz, two breakpoints, single-step capability and extensive mappable memory. All to ensure that you get an accurate simulation of your Z8 operating environment.



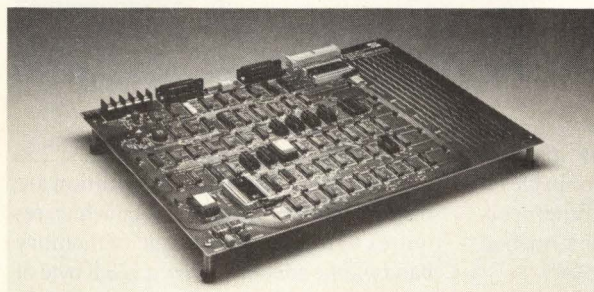
The Z-SCAN 8 Emulator is a combination of hardware and firmware that allows efficient, interactive emulation of the Z8 MCU. When hooked to an IBM PC software host, Z-SCAN 8 provides real-time, in-circuit development system capabilities. The Z-SCAN 8 will connect easily to other PC's making it a highly versatile unit.

The Z-SCAN 8 operates with both Zilog systems and other 8-bit development systems running CP/M\* and/or other operating systems. Its standard RS-232 serial link makes it particularly useful with the IBM PC and other CRT terminals. Hardware and software debugging is fast and convenient. Two screens display the status of the Z-SCAN 8 monitor and Z8 MCU target resources. Target memory can be displayed and modified in a scrollable window. Moreover, the Z-SCAN 8 is interactive and easy to use. Commands are selected from menus and command arguments are self-prompting.

The set-up procedure and initialization for the Z-SCAN 8 is done for you—a unique feature in itself. The Z-SCAN 8 is designed to reduce design time. But it's not the only time-saving device Zilog provides for the Z8 MCU.

## THE Z8 MCU DEVELOPMENT MODULE CUTS HARDWARE AND SOFTWARE DEVELOPMENT TIME.

The Z8 Development Module (DM) features two 4K Z8 devices on a single-board microcomputer. It's designed to assist you in the development and evaluation of hardware and software designs based on the Z8 MCU. With it, you can easily build a prototype using the Z8 prototyping device, and then develop code that will eventually be mask-programmed onto the Z8 on-chip ROM.



The Z8 Development Module allows you to build a prototype using the Z8 prototyping device, thereby developing code that will eventually be mask-programmed into the Z8 on-chip ROM. The Module is a single-board microcomputer system designed to develop and evaluate hardware and software designs based on the Z8 family.

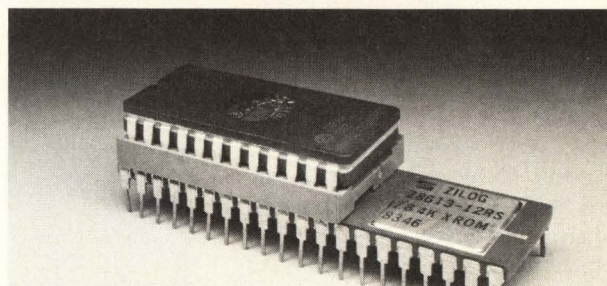
The Development Module connects to the CRT terminal and host system through two on-board RS-232 serial ports. So the DM fits between the CRT and host. A simple command makes the DM transparent in the serial path, which allows software

to be developed on the host-resident assembler without disconnecting the DM from the CRT and host.

The DM has a range of features to make Z8 designs easier than you ever thought possible: • 4096 bytes of static RAM for convenient creation and debugging of user code; • an on-board socket that tests user code in a 2716 or 2732 EPROM; • up to 4096 hardware breakpoints on address compare that can cover the entire internal ROM space; • a wire wrapped area for prototyping; and much more.

## Z8 MCU DEVELOPMENT SOFTWARE SPEEDS UP DESIGN TIME.

Zilog also provides you with a growing library of sample programs and convenient assembler packages to help you get started testing your Z8 MCU designs. In our Subroutine Library, for example, there's our arithmetic subroutine, an I/O subroutine and a general control subroutine. What's more, there are several versions of the Z8 device: a 2K and 4K ROM version; a ROMless version; and a Protopak for prototyping. Each offers different memory addressing structures. Zilog is developing more all the time. Plus, there's an existing software base for all the Z8 MCU's. We can provide you with samples of designs currently in use.



The Z8613 MPE is used for prototype development and preproduction of mask-programmed applications. The Protopak is a ROMless version of the standard Z8611, housed in a pin-compatible 40-pin package.

## SERVICE AND SUPPORT AT EVERY LEVEL FOR YOUR Z8 MCU DESIGNS

From the factory to the field, Zilog provides support at every level. A worldwide field sales network stands ready to help you with both hardware and software support. And you can get all the Z8 MCU's you need right now. Yields for the device are up 40%, and price reductions reflect our new supplies. What's more the upcoming Z8 Super 8™ promises a smooth migration path for today's Z8 MCU family.

Zilog's Z8 single chip microcomputer. Believe the myths. Or get the facts. If bringing your product to market is important to your business, then design with the part that does more for success than any other. The Z8 MCU makes getting over the design hill and into production a lot easier than you might think.

For more on the Z8 MCU, send for our complete overview or call our Literature Hot Line at 800-272-6560. For seminar dates and locations, or information on Zilog training, call (408) 370-8091. Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.

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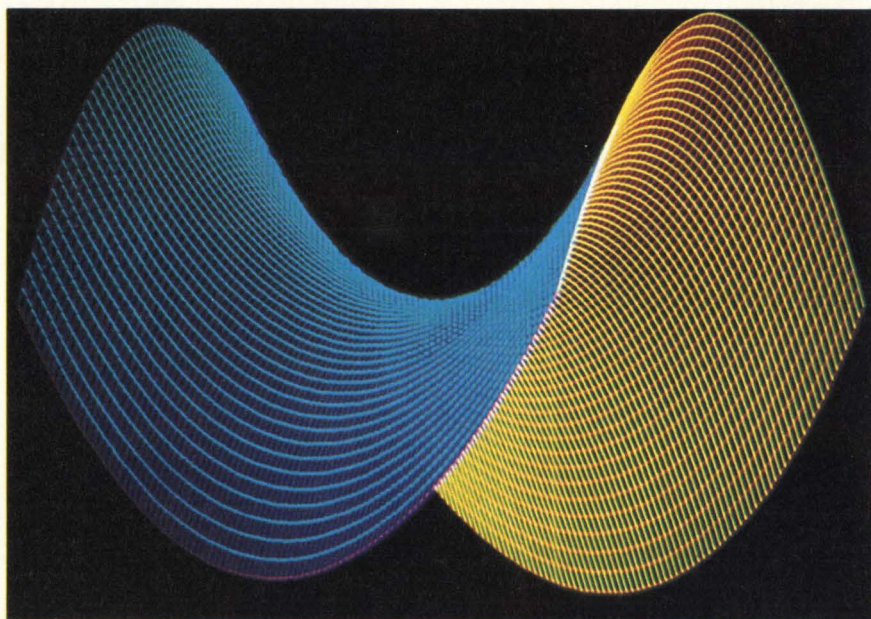
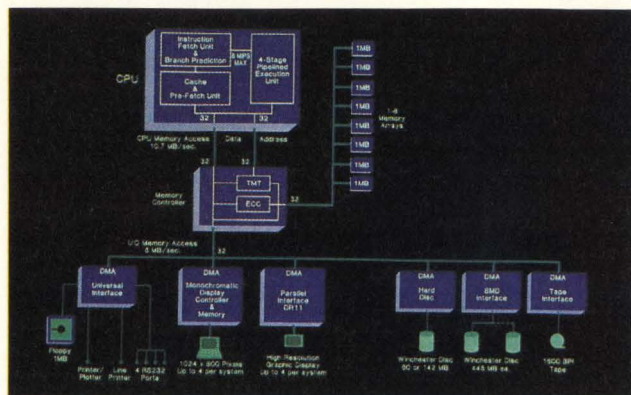
## Ridge Implements RISC-Based Personal Workstation

Mainframe systems offering great speed and power, suffer from a common problem; they are typically shared. As a result, users often never see the capability of the mainframe unless they use it during off hours. Ridge Computers (Santa Clara, CA) offers, not only a very fast mainframe, but a personal workstation aimed at applications where a user must optimize functionality rather than share it. Applications such as animation, CAD, or execution intensive situations require optimized performance not often experienced when timesharing a large centralized host. Recently, the trend has been toward smaller systems that use fast LANs for information sharing. The advantage of smaller systems is less initial investment and avoiding a whole department waiting idly while a down system is being repaired.

The Ridge 32S is totally compatible with their larger version, the 32C. The 32S is a full 32-bit machine based on standard Schottky bipolar components rather than a microprocessor. In addition, the architecture is an implementation of the reduced instruction set computer (RISC). The concept, developed at UC Berkeley, is based on a computer having few, but very fast, instructions that execute one instruction in one machine cycle. The Ridge differs from the full RISC implementation in avoiding the use of custom VLSI, use of paged virtual memory, addressing of half, full and word-and-half instructions, and fast context switching supported by hardware. The RISC concept, in addition to four-staged pipelined architecture, cache and branch prediction, 375 nsec memory access time, and a 125 nsec clock cycle time allows faster performance than a VAX. The puzzle benchmark, for example, is five times faster on a Ridge than on a VAX11/780 with a floating point accelerator.

The 32S consists of the 28" x 17" x 30" desk-sized unit, a 14", 78-Mbyte Winchester disk and a double-sided, double-density floppy disk. The computer does not require air conditioning and is designed to be very quiet. Using the UNIX system V/4.2 BSD operating system, the 32S comes with a Pascal compiler, C compiler, multi-window text editor and utility system. Third party software supporting the 32S includes mechanical and elec-

*The Ridge 32S, manufactured by Ridge Computers, is a 32-bit, single-user workstation capable of executing up to 8 million instructions per second (8 MIPS). It features virtual memory, four-stage pipelined architecture, and an operating system designed to support scientific, engineering, and graphics applications. Monochromatic and color displays are available.*



tronics CAD, graphics, database management, and software currently available on the UNIX operating system. Ethernet is also available for transferring information quickly to other stations.

Graphics support is more extensive than typical mainframe vendors. Because the 32S is geared for single users, it is finding popularity with computer graphics professionals who have greater demands on processing time. The 32S supports high resolution bit mapped graphics using the Ridge 1024 x 800 pixel black and white monitor or a high resolution 19"

color monitor at 1024 x 768 pixels; 256 colors out of a palette of 16.7 million are displayable. The display screen which requires 10 Mbytes per second of memory bandwidth, contains its own 128 Kbyte of refresh memory for updating at 50 Hz. The display is bit mapped by saving a 128 Kbyte portion of the user's virtual address space. The virtual memory area is paged in and out to the display controllers refresh memory, just as normal memory is paged to and from the disk. To update the screen, the user turns on bits in the user's own address space and the new data is



paged in and out to the display. Two additional RS-232 ports are available for a graphics tablet and other devices. The 4 Mbytes of memory and 4 Gbytes of addressable code and data size, in addition to an optional 445 Mbyte drive, makes the 32S very attractive as a dedicated graphics system.

A special architecture was employed to reach the performance of 8 million instructions per second and 1.5 million operations per second as measured by the Whetstone benchmark. It was discovered that load, call, and branch instructions usually appear in compiled code more often and take longer than other instructions. In addition, simple instructions are used more frequently. A complex operation can be executed faster using a set of simple operations than a single complex instruction. The architecture took that into consideration including optimizing data and I/O control. As seen in **Figure 1**, the

memory controller uses a translation mapping table (TMT) that contains virtual to real memory addresses. The TMT access is overlapped with the memory array access, thus the translation process is very fast.

The two board CPU is two parts: the fetch board and the execute board. The execution unit contains 16 32-bit general registers, a 32-bit ALU and a 32-bit barrel shifter. The instruction fetch unit prefetches memory words and fetches up to two words ahead of the instruction being executed. The instruction fetch unit has an instruction cache and a branch prediction unit. The branch prediction unit detects a conditional branch takes 0  $\mu$ sec. The prefetch unit is capable of initiating one instruction every machine cycle (125 nsec).

Memory access is a three step process. After the translation table has made the virtual to real translation, access of RAM is made, and the data is stored in the register. A 39-bit wide memory path is used where seven bits are used for error cor-

rection. The fetch process takes only 375 nsec.

The Ridge operating system (ROS) is "UNIX compatible." This means that the operating system has the facilities of UNIX V and 4.2 but due to the architecture of the Ridge, they are not implemented in the same way. Ridge, attempting to remedy some of the shortcomings of the UNIX system such as a monolithic kernel design, has implemented a process-based system. Here, the operating system provides minimal support for process management, memory management, and device management. While the method of implementation is different, the interface to these devices remains the same. Performance is increased two ways. First, memory management techniques ensure that heavily used code and data is rarely swapped out. Secondly, hardware support for copy-on-write page access eliminates unnecessary copies of message data. This results in optimized performance and faster operation.

—MacNicol  
Write 245

## Industry Standards Mold New 32-Bit VMEbus Supermicro

Adhering to open system standards and buying outside allows the OEM to keep all aspects of a computer system state-of-the-art. One new supermicrocomputer was built on the premise that standards to allow high-performance computing are the key to OEM market success. Charles River Data Systems (Framingham, MA), until now a supplier of VERSAbus computers, has introduced a VMEbus system that uses /usr/group approved UNIX, Motorola's 68000 family, 802.3 Ethernet networking and SCSI interfaces.

The Universe 2203 (**Figure 1**) is their configured system; the two-board CPU is also available alone, as the model VCP2000. Both are based around the 68000 now, but will incorporate the 68020 when it becomes available; CRDS claims 1.25 MIPS operation for the 32-bit computers. Networking to the IEEE 802.3 standard for CSMA/CD baseband with software to ISO specifications is also available, in UniverseNet.

VME is gaining momentum for 32-bit architectures, as Multibus II products from Intel have not yet been announced. CRDS also cites the asynchronous operation of the VME as an advantage over Multibus II. They feel the FutureBus has too little acceptance from vendors to compete.

*Figure 1: The 2203 is a seven-slot VMEbus backplane with Winchester and backup designed for 32-bit operation.*



Charles River's VERSAbus product line, which can also handle 32-bit processing, will continue to be important. However, the advantages of VME over VERSAbus include smaller card size, DIN connectors that are gas-tight and sturdy, faster clock speed, a bandwidth of 40 Mbytes/sec, and acceptance as a European standard.

Until the 68020 processor is available, CRDS is using a 12.5 MHz 68000. Because the 68020 has only instruction cache, the next version of the 2203 will

incorporate more cache, both for instructions and data. To increase cache hit rate and speed up memory fetches, a 32-bit cache is already used with the 16-bit 68000 processor. At present, memory management is implemented in discrete logic; CRDS claims that the Motorola 68451 MMU introduces too many wait states and would degrade the performance of the system. To take full advantage of the speed of a 32-bit processor, Charles River is developing its own demand paged MMU for the 68020.



One market that the 2203 is aimed at is industrial; General Motors has adopted the VMEbus as its standard. Its small form factor, vibration-resistant connectors and speed are important to harsh factory environments. Systems designed for 32-bit operation with open architectures could find large new markets in industry. Microcomputers attached to more intelligent industrial equipment are proliferating, and need speed. Industrial computers also provide a factory data-

base; this requires memory and computing power for ease of access at the corporate level.

Another need for both factory and tamer environments is networking. The networking products introduced simultaneously with the 2203 similarly meet standards: in this case, IEEE 802.3. Charles River participated in the NBS network demonstration at NCC this summer (*Digital Design*, June 1984), and has been certified for 802.3 compatibility. Using ISO protocol software, CRDS offers five network applications: electronic mail, file transfer, remote job initiation,

remote printer spooling and write.

All of these products are scheduled for availability this month. The network software has an initial license fee of \$1500; the list price for the VME UniverseNet board is \$3000. The configured single-box 2203, including 35-Mbyte Winchester and choice of 8" floppy or 1/4" streamer uses five cards, with two slots free. System cost is \$14,900 with floppy and \$16,900 with 45-Mbyte streamer. The dual-board CPU alone is \$4,000. Quantity 100 OEM discount is 40% on Charles River products.

—Pingry  
Write 233

## DEPARTMENTS/Boards

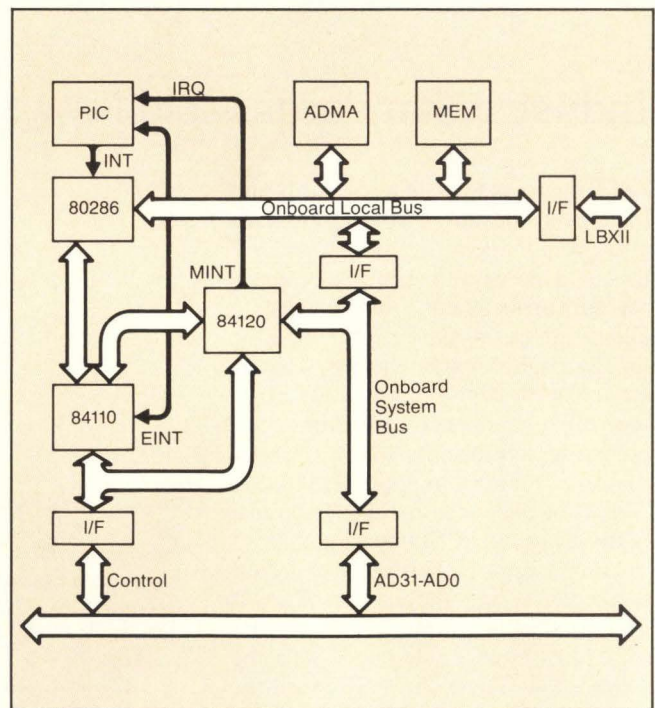
### ICs Help Designers Implement New Bus Structure

Since the announcement last year of the Multibus II, designers have awaited the arrival of silicon to help with the implementation of the advanced architecture. Recently, Intel has announced two devices, the 84110 Bus Arbiter Controller (BAC) and the 84120 Message Interrupt Controller (MIC). A block diagram of how the parts interface in a single board computer design is shown in **Figure 1**.

The 84110 BAC provides a generalized interface to the Parallel System Bus (iPSB) of the Multibus II architecture. It performs the functions of arbitrating for ownership of the iPSB and conducting bus transfers and exception cycles. The BAC supports both requestor and replier functions in addition to parity generation, checking and error reporting. The 84110 has three interfaces; the iPSB bus interface, the host interface in the on-board local environment and the register interface.

The host interface consists of a primary and secondary agent interface. The primary agent interface supports both requestor and replier functions. As a requestor, the primary interface supports bus request, initiation, arbitration in normal or high priority mode, transfers in all four address spaces (memory, I/O and interconnect), transfer widths of 8-, 16-, 24- and 32-bits, transfer options (read/write, block, or locked), and broadcast capability. As a replier, the primary agent interface supports all single replier mode data transfers of any length, broadcast mode data receptor and

Figure 1: 84120 MIC host CPU, 84110, and iPSB bus interface requirements.



reporting agents errors.

The Multibus II architecture uses a message address space for implementation of multiple processor (multiple agent) systems that require interprocessor communication. The message address space is accessible to agents on the parallel system bus. Messages used in interprocessor communication are categorized as "interrupt-like" and "data-like." The Message Interrupt Controller or 84120 implements a subset of the unsoli-

cited message types defined in the Multibus II specification.

Like the 84110, the MIC has three interfaces: the iPSB, the host CPU and its interface to the BAC. On the host side, the component behaves like a slave I/O port to the CPU, providing a register-based interface by which the host CPU sets up its control and output message commands and receives source and status information on incoming interrupts.

—Wilson  
Write 240



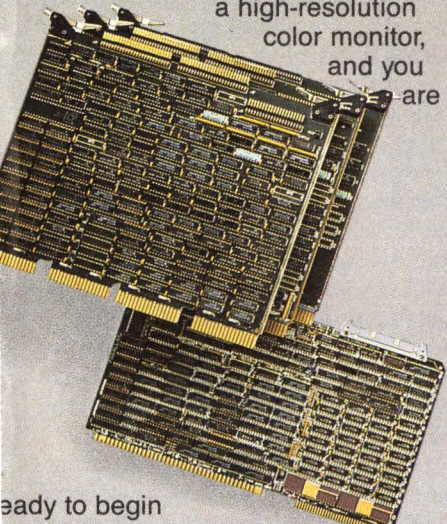
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**“...drawing speeds of up to 88 million pixels per second.”**

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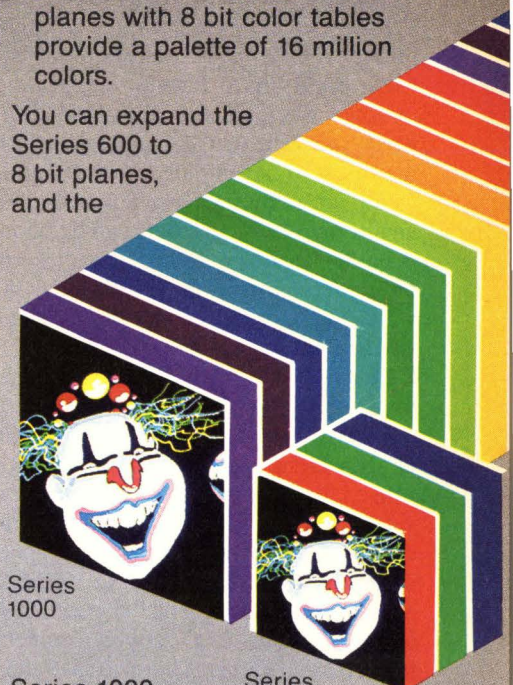
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1024 x 1024, 60 Hz non-interlaced display is yours with Parallax's high-performance graphics controllers.

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Series 1000

Series 600

Series 1000 is expandable to 24 bit planes. Other standard Parallax features include double buffering, smooth pan, and integer zoom along either axis — Parallax controllers have a long list of features that mean high performance graphics power for your microcomputer system.

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## Calma Introduces Complete Design Solution

Essential to meeting narrow market windows are the tools that take the project from conception to prototype. With this in mind, Calma (Santa Clara, CA) recently introduced a full line of integrated design tools that allow the system architect to execute a design project from beginning to end.

Unfortunately, many workstation manufacturers and software vendors frequently offer a limited portion of the software necessary to complete a design project. When this occurs, system architects usually have several unappealing options. Seeking out additional third party software that is compatible with their host or developing in-house application programs are two alternatives. As an alternative, design data can be reformatted so the output from one application program runs on a different vendor's software. These choices can be both expensive and time consuming. Provided CAD/CAE tools perform the tasks they claim, one-stop shopping is highly desirable.

Calma has been known for their Graphic Design System II (GDS-II) which is used for custom IC design. However, since General Electric's (GE) 1981 purchase of Calma, a wide variety of support tools have been announced. In 1983 GE acquired Comsat General Integrated Systems (CGIS)(Austin, TX) which brought the TEGAS logic simulator into the Calma product line. Following the acquisition, Calma announced their Apollo computer-based TEGASStation engineering workstation. This month marks the debut of TEGASStation 3.0, an enhanced version.

TEGASStation 3.0 includes an Apollo DOMAIN computer (DN300, DN460 or DN660), the TGATE schematic capture software, the netlist extractor (TDL, SPICE and Scicard formats), the TEXSIM logic simulator which is an extension of TEGAS-5 and TaskMaster. TaskMaster is an applications and file management program that provides the user with a common interface to all integrated design applications making Apollo's AEGIS operating system transparent to the user. Both the DN460 and DN660 come with 2 Mbytes of main memory, a 167 Mbyte Winchester Disk and a 1.2 Mbyte floppy disk. The less expensive DN300 includes 1.5 Mbytes of main memory, a 70 Mbyte Winchester disk and a 1.2 Mbyte floppy disk.

TaskMaster represents the core of the

Calma design solution since it manages the files and application software. Presently, the TEGASStation software can be ported to a VAX without TaskMaster, however, the user must be familiar with the VAX VMS operating system. According to Calma Product Manager Dave Niehaus, the TaskMaster will be available on the VAX in the second quarter of 1985. At that time, the VMS operating system will be transparent to users running TEGASStation software on a VAX.

In addition to choosing among the three Apollo DOMAIN computers, there are three configurations of the TEGASStation. The DN660 and DN460 can be purchased as either Distributor nodes, Peripheral nodes or Standard nodes; and the DN300 can be purchased as either a Distributor node or Standard node. Both the Distributor and Peripheral nodes come equipped with a Multibus card cage and a peripheral to node adapter (PNA) board which acts as a high speed interface between the workstation and any peripherals. The Distributor node, however, includes a tape drive which gives the user additional file storage capability. The Standard node does not have a Multibus card cage and does not support high speed peripheral interfacing.

Unfortunately, in order to get the TEGASStation software, Calma requires the Distributor node to be purchased initially. The Peripheral and Standard nodes do not come equipped with the software, however, once the Distributor node is purchased the software can be ported to all other TEGASStation configurations.

Prices for the various configurations are as follows: DN660-based TEGASStation is \$108,000 (Distributor), \$94,000 (Peripheral) and \$89,500 (Standard); DN460-based TEGASStation is \$93,000 (Distributor), \$79,500 (Peripheral) and \$74,500 (Standard); DN300-based TEGASStation is \$54,000 (Distributor) and \$47,500 (Standard).

Calma also offers their TNET network which establishes communication between the TEGASStation and a VAX. Raw speed of TNET is 500 Kbytes/sec but after factoring in the higher level protocols the effective rate becomes 25 Kbytes/sec. The network sells for \$14,000 and includes a Multibus board for the TEGASStation, a Unibus board for the VAX and software packages for both Apollo and VAX computers.

Two approaches are available for net-



*Based on Apollo's DOMAIN Computers, Calma's TEGASStation includes schematic capture, netlist extraction, logic simulation and fault simulation.*

working TEGASStations. First, to communicate with a VAX, TNET requires a Distributor or Peripheral node because these two configurations have the necessary Multibus cardcage. If the user wishes to establish a network with just standard nodes, Calma offers their DSP-80 (\$9,000) which is a dedicated file server and gateway for communications.

For testability analysis, fault simulation and test pattern generation there is the Tegas Computer Aided Test (TCAT) software package. This enhanced version of TEGAS-5 test software, costs \$10,000 and runs on all TEGASStation configurations. TCAT will not run on a VAX but for users that need a VAX based test software package, Calma will provide the TEGAS-5 package.

For printed circuit board (pcb) layout, the General Electric subsidiary announced the T-BOARDS system which is based on the DN660 and costs approximately \$100,000. T-BOARDS is an automatic/interactive pcb layout system that can route eight layers simultaneously while alerting the designer to any mistakes. Although T-BOARDS shares the same database as the TEGASStation software, this pcb layout system must be purchased separately. T-BOARDS, however, does include the TGATE schematic capture software.

Calma also has automatic place-and-route software for single and double layer metal CMOS gate arrays. Presently available on either a VAX or Tektronix 4000 graphics terminal, T-ARRAYS will be offered in a workstation configuration in the first quarter of 1985 and will be priced at around \$120,000. This configuration does not include the TEGASStation software.

— Collett  
Write 232



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Write 80 on Reader Inquiry Card



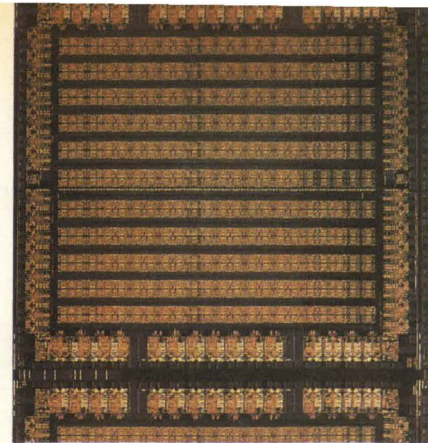
## Bipolar High Density Power/Speed — Programmable Gate Array

When implementing a gate array, system architects are often forced to choose between a power consuming high-speed bipolar technology and CMOS, a slower, less power hungry semiconductor. Even worse, the designer frequently must use an all-bipolar array when only a few functions actually require high speed logic. When this occurs, the balance of the array, although not running at high speeds, consumes excessive quantities of power. The penalty often comes in the form of larger power supplies and thermal management problems. Low gate counts has been another shortcoming of bipolar digital arrays with most vendors offering parts having fewer than 2500 gates.

In response to the need for a power-efficient high-speed array, Applied Micro Circuits Corp. (San Diego, CA) recently introduced the Q3500S series. With this new ECL gate array, designers can combine signals of varying speed and

power in one chip. High-speed power-thirsty circuits need only be implemented where minimum delays are necessary. The array's remaining circuitry can be configured with slower more power-efficient logic. When partitioning different functions onto the array, the system architect can choose macros of varying power consumption and gate delays: 650, 500, 350 or 275 psec. In addition, the 3500 equivalent gates give designers the capability to implement much larger amounts of logic than usually possible on a bipolar array.

The Q3500S has 120 universally programmable I/O cells and interfaces to TTL, ECL 10K, ECL 100K, mixed TTL/ECL or 5V referenced ECL. Speed/power programmability is also possible in the TTL I/O cells. The designer has three TTL I/O speed options: high speed-5.5 nsec, standard-7.0 nsec and low power-9.0 nsec. For drive and loading capability, TTL outputs sink 20 mA and input cells



AMCC's new Q3500S ECL gate array can be customized to cut power consumption by as much as 50%. Shown is the array before customization.

have an LS-equivalent load. ECL outputs drive 50 ohm loads and input loading is much less than standard SSI/MSI devices. Also, to drive 25 ohm loads, two ECL output cells can be paired.

The Q3500S uses a 3-micron oxide isolated fabrication process and dissipates an average of 1 milliwatt/equivalent gate. In addition, to reduce noise the new array has 28 power and ground pads.

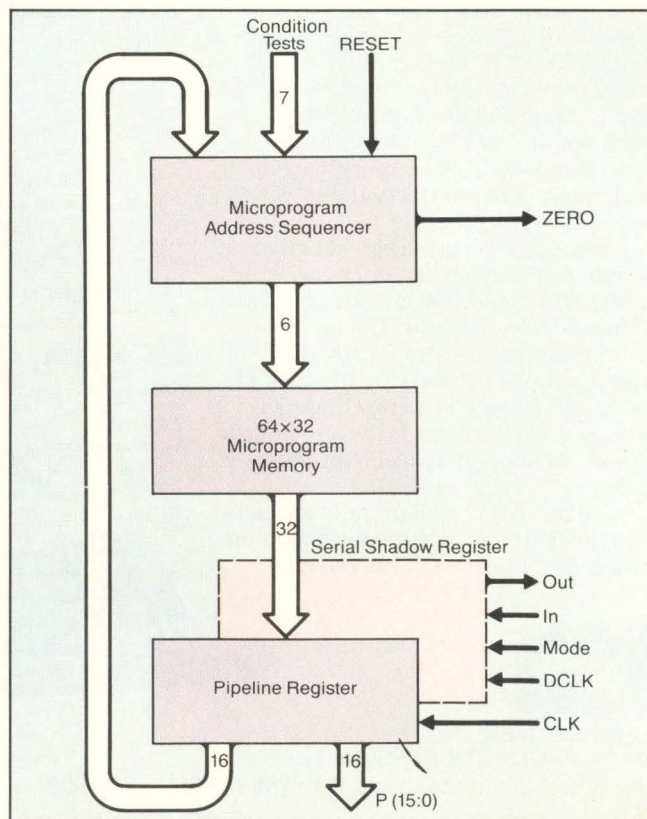
— Collett  
Write 231

## Fuse Programmable Controller Allows For Distribution Of Control

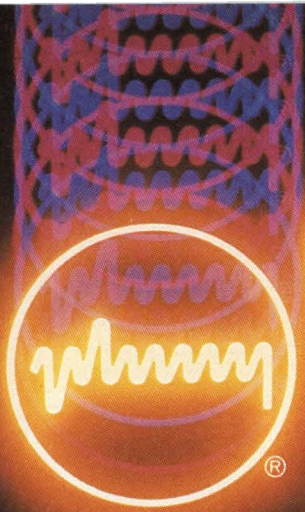
Off-loading specific duties from host CPUs to intelligent peripherals has long been one way the system designer has boosted the performance of his system. Following this trend is a new fuse programmable controller (FPC) from Advanced Micro Devices (Sunnyvale, CA). It allows the designer to off-load the central controller by distributing FPCs as the control for various self-contained functional units, such as register file/ALU, I/O, interrupt, diagnostic and bus control units.

The FPC consists of four main logic blocks: the microprogrammed memory, microaddress control logic, condition code selection logic and microinstruction decode. As an option, the FPC may be programmed to have on-chip serial shadow register (SSR). Microinstructions can be serially shifted in, executed, and the results shifted out in order to facilitate system diagnostics.

Figure 1: Functional block diagram of the AM29PL141.







# VME

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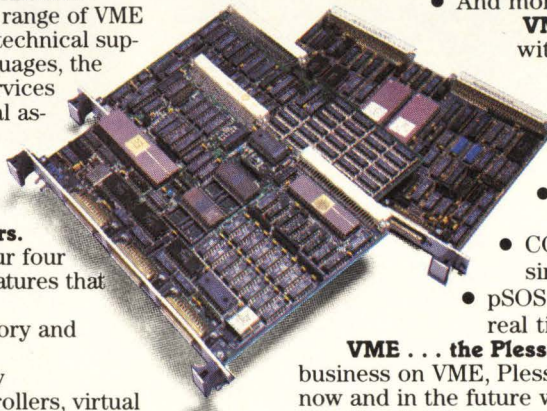
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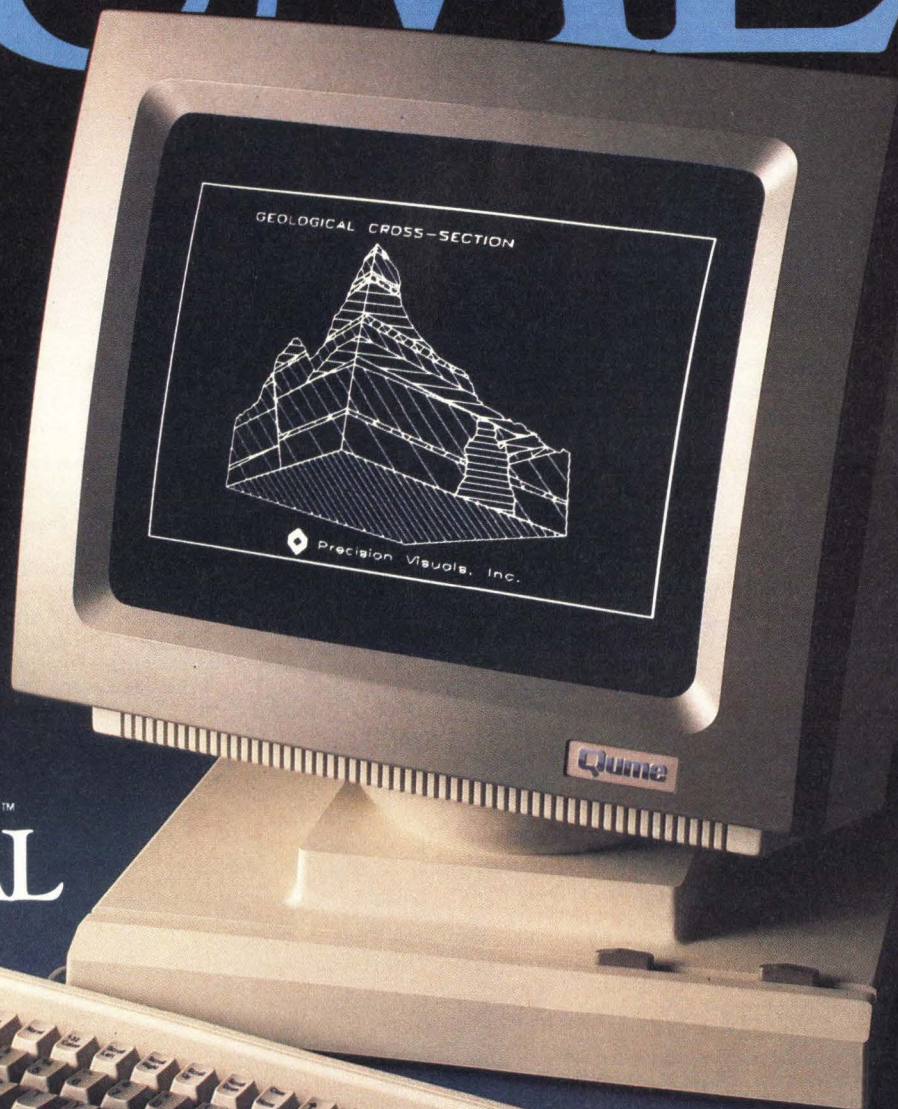
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# QVT-311GX™

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Now even a modest budget can include a full spectrum of business, engineering and scientific graphics as well as alphanumeric text editing. This new QVT 311 GX raster-scan graphics terminal is compatible with Digital's VT-125 and Tektronix 4010/4014, but costs a lot less than either. It runs both ReGIS and PLOT 10 graphics software, and conforms to ANSI X3.64 in the text mode allowing it to be used with a wide range of existing business and engineering applications software.

Qume's new QVT 311GX offers full bit-mapped graphics on a 14-inch, non-glare, white snow phosphor screen and a resolution of 640 by 480 pixels—greater than most other monochrome graphics terminals in its price range.

Two graphics memory planes make it possible to generate four shades of gray. Flexibility is further enhanced through the use of six character attributes, six line types, and area fill.

Standard features of the QVT 311GX include a detached, low-profile capacitive keyboard with superior tactile feedback and a full tilt-and-swivel display. For easy drawing and editing, an optional mouse is available. Best of all, the affordable QVT 311GX monochrome graphics terminal is backed by Qume's proven record for reliability and service.

For more information about the new QVT 311GX and Qume's other graphics and alphanumeric terminals, or our full line of daisywheel printers and disk drives, call (800) 223-2479. Or write Qume Corporation, 2350 Qume Drive, San Jose, CA 95131.

VT 125, ReGIS, and LA 30 are registered trademarks of Digital Equipment Corporation. Tektronix 4010, 4014 and PLOT 10 are registered trademarks of Tektronix Inc. FX80 and MX80 are registered trademarks of Epson Corporation. ANSI is designed to American Standards Institute, Inc., ANSI X3.64 - 1979 guidelines.

### CHARACTERISTICS

#### Data Transmission

Data Rate: 50-19.2 K baud  
 Communications Interface: RS-232C  
 Transmission Mode: Half duplex/full duplex/asymmetric asynchronous

#### Display

Medium: Snow white phosphor  
 Screen Size: 14 inches  
 Screen Surface: Non-glare  
 Refresh Rate: 50 Hz or 60 Hz, non-interlaced

#### Keyboard

Detachable, low-profile, with telephone type modular connector. Optionally available in multiple languages.

#### Mouse Device

Optionally available for graphic crosshair cursor control.

#### Graphics

Addressability:  
 VT 125 Mode: 800 x 600 points  
 Tek 4010/4012 Mode: 1024 x 1024 points  
 Tek 4014 Mode: 4096 x 4096 points  
 QVT 311 (native) Mode: 800 x 560 points  
 Resolution: 640 x 480 pixels (visible)  
 Line Types: Solid, dashed (various types)

Graphic Command: PLOT 10 compatible and ReGIS command set compatible  
 Graphic Primitives: Vectors, panels, polygons, text and markets  
 Two Full Graphics Planes: 4 shades of gray

#### Alphanumeric Mode

Character Set: X3.64-1979 for seven bit character set or X3.41-1977 (ASCII) for eight-bit character set  
 Character Format: 7 X 9 dot matrix in 8 X 14 dot character cell.  
 34 rows by 80 columns, the 33rd and 34th rows are the status/set-up/user-programmable lines

#### Auxiliary Port

Compatible with: Digital LA 30 and Epson FX80 or MX80

#### AC Power

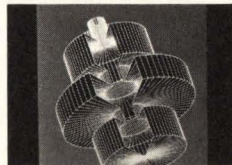
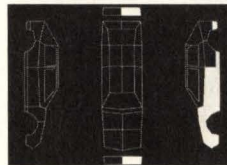
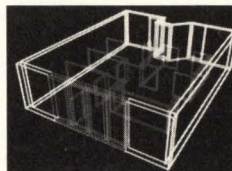
Line voltage: 90 to 135 VAC or 180 to 270 VAC  
 Line frequency: 50 to 60 Hz with ±3% variation

#### Physical Characteristics

Dimension	Display	Keyboard
Width	14½"	18"
Height	16"	1½" with two-step height adjustment
Depth	14½"	8"

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A microprogram address sequencer is the heart of the FPC, dubbed the Am29PL141. It provides the microprogram address to an internal 64 word by 32-bit PROM. The fuse programming algorithm is almost identical to that used for AMD's programmable logic family.

The control logic supports high level

microinstruction functions including conditional branching, subroutine calls and returns, loops and multiway branches. The condition code selection logic chooses the condition code input to be tested when a conditional microinstruction is executed. The polarity of the selected condition code input is controlled by a single bit in the microword.

The microinstruction decode generates the control signals necessary to per-

form the microinstruction specified by the microinstruction part of the microword. The new part should make life easier for those implementing complex state machines and controllers by allowing the designer to simply program the appropriate sequence of microinstructions into the device. The Am29PL141 will be available at a 20 MHz clock rate and comes in a 28-pin DIP.

—Wilson

**Write 242**

## DEPARTMENTS/Peripherals

### Shuttle Design Reduces Printing Downtime

One of the key considerations in designing a printer for high volume output, such as those required by OEM duty cycles, is eliminating printer downtime. Generally this translates into a greater possibility of breakdowns as the number of parts increases.

Genicom Corp. (Waynesboro, VA) has recently introduced a shuttle matrix line printer designed with a cantilevered leaf spring-driven shuttle which has eliminated the need for belts, pulleys and bearings. The Series 4000 has speeds of 600 lines per minute (lpm), print modes for draft, near letter quality and block graphics and is suited for information processing and business computing environments.

Based on a closed-loop design, the printer keeps track of shuttle locations through a linear velocity transducer. Six pin tractors above and below the print line provide dot positioning in character matrices of five of 9×9 (draft) and 9×18 near-letter quality (nlq).

The printer has a 132 column width and character spacing is available in 10, 12 and 13.3 characters per inch (cpi). There are two character sets of 64 and 96 characters which can print in draft mode at 240 lpm and 480 lpm, respectively.

Because of its matrix impact design, which is one of the best methods for printing multiple forms, the Model 4000 can print up to six copies and accommodate paper widths of 3" to 16.54". When used in forms length applications, the printer uses a 12 channel vertical format unit (vfu) which is controlled by the operator through a touch panel. The printer handles form lengths of 3" to 22".

All of the printer parameters and dot

generation logic are retained in non-volatile memory, reflecting a trend in dot matrix technology towards implementing more sophisticated control circuitry. Printer parameters can be either locally selected by the operator or remotely selected by ESC/CTL codes. Additional features include automatic perforation skipover at the bottom of forms, horizontal tabs which can be set in 22 positions, vertical tabs, right/left margin set and paper low and motion sensors.

In graphics applications, the range of resolutions is 60 to 210 dots per inch (dpi) horizontally, and 72 to 144 dpi vertically. The printer can produce line drawing, block and bar code graphics and has two formats, either Printronix P300/P600 or

ANSI X3.64.

For draft and nlq printing, Genicom supplies operator replaceable print modules. Character sets include courier, italics, OCRA, OCRB, math symbols, greek symbols and 16 international subsets.

Parallel and serial interfaces are standard. They include Printronix, Centronics, and Dataproducts as well as RS-232C to 19.2 Kbaud. The design, for which patent is pending, sells for \$5,500 to \$7,200. Genicom has tried to attack the cost of ownership by introducing a design which keeps maintenance to a minimum, largely by eliminating all moving parts in the shuttle mechanics.

—Coville

**Write 236**



The Genicom 4000 operates at 300 lpm.



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## Priam Imbedded Controllers For Intelligent Interfacing

Recently, the industry trend has been to provide more and more intelligence within disk drives. That is, what was normally considered a controller function is now being integrated into the disk drive. Priam (San Jose, CA) will support these new standard intelligent interfaces, in addition to its own proprietary interfaces.

Disk controller technology, particularly for OEM Winchester drives, has evolved rapidly over the last five years. Today, features which were usually only found in large mainframe type controllers are now found in smaller single board controllers. For example, house keeping functions such as error detection and correction, disk formatting, and defect mapping used to be shared between the host CPU and the controller. Both the CPU and device interfaces were dedicated to specific devices which limited the controller to a specific application.

The arrival of the microprocessor and VLSI semiconductor technology made it possible to implement typical control functions in the space defined by the form factor of the printed circuit card of either an 8" or a 5 1/4" disk drive. As a result, a conglomeration of single board OEM controller products exists today, making it possible to connect drives with any interface to the computer of one's choice.

The primary arguments for why these new intelligent interfaces are needed include the following: a) Using an 8- or 16-bit parallel, rather than a serial data transfer technique, makes the disk transfer rate less critical. b) The data separator stays in the drive, which makes it easier to guarantee the data integrity or the drive read error rate. The data separator location has been a constant source of controversy between drive and controller manufacturers. c) A higher level disk interface simplifies the host CPU interface and off-loads complex tasks such as ECC and defect management on to the peripheral instead. d) Multiple device types may be connected to the interface bus, simplifying the user's overall peripheral design effort. e) The user's second source potential is improved.

Originally, both of the ANSI (American National Standards Institute) proposed intelligent interfaces were being considered as candidates to be imbedded

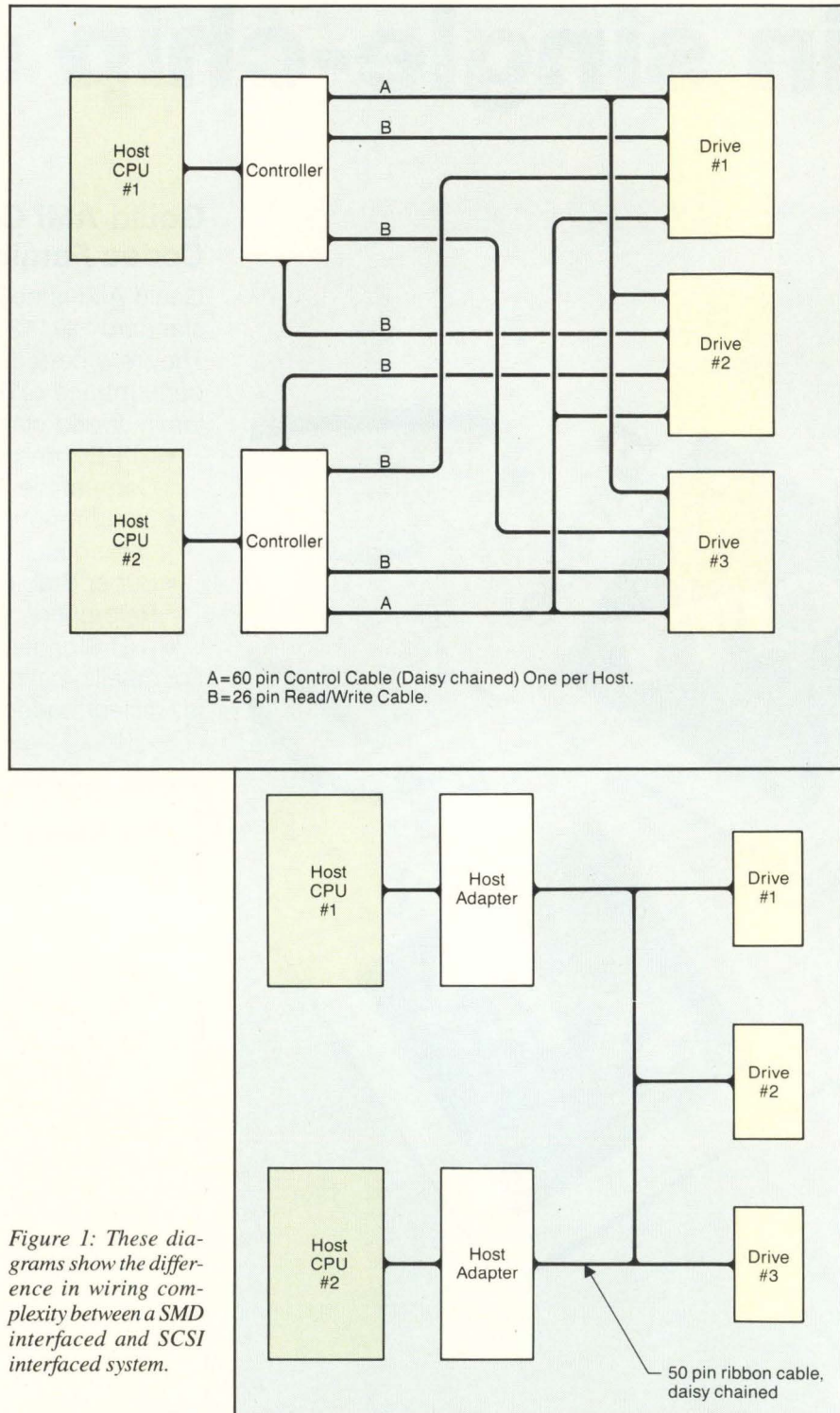
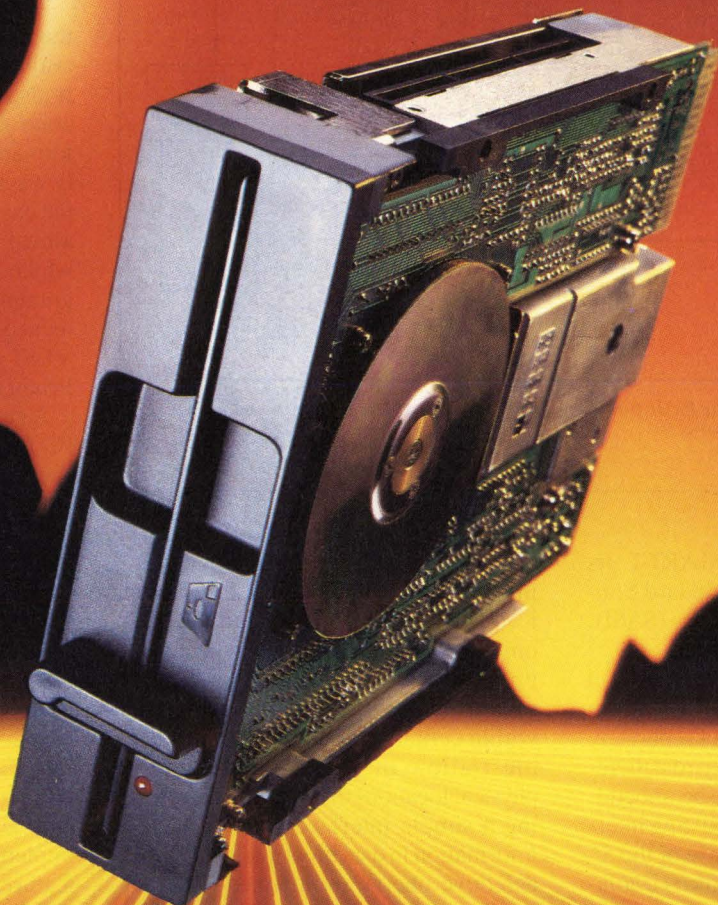


Figure 1: These diagrams show the difference in wiring complexity between a SMD interfaced and SCSI interfaced system.

into Priam's 5 1/4" and the new advanced 8" drives. They were the Small Computer Systems Interface (SCSI-X3T9.2) and the Intelligent Peripheral Interface (IPI-X3T9.2). After some consideration,

the SCSI interface was chosen as the first one to be completed. One reason was that it was well defined and it permitted the implementation of desired features already in existing Priam controller prod-





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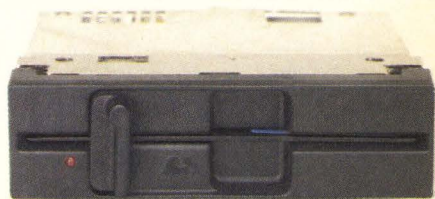
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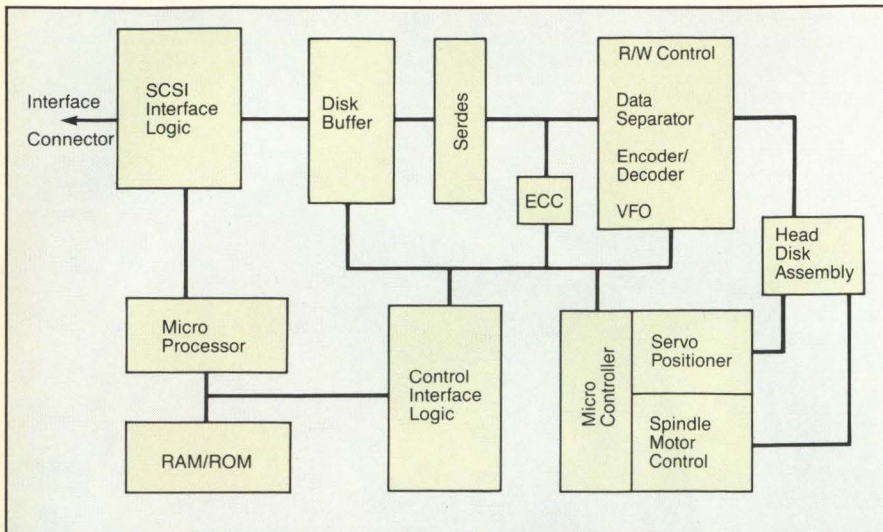


Figure 2: This diagram shows the basic functional blocks of a disk drive using an imbedded SCSI interface.

ucts, the SMART-E and SMART-T. Its similarity to the industry standard Shugart Associates Systems Interface (SASI), also played an important role.

Since the 5 1/4" and the 8" products had to conform with the standard drive form factor, this ruled out the use of separately mounted controller circuit boards; therefore the design would have to be imbedded into the drive like other existing interfaces. One criteria, in the case of the 8" product, that limited the choices available to the designers was the requirement to handle disk transfer rates of up to 2 Mbytes/sec.

Another design consideration involved the Priam specific formatting features. During initial formatting, all defective data blocks are automatically assigned an alternative location without the host knowing where the defective block and its

alternate is located. This is possible since information specifying the disk defect locations is prerecorded on specific areas on each disk during the manufacturing process. If, during normal use, the host system experiences high error rates within certain data blocks, the interface must allow the host to reassign the physical locations of these data blocks using a simple interface command. The information in data blocks adjacent to the defective one is not affected. In other words, only the defective sector will be reformatted. The list recorded on each disk, identifying the disk defect locations, can be updated by the host system. This guarantees that all disk defects are mapped out if the drive is reformatted at some future time. Again, a simple interface command is used.

The Priam design implementation

team was faced with three basic choices. One was to purchase an existing hardware/firmware design from an established controller house. The second was to develop an in-house design using readily available VLSI IC's and the third was to develop an in-house design including custom VLSI.

The above arguments also applied to the second choice, which combined available VLSI with an in-house design. It also became evident that most of the controller IC's were aimed at lower performance drives. The transfer rate usually was limited to 1.25 Mbytes/sec, while the basic controller functions often were aimed at the popular ST506 interface which did not have the necessary programming capabilities required to implement out disk format features. Using the VLSI approach did, however, allow Priam much more flexibility.

A custom design, using the NCR 5385 IC for the SCSI front end, was the approach chosen for the 8" SCSI product. The data transfer rate was the primary concern in this case. In the 5 1/4" SCSI product, space was the biggest obstacle while transfer rates, being lower, were not a problem. In this case, three Adaptec IC's, the AIC250 (Encoder/Decoder), the AIC300 (Buffer Controller) and the AIC010 (Controller) were used to implement both the SCSI interface and the controller functions. These IC's provided the required space savings, and the AIC10's programmability allowed implementation of the desired controller features.

Priam is implementing the SCSI interface in the advanced 8" model 806, and in the new 5 1/4" model 507, disk drives. The IPI (Level 2) interface will be implemented in an 8" product during the coming year.

— Erik Walberg, Manager, Drive Interface Development, Priam

Write 235

## Calcomp Brings More Intelligence To Plotters

When Calcomp designers began work on the 1040 Series plotters, one problem they faced was lowering the unit cost without sacrificing performance. They were striving for an entry level price in the \$5,000 to \$10,000 range using proven firmware from higher-priced Calcomp plotters, instead of developing new technology. Plot speed was reduced slightly

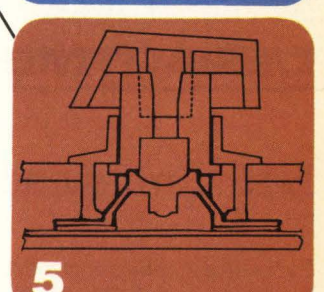
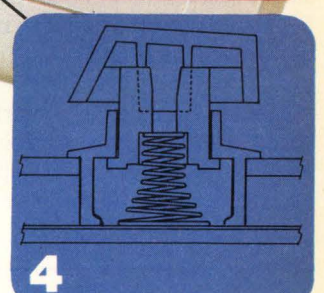
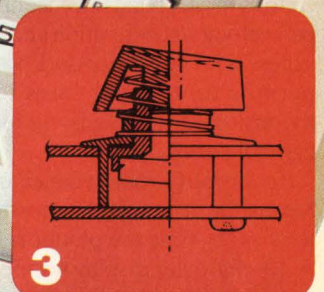
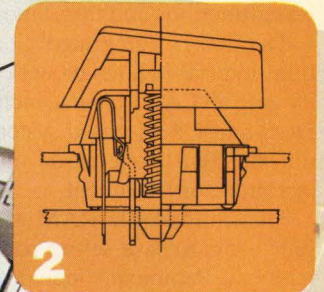
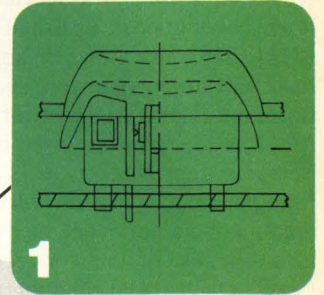
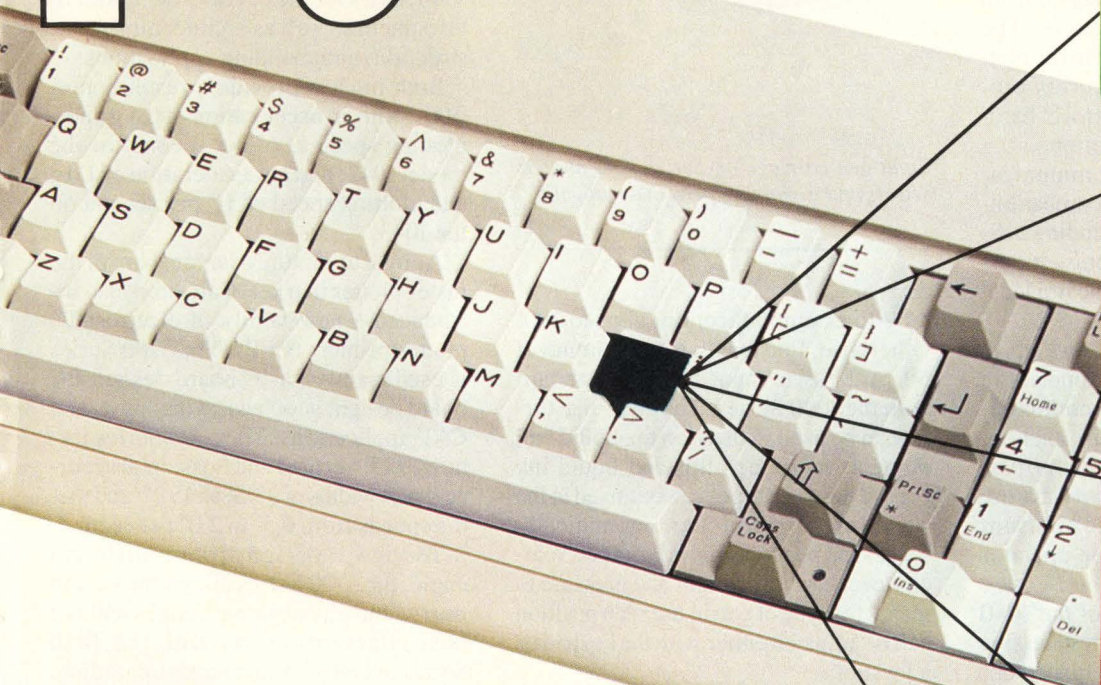
to lower costs, and the time loss was compensated for by adding a more efficient pen-exchange system, making it comparable to plotters with higher speeds and stationary pen carousels. Calcomp also used a friction drive, instead of the traditional sprocket drive approach which requires more hardware.

Series 1040 plotters can be interfaced

to a standalone workstation or incorporated as a shared resource in a traditional, host-dependent CAD environment. Based on dual microprocessors, the 1040 Series incorporates a 6803 to control servo motion and linear pen motion, and a 68008 main microprocessor to control data communications and other functions. The 1040 is equipped with 16



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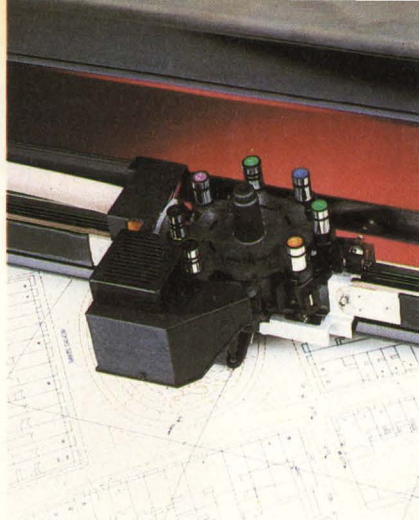
Kbytes of RAM and 64 Kbytes of ROM. It will accommodate up to half a Mbyte of ROM. This "open-ended" approach allows for future expansion, such as additional interfacing capability or protocols. Much of the firmware used in the 1040 Series plotters is taken unchanged from higher-priced Calcomp plotters. The amount of memory contained in the plotter allows use of an error-recovery protocol, as well as real-time control of hardware functions and turret motion.

The 1040's Integrated Communications Interface allows plotter compatibility with all CAD systems, including MS-DOS and CP/M-based systems. It permits the 1040 to operate on-line in a local or remote environment.

The non-volatile RAM allows up to four users to save set-up parameters in memory. Parameters include communications mode, baud rate, scaling rotation, pen velocity/acceleration and logon messages. The Auto Logon/Logoff feature permits up to eight users to transmit logon/logoff messages via the operator control panel.

To simplify maintenance of the 1040 Series, built-in self-diagnostics run five tests every time the plotter is turned on. A 40-character display notifies the operator if further attention is required. If a fault occurs, technicians can run up to 12 built-in test plots and/or diagnostic routines to pinpoint the cause.

Input is via an RS-232 interface with a speed of 19.2 Kbauds. An RS-232-C interface is also standard. An optional RS-449/422 interface is available to support



*Eight-pen carriage on Series 1040 plotters selects and exchanges pens automatically.*

long-line communications of up to 200'. Otherwise, line length is a maximum of 50'. A 2-Kbyte input buffer is standard with the 1040 Series. The eight-pen turret can be used with nylon tip, liquid ball point, ceramic pen tips and liquid ink pens. These pen types can be mixed in the same turret; the plotter automatically senses the pen type and adjusts pen velocity/acceleration, height and pressure to match the type of pen in use. Pen position can be adjusted either with the keypad or a joystick.

The 1040 can draw on E-width media in addition to the ANSI size D sheet. This capability was incorporated to address extensive engineering applications which employ ANSI sized media, A through E.

The 1040 Series, introduced at 1984 SIGGRAPH in Minneapolis, MN, consists of two plotters, models 1042 and 1043. Model 1043 performs in cut-sheet

mode only, while model 1042 is a dual-mode plotter that operates in both cut-sheet and roll-feed modes. With a dual-mode plotter, a user can produce single plots and also batch jobs in production environments. Calcomp developed the 1040 Series for the CAD/CAM/CAE environment as well as architectural, construction, and mapping applications.

Both models provide a resolution of 0.001" with an acceleration of 0.5 g and a plotting speed of 6" per second for the model 1042, and an acceleration of 1.0 g and plotting speed of 14" per second on the 1043.

Aiming to capture a larger share of the raster plotter market, CalComp also introduced a new family of electrostatic plotter/printers (EPP). The 5700 Series is used mainly for IC board design, PC board design, geophysical mapping, and CAE applications. The 5700 Series features 0.1% vertical and horizontal accuracy; plot widths of 23.5" or 35.2"; and media speeds from 0.5" to 2.0" per second.

To view a design from a different angle, the 5700 Series allows the user to mirror and plot negative images without host intervention. As with the 1040 Series, when firmware needs upgrading, the user unplugs the self-contained ROMpack and replaces it with the desired upgrade.

The 5700 Series EPPs are software and controller compatible with most current EPP users' systems, including CalComp, Versatec and Benson.

—Hanrahan  
Write 239

## DEPARTMENTS/Graphics

### NEC Enhances Graphics Display Controller

Ever since graphics controller chips have been introduced, their importance has created a demand that is still increasing. Most notably, the NEC 7220 has created such an impact that over 40 companies depend on the chip for the success of their graphics systems. Having great power in a single chip, it still suffered from speed limitations and configuration problems. As a result, many designers have been

considering the alternatives such as different chips or multiple 7220s.

Now an enhanced version of the chip is available with many improvements, the most important being speed. The newer chip, the  $\mu$ PD7220A, has an increased video data rate and higher pixel drawing speed. The new chip runs at a higher clock rate than the 5.5 MHz maximum frequency of the earlier version. The

7220A is available in three versions at different frequencies: 6,7, and 8 MHz. The 8 MHz version draws pixels at 500 nsec each, an improvement of 300 nsec.

The new version also has additional commands that gives it greater flexibility. The earlier 7220, when used as a slave, for example, synchronized its internal sync generator to an external Vertical Sync signal. The enhanced version still retains this capability using the Reset 1 and Blank 1 providing graphics overlays and text over graphics. The new commands, Reset 2, Reset 3, and Blank 2, allow greater control of the slave controller, such as blanking the slave's display.



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With peak performance rated from 33 to 341 million floating-point operations per second, depending on configuration, and up to 7 Mwords of 64-bit memory available to the user, the new FPS-164/MAX gives you all the speed and accuracy you need to make those matrix computations manageable.

The FPS-164/MAX configuration is able to compute up to 124 vector operations at one time, allowing a fully-

configured 164/MAX to factor a 1,000 by 1,000 matrix in about 1 second, multiply two 10,000 by 10,000 matrices in less than two hours.

### FPS-164/MAX Specifications

Peak Capacity (MFLOPS) .....	341
Number of Arithmetic Pipelines .....	63
Number of Independent Processors .....	1
Vector Register Capacity .....	2K x 124
Main Memory Capacity .....	7 MWords
Disk Subsystem Capacity .....	3 Gbytes
Word Size .....	64 bits +8-bit error correction
Precision .....	15.3 decimal digits
Dynamic range .....	$2.8 \times 10^{-309}$ to $9.0 \times 10^{307}$
Cooling Method .....	Forced Air
Footprint .....	~20 ft <sup>2</sup>
Weight .....	1800 lbs. including power supplies

### The FPS-164/MAX is powerful.

A parallel-pipelined machine designed to run FORTRAN at high speed, the FPS-164/MAX has all the scalar capability of our original FPS-164. We've just added a lot more power, with multiple special processing units which amplify the vector processing capability of the original FPS-164 by up to 31 times.

### The FPS-164/MAX is cost-effective.

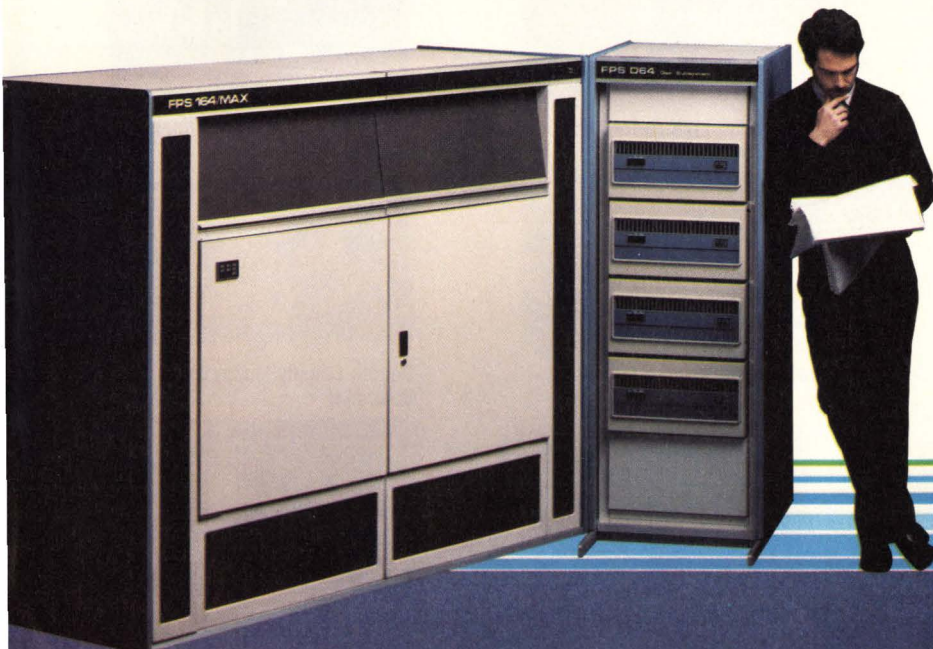
In structural analysis, computational chemistry and physics, fluid flow analysis, electromagnetic modeling, or any application requiring fast handling of large matrices, the FPS-164/MAX offers unparalleled cost efficiency. In fact, it can run certain key matrix computations as fast or faster than supercomputers costing over 10 times as much.

Whether you're looking to upgrade your existing FPS-164 — or searching for a complete new system — you won't find supercomputer performance for one million dollars or less anywhere else.

What's more, the FPS-164/MAX is backed by the considerable resources of Floating Point Systems. With 21 field service offices world-wide, full remote diagnostic capabilities, and a record of product quality and reliability second to none, you can be sure the FPS-164/MAX will be up, running, and ready to meet your problem solving needs.

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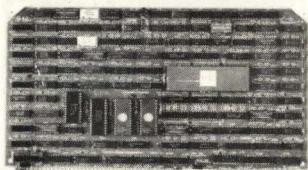


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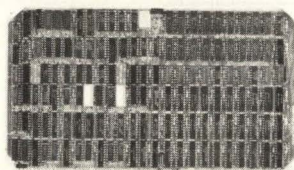
P.O. Box 23489  
Portland, OR 97223  
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TLX: 360470 FLOATPOIN BEAV



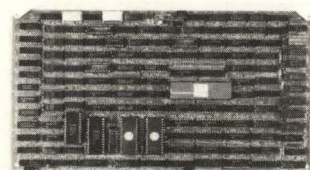
# 23 things Multibus\* know about



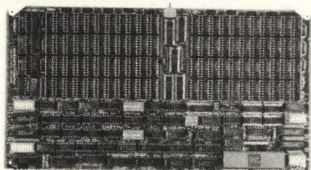
12.5 MHz 68000 CPU



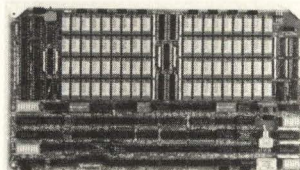
iLBX\* Cache Memory Board



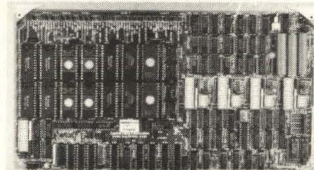
10 MHz Z8000\* CPU



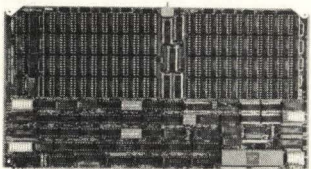
180ns 128K-2Mb EDC DRAM Board



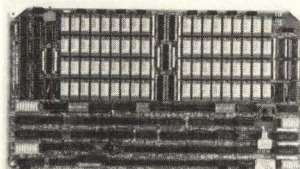
140ns 128K-512K EDC DRAM Board



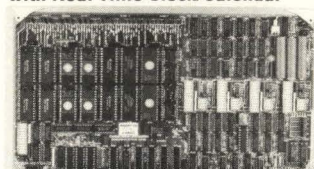
EPROM/RAM/EEPROM Board  
with Real Time Clock/Calendar



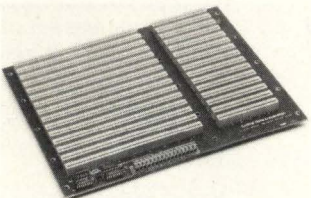
170ns 128K-2Mb Parity Only  
DRAM Board



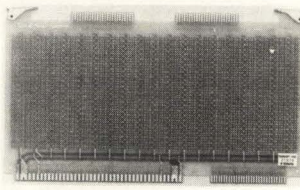
135ns 128K-512K Parity Only  
DRAM Board



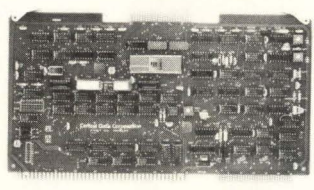
Static RAM Board with 128K CMOS



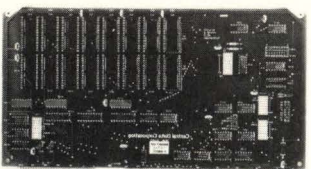
iLBX Backplane



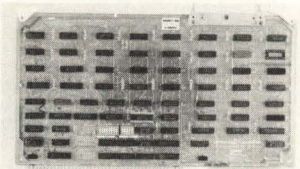
Prototyping Board



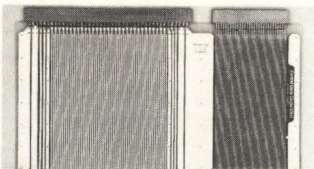
Double-Density Floppy Disk  
Controller



PROM Board



QIC-02 Cartridge Tape and Controller

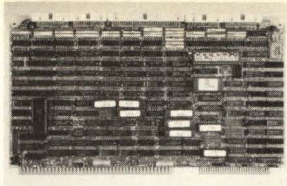


Extender Board

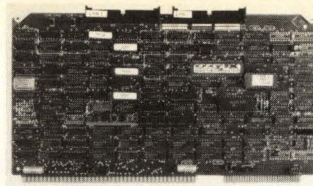




C2000 System Cabinet

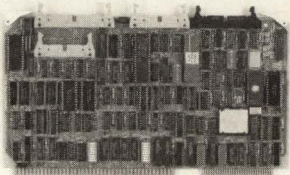


SMD Disk Controller

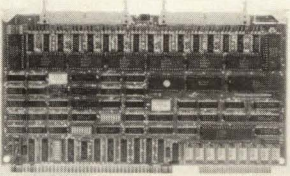


9-Track Tape Controller

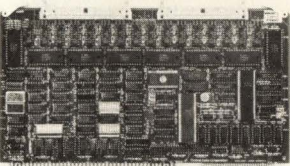
# users should Central Data



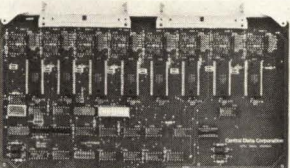
Multi-Media Controller  
(Disk/Floppy/Tape)



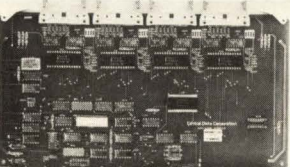
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Octal Serial Interface



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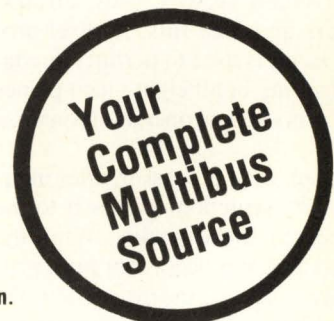
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Additional enhancements include better control of the cursor, increased horizontal pixels per line to 8196 pixels, elimination of an external latch for read-modify-write, better scrolling and zooming control, and a drawing wait state for better light pen control.

The 7220 Graphics Display Controller has three primary functions: control of the horizontal and vertical timing signals, control of display memory, and the ability to draw. Positioned between the microprocessor and the display memory, the 7220 can support 512K of video RAM and display resolutions of 2048 × 2048. A built in DMA channel allows block transfers of an image taking four clock cycles, which relates to about 175,000 pixels per frame. Although this may require using a frame to completely rewrite a screen using DMA, a designer may have to sacrifice an occasional frame refresh to gain access to the memory. This may cause flicker. The enhanced version, with its higher clock rate, allows 256 Kbits through the DMA channel in a

single frame, which is enough to rewrite an entire 512 × 512 display.

The enhanced version of the 7220 includes all of the commands of the predecessor such as pan, zoom, scroll, screen partitioning, light pen interface, and is plug compatible with the original 7220.

Adding to the graphics power of the 7200A is a new chip from NEC that enhances functions of display oriented graphics. Targeted at image processing applications and pattern recognition, the  $\mu$ PD7281 has a totally different architecture than conventional processors. The chip combines data flow techniques with a pipelined processor to overcome the limitations of conventional von Neumann architecture. A data flow architecture differs from conventional methods by letting its data drive the instructions of the processor rather than a set of linearly executed instructions. Dataflow architecture allows concurrent operations to be executed while avoiding storing intermediate results during computations. It also avoids instruction fetches, which slows processing. Its speed is further increased due to its increased bandwidth between its memory and the processor. All data

has a 16-bit tag which tells the processor where to send the data and what to do with it. This feature also allows each processor to handle different parts of memory in a dedicated and parallel fashion.

Typical benchmarks of the  $\mu$ PD7281 include the ability to rotate a 512 × 512 pixel image in 1.5 sec. Shrinking the same image in half takes only 30 ms. Other operations typical of image processing are smoothing, convolution, FFT, and fixed point trigonometric calculations.

The 7281 includes an array of cache memories that contains the data, instructions, and intermediate results. The high speed ALU and 16 × 16 bit multiplier performs all the operations of a high speed number cruncher including add, subtract, shift, barrel shift, and format adjust.

While still enjoying high sales of the 7220, NEC is supporting and enhancing its graphics display architecture in addition to developing a graphics chip set with an entirely new architecture.

—MacNichol  
Write 244

## Display Processor For Multibus Graphics

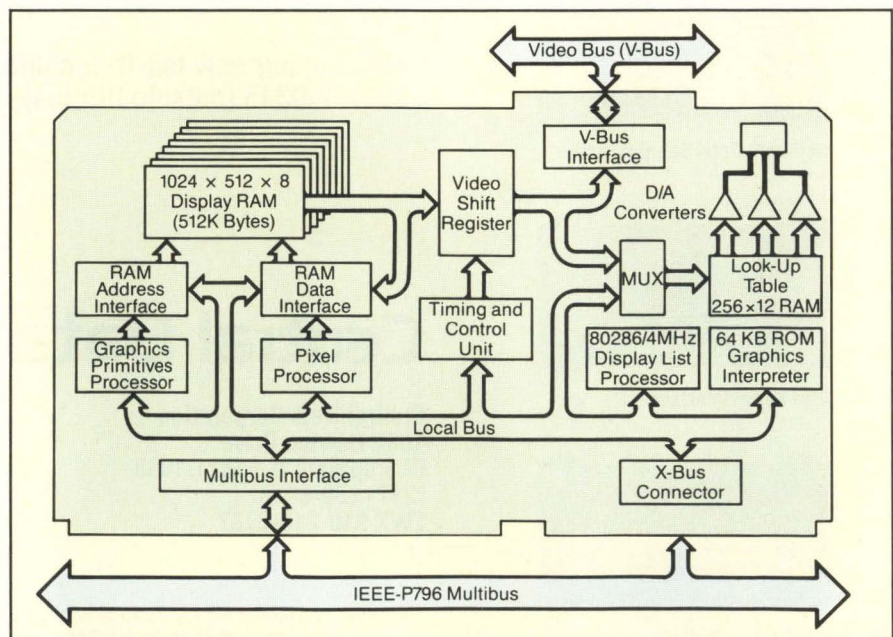
The SX-900 is a single-board Multibus color-graphics display processor containing a 512-Kbyte video frame buffer, a 4096 color look-up table, several on-board processors, and powerful graphics firmware. The SX-900, from Matrox Electronic Systems, Ltd. (Montreal, Canada) incorporates the concept of pipelined display processors. The display list processor is an 80286 which fetches, interprets, and sequentially executes commands from a display list. Several additional hardware processors are used to improve drawing speed. The 7220 GDC graphics primitive processor controls all video vectors, arcs, circles, characters and area fills. A pixel processor circuit is used to permit simultaneous drawing of all eight video planes and performs logical operations on pixel values.

The display list processor, after interpreting an instruction, passes it to the next processor in the pipeline. While the graphics display processor or pixel processor are executing the instruction, the 80286 is free to fetch and interpret the next command. The graphics firmware is

software compatible with the Matrox GXB-1000A high resolution graphics controllers.

The user can think of the SX-900 board

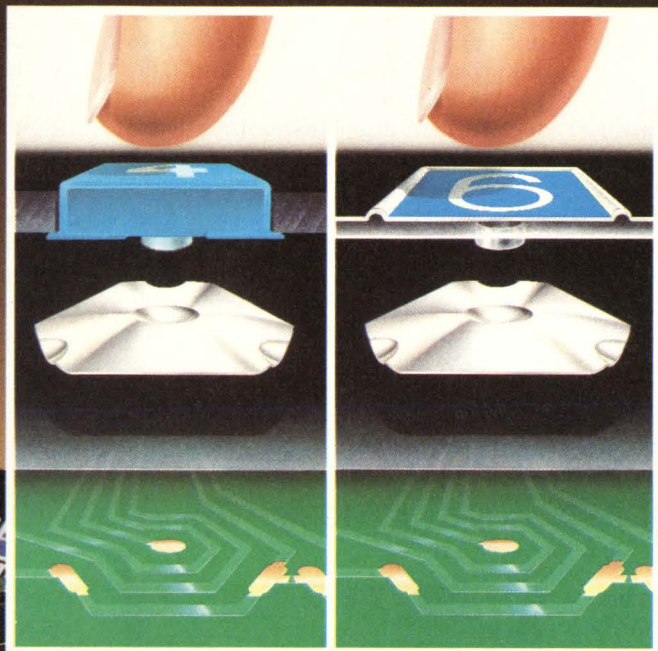
as a graphics processor which executes its own instruction set. The internal CPU, together with local resources (ROM, RAM, graphics processor, PIP, refresh



SX-900 block diagram.



# They Touch Back



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memory, etc.) can be thought of as a single graphics CPU with microcode stored in on-board ROM. A particular graphics instruction is performed by executing microcode (actually 80286 machine language).

The host computer has to transfer the starting address of the display list into the SX-900's I/O Command Input Port (4 byte transfer). The host then issues an Enter Graphics Mode command, after which the SX-900 fetches successive bytes starting from the starting address by becoming the bus master for each fetch. The display list can be up to 16 million bytes long. Multiple display lists can also exist anywhere in the 24-bit Multibus address space.

The local CPU fetches and executes instructions one by one always updating the graphics pseudo program counter. The pseudo PC is updated to point to the address of the next instruction. During execution the Multibus is not used, thereby freeing it for higher level CPU communications.

Synchronization between the host CPU and the SX-900 can be handled in two ways; interrupt or polling. The local CPU (80286) can issue an interrupt to the host, to signal that a display list has been started or finished. Alternately, the host can poll the SX-900's I/O port, which changes value to indicate that a display list has been started or finished. These methods allow for multiple display lists to be stored in memory. Nesting of display lists are also permitted.

The SX-900 display processor allows

the system builder to construct a single or multiple screen display system in a modular fashion depending on his particular requirements. The on-board intelligence permits the user to communicate with the display processor at a high level, thereby greatly simplifying the programming task.

A higher performance upgrade path is provided by the software compatibility with the high resolution GXB-1000 series controllers. OEMs can offer both high or medium resolution systems with no additional software investment.

The SX-900 is suitable for multiple display systems. Because of its on-board processing power, a single in-bus CPU can control multiple SX-900s with minimal degradation of performance.

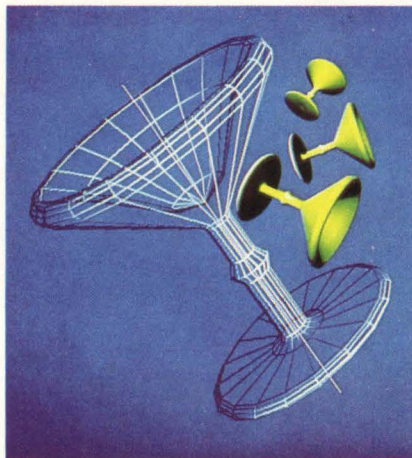
—Hanrahan  
Write 243

## Merlin Adds Database, Local Processing, And "Pixel Phasing"

The Merlin 9200 from Megatek offers, what the company believes to be, a breakthrough in raster display technology. The proprietary, patent-pending "Pixel Phasing" uses micropositioning of individual pixel boundaries and locations to achieve a projected visual acuity and image sharpness two to three times better than commercially available 1000 line raster monitors. The system also incorporates a local hierarchical database for organizing and retrieving both graphic and non-graphic information; local multitasking computing power; and networking capabilities.

Database management and editing capabilities, provided by an Intel 80286 microprocessor with 512K dynamic RAM expandable to 4.5 Mbytes, permit users to create graphics entities, integrate graphic and non-graphic information, and build list and array data structures without host intervention. Users can interactively create or modify graphics on the screen, while automatically building or changing the corresponding database. This database can be stored in the system's memory for later recall, or archived in a host processor's memory or any other system linked to the graphics station via the network.

Graphics information is organized and manipulated in the tree-like structure of the hierarchical database, permitting the rapid data retrieval required for real-time interactive graphics. This structure also allows for flexibility in developing ap-



The above photo shows a split wire frame, half with Pixel Phasing enabled and half with this antialiasing feature disabled.

plications such as mechanical design or PC board layout that utilize component libraries. Parts can be created and addressed by name, and associated into larger assemblies or subassemblies. In such applications, non-graphics information can be used to determine whether component parts are masked, displayed, or highlighted.

The Merlin 9200, as a result of the freely-structured database, allows library cataloging of generic shapes, such as pyramids or cones, for which specific coordinates can later be assigned in a referenced array. This eliminates the need

to repeatedly redefine common objects and lets the designer modify an object by changing the coordinates in the array.

Driven by an Intel 80186, the system's local task processor permits users to run up to eight concurrent tasks locally. Written in Megatek's high-level language, local tasks can be used for applications such as configuring and controlling peripheral linkage, creating display managers or menus, initiating continuous events and triggering criteria-based component highlighting.

Standard applications for the local task processor supplied with the system include picking, cursor tracking, and VT-100 emulation for complete alphanumeric capability and interfacing.

### Pixel Phasing

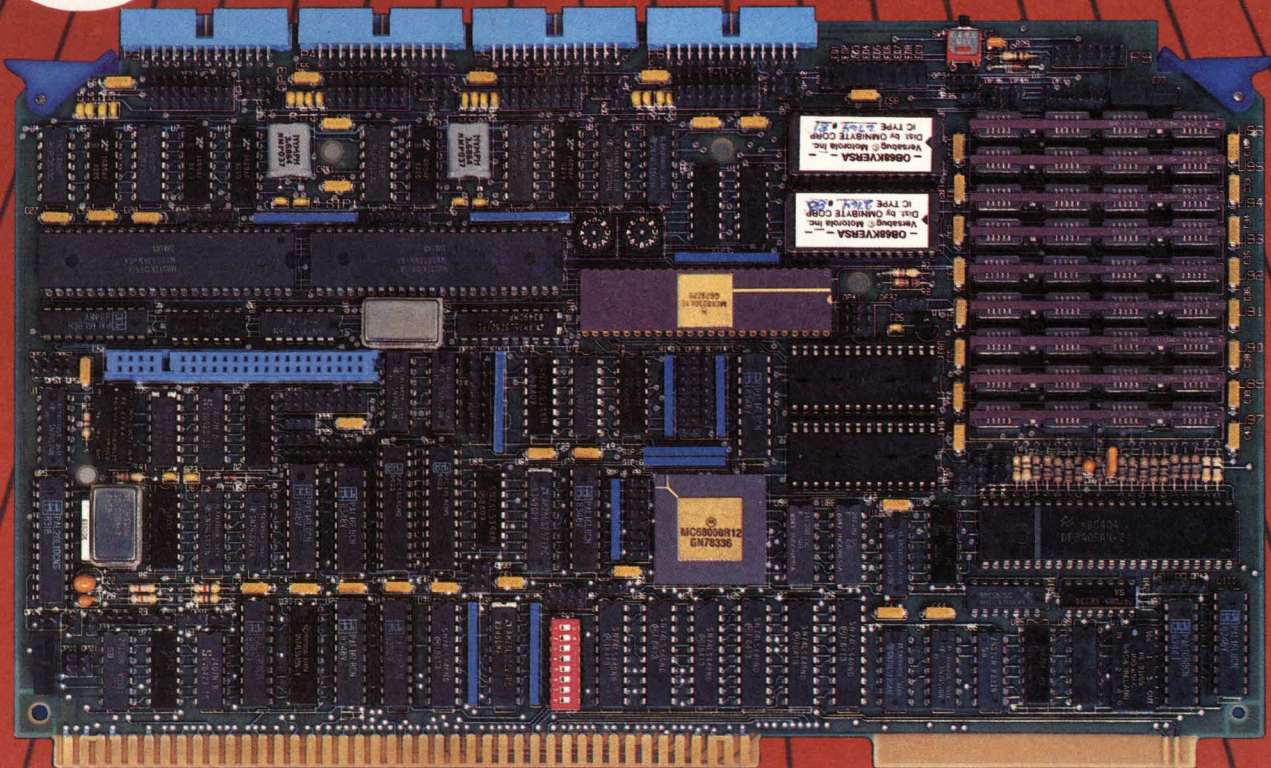
Merlin 9200's solids-rendering capabilities are the first implementation of the Pixel Phasing antialiasing display technology. This technique eliminates "jaggies" appearing on lines and polygon boundaries in traditional raster scan displays.

Pixel Phasing solves the jaggie problem through micropositioning of the pixel boundaries and deflecting the electron beam by fractions of a pixel. This technique actually increases virtual screen addressability while avoiding the thicker lines, defocusing or reduced resolution characteristics of other antialiasing techniques currently in vogue. The Merlin 9200 offers virtual screen addressa-



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bility of  $3072 \times 2304$  on the 19" screen of a 60 Hz non-interlaced monitor. It provides from 64 to 4096 simultaneously displayable colors from a palette of up to 16.7 million, depending on the size of the frame buffer specified.

The innovations of the new system rest on a firm base of advanced graphic capabilities including 2D and 3D viewing transforms, 3D transformations (translate, rotate and scale), 3D clipping in hardware and selective perspective transforms in hardware. Further graphics capabilities include a proprietary Gouraud or Phong real-time smooth-color shading method based on a programmable light source, depth cueing, translucent and opaque solids, surface texturing or patterning which adheres to the surface of stationary or transformed objects, and 3D entity detection. Hidden surface removal is available through either back face elimination or optional Z-buffer hidden surface removal.

— Hanrahan  
Write 241



*Megatek's proprietary antialiasing technique reduces jaggies appearing on lines and polygon boundaries in traditional raster display systems. These actual screen photos of the same image on the same monitor demonstrate the increase in addressable points to  $3072 \times 2304$  achieved using the technique (left) on the Merlin 9200.*

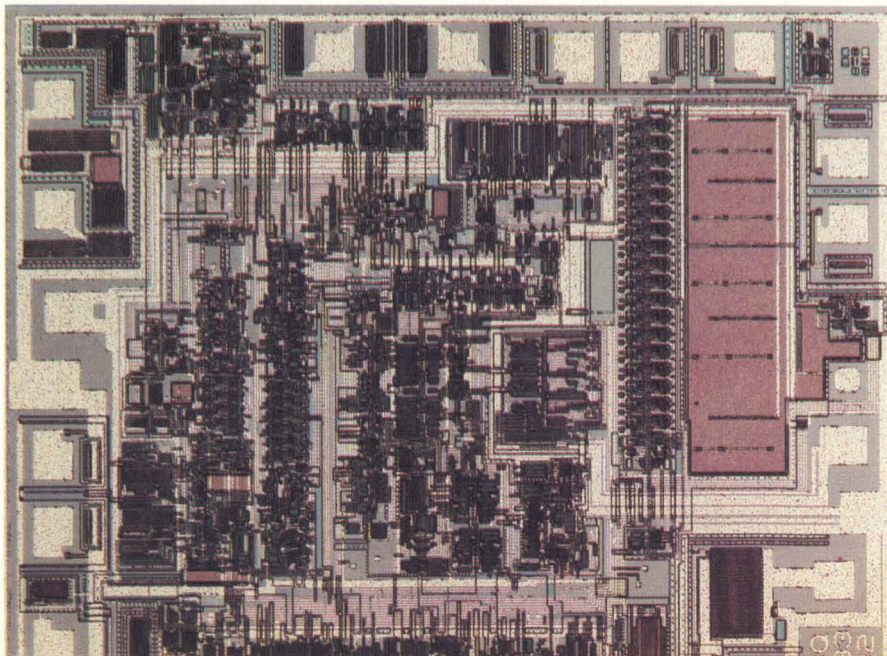
## DEPARTMENTS/Communications

### CMOS Manchester Code Converter Streamlines Ethernet Board Design

The past year has seen the introduction of Ethernet and/or IEEE 802.3 controller chips from several major manufacturers. Accomplishing the physical interface to the network, however, requires Manchester encoding and decoding of data. All of the controller manufacturers have announced intentions to make a Manchester Endec chip, but at this writing, only Fujitsu (Santa Clara, CA) and Seeq (San Jose, CA) have products available in production.

Several differences between the Seeq 8023 (numbered like the IEEE spec it meets) and all of the other Manchester chips, planned or announced, make it significant. First, the 8023 is a CMOS part; since encoding/decoding has traditionally been performed by discrete bipolar ECL, the new parts from other

*The die of Seeq's 20-pin 8023 Ethernet Manchester Code Converter.*





vendors will be integrated using the same technology. In addition, Seeq has designed the 8023 to work with either their 8001 and 8003 controllers, the Rockwell 68802 second-source or Intel's 82586. Further differences between the Seeq and Fujitsu parts is that the 20 MHz 8023 is in a 20-pin 6/10" wide package, rather than a 24-pin package twice that width running at 60 MHz.

Volume production is just gearing up, but several large manufacturers already use the part. Interlan (*Digital Design*, July, 1984), 3Com, and Bridge are using the 8023 in their newer products, and system vendors, Burroughs, AT&T (for their personal computer), and Hewlett-Packard are also designing with the part. The integration of phase lock loop, carrier sense and collision circuitry on the receive portion and crystal clock oscillator, serial to Manchester conversion, and internal loopback control on the transmit half allow quick product development. Line drivers and receivers, and handshake and logic levels to interface to the data link layer controller chips permit rapid time to market for a physical layer Ethernet link. Switching from discrete to integrated circuitry also cuts board density greatly (**Figure 1**).

Whether used in conjunction with their own 8003 controller, Rockwell's equivalent or the Intel 82586, seven lines are needed for the interface (**Figure 2**). Three lines each are used for receive and transmit, and one is used for collision information. Use with Intel's controller chip only requires pin 2 to be tied high, to change its polarity. The part is designed so that with some similar selection, it might be announced for use with other 802.3 controllers, such as the popular AMD/Mostek LANCE.

In integrating Manchester functions in CMOS, Seeq took a risk and had to consider large design changes from the discrete bipolar. But with their success, they can offer the low power dissipation and noise immunity that are increasingly critical in board design. The 20-pin package is an advantage that Intel's 82501 will share, but controller interface may be limited to the 82586.

The 20 pins are used as follows: seven-line controller interface, a three-line transceiver interface, two clock input lines for the 20 MHz crystal, three lines for loopback and 25 msec watchdog timing, two mode lines (pins 1 and 2) for 8002 compatibility and use with various

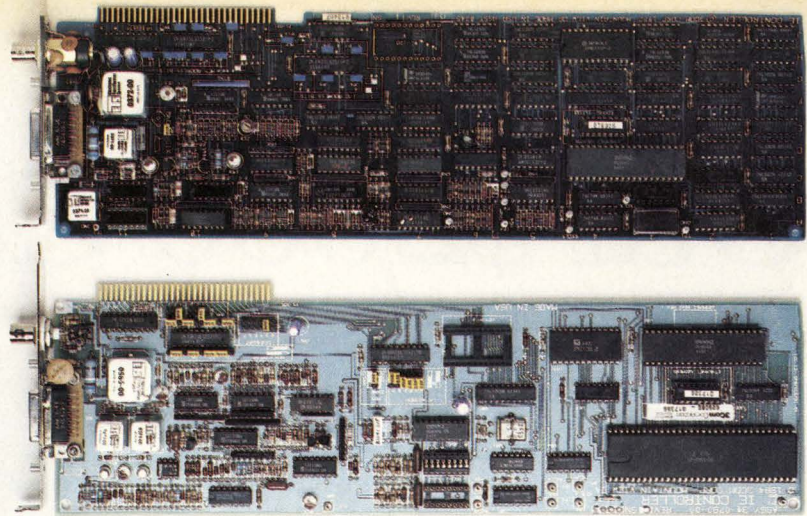


Figure 1: 3Com's Ethernet board design is simpler, not as dense using the 8023 Manchester Code Converter (upper) versus discrete bipolar parts (lower).

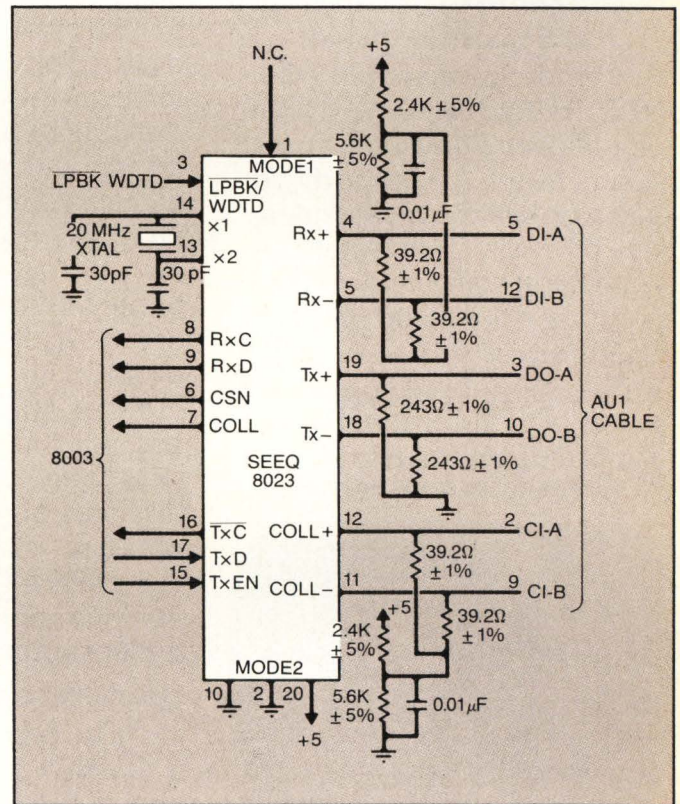


Figure 2: Pin configuration of the 20-pin CMOS Seeq 8023 Manchester Code Converter; Interconnecting the 8023 to Seeq's 8003 Ethernet controller uses seven of the chip's 20 pins.

controller chips, power to the +5V supply and ground (**Figure 2**). Using discrete logic, about 20 ICs would be required to perform all of the same functions.

By coming out with a CMOS part that functions with more than one controller, Seeq has gotten some market lead. And according to Howard Charney, VP of Engineering for 3Com (Mountain View, CA), support has been as good as availability for the part. 3Com and Seeq cooperated to bring out the 8001, the first Ethernet controller, and the Manchester IC has also been refined jointly. With the 8023 in its second or third revision, it is a stable part.

Designs requiring 802.3 physical link circuitry for rapid volume production have limited choices. It is almost certain that the Manchester chips from various vendors will not be interchangeable, though they may all meet the IEEE standard for 10 Mbit/sec Manchester code conversion. With many encoders just sampling now, the ramp up time could be prohibitive for products near market introduction. The Seeq 8023 is in production, with a price of \$34.75 per 100 units. For comparison, other vendors' Manchester chips are available in sample volumes.

-Pingry  
Write 234



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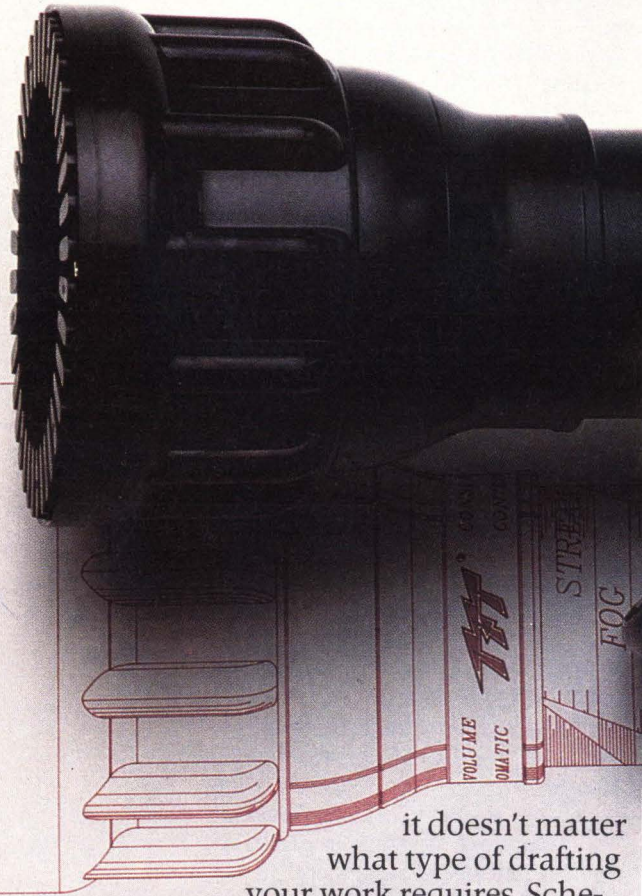
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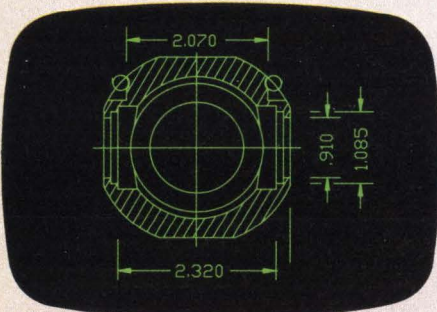
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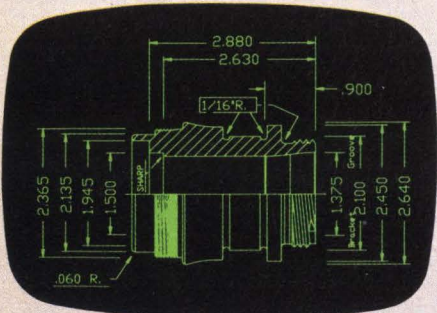


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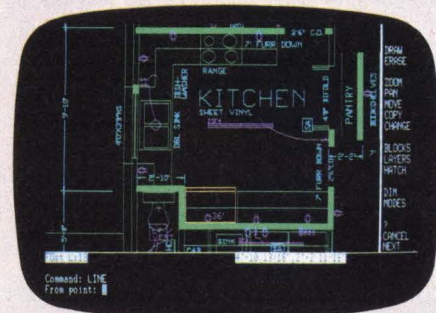
Zoom in on a part to focus on the details

AutoCAD automatically dimensions distances and angles



Architectural layout courtesy of Lansing Pugh, Architect

Solar Panel Assembly plot courtesy of Future Technology, Inc.



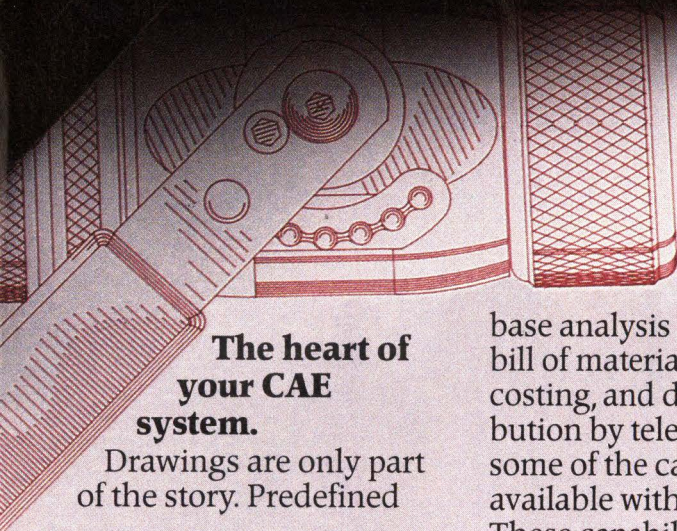
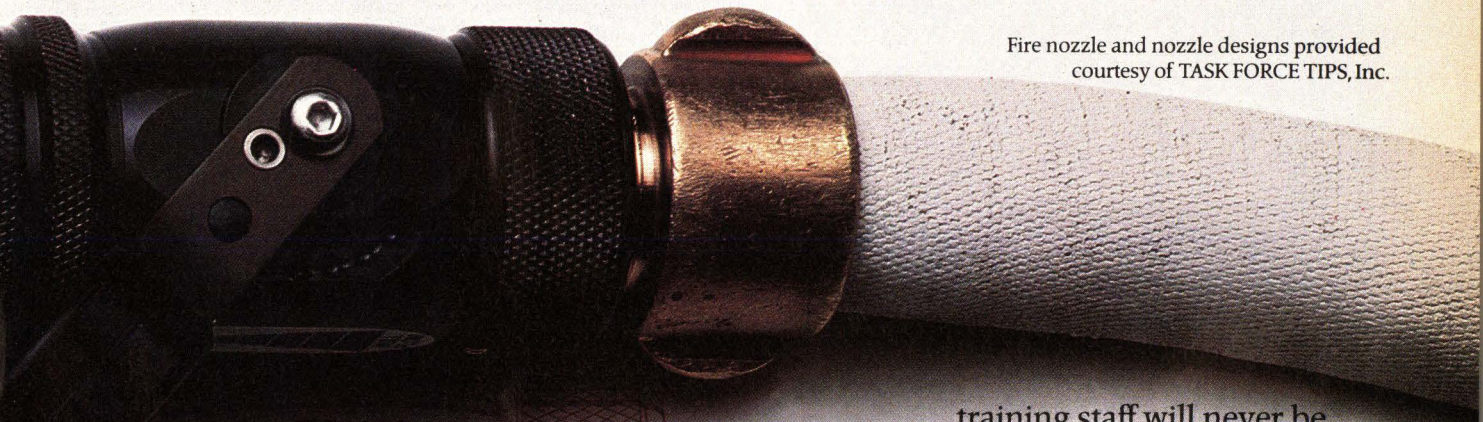
Would the Pantry be better where the stove is? Use the MOVE command

site documentation, wheelchair design, chemical plant piping diagrams, and stained glass layout have all been done with AutoCAD.



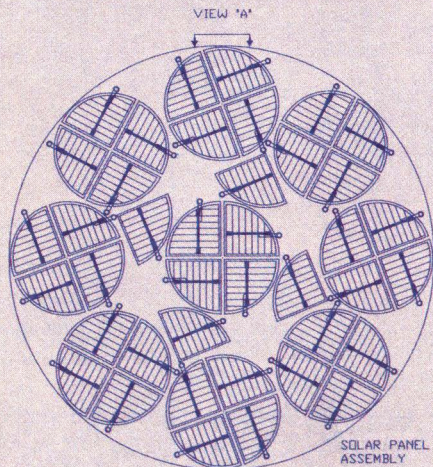
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Fire nozzle and nozzle designs provided  
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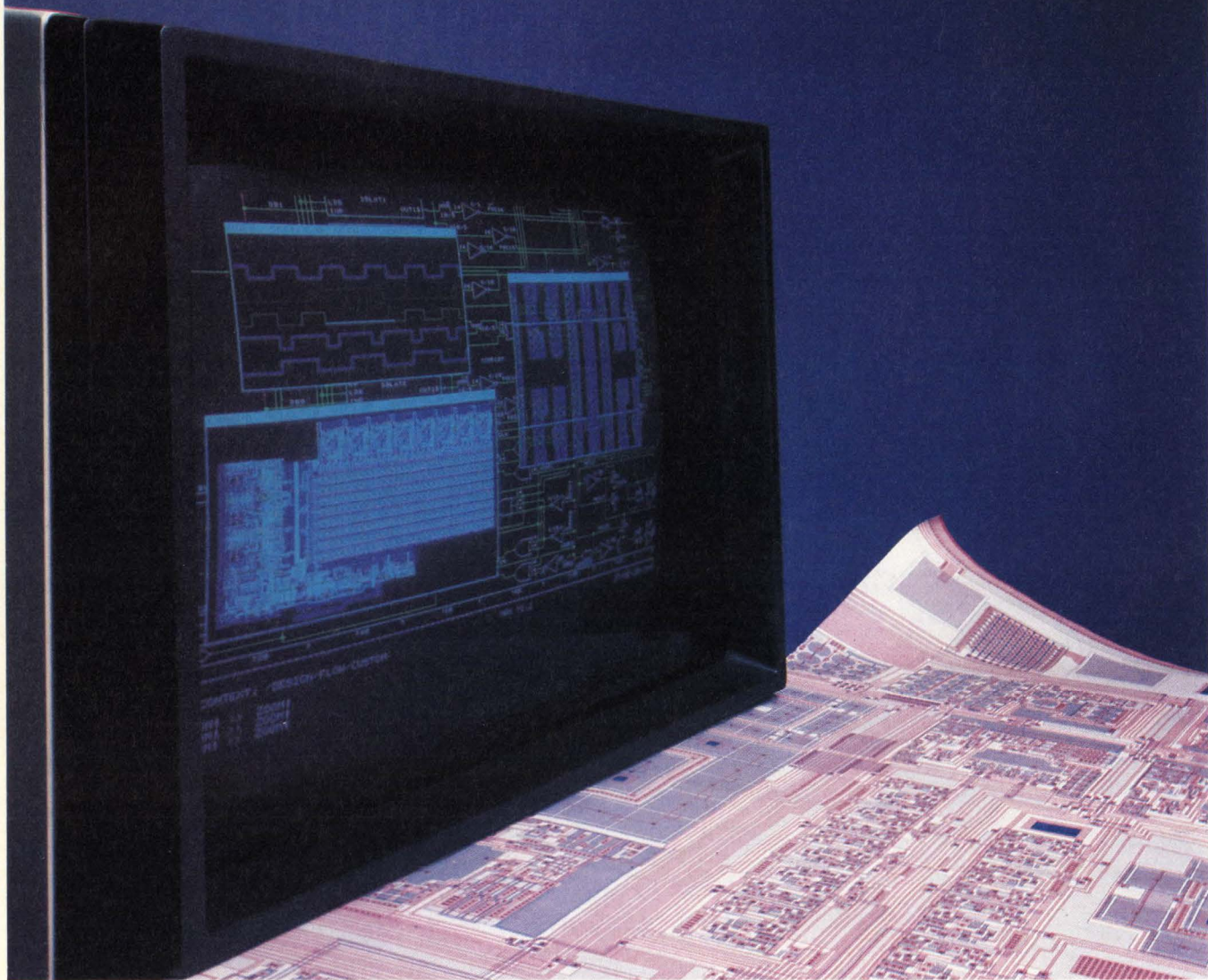


PHOTO COURTESY DAISY

# Trends And Developments In Engineering Workstations

by Ronald Collett, Technical Editor

Critical to the selection of a workstation is the question of which CAD/CAE manufacturers will remain in business over the next few years. Engineering firms looking to purchase workstations are voicing concern over choosing design systems that will not only be continually supported and enhanced, but also will not be obsolete in two years. And with stif-

fering competition between vendors and speculation of major price reductions, potential buyers may be reluctant to make purchases until the market begins to stabilize.

As with any relatively young industry, the key to selling a new product revolves around convincing the market that the product is not only a fine piece of engineering, but also that the manufacturer will not disappear and abandon its cus-

tomers. CAD/CAE vendors are painfully aware that creating a credible image is one of the major challenges they face.

Designing state-of-the-art systems that exude design savvy is another hurdle that workstation suppliers must continually leap. Most manufacturers will attest to the major engineering efforts necessary to build a full-blown workstation. On top of that, market windows for these products continue to shrink.



## Manufacturers of CAD/CAE tools continue to grow in number, but should designers use a general purpose workstation or an application-specific system?

One solution to the growing competition and narrowing market windows is to merge with a competitor. Computervision (Bedford, MA) and Metheus (Hillsboro, OR) recently embarked on such a venture in hopes that their combined efforts will keep both alive. Other similar agreements include Data I/O (Redmond, WA) and FutureNet (Canoga Park, CA), General Electric and Calma (Santa Clara, CA), Tektronix (Beaverton, OR) and VR Information Systems (Austin, TX). In addition, numerous vendors have engaged in joint marketing ventures and software support agreements.

Another component adding to the competition is the announcements from Tektronix, Data General (Westboro, MA), Hewlett-Packard (Palo Alto, CA), Xerox/Versatec (Santa Clara, CA), and Prime Computer (Natick, MA) that they too have entered the workstation business. And with all the third party software available for the MicroVax I, DEC (Maynard, MA) is another major workstation force to be recognized.

An abundance of CAD/CAE tools on the market brings forth the question of whether a particular workstation is superior to another. According to present CAD/CAE users, fully integrated systems, portable software and a full line of engineering application programs are the characteristics most frequently demanded.

Workstations based on personal computers cannot possibly offer complete solutions since they lack the computing

power necessary for tasks such as large analog simulations, place-and-route and printed circuit board layout. The key to ensuring a quality PC-based system, however, is to observe whether the design data from the PC can be ported to a larger computer system running a similar application program. Suppose, for instance, a logic simulation running on a PC takes 15 minutes to execute. Having the option to move the simulation to a larger computer requires that the design data be compatible with the host's simulator. This example can be extended to almost any computer-aided design task.

### Application Specific Or General Purpose Workstation?

Daisy (Sunnyvale, CA), Mentor Graphics (Beaverton, OR) and Valid Logic (Mountain View, CA) were the early entries into the workstation arena, but new startups as well as established companies promise to take a slice of the pie. Being first to market has both advantages and disadvantages. Having an early lead in the race is an obvious benefit, but vendors often pay the price.

The workstation industry is maturing, and as a result, certain standards are emerging. Trying to tailor or even overhaul a system to accommodate these standards can produce an inferior product. Instead of reworking the old system, developing a new, more sophisticated product is another alternative. Taking this path,

however, can lead to difficulties in maintaining compatibility between products first introduced and more recent versions. Similarly, older systems may not have the computing power necessary to execute newer sophisticated software. When software is constrained by its host the result is usually lengthy execution times.

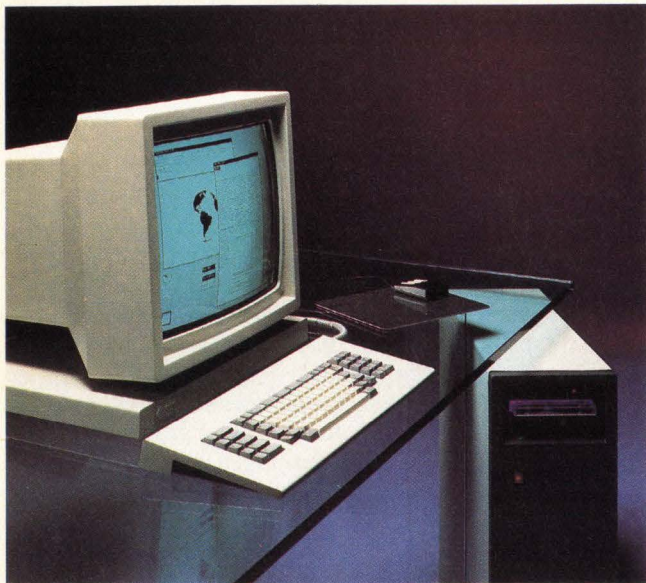
Whether to pick a dedicated workstation or a general purpose computer is a decision that requires some thought and analysis. When CAD workstations were first introduced several years ago, it was necessary to use a dedicated system. This was due to the lack of graphics performance found in general purpose computers. Although dedicated workstations could not match a general purpose computer's flexibility, they had superior graphics capabilities. Since that time, however, 32-bit general purpose computers have attained much of the sophistication once held exclusively by dedicated systems.

Some dedicated workstation manufacturers claim that the term general purpose computer leads to a false sense of security. They tend to argue that their systems are built with many off-the-shelf standard parts and bus structures. But this usually does not count for very much. Just because a system has a standard bus structure does not mean that compatible boards can simply be plugged into the cardcage. For the most part, the operating system and application software (as well as the



Figure 1: VIA Systems' workstation is based on DEC's 11/73 processor, includes a 330 Mbyte Winchester disk and runs VIA's VLSI design and layout software.





*Figure 2: Sun Microsystems' model 2/120 workstation runs UNIX 4.2bsd, is based on the MC68010 processor and has a 15 slot Multibus cardcage.*

hardware) dictate the expandability of the machine.

What is sometimes overlooked is that users do not want to spend time playing around with the system's operating system. Software support is thus a serious consideration when expanding a system.

On the other hand, dedicated systems are often optimized for particular applications. And although many general purpose systems have the graphics capabilities of an application-specific system, some do tend to be slightly slower in terms of display speed and user-machine interactivity. Then again, dedicated systems may sit idle when not called upon for CAD/CAE tasks, whereas a general purpose machine would certainly be utilized for non-engineering tasks. Obviously there are many other considerations, but above all, having a system that can meet future demands as well as today's is well worth the investment.

### General Purpose Computers for CAD/CAE

Several workstation companies have based their systems on Apollo's (Chelmsford, MA) general purpose 32-bit Domain series computers. Evidence of this is exemplified by workstations from Silvar-Lisco (Menlo Park, CA), Calma, CAE Systems (Sunnyvale, CA), Mentor Graphics and Racal-Redac (Westford, MA).

Silvar-Lisco's software, which also runs on DEC/VAX, IBM and Prime Computers, includes: Stardesigner, for design capture and simulation; Stargate, for gate array design, simulation, and placement and routing; Starcell, for standard cell design, simulation and layout;

Starboard, for PC board design and simulation; and Starcap for switched capacitor circuit design. Starboard is not a PC board layout program, but rather a software interface to popular layout programs like Scicards from Scientific Calculations (Fishers, NY). Racal-Redac offers a similar integrated CAD/CAE system called Computer Integrated Electronic Engineering (CIEE) which, in addition to running on the Apollo, runs on the VAX and IBM PC.

Other workstation vendors such as Phoenix Data Systems (Albany, NY) and VIA Systems (Billerica, MA) also offer DEC-based workstations. VIA's uses the 11/23 and the 11/73 processors for their SystemNode 100 series which runs the firm's schematic capture, simulation, IC layout and circuit fabrication software. VIA also integrated ECAD's (Santa Clara, CA) design verification software into their system.

ECAD's CAE system not only runs on VIA equipment, but on the VAX, Apollo, IBM, Data General and Gould Computers as well. This package, named Dracula, is a layout verification system that includes: design rule checking; electrical rule checking; layout/schematic consistency; layout parameter extraction; and critical path timing verification.

Phoenix Data Systems also offers DEC VAX-based systems. Their System 5000 workstation is based on the MicroVax I, the System 6000 on the VAX 11/725 and the System 7000 on the VAX 11/750. The software for these systems includes: Hiss, a schematic capture program; Waves, a waveform analysis module; Hail, (hierarchical auto-interactive layout system)

for transforming symbolic data into layout; Maskap, for electrical rule checking, electrical parameter extraction and checking, logic verification, short/connectivity analysis; and a 12-state, event driven, mode and strength sensing simulator.

Although DEC themselves have not specifically undertaken a CAD/CAE software development project, they have entered several cooperative marketing agreements with third party vendors. Their new partners include VLSI Technology (San Jose, CA), Silvar-Lisco, GenRad (Concord, MA), University of California-Berkeley, NCA Corp. (Santa Clara, CA), Phoenix Data Systems and Scientific Calculations.

At the Design Automation Conference (DAC) this past June, these vendors displayed their software running on VAX systems at DEC's booth. VLSI Technology's software included schematic entry, simulation, layout and design verification for VLSI design tasks. Silvar-Lisco showed their Structural Design System module which includes schematic entry, netlist extraction and database management along with the GARDS module for gate array layout.

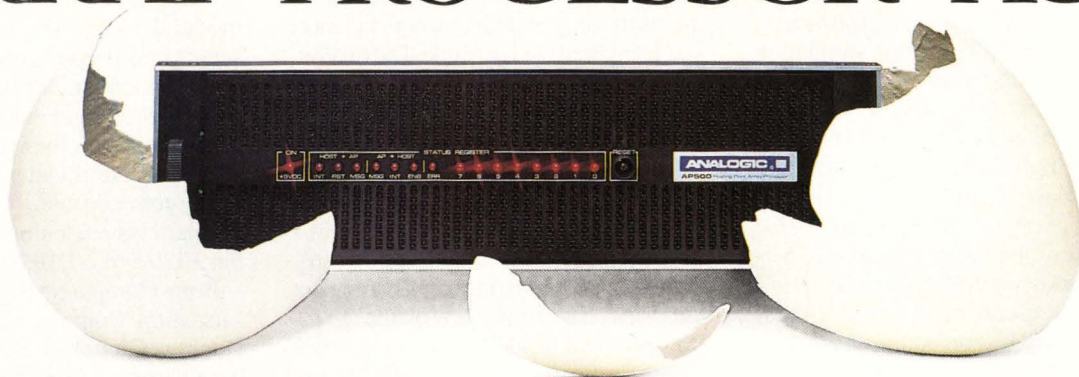
The Engineering Test Products Group of GenRad displayed the HILO-2 simulator which offers gate- and functional-level logic simulation, timing verification, fault simulation and functional modeling (HILO-2 also runs on IBM, Apollo and Prime computers). Design automation tools developed at the University of California include the KIC2 VLSI layout editor and SPICE2 circuit simulation package. NCA demonstrated its latest version of the NCA/DVS VLSI design verification system. This tool addresses all phases of the IC design cycle, including design verification and mask pattern generation. Scientific Calculations showed Scicards and Schemactive, a schematic capture package.

Prime Computer, known for their Series 50 general purpose 32-bit computers, provides their electronic design management system (EDMS) which enables users to interface to many common third party CAD/CAE software packages. Scicards, the TEGAS-5 logic/fault simulator from GE/Calma, and Merlyn, a gate array routing system from Tektronix/VR Information Systems are a few of the design packages that link to the EDMS. In addition, EDMS combines a component library, a design database and electronic design utilities with the various software interfaces.

Prime has also made Themis, their in-



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house logic simulator, available to Series 50 users. Themis is capable of simulation and testing on switch, gate, functional and network levels. Fault simulation and delay modeling as well as four-state, three strength MOS circuit simulation are all part of this software.

Data General (DG) also recently announced their entry into the 32-bit workstation market with the DS/4000 and DS/4200. Based on the Eclipse MV/4000, the new family of systems offer high-resolution graphics, local area networking and run either Data General's Advanced Operating System/Virtual Storage (AOS/VS) software or a native Berkeley UNIX operating system.

Equally important to adopting a standard operating system such as UNIX is DG's effort to support several networking standards. By using the Transmission Control Protocol/Internet Protocol (TCP/IP), the family can coexist in local area networks that comprise non-Data General equipment. This protocol was originally developed at the University of California at Berkeley (for the Department of Defense) and has become a standard LAN protocol for UNIX. A connection-oriented point-to-point protocol, it offers features such as file transfer and remote terminal log-on through Telenet.

The Transmission Control Protocol, or TCP, monitors the flow and sequencing of data to insure error free transmission

from the host. Internet Protocol, or IP, services the TCP when files are being transferred, and provides information to the TCP. IP is primarily responsible for the addressing of nodes on both the local and interconnected network. The two systems also have IEEE-802.3 (Ethernet), SNA and X.25 networking capability.

Data General's DG/UX, an implementation of Berkeley UNIX, is a demand paged, virtual memory operating system that is supposedly compatible with the 4.1 Berkeley Software Distribution (bsd). According to the firm, users may select the bsd C-Shell interface or the AT&T Bourne Shell. In addition, DG/UX offers compatibility with AT&T UNIX 5.2 and selected features from 4.2bsd: a faster file system; and as mentioned, networking support.

Another workstation manufacturer supporting Ethernet, the TCP/IP protocol and the UNIX operating system is Sun Microsystems (Mountain View, CA). All three of their workstations, the Sun-2/120, Sun-2/120FS and Sun-2/170 run Berkeley UNIX 4.2bsd, are based on the MC68010 processor, have 16 Mbytes of virtual address space and accommodate up to 4 Mbytes of physical memory.

The system configurations are almost identical; the primary difference is the 120's 9-slot Multibus cardcage and the 170's 15-slot cardcage. The 120 also has 1 Mbyte standard main memory as well

as disk and tape options for local mass storage whereas the 2/170 offers 2 Mbytes of main memory. Also, the 2/170 is housed in a 19" rack-mountable package. The model 2/120FS acts as a network file server and is configured without a bit-mapped monitor, display controller, keyboard, and optical mouse. Instead of the graphics display, the user supplies a standard ASCII terminal which functions as the system console. Otherwise, all the standard system features and options for the 2/120 and 2/120FS are identical.

Both Computervision/Metheus and Lucasfilm Computer Division (Marin County, CA) offer Sun Microsystem-based workstations. Lucasfilm offers Cadroid, a schematic capture package, and Wrapdroid, a place-and-route program for wire wrapped boards. In addition to running on Sun workstations, these programs can be ported to Apple's Lisa, Apollo Domain and Cadmus Systems' (Lowell, MA) CADMUS 9790.

All members of the CDS 3000 series workstations from Computervision/Metheus are based on Sun's equipment. Among the models available are two desktop engineering workstations of the CDS 3300 series and two configurations of the CDS 3900 series Shared Resource Manager. The CDS 3300 series includes the 3310 clustered workstation and the 3311 standalone workstation. Application software for the 3000 series includes: schematic capture, logic simulation, timing analysis, functional modeling and fault analysis.

The CDS 3900 series 3901 and 3911 serve as central data and peripheral management resources for clusters of terminals. Both units have 300 Mbytes of on-line disk storage and support peripherals such as printers and plotters. The 3911, however, provides additional graphics support capabilities.

Sun is also an OEM for Chromatics (Tucker, GA), manufacturer of VLSI design workstations. Sun's model 2/120FS will be used in conjunction with the Chromatics CX 1500 Colorgraphic Engine. The CX Color Graphic Display System provides a 500,000/sec vector drawing speed with 1536x1152 resolution using a GKS package.

In addition, Chromatics uses the Sun equipment in its new VLSI Designer II Workstation. This system includes: CAEPAC II for schematic capture; CAEPAC III for design rule checking; CAESIM for logic simulation; CAEPAC IV for design verification consistency between the schematic and layout;



Figure 3: Hewlett-Packard's 9000 series Model 520 desktop workstation has a 5¼" floppy disk, can accommodate up to 5 Mbytes of RAM and runs HP-UX.



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CAEPAC V for auto routing gate array and standard cell designs; and CAELIST for netlist extraction. This netlist extraction program reformats the CAEPAC II database for input to CAESIM, SPICE, CAEPAC IV or user-defined formats.

Hewlett-Packard (HP) continues to capture market attention with their 32-bit series 9000 workstations which include the models 520, 530 and 540. The computing engine behind these machines is HP's proprietary 32-bit processor. One of the interesting features of this line is that the systems can be upgraded to accommodate three CPU cards, which supposedly increases the speed by as much as 2.8 times. When upgrading, the operating system oversees and maintains the extra processors so no reprogramming is necessary.

All three systems run under the HP-UX operating system, a UNIX extension that is fully compatible with Bell Laboratory's UNIX. Some of the additional features of the HP-UX operating system include virtual memory capability and networking (Ethernet). A general purpose emulator allows communication with any remote system that supports logon asynchronous ASCII terminals. HP-UX offers the standard UNIX communication tools — `cu`, `uux` and `uucp` — for terminal emulation, file transfer and remote executions with other UNIX or HP-UX systems.

HP does not offer a wide variety of CAD/CAE software, but there are many third party UNIX packages. With a superior reputation for supplying test equipment, HP have now committed themselves to the workstation market and are aggressively involved in a third party software support program. For instance, software is available for establishing communications between these systems and IBM or DEC VAX mainframes.

A newcomer to the workstation battleground, Mosaic Technologies (Billerica, MA) recently unveiled a 32-bit UNIX-based workstation built around National Semiconductor's (Santa Clara, CA) NS32000 chip set. This includes: the 32032 processor, the 32081 demand-paged memory management unit and the 32081 floating point processor. In addition, a 16 Kbyte high speed cache, 16 Mbytes of virtual address space, 1 to 8 Mbytes of ECC RAM and a dedicated Am29116 graphics processor make this a truly high performance system.

As far as standards are concerned, the Mosaic operating system is UNIX 4.lbsd with features from 4.2bsd and System V. For communications and hardware



Figure 4: Hewlett-Packard's 9000 series model 540 workstation can be configured with three processors, runs HP-UX, supports up to six users and each I/O processor adds 8 DMA-capable I/O slots.

expansion, Mosaic has incorporated two RS-232 asynchronous ports, an Ethernet interface and Multibus cardcage. Terminal emulation software for the VT100 and Tektronix 4014 is also available.

### The Big Three

There is no doubt that Daisy, Mentor and Valid are the frontrunners in this fast

moving industry. One of the major advantages of these systems is the numerous agreements that have been signed, with vendors of semi-custom (gate array and standard cell) devices. These agreements allow the chip vendor's component libraries to be ported to the workstation. If the front-end semi-custom design tasks are to be done in-house, then it is necessary to



Figure 5: Daisy's Megalogician is a completely integrated workstation with capabilities ranging from schematic capture and gate array place-and-route to hardware simulation and physical modeling.



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have either a link between the vendor's CAD system or a self contained system that holds the vendors library. And to date, most semi-custom houses have signed with at least one of these three workstation suppliers.

Both Daisy and Valid built their systems around proprietary hardware. However, Valid's Scaldsystems I and II run an extended version of UNIX 4.1. Similarly, Daisy's spec-sheets speak of an already existing UNIX-based system, but recent statements from the firm indicate that the UNIX engineering effort is near completion. So the question still remains as to what degree of compatibility this UNIX will offer. Nonetheless, both the Daisy Megalogician and Valid Scaldsystems are highly sophisticated integrated workstations that offer complete design capabilities from schematic capture to physical modeling.

Most industry experts agree that simulation and design verification are the most important functions of a CAD/CAE system. And this is where dedicated systems often outperform their general purpose counterparts. Mentor, Daisy and Valid workstations offer hardware accelerators that cut simulation and design verification execution times by orders of magnitude. Both Daisy and Valid built their own accelerators while Mentor worked with Zycad (Arden Hills, MN) to acquire a similar system.

Daisy and Valid have also engineered physical modeling systems that link to their existing workstations. Daisy's Physical Modeling Extension (PMX) and Valid's Realchip allow actual chips to be used in simulation. The user simply plugs these ICs into the machine, and the simulation uses the software models and the chip to execute the simulation.

Although Mentor was an early entry into the market, they designed their system around Apollo's Domain computers as opposed to building a new system. Originally designated the IDEA 1000 series, the firm recently renamed the series with functional descriptive designations. In addition, a new lower cost workstation called Capture Station has been added to the product line. Capture Station primarily addresses schematic capture needs.

Other workstation configurations from Mentor include: Idea Station, for simulation and timing verification; Spice Station, for analog simulation; Gate Station, for gate array design and layout; Cell Station, for standard cell design; Chip Station, for full-custom design; Test Station,

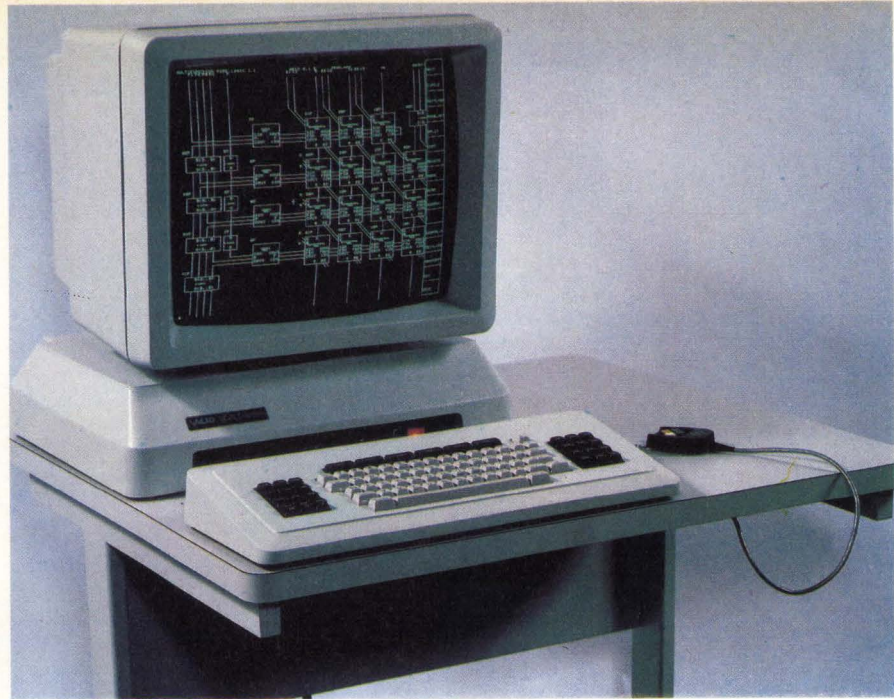


Figure 6: Valid Logic's Scaldsystem can be configured with Realchip for physical modeling and Realfast, a hardware simulator.

for hardware verification via logic analysis; and Doc Station, for documentation and database access.

This series of workstations can reside in several different desktop computational nodes that have anywhere from 1.5 to 4 Mbytes of main memory and perform up to 1.2 MIPS. As mentioned earlier, Mentor's workstations have a hardware accelerator, XSIM, for logic simulation as well as an interface for Zycad hardware simulators.

### Conclusion

Compatibility between workstations is one of the most important issues surrounding today's workstation industry. Based on the systems currently available, the obvious compatibility trends are the use of the UNIX operating system and Ethernet, as well as software that will run on VAX, Apollo and Sun Microsystems computers.

A problem that is somewhat obscured in the descriptions of these products is the issue of design data compatibility. To transfer data between systems requires that the data's format be compatible. This has been an area of concern for workstation manufacturers, because each would like their particular formatting scheme accepted as an industry standard. This is, of course, impossible.

For several years a number of committees composed of representatives from different vendors have attempted to

devise a standard. Unfortunately, most have failed. On the brighter side, one is on the verge of success. This committee, which includes Daisy, Mentor, Motorola, National Semiconductor, Tektronix and Texas Instruments, is about to release version 1.0 of the Electronic Design Interchange Format (EDIF). This represents a significant breakthrough in compatibility.

If EDIF becomes a standard, there will be winners and losers. The winners will be those that adopt it as soon as it is released while the losers will be those that wait until it is a recognized standard. One known manufacturer other than those involved in creating the format that plans on adopting it immediately is FutureNet/Data I/O.

Finally, whether to use an application-specific workstation or a general purpose computer should be thoughtfully decided. One thing is certain: workstations will eventually become a necessity as opposed to a luxury, and system architects planning to purchase such a system must decide when that time arrives. □

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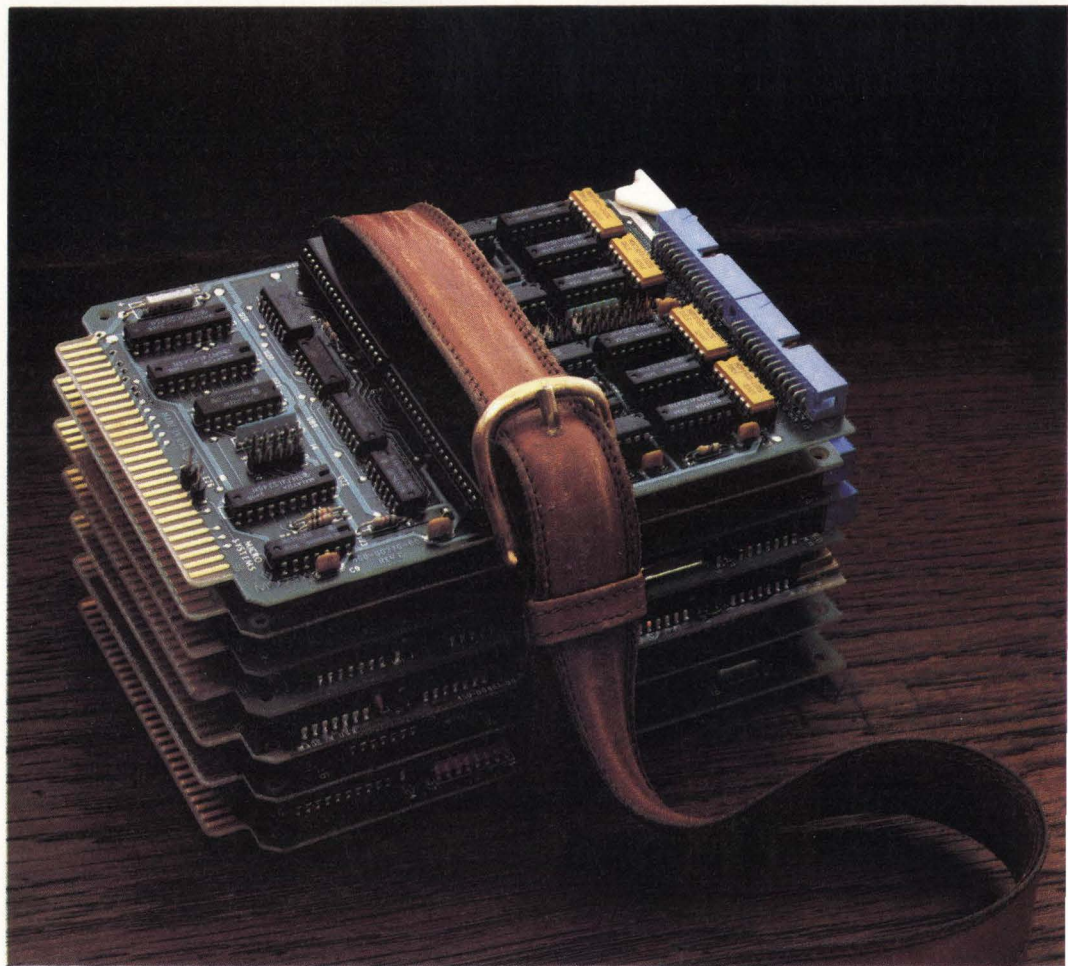
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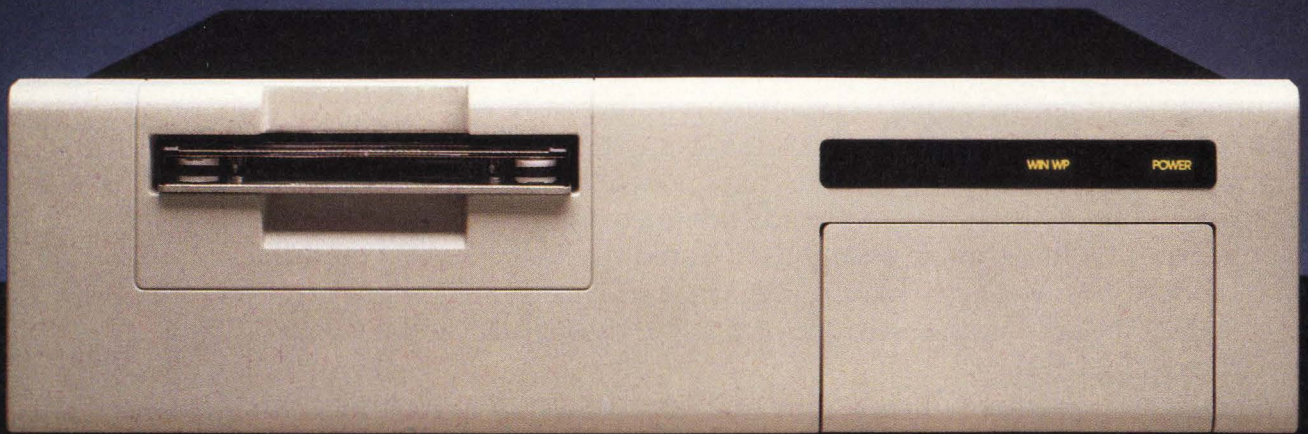
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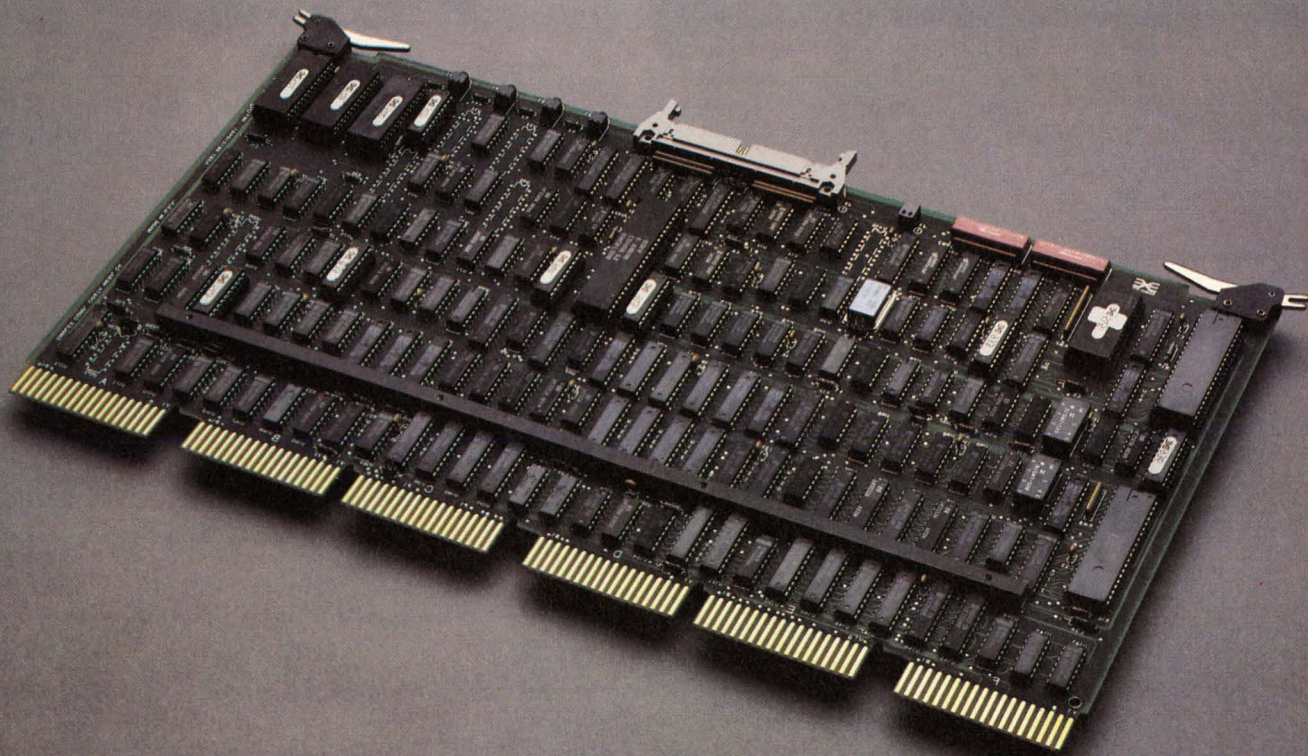
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# Designer's Guide To The Q-bus/Unibus

by Dave Wilson, Executive Editor

For third party vendors, keeping up with Digital Equipment Corp. strategy in the OEM business has become a difficult if not impossible job. In some market areas, it appears that DEC — if not actually providing encouragement — allows vendors to design and manufacture compatible products without any undue problems. From the announcements of the J-11 and T-11 chip sets together with a range of development tools, DEC seems to be trying to stimulate activity around its microprocessors rather than to curtail it.

Allowing third parties to build DEC compatible products has its advantages and disadvantages. On the positive side, it may eventually be responsible for selling more DEC machines, since the variety of products available to the OEM will be greater and more diverse than those available solely from DEC. But since DEC is also in the board and system business, those products may present a conflict with DEC's own interest by providing greater capability than equipment available from DEC.

Whereas smaller computer companies will promote the con-

cepts of open systems architecture and industry standard interfaces, the larger companies will often protect their large installed base of machines by doing something different. In some cases, this results in sophisticated high-speed interfaces being introduced, giving the larger companies an edge over their competition. They do not get involved with slow decision making committees from several vendors who may take their time and disagree about the final spec.

In the scientific and technical marketplace, smaller start-ups are emerging with relatively low-cost UNIX/Ethernet/ Multi-bus workstations challenging the role once held by the mini-computer giants. However, even if phrases like "power of the '780 for \$40,000" can be justified, these smaller vendors have much catching up to do. Primarily, this is because of the enormous installed base of VMS and not UNIX software that has been tailored specifically for the design environment. Second,

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*Above: The Emulex UCI2 host adaptor emulates the MSCP protocol and fits in any single hex slot of a standard PDP/VAX-11 backplane.*



the importance of communication between workstations and a central host is of primary significance.

Albeit late in introduction, the microVAX on the Q-bus completes a range of machines from DEC, from the microVAX 1 to the VAX 11/785, that offer compatibility from the low-end to the high-end. When the 32-bit BI bus-based microVAX 2 and microVAX 3 workstation products are announced, they should protect Digital's installed base further. Hedging their bets even further against the UNIX threat, DEC recently announced VAX Ultrix for their range of VAX machines.

## Controllers

One of the most important areas of computer design, particularly as it relates to workstations, is in the area of access to data on disk and tape, the role held by disk and tape controllers. In the open market, the performance push has led to the introduction of new disk and tape interfaces, and the distribution of intelligence into the peripherals.

Initially, it appears that these new interfaces may actually leave the controller houses to manufacture nothing more than a bus adapter. IPI, for example, seen by many to be the successor to the SMD, takes the formatter away from the controller and places it onto the disk drive. Although this trend is likely to continue, there is plenty of room left for the controller houses to add value in their products.

One dominant performance enhancement that is likely to be addressed soon is the partitioning of operating system functionality between the host and the controller. As a result, disk controllers may perform file management duties in the system, removing the burden from the host system.

This overall direction that the industry is taking has not been overlooked at DEC. In 1982, DEC specifically announced their own mass storage control. DEC's plans included a new controller, the UDA50, and a new series of disk drives that have been shipping very slowly even today. These included the RA60, RA80 and RA81. Introduced at the same time were Digital Storage Architecture and the Mass Storage Control Protocol, known now as the DSA and the MSCP.

Since then DEC has brought the architecture down to the small systems end of their business. First product out was an RQDX-1 Q-bus controller that received poor acceptance in the marketplace, according to industry sources, because of its low performance. There is speculation that DEC is working on a QDA50 controller for the Q-bus that may be announced by the end of the year.

Performance considerations were not the only rationale behind the new architecture. In the past DEC had a hard time trying to cut loose old drives from supported operating systems, leaving some customers out in the cold. Every time a new version of an operating system was announced, DEC had to ensure that the drive for the obsolete products were compatible with the new operating system.

Within the framework of the DSA, mass storage functions are partitioned into three separate components — host, controller, and drive (**Figure 1**). Each component supports defined tasks, and corresponding layers within the components are able to operate independently of the other layers. Central to this philosophy is the reduced role of the host software in mass storage control. Device specifics such as drive types, geometry format and error recovery are no longer host concerns. Instead, important host issues concern device class, number of available storage blocks and if needed, error reporting — freeing the host



*DML's UDA50 compatible intelligent disk controller implements both the MSCP and the DUP protocols.*

up to address more important tasks such as executing applications software.

Under DSA, the bulk of the mass storage functions are off loaded to the controller. The controller employs a high degree of intelligence that determines the number of subsystem devices, their type, geometry and unit number, capacity, availability, and status. It receives and optimizes I/O requests, executes those requests and manages the data transfer between the host and the drive. It also performs the translation between the logical addresses of an I/O request and the physical drive address. Moreover, the controller performs all error detection and recovery transparent to the host. The host's only responsibility at this level is to handle any error messages reported back to it.

The last item in the DSA partition is the drive. Data rates are faster, capacities are greater and access times are reduced. Furthermore, the host is independent of bus specifics or device type. The controller and drive subsystem appear to the host as an ideal storage device, characterized by a fixed size error free medium.

## MSCP

The Mass Storage Control Protocol (MSCP) is used by all members of the DSA family. It is a packet-driven approach to subsystem communication where the MSCP controller handles all details of I/O related tasks. The host simply sends command messages to the controller, such as reads and writes, and receives responses from the controller as each command finishes. A diagram of the MSCP subsystem is shown in **Figure 2**.

The host uses two software levels to support its end of the MSCP subsystem. The higher level, the "Class Driver," assembles command messages, sends them to the controller and receives response messages. The class driver does not handle details of I/O communications and message handling. It leaves this to lower level software functions maintained by the "Port Driver." The port driver passes messages to and from the com-



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DT2758	A/D dual	4SE	Simultaneous inputs, 4 level interrupts	100	•	•
DT3362	A/D quad	64SE 32DI	Dual Port, channel/gain list, PGH	50/250	•	•
DT3368	A/D quad	12SE	Dual Port, Simultaneous inputs	100	•	•
DT3382	A/D quad	64SE 32DI	Multi-channel, PGH	50/250	•	•
DT3388	A/D quad	12SE	Simultaneous inputs	100	•	•
DT2751	D/A dual	2	D/A, 4 level interrupts	200	•	•
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munications link or bus. At this level, the port driver is unaware of the messages' meaning or of the exact nature of the bus communication link.

There are also two software levels in the controller. The lower level is called the port driver. Like the port driver in the host, it passes messages on and off the bus. The true intelligence of the controller, however, is in the higher level "MSCP server." The MSCP server determines which devices are connected to the controller. These include the number of devices, type, their geometry, unit numbers, capacities, availability and status. The MSCP server receives host command requests, and can optimize those requests. It also initiates data transfers both to and from the host, and to and from the storage device. It provides data buffering, error detection, error correction and error reporting.

An additional function provided by the MSCP server is "dynamic bad block replacement." When a data block becomes marginal, the server activates a Replacement Control Task (RCT) in the host. RCT buffers the corrected data, marks the block bad, and then moves the data to the replacement block. During normal data transfer operations, when the "marked bad" block is encountered, the server automatically vectors to the replacement block and continues the data transfer.

In the MSCP subsystem, there are two levels of communication—the physical level and the logical level. The physical level proceeds through both the port driver and the bus interconnect. At the logical level, the class driver communicates with the MSCP server via MSCP protocols, while the port drivers communicate with one another via System Communication Architecture (SCA) protocols. The connection between the host and supported devices occurs via DMA transfers to and from a host memory communication region called the command/response ring (Figure 3). The port driver polls this region for command messages while the host polls it for responses. I/O operations start when the host deposits a descriptor pointing to a command in the command ring. The operation is complete when the descriptor pointing to a corresponding response packet is removed from the response ring by the host. Interrupts occur when the command ring makes a transition from full to empty or when the response ring makes a transition from empty to full. This mechanism minimizes the interrupt overhead required by the host during peak I/O loading.

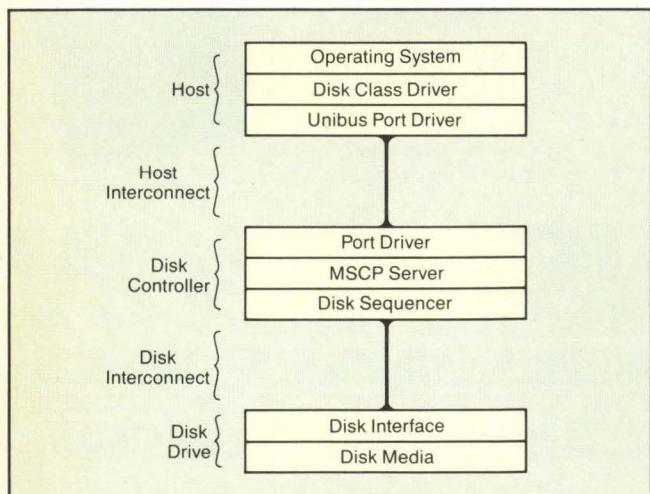
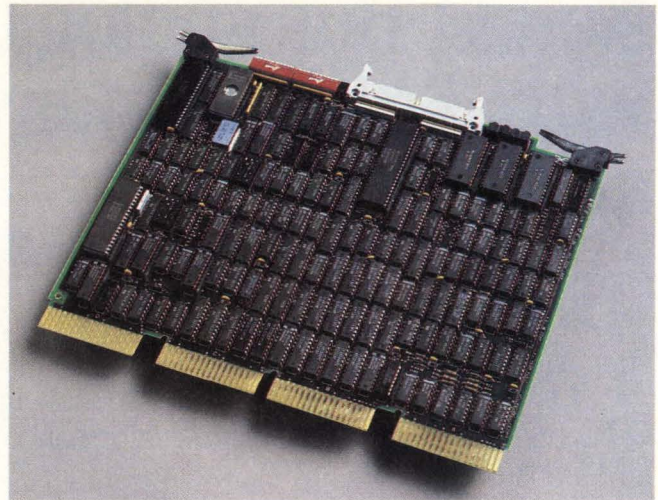


Figure 1: The Digital Storage Architecture (DSA).



The Emulex UC02 host adaptor emulates the MSCP protocols and fits in any single quad slot of a standard LSI-II backplane.

### Command Stacking

Building a controller to meet the DEC specification is not a difficult task, but it is compounded by two problems, the greatest of which is the lack of information about DSA. Shortly after the introduction, DEC strictly limited the availability of the UDA50 programmers documentation kit. The second problem is designing products with performance characteristics that will allow the architecture to work at high performance levels. The UDA50 has basically done that through enhanced throughput techniques, error detection and correction and diagnostic and disk maintenance techniques.

Command stacking and seek ordering allows a number of re-

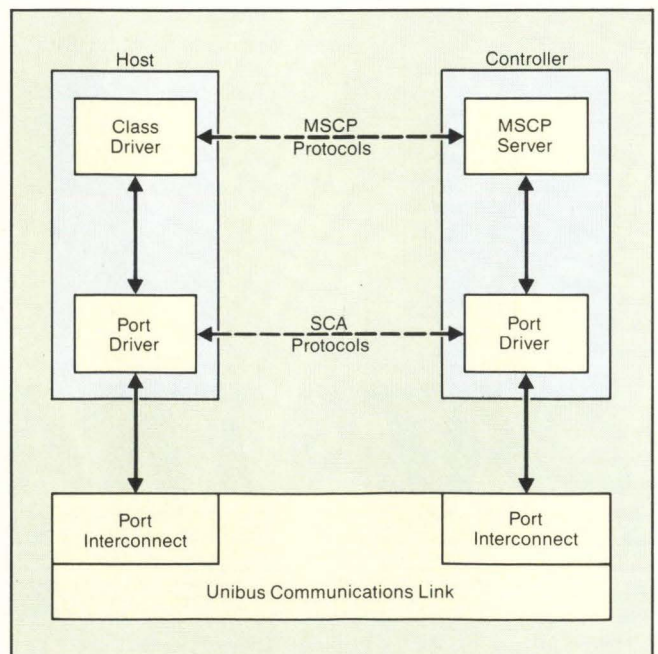


Figure 2: The Mass Storage Control Protocol (MSCP).



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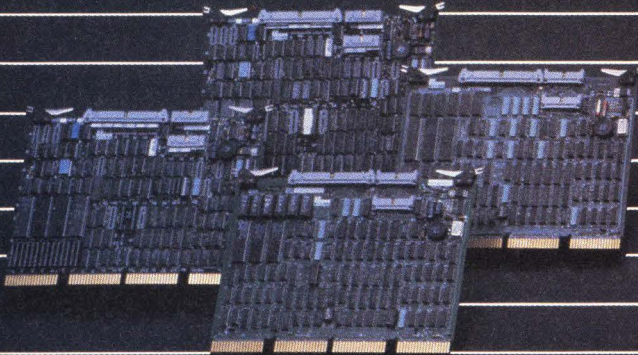
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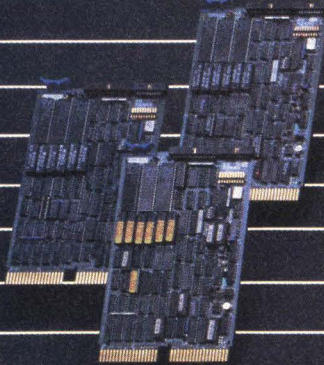


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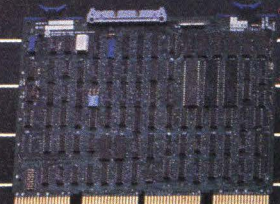
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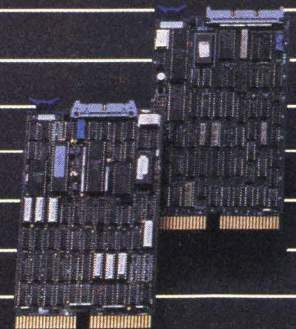
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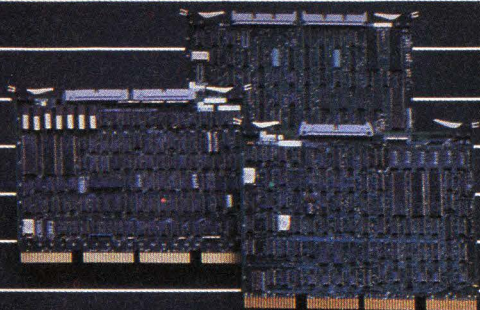
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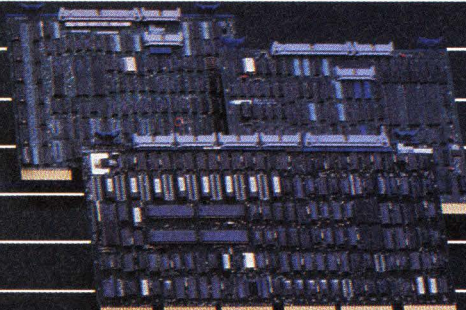
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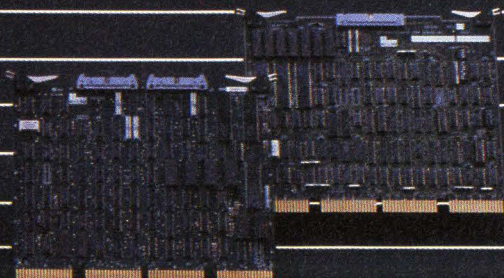
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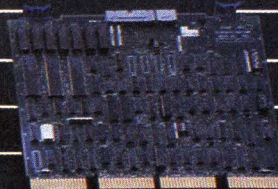
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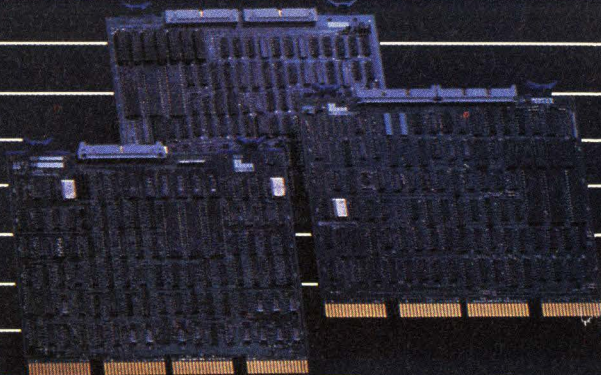
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quests to be stored in a queue. These requests are sorted to set up logical command queues for each disk in the subsystem. When a disk has more than one request present, the controller rearranges them in order to execute the requests by cylinder address instead of order received. Another level of optimization may be obtained through overlapped seeks and rotational position sensing.

To provide rotational optimization, a real-time status of radial distance is maintained between the read/write head and the requested section for each disk in the subsystem. The drive nearest its beginning requested sector is selected to perform the data transfer.

Media defects in subsystems typically cause disk volume to be fragmented because of the unusable disk sectors. This degrades file processing performance and makes data backup tenuous and time consuming. By implementing a revectoring process, however, it is possible to improve performance. When an unusable sector is detected, a replacement can be referenced on the same or nearest adjacent track without having to reseek to a look-up table. This results in use of large contiguous sectors without concern for possible bad sectors. These performance enhancement techniques are implemented through algorithms that are not defined in the MSCP. The problem third parties face is what algorithm to implement to provide a performance level to compete with DEC.

If that isn't hard enough, DEC also has implemented a set of diagnostic and utility protocols in some of their high-end products. The DUP commands allow the controller to move a program in host memory to its own buffer and begin program execution as well as allowing the controller to search for a specific program on a drive, load it and begin execution. Currently, drives are formatted through that protocol. In order for third parties to meet this part of the DEC spec, it is necessary to put a PDP-11 on board the controller. In the UDA50, for example, DEC has designed a bit-slice emulation that looks strikingly similar to the PDP-11. DEC also does not publish the instruction set to this processor, compounding the design problem.

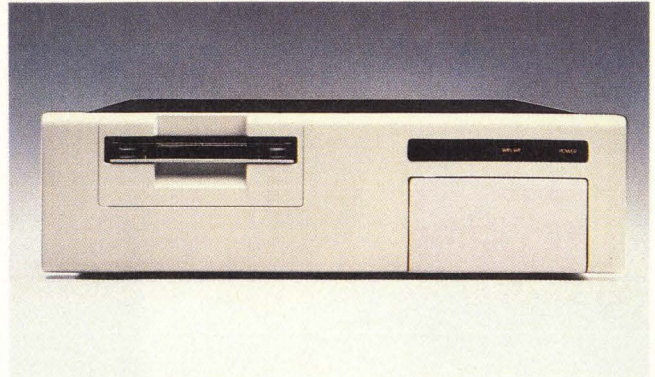
**Intelligent Functions**

In the future, DEC may use the DUP to help migrate more intelligent functions to the controller. Because of the generic nature of the MSCP, a standard set of commands at a higher level than read/write may be executed—like file transfer.

DEC is already moving towards that with the HSC-50. Although it is not claimed to be a file server, it could, with little effort, become one. That sort of configuration would be a natural progression for DEC to take—pulling increasingly more of the driver that used to be unique to the O/S out to the controller.

It is also conceivable that DEC could use the DUP to force diagnostics into the controller to ensure that only a board from DEC is in the system. Most third party vendors have mixed opinions about whether this will become a reality.

In their low-end controller, the RQDX-1 on the Q-bus, DEC does not support the DUP. Third parties claim that it would not be cost-effective for the company to build a PDP-11 look alike controller board and stay within the price range that their customer base demands. Similarly, there is also the question of how many of those high-end features like RPS, overlapped seeks and command stacking need to be supported in a low-end product. Third parties will probably take a "wait and see" approach. If DEC announces an inexpensive product that does have those



The DEC compatible Cyclone subsystem from Qalogy (formerly Data Systems Design).

characteristics, they may be forced into designing something similar.

Most controller houses interface their products to industry standard interfaces, like ESDI and ST506 to hook up to drives from vendors like Fujitsu and Priam. DEC, on the other hand, has defined a radial serial co-axial interface to hook its high-end controller products to its drives.

Consequently, third party controllers, for example, take commands out of the command ring, stack them in a similar manner to the UDA50, but instead of converting directly to serial bit stream, data is converted to a parallel data stream that goes out to a SCSI controller along with the read/write command packet information. The SCSI device then actually does the read or write. This allows multiple drives to be dropped off the

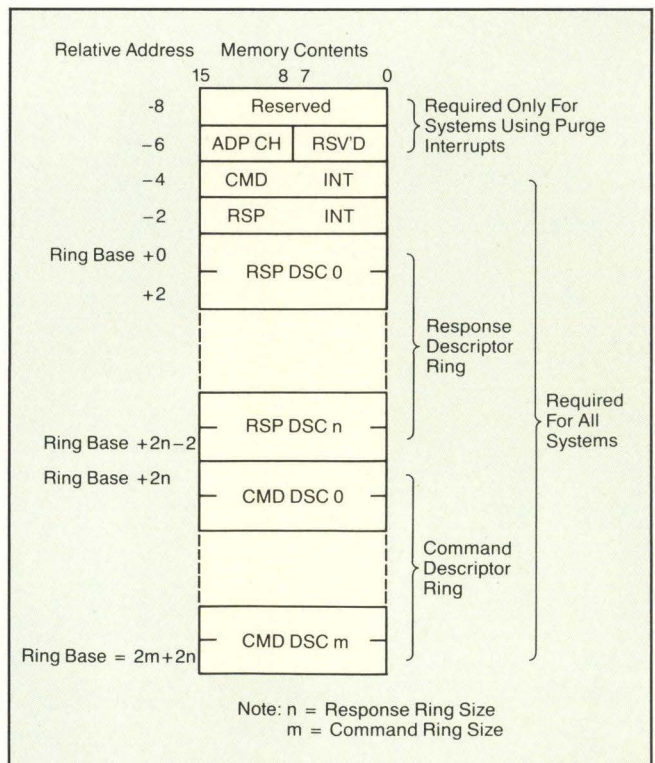
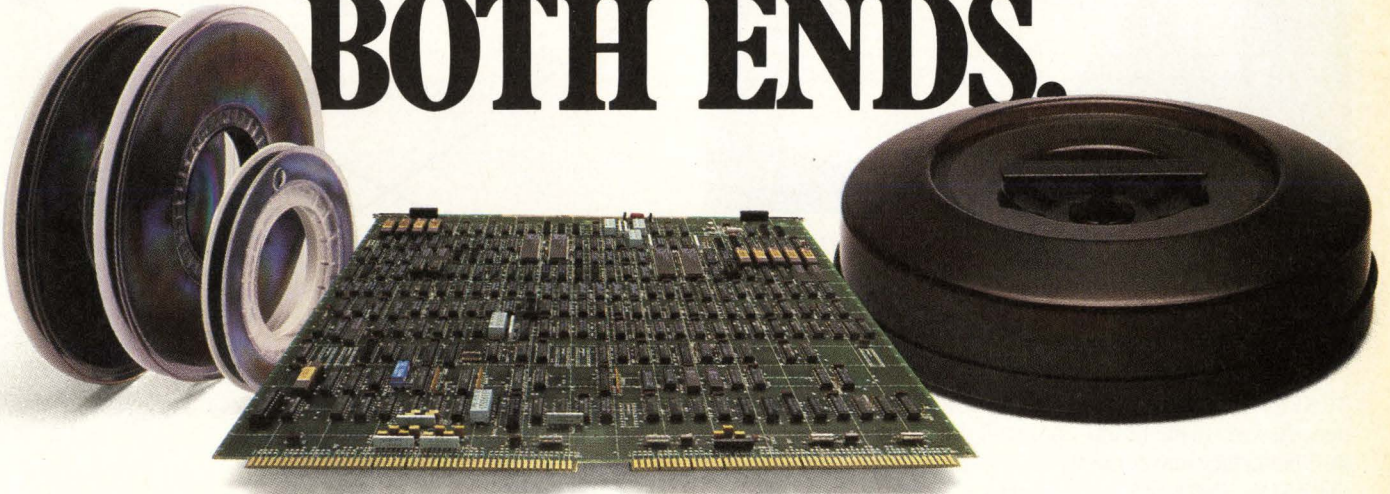


Figure 3: The command/response ring.



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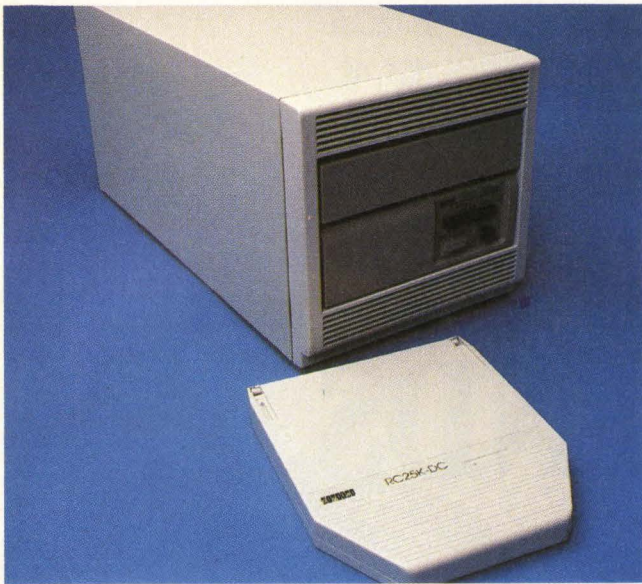
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The RC25 is DEC's fixed/removable drive that supports the MSCP protocols.



The RA81 disk subsystem from DEC. Shown in the background is a VAX 11/780.

SCSI bus, and as far as the DEC CPU is concerned, the SCSI doesn't exist. In the future, companies like this may abandon the SCSI interface and come right out of the edge of the board with the ESDI, SMD or ST-506 interface.

Tape controllers conforming to the MSCP will emerge next year, although once again because of a lack of available documentation, their design has been difficult up to now. The trend towards placing large disk subsystems onto microcomputers has been an evident market direction over the past few months. At the NCC, for example, both Priam and Interphase announced products for the Apple and IBM PC, respectively (*Digital Design*, September, 1984). This could present DEC with a marketing headache. The problem is twofold. First, the cost of DEC disk drives, manufactured by the company in its Colorado plant, are higher than many standard drives offered to the OEM. Second, since DEC is primarily a system house, their sales emphasis has conventionally been in the systems area, and marketing large drives to microcomputer/supermicro users would require a change in marketing philosophy.

### Massbus Support

Though DEC continues to support the Unibus and Q-bus for its disk and tape controller product line, DEC has dropped support for the Massbus, leaving many customers with no DEC upgrade path for Massbus subsystems. This has left a market wide open for third party vendors still building products for that bus. Some of these vendors claim performance levels greater than that of the Unibus/DSA from DEC; this is due to both Unibus contention from a number of devices and time penalties paid on disk access because of DEC's imbedded servo technique that requires an effective reseek each time a head is switched.

Undoubtedly, DEC is committed to the MSCP protocols. The MSCP type devices already introduced include the RQDX-1, the UDA50/RA60/RA80 and RA81 for the PDP-11 Unibus and VAX Unibus, the RC25 Fixed/Removable Disk, the TA78 GCR Tape Subsystem and the HSC50 high-end multidisk/VAX clus-

ter storage server. One can expect to see higher capacity and faster magnetic and optical disks soon.

### Conclusion

The most important feature of the DSA architecture is the universality of its MSCP protocols. MSCP supports all types of storage technologies including tape, disk and optical disk. MSCP protocols offload the majority of the hardware considerations onto the peripheral controller. The host software is thus free from the time consuming details of media organization, address mapping and correction of data errors. The host assumes the media to be error free and treats it as a contiguous set of logical blocks, allowing expansion to thousands of Gbytes of storage capacity. Lastly, MSCP protocols minimize the interrupt loading on the host. Whereas earlier generations of peripheral controllers interrupted the host after each command, an MSCP controller interrupts only on an exception condition. Communication between host and controller is accomplished via the more efficient polling and command stacking method.

### Acknowledgements

The author would like to thank the members of the engineering and marketing departments at the following companies for their help with this article: Data Management Labs, Emulex, Western Peripherals, MDB Systems, Qualogy (formerly Data Systems Design), Acceleron, Spectralogic, and Microtechnology; and Dataram for their description of the command/response ring. □

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# AI Makes The Transition From Theory To Practice

by Gregory MacNicol, West Coast Technical Editor



*Data General's Common Lisp programming environment. The graphic design appears on DG's GW/4000 engineering workstation.*

Once considered an obscure fringe of computer science, Artificial Intelligence (AI) is growing from academic research projects to advanced problem-solving methodology used to answer practical problems in the real world. AI is utilized in pattern recognition, robotics, speech recognition, simulation, and not surprisingly, in theoretical computer model building. Though some of the promising work is many years away from substantial rewards, some of the results are being witnessed now in small but effective ways.

## AI Comes Of Age

AI is suddenly attractive after receiving little attention outside of the computer science academic community. Some of the activity is being seen in the government, where over \$1 billion for AI R&D is being requested for DARPA; the NSF is requesting \$500 million over a three year period; and a growing number of federal agencies and the military, particularly the Air Force and the Navy are exploring the possibilities of AI. Venture capitalists are supporting the development of AI companies, saying there have

been no commercial AI failures yet. Computer scientists, too, are now seeing the commercial and ongoing potential of AI application and are forming companies whose sole objective is the commercial development of AI products and services. One potential reason why the attention is so great is because AI represents the computation of concepts and ideas not just numbers and words.

The primary underlying purpose of AI is to make computing machines smarter. As the demands for greater intelligence and functionality on computers increase, new models, programming methods, and ways of thinking need to change to meet these needs. As a secondary goal of AI, understanding the principle and processes of intelligence is sought. These models may then be incorporated into not just smart machines but more useful machines to aid in complex decision-making. Problems that have ambiguous values and weighted qualities require experts to decipher proper actions. In order to mimic an expert in the decision-making process, the structure of the logic, relationships to the values and the ability to compound information are key ingredients. In essence, a computer using AI should not be told what to do, but what to know.

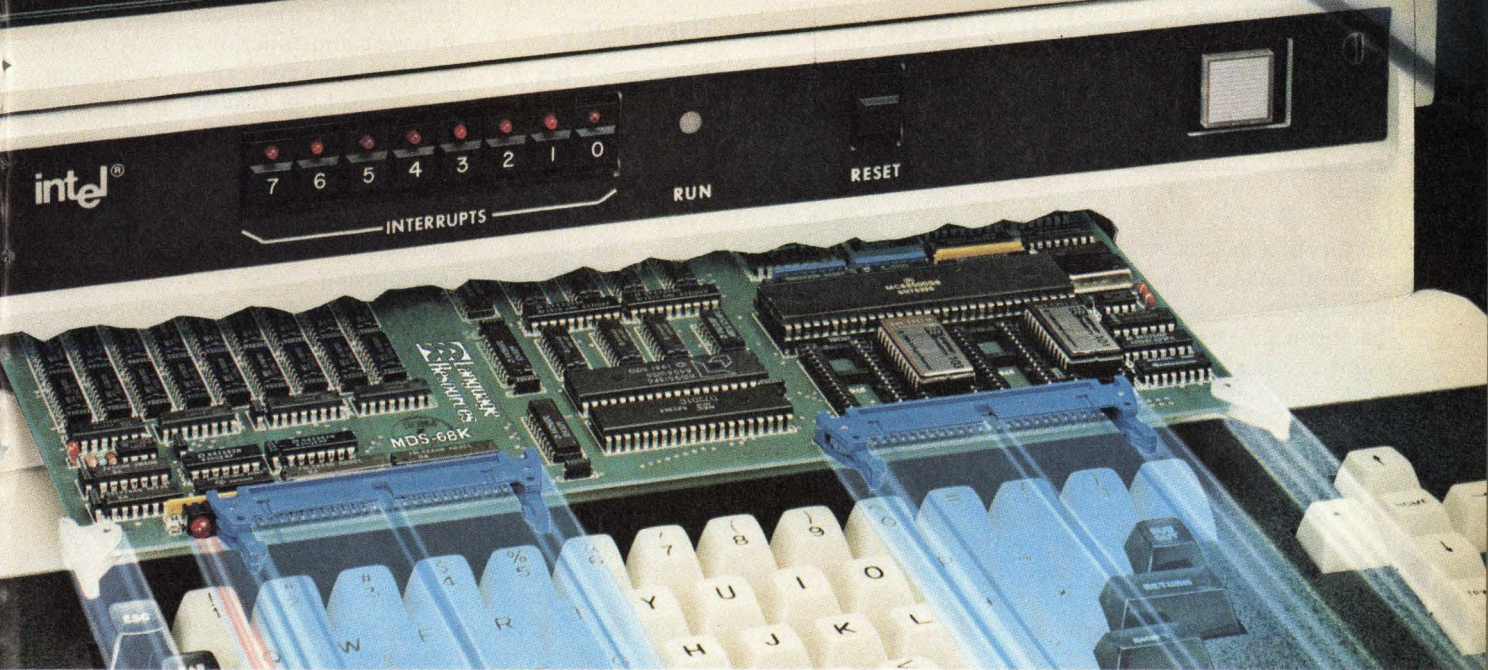
While some computer scientists contend there is no such thing as "artificial intelligence," there are clearly some unique qualities to AI programming. A highly useful function is the ability for the program to learn. During the 1960s a chess program was written to play itself. While



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*It should be no surprise that the present popularity of AI, which depends on a very large database that requires mass memory, coincides with the dropping cost of memory.*

that function was not very unique, it had the ability to "teach" the other side how it won, thereby successfully increasing its "intelligence." Presently, many AI programs are designed to self-organize, create analogies and search a large database while modifying and expanding the original database. A key element in the newer AI programs is the ability to create inferences in its database. It should be no surprise that the present popularity of AI, which depends on a very large database that requires mass memory, coincides with the dropping cost of memory.

### Lisp

The software requirements for AI are demanding and the result of ongoing research from the 1920s by mathematicians such as Kurt Godel. The earliest AI language was IPL (Information Processing Language) from the 1950s and was replaced by an elegant algebraic list processing language called Lisp. It was developed by John McCarthy at MIT and quickly attracted many followers. Since then, many dialects sharing the original kernel have been developed and can be executed on several computers.

Lisp is only one of the more popular languages becoming known as symbolic computing. Symbolic computing tries to simulate human intelligence allowing creative representation of data structures and their relationship and association to derive human-like intelligence. Whereas traditional computers automate operations such as sequential, repetitive, and logical calculations, symbolic processing tries to automate mental operations that assimilate large amounts of data, arranging it into abstract categories and exploiting the information from the data into useful forms.

The new methodology requires new programming techniques and terms such as object-oriented, rule-based, logic-

based, and active variables. The data is also represented differently, such as knowledge-based or dynamic-relation lists. Algorithmic structure is also different requiring search methods and inferring. One of the truly unique qualities of structured computing is the use of embedded languages where domain specific languages are developed and integrated into the programming solution. These new languages are sometimes referred to as the fifth generation languages.

The evolution of AI has produced many languages, some that are dialects of others. Clearly the most popular is Lisp, and many companies have dedicated

themselves entirely on this language. Two companies, Symbolics (Cambridge, MA) and Lisp Machines (Los Angeles, CA), offer dedicated hardware for Lisp. Lisp, which is the second oldest programming language, has never been standardized and as a result has been growing in power and functionality. Already several versions coexist such as Common Lisp, Franz Lisp, Zetalisp, Maclisp and Interlisp.

The evolution of Lisp's dialects have generated many useful features such as a total Lisp environment for editing, windowing, and support tools. Of the three most popular Lisps, Zetalisp, runs on Lisp machines currently manufactured by Symbolics and LMI, Interlisp runs on Xerox (Pasedena, CA) products such as the Dolphin and Dandalion, and Common Lisp runs on several machines. Today, Lisp is supported as a commercial product by companies such as DEC (Maynard, MA), Xerox, Honeywell, Symbolics and Lisp Machines Inc. (LMI).

Common Lisp, which was developed jointly by DEC, TI, Carnegie-Mellon, Lawrence Livermore Laboratory, and MIT, and a number of universities and AI companies, is emerging as an industry



*The standard Tektronix 4404 Artificial Intelligence System features a monochrome bit-mapped display; keyboard; mouse; 32-bit microprocessor with virtual memory management; hardware floating point; 1 Mbyte RAM; and a 20-Mbyte hard disk with a single 5 1/4" floppy disk.*





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standard. In addition, it is blessed by a major figure in AI, Patrick Winston, author of *Artificial Intelligence* (Addison-Wesley). The source code, which is public domain, runs on systems ranging from a VAX, PERQ, Data General (Westboro, MA) to an IBM PC.

In spite of Common Lisp's support, there are criticisms. Some believe that the floating point arithmetic in addition to generalized arithmetic operation was poorly defined, and that any compiler would be slow, require copious declarations, or require specially micro-coded machines on which to run. Arrays, too, are a problem because they are very complex. The same critics of Common Lisp believe the original goal of transportability may be lost.

Lisp programs consist of a group of functions, in contrast to conventional languages, which consist of sequential instructions and attendant subroutines. It is modular and recursive, allowing a function to call itself. The advantage of the Lisp list structure is that a single sublist, if appearing elsewhere in other lists, can be represented in memory only once using a pointer. Moreover, the elements of a list needn't be adjacent to each other, providing efficient memory space. If changes occur, only the pointer changes, which is different from Fortran where the list is moved up or down during changes.

Lisp can be interpreted or compiled. In the interpreted mode, Lisp functions and data have the same structure; therefore, functions can manipulate or even create other functions. The interpreter is always around, even when executing compiled Lisp code. Memory, which is critical in AI, is handled dynamically, in addition to "automatic garbage collection" which is essential. Some of the smaller versions of Lisp have differences in interpreted versus compiled operation, so it is important to determine the version's characteristics beforehand.

Lisp's syntax is simple and uniform which is one of the reasons for its popularity. Parsing is easy and since Lisp expressions are represented by Lisp data structures, an expression is its own parse tree. Syntactic distinctions between built in and user written functions do not exist. With Pascal, in contrast, you can make up new procedures but not new statement types. Lisp is very extensible and transparent, a user wouldn't be able to tell whether a given function is primitive or an extension. A major reason why pro-



Gold Hill Computers' Golden Common Lisp displayed on an IBM PC.

grammers appreciate Lisp is its rapid prototyping. Developing programs under the Lisp environment and language is fast and logical.

### Prolog

Another major contender in AI languages is Prolog. More popular in Europe and Japan's fifth generation language of choice, Prolog has many features built from Lisp. Prolog, which is a "logic programming" language, is based on a subset of first order logic called Horn Clauses. Logic programming languages such as Prolog are both procedural and declarative. As a declarative language, it allows the programmer to state what the problem is rather than how it should be solved. This means logic programming allows active systems analysis before system specification.

As a procedural language, Prolog provides a high level language, rapid prototyping, and fast execution. It provides a form of pattern matching called unification and a rule of inference called resolution which facilitates writing theorem proving program and deductive inference systems. It has been used to implement inductive reasoning with database using natural language.

It turns out that first order logic is inadequate for handling imprecise or uncertain information. Efforts to resolve the representation of imprecise information has led to formalisms called "fuzzy sets" and "possibility theory." "Fuzzy logic," as it is called, deals with the measures of confidence we have in a set of facts. The importance of fuzzy reasoning is that natural language, an important realm of AI, is a sophisticated representation of imprecise or uncertain information. Extending a database system to let it represent fuzzy reasoning may easily lead to inconsistencies and problems in data manipulation. As a result, fuzzy reasoning is a major research frontier.

A major reason for using Prolog is the ease in which you can connect a database to the language. A logic language like Prolog accommodates the inclusion of knowledge within a program. In addition, writing a compiler is much faster.

In spite of the high interest in Prolog, there are criticisms leading to its abandonment by many AI experts. Some refer to it as a "dead end," contending that no major AI programs have ever been written in Prolog. In addition, Prolog suffers from too much "backtracking." The Japanese, too, state they have no commitment





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to Prolog and envision use of logic programming but not in the Prolog language.

### Programming Alternatives

As AI develops, many more languages and tools are being developed, resurrected, and enhanced. Some of these are Loglisp, VAL, Q, OPSS, KEE, and Q'NAIL. But does it really matter what languages are used to implement AI? Seemingly not. At closer inspection, it is more important to match a user's or programmer's specification first and then consider the alternatives.

A non-AI language, however, has problems in the AI world. C, for example, has difficulty "binding" between program operations and the types of objects on which they operate. In existing languages that use "static" binding the programmer is required to explicitly write different functions for each kind of output and make sure that the operand type matches the function appropriate to it. Object oriented programming, in contrast, makes use of "dynamic" binding which is not specified until run-time. An example of implementing this concept is Smalltalk-80 from Xerox Palo Alto Research Center. A remarkable and enjoyable language, Smalltalk-80 makes an object out of everything which unfortunately makes it large and slow.

### Expert Systems

One of the off-shoots of AI getting much attention is expert systems. Expert systems are programs that use AI techniques such as rules of inference for problem solving in narrowly focused subjects. The system derives its expertise by consulting lists of facts, rules of thumb and observations gleaned from questioning human experts. Further, the person who translates expertise into a program is called a knowledge engineer.

There have been some excellent programs created to illustrate the power of expert systems. One of the more famous, MYCIN, was developed at Stanford's Heuristic Programming Project to help physicians analyze certain kinds of bacterial infections. Later, its inference engine was extracted as the basis of Puff, a pulmonary disease expert, and SACON, a structured engineering expert. Another expert system, CADUCEUS, is used for internal medicine. Electronic circuit analysis through EL, an expert system, uses human-like reasoning rather than brute-force on network equations in

terms human engineers can understand. Expert systems are rapidly gaining popularity in the oil and geological industry such as PROSPECTOR which helps in locating molybdenum.

Expert systems are based on four major attributes: knowledge representation such as how to describe a problem and how to store knowledge in the computer, inference methods, explanation to the user, and natural language. Expert systems demonstrate high performance in specialized areas (domains) and emphasize knowledge processing such as public knowledge as in textbooks and private knowledge from personal experience. Many of the goals and qualifications in expert systems are:

- separation of search mechanism from data and knowledge
- capability to deal with non-numeric data
- ability to deal with uncertain or incomplete data
- use of natural language with the user
- capability of the system to explain how conclusions were reached.

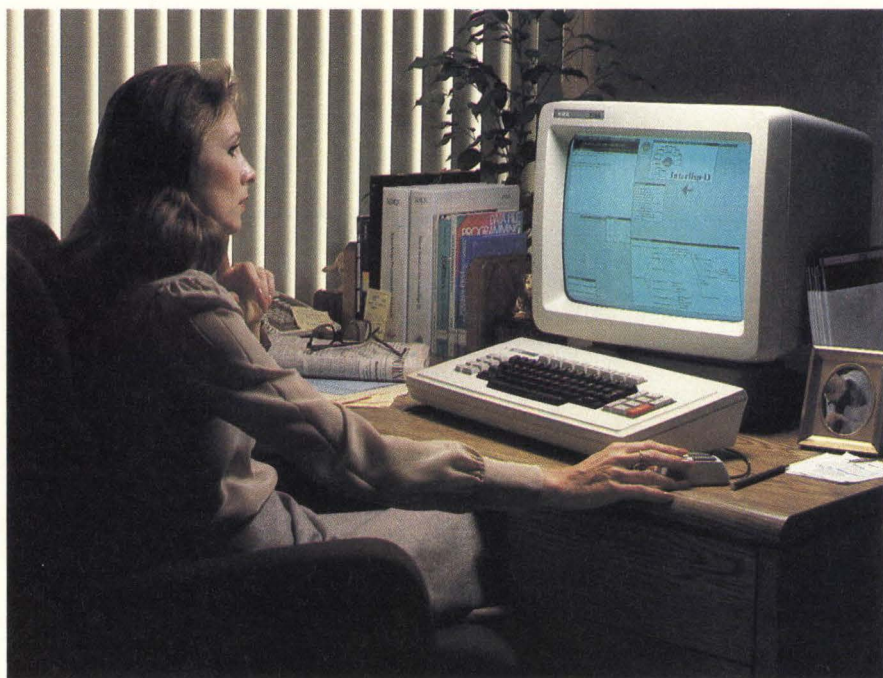
The last qualification is important and can be the deciding factor whether or not a program is an expert system. During a questioning session a user might be told a fact or question. A legitimate expert system can be asked "Why?" and a com-

plete explanation of the question and logical process of thinking represented. Some so-called expert systems cannot do this and are considered by many AI engineers to be non-valid.

Expert systems consist of two parts: a knowledge base and an inference engine. The knowledge base contains all the related facts, associations, relationships, procedures, strategies and analogies of the domain. Although more is better, the hardware limitations can determine the capability of an expert system. Recently many expert systems are appearing on the market that run on PCs, but many AI specialists feel these are poor representations of expert systems due to their small memory size and thus poor ability to store knowledge.

The inference engine manipulates the knowledge in the knowledge base in order to solve the problem being asked. The inference engine is based on logical relationships and is the reason why there are many software packages and languages being sold to develop expert systems.

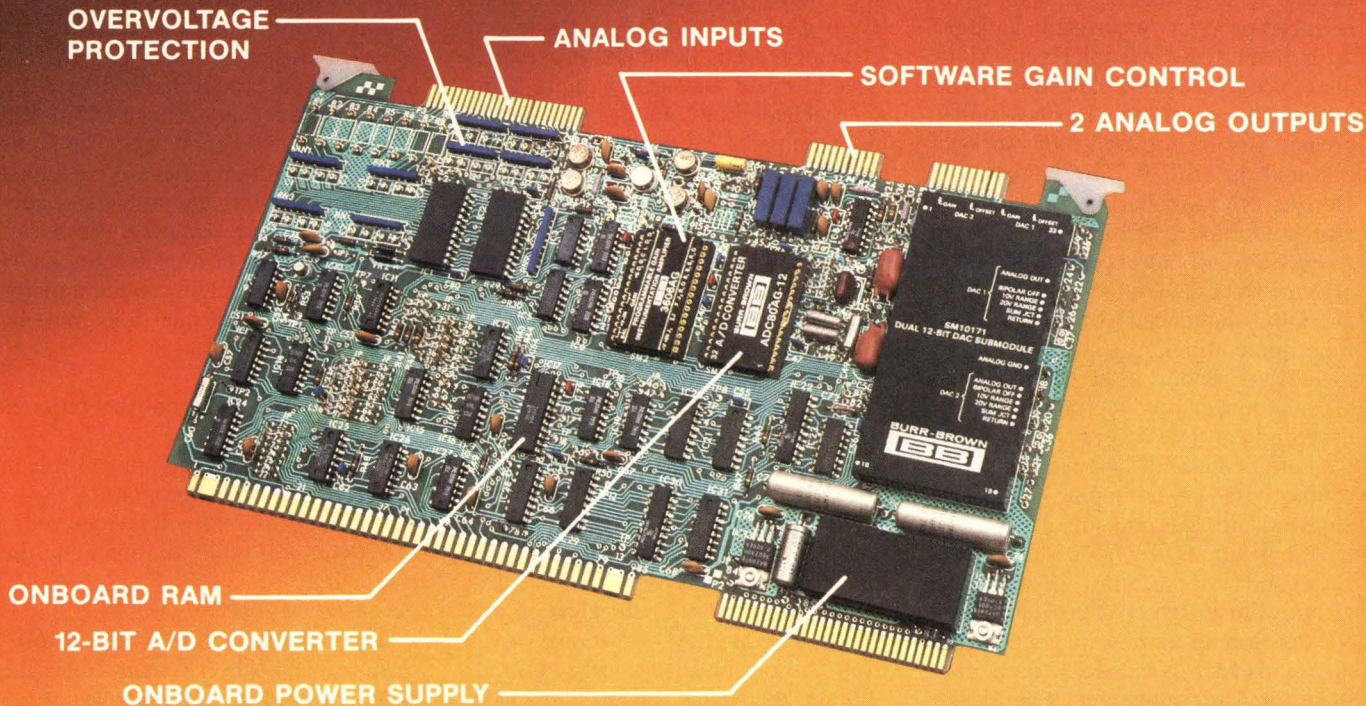
Naturally, due to architecture specifically designed for AI, the major AI companies such as Symbolics and LMI provide excellent tools for creating expert systems. Symbolics, which manufactures a powerful Lisp machine, offers over nine expert system tools developed by third party vendors, in addition to programs for training, simulation diagnostics, and



Xerox offers AI capabilities by providing the language Interlisp.



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natural language. LMI also offers a software environment on their Lisp machine for developing expert systems.

**AI In The Marketplace**

During the last American Association of Artificial Intelligence Conference (AAAI) in August, several larger companies announced products specifically aimed at AI and expert system development. Xerox announced it has established an Artificial Intelligence System Business unit to create software for their 1108 workstation and the IBM PC. IBM (Yorktown Heights, NY) announced their version of Lisp in addition to PRISM (Prototype Inference System), an expert development system. Data General (Westboro, MA) and DEC announced Common Lisp for their minicomputers.

Software vendors in the AI community also announced products targeted for AI development. IntelliCorp (Menlo Park, CA) offers the KEE language and environment used for developing knowledge-based systems for commercial and industrial applications. It runs on Xerox, Symbolics and LMI machines. The Carnegie Group (Pittsburgh, PA) provides a tool for developing natural language interfaces call PLUME and SRLT, an environment for AI development. Rule Master by Radian (Austin, TX) is an expert system development tool that is easy to use and runs on UNIX, providing transportability. The Rule Master builds rules by a process called rule induction where rules are induced by generalization over examples of expert decision making.

A powerful and versatile AI system has also been developed by Tektronix (Wilsonville, OR). The 4404, priced below \$15,000 comes with Smalltalk-80, and Lisp, Franz Lisp, and Prolog languages as options. Smalltalk, although not known as a language, has features that support integrated exploratory and development with an excellent user interface that is highly visual.

A major problem with the use of AI machines is that programs require use of complete workstations, which are presently expensive. Seeking a greater market are several software companies making AI products for PC-based systems.

Teknowledge (Palo Alto, CA) offers MI, a knowledge engineering tool for the IBM PC. It is used to design, build, and run stand-alone knowledge systems using English-like language. Texas Instruments

(Dallas, TX) has also entered the AI fray with its Personal Consultant, an expert development tool. Running on the TI professional computer under MS-DOS 2.1, it represents knowledge in the form of if/then rules using a similar rule structure to MYCIN. Backward and forward chaining control mechanisms are separate from domain knowledge. Backward chaining reduces the number of questions asked, while forward chaining helps restrict irrelevant solutions. In addition, user defined Lisp functions using IQ-Lisp provide an escape mechanism to add non-standard features. TI which is actively involved with AI recently received \$6 billion from the Navy to develop a compact Lisp machine based on 1.25 micron geometry VLSI. A new version of Expert-ease from Perrone and Associates (San Francisco, CA) also runs on the IBM PC and, relying primarily on a decision tree, is intended for business applications such as make or buy decisions.

Common Lisp is becoming a standard with quality endorsements and is available for the PC from Gold Hill Computers (Cambridge, MA). Gold Hill also provides excellent documentation and can be used as an AI educational tool as well. Prolog is available on the PC in addition to the Apple, Kaypro, TRS-2000, and the DEC rainbow. It is sold through Programing Logic Systems (Milford, CT) who also provides a primer that makes the package useful for teaching Prolog. There are many critics of the use of AI on the PC. The primary problem is memory space. Architecture, too, which is not intended for AI, makes execution of the programs very slow. The biggest problem is that some programs that are called AI are really mathematical matching or name association programs.

**Conclusion**

Interest in AI is increasing at a remarkable rate. As a result, soon there will be a growing number of tools, languages and methods that will be provided by several new start ups dedicated to AI. In addition, there will be a comparable amount of confusion and poorly conceived products all targeted at the same market. This requires users to clearly scrutinize and evaluate the target problems to be solved, and the capabilities and limitations of an AI program to solve them. In an era where buzz words of AI are very popular it is more important than ever to deter-

mine what is legitimate versus what is merely in vogue.

A major problem hindering AI research is the lack of qualified people. An expert may not be fully aware of how decisions are made and require a knowledge engineer who knows psychology and a great deal of knowledge encoding expertise. It requires intuition, heuristic reasoning, and aspects of knowledge that are hard to define. In addition, few books are truly up to date enough to be very useful to prospective AI engineers. The problem of a lack of qualified AI personnel also translates into the problem of adequately judging a program's effectiveness.

When planning on implementing an AI program, which might require a major investment, several questions must be raised to begin evaluation:

- Which task is the one that requires AI?
- What will be the computer's role in implementing the AI program?
- What resources will be required?
- Who will build and maintain the program?

Some users measure an expert program's capability by how many "rules" the system can analyze where 40 rules are being seen on PCs and over 400 are being seen on mainframes. Others like to measure speed in decisions or rules per second. But ultimately, the clearer the task is defined, the better functionality and effectiveness can be determined.

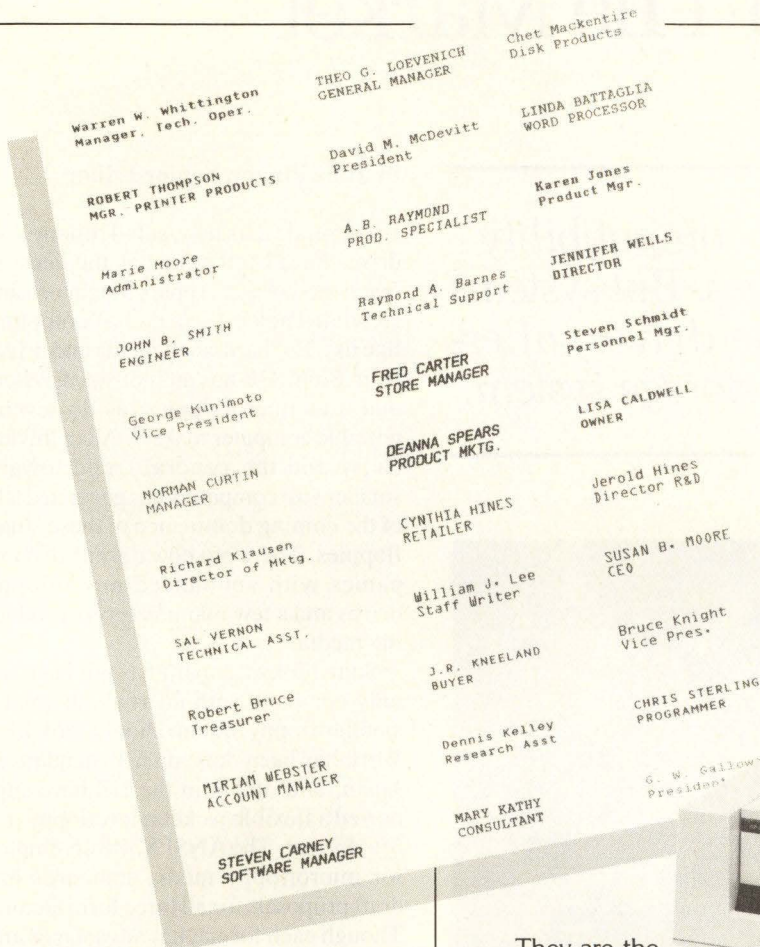
The results of research on AI have not even begun to surface. Companies like Schlumberger-Doll (Ridgefield, CT), whose interest in applying AI to geological research, and General Motors (Kokomo, IN), whose practical problem solving in manufacturing, are doing research that is beyond theoretical science. Computer companies, such as Apple, are actively researching AI and have hired some of the top Smalltalk people from Xerox PARC. Clearly, the work in AI is just beginning. The most impressive results are still yet to blossom. □

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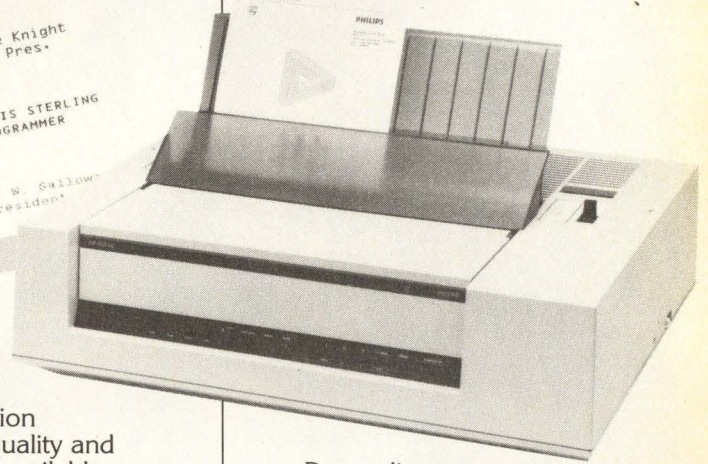
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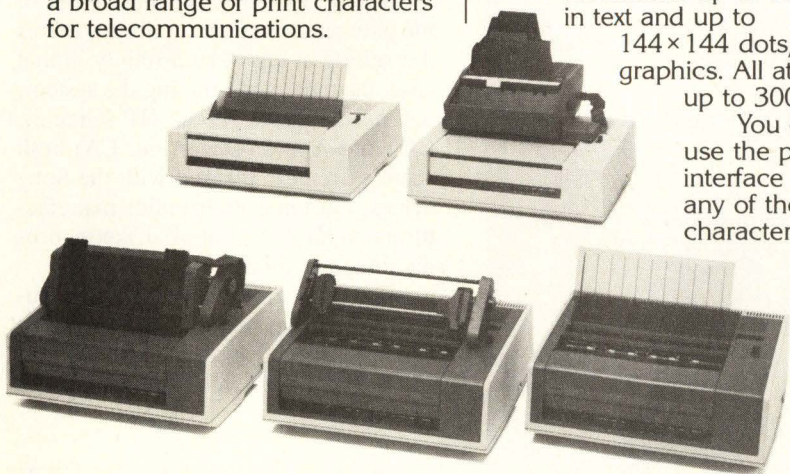
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# Microflops Squeeze Their Way Into The Market

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*Microflops now offer 5 1/4" compatibility as well as technical advantages. But systems must be designed with these drives; after-market will not carry a new storage system.*

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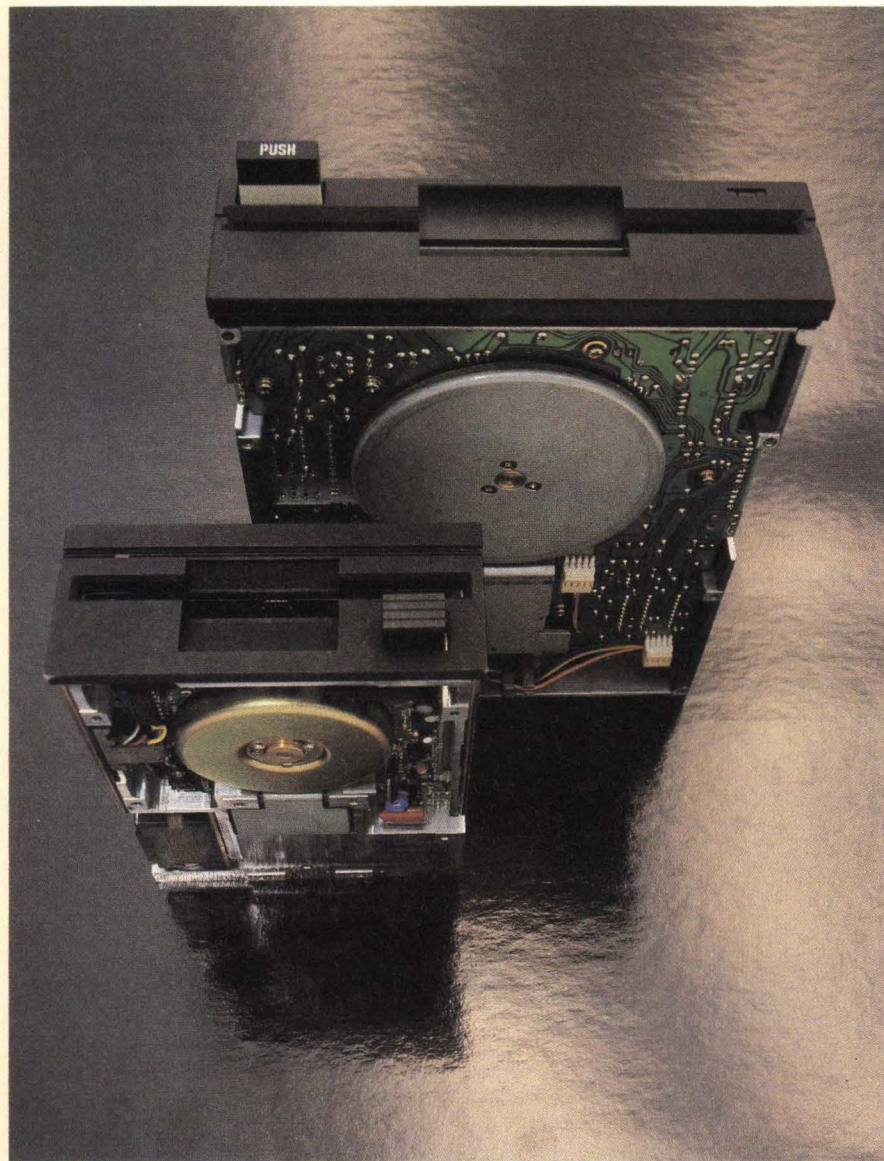
by Julie Pingry, Senior Editor

For several years now, sub-4" floppy disk drives have been touted as the latest in magnetic storage. Apple's Macintosh and Hewlett-Packard's personal computer line use 3 1/2" hard-shell media and drives from Sony. GE has an industrial system that uses microflops, as do several portable computer makers. All of this activity and the general trend toward smaller size computers has generated talk of the coming dominance of these small floppies. There are now dozens of companies with announced microflop drives and a few manufacturers producing media.

Sony (Tokyo, Japan) has not been the only company with ideas about what a smaller floppy system should look like. Work has been done on a 3" standard in Japan, and others in the US have supported a flexible jacket microflop in a 3 1/4" format. The ANSI X3B8 committee for microflop media standards has draft proposals for all three form factors. Though each format has advantages and supporters, makers of 3" and 3 1/4" drives (with the exception of Hitachi, originator of the 3") have now all announced 3 1/2" drives, as well. Market demands have been the basis for de facto standards and products for all disk sizes.

So the leading question is: where is the market for downsize floppies? To date, the popularity of the Macintosh is one of the only reasons that microflop drives are selling at all. And certainly in that case, customers are buying the system, and not the drive per se. HP (Greeley, CO) and Apple (Cupertino, CA) both seem extremely pleased with the Sony drives, but until other major manufacturers commit to a sub-4" diskette, production may not pay off.

Many of the microflop drive manufacturers suggest that this fall will bring announcements that could make the market fly. And portable/laptop computers



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*Floppy drives in micro and mini form factors from Epson.*



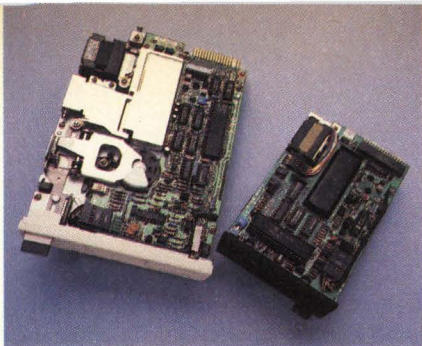


Figure 2: Epson's 3 1/2" drive next to their 5 1/4" shows the space savings.

are not the only type of system that may use microflops; in designing compatible lines of computers, new systems from desktop to workstations and instrumentation may use the same smaller disk drives.

There are advantages to microflops other than small size. Power consumption of drives is dramatically (at least half) less: this allows their use in battery-powered transportable computers. Carrying a computer also requires the light weight of a smaller drive. Size and power reductions should permit cost decreases. Though initial disk and drive products in the microflop form factors do not present price savings, smaller power supplies, less material and quantity LSI circuitry should eventually allow their smaller size to be matched by lower price.

Nevertheless, microflops must provide specific benefits to win over the established 5 1/4" products. In the final analysis, the end-user considerations around which microflops were conceived must be what users truly want.

### End-User Floppies

Some of the initial applications for microflops may be in home and small business computers. The small size is not only an advantage for carrying, but lessens the effects of temperature and humidity. Reliability and costs are always critical in low-end markets, and small disks and drives offer those potentials. The 3 1/2" and 3" hard shells also provide ease of handling and protection from dust and fingers; their automatic shutters complete the seal.

Unlike most other products, 3 1/2" floppies have developed through the planning of a group of media, drive and system manufacturers. Work by the Microflop Industry Committee (MIC), formed in May 1982, led to early ANSI work on a 3 1/2" medium similar to Sony's. They considered other sizes briefly, and decided the 3 1/2" hard shell already in use could meet their criteria.

	Unit	Fuji Film 3 1/2" Micro Floppy Disk MF1D, MF1DD, MF2D, MF2DD	Fuji Film 5 1/4" Floppy Disk MD2D
Dimensions Disk Diameter Outer Dimensions	mm mm	86 94x90x3.3	130.2 133.35x133.35
Recording Capacity (MFM, unformatted)	bytes	250K (MF1D) 500K (MF1DD) 500K (MF2D) 1000K (MF2DD)	250K (single-sided) 500K (double-sided)
Recording Density (MFM)	BPI	8.717 (side 1)	5.876 (side 1)
Data Transfer Rate (MFM 300 RPM)	Bits/ Sec.	250K	250K
Track Density	TPI	135 (80 tracks) 67.5 (40 tracks)	48
Number of Tracks/ Side	Tracks	80 (MF1DD, MF2DD) 40 (MF1D, MF2D)	40
Operating Conditions Temperature Humidity	°C %RH	10-60 8-80	4-52 8-80

Figure 1: Comparison of the specifications for Fuji's 3 1/2" and 5 1/4" floppy disks shows compatibility, greater capacity.

Stated goals for the new disk were: the disk should fit into a shirt pocket; be plug-compatible with 5 1/4" floppies for using existing software and controllers; have a hard covering for protection; and be proven reliable before introduction. Sony agreed to slight specification changes, and the group took a proposal to ANSI.

Draft standards for 3 1/4", 3" and 3 1/2" disks have all been drawn up. The 3 1/2" media standard is furthest along by about six months, according to X3B8 Committee Chairman Jim Barnes of Control Data. But he hastens to add that ANSI committees and standards do not perform companies' product planning. ANSI standards are only now being finalized for 5 1/4" floppy disks, a true commodity item.

Copies of the latest ANSI X3B8 committee draft proposals are available from CBEMA, 311 1st Street, N.W., Suite 500, Washington, DC 20001. The document codes are: 3 1/2"—X3B8/84-136; 3 1/4"—X3B8/84-138; 3"—X3B4/84-140. Also in the works, but about a year behind media specifications, are subsets for formatted media. Even 5 1/4" and 8" floppies do not have standards for recorded format.

Though all of the formats offer some advantages, the 3 1/2" has market mo-

mentum. Other microflops may find applications, but they will not likely match that acceptance. At one point, IBM had their own 3.9" microflop, but soon dropped it in the face of growing acceptance of 3 1/2". One reason for choosing the 3 1/2" initially was the hard jacket. The protection it affords may permit density increases not feasible with exposed media, and the inside shutter on the 3" was seen as a problem for reliability and wear.

Dysan (Santa Clara, CA) and Tabor (Westford, MA), the major proponents of 3 1/4" soft-jacketed disks, point out that the hard shell will be more expensive to make. And even the 3 1/2" media suppliers admit that it is a different process than other floppies, with seven added parts needing assembly. The low costs and simplicity of the flexible jacket with proven technologies are the advantages of 3 1/4". Seikosha (Tokyo, Japan) introduced single and double sided 3 1/4" drives to the US OEM market at NCC.

Sequa (Odenton, MD) uses 3 1/4" soft-jacket disks and drives in their Chameleon portable, but that system has only been shipped since this past summer, so demand for disks is not enough to make production profitable for other magnetic manufacturers. Xetec (Salina,



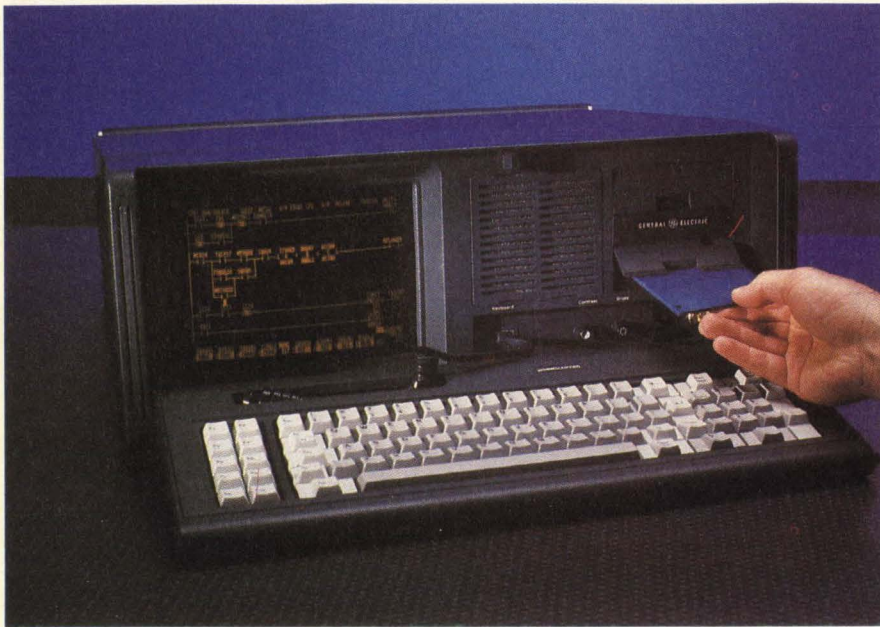


Figure 3: Environmental considerations led GE to choose 3 1/2" diskettes for their Workmaster industrial system.

KS) also uses these microfloppies for an add-on drive subsystem for the PCjr. Still, 3 1/4" drive manufacturer Tabor has now announced drives for 3 1/2" hard-shell disks, as well.

One advantage Dysan created for their format is software availability. The Sequa computer comes bundled with five packages, and Dysan now offers about 37 titles. Other than Macintosh software, which is specific to that computer, not much software has been published on 3 1/2" disks. Since most new systems record the same amount per side as a 5 1/4", transferring software should not be a major undertaking.

Putting 80 tracks on a side that is 3 1/2" in diameter makes these dense disks, at 135 tpi, compared to 98 tpi on an 80-track 5 1/4". That is not a technical problem for current heads or media, but the availability of heads is poor. It is widely held that those capacities would stretch technology on a 3" disk. With the right drive and heads, media makers suggest that the same 3 1/2" disks used for 1 Mbyte unformatted double sided now could hold 2 Mbytes.

### Micro Vs. Minifloppies

Sheer volume of 5 1/4" systems in use and disks with programs and data stored on them assures them a long life. Shugart (Sunnyvale, CA), now a producer of 3 1/2" drives, points out that they shipped more

full-height 8" floppy drives this year than ever before, though most new designs incorporate 5 1/4" drives. Similarly, 5 1/4" sales are expected to exceed those of micros for several years.

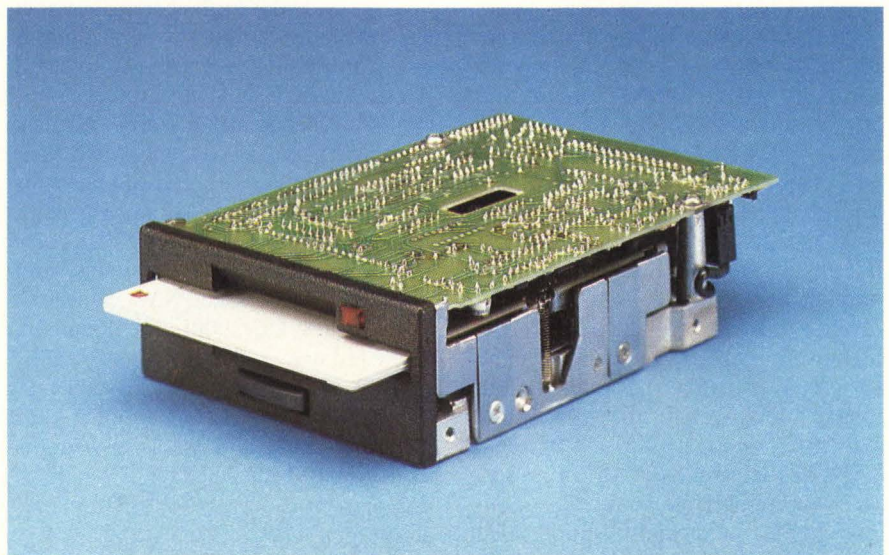
Besides size, several other parameters of microfloppies are a departure from 5 1/4". There is a difference in the source of 3 1/2" drives: the sub-4" drive manufacturers are primarily in Japan. That has advantages in reliability (John Boose of HP claims that they have four times better reliability for the 3 1/2" than for 5 1/4",

to date) but the accessibility and overseas base of drive manufacturers could be seen as a problem for US OEM integrators.

A smaller surface may suggest less storage capacity, but as Hewlett-Packard points out in their reasons for choosing the 3 1/2" medium, it has the potential for greater capacity than previous sizes. Factors contributing to that ability are the hard shell and hub, small area for expansion in heat or humidity and for stepper motors to cover and shutter protection of the head access area.

Floppy disks are really the first soft-shell magnetic media. Audio, video and storage tapes all come in hard plastic cassettes, so the hard case on 3 1/2" disks is not a great departure. The high bit density required to provide enough storage to make small disks useful means small magnetized areas. For accurate reading of these tiny domains, extra protection from dust is critical. But media suppliers must procure either the technology for injection molding the hard case or a dependable supplier.

The 600-650 Oer. media is no longer novel; but with its use for larger disks, microfloppies will be recorded at high track and bit densities. Some speculate that the capacity of 3 1/2" disks may limit their use to home and lower-end computers and that business systems will continue to store data on 5 1/4" sides. But comparisons by media makers such as Fuji (Tokyo, Japan) show that smaller does not mean less capacity (Figure 1). Most new drives tout equal recording per side to minifloppies, and double-sided drives



Shugart's 300/350 is one of the few 3 1/2" drives being manufactured in the US rather than Japan.



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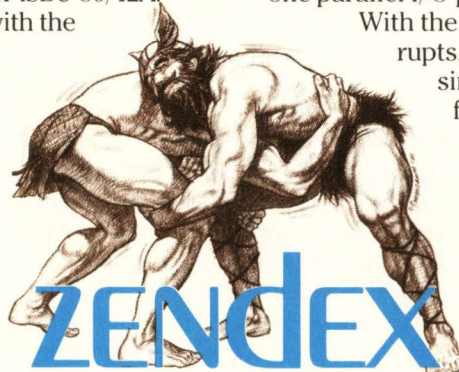
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The first systems announced to use microfloppies were Hewlett-Packard's Personal Computers; HP now offers a line of microfloppy drives that can also be used with IBM PCs.

and media have been shown.

Few double-sided drives have actually been integrated, however. Skeptics doubt that two-sided drives work well, but even if there have been initial problems, they will likely be ironed out soon. Some of the most popular microcomputer programs are integrated packages that need large spaces. Most applications will demand the 1 Mbyte of a double-sided 3½", and with 1.6 Mbyte and 3.3 Mbyte 5¼" disks, pressure to increase disk storage is on.

Availability of sophisticated software programs on 3½" disks will allow their entry into the business market. Software does drive hardware sales, and micro diskettes will be of little use without software transported to them.

Microfloppy drive maker Epson (Tokyo, Japan) says software will not be a problem, since they provide software transportation service from 5¼" to smaller disks. And since 3½" disks are mostly specified to hold 40 or 80 tracks on a side just like a 5¼" disk, the job is not difficult. Still, since most new drives will be sold integrated into systems, software support will be critical to making a new system attractive.

Integration of microfloppies should present no design problems. The current drives are designed for 'plug and play'

compatibility with 5¼". Transfer rates and interface are those of standard minifloppy drives. Shrinking the package has, in most cases, meant including more VLSI as well as disk size. But interface circuitry can be identical.

Right now, costs of 3½" systems and disks are considerably higher than those of 5¼". Drives generally retail for between \$500 and \$700, compared to \$250 for standard minifloppy drives. Media is also expensive; but as production ramps up and vendors slide down the learning curve, costs should be comparable or even less.

Reductions in costs for incoming test and maintenance could offset current price penalties, and make integration profitable even in the short term. Certain applications call for the other advantages of micros, as well.

### Where Microfloppies Fit

Transportable computers, the obvious systems that need small size and weight storage, have not dominated uses for microfloppies. Varying estimates on the size of the market for portable computers leave their short-term importance in question, as well. But microfloppies do have clear applications in these systems.

Naturally, size and weight are critical for carrying a system. But the more cru-

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## Stability of small floppies could allow capacity increases.

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cial factor is power consumption. Needing about half the power of a 5¼" drive, microfloppy drives can operate off batteries, for systems that not only can be carried, but can be used away from outlets. This hasn't really been used extensively; but as kneetop computers are improved and traveling computing becomes practical, the difference will be crucial.

Several new portable systems do not incorporate disk memory, and there is speculation by some forecasting companies that most portables will use solid state memory only. Some recent introductions suggest the truth of that, and indeed, PROM-resident software protects profit margins and eliminates piracy. Systems for specific, limited applications may be able to accommodate all of the memory needed in PROM. But studies of user desires show that removable storage is important.

Removable bubble memory is a possibility for portable solid-state memory. Industrial system integrators once held this as the ultimate panacea. But improvements in performance and price have not come about. For size and expandability, cartridge bubble cannot compete with small rotating memory. In addition, the technology is expected to remain expensive for some time. Since the small computer market is very much cost-driven, add-ons for diskless portables may be a market for microfloppy drives.

Portables are not the only place where integration will make sense. HP and Macintosh computers are desktop computers, but HP declared that the footprint of their computers was important. Although the space saving of a 3½" over a 5¼" (Figure 2) is not as significant as that of a 5¼" over an 8" drive, it has allowed the 'square foot' desktop computer space.

The stability of a small disk with a hard hub could be a factor in increasing capacity of floppy disks. The hard hub assures centering and improves reliability of the head-to-medium interface. 3½" soft-jacket disks also present a smaller surface to expand in heat or humidity and require smaller increments of the stepper motor to cover the surface.




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 CONTROL DATA





One media maker already producing 3 1/2" disks is BASF.

GE (Norwalk, CT) chose 3 1/2" micro-floppy storage for their Workmaster industrial system (Figure 3) mainly for environmental reasons. In dusty environments, both the open head access window and the lack of an outer covering are problems for standard floppies. In addition, the flexible jacket 'nearly exploded' during heat tests, according to a GE spokesman. They are enthusiastic about the 720 Kbytes of formatted storage possible on a double-sided, double-density disk, as compared to 380 Kbytes on a standard 5 1/4" disk.

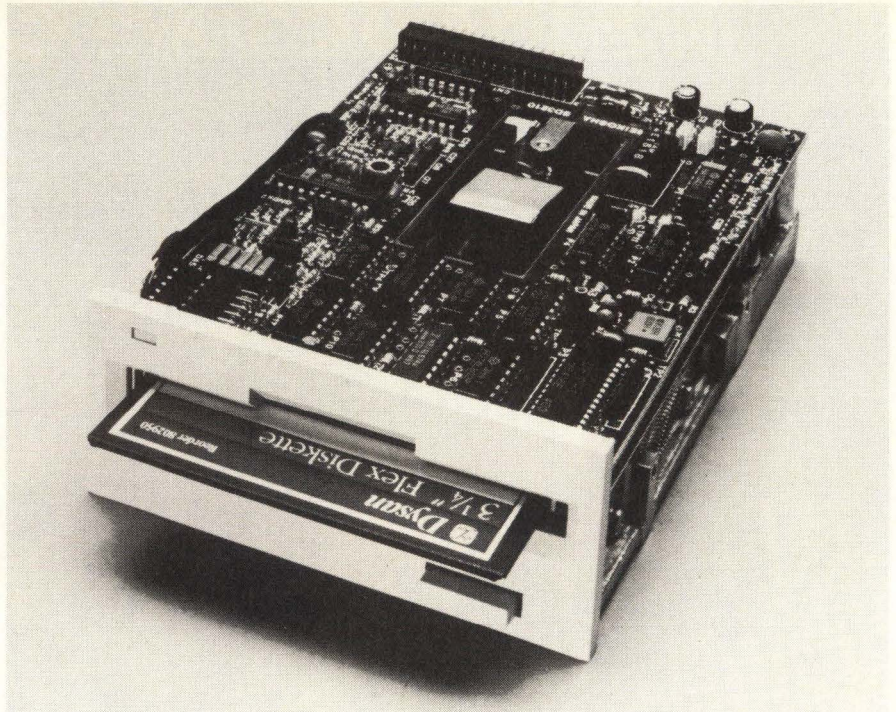
As networking becomes more common, floppy disks may be a less desirable means of file sharing. Communication systems will allow many computers access to the same mass storage system; for these applications, the capacities of Winchester will be needed. By using access codes, portions of the data stored for a network can be protected like a personal disk, while others are open to all, as a floppy that is passed around.

The importance of smaller hard disk systems may expand rather than reduce the market for microflopies, however. 3" and 3 1/2" Winchester disk drives with capacities from 20-30 Mbytes have been announced recently, and will need backup. The space savings that they present will need to be matched by micro backup storage. Though this may be tape, microflopies are a natural extension of disk backup for Winchester of the same form factor.

### New Floppies

Although only a handful of systems have integrated sub-4" floppy drives, there are indications that the design cycle may be near its end. Introductions of systems ranging from desktops to portables and instrumentation with these drives could be upon us.

And integration could well be the key to market success of small drives. Though



Seiksha's SD-3210 drive uses 3 1/4" soft-jacket disks at 1 Mbyte.

many microflopie disk drives have been introduced and shown over the last year, they have not been evident in products. According to both drive and media manufacturers, that is changing right now.

The few media manufacturers producing for HP and Macintosh drives claim that they cannot keep up with demand now. Production ramp-up on media and drives is predicted for 1985. Makers of 3 1/4" and 3" products also feel they will make sales next year.

The growth path for capacity of these disks is good. One of the criteria Hewlett-Packard set for the storage system on their personal computers was better capacity potential than previous sizes. Using different heads and drives, the disks' capacity could double, to 2 Mbytes for a double-sided unformatted disk. If an inexpensive closed-loop or servo system for drives is developed, another doubling in disk capacity would be feasible. But the cost-sensitivity of this micro market may not allow a drive that complex much penetration.

Microflopies are also a prime candidate for vertical recording; Vertimag (Minneapolis, MN), a pioneering company in that field, is reported to be working on just such a system. Common estimates are that a vertically recorded 3 1/2" disk could store 10-12 Mbytes, or a ten-

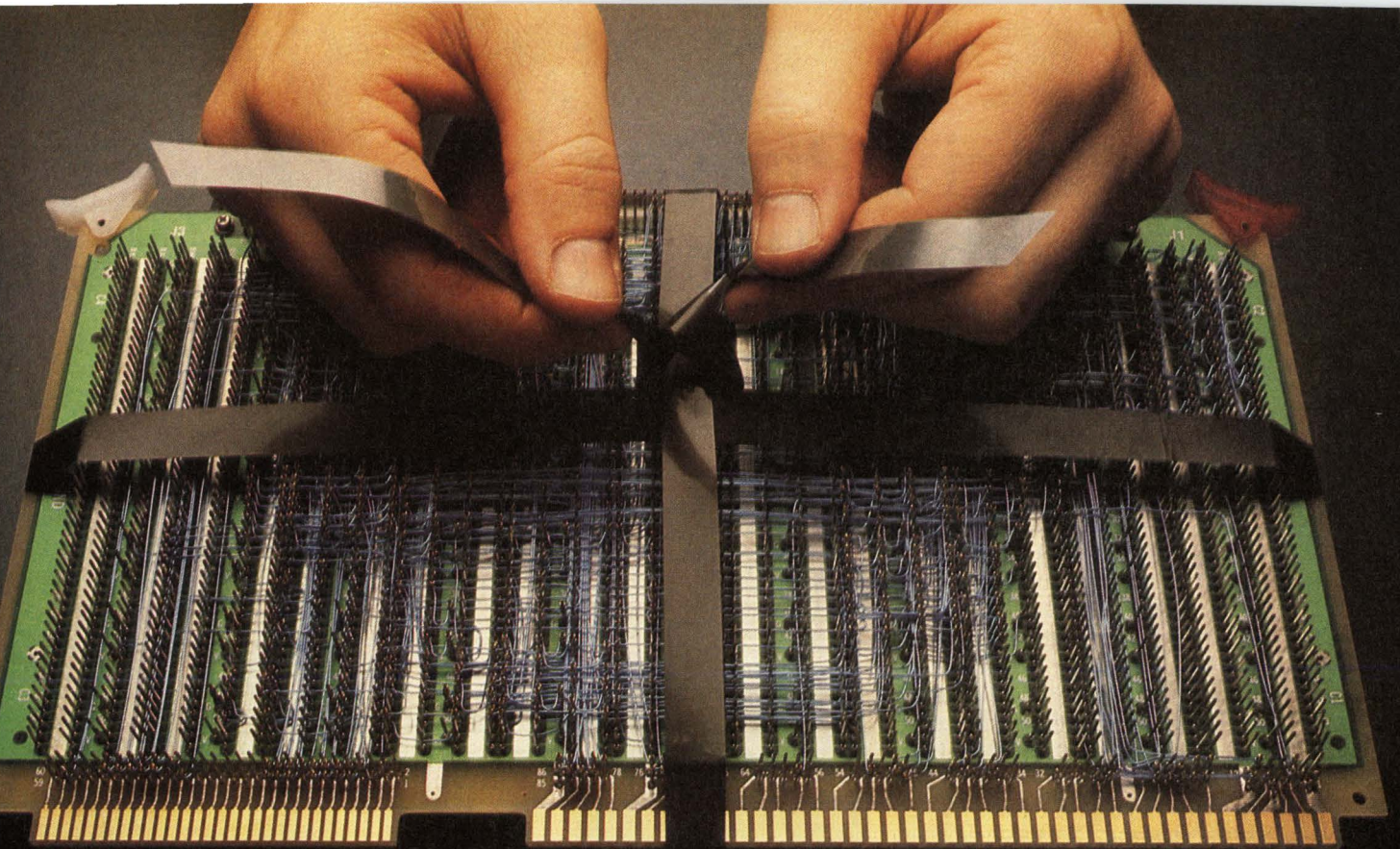
fold increase over current technologies. Another possibility for increasing capacity is 3M's SSR (stretch surface recording) hard rim/flexible media. Other major magnetic media manufacturers are working on their own schemes for increasing floppies' capacities.

Though standard miniflopies have great hold on the market now, the size, reliability and technical advantages could put 3 1/2" floppies in a good position to overtake them in the next few years. Potential capacities are greater due to the size and stability of the disks. When systems designed with microflopies become popular, costs should drop to compete with 5 1/4", too. At that same point, software will likely be produced on smaller disks, eliminating nearly all of the drawbacks of a new format. Though existing magnetic storage systems will continue strong, a few years from now, the low power, small size and high capacities of microflopies could push them into the market lead. □

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# Dot Matrix Printers Approach Letter Quality

by Andrea Coville, New Products Editor

Dot matrix printers have been regarded as fast, reasonably inexpensive impact devices suitable for draft mode printing tasks. With the implementation, however, of sophisticated electronics, ribbonless ink systems and printheads with high pin counts, dot matrix printers have emerged as intelligent devices for the high speed, color graphics and near letter quality (word processing) applications, making them the most popular computer hard-copy output devices.

When using cost and speed as parameters for evaluation, the dot matrix printer lies in the middle of the spectrum of printing technologies. Speed ranges of 80 to 320 characters per second (cps) and prices of \$250 to \$4,000 are typical. **Figures 1 and 2** show the relationship of both serial and line dot matrix printers to other impact and non-impact technologies.

**Figure 1** shows a comparison of serial printers, whose design is typified by a printhead that moves horizontally across the page and prints characters as it moves. Print speed is given in characters per second (cps), this typically being the maximum print rate over a single line of print, which includes both characters and blank spaces.

The non-impact technologies are ink jet, thermal and electrosensitive. As **Figure 1** shows, ink jet and electrosensitive are respectively, the fastest and the most expensive. The impact serial printers, ball, daisy wheel and impact wire matrix, vary in print speed from 10 to 600 cps. Ball printers, the least expensive, offer better quality printing at very low speeds (around 15 cps) due to the high inertia of the mechanism. Daisy wheels print characters approach the quality of ball printers but have the advantage of speed with models ranging from 30 to 50 cps. Wire matrix printers have high printing rates, 30 to 600 cps, graphics capability and a print quality that increases with matrix density. Unlike daisy wheels, dot matrix printers can change typeface in mid page,



The M-100L dot matrix printer from Dataproducts shows an example of output which mixes graphic, draft and near-letter quality printing.

but are unable to put ink anywhere on a line or page.

Like serial printers, line printers can be classified as impact and non-impact. Their design involves a number of activators which are arranged horizontally across a page and can be fired concurrently. Each line is printed after a complete line of data has been received from the host computer. Print speeds are designated at lines per minute (lpm) in

three subgroups: low, medium, and high.

**Figure 2** shows the relationship of various line technologies, with electrophotographic, electrostatic and ink jet representing the most expensive and fastest non-impact technologies. Lasers represent the most widely used means of putting images on paper, although they are being challenged by ink jet and thermal at speeds below 10 pages/min.

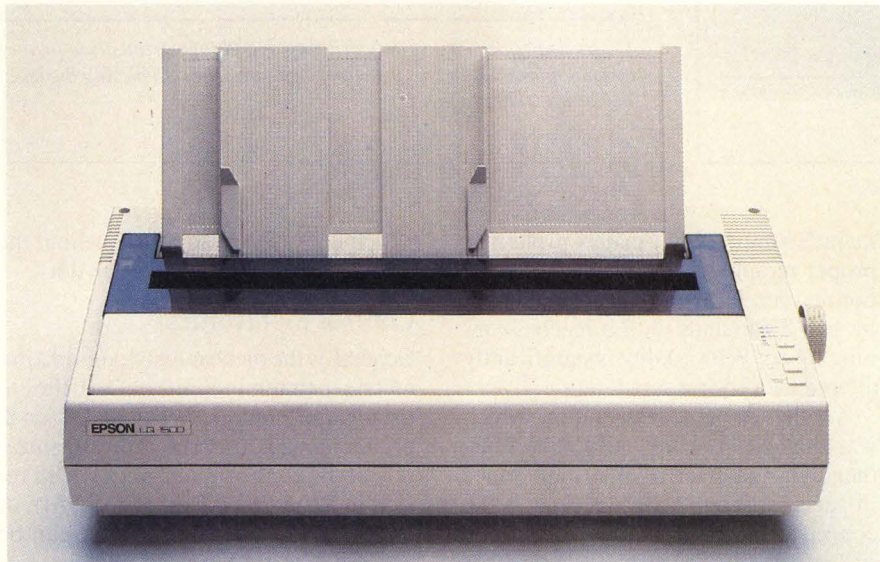
The impact line printer falls into the



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Dot matrix printers have emerged as intelligent devices for high speed, color graphics, and word processing applications making them the most popular computer hardware output device.

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The most recent introduction from Epson, the LQ-1500. Epson established the dot matrix market with the introduction of the MX-80.

low to high speed categories, but starts at a relatively expensive level of \$5,000. The raster matrix printer operates from 150 to 600 lpm with print quality depending on pin head density and speed. Chain/train, drum and belt band all have higher speeds, and higher cost, and for most applications, wire matrix is a more cost effective solution.

### Dot Matrix Design

Dot matrix printers incorporating stored energy solenoids represent the most recent in printhead design and will be used as an example in the following mechanical description.

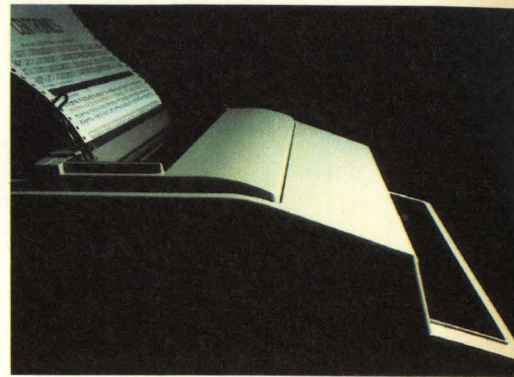
The printing mechanism on a dot matrix printer involves the electromagnetic release of a spring-steel tine called a hammer. A small permanent magnet draws the hammer back from the paper into a strike-ready position. When an electro-

magnet overcomes the field of the permanent magnet, the tip of the hammer impresses the ribbon between the paper and platen to print the dot. As the hammer rebounds from the platen, the small permanent magnet pulls it again into its field or strike-ready position.

The hammers and magnets are arranged along the print bar which moves back and forth. A character is printed after the bar moves the head to different dot positions. These dots are printed in the appropriate position of each row of the character dot matrix.

When the printer receives the information to be printed, any combination of the hammers can be fired simultaneously. After each dot row is complete, the printer bar reverses direction as a stepper motor advances the paper exactly one vertical row of dots. The next row of dots is printed and the process continues.

Using the Epson Model 321 as an example, the printer mechanism generally



The Centronics Printstation, Model 358, features eight color printing.

consists of four basic subassemblies: the chassis or frame, the paper feed mechanism, the stepper motor and the printhead assembly. The paper feed mechanism is often a tractor feed type. The paper is moved through the paper guide by two sprocketed wheels mounted on a center sprocket shaft. The sprocket shaft is driven by a four-phase stepper motor. The rotation of the stepper motor is transmitted to the sprocket shaft through a series of four reduction gears.

The carriage motion mechanism consists of another four-phase stepper motor which controls the left to right or right to left printhead assembly motion. Both the speed of the stepper motor and the movement of the printhead assembly are independently controllable in either direction. The rotation of the stepper motor is converted to the linear motion of the printhead assembly via a series of reduction gears and a toothed drive belt. The drive belt also controls a second set of reduction gears which advances the print ribbon as the printhead assembly moves.

Two optical sensors provide feedback information on the carriage assembly position and speed. These two sensors are monitored under software and provide the critical feedback needed to control the printhead assembly and paper feed motion accurately. The process of a stepper motor drive and control via feedback signals is called closed-loop stepper motor control.

A new family of printhead has emerged as the dot density requirements have increased. The newest heads hold as many as 24 printwires in the same size head as the common nine-wire model. These high density heads use very small wire, approximately 0.012" or 0.010" in diameter, compressing more dots into an area



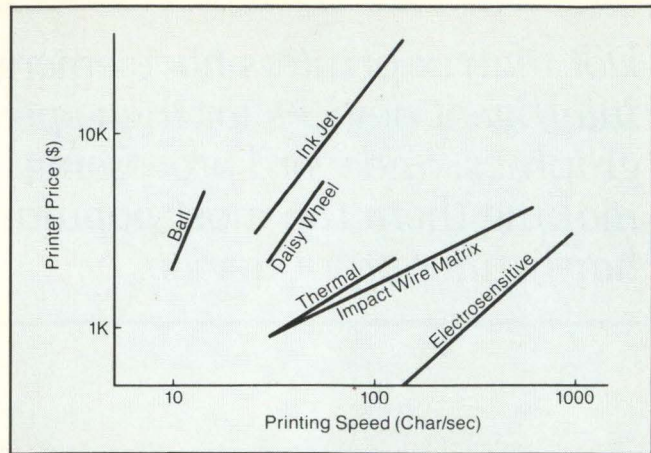
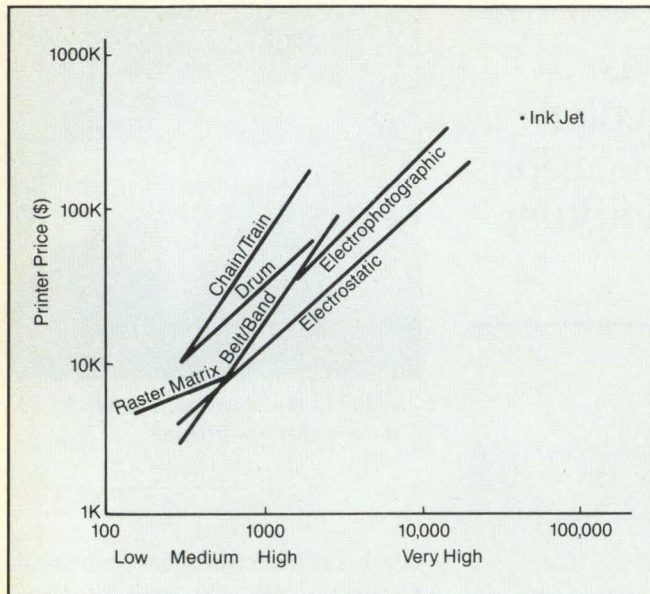


Figure 1: Printer cost versus printing speed for various line printer technologies. Figure 2: A price/performance chart depicting the leading serial technologies.

and giving better character formation.

Previously, density was achieved by overlapping pins or multiple passes of the printhead. This had a negative effect on throughput (which is measured in lines per minute). Three pass printing cuts throughput by one third, while throughput is increased if the same density is achieved in one pass (using heads with more pins). The new matrix heads still do not approximate the quality of daisy wheels, however, matrix printers have the advantage of being able to do pin controlled graphics, manipulate character size and use unlimited fonts.

Today's dot matrix designs also require that the head and carriage move smoothly and precisely. A key consideration for

manufacturers of dot matrix printers is proper ramping, which is the acceleration and deceleration of the stepper motor by step commands until it reaches running speed. Print quality is significantly altered by a poor ramp design.

Another design consideration, which was touched on earlier and deserves further attention in terms of its importance in successful dot matrix design, is the concept of closed-loop versus open-loop systems. Before the printer can send dot firing information it must know where the carriage is. The design tendency towards high pin count further requires precise control of carriage location.

Open-loop systems are designs in which the printer's control electronics get no feedback concerning the position of the carriage drive, except for initializing with a home position sensor. The mechanism depends on the stepper motor receiving a series of pulses, thus moving the carriage. This method depends on a mechanical system with precise ramps and predictable function and masses.

Closed-loop systems, like the Epson 3210, have optical detectors which send off pulses as the motor rotates or the carriage moves. This type of system monitors ramping at all times and can control the location of where the pin heads are to be fired. Two deterrents to this type of system for low priced printers are the cost of hardware to implement closed-loop control and the negative effects of vibration,

which cause the head to fall behind the carriage motion, making weak dots.

### Control Electronics

Generally, the mechanical design of a dot matrix printer is similar in different makes and models. What makes each printer unique, however, is the organization of the control electronics which reside in Read Only Memory (ROM). A dot matrix impact line printer can be organized into I/O, control-microprocessor, and dot generation logic (dgl) sections. Data is passed through I/O where it is parsed for control information and non-printable characters, and formatted by the microprocessor. Data is then converted into dots and passed to the print mechanism in the proper order by dgl.

DGL has a buffer memory for characters which are to be printed on a line, different ROMs for different character sets and dot-image ROMs. Each printable character is mapped through its dot-image ROM, yielding 8 bits. Based on the column being printed, 1 bit is extracted and passed to the hammer-driving electronics.

The UPI-42 from Intel is the most recent introduction in the company's line of control microprocessors for dot matrix technology. The UPI-42 has 2048 bytes of EPROM/ROM, 128 bytes of RAM and operates at a maximum speed of 12 MHz. Software includes data and program memory addressing, two independent and selectable 8 byte register banks and software testable I/O pins. Using the UPI-42, a dot matrix design codes its proprietary peripheral control algorithm into the UPI device, rather than into main



The Microline 92 and 93 from Okidata prints in a 9x9 matrix at speeds of 160 cps.

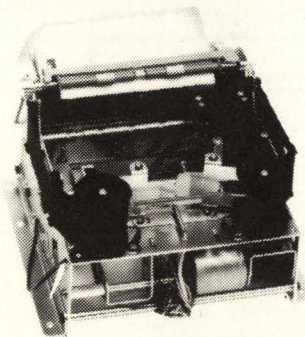


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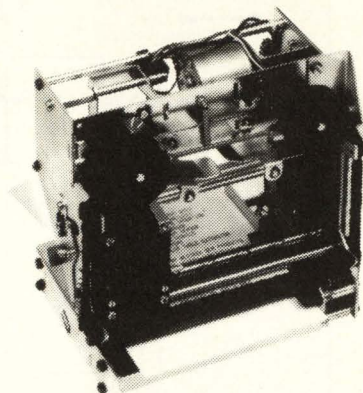
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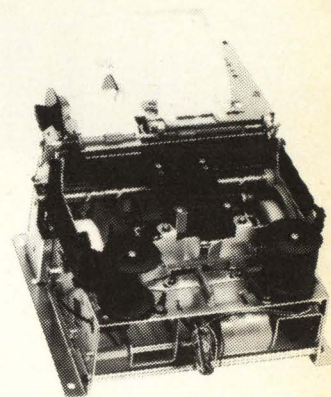
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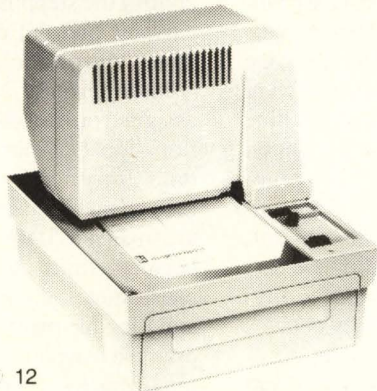
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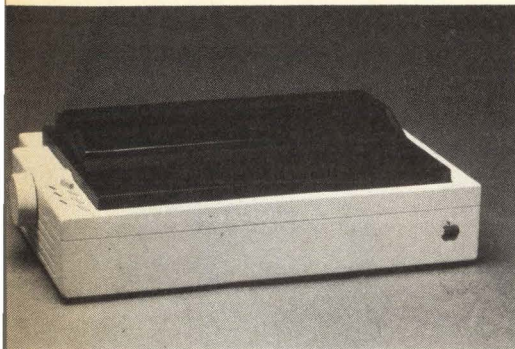


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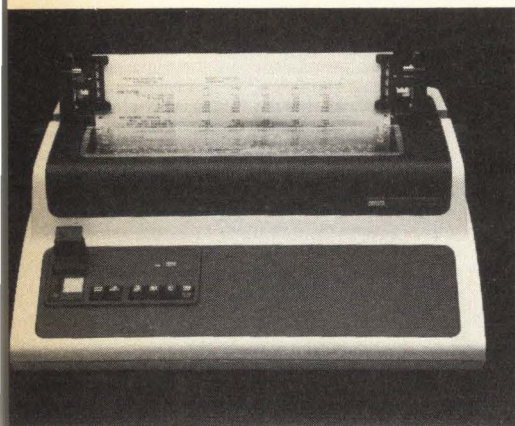
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The Scribe Printer from Apple Computer supports any personal computer with an RS-232C interface.



The bi-directional Letterprinter from Digital Equipment Corp. has 240 cps draft and 30 cps near-letter quality printing.

system software, allowing the host processors to simply issue commands and transfer data.

The host system interfaces to the printer through a parallel port to the UPI-42 data bus. Four handshaking signals are used to control data transfer. The data strobe line of the host parallel port is tied directly to the UPI-42 WR/pin. This provides a low going pulse on the UPI-42. Characters transmitted to the UPI-42 by the host are loaded into the UPI-42 data bus buffer in register, and the input buffer full interrupt and UPI-42 status flag are automatically set.

Another port provides both carriage and paper feed stepper motor phase shift signals to the printer mechanism drive circuit. Each of the resulting eight stepper motor drive signals is interfaced to a discrete drive transistor through an inverter. The emitter of the drive transistor is tied to the open collector of the inverter to provide high current sinking capability for the drive transistor. Each stepper

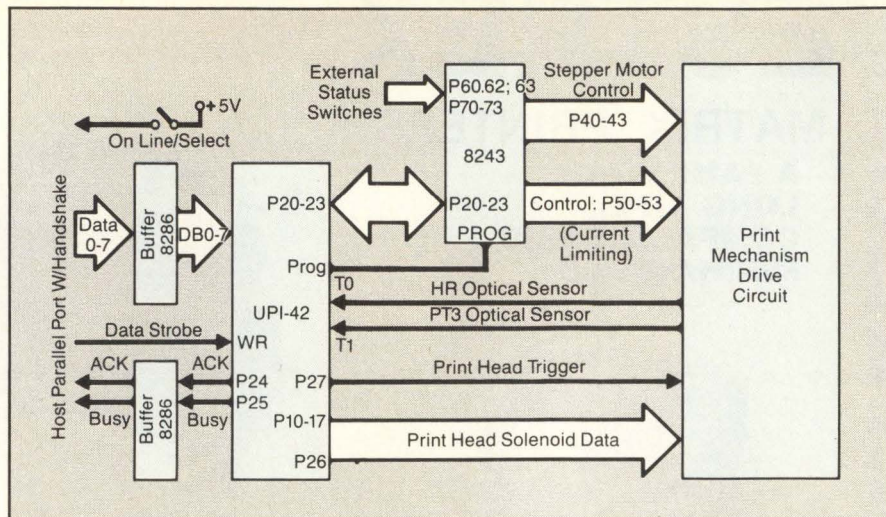


Figure 3: Hardware block diagram of the UPI-42 and 8243 interface.

motor requires two current levels for operation. These currents, called "Rush" and "Hold," allow the stepper to move with the next step signal output by switching back and forth.

By varying the voltage applied to the stepper motor biasing circuit and current, it is possible to vary the distance the motor moves the printhead assembly with each step. Enabling one of two different voltage biasing levels and changing the timing rate at which the motor has stepped, facilitates either 80 or 132 character column printing. Software design implements 80 character column printing.

A total of 11 I/O lines control the printhead solenoids and solenoid firing. Nine lines are used for character dot data, one for printhead trigger, and one for reset of the printhead trigger. Each of the nine character dot data lines is buffered by an open collector hex inverter. The printhead trigger input is tied to the trigger input of a 555 Monostable Multivibrator. The output pulse generated by the 555 triggers the printhead solenoids to fire. This output pulse momentarily enables the printhead solenoid line output, turning on the solenoid drive transistor, and firing the printhead hammer.

The TMS7041 single-chip microcomputer from Texas Instruments is well suited to character-oriented applications performed by dot-matrix printers because its serial port consists of a UART and baud-rate generator. The inclusion in the controller of a hardware-constructed serial port reduces the amount of code that must be stored in ROM and permits

higher data transmission rates than can be achieved with software.

All microcomputers in printer control systems store the printing algorithm in ROM. Dot pattern tables are placed in ROM and read as needed. The limiting factor is the speed at which these dot patterns can be referenced, causing the controller chip to rely on indexed and indirect addressing. The TMS7041 uses a table driven code which puts a major share of the microcomputer's intelligence into tables to reduce the CPU section's calculation burden. The controller is especially suitable for open-loop systems, as it incorporates two timers which control the stepping speed of the printer carriage and dot density and relies on table-driven code.

In any printer system, priorities are assigned on the basis that certain operations must be performed at a specific time. Top priority is assigned to carriage movement because motor phase voltages are involved. If the motor phases are incorrectly timed, velocity variations will cause motor jitter, resulting in uneven and illegible print. The firmware in this example is centered around the multitasking operating system. The code and dot tables fit into an on-board 4 Kbyte ROM and another 8 Kbytes are required off-chip to store information for tasks.

### Specifications Can Be Misleading

Classifying dot matrix printers by price and print speed can be as misleading as analyzing the specifications on data sheets. There are, however, three general



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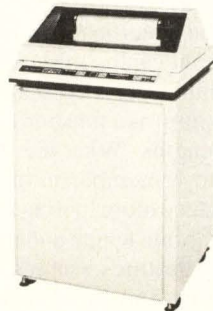


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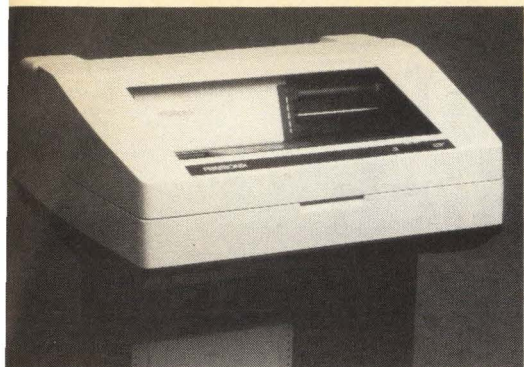
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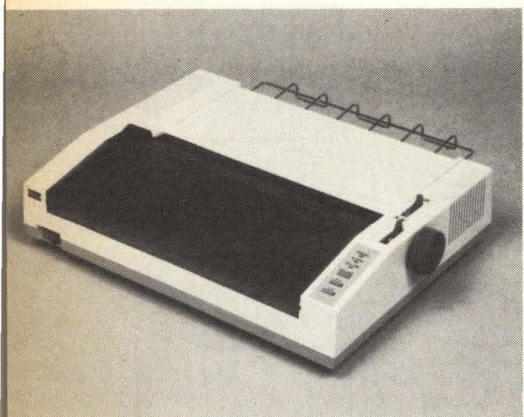
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The MVP 150B matrix line printer from Printronix.



The DMG9 from Fujitsu America is a nine-wire dot matrix printer which has a writing speed of 180 cps.

divisions into which dot matrix printers fall and all include the criteria of speed, print quality and durability.

According to Jim Shero, Vice President of Engineering at Datasouth, "It is hard to cut the dot matrix market by price or print speed. One of the big indicators is how heavy and durable a machine is which depends a little bit on price. You get what you pay for from a mechanical point of view."

Shero divides the market in the following way. At the low end, there are the light duty machines which print up to speeds of 120 cps. "This is for the user that every now and then needs hardcopy," says Shero. "It's what keeps the world going in terms of printers."

The second category includes printers for medium speed applications which have speeds ranging from 120-250 cps. These printers often have wider carriages and can print up to six copies at a time. They are heavier and more durable and have longer duty cycles. At the high end are the printers which operate at speeds of 150-400 cps. These printers have better feeding mechanisms, are more rugged in high speed applications and can handle

heavier forms. In the lower end of printers there is often the noticeable absence of a fan or blower. At 100% duty cycle, the driver circuits get warm and the power supply heats up. "If you're going to sell this printer for \$400," says Shero, "you have to build it for \$150 to \$200."

Datasouth makes three printer products which can be classified as fitting into the medium speed range. Other manufacturers, whose products range in price from \$1,000 to \$4,000, are Centronics, Data Products, Toshiba, NEC Information Systems and Genicom. These printers have graphics, high throughput rates in draft mode and near letter quality print speeds of approximately 50 cps. This category includes both line and serial printers. It is important to note that many of these manufacturers have products in all price/performance ranges and very individual methods of attaining print quality.

According to Dennis Cox, Product Marketing Manager of Printers for Epson, these individual methods are what differentiate printers. "I think basically people use the same schemes. Most of the printheads are fairly similar. It's a vertical column of dots and typically nine wires that are sweeping back and forth on the page. What happens is that people come up with more precise mechanisms and ingenious ways of doing printing functions through control coding. For instance, it is one thing to get 10 cps and an entirely different matter to do it so it's proportionately spaced." Epson has the distinction of founding the digital printer market with the MX-80, a light duty machine for personal computer applications. Price typically ranges from \$400 to \$1,000. Other manufacturers include Olympia USA, Apple Computer, Star Micronics, Fujitsu, C. Itoh, and Okidata and Digital Equipment Corp.

In all categories of dot matrix printers, analyzing the specifications for speed and throughput can be misleading. For instance, data sheets typically show throughput (lmp) as a function of several fixed line lengths. What the potential buyer has to remember is that serial printers produce more lpm because they have a shorter line length and that more sophisticated features such as bidirectional printing and logic-seeking intelligence also affect throughput.

Another factor affecting increased throughput is an efficient paper drive system, for as print speed increases, so does line speed. Whether or not a printer is bidirectional can affect throughput by 100% as throughput for a 200 cps unidi-

rectional printer is the same for a 100 cps bidirectional printer.

Reducing nonprinting time is handled by many dot matrix manufacturers by the inclusion of logic-seeking intelligence. Software logic elements can instruct the carriage to always seek the shortest nonprinting distance, and even calculate the effect of acceleration and deceleration times.

A final factor that can increase throughput is the use of a data buffer if the printer is attached to a personal computer. Often the computer may be occupied by a higher priority operation and can delay long enough in responding to the printers request for more data to affect throughput by 10%.

## Future Trends

Dot matrix design will continue to see advancements in the areas of increased intelligence and printhead design. The dot matrix printer will continue to be the primary output means in medium speed applications and will compete with daisy wheels to some degree in word processing applications. This trend will continue as long as the price/performance factor for these technologies maintains an advantage over non-impact printers.

High pin count heads are creating the greatest concern for daisy wheel manufacturers. Even though daisy print quality still surpasses new matrix heads, the difference is becoming smaller. It is entirely possible that in the near future intelligent dot matrix printers will be able to produce arbitrary patterns at any place on a page and mix text, graphic and natural images. According to Shero, "The nicest thing about dot matrix printing is that tradeoff of being able to put dots down to form a character which is legible, but not super deep, and get high speeds. Or by lowering speed, you can put down more dots which looks very nice."

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Jim Shero, "Impact Printing Technologies For the '80s," January 1980. □

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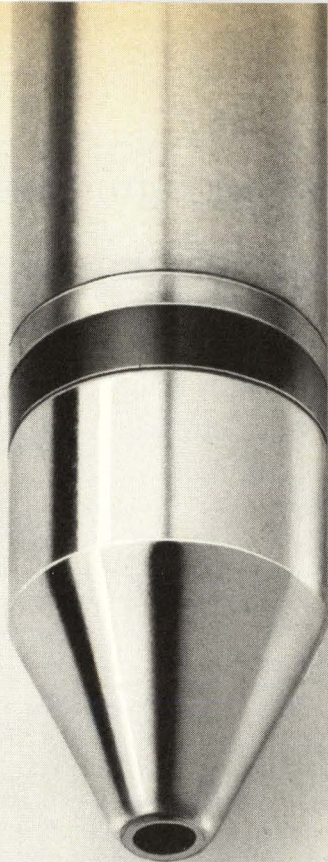
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## Texas Instruments Attacks Programmable Logic Market

Texas Instruments' new programmable logic chips are an example of how the semiconductor fabrication processes are spearheading improvements in the computer/peripherals industry. Using their improved two-micron IMPACT (implanted advanced composed technology) process, TI now offers four PALs (programmable array logic) with propagation delays of 15 nsec (max)/10 nsec (typical) and toggle frequencies of 50 MHz (Figure 1). Concurrent with this announcement, TI introduced two FPLAs (field programmable logic arrays) with delays of 20 nsec (max)/10 nsec (typical). Sophisticated processes, such as IMPACT, result in higher performance components, which translates to improved system capabilities.

According to Bob Gruebel, TI's Engineering Manager for field programmable logic, "IMPACT has been improved by utilizing more aggressive design rules made possible by improved lithography." TI also claims to offer 16K PROMs which use 165 mA of current (ICC) and have maximum address access times less than 30 nsec, although at this writing the data sheets were unavailable. TI also plans to introduce 24- and 28-pin logic sequencers in mid-1985.

The two FPLA devices, model numbers TIFPLA839 (tri-state outputs) and TIFPLA840 (open collector outputs), have 14 inputs, 32 product terms, six outputs and programmable output polarities. Like PALs, FPLAs have basic AND/OR array logic structure and are primarily used to replace random "glue" logic. FPLAs, however, provide greater programming flexibility than their PAL counterparts since both the AND and OR arrays are programmable. With PALs, the AND array is programmable but the OR array is fixed and all of the product terms are not available to each output.

Both the FPLAs and PALs use a titanium-tungsten (TiW) fuse technology. This helps to eliminate the tendency of a blown fuse to grow back by insulating it with a layer of titanium oxide. The FPLAs and PALs are housed in 24- and 20-pin 300-mil DIPs, respectively.

Like semi-custom ICs (gate arrays and standard cells), programmable logic offers an alternative to handcrafted full custom chips. Programmable logic, however, is usually the least costly solution to

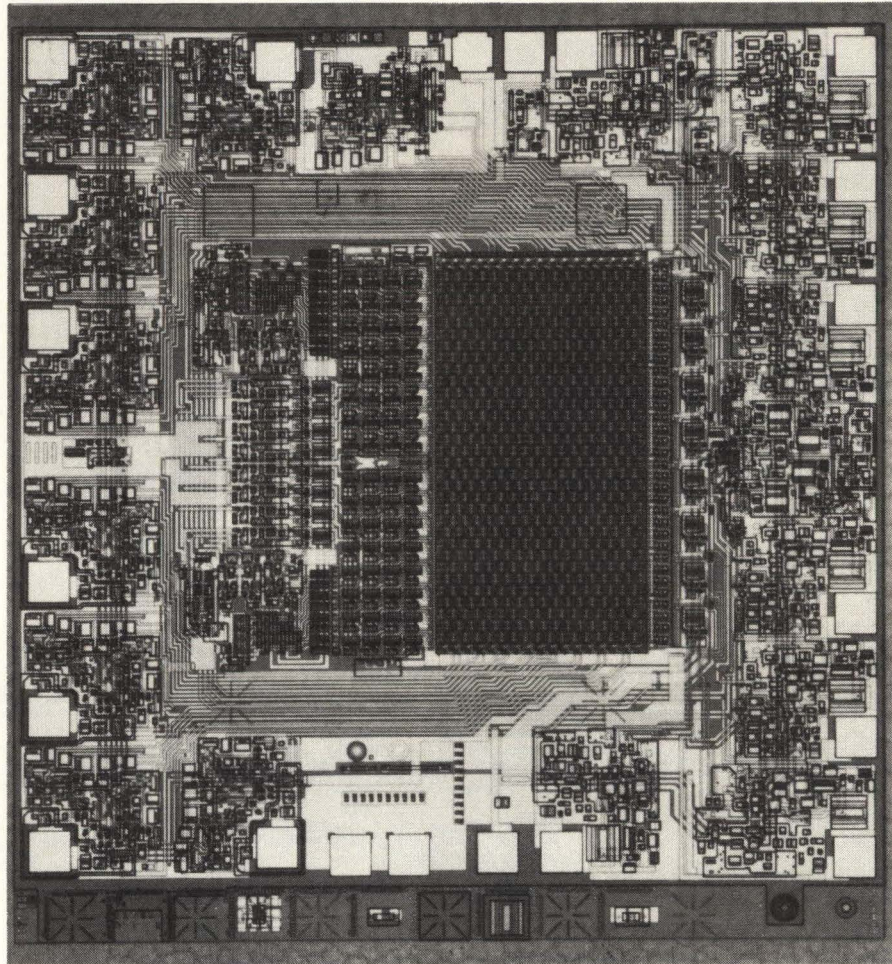


Figure 1. A photomicrograph of TI's new PAL, including some of the I/O specifications. These ICs have propagation delays of 15 nsec (max) and output-register toggle frequencies of 50 MHz.

Device	I Inputs	3-State O Outputs	Registered Q Outputs	I/O Ports
TIBPAL16L8-15	10	2	0	6
TIBPAL16R4-15	8	0	4 (3-state)	4
TIBPAL16R6-15	8	0	6 (3-state)	2
TIBPAL16R8-15	8	0	8 (3-state)	0

Note: PAL is a registered trademark of Monolithic Memories, Inc.

Comparative chart of TI's four new PALs.

reducing the number of SSI/MSI parts in a system. Development tools for programmable logic devices typically cost less than \$10,000. With low development costs and increasing levels of performance, FPLAs/PALs and PROMs provide an alternative to small high performance gate arrays.

Some of the feature/performance trends

currently evolving in programmable logic include: CMOS technology, ECL speeds under 10 nsec, TTL speeds less than 25 nsec, registered inputs, power-up clear, register preload and output polarity options. Also, larger arrays with I/O counts up to 64 pins will most likely be available soon.

—Collett

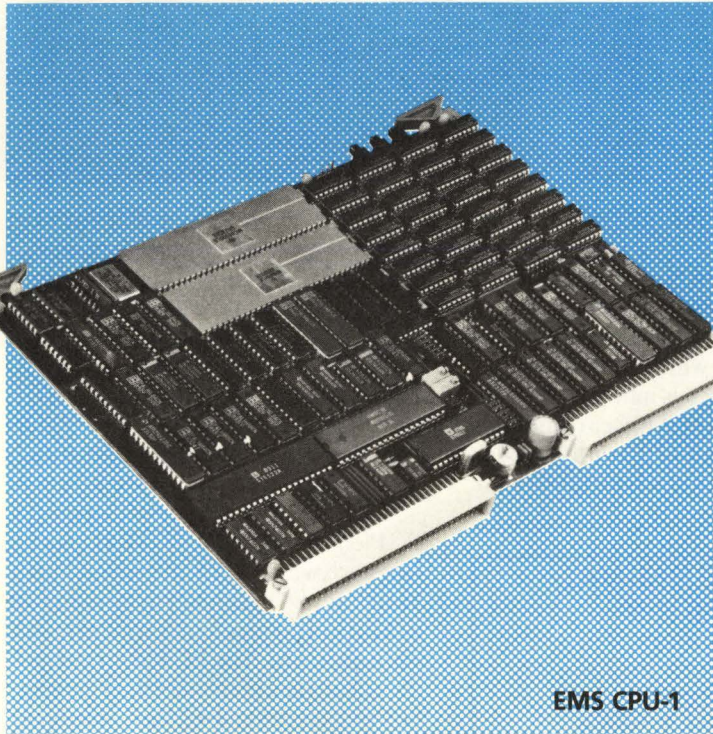
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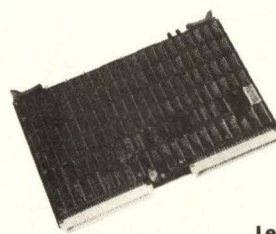
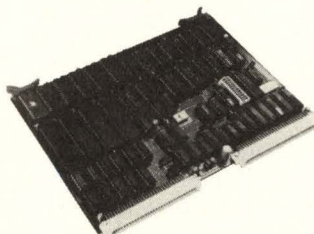
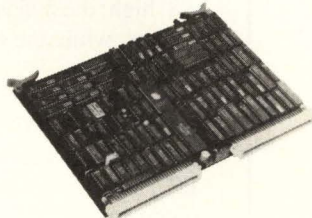
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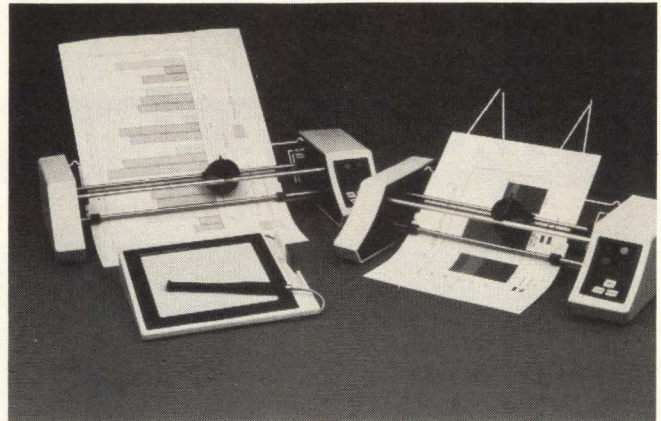


## PC Plotters Establish Market Base

As the personal computer market continues to grow rapidly, enhancements and add-on devices have caught the tailwind of this fast-paced industry. Plotters in particular, once exclusively drafting devices, have moved into many application areas, among them personal computers. More than 30,000 desktop pen plotters were shipped for use in business graphics applications in 1983. By 1987, market analysts predict annual shipments will exceed a quarter of a million. Sales are projected to increase 35% to 45% over the next five years.

The graphics boom impacts almost every market segment, spanning engineering, business, and educational products. Plotter technology has been divided into high-end and low-end products which cater to the requirements of these varied applications. High-performance desktop plotters, used for preliminary engineering drawing or quality presentation graphics, are typically priced from \$1500 to \$6000. Models for less technical

*Houston Instrument's newest desktop graphics peripherals: PC Plotter Model 695 (left), PC Plotter Model 595 (right) and the new PC PAD digitizer (foreground).*



applications fall into the \$500 to \$1500 range.

In the desktop or business graphics applications, two varieties of desktop pen plotters dominate the current market. Flatbed models, which hold the paper in place while the pen is moved on X and Y axes, traditionally have been considered the most accurate products in the desktop category. The introduction, however, of

an innovative grit drive technology five years ago made small drum plotters as accurate as flatbed models. Design engineers were able to use fewer mechanical parts, making the plotters economical and easier to use.

Houston Instrument (Austin, TX) recently introduced a multi-pen PC Plotter in the \$600 range, developed specifically for the personal computer market. As with all Houston Instrument plotters, the PC Plotter contains their DM/PL plotting language which, with the added intelligence, allows the plotter to be used with a variety of commercially available software packages. The PC Plotter can produce charts and graphs at a drawing speed of 3"/sec (axial) and 4.2"/sec (diagonal). A resolution of 0.004" is the resulting line width. The PC Plotter can be used with any computer featuring an RS-232-C interface. To accommodate difference sized plots, Houston Instrument manufactures two models of the plotter: the 595 for 8½" × 11" graphics, and the 695 for 8½" × 11" or 11" × 17" graphics. Both models are 3.8" high; the 595 is 15" wide and weighs 4.5 lbs. while the 695 is 17.5" wide and 6.5 lbs.

Houston Instrument also introduced a dual-function PC Pad which is both a compact digitizer and a mouse. On the PC Pad's 5" × 5" active area, up to 100 coordinate pairs per second can be sent to the computer, depending on the baud rate and output format. Although the PC Pad is primarily a graphics tool, it can also be used in cursor control applications with software, including a driver for a mouse. For specific OEM applications, the PC Pad may be connected so that all functions are controlled by the software and the host computer.

—Hanrahan  
Write 246

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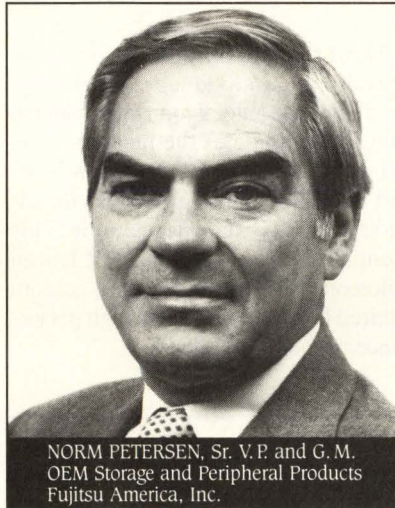
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## Floppy Disk Interface Cuts Through TTL Glue

NEC Electronics (Natick, MA) recently developed a floppy disk interface to be used as a companion chip to NEC's  $\mu$ PD765A floppy disk controller, now considered an industry standard. The  $\mu$ PB920IC may vastly simplify the task of floppy disk controller design. Using the new chip, an engineer can design a complete floppy disk controller in a single afternoon. A typical controller can be implemented with seven to nine ICs, at most. The Floppy Disk Interface (FDI) circuit eliminates from 60% to 70% of the transistor-to-transistor logic (TTL) glue chips now used in floppy disk controller design.

The  $\mu$ PB920IC FDI is an LSI device available in a 40-pin package that provides a range of functions. A floppy disk controller design using  $\mu$ PD765A and the

Table 1: Absolute maximum ratings for the  $\mu$ PB920IC.

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	VCC	+7.0	V
Input Voltage	VI	-0.5 to +7.0	V
Output Voltage	VO	-0.5 to +5.5	V

$\mu$ PB9201 requires only four to five chips, depending on individual requirements. The digital phase lock loop implemented in the FDI simulates the function of an analog PPL. If higher resolution is required, the device has provisions for addition of a VCO IC external to it. This essentially converts the digital PLL to an analog one. The external VCO is seldom required however, due to the high performance of the digital PLL.

The FDI generates the write clock and processor clock for the  $\mu$ PD765A. The clocks are automatically switched in frequency when the 8" or 5 1/4" mode is selected. These clocks are changed synchronously so that random clock edges are not generated. The FDI includes a precompensation circuit that allows delays of 0 nsec, 125 nsec, 187.5 nsec, and 250 nsec.

The on-chip drive select logic com-

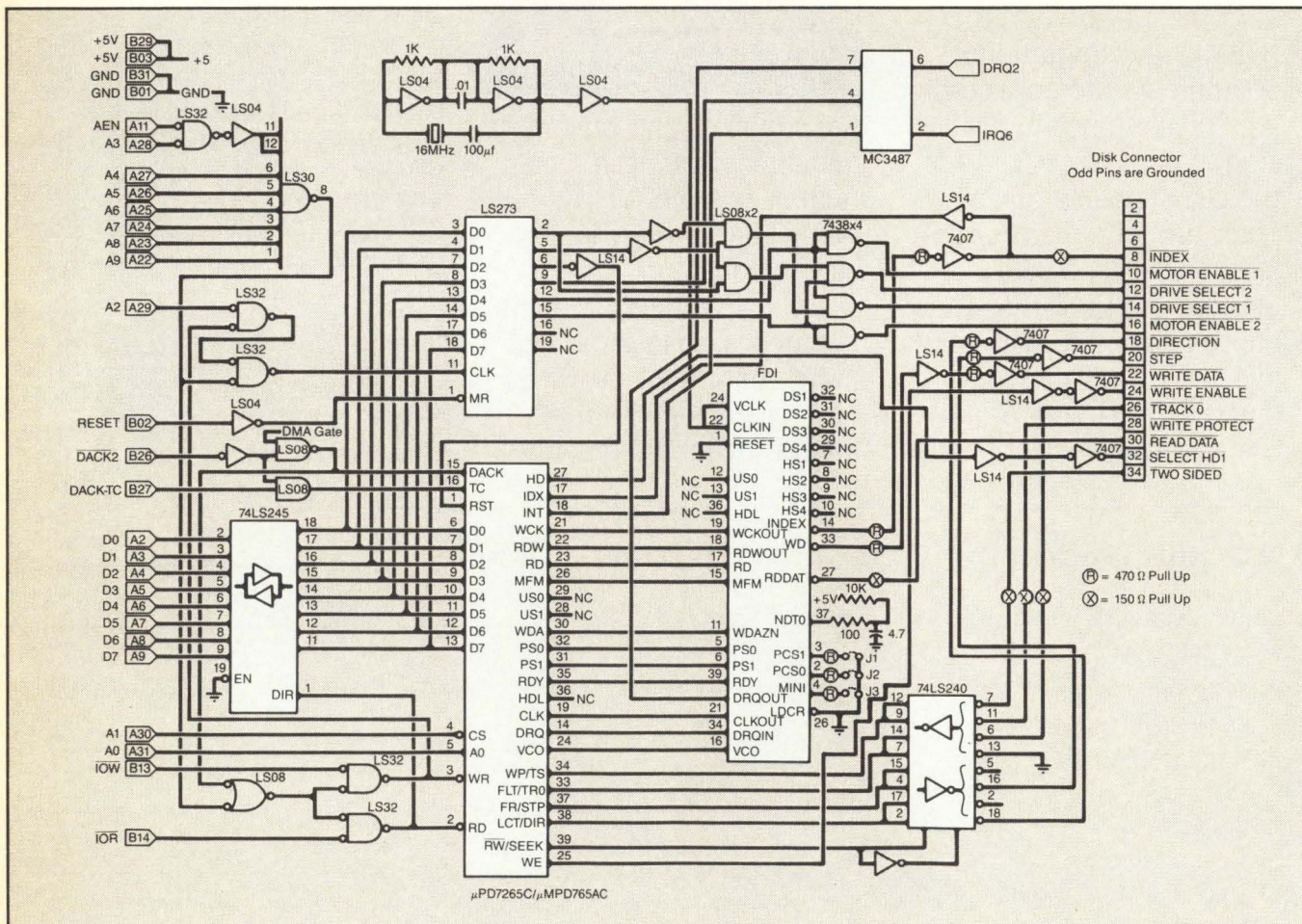


Figure 1: A logic diagram illustrates a floppy disk controller as implemented on a personal computer. It is compatible with the existing controllers, but has the ability to control 8" drives and single and double density as well.



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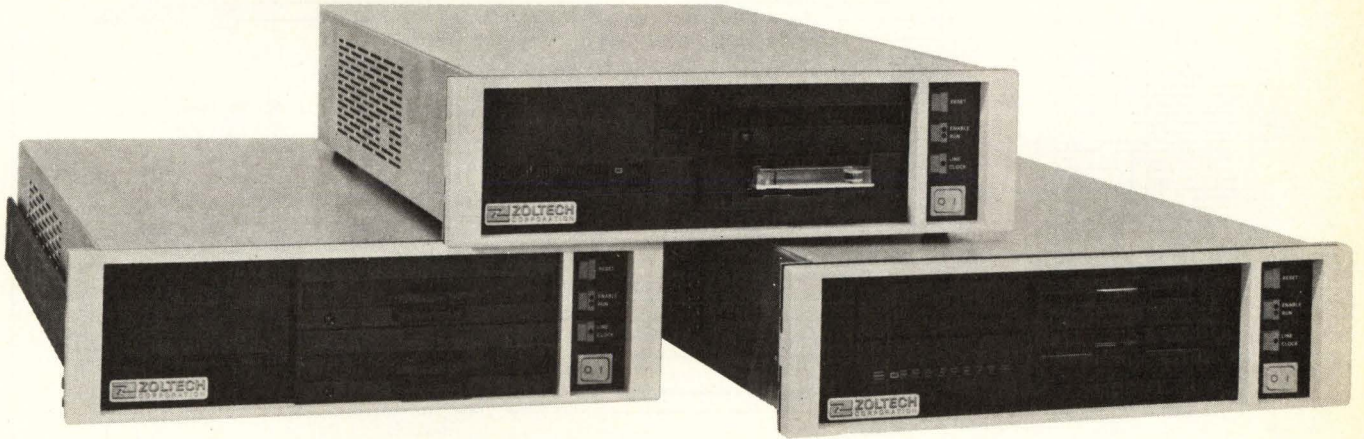
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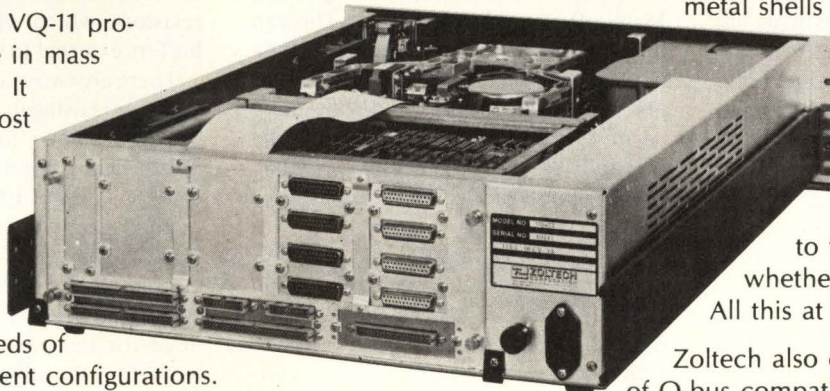
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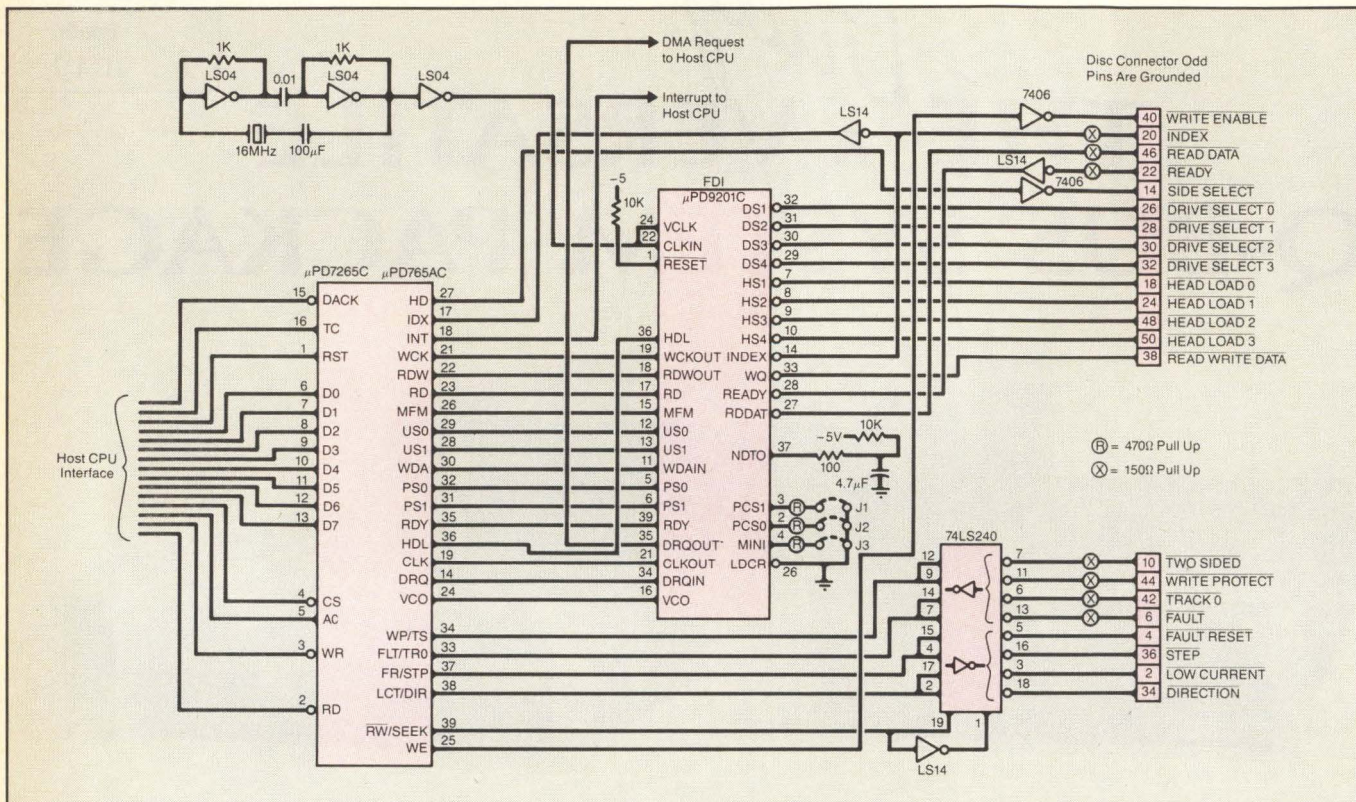


Figure 2: Typical 8" floppy disk controller; minimum parts count.

bined with the HDL (Head Load) signal eliminates the normally required selection logic. The on-chip buffers allow direct connections from DS<sub>0</sub>-DS<sub>3</sub> and HS<sub>0</sub>-HS<sub>3</sub> to the floppy disk drive. The FDI provides the designer with the ability to delay the DRQ signal that normally goes from the FDC to the host DMA controller. The minimum delay is either 0.75 μsec or 115 μsec depending on the selection of 8" or 5 1/4" mode. This allows the use of fast DMA controllers such as μPD8237A-5.

The FDI is capable of correcting a rare hang-up condition that occurs when there is no data coming from the disk drive. System problems are prevented when a read or write command has been issued and an operator mistakenly leaves a disk drive door open, or other faults occur.

## Interfacing

All the required interconnections between the FDI and a typical FDC chip such as μPD765A are shown in Figure 1. An external 16 MHz clock input to the CLKIN pin is required. The FDI generates all the internal timing from this input clock. An alternate method of utilizing

the μPB9201C is shown in Figure 2. This method minimizes the parts count and fully utilizes all of the FDI features.

The type of drive can be selected by setting the value of the MINI pin; ie, MINI=0:8" and MINI=1:5 1/4". This can be achieved by either a jumper or by a peripheral port. The PCS<sub>0</sub> and PCS<sub>1</sub> pins are used to program the device for a desired amount of precompensation. The PS<sub>0</sub> and PS<sub>1</sub> signals from the μPD764A inform the FDI on whether the bit shift is late, normal, or early.

The Load Control Register (LDCR) pin can be used as a strobe to latch the values of MINI, PCS<sub>1</sub>, and PCS<sub>0</sub> into the control register of the FDI. Whenever LDCR is low, the control register is updated. If the strobing of LDCR is not preferred, then LDCR should be connected to ground and MINI, PCS<sub>1</sub>, and PCS<sub>0</sub> should be connected either to logic one or zero, depending upon the desired mode of operation.

The FDI uses the US<sub>1</sub>, US<sub>0</sub>, and HDL signals from the μPD765A to generate the DS<sub>0</sub>-DS<sub>3</sub> (Drive Select) and the HS<sub>0</sub>-HS<sub>3</sub> (Head Select) signals. All these output

signals are capable of sinking 24mA and can be directly connected to the corresponding FDD signals (assuming the FDD contains 220/330 termination resistors; some drives contain 150 ohm pull up resistors, which will require the use of buffers external to the μPB9201).

There are two options available for the designer in using the Head Select signals. The first option is to connect all the Head Select signals together to the Head Load 0 signal of the FDD interface. This method generates one common "Head Load" signal for all drives. The second option is to add external delay circuits to each Head Select signal. This causes the head for the particular drive to stay loaded for the amount of specified time delay when the drive is deselected. The advantage of this method, as compared to the former one, is that it eliminates redundant head loading and unloading when copying diskettes to one another.

Pricing for the μPB9201C is \$12 per unit in 1K lots. Samples are available immediately, and NEC has been taking orders since the second quarter of 1984.

Write 237

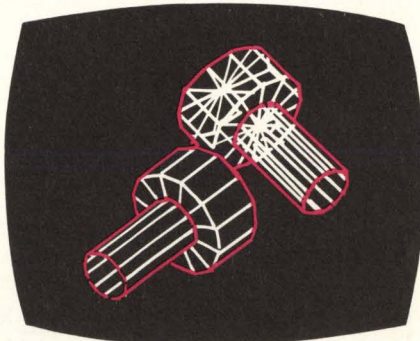


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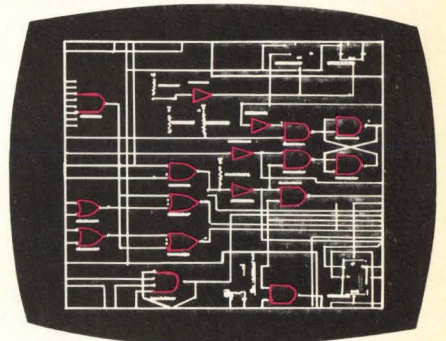
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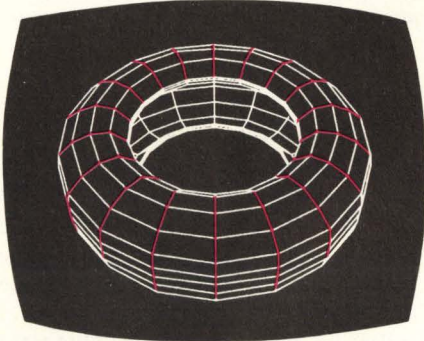
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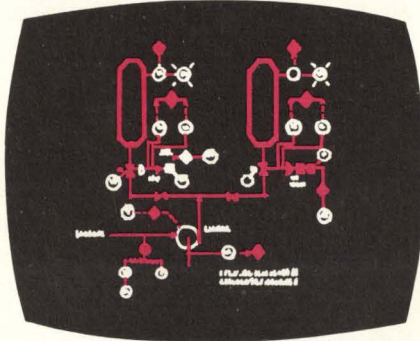
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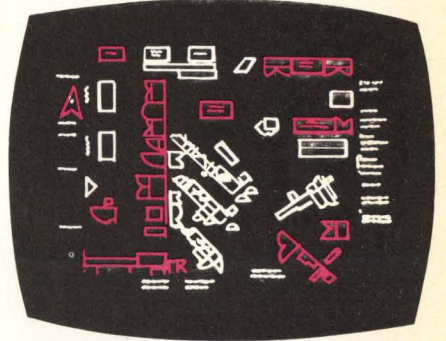
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## 14-Bit D/A Converter Provides Complete Microprocessor Interface Over Wide Temperature Range

High resolution monolithic D/A converters have been dominated by designs requiring numerous external components to provide microprocessor interface and insure accuracy. Analog Devices' (Norwood, MA) AD7534 is a monolithic 14-bit CMOS D/A converter that provides a double-buffered latch to directly interface to 8-bit buses and offers guaranteed monotonicity over the specified temperature range. A 14-bit D/A converter offers a fourfold increase in resolution compared to a 12-bit D/A converter. For audio and telecommunications designs, a 14-bit D/A converter also provides 84dB of dynamic range.

### Architecture

The AD7534 in **Figure 1** follows the standard 4-quadrant CMOS multiplying D/A converter architecture. It consists of a 14-bit D/A converter, DAC register, 6-bit MS register, 8-bit LS register and control logic. A microprocessor loads the 6 MSBs and 8 LSBs in 2 bytes and then transfers the data to the DAC register. Latching all output data simultaneously eliminates the problem of D/A converter skewing as the output takes on a new value. The converter operates as a 2- or 4-quadrant multiplying D/A converter when supplied with a variable  $V_{REF}$ .

### Converter Performance

The primary problem encountered with high resolution monolithic D/A converters is their departure from ideal performance as the converter deviates from the specified temperature at which it is tested, usually 25°C. Temperature re-

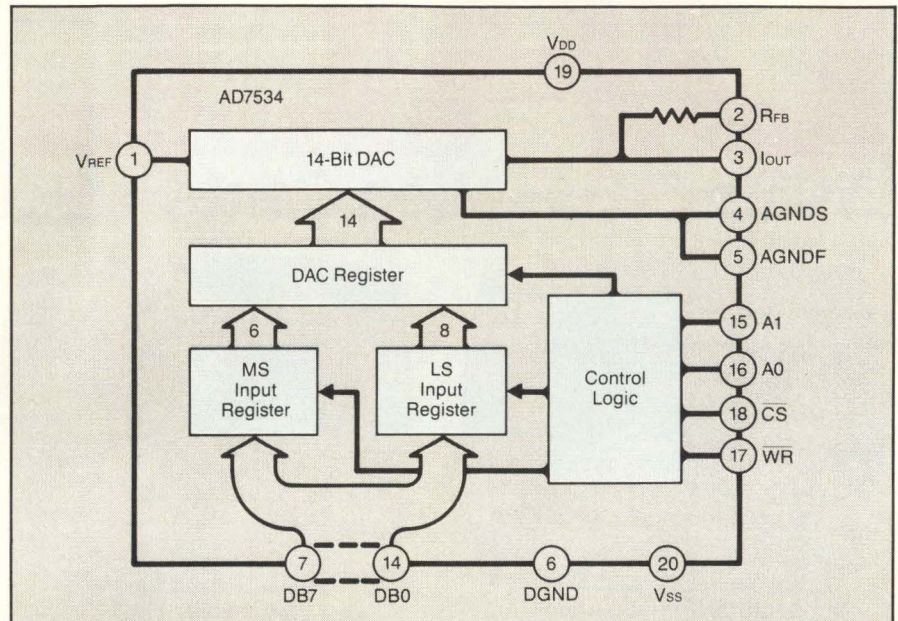


Figure 1: The AD7534 follows the standard 4-quadrant CMOS multiplying D/A converter architecture.

lated errors accumulate to where the converter is no longer monotonic; monotonic performance requires an increase in an output for each increase in the digital input code. The key specification insuring a converter is monotonic is differential nonlinearity, which must be less than or equal to  $\pm 1$ LSB (Least Significant Bit) over the entire temperature range. The AD7534 guarantees  $\pm 1$ LSB differential nonlinearity over three temperature ranges: 0°C to +70°C, -25°C to +85°C and -55°C to +125°C.

Another key specification for D/A converters is maximum full scale error. This is the absolute deviation between the expected output from a digital input code and the actual output. The lowest grade on the AD7534 guarantees  $\pm 8$ LSB of full scale error (no trims). This tight specification and low-cost of the AD7534 allow it to compete against 12-bit converters in high precision applications. The usual practice in these types of applications is to improve the converter's total accuracy by trimming out errors with external trim potentiometers. Replacing a 12-bit converter with a 14-bit converter, however, allows the user to eliminate the cost of external trims while still obtaining tighter accuracy. For example, a 12-bit D/A converter with a full scale input of 10 volts and  $\pm 3$  of LSB gain error will have a maximum output error of approximately 7.3 millivolts ( $10/4096 \times 3$ ). The AD7534 with 8 LSBs of gain error and a 10 volt full scale input will exhibit a maximum output error of only 5.5 millivolts ( $10/16384 \times 8$  LSB).

### Low Leakage Design

A major reason for temperature related errors in CMOS D/A converters is leak-

ASSUME DS: DACLOAD, CS: DACLOAD DACLOAD SEGMENT AT 000			
00	8CC9	MOV CX, CS	: DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	: TO CODE SEGMENT REGISTER
04	BF02D0	MOV D1, #D002	: LOAD DI WITH D002
07	C605"MS"	MOV MEM, #"MS"	: MS INPUT REGISTER LOADED WITH "MS"
0A	47	INC DI	
0B	47	INC DI	
0C	C605"LS"	MOV MEM, #"LS"	: LS INPUT REGISTER LOADED WITH "LS"
0F	47	INC DI	
10	47	INC DI	
11	C60500	MOV MEM, #00	: CONTENTS OF INPUT REGISTERS ARE LOADED TO THE DAC REGISTER.
14	EA0000	JMP MEM	: CONTROL IS RETURNED TO THE MONITOR PROGRAM
17	00FF		

Table 1: Sample program for loading AD7534 from 8086.



age current. Leakage current results from current flowing through the D/A current switches in the OFF state. This current increases as the temperature of the D/A increases. The external output amplifier "sees" this leakage current as a valid signal and adds it to "real" analog output, resulting in linearity, gain and offset errors. For example, the AD7534's leakage current only increases from 10nA max at 25°C to 20nA at 125°C, while many other CMOS D/A converters would increase to 200nA at 125°C. Low leakage in the AD7534 is assured by tying  $V_{SS}$  to a voltage of approximately  $-0.3V$ . The AD7534 uses this negative bias current at  $V_{SS}$  to block current flowing from  $V_{REF}$ , across the CMOS current switches in the internal resistor ladder, and out the  $I_{OUT}$  terminal. A simple resistor divider of 47K ohms and 1K ohm produces  $-312mV$  from a  $-15V$  supply. A capacitor is also required in parallel with the 1K ohm resistor to insure low leakage and must be  $4.7\mu F$  or greater.

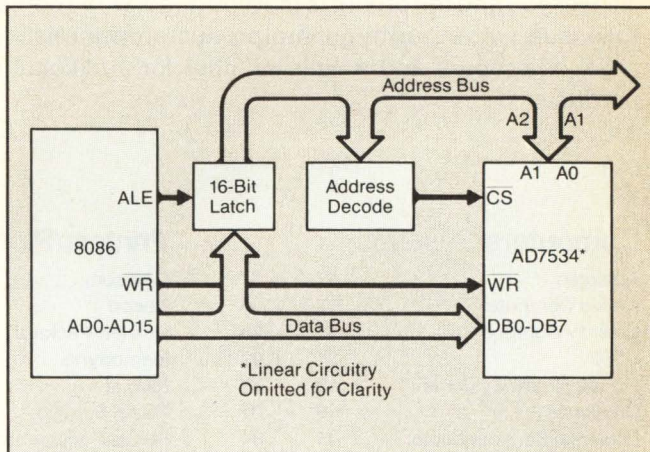


Figure 2: The AD7534-8086 interface.

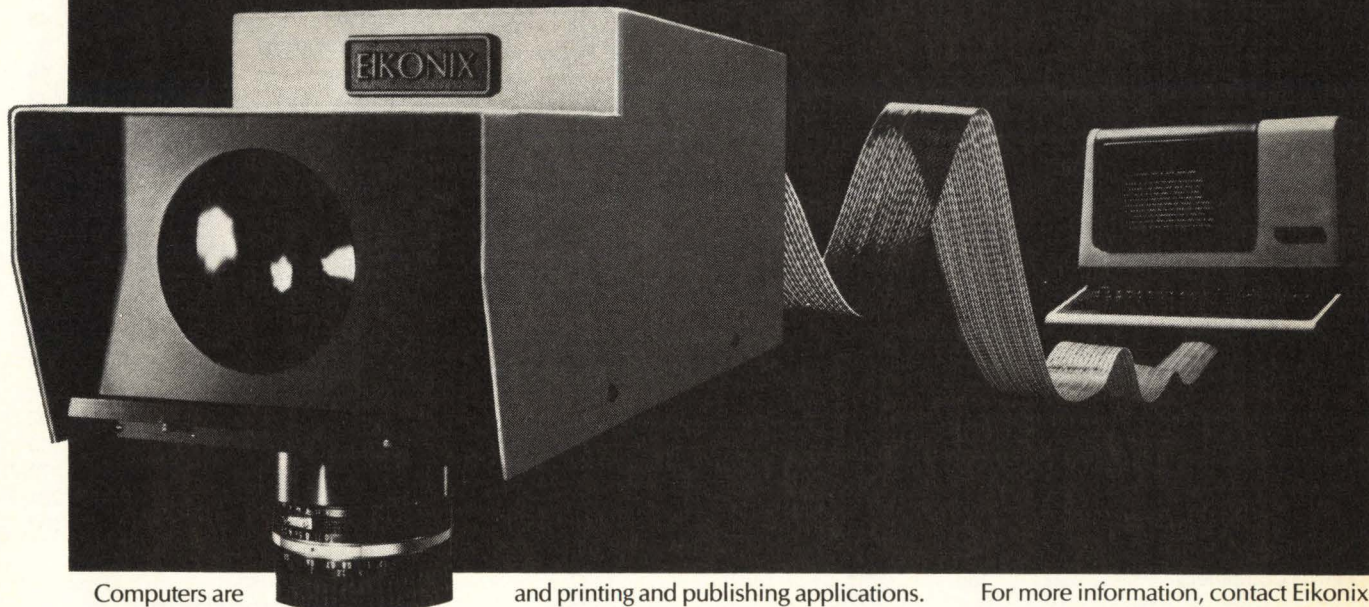
## Application

Figure 2 shows an AD7534-8086 interface. The bottom 8-bits (AD0-AD7) of the 16-bit data bus are connected to the D/A converter data bus. The 8086 loads the 14-bit word in 2 bytes using the MOV

instruction. A further move loads the DAC register and causes the analog output to appear at the converter output. The program for loading the D/A is given in Table 1.

— John Sylvan,  
Analog Devices, Inc.  
Write 238

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# PRODUCT INDEX

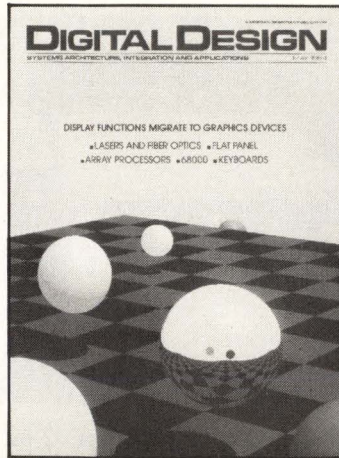
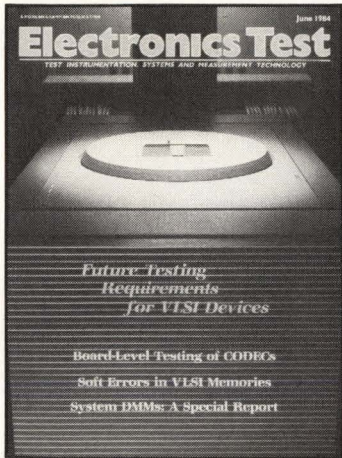
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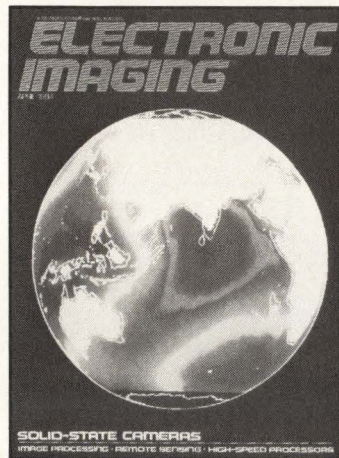
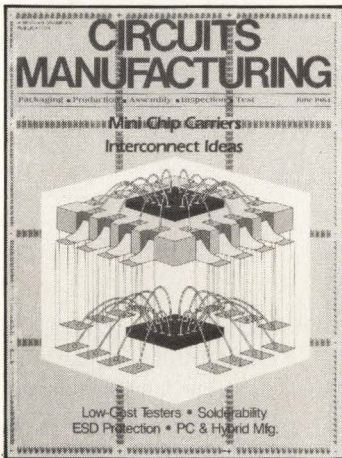
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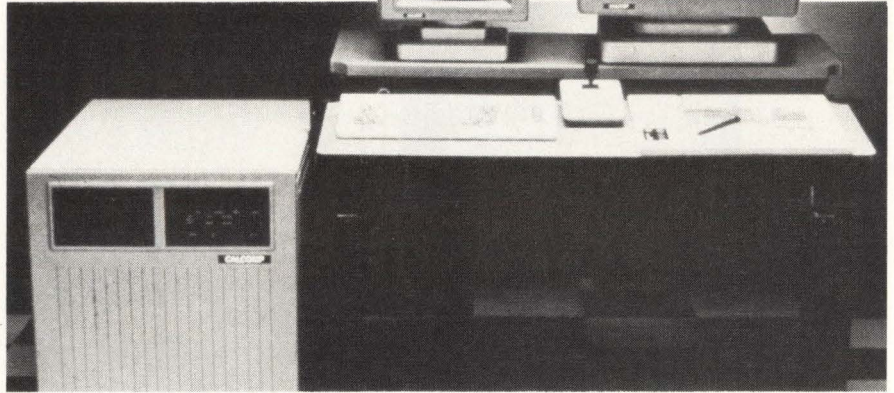
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# NEW PRODUCTS

## Graphics Design System

**C**alcomp's System 25 features a 32-bit central processing unit, distributed processing and a modular building approach that enables system expansion. The system is VAX compatible has Ethernet local networking ability, a UNIX operating system and a Multibus interface. The System 25 can be organized into single-user standalone, multi-user or mainframe-based configurations. The main station consists of two displays, a 12" alphanumeric screen and a high-resolution (20" monochrome or 19" color) graphics screen. The screen displays operator prompts and messages without interrupting information on the graphic display. The screen is furnished with a joystick for pan and zoom, and allows the operator to view either portions of the drawing close up or the entire graphic image. A digitizer tablet and

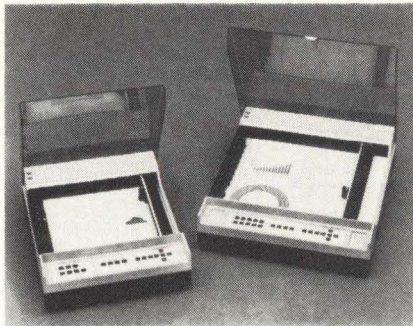


stylus are also provided. A 32-bit dual MC68000 microprocessor system with one Mbyte of memory performs all design calculations, while CalComp's Picture Processor utilizes a series of separate microprocessors to perform all the display processing. The application pro-

cessor also contains a 20-Mbyte disk drive for drawing and software storage and a 1-Mbyte floppy disk unit for data backup. An optional 1/4" cartridge or 1/2" reel magnetic tape unit is also available. Price is \$65,000. **CalComp**, Anaheim, CA **Write 126**

## Pen Plotters

**T**he Colorwriter 6300 Series of pen plotters are designed for advanced engineering, CAD, business and biomedical applications. Two formats are available: the 6310, 7-pen, 8 1/2" x 11" chart mode, and the 6320, 10-pen, 11" x 17" chart model. Both formats provide an array of colors and pen types including fiber tip and roller ball of selectable widths. An adapter accommodates Rotring or Pentel pens. Pens for producing transparencies, foils and other clear media are available. The 6300 Series has an optional continuous roll chart for high volume applications, eliminating the need to change paper manually. Using a RS-232C or IEEE-488 interface, the Colorwriter can be con-



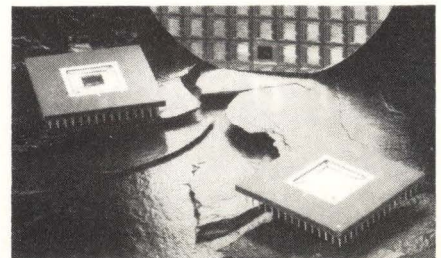
nected to any digital computer, computer controlled system or time share terminal for on-command digital plotting. Firmware includes Gould's graphic language, HP graphics language based protocols, and additional graphics standards with interchangeable PROMs. Three character sets include a Greek alphabet and upper

and lower case drafting quality characters. Other features include variable line fonts, cross-hatching, bar and pie chart capability, arc and circle generation, character rotation and slant, and zoom and window controls. Buffer memory permits 2K, 8K, and 16K word storage capability to transfer plots while the host computer is processing. The 6300 Series has a writing speed of 16"/sec. or 20"/sec. with the pen up. Addressable resolution is 0.001". An optional digitizing sight allows the Colorwriter to feedback into the computer, archive and retrieve accurate coordinates for positioning and plotting of shapes. Price starts at \$1,995. **Gould**, Cleveland, OH **Write 156**

## 64-Bit Floating-Point Chip Set

**T**his 64-bit floating-point chip set is the first to offer 2 to 8 Mflops performance, conform to IEEE and DEC floating-point standards, and provide an arithmetic solution for high-speed processors and co-processors. The

WTL 1064 and 1065 handle single (32-bit) and double (64-bit) precision formats as well as 32-bit two's complement integers. The array flowthrough time for the WTL 1064 is under 360 nsec for a single-precision multiply and under 600



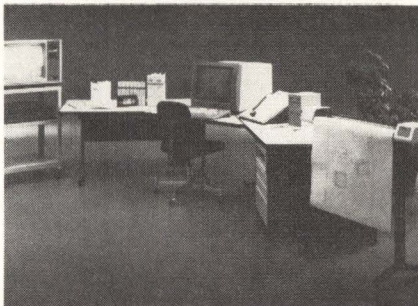


nsec for a double-precision multiply. For the WTL 1065, array flowthrough time is under 360 nsec for either single- or double-precision functions, including addition, subtraction, conversion to and from 32-bit two's complement integers, absolute value and compare. These figures include the time needed to perform the arithmetic function as well as denormalization, renormalization and exponent adjustments. The array can be divided into stages separated by pipeline registers to that another operation can begin before previous operation is completed. For the WTL 1064 multiplier, new operands can be loaded and a result unloaded every 240 nsec for single-precision and 480 nsec for double-precision multipliers. For the WTL 1065 ALU, pipelined operation time is 120 nsec for all functions. Internal timers on the chips permit the pipeline to be automatically advanced, so explicit pipeline flushing is not required. The devices dissipate 2.0 watts measure approximately 300 mils on a side. They are housed in standard 144-pin grid-array packages. **Weitek**, Sunnyvale, CA **Write 186**

## MASK-PREPARATION PACKAGE

Shapesmith PC is a mask-making software package aimed at both general manipulation of artwork data and production of pattern generation tapes for semiconductor design. The package is based on a plane-sweep algorithm and a model of a polygon to handle complex annular shapes. Shapesmith PG consists of three main programs: Polymerge, Procif, and Fracture. For optical machines, there are options to bloat the rectangles produced by a specified amount; to indicate purely orthogonal geometry, 45° geometry, or randomly oriented geometry; or to output in the form of CIF a file containing the boxes produced. For electron beam machines, the width of the electron beam can be specified. For all machines, a scaling factor can be applied to the input data. **Lattice Logic**, Edinburgh, UK **Write 153**

## TURNKEY CAD SYSTEM



The ProEd is a turnkey instructional CAD system which consists of a 6.7 Mbyte hard disk 15" raster display screen and A-B size plotter. System options include dual 19" monochromatic/color displays, dual 15" monochromatic displays, a C-D size plotter, line printer, 27 Mbyte hard disk and software packages. Price is \$20,000. **Bausch & Lomb**, Austin, TX **Write 135**

## PC/XT-COMPATIBLE INDUSTRIAL COMPUTER

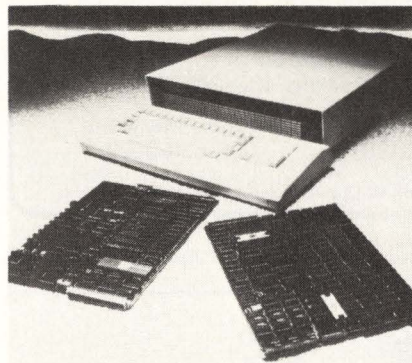
The ISI 6160 is an IBM PC/XT compatible industrial computer which can be customized for individual applications. The ISI 6160 consists of the system baseboard, five expansion slots, a 125 watt power supply and cooling fan. The system is provided in a 19" rack mountable RETMA enclosure and is protected by removable dust filters. A desk-top enclosure is available as an option. Disk storage con-

sists of one or two 5 1/4" floppy disk drives and optional 10, 20 or 30 Mbyte Winchester drives. The system baseboard contains a 4.77 MHz 8088 CPU, a socket for an 8087 Math Coprocessor, 128 Kbytes of DRAM, a floppy disk controller, a battery back-up calendar/real-time clock, two RS-232C serial data ports and a parallel data printer port. **ISI International**, Sunnyvale, CA **Write 147**

## COMMUNICATIONS SOFTWARE

The new version 4.0 of HASP+ supports the DEC DMF32 combination board on VAX systems. Users reduce overhead by using front end DMA capabilities at speeds to 56 Kbps. Using HASP+ with the DMF32 board also provides eight DMA asynchronous lines and a DMA line printer interface. HASP+ supports DEC's DPV11 synchronous interface on Q-Bus machines. A host-mode functionality has been added to allow VMS systems to act as the mainframe in a Remote Job Entry network. **Datanex**, Eugene, OR **Write 151**

## COLOR GRAPHICS CONTROLLER

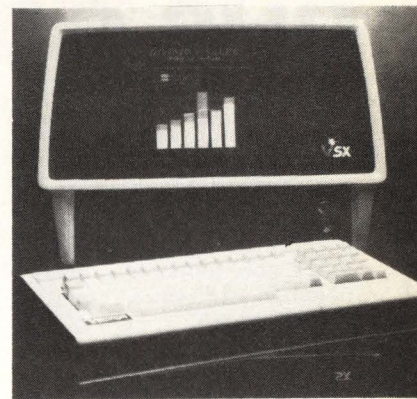


The CG2100 color graphics controller consists of a 68000 processor-based color graphics display generator with a detachable keyboard. The CG2100 provides 1024x781 pixel resolution with Tektronix 4100 compatibility. Hardware features include pixel pan and zoom over each graphics surface. The standard configuration supports either one or two graphics surfaces. Other features include VME bus compatibility, a SCSI interface, and a CPO which is ported into memory. The basic system includes one CPU module, one graphics surface (1K x 1K 16 color), keyboards and two parallel and two RS-232 interface. Price is \$3,995. **Cybernex**, Ottawa, Ontario **Write 138**

## SIGNAL PROCESSING SOFTWARE

The ILS-PC 1 is signal processing software with 30 integrated programs providing data acquisition support, waveform display and editing, digital filtering, and spectral analysis. Data acquisition includes support of A/D and D/A hardware of select vendors. Waveform-related features include graphical display (single- or multi-channel) and cursor editing of signals. Digital filtering capabilities include the design of elliptic, Butterworth, and Chebyshev filters and their application to filter time series data. Spectral analysis functions encompass Fast Fourier Transform, Cepstrum, and 2-D and 3-D graphical displays of spectra. Other support functions include arithmetic operations, linear regression, test function generation, multiplexing and demultiplexing operations. The ILS-PC 1 requires 256 Kbytes of memory and a graphics board running DOS 2.1. License fee is \$1,495. **Signal Technology**, Goleta, CA **Write 141**

## HARD DISK COMPUTER

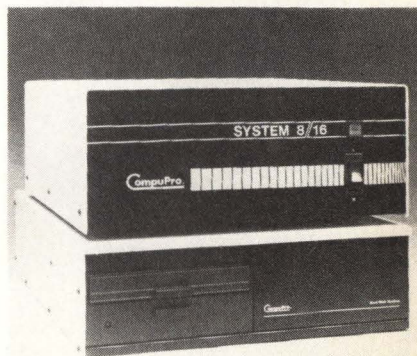


Vector Graphic has introduced 5 Mbyte models of its single-user Vector SX and multi-user Vector MX computers. The integrated 5 Mbyte hard disk in a Vector SX 2500 or Vector MX 2500 computer can be replaced with a 10-, 28-, or 36-Mbyte hard disk and a single-user computer. A Vector SX single-user computer can be upgraded to become a multi-user system. The systems have 896,000 bytes of expandable RAM. Both computers incorporate dual 8-bit Z80 and 16-bit 8086 processors. A typical configuration includes a 12" high-resolution display, integrated 737 Kbyte floppy and 5 Mbyte hard disks, one MT-50 terfihal, 384K of memory. Multi-user Concurrent CP/M-86, and the GSX-86 Graphics System Extension. Price is \$7,280. **Vector Graphic**, Thousand Oaks, CA **Write 130**

## 16-BIT MICROCOMPUTER

The SYSTEM 68 is a 16-bit microcomputer equipped with one Centronics port, 512 Kbytes of memory, 85 Mbyte hard disk and 1 Mbyte 8" floppy. The SYSTEM 68 is based on a 10MHz 68010 microprocessor, and is upgradeable to 16 users. UNIX V operating system is supported by the SYSTEM 68. Price is \$19,995. **IBM**, Chatsworth, CA **Write 144**

## 32-BIT MICRO SYSTEMS



The System 816/G and System 816/Gg are IEEE 696/S-100 compatible micro computer which can be configured with 80 Mbytes, 40 Mbytes or 20 Mbytes of hard disk storage, or a 2.4 Mbyte dual 8" floppy subsystem. The NS32016 microprocessor has a 32-bit internal architecture and a 16-bit external data bus. The basic System 816/G features 1 Mbyte of static RAM, expandable to 16 Mbytes, 2 Mbytes of solid state disk memory, 12 serial ports, one printer port and one parallel port. The Forth operating system is bundled as well. Price is \$17,495-\$23,995. **CompuPro**, Hayward, CA **Write 146**

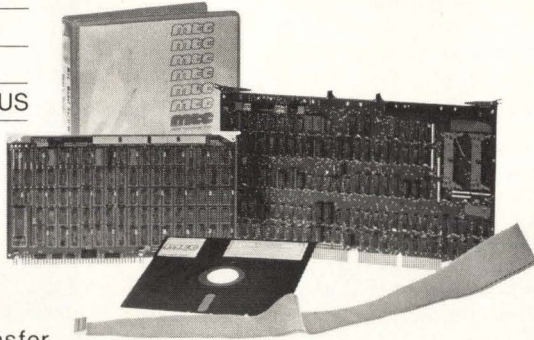


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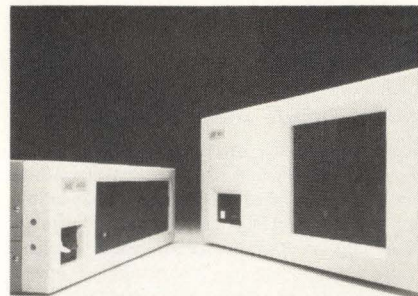
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## NEW PRODUCTS

### C COMPILER

The Safe C Compiler provides run-time checking of C programs and produces a dynamic trace of function calls with their arguments and returned values. A C program that has been compiled with Safe C behaves as if it were compiled by the system's C compiler, with the exception of messages that are written to the standard diagnostic stream warning of potential problems. Each of the run-time checks and tracing can be controlled at run time from within the program. Code generated by the compiler can be linked with object modules generated by other compilers and assemblers. Prices range from \$400 for an MS-DOS version to \$4000 for a VAX II/780. **Catalytix**, Cambridge, MA    **Write 154**

### 68000-BASED SYSTEM



The Multibus-compatible SBE 300 line of 16/32-bit computer systems executes at 10 MHz with no wait states. The systems combine a 68000 or 68010 MPU with the REGULUS operating system. The memory management circuitry contains 32 independent maps and each is capable of supporting a real-time task 4K to 8 Mbytes in size. Up to 8 Mbytes of hardware-refreshed, no-wait-state dynamic RAM can be accessed by the CPU at a 10 MHz rate. The CPU interfaces with a high-speed disk controller through a multimodule interface. Mass storage is provided by a 10Mbyte 5 1/4" hard disk and a 320 Kbyte 5 1/4" floppy. Price is \$5,795. **SBE**, Emeryville, CA

**Write 148**

### MULTIAPPLICATION SYSTEM

The Designer V-X Series M system incorporates a CGP graphics processor and supports four additional 300 Mbyte disk drives along with the standard 300 Mbyte disk included with the system. The system can support three interactive users simultaneously, and is available in several configurations. A basic system includes a CGP 200X processor, CADD5 4X software, one 300 Mbyte disk, tape drive, two color graphics terminals, and an application package. Price is \$250,000. **Computer-vision**, Bedford, MA

**Write 131**

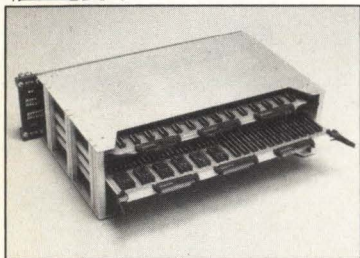
### INTELLIGENT TERMINAL EMULATOR

This emulator from Rabbit Software is a new version of its 3270-Plus intelligent terminal emulator, which is based on UNIX operating systems and compatible with IBM's SNA. 3270-Plus/UNIX is compatible with all 16- and 32-bit microcomputers running AT&T UNIX or OEM-compatible operating systems. Facilities include screen-to-file, record options and printer-to-file to move data from host computer to workstation cluster. 3270-PLUS provides IBM 3286 and 3287 printer support. **Rabbit Software**, Malvern, PA

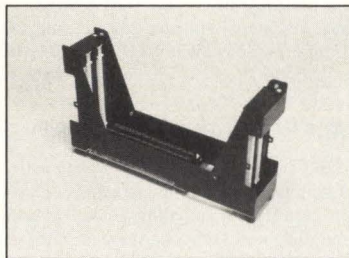
**Write 142**



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ON THE  
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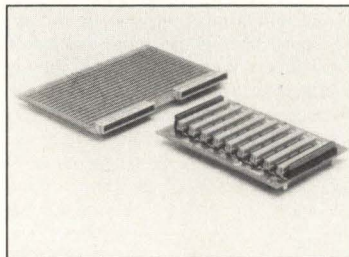


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## GRAPHICS TERMINALS

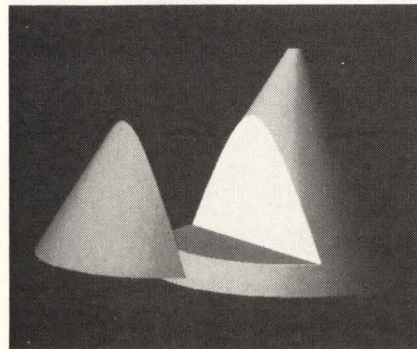


Digital Engineering's Hi-scan graphics 4210 monochromatic and 4205 color terminals now support I/O devices from manufacturers such as Tektronix, HP, DEC and Summagraphics. The terminals have vector graphing speeds of 1 Mpixel/sec. The terminals have 800 x 600 pixel monochrome and 800 x 300 pixel color display resolution, non-interlaced display, and compatibility with Tektronix and DEC protocols. Four-level gray scale is offered in monochrome and 16 simultaneously displayable colors out of a palette of 64 in color. **Digital Engineering**, Sacramento, CA **Write 134**

## MULTI-USER DESIGN SYSTEM

SuperPDL is an interactive Multi-User design system featuring a structured design language, design analysis facility, and full documentation capability. SuperPDL is based on top down design, information hiding, and structured design, generating modules with defined interfaces. Its menu-driven software includes a full-screen structured editor. Design analysis is provided by a consistency processor which continuously alerts the user to possible design inconsistencies, insuring compatibility of his design with the rest of the project. Documentation comprises reports, including the calling tree, cross references, and design-analysis data. **Advanced Technology Information**, New York, NY **Write 150**

## SOLID MODELING SYSTEM



Cubicomp has added a boolean construction operations extension to its microcomputer-based solid modeling system. The extension permits industrial designers and other CAD users to simulate the fabrication process that transforms raw material into a finished product. The Cubicomp solid modeling system is based on the IBM PC and permits users to create, display, manipulate, and store three-dimensional, full-color shaded-surface solid models. The system displays up to 4096 colors out of a palette of 16.8 million. Price is \$1,900. **Cubicomp**, Berkeley, CA **Write 140**

## LOGIC SIMULATION INTERFACE

The NX-TDL interface allows engineers using P-CAD software to upload logic designs to the TEGAS simulator for processing. NX-TDL converts netlists generated from P-CAD logic designs into the TEGAS format. TEGAS simulates logic for electronic devices ranging in size from ICs, VLSI chips to complete systems. All programs are Texas Instrument and IBM compatible. Price is \$500. **Personal CAD Systems**, Los Gatos, CA **Write 132**

## 68000 MICROCOMPUTER

The Pinnacle is a 12 MHz 68000 microcomputer which executes three million instructions/sec. Clock speed is 12 million cycles/sec and its RAM operates with no wait states. RAM size can accommodate eight million characters and the Pinnacle's hard disk capacity is 32 Mbytes. The microcomputer includes 8 ports UCSD p-system operating system and real-time clock. Price is \$3,895. **Pinnacle Systems**, Dallas, TX **Write 137**

# BA11-VA BA11-ME USERS:

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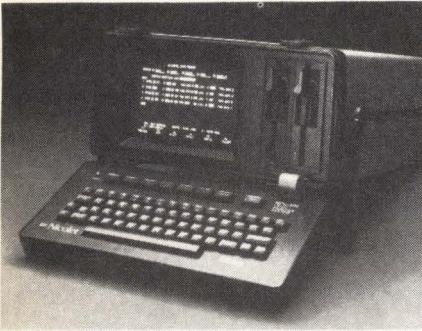


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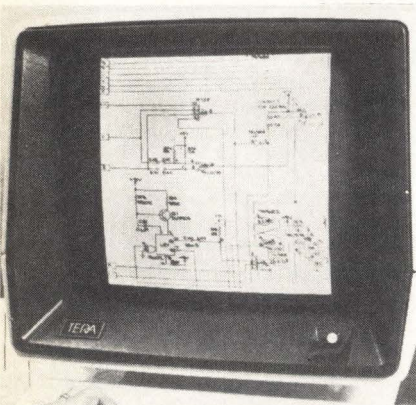


## LOGIC ANALYZERS



The five 800-Series machines include the NPC-800A, which is a logic analysis system with a 32-channel state analyzer and a 16-channel timing analyzer displayed on a 9" CRT. Other models are: the NPC-800B, which has 8- and 16-bit micro-processor capability; the NPC-800C, which permits 200-MHz timing; the NPC-800D, which has 200-MHz timing and state analysis; and the NPC-800E, which is for users requiring 200-MHz timing analysis without a state analyzer. The timing analyzer collects data and processes two trigger levels at 200 MHz on 16 channels. Options include a IEEE 488 controller, non-volatile memory, second disk drive, counter/timer/signature analyzer and performance analysis histograms. Others are a waveform recorder, dot matrix printer, printer software, dedicated probes and in-circuit emulators. Price is \$7,950-\$14,900. **Nicolet**, Fremont, CA **Write 128**

## GRAPHIC EDITING WORKSTATION



This editing workstation converts film, paper and CAD-generated drawings into raster images. Engineering drawings can be created, manipulated, erased and corrected on one stand-alone workstation. Drawings stored on film and paper can be scanned into the editing workstation and modified. In addition, new records can be transmitted directly from installed CAD systems, edited, and output to film and paper. The workstation is comprised of four primary components: an aperture card scanner with Hollerith code reading capability; a display terminal; M68000 and IBM PC-XT processors which provide image panning, zooming, rotation, raster and vector editing, and a laser printer. Price is \$63,000-\$98,000. **Tera**, Berkeley, CA **Write 136**

## ENTRY-LEVEL SUPERCOMPUTER

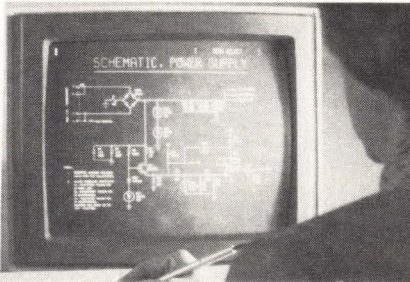
The five IBM mainframe-compatible entry-level supercomputers from National Advanced Systems, the AS/91X0 series are designed to handle vector-

processing applications. The AS/91X0 performs at 28 MFLOPs and is field upgradable. The AS/91X0 computers include a software tool, called VAST, which looks for operations it can vectorize, and when it finds them it inserts appropriate code to activate the vector-processing hardware. VAST does not have to recode existing programs. Price ranges from \$2.1 to \$5 million. **National Advanced Systems**, Mountain View, CA **Write 152**

## APPLICATIONS PROCESSOR

The SP/1008 Application Processor utilizes the 8-bit Z80B operating at 6MHz. Each processor contains its own local memory and I/O. Sixteen SP/1008 processors may reside in a NoHALT system, each with its own operating system, application program, and application data area. The processor has four serial communication channels. Two standard channels offer asynchronous, synchronous, or high level protocol operation supporting SNA and X.25 protocols with optional NoHalt software. The signal interface level is RS232-C with modem support on all four channels. **NoHalt Computers**, Farmingdale, NY **Write 143**

## TURNKEY CAD/D SYSTEMS



The DesignPro/E is a turnkey CAD/D system for PCB design. Supported by a 8510 monochrome and 8600 color high-resolution graphics system, the DesignPro/E system provides digitizer and interactive schematic capture, schematic drawing, interactive PCB layout, netlist extraction for off-line autoplacement and routing, bills of material reports, tape output for off-line photoplotter PCB artwork, and automated back annotation for schematic updating. The system includes a CPU memory, graphics raster processor, 10 Mbyte disk and 1.2 Mbyte floppy disk, 15" high-resolution tilt-swivel monitor, digitizer, 22 ips "D" size plotter, keyboard, and software. Price is \$40,000. **Terak**, Scottsdale, AZ **Write 155**

## MICROPROCESSOR DEVELOPMENT SYSTEM

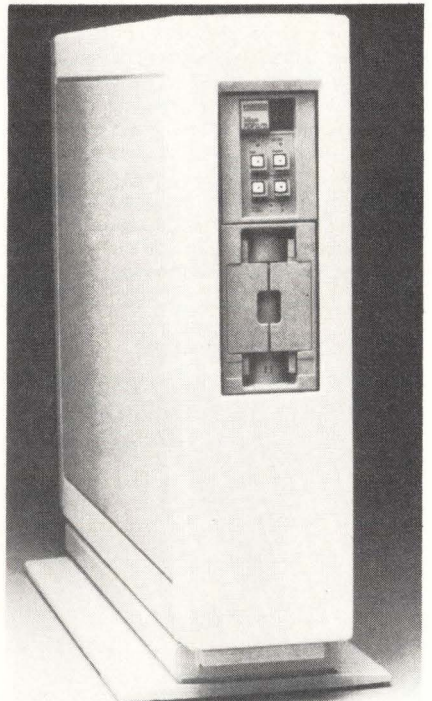
The Series IV microprocessor development system from Intel, has been enhanced for multiuser development operation. Two users can share a Series IV by connecting a second terminal to one of the system's serial ports. Series IV stations operating in Intel's network development system environment (NDS-II) can be augmented with plug-in boards that allow additional users to gain access to the network through that station. The Series IV permits single users to switch back and forth between foreground and background tasks. By attaching a second terminal via the Series IV serial port, one user can work in the foreground while a second works in the background. Workstations on the NDS-II can be Series II, III and/or IV development systems. Four cluster boards can be hosted in Series IV. **Intel**, Santa Clara, CA **Write 129**

## 8086 BASED PERSONAL COMPUTERS



The Compaq Deskpro Family consists of four personal computers which utilize the 8086 micro-processor. The entry-level system includes a 360 Kbyte diskette drive, 128 Kbytes of RAM and a dual-mode monitor which displays text and graphics on the same screen. The monitor is available in green or amber display. The Model 4 has 640 Kbytes of RAM, one 360 Kbyte diskette drive, a 10 Mbyte fixed-disk drive, an internal 10 Mbyte fixed disk drive backup system, a dual-mode monitor, and an asynchronous communications/clock board. Price ranges from \$2,495-\$7,195. **Compaq**, Houston, TX **Write 133**

## MULTI-USER SYSTEM



The MicroPDP-II/73 is a higher capacity version of DEC's MicroPDP-II series of supermicro-computers. The MicroPDP-II/73 runs Digital's A-to-Z integrated multi-user applications software and two systems incorporating the RC 25 disk subsystem are also now available. The MicroPDP-II/73 features the 15MHz J-II chipset, 512 Kbytes of main memory, the RC 25 single disk subsystem with 26 Mbytes of fixed storage and 26 Mbytes of removable storage on an 8" disk cartridge for backup. Price is \$19,500. **Digital Equipment**, Maynard, MA **Write 127**



## KEYBOARD



The KB5150 keyboard is designed to upgrade the existing keyboard on the IBM PCjr. It features a typewriter layout with standard size keys and a low profile design. The KB5150jr has LED indicators on the lock keys, key legends rather than symbols, index finger homing keys, and an ENTER key. Price is \$219. **Key Tronic**, Spokane, WA **Write 180**

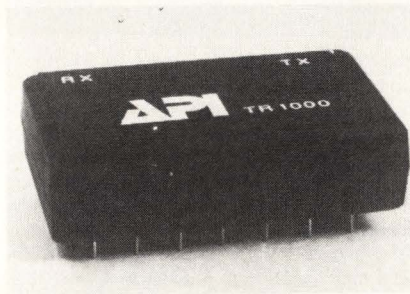
## CSMA/CD LOCAL AREA NETWORK

Tienet is a vendor independent baseband CSMA/CD LAN which provides high-speed intercommunications between diverse computers and peripherals without regard to differences between them. Tienet has a 1 Mbit/sec aggregate data rate allows multiple connections, cable lengths of five miles and noise immunity. Tienet can intercommunicate 5,000 user stations at a rate of 19.2 Kbaud. The maximum number of station connections is 24,000. Tienet supports the OSI model layers one, two, and three, and provides partial services in OSI layers four, five, and six. Price is \$626 to \$910 per station connection. **Pramatronics**, Boulder, CO **Write 226**

## 1.6 MBYTE FLOPPY DISK

The MD2HD is a 5 1/4" 1.6 Mbyte floppy disk which has a recording density of 9650 bpi. Other features include a RD Binder system, which is a three-dimensional network structure. The MD2HD is compatible with existing 8" disk software and controllers by installing the 5 1/4" 1.6 Mbyte drive units. Price is \$11.00. **Fuji Photo Film**, New York, NY **Write 177**

## FIBER OPTIC TRANSCEIVER



The TR1001S Series of fiber optic transceivers are capable of transmitting data at rates of 100Mbps NRZ. Two versions are available; the TR1001SA which has an 8dB system margin and utilizes a surface emitter LED in the transmit section; and the TR1001SB which has a margin of 17dB utilizing a edge emitter LED. The TR1001SA and TR1001SB sell for \$275 and \$550 each. **American Photonics**, Brookfield Center, CT **Write 164**

## 25 CPS DAISY WHEEL PRINTER

The 5025 is a 25 cps letter-quality printer which includes a 2K or 8K buffer. The printer is designed with either RS-232C Serial or Centronics/IBM Parallel interface. It prints in both directions with adjustable character spacing of 10, 12 or 15 cpi, and can handle paper up to 15" wide. The daisy wheels are cartridge-designed. Price is \$899. **Amdex**, Elk Grove Village, IL **Write 179**

## HARDCOPY OPTION

The CH-5201 video interface adds color hardcopy to the IBM 5080. The CH-5201 produces both color transparencies and plain paper copies in resolutions of 150 dpi with light colors. The CH-5201 incorporates a local frame buffer memory to store the image prior to generating output on paper. The image is loaded into buffer memory after the copy button is depressed. The frame buffer allows an image to be retained for multiple copies. Sensors control the amount of ink transferred from its donor sheet to paper or transparency film. The CH-5201 uses a dry ink sheet roll. Price is \$11,950. **Seiko Instruments**, Milpitas, CA **Write 167**

## FLEXIBLE DISK DRIVE

The FD 1155 is a 5 1/4" disk drive which has an unformatted 1.6 Mbyte capacity. The drive has 96 pi and uses 4.5 watts. Media eject, high mean-time-between-failure, 12,000 POH and direct-drive brushless motors are standard. **NEC Information Systems**, Boxborough, MA **Write 160**

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- Model 80-0026 Z80, A,B CPU/Mem/Dart/CTC/PIO
- Model 80-0027 Z80, A,B CPU/Bat-Backed Mem/Clock

### INPUT/OUTPUT

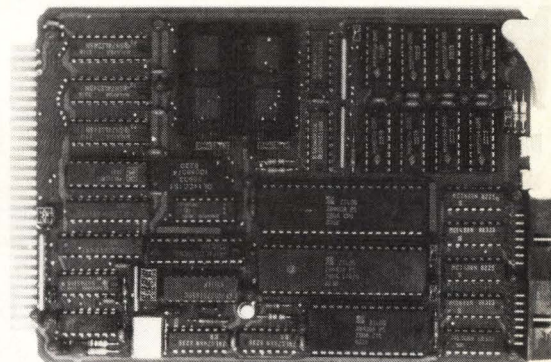
- Model 80-0021 6 Port SIO RS-232
- Model 80-0022 OPTO-22 Interface
- Model 80-0023 24 Pos. OPTO-Input
- Model 80-0024 24 Pos. OPTO-Triac Output
- Model 80-0025 24 Pos. OPTO-Output

### MEMORY

- Model 80-0000 16K CMOS RAM/Battery Backed
- Model 80-0001 Byte-Wide Memory
- Model 80-0010 16K/32K EPROM
- Model 80-0016 65K RAM
- Model 80-0017 I/O Access Byte-Wide Memory

### SPECIAL FUNCTION

- Model 80-0028 103 Modem/RS-232 Port
- Model 80-0029 212A Modem
- Model 80-0015 Real Time Clock
- Model 80-0012 STD Proto Card
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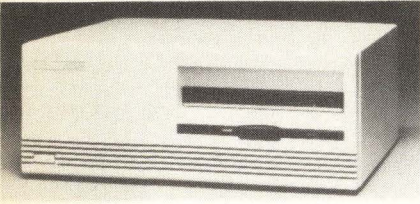
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## 1/4" TAPE DRIVE



The HP 9144A 1/4" cartridge tape drive is designed for use on small to mid-range computer systems. The tape drive was designed to back up HP fixed disks with capacities up to 132 Mbyte using one or two cartridges. The drives feature a read-after-write capability, which provides automatic data verification during the write process. Also included in the design are error correction and a media monitor. The drive can backup a 60-Mbyte disk in 30 minutes and has a 12-Kbyte buffer. Search speed is 9 ips and read/write speed is 60 ips. The cartridges are available in two capacities, 16 and 67 Mbytes. Price is \$3,500. **Hewlett-Packard**, Palo Alto, CA

**Write 227**

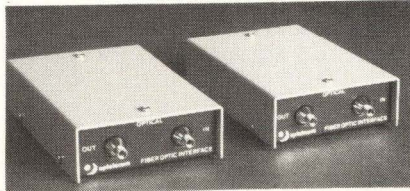
## 1/4" TAPE DRIVE

The 540S is a SCSI streaming 1/4" cartridge tape drive. The addition of the SCSI standard provides system integrators with a choice of three interfaces for the 540: the 540 with a QIC-02 compatible interface, the 540B with a QIC-36 compatible interface and the 540S with SCSI. Each of these 540 drives offers up to 60 Mbytes of data storage and formats

data to the QIC-24 specification, utilizing 1/4" tape cartridges. An optional 8" form factor package is available. **Cipher Data Products**, San Diego, CA

**Write 166**

## FIBER OPTIC LINKS



The fiber optic links are designed for Apollo Domain networks. Optical fibers replace coaxial cables, extending the range to remote workstations up to 3 kilometers. Domain's network utilizes a token ring passing structure allowing any subscriber to send information to all others by putting data in an available time slot on the ring. Optelecom's system converts the electrical signals to their optical equivalent and reconverts them at their destination. The fiber optic interface is available as a stand-alone module or a circuit card that plugs into the Optelecom Model 5000B card chassis. Price is \$650-\$700. **Optelecom**, Gaithersburg, MD

**Write 165**

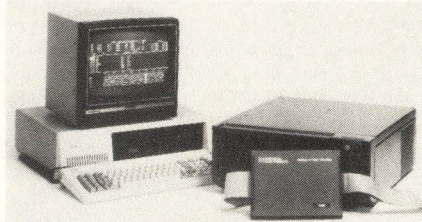
## PROTOCOL CONVERTER

The MC800 protocol converter allows 32 asynchronous ASCII devices to communicate with an IBM or-equivalent host computer using either SNA/SDLC or BSC protocols. The MC800 appears

to the host computer as an IBM 3274 or 3276 communications controller with IBM 3278/3279 terminals attached. Any mixture of CRTs and printers may be attached with automatic baud rate detection for CRTs at all speeds. Full screen mapping is performed by the MC800 and data displayed on the asynchronous terminal will be the same as an IBM. The MC800 comes in port configurations of: 5, 7, 8, 9, 12, 16, 20, 24, and 32 ASCII ports. Price is \$3,600. **Innovative Electronics**, Miami, FL

**Write 172**

## EMULATOR PORT



The KPCI is an emulator port that turns the IBM PC/XT into a universal development system for the design, test, debug and implementation of hardware and software for most microprocessor devices. The KPCI package consists of hardware and a set of development support software tools, including cross-assembler, linker, emulator software and additional CP/M utilities. For operation, the KPCI requires an IBM PC/XT with monitor and DOS. A Kontron emulator subsystem and Pascal compilers are optional. Price is \$1,500. **Kontron Electronics**, Redwood City, CA

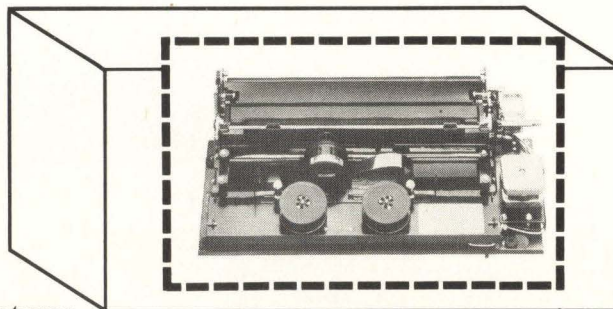
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## STREAMING TAPE DRIVE



The PCT-1000 Mainstreamer is a reel-to-reel streaming tape drive which uses 1/2" tape, stores up to 138 unformatted Mbytes per reel, and runs at 100 ips. Recording density is 800 cpi NRZI for CAD/CAM use and 1600 and 3200 cpi PE for Winchester hard disk backup. Compatible with the Cipher/Pertec interface, the Mainstreamer has three vertical and horizontal mounting options; door, drawer and desk top. A file save/restore rate of 9.6 Mbyte per minute enables data logging and data entry in key-to-tape, key-to-disk modes. Price is \$1,850. **Ibex Computer**, Chatsworth, CA **Write 162**

## 50W SWITCHING POWER SUPPLY

The OES-50 Series of switching power supplies are UL and CSA certified, and come in four models offering options of three or four regulated DC outputs. The models include the OES-50-101 (5V@8A and +/-12V@1.5A outputs); OES-50-102 (5V@8A and +/-15VA@1.5A outputs); OES-50-103 (5V@6A, +/-12V@1A and -5V@1A outputs); and, the OES-50-104 (5V@6A, +/-15V@1A and

-5V@1A outputs). The input on the OES-50 models range from 90-135 VAC, or 180-270 VAC user selected via a jumper. Features include open frame construction, soft start input, greater than one line cycle hold-up, full overcurrent protection, input EMI filter, +5V overvoltage protection, brown-out protection and typical efficiency greater than 70%. Price in quantities of 1,000 are \$53.25-\$58.00. **General Instrument**, El Paso, TX **Write 178**

## MEMORY PACKAGE

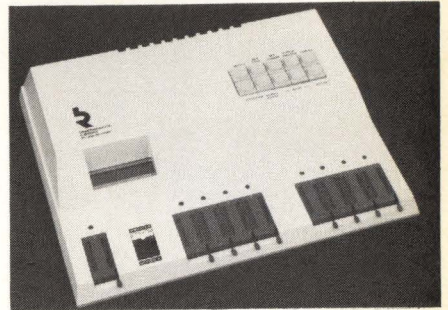
This optional memory package for Plexus P/35 super-microcomputers provides the system with an additional 145 Mbytes. The Winchester disk drive doubles the maximum storage capacity of the P/35 to 435 Mbytes by using an optional storage expansion module that holds two 145 Mbyte drives. The disk drive is available to P/35 owners as either an expansion of the current 72 Mbyte system, or as an option in an existing P/35. Price is \$27,950. **Plexus Computers**, Santa Clara, CA **Write 158**

## MEMORY AND PRINTER OPTIONS

Megatek has added memory and color hardcopy output options for its Whizzard 1600 series desktop engineering terminals. A 512 Kbyte memory expansion board is now available for both the monochrome Whizzard 1645 and the color 1650 model, to supplement the standard 128K RAM provided. An eight-color, 150 dpi color thermal printer has 640 x 480 pixel resolution and a 44 Hz interlaced interface. The Whizzard 1600 Series provide 2D or optional 3D interactive graphics concurrent with

alphanumeric capability. The 1650 features a 19" color raster monitor, 640 x 480 resolution and simultaneous display of 16 colors from a palette of 4096. **Megatek**, San Diego, CA **Write 170**

## EPROM AND EEPROM PROGRAMMER



The L800 eight gang EPROM and EEPROM programmer can program most single rail NMOS, CMOS and HMOS devices. The programmer is specifically designed for operation in a production environment and uses the algorithms as specified by Intel, AMD, Fujitsu and Hitachi. 10 separate function keys select programming functions. The L8000 is fitted with a programmable serial interface to program the 'first' device. Data can be downloaded in several MDS formats as well as between specified addresses. The L8000 tests the Intelligent Identifier codes of all relevant devices to ensure the correct device is fitted, incorporating overvoltage and overcurrent protection on all pins. **Lloyd Research**, Warsash, South Hampton, England **Write 183**

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## FLOPPY DISK SYSTEMS



The 2000 series is an intelligent floppy disk data storage subsystem with high-level data file management, 1600 Kbyte of storage, and a RS-232C interface. The standalone subsystem includes two or more 5 1/4" 400 Kbyte floppy disk drives, a disk controller and power supply. On-board firmware utilizes CP/M structured commands, operations and formats. The 2000 series includes a Da-Tech dual drive master module a dual drive expansion module, and a quad drive subsystem. Additional features include directory-controlled file allocation, file and disk copy capability in the subsystem, interchangeable 5 1/4" double-sided flexible disk, 25 system and maintenance commands to facilitate data transfer, eight baud rates up to 19.2 K, and optional 20mA current loop interface. Price is \$2,600-\$5,500. **Da-Tech**, Ivyland, PA **Write 163**

## HARD DISK SASI CONTROLLER

The DJ1100 SASI controller is designed around the industry standard SASI specifications and either one or two ST-506/412 5 1/4" fixed and/or cartridge hard disk drives. The DJ1100 features error correction, implied seek, multiple sector transfers with automatic head and cylinder switching. It has overlapped seeks, individually programmable characteristics for each drive, selectable sector size (256 or 512 bytes), buffered seek (software selectable), programmable interleave, multiple controllers (eight) per SCSI channel, and automatic retries upon error. Price is \$180. **Konan**, Las Vegas, NV **Write 159**

## C COMPILER

The C compiler is designed for the Intel 80186 family including the 80186, 80188, 8086, and 8088. It supports the microprocessor's medium addressing model, permitting programs to be written to the addressing range of 1 Mbyte of the 8086/80186. The compiler includes a Run-Time Support library, operating system interface and the capability for separate compilation and recursive programming. The compiler also offers extensions for interrupt handling and I/O statements. Price is \$5,000. **BSO**, Waltham, MA **Write 157**

## DATA ACQUISITION SYSTEM

The Macquisition is based on the Apple Macintosh and the Taurus One/05 data acquisition front-end from Taurus Computer Products. Hardware includes an Apple Macintosh with Imagerwriter printer, 16 analog input (12 bit) channels, 16 digital I/O points and a termination panel for field wiring. Software includes Microsoft Basic and Multiplan and Macquisition software. Price is \$6,600. **Small Business Computer**, Amherst, NH **Write 184**

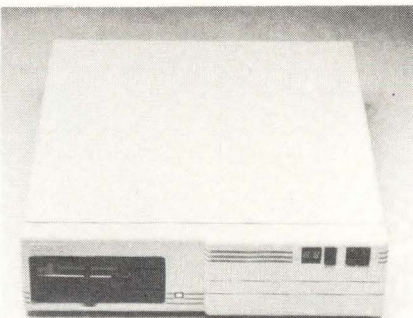
## PASCAL COMPILERS

These Pascal cross compilers are designed for the 68000 and 8086 microprocessors. The InterPas cross compilers implement the Pascal standard, including conformant arrays. A pre-processing capability supports conditional compilation as well as an include facility and an ability to define macros with or without arguments. InterPas/68000 and InterPas/8086 are compatible with InterC compiler and assembler output to allow the mixing of high level languages and assembler routines in a load module. InterPas/68000 and InterPas/8086 are source-compatible with native host compilers. Price is \$8,000. **Intermetrics**, Cambridge, MA **Write 168**

## RACAL-REDAC INTERFACE

The DI-Redac Translator is an interface translator to transfer the designs created on a DASH-I Schematic Designer to Racal-Redac's printed circuit development system. The interface eliminates the task of manually entering, and perhaps translating, design netlists. Once the schematic is transferred from the front-end IBM PC- or XT-based DASH-I, the design engineer can move on to use the fully integrated Racal-Redac CAE/CAD/CAM system, which links all phases of product development and manufacturing through a single database. Price is \$800. **FutureNet**, Canoga Park, CA **Write 174**

## 1/4" TAPE BACKUP

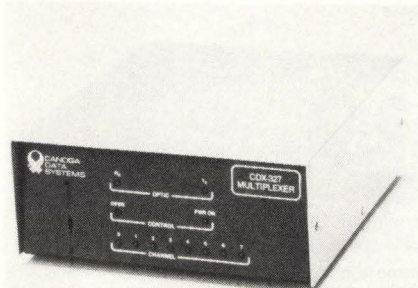


The Sponge, Model T100, is a 1/4" tape-drive subsystem with a formatted capacity of 20 Mbytes. It can backup a hard disk without using a host computer and will run like a hard disk with full random-access capability. The Sponge is positioned to provide a backup solution for HP or Bering hard disk below 100 Mbytes in capacity. It is designed for use with the Series 80, HP150, 120/125, Series 200, HP250, HP98xx desktops, and HP1000. Non-HP computers with IEEE-488 or HP-IB interface may use the device by installing special drivers. Full-streaming rate of the tape drive is 25 sec/Mbyte. A 64-Kbyte cache memory is included. Price is \$2,380. **Bering Industries**, Fremont, CA **Write 171**

## 420 CPS MATRIX PRINTER

The BP-5420 has text and graphic capabilities, includes switch-selectable characters and has a built-in, 18-Kbyte buffer. The BP-5420 features 8-pin print head and bi-directional printing at speeds up to 420 cps in draft mode, and up to 104 cps in correspondence quality mode. The built-in buffer enables the unit to accept new data while printing. The BP-5420 has 96-character ASCII set and 17 character fonts. Price is \$2,000. **Seikosha**, Cupertino, CA **Write 176**

## COAX/FIBER OPTIC MULTIPLEXER



The Eliminator is a multiplexer designed for IBM 3274 controllers. A pair of Eliminator multiplexers at the controller and terminal cluster replace 32 coax cables with one coax or fiber optic cable. A stand-alone unit supports eight terminals on one cable and modular rack mount unit can be configured to support 8, 16, 24 or 32 monitors and printers. The muxes are transparent to IBM Category A devices and in many PCM vendor 3270 systems. The Eliminator has point-to-point, multidrop or star topologies. **Canoga Data Systems**, Canoga Park, CA **Write 182**

## COLOR LIGHT PEN

The 260 HP is a color light pen designed for conditions where the illuminance is as low as 0.2 foot-Lamberts, or where the CRT phosphor persistence is considered as "medium". The 260 HP has high resolution color applications, including: interactive graphics (CAD, CAM, CAE), interactive alphanumeric, medical electronics, and industrial process control. The pen is actuated by pressing the push-tip against the CRT over the spot of light to be detected, requiring a force of less than four ounces. The polycarbonate push-tip actuator prevents marring of contacted surfaces. The pen operates from a 5V source. **Interactive Computer Products**, El Toro, CA **Write 175**

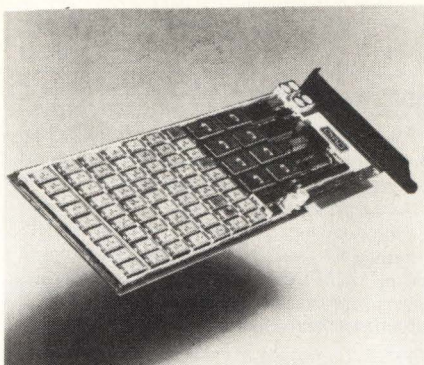
## GRAPHICS NETWORK PROCESSORS



The 45 X graphics network processors support color and monochrome remote electrostatic plotting under SNA, HASP, or ASYNC. Emulating a 377x RJE station, the 451 sends and receives EBCDIC or binary data on a SNA network using SDLC protocol. The 452 emulates a 360-20 IBM HASP workstation. The 454 handles ASYNC XON and XOFF. All use Versatec byte-parallel format for data transfers. Synchronous versions protect data integrity with 16-bit CRC-CCITT error detection and recovery. Price is \$5,000-\$8,000. **Versatec**, Santa Clara, CA **Write 181**



## ADD-ON BOARD



The PC/VRTX is an add-on board which turns the IBM PC into a real-time machine. The board is based on the VRTX Versatile Real-Time Executive made by Hunter & Ready. Plugged into an empty IBM PC slot, PC/VRTX concurrently manages and processes all tasks associated with the execution and performance of the user's application programs. PC/VRTX supports the IBM PC's DOS operating system concurrently with its real-time operating system, allowing users to access BIOS functions and perform DOS operations as tasks running under VRTX. This capability reduces the amount of programming needed to support and manage PC peripherals such as hard and floppy disks, keyboard/display, parallel and serial interfaces, and real-time clock. Price is \$1,495. **Dyad**, San Diego, CA

Write 187

## MULTIBUS BACKPLANE

The MB12 Sentinel is a 12-slot combination Multibus backplane and system monitor. The board possesses 24-bit addressing and the backplane has fifty-two LEDs and eight programmable switches. Together with the cable provided, the View Monitor can be mounted on the front panel of any system. A built-in power harness for system peripherals allows monitoring of disk voltages. The MB12 provides controlled impedance of all signal lines with ground traces between every PI signal. An integrated P2 private bus allows 24-bit addressing, as well as the use of memory expansion boards without the need for a supplementary backplane. Price is \$1,000. **Pacific Microcomputers**, San Diego, CA

Write 204

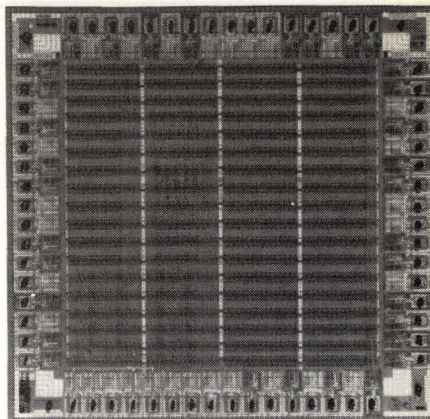
## ONSPEC CONTROL BLOCKS

Onspec Control Blocks provide the control engineer with a set of preprogrammed control blocks for implementing control strategies on personal computers. The engineer console is used to establish blocks to form control loops from fill-in-the-screen data obtainable from project engineering sources. A set of mnemonic commands permits change and display of control information. The faceplate symbol provides an operator man/machine interface. The Onspec control blocks compute feedback, feed-forward, and batch algorithms and perform status, switching, set point and failure alarming, clamping, and output function for multiple control loops.

**Heuristics**, Sacramento, CA

Write 193

## CMOS GATE ARRAYS



The Mostek GA Series of CMOS gate arrays includes four generic arrays which are: the MK GA1000D gate array with the equivalent of 1152 two-input NAND gates, the MK GA2000D with 2016 equivalent gates, the MK GA3000D with 3016 equivalent gates and the MK GA4000D with 4080 equivalent gates. The gate arrays are fabricated using the Mostek LDD/TT process, a three micron, twin-tub CMOS process utilizing double-level metal for interconnection. This process, which features 1.8 micron effective gate lengths, yields devices with typical loaded on-chip gate delays of 2.5 nsec. Price in quantities of 1,000 is \$9.30. **United Technologies**, Carrollton, TX

Write 194

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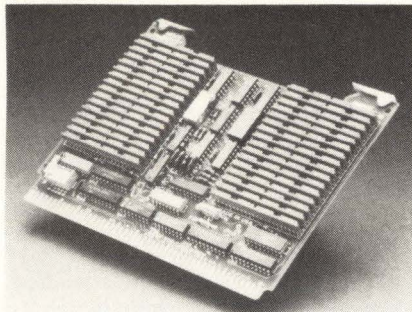


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Write 44 on Reader Inquiry Card

## NEW PRODUCTS

### ONE MBYTE MEMORY BOARD



The AM200 is a 1 Mbyte memory board for Hewlett-Packard 9000 Series 200 Computers, models 9816, 9826, 9836 and 9920. The AM200 is interchangeable with the original memory and can be used to augment or replace the original 256 Kbyte memory cards. The AM200 will fit into any available I/O slot. Up to seven memory boards can be installed in the 9826, 9836, and 9920. Two AM200 boards can be added to the 9816 and allows the user to use peripherals without an I/O expander. Price is \$2,950. **Infotek Systems**, Anaheim, CA

Write 213

### COMMUNICATIONS INTERFACE

The NS8050U is a new version of the 8050 microcontroller that has expanded communications capability via a three-wire serial communications port. The device utilizes an expanded 8048 instruction set with three I/O pins assigned to the Microwave Plus interface. This enables serial communication between two or more NS8050Us or National's line of Microwire peripherals. The NS8050U is available in both 6 MHz and 11 MHz clock speeds, and in commercial and extended temperature ranges. The NS8040U is the ROMless version of the NS8050U. Price in quantities of 100, is \$6.70. **National Semiconductor**, Santa Clara, CA

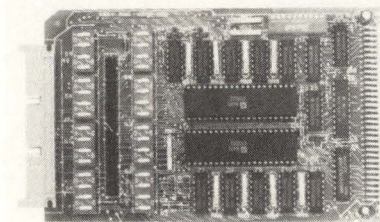
Write 201

### CMOS MULTIPLIERS

The IDT7216/7217 are 16 x 16 parallel CMOS multipliers which operate at a worst case 64 nsec clocked multiplication time and have a typical power consumption of 220mW. The IDT7216 has four independent clocks, one for each of the circuit's two input and two output registers, and the IDT7217 employs a single clock, making it suitable for pipelined microprogrammed systems. Price in quantities of 100 is \$135. **Integrated Device Technology**, Santa Clara, CA

Write 211

### BUFFERED I/O MODULE



The DBIO32 is a buffered I/O module that allows 32 relays on two Gordos or Opto 22 type boards to be added to microcomputer based systems. The Eurocard-sized module includes bank select switches which permit the addressing of external

boards in any configuration. Each I/O line can be set for input or output, with all outputs buffered. Connection is through 50-conductor flat ribbon cables. Price is \$280. **Dynatem**, El Toro, CA

Write 219

### DISPLAY CHIP SET

The Am8052/Am8152A is a display controller chip set which features a video dot rate of proportional spacing from two to 19 pixels per character, on-chip logic to support vertical or horizontal split screens, and three on-chip line buffers. The AM8052 CRT controller has on-chip, linked-list, DMA control and the Am8152A video system controller provides video path timing and control. Price is \$32-\$92. **Advanced Micro Devices**, Sunnyvale, CA

Write 209

### SERIAL INTERFACE PACKAGES

These FCC compliant asynchronous serial interface packages consist of a base module, internal cable, serial distribution board and metal bulkhead connector plate. The board provides multifunction capabilities and allows all of the signals normally used by BC05C RS-232 type cables or BC05M current loop cables, to be presented to the pins of the 25-pin RS-232 type male connector. Thus, either the RS-232 or 20 mA current loop capabilities of each board can be utilized. Transmit Data and Receive Data Signal functions can be presented to pins two and three respectively or be transposed so that a NULL modem effect is created for these signals. Price is \$460-\$585. **MDB**, Orange, CA

Write 192

### SIGNAL CONDITIONING MODULES



Six signal conditioning modules from Analog Devices, offer system users a plug-in alternative to strain gage, dynamic voltage, and power monitoring applications. The 3B18 module provides wide-bandwidth signal conditioning of strain gage sensors; the 3B40 and 3B41 offer a 10kHz isolated input capability to monitor dynamic voltages, and the 3B42, 3B43, and 3B44 offer an isolated input capability to monitor power-line voltages or currents. Designed to plug into Analog Device's 3B Series Signal Conditioning Subsystem, the modules expand the signal conditioning options for computer-based industrial measurement and control. Price is \$175-\$200. **Analog Devices**, Norwood, MA

Write 196

### Errata

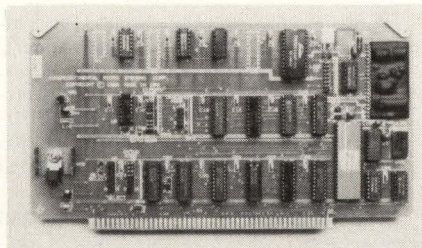
The article, "32-Bit Microprocessors Support Parallelism and Cache," which appeared in the August, 1984 issue of *Digital Design*, contained several inaccuracies relating to the Motorola 68020. The HCMOS part has 114 pins and operates at 12.5 MHz and 16.67 MHz. It has a directly addressable memory of 4 Gbytes and a three word instruction queue. We apologize for any misunderstanding.



## 128K CMOS MASK ROM

The SMM6313 is a 128K CMOS ROM which is organized as 16K  $\times$  8. The ROM uses proprietary selectox silicon gate CMOS technology and has an operating current of 16mA typical, 30mA worst case. The SMM6313 is pin compatible with 613128 and 23128 types and 27128 EPROM, which can be used for breadboarding. Price in quantities of 10,000 is \$6.22. **S-MOS Systems**, San Jose, CA **Write 208**

## S100 NETWORKS



The LANS100 is a bus compatible hardware coupled with software that combines TurboDos and ARCnet network architectures. The board meets 696.2/D1 S100 specs, features 255 nodes per network segment and provides data rates of 2.5 Mbits/sec. Using the CPZ4800X Master/File server with 16 slaves in 255 nodes makes systems for up to 4080 users possible. Both 8-bit and 16-bit processors can be accommodated on the same network. Price is \$545. **Intercontinental Micro Systems**, Anaheim, CA **Write 202**

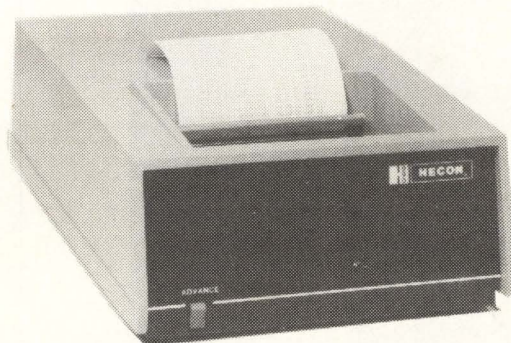
## BIPOLAR TTL PROM

The 53/63S081A is a 32  $\times$  8 bipolar TTL PROM device with an access time of 15 nsec. Power supply current is 125 mA and the output drive capability is 16 mA. The PROM features pnp inputs for low input current, three-state outputs, and full Schottky clamping, applications for the 63S081A include decoders, look-up tables, random logic replacement, and code converters. Price in quantities of 100 is \$2.98. **Monolithic Memories**, Santa Clara, CA **Write 191**

## DIGITAL SERVO

The MCC 3000 is a digital servo chip set which can control torque, speed, ramp-up, ramp-down, limits, cycle-time and all other aspects of a servo system. It includes a digital filter which stabilizes the position loop and does not require velocity feedback transducers. The MCC 300 chip set is fully programmed and commands may be generated by a host computer or it is compatible with any micro-processor. **Gaill Motion Control**, Mountain View, CA **Write 203**

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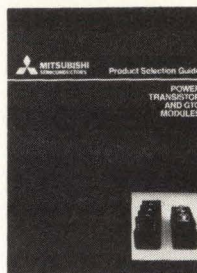
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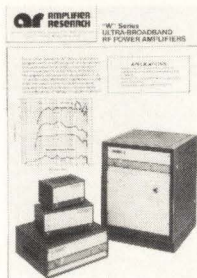
## NEW LITERATURE



**Power Transistor and GTO Modules Guide.** This 12-page guide from Mitsubishi highlights its line of power transistor and GTO modules. Described are pin connections, ratings, and outline and circuit diagrams for both products.

**Mitsubishi**

**Write 263**



**RF Power Amplifiers Data Sheet.** This four-page bulletin from Amplifier Research presents specifications of its "W" Series ultra-broadband rf power amplifiers. Covered are models that provide linear operation from 100 kHz to 1000 MHz. Features, advantages, performance specifications as well as dimensions, typical power curves, and related data are also included.

**Amplifier Research**

**Write 255**



**Service Test Brochure.** This brochure from Fairchild Service Test Systems, describes its line of automatic test equipment. Included are the 3500 Desk LSI In-Circuit Tester, 3000C Desk MSI In-Circuit Tester, 3050C Iceolator Functional Test Option, 1500 Benchtop MSI In-Circuit Tester, and accessories.

**Fairchild**

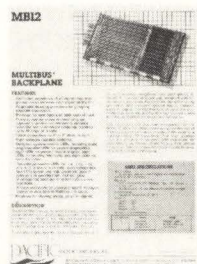
**Write 272**



**Controller Product Sheets.** This series of product sheets from General Robotics describes its family of LSI-II QBus compatible controllers, which can be integrated with DEC LSI-II CPU's and peripheral devices to create customized system configurations. The features and engineering specifications of each product are also provided.

**General Robotics Corp.**

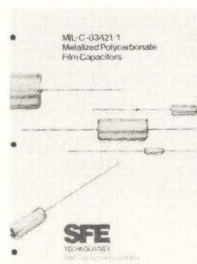
**Write 258**



**Multibus Backplane Brochure.** This brochure from Pacific Microcomputers describes its Sentinel Multibus backplane which is a systems monitor as well as a backplane. The backplane monitors systems activity, including temperature and electrical, while acting as a power harness to provide power to the disk and other system components.

**Pacific Microcomputers**

**Write 278**



**Capacitor Catalog.** This 11-page catalog from West-Cap Arizona, a subsidiary of SFE Technologies, describes its MIL-C-83421/1 metallized polycarbonate film capacitors. The catalog features complete specifications on the line of capacitors.

**West-Cap Arizona**

**Write 221**



**Disk Drive Data Sheet.** This two-page data sheet from MegaVault provides specifications and features on its 8" pram Winchester disk drive (the MVP212). Included are head positioning, drive and environmental and mechanical characteristics as well as power requirements.

**MegaVault Write 250**



**Bus Bars Application Note.** This two-page note from Rogers describes the use of Mini/Bus printed circuit board bus bars on half-height Winchester disk drives manufactured by SyQuest Technology. Included are photos, product features and application information.

**Rogers Corp. Write 260**



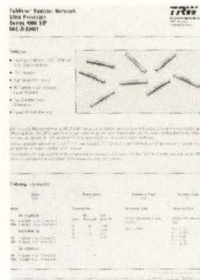
**Stepping Motor Control Cards.** This bulletin from I/O Controls Inc. describes its single-channel PPCI-X and dual-channel PPCI-XY stepping motor-control cards. Description includes programmable features and block diagrams show the circuitry and components of both cards.

**I/O Controls Write 220**



**Resistor Network Data Sheet.** This data sheet from the Resistive Products Division of TRW discusses product specifications for its 4900 Series Precision SIP resistor networks. Featured are performance data, ordering information and ratings and specifications. Outline drawings provide dimensions of the 6-, 8- and 10-pin sizes of the resistor network. A picture and schematics for each pin size are also featured.

**TRW Write 271**



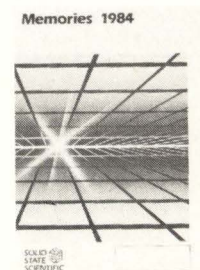
**UHF Frequency Synthesizers.** This four-page data sheet from Wavetek describes its 100 KHz to 1GHz UHF Frequency Synthesizers. Model 5155A is for use as a laboratory instrument and Model 5156A, a remote-only instrument, is intended for ATE and OEM applications. Both instruments offer sub-microsecond frequency switching when utilized in the BCD, TTL remote programming mode.

**Wavetek Write 261**



**CMOS Memories Catalog.** This 64-page catalog from Solid State Scientific, Inc. describes a family of CMOS memory devices based on a proprietary HCMOS process. Covered are low, medium and high density memories, which feature high speed and low power. The HCMOS family includes 1K, 4K and 16K static RAMs and 32K, 64K, and 128K and 256K ROMs.

**Solid State Scientific Write 252**



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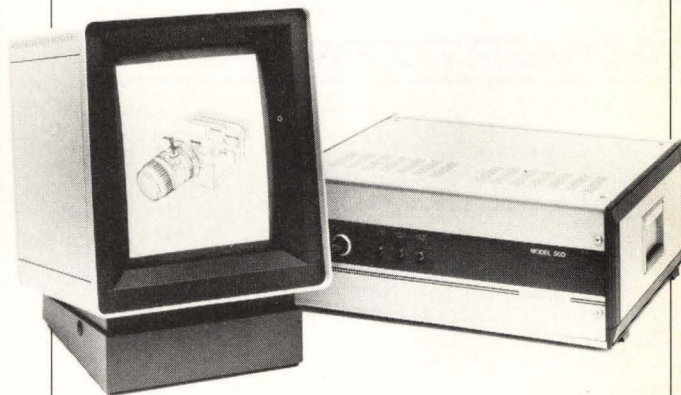
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Write 60 on Reader Inquiry Card



## October 30-November 1

**International Test and Measurement Exhibition and Conference '84 (ITAME).** London, England. Contact: Network Events Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, England. Tele. Buckingham (0280) 815226.

## November 4-8

**The Second International Congress on Advances in Non-Impact Printing Technologies.** Arlington, VA. Contact: Society of Photographic Scientists and Engineers, 7003 Kilworth Lane, Springfield, VA 22151. (703) 642-9090.

## November 6-10

**Intelligent Robots: Third International Conference on Robot Vision and Sensory Controls.** Cambridge, MA. Contact: The Society of Photo-Optical Instrumentation Engineers, PO Box 10, Bellingham, WA 98227. (206) 676-3290.

## November 7-8

**IEEE Workshop on Languages for Automation.** Chicago, IL. Contact: Shi-Kuo Chang, Dept. of EE, Illinois Institute of Technology, ITT Center, Chicago, IL 60616. (312) 567-3401.

## November 7-9

**24th Annual Symposium on Foundations of Computer Science.** Tucson, AZ. Contact: Paul R. Young, TE021, Electrical Engineering and Computer Science Dept., Evans Hall, University of California, Berkeley, CA 94720. (415) 642-1024.

## November 7-9

**Networking Personal Computers.** Hasbrouck Heights, NJ. Contact: Data-Tech Institute, PO Box 569, Nutley, NJ 07110. (201) 661-2300.

## November 7-9

**Joint Airforce - Industry Electronics Manufacturing Productivity Conference.** Charleston, SC. Contact: The Electronic Systems Div., Hanscom Air Force Base, Charleston, SC. (703) 536-8660.

## November 7-11

**Compsac 83, The IEEE Computer Society's Seventh International Computer Software and Applications Conference.** Chicago, IL. Contact: Compsac 83, PO Box 639, Silver Spring, MD 20901. (301) 589-8142.

## November 7-11

**Iecon 83, Ninth Annual Conference on Industrial Electronics (IEEE et al.).** San Francisco, CA. Contact: LeRoy Bushart, ESD Corp., 600 Meridian Ave., San Jose, CA 95126. (408) 280-2593.

## November 8-11

**Chicago Computer Showcase Expo.** Chicago, IL. Contact: The Interface Group, Inc., 300 First Ave., Needham, MA 02194. (617) 449-6600.

## November 8-11

**Wescon and Mini/Micro West (IEEE et al.)** San

Francisco, CA. Contact: Electronic Conventions, Inc., 8110 Airport Blvd., Los Angeles, CA 90045.

## November 8-11

**Philadelphia Computer Showcase Expo.** Philadelphia, PA. Contact: The Interface Group, Inc., 300 First Ave., Needham, MA 02194. (617) 449-6600.

## November 13-16

**Computer Graphics.** Los Angeles, CA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

## November 14-16

**Data Communications.** Chicago, IL. Contact: Software Institute of America, Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

## November 21-26

**China International Microelectronics/Computers Exhibition and Conference.** Shanghai, People's Republic of China. Contact: Harry Lepinske, American Exhibition Services International Inc., PO Box 66373, O'Hare International Airport, Chicago, IL 60666. (312) 593-2462.

## November 28-30

**UNIX Application Forum.** Los Angeles, CA. Contact: Yates Ventures, 4962 El Camino Real Suite 111, Los Altos, CA 94022. (415) 964-0130.

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