A CAHNERS PUBLICATION

JUNE 22, 1989

EDN®

Modular logic analyzers let you upgrade easily

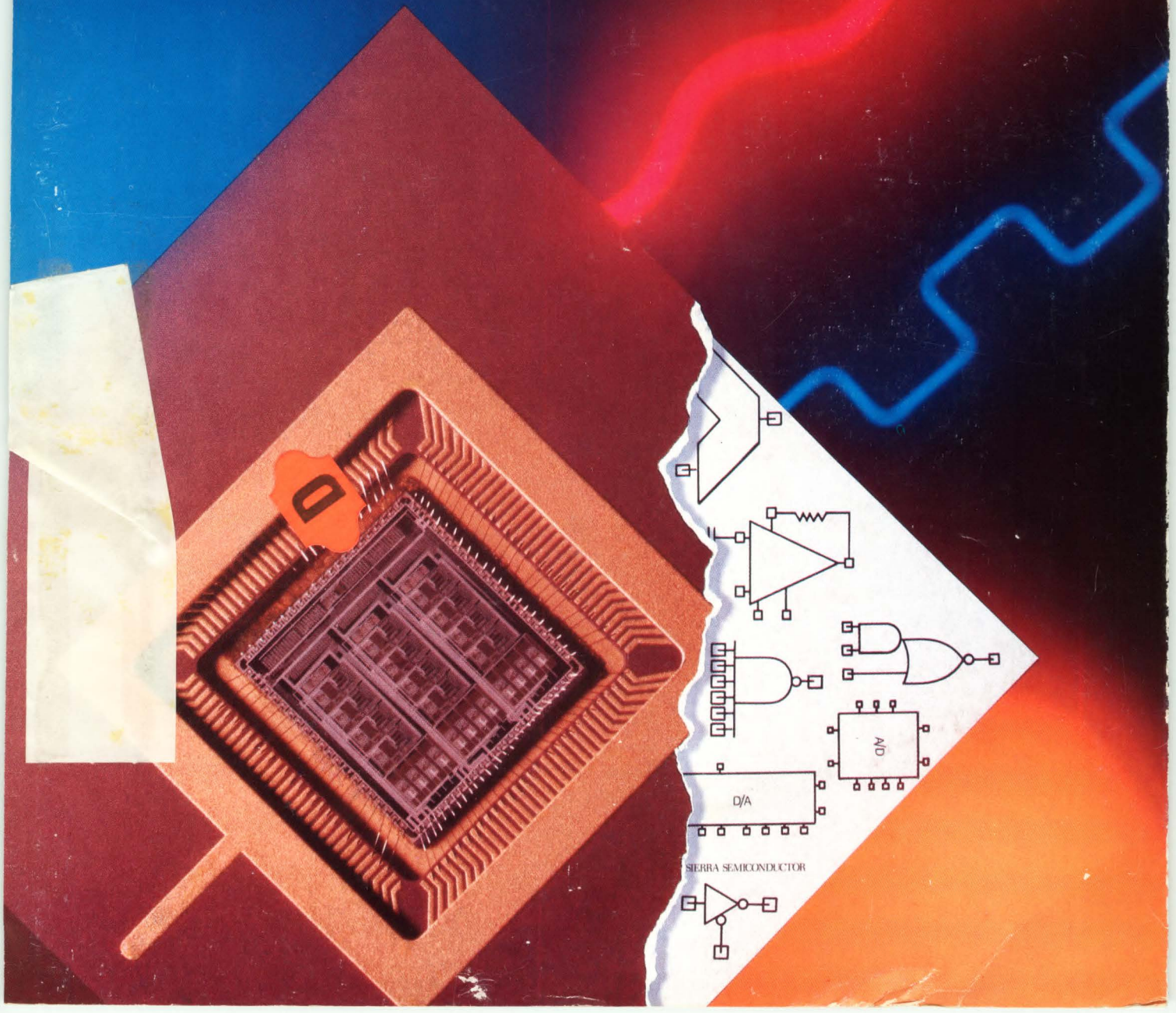
16- and 32-bit bus extensions

Heeding thermal effects helps ensure circuit reliability

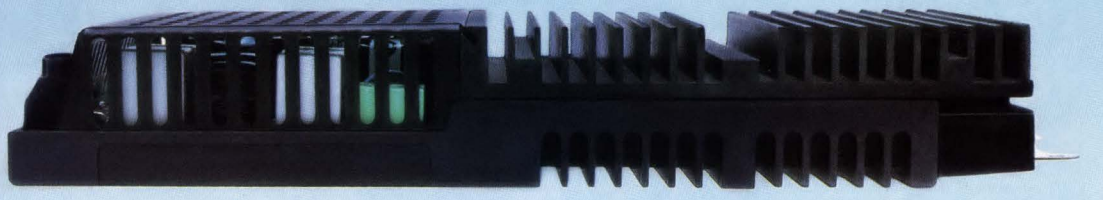
Delta modulators simplify A/D conversion

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

ASICs mix analog and digital functions for high integration



FLATPAC



In Off-Line Switchers.

take care of even your most unusual voltage requirements. For special requirements, outputs as low as 2 Volts, and as high as 95 Volts can be provided.

And you don't give up features to get FlatPAC's advantages: besides being trimmable, all FlatPAC outputs have remote sensing and overvoltage and overcurrent protection. Individual FlatPAC outputs are totally isolated: there are no cross regulation issues; any output can be positive or negative; and output returns can float up to 500V, rms, apart. FlatPAC's run on either 110 or 220 Volt lines, meet "Class A" interference specs, have built in fusing, and conform to UL, CSA, and TUV safety agency requirements. Two and three cell units also provide two isolated, sequenced, logic outputs to indicate pending loss-of-line and pending loss-of-output for system housekeeping during power cycling or brownouts.

The key to FlatPAC's flexibility and power density is Vicor's VI-200 family of high density, high efficiency, UL, CSA, and TUV recognized, component level DC-DC converters. When you specify a FlatPAC, you benefit from the field reliability and predictability that's been established in an installed base approaching half a million units.

Join The Celebration Now

Call Vicor now to discuss your special needs...you'll be celebrating when you find how quickly Vicor can ship you the smallest, most efficient, most cost effective solution to your power system requirements...at prices as low as 85¢/Watt in OEM quantities.

To Receive A Complete Catalog, Including Information On Vicor Products, Applications And Accessories, Call Vicor Today At (508) 470-2900, 23 Frontage Road, Andover, MA 01810.

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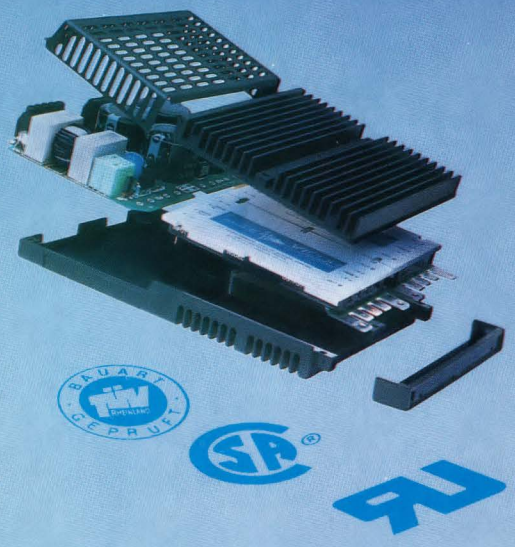
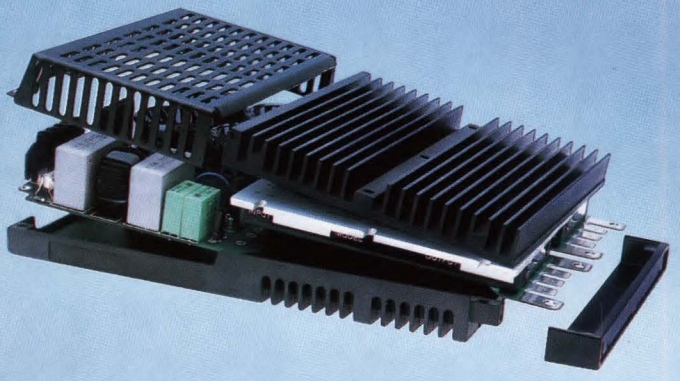




Celebrating The New Profile

Introducing the FlatPAC™ ... Vicor's Family of User Definable, Multiple Output, Switching Power Supplies

Until now, your power system decision meant choosing between costly and unpredictable custom development, or bulky and inflexible catalog supplies...or you had to design and manufacture it yourself. Taking the next step in the power-component revolution, Vicor introduces FlatPAC, the user-definable, "off-the-shelf" alternative to customs that's economical from single units to OEM quantities...and which fits in a fraction of the space required by conventional off-line supplies!

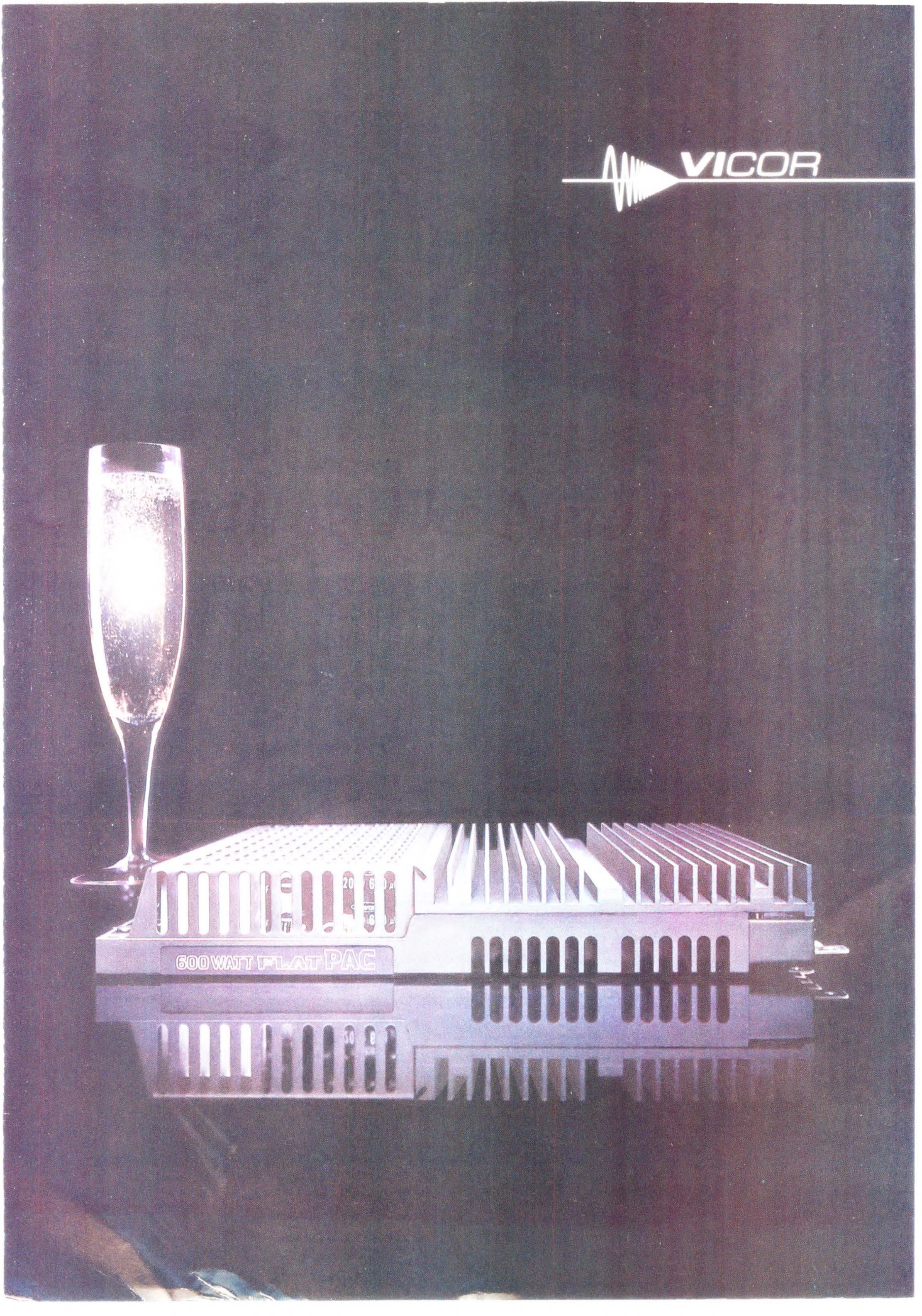
The Off-The-Shelf Alternative

FlatPAC's unique modular design allows Vicor to provide next day delivery on over 10,000 different FlatPAC configurations. You define your power requirements... Vicor does the rest – while eliminating the non-recurring costs, unpredictable lead times, risk, inflexibility, and reliability uncertainties associated with conventional solutions. No other power product offers FlatPAC's combination of power density, economy, and "off-the-shelf" flexibility!

Power Cells

Sharing a distinctive, space saving flat package profile (1.37" high x 8.6" long), FlatPACs come in widths of 2.5", 4.9", and 7.4", and supply up to 200, 400, and 600 Watts of total output power...an unprecedented 7 Watts per cubic inch in an off-line switching power supply!

The three different packages provide one, two, or three user definable "Power Cells". Each Power Cell may be specified to be an independent, isolated output with a power rating of 50, 75, 100, 150, or 200 Watts, or cells may be combined to form higher power outputs...up to 600 Watts from a single output. Standard output voltages are 5, 12, 15, 24, and 48 Volts – and because all FlatPAC outputs are field trimmable down to zero and up to 110% of nominal, a standard output can likely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600 WATT FLAT PAC

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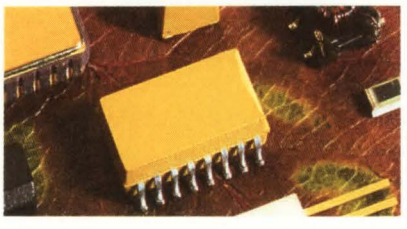

Partnering with Dale gives you broad compatibility with automatic placement equipment and standard soldering methods, plus ship-to-stock capability assured by strong emphasis on statistical process control.

For complete information, call: **Thick Film Resistor Networks, Thermistors:** 915-592-3253; **Thin Film Networks, Thick/Thin Film Chips:** 402-371-0080; **Wirewound Resistors:** 402-563-6283; **Chip Potentiometers, Oscillators:** 602-967-7874; **Inductors, Transformers:** 605-665-9301.

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CIRCLE NO. 1

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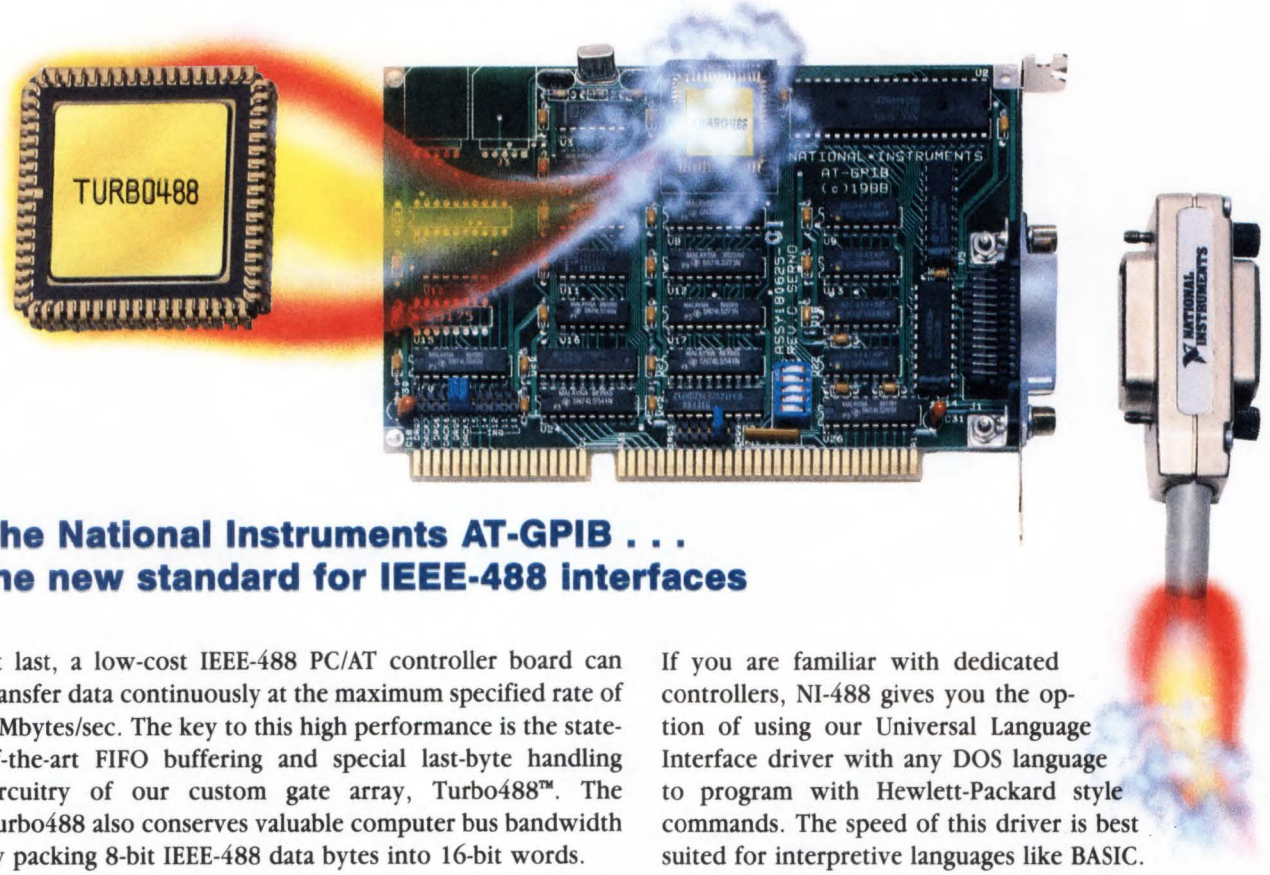
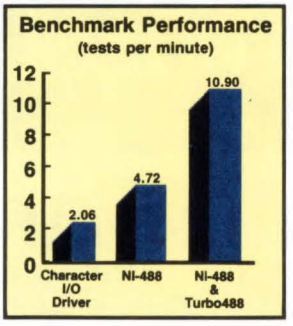


The National Instruments AT-GPIB . . . the new standard for IEEE-488 interfaces

At last, a low-cost IEEE-488 PC/AT controller board can transfer data continuously at the maximum specified rate of 1 Mbytes/sec. The key to this high performance is the state-of-the-art FIFO buffering and special last-byte handling circuitry of our custom gate array, Turbo488™. The Turbo488 also conserves valuable computer bus bandwidth by packing 8-bit IEEE-488 data bytes into 16-bit words.

By moving time consuming software functions into hardware, the Turbo488 significantly reduces the overhead of a software driver too. The combination of the AT-GPIB and our streamlined software driver gives you the power needed for today's high speed digitizers.

The AT-GPIB is controlled by the *de facto* industry standard NI-488 software. NI-488 has high-level routines that transparently handle IEEE-488 protocol and buffered DMA transfers. These routines can be used with any popular language and are the perfect match for the structured, hierarchical programming style preferred by users of high-speed, compiled languages such as C and Pascal.



If you are familiar with dedicated controllers, NI-488 gives you the option of using our Universal Language Interface driver with any DOS language to program with Hewlett-Packard style commands. The speed of this driver is best suited for interpretive languages like BASIC.

Your investment in National Instruments is a sound one. You can still run your existing NI-488 programs yet automatically take full advantage of the Turbo488. If you're just getting started, our interactive instrument control and menu-driven configuration utilities will get you up and running in no time.

Your relationship with National Instruments does not end when you purchase our products. A staff of applications engineers is always a free phone call away. Demand the best IEEE-488 controller available . . . give us a call today at **(800) IEEE-488.**

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Turbo488 technology is standard on our boards for Micro Channel and Macintosh computers

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SPECIFICATIONS

	TOSW-230DR ZFSW-230DR		TOSW-425DR ZFSW-425DR	
Freq. Range(MHz)	10-3000		10-2500	
Insert. Loss (dB)	typ.	max.	typ.	max.
10-100MHz	1.3	1.7	1.3	1.7
100-1500MHz	1.1	1.7	1.1	1.7
1500-3000MHz	1.8	2.5	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	30	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ.	max.	typ.	max.
	1.3	1.6	1.3	1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
Oper. Temp.(°C)	-55 to +100		-55 to +100	
Stor. Temp.(°C)	-55 to +100		-55 to +100	
Price (10-24)	$39.95		$59.95	
(1-9)	$89.95		$109.95	

10 to 3000MHz from $39.95

Now, high-speed, high-isolation switches with with built-in drivers, tough enough to pass stringent MIL-STD-202 tests. There's no longer any need to hassle with the complexities of designing a TTL driver interface and then adding yet another component to your subsystem... it's already included in a rugged, low-cost, compact assembly. Available in the popular hermetically-sealed TO-8 package or a small EMI-shielded metal connectorized case, these tiny PIN-diode reflective switches, complete with driver, can operate over a 10 to 3000MHz span with a fast 2μsec switching speed.

Despite their small size, these units offer isolation as high as 40dB(typ), insertion loss of only 1.1dB(typ), and a 1dB compression point of +27dBm over most of the frequency range. All models are TTL-compatible and operate from a dc supply voltage of 4.5 to 5.5 V with 1.8mA quiescent current. Switch to Mini-Circuits for highest quality innovative products... and leave the driving to us.

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2.5KHz to 500MHz 250mW only $199

POWERFUL up to +23dBm undistorted output

FLAT within 1dB over the entire band. 2.5KHz to 500MHz

UNCONDITIONALLY STABLE regardless of load

DAMAGE-RESISTANT built-in voltage regulator; supply voltage 24V, 0.35A

RUGGED operates from −55 to +85° C, withstands shock and vibration, ground equipment

COMPACT only 3.75 by 1.8 by 2.6 in.

Packed with these super performance features, 22dB flat gain and a typical VSWR of 1.3 to 1, the ZHL-6A amplifier is ideally suited for your latest broadband systems designs. And where space is critical, its height can be cut in half, to only 0.9 in., by removing the heat sink and attaching the unit to your chassis.

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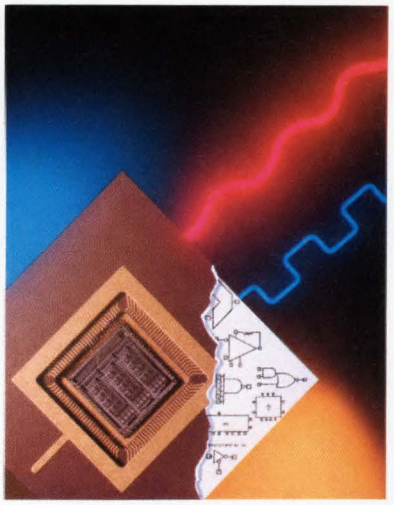
Volume 34, Number 13 June 22, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Recent findings in mixed analog-digital ASIC technology have uncovered a wide variety of circuit-design options for your high-integration needs. See the Special Report, beginning on pg 146. (Photo courtesy Sierra Semiconductor; concept and photography by Imagination)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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CG08903

Continued from page 5

***Modular logic analyzers** give you the flexibility to buy only as much instrument as you need now; you can upgrade later without losing your original investment (pg 73).*

TECHNOLOGY UPDATES

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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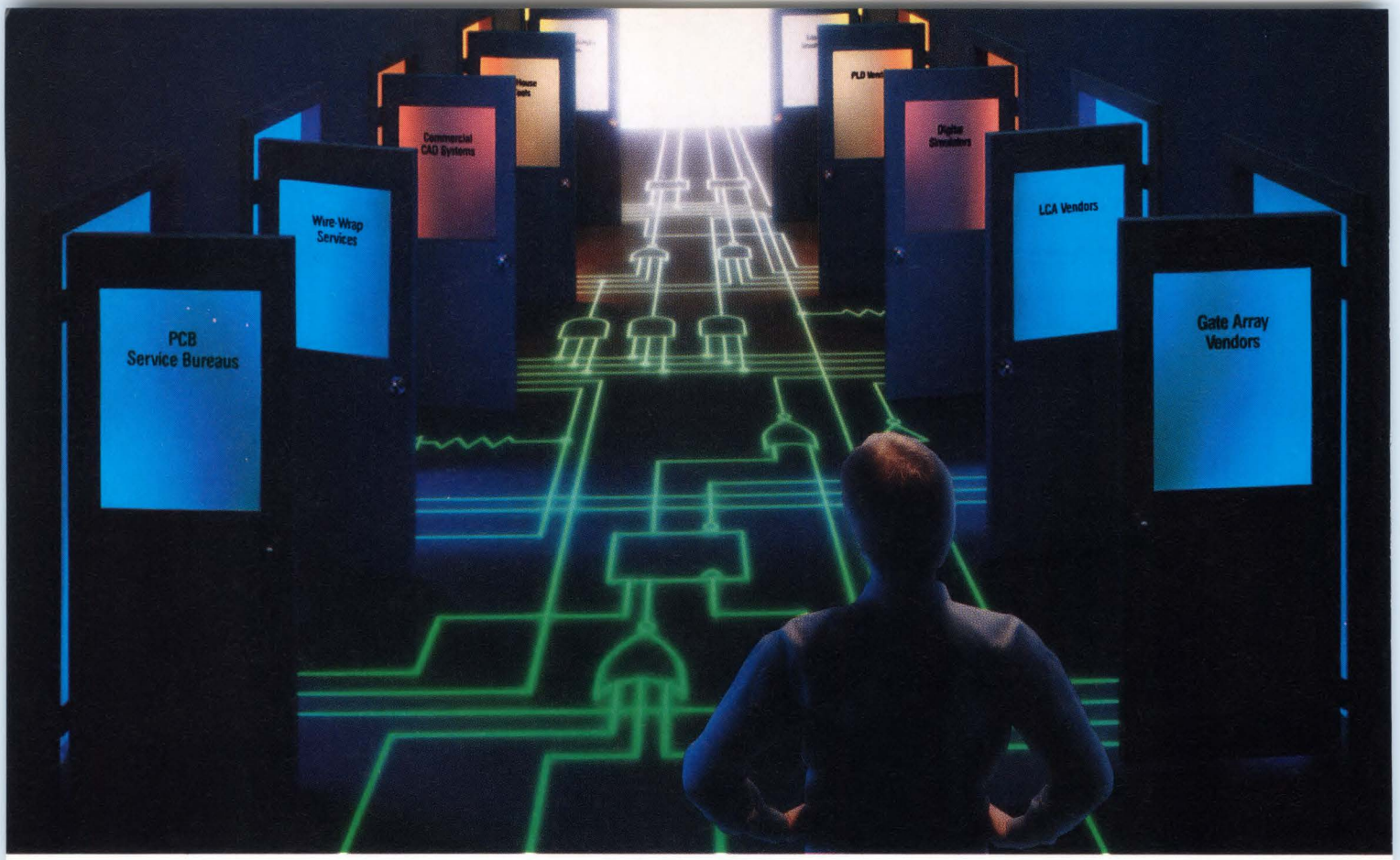

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EDITORIAL

Recent press coverage of cold-fusion experiments shows that few reporters understand how science really works.

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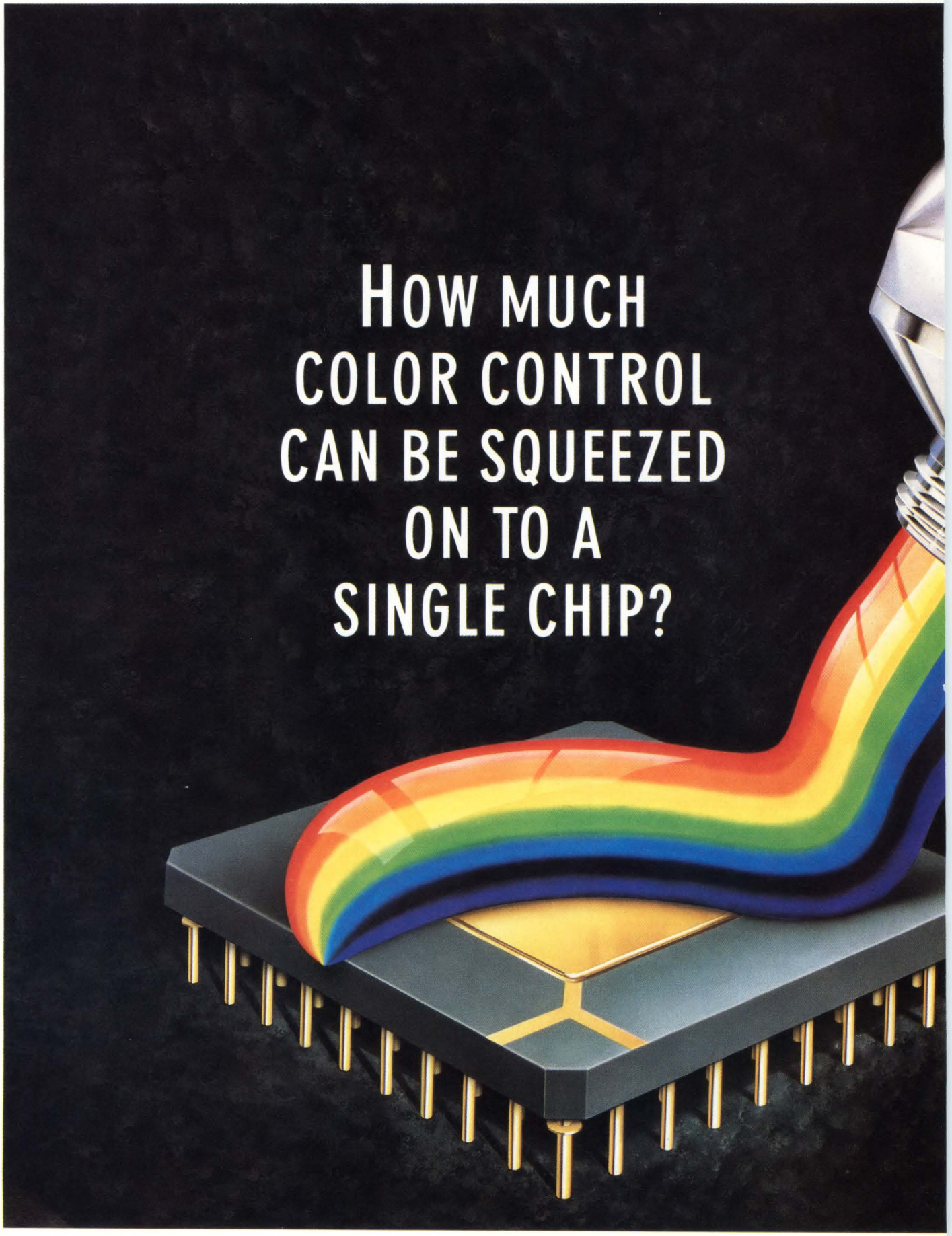
G300 CVC • PROGRAMMABLE VIDEO TIMING GENERATOR • COLOR LOOK-UP TABLE •



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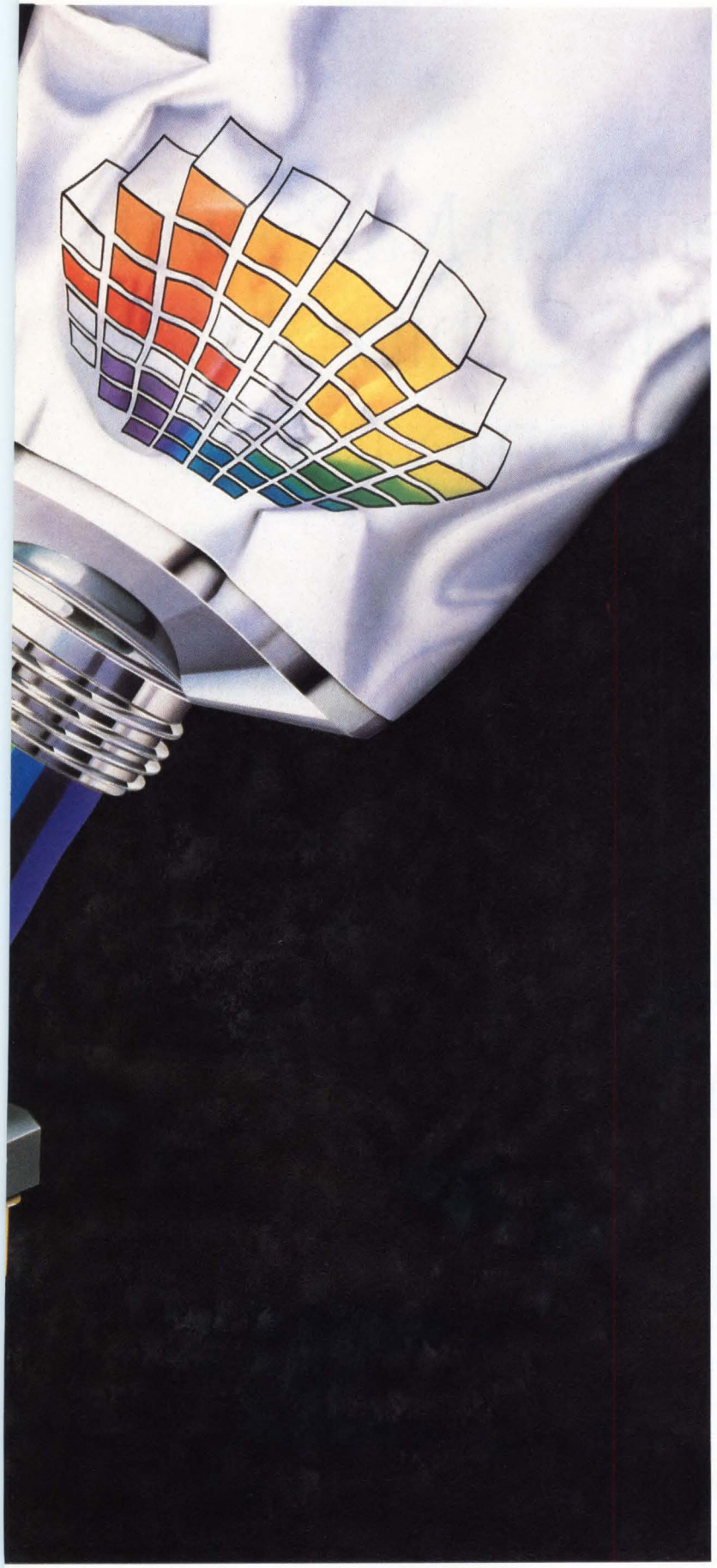

If the chip in question is the new IMSG300 Color Video Controller (CVC) from INMOS, the answer is quite simply, "all of it".

Through high integration, INMOS has combined total graphics control and data conversion onto a single 84 pin device. This includes a color look-up table, programmable video timing generator, full bitmap management, triple 8-bit video DACs and a phase-locked loop.

Because the IMSG300 is programmable, it is easily interfaced to any processor or monitor that may be used in your system. The G300 promotes the technique of using software drawing algorithms as opposed to designing them in hardware. This dramatically reduces design-in time and allows for easy upgradability.

The IMSG300 also provides an optional 24-bit pixel mode for full color as well as pseudo color, an on-chip phase-locked loop for generating all high frequency clocks, and a 32-bit multiplexed pixel port for achieving pixel rates up to 110MHz.

Only the INMOS G300 CVC gives you all the options you need to tailor inmos your systems exactly the way you want them – both now and in the future.

The INMOS G300 CVC single chip solution. Find out more today.

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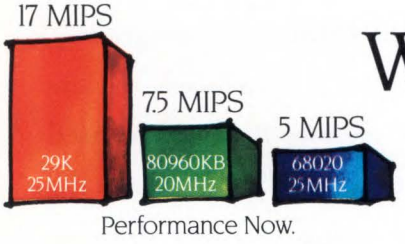

ANSI C optimizing compiler by Metaware. Assemblers by Microtec. Architectural simulators. Hardware debug module by Step Engineering.

Advanced Mic

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And half the price you'd expect to pay for electrostatic performance.

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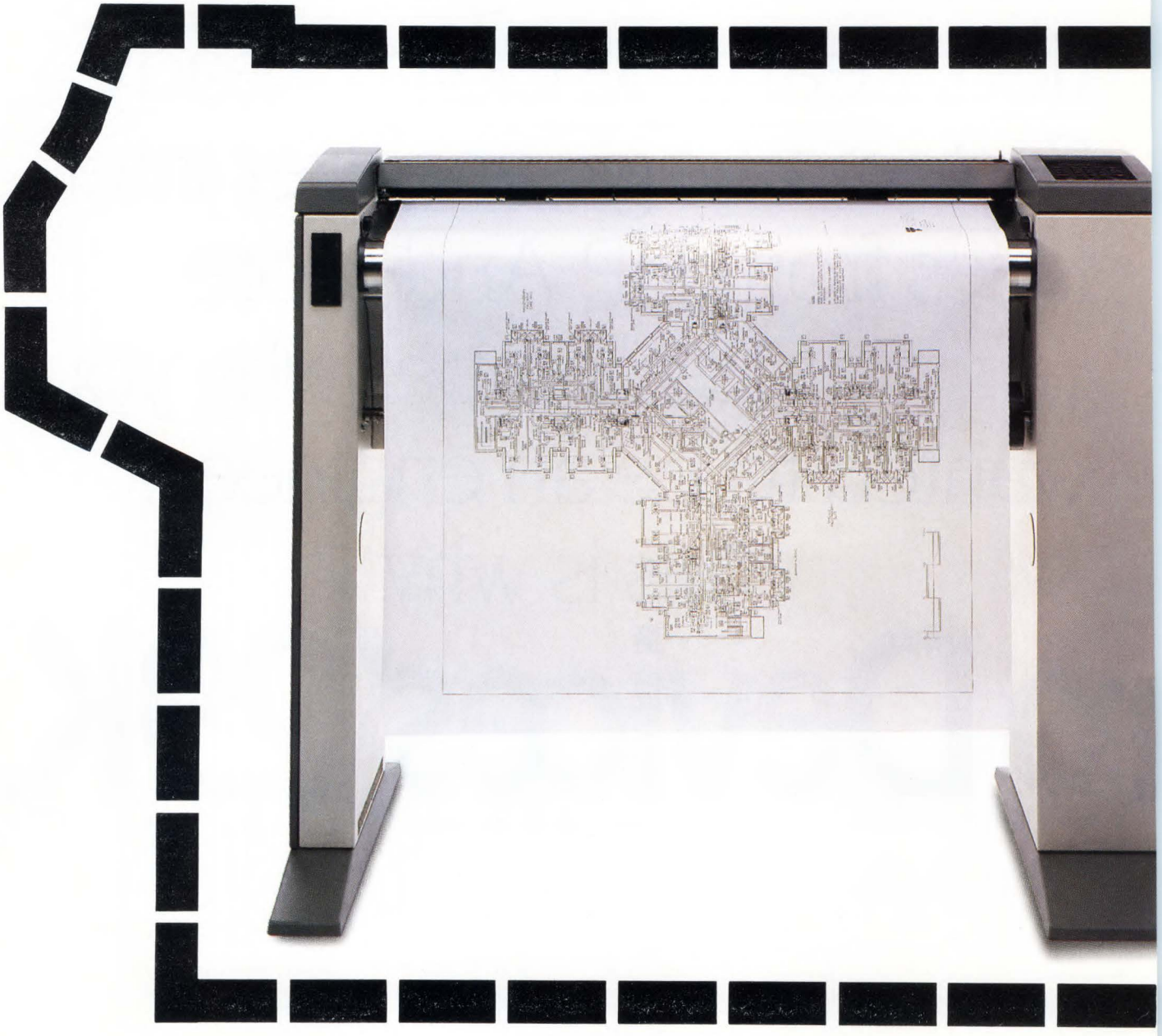
And while squeezing down the size of our plotters, we managed to squeeze out a lot more performance. By teaming a lightning-fast 68020 32-bit microprocessor with a unique page buffer, data processing time is virtually eliminated, freeing your computer to do other tasks.

Reprints are a revelation too. You can generate up to 999 reprints without re-transmitting or re-rasterizing plot data. So your computer is



announces electrostatic plotters.

freed-up immediately for other projects.

Also note that our transfer speed is the industry's fastest. 38.4K baud rate over a serial RS232C interface. And even faster with a Centronics interface. Compared to pen plotters, that means 6-20 times the throughput.

Now that's fast. But the 8500 Series is easy to handle as well. Media loading is up front. No more going behind the plotter to load.

Starting up is easy. You simply plug in the system and it's ready to plot. A unique user-friendly keypad takes anyone through the plotting process quickly, easily and in plain English. And a built-in micro-floppy drive saves even more time by storing plotter setups and interfacing configurations on-disk. Which means no more time-consuming setups.

The 8500 Series is also the first plotter that's literally ready-to-roll.

Because its built-in casters let you move quickly to any location for sharing. You can also share through networking with a plot server. And at a quiet 55 db, the 8500 can work anywhere without disturbing anyone's concentration.

With optional features the 8500 also automatically cuts and winds plots. Up to 999 copies, overnight, completely unattended if you want. And it's available in both 400 and 200 ppi resolution, in either 24" or 36" formats.

You also get full support for 906/907 and HP-GL pen plotter data formats. So designers have the freedom to use virtually any major CAD package they choose.

Incidentally, the same technology that reduces the size of the 8500 also makes it more reliable. Three to four times more so than the industry standard. Which means you'll have little need for our service personnel. Still, it's nice to know that we offer the most comprehensive service and support in the world. All over the world.

For more information on our 8500 Series, call our toll-free number now: (800) 538-6477; in California, (800) 341-6060.

But do it now. Because choosing any other electrostatic plotter could have drastic consequences for your budget.

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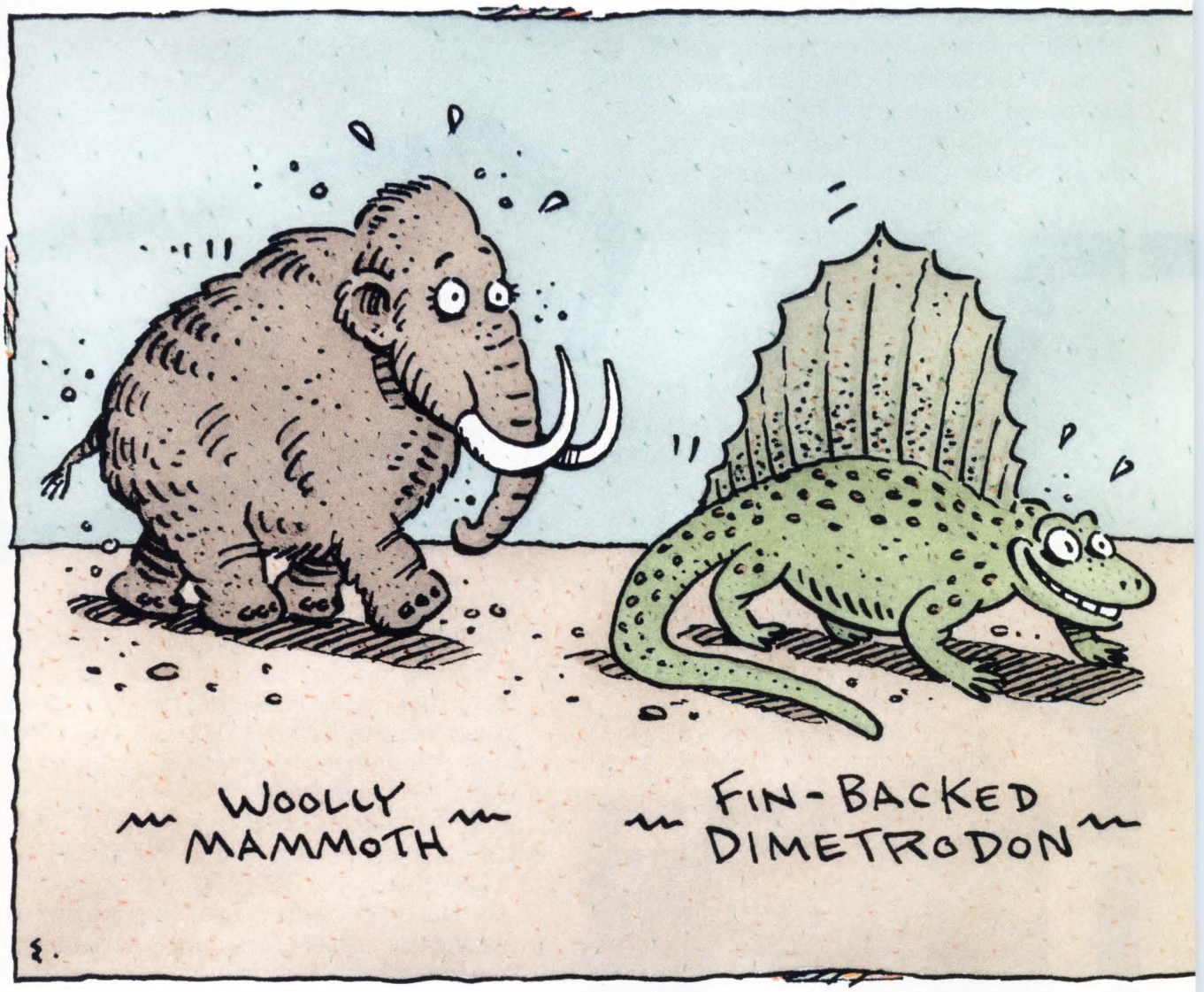
A SLOW FIF



When you're too slow, you don't last long.

Dinosaurs didn't make it, the woolly mammoth didn't make it, and the dodo bird didn't make it.

Up until now, for high-performance applications FIFOs haven't made it either. Because they haven't been fast enough to do the job.

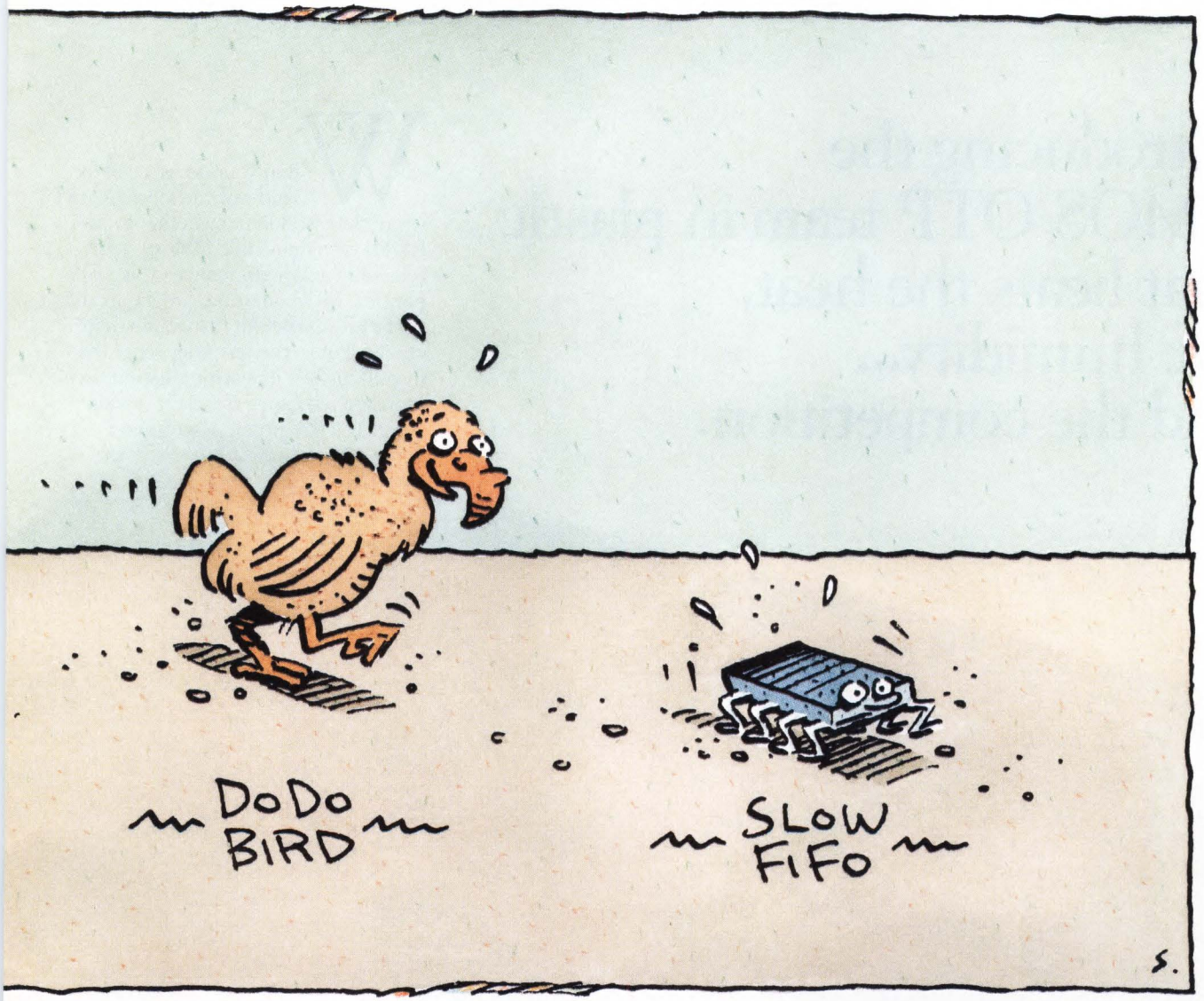
THE FASTEST FIFOs MADE.

Part Type	Org.	Speeds	Packages
KM75C01A	512x9	20, 25, 35, 50, 80 ns	28-pin DIP 32-pin PLCC
KM75C02A	1Kx9	20, 25, 35, 50, 80 ns	28-pin DIP 32-pin PLCC

Samsung's Fantastic FIFOs™ change that. In speeds now up to 20 ns, they're the fastest ever made.

Which means that in areas like parallel processing, where designers have had to use fast static RAMs because FIFOs were too slow, you can now get the speed you need in a FIFO.

O, IS NO FIFO.



Our Fantastic FIFOs are in the ×9 organization, they're in CMOS, and we now have them in both DIP and PLCC surface-mount packaging.

Equally good news: in areas where you need a *lot* of FIFOs, like large networks and even mini-supercomputers, you can now get the *pricing* you need.

All in all, Samsung's Fantastic FIFOs, once and for all, fulfill the *promise* of FIFOs.

Because a slow FIFO is no FIFO, and these parts make *that* problem go away.

For pricing and data sheets on the fastest FIFOs in the world, call 1-800-669-5400 or 408-434-5400 now. Or write to FIFO Marketing, Samsung Semiconductor, 3725 No. First Street, San Jose, CA 95134.

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When your designs call for read-only memories, don't waste time wondering whether to use ROMs or ceramic EPROMs to assure reliability and performance. Make TI's plastic CMOS one-time-programmable (OTP) PROMs your first-round draft choice. Put to the test, they score the overall highest marks for reliability and moisture resistance (*see chart opposite page*). You'll maintain your system performance plus realize significant system savings.

STIC OTP PROMs

Our chips sport the right equipment

TI solved the moisture problem with innovative multilevel oxide and double-layer passivation oxide processes. The result is an overcoat which protects the chips from contamination and corrosion. The test results speak for themselves.

It's only natural that TI should come up with the solution to an industry-wide problem. After all, we were a pioneer in plastic packaging. We have more than 25 years of experience in this packaging technology, and we are the largest U.S. supplier of plastic DRAMs.

Big scores on savings

Our OTPs in plastic packages can save you money in more ways than one.

If your design calls for high volumes, say 5,000 to 10,000 or more a month, the savings with plastic quickly mount up to a sizable figure.

Independent research shows that about 85% of all EPROMs are only programmed once. So if you are presently specifying ceramic EPROMs for their reliability, chances are you are paying for more programmability than you need. Specify our OTPs and save.

Another savings: Our plastic OTPs (32K to 512K) in DIPs and space-saving surface-mount PLCCs can be used with automatic insertion equipment to improve manufacturing throughput and efficiency.

Whichever package you choose, our CMOS OTPs are direct replacements for EPROMs in like packaging and are pin- and upgrade-compatible with mask-programmed MOS ROMs.

TI VS. COMPETITOR OTPs MOISTURE RELIABILITY COMPARISON
(PERCENT DEFECTIVE AT HOURS OR CYCLES)

TEST	HOURS OR CYCLES	TI PC256 (CMOS)	A P256 (NMOS)	B P256 (NMOS)	C P256 (NMOS)	D P256 (NMOS)	E P256 (NMOS)
85°C/85% Humidity Moisture Test	1,000 Hours	0.0%	5.0%	0.0%	14.0%	1.0%	2.0%
Pressure Cooker Test	240 Hours	0.0%	32.5%	0.0%	26.0%	10.0%	0.0%
–65°C to 150°C Temperature Cycle	1,000 Cycles	0.0%	2.5%	24.0%	12.0%	92.0%	6.0%

Grueling heat and humidity tests prove the high reliability and superior moisture resistance provided by a proprietary plastic and wafer protective overcoat system used in TI's OTPs. Devices tested were TI 256K CMOS OTPs and 256K NMOS OTPs from five other leading U.S. and Japanese manufacturers.

No trades on performance

Performance of our high-speed, one-time-user-programmable PROMs is comparable to that of NMOS counterparts. Because these are CMOS devices, power dissipation is very low, reducing power-supply burden and enhancing chip reliability.

Quick programming at your home base

You can quickly program our OTPs in-house to any code you like.

In fact, TI's new SNAP! Pulse algorithm speeds you through programming in less than one-tenth the time of earlier algorithms. For example, you can program one of our 256K OTPs in less than four seconds compared to the 132 seconds required by earlier algorithms.

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Three year warranty	Three year warranty	True rms ac
		1 ms PEAK MIN MAX
		4½ digit mode
		Back lit display
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The new Fluke 80 Series shown actual size

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FLUKE

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

FLOATING-POINT COPROCESSOR AVAILABLE FOR THE 80486

Weitek Corp (Sunnyvale, CA, (408) 738-8400) has introduced a floating-point coprocessor for the Intel 80486. Named the Abacus 4167, the coprocessor delivers 17M Whetstones in single precision when running at 25 MHz. It offers 16 64-bit data registers and a 64-bit floating-point data path, and it completes a double-precision addition in 80 nsec when operating at 25 MHz. The device is memory mapped—it appears as a block of memory to the host processor—and is easy to incorporate into a 80486-based system: System designers can connect the appropriate signals to a 142-pin pin-grid-array socket for the later addition of the coprocessor.

The device is upwardly binary compatible with the Abacus 3167 floating-point processor, thus allowing existing 3167 applications to be run without modification. The coprocessor costs $565 (1000); samples will be available in September.
—Richard A Quinnell

POWER-FACTOR CORRECTOR BOOSTS POWER UTILIZATION

The ML4812 power-factor controller from Micro Linear (San Jose, CA, (408) 433-5200) lets you get the most from your wall outlet. The phase difference between the voltage and current in an ac circuit causes the actual power available to be less than the maximum. This device controls the current drawn by your power supply to match its phase and waveform to the supply voltage's phase and waveform. The result is near optimum use of ac power: 99% utilization. The device comes in a 16-pin DIP or 20-pin plastic chip carrier and costs $5.95 (100).
—Richard A Quinnell

ECL RISC PROCESSOR OPERATES AT 80 MHz

Bipolar Integrated Technology (Beaverton, OR, (503) 690-1498) has introduced the B5000 RISC-processor chip set. This chip set implements a SPARC-based processor in ECL and operates with a clock frequency of at least 80 MHz, thus achieving a performance of 50 to 65 MIPS. The device features a double-word-wide cache interface, which enables the processor to read double-precision data in a single clock cycle. The 6-chip set comprises a processor, a floating-point controller, two register files, and a 2-chip floating-point unit. The set costs $3300 (100) and is in sample production. Full production is scheduled for the first quarter of 1990.
—Richard A Quinnell

FRAMEWORK GIVES TOOL AND ASIC-VENDOR INDEPENDENCE

Giving you the freedom to pick and choose both your CAE tools and the vendor you want to fabricate your ASIC, Motorola's (Chandler, AZ, (602) 821-4426) Open Architecture CAD System (OACS) is a technology-independent CAD system for ASIC design. Available on both Apollo and Sun workstations, OACS is a framework that lets you plug in design tools from third-party vendors: You can connect synthesis tools, simulators, timing analyzers, automatic-test-pattern-generation (ATPG) software, floor planners, and chip-layout packages. A framework gives you the opportunity to customize your design system and to upgrade and update either as your needs grow or as new tools become available. EDIF (Electronic Data Interchange Format) provides the industry-standard window into the OACS. In addition to giving you flexibility to change CAE tools, the OACS also provides fabrication-vendor independence. The OACS currently supports third-party tools from Mentor Graphics

(Beaverton, OR), Valid Logic Systems (San Jose, CA), EDA Systems (Santa Clara, CA), Cadence Design Systems (San Jose, CA), and Gateway Design Automation (Lowell, MA). Low-end systems should sell for less than $10,000 on Apollo-based systems.

You can change ASIC vendors by inserting an attribute file, whose parameters you would have to get from your ASIC vendor, into the OACS. Then you would let software within the framework calculate the appropriate model effects. The OACS currently supports Motorola's 1-μm, triple-layer-metal CMOS arrays.
—Michael C Markowitz

NEW IC TEST TECHNOLOGY UNDER DEVELOPMENT

In an effort to address IC designers' complaints about the area and performance impact of design-for-testability (DFT) techniques and the extra time it takes to design in testability, CrossCheck Technology (San Jose, CA, (408) 452-0344) has developed a way to achieve high fault coverage at minimal cost on a gate array. Best of all, you get the benefit of testability without any extra design effort.

Typical DFT techniques, such as scan and built-in self test, can use as much as 20% of your chip area and degrade performance by requiring additional gate delays and capacitive loading. The CrossCheck technique involves placing a testability matrix on the base array and is like a virtual bed-of-nails test prober. With a CrossCheck-licensed gate array—currently, only LSI Logic (Milpitas, CA) has signed on—you have observability at every node in your circuit without having to add extra gates to the functional part of your design. The IEEE 1149-compatible test controller and matrix drivers and receivers will use only about 10% of your gate array. The performance effects will be minimal and caused only by capacitive loading. And because you have observability at every node, CrossCheck-software-generated test vectors are more efficient than either normal ATPG vectors or manually generated vectors.
— Michael C Markowitz

BUS-INTERFACE LOGIC DEVICES AVAILABLE IN VSOPs

Texas Instruments (Dallas, TX, (800) 232-3200, ext 700) is developing a series of wide-word bus-interface logic devices in 48- and 56-pin very-small-outline packages (VSOPs). These devices consist of 16-, 18-, and 20-bit-wide line drivers, transceivers, flip-flops, registers, and registered receivers. They can be used as dual, independently controlled, 8-, 9-, or 10-bit-wide devices or as full-width devices. The VSOPs are 300 mils wide and have 25-mil center-to-center pin spacings. The ACL devices are fabricated in 1-μm technology and have distributed V_{CC} and ground pins as well as output edge-control circuitry. Samples in the series, which operates from −40°C to +85°C, are available now; production quantities will be available in the fourth quarter of this year.—John Gallant

SONY OPENS AN ADVANCED VIDEO TECHNOLOGY CENTER

Sony Corporation of America (New York, NY, (212) 418-9427) has opened an Advanced Video Technology Center as part of its Technology and Engineering Operation in San Jose, CA. The center will focus on research and development for high-definition television (HDTV) program-production and postproduction equipment. Such equipment is needed for the creation of HDTV programming material, regardless of the broadcast formats finally chosen for US and European use. Sony intends to double its present engineering staff at the Center to support the Center's mission.
—Richard A Quinnell

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More performance. Speeds to 16ns and 35MHz. No propagation delay — cascade as many as you need.

More choices. We have 12 devices, available in just about any configuration you could want. From 64 x 4 to 2048 x 9, with many in between.

Less work. Designing with FIFOs is easier and quicker. No addresses to contend with.

Less space. Available in 300-mil DIP (including our 2K x 9 FIFO), PLCC and SOJ packages, so that your buffer logic doesn't consume acres of precious real estate.

Cool, low power. From our cool, 0.8 micron CMOS fab, less power and heat for your system.

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NEWS BREAKS

ATE SYSTEM BOASTS 16-BIT RESOLUTION AT 1 GHz

Although it's not the first application of equivalent-time sampling in a large ATE system, the $10,000 to $15,000 high-speed sampling option recently announced by Teradyne Inc (Boston, MA (617) 482-2700) for its A500 and A520 analog/VLSI device testers has an unusual configuration and delivers performance that Teradyne claims was previously unavailable in a large tester. The subsystem, most of which resides within the A500 or A520 test head, includes a small sampler that mounts on the underside of the device-interface board immediately adjacent to the pins of the device under test. Because the sampler's output is a medium-frequency signal, this configuration limits the distance that high-frequency waveforms must travel, thus minimizing aberrations introduced by the transmission-line behavior of interconnecting cables. Hence, the test systems can measure repetitive 1-GHz signals with 16-bit precision. Among the applications for this capability is determining the settling time of high-speed op amps to 0.01% of full scale on 100% of the units produced. Previously, IC vendors could afford to make this type of measurement on only a small fraction of the devices they manufactured.—Dan Strassberg

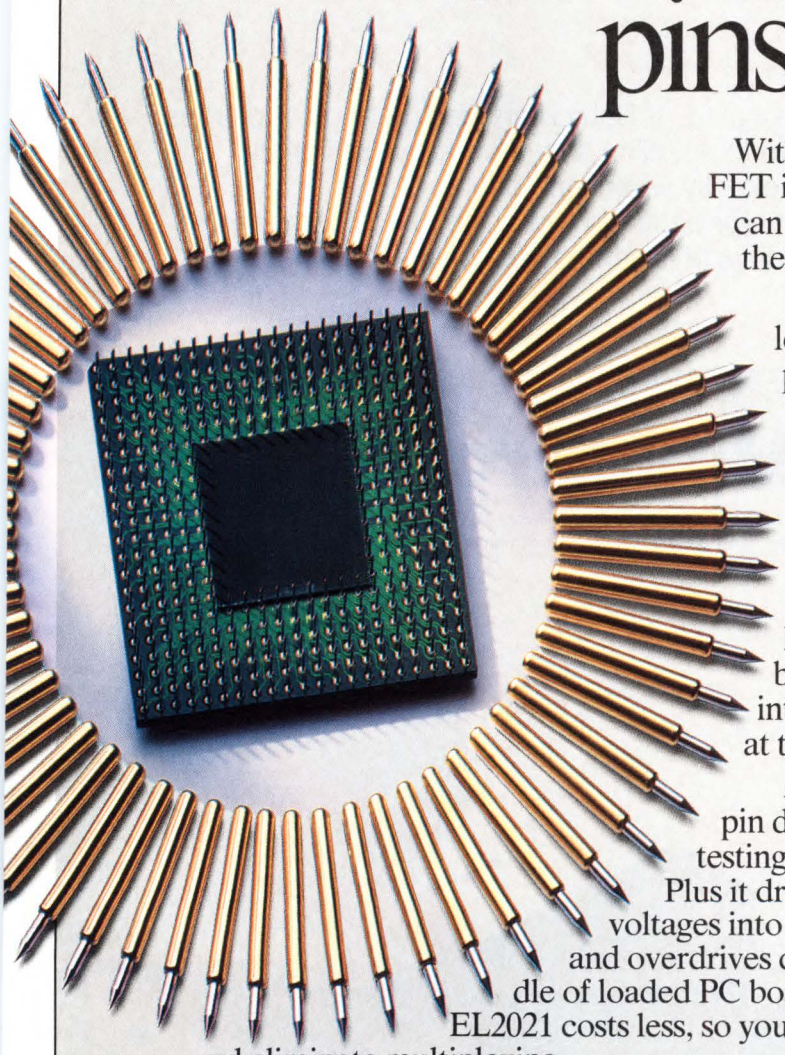
32-BIT MICROCONTROLLER DUE BY YEAR'S END

Although 16-bit microcontrollers (μCs) are fairly new and hold a small part of the μC market, Motorola Inc (Austin, TX, (512) 891-3260) expects to surpass its competitors by offering a 32-bit μC before the end of 1989. You won't have to wait for samples of the 32-bit 68332 μC chip; they're available now for $125. In addition to the basic 68020 μP CPU architecture, the 68332 chip also supplies 2k bytes of static RAM, a serial-communication module, and a timing unit. The autonomous time-processing unit (TPU)—a 16-bit counter/timer—is particularly useful in real-time-control applications. The TPU lets the chip process as many as 16 external timing signals independent of one another. Because the chip is an offspring of the 68020, many development tools will be available quickly. Already, Introl (Milwaukee, WI), Hewlett-Packard (Palo Alto, CA), Tektronix (Beaverton, OR), Intermetrics (Cambridge, MA), Ready Systems (Sunnyvale, CA), and Software Components Group (San Jose, CA) have announced software or development tools for the 68332.—Jon Titus

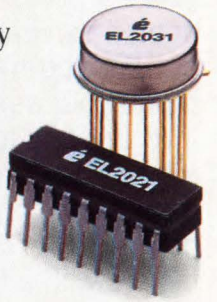
IEEE-488 BUS-CONTROL SOFTWARE RUNS UNDER UNIX

Instrument users who rely on the IEEE-488 bus can now run their application programs on 80386-based computers that offer the SCO-Xenix version of Unix. The Personal488/UX package lets you use familiar Hewlett-Packard-style commands to control as many as four sets of instruments and peripherals on IEEE-488 buses. You'll need a separate GP488C controller card—which plugs into your computer—for each set of instruments; but to ease the burden on your PC's hardware, the cards share common DMA and interrupt channels. The cards furnish a complete set of IEEE-488 listener, talker, and controller functions. Application software can be written in C or in another high-level language that controls Unix system devices. The complete package of a GP488C controller board and Driver488/UX software comes from IO Tech (Cleveland, OH, (216) 439-4091), costs $695, and is available now.
—Jon Titus

Thanks to Elantec, ATE design engineers are no longer kept waiting on pins and needles.



With Elantec pin drivers and FET input buffers, the ATE industry can stop sitting on the edge of their seats.



Whether it's for IC or loaded PC board testers, our parts are higher performing than the competition. Not to mention more affordable.

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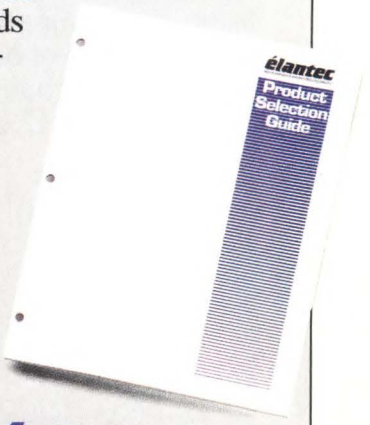

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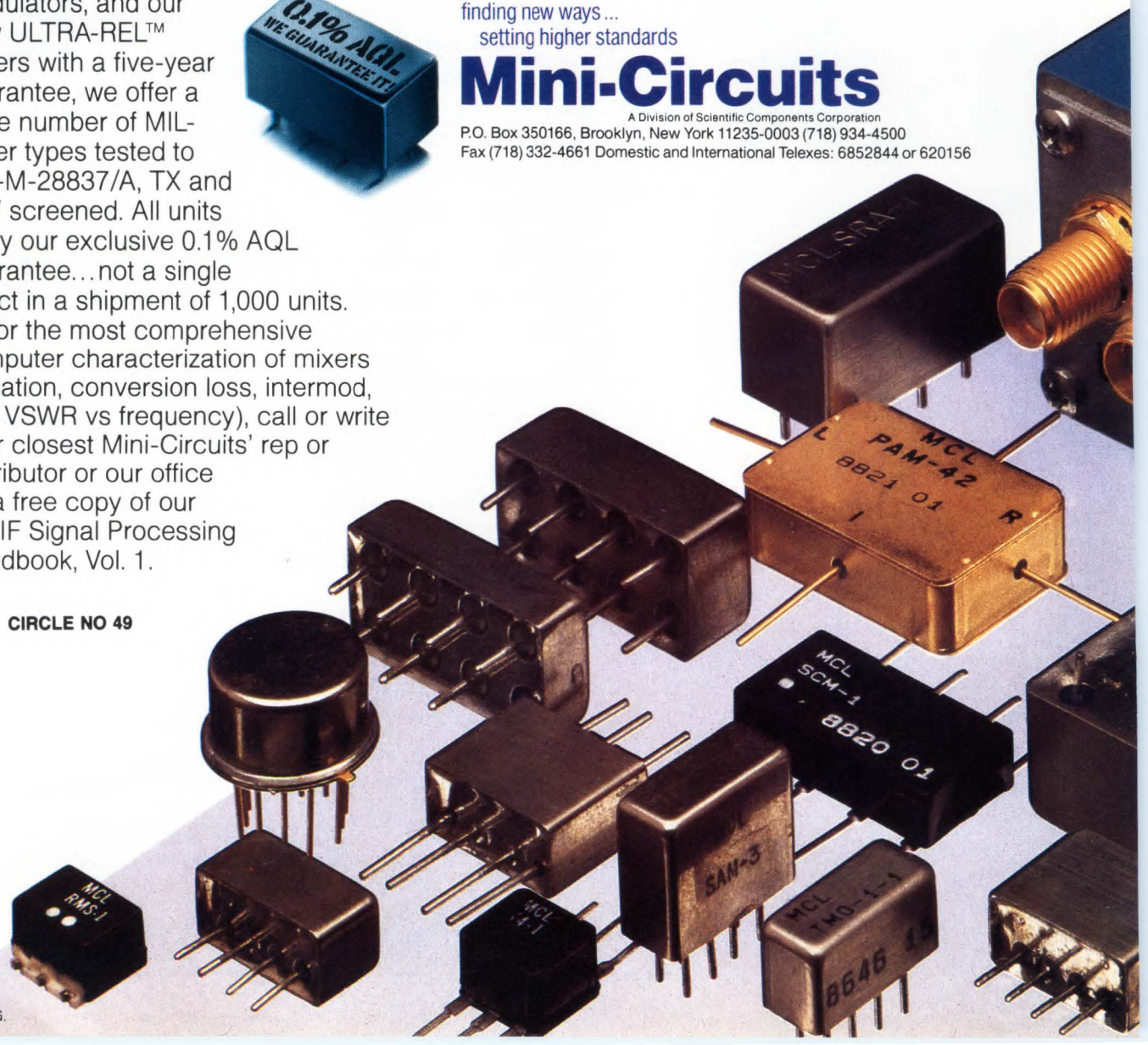

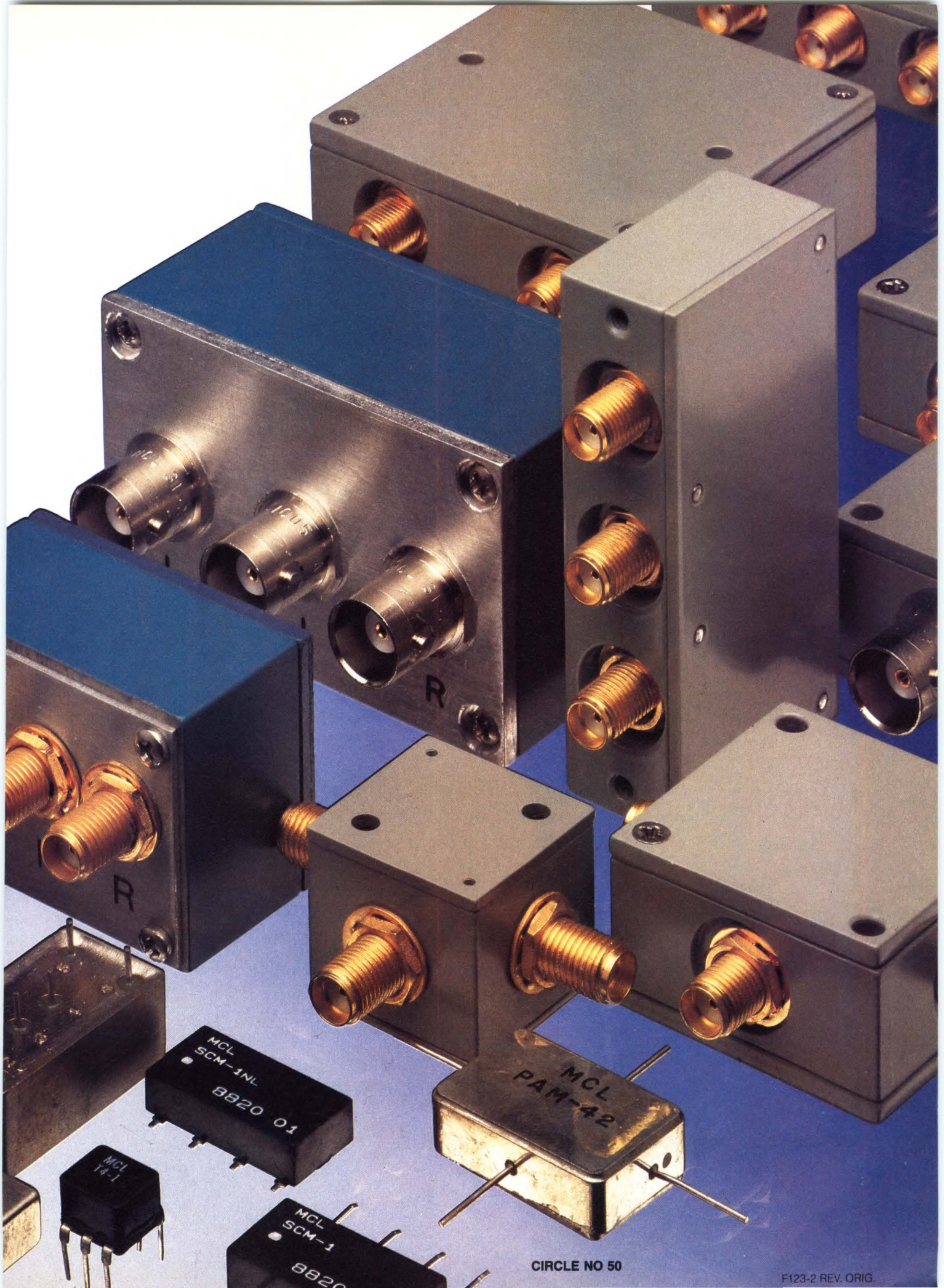

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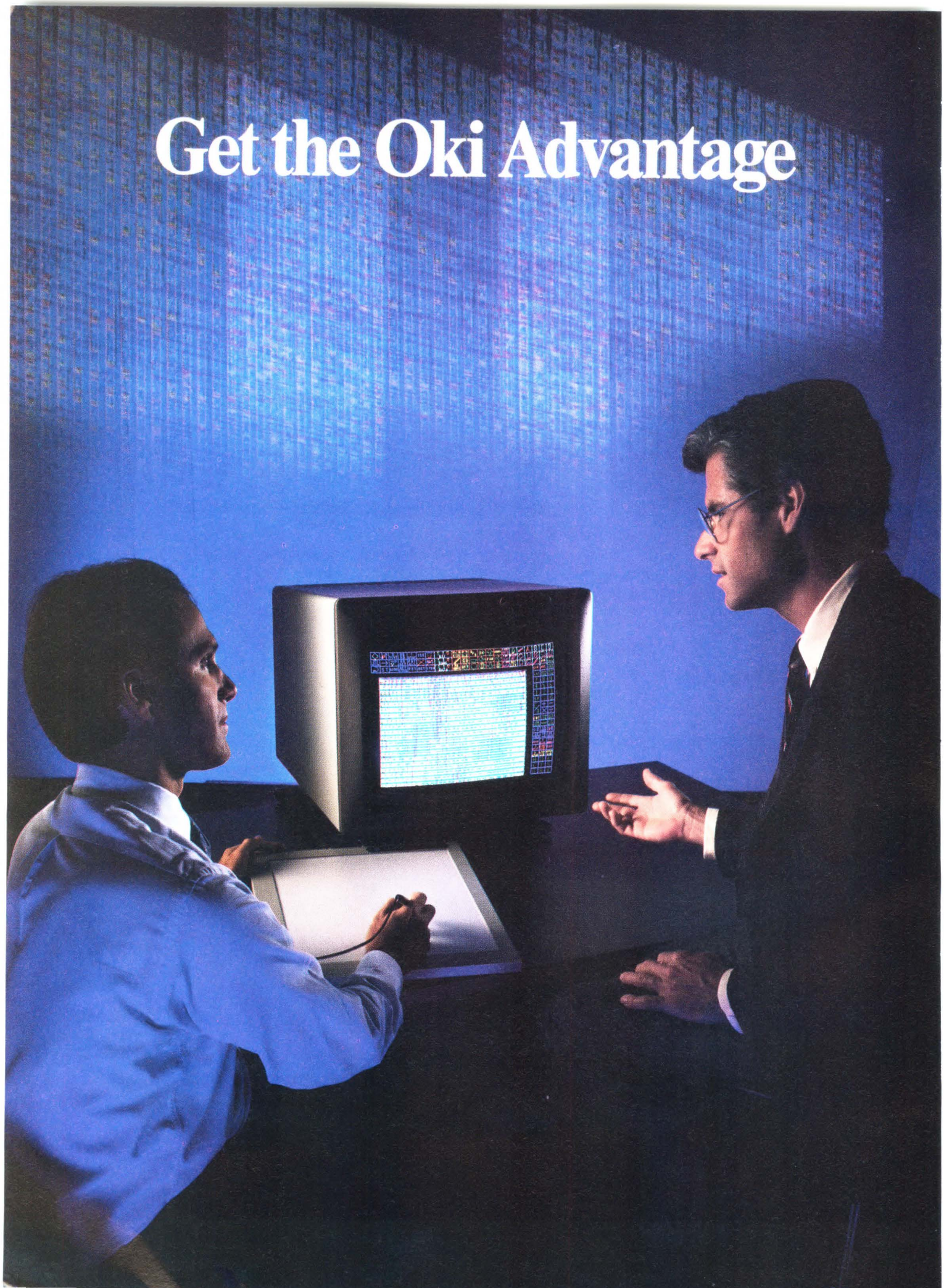
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▶ *Channeled array:*
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▶ *Standard cell:*
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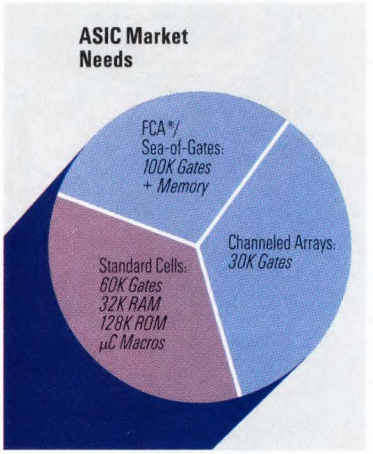

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CIRCLE NO 51

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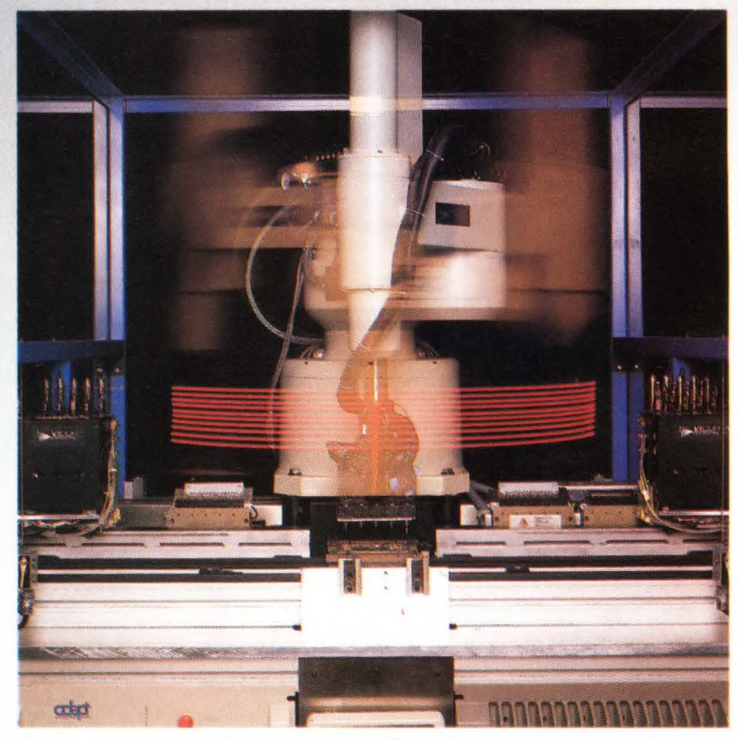

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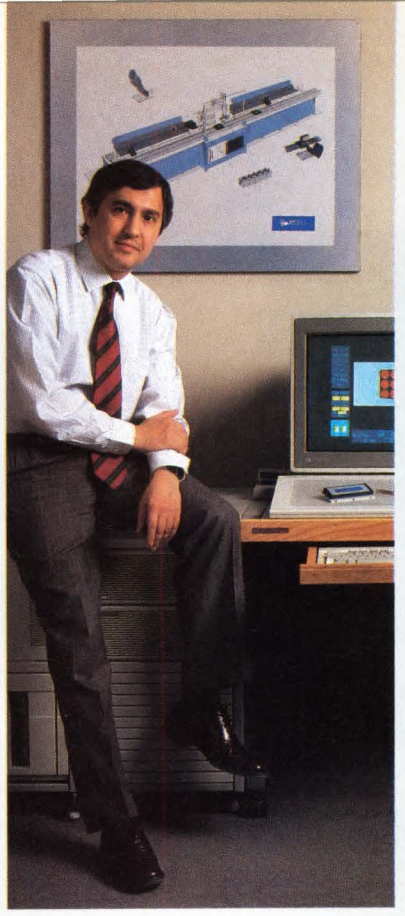

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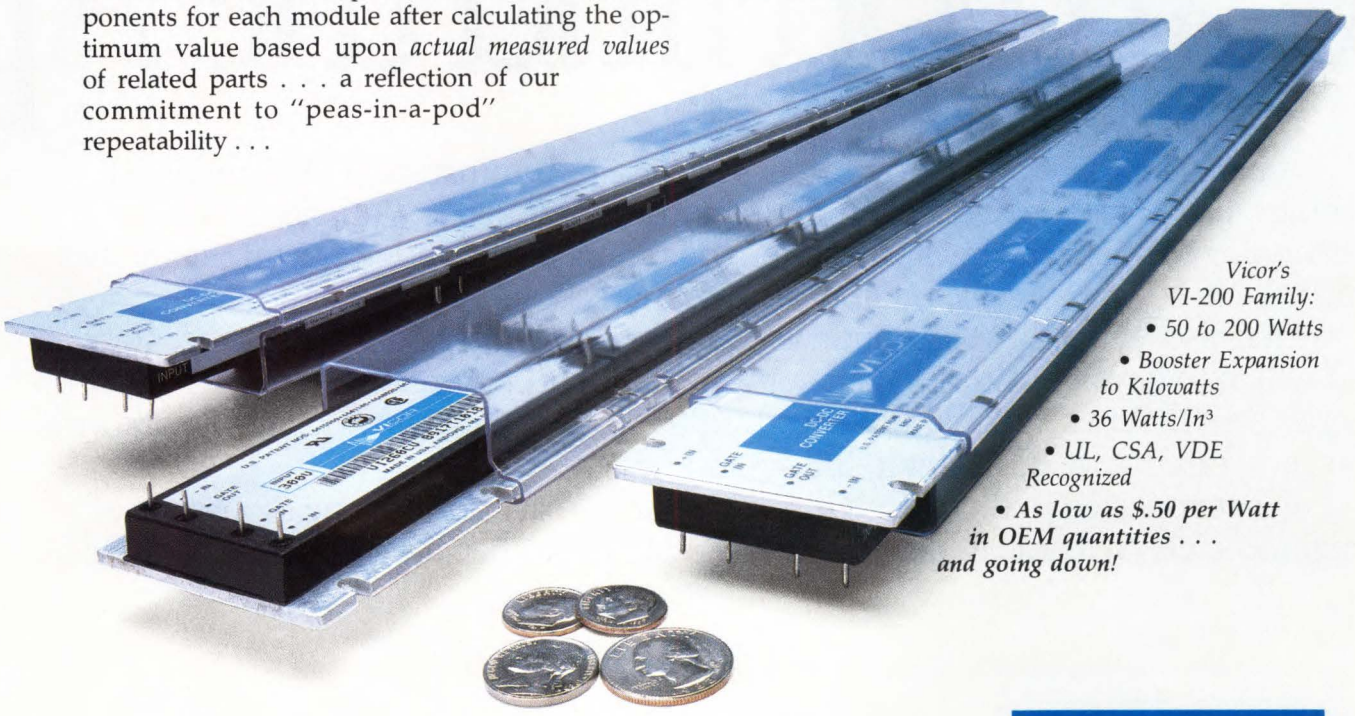

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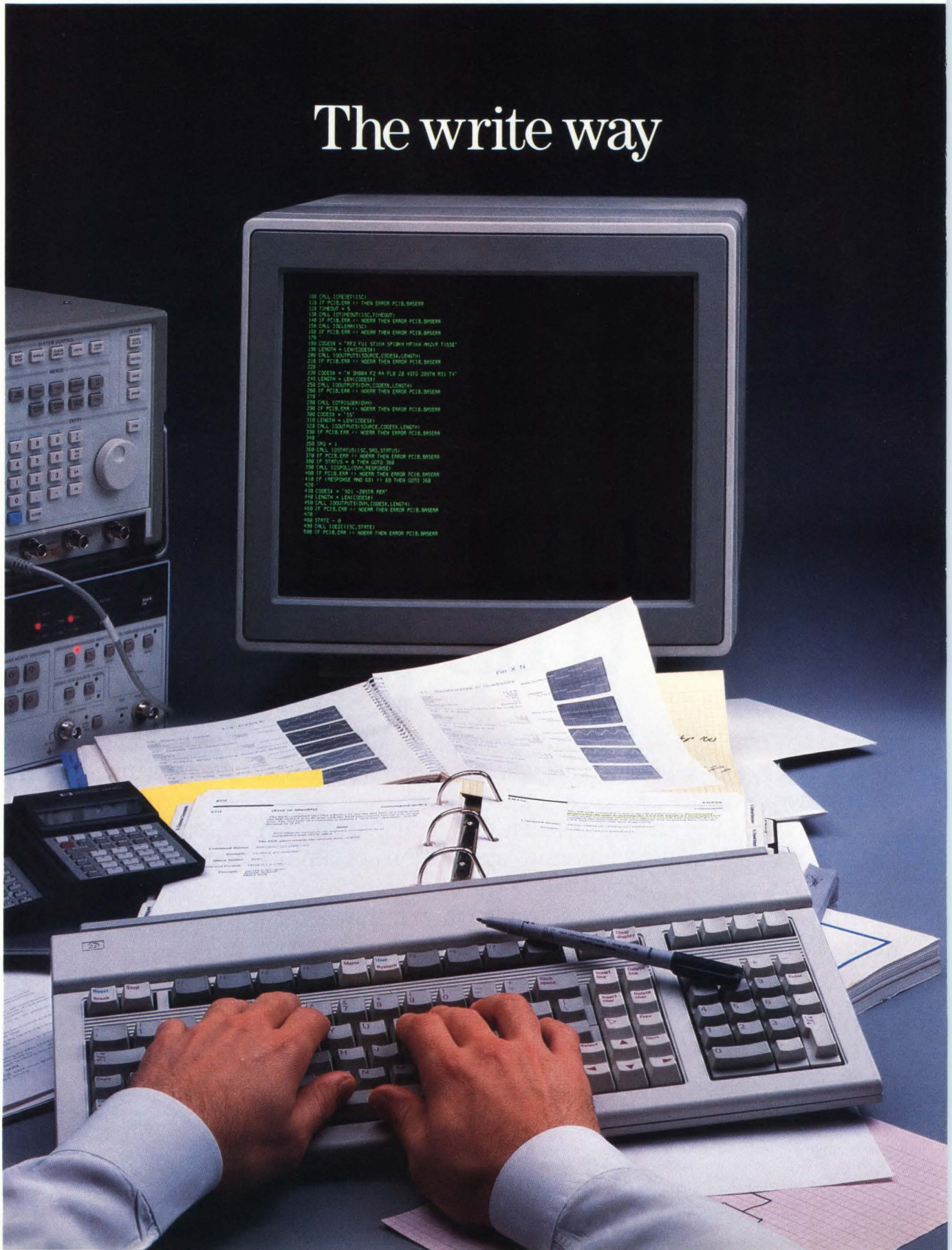

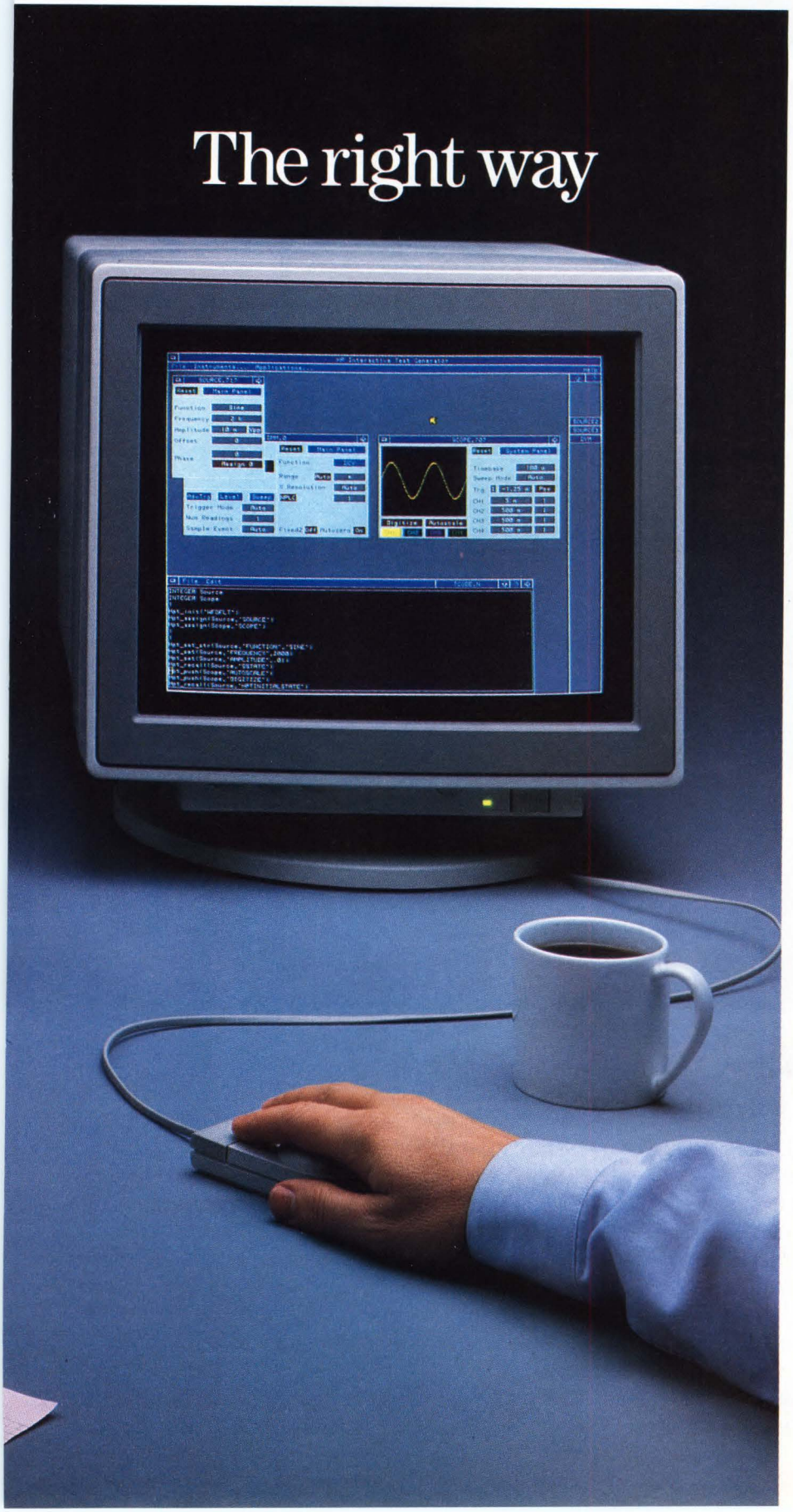

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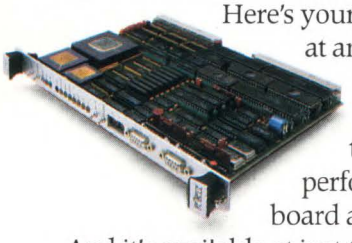

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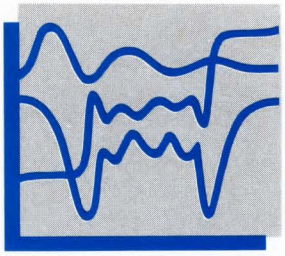

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SIGNALS & NOISE

Super Collider offers no practical benefits

I disagree with the letter of Kenneth C Kmack (EDN, January 5, 1989, pg 34, which discusses the proposed Superconducting Super Collider (SSC)). It seems to me that the letter writer got some of his facts wrong.

How naive to believe that advanced control elements or instrumentation or factory automation would be readily available! Has Kenneth forgotten all about the COCOM list? And the issue of national security? Just remember the Toshiba affair of selling advanced computer-controlled machine tools to the USSR (tools capable of making quieter submarine propellers and some such things)!

Granted, on the other hand, the knowledge of the structure of matter can be useful. But when we come to such gigantic dimensions, we should start to question the real usefulness of artificially simulating the universe on the Earth. Is it not just our perpetual obsession with machines? Keep in mind that although Ernst O Lawrence and Luis Alvarez won Nobel prizes for the invention of the cyclotron and the linear accelerator, respectively, and kept building larger and larger machines, they never made any significant discoveries with them. As a result, the first nuclear disintegration, of lithium and beryllium, was achieved by Cockroft and Walton at the Cavendish Laboratory, Cambridge University, with an electrostatic generator. The same sort of thing happened with artificial radioactivity, which was discovered in France by Frederic Joliot. Joliot used a petty apparatus powered by a minute quantity of radium . . . . The Berkeley group also missed out on making the most significant discovery in nuclear physics—namely, fission—even though the group had the world's most intense neutron beam. That discovery was made because of the work of O Hahn, F Strassmann, Lise Meitner, and O Frisch in Germany.

Are we not trying to substitute for the lack of ingenuity and insight with brute force?

"The SSC could be extremely important to the future of mankind," [Kmack says]. I would challenge that statement. As far as I can tell (as an applied physicist working in electronics/microelectronics), most electrical, electronic, computer, software, and other engineers cannot appreciate anything more sophisticated than classical electrodynamics (that is, Maxwell's equations). Most of them are not even familiar with relativistic electrodynamics, let alone quantum electrodynamics (QED) or more exotic and esoteric things, such as quantum chromodynamics (QCD) or quantum flavor dynamics (QFD); as a rule, they don't learn more involved, specialized mathematical techniques such as the Feynman integral, Kac-Moody or Virasoro algebras, Calabi-Yau spaces, and other weird and wonderful subtleties and intricacies. Where does that leave the rest of mankind?

[Kmack goes on:] "And what would we electronics engineers be doing if not for modern solid-state physics, which is based on quantum mechanics?" I fail to see the connection; what has the creation of quantum mechanics to do with accelerators? The origins of quantum mechanics can be traced to black-body radiation and spectroscopy—long before the idea of particle accelerators was born. Further, what has the invention of a transistor to do with quantum mechanics? It is unrealistic to see the transistor as the product of physics alone. Rather, its invention required the contributions of hundreds of scientists working in many different places, in many different fields, over the years.

For example, you could examine

the contribution of scores of chemists and metallurgists to an understanding of semiconductors and to the development of the ability to produce them in a form useful to physicists. Without this material-research effort, there could have been no transistor. And the planar process was the key to the whole of semiconductor work.

Today we have a whole new class of high-temperature superconductors—but we have no fitting theory to explain their behavior! Besides, what is the hurry? Why not wait until we make our ideas clearer? Leading quantum theorist David Bohm said: "I don't think the present fact is clear enough to assimilate into any mathematical system. That is one reason why so little progress has been made over the past 40 years."

I would like to finish with some words from Norbert Wiener ("the father of cybernetics"): "There is one quality more important than 'know-how' . . . . This is 'know-what,' by which we determine not only how to accomplish our purposes, but what our purposes are to be . . . . Whether we entrust our decisions to machines of metal, or to those machines of flesh and blood which are bureaus and laboratories and armies and corporations, we shall never receive the right answer to our questions unless we ask the right question . . . ."

Igor Fodor
Semiconductor Div
Siemens
Munich, West Germany

Correction

An incorrect phone number for Covox Inc (a manufacturer of speech-recognition products) appeared on pg 120 of the January 19, 1989, issue of EDN. The correct phone number is (503) 342-1271.

Text continued

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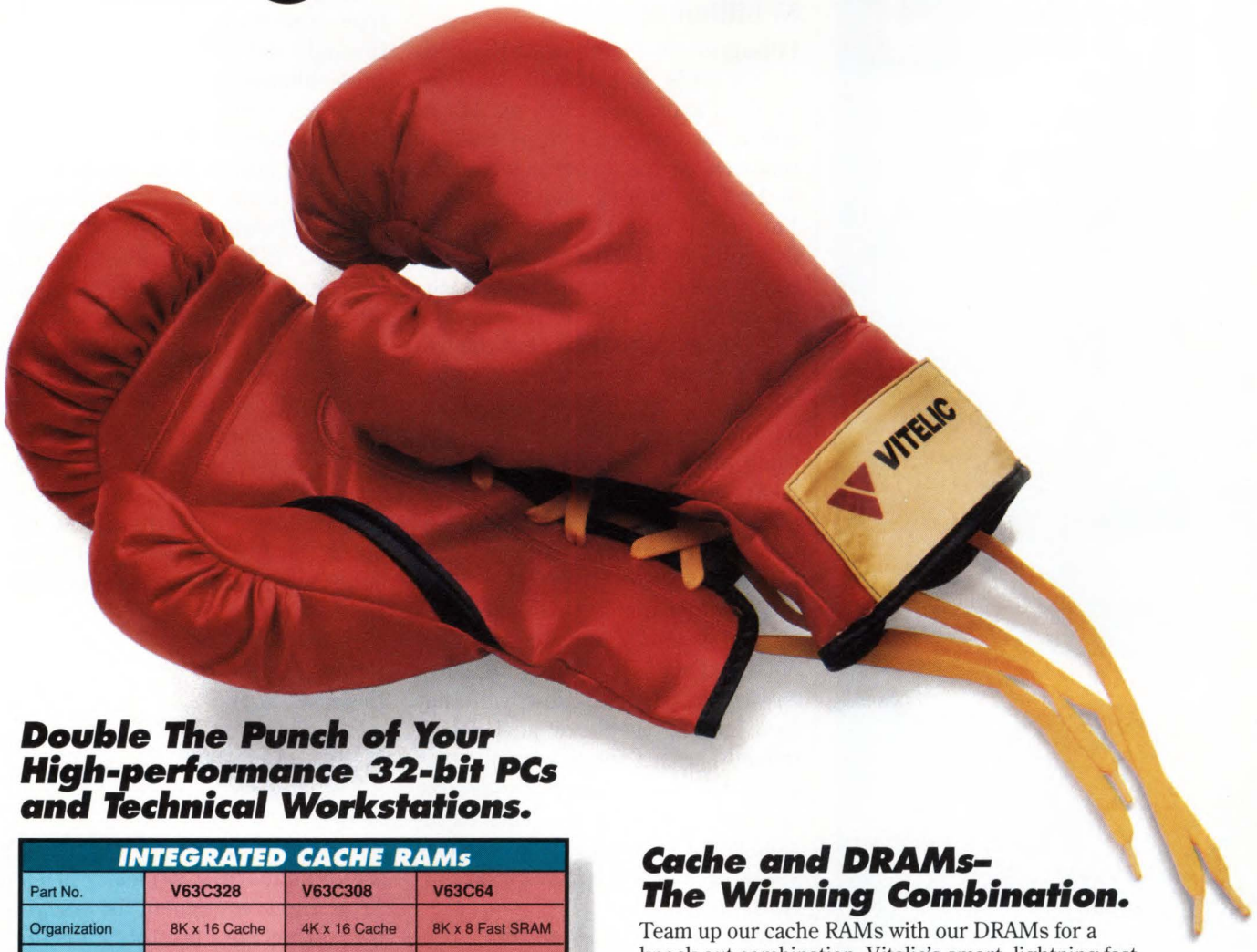

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SIGNALS & NOISE

Supercollider is a $5 billion mistake

I disagree completely with Kenneth C Kmack's half-baked analogy (EDN, January 5, 1989, pg 34), in which he compares Supercollider research to the experiments done in 1887 by Morley and Michelson. I'm pretty sure they didn't spend five billion dollars of somebody else's money to conduct their experiments.

People seem to think that the five billion is sitting in a bank somewhere waiting to be spent, either on the Supercollider or on something else. In reality, the government will simply print five billion dollars or more to pay for the Supercollider, and that will inevitably lead to inflation.

Then, when the Supercollider is up and running, *maybe* we'll find out about some previously unknown subatomic particle. How will that feed hungry people or keep felons behind bars? If the Supercollider is going to make something possible that everybody can use (such as fusion power), somebody had better speak up and tell us what it is.

Andrew Dart
Andy's Bureau of Standards
Duncanville, TX

The US should get in on HDTV

Why didn't the FCC include Japan's HDTV standard in our future? The FCC continues to talk of updating NTSC to a wide screen, when nothing has been demonstrated or built. It's a bad idea—the splicing of margins onto the picture is going to be visible—especially when reception is poor.

Even if NTSC could be updated, we should cooperate with a new standard. Too bad we didn't lead in HDTV, but if we don't participate, it will become very difficult to develop and export any HDTV-related product.

They say we don't have enough free spectrum. Not true; 470 through 890 MHz is basically vacant—allocated for 69 dead UHF channels. I see only three active in Seattle. Reallocate it for HDTV, and some other things besides.

It's as simple as AM/FM radio. AM didn't stop the upgrade to FM. Let the folks with existing TVs keep watching NTSC 2 to 13. Meanwhile, those of us living in the present can buy HDTVs that tune in 20 or 30 new wide-screen channels—and our sets will work with HDTV camcorders and VCRs.

Why doesn't anybody see the obvious? Where does EDN stand on this problem? Do other EEs care about the FCC's lack of vision? An outcry could still correct this shortsightedness.

Norman M Hill
Zetron Inc
Bellevue, WA

Oops

The second article in Bob Pease's troubleshooting series, entitled "The right equipment is essential for effective troubleshooting" (EDN, January 19, 1989, pg 157), contains two schematic errors. The first appears in **Fig 4**, pg 160: there should be a connector dot at the point where the signal lines cross just to the left of V_{OUT}. The second error occurs in **Fig 8** (pg 165): The 24-kΩ resistor shown in the lower right corner of the drawing should be 240 kΩ.

WRITE IN

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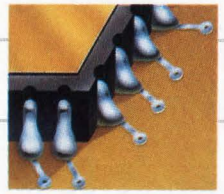

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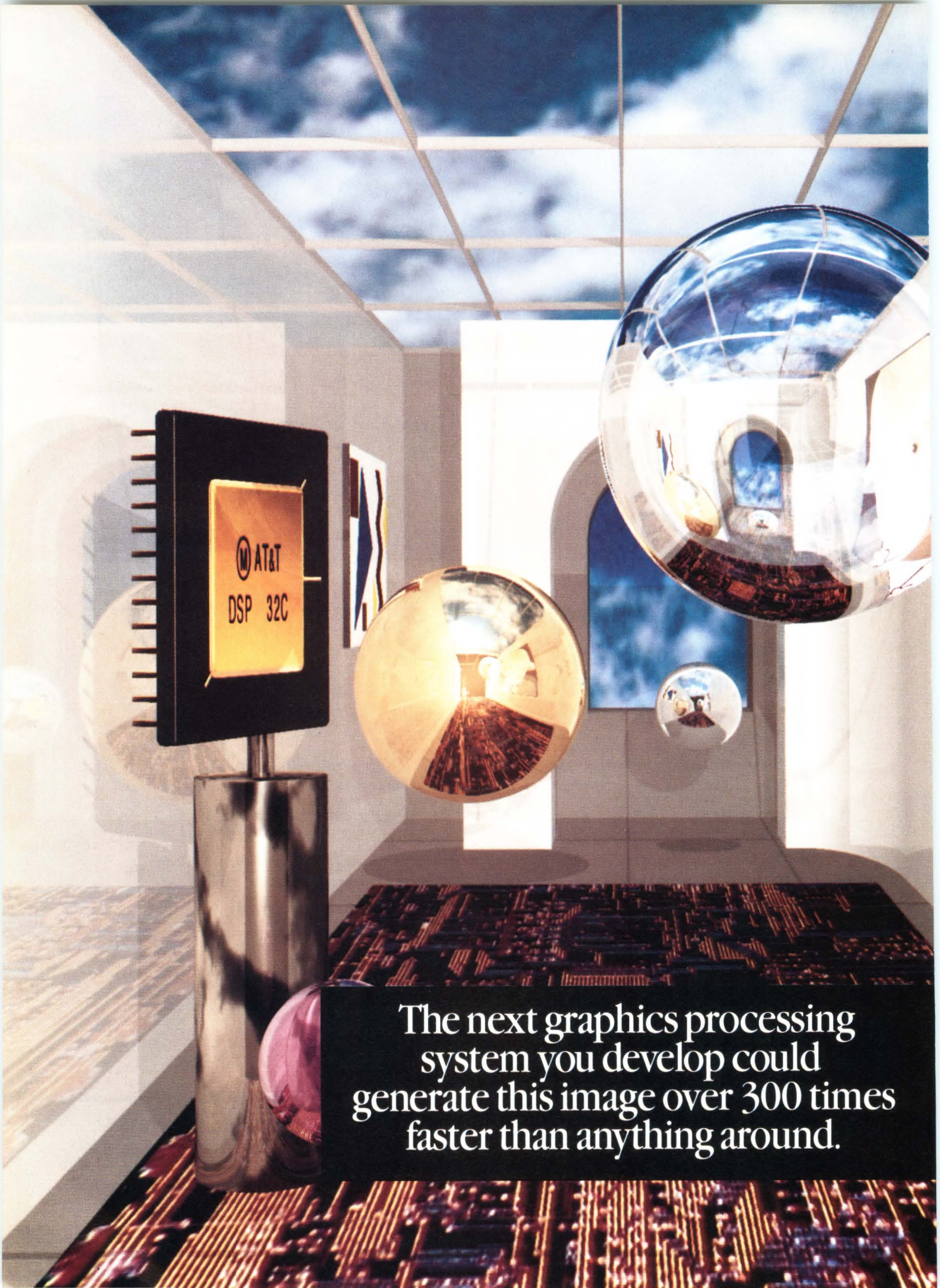

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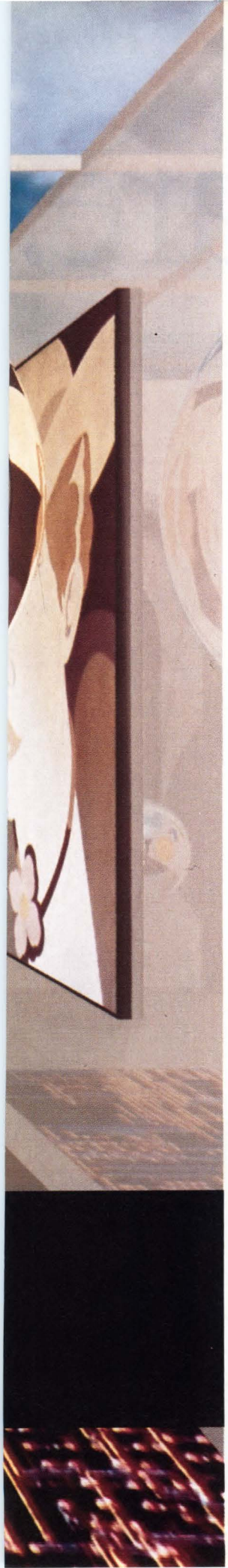

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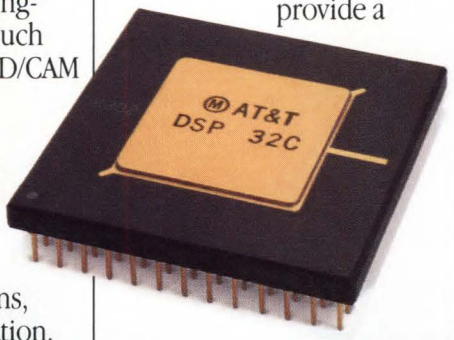

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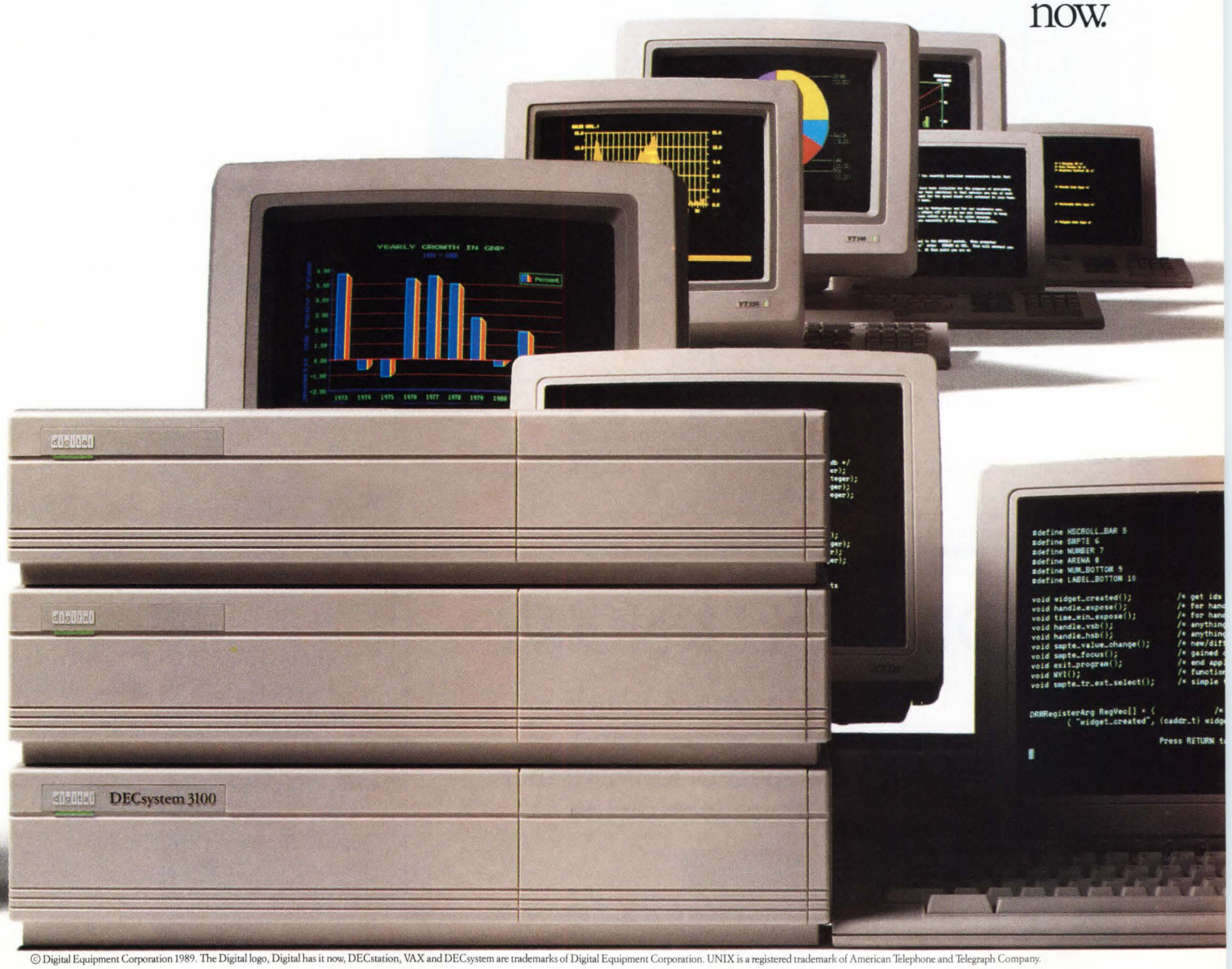


CALENDAR

Fiber Optics in Local Communications (seminar), New York, NY. Raycom Systems Inc, 6395 Gunpark Dr, Boulder, CO 80301. (800) 288-1620. June 22.

26th Design Automation Conference, Las Vegas, NV. MP Associates, 26th Design Automation Conference, 7490 Clubhouse Rd, Suite #120, Boulder, CO 80301. (303) 530-4333. June 25 to 29.

Intelligent Network ComForum, Chicago, IL. IN ComForum, 303 E Wacker Dr, Suite 740, Chicago, IL 60601. (312) 938-3500. FAX 312-938-8787. June 26 to 28.

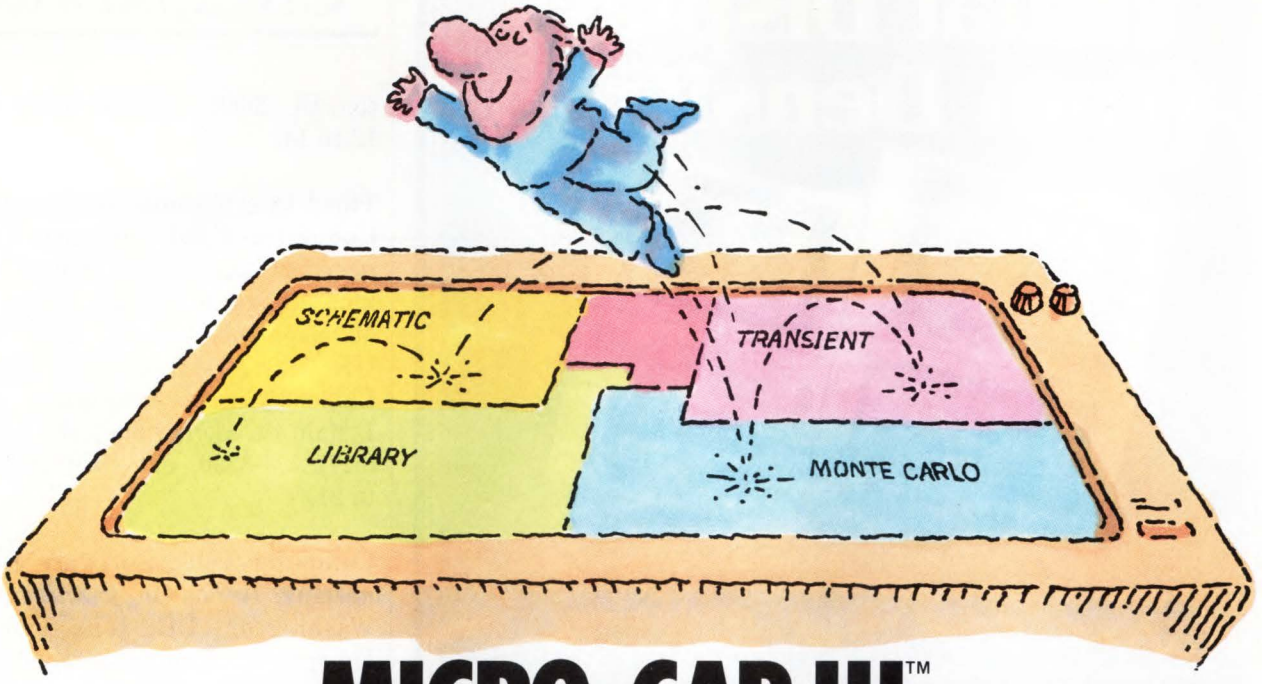
Knowledge Engineering Today's Marketplace, The Annual Conference of the International Association of Knowledge Engineers, College Park, MD. Fred Whiting, IAKE Conference, Georgetown Box 25461, Washington, DC 20007. (301) 231-7826. June 26 to 28.

OS/2: A Comprehensive Hands-On Introduction (short course), Ottawa, Ontario, Canada. John Valenti, Integrated Computer Systems, 5800 Hannum Ave, Culver City, CA 90231. (800) 421-8166; in Canada, (800) 267-7014. June 27 to 30.

World Tech '89, New York, NY. A Robert Terrero, AETEC, 225 W 34th St, Suite #906, New York, NY 10122. (212) 563-5350. FAX 212-736-0027. June 28 to 30.

National Conference of Standards Laboratories (NCSL '89) Workshop and Symposium, Denver, CO. Ken Armstrong, NCSL, 1800 30th St, Suite 305B, Boulder, CO 80301. (303) 440-3339. July 9 to 13.

Quality Management Conference, Denver, CO. Pam Frye, Quality Management Conference, ACEC, 1015 Fifteenth St NW, Washing-



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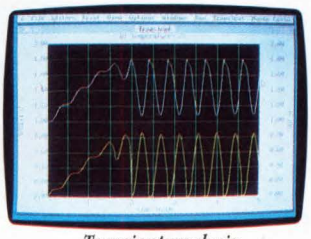
THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

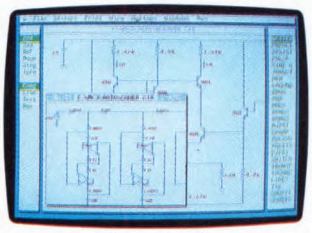
MICRO-CAP III,™ the third generation of the top selling IBM® PC-based interactive CAE tool, adds even more accuracy, speed, and simplicity to circuit design and simulation.

The program's window-based operation and schematic editor make circuit creation a breeze. And super-fast SPICE-like routines mean quick AC, DC, Fourier and transient analysis — right from schematics. You can combine simulations of digital and analog circuits via integrated switch models and macros. And, using stepped component values, rapidly generate multiple plots to fine-tune your circuits.

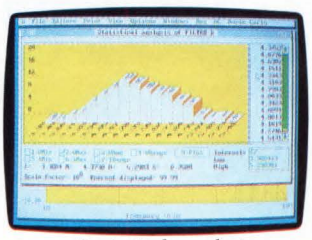
We've added routines for noise, impedance and conductance — even Monte Carlo routines for statistical analysis of production yield. Plus algebraic formula parsers for plotting almost any desired function.



Transient analysis



Schematic editor



Monte Carlo analysis

Modeling power leaps upward as well, to Gummel-Poon BJT and Level 3 MOS — supported, of course, by a built-in Parameter Estimation Program and extended standard parts library.

There's support for Hercules,® CGA, MCGA, EGA and VGA displays. Output for laser plotters and printers. And a lot more.

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CIRCLE NO 64

CALENDAR

ton, DC 20005. (202) 347-7474. July 12 to 14.

Third International Workshop on Computer-Aided Software Engineering, London, UK. John O Jenkins, Imperial College, School of Management, London, SW7 2PG, UK. 01 589 5111, ext 7112. Elliot J Chikofsky, Index Technology Corp, 1 Main St, Cambridge, MA 02142. (617) 494-8200, ext 1989. July 17 to 21.

Computer-Aided Software Engineering, Hands-On (short course), Washington, DC. John Valenti, Integrated Computer Systems, 5800 Hannum Ave, Culver City, CA 90231. (800) 421-8166; in Canada, (800) 267-7014. July 18 to 21.

SparcIntosh (conference), San Francisco, CA. Corey Green, The Yankee Group, 200 Portland St, Boston, MA 02114. (617) 367-1000. July 25 to 26.

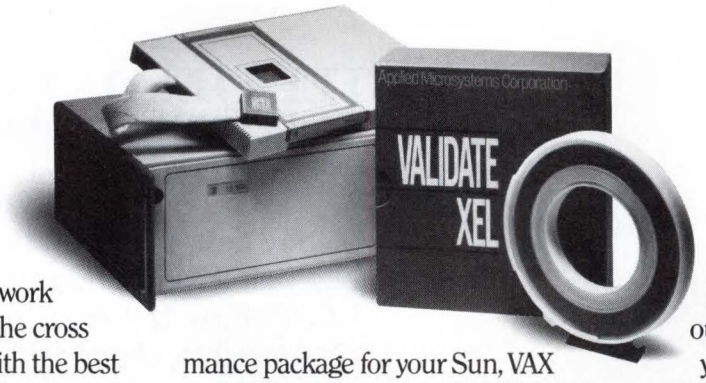
Supercomputers, Hypercubes and High Performance Architectures (short course), Boston, MA. John Valenti, Integrated Computer Systems, 5800 Hannum Ave, Culver City, CA 90231. (800) 421-8166; in Canada, (800) 267-7014. July 25 to 28.

11th Quartz Devices Conference and Exhibition, Kansas City, MO. Electronic Industries Association, 1722 Eye St NW, Washington, DC 20006. (202) 457-4981. August 28 to 31.

Surface Mount '89, San Jose, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. August 28 to 31.

International Test Conference 1989, Washington, DC. International Test Conference, Box 264, Mt Freedom, NJ 07970. (201) 895-5260. FAX 201-895-7265. August 29 to 31.

CROSS DEVELOPMENT SOFTWARE THAT'S MAKING NETWORK NEWS.



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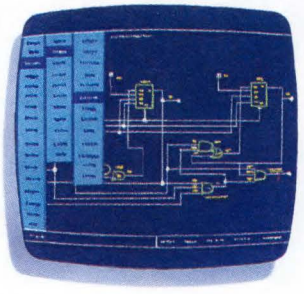
In Japan contact Applied Microsystems Japan Ltd., Nihon Seimei, Nishi-Gotanda Building, 7-24-5 Nishi-Gotanda, Shinagawa-KU, Tokyo T141, Japan. Call 03-493-0770.

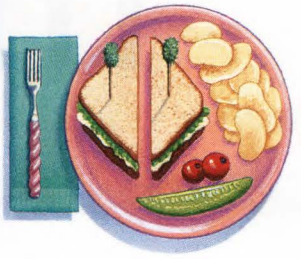
Be Brilliant At In Productio

7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

ACTEL FIELD PROGRAMMABLE GATE ARRAYS

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL®, or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

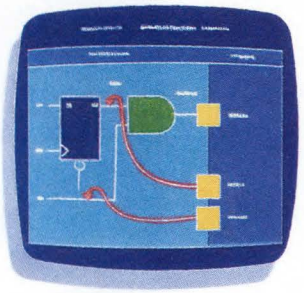
They're the core of Actel's comprehensive design and production system for creating your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic,™ OrCAD™ and Mentor.™

And do it in hours instead of weeks. Even between meals.

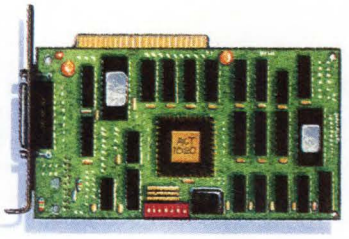
How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic

Breakfast And n By Dinner.

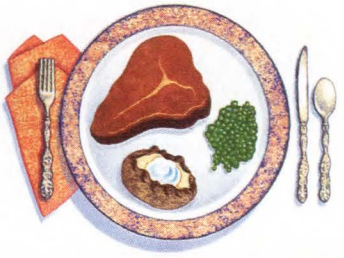
1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a *very* quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most tedious part of the job by hand. And design verification is quick and easy, with on-chip Actionprobes™ that work with your logic analyzer to provide 100% observability of internal logic signals. Guaranteed.

All this is made possible by Actel's invention of the revolutionary PLICE™ antifuse programming element. Developed specifically for logic integration, PLICE antifuses and Actel's gate array architecture let you pack more functionality into much smaller spaces. No more splitting equations across multiple PLDs. Or being short on flip flops. Or running out of connections halfway through routing.

Every Actel part is fully tested at the factory, and each antifuse is verified during programming. So you don't have to give up testability for convenience.

You can be brilliant right now with 1200- and 2000-gate devices, and 6000-gate parts are on the way.

Call **1-800-227-1817, ext. 60** today for a free demo disk and full details about the whole Actel logic solution.

It could make your whole day.

Actel

VF Technology... The Bright Decision

Futaba, a world leading manufacturer of vacuum fluorescent displays, offers a wide assortment of *display tubes* in many sizes and formats. Also, Futaba offers *display modules* with all the electronics required to refresh the display and easily interface with host system.

GRAPHIC DISPLAY

Both front glass phosphor, which provides maximum viewing angle and uniform surface appearance, and conventional back glass phosphor, with optimum brightness and software dimming capabilities, are available. All Futaba graphics modules offer complete drive electronics, bit mapped control with a DC/DC converter. All active components are surface mounted onto a single board.

DOT MATRIX MODULES

Utilizing Futaba's dot matrix displays, a completely intelligent line of "dot modules" is available. Each includes all drive, power supply and microprocessor components surface mounted onto a single board. Surface mounted technology results in higher reliability and allows for a smaller overall package and lower cost. All dot modules require only a 5V DC power source and can accept parallel or 8 possible serial baud rates.

GRAPHIC DISPLAYS/MODULES

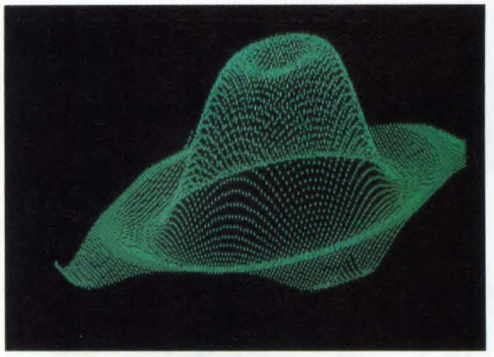
Futaba Display	Futaba Module	Pixels (Row X Char.)	Brightness (FT-L)	Module Dimensions (in.)
GP1013A	GP1013A02	64X34	200	3.35X2.95X0.7
GP1005B	GP1005B03	128X64	400	7.28X3.35X1.77
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1009B	GP1009B03	240X64	200	6.2X2.76X1.57
GP1006B	GP1006B04	256X64	200	9.84X3.35X1.77
GP1002C	GP1002C02	320X240	100*	7.10X6.30X1.60
GP1018A	GP1018A01	400X240	40	7.10X6.30X1.61
GP1004C	GP1004C03	640X400	30	9.65X7.3X1.85
GP1019A	GP1019A03	640X400	35	7.10X6.70X2.56

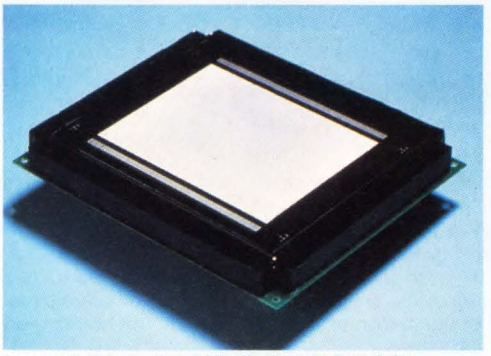
*Different Versions Available

DOT MATRIX/CHARACTER DISPLAY MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
16LD03G	M16LD03B	16X1	5X7	0.433	8.90X1.95X.98
16SY03Z	M16SY03B	16X1	14 SEGMENT ALPHANUMERIC	0.200	4.92X1.32X.83
20SD01Z	M20SD01	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04	40X2	5X7	0.200	10.43X2.56X.90

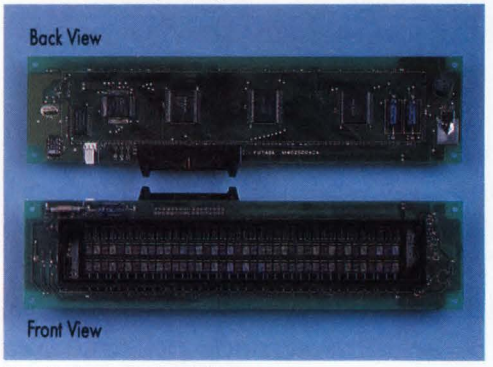
MANY OTHER DISPLAYS **NEW MODULES AVAILABLE SOON**





Compact, flat panel graphic displays and modules present clean, sharp images, whether for text or full graphics application.

2 x 40 character (display)



2 x 40 character (module)

Pattern flexibility and pleasing appearance are offered by Futaba in dot displays and modules.

Futaba also offers a complete catalog of alphanumeric, segmented displays.

Futaba supports its products with design engineering and system integration assistance. Call or write today.

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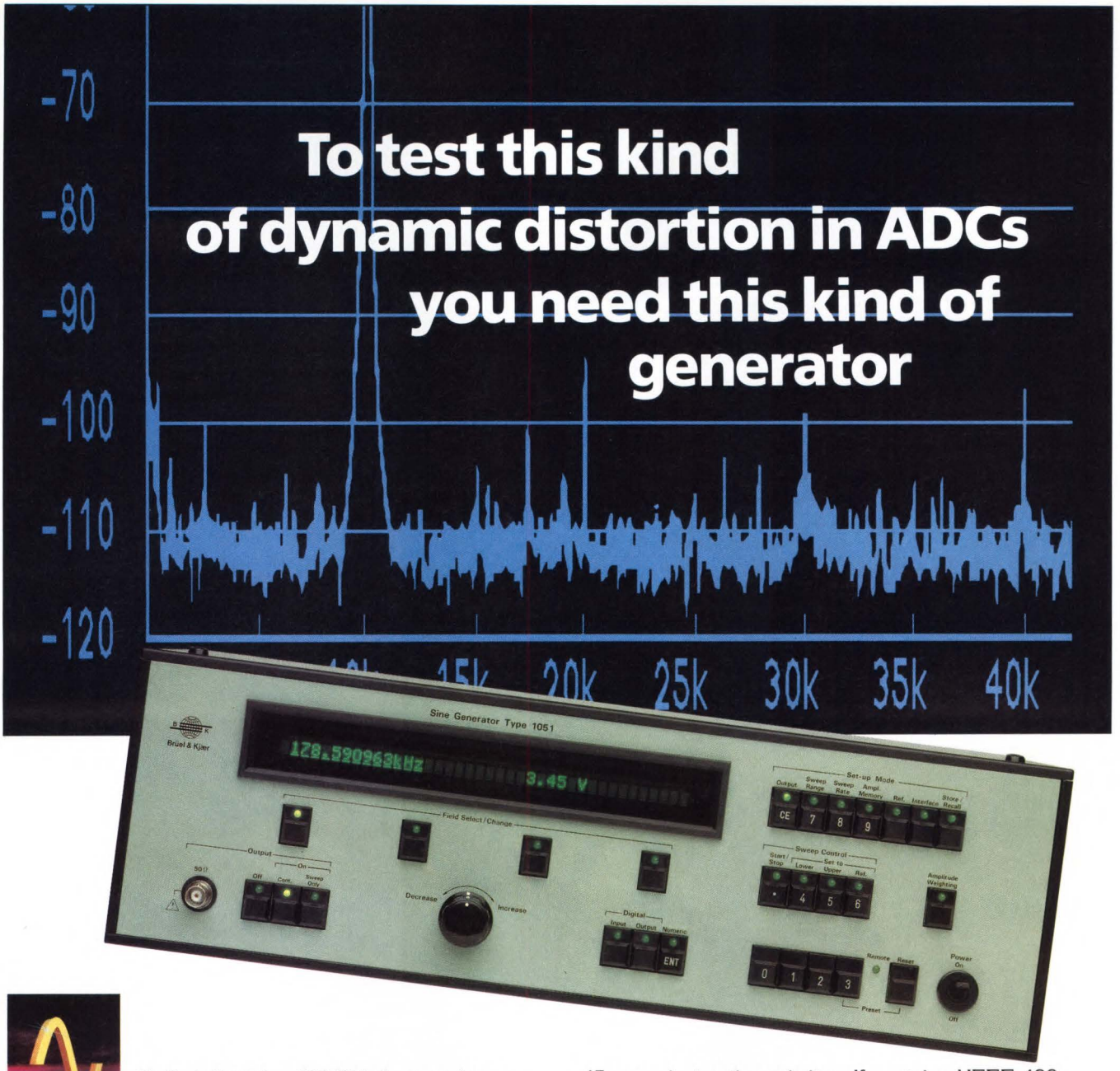

To test this kind of dynamic distortion in ADCs you need this kind of generator

To find distortion 100dB below maximum signal, you need a generator that's at least two times better than the device under test.

That's why the Bruel & Kjaer 1051 is the generator of choice when you want to pinpoint dynamic distortion in ADCs due to differential and integral non-linearities, missing codes, noise and aperture uncertainty.

Individual harmonics from the B&K 1051 are less than 0.0008% (− 102dB) in the critical 20Hz to 20kHz range, and its broadband noise and distortion is better than − 85dBc.

Its amplitude is accurate within 0.05dB and its crystal-clock-based freqency synthesizer is accurate to + 0.18mHz/ − 0Hz.

And all this signal purity and frequency precision does not cost you any additional testing time. The B&K 1051 settles to its set frequency and amplitude in less than 45ms on instructions via its self-contained IEEE-488 interface (three times faster than most other generators).

You get plenty of convenience features too. Like easy external control with English language commands, a 1024-point amplitude memory, storage of user-defined test routines, and six-decade log or linear frequency sweep in one range with selectable upper and lower frequency limits.

For ADC characterization, ATE, testing ADC front ends in telecommunications, navigation systems, laboratory and medical instruments and general AC calibration, choose the Bruel & Kjaer 1051. It gives you what you've always wanted in a test source and never had; signal purity, frequency and amplitude accuracy and testing speed combined in a single instrument.

For complete information on the 1051 generator, call your nearest Bruel & Kjaer office today or circle reader service number.

Brüel & Kjær

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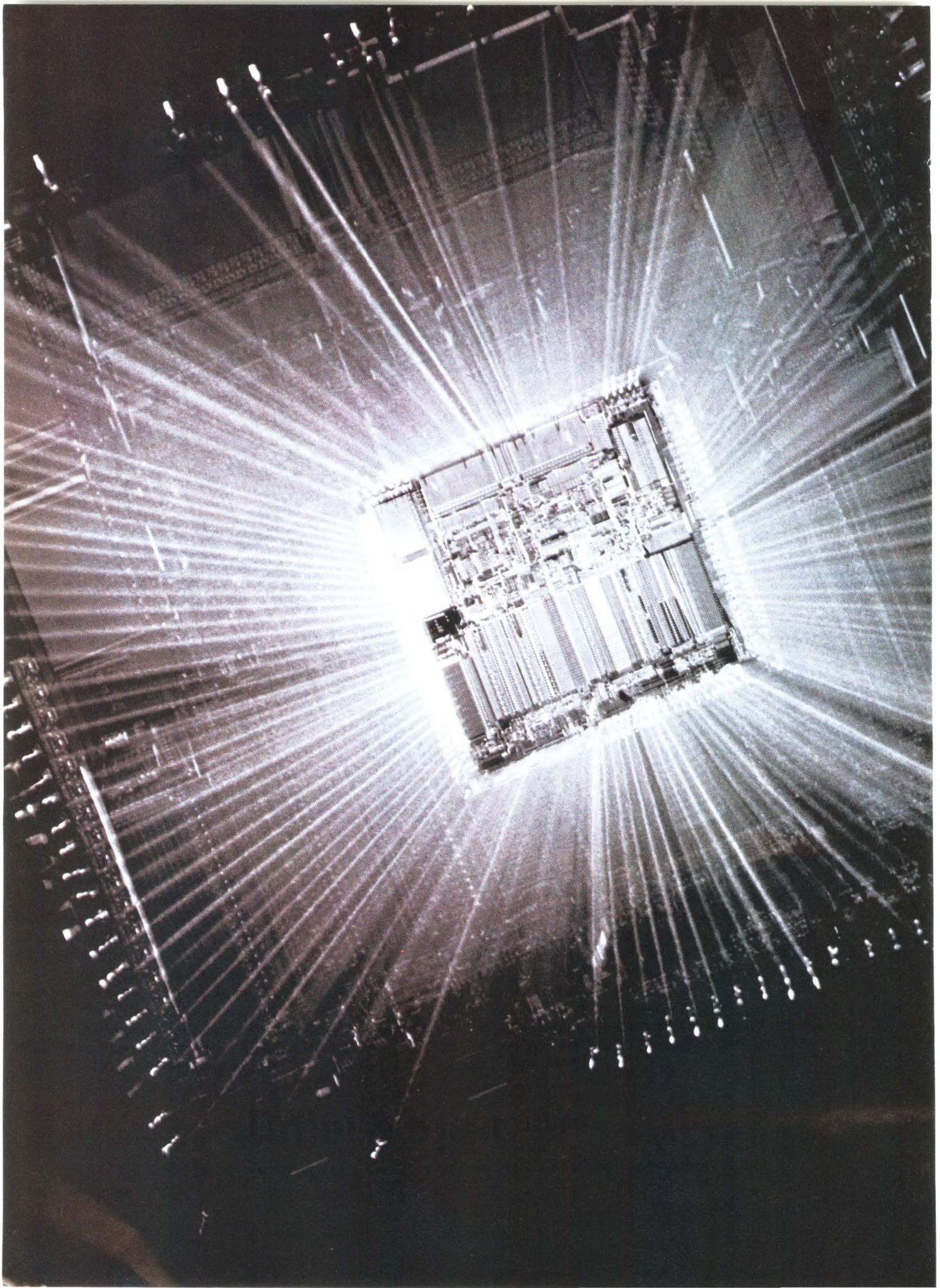

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In the computer industry with its never ending goal of miniaturization, nothing is more important than using the highest performance engineering plastics.

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Our Xydar® resin, for example, has excellent dimensional and creep stability at elevated temperatures. It is a natural choice for higher density connectors and IC sockets. Plus, it has low ionic contamination and is ideal for surface mount assembly.

For more information, write for our brochure, "Engineering Plastics for Performance and Value." Amoco Performance Products, 38 C Grove Street, Ridgefield, CT 06877. Or call 1-800-621-4557.

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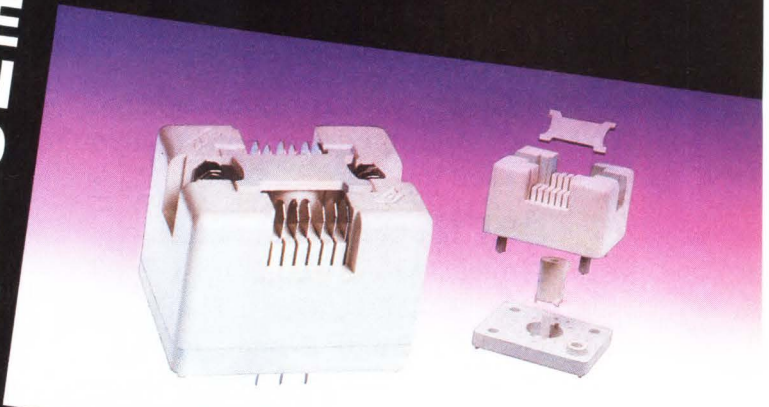
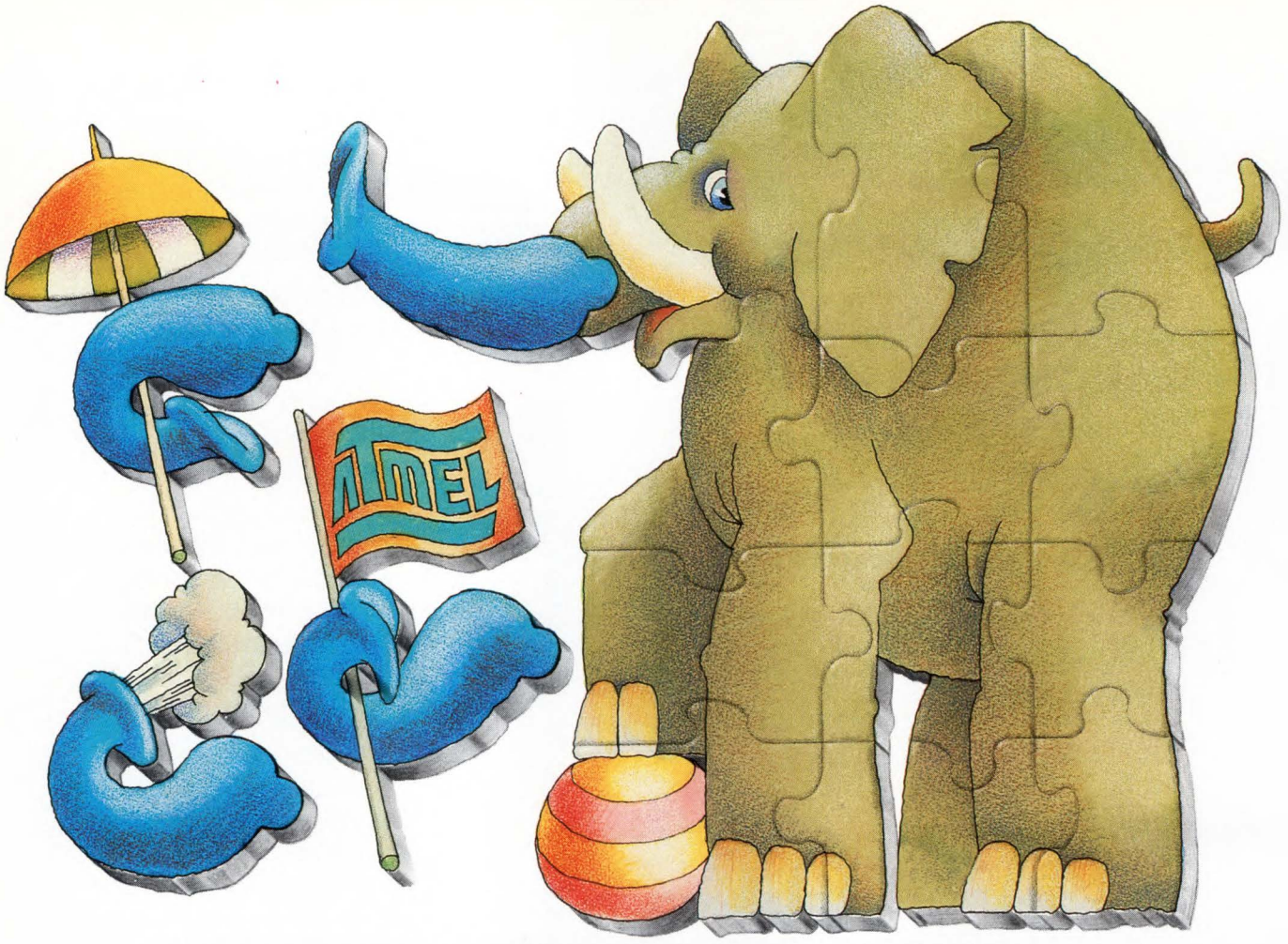
The higher performance plastics.



Xydar® resin was chosen by J.M. Ney for this extremely high temperature burn-in socket because of its dimensional and creep stability at temperatures above 200°C.

CIRCLE NO 71



THE JUMBO REPROGRAMMABLE GATE ARRAY

Puzzled by all the logic arrays in the jungle? There's only one leader. To spot him make sure that:

- His array can really do the big jobs. It should be able to replace a whole board of old-fashioned logic.
- His array gives you a speed/power savings.
- His array is easy to use, and has a programming scheme that you're used to.

MEET THE REALLY BIG ARRAY

Atmel's ATV 2500 has up to 2500 gates. Call it JUMBO. That's about eight AT22V10s in one—enough resources for most board-sized jobs. And you can reprogram it, again, and again and again.

Atmel's Jumbo leads the herd with 30MHz operating frequency, but only needs 5mA—about one-half of what his competitors offer.

NOW THE GOOD NEWS!

You probably already know how to run this beauty. Its structured architecture is similar to what you have been working with all along, so you use your usual design methods and make only minor changes to your software and hardware.

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The people who make the difference

CIRCLE NO 72

EDITORIAL

Weird science

What we've read about science in the popular press during the past few months shows a very poor understanding of what science is and what scientists really do. A good example occurred in April when two researchers, B Stanley Pons and Martin Fleischmann, announced that they had observed "cold fusion," the fusing of two deuterium nuclei to produce a helium atom, a neutron, and heat. Unlike most scientific announcements and rebuttals, which take place at staid scientific meetings and in arcane scientific journals, Pons and Fleischmann revealed their *raw* results to the popular, and generally unscientific, press. That revelation touched off a storm of press coverage.

Once again, the press and many others flocked to the story of a so-called scientific breakthrough; they inflated reports of a preliminary scientific experiment into a cure for the world's energy problems. Even before other laboratories had attempted to duplicate the Pons-Fleischmann experiment, members of the House Committee on Science, Space, and Technology wanted to know how much money the two researchers would need to continue their work. All we're missing now is talk of a "cold-fusion" gap with various foreign countries.

Those who wrote about the cold-fusion experiments and many of those who read about them have an unusual view of science. To them, lonely scientists spend time working on far-fetched ideas and then suddenly announce a breakthrough that the world accepts as scientific fact. When I studied science I learned that anyone could propose a theory or develop a hypothesis, but that most scientists did so very cautiously and after running many, many careful and duplicate experiments. Only after such painstaking research could scientists be fairly sure that their hypothesis was proven. Obviously, you didn't announce a major finding based upon a few haphazard experiments that yielded nebulous results.

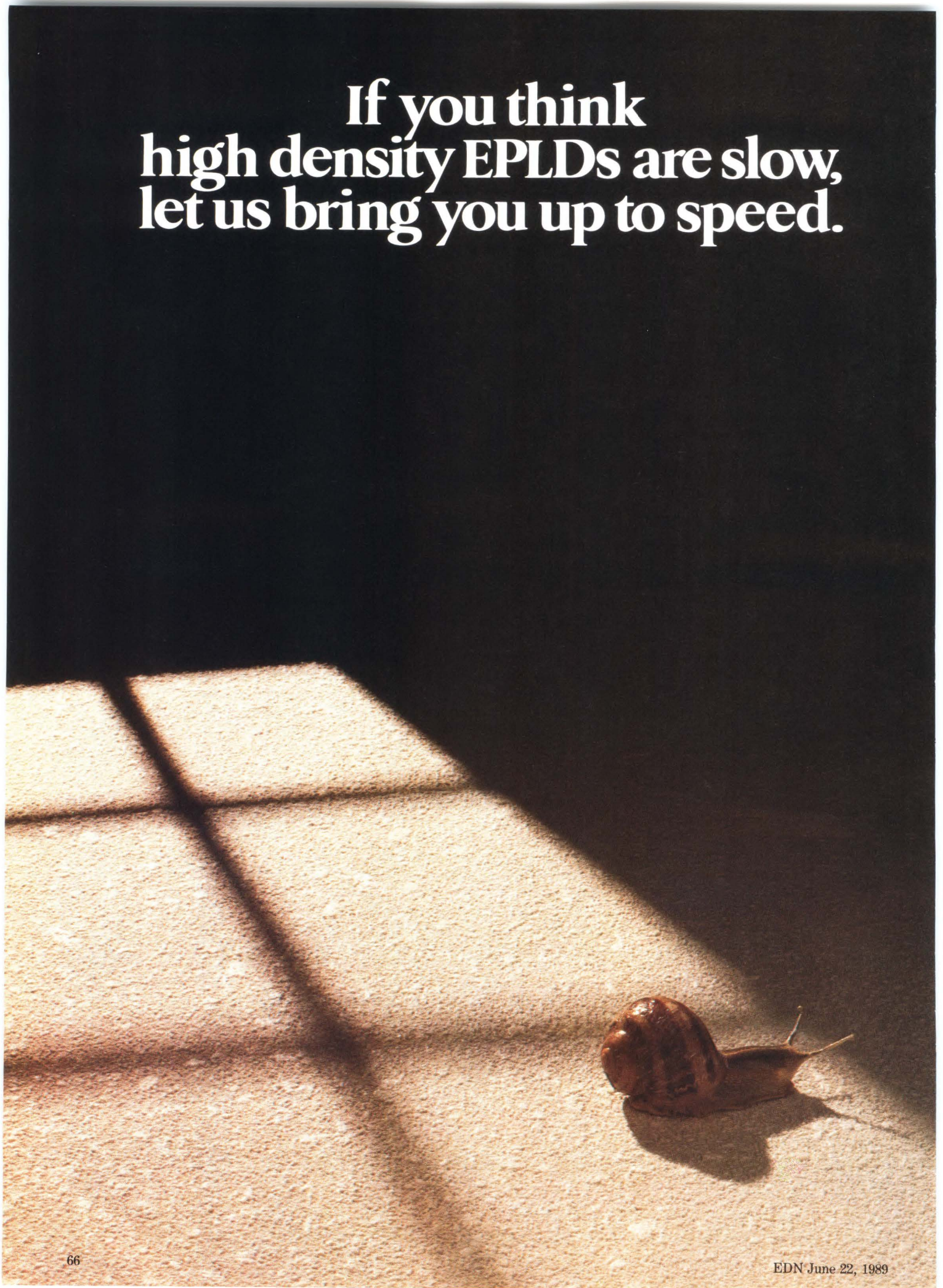
Generally, the press reports about sensational science and not about science as it really takes place. Perhaps the Pons-Fleischmann reports of cold fusion will be proven true, but it will take more research than can be done by a few laboratories in a couple of weeks. Real science demands careful and rigorous experiments that are done by many scientists under carefully controlled conditions. During that time, the press has a responsibility not only to report events fairly, but also to be skeptical about discoveries until they are proven true or false. Maybe it's time to send some of our reporters back to school for a lesson in what science is all about. In the meantime, two scientists could use a reprimand for making wild claims about inflated, extrapolated, and unconfirmed experimental results.

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

Jon Titus
Editor

If you think high density EPLDs are slow, let us bring you up to speed.



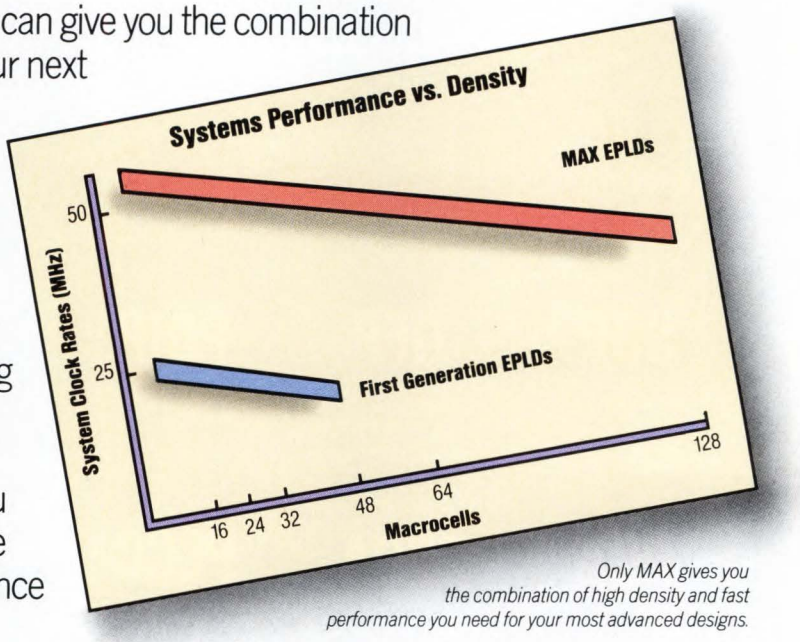
Introducing the MAX family. At up to 50 MHz, it's twice the speed of any other high density EPLD.

MAX is the only family of EPLDs that can give you the combination of speed and density you need in your next system design.

And not just raw speed, but predictable speed as well.

Because MAX's unique architecture gives you predictable delays between all corners of the chip.

And that means no more hair-pulling over lost speed. No gate array timing skews. No more multiple design iterations to get the speed you thought you were going to get in the first place. The result is more usable system performance at system clock rates up to 50 MHz.



Only MAX gives you the combination of high density and fast performance you need for your most advanced designs.

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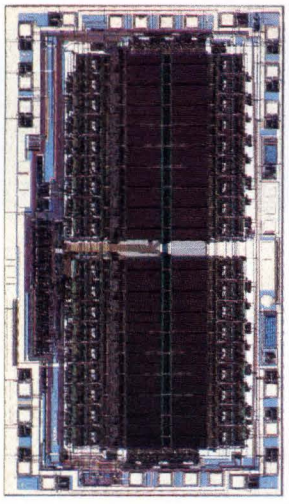

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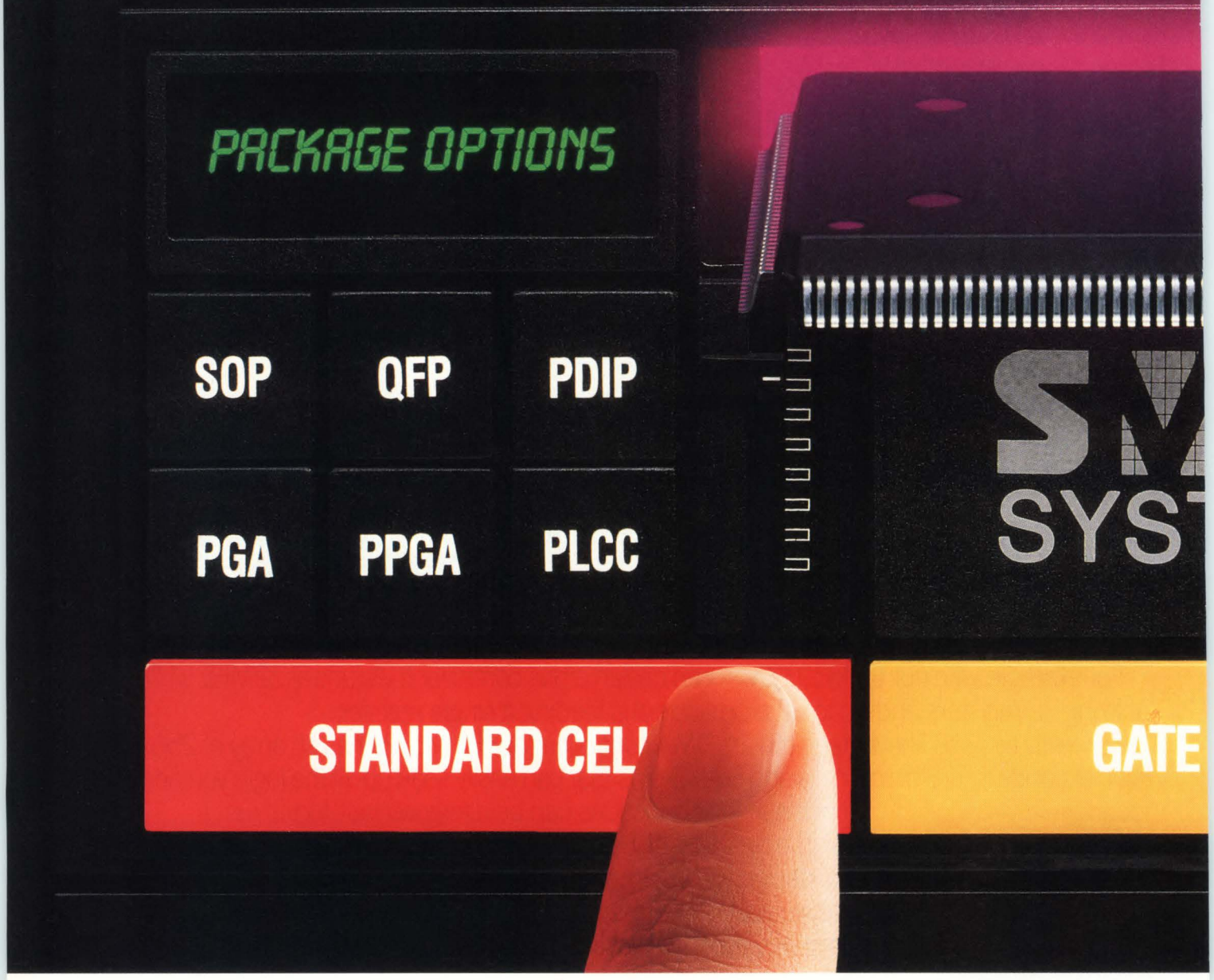

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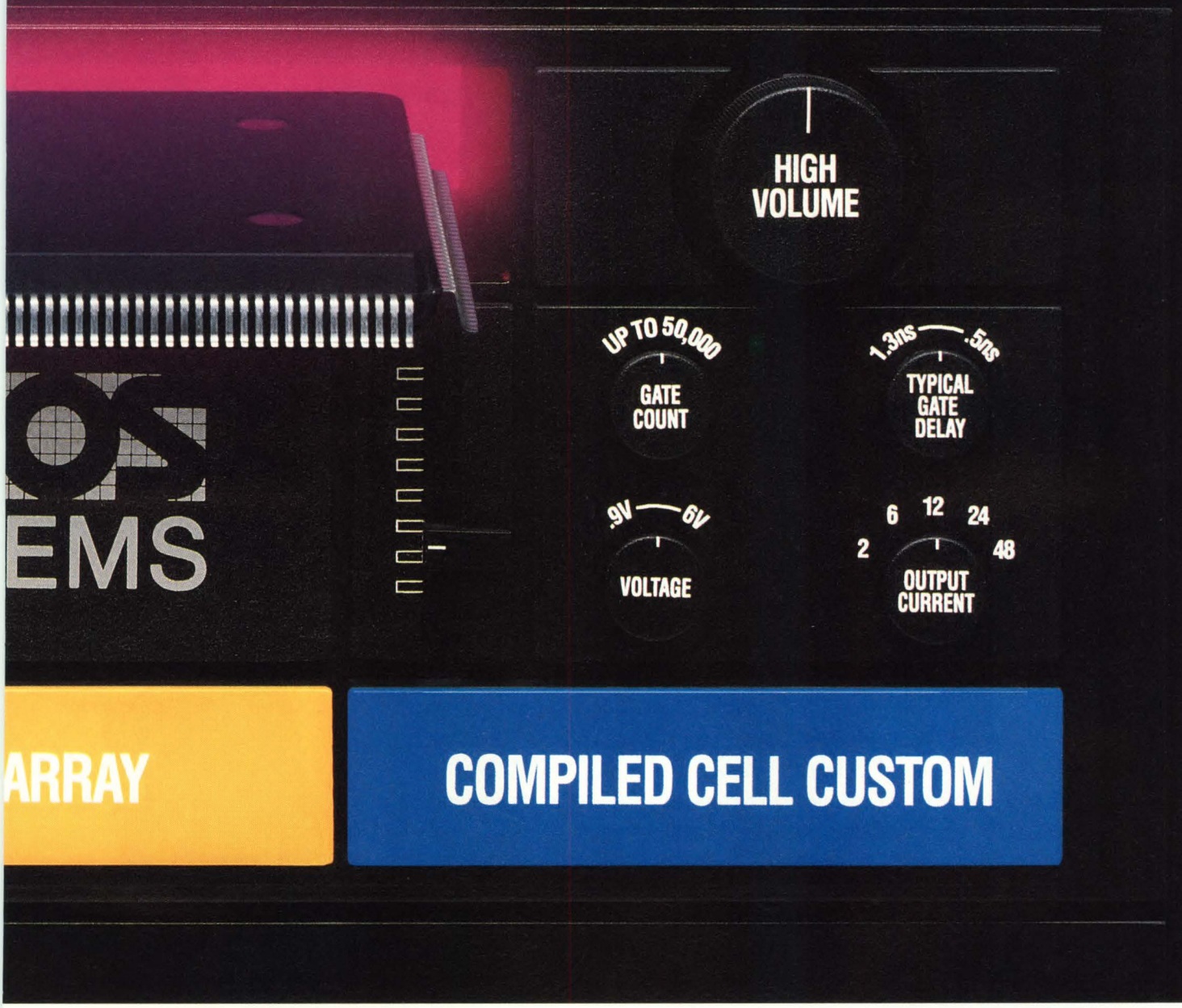

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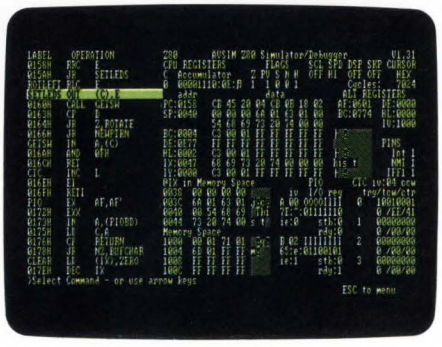

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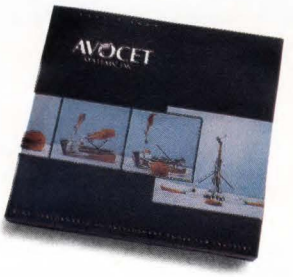

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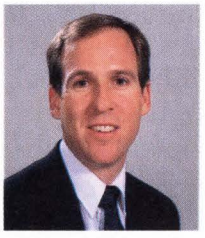
Modularity makes logic analyzers flexible



Modular logic analyzers can be configured for your current requirements, yet they let you add more channels and higher performance as your needs grow.

Doug Conner,
Regional Editor

When you buy an instrument to solve today's design problems, you may wish you had a crystal ball that would tell you what tomorrow's problems will be. That way, you could choose the perfect instruments now. After all, whether your company is large or small, you can't afford to replace expensive instruments too often. Until an accurate crystal ball is invented, however, your best choice is a modular logic analyzer. You can buy a basic version of one of these instruments and add channels later if you need them. In many cases, you can also add higher-performance modules. That way, you buy only as much instrument as you need, and you retain the flexibility to upgrade the analyzer later without losing your earlier investment.

Despite the flexibility of modular logic analyzers, however, you can't buy the lowest priced system and expect to use it for a 32-bit multiprocessor system later. You've got to buy one that has sufficient channel capacity and fast enough clock rates to fit the general performance class you'll be needing.

Whether you're evaluating a standard fixed-configuration logic analyzer or a modular one, you'll need to consider many of the same factors when examining the machines' performance. You'll want to know the synchronous and asynchronous clocking rates, triggering, and display information. **Table 1** shows some of this information for a representative sample of modular logic analyzers. The table concentrates on instruments' maximum capabilities. However, remember that because the systems are modular, you don't have to buy all the available channels until you need them. The prices in the table are for the minimum configuration of each instrument.

A large channel capacity is characteristic of many modular logic analyzers. Although you may not initially need the 200 to 400 channels typically found on the higher-performance modular logic analyzers, some applications, such as 32-bit microprocessors (especially in multiprocessor systems), can require surprisingly large numbers of channels.

In evaluating a logic analyzer, you may want to look at more than just the instrument's actual channel count and clock rate. In order to reduce cost but maintain high clock rates, many

The DAS 9200, now three years old, is still a top performer. *This system still has the highest channel-count capacity at any clock rate from 20 MHz to 2 GHz. Tektronix continues to introduce new modules for this system.*

Modular logic analyzers

manufacturers of both modular and fixed logic analyzers provide high clock rates on a few channels, often just for asynchronous clocking, and let you look at a greater number of channels at lower synchronous or asynchronous clock rates. The concept is generally sound, because you often need high timing resolution only on a few channels, to check timing relationships.

The disadvantage of having a number of tradeoffs in channel count and clock speed is that you must normally reconnect probes when changing the clock speed. To avoid this problem, Gould uses a crosspoint switch on its CLAS 4000. The switch lets you select any channels as the high-speed channels for the company's general-purpose modules, and you don't have to reconnect any probes. This setup allows the fully configured mainframe to support 384 channels at 50 MHz, 192 channels at 100 MHz, and 96 channels at 200 MHz. As long as you have a probe connected to the signal you need, you can vary the clock rate of the channels by means of the user interface, without reconnecting probes.

Instead of multiplexing resources to achieve higher clock rates, some logic-analyzer makers use separate high-performance modules that typically support 1- to 2-GHz asynchronous clock rates. High-performance channels with clock rates of 1 GHz and higher require special high-performance probes with low capacitance and typically lower impedance. Such high-performance modules are available for Gould's CLAS 4000, Hewlett-Packard's 16500A, Kontron's KLA/2, and Tektronix's DAS 9200.

Channel count and clock rate

TABLE 1—REPRESENTATIVE MODULAR LOGIC ANALYZERS

MANUFACTURER	MODEL	BASE PRICE	BASIC NUMBER OF CHANNELS	MAXIMUM CONFIGURATIONS		MAXIMUM AVAILABLE UNMULTIPLEXED MEMORY DEPTH (WORDS)	TRANSITIONAL TIMING	MEMORY COMPARE	TRIGGERING			
				SYNCHRONOUS CHANNELS/ FREQUENCY (MHz)	ASYNCHRONOUS CHANNELS/ FREQUENCY (MHz)				SYNCHRONOUS			
									NUMBER OF WORDS	RANGE RECOGNITION	NUMBER OF LEVELS	DECISION TIME FOR LEVELS (NSEC)
ARIUM	ML4400	$5495	40	320/25, 160/50, 64/100	64/100, 32/200, 16/400	8k	●	●	8	●	14	10
ARRAY ANALYSIS	MFI-1000	$2985	32	384/25	384/25, 192/50, 96/100, 48/200	1k	—	●	1	●	14	40
BITWISE DESIGNS INC	LAC	$2400	40	320/20, 40/25	320/20, 8/100, 40/25	64k	—	●	1	●	16	40
EL TORO SYSTEMS	LA-27200	$1899	24	96/50	96/50, 24/100, 24/200	4k	—	—	24	●	16	20
GOULD	CLAS 4000	$19,950	96	384/50, 192/100	384/50, 192/100, 96/200, 64/1000	4k	●	●	8	●	16	20
HEWLETT-PACKARD	16500A	$12,400	80	400/35	400/100, 80/1000	1k 8k	●	●	8	●	8	28
KONTRON	PLA/2	$11,645	48	192/50	192/100, 96/200	16k	●	●	15	●	12	20
	KLA/2	$22,990	96	192/50	192/100, 96/200, 96/1000, 48/2000	16k	●	●	15	●	12	20
PHILIPS	PM 3655	$4900	24	96/100	96/100	2k	—	●	3	—	4	40
	PM 3570	$7500	35	115/20, 31/50	32/100, 16/200, 8/400	1k	●	●	7	●	7	50
TEKTRONIX	1230	$2995	16	64/25	64/25, 32/50, 16/100	2k	—	●	2	—	14	80
	DAS 9200	$15,527	60	540/20, 384/200	384/200, 160/2000	128k	—	●	16	●	16	5

alone do not make a particular logic analyzer the right one for your application. The instrument's triggering system must also be able to capture the events you want to analyze. Triggering, or trace control, as it is often called, has always been complex. Much to the dismay of the engineer who's unfamiliar with it, triggering is often specified differently by different manufacturers.

One triggering concern in modular logic analyzers that isn't usually a concern in fixed-configuration logic analyzers is the width of the trigger word. Some products, such as Array Analysis's MFI-1000 and El Toro Systems' LA-27200, are limited to the width of one module, or 32 and 24 channels, respectively. A Hewlett-Packard 16500A with 80 channels in a general-purpose module can have trigger words across two modules, giving you a 160-channel-wide trigger word. This configuration is smaller than the instrument's maximum configuration of 400 channels, but it will probably satisfy the needs of most users. Gould's CLAS 4000 can have a trigger word across all 384 channels in its maximum configuration.

TRIGGERING				DISPLAY					
ASYNCHRONOUS									
NUMBER OF WORDS	TIME FILTERS	TRIGGER WORD ACROSS MULTIPLE MODULES	MULTIPROCESSOR APPLICATIONS	SPLIT SCREEN	TIME STAMPING	HISTOGRAMS	HEXADECIMAL DISPLAYS OF BUSES IN TIMING DISPLAY	PROBE LOADING (Ω ‖pF)	NOTES
8	•	•	4	•	•	•	•	150k/6	
1	—	—	4	—	—	—	—	100k/5 TTL	IBM PC/XT, PC/AT OR COMPATIBLE COMPUTER REQUIRED
1	•	•	8	•	•	—	•	1M/15	IBM PC/XT, PC/AT, OR COMPATIBLE COMPUTER REQUIRED, CUSTOM DEVELOPMENT SOFTWARE
24	—	—	—	—	—	—	—	500k/5	IBM PC/XT OR COMPATIBLE
8	•	•	4	•	•	•	•	1M/6 250k/3	INCLUDES COMPUTER
1	•	2	5	•	•	•	•	100k/8 50k/2	
3	•	•	4	—	•	•	•	1M/5	DESKEW CAPABILITY
3	•	•	4	—	•	•	•	1M/5 100k/1.2	DESKEW CAPABILITY
3	•	•	4	•	—	—	—	1M/7	
4	•	•	—	•	•	•	—	1M/5	
2	•	•	—	—	—	—	—	1M/8	
16	•	•	6	•	•	•	•	1M/15 10k/1	

Not every designer needs such a wide trigger word, but if you deal with 32-bit processors in multiprocessor applications or in special applications such as dual-port RAMs, you may find you need these large trigger words.

Combine multiple trigger words

Once you know how wide a trigger word can be, you might be interested in how many trigger words a particular analyzer provides. Most logic analyzers let you combine multiple trigger words logically (usually with AND, OR, and NOT) for each of several decision levels. The trigger sequence progresses by satisfying each decision level in turn until the last level is satisfied and data is acquired.

For hardware analysis, you typically don't need lots of word combinations or trigger levels. For software analysis, you'll require more words and levels to help you zero in on a particular subroutine entered through a specific path. Note that some manufacturers' specifications list the total number of words you can recognize at each level, multiplied by the number of levels. This information can be misleading if you think you can use all those words in a combination at one level.

Decision levels are not handled in a standard manner in the logic-analyzer industry. Some logic analyzers offer sequential decision levels that don't allow branching. Others allow branching, and some offer states that can be used more than once, so that trigger decisions can be looped.

Triggering changes with speed

Logic analyzers typically offer sophisticated triggering functions with many decision levels for slower clock rates, especially when the analyzers are operating in the external or synchronous clocking mode. For higher clock speeds, the

Modular logic analyzers

instruments don't offer as many triggering functions, because it's difficult for the manufacturer to set up all the data for the next trigger level between clock cycles. As a result, at high clock rates, analyzers often provide only one decision level for triggering. If you need sophisticated triggering at high clock rates, make sure that when you evaluate a particular logic analyzer, you understand which triggering functions work at the higher clock rates and which don't. Data sheets don't always include such information.

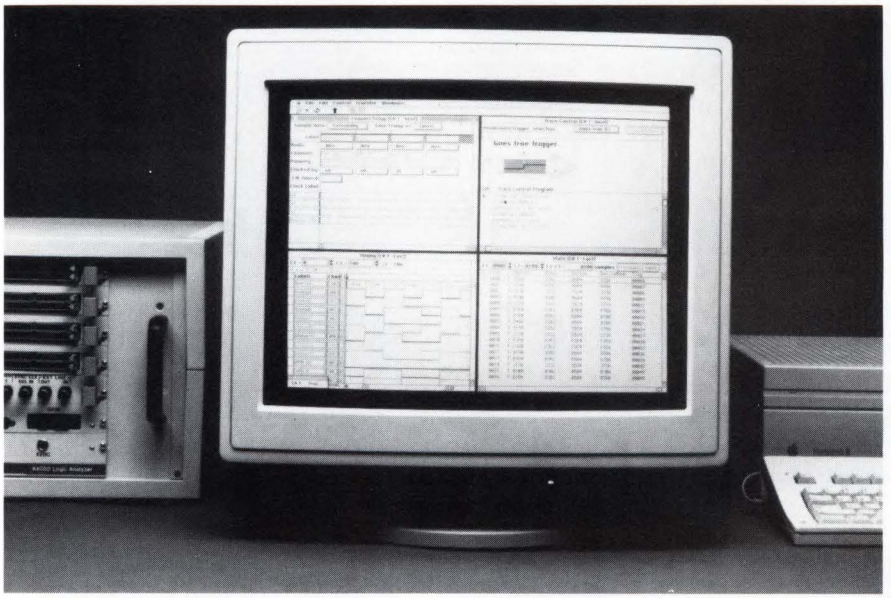
Another trigger feature that has become almost a standard feature on logic analyzers is the time filter. Time filters do vary somewhat, but their basic function is to make sure that a trigger word exists for at least some specified length of time before the instrument triggers on it. Variations of the time-filter function include checking for a "not-greater-than" time in addition to the "not-less-than" time. You might need a time filter while the logic analyzer is clocking asynchronously, for example, to keep it from triggering on a temporary condition before a bus has settled and the data is valid.

A triggering feature that's fairly standard—at least in concept, if not in implementation—is range recognition. Range recognition lets you trigger easily on data or addresses that fall within a certain range. Range recognizers typically vary in width from 8 to 32 bits. Implementations of range recognizers differ; some logic analyzers use memory look-up tables, and some use register comparisons. Memory look-up tables aren't as wide, but they can trigger on multiple ranges and addresses.

In addition to examining the triggering capabilities of modular logic analyzers, you may want to look into the instruments' acquisition-memory capacity, which varies widely. **Table 1** shows the maximum capacities available for the systems listed. These maximums are not necessarily available on every type of module that each manufacturer offers. Further, the values in the table are given for operations that use the highest channel count at the lowest clock rate. Systems that multiplex channels normally offer higher memory capacities when operating with high clock rates and low channel counts.

Tektronix's DAS 9200, which offers 128k words on some modules, has the greatest memory depth

Recently upgraded, the general-purpose logic-analysis modules *for the 16500A from Hewlett-Packard now support 35-MHz synchronous clocking and a memory-compare capability. High-performance modules support clock rates reaching 1 GHz.*



Providing as many as 384 channels at 50 MHz, *or fewer channels at clock rates reaching 1 GHz, Gould's CLAS 4000 has a broad range of capabilities to take on demanding problems. The system requires an Apple Macintosh for control and display. When used with a Macintosh II, it supports multiple large display windows.*

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Modular logic analyzers

available, but that's not the entire story. The DAS 9200 doesn't use transitional timing. Transitional timing is a recording method that lets you measure events with high timing resolution even though they may be separated by long intervals.

Conventional timing analysis records the state at every clock cycle that exhausts the logic analyzer's memory in a period equivalent to the clock period times the memory depth. Transitional timing checks a group of channels every clock period to see if it has changed state, recording the time whenever it sees a transition.

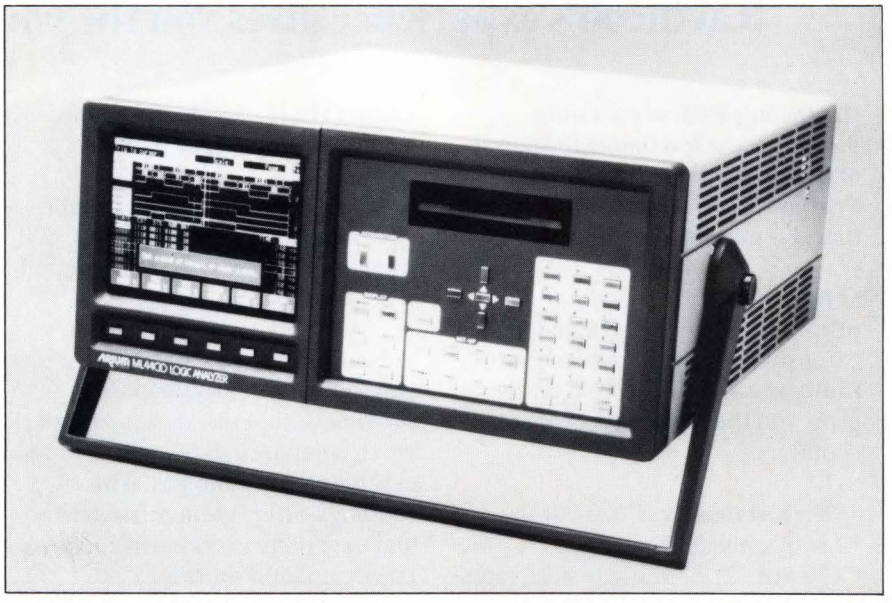
If you're looking at a group of signals that changes every clock period, transitional timing buys you nothing. If, however, you're looking for an infrequent event, you can, depending on the system, record events that happen hours or even days after the trigger.

Tektronix's competitors claim that Tektronix had to offer the long memory on the DAS 9200 because the instrument doesn't offer transitional timing. Tektronix defends itself by noting that you usually need to know the timing of a signal in relation to other signals, and one of those other signals is usually the clock on the circuit you're examining. A fast clock, therefore, will consume memory fairly quickly even on instruments that have transitional timing.

On the other hand, when operating at high asynchronous clock rates, a logic analyzer is often sampling signals 10 or more times faster than the rate of the clock on the circuit under examination. Therefore, when the logic analyzer uses transitional timing, you might expect to be able to examine a period 10 times as long. However, remember that the more state changes there are, the more memory gets used up. It won't be a clear tradeoff for you, either; you'd probably like to have both a long memory and transitional timing. Which one you'll need more simply depends on the particular measurement problem you are facing.

***Designed for high-performance applications**, the KLA/2 from Kontron supports 192 channels at 50 MHz plus additional high-speed modules that are capable of 2-GHz clock rates. The system is available both in a portable 10-MHz IBM PC/AT-compatible version (shown here) or as a separate computer-controlled mainframe with two additional card slots. The unit has built-in channel-deskewing capability. A hexadecimal display of the address and data buses is next to the timing display.*

When you shop for a logic analyzer that has transitional timing, make sure you understand how the transitional timing works; every manufacturer has its own twist. For



***Providing a good blend of channel width and speed** in a moderately priced portable logic analyzer, the ML4400 from Arium supports 320 channels at 25 MHz, 160 channels at 50 MHz, and other configurations to as many as 16 channels at 400 MHz. It supports histograms and other time-measurement features found on many of the higher-priced systems.*

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example, on Hewlett-Packard's 16510A module, the transitional timing comes in channel groups of 16. Any time a transition happens on any channel in the group of 16 channels, therefore, a word of memory across all 16 channels is used. To get the maximum number of transitions from this system, you'd have to use only one channel in the group of 16 and leave the rest in an inactive state.

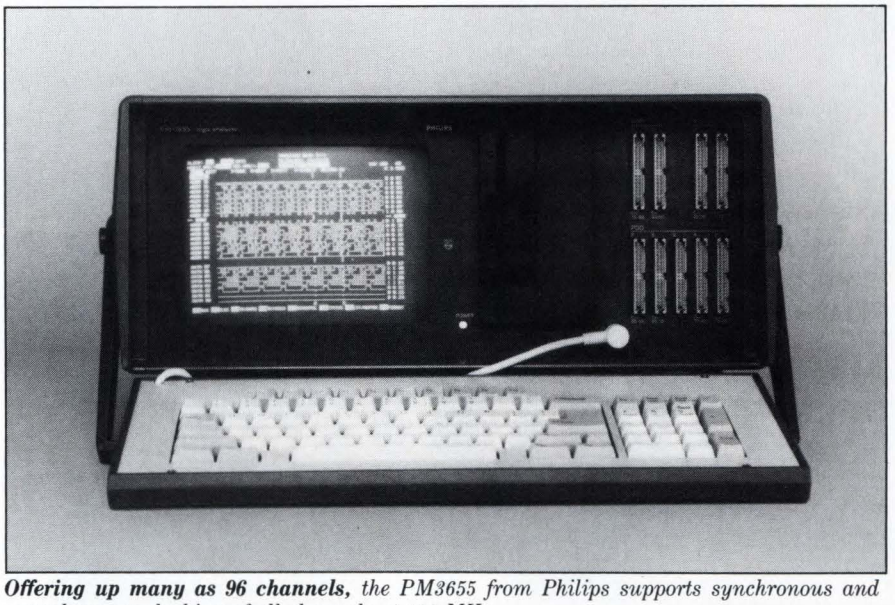
Compare the memory compare

Once you've got the data in memory, regardless of whether or not you use transitional timing, you'd often like to compare the data with data you've stored previously. Including a versatile memory-compare capability on a logic analyzer isn't as easy as it may sound at first. It's one thing to compare acquired data bit by bit with data in memory. Every logic analyzer in **Table 1** for which a memory-compare feature is listed does at least that.

Some logic analyzers have additional features that are necessary for getting the most from a data comparison. For example, some allow you to put a "don't care" condition on certain fields of the data so they won't be compared.

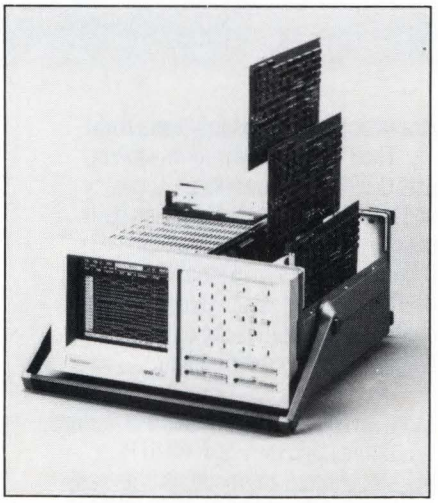
Some also let you set the compare function to disregard transitions that differ by one or two clock cycles. This feature comes in handy for acquiring data with an asynchronous clock. In such a situation, it would be quite unlikely for two acquisitions of data from the same circuit to be identical. At least some of the data transitions will vary by one clock cycle, causing a mismatch, unless you set the compare function to ignore such variations.

Still other logic-analyzer features may come in handy for particular applications. If you'll use your logic analyzer for developing and debugging microprocessor-based circuits, it's obviously of paramount importance for you to check on the microprocessor support available for the instrument you're considering.



Offering up many as 96 channels, *the PM3655 from Philips supports synchronous and asynchronous clocking of all channels at 100 MHz.*

One related consideration that can be confusing is the question of what synchronous clock rate your application will require. Although microprocessor manufacturers claim their chips run at speeds of 25 or 33 MHz, these numbers are clock-oscillator rates, not bus rates. You use a logic analyzer to look at bus rates. In general, microprocessor bus rates fall well below 20 MHz, although some RISC processors and microprocessors with caches can exceed those speeds.



Expandable from 16 to 64 channels, *the 1230 from Tektronix is suitable for 8- and 16-bit microprocessor applications.*

Multiple timebases

If your applications include multiprocessor systems, your logic analyzer will have to acquire data externally and simultaneously from multiple sources. Most of the higher-performance logic analyzers can operate on independent time bases on a per-module basis. These machines typically (as long as they have enough channels) let you examine four or more processors.

When you get involved with multiprocessor applications, you not only need the ability to operate with multiple timebases, but you need some way to correlate data by time so that you know what each processor is doing at a given time. The usual way to accomplish this end is to use time stamping.

Time stamping, as the name suggests, records the time at which a logic analyzer takes a sample. Time stamping enables the logic analyzer to display cursors, highlight simul-

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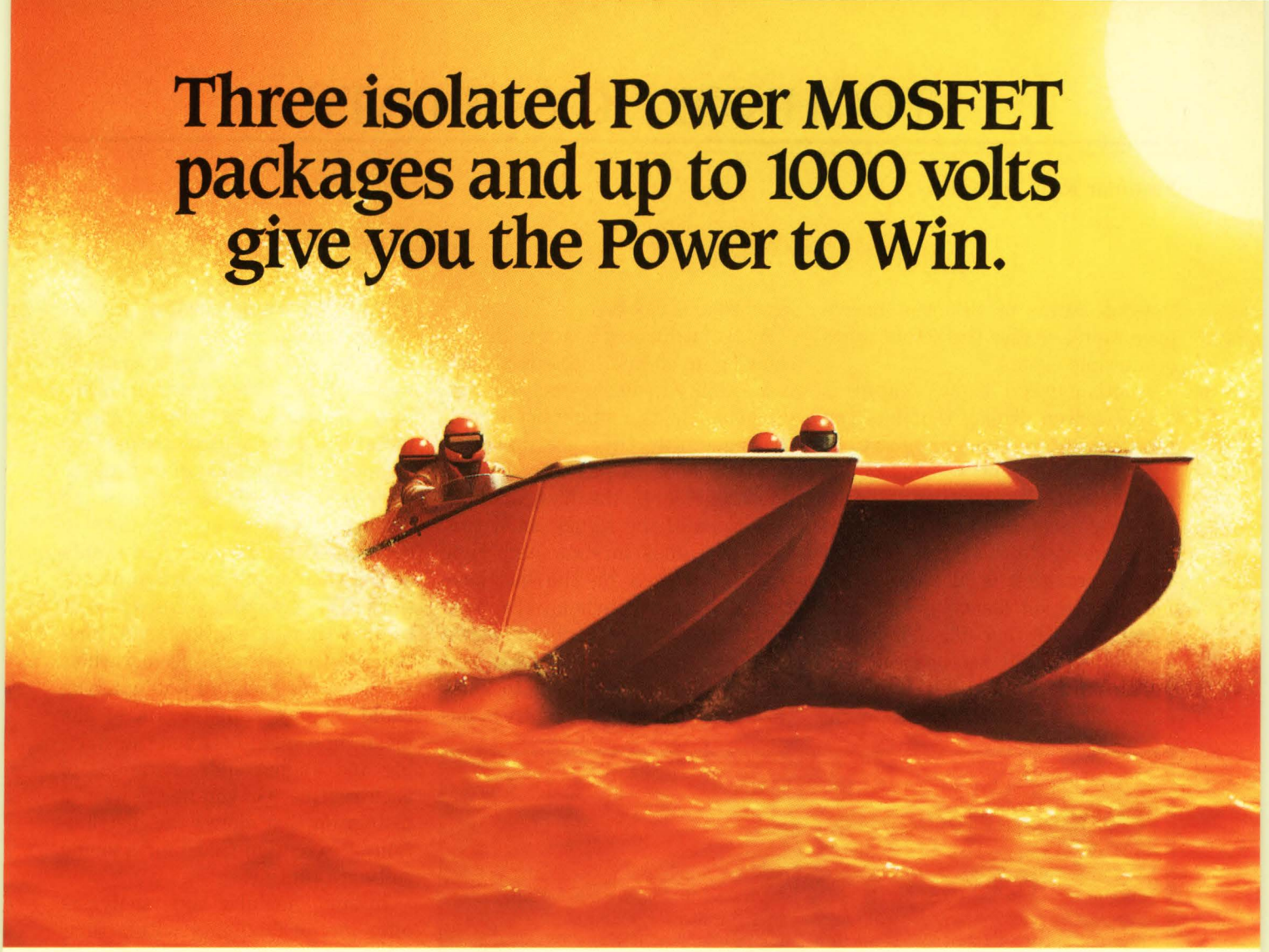

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CIRCLE NO 79

taneous events on different microprocessors, or give the actual times of multiple events.

Another useful display feature is a split-screen display that lets you view both state and timing data at the same time. Split screens can be useful for troubleshooting potential timing-related problems on synchronous systems. Some form of time correlation is also necessary for split-screen displays, and time stamping with time-aligned cursors is common. Split screens can also permit simultaneous viewing of state data acquired with different synchronous clocks.

A useful display feature that is showing up on many logic analyzers is the ability to display multiple timing channels as a single bus signal, the same way they are displayed in a data book. A pair of horizontal lines represents the high and low conditions of the signal; an X connects the lines to show each time that the signals on the bus have changed state. Between the horizontal lines is the bus's hexadecimal value. This feature can be a real timesaver when you want to know the value on a data or address bus while using timing displays.

Logic analyzers are often used to examine software performance as well as that of hardware. To facilitate this use, logic-analyzer manufacturers have added histograms and other timing-related features to their products. These features can perform a variety of operations to determine the frequency of events or the time spent in certain operations. For example, you may want to know how much time your real-time system is spending in various software routines. To find out, you could display a histogram of the mean time spent between the starting and ending address ranges of each routine. Or you might want a histogram that shows the distribution of execution times for a single software routine.

In sum, modular logic analyzers offer lots of flexibility within their general operating classes. Careful consideration of your logic-analysis needs—both present and future ones—can help you choose a system that can adapt to your changing requirements instead of becoming obsolete. EDN

For more information . . .

For more information on modular logic analyzers, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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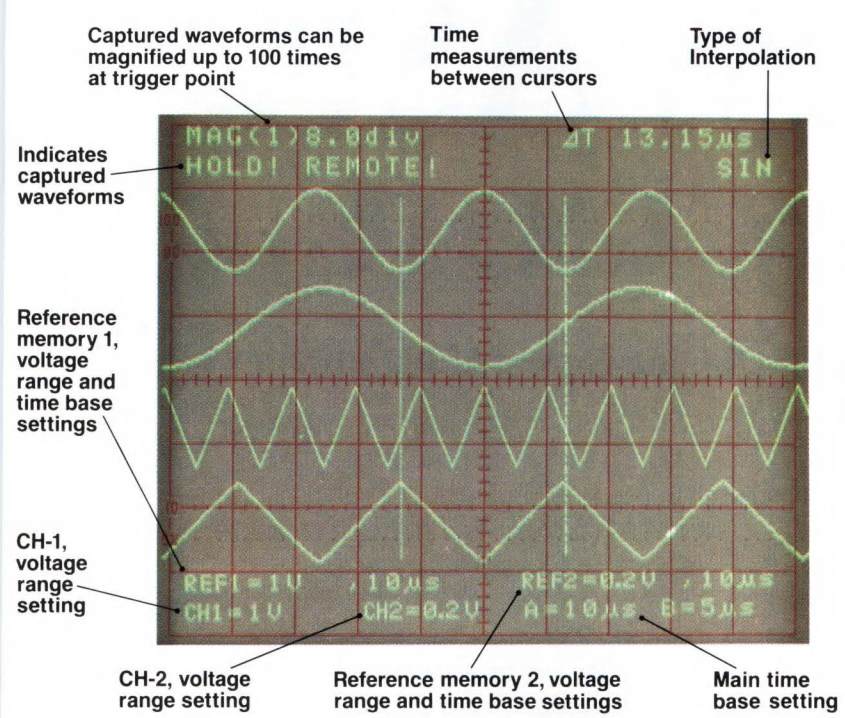

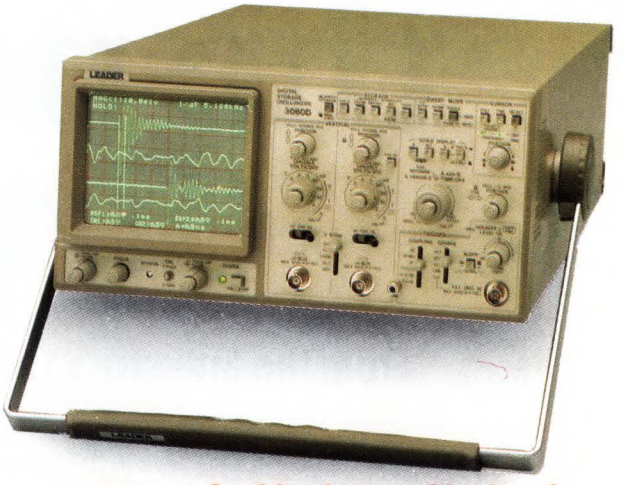

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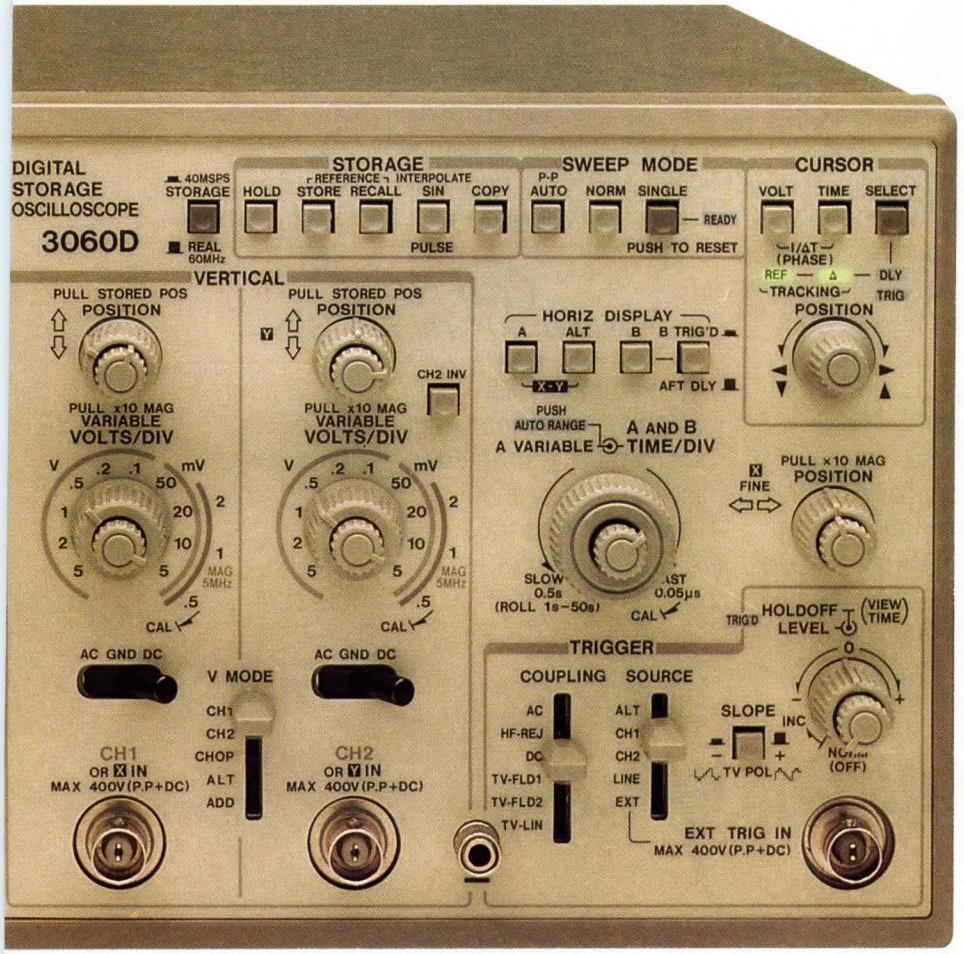

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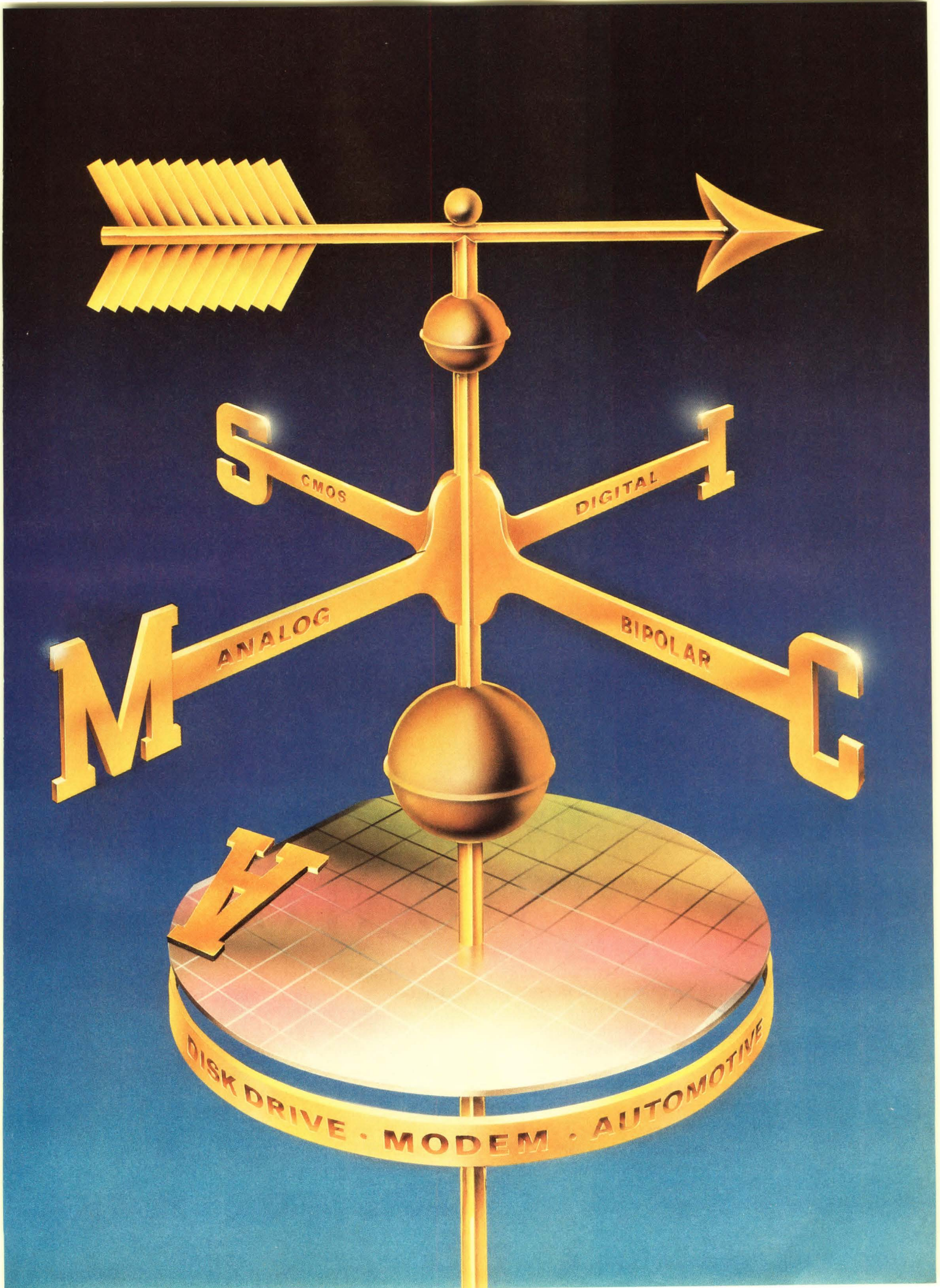
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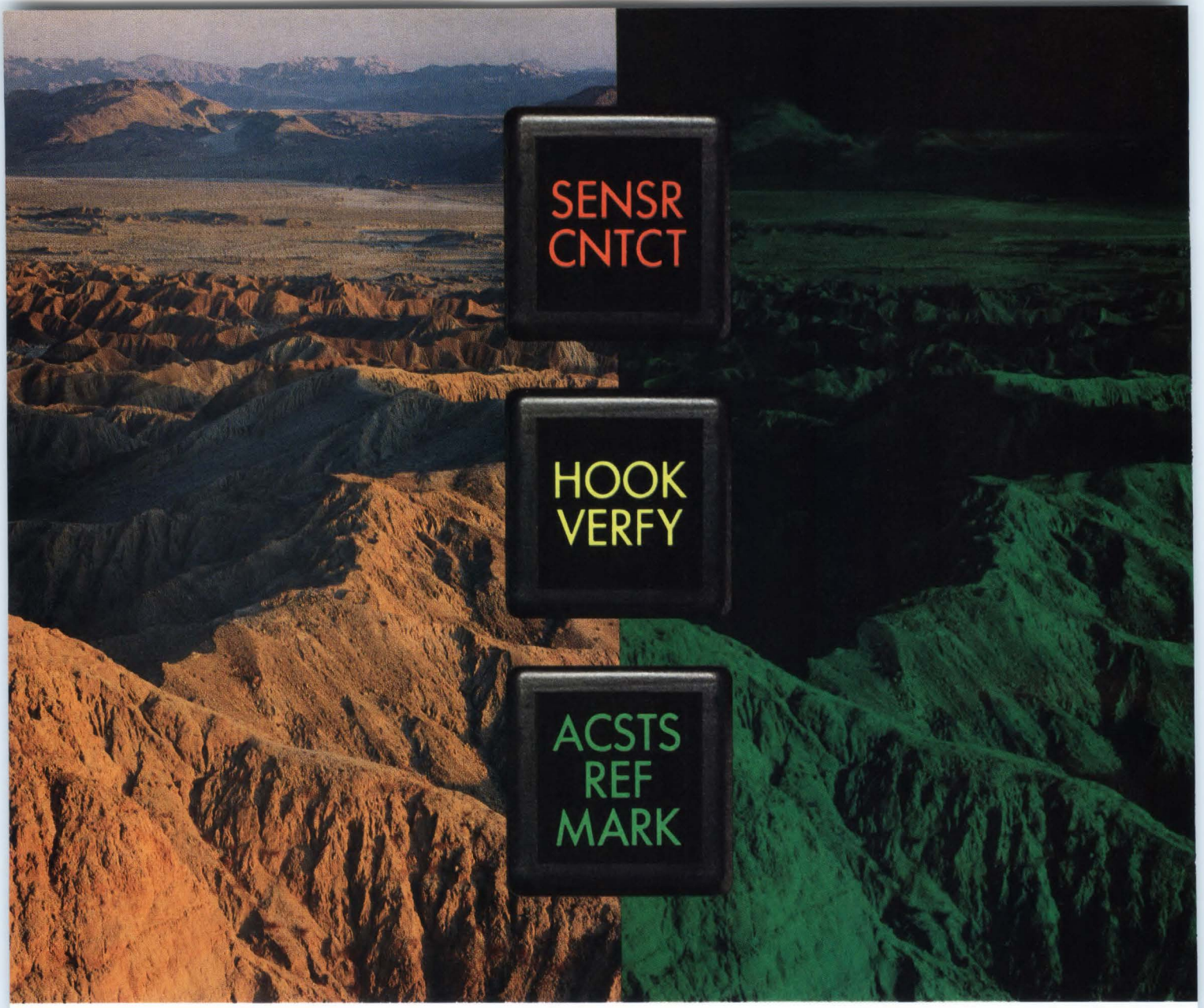

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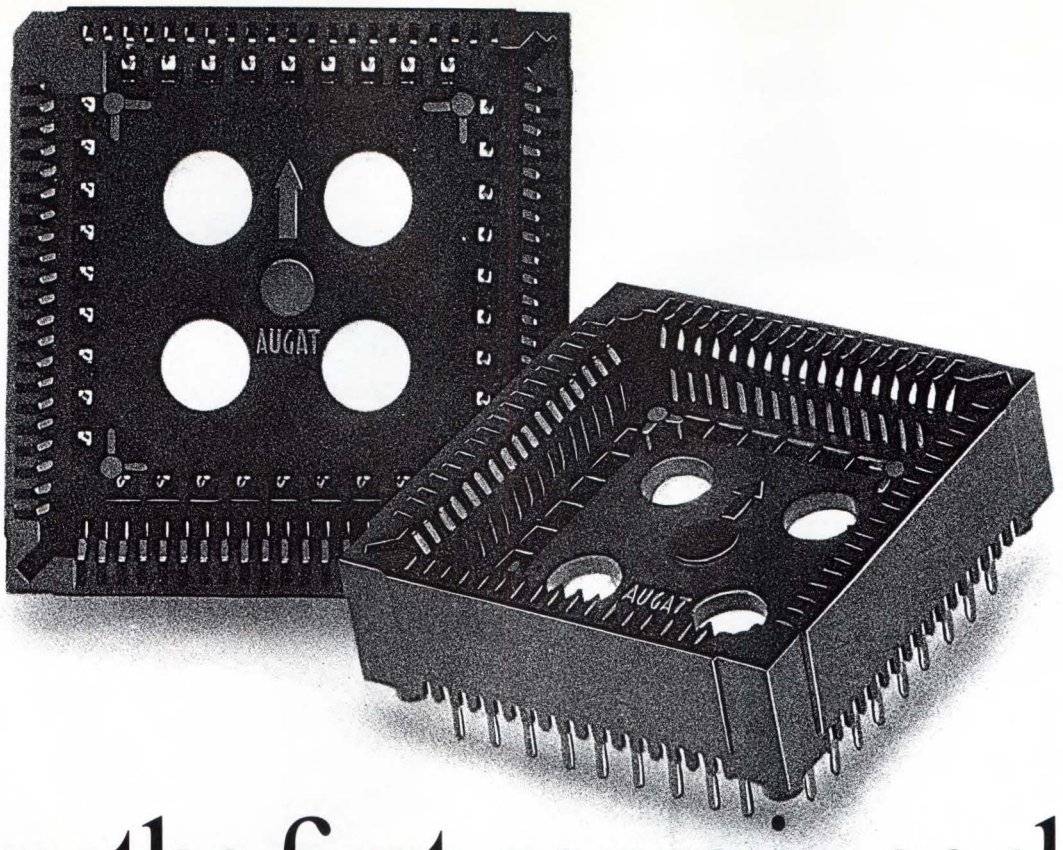

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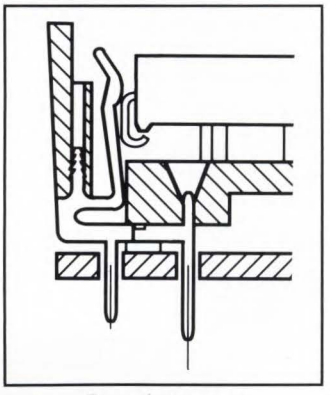

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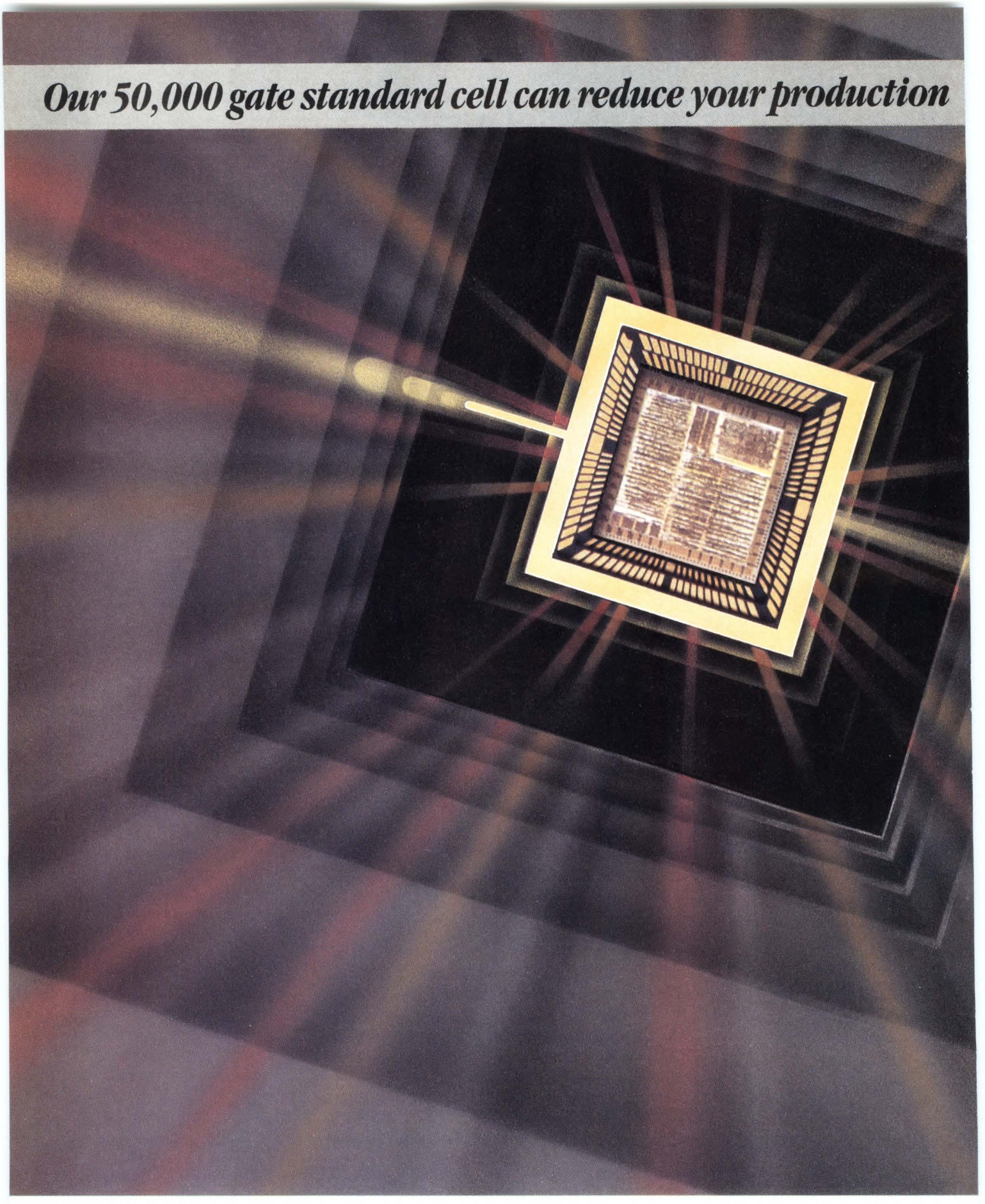

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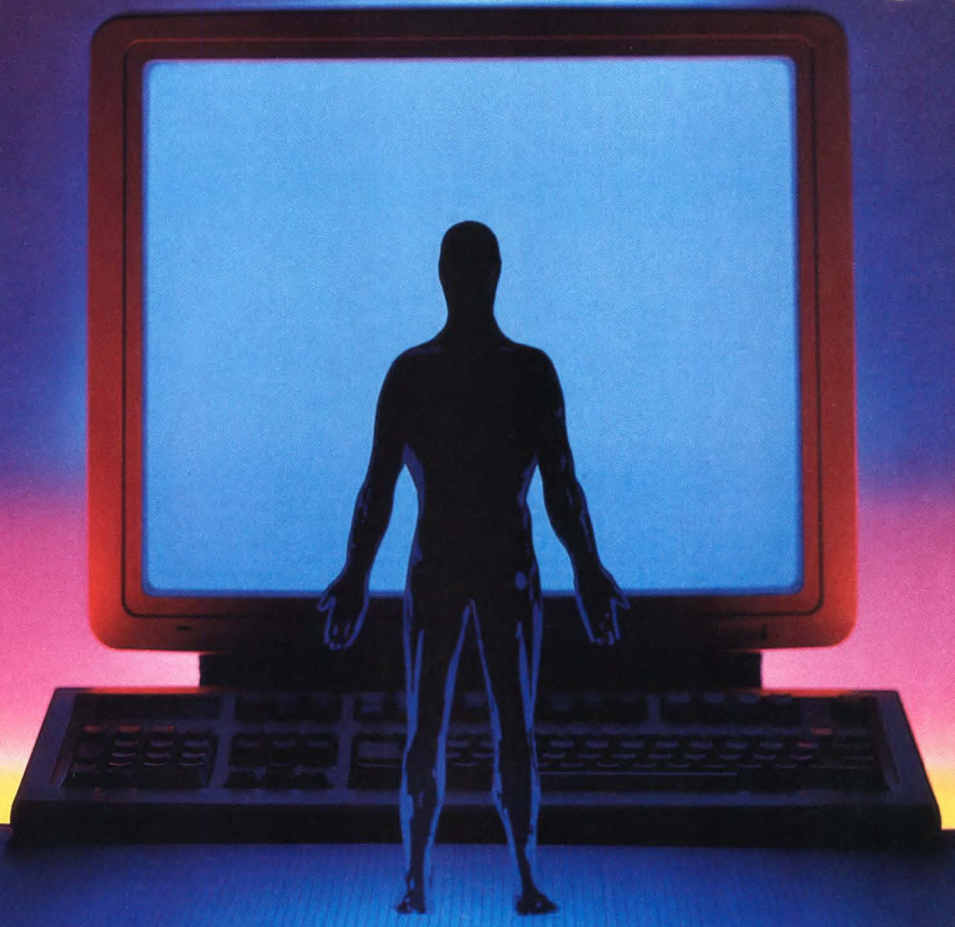

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THERMAL-MANAGEMENT PRODUCTS

Circuit design requires thermal expertise

Don't view your circuit in purely electrical terms; consider the thermal circuit as well.

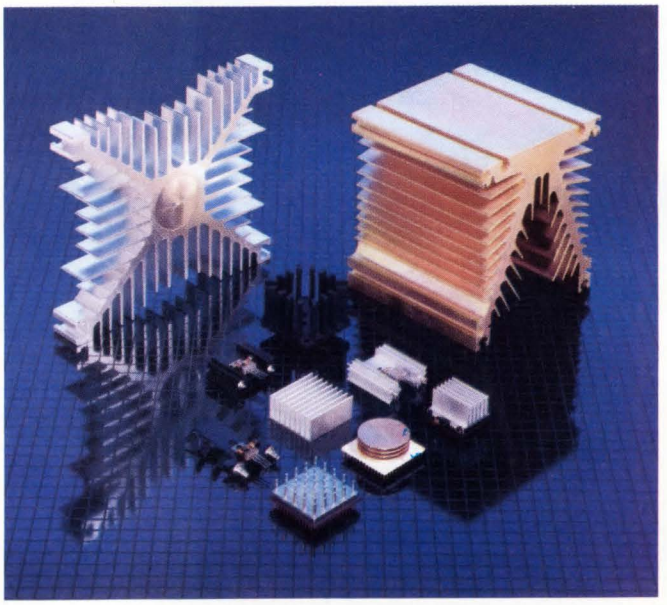
Anne Watson Swager,
Associate Editor

Thermal Management isn't a graduate program offered by MIT, but every electrical engineer involved in circuit design or printed-circuit-board layout should master the subject. As ICs and circuit boards increase in transistor and device density, you must design and lay out your circuit with temperature effects in mind. Heeding thermal effects helps ensure your circuit's reliability and performance. Neglect to do so and you risk device destruction.

Knowing some of the basics of semiconductor heat-transfer theory will go a long way toward solving some of the heat-related problems you'll encounter in product development. There are a tremendous variety of heat-sink products available to help you solve such problems. These products include single-device solutions, such as individual heat sinks; and custom-board solutions, such as thermal substrates. You'll even find liquid heat sinks—bags filled with a liquid that transfers heat via fluid convection.

Admittedly, most designers of military equipment are well acquainted with reliability issues inherent in thermal management. Military programs demand, and are provided sufficient funds for, the time and labor required to ensure a design's reliability. However, heat-sink manufacturers deal with many engineers who ignore thermal effects until after their circuit design and pc-board layout have reached the point of no return. This after-the-fact approach only serves to limit an engineer's heat-sinking options, and, depending on the problem's severity, may cause expensive delays in a new product's introduction. You can avoid such problems if you consider thermal effects from the start.

The ultimate goal of any heat-removal system is to maintain the semiconductor junction at a safe operating temperature. By doing so, you're not only protecting the device from destruction, but also ensuring its optimum performance.



The size and variety of heat-dissipation devices, *such as these from EG&G Wakefield Engineering, illustrate the many existing solutions to heat problems. In order to choose the appropriate heat sink or overall thermal-management approach, you need to take some basic thermal characteristics into account.*

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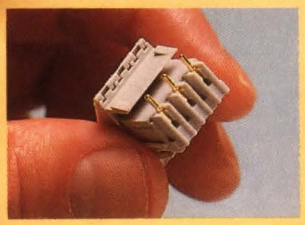

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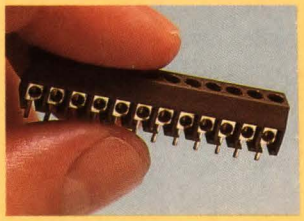

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Thermal-management products

One parameter has the greatest effect on junction temperature: the overall thermal resistance between the junction and ambient air. Several electrical and mechanical components contribute to this resistance, and the best way to view these components is to think in terms of the thermal model (**Fig 1**).

The thermal components shown in **Fig 1** are analogous to electrical components; Θ is the thermal resistance between two points and is analogous to resistance. C_T is the heat capacity and is analogous to capacitance. Certain thermal characteristics also have electrical analogues; ΔT is the temperature difference between two points and is analogous to voltage; K is the thermal conductivity and is analogous to electrical conductivity, (σ), and P is the power generated or dissipated and is analogous to electrical power in watts.

In general, the thermal resistance between any two points is defined as the temperature drop divided by the heat (power) passing between them. This relationship is stated mathematically as

$$\Theta=\frac{\Delta T}{P_D},$$

where Θ is the sum of all of the resistances between the two points of interest, such as junction and ambient, and ΔT equals the temperature difference between those two points.

This equation can take a number of forms. For instance, **Fig 1**'s model includes two resistive paths over which heat can travel from the junction to the ambient environment. When there is no heat sink present, the junction-to-case thermal resistance, $\Theta_{J\text{-}C}$, and the case-to-ambient resistance, $\Theta_{C\text{-}A}$, determine the amount of heat flow. In this case, you can rearrange and rewrite the equation as follows:

$$P_D=\frac{T_J-T_A}{\Theta_{J\text{-}C}+\Theta_{C\text{-}A}}.$$

If you use a heat sink, the heat-travel path includes three resistance specs: $\Theta_{J\text{-}C}$; the case-to-sink thermal resistance, ($\Theta_{C\text{-}S}$); and the sink-to-ambient thermal resistance, $\Theta_{S\text{-}A}$. In this case, the equation would read as

$$P_D=\frac{T_J-T_A}{\Theta_{J\text{-}C}+\Theta_{C\text{-}S}+\Theta_{S\text{-}A}}.$$

One resistance spec that is common to the latter two equations is the semiconductor device's junction-to-case thermal resistance. $\Theta_{J\text{-}C}$ depends completely on the device's design; you have no control over its value, and you must rely on specs given by the manufacturer. $\Theta_{J\text{-}C}$ is generally quoted for a device's highest-power semiconductor junction, such as a drive transistor in the output stage.

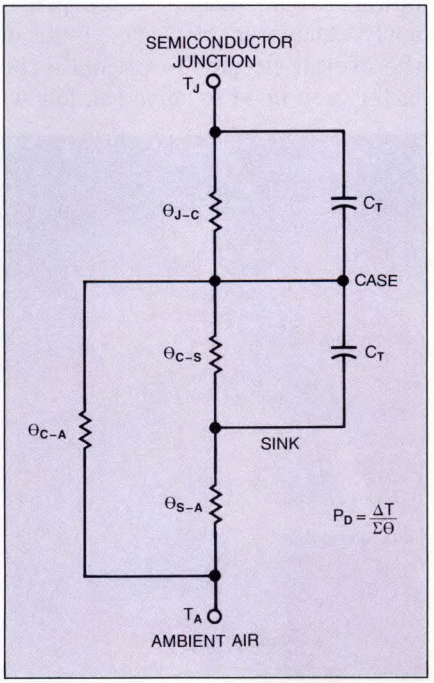


Fig 1—It's important to consider this thermal model *when you design your circuit. In order to achieve the desired performance and to ultimately protect the device from destruction, you must ensure that the junction temperature never exceeds its maximum value.*

The data sheets for most ICs designed for power applications prominently display $\Theta_{J\text{-}C}$, but you might be surprised at the number of devices whose data sheets don't quote this junction-to-case resistance. Apparently, semiconductor manufacturers quote it only for those components that they anticipate will require heat-sink calculations. Many semiconductor manufacturers offer this information in separate publications, such as reliability handbooks.

On the other hand, certain data sheets provide you with so much information that they practically do your job for you. Some even suggest a specific heat-sink manufacturer and part number. They also give you enough technical information to calculate certain values to determine whether they exceed maximum ratings.

For instance, Analog Devices quotes both $\Theta_{J\text{-}C}$ and $\Theta_{C\text{-}A}$ for its AD9620 wide-bandwidth, fast-settling op amp. The data sheet also provides a thermal model and formulas based on the part's design to help you solve for power dissipation. Burr-Brown's 3571 data sheet includes a discussion of thermal considerations and some necessary formulas. Harris's HA5190 data sheet provides some brief notes and heat-sink suggestions.

In addition to the device-dependent thermal-resistance specs, **Fig 1** includes two other resistance values for the instances when you will use a heat sink. $\Theta_{C\text{-}S}$, the thermal resistance between the case of the semiconductor device and the heat sink, depends on the material you use as the interface and the mechanical connection between the device and the heat sink. The last resistance

is $\Theta_{S\text{-}A}$, which is the thermal resistance between the heat sink and ambient air.

Fig 1 also includes two energy-storage elements, denoted C_T, to illustrate the transient thermal properties of semiconductors. C_T affects heat transfer in pulsed-power situations, but most thermal calculations are based only on steady-state conditions, and thus deal only with thermal resistance values.

Solve for the unknown

You can use any form of the thermal equations, including the two given above, to solve for unknown quantities. For instance, given fixed thermal-resistance values, you may want to determine the maximum allowable ambient temperature. Or, you may want to solve for the desired thermal resisltance of an external heat sink.

Instead of simply plugging values into this equation, you can take a more intuitive approach. Consider the thermal drop that must take place at each stage from the junction to ambient to ensure safe operation. Basically, you work your way out from the semiconductor junction to the ambient air, calculating the temperature drop at each step.

To begin, you'll need to know the maximum junction temperature and the junction-to-case thermal resistance. Using the AD9610 as an example, you'll find that the manufacturer specifies a maximum junction temperature of 165°C and a junction-to-case thermal resistance of 210°C/W. To determine the heat dissipated between the junction and the case, you'll need to calculate the power in the output stage. Analog Devices provides the following formula:

$$P_{XXX}=[(\pm V_{CC})-V_{OUT}-I_{COL}(8)]\times(I_{COL})(\%\ \text{DUTY CYCLE}).$$

The collector current, I_{COL}, equals V_{OUT}/R_{LOAD} or 3 mA, whichever is greater. (Note: Some power-dissipation equations given by manufacturers are tailored specifically to their devices, and depend on operating and load conditions. Still, the equations are all essentially $P=VI$.)

If $V_{CC}=15V$, $V_{OUT}=4V$, $R_{LOAD}=50\Omega$, and the duty cycle is 50%, the power dissipated by the output stage is 0.414W, which, when multiplied by 210°C/W, yields 87°C. Thus, the maximum case temperature you can allow if you want to limit the junction's temperature to 165°C max is the difference between 165 and 87, or 78°C.

Now, to work out from the case to ambient air, multiply the case-to-ambient thermal resistance by the total power that the device dissipates. This total power includes the power of the output stage previously calculated *and* the power of the overall circuit. To calculate the latter, you need to solve the following equation provided on the AD9610's data sheet:

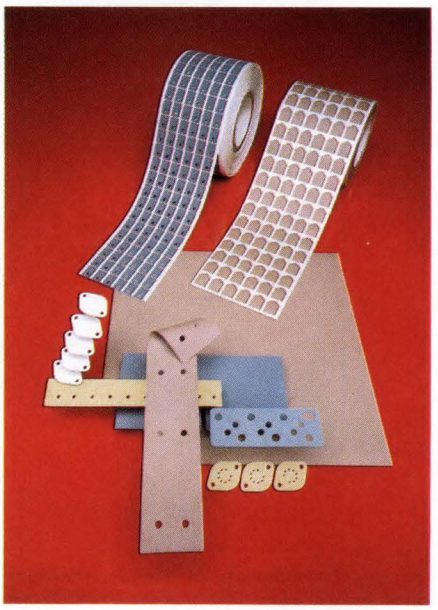
$$P_{CIRCUIT}=I_{CC}[V_{CC}-(-V_{CC})].$$

The data sheet specifies a supply current of 21 mA when $V_{CC}=15V$. $P_{CIRCUIT}$ then equals 0.63W, and the total power is $0.63+0.414$ or ~1W. Using the $\Theta_{C\text{-}A}$ value from the data sheet, which is 65°C/W, you can solve for the case-to-ambient temperature drop: $65°C/W\times 1W=65°C$. This 65°C drop between the case and ambient implies that to maintain a case temperature of 87°C, your ambient temperature can't exceed 13°C.

In this manner, you can work your way from junction temperature to ambient temperature or vice versa to see if you exceed any maximum temperature ratings. If you decide to include a heat sink, you can use the same method to determine the device's maximum thermal resistance.

If you perform these calculations, heat-sink manufacturers will be able to present you with a variety of different solutions for your circuit. Even if you choose not to go through the calculations yourself and simply anticipate that you'll need a heat sink, you still must supply a minimum amount of information to the heat-sink manufacturer.

According to Gary Kuzmin, a project engineer at IERC, many engineers call heat-sink vendors before they've defined their system's needs. If you want a heat-sink manufacturer's assistance, you'll need to provide the same information that you would need if you were going to perform the calculations yourself. Namely, you'll need to know the values for $\Theta_{J\text{-}C}$, P_D, T_J, and T_A. Some heat-sink vendors recommend that you add a safety margin to the manufacturer's absolute rating of T_J; that is, choose a



The thermal resistance from case to sink *is determined by the quality of the interface. Grease performs well but is messy and takes time to apply. Berquist's Sil-pads are an easy-to-install option.*

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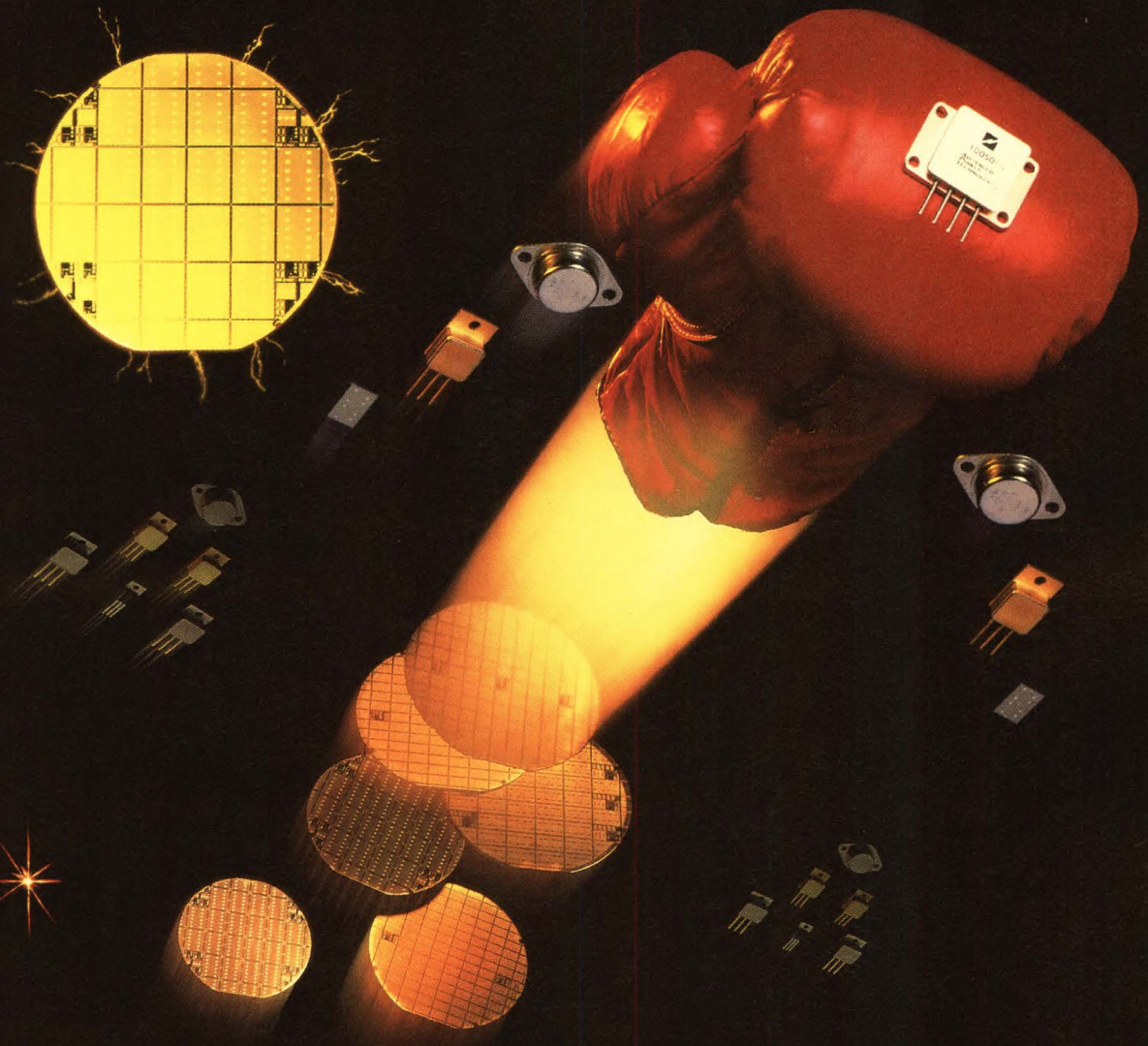

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0.021 - 0.21	95.0 - 39.0	380 - 156	9000 - 13000	360 - 675	0.738 × 0.585 (108)
0.04 - 0.40	83.0 - 20.5	332 - 82	4500 - 6500	160 - 370	0.588 × 0.388 (107)
0.20 - 1.30	26.0 - 8.5	104 - 34	1800 - 2950	60 - 130	0.414 × 0.254 (106)
0.30 - 2.40	18.5 - 5.0	74 - 20	1300 - 1800	45 - 105	0.290 × 0.250 (105)
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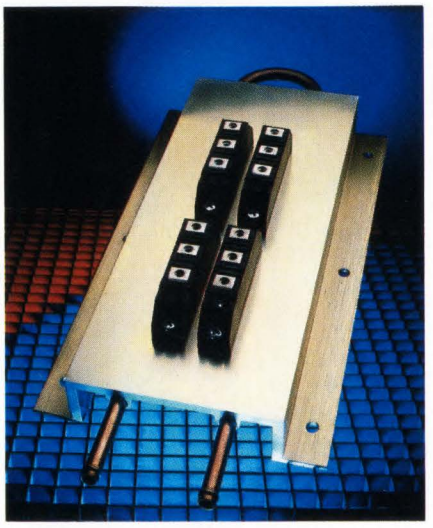
maximum junction temperature for your heat-sink calculations that is 10 to 20% below the manufacturer's maximum number.

In addition to these electrical and thermal specifications, you need to determine your space requirements and the type of interface you prefer between the case and heat sink. If space is at a premium, you'll be concerned about the size of your heat sink. The interface you choose, whether thermal grease, mica, or thermally conductive pads, has a thermal resistance which you must take into account to choose the proper heat sink.

Once a heat-sink vendor knows your system's specs and space requirements, he can easily direct you to one or many products that will suit your requirements. In some cases, the vendor will use the thermal equations to solve for $\Theta_{S\text{-}A}$, and then match it with the thermal resistance of one or many of its heat-sink products.

Each heat-sink manufacturer has a preferred way of specifying its heat-sinks' performance data. Instead of quoting a single number for thermal resistance, you often find two sets of curves: one for natural-convection cases and one for forced-air cases. In the case of natural convection, many manufacturers quote specs in terms of heat-sink or mounting-surface temperature rise above ambient temperature versus heat dissipated. The same graph often includes the forced-air curves in terms of air velocity versus thermal resistance.

It's not absolutely necessary to pore over these heat-sink data sheets in order to choose the right product. One company, Thermalloy, offers a PC-based heat-sink selection program. The program guides you to Thermalloy products that meet your specs, based on the values you input for P_D, $\Theta_{J\text{-}C}$, $\Theta_{C\text{-}A}$, T_J, and T_A. If you have a color monitor, you can view the actual heat sink and its mechanical dimensions. At your request, the program will take you through the thermal calculations step by step.



***Heat-dissipation products are classified** as passive and active. Heat sinks are passive devices—they require no external work or energy. Liquid-cooled Cold Plates (Aavid Engineering) are examples of active cooling—some external element controls the flow of water through the pipe.*

You'll arrive at a final thermal-management solution by an iterative process. There may in fact be no heat sink that matches your initial set of specs—as Thermalloy's program will readily point out. If that happens you must change directions. For instance, you may find that there is no heat sink large enough to provide the necessary cooling under natural convection. And, if board space is a problem, you're again restricted to smaller heat sinks. Therefore, you'll need to add forced air to your system to meet the desired thermal specifications. Once you've provided forced air, you'll probably find that any number of heat sinks will work, and you can choose one based on other factors besides thermal resistance, such as the amount of labor required to attach the heat sink.

Heat-sink manufacturers' catalogs are currently filled with a wide variety of extruded heat sinks, which are produced by forcing the heat-sink material through grooves to form the fins that protrude from the heat-sink baseplate; bonded heat sinks, which have metal fins bonded into the heat-sink baseplate; a variety of labor-saving clip attachments; heat sinks designed for use with pin-grid arrays (PGAs); and board-level products such as thermally conductive planes; and heat-conducting substrates.

A new heat-sink product tackles the problem of how to attach a heat sink to a PGA. Thermalloy's PGA E-Z Mount assembly consists of a spring clip and either a plastic frame or "shoes" for the PGA (**Fig 2**). First, you place the PGA in the plastic frame, and then fit the spring clip into the heat sink, over the ridges on the frame. This procedure attaches the heat sink securely to the PGA. E-Z Mount is currently available for 11-, 14-, 15-, and 21-pin PGA packages. The 15-pin version costs $0.40 (1000).

If you don't want to use any additional hardware, you can use one of several available PGA heat sinks. IERC provides PGA heat sinks in

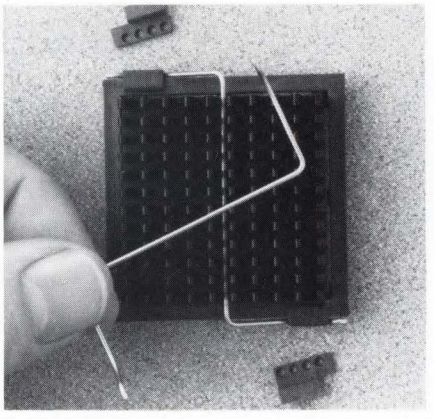
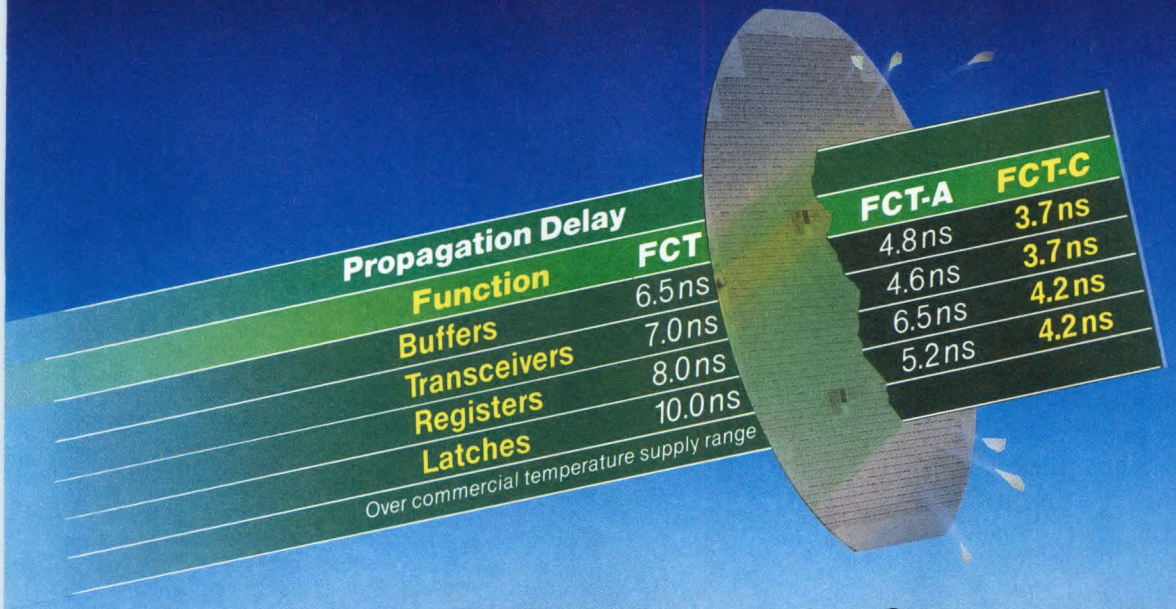


***Fig 2—Heat sink manufacturers offer many variations of labor-saving attachment methods.** Thermalloy's E-Z Mount is their solution to attaching this heat sink to a PGA device.*

Breaking the TTL Speed Barrier



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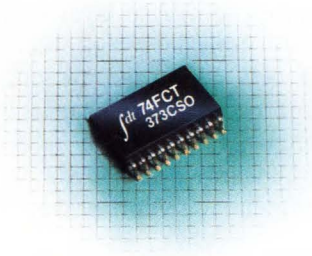

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Thermal-management products

either an omnidirectional, pin-fin design or a standard extrusion format. Both models are available in a wide range of configurations to match specific requirements such as maximum allowable temperature rise, height restrictions, and cooling method. You attach the heat sinks to the PGA either by using a thermally conductive epoxy adhesive or by specifying a hole pattern for stud-mounted PGA packages. Depending on your choice of fin configuration and plating material, and on whether or not you select a hole pattern, prices for the PGA140 series range from $0.34 to $2.12 (1000).

You'll find a wide variety of heat sinks specifically designed for TO-220 packages, such as the 667 Series from EG&G Wakefield (**Fig 3**). This series features the "speed clip" for rapid device assembly. Four heights, two solderable-pin styles, and two speed-clip types are available for vertical mounting to the pc board. These heat sinks cost around $0.40 (1000).

To provide cooling for high-power semiconductor modules, Aavid Engineering's Series 6760 heat sinks feature precision-fit aluminum fins that are bonded to the back of the mounting surface with thermal epoxy. This type of bonded-fin heat sink provides as much as 100% greater cooling surface per cubic inch of space than extruded or cast heat sinks. These heat sinks are available in nine standard sizes to accommodate multiple mounting of power modules. Forced-air models accept standard muffin fans and can achieve thermal resistances of 0.024°C/W to 0.08°C/W. Natural-convection models feature thermal resistances from 0.22°C/W to 0.30°C/W and are 3.13-in. high and either 7 or 12 in. long. Pricing for the 7-in. natural-convection model with gold chromate finish is $39.37 (100).

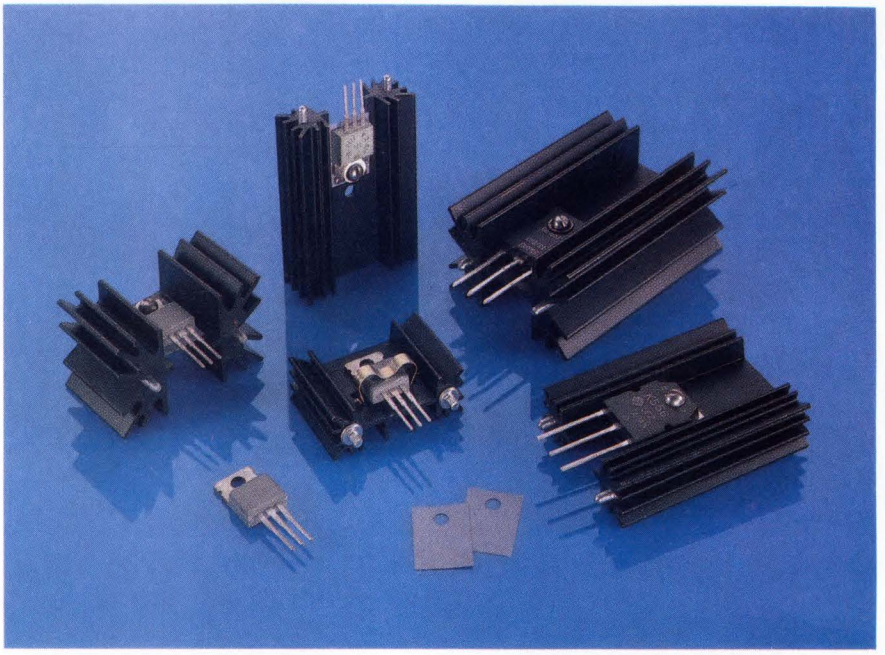

Fig 3—The popular TO-220 package style *now has many heat sink possibilities. Many manufacturers offer a wide variety of sizes and device-attachment options, such as these products from EG&G Wakefield.*

Device-level solutions such as these only scratch the surface of your heat-sink options. Depending on your size, performance and budget constraints, your design may justify the use of one of the many custom, board-level products on the market.

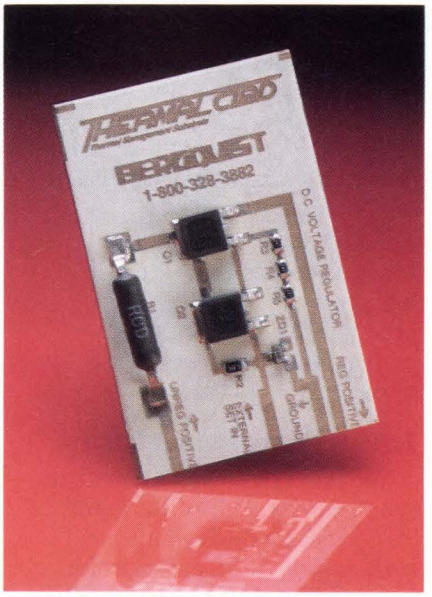

Fig 4—Single-layer board solutions *such as Berquist's Thermal Clad can be used in SMT applications and as a mounting surface for power hybrids.*

TI-strate, produced by the Metallurgical Materials Div of Texas Instruments, is a polymer-on-metal surface-mount technology substrate for single-circuit-layer power assemblies. This printed-wiring board product utilizes a thin, thermally conductive dielectric to isolate a copper circuit and pad layer from a heat-sink base. The dielectric exhibits thermal resistance of 0.5°C/W and maintains a minimum breakdown strength of 3000V. TI-strate is priced by the square inch and ranges from $0.50 to $1/in^2.

A similar pc-board product is Berquist's Thermal Clad (**Fig 4**), which consists of a foil layer that is laminated to a base layer with a thermally conductive dielectric. The material is suited to single-sided surface-mount pc boards; it is also commonly used as an alternative to ceramic materials as a mounting surface for power hybrids.

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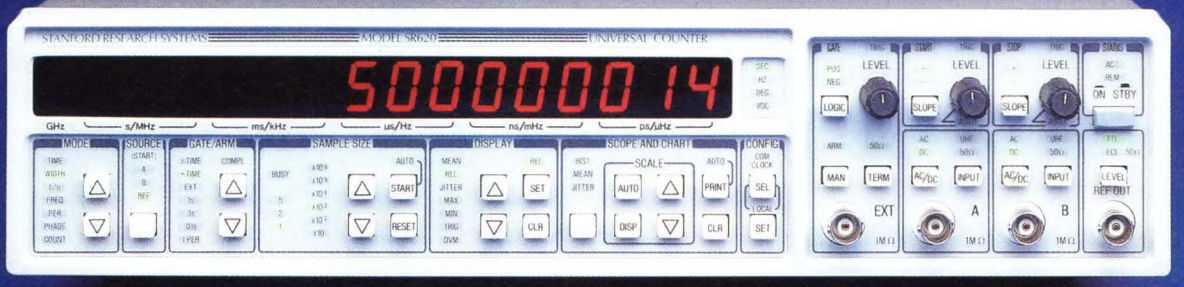

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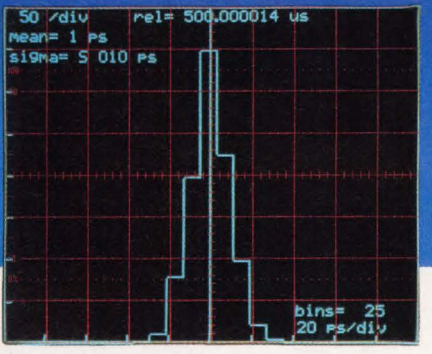

The SR620 provides graphic display of histograms and strip charts on any X-Y oscilloscope. With Autoscale and Zoom, graphics can be easily scaled. Attach a dot matrix printer or an HP-GL plotter and obtain hardcopy of any graph.

Finally, high resolution time interval measurement at an affordable price. The SR620 Universal Time Interval Counter offers 4 ps single-shot LSD on time intervals, and 11 digits of frequency resolution in one second. With powerful arming, gating, and triggering modes, the SR620 can measure time interval, frequency, period, pulse width, and phase, as well as rise and fall times.

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strate is as a heat pipe: Thermal Clad offers lower thermal resistance between the device's mounting surface and the substrate, but you still must provide a path, such as card guides, for heat to flow from the Thermal Clad board to some cooler surface. This surface can be the outside of an enclosure or a surface with active cooling, such as a liquid-cooled plate. In addition, depending on the types of devices you mount on the substrate, a secondary heat sink may be required.

The thermal resistance of the material depends on the surface area of the Thermal Clad and the device's package. A TO-220 transistor mounted to an etched pad on a 4×5-in. Thermal Clad panel exhibits thermal resistance of 1°C/W. As with the other board products, Thermal Clad is custom based. Price varies according to the type of metal backer you choose, the complexity of the circuit and mechanical pattern, and the size of the Thermal Clad board. Typical prices range from \$0.35 to \$0.90/in^2.

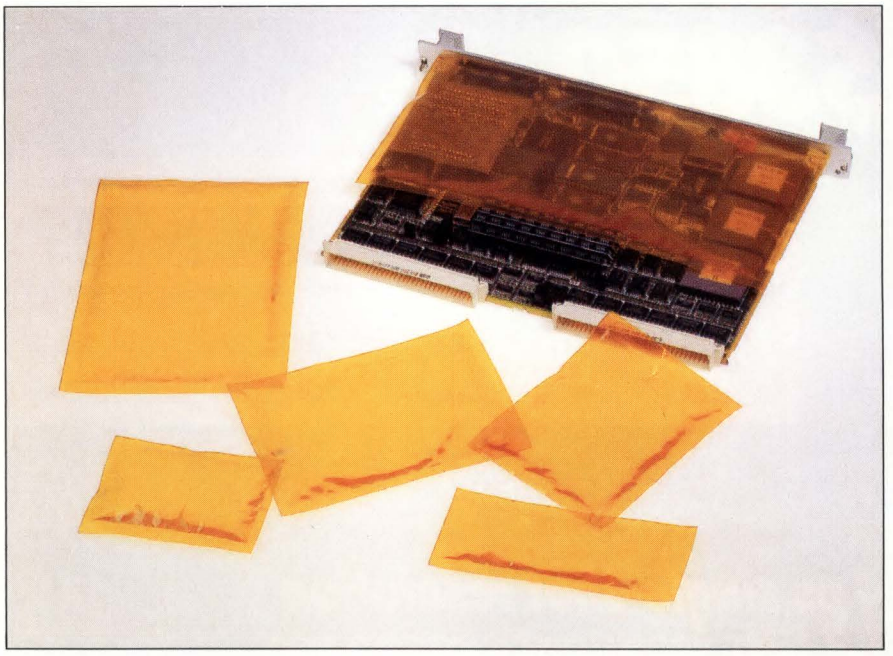

Fig 5—These Liquid Heat Sinks *manufactured by 3M contain Fluorinert liquid; when fitted into tight spaces, they transfer heat from a heat-generating component to a cooler surface by liquid convection.*

You can also find products that are designed to fit on top of a pc board. Aavid Engineering's thermal planes fit over a pc board and transfer heat via metal conduction to the exterior of the enclosure via the card guides. Again, these are custom items, but typically, price varies from \$10 to \$220 each. Aavid can produce the thermal planes in a variety of aluminum alloy and copper alloy materials. You can use the planes with both through-hole and SMT designs.

An innovative approach to heat removal is 3M's Liquid Heat Sink (LHS). The LHS is a multilayer plastic bag filled with Fluroinert liquid (**Fig 5**). Fluorinert liquids are perfluorocarbons and do not contain hydrogen, chlorine, or bromine. The liquids are not chlorofluorocarbons and are not associated with ozone-layer depletion.

The LHS dissipates heat in tight spaces by using natural convection. Heat flux from a power component conducts through the wall of the LHS into the Fluorinert liquid. Convective fluid movement then transfers heat from the component to the opposite LHS wall. Heat then flows from this wall to an exterior surface that touches the LHS.

For more information . . .

For more information on the thermal-management products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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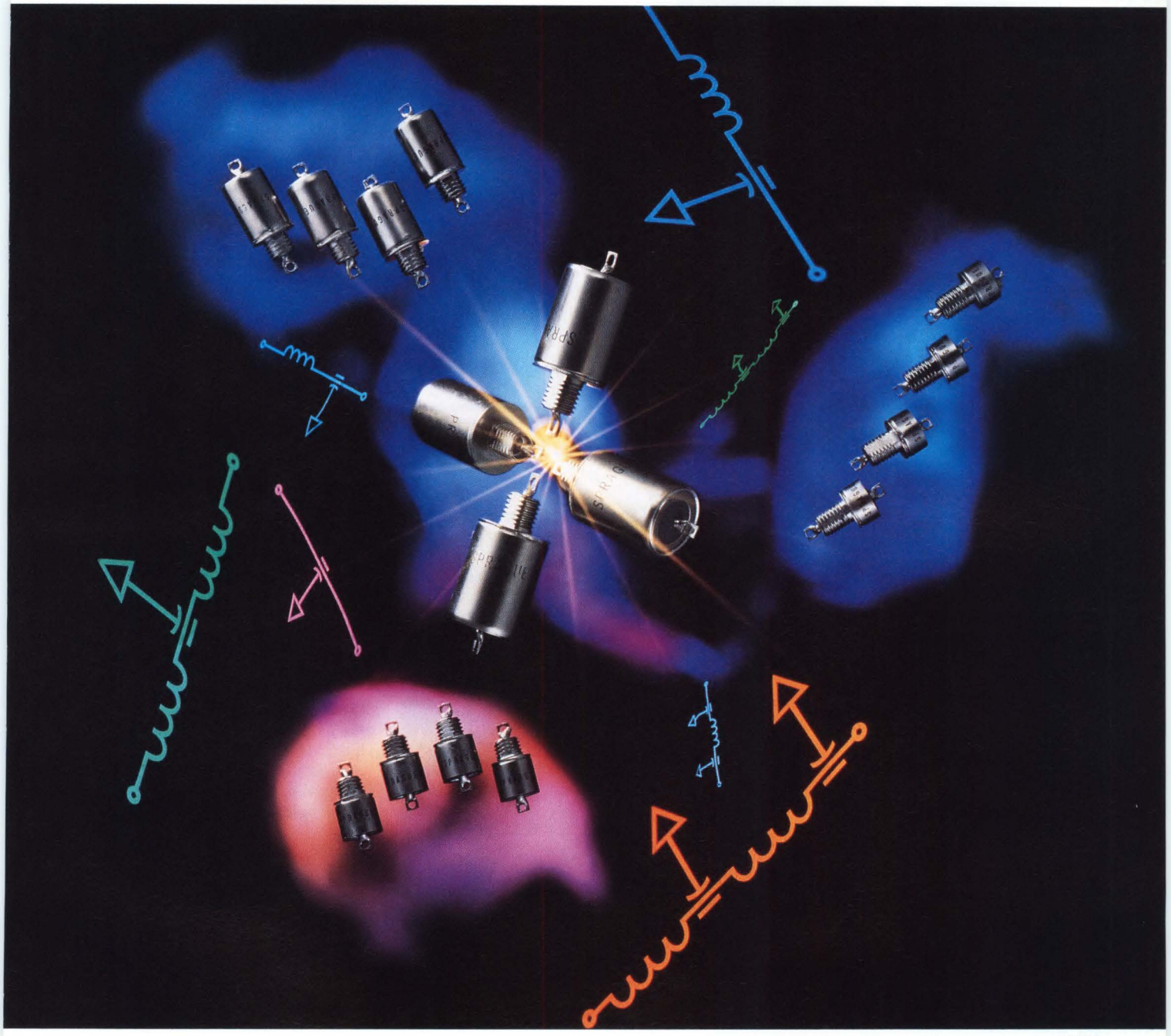

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UPDATE

Six standard LHS sizes are available: 1.5×4-, 2×3-, 3×4-, 3×4.75-, 4×6-, and 4×9-in. packages. Prices range from $10 to $20 each. You can obtain a sample of any one of the sizes by contacting 3M.

Heat-sink manufacturers manage to keep up with changing package styles, and higher-density and higher-heat-producing semiconductors. Their products will become increasingly important, just as temperature effects should be to the engineer. Though the commercial and industrial markets don't have the same financial resources as does the military market, marketplace competitivness and higher component densities still demands that your products be correctly designed the first time. Budget and time-to-market constraints simply do not allow you to lay out a pc board twice or select alternate components. EDN

References

1. *Heat Sink/Dissipator Products and Thermal Management Guide*, IERC, Burbank, CA, 1985.
2. *Standard Products Catalog*, Heat Dissipation Components, EG&G Wakefield Engineering, Wakefield, MA, 1988.

Article Interest Quotient
(Circle One)
High 500 Medium 501 Low 502

MAXIM DESIGN NEWS

Analog Design Insights from Maxim Integrated Products July '89

New 12-Bit ADCs Convert 6MHz Signals

Complete 10µs A/D Converters with Track-and-Hold Simplify System Design in DC or DSP Applications

In high resolution DSP and data acquisition systems, even a fast analog-to-digital converter (ADC) can digitize only the slowest moving analog signals without help from a separate track-and-hold (T/H) or sample-and-hold (S/H) amplifier. Because the analog signal cannot change significantly during the ADC's quantization period, the limit on input frequency imposed by a non-sampled ADC can be surprisingly severe if the full accuracy of the ADC is to be maintained. **Figure 1** illustrates the relationship between an ADC's quantization period (or aperture time, t_A) and the error caused by a time-varying input signal. Assuming a full scale sine-wave input, the fastest signal that can be quantized by an ADC is calculated with the formula:

$$f = 1 / (2^n \pi t_A)$$

where f is the input frequency, and n is the resolution for 1-bit of error. If a track-and-hold is not used, the aperture time then equals the ADC's conversion time. Consequently, by using this formula, we find that a 12-bit 5µs ADC, without help, can only accurately quantize signals slower than 15.5Hz. But, if we then add a T/H to reduce t_A, the analog signal can be "frozen" throughout the conversion, enabling the ADC to digitize much higher frequency signals.

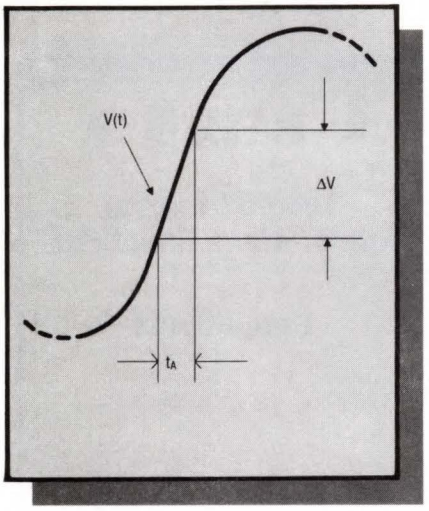

Figure 1. Errors can result when converting time-varying signals due to uncertainty of signal during conversion.

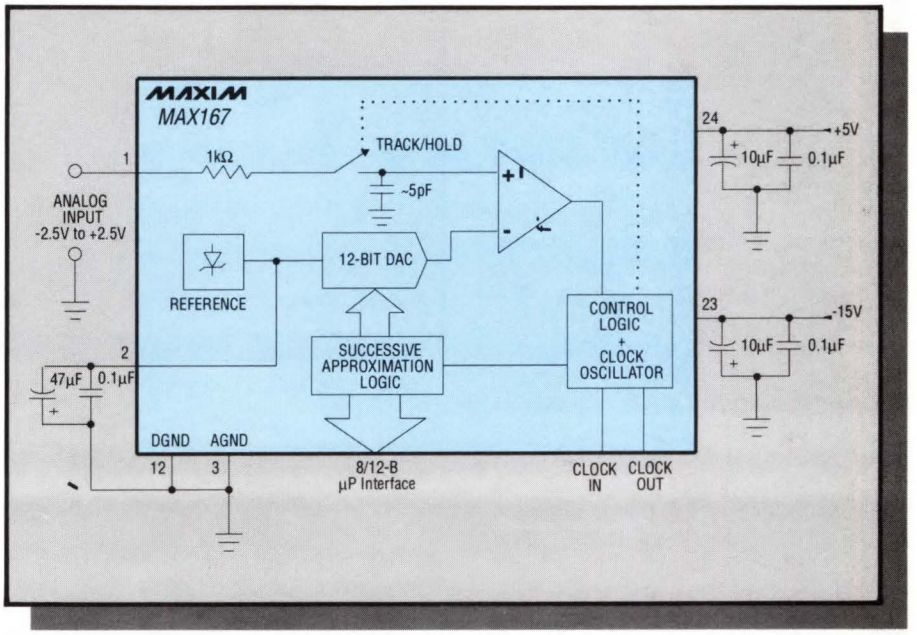

Figure 2. MAX167 plugs into the AD7572/MAX162 socket and replaces the circuit shown in Figure 3.

Figure 2 shows the circuit for Maxim's MAX167 sampling A/D converter, which replaces the circuit of **Figure 3** that combines the Maxim AD7572 5µs 12-bit ADC (or the 3µs MAX162) with an HA5320 or AD585 track-hold amplifier. Besides providing a fast aperture time, the T/H also supplies a low AC and DC impedance to drive the ADC input. A low impedance source is essential to drive the ADC (even when a T/H isn't used) since the ADC's analog input current is somewhat modulated at the clock rate during the conversion.

Although adding a T/H in front of an ADC improves dynamic performance, it also introduces several new potential error sources that can degrade the overall DC and AC performance of the system. These new problems include hold-step errors, slew rate limitations, settling time delays, signal droop, and most importantly, added noise and distortion. Some of these errors can be reduced with trimming or by simply using a very high performance (and very expensive) T/H, but such solutions rapidly increases the system cost.

Sampling ADCs Dramatically Reduce Component Count

Maxim's monolithic ADCs provide the best means of minimizing the above errors while saving the cost of an external track-and-hold amplifier. A sampling A/D converter contains the T/H function in the same package as the ADC. As a result, DC specifications such as gain error, offset, integral nonlinearity (INL) and differential nonlinearity (DNL), as well as dynamic specifications such as signal-to-noise ratio (SNR), total harmonic distortion (THD) and intermodulation distortion (IMD) are tested and guaranteed for the complete ADC-T/H system. The designer then need not worry about additional errors generated by the T/H, or by the T/H-ADC interface. Other benefits that are provided for the same

reduced cost are higher system reliability, reduced board-space, and dramatically decreased component count as seen by comparing Figures 2 and 3.

Both DC and AC Specs are Guaranteed

Maxim's MAX163, MAX164 and MAX167 integrate a track-and-hold function and a fast ADC on a single chip at a cost ($21.25* in 100s) comparable to monolithic ADCs *without* the track-and-hold. The ADCs use an innovative CMOS comparator with a built-in track-and-hold that employs a very small (5pF) on-chip hold capacitor. This optimizes high speed tracking performance and provides excellent large signal and wide bandwidth behavior -- without the slew-rate limitations inherent in many other sampling ADCs. A 6MHz full power bandwidth makes it possible to digitize high speed transient events and, by employing undersampling techniques, to measure periodic signals whose bandwidth exceeds the ADC's sample rate of 100kHz. **Figure 4** shows an FFT plot of the output level at various spectral bands of a MAX167 when digitizing a pure 10kHz sinusoid at a 100kHz rate. The theoretical minimum ADC noise is caused by quantization error and is a direct function of resolution. The limit of a "perfect" 12-bit ADC would be 74dB. The MAX167 is fully tested to meet or exceed a signal-to-noise plus distortion of 70dB and a THD of 80dB for an 85% of full-scale input signal.

With the MAX163/4/7, *providing precise AC specification does not dictate that DC performance be compromised in any way.* 12-bit DC specifications are guaranteed over the full operating temperature ranges. Since these ADCs are plug-in replacements (*with track/holds*) for the Maxim AD7572, MAX162, and MAX172

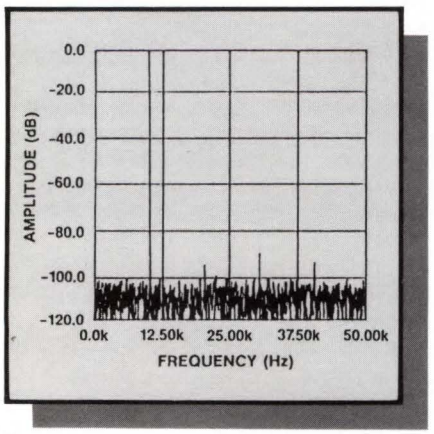

Figure 4. FFT plot of spectral response for a 10KHz sinusoidal input.

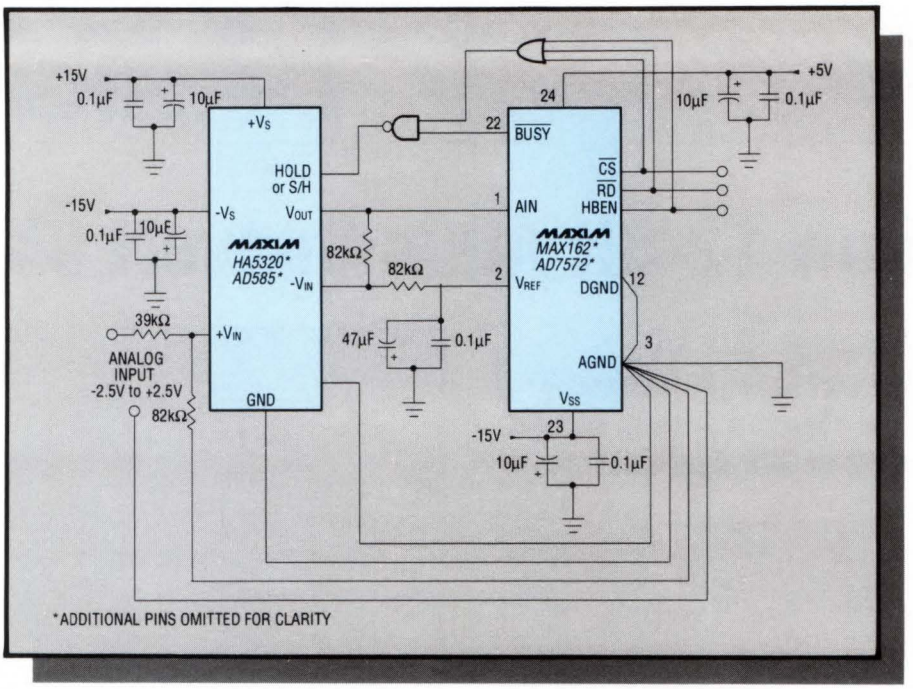

Figure 3. A sample-and-hold amplifier used with an A/D converter improves the accuracy.

an existing circuit can be easily modified to eliminate the external track-and-hold by shorting the circuit's signal input directly to the input of the ADC (Figure 3). The high input impedance (500MΩ) of the MAX163/4/7 also eliminates the need for a fast driver amplifier, thus completely replacing the track-and-hold amplifier. For applications that require even faster sampling rates, a 3µs MAX162 used with a high performance T/H is still a good alternative. The 10µs, $10* (in 1000s) MAX172 can be used with an inexpensive T/H when cost is more important than performance.

DSP Requires Fast Interfaces From ADCs

Although sampling converters can be used in slower applications, they are especially suitable for fast digital signal processing and data acquisition applications. The latest generation of digital-signal processors and microprocessors require fast processor interfaces from ADCs. The MAX163/4/7 meets this requirement with a 10µs conversion time, which includes the acquisition time of the internal T/H, and a data access time of less than 100ns. This eliminates the need for wait-states and associated discreet logic in your circuit design.

In addition to the track-and-hold, the MAX163/4/7 also include an on-chip voltage reference while maintaining low power consumption. An internal buried zener reference provides low drift (25ppm/°C) with low noise. The three ADCs offer three different analog input ranges: The MAX163 accepts 0V to +5V inputs, the MAX164 accepts -5V to +5V inputs, and the MAX167's input range is -2.5V to +2.5V. External components are limited only to decoupling capacitors for the power supply and internal reference voltage (Figure 2). On-chip clock circuitry can either be driven from an external clock source or a crystal. A standard microprocessor interface includes three-state data outputs that can be configured for 8- or 12-bit buses. Data access and bus release timing specs are compatible with most popular microprocessors. The MAX163/4/7 is available in 24-pin narrow DIP as well as surface-mount (SO) packages in commercial, extended and military temperature ranges.

*Prices F.O.B. USA

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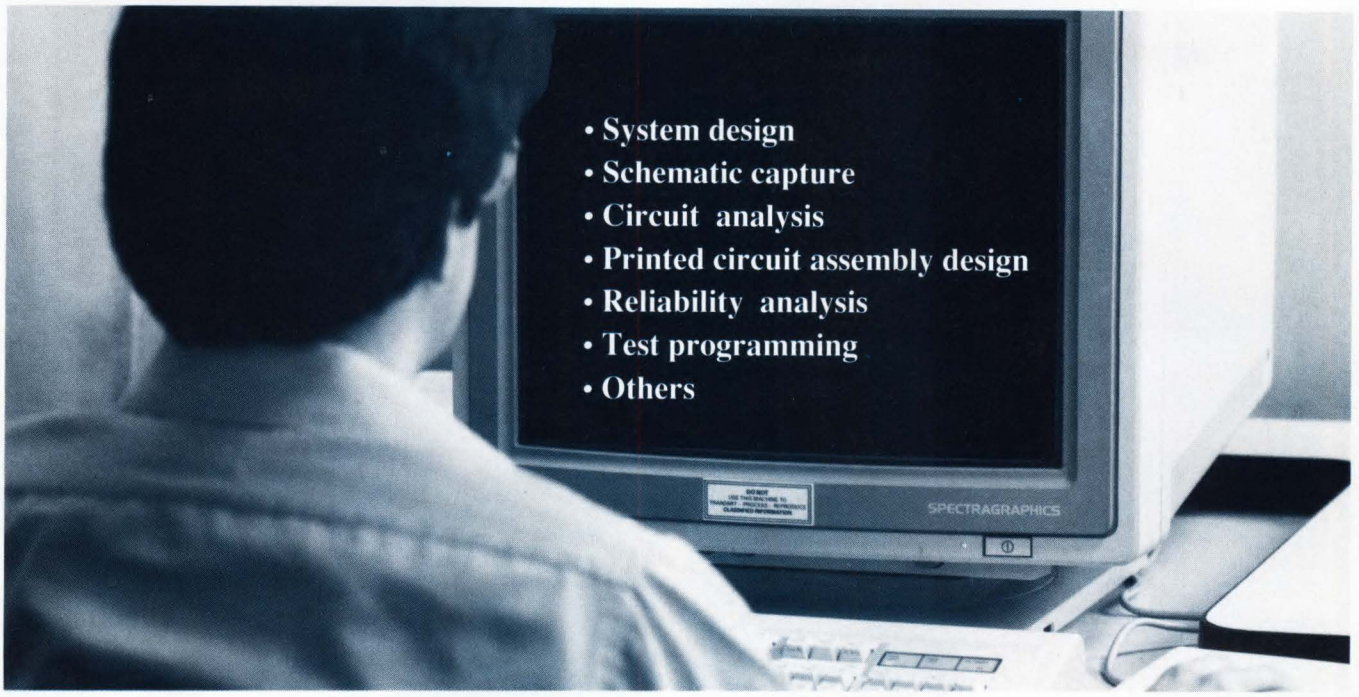

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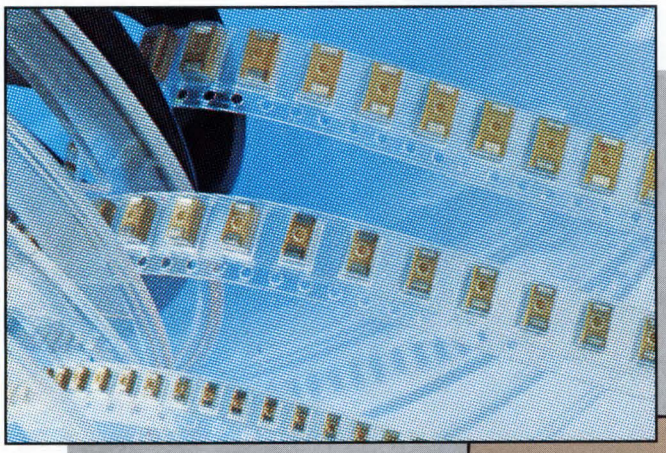

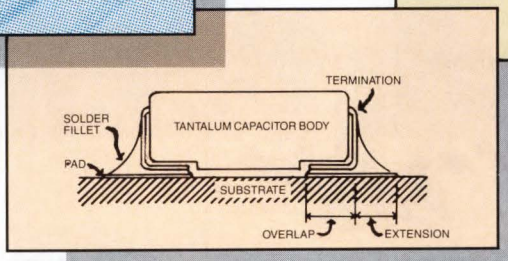

Figure 1 • Tantalum Capacitor Showing Overlap and Extension.

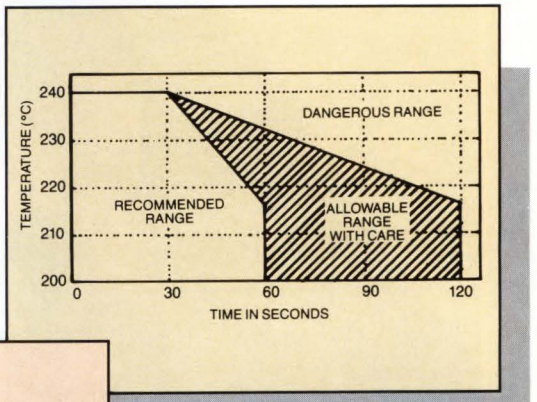

Figure 2 • Vapor Phase and Convection Infrared Soldering Range of Time and Temperature.

Surface Mount Pad Design and Solder Processes

Surface mount tantalum capacitors, like all electronic components, require specific pad designs and controlled solder processes in order to achieve zero defects.

Pad Designs

Proper pad design is essential for reflow soldering because only molten solder surface tension holds the part in place. Induced defects are minimized when the pad width matches the components solderable termination width and when the pad is approximately twice the length of the solderable bottom side (see Figure 1).

Soldering Processes

Wave soldering results in the highest temperatures and heat transfer rates. It therefore must be tightly controlled to 5 seconds maximum dwell time for a single wave at 250°C and 7.5 seconds maximum time at 230°C.

Vapor phase soldering has the second highest heat transfer rate, its range of 60–120 seconds is safe for tantalum chip capacitors (see Figure 2).

Infrared (IR) soldering uses surface heating like the vapor phase process, but the heat source is at a higher temperature than the substrate and component temperatures. Therefore, depending on the type of IR source, severe temperature gradients are possible.

Component temperatures are the control point for convection/IR systems and temperature monitoring of capacitor surfaces is mandatory when lamp systems are used.

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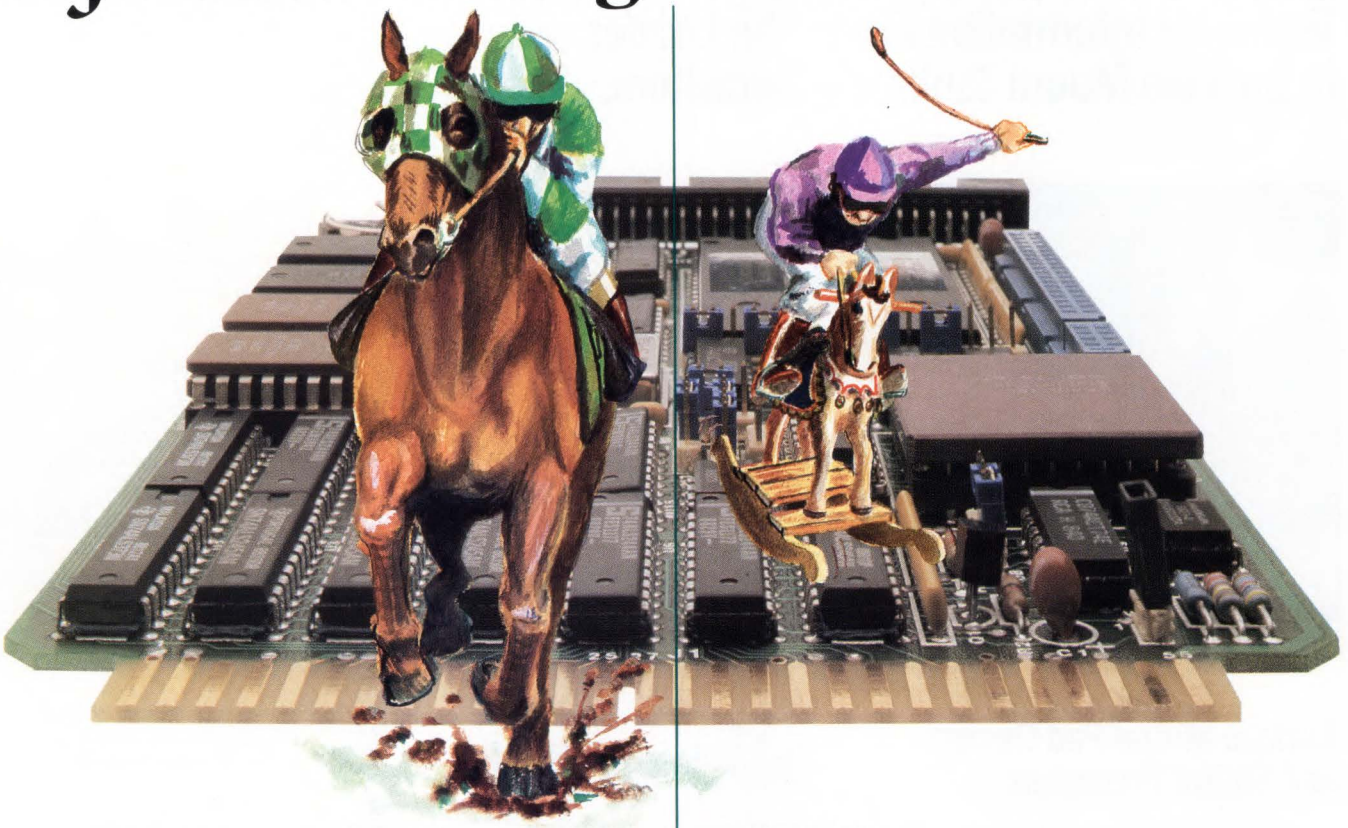
STD Bus Software Challenge:

CμBIT's C-Engine vs STD-DOS



C-Engine Features:

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- **Efficient Embedded System Code**

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Cubit's C-Engine includes our Model 8600 CPU board with a 10 MHz 80186 microprocessor, Turbo C Professional Package, a serial interface board and all necessary interfacing software including automatic ROM generation for only $995. You will have all the tools needed to produce fast, efficient ROM based code, which may be run on our $595 Model 8600 CPU without any additional software.

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Real OEM's Don't Use DOS. You want to use DOS as a development tool, but when you complete your development, DOS sticks around. Since your application runs under DOS, you will need to ship DOS with every system. OEM's can save big money by ditching DOS.

DOS is great if your system needs to run Flight Simulator. But for embedded control system development, keep DOS on your PC where it belongs. Cubit's C-Engine lets you develop code using DOS and Turbo C on your PC, while keeping the final code fast, clean and without DOS clutter.

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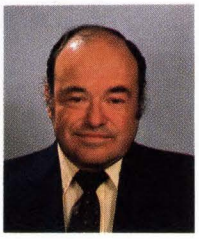
CIRCLE NO 95

16- AND 32-BIT BUS EXTENSIONS

Mature buses keep pace with technology



Technological changes continually challenge a computer's fitness for survival. If you've invested in older bus structures, you'll be happy to know that board manufacturers are updating their products for use with the latest μPs.

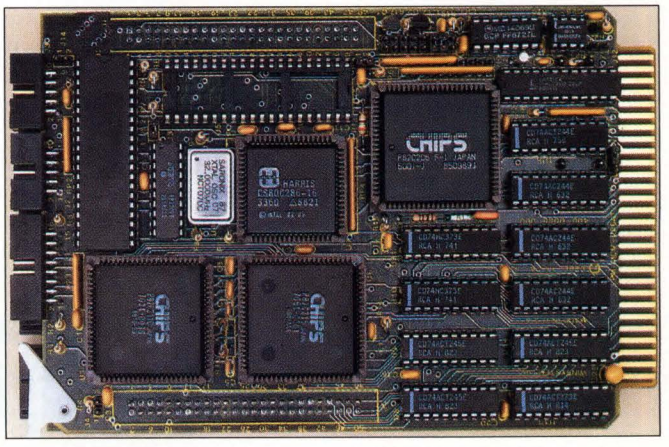
John Gallant,
Associate Editor

In this revolutionary age in which new computer architectures continually appear, it's refreshing to know that some mature architectures are adapting to changes in an evolutionary manner. The advent of the μP in the 1970s spawned a number of open bus structures for industrial control that are still in wide use today. The STD Bus, Multibus I, and G64 Bus were conceived to accommodate the μPs, memory densities, and I/O capabilities available at the time. As technology advanced through the 1980s, new open bus structures, such as the VMEbus, the Multibus II, and the industrial IBM PC/AT bus evolved to accommodate μPs with wide data paths, high memory densities, and multitasking I/O operations.

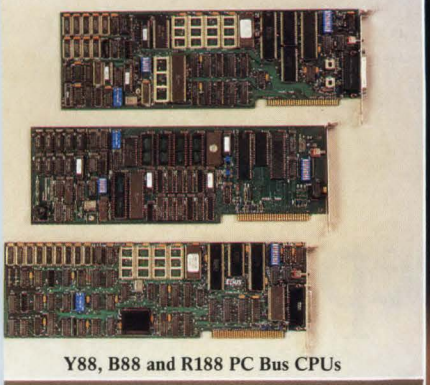
Although some of the newer bus structures threaten to extinguish the older structures eventually, for now, buses such as the STD Bus, Multibus I, and G64 Bus are as strong as ever. These earlier buses owe their survival to the fact that suppliers of boards for the older structures have redefined the bus specifications to accommodate changes in technology while remaining compatible with existing cards. The revised specifications permit users with large installed bases of industrial-control systems, for example, to upgrade their systems without investing in new embedded hardware and software.

One of the potentially endangered species is the STD Bus, which was designed and introduced by Mostek and Pro-Log in 1978 as a low-cost embedded system for industrial control. The bus soon gained IEEE approval as the IEEE-961 standard. The original specification defines a 56-pin synchronous bus with four pin-assignment categories: power, control, address, and data. The address bus consists of 16 bidirectional, 3-state lines labeled A_0 through A_{15}. The data bus consists of eight bidirectional, 3-state lines labeled D_0 through D_7. The original bus is well suited to μPs such as the 8085, Z80, 6809, and NSC-800, which have 8-bit data paths and 64k-byte memory maps.

The introduction of the 8088 and 68008 μPs around 1980 caused the STD Manufacturers Group to modify the STD Bus specification in 1983. Both of these processors have 8-bit data paths, but 1M-byte memory maps. To accommodate the larger address space, the modification multiplexes address lines A_{16} through A_{19} and data lines D_0



The MCM-26AT, an IBM PC-compatible board, conforms *to the 16-bit STD Bus specification. In addition to its 80286 CPU, this WinSystems board can have as much as 2M bytes of onboard RAM.*



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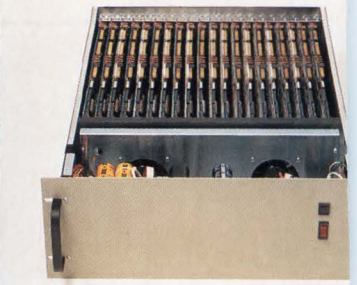

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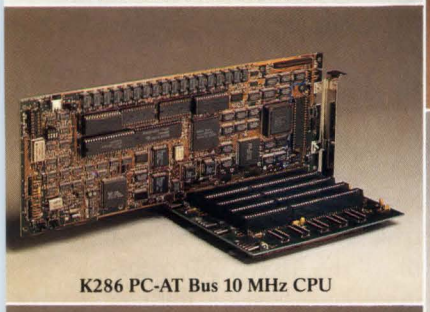

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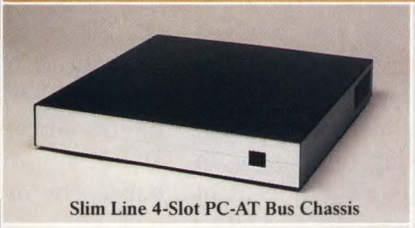

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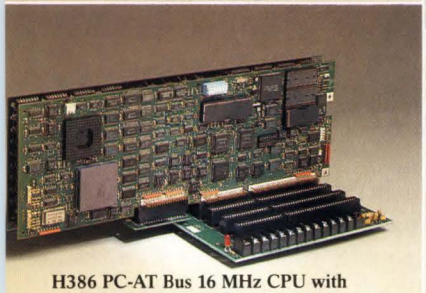

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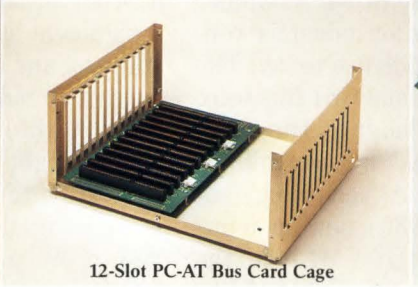

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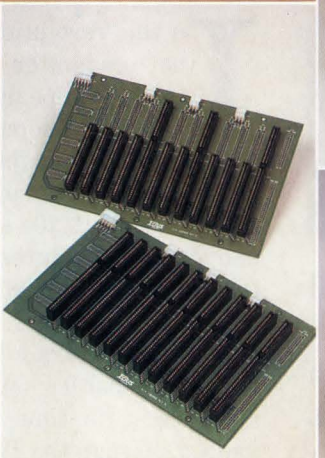

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16- and 32-bit bus extensions

through D_3 onto the same bus pins. Cards using the upper address space must latch A_{16} through A_{19} by using the rising edge of the $\overline{\text{MCSYNC}}$ control line. The modified STD Bus standard is known as STD-8088.

The emergence of the 16-bit μP families, such as the 68000 and 80X86, also in the early 80s, presented a dilemma for STD Bus-board manufacturers. Both these μP families have 16-bit data paths and include chips having 16M bytes of address space. Upgrading the boards to STD-8088 let the boards easily accommodate the expanded address space (from 1M byte to 16M bytes.) The upgrade multiplexed the address lines, A_{20} through A_{23}, with the data lines, D_4 through D_7, onto the same bus pins. However, both of the μP families define two control signals that can be used as high-byte, low-byte, or full-word transfers. Because the IEEE-961 standard accommodates byte transfers only, it creates a bottleneck for off-board full-word transfers. A 16-bit data transfer requires two memory fetches, reducing the board's throughput by half.

Some STD Bus manufacturers approach the dilemma by offering 16-bit CPU boards that have on-board memory for reducing bus traffic. The CPU-188 card from Computer Dynamics, for example, conforms to the original IEEE-961 specification and contains an 80188 CPU, 1M byte of dynamic RAM (DRAM), and a 128k-byte EPROM. It accesses an additional 128k bytes of off-board memory by using the memory expansion (MEMEX) control line, and it performs 8-bit data transfers on the bus. Ziatech's ZT 8814 single-board computer conforms to the STD-8088 specification and contains an 80188 CPU, 32k bytes of RAM, and 64k bytes of ROM. It can access 1M byte of off-board memory and performs 8-bit data transfers on the bus.

STD becomes a 16-bit bus

To overcome the 8-bit data-transfer bottleneck, the STD Manufacturers Group appointed WinSystems Inc chairman of a committee to revise the STD Bus standard for full 16-bit data transfers. Known as the 16-bit specification, the revision provides for compatibility with all existing I/O-mapped cards that don't use the MEMEX line, and for

TABLE 1—STD BUS 16-BIT SPECIFICATION

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	V_{CC}	IN	LOGIC POWER (5V DC)	2	V_{CC}	IN	LOGIC POWER (5V DC)
	3	GND	IN	LOGIC GROUND	4	GND	IN	LOGIC GROUND
	5	VBB #1/VBAT	IN	LOGIC BIAS #1/BAT PWR	6	VBB #2/$\overline{\text{DCPD}}$	IN	LOGIC BIAS #2/PWR DWN
DATA BUS	7	D_3/A_{19}	IN/OUT	DATA BUS/ADDRESS EXT	8	D_7/A_{23}	IN/OUT	DATA BUS/ADDRESS EXT
	9	D_2/A_{18}	IN/OUT		10	D_6/A_{22}	IN/OUT	
	11	D_1/A_{17}	IN/OUT		12	D_5/A_{21}	IN/OUT	
	13	D_0/A_{16}	IN/OUT		14	D_4/A_{20}	IN/OUT	
ADDRESS BUS	15	A_7	OUT	ADDRESS BUS	16	A_{15}/D_{15}	OUT	ADDRESS BUS/DATA BUS EXT
	17	A_6	OUT		18	A_{14}/D_{14}	OUT	
	19	A_5	OUT		20	A_{13}/D_{13}	OUT	
	21	A_4	OUT		22	A_{12}/D_{12}	OUT	
	23	A_3	OUT		24	A_{11}/D_{11}	OUT	
	25	A_2	OUT		26	A_{10}/D_{10}	OUT	
	27	A_1	OUT		28	A_9/A_9	OUT	
	29	A_0	OUT		30	A_8/D_8	OUT	
CONTROL BUS	31	$\overline{\text{WR}}$	OUT	WRITE TO MEMORY OR I/O	32	$\overline{\text{RD}}$	OUT	READ MEMORY OR I/O
	33	$\overline{\text{IORQ}}$	OUT	I/O ADDRESS SELECT	34	$\overline{\text{MEMRQ}}$	OUT	MEMORY ADDRESS SELECT
	35	IOEXP	IN/OUT	I/O EXPANSION	36	MEMEX	IN/OUT	MEMORY EXPANSION
	37	$\overline{\text{REFRESH}}$	OUT	REFRESH TIMING	38	$\overline{\text{MCSYNC}}$	OUT	CPU MACHINE CYCLE SYNC
	39	$\overline{\text{STATUS 1}}$	OUT	CPU STATUS	40	$\overline{\text{STATUS 0}}$	OUT	CPU STATUS
	41	$\overline{\text{BUSAK}}$	OUT	BUS ACKNOWLEDGE	42	$\overline{\text{BUSRQ}}$	IN	BUS REQUEST
	43	INTAK	OUT	INTERRUPT ACKNOWLEDGE	44	INTRQ	IN	INTERRUPT REQUEST
	45	$\overline{\text{WAITRQ}}$	IN	WAIT REQUEST	46	$\overline{\text{NMIRQ}}$	IN	NONMASKABLE INTERRUPT
	47	$\overline{\text{SYSRESET}}$	OUT	SYSTEM RESET	48	$\overline{\text{PBRESET}}$	IN	PUSHBUTTON RESET
	49	$\overline{\text{CLOCK}}$	OUT	CLOCK FROM PROCESSOR	50	$\overline{\text{CNTRL}}$	IN	AUX TIMING
	51	PCO	OUT	PRIORITY CHAIN OUT	52	PCI	IN	PRIORITY CHAIN IN
AUXILIARY POWER BUS	53	AUX GND	IN	AUX GROUND	54	AUX GND	IN	AUX GROUND
	55	AUX +V	IN	AUX POSITIVE (12V DC)	56	AUX –V	IN	AUX NEGATIVE (–12V DC)

16- and 32-bit bus extensions

full 16-bit-wide data transfers for new word-wide cards. The card dimensions, bus connector, and power-supply definitions remain the same. Further, the revision supports the same interrupts as defined in the STD Bus Recommended Practice document, and it supports the CMOS STD Bus.

To accomplish these goals, the 16-bit specification redefines MEMEX and multiplexes the address and data lines together. **Table 1** shows the redefined pinout for the 16-bit specification of the STD Bus. Data lines D_0 through D_{15} share bus pins with the address lines A_8 through A_{23}. The specification uses the machine-cycle sync ($\overline{MCSYNC}$) line to latch the address lines before data appears on the bus. The bus master issues an $\overline{MCSYNC}$ signal at the beginning of a machine cycle to synchronize peripheral devices. Because the data bus is idle during this time, no performance penalty ensues.

TABLE 2—CORRESPONDING STD BUS SIGNAL RELATIONSHIPS

STD BUS SIGNAL	68000 SIGNAL	80X86 SIGNAL
MCSYNC	$\overline{AS}$	$\overline{ALE}$
MEMEX	$\overline{LDS}$	$\overline{BHE}$
A_0	$\overline{UDS}$	A_0

The 68000 family has two control lines, the upper data strobe (UDS) and the lower data strobe (LDS), which indicate whether a high-byte, low-byte, or 16-bit-word transfer is occurring. The equivalent control lines for the 80X86 family are the zero address line (A_0) and the byte-high-enable line (BHE). In addition, each μP family has a strobe signal that indicates when an address is valid. The 68000's strobe is called the address strobe (AS), and the 80X86's strobe is called the address latch enable (ALE). **Table 2** shows the relation of these control

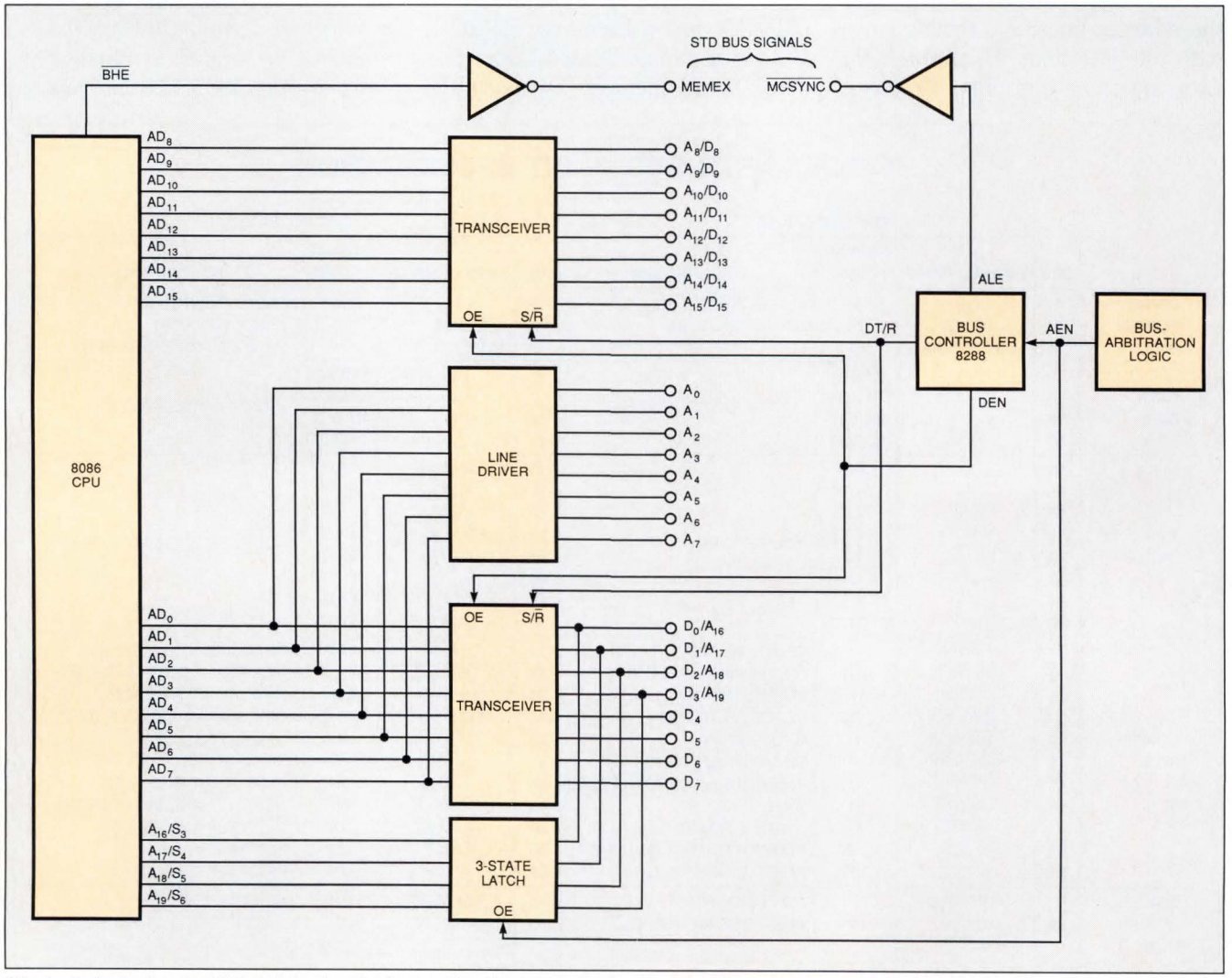

Fig 1—Interfacing an 8086 μP to the 16-bit specification *requires a 3-state latch to accommodate the 20-bit address space.*

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signals to the signals in the 16-bit specification for the STD Bus. **Table 3** provides a truth table for data transfer.

The memory-expansion line plays a different role in the 16-bit specification than in the original IEEE-961 specification. The original specification used the line as an additional address line for accessing 128k bytes of off-board memory. The 16-bit specification uses it to designate when a high-byte transfer occurs. **Fig 1** shows the typical circuitry required to interface an 8086 μP to the STD Bus under the 16-bit specification. **Fig 2** gives the timing diagram for a read operation.

The WinSystems LPM-SBC50 uses two methods for implementing the 16-bit specification—the 16-bit-only mode and the address-segmentation mode. The card has an NEC V50 CPU, which is similar to a CMOS 80186 μP. When operating in the 16-bit-only mode, the card can transfer the upper and lower bytes independently, or it can transfer the full 16-bit-wide word. The card operates directly with 16-bit memory cards, such as the company's LPM-UMC3 memory card, with no wait states. The $\overline{BHE}$ signal controls the MEMEX line on the STD Bus to indicate an upper- or lower-byte transfer.

TABLE 3—DATA-TRANSFER TRUTH TABLE

MEMEX	A_0	CHARACTERISTIC
0	0	FULL-WORD TRANSFER
0	1	UPPER-BYTE TRANSFER
1	0	LOWER-BYTE TRANSFER
1	1	NOT DEFINED

Although the 16-bit-only method is straightforward, it doesn't allow you to combine 8- and 16-bit data transfers. Because most existing I/O cards have 8-bit data paths, a CPU card must be able to support both data widths. The address-segmentation method divides the memory and I/O map into two areas. Cards with 8-bit data paths reside in one area, and 16-bit cards reside in the other. The LPM-SBC50, for example, divides the map at address location FF_{HEX}. When using the address-segmentation mode, the card transfers 8-bit data to address locations below the boundary and 16-bit data to locations above the boundary.

You must also account for the difference in the byte-ordering convention of the Motorola and Intel μPs when you use address segmentation. In the Motorola convention, the high byte occupies the lower memory address, whereas in the Intel architecture, the high byte appears in the higher memory address. When a 68000 or a 80X86 performs a 16-bit memory-access operation, the disparate ordering conventions aren't a problem because the processor selects both even- and odd-byte memory locations, and it doesn't matter which section of memory is called even or odd. However, byte accesses do require the software designer's attention. The LPM-SBC50, for example, has onboard buffer-swapping logic to route high- and low-byte data correctly to existing 8-bit I/O boards.

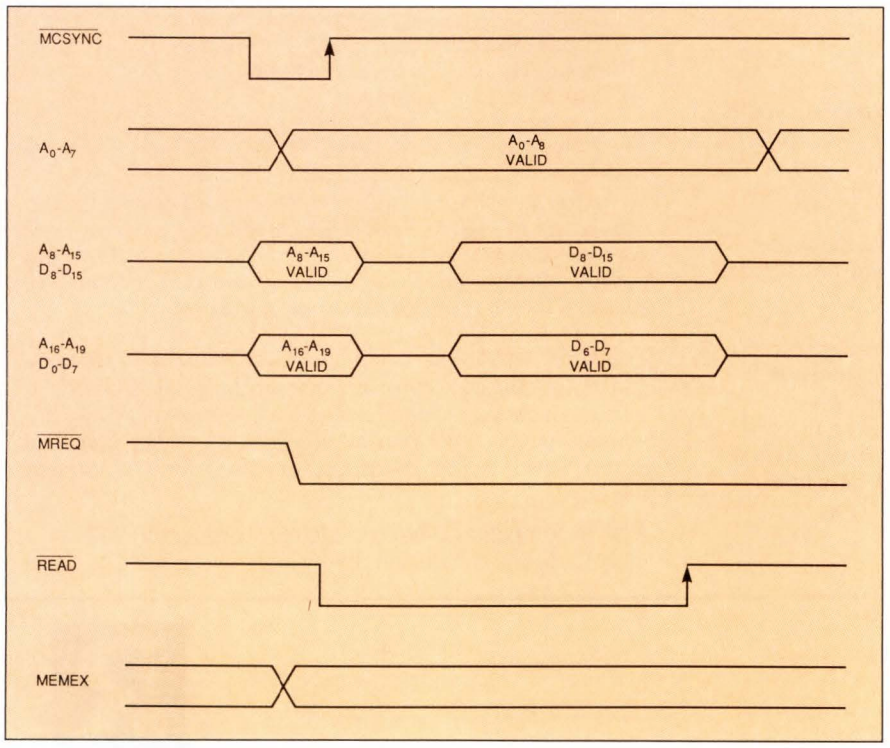

***Fig 2—The $\overline{MCSYNC}$ signal indicates** the start of an STD Bus cycle. Memory cards using the 16-bit specification use the rising edge of this signal to latch the upper addresses.*

Multibus I keeps pace

The STD Bus is often called the "blue collar" microcomputer bus, because it's well suited to low-cost embedded applications that don't require more than 8- or 16-bit processing power. The Multibus I architecture, which was introduced by Intel in 1976 as an 8-bit data bus, was redesigned to support the 16-bit μPs when they became available. The 1980s witnessed the rise of new and powerful 32-bit μPs, which caused Intel to introduce an entirely different 32-bit bus structure called the Multibus II. Many board manufacturers switched to

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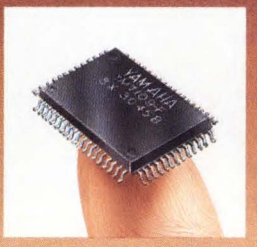

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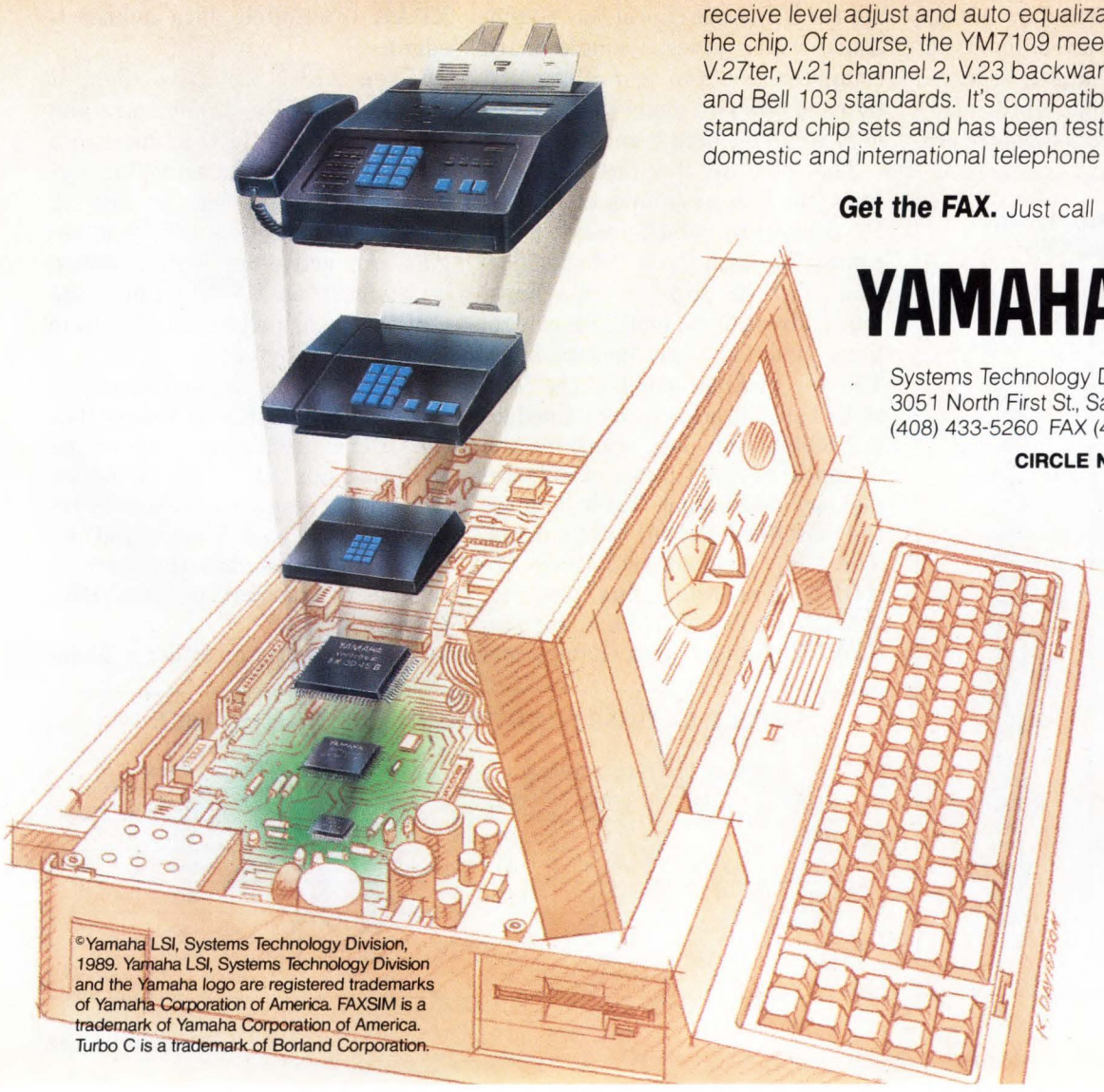

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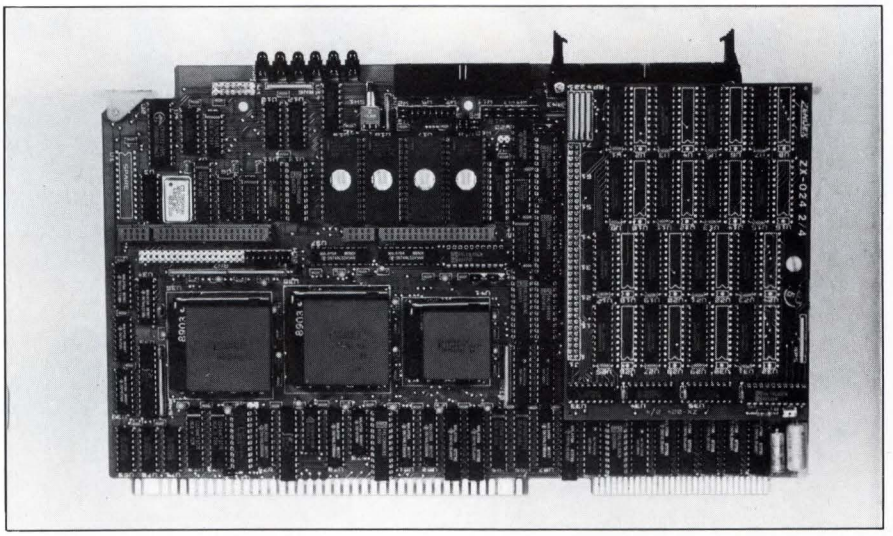
the Multibus II or the 32-bit VMEbus architecture to accommodate the wide-data-bus CPUs.

In 1987, Zendex Corp found a way to extend the capabilities of the 16-bit Multibus I structure to transfer 32-bit-wide data. The company calls it the TRU-32 specification, and it enhances the Multibus I (IEEE-796) specification. The TRU-32 specification preserves compatibility with Multibus I products so that users can maintain their investment in hardware and software while upgrading their systems to 32-bit technology.

The IEEE-796 specification defines two connectors for Multibus I—a primary 86-pin (P1) and a secondary 60-pin (P2) connector. For 16-bit-system bus transfers, all the P1 connector's pins are defined, but the P2 connector is largely reserved for future definitions. Intel originally used the undefined pins to create the iLBX bus (Local Bus Extension), which gives a single-board computer access to as much as 16M bytes of offboard memory by means of 8- or 16-bit data transfers.



The ZX-386/16 board conforms *to the TRU-32 specification for 32-bit data transfers and offboard memory addressing of 256M bytes. The Zendex board also contains as much as 8M bytes of dual-port RAM.*

The TRU-32 specification redefines the pin assignments for the P2 connector, which makes it incompatible with the iLBX specification. TRU-32 adds 16 data lines, four address lines, four byte-control lines, and four new control lines. The specification expands the Multibus I specification to accommodate full 32-bit-wide data transfers and as much as 256M bytes of offboard memory addressing. **Table 4** shows the redefined P2 pin assignments. The four new control lines are $\overline{\text{XBEN}}$ (extended bus enable), $\overline{\text{XAEN}}$ (extended address enable), $\overline{\text{XDEN}}$ (extended data enable), and $\overline{\text{XDAK}}$ (extended data acknowledge).

When $\overline{\text{XBEN}}$ is active high, it disables the TRU-32 interface and places all of the TRU-32 lines in a 3-state condition. An active-low signal on $\overline{\text{XBEN}}$ enables the TRU-32 interface whenever a bus cycle begins. An active-low signal (issued by the host) on $\overline{\text{XAEN}}$ extends the CPU's offboard address range from 16M to 256M bytes.

An active-low signal (issued by the host) on $\overline{\text{XDEN}}$ indicates that the CPU is transferring data on the DB_{16} through DB_{31} lines. An active-low signal (issued by a slave in response to an $\overline{\text{XDEN}}$ command) on $\overline{\text{XDAK}}$ indicates that the slave is capable of transfers on lines DB_{16} through DB_{31}.

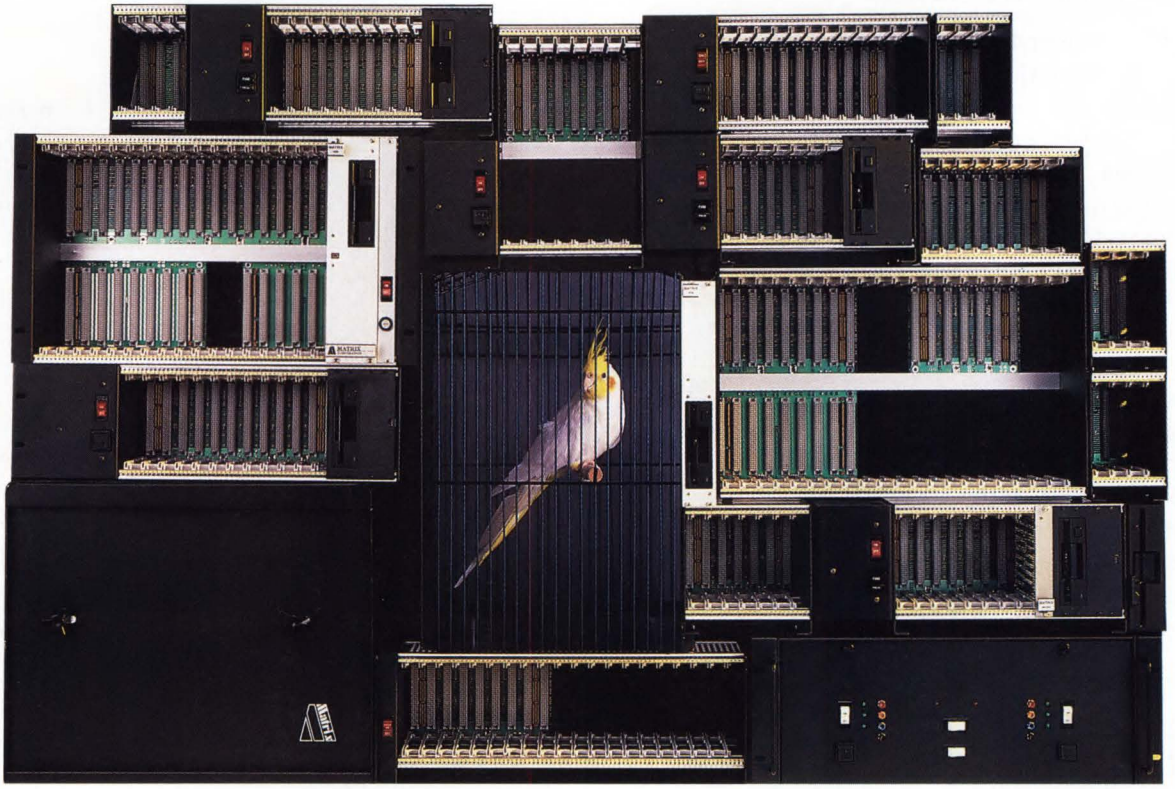
The host initiates either a mem-

TABLE 4—TRU-32 PIN ASSIGNMENTS

P2 PIN ASSIGNMENT	TRU-32 SIGNAL
31	$\overline{DB_{16}}$
33	$\overline{DB_{17}}$
35	$\overline{DB_{18}}$
37	$\overline{DB_{19}}$
39	$\overline{DB_{20}}$
41	$\overline{DB_{21}}$
43	$\overline{DB_{22}}$
45	$\overline{DB_{23}}$
47	$\overline{DB_{24}}$
49	$\overline{DB_{25}}$
51	$\overline{DB_{26}}$
53	$\overline{DB_{27}}$
05	$\overline{DB_{28}}$
09	$\overline{DB_{29}}$
60	$\overline{DB_{30}}$
40	$\overline{DB_{31}}$
42	$\overline{ADR_{24}}$
44	$\overline{ADR_{25}}$
46	$\overline{ADR_{26}}$
48	$\overline{ADR_{27}}$
50	$\overline{BE_0}$
52	$\overline{BE_1}$
54	$\overline{BE_2}$
10	$\overline{BE_3}$
14	$\overline{\text{XAEN}}$
34	$\overline{\text{XDAK}}$
36	$\overline{\text{XDEN}}$
59	$\overline{\text{XBEN}}$

TABLE 5—TRU-32 CONTROL-SIGNAL TRUTH TABLE

TRU-32 CONTROL SIGNALS				INTERFACE CONFIGURATION	
$\overline{\text{XBEN}}$	$\overline{\text{XAEN}}$	$\overline{\text{XDEN}}$	$\overline{\text{XDAK}}$	32-BIT DATA	28-BIT ADDRESSING
HIGH	X	X	X	NO	NO
LOW	LOW	HIGH	HIGH	NO	YES
LOW	HIGH	LOW	HIGH	NO	NO
LOW	HIGH	LOW	LOW	YES	NO
LOW	LOW	LOW	LOW	YES	YES



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ory-write or a memory-read bus cycle by driving either the $\overline{MWTC}$ or the $\overline{MRDC}$ bus signal low, respectively. Coincidentally, the host drives the $\overline{XDEN}$ line low if it wants to transfer 32-bit-wide data. Any slave that is capable of transferring data on the DB_{16} through DB_{31} lines must drive the $\overline{XDAK}$ line low within 50 nsec of the falling edge of the $\overline{XDEN}$ signal. The host accomplishes the data transfer by using the standard transfer-acknowledge ($\overline{XACK}$) handshake. **Table** 5 is a truth table for TRU-32 operation.

The four byte-control lines, $\overline{BE_0}$ through $\overline{BE_3}$, gate the four respective data bytes—DB_0-DB_7, DB_8-DB_{15}, DB_{16}-DB_{23}, and DB_{24}-DB_{31}—onto the Multibus. The byte-control lines are active only if the host receives the $\overline{XDAK}$ signal within the allotted 50-nsec window. When it's in the TRU-32 transfer mode, the slave ignores the standard Multibus byte-high-enable ($\overline{BHEN}$) control line and the A_0 and A_1 memory-address lines. In their place, the slave uses the byte-control signals for byte steering. If the host does not receive the $\overline{XDAK}$ signal, a standard Multibus I data transfer takes place.

TABLE 6—G96+ PIN ASSIGNMENTS

ROW C	ROW B	ROW A		DEFINITION
GND	GND	GND	1	POWER
A_{16}	A_8 :$\overline{D_{28}}$	A_0 :$\overline{D_{24}}$	2	ADDRESS
A_{17}	A_9 :$\overline{D_{29}}$	A_1 :$\overline{D_{25}}$	3	LINES A_0
A_{18}	A_{10} :$\overline{D_{30}}$	A_2 :$\overline{D_{26}}$	4	TO A_{23}
A_{19}	A_{11} :$\overline{D_{31}}$	A_3 :$\overline{D_{27}}$	5	
A_{20}	A_{12} :$\overline{D_{20}}$	A_4 :$\overline{D_{16}}$	6	
A_{21}	A_{13} :$\overline{D_{21}}$	A_5 :$\overline{D_{17}}$	7	
A_{22}	A_{14} :$\overline{D_{22}}$	A_6 :$\overline{D_{18}}$	8	
A_{23}	A_{15} :$\overline{D_{23}}$	A_7 :$\overline{D_{19}}$	9	
$\overline{BWD}$	$\overline{BRQ}$	$\overline{BGRT}$ (BGRT)	10	CONTROL
$\overline{LWORD}$	$\overline{DS1}$	$\overline{DS0}$	11	AND
$\overline{BARB}$	$\overline{BBUSY}$	$\overline{HALT}$	12	INTERRUPT
GND	ENABLE	SYCLK	13	LINES
RESERVED	$\overline{RES}$	$\overline{VPA}$	14	
RESERVED	$\overline{NMI}$	RDY/$\overline{DTACK}$	15	
$\overline{IRQ3}$	$\overline{IRQ1}$ ($\overline{IRQ}$)	$\overline{VMA}$	16	
$\overline{IRQ5}$	$\overline{IRQ2}$ ($\overline{FIRQ}$)	R/$\overline{W}$	17	
VED	$\overline{IACK}$ (IACK)	$\overline{IRQ4}$ (HALT ACK)	18	
GND	$\overline{D_{12}}$	$\overline{D_8}$	19	DATA LINES
$\overline{P5}$	$\overline{D_{13}}$	$\overline{D_9}$	20	D_0 TO D_{15}
$\overline{P4}$	$\overline{D_{14}}$	$\overline{D_{10}}$	21	AND ARBI-
$\overline{P3}$	$\overline{D_{15}}$	$\overline{D_{11}}$	22	TRATION
$\overline{P2}$	$\overline{D_4}$	$\overline{D_0}$	23	LINES
$\overline{P1}$	$\overline{D_5}$	$\overline{D_1}$	24	
$\overline{P0}$	$\overline{D_6}$	$\overline{D_2}$	25	
RESERVED	$\overline{D_7}$	$\overline{D_3}$	26	
$\overline{SYSFAIL}$	$\overline{BERR}$	$\overline{PAGE}$	27	MISC
RESERVED	CHAIN IN	CHAIN OUT	28	
RESERVED	5V BATTERY	$\overline{PWF}$	29	POWER
RESERVED	–12V	12V	30	
5V	5V	5V	31	
GND	GND	GND	32	

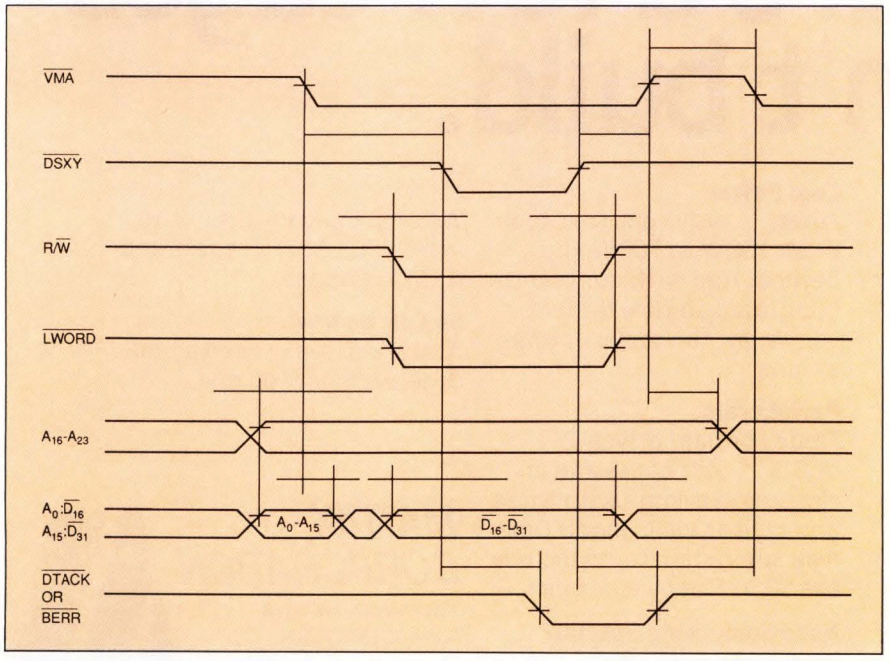


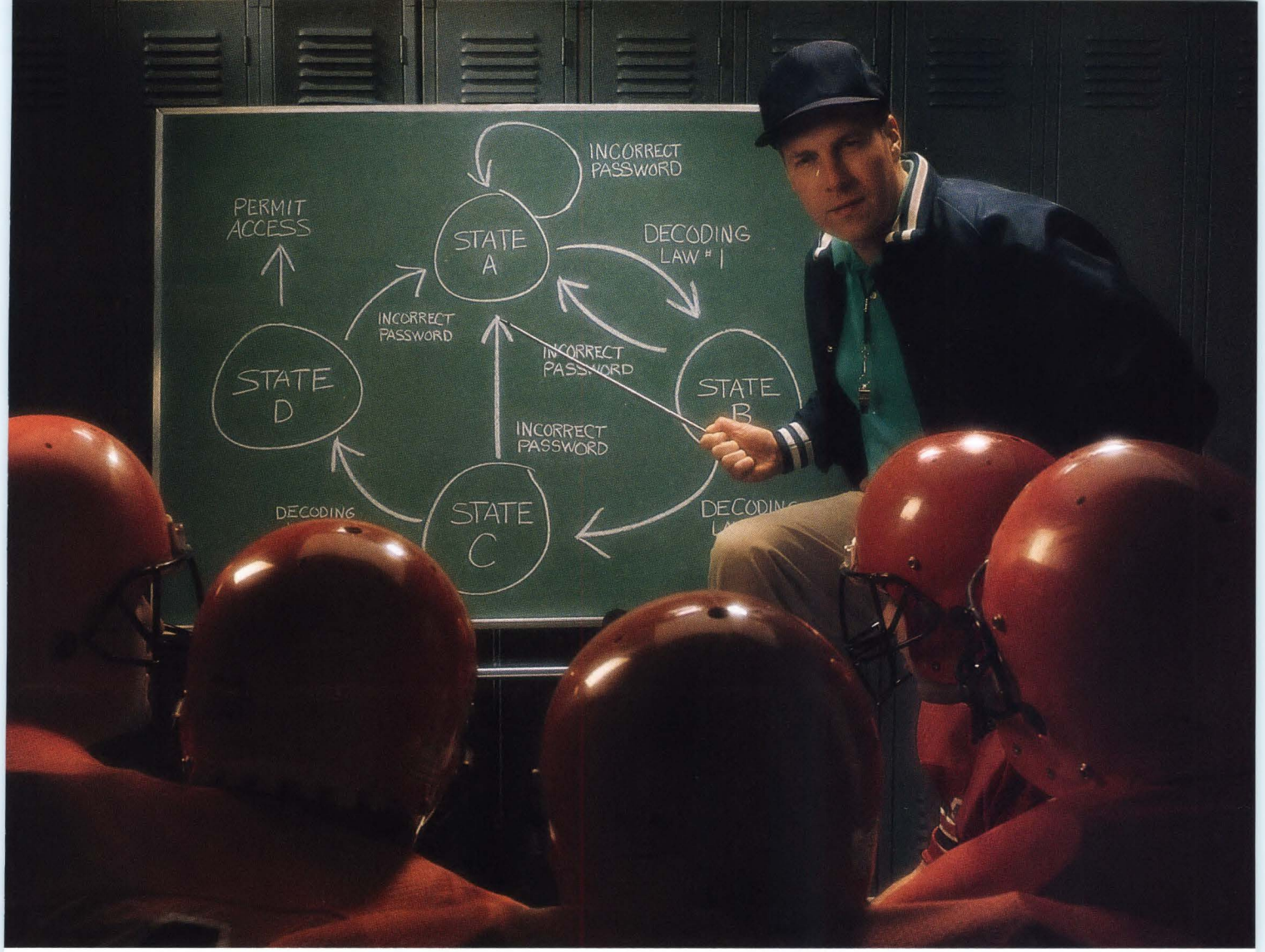
Fig 3—In the G96+ specification, *the bus master drives the $\overline{VMA}$ line low when address lines A_0 through A_{15} are valid. A slave latches the address on the falling edge of this control line.*

To design a Multibus I board that implements the TRU-32 specification, you must program a PAL to execute three equations. To implement the first of these equations, which allows the master to address more than 16M bytes, the board requires an address decoder that provides a signal indicating that the address is above the boundary. The equation for the extended-address enable line is:

$$\overline{XAEN} = \overline{XBEN} * AAB * \overline{BPRN}$$

(where AAB stands for the "address above the 16M-byte boundary" signal).

The $\overline{BPRN}$ signal is a standard



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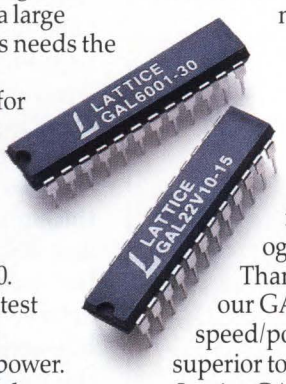

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16- and 32-bit bus extensions

Multibus I signal that makes the board the bus master. In addition, the master must assert the $\overline{INH1}$ line in order to inhibit any older Multibus memory boards from responding during an extended-address memory cycle. The extended data-enable-line equation for transferring 32-bit-wide data is:

$$\overline{XDEN} = XBEN * \overline{BPRN}$$

The bus master must also issue the byte-control lines. The 80386 provides these signals, but other processors require decoders to provide the equivalent signals. The equation for the byte-control lines is:

$$\overline{BE[0 \ldots 3]} = \overline{XBEN} * \overline{XDEN} * \overline{XDAK} * \overline{BPRN}.$$

Another bus architecture from the 1970s that's keeping pace with the times is the G64 Bus. The bus was defined by Gespac in 1979 as a 96-pin backplane that uses DIN female connectors. The G64 modules consist of single-height Eurocards with mating male connectors. The original specification provides the necessary signals for an 8-bit, synchronous I/O system. Gespac modified the specification to accommodate 16-bit, asynchronous data transfers and called the modified specification "G96." In 1988, the company extended the G96 specification to support 32-bit, asynchronous data transfers. The latest specification, G96+, multiplexes address lines A_0 through A_{15} with data lines $\overline{D_{16}}$ through $\overline{D_{31}}$.

Table 6 shows the pinouts for the G96+ specification. The specification uses address lines A_1 through A_{23} to select a 32-bit long-word memory location. It then uses four byte-control lines—$\overline{LWORD}$, $\overline{DS_0}$, $\overline{DS_1}$, and A_0—to select individual bytes within a 32-bit word. When the bus master doesn't assert an $\overline{LWORD}$ command during a bus cycle, the bus automatically reverts to a 16-bit data-transfer mode. **Table 7** gives a truth table for G96+ byte selection.

Fig 3 shows a timing diagram for an asynchronous write cycle on the G96+ bus. The master issues a valid memory address ($\overline{VMA}$) at the beginning of a memory-write or -read cycle to indicate that the address is valid. A 32-bit memory card uses the falling edge of the $\overline{VMA}$ line to latch address lines A_0 through A_{15}. After using the $\overline{DS_0}$ and $\overline{DS_1}$ line to transfer the data, the memory card issues either the data-acknowledge ($\overline{DTACK}$) or the bus-error ($\overline{BERR}$) signal to inform the master of a successful or unsuccessful bus cycle.

Another major development of the 1980s is the emergence of MS-DOS as an operating system for developing software on the IBM PC/

TABLE 7—G96+ BYTE-SELECTION TRUTH TABLE

$\overline{LWORD}$	$\overline{DS_1}$	$\overline{DS_0}$	A_0	BYTE 0	BYTE 1	BYTE 2	BYTE 3
1	1	1	1/0	NO	IF A_0 IS 0	NO	NO
1	1	0	1/0	NO	YES	NO	NO
1	0	1	1/0	YES	NO	NO	NO
1	0	0	1/0	YES	YES	NO	NO
0	0	1	0	YES	YES	YES	NO
0	1	0	0	NO	YES	YES	YES
0	0	0	1	NO	YES	YES	NO
0	0	0	0	YES	YES	YES	YES

For more information . . .

For more information on the 16- and 32-bit bus extensions and boards discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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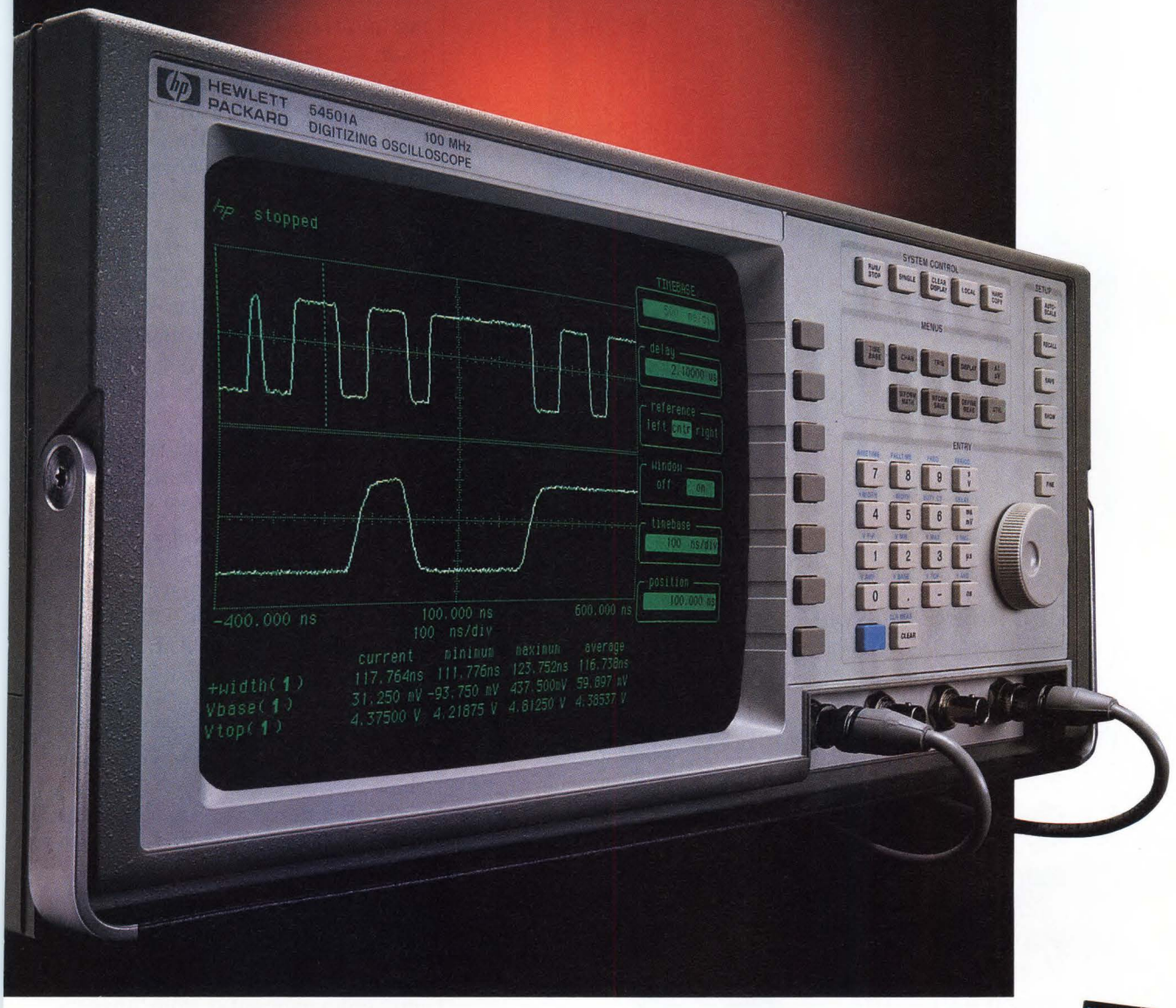

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UPDATE

16- and 32-bit bus extensions

XT and PC/AT and compatible computers. To take advantage of this wide software base, many board manufacturers have ported MS-DOS to embedded systems. In addition, manufacturers are incorporating multimaster capabilities into their systems. For example, Pro-Log's System 2 Model 30 for the STD Bus enables MS-DOS and real-time multitasking software to run simultaneously. The hardware/software combination provides multimaster capabilities for as many as eight CPUs. The CPUs—one of which runs MS-DOS—can run concurrently on the bus, sharing specified I/O and memory resources.

The G96+ specification also permits you to place multimaster processors on the G64 Bus. The specification supports as many as 31 masters on the bus, along with existing peripherals that have DMA capability. In addition, the Gespac AT system provides IBM PC/AT compatibility for the bus. The system consists of a 10-MHz, 80286 CPU board with 512k bytes of DRAM, an EGA board, and a floppy-disk-controller board. The boards can also operate with 32-bit CPUs, so you'll be able to upgrade them for use with those chips.

Clearly, board manufacturers are responding to the demands that ensue from advancements in technology. Because board manufacturers adhere to the rule of keeping their new boards compatible with earlier standards as well as the extensions and enhancements, your investment—and your customer's—will remain intact yet allow for upgrading. Instead of being put out to pasture, the mature bus structures remain solid productive workhorses. EDN

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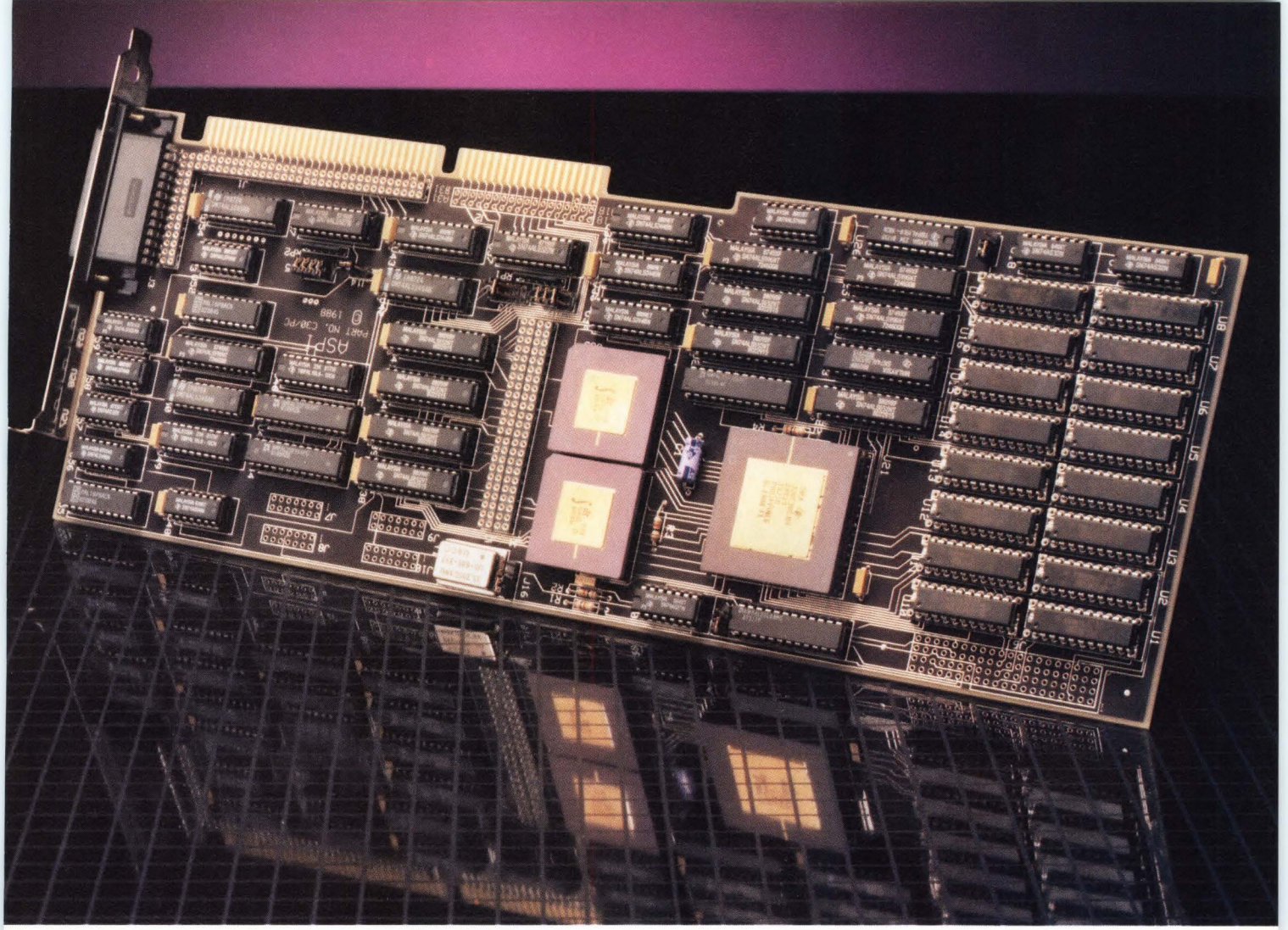

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HPC16083*	8	Yes	52	8K	256	4 ICRs
HPC16104	8	Yes	32	0	512	8 CH A/D
HPC16164	8	Yes	52	16K	512	8 CH A/D
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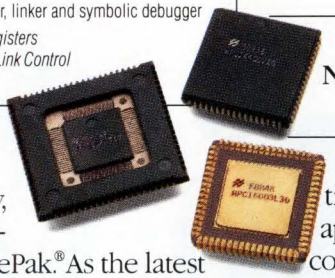

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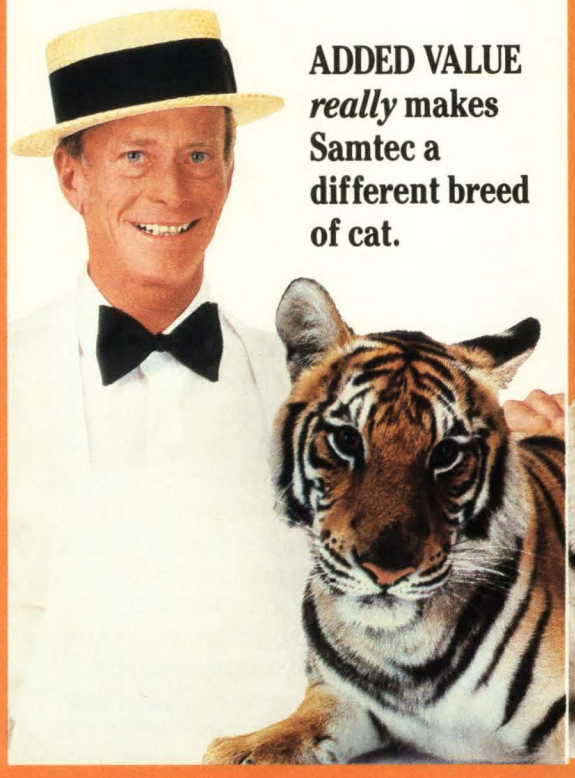

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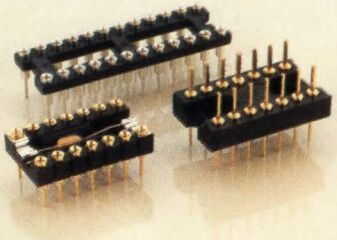

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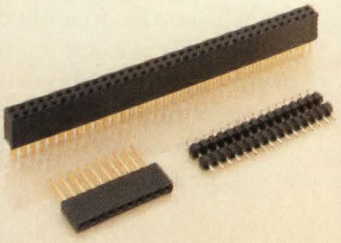

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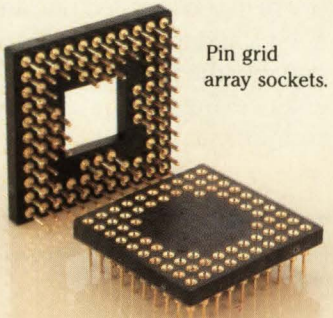

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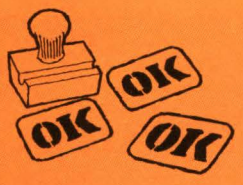

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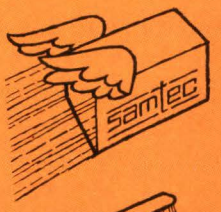

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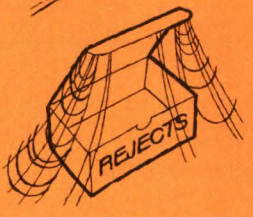

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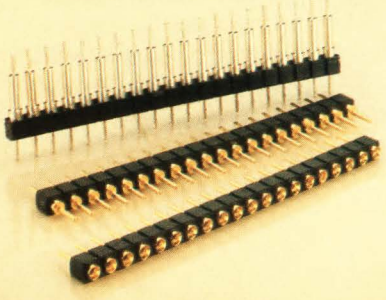

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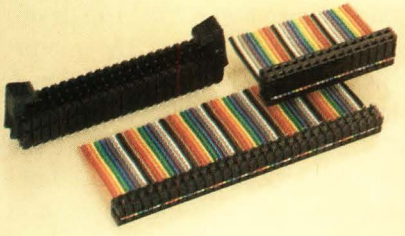
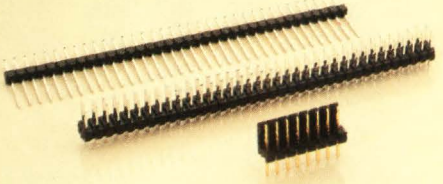
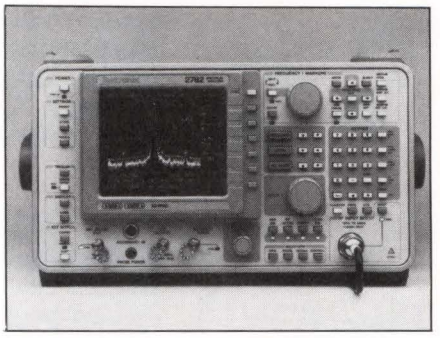


.025″ sq. terminal strips, single/double row, shrouded.



Analyzer shows 33 GHz—1.2 THz with external mixers

According to the company, when Tektronix design engineers and marketers sat down to define the 2782 microwave spectrum analyzer, their approach was to "take no prisoners." The resulting product, which is about half the size of its principal competition, boasts a list of operating conveniences that just won't quit and an impressive set of specifications.



***A 2-color display** and a thoughtfully conceived menuing system highlight the front-panel features of Tektronix's 2782 microwave spectrum analyzer.*

The compact, 42-lb instrument has a 1024 × 1024-pixel, nonfading, 2-color display that uses a CRT in conjunction with a liquid-crystal shutter. The analyzer can indicate the presence of signals from 100 Hz to 33 GHz and perform direct fundamental mixing to 28 GHz. Using external waveguide mixers, the analyzer can display signals at 1.2 THz. Above 5 GHz, its dynamic range is 100 dB. Even at 28 GHz, the instrument's resolution bandwidth can be as small as 3 Hz or as large as 10 MHz. At 18 to 20 GHz, its single-sideband phase noise is as much as 30 dB lower than that of some competitive instruments. The modulation process yields third-order products that are −90 dBc (90 dB below carrier) to 6.5 GHz and −80 dBc above 6.5 GHz.

The menu-driven operator interface clearly demonstrates attention to detail. When a menu appears, the display shows the names of all menus that are above the current one in the hierarchy. By pressing the "ESC" key, you can exit from the current menu to one at the next higher level. From the top level, pressing "ESC" causes the menus to disappear and enlarges the spectrum display. In addition to the "soft" keys beside the display, the front panel includes a dedicated numeric keypad, cursor keys, and three rotary control knobs. One knob always controls frequency. You assign functions to the other knobs via the menu system.

You can also assign functions to the cursor keys. By pressing the program/run key, followed by a single cursor key, you can execute operations that would otherwise require you to press many keys in sequence. The instrument "learns" these command sequences as you perform them and can store 20 sequences in nonvolatile memory. The analyzer's command language is the same as that of a competitive product and has become a de facto standard since the competitive product's introduction.

The 2782 includes two IEEE-488 ports, simplifying the creation of control programs that, for example, send data to mass-storage peripherals. The analyzer costs $65,000—a price that's in line with that of competitive instruments.

Tektronix Inc, Microwave and RF Instruments Div, D/S 58-183, Box 500, Beaverton, OR 97077. (800) 835-9433.

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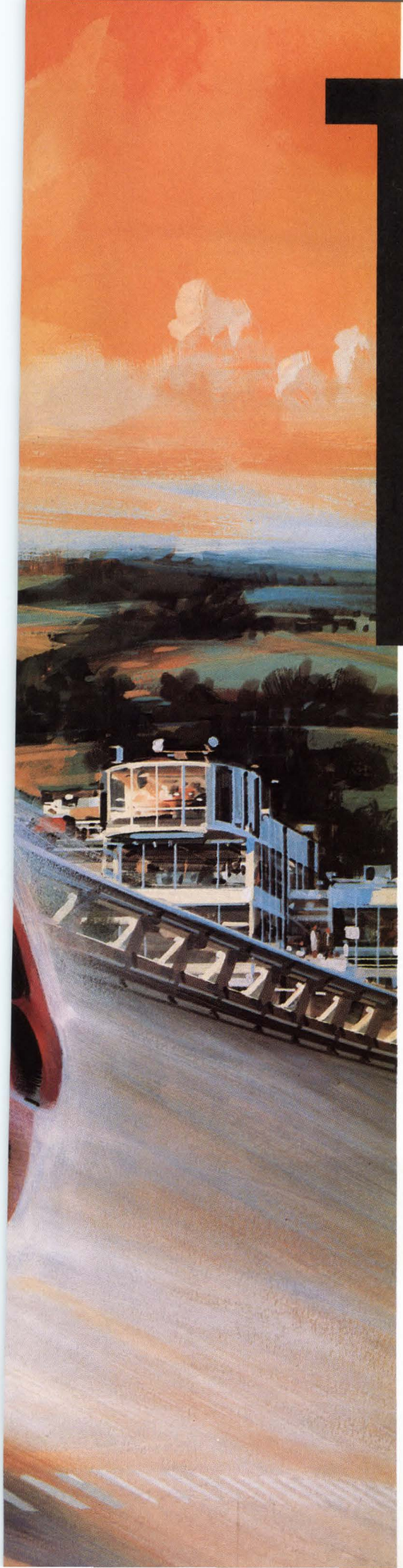
SONY HIGH-SPEED, HIGH-DENSITY SRAMS.			
MODEL	CONFIG-URATION	SPEED (ns)	PACKAGE
CXX5863P	8K x 8	25/30/35	DIP 300 mil
CXX5863M	8K x 8	25/30/35	SOP 450 mil
CXX5863J	8K x 8	25/30/35	SOJ 300 mil
CXX5464AP	16K x 4	25/30/35	DIP 300 mil
CXX5464AJ	16K x 4	25/30/35	SOJ 300 mil
CXX5465P*	16K x 4	25/30/35	DIP 300 mil
CXX5465J*	16K x 4	25/30/35	SOJ 300 mil
CXX5164P	64K x 1	25/30/35	DIP 300 mil
CXX5164J	64K x 1	25/30/35	SOJ 300 mil
CXX5971P	8K x 9	25/30/35	DIP 300 mil
CXX5971J	8K x 9	25/30/35	SOJ 300 mil
CXX58255AP	32K x 8	25/30	DIP 300 mil
CXX58255AJ	32K x 8	25/30	SOJ 300 mil
CXX58258P	32K x 8	35/45	DIP 600 mil
CXX58258SP	32K x 8	35/45	DIP 300 mil
CXX54256P	64K x 4	35/45/55	DIP 300 mil
CXX51256P	256K x 1	35/45/55	DIP 300 mil
*O/E			



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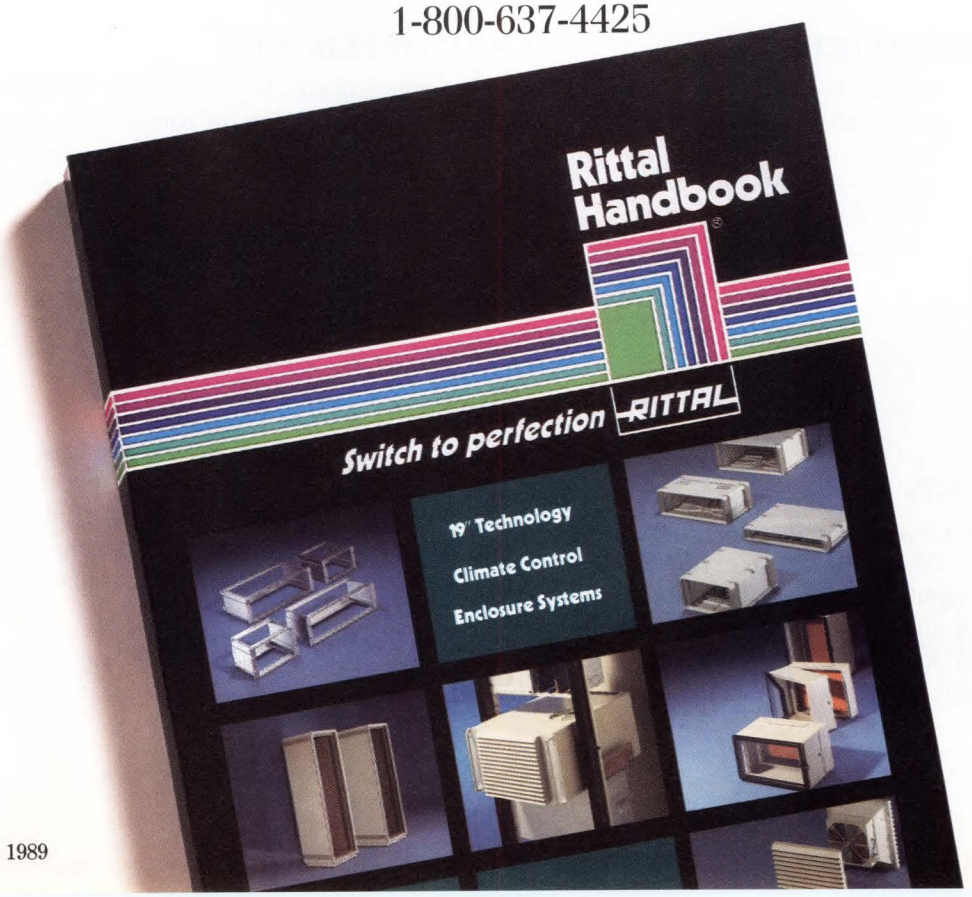

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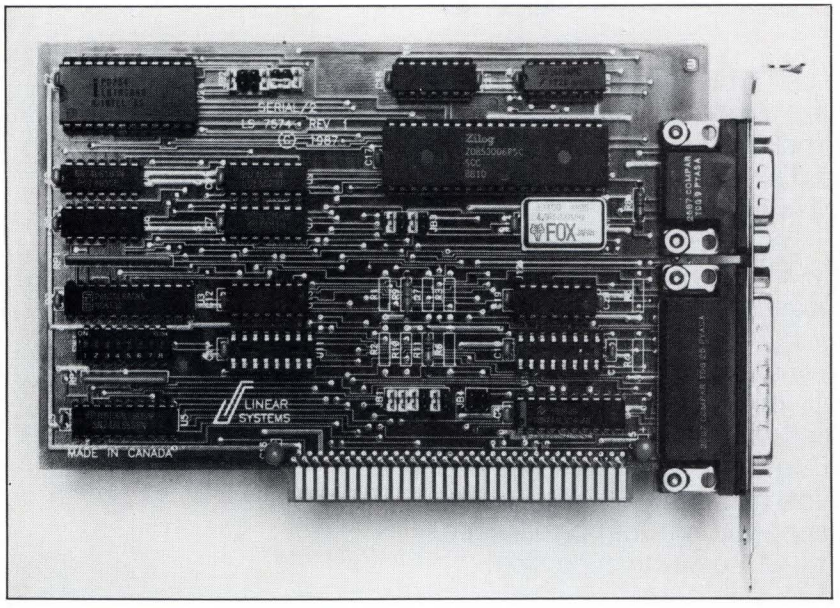
CIRCLE NO 108

READERS' CHOICE

Of all the new products covered in EDN's **March 2, 1989,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, refer to the indicated pages in our **March 2, 1989,** issue, or use EDN's Express Request service.



SERIAL-INTERFACE BOARD

The LSPC Serial/2 dual-channel, multiprotocol serial-interface board for IBM PC/AT computers uses the Intel 82530 serial-communications controller; therefore, each channel can support communications with a data terminal, a modem, an X.25 network, or a T1 gateway (pg 199).
Computer Modules Inc
Circle No. 385

WIDEBAND AMPLIFIER

Unlike conventional amplifiers, the bandwidth and rise time of the HA-5004 wideband amplifier are nearly independent of closed-loop gain. At a gain of 10, the device's unity-gain bandwidth of 100 MHz reduces only to 65 MHz (pg 183).
Harris Corp
Circle No. 382

SMD REPAIR KIT

This surface-mount-technology kit includes tools, supplies, and instructions for component replacement on surface-mount assemblies. It comes with a handheld, temperature-regulated, hot-air soldering/desoldering tool with three nozzles (pg 204).
John Fluke Mfg Co Inc
Circle No. 384

DRIVER MOSFETs

Combined with one decoupling capacitor, just one of the drivers from the TSC1426-1428 family of MOSFET drivers can replace eight discrete components. The devices have dual 1.2A outputs and are available in inverting and noninverting configurations (pg 191).
Teledyne Semiconductor
Circle No. 386

INTERACTIVE DSP TOOL

PC Data Master 2.0, an interactive DSP (digital signal processing) and analysis package, provides independent console and graphics windows. It also features piping facilities that let you link independent executable files to perform multistage data transformations (pg 213).
Durham Technical Images
Circle No. 383

88000 WAYS TO GET TO UNIX V.4 FASTER.

The future of computer operating systems is UNIX,® and the fastest way of getting to its next release, V.4, is Motorola's 88000 microprocessor.

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That's one reason AT&T chose the 88000 BCS as the early development platform for their V.4 Application Binary Interface.

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The Motorola 88000 microprocessor.

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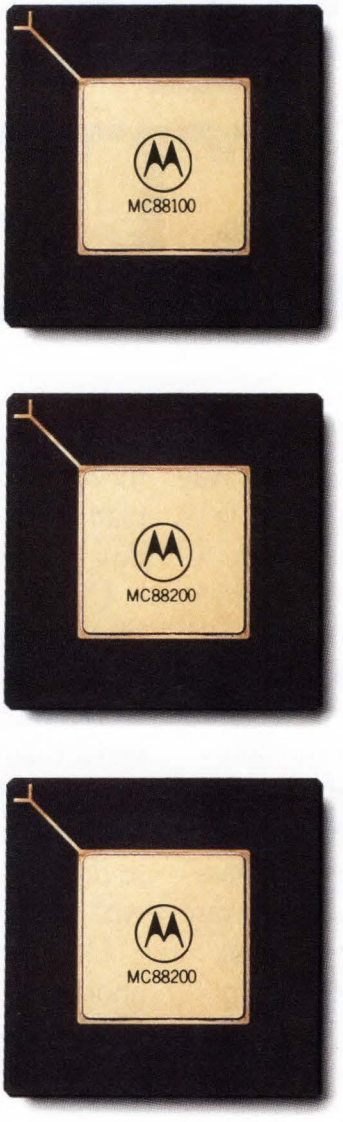
For instance, at 25MHz, the 88000 is as fast and powerful as 21 MIPS and 9 million floating point operations per second. But that's just for starters. By 1991, we'll have an ECL version running at a blistering 100 MIPS.



What's more, you can accomplish with three Motorola chips what would take up to 70 chips in other RISC systems. And you'll do it in less than one-eighth the board space.

So it's no surprise that experts are hailing the 88000 as the definitive RISC solution. And the one that's well on its way to becoming the industry standard.

*Reduced Instruction Set Computer. **Design environments shown above include Data General AViiON workstation, Tektronix DAS 9200 logic analyzer and target board with Macintosh II for software development. ***Software Vendors: Absoft, Aitech, Applied Logic Systems, Diab, Franz, Green Hills/Oasys, Language Processors, Inc., MBP Software, Micro Focus, NKR Research, Silicon Valley Software, Tadpole Technology, Telesoft, Translation Systems, Unisoft, Wollongong. Languages: ADA, BASIC, C++, C, COBOL, FORTRAN, LISP, Pascal, PL/M, Prolog, RPG-II.

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This is why the 88000 is no risk at all.

It comes with a complete RISC design environment: assemblers, linkers, code simulators, compilers, emulators, logic analyzers and more.** From companies like Green Hills®/Oasys,® HP,® Language Processors, Inc.® and Tektronix,® to name a few.***

The 88000 also comes with the full support of the 88open, a consortium of over 50 leading hardware and software vendors devoted to making the 88000 the RISC microprocessor standard.

The 88open has already established a Binary Compatibility Standard for the 88000 family, and has mobilized over 30 companies who are developing UNIX application software for 88000 machines. Word Perfect,® Relational Technology,® Frame,® Access®—the list keeps growing.

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LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
TRANSFORMERS								
Toroidal	0	0	71	29	0	0	10.1	8.6
Pot-Core	0	0	57	43	0	0	11.2	8.7
Laminate (power)	0	22	57	21	0	0	8.4	10.7
CONNECTORS								
Military panel	0	33	56	11	0	0	7.1	9.0
Flat/Cable	6	63	31	0	0	0	4.3	4.8
Multi-pin circular	0	33	42	25	0	0	8.2	7.2
PC (2-piece)	0	54	46	0	0	0	5.3	5.6
RF/Coaxial	21	32	42	5	0	0	5.0	5.8
Socket	17	35	26	22	0	0	6.5	4.7
Terminal blocks	6	47	35	12	0	0	6.0	5.4
Edge card	6	44	50	0	0	0	5.3	5.8
D-Subminiature	8	40	44	8	0	0	5.9	5.1
Rack & panel	0	40	40	20	0	0	7.4	6.4
Power	8	50	42	0	0	0	4.8	5.2
PRINTED CIRCUIT BOARDS								
Single sided	6	55	22	17	0	0	6.0	5.6
Double sided	0	38	48	14	0	0	7.1	8.2
Multi-layer	0	25	62	13	0	0	7.7	8.4
Prototype	0	90	10	0	0	0	3.5	5.2
RESISTORS								
Carbon film	55	25	20	0	0	0	2.3	5.6
Carbon composition	53	7	27	13	0	0	4.3	6.5
Metal film	41	30	29	0	0	0	3.2	5.0
Metal oxide	29	29	42	0	0	0	4.2	5.7
Wirewound	20	27	53	0	0	0	5.0	7.6
Potentiometers	33	33	29	5	0	0	4.0	7.0
Networks	19	37	38	6	0	0	5.0	6.4
FUSES	40	27	33	0	0	0	3.4	2.6
SWITCHES								
Pushbutton	20	20	33	27	0	0	7.4	5.8
Rotary	8	30	31	31	0	0	8.1	6.3
Rocker	15	16	46	23	0	0	7.7	5.9
Thumbwheel	10	30	40	20	0	0	7.1	8.1
Snap action	18	19	36	27	0	0	7.6	6.4
Momentary	18	27	36	19	0	0	6.6	7.8
Dual-in-line	11	22	56	11	0	0	6.8	9.4
WIRE AND CABLE								
Coaxial	6	56	31	0	7	0	5.9	5.1
Flat ribbon	29	41	24	6	0	0	4.0	4.1
Multiconductor	21	36	36	7	0	0	5.0	5.4
Hookup	32	45	18	5	0	0	3.5	2.6
Wirewrap	33	34	33	0	0	0	3.6	2.8
Power cords	6	62	19	13	0	0	5.3	6.2
POWER SUPPLIES								
Switcher	0	33	42	17	8	0	9.0	7.3
Linear	10	20	50	10	10	0	8.6	9.9
CIRCUIT BREAKERS	0	42	29	29	0	0	8.0	8.4
HEAT SINKS	8	50	33	9	0	0	5.5	6.9
BATTERIES								
Lithium coin cells	9	45	36	0	0	10	7.3	5.9
9V alkaline	50	33	17	0	0	0	2.3	3.6
Real-time clock back-up	17	33	50	0	0	0	4.9	6.4
RELAYS								
General purpose	8	42	17	33	0	0	7.7	6.9
PC board	12	35	29	24	0	0	7.0	10.8
Dry reed	0	44	12	44	0	0	9.0	9.4
Mercury	0	43	14	43	0	0	9.0	12.5
Solid state	0	46	23	23	8	0	8.8	11.9
DISCRETE SEMICONDUCTORS								
Diode	21	33	21	21	4	0	6.9	6.8
Zener	24	28	19	29	0	0	6.8	8.5
Thyristor	6	31	38	25	0	0	7.8	9.1
Small signal transistor	22	28	33	17	0	0	6.1	7.5
MOSFET	10	30	30	30	0	0	7.9	8.8
Power, bipolar	9	36	28	27	0	0	7.5	8.3
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	7	33	20	33	0	7	9.8	10.0
CMOS	10	45	30	10	0	5	6.8	8.1
TTL	14	42	29	10	0	5	6.6	8.7
LS	20	45	20	10	0	5	6.0	8.4
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	13	24	25	25	0	13	10.6	10.0
OP amplifier	17	32	28	17	0	6	7.6	9.2
Voltage regulator	5	42	37	11	0	5	7.4	8.0
MEMORY CIRCUITS								
DRAM 16K	0	25	13	37	0	25	15.2	12.7
DRAM 64K	7	36	21	21	0	15	10.6	9.6
DRAM 256K	0	33	33	25	0	9	10.2	10.6
DRAM 1M-bit	0	17	17	32	17	17	16.4	14.1
SRAM 4K × 4	0	0	40	40	0	20	15.5	9.7
SRAM 8K × 8	9	0	64	18	0	9	10.6	11.7
SRAM 2K × 8	0	0	50	33	0	17	14.3	12.6
ROM/PROM	0	49	25	13	0	13	9.5	8.8
EPROM 64K	10	20	40	20	0	10	9.9	10.3
EPROM 256K	0	30	30	30	0	10	11.0	9.2
EPROM 1M-bit	0	1	33	33	0	33	18.0	10.7
EEPROM 16K	14	15	43	14	0	14	10.4	9.9
EEPROM 64K	0	15	57	14	0	14	11.5	12.1
DISPLAYS								
Panel meters	0	29	42	29	0	0	8.7	7.7
Fluorescent	0	0	33	67	0	0	13.0	8.7
CRT 12-inch monochrome	0	20	40	40	0	0	9.9	8.9
LED	9	55	18	18	0	0	5.8	7.1
Liquid crystal	0	13	49	25	0	13	12.2	10.2
MICROPROCESSOR ICs								
8-bit	6	44	25	25	0	0	7.1	7.9
16-bit	10	40	30	20	0	0	6.6	9.7
32-bit	13	13	49	25	0	0	8.1	9.5
FUNCTION PACKAGES								
Amplifier	13	13	37	37	0	0	9.0	8.5
Converter, analog to digital	9	19	36	36	0	0	9.0	8.9
Converter, digital to analog	9	28	27	36	0	0	8.5	9.6
LINE FILTERS	0	43	14	43	0	0	9.0	8.2
CAPACITORS								
Ceramic monolithic	39	21	25	15	0	0	4.9	7.0
Ceramic disc	14	31	32	18	0	5	7.8	6.7
Film	14	36	29	21	0	0	6.6	7.9
Aluminum electrolytic	6	55	22	17	0	0	6.0	8.8
Tantalum	7	39	27	27	0	0	7.5	7.5
INDUCTORS	7	33	40	20	0	0	7.2	8.6

Source: Electronics Purchasing Magazine's survey of buyers.

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It's being supported by a complete array of business software. For applications like office automation, desktop publishing, word processing, database management, spreadsheets and MS/DOS-compatible software. And the list is growing.

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The 88open has developed a Binary Compatibility Standard (BCS) that guarantees a standard software design environment for the 88000. So, in the same way that MS/DOS® software runs on any PC, any software written for one 88000-based machine runs seamlessly on every 88000-based BCS-compliant system.

What's more, since AT&T has endorsed the 88000 BCS as the early development platform for their UNIX System V.4 ABI, the 88000 is the fastest way to get to tomorrow's UNIX V.4.

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This 8-bit microcontroller harnesses the power of a 10MHz CPU with a 16-bit internal architecture. It muscles its way through complex math problems with a 200ns minimum instruction cycle time, 2.3μs 16 x 16-bit register multiplies, and 2.6μs 32/16-bit register divides. In addition, the H8/532 supports "C", making it easier for you to put its power to work.

The H8/532 ZTAT™ (Zero Turn-Around Time) microcontroller features an unprecedented amount of one-time user-programmable EPROM. . . 32 Kbytes. The ZTAT microcontroller gets you to market fast. The very day you finish development. No waiting for mask ROM parts. You get unbeatable flexibility—change code instantly without creating an inventory of obsolete devices. The ZTAT feature also saves you money by eliminating mask charges and minimum order quantities. For high volume, you can go to a mask ROM version of the H8/532 for the lowest high-volume unit cost.

The H8/532 contains a wagonload of on-chip peripherals; including 1 Kbyte RAM, 8-channel 10-bit A/D, 8 timers, a serial communications interface, 65 I/O pins, and a data transfer controller—all tightly packed in a small, surface-mount plastic package. This combination of high integration and large memory makes the H8/532 a true single-chip solution.

Now you have the right device for challenging office automation, automotive, industrial, and telecommunications applications. Applications requiring heavy-duty math, I/O, or timing control. The H8/532 provides the horsepower for a broader range of applications than you thought a single 8-bit microcontroller could ever manage.

Development with the H8/532 is easy, with our full stable of development tools running on IBM PC* or VAX* computers: a "C" compiler, a cross-assembler, a simulator/debugger, an in-circuit emulator, ZTAT programming socket adapters, and a low-cost evaluation board. The H8/532 has a familiar architecture, and its instruction set is similar to industry standards.

With the H8/532, you can harness a whole team of Hitachi devices to work together in your application: memories, peripheral devices, logic, LCD drivers, opto and analog ICs.

The H8/532 is the first in a long line of new H8 workhorses. Each created for a different cost/performance objective. All H8 devices have the bloodlines common to all Hitachi products—quality and reliability. For more information on the hard-working H8/532, contact your local Hitachi Sales Representative or Distributor Sales Office today.

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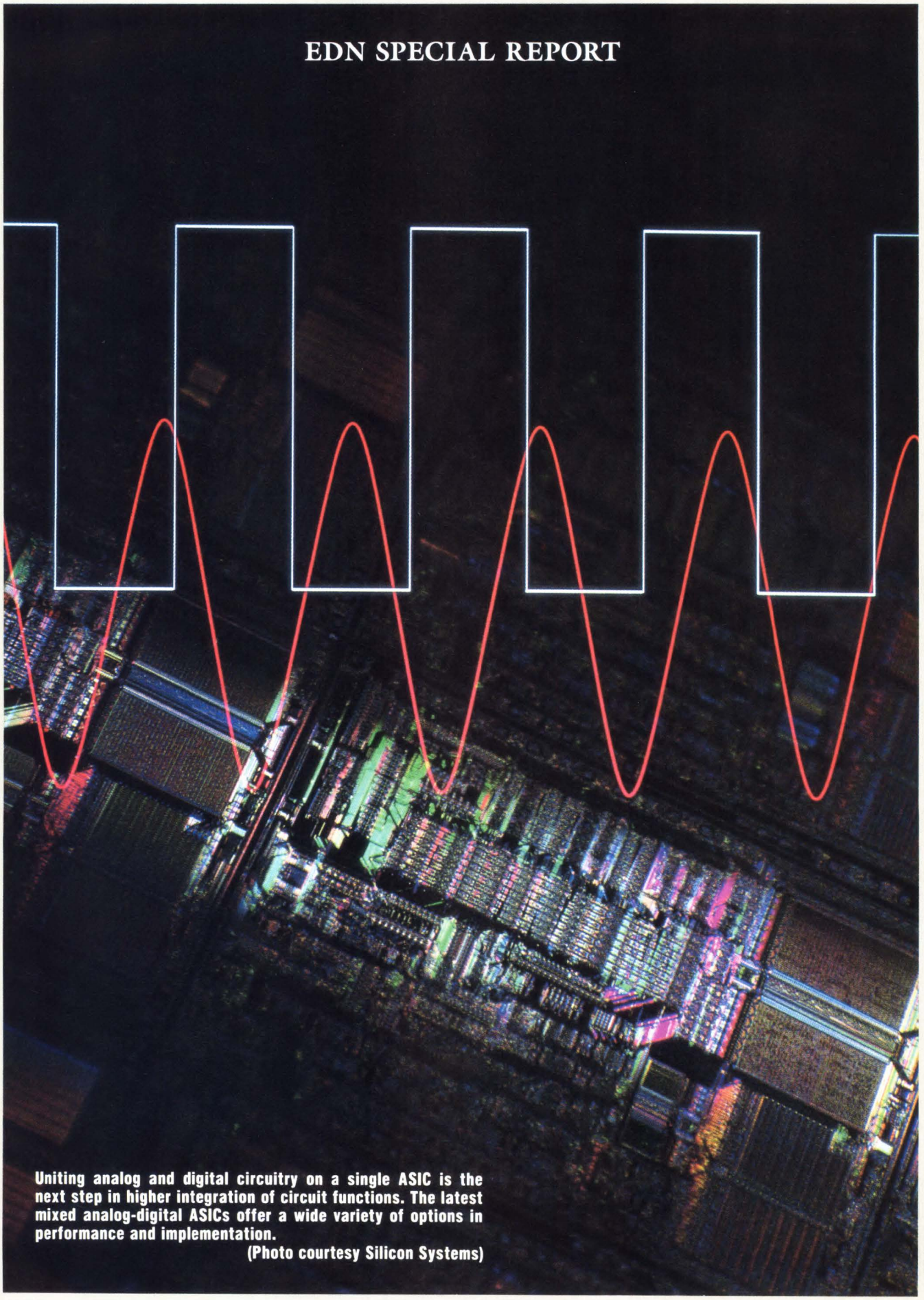


Uniting analog and digital circuitry on a single ASIC is the next step in higher integration of circuit functions. The latest mixed analog-digital ASICs offer a wide variety of options in performance and implementation.

(Photo courtesy Silicon Systems)

MIXED ANALOG-DIGITAL ASICs

Richard A Quinnell, *Regional Editor*

To meet the demand for greater levels of system integration, you can design an ASIC that combines analog and digital circuitry on a single IC. The design options now available, ranging from special-function arrays to large cell-based design libraries, make it simpler than ever to create mixed analog-digital ASICs.

If you're like many system designers, your next project will cry out for high integration. Because of constraints on board size and production costs, you'll want to implement a lot of functions with a relatively low parts count. The solutions you're familiar with—PLDs and programmable gate arrays along with discrete-component analog circuits—won't be adequate for this task; they take up too much board space. You'll need a mixed analog-digital ASIC (application-specific IC).

Mixed analog-digital ASIC technology has expanded in recent years to offer a wide variety of options, both in performance and ease of implementation. You have a choice of process technologies and design strategies. For example, you can design at the transistor level or work with predesigned circuit macros. You may even find an ASIC that is completely prestructured for your application and requires only minor modifications to meet your specific needs. The choice you make will depend on your analog-performance requirements, your circuit's complexity, and the integration level you need.

Consider the process

The first step in choosing a mixed analog-digital ASIC is to consider the process technology. Generally speaking, you'll want to choose a bipolar process for high-performance or high-power applications and a CMOS process for applications that are mostly digital (**Ref 1**). The small-signal npn transistors in most bipolar ASIC offerings have toggle frequencies (f_t) of greater than 500 MHz; some go as high as 6 GHz. In bipolar ASICs, you can find medium-sized power transistors whose current-handling capability is conservatively rated at 200 mA. In fact, transistors with even higher power are available, but they're better left off

You can design a mixed analog-digital ASIC as either an array-based or a standard-cell-based circuit.

chip because their power dissipation and large die sizes complicate the design.

If high integration is your aim, however, CMOS is your best choice. Logic gates are much smaller and easier to implement in CMOS, so you can achieve much higher digital-circuit density. Although their overall linear performance is not as good as that of bipolar devices, CMOS devices handle analog switches and active filters very well.

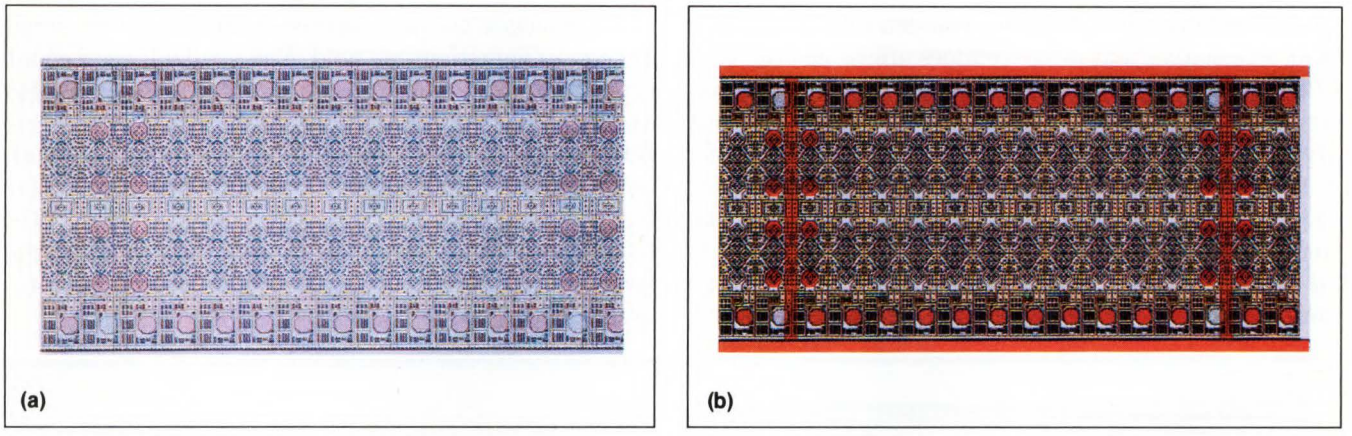
You can design a mixed analog-digital ASIC in one of two ways: It can be either array-based or standard-cell based. Which method you choose will depend strongly on the particular ratio of analog to digital circuits, the performance needed from both the analog and the digital circuitry, and the production quantities. Typically, circuits that use arrays are more than 80% analog, need higher analog performance, and have smaller production quantities. Standard-cell-based circuits are about 30% analog, require better digital performance, and are intended for large-volume production.

Array-based ASICs begin with a partly finished wafer. The array vendor processes the wafer through all the steps necessary to fabricate a collection of disjointed circuit elements. You complete the circuit by specifying its interconnections. This fabrication method allows you to design your circuit without first having to design the transistors. You can then proceed as though you were working with a collection of discrete transistors. If you'd rather design at a higher functional level, you can use a library of macros (layout patterns for commonly used circuits such as op amps), which vendors typically offer to fit their arrays. Designing with the macros is much like designing with off-the-shelf components. If you're weak in analog design, you can always have the vendor assist in or take over the circuit's design while you supply only the specifications.

Because the arrays are partly finished, their NRE costs will be lower than those of standard-cell-based ASICs. For example, when you use the arrays, you'll pay to design two mask layers instead of the typical 16 to 20. NRE costs for arrays range from $3000 to $40,000, depending on how much design the vendor performs. Prefabrication has its drawbacks, however. You may need a different combination of active and passive components or transistor types than the array

TABLE 1—REPRESENTATIVE MIXED ANALOG-DIGITAL ARRAYS

COMPANY	PRODUCT NAME	PROCESS	ANALOG VOLTAGE (V)	TOGGLE FREQUENCY OR GATE DELAY	TRANSISTOR BANDWIDTH	ANALOG/DIGITAL RATIO	GATE CAPACITY	TURNAROUND TIME (WEEKS)
AT&T MICROELECTRONICS	ALA501	BCDMOS	350	10 MHz	N/A	80/20	35	6 TO 8
	ALA450	8-μm BIPOLAR	30	2 MHz	250 MHz	50/50	384	6 TO 8
CHERRY SEMICONDUCTOR	GENESIS	4-μm BIPOLAR	50	50 NSEC	800 MHz	40/60 TO 70/30	250	8
EXAR	DELTA 2000 DELTA 4000	3-μm BIPOLAR	20	—	1 GHz	4 GATES/CELL	VARIABLE	2 TO 4
LSI LOGIC	LAD 310	BiCMOS	5	0.8 NSEC	6 GHz	VARIES	600 TO 46,000	—
MICREL SEMICONDUCTOR	MPD8020	CMOS DMOS BIPOLAR	100	2 NSEC	4 MHz	50/50	200	9 TO 12
MICRO LINEAR	FB3635	BIPOLAR	12	2 NSEC	720 MHz	50/50	132	8
	FB3480	BIPOLAR	36	2 NSEC	720 MHz	VARIES	140	8
SGS-THOMSON MICROELECTRONICS	POLYUSE J	BIPOLAR/ECL	15	100 MHz	3 GHz	75/25 TO 95/5	54 TO 486	4
PLESSEY SEMICONDUCTOR	ULA DF SERIES	BIPOLAR	5	0.8 NSEC	2 GHz	50/50	2500	6
	MA SERIES	CMOS	14	50 MHz	N/A	VARIES	45 TO 1150	8 TO 16
SILICON SYSTEMS	MSA 6600/ 6700/6900	CMOS BIPOLAR/ECL	12	1.8 NSEC	1.5 GHz	50/50 TO 90/10	70	8 TO 10



You can define the transistors as either npn or pnp devices *in the Flexar Delta array from Exar. You can wire a transistor site as either polarity. You choose the array width you need and add bonding pads as necessary to obtain additional I/O lines. The array before bonding pads have been added appears in* ***a****; the array complete with bonding pads is shown in* ***b****.*

provides. To accommodate the difference, you'll have to choose an array large enough to meet the greatest need and waste the extra elements. Worse still, the array may not be available in a size that meets your needs; in that case, you'll be forced to redesign your circuit to fit.

NRE COST	UNIT COST (100,000)	COMMENTS
$35,000	$5 TO $6	INTENDED FOR HIGH-VOLTAGE SWITCHING.
$22,000	$3 TO $4	
$3000 TO $5000	$0.75 TO $3	
$20,000	$1 TO $2	ARRAY DESIGN ALLOWS USER TO SPECIFY SIZE AND COMPONENT MIXTURE.
CONSULT FACTORY		
$30,000 TO $40,000	$5 TO $25	INTENDED FOR SMART-POWER APPLICATIONS.
$40,000	$2.50	
$7500	$5	SPECIALIZED ARRAY FOR SWITCHING-POWER-SUPPLY CONTROL.
$10,000 TO $30,000	FROM $1.17	FIVE ARRAY SIZES IN FAMILY.
$15,000 TO $20,000	$3	ARRAY MIXTURE IS OPTIMIZED FOR EACH APPLICATION.
$10,000 TO $50,000	—	ARRAY MIXTURE IS OPTIMIZED FOR EACH APPLICATION.
$29,000 TO $55,000	$5 TO $10	

Arrays come in two varieties: component arrays and tiled arrays. The component arrays offer a circuit pattern that makes no distinction between analog and digital areas. Tile arrays, on the other hand, have their elements in blocks that are optimized for each purpose. A tile array's block structure simplifies automatic circuit placement and routing, but if you use it, you risk wasting silicon area. An array that has enough digital tiles may have too many analog tiles, or vice versa. Between 25% and 30% of Silicon System's customers, for example, have circuit designs that fit poorly into the company's standard arrays, according to array-development engineer Greg Winner. For those customers, he says, the company creates custom array combinations.

To reduce wasted silicon in their array-based product, Exar developed the Flexar Delta Series. This component array does not have fully defined components. Instead, it offers a collection of generic sites that you define along with your circuit wiring. A transistor site, for example, can become an npn transistor, a pnp transistor, or a buried resistor, depending on the way you connect it. An interconnection site can be used to make signal lines cross one another or can become a capacitor.

The Flexar array is expandable. Instead of being restricted to using a set array size, you can extend the array along one dimension to encompass the number of elements you need. Predefined I/O structures lie along two edges of the array, and the manufacturer places bonding pads as needed along the other two edges once you've chosen the array's size.

If you find after completing your array design that

Prefabrication has drawbacks—you may need a different combination of components or transistors than the array provides.

you're wasting a lot of silicon, you can take advantage of an alternative that many vendors offer—custom ICs. Custom ICs may be less expensive for large production quantities (more than 100,000). You can begin your production with a standard array. Then, when production volumes dictate, you can have the array vendor redesign your circuit to eliminate the waste. When the custom device is ready, you can simply substitute it for the array-based device without disturbing production.

A drawback to many arrays is the relatively small amount of logic they can hold. The available gate count typically ranges from tens to hundreds of gates. One exception is the LSI Logic LAD 310 Series. This BiCMOS tiled array takes the best advantage of both technologies: Its analog tiles are fabricated in bipolar technology and its digital tiles are fabricated in CMOS technology. The arrays come in a variety of sizes; the largest size offers as many as 46,000 usable gates together with enough transistors for 100 op amps.

Control costs by planning for test

When you design a mixed analog-digital ASIC, you should be aware that device testing will contribute significantly to your ASIC's production cost. Fortunately, you can influence this cost early in the design stage. The more you design for testability, the less testing will cost when your ASIC is in production. For example, by adding analog multiplexers to your circuit, you can partition your design into smaller sections that can then be tested independently. The way you partition your design's analog section affects both how easy test development will be and how fast you can test devices during production. The more time and money you spend on developing test software, the less you'll spend on production testing, and vice versa. You'll have to make that tradeoff in the design stage, therefore.

There are essentially three levels at which you can partition your design's analog portion (**Ref A**). At the first level, you separate the digital and analog sections, providing a means of controlling their input lines and monitor their output signals independently of each other. This level allows you to test your digital logic at high clock rates without being concerned about the response time of the analog circuitry. You can then test the analog section as a block, verifying its performance without bothering with the details of its internal performance. Choosing this level results in a reduced set of tests for the analog section, but the tests are highly customized, and hence error prone. The test-development time may be long and the fault coverage may not be as high as you require. You may also have a hard time finding someone capable of writing a thorough test program for your ASIC.

The second level of partitioning divides the analog section further, segregating functional blocks such as comparators and instrumentation amplifiers. Writing test programs for these blocks is a much easier task. You could develop a library of generic test software and adjust its parameters for specific implementations. This library would then be applicable to many devices. The disadvantage of this method, of course, is that the amount of device overhead required, both in silicon and I/O pins, will increase. Test time may also increase, because you're performing more tests.

The third level of partitioning permits you to test each analog component individually. Creating the test software becomes almost trivial. You can use standard test routines and obtain the test specifications from data sheets. Unless you have only a few analog elements, however, the test-pin requirements can be prohibitive.

Ultimately, the level of partitioning you choose is a matter of tradeoffs. The finer a partition you use, the easier and more reliable the test will be, but the more time you'll spend writing the test software. Another way to look at the tradeoff is that as test-development costs go down, test time and test-related device overhead increases. You must decide in the design stage which of these tradeoffs you're willing to make.

Reference

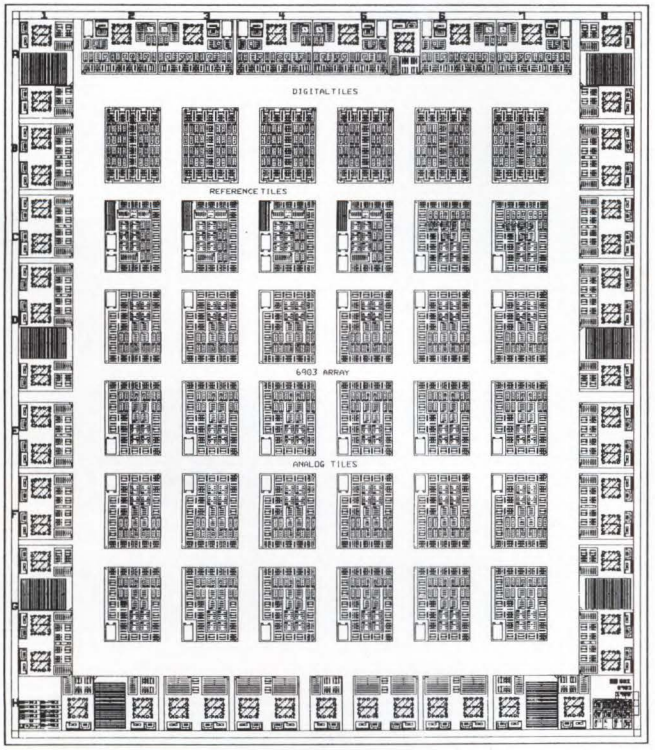
A. Bubrowski, Ken, and Thomas Wang, "Mixed analog/digital ASICs," *VLSI Systems Design*, September 1988, pg 60.

If arrays are not adequate for your needs, consider using a cell-based design. Cell-based designs, also called all-layer semicustom devices, do not begin with prefabricated circuit elements. All the fabrication steps depend on your design. You define your circuit by using functional blocks that are already designed and stored in the vendor's standard-cell library. Both analog and digital functions are included, so designing with these standard cells is much like designing with discrete devices.

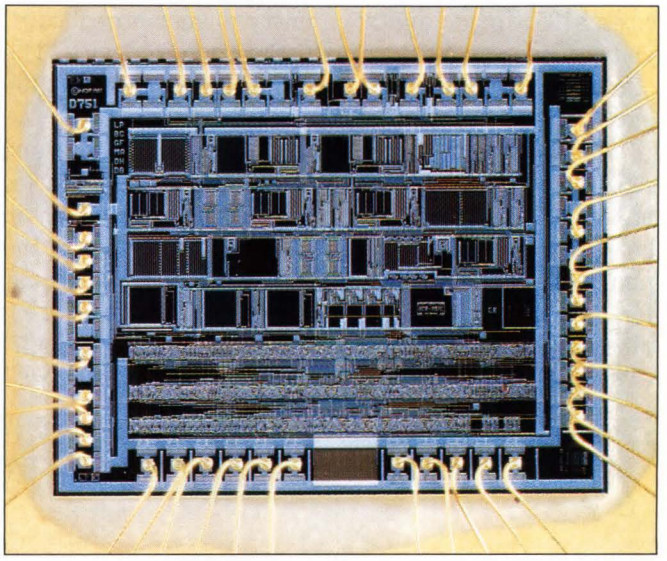
Design a standard-cell-based circuit

The term "standard cell" refers to a cell's physical design: The cells have uniform height; they vary in width to accommodate the number of transistors needed. The common height dimension simplifies cell placement and makes it easy to route power and signal connections. The method applies to both analog and digital cells, although the heights are different. (Digital cells are much smaller than analog cells.)

You design a standard-cell-based circuit by using functional blocks drawn from the vendor's cell library. Library entries come in a variety of forms, including cells, megacells, compiled cells, and soft macros. Many SSI functions are simply single cells. Megacells are large functions that can't fit into the standard height. Compiled cells are standard-height cells that vary in width depending on the circuit's needs. A memory array, for example, is a compiled cell that varies with the number of bits needed. Soft macros are larger functions composed of a set of cells. However, the set has no defined form; it is defined as needed to fit the available space. Further, the overall shape doesn't have to be rectangular.



Separate digital and analog tiles *are visible in this array from Silicon Systems.*



Standard-height cells form rows *that make it easier for you to route the power and signal lines in this cell-based design. The analog cells are much larger than the digital cells. (Photo courtesy NCR)*

No tools needed

Typically, you need a workstation, such as a Sun or Apollo machine, to perform schematic capture, and you need a workstation or a mainframe to perform simulation when designing a standard-cell-based ASIC. An exception to this workstation requirement is the standard-cell offering from Advanced Linear Devices. You design an ASIC with the company's cells the same way you would design a board with its standard products—you create a schematic, then breadboard your design to test its performance. If the breadboard works in your system, the company claims, so will the ASIC.

The reason this technique works is that the company's standard products are also the standard cells. The technique's similarity to board design allows you to create a mixed analog-digital ASIC with a minimal investment in tools. The FSK-11 design kit costs $185 and contains samples of all the company's standard-cell

Arrays come in two varieties: component arrays and tiled arrays.

analog parts. A kit for military-grade parts, FSK-12, costs $495. To add digital circuitry to your breadboard, you can use any 4000 or 74HC Series logic device. The standard-cell ASIC can accommodate as many as 100 gates.

Vendors of both array-based and standard-cell-based ASICs simplify your design task by offering libraries having predefined components. A major problem in creating libraries of analog functions, however, is the number of possible library entries. "Seven cells account for 60% of digital cell usage," says IMP's marketing director, Peter Hillen, "but analog cells are more fluid." "The 80/20 rule—20% of the library accounts for 80% of usage—just doesn't hold for analog," says Plessey applications engineer Phil Welsh.

To accommodate the nearly infinite variety of analog needs, IMP, Gould/AMI, and several other companies have chosen to use their cell libraries simply as a starting point. The companies then modify the cells to accommodate specific needs, taking the analog design out of the customer's hands entirely. Sierra Semiconductor has chosen to create a very rich library of functions: It offers more than 300 analog and digital cells.

A number of other vendors have taken a niche approach, modifying their cell libraries and arrays to meet the needs of specific application areas. Plessey

TABLE 2—MIXED ANALOG-DIGITAL STANDARD CELLS

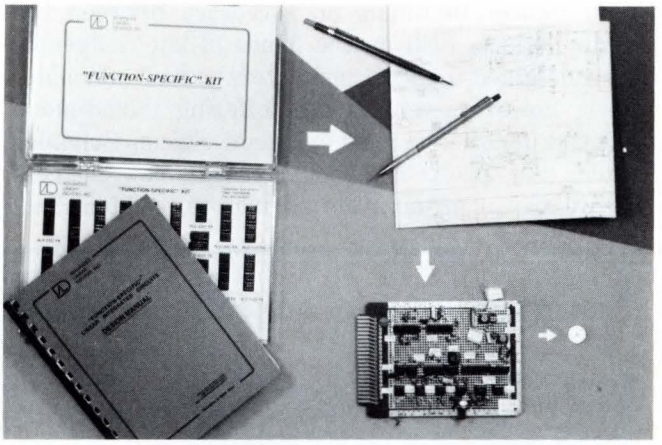
COMPANY	PRODUCT NAME	PROCESS	ANALOG OPERATING VOLTAGE (V)	GATE DELAY	DESIGN TOOLS REQUIRED	PROTOTYPE TURNAROUND (WEEKS)
ADVANCED LINEAR DEVICES	FUNCTION SPECIFIC	3-μm CMOS SINGLE METAL	±7.5 OR 15	SIMILAR TO 74HC OR 4000 SERIES CMOS	DESIGN KIT	12 TO 16
ANALOG DEVICES	BiCMOS MIXED SIGNAL	2-μm BiCMOS	±15	6 μSEC	NONE	30 INCLUDING DESIGN TIME
EXAR	N2000	2-μm CMOS	18	0.8 NSEC	MENTOR	8 TO 10
GOULD AMI	CCI MIXED MODE	2-μm CMOS 2-LEVEL METAL	±6 OR 12	2.5 NSEC	SPICE ON WORKSTATION	8
INTERNATIONAL MICROELECTRONIC PRODUCTS	ACL 1.2 DCL 1.2	1.2-μm CMOS	3 TO 11	0.5 NSEC	—	10 TO 14
MICRO POWER SYSTEMS	—	BIPOLAR CMOS BiCMOS	36	1.2 NSEC	SCHEMATIC CAPTURE	20 TO 26 INCLUDING DESIGN
NATIONAL SEMICONDUCTOR	SCL SERIES	2-μm CMOS BiCMOS 2-LAYER METAL	15	0.9 NSEC	D4 ON SUN, DEC, OR APOLLO	6 TO 8
	CLASIC	BIPOLAR	15	1.8 NSEC	IBM PC SCHEMATIC CAPTURE	8 TO 10
		CMOS	12	2 NSEC		
NCR MICROELECTRONICS	VS1500	1.5-μm CMOS 2-LAYER METAL	5	0.4 NSEC	NCR PROPRIETARY	5 TO 8
	VS2000	2-μm CMOS 2-LAYER METAL	5	0.55 NSEC		
SEATTLE SILICON	CHIPCRAFTER/MAX	1.2-, 1.5-, AND 2-μm CMOS	5	<1 NSEC (1.2-μm PROCESS)	MENTOR/APOLLO VALID/SUN	8
SGS-THOMSON MICROELECTRONICS	TSGSM SERIES	3.5-μm HCMOS 1 METAL LAYER 2 POLY LAYERS	12	6 NSEC	ANALOG DESIGN SYSTEM ON VAX, DAISY, OR MENTOR	7 TO 10
SIERRA SEMICONDUCTOR	SC8000	1.5-μm CMOS	3.3 OR 5	1 NSEC	MONTAGE DAISY MENTOR	5 TO 7
STANDARD MICROSYSTEMS	CUSTOMIZATION	1.6-μm CMOS 2-LAYER METAL	4 TO 6	1.1 NSEC	—	7
UNITED SILICON STRUCTURES (US2)	—	1.2-, 1.5-, AND 2-μm CMOS	5	0.57 NSEC	SOLO 1200	<6

Semiconductor, for example, offers arrays structured to meet the needs of disk-drive manufacturers.

Another niche-oriented array vendor, Micrel Semiconductor, has designed its MPD8020 array for smart-power applications. The array has power FETs and predefined areas for an op amp, an overtemperature sensor, a bandgap reference, a comparator, and a digital gate array. You define the logic and interconnections, then specify such details as amplifier gain and comparator thresholds to create your customized device.

Micro Linear has taken a similar approach with its FB3480 switch-mode power-supply array. The array contains all the building blocks needed for a switch-mode controller: oscillator, voltage reference, error amplifier, undervoltage lockout, and drivers. You also have a user-definable area for comparators, logic, and other circuits. You design your custom logic, then give final specifications for the analog building blocks. In eight weeks, you can get a customized switch-mode controller for an NRE cost as low as $7500.

NRE COST	COMMENTS
$20,000 TO $50,000	YOU DESIGN BY BREADBOARDING A CIRCUIT WITH THE DESIGN KIT.
$50,000 TO $200,000	TURNKEY DESIGN SERVICE.
$35,000 TO $100,000	VENDOR DOES ANALOG DESIGN.
VARIES	CUSTOMER DOES DIGITAL DESIGN; VENDOR DOES ANALOG DESIGN.
$35,000 TO $80,000	
FROM $70,000	TURNKEY DESIGN SERVICE FROM SCHEMATIC. CELLS COME FROM STANDARD PRODUCTS.
FROM $40,000	BREADBOARD KIT AVAILABLE.
$35,000	CMOS DESIGNS ARE TURNKEY ONLY.
$30,000 TO $50,000	CUSTOMER DOES DIGITAL DESIGN; VENDOR DOES ANALOG DESIGN.
$35,000 TO $70,000	DESIGN SERVICE WITH FOUNDRY CONTACTS.
$10,000 TO $40,000	
$60,000	
$25,000 TO $55,000	CUSTOMER DOES DIGITAL SCHEMATIC CAPTURE ONLY; VENDOR DOES ANALOG DESIGN AND IC LAYOUT.
$10,000 TO $50,000	LOW-VOLUME/PROTOTYPE SERVICE 10 TO 10,000 PIECES; E-BEAM DIRECT WRITE; NO MASK CREATED.



You don't need special design tools *when you use Advanced Linear Devices' design kit. The company's design library consists of standard cells that the firm also offers as off-the-shelf parts. After you design a breadboard with those parts, the company simply turns your breadboard into an ASIC.*

Regardless of the design methods you have chosen, you will want to simulate your circuit to verify its performance before you begin fabricating a prototype. In the past, the lack of adequate CAD tools—simulation in particular—has been a major stumbling block to the engineer who designed mixed analog-digital ASICs. That situation has changed. Several major vendors have announced mixed-mode simulators that they believe will chip away at that stumbling block. Their goal is to provide you with a simulator that allows you to validate your design without your first having to become an IC expert. Says Gould/AMI's engineering vice president, Gerald Homstad: "Without an effective, accurate, timely mixed-mode simulator in the customer's hands, this is effectively a custom business."

Early attempts at mixed-mode simulation simply handled the digital and analog sections separately, using logic simulation and Spice. There was no method of accounting for interaction between the two parts. If the digital portion was small enough, Spice was used for the entire circuit. Then vendors created glue software that allowed the two simulators to exchange intermediate results. This method did little to resolve

Some vendors take a niche approach, modifying their cell libraries and arrays to meet the needs of specific application areas.

the differences in timing and accuracy between the two simulations. Still, in the hands of knowledgeable users, the glued-together simulators proved adequate.

Now, however, vendors are offering mixed-mode simulators for the systems engineer. Silicon Compiler Systems (San Jose, CA), which created a new business unit to develop mixed-mode simulators, combined its Lsim digital simulator with Meta-Software's (Campbell, CA) HSpice. Sierra Semiconductor combined its schematic-capture and modeling software with SCS tools to produce Montage, a mixed-mode simulator that's fast enough to evaluate design changes interactively. Analogy (Beaverton, OR) has combined its Saber analog behavioral simulator with GenRad's

Manufacturers of mixed analog-digital ASICs

For more information on ASICs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Advanced Linear Devices
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Sunnyvale, CA 94086
(408) 720-8737
Circle No 650

Analog Devices
Box 9106
Norwood, MA 02067
(508) 658-9400 ext 216
Circle No 651

Aptek Technologies Inc
700 NW 12th Ave
Deerfield Beach, FL 33442
(305) 421-8450
TLX 441020
Circle No 652

AT&T Microelectronics
555 Union Blvd
Dept 50AL330240
Allentown, PA 18103
(800) 327-2447
Circle No 653

Cherry Semiconductor
2000 S County Trail
East Greenwich, RI 02818
(401) 885-3600
TLX 6817157
Circle No 654

Exar
222 Qume Dr
Box 49007 San Jose, CA 95161
(408) 434-6400
TWX 910-339-9233
Circle No 655

Gould/AMI
2300 Buckskin Rd
Pocatello, ID 83201
(208) 233-4690
Circle No 656

International Microelectronic Products (IMP)
2830 N 1st St
San Jose, CA 95134
(408) 434-1281
TLX 4991041
Circle No 657

LSI Logic
1551 McCarthy Blvd
Milpitas, CA 95035
(408) 433-8000
TLX 172153
Circle No 658

Micrel Semiconductor
560 Oakmead Parkway
Sunnyvale, CA 94086
(408) 245-2500
TWX 910-379-0007
Circle No 659

Micro Linear Corp
2092 Concourse Dr
San Jose, CA 95131
(408) 433-5200
Circle No 660

Micro Power Systems
3151 Jay St
Santa Clara, CA 95054
(408) 727-5350
TWX 910-338-0154
Circle No 661

Micro-Rel
2343 W 10th Pl
Tempe, AZ 85281
(602) 968-6411
TWX 910-950-1941
Circle No 662

National Semiconductor
2900 Semiconductor Dr
Box 8090
Santa Clara, CA 95052
(408) 721-3031
Circle No 663

NCR Microelectronics
2001 Danfield Ct
Fort Collins, CO 80525
(303) 226-9500
Circle No 664

NEC Electronics
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Mountain View, CA 94039
(415) 960-6000
TWX 910-379-6985
Circle No 665

Plessey Semiconductor
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Scotts Valley, CA 95006
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Seattle Silicon
3075 112th Ave NE
Bellevue, WA 98004
(206) 828-4422
Circle No 667

SGS-Thomson Microelectronics
1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6100
TLX 249976
Circle No 668

Sierra Semiconductor
2075 N Capitol Ave
San Jose, CA 95132
(408) 263-9300
Circle No 669

Silicon Systems Inc
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(714) 731-7110
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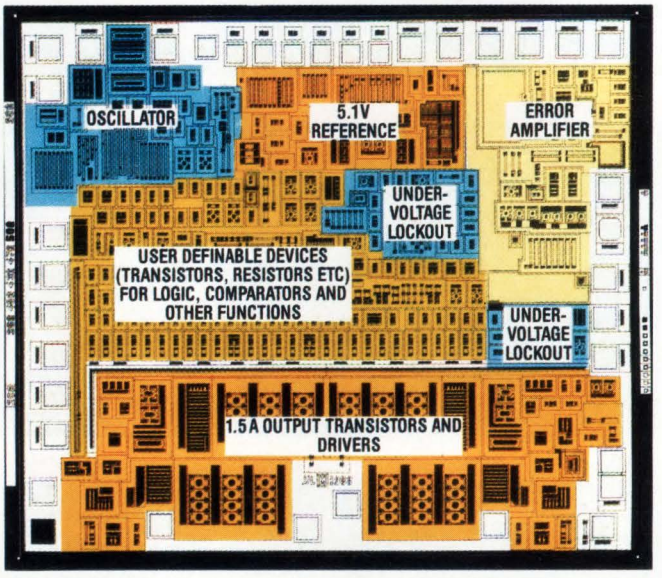

***This special-purpose array**—Micro Linear's ML34380—provides all the functions needed for a switch-mode power-supply controller. The user customizes the logic area and sets specifications for the major analog blocks.*

(Concord, MA) Hilo and with Gateway's (Westford, MA) Verilog digital simulators. NCR has teamed up with Analogy and HHB Systems (Mahwah, NJ) to link Saber/CADAT with NCR's proprietary DesignSim tools. And Seattle Silicon has added the Mixed ASIC Expert (MAX) option to its ChipCrafter design system.

The long-term goal of many vendors of mixed analog-digital ASICs is to give their customers the ability to customize their own cells. Both IMP and Gould/AMI are developing tools to generate compiled analog cells—cells that are computer designed from a set of parameters. The first results are already available from IMP, which offers a compiled switched-capacitor filter. The designer need only specify the filter's characteristics; the software creates the cell. Gould/AMI expects to have a similar filter-design tool for in-house use this year. Beyond that, however, no manufacturer has released any definite timetable for any other kind of analog cell. EDN

Reference

1. Moore, Bruce and Will Ritmanich, "Consider the trade-offs when evaluating linear-semicustom ICs," *EDN*, February 4, 1988, pg 135.

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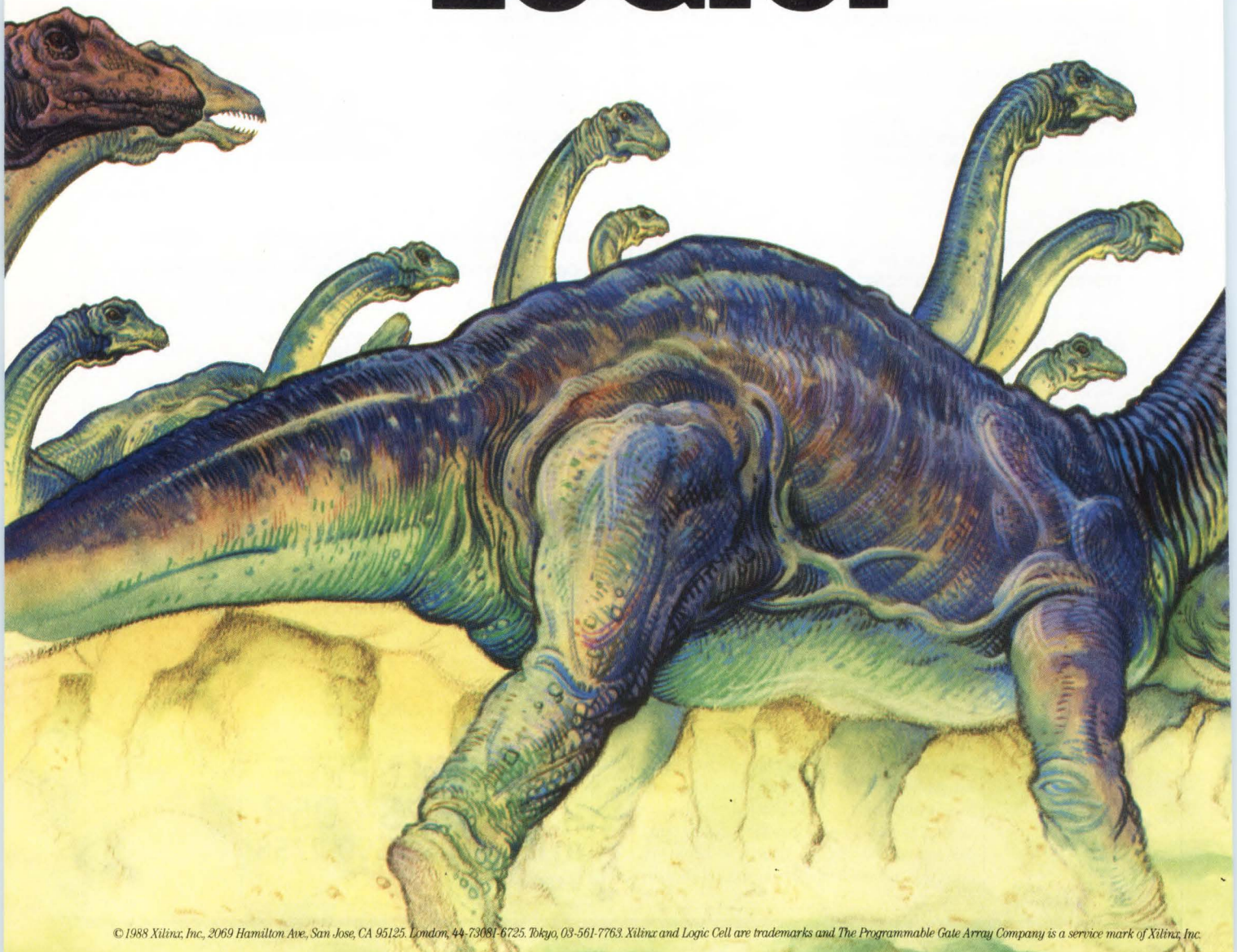

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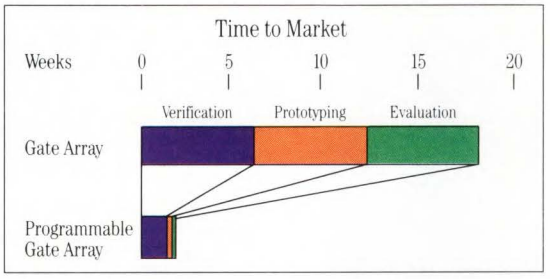

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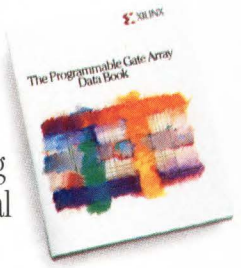

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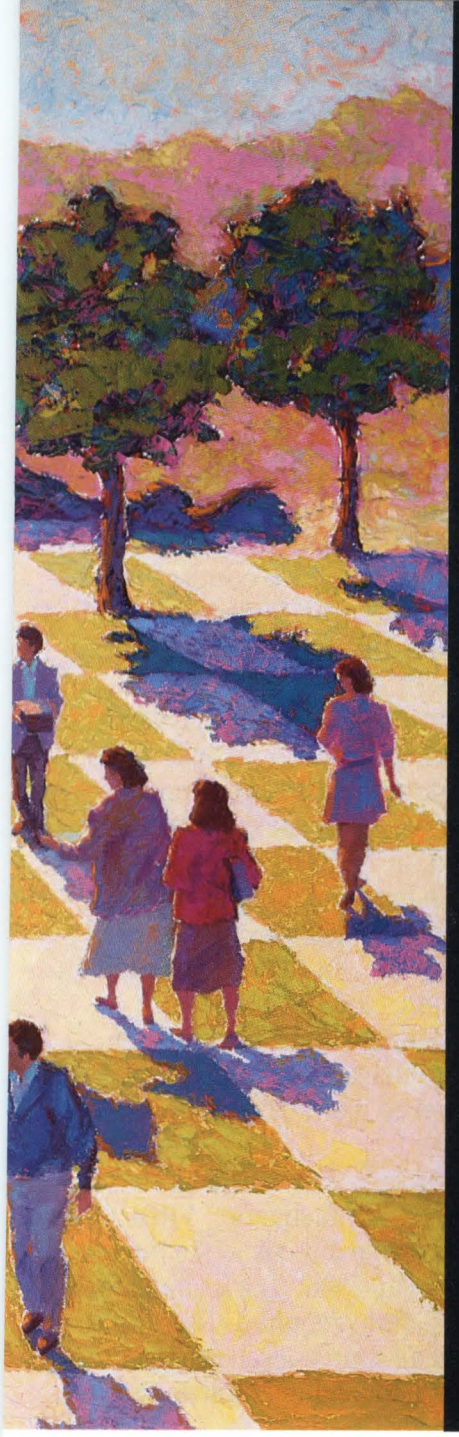

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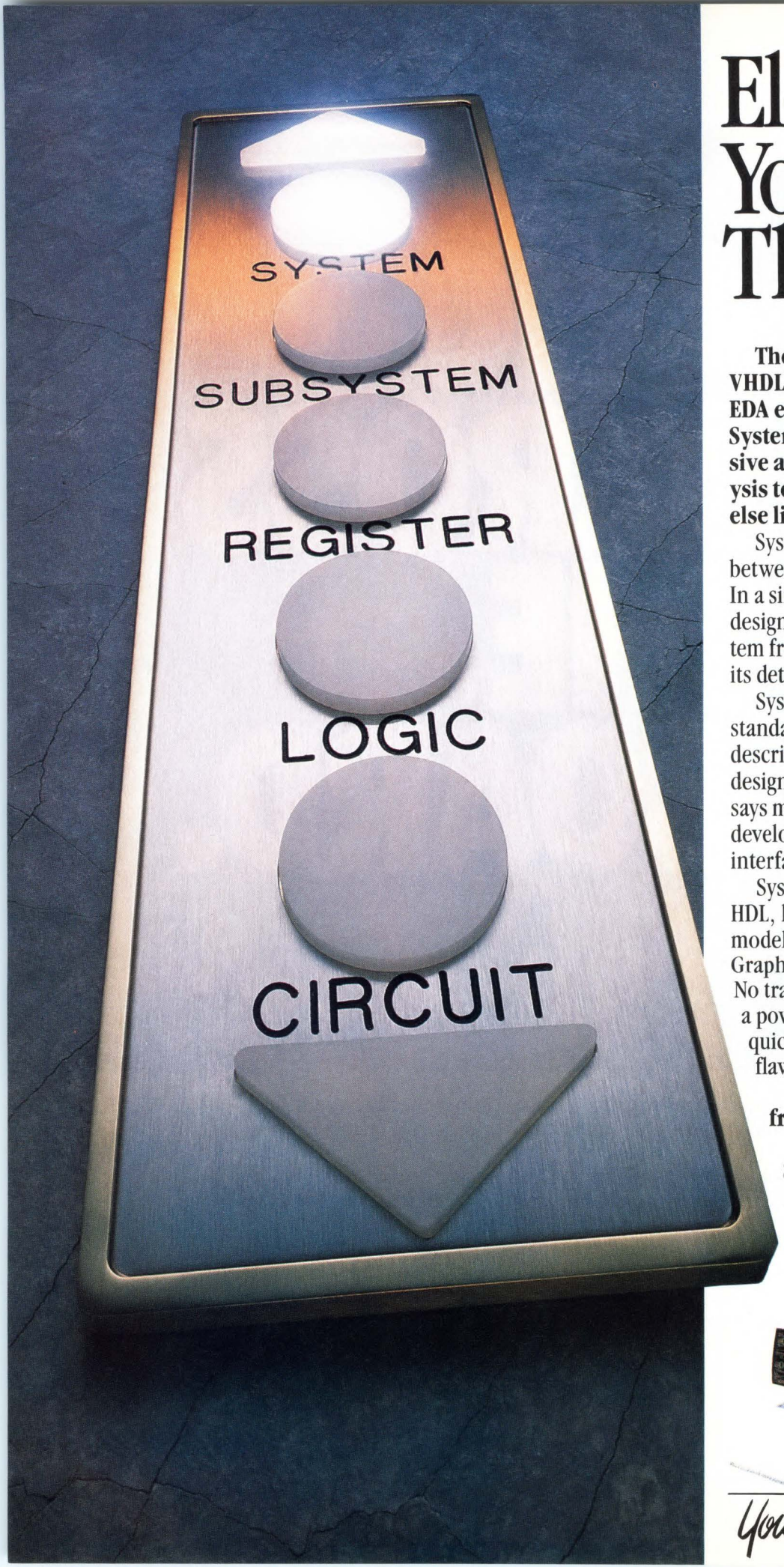

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Delta modulators simplify A/D conversion

Although you can use many different methods to perform A/D conversion, few are as flexible as delta modulation and none exceed its harware simplicity.

Barry Harvey, *Elantec Inc*

Delta modulators are useful circuit tools for performing A/D conversion. Although they can't convert rapidly changing analog inputs with high accuracy, delta modulators can perform highly accurate conversions on slow inputs or moderately accurate conversions on audio-frequency inputs. Keeping these speed constraints in mind, you can take advantage of a delta modulator's key attributes—hardware simplicity and circuit flexibility. Delta modulators let you enhance a variety of performance characteristics such as conversion accuracy, dynamic range, and noise level. By modifying the basic delta-modulator circuit, you can configure several circuits, including an A/D converter, a quantized-feedback converter, a V/F (voltage to frequency) converter, and a companding modulator.

Fig 1 shows the basic components of a delta modulator. The circuit compares the analog input to a feedback current that comes from the integrator's input and goes through R_f. The comparator compares the summing junction to 0V and passes on the result to the input of the D-type flip-flop. The flip-flop's output controls an analog switch that connects R_{INT} to either V_{REF+} or V_{REF-}, thereby completing an overall feedback path. The DG243 analog switch and the flip-flop's digital data-out line are clocked and change state only once per clock cycle. The delta modulator is thus a servo system that attempts to balance the duty cycle of a stream of pulse-coded bits against an analog input voltage or current.

Delta modulators perform only one bit (an unweighted bit) of digital conversion per clock cycle out of the maximum 2^{n-1} possible counts of an n-bit digital word. A delta modulator therefore requires 2^n clock cycles to complete a full-scale A/D conversion. Fortunately, because of their hardware simplicity, delta modulators can run on fast clocks. Although a delta modulator performs many of the same functions as an integrating A/D converter, a delta modulator's output is useful even in the middle of the 2^n possible counts. Like a tracking A/D converter, a delta modulator attempts to keep a valid running total of the analog input.

Choose components carefully

Because high clock frequencies are present in the circuit, you must carefully select the components in your delta modulator. The comparator should have a propagation delay that's short compared with the circuit's clock period. Also, the comparator should have a high gain to preserve the modulator's noise characteristics. Because the circuit's servo action keeps the comparator inputs nearly in balance, the comparator shouldn't exhibit any tendency to oscillate. The EL2018 comparator satisfies these criteria; it has a fast response time (20 nsec) and a high gain (30,000). More-

A delta modulator is a servo system that attempts to balance the duty cycle of a stream of pulse-coded bits against an analog input signal.

over, the EL2018 is less prone to oscillate than a typical ECL comparator.

Another device, the EL2019, combines a D-type flip-flop with a comparator. This device doesn't provide the amplified comparator output that can generate parasitic feedback to the input. You can also use the LM311 comparator, which can work at clock rates to 2 MHz.

The integrator op amp you select should have a gain-bandwidth product at least as great as the clock frequency. If the integrator doesn't have a high enough gain-bandwidth product, it won't effectively filter out the analog switch's waveform and will therefore degrade the system's noise characteristics. In **Fig 1**'s circuit, the EHA2500 maintains a low enough output impedance at high frequencies to preserve its filtering ability. However, many op amps, such as those whose main compensation device is a Miller integrator, don't maintain a low output impedance at moderate-to-high frequencies. The 2500 series of op amps are compensated with a capacitor connected to a supply rail (ac ground) and therefore display better impedance characteristics as a function of frequency.

The final component of a delta modulator that you must select is an analog switch. The suggested DG243 switch has a reasonably low charge injection. The charge injection occurs with every transition of the analog switch's digital control input. The integrator captures the charge as an error. The higher the clock frequency, the greater the number of output data transitions per second and the greater the accumulated error due to the charge injection.

A delta modulator's output is a pair of serial lines—a data line and a synchronizing-clock line. **Fig 2** shows the analog input (V_{IN}), the integrator's output, and the digital data stream. Note that the servo action of the modulator loop attempts to make the integrator's output closely track the negative of the analog input. The summing-junction voltage therefore represents the accumulated error of the modulator output with respect to the input analog signal. When the analog input rises, the summing-junction voltage rises, and the comparator provides a series of ones through the flip-flop. The stream of ones causes the analog switch to connect R_{INT} to V_{REF+} more often than V_{REF-} and drive the integrator output more negative, thereby balancing V_{IN} at the summing junction.

Because the digital stream in **Fig 2** isn't synchronized to the analog input, the stream appears as a blur of transitions. Note that a majority of ones occur if the input has a positive slope (shown as a thick trace at a high logic level). Conversely, if the analog input has a negative slope, a majority of zeros result, and the regions of zero slope establish a 50% duty cycle in the

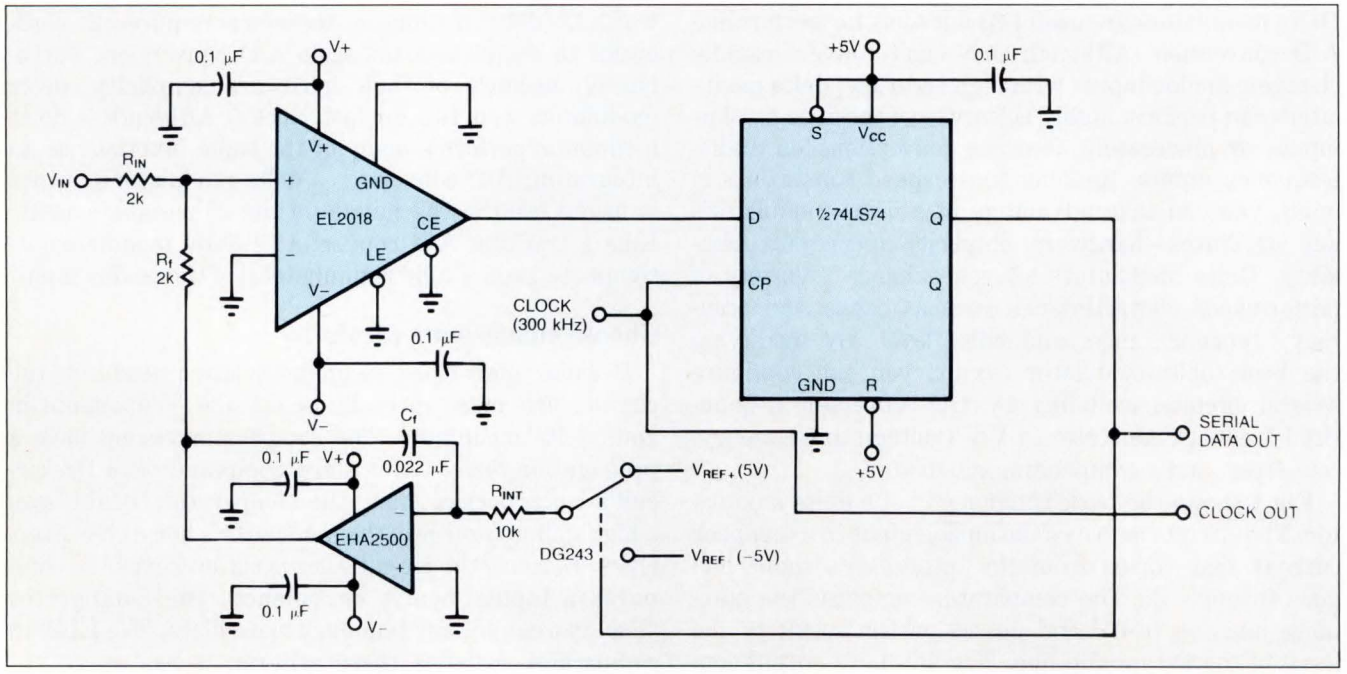

Fig 1—The basic components of a delta modulator *include a comparator, an integrator op amp, a D-type flip-flop, and an analog switch.*

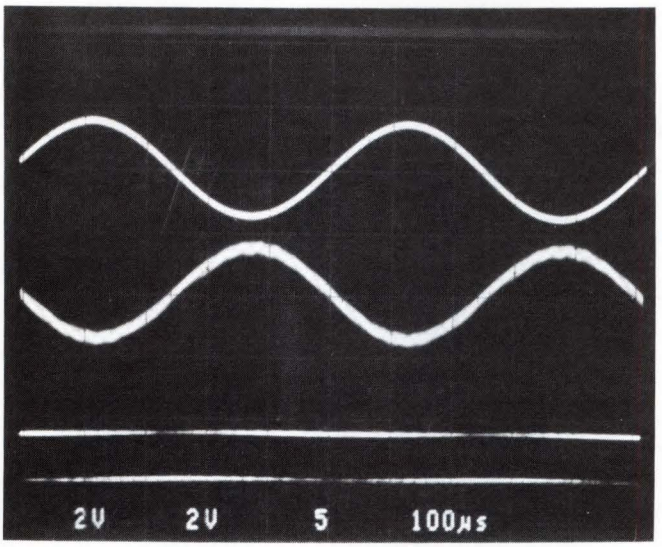

Fig 2—A scope trace from Fig 1's circuit *shows the analog input, the integrator's output, and the serial-data output. Note that the servo action of the modulator loop attempts to make the integrator's output closely track the analog input.*

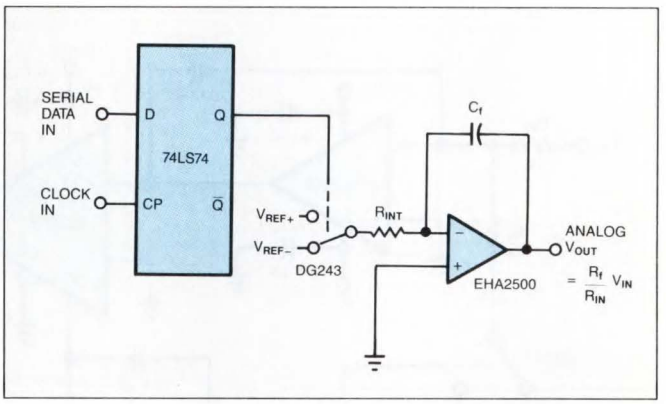

Fig 3—You can convert Fig 1's digital output back to analog form. *The EHA2500's internal feedback resistance is in shunt with the capacitor, C_f, thus restoring the dc level.*

digital output data. Also, note that the digital output continuously attempts to track the moving analog input. In **Fig 2,** the analog input is set near the modulator's slew-rate limit to enhance the digital pattern for the photograph. Normally, the output-data stream has about a 50% duty cycle, which makes the patterns in the stream difficult to see.

The integrator, which is placed in the feedback path, causes the output data to represent the derivative of the input. When the modulator receives a steady input voltage, the integrator output settles to a balanced level. The integrator doesn't require a net-input current to maintain this level. The digital output then produces an equal number of zeros and ones so that the analog switch toggles equally between V_{REF+} and V_{REF-} and provides a net-zero input current to the integrator. A rising input causes the summing junction to rise and causes the comparator to output more ones through the flip-flop. You can assume that each one in the digital data output is equal to the input; the change in the output is equal to

$$\frac{V_{reft}(R_{in}/R_f)}{R_{int}C_fF_{clock}}.$$

A zero represents the negative of the above equation. The resulting voltage is the LSB value, and the rms noise is ⅓ this voltage.

If $R_{IN} = R_f$ and the largest V_{IN} equals V_{REF}, the dynamic range is $2R_{INT}C_{INT}F_{CLOCK}$. You can maximize the dynamic range by raising C_{INT} and F_{CLOCK} as much as possible. The maximum slew rate that the integrator can accommodate is determined by I_{INT}/C_f. In **Fig 1**'s circuit, I_{INT} is set at 2 mA. In a circuit that properly handles a 10V p-p input to 3 kHz, the analog slew rate will be 0.094V/μsec. You must therefore limit C_f to a maximum of 0.022 μF. Using this value and the dynamic range of 256 (8-bit quantization), the clock frequency should be at least 2.3 MHz. You can increase the clock frequency in this circuit tenfold and still obtain a signal-to-noise ratio as high as 72 dB.

You can convert the digital output from **Fig 1** back to analog form by using the circuit in **Fig 3**. The lack of a dc baseline in the integrator output presents a problem, but you can restore the dc level by placing a resistor, R_{fINT}, across the capacitor, C_f. R_{fINT}, however, degrades the filtering action of the integrator and adds quantizing noise equal to

$$2(R_f/R_{in})(V_{ref})(R_{int}/R_{fint}),$$

which is limited in bandwidth to about $F_{MAX}(R_{INT}/R_{fINT})$. To minimize the conversion noise in this example, R_{fINT} should be greater than 512 R_{INT} for a 2.3-MHz clock. Note that the integrator and the V_{REF} offsets are magnified by the ratio R_{fINT}/R_{INT}.

To avoid the dc offset problem inherent in a classic delta modulator, you can use the circuit of **Fig 4**. In this configuration, the digital output represents the level of the actual signal, not its derivative. The comparator attempts to null the integrator output by providing a string of ones and zeros whose duty cycle tracks the average value of the input. The integrator's

A delta modulator's serial digital output takes the form of a data line and a synchronizing-clock line.

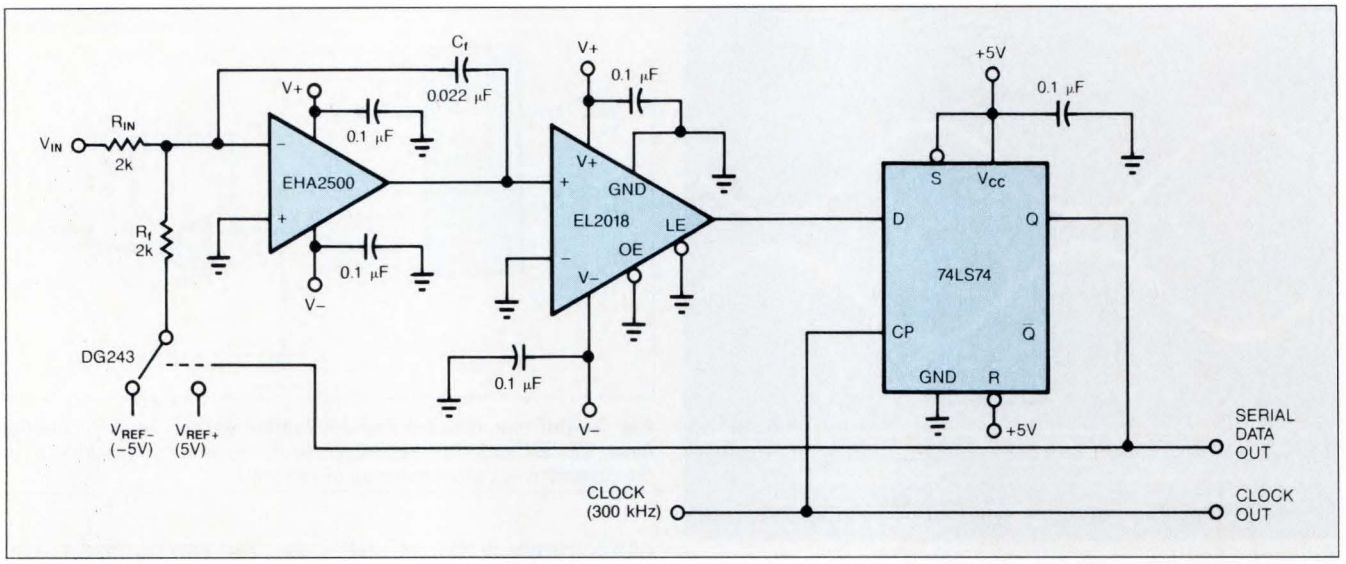

Fig 4—An average-output delta modulator *avoids the dc-offset problem inherent in a classic delta modulator. The digital output represents the level of the actual signal, not its derivative.*

output represents the derivative of the modulator's error.

One of the oddities of delta modulators is that their digital outputs are sometimes unpredictable. Many possible bit patterns can represent an analog input, but a modulator often chooses its own pattern. Much of this unpredictability is caused by digital feedback that goes to the input of the integrator or the comparator. At high clock rates, the integrator has difficulty maintaining the attenuation implied by its $R_{INT}C_f$ product. An op amp with a gain-bandwidth product comparable to the clock frequency can alleviate this problem.

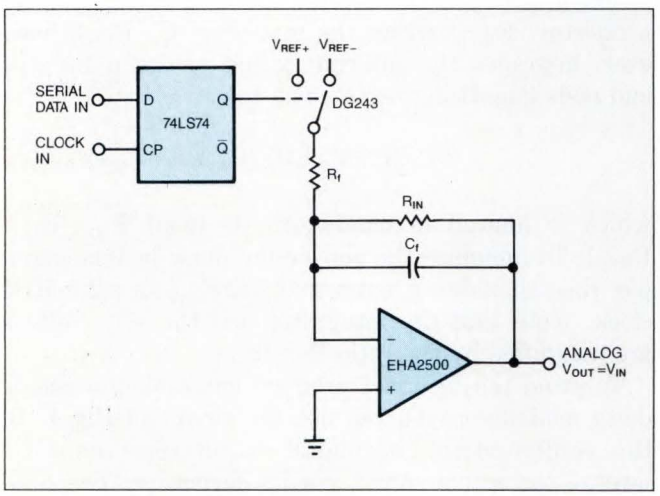

Fig 5—In a demodulator circuit, *the offsets are magnified by the ratio R_{in}/R_f+1. The circuit's gain accuracy is usually limited only by resistor ratios.*

You can convert **Fig 4**'s digital output to analog data by using the circuit in **Fig 5**. In this configuration, the offsets are magnified by R_{IN}/R_{f+1}; R_{IN}/R_f is approximately equal to unity in most cases. This circuit's gain accuracy is usually limited only by resistor ratios. The circuit's noise and dynamic range are typically 6 dB worse than that of a standard delta modulator. However, the circuit has an accurate baseline and performs better at low frequencies than do standard delta modulators.

This type of modulator is the basic circuit of a dc isolation amplifier. The serial data and the clock signal are transformer coupled from the input modulator to the output demodulator. Because the transformer isolates the input and output grounds, the circuit can withstand as much as 2000V of common-mode voltage. The circuit has an accuracy of 0.1% or better. Even if the digital lines are long, the data retains its integrity through the isolation amplifier.

At low bandwidths of about 5 Hz, you can make the delta modulator's dynamic range high enough to handle six digits of data resolution in instrumentation systems. Audio signals are too fast for delta modulators to accommodate; you would have to sacrifice dynamic range to keep clock frequencies manageable. Also, you would need a 25-MHz clock to maintain an 8-bit dynamic range across the 20-kHz audio band.

The A/D converter in **Fig 6** illustrates one possible application of **Fig 1**'s delta-modulator circuit. The

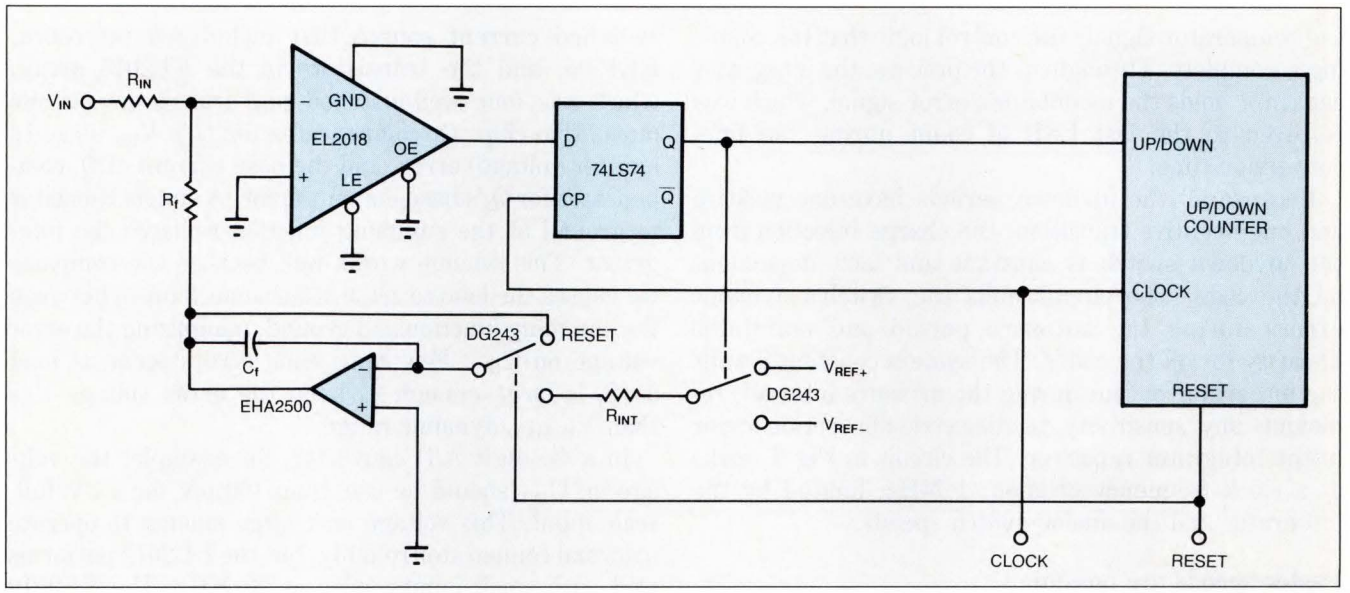

Fig 6—You can design an A/D converter *based on a delta-modulator circuit. The data in the counter, which accumulates each clock's serial data, is a valid estimate of the analog input at the instant it's read.*

modulator and the counter are reset for each new measurement. Assuming a positive voltage is present at V_{IN}, the modulator provides a series of ones, and the integrator output ramps negative, eventually balancing the comparator input. The comparator then provides a 50% duty-cycle stream of ones and zeros, and the integrator output dithers around a count equal to $-1V_{IN}(R_f/R_{IN})$. The counter accumulates each clock's serial data and also dithers around a final count. Eventually, the circuit reads the counter's data, and the converter is reset for the next conversion.

The data in the counter is a valid estimate of the analog input at the time the data is read. You don't need a sample-and-hold circuit to stabilize the analog input for conversion; the delta modulator and the counter track the analog input dynamically. The reset pulse sets both the integrator output and the counter to an initial zero-offset calibration.

Design a fast quantized-feedback converter

You can also use a delta-modulator circuit to perform the quantized-feedback method of A/D conversion (**Ref 1**), which is used in some DVM chips. **Fig 7** shows the analog section of a fast quantized-feedback converter. The converter has two periods: autozero and measure. During the autozero cycle, the control logic switches the input to ground, closes the measure/zero switch, and cycles the up/down switch four clock cycles up and four clock cycles down. The 50% duty cycle sets I_{REF} equal to $V_{REF}/2R_f$. The feedback through the measure/zero switch causes the voltage follower's output to provide a current, $-I_{REF}$. This action sets up a voltage on C_{AZ} to emulate a V_{REF-} and null the integrator-offset voltage.

During the measure cycle, the input is connected to V_{IN}, the measure/zero switch is open (to sample and hold the $-I_{REF}$ reference level), and the up/down waveshape in either **Fig 7b** or **Fig 7c** is applied, depending on the comparator output at the beginning of the up/down period. The counter accumulates either a count of $+6$ or -6 for each sequence of eight clock cycles in the up/down period. Seven clock cycles up and one clock cycle down cause the up/down switch to add an average current of $7I_{REF}/4$ to the integrator input. At the same time, the stored C_{AZ} voltage sets up a $-I_{REF}$ current; a total current of $3I_{REF}/4$ goes to the integrator for each up/down cycle. The sequence of one clock cycle up and seven clock cycles down adds an average of $I_{REF}/4$ to the integrator input; the $-I_{REF}$ autozero current going to the integrator equals $-3I_{REF}/4$.

The control logic establishes up/down cycles that are worth $+6$ or -6 digital counts and are followed by a final fine conversion. When the input is connected to ground, the integrator is driven 12 counts positive by two logic-one sequences of the up/down switch. The up/down switch is then connected to ground while the data counter decrements each clock cycle. When the integrator output is driven through ground potential,

Although many possible bit patterns can represent the analog input in a delta modulator, the modulator usually chooses its own pattern.

the comparator signals the control logic that the counting is complete. Throughout the process, the integrator capacitor holds the modulator's error signal, which was resolved to the last LSB of count during the fine-conversion time.

Because all the up/down periods have one positive and one negative transition, the charge injection from the up/down switch is constant and isn't dependent on the code. The circuit nulls the switch's dynamic errors during the autozero period and maintains linearity for all the codes. The system constantly nulls the integrator output during the measure interval, removing any sensitivity to dielectric-absorption error in the integrator capacitor. The circuit in **Fig 7** works at a clock frequency of about 1 MHz, limited by the integrator and the analog-switch speeds.

Faster speeds are possible

The quantized-feedback converter in **Fig 8** works at clock speeds of about 20 MHz. To configure this circuit, replace the up/down switch in **Fig 7** with a switched current source that includes a reference, REF-05, and the transistors in the EL2015 array, which has four well-matched pnp transistors on one monolithic chip. Q_1 compensates for Q_2's V_{BE} (base to emitter voltage) error, and the base current of Q_4 compensates for Q_2's base-current error. A simple capacitor to ground at the summing junction replaces the integrator. This scheme works well because the comparator causes the loop to act as a servomechanism between the summing junction and ground, minimizing the error voltage on C_{INT}. Few conversion errors occur as long as C_f is large enough to keep the error voltage less than $V_{IN(MAX)}$/dynamic range.

In a 4½-digit A/D converter, for example, the voltage on C_{INT} should be less than 100 μV for a 2V full-scale input. This voltage isn't large enough to operate a normal comparator reliably, but the EL2019 performs well with small inputs, even at 20 MHz. The EL2019 has an internal D-type flip-flop that prevents the amplified comparator input from escaping the EL2019 package and causing feedback. Because the EL2019 has a

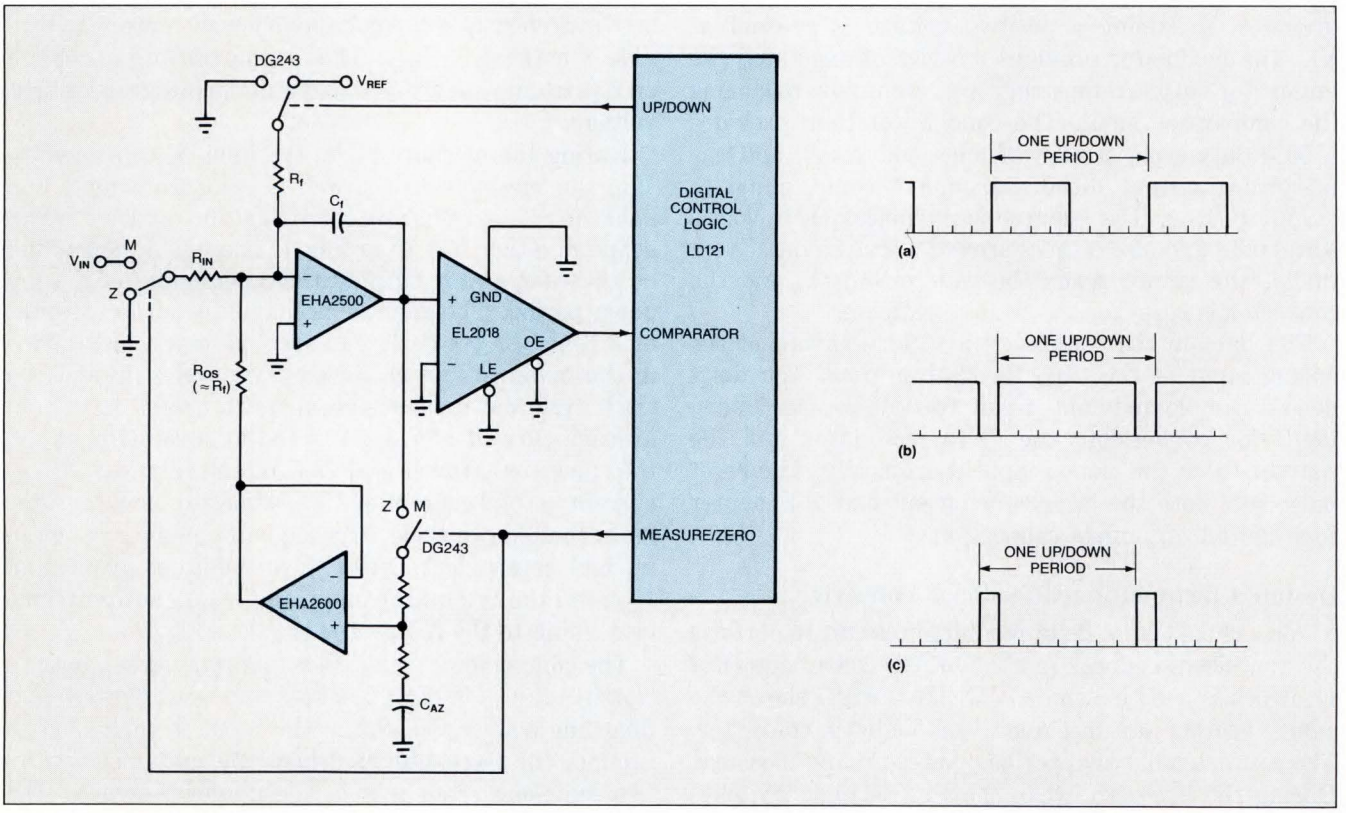

Fig 7—The quantized-feedback method *of A/D conversion, which is used in some DVM circuits, has two periods: autozero and measure. The up/down waveform in* ***(a)*** *occurs during the autozero cycle, the waveform in* ***(b)*** *occurs during a 1-sequence measuring cycle, and the waveform in* ***(c)*** *is present during a 0-sequence measuring cycle.*

10-nsec setup time and a 3-nsec typical hold time, the clock doesn't interfere with the analog conversion. The EL2019's analog input is quantized when the clock edge occurs.

To effect the autozero function, the circuit employs the typical switch timing, except that the EHA2600 autozero buffer is an integrator whose input is the comparator's output. This arrangement ensures low drift in the autozero feedback during conversions, keeping conversion offsets low. The EHA2600 has a good bandwidth and a bias current of only tens of nanoamperes. Alternatively, you could also use an LM356. With resistor values of 2k and 15k, the comparator approximately clocks a 50% duty cycle and closes the autozero loop, thereby nulling the summing-junction voltage.

When the clock is running at 20 MHz, the circuit can perform as many as 400 conversions/sec at a 4½-digit resolution. Compared with a dual-slope converter, the analog circuitry is simpler and less critical, but its digital sequencing is more involved. Considering the availability of economical gate arrays, though, the circuit in **Fig 8** is the better alternative.

Perform V/F conversions, too

You can also use delta modulators as V/F converters, such as the one shown in **Fig 9.** In this circuit, the charge pump replaces the analog-feedback switch. In the standard-feedback method, the circuit integrates a current for a clock-controlled time; that is, a fixed charge is metered into the integrator. In **Fig 9**, the output of a CMOS NAND gate places a voltage across

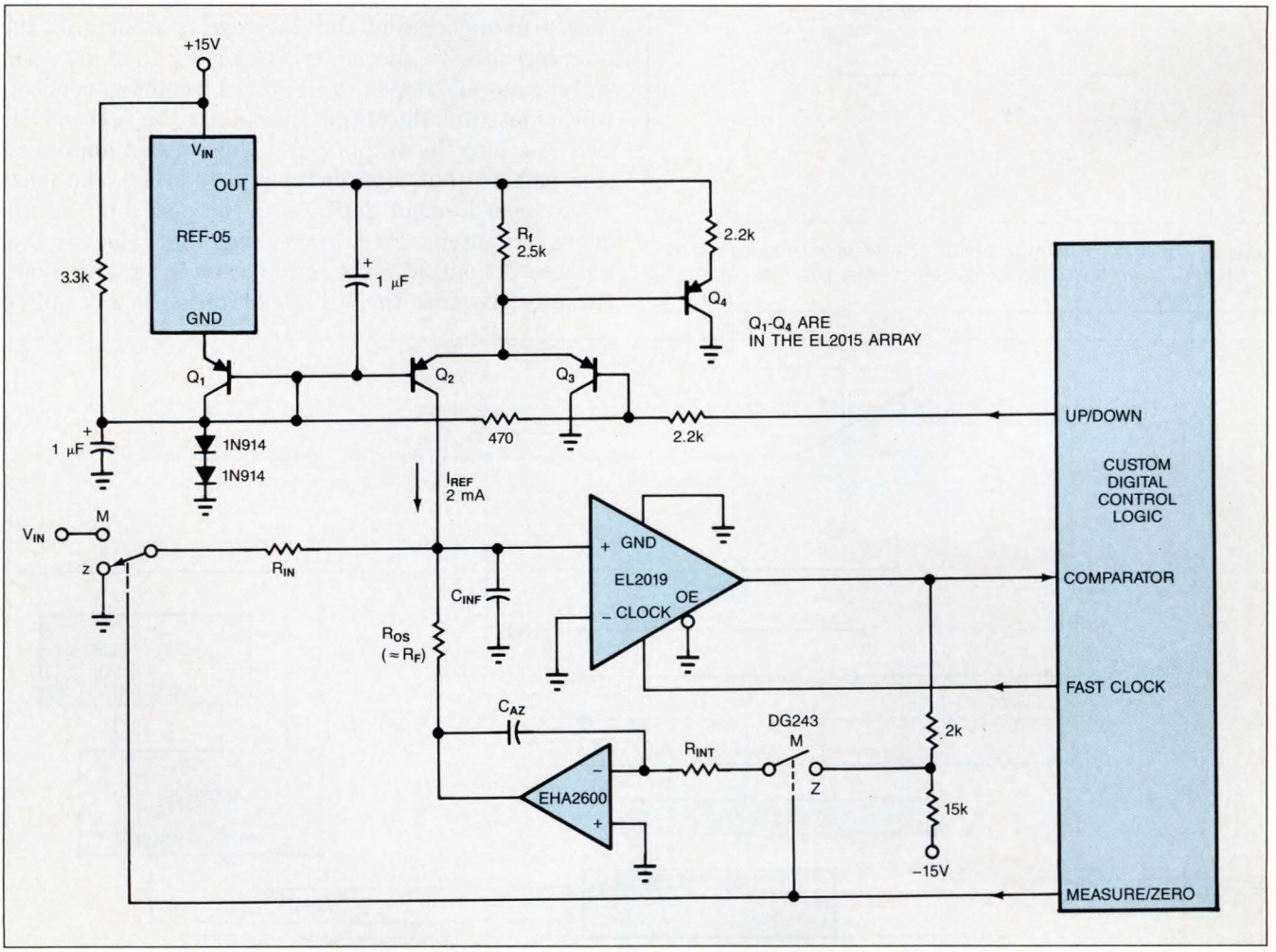

Fig 8—You can design a quantized-feedback A/D converter *that operates at clock frequencies to 20 MHz. To do so, replace the up/down switch in* **Fig 7***'s circuit with a switched current-source composed of REF-05 and the four transistors in the EL2015 array.*

The dynamic range of a delta modulator is high enough to handle six digits of data resolution at low bandwidths.

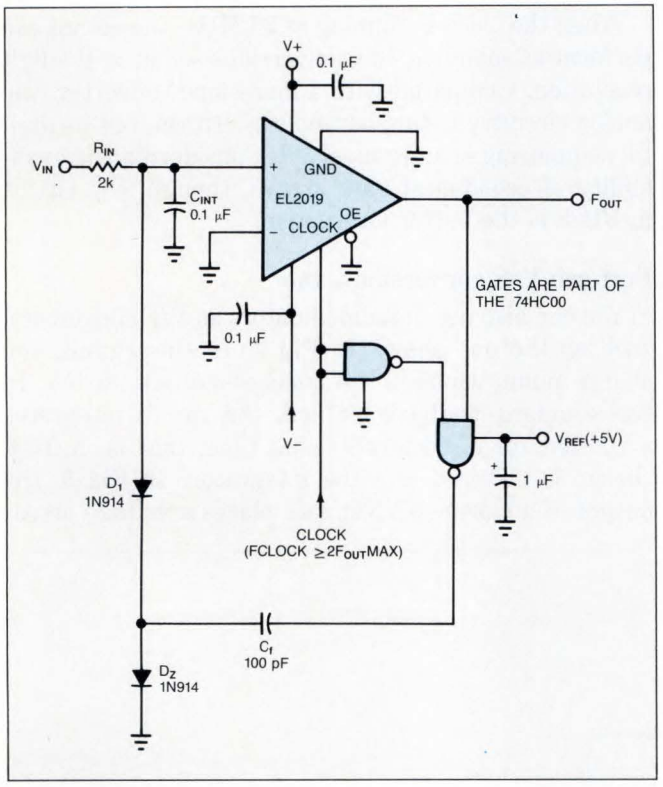

Fig 9—By using a charge pump *instead of an analog-feedback switch in an average-output delta modulator, you can construct a V/F converter.*

C_f for each clock-low cycle. If the analog input rises, the EL2019 provides a high signal after the next positive clock edge. The NAND gate then provides a low signal during the next clock-high level. This negative edge couples through C_f and D_1 to send a charge approximately equal to $V_{CC}C_f$ into the modulator's summing junction. If the negative charge from C_f can sufficiently drive the summing junction below ground, the EL2019 provides a zero during the next positive clock edge, and no charge injection occurs at the next clock cycle. If the charge can't sufficiently null the junction, the comparator provides another high in the next clock period, and the charge pump begins to operate again.

According to this procedure, the V/F converter generates several half-clock pulses per second that are proportional to the input analog voltage. The output frequency, F_{OUT}, is insensitive to both the reference clock's frequency and the duty cycle, as long as the reference clock's frequency is greater than the converter's output frequency. A simple frequency counter, which measures the output, completes the A/D conversion. Because the output-pulse train has an unpredictable pattern (but a predictable duty cycle), the noise of the measurement depends on the period of the frequency counter's gate. Increasing the value of C_{INT} reduces the output noise of the counter measurement. However, because the V/F converter's noise is shifted

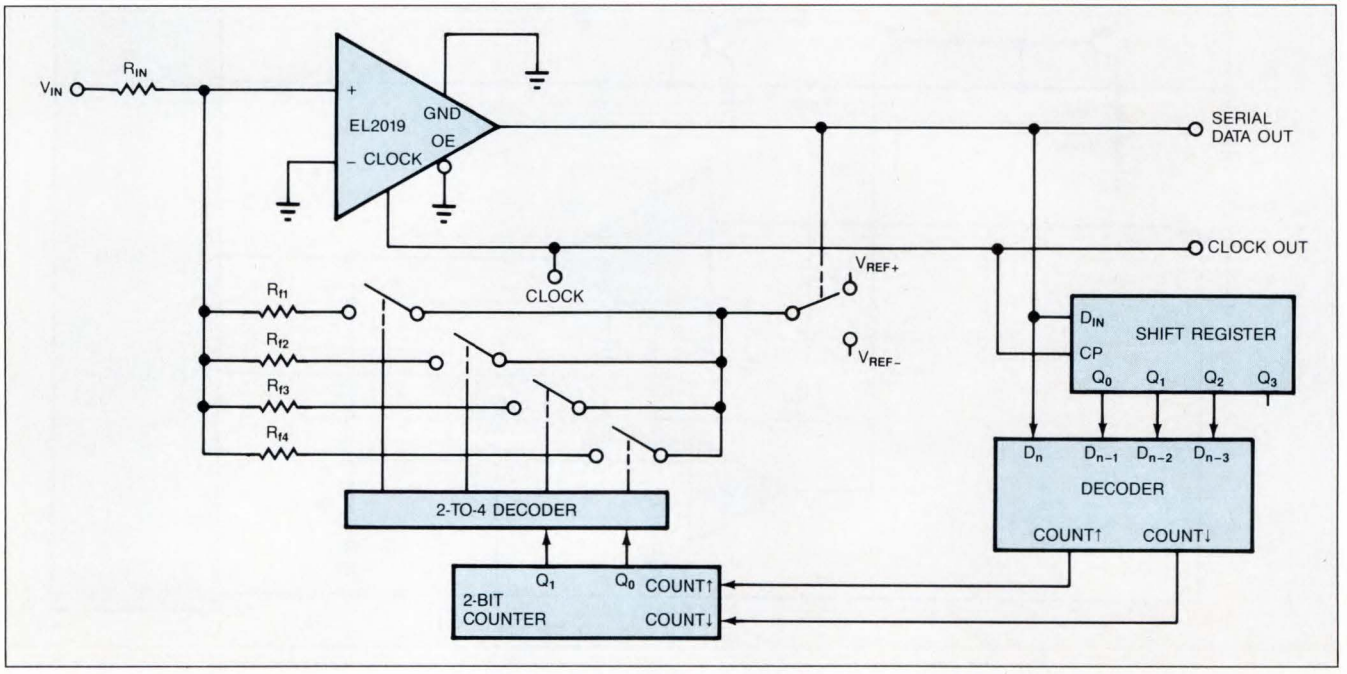

Fig 10—Based on an average-output modulator, *this circuit uses companding feedback to expand the dynamic range.*

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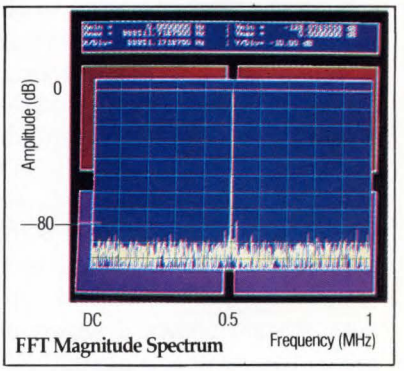
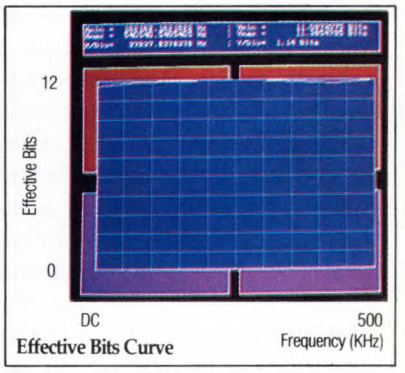


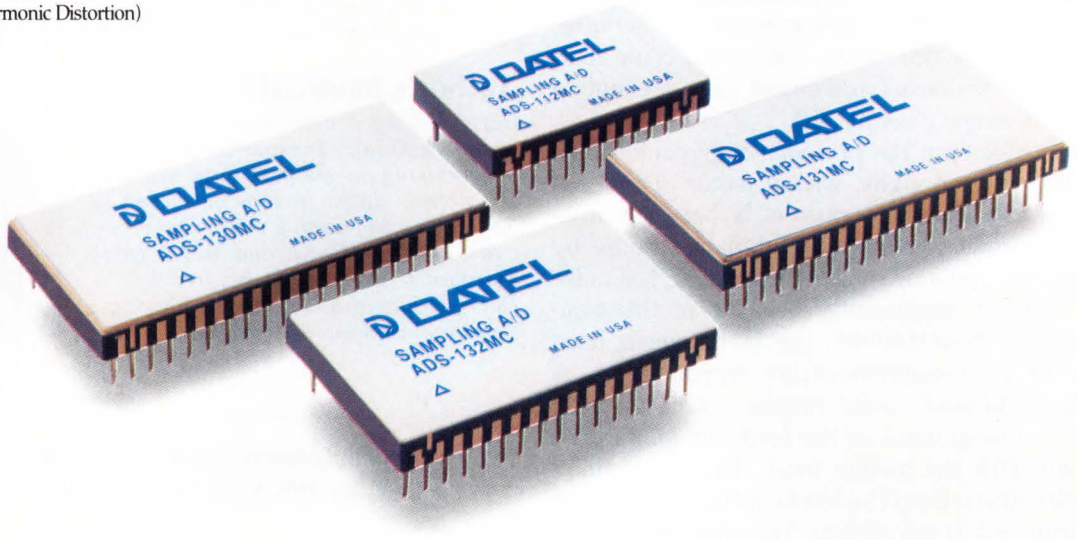
FFT Magnitude Spectrum



Effective Bits Curve

Model	Sampling Rate	Effective Bits at Nyquist Frequency	THD* at Nyquist Frequency	Power Dissipation	Package	Price (1-9)
ADS-112	1MHz	11.0	-73 dB	1.3 watts	24-pin DDIP	$259
ADS-132	2MHz	11.0	-73 dB	2.9 watts	32-pin TDIP	$346
ADS-131	5MHz	10.6	-69 dB	4.2 watts	40-pin TDIP	$549
ADS-130	10MHz	10.6	-69 dB	4.5 watts	40-pin TDIP	$775

* THD (Total Harmonic Distortion)



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In addition to its use in A/D conversion, the delta modulator is also useful in V/F conversion.

to a lower frequency, the counter needs a wider gate period.

As you have seen in previous examples, you can change the characteristics of the feedback path to improve the modulator's performance. In delta-modulator telephone applications, for example, you can alleviate the tradeoff between slew rate and dynamic range by making the feedback magnitude vary with the analog amplitude. The algorithm is as follows: If four or more ones or if four or more zeros occur in a row in the data stream, the input slew rate is too large for the feedback magnitude. The feedback is then, for example, increased by a factor of two. On the other hand, if the data stream shows a series of alternating ones and zeros, the feedback magnitude is too large to resolve the input; the feedback is reduced by a factor of two. Analog inputs have a companding range of feedback levels to null to, and the signal-to-noise ratio is fairly constant over large input ranges.

Fig 10 is a partial schematic of a compandor, which uses the general arrangement of **Fig 4**'s average-output modulator. **Fig 10** includes four R_fs; three of them are half the value of their respective predecessors. The 2-bit counter selects one of these resistors through the 2-to-4 decoder. The circuit compares the EL2019's output and the last three shifted outputs to obtain the 1111, 0000, 1010, and 0101 codes. The decoder's outputs cause the 2-bit counter to increase, decrease, or remain the same. The 2-bit counter is designed so that it doesn't increment past a count of 3 or decrement below a count of 0.

The presence of four R_fs provides a dynamic-range enhancement factor of eight, with a factor of two between each R_f. To provide a ratio of N between adjacent R_fs, the circuit enhances the dynamic range by N^3. Although the dynamic range is expanded, the noise floor isn't reduced significantly because of the companding process. Nevertheless, the technique is used extensively in voice-communication transmission. A companding modulator's noise remains constant with respect to the analog input as the feedback loop cycles up and down with the analog level. Thus, you don't need AGC circuits to keep the levels optimally constant when performing A/D conversion. The noise and distortions aren't equal to the requirements of audiophile equipment, but simple circuits can reliably transmit variable-level audio signals suitable for telephony.

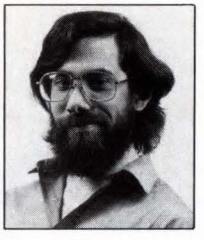
The companding demodulator simply places **Fig 10**'s variable feedback elements into **Fig 5**'s demodulator. To recover a digital word, you must replace the simple counter with a parallel adder and an accumulation register. The 2-to-4 decoder in **Fig 10** shifts a one or a negative one a few bits and adds them to the accumulation register during each clock cycle. The adder must also prevent its output from overflowing, thereby effecting a limiting action on the data extremes.

The recovered code is useful in digital-oversampling filters. It's updated at fast clock rates and requires relatively simple analog filters to limit the input slew rate. You can then process the recovered data with Z-transform filters in the digital domain to eliminate the data components above the Nyquist frequency of subsequent transmission rates. For example, a telephony system transmits audio data at an 8-kHz update rate. The companding delta modulator may be operating at a 3-MHz rate. The digital filter can be operating at a 200-kHz calculation rate with little phase aberration near the 8-kHz audio maximum. The digital filter is thus oversampling with respect to the system transmission rate and easily performs the Nyquist filtering. EDN

References

1. *Siliconix Switches and Integrated Circuits Data Book*, LD110/LD111 and LD120/LD121 data sheets and application notes, Siliconix, Santa Clara, CA.

Author's biography



Barry Harvey is a senior design engineer with Elantec Inc and has been with the company for the past three years. His present duties include designing and evaluating analog integrated circuits. He has a BSEE and MSEE from Stanford University. In his free time, Barry enjoys running, guitar playing, and programming his computer in C.

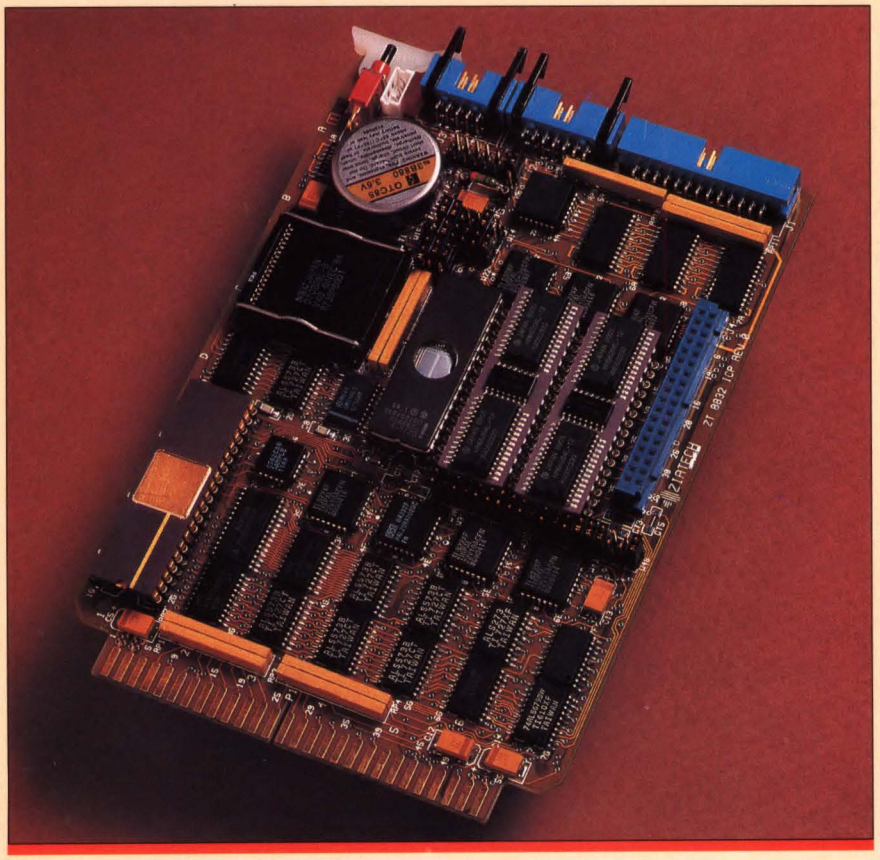
Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490

ZIATECH CORPORATION

CONTROL POINT

Test and Control Product News from Ziatech Corporation Summer, 1989

STD MULTIPROCESSING BOOSTS PERFORMANCE



Ziatech's new ZT 8832 I/O Control Processor

New Ziatech Multiprocessor Advances STD Bus Control System Capabilities

Ziatech's new STD Bus single board multiprocessing computer and DOS Multiprocessing Extension (DOS MPX) software bring more performance, control, modularity and development flexibility to control applications.

MORE PERFORMANCE

Multiprocessing brings more performance to demanding STD applications by partitioning control systems functions into smaller functions assigned to individual multiprocessors.

Ziatech's new multiprocessor features a large complement of on-board I/O and communicates

(Continued on page 3)

New Single Board PLC Takes the Shape of STD Bus

Ziatech now offers the functionality of a programmable logic controller (PLC) in the compact and cost-effective STD Bus format.

NEW PRODUCT

The company's new Single Board PLC is equipped with 86-LADDER, a high performance ladder logic program from Wizdom Systems. This Allen–Bradley PLC-compatible

(Continued on page 2)

INSIDE

ZIATECH CORPORATION

New Single Board PLC is Fast and Flexible Controller

(Continued from page 1)

program enables the Ziatech Single Board PLC to run faster than conventional PLCs while providing on-line programming, editing, execution and documentation.

LOW COST ALTERNATIVE

This Single Board PLC provides a low-cost alternative to PLCs because it utilizes Ziatech's rugged, low cost STD Bus industrial computers, which are equipped with IBM PC DOS and can run software like 86-LADDER.

SEVERAL COMPUTER CONFIGURATIONS

This industrial computer is available in several configurations, depending upon the control application's requirements.

The Single Board PLC can be purchased in a small STD card cage for embedded applications, or in a panel-mount, a rack-mount or a NEMA 4/12-compatible enclosure.

For more information, check the SBC PLC/86-LADDER box on the return card.

LADDER LOGIC SOFTWARE PROVIDES ALTERNATIVE TO PLCS

Ziatech Corporation has joined forces with Wizdom Systems, the maker of the popular 86-LADDER software package to give control system integrators an exciting alternative to programmable logic controllers (PLCs).

ALLEN-BRADLEY COMPATIBLE

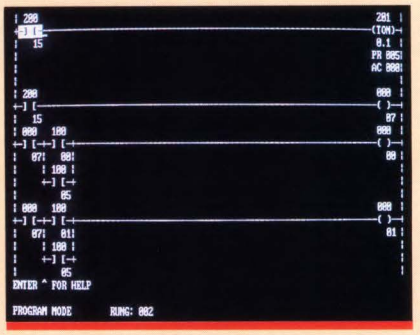
86-LADDER is a family of stand-alone software packages that operates like an Allen-Bradley PLC. The software provides on-line programming ability for Ziatech's STD Bus industrial computers.

FAMILIAR TO WORK FORCE

86-LADDER is intended for control applications where ladder logic is already understood by the work force. This allows use of existing programs and enables trained personnel to quickly develop, test and document factory control systems.

COST REDUCTION

Through its use of the industry standard STD Bus, 86-LADDER can provide a significant cost reduction when compared to a PLC. At the same time, this ladder logic program offers more flexibilty and better performance than its PLC counterparts. The universal compatibility and modularity of the STD Bus platform make this approach especially attractive.



Ladder logic software displayed on the screen of a Ziatech industrial computer.

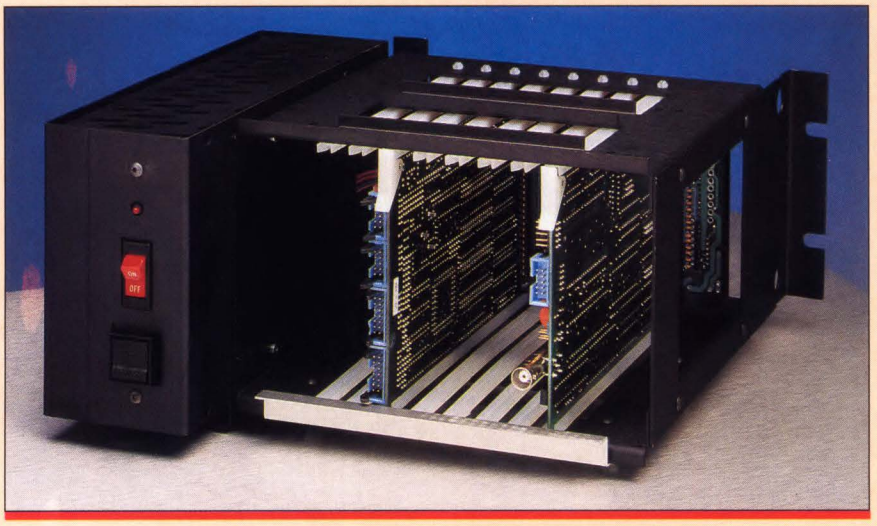
RUNS ON ZIATECH COMPUTERS

The software environment does not require a special PLC programming terminal. It will use any DOS-based computer such as a PC or Ziatech's ZT 1000 Industrial Workstation as the programming and execution device. 86-LADDER supports standard industrial I/O like Opto 22, Digitronics, etc., so a user isn't locked into specific hardware.

ON-LINE DOCUMENTATION

86-LADDER uniquely accepts on-line written comments within the programming environment and produces a "hard copy" printout, keeping the documented version consistent with the actual version running.

For more information, check the SBC PLC/86-LADDER box on the return card.



Ziatech's ZT 200 Embedded Computer emulates a programmable logic controller when running 86-LADDER.

NEW MULTIPROCESSOR FEATURES DOS MPX SOFTWARE FOR FAST DEVELOPMENT, USER INTERFACE

(Continued from page 1)

with the STD system's master processor through shared memory. This technique maximizes the performance of I/O-intensive applications because the master processor delegates tasks through memory and doesn't have to compete with other processors for STD backplane access.

COMPACT STD FORMAT

The new ZT 8832 I/O Control Processor's (ICP) surface mount design features a V40 processor, 800K on-board memory capacity, a math coprocessor option, an SBX expansion socket, three parallel ports, and two serial ports on the compact STD Bus format.

MORE CONTROL

The use of multiprocessors can be an attractive alternative to multitasking, because instead of relying on complex and expensive software to interleave task execution, the system integrator can dedicate specific ICPs to specific tasks that are literally running simultaneously.

MORE MODULARITY

Ziatech multiprocessing provides a simple approach to upgrading or expanding control system performance. Instead of redesigning an entire application to use a faster processor, ZT 8832 ICPs can be added to provide the performance boost required.

MORE DEVELOPMENT FLEXIBILITY

The development of an ICP-based multiprocessing system is simplified by Ziatech's new DOS Multiprocessing Extension (DOS MPX) software, which supports multiple ICPs as DOS devices. The software package includes a ROM for booting the ICP, an installable device driver for the system's master processor and a loader utility. Another significant component of DOS MPX is the Virtual Processor Console (VPC), which provides a user and runtime interface to the ICPs in a multiprocessing system.

DEVELOP IN HIGH LEVEL LANGUAGE

DOS MPX allows programmers to develop applications in a high level language (C is recommended), download them to the ICP and debug them with PC DOS development software. Because DOS MPX is a DOS extension, the ICPs run as if they are in a DOS system.

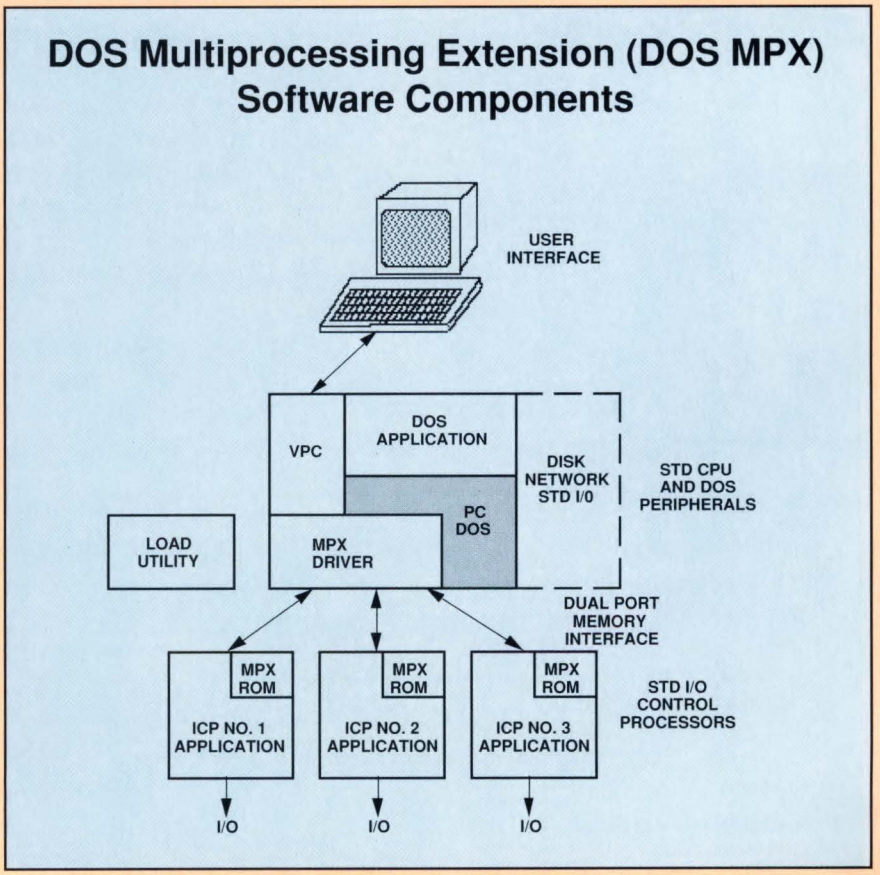
DOS MPX USER INTERFACE

Virtual Processor Console (VPC) allows the system user to toggle via a "hot key" to individual ICP screens for the purpose of viewing application and diagnostic output, and to input data. Soon, VPC will also contain a screen that displays the status of all ICPs in the system.

APPLICATION NOTE

An application note describing the advantages of multiprocessing is available from Ziatech, as well as data sheets on the ZT 8832 ICP and DOS MPX.

For more information, check the ZT8832 ICP box on the return card.



DOS MPX simplifies multiprocessing system development and provides a user interface to multiple processors.

NEW PRODUCTS SERVE REAL-TIME AND RUGGED APPLICATIONS

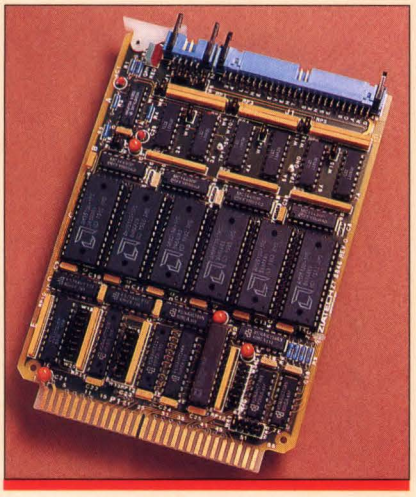
Ziatech continues to add to its line of STD Bus industrial computer products. A round up of recent product releases is featured below.

REAL-TIME EVENT SENSE INTERFACE

This unique STD interface provides high-speed digital I/O for real-time applications. It provides 24 event sense inputs for interfacing STD Bus computers to digital devices of all types.

The ZT 8846 can be programmed to generate interrupts when an event occurs, such as a tripped switch on a material handling conveyor. These interrupts provide an efficient means of signalling an STD Bus processor of real-time events without the burden of polling digital I/O points.

For more information, check the ZT 8846 box on the return card.



ZT 8846 Real-Time
Event Sense Interface

2400 BPS MODEM FOR STD BUS

The ZT 8843 provides full modem capability to STD Bus computers at data rates of 300, 1200, and 2400 bits per second (BPS). Automatic answer capabilities allow for unattended operation, while a speaker interface allows on- or off-board audible phone line monitoring.

This STD modem is compatible with the industry standard Hayes AT Command Set, providing access to a vast range of existing PC communications software.

For more information, check the ZT 8843 box on the return card.

QUAD SERIAL INTERFACE

The ZT 88CT41 provides four RS-232 serial channels to STD Bus systems with two of those channels configurable for RS-422/485. This STD interface features an optical isolation option for the RS- 422/485 channels and a FIFO option for all channels.

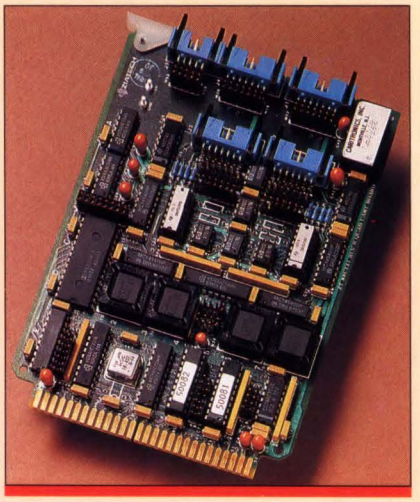
The ZT 88CT41 is a TTL backplane-compatible CMOS interface with low power consumption and an extended temperature operating range of -40° to +85° C for harsh environments.

For more information, check the ZT88CT41 box on the return card.

COMPACT COMPUTER

In addition to the ZT 88CT41 Quad Serial Interface described above, Ziatech also offers a single board computer and a byte-wide memory card that combine TTL-compatible CMOS for low power consumption with an extended temperature operating range (-40° to +85° C) for harsh environments.

The ZT 88CT08 Single Board Computer utilizes the 80C88 microprocessor and contains several IBM PC/XT peripherals and a 520K memory capacity on board.



ZT 88CT41
Quad Serial Interface

EXPANDED MEMORY

The ZT 88CT25 Expanded Memory System provides expanded memory capabilities to STD Bus systems as a PROM disk and/or battery-backed RAM disk, as main memory or as expanded main memory.

For more information, check the CMOS/Extended Temperature Products box on the return card.

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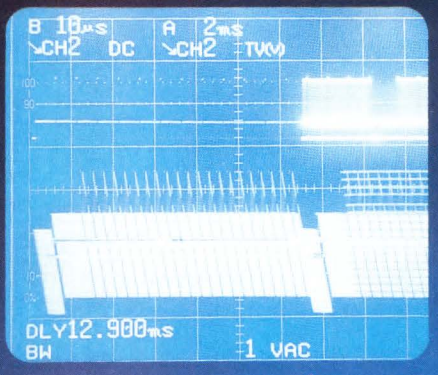

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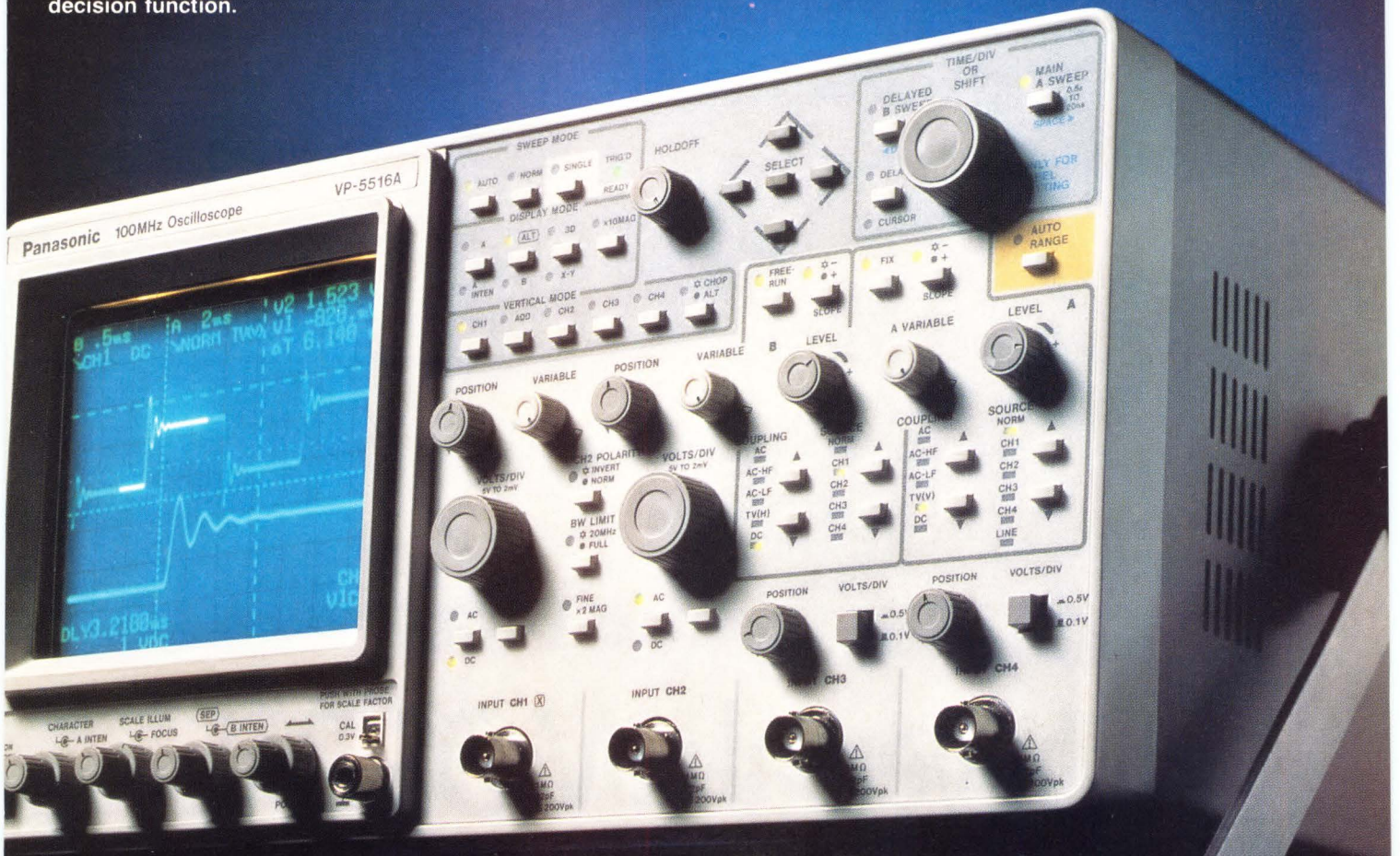

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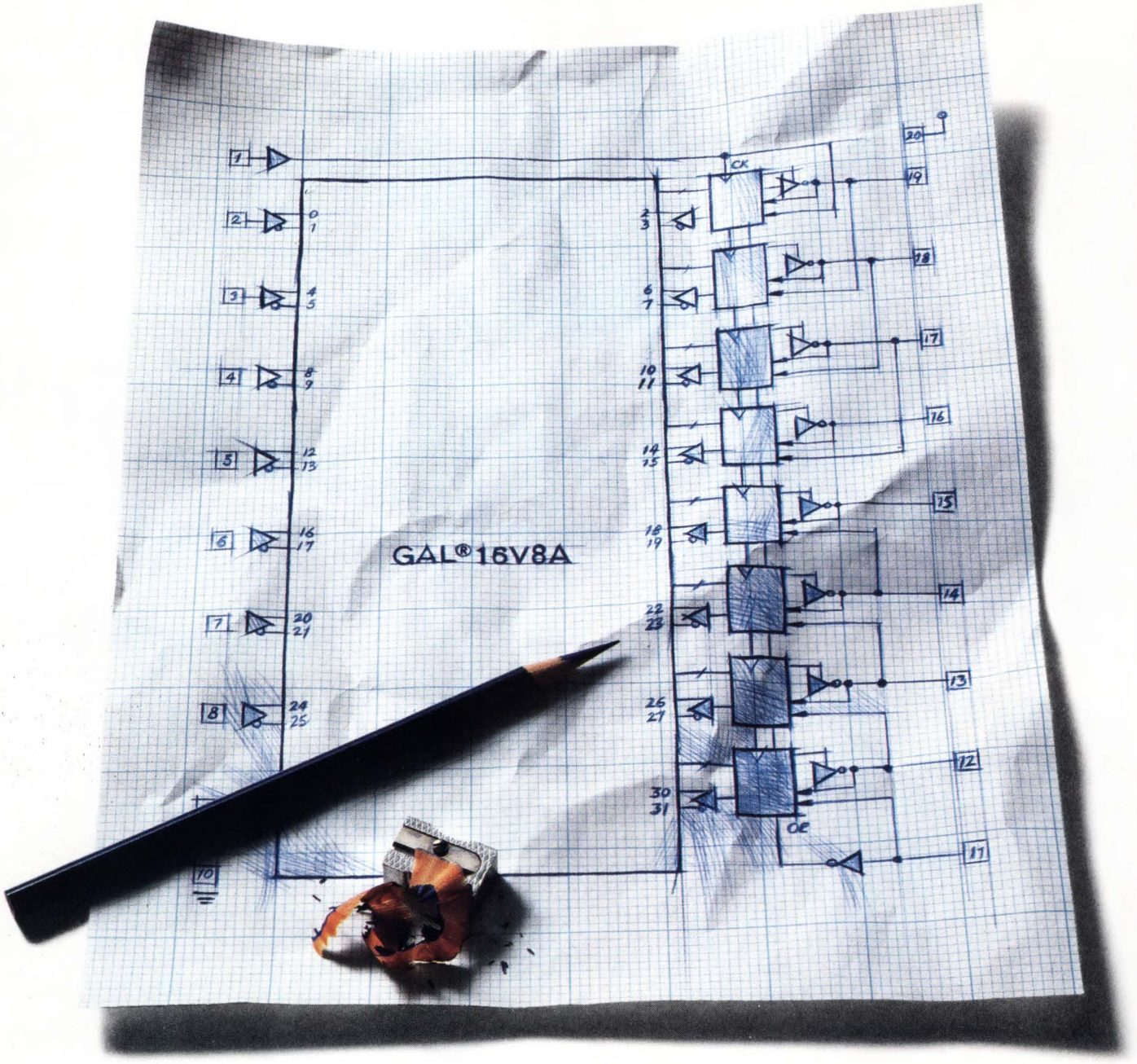

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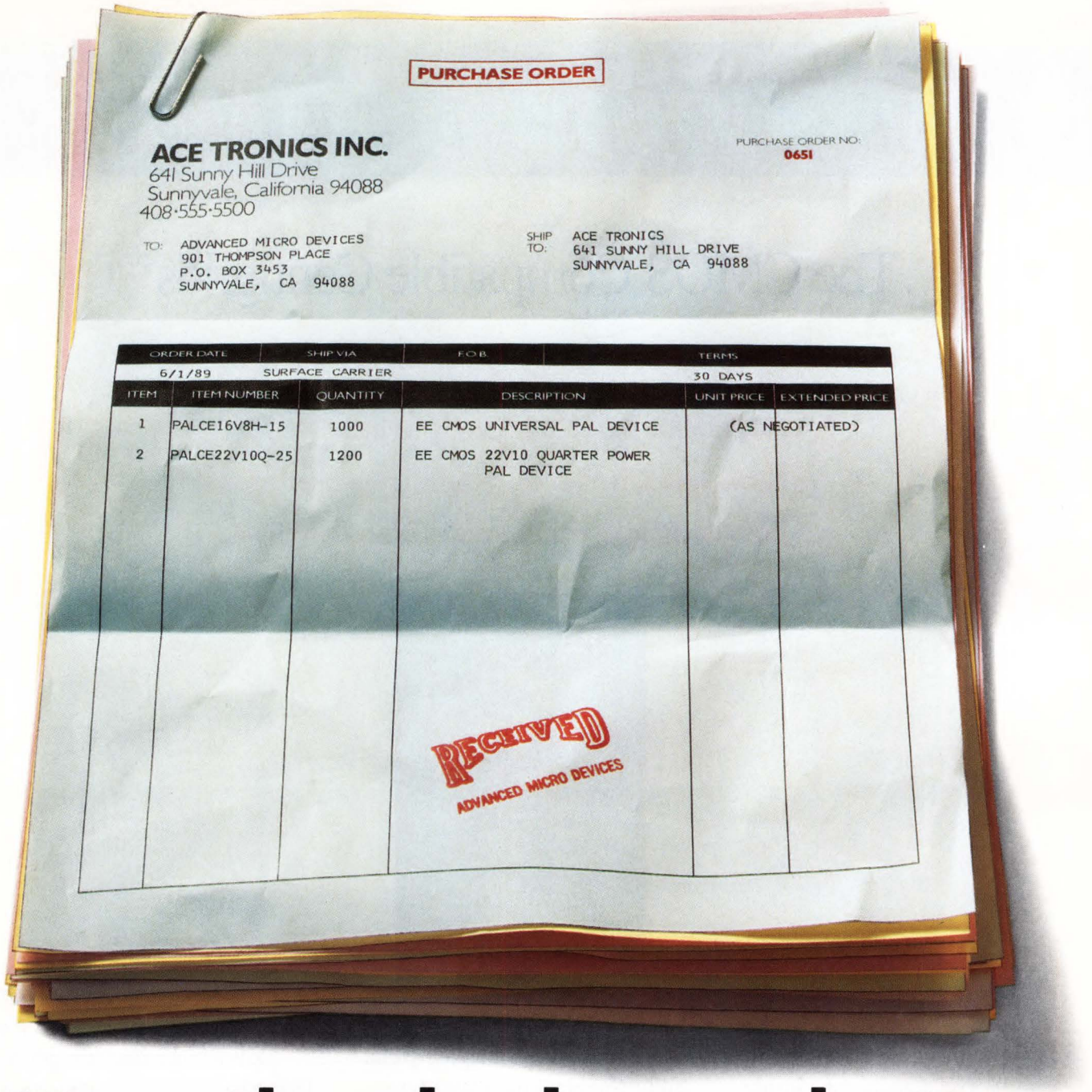

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Clamping circuits improve precision of bipolar limiters

Simple clamping circuits consist of back-to-back zener diodes, but their performance suffers from many limitations. Op-amp feedback improves the clamp response, and a DAC-based design gives you the greatest combination of precision and flexibility.

Jerald G Graeme, *Burr-Brown Corp*

Signal-clamping circuits prevent overloads, which can cause measurement delays and phase-reversal-induced servo latch-up. Simple zener-diode clamping circuits introduce errors and only let you choose from a limited number of clamping levels. By using op amps and DACs, you can overcome these limitations. Precision bipolar limiters incorporating these components provide continuous level control from 0 to ±40V. Clamping circuits that use op amps—though still zener-based designs—use feedback control to remove the zener restrictions. A DAC-based clamp lets you eliminate the zener diode entirely.

The simplest bipolar clamping circuit consists of two zener diodes connected back-to-back as shown in **Fig 1**. During operation, one diode is forward biased; the other operates in zener breakdown. The magnitude of the limit voltage, V_{OUT}, is $V_F + V_Z$, where these two voltages are the forward and zener voltage values. For almost all zener diodes, V_F is simply the 0.6V forward drop common to all silicon signal diodes. The forward- and reverse-biasing roles of D_1 and D_2 switch depending on the input signal's polarity. As a result, the circuit limits both positive and negative signals.

This basic zener approach is limited in precision and restricts the number of available clamp levels. The actual clamp response deviates from the ideal with rounded corners and limit levels that are not flat (**Fig 1b**). The rounding of the response results from the zener voltage-vs-current characteristic, which lacks the ideal square corner. In addition to these rounding effects, the limit-region characteristic exhibits a nonzero slope due to zener resistances that form voltage dividers with R_1. Further deviations from ideal performance result from the zener diodes' temperature coefficients. These coefficients are a function of the zener voltage and approach zero for 5.6V zeners. Unfortunately, your choice of a zener diode is based on the clamp level that you want to achieve and not on optimum temperature stability. If you choose a 5.6V zener for temperature stability, the clamp level is fixed at 6.2V. If you choose a different zener voltage, you still can't achieve clamp levels less than 1.5V.

All of these restrictions are removed by placing the zener diode in an op-amp feedback loop or by replacing the zeners with a DAC. You can manually or digitally direct op-amp feedback-controlled limiters. By using a DAC for control, you can achieve a high-resolution

Signal clamping prevents circuit overloads, which can cause measurement delays and servo latch-up.

design with total independence of signal gain and limit levels.

The op amp feedback control method shown in **Fig 2** forces the clamping circuit's response to follow its ideal characteristic more closely **(Fig 2b)**. A single zener diode enclosed in a diode bridge provides both positive and negative limit polarities for improved accuracy and speed; the loop gain counteracts the zener's rounding and resistance effects. This circuit also provides you with an unrestricted clamp-level selection set: You can achieve clamping levels at any multiple or fraction of the actual zener voltage over an unlimited range.

From the transfer characteristic, you can identify three basic areas of circuit operation: the linear range, the transition state, and the clamp state. To highlight how the circuit in **Fig 2** works, it is useful to identify the active components that correspond to these three areas of operation **(Fig 3)**. To ease this description of circuit-state switching, inactive bridge components and the phase-compensation elements, R_4 and C_1, have been deleted. For the moment, consider the amplifier offsets shown in **Fig 3**, V_{OS1} and V_{OS2}, to be zero.

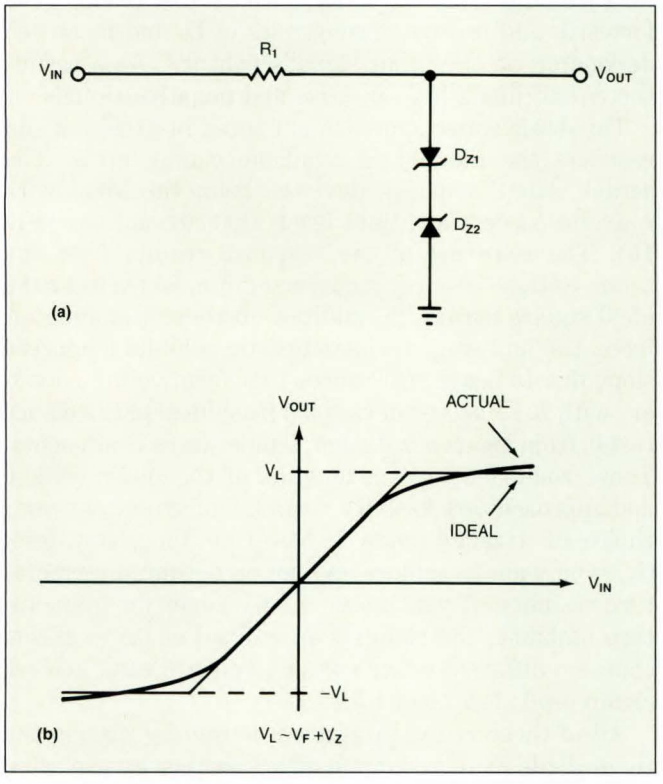

***Fig 1—Back-to-back zener diodes** implement the simplest form of clamping **(a)**. Unfortunately, the circuit response **(b)** includes significant rounding errors and a nonzero slope in the limit states.*

While the input signal is within the $\pm V_L$ clamp levels—that is, within the linear range—the signal is affected only by the feedback loop encompassing the two amplifiers, IC_{1A} and IC_{1B} **(Fig 3a)**. All the bridge elements, including the zener diode, are off; only the voltage divider comprising R_1 and R_V is active between the output of IC_{1A} and the noninverting input of IC_{1B}. This divider attenuates the IC_{1A} output with little effect in this linear range because of the counteracting gain of the 2-amplifier loop. The loop drives the attenuated IC_{1A} output signal in order to make the IC_{1B} inverting input follow V_{IN}. Only then will the voltage between the inputs of IC_{1A} be equal to zero. In this range, the circuit behaves as a simple voltage amplifier. The output is determined by the following equation:

$$V_{OUT}=(1+R_3/R_2)V_{IN},$$

for $-V_L<V_{OUT}<V_L$. The actual circuit response will include the input errors of IC_{1A} but not those of IC_{1B}. Since IC_{1B} is enclosed in the common feedback loop, its input errors are attenuated by the loop gain of IC_{1A}.

The circuit enters the transition state when the input amplitude approaches a clamp level and the zener diode begins to turn on **(Fig 3b)**. Under these conditions, the voltage across the bridge approaches $\pm(V_Z+2V_F)$. The zener resistance begins to drop from its very high, off-state value to some smaller value. This zener resistance, R_Z, loads the voltage divider formed by R_1 and R_V and changes the divider ratio. As the zener turns on further, R_Z continues to drop, thus increasing its loading effect. This varying zener resistance causes the rounded transition response of **Fig 1**, but in this case the loading error is sensed through the feedback connection to IC_{1A}. The feedback forces the inverting inputs of IC_{1A} and IC_{1B} to follow V_{IN}. That is, the loop gain drives the output of IC_{1A} higher, thus increasing the voltage-divider signal to compensate for R_Z's loading effect. This feedback correction enables the circuit to retain a linear response until IC_{1A} reaches its saturation limit.

At this limit, a sharp transition occurs, which transfers circuit control from the input signal to the bridge-connected zener: The amplifier loop is now broken. The gain of IC_{1A} drops dramatically because of internal saturation, and the amplifier's output voltage holds at a level independent of the input signal. This output saturation effectively clamps the voltage presented to R_1 and transforms the circuit to that shown in **Fig 3c**.

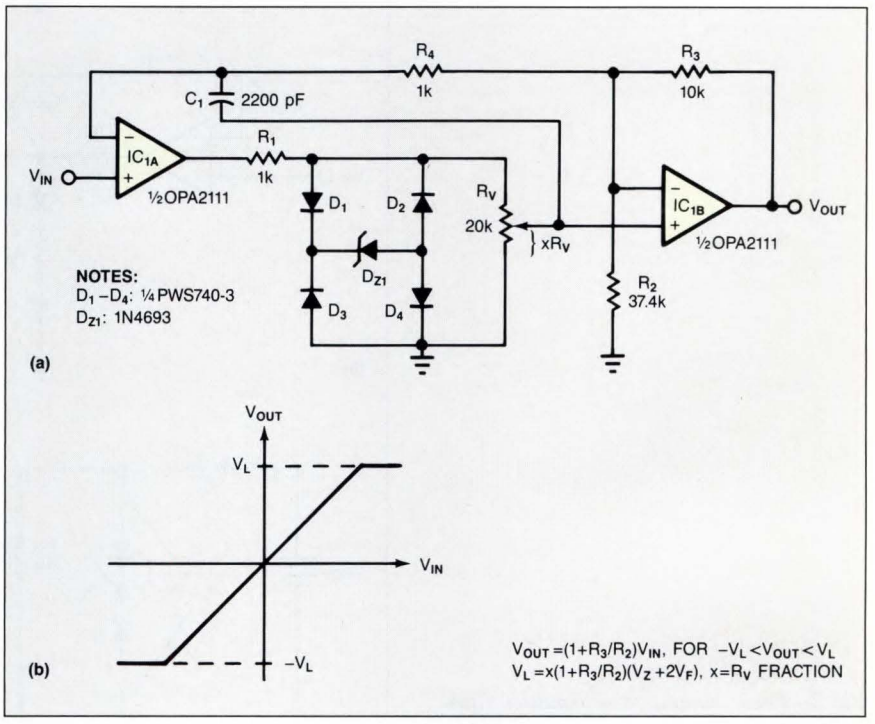

***Fig 2—You can minimize rounding errors** by using this single-zener-diode bridge approach **(a)**. The loop gain counteracts the turn-on-resistance effects of the zener to produce a more ideal clamp response **(b)**.*

In this circuit, the fixed voltage, V_{SAT1}, supplies constant current to the zener diode, even with further increases in V_{IN}. With a supply of constant current, the voltage drops across the zener diode, and diodes D_1 and D_4 remain fixed. The voltage across R_V clamps at a stable voltage equal to V_Z+2V_F. The circuit shown in **Fig 3c** corresponds to positive clamping. The circuit that corresponds to negative clamping is identical to **Fig 3c,** except that the zener is connected through D_2 and D_3. The polarity of the voltage V_Z+2V_F is reversed, but its magnitude stays the same.

The R_V divider attenuates and transfers bridge voltages resulting in positive or negative limit states to IC_{1B}. You can replace this adjustable voltage divider with resistors in fixed-level applications. In either case, with a divider fraction of x, the voltage transferred to the IC_{1B} input is $\pm x(V_Z+2V_F)$. The limit voltages are scaled further by the gain of IC_{1B}; the final output voltage is equal to $\pm x(1+R_3/R_2)(V_Z+2V_F)$.

Note that neither R_V nor R_1 appears in the above equation for V_L. Since R_V serves as a voltage divider, its absolute value drops out in the divider ratio and only the divider fraction x remains. Thus, the temperature coefficient of R_V is not a factor in the clamp stability. R_1 only affects V_L by the amount of clamp-state current it supplies to the zener diode. The effect of this constant current is reflected in the actual zener voltage developed as V_Z.

The absence of R_V and R_1 in the expression for V_L is the primary reason **Fig 2** improves upon the limited voltage levels and unoptimized temperature stability of simple zener clamping. First, the potentiometer fraction, x, and the gain factor, $1+R_3/R_2$, let you access limit levels at any fraction or multiple of the bridge voltage. By adjusting both x and the gain simultaneously, you can select clamp levels from almost zero to $\pm(1+R_3/R_2)(V_Z+2V_F)$. Clamp levels as low as 5 mV are practical—an advantage when compared with the 1.5V lower limit of basic zener clamping. To accurately access the very small clamp levels, you must modify the circuit of **Fig 2** to include a precision potentiometer or a trimmed resistor-divider substitute and trim the op-amp offsets.

As previously mentioned, the thermal stability of the diode-bridge design is much greater than that of simple zener clamping. You can now choose the zener diode based on temperature stability requirements and leave the clamp voltage requirements to the circuit controls. The 1N4693 zener diode used in **Fig 2** develops a temperature coefficient of zero for the bridge voltage of V_Z+2V_F. Both V_Z and V_F will drift with temperature; for a 7.5V zener diode, their magnitudes cancel to within 40 ppm/°C.

Using a 7.5V zener diode causes the bridge to clamp

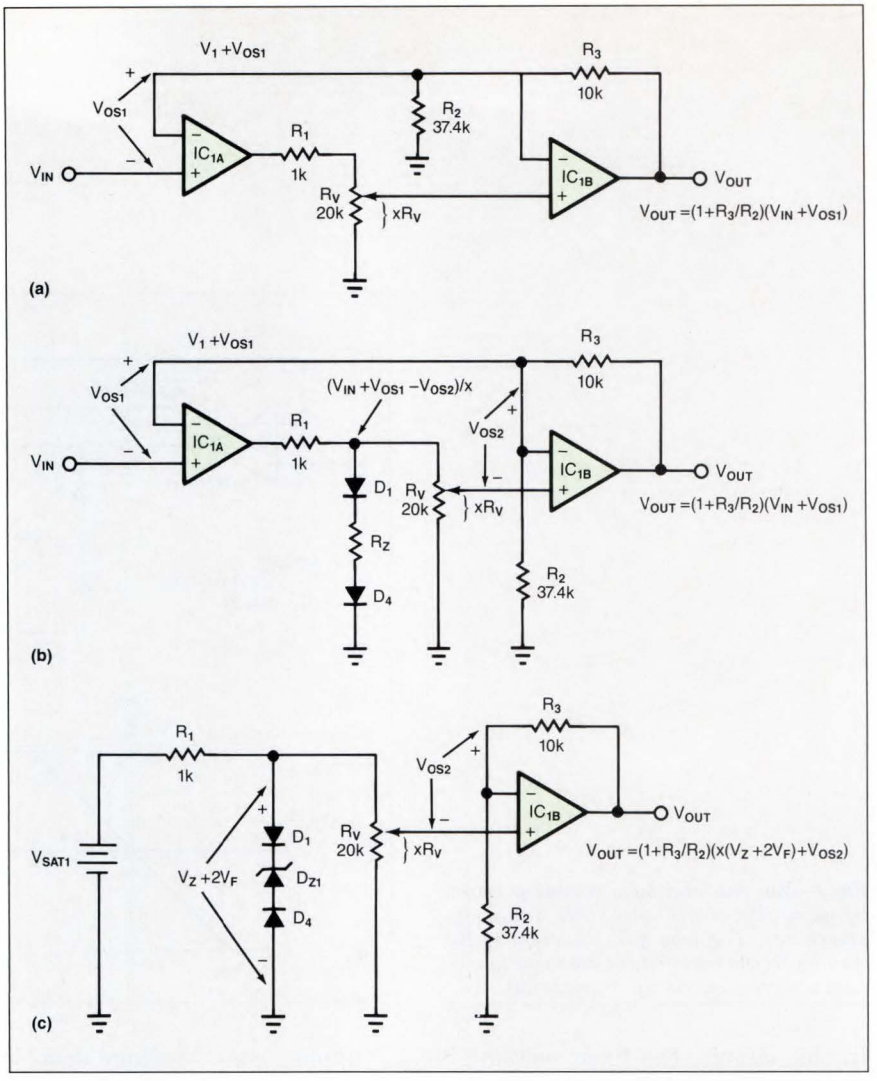

Fig 3—These simplified schematics illustrate *the dominant circuit elements of* ***Fig 2****'s operation in the linear range* ***(a)****, a transition state* ***(b)****, and a clamp state* ***(c)****.*

at 8.7V. If you take into account the gain added by IC_{1B}, which in **Fig 2** is 1.26, the maximum output clamp level is 11V. You can increase the clamp levels up to the limits imposed by the amplifier's power supply and output ratings. If you use the OPA2111 and operate the circuit from ±18V power supplies, this limit is ±14V. Using the high-voltage OPA445 and ±45V power supplies, you can raise the upper limit to ±40V.

The circuit of **Fig 2** is closer to the ideal limiter than the circuit of **Fig 1,** but it's not without errors. Amplifier offset voltages, component tolerances, diode-bridge matching, and rounding errors still cause the circuit to deviate from ideal performance.

The nonzero offset voltages of both amplifiers in **Fig 2** contribute to limiter errors; their effects differ depending on the various stages of operation. In the linear range of **Fig 3a,** only the offset voltage of IC_{1A} is significant; the effect of the IC_{1B}'s offset voltage is attenuated by the loop gain. The output error in this case is $(1 + R_3/R_2)V_{OS1}$.

The offset voltages of both amplifiers alter the input-signal trip points at which clamping begins. In the transition stage of **Fig 3b,** feedback adjusts the voltage across the bridge by $(V_{OS1} - V_{OS2})/x$ to compensate for the amplifier offsets. For small values of x, this voltage adjustment is large and alters the turn-on point of the bridge. If you trace this adjustment back to the circuit input, the input levels that produce clamping are shifted by $V_{OS1} - V_{OS2}$. When the circuit is in the clamp state of **Fig 3c,** IC_{1A} has no control over the output, and IC_{1B} sets the output offset error at $(1 + R_3/R_2)V_{OS2}$.

The OPA2111 dual op amp has a ±2-mV offset, which results in a ±2.5-mV output offset in the linear and clamping states. This offset shifts the input trip levels by as much as ±4 mV. In low-level applications, you can replace this dual op amp with trimmable OPA111s and adjust the offsets to the ±100-μV range. To ensure dc accuracy, the op amp you choose for IC_{1A} should have high input impedance under overload. In the clamp states, the inverting input of IC_{1A} is held at a fixed voltage while its noninverting input is driven by V_{IN}. This situation produces a differential input overload, but either the OPA2111 or OPA111 ensures that no input current flows through IC_{1B}'s feedback.

The accuracy of the circuit in **Fig 2** is limited by the tolerances of the components you choose, but the zener's bridge connection compensates for the largest errors. If you choose 1% tolerances for R_2 and R_3 and combine their tolerances with the typical 5% zener error, clamp levels can deviate by as much as 7%.

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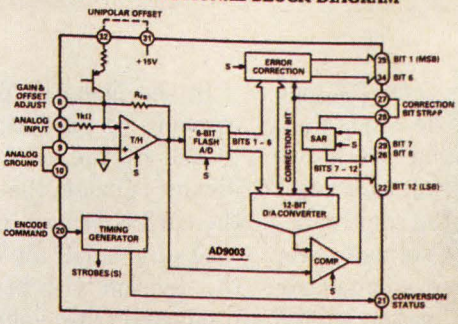

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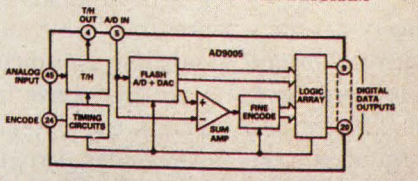

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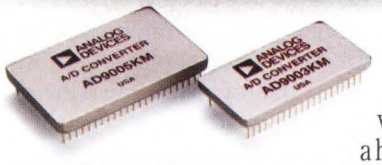

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CIRCLE NO 122

By using op amps and DACs, you can overcome the limitations of the simple back-to-back zener-diode clamping circuit.

Trimming R_2 and R_3 obviously removes their 2% gain error effect. An advantage to the bridge design is that, unlike the back-to-back zener approach in which two different zener diodes and thus two different tolerances control the positive and negative limits, the same zener diode establishes both limits. Thus, its voltage error is common to these two limits. You can compensate for this common error simply by adjusting the gain of IC_{1B}.

However, to a reduced degree, the polarity-sensitive error of back-to-back zeners continues with the bridge approach. Differing bridge drive currents and mismatches in the bridge diode drops still differentiate the two limit magnitudes. In each clamp state, the drive current supplied to the bridge is a function of either the positive or negative saturation level of the IC_{1A} output. These two output saturation voltages differ, and the bridge currents that result produce slightly different zener voltages for the two polarities. These saturation-voltage effects of **Fig 2**'s design produce an uncompensatable error of around 0.5% compared with the 5 to 10% error of the back-to-back zener case.

Unfortunately, the diode bridge that provides this zener error reduction introduces a polarity-sensitive error of its own. Different bridge diodes influence the positive and negative limits, and their voltage drops must match. Matching bridge diodes, however, is complicated by the fabrication techniques available for bridge assemblies. Because they lack a node with consistently more negative voltage, bridges cannot be built on a single chip with conventional junction-isolated processes. Most bridge assemblies consist of four independent diodes and lack the inherent matching of single-chip fabrication. For a typical bridge, diode forward voltages mismatch by around ± 30 mV, which doubles the polarity-sensitive error described above. The PWS740-3 bridge shown in **Fig 2** is made with dielectric, rather than junction, isolation to combine the diodes on one chip for voltage matching of around ± 3 mV.

Other clamping errors in **Fig 2** result from residual rounding in the input/output response. The ability of the loop gain to counter the zener error is a function of the compound voltage divider in the feedback loop. As shown in **Fig 3b,** this divider is formed by R_1, R_V, and the zener resistance, R_Z. Direct analysis of this divider is complex due to the nonlinear variation of R_Z. Instead, it's easiest to illustrate the relative improvement over basic zener clamping by examining the end points of the clamp transition.

In the linear-response range of **Fig 3a,** R_1 and R_V combine to produce a voltage divider primarily controlled by the potentiometer fraction x. This voltage divider is inside the feedback loop and directly reduces the corrective loop gain supplied by IC_{1A}. In the worst case, x is small for low clamping levels and dominates the division with practical values as low as 0.001. The product of this value and IC_{1A}'s dc open-loop gain of 1,000,000 yields a loop gain of 1000 as the circuit approaches the transition state. So, the initial transition rounding is reduced by a factor of 1000.

As the zener begins to turn on, R_Z decreases and shunts the potentiometer in **Fig 3b**. The attenuation of this compound divider increasingly reduces IC_{1A}'s loop gain right up to the limit point. At this limit point, R_Z typically approaches 100Ω, resulting in a 0.09 divider fraction formed with the 1-kΩ R_1. The net division caused by R_Z and R_V when $x = 0.001$ drops to 0.0009. The product of 0.0009 and the dc open-loop gain of IC_{1A} yields a loop gain of 90. Thus, the bridge circuit reduces the zener rounding effect by a factor varying from 1000 to 90 at low clamp levels and low frequencies. If you increase the clamping level, x becomes larger. This increase results in even sharper limiting with loop gains that remain as high as 90,000.

The clamping response of high-frequency signals exhibits more rounding because of the loop-gain reduction as the amplifier's open-loop gain rolls off. However, once the circuit settles into a limit state, the clamp level is controlled by the higher level of the dc gain. Higher-frequency clamping is also aided by the bridge connection of the zener diode. This circuit configuration reduces the time required to charge and discharge the zener capacitance. This capacitance is typically large, and, with the back-to-back zener connection of **Fig 1**, it must be charged and discharged continually as the signal swings. The resultant time delays, which inhibit signal transmission and reduce bandwidth, are reduced if you use the bridge configuration.

The bridge design effectively disconnects the zener and its capacitance when the circuit is not in the clamp state. Gating by the bridge diodes removes the zener from the circuit in the linear range and preserves the charge on the zener capacitance between clamp states. When disconnected, the zener capacitance holds its charge and doesn't need replenishment at the next clamp state. Only the much smaller capacitances of the bridge diodes are charged and discharged in this operation.

You can achieve still sharper clamping for both high

and low frequencies by supplying continuous dc bias for the zener (**Ref 1**). Sustained zener bias reduces the variation of diode resistance with signal swing and keeps the large zener capacitance more fully charged. When quiescent-current constraints permit this addition, you can provide the bias with two resistors. One resistor is connected from the positive supply to the zener cathode and the other from the negative supply to the anode.

Other components shown in **Fig 2** ensure frequency stability. R_4 and C_1 ensure that the roll off of IC_{1A} is always the dominant pole. This condition is automatically the case over much of the control range because the attenuation of R_V keeps the IC_{1A}'s feedback factor at low levels. A low closed-loop bandwidth accompanies this reduced feedback factor, so that IC_{1A} dominates the loop response. However, as x approaches unity, so does the IC_{1A} feedback factor. This condition requires phase compensation. The network made up of C_1, R_4, and R_1 ensures that, with $x=1$, IC_{1A}'s pole is still dominant.

Aided by the impedance isolation of R_4, C_1 bypasses the common feedback at higher frequencies by connecting the output of IC_{1A} to its inverting input. Then, IC_{1A} and IC_{1B} operate with independent feedback loops that only require the stability of the individual amplifiers. This phase compensation permits stable high-frequency operation to coexist with the common feedback loop and its dc error reduction. Still, any phase compensation added to a loop slows down its response. For higher-speed operation, you can break the common loop by removing R_4 and replacing C_1 with a direct connection. The zener action will remain within the IC_{1A} feedback loop, but the input-offset errors of IC_{1B} will also affect linear-range operation.

The potentiometer control circuit of **Fig 2** is suited for bench test requirements; it requires an operator to adjust limit levels. However, automated systems require digital control of clamping. Two ways to implement this control are a multiplexer adaptation of **Fig 2** and a DAC-controlled limiter design.

In the multiplexer-based design shown in **Fig 4, Fig**

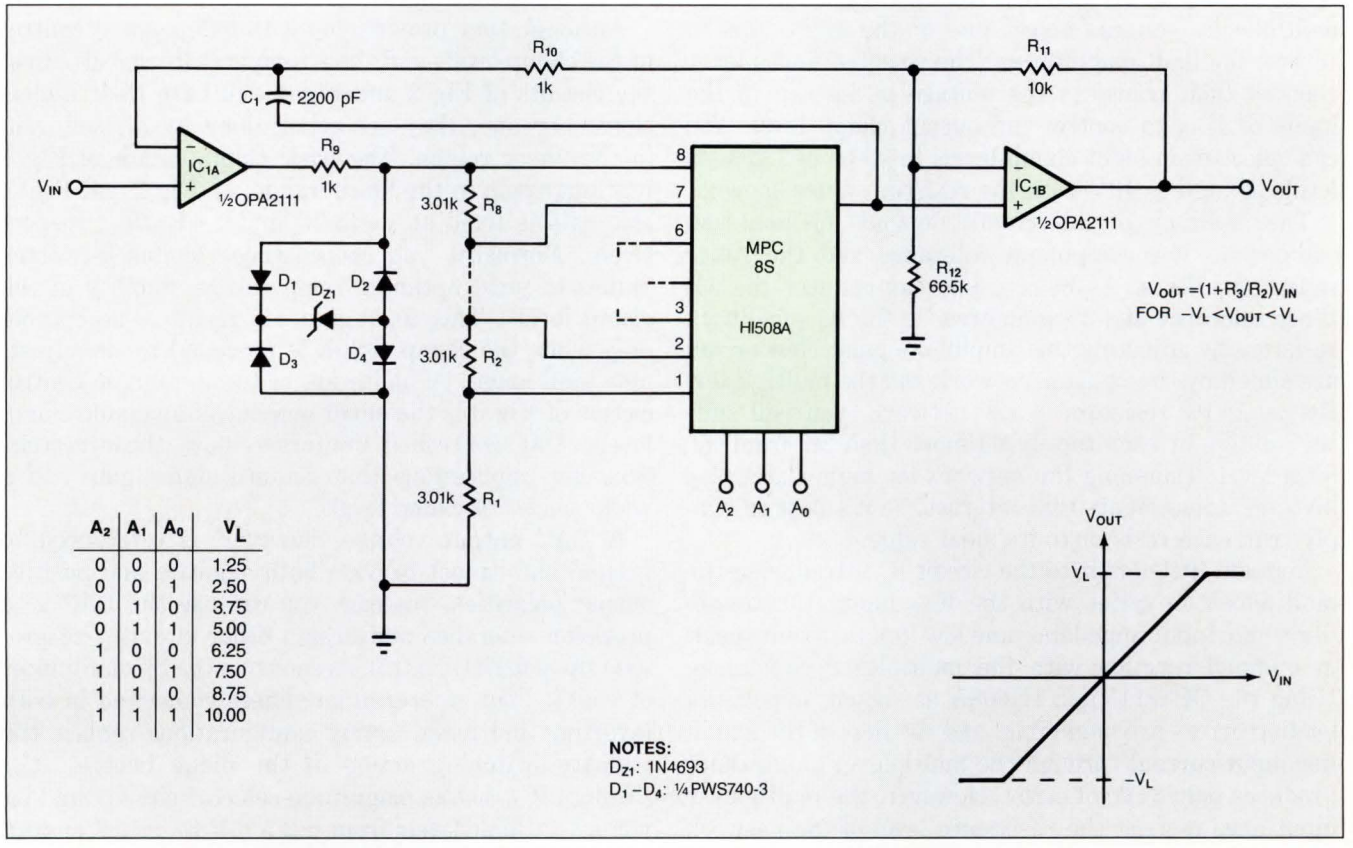


Fig 4—You can control clamp levels digitally *by replacing the potentiometer of* ***Fig 2*** *with a resistor network and a multiplexer. This circuit provides you with eight possible discrete clamp levels.*

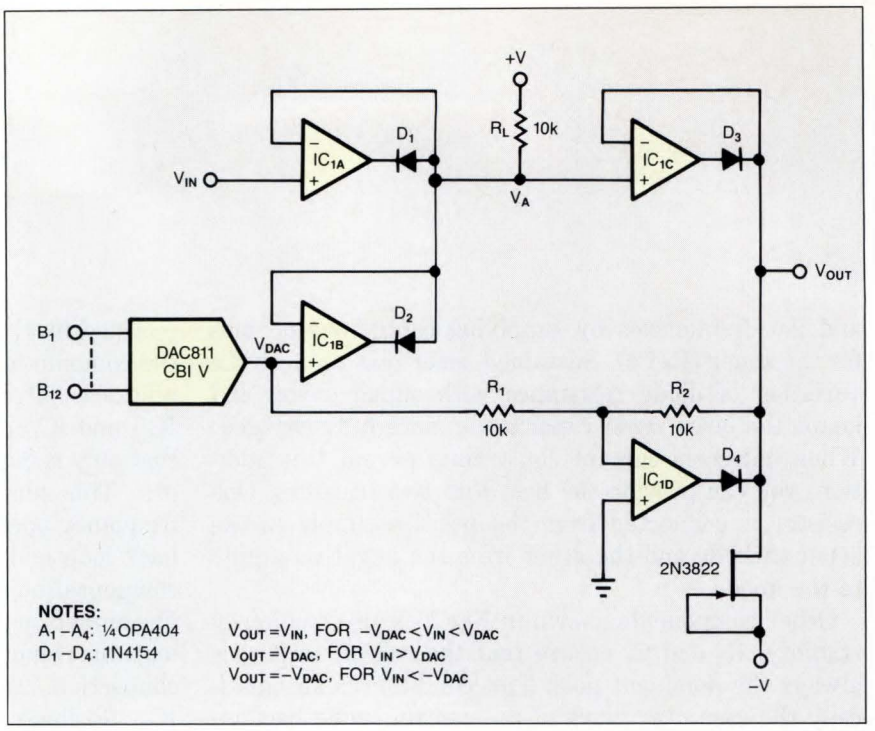


***Fig 5—The most flexible clamp circuit uses a DAC** to control limit levels. You can select among 4096 limit levels between ±2.5 mV and ±10V.*

2's potentiometer is replaced with a resistor network and a multiplexer. All of the advantages of **Fig 2** are retained with this new circuit. If you use a network with equal-valued resistors, the multiple taps of the **Fig 4** network provide you with a series of eight equally spaced voltage divisions. These eight taps divide the bridge output and provide the same control as R_V in **Fig 2**. By sending digital commands to the multiplexer, you can select one of the eight taps to control the limit magnitudes. The selected multiplexer channel then transfers the voltage at its tap to the input of IC_{1B} to control the output clamp level. You can select from eight clamp levels in steps of 1.25V to levels as high as 10V with the resistor values shown.

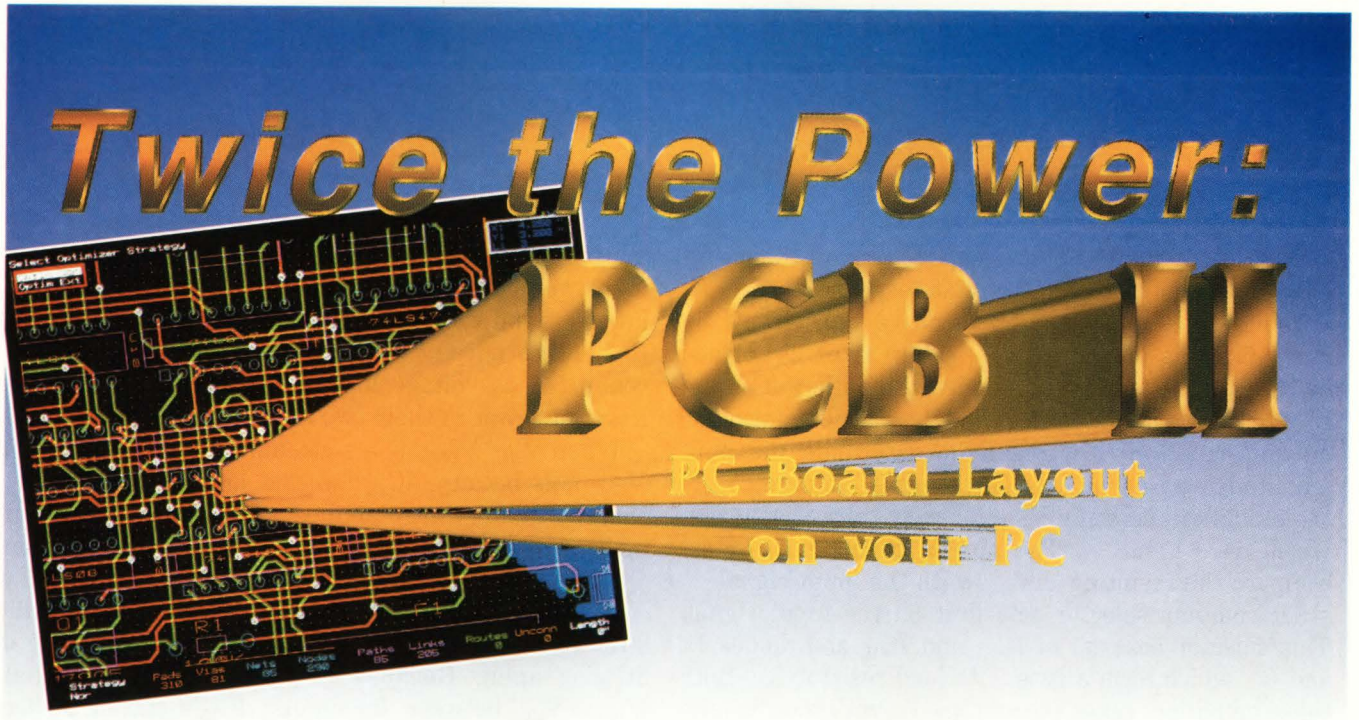
The accuracy of this circuit depends on how you compensate for component tolerance and the zener rounding effects. As before, you can counter the 5% zener tolerance and 2% gain error of the IC_{1B} feedback resistors by adjusting this amplifier's gain. New errors are added by the resistor network and the multiplexer. By using 1% resistors in the network, you will shift the voltage at each tap by no more than 2% from the ideal level. Trimming the network for higher accuracy involves adjustments that interact, so it's best to simply trim each resistor to its ideal value.

You add little error to the circuit by introducing the multiplexer in series with the IC_{1B} input; this amplifier's high input impedance and low input current result in minimal reaction with the multiplexer resistance. Using the OPA2111 and HI508A as shown, impedance loading errors are negligible, and the flow of the amplifier input current through the multiplexer's resistance produces only 3 nV of error. However, the multiplexer input does restrict the resistance level of the network in ac response considerations. The multiplexer input impedance is 1.5 kΩ in series with 25 pF to ground. This impedance loads the bridge-network output at higher frequencies; the result is a time-dependent rounding of the clamp turn-on response. When operating with input signal frequencies above 100 kHz, you can avoid rounding by reducing the values for R_1 through R_8.

A DAC adds flexibility

Although they provide you with independent control of the clamp levels and their temperature sensitivities, the circuits of **Fig 2** and **Fig 4** still have their limitations. For one, they are constrained by a fixed gain in the linear region. The basic clamp circuit of **Fig 1** has unity gain in the linear range. In **Fig 2** and **Fig 4**, this gain is fixed at $1+R_3/R_2$ and $1+R_{11}/R_{12}$, respectively. Normally, you choose these feedback-resistor values to yield optimum temperature stability of the clamp levels. This fixed-gain constraint is acceptable only when the clamp circuit is preceded by an adjustable gain stage. A limitation of the automatic control circuit of **Fig 3** is the small number of available clamp levels. DAC-controlled limiters remove these restrictions for applications that require signal gain and a wider choice of clamp levels.

A DAC output voltage, however, is referenced to ground and cannot provide both negative and positive output polarities. Instead, you can use the DAC as a precision reference and design other circuitry to provide the polarity control, as shown in the bipolar limiter of **Fig 5**. Four reference amplifiers connected in both inverting and noninverting configurations replace the polarity-switching action of the diode bridge. IC_{1A} through IC_{1D} act as magnitude-selector circuits and let you select limit levels from ±2.5 mV to ±10V in 4096 steps using the DAC811. Gating diodes D_1 through D_4 provide the switching for the clamp action and are



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A single zener diode enclosed in a diode bridge implements both positive and negative limit polarities and improves the circuit's accuracy and speed.

enclosed in op-amp feedback loops to remove their voltage drops from the overall circuit response.

You set the positive and negative limit levels by using maxima and minima selectors (**Ref 2**) formed by the op amps and gating diodes. Amplifiers IC_{1A} and IC_{1B} form the minima selector; IC_{1C} and IC_{1D} form the maxima selector. IC_{1B} and IC_{1D} determine the limit amplitudes based on the DAC output voltage, V_{DAC}; the amplifiers multiply V_{DAC} by their respective gains, which are $+1$ and -1. The minima and maxima circuits compare the resulting $\pm V_{DAC}$ with the input signal.

The minima selector acts first on the input signal. This selector consists of IC_{1A} and IC_{1B} and diodes D_1 and D_2, which form a gate with load resistor R_L. Both these amplifiers sense the voltage V_A with their inverting inputs, and each amplifier attempts to transfer its input voltage to V_A. Only one amplifier can do so, however; and the gate diodes select the amplifier with the lowest output voltage. Since IC_{1A} and IC_{1B} are connected as voltage followers, the gate actually selects the lower of their two input voltages.

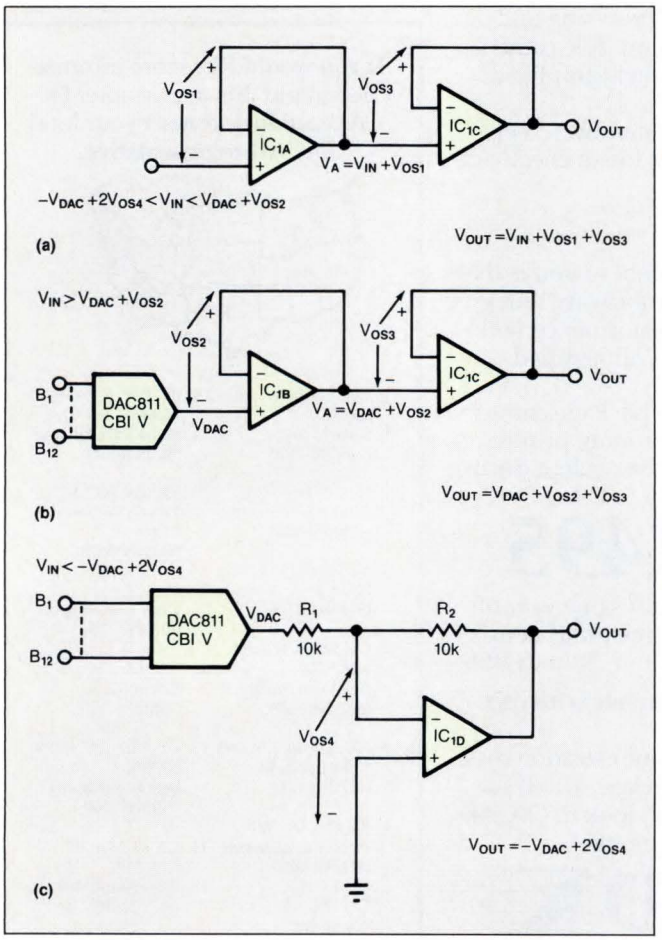

Fig 6—Depending on the input level, *the active amplifiers of* ***Fig 5*** *will be some combination of minima and maxima selector circuits. A linear-range input activates two voltage followers* ***(a)****, an input greater than* V_{DAC} *activates the positive DAC control and two voltage followers* ***(b)****, and an input less than* $-V_{DAC}$ *activates DAC control and an inverting amplifier* ***(c)****.*

When $V_{IN} < V_{DAC}$, IC_{1B}'s attempt to force V_A to equal V_{DAC} fails because IC_{1A} forces a lower voltage at V_A, thereby taking control of diodes D_1 and D_2. The output of IC_{1A} forward biases D_1 and reverse biases D_2. Then, the IC_{1A} acts as a voltage follower, forcing V_A to follow V_{IN} for a linear, unlimited response at this point in the circuit. With D_2 reverse biased, the feedback loop of IC_{1B} is open. Because of the differential signal, $V_{DAC} - V_{IN}$, between its inputs, IC_{1B}'s output swings to its positive saturation level. Only slight differences between V_{DAC} and V_{IN} are required to activate this selection gate because of the high open-loop gains of the op amps.

Increasing V_{IN} above V_{DAC} reverses the bias states of D_1 and D_2, thus putting IC_{1B} in control of V_A. Under these conditions, the minima selector output, V_A, is clamped at V_{DAC}, thereby setting the level of the upper boundary of the bipolar limit.

The signal passed through the minima selector, whether V_{IN} or V_{DAC}, still faces the maxima selector of IC_{1C} and IC_{1D}. Diodes D_3 and D_4 perform maxima signal gating, so that the amplifier with the larger output voltage prevails. Note that the diodes' directions are opposite to those in the minima selector. IC_{1C} attempts to set the output equal to V_A, and IC_{1D} attempts to set the output equal to $-V_{DAC}$. When $V_A > -V_{DAC}$, the higher voltage at IC_{1C}'s output forward biases D_3 and reverse biases D_4. Then, $V_{OUT} = V_A$, and the output is equal to either the linear transmission of V_{IN} or the positive limit level of V_{DAC}. However, when the input signal drives V_A below $-V_{DAC}$, IC_{1D} reverses the states of D_3 and D_4 to take control of the output. Then, $V_{OUT} = -V_{DAC}$.

As with the circuit of **Fig 2,** you can draw simplifed circuit diagrams of the circuit of **Fig 5** that correspond to the linear mode of operation and its positive and negative limit states (**Fig 6**). If $V_{IN} < V_{DAC}$, the signal is passed by the minima selector, so that $V_A = V_{IN}$. If this signal is also greater than $-V_D$, it passes through the maxima selector as well. As a result, $V_{OUT} = V_A = V_{IN}$. In this case, the controlling circuit is simply two voltage followers in series, as shown in **Fig 6a.** Here, reverse-biased diodes remove amplifiers IC_{1B} and IC_{1D} from the control path.

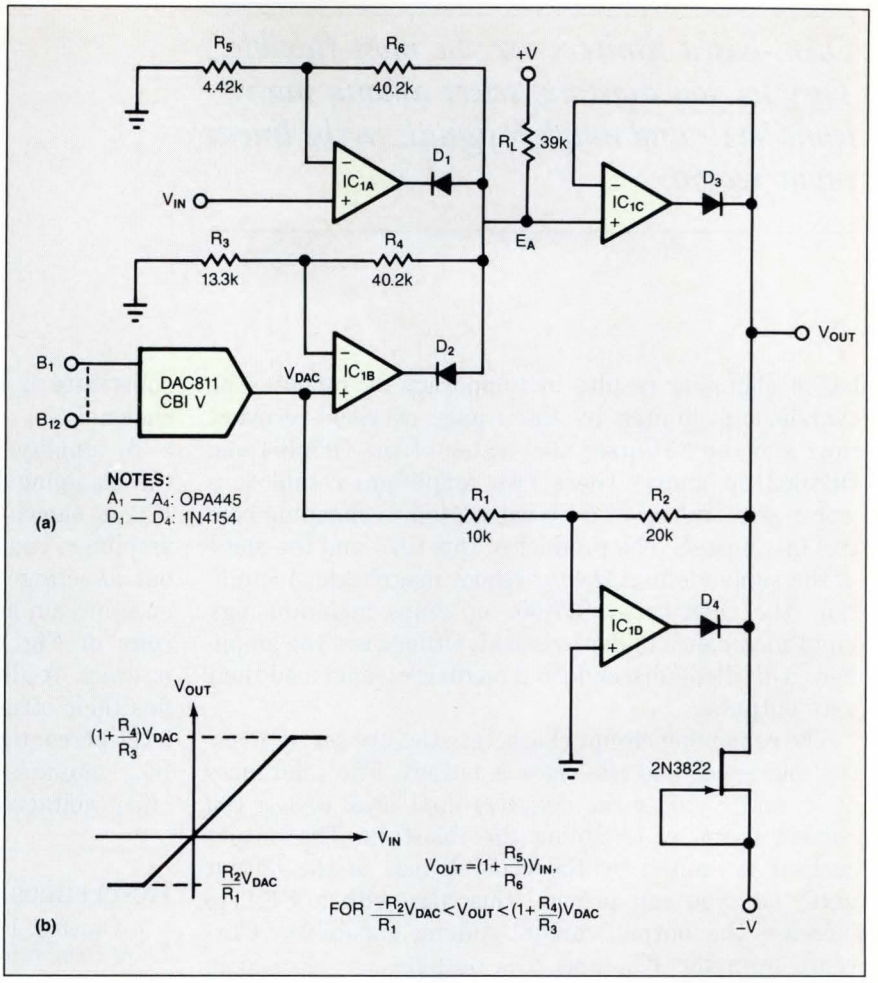

***Fig 7—By altering the feedback** around IC_{1D} and adding gain to IC_{1A} and IC_{1B}, you can modify **Fig 5** for asymmetrical clamping, higher clamping levels, or signal gain.*

When $V_{IN} > V_{DAC}$, the input signal is stopped by the minima selector, and $V_A = V_{DAC}$. This condition makes V_A greater than the $-V_{DAC}$ limit of the following maxima selector, so $V_{OUT} = V_A = V_{DAC}$. As shown in **Fig 6b,** this positive clamp state also enables two voltage followers in series. This time, however, the followers are connected to the output of the DAC instead of the signal input.

In the third case, $V_{IN} < -V_{DAC}$, so that the input signal passes through the minima selector. However, this negative V_{IN} is stopped by the maxima circuit, thus leaving IC_{1B} and IC_{1C} disabled. IC_{1A} and IC_{1D} both retain control of their feedback loops, but only IC_{1D} has access to the output. As shown in **Fig 6c,** IC_{1D}'s inverting amplifier is connected to the DAC output and controls V_{OUT} to yield $V_{OUT} = -V_{DAC}$.

The circuit's conformance to the three ideal states is altered by static and dynamic errors. The simplified diagrams of **Fig 6** help you identify the component offsets that contribute to error in each of the three states. The DAC's offset voltage affects the clamp states of **Figs 6b** and **6c**; you can trim the DAC811 to reduce its 5-mV error to 0.1 mV. As shown in **Fig 6,** amplifier offsets affect all three circuit states. You can trim IC_{1A} and IC_{1B} separately to remove offsets in the linear and positive limit states of **Figs 6a** and **6b.**

In the negative limiting state, IC_{1D} is the only amplifier that affects the output offset voltage, as shown by **Fig 6c.** However, IC_{1D}'s input offset is amplified by $1 + R_2/R_1$, which is equal to 2 in this example. Due to this amplification, the amount of offset error in **Fig 6c** is equal to those of the 2-amplifier states of **Figs 6a** and **6b.** The 0PA404 quad op amp shown in **Fig 5** doesn't let you trim offsets. But you can replace this quad device with four equivalent OPA602s, which do let you trim the offset. In each of the **Fig 6** cases, the untrimmed OPA404 typically produces an output offset of 520 μV; the OPA602 replacement lets you trim this error to 100 μV. By using the OPA602, you can hold the circuit's overall static errors—including those contributed by the DAC—to 200 μV.

Saturation adds recovery error

Dynamic errors due to amplifier overload recovery and slew rate also constrain the **Fig 5** response. While most op-amp circuits stay in the linear range of operation, the **Fig 5** limiter lets its amplifiers saturate. When one amplifier of the gating supercedes another, the loser drops into an output-saturation state. To switch back into control, the saturated output must first recover from the saturation overload and then slew to the voltage required for output control.

During such time delays, the circuit state is in error. The error is most noticeable upon entering a clamp state: The circuit output continues to follow the input signal, while the saturated amplifier recovers. This de-

DAC-based limiters are the most flexible: They let you digitally select among many limit levels and amplify signals in the linear input region.

lay in clamping results in temporary overshoot. The overshoot is limited by the 1-μsec overload-recovery time and the 35V/μsec slew rates of the OPA404 and OPA602 op amps. These two amplifiers complete a worst-case transition from saturation to clamping control in 1.6 μsec. The product of this time and the slope of the signal defines the overshoot magnitude. In addition, the OP404 and OPA602 op amps maintain high input impedance under overload. Otherwise, the amplifiers with diode-disconnected feedback would load their gate outputs.

The remaining circuit characteristics are set by resistor tolerances and the class A output. The tolerances of R_1 and R_2 alter the negative limit level unless you correct them by trimming the resistors. The output current is limited by the class A bias of the output gate, but you can provide this bias with a FET to increase the output current-sinking capability. Currents from the IC_{1C} and IC_{1D} outputs are blocked in one direction by diodes. In these cases, only the FET can sink load current. However, the FET is an improvement over simple resistor bias, since the current-sinking ability of a resistor is restricted under large, negative output-voltage conditions. The FET ensures that the circuit's current-sinking capability remains constant as the output swings; the FET shown in **Fig 5** sinks 1 mA down to a −10V output.

Modifications add functionality

You can modify **Fig 5** to achieve unipolar or asymmetrical limiting, higher voltage limits, or higher signal gain. For unipolar clamping, simply remove either the maxima or minima stage. You can introduce asymmetrical limiting most easily by increasing or decreasing the negative clamp limit. You can make this adjustment by altering the closed-loop gain of IC_{1D}—that is, by changing the value of either R_1 or R_2.

You can similarly adjust and increase the positive limit level by adding feedback around IC_{1B}. You now have independent control over the positive and negative limit levels; the two limit magnitudes are related only by the ratio of the IC_{1B} and IC_{1D} gains for all DAC input control codes. By setting both gain magnitudes above unity, you can achieve limit levels beyond the output capability of the DAC. By using the component values indicated in **Fig 7,** the circuit can achieve clamp levels as high as 40V and as low as −20V. If you want your circuit to support these higher voltages, substitute a high-voltage OPA445 for the op amps shown.

To amplify input signals and simultaneously fulfill the clamping function, you can alter the feedback of IC_{1A} as shown in **Fig 7.** By converting IC_{1A} to a voltage amplifier, you introduce gain into the signal path without affecting the output clamp levels. This independence of gain and level clamping contrasts with the circuits of **Fig 2** and **Fig 4,** where the two functions interact. Adding gain to the various amplifiers magnifies their offset errors but doesn't increase the clamp-level percentage errors. Raising the gains of IC_{1B} and IC_{1D} amplifies the clamp-level voltages along with the offset voltages. EDN

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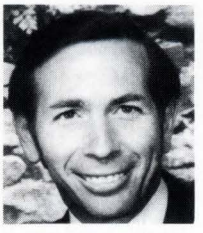
2. Graeme, J G, *Designing with Operational Amplifiers*, McGraw-Hill, New York, NY, 1977.

Author's biography



Jerald G Graeme is manager of instrumentation-components design at Burr-Brown Corp (Tucson, AZ) where he directs a linear-IC development group. He holds a BSEE from the University of Arizona and an MSEE from Stanford University. Jerry has eight patents to his credit. His leisure pursuits include photography, woodworking, and scuba diving.

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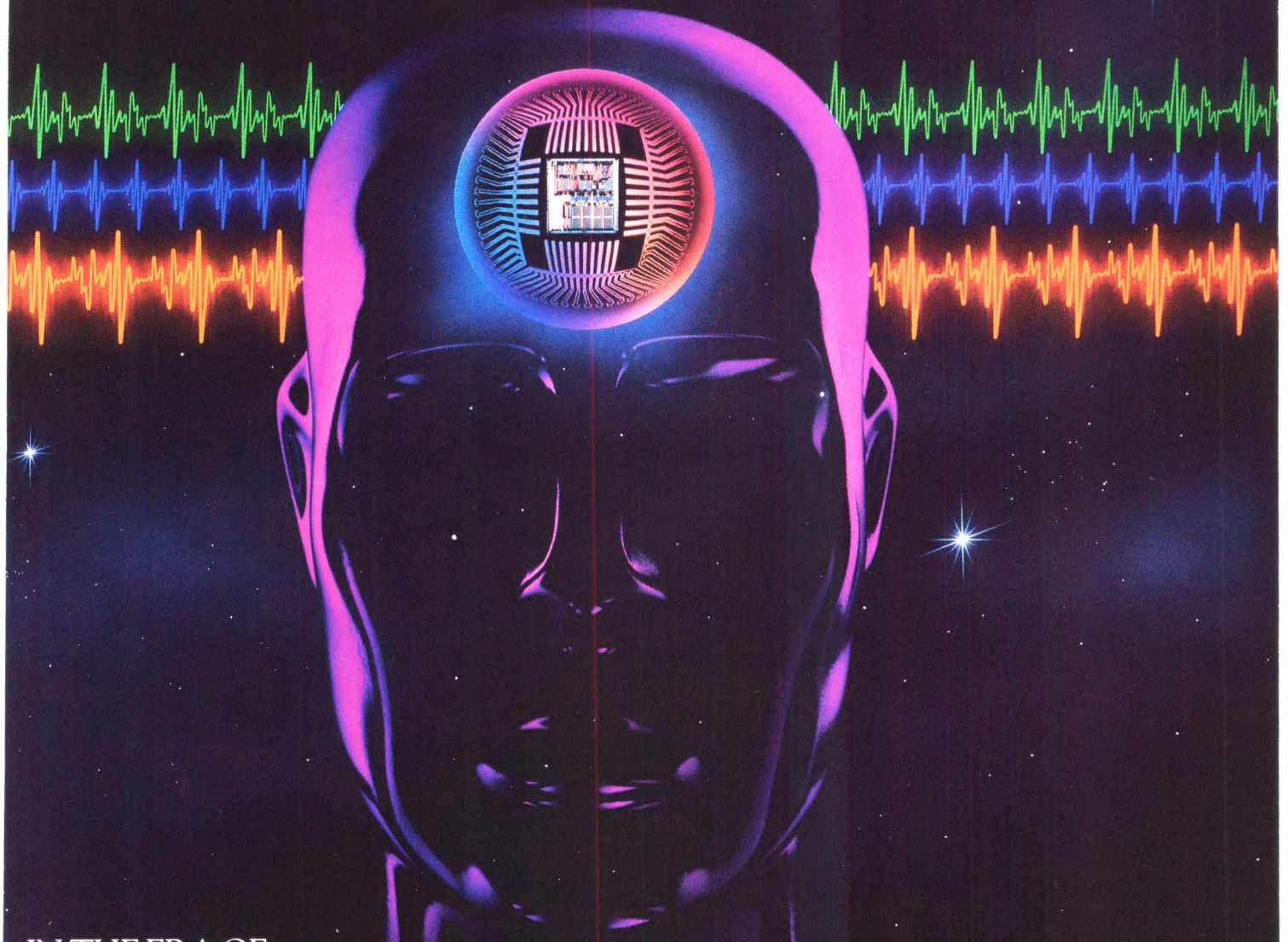
New ways to link digital brains to advanced analog worlds



IN THE ERA OF

MegaChip TECHNOLOGIES

Next-generation analog: Advanced Linear ICs

A new breed of linear chips, born of leadership processing at Texas Instruments, can help you design superperformance systems.

Sophisticated design and simulation tools shorten development cycles of TI's Advanced Linear ICs, helping you get to market faster. By using these tools, TI can offer as standard circuits many designs that previously would have had to have been customized.

The human brain has separate but dependent left and right sides. Similarly, an electronic "brain" or system has separate but dependent parts, one digital, one analog. Designers accustomed to the spectacular performance gains made in digital chips are now demanding comparable improvements in analog devices so that both parts of their systems can function to full potential. Leading the analog evolution: Advanced Linear circuits from Texas Instruments.

These new chips are called *advanced* for one or more reasons. They are more highly integrated than ever before, often combining digital and analog functions on a single chip. They offer higher performance and greater flexibility. They are often the result of advanced processing that may merge two or more technologies.

Better parameters from better processing

Because advanced analog system requirements for performance and flexibility vary greatly, a single workhorse technology typically can't do the job any longer. Nor can creative circuit designs alone. We at TI are convinced the key to driving the linear evolution lies in the excellence of our processing technologies.

TI is committed to developing and implementing a range of leadership wafer-fabrication processes (*see descriptions on back page*). The result: TI's Advanced Linear devices are already helping system designers link digital brains to advanced analog worlds more efficiently and with greater ease in many applications. Here are a few examples.

Advanced Linear: Displaying greater brilliance

Out of our pacesetting LinEPIC™ processing comes our high-performance Color Video Palette, operating at 125 MHz with a very high-resolution 1024 x 1024 pixel count. Because of one-micron CMOS processing, power consumption is reduced more than 40% compared to other CMOS implementations. Additionally, the device is pack-

...the key to driving the linear evolution lies in the excellence of processing technologies.

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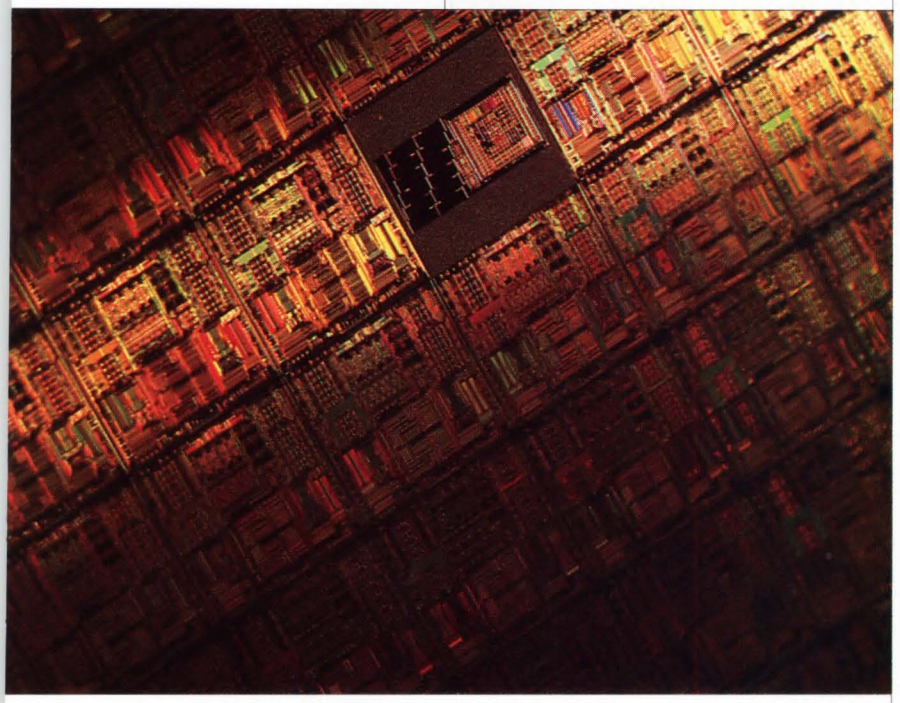
LinEPIC has also produced such high-speed, high-density interface chips as our Flash A/D and our Video DAC for use in graphics displays, imaging systems, monitors, and cameras. Both devices require about five times less power than bipolar equivalents.



High-density Analog Interface Circuit chips demonstrate the greater integration achieved by TI's innovative linear processing technologies. These DSP interfaces allow you to alter circuit configuration under software control without external adjustments.

Advanced Linear: Intelligent power for every car

Chips fabricated with our Power DMOS-based BIDFET™ processing are replacing electromechanical relays in many automotive applications, such as driving headlamps and motors. Power BIDFET allows us to minimize power loss in the switch and add high-complexity logic functions.

Multi-EPI bipolar processing, a very cost-effective technology, is used to produce chips having inherent reverse battery protection and high operating voltages. Such chips are ideal for use in automotive antilock braking systems, electronic transmissions, and active suspension systems.

Either technology can produce devices with low-side drive, high-side drive, or H-bridge configurations.

In the future, these developments may lead to multiplexed systems for cars, replacing bulky wiring harnesses.

Advanced Linear: Enhancing modems and facsimiles

TI's dual driver/receiver is a good example of the integration achieved with advanced processing technologies. LinBiCMOS™ processing has enabled us to put the drivers and receivers needed for RS-232 voltage levels on the same chip with the charge pump required to generate the necessary split rails from a single 5-V supply. You eliminate external power supplies and get a device that's easier to design with—it is available in our LinASIC™ cell library for integration with digital ASICs.

A new family of Analog Interface Circuits (AICs) is emerging from our Advanced LinCMOS™ processing. The voice-band AICs, designed for modems and fax equipment, combine high-performance analog functions—14-bit A/D and D/A converters and switched capacitor filters—with digital functions such as control circuitry, program registers, and DSP interface. The usual clutter of resistors, capacitors, and pots is eliminated.

High-speed AICs are available for use in servo controllers and hard-disk-drive applications.

These AICs are also high-performance members of our LinASIC standard-cell library. Based on TI's proven digital ASIC methodologies, the LinASIC library has allowed us to develop complex, semicustom chips in as little as 16 weeks.

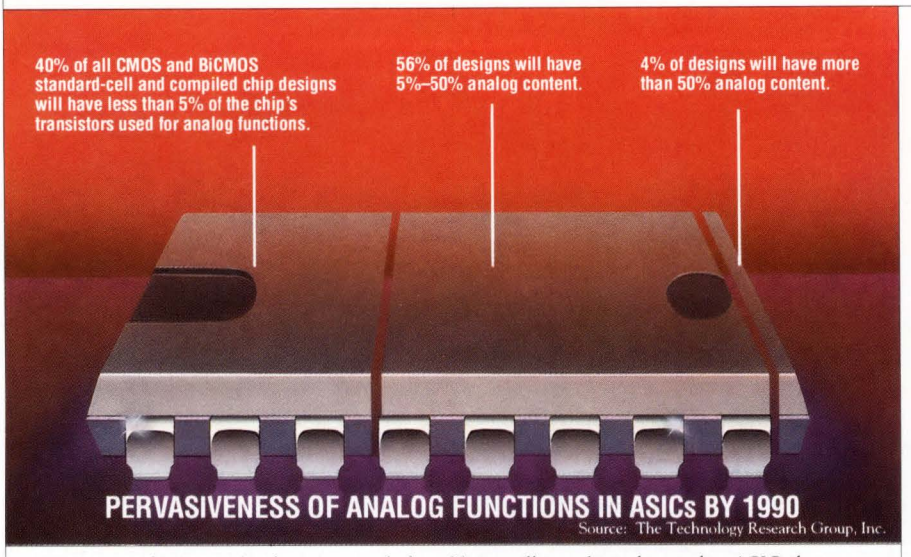
Advanced Linear: Boosting instrumentation accuracy

Even one of the most basic analog building blocks, the operational amplifier, is benefiting from TI's Advanced Linear technologies. Our Excalibur op amp family combines low power consumption with a 5X speed improvement while retaining low offset voltages. Offset-voltage drift has been cut from 300 μV to 60 μV to reduce your calibration, test, and measurement expenses.

For high-accuracy applications, Advanced LinCMOS is making possible Chopper Stabilized Op Amps with chopping frequencies 10 times higher than previously available (10 kHz). Noise levels are the lowest on the market.

The evolution in analog devices has only begun. Dramatic progress lies ahead throughout the 1990s. As the Advanced Linear leader, Texas Instruments is pledged to remain at the forefront, supplying you with new ways to link digital brains to advanced analog worlds.

For suggestions on choosing a linear supplier, turn the page.



Circuits combining analog functions with digital logic will soon be widespread in ASIC chip designs. TI is taking a leadership role with the development of its LinASIC methodology.

Checkpoints for choosing an analog supplier in the 1990s.

Questions and answers with Tom Engibous, Vice President, Semiconductor Group, and Manager, Linear Products, Texas Instruments Incorporated.

Q. What is the first thing to look for in choosing a linear supplier?

A. Product performance is definitely the first priority. Our customers are asking for ever-increasing linear device performance. At TI, we believe creative circuit designs alone won't meet the challenge. Advanced process technologies—note the plural—are becoming the keys to success in linear device performance of the '90s.

Q. What else should a designer look for?

A. Whether or not the supplier has experience with digital as well as analog devices. These two worlds are merging (*see chart above*). Functions once performed by analog are now done digitally, and a growing percentage of our Advanced Linear devices combines analog and digital circuitry on one chip.

At TI, we've leveraged our 30 years of digital expertise into the development of our Advanced Linear products and processing with highly satisfactory success. This has been especially noticeable with our LinASIC methodology.

Q. Do you expect ASICs to play a major role in your linear future?

A. Very definitely, as they already do today. Cell-based designs will be the rule in both user-specified functions and highly integrated standard products. Digital ASIC methodologies are also the key to cutting system design cycles. As our digital experience proves, suppliers who have advanced process technologies and fast, accurate design-automation tools will be the best equipped to deliver single-chip solutions.

Today, we have customers doing their own LinASIC designs using our advanced processes and design-automation tools.

Q. What role does manufacturing capability play in picking a supplier?

A. It is always a factor, and the need for efficient worldwide manufacturing facilities such as TI has in place will become even more important. Today's semiconductor market is global in nature. You can't serve worldwide customers from a single plant—you have to be "multilocal." This is particularly true with ASICs.

Q. Any other important factors?

A. Yes, I'd suggest that, in choosing a linear supplier, the designer find one he can live with for a long time. Close supplier-customer relationships are essential to the development of products that will provide the highest performance and lowest cost systems.

TI's Leadership Linear Processing Technologies

LinBiCMOS—Combines Advanced LinCMOS, digital ASIC CMOS, and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

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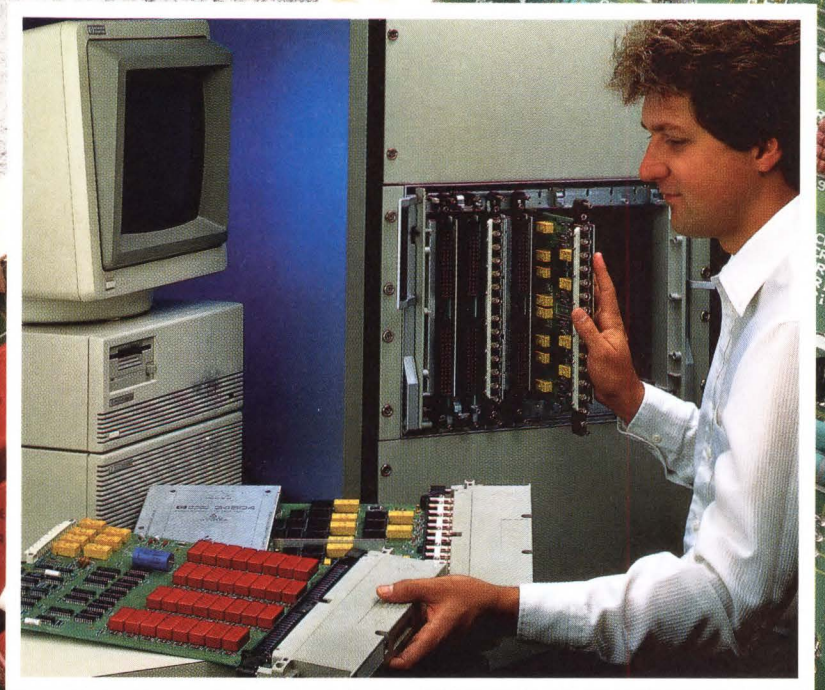

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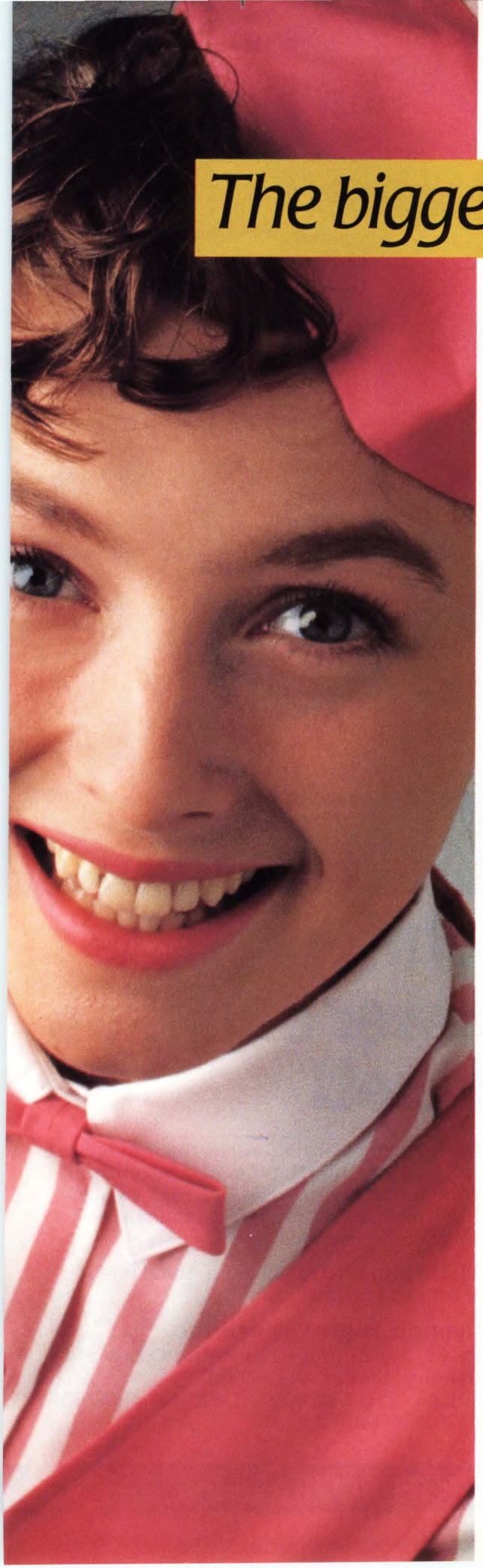

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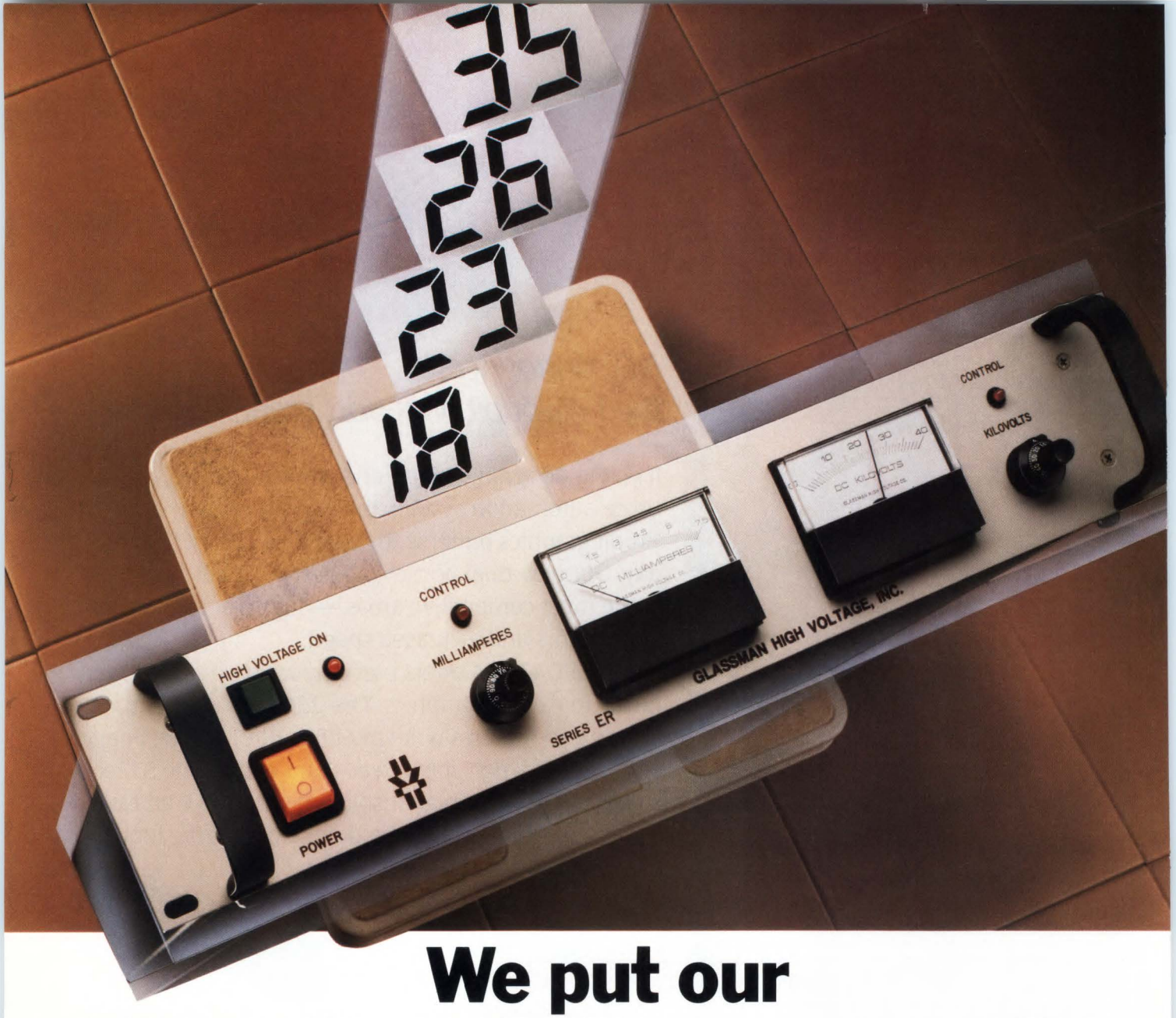

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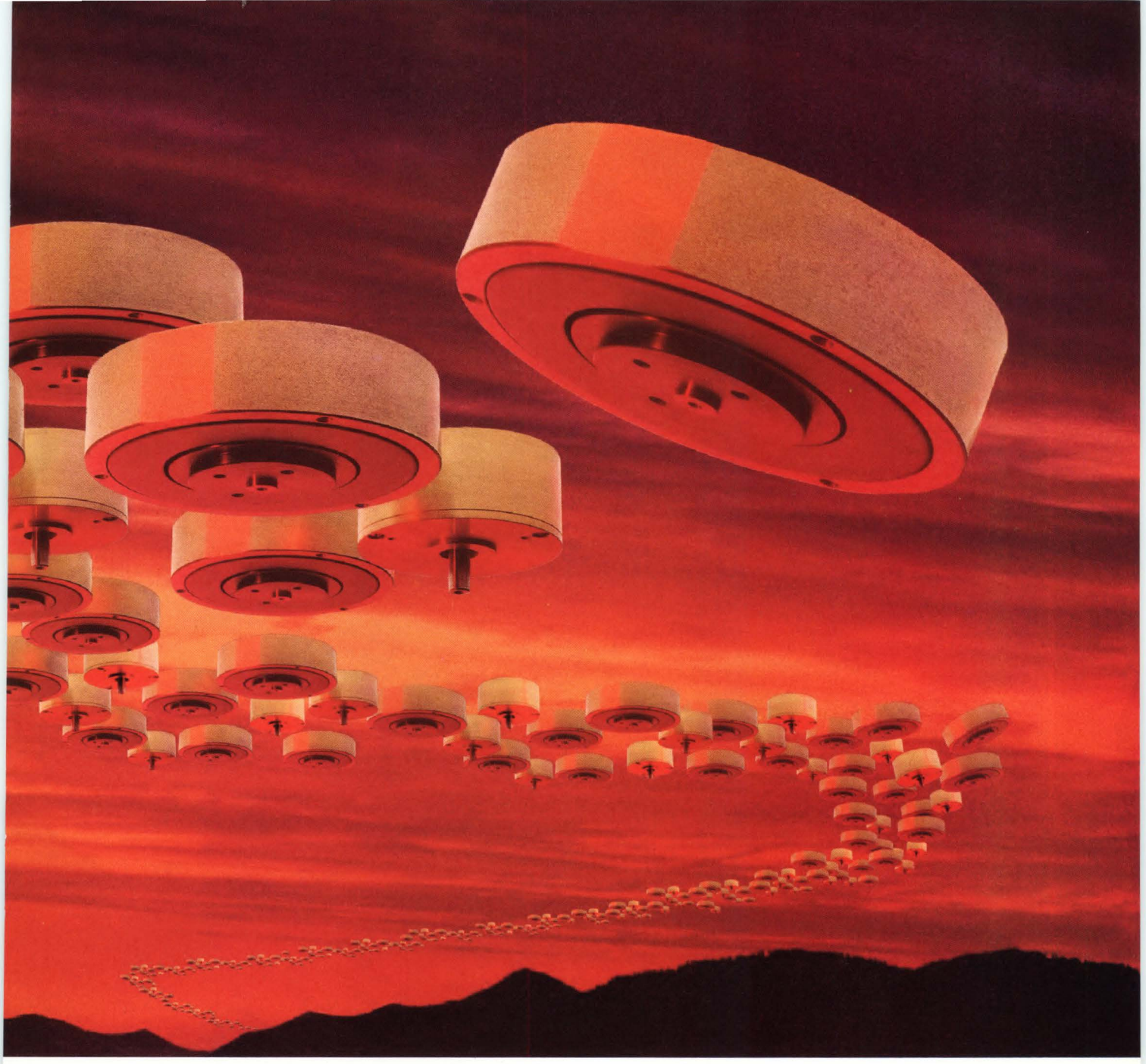

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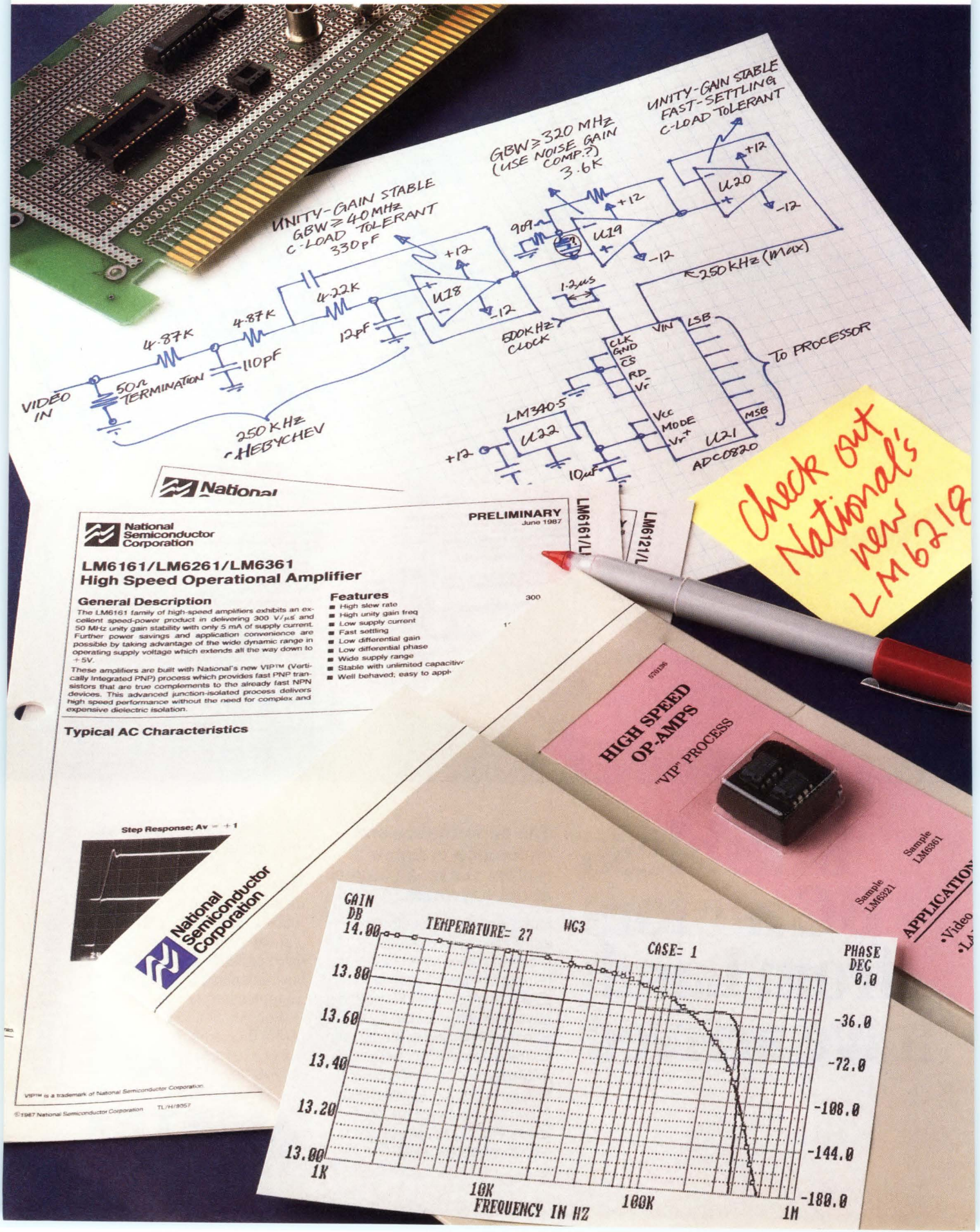

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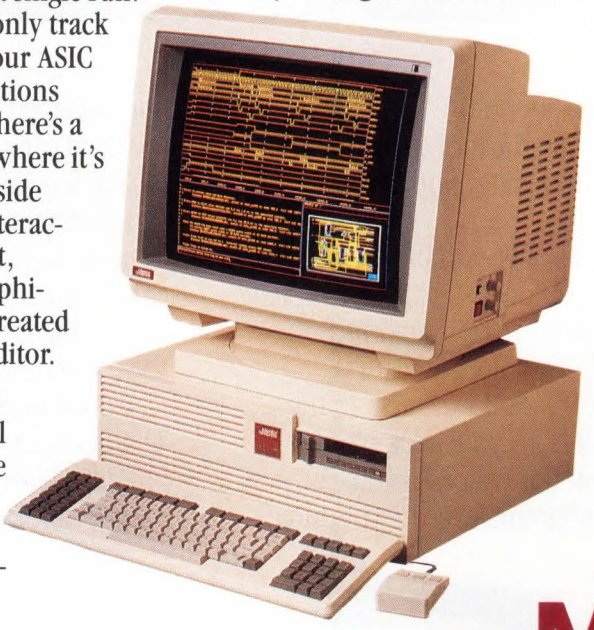

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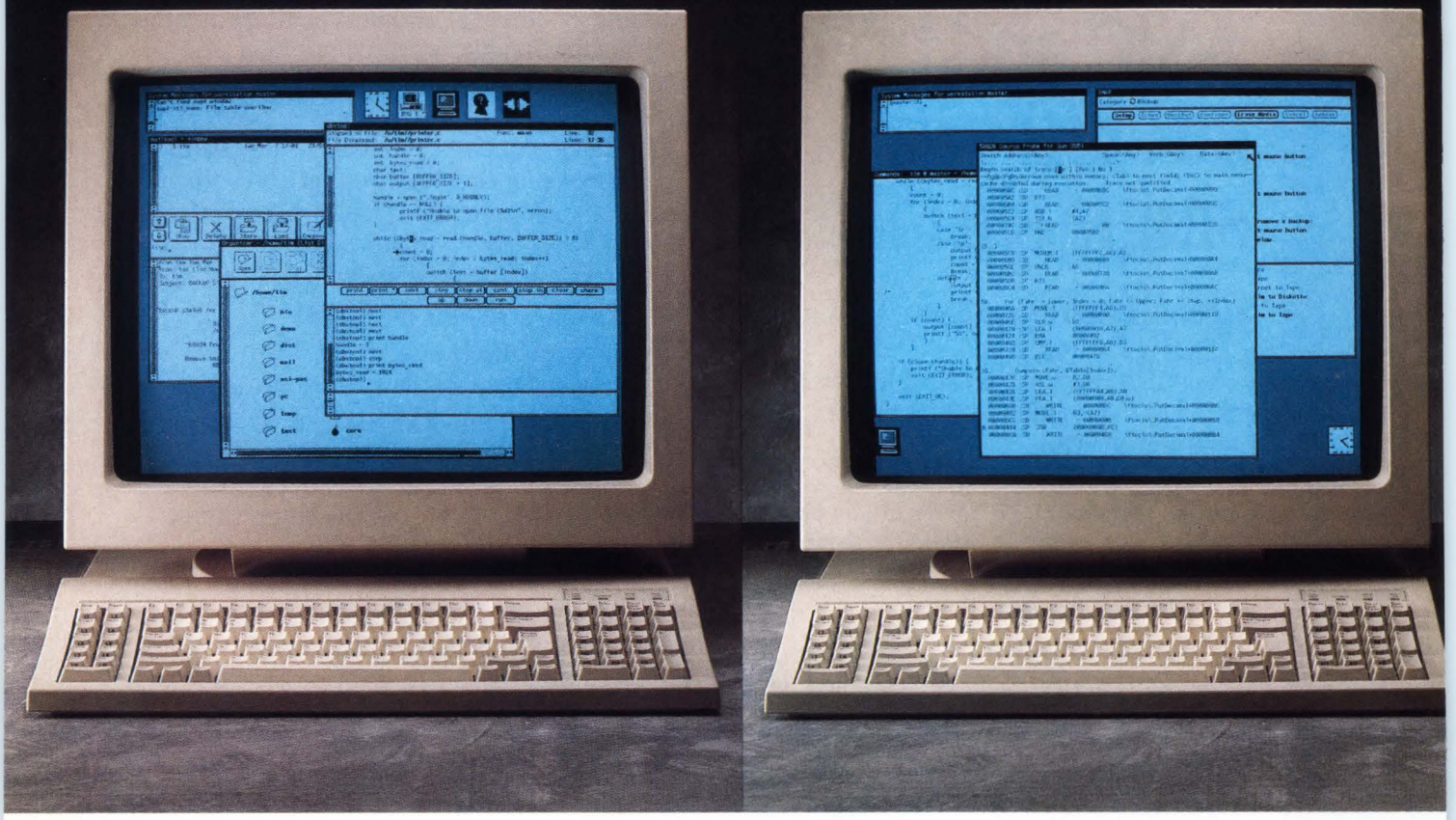

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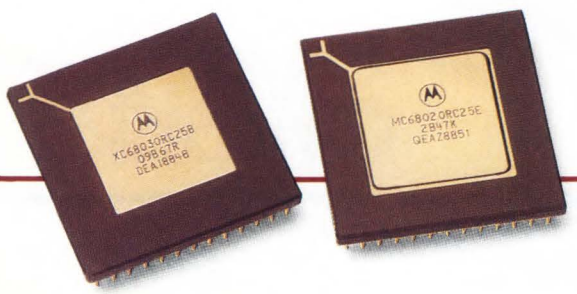

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Design simple routines to diagnose ills in complex systems

By following some basic guidelines when you design internal diagnostic routines and by ensuring that the hardware includes the proper circuitry, you can develop effective and easy-to-use debugging routines.

Matt Klein, *Hewlett-Packard Co*

Because today's RF and microwave systems are more sophisticated than ever, internal diagnostic routines are no longer an option, but a necessity. System operators must be able to localize and repair faults without extensive downtime. Furthermore, many remote or high-security organizations, such as military facilities, can't afford the time or risk of sending an instrument or an entire system to a factory for repair. If you design internal diagnostic programs properly, though, users or technicians can quickly test and repair today's complex systems on site, therefore minimizing downtime and repair costs.

Internal diagnostic programs are usually firmware routines that users can easily access by using some basic computer commands. Unlike most test equipment, diagnostic routines also let the users test systems in real time. With minimal auxiliary equipment, users can test components as simple as a subsystem of an instrument or as complex as an entire system of instruments. If the routines identify a bad field-replaceable unit, the user can replace it while in the field and later analyze the problem on the bench with more extensive diagnostic routines and test equipment.

Internal diagnostic routines not only benefit the end users, but also help designers and vendors prevent problems before a system reaches the market. During the system-integration process, for example, these routines let R&D specialists verify that their subsystems are compatible and can communicate properly. Manufacturers can use diagnostic routines to identify both assembly and electrical problems as well as problems that result from environmental life-cycle testing.

To develop internal diagnostic routines that can achieve these different levels of performance, you must incorporate some general principles in your design. You should also participate in the hardware design process to ensure that systems include circuitry that facilitates internal diagnosis; good diagnostic programs are effective only if diagnostic hardware exists in the systems to be monitored.

Keep it simple

Simplicity is the key to designing an effective diagnostic program. Users shouldn't have to know a lot about the instrument under test and shouldn't have to connect external equipment to use diagnostic routines. For example, the Frequency Agile Signal Simulator (FASS), a system of RF, microwave, and digital instruments (**Fig 1**), lets users execute the system's

Simplicity is the key to designing an effective diagnostic routine.

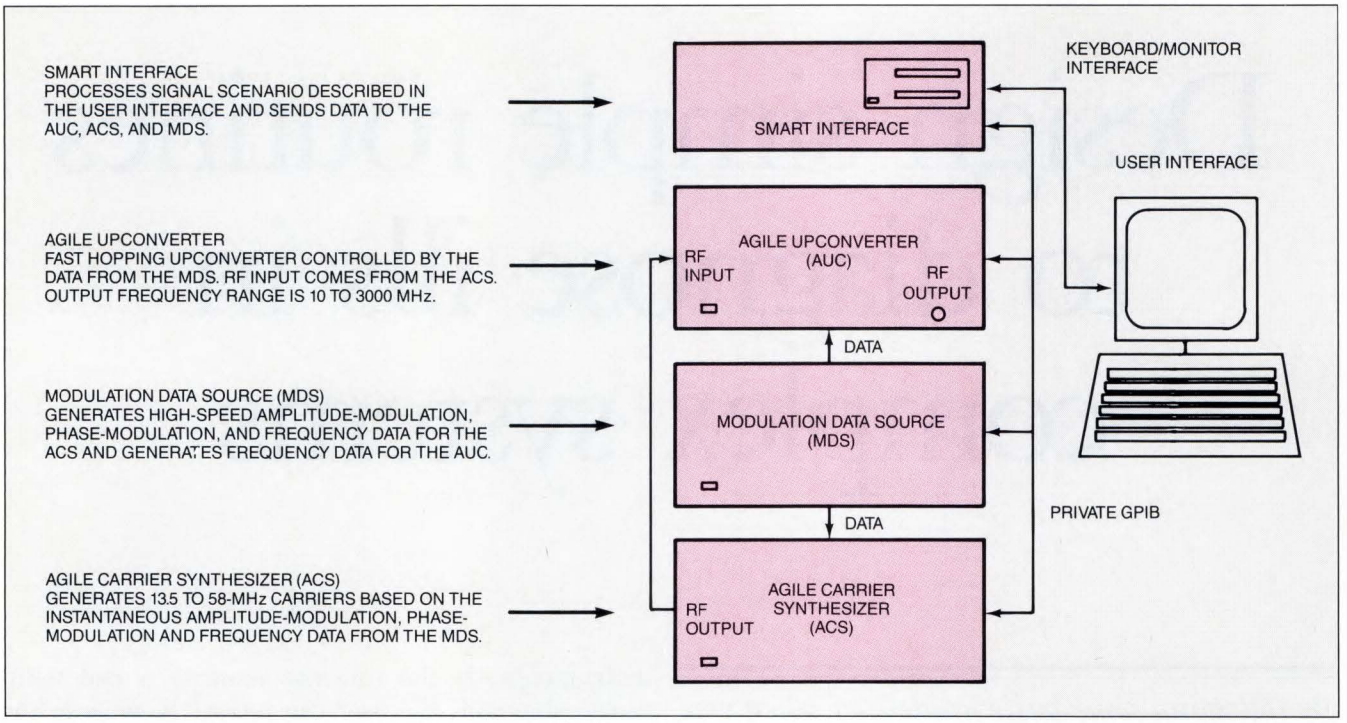


Fig 1—You can write diagnostic routines for any system or module. *The 200 diagnostic routines included in the FASS system, for example, evaluate the system's 8100 electrical parts on 40 assemblies.*

normal functions and diagnostic routines through its user interface.

The degree of detail that the programs provide to describe system failures is another vital design consideration. As shown in **Table 1,** different users need different fault-isolation or resolution capabilities. You can design programs that meet both high- and low-resolution needs by incorporating a hierarchical structure in your design **(Fig 2).** With this hierarchical test format, users can select a higher level of resolution if they need to delve deeper into the problems.

To develop routines that can diagnose specific faults and prescribe appropriate solutions, you must include the same troubleshooting skills that experienced technicians use to debug an instrument without any diagnostic programs. When testing prototypes, experts set up various situations to detect faults in the instrument under test. Experts can then use the information they

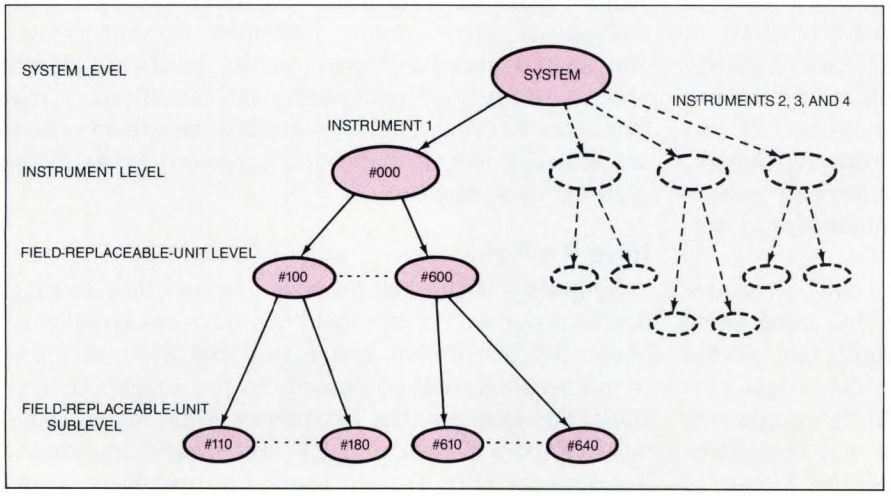


Fig 2—By setting up a system hierarchy, *you can create diagnostic routines that provide as much—or as little—resolution as is necessary. You can access the test hierarchy at any level; the lower the level, the greater the detail that the test provides.*

TABLE 1—RESOLUTION REQUIREMENTS

DEGREE OF RESOLUTION	SERVICE TECHNICIANS	MANUFACTURERS	R&D SPECIALISTS	CUSTOMERS
LOW RESOLUTION	QUICK ON-SITE MODULE REPLACEMENT TO REDUCE SYSTEM DOWNTIME	GO/NO-GO VERIFICATION PRIOR TO SHIPMENT	GO/NO-GO VERIFICATION AFTER MECHANICAL AND ELECTRICAL STRESS TESTS	GO/NO-GO VERIFICATION READ OVER GPIB OR DISPLAYED ON FRONT-PANEL LEDs
HIGH RESOLUTION	TROUBLESHOOTING DURING BENCH REPAIR TO ACHIEVE LOW-COST REPAIR	TROUBLESHOOTING, TRACKING DEFECTS, FINDING FAILURES DURING INSTRUMENT "BURN-IN." RESULTS READ OVER GPIB	DEBUGGING PROTOTYPE INSTRUMENTS, UNCOVERING DESIGN PROBLEMS BY USING DIAGNOSTICS WHILE STRESSING PROTOTYPES	TROUBLESHOOTING DURING BENCH REPAIR TO ACHIEVE LOW-COST REPAIR

NOTES:
1. LOW RESOLUTION DIAGNOSTICS INDICATE A FAILURE ON AN INSTRUMENT OR A FIELD-REPLACEABLE UNIT.
2. HIGH RESOLUTION DIAGNOSTICS INDICATE A SPECIFIC FAILURE ON A SINGLE FIELD-REPLACEABLE UNIT WITHIN AN INSTRUMENT.

gathered from these tests to identify similar symptoms in actual instruments or systems in the field.

You must, in effect, code an expert's thought process into your diagnostic firmware so the routines can use the results of several hypothetical tests to evaluate each subsystem of the instrument under test. The programs should analyze the data that the diagnostic routines generate and make conclusions, rather than simply offering test results that the engineer or technician must then analyze. A diagnostic routine should also identify the path of reasoning it took to arrive at the conclusion so the user can analyze the problem and, if necessary, perform hands-on troubleshooting.

The programmable microwave upconverter in **Fig 3**, which is a simple model of the Agile Upconverter in the FASS system, illustrates this logical evaluation

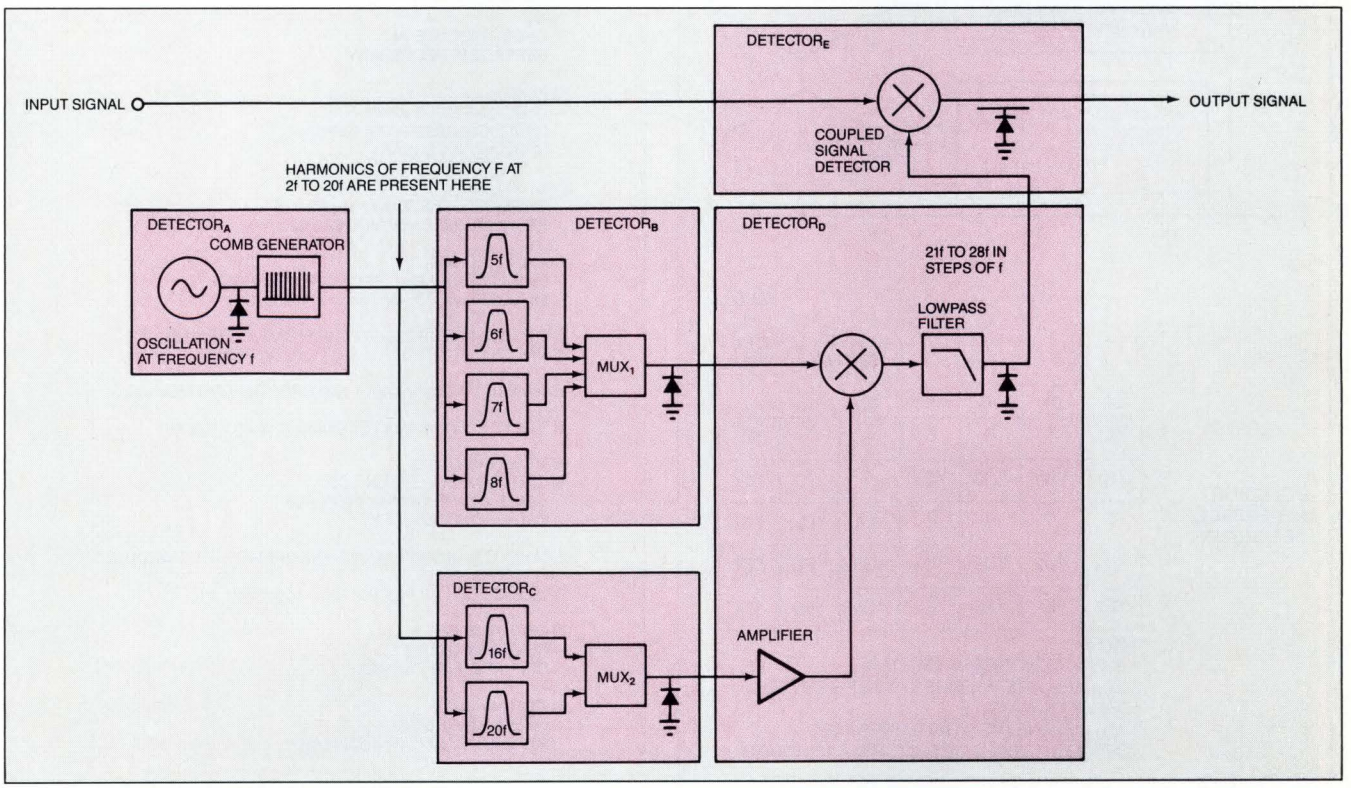
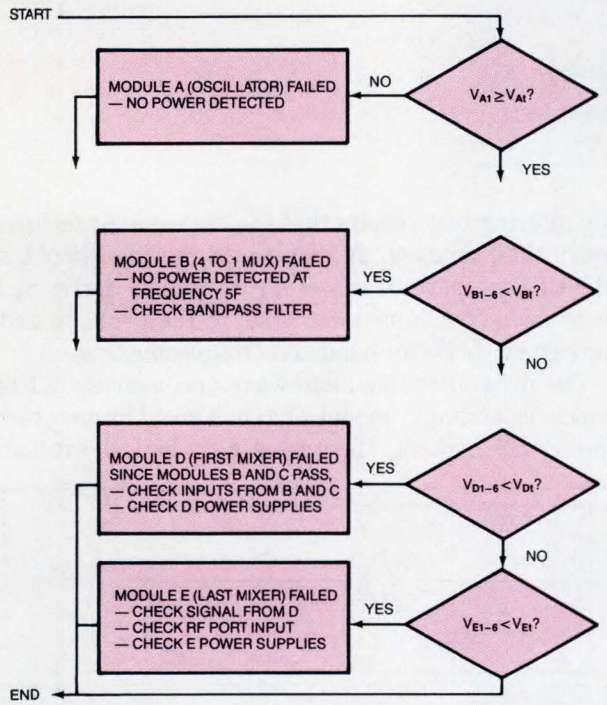


Fig 3—Five analog RF detectors *in this programmable microwave upconverter subsystem combine with an A/D converter and a microprocessor to monitor internal nodes. Detector* **(a)** *measures the oscillator power; detectors* **(b)** *and* **(c)** *measure the output voltages from the MUXes. Detector* **(d)** *reads the power level of the upconverted signal, and* **(e)** *measures the output signal power. (The A/D converter and the microprocessor, which controls the MUXes, aren't shown.)*

Diagnostic routines should contain the knowledge and intuition of a skilled troubleshooter.

process. The upconverter is an analog subsystem that includes several mixers, filters, analog switches, an oscillator, and five detectors, which are essentially hardware hooks for the diagnostic routines. You can use the five analog RF detectors, A through E, in your program to monitor internal signals. You can use an A/D converter with a microprocessor to read the analog voltages for diagnostic purposes. The flowchart in **Fig 4** shows the upconverter's troubleshooting procedure.

First, the diagnostic routines analyze the measurements taken by the detectors. The routines then display their conclusions and their deductive-reasoning process. You can use an external controller to run the routines for each of the instruments in the FASS system. This controller sends the commands to the instru-



DETECTOR REFERENCE DESIGNATOR	MUX_1 SETTING 00	01	10	11	MUX_2 SETTING 00	01	PASS/FAIL THRESHOLD
A	V_{A1}	X	X	X	X	X	V_{At}
B	V_{B1}	V_{B2}	V_{B3}	V_{B4}	X	X	V_{Bt}
C	X	X	X	X	V_{C1}	V_{C2}	V_{Ct}
D	V_{D1}	V_{D2}	V_{D3}	V_{D4}	V_{D5}	V_{D6}	V_{Dt}
E	V_{E1}	V_{E2}	V_{E3}	V_{E4}	V_{E5}	V_{E6}	V_{Et}

NOTES:
1. X IS A "DON'T-CARE" VOLTAGE.
2. V_{A1}–V_{E6} ARE VOLTAGES AT THE 5 DETECTORS, A THROUGH E.
3. V_{At}–V_{Et} ARE PASS/FAIL THRESHOLD VOLTAGES AT THE 5 DETECTORS, A THROUGH E.

Fig 4—Diagnostic routines isolate problems *by recognizing how instrument failures affect voltages in a matrix. This voltage matrix is a function of the different MUX settings.*

```
SAMPLE AI DATABASE FILE CONTAINING
KNOWN FAILING TEST SCENARIOS

(100)
—CHECK MODULE #1.
  REPLACE IF NECESSARY.

(200)
—CHECK MODULE #2.
  REPLACE IF NECESSARY.

(300)
—CHECK MODULE #3.
  REPLACE IF NECESSARY.

(400)
—CHECK MODULE #4.
  REPLACE IF NECESSARY.

(200, 400)
—CHECK MODULE #2–#4 FOR
  CABLE CONNECTIVITY. REPLACE
  CABLE IF NECESSARY.

(200, 300, 400)
—CHECK CLOCKS TO MODULE #2. IF
  PRESENT REPLACE MODULE #2.

(100, 200, 300, 400)
—CHECK MODULE #1 BECAUSE TESTS ON
  MODULES #2, #3, AND #4 ARE FAILING.

SAMPLING FAILURES AND THEIR CAUSES FOUND,
USING THE AI PROGRAM AND THE DATABASE.

EXAMPLE 1—DEPENDENT FAILURES ON TWO MODULES

RESULTS FOR FAILING TESTS 200, 220, 230, 400, 410

MATCH #1=200, 400
—CHECK MODULE #2–#4 FOR
  CABLE CONNECTIVITY. REPLACE
  CABLE IF NECESSARY.

EXAMPLE 2—INDEPENDENT FAILURES ON TWO MODULES

RESULTS FOR FAILING TESTS 200, 220, 300, 310

MATCH #1=200
—CHECK MODULE #2.
  REPLACE IF NECESSARY.

MATCH #2=300
—CHECK MODULE #3.
  REPLACE CABLE IF NECESSARY.
```

Fig 5—To isolate the cause of a system failure, *the diagnostic routines match failing-test scenarios contained in the database to the actual results of the diagnostic tests.*

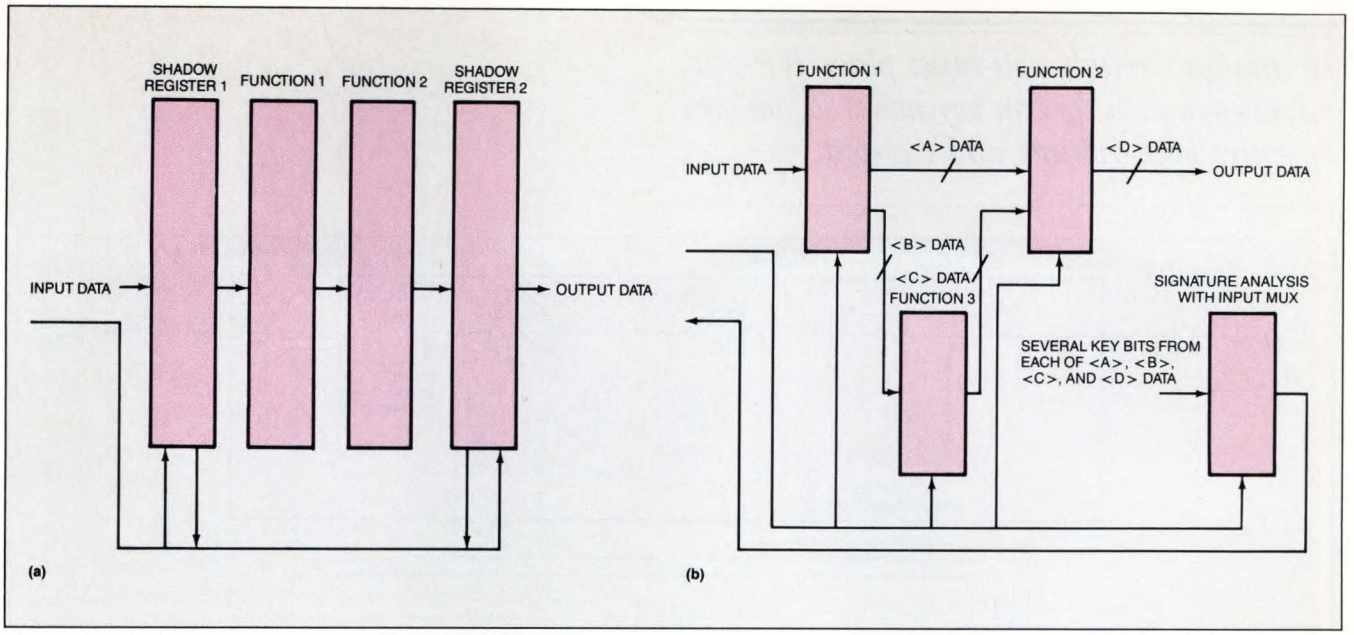


Fig 6—By choosing diagnostic points *either in series* **(a)** *or in parallel* **(b)** *with key digital pathways, you can easily obtain information on the status of a system.*

ment or module under test and receives the results over the GPIB.

The user needs only three commands to run the diagnostic routines in the FASS and to obtain pass/fail status, test results, and failing test numbers of the instrument under test. The first command, "DIAG:TEST? (test number)," runs the test that you specify. The routine returns a 0 to the controller if the test passes and a 1 if the test fails. The second command, "DIAG:TRES?" (DIAGnostic Test RESult), lets you retrieve a failure message. The failure message is a character string containing carriage returns and line feeds that describes the results of the tests. The final command, "DIAG:FLIS?" (DIAGnostic Failure LISt), returns a list of all the failing tests for the previous "DIAG:TEST? (test number)." The "DIAG:FLIS?" command lets users record the failing tests.

The system-level intelligence is in the form of a database that contains failing-test scenarios and an AI-like (artificial intelligence) program **(Fig 5).** The AI-like program finds the best matches between the actual failing tests and the multiple failing-test scenarios stored in the database. The diagnostic program then selects from the database all the possible causes of the failure that correlate to the failing-test scenarios. If you code your database properly, the routines will report a single fault if the failures are caused by related events. Conversely, the routines will report numerous, independent faults if the causes of the failures are unrelated. You should write the failing-test-scenario database to a text file so you can update it when you discover new failure scenarios. You can then provide users and service technicians with updated files.

Get involved in the hardware design

To ensure that your diagnostic routines can perform the proper tests on a system, you should participate in the hardware design process. Consult with the design teams and evaluate the short-term cost of adding special diagnostic circuitry and the long-term cost of supporting a product that doesn't have diagnostic capabilities. Hardware designers can easily add different types of circuitry for digital and analog circuits to incorporate diagnostic capabilities into the hardware.

For digital circuits, designers can place diagnostic points in series or in parallel with key digital pathways **(Fig 6).** For series placement, the circuit designers can set up the diagnostic mode by electrically inserting test circuitry into the circuit paths that the instrument uses during normal operation.

One method of inserting test circuitry is to use a "shadow register." This register is a latch that hardware designers place in the path of a digital circuit and use as either a normal latch or a serial latch. The test circuitry can either read from or write to (serially) the latch to interrupt the normal data path for diagnostic purposes. Digital-system designers commonly use this technique because it's easy to implement.

If the diagnostic test points are placed in parallel with the digital paths, your diagnostic routines will probe key locations in the circuit and feed the results into a signature analyzer that the circuit designers build into the subsystems. The signature analyzer performs a CRC (cyclical redundancy check—a method of signature analysis) on one high-speed digital line at a time. The CRC process is similar to using an external signature analyzer with a start and a stop bit to probe many different points in an area of circuitry and isolate a bad section. Built-in circuitry, however, is faster, easier to use, and more reliable than external test hardware.

Digital diagnostic hardware that's connected in parallel is more complicated than the series hardware, but the parallel type provides better fault isolation.

In analog circuits, you must place RF and microwave detectors on key nodes so you can measure both voltage and current.

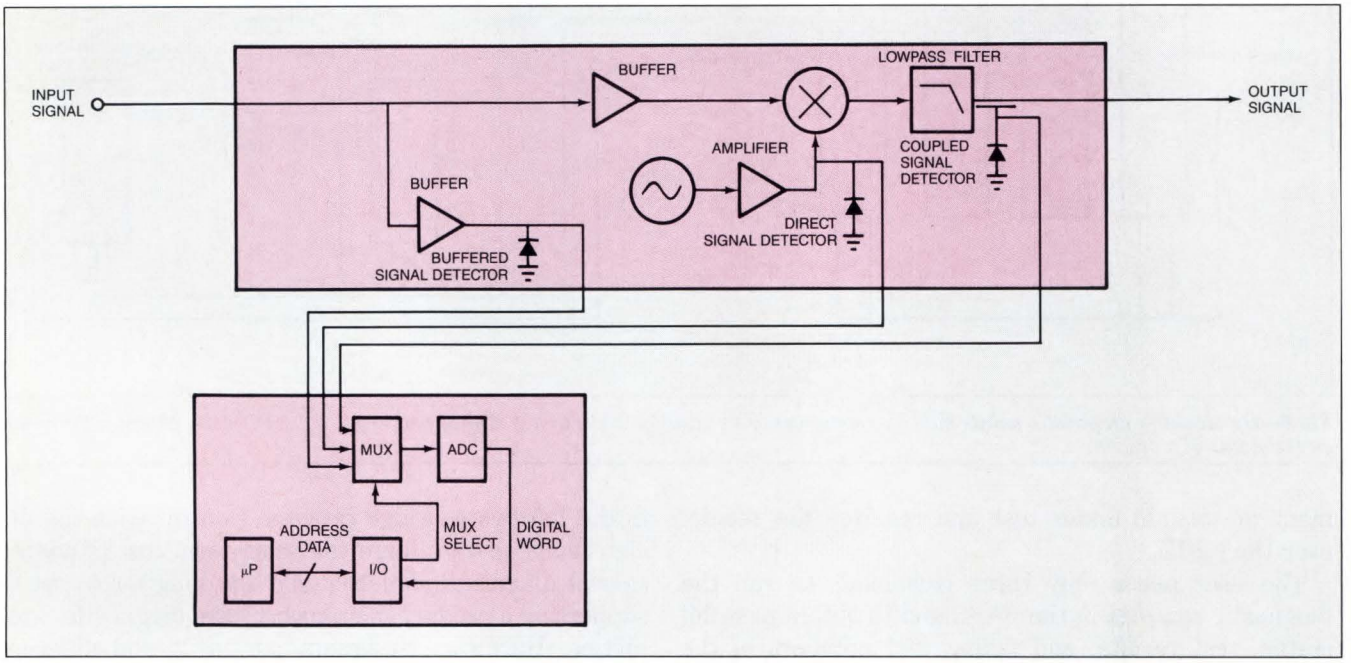


Fig 7—The microprocessor selects a detector *by using the analog MUX, the A/D converter reads the detector value, and the processor compares the voltage to the expected value. The diagnostic program isolates faults by determining which detectors fail and under what conditions they fail.*

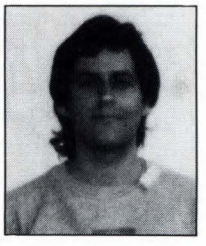
Because this technique lets you directly monitor normal high-speed functions, you can leverage the parallel approach during the prototype testing phase of the design cycle to find marginal design problems or to test the limits of the design.

Analog circuits need detectors, too

For analog circuitry, you should make sure that the circuit contains RF and microwave detectors. **Fig 7** shows three methods of incorporating detectors: the buffered, direct, and coupled signal-detector schemes. Designers can place the detectors on key nodes in an analog system's modules. By detecting signal power in the form of a dc voltage, the detectors (under the control of the diagnostic routine) can evaluate an instrument's module. If you write diagnostic routines properly, they can measure signals derived from coupled, buffered, or direct locations in either the circuit or module under test. Other detector schemes exist, but these three types are particularly noteworthy.

The cost of implementing any of these detection schemes is greatly affected by the complexity of the circuitry, the signal's frequency and power, and the desired detector performance. You should use the coupled signal-detection technique when signal frequencies are above a couple gigahertz. This method of detection has little effect on the signal path's SWR. However, detectors for the microwave frequency range are expensive, and printed-circuit layout constraints increase the overall cost of the design. If the frequency range is less than about 100 MHz, simply buffering the signal under test may work well because SWR problems are less prominent than in higher frequency applications, and buffers are relatively inexpensive. Finally, you can perform direct detection by placing the detector in series with the signal under test. You should use the direct detection scheme if cost is a key concern or if relatively large changes in the signal level (as a function of frequency) won't significantly impair the circuits performance. EDN

Author's biography



Matt Klein is an R&D engineer with Hewlett-Packard. He is responsible for designing firmware and diagnostic routines as well as RF and microwave test software. Before starting his 5-year tenure with HP, he earned his engineering degree at Case Western Reserve University. In his spare time, Matt enjoys cooking, computer programming, skiing, and designing hi-fi speakers.

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*RS4004	Digital Pattern Generator	45,500	9,000
*RS432W/OPTS	Gen w/2ea opt 2/1ea opt 5,7,9,11,13	12,160	2,400
*RS660	Word Generator/Timing Simulator	7,700	750
*RS680	Word Generator	17,000	750

SOPHIA COMPUTER SYSTEMS

*SA700-xx	8/16 Bit Emulators	$ 9,995	$ 700
*SA710-xx	8/16 Bit Emulators	7,995	700

TEKTRONIX

1200C02	GPIB Comm Package for 1240	$ 850	$ 450
1240	Logic Analyzer	4,500	2,500
1240-D21	8Ch/50MHz Data Acquisition Card	3,700	1,800
1241	Logic Analyzer, Color	6,000	3,595
12RMxx	Mnemonics ROM Packs	400	250
12RS01	8K RAM Pack for 1240	300	125
4105	Color Graphics CRT Terminal	3,995	275
7D02/1/3	Logic Analyzer	8,450	1,500

MODEL	DESCRIPTION	LIST PRICE	SALE PRICE
8300Exx	Emulation Control Boards	$ **	$ 1,000
8300Pxx	Prototype Control Probe	**	1,000
8540/1/2/3	Integration Unit/TTA/Comm Package	14,890	2,500
8540/1/3/15	Integration Unit/TTA/Comm Package	10,190	2,500
8540F26	512K Emulation RAM	4,800	2,400
8560F06	512K Memory Expansion/8560	4,900	500
8561	Multi-user System/FP/512K	16,400	3,000
8561/2/5/8	Multi-user Model/FP/512K	18,900	3,000
91A08	100MHz Data Acquisition Module	3,255	1,595
91A24	Data Acquisition Module	2,890	1,495
91A32	25MHz Data Acquisition Module	2,070	1,525
91AE24	Data Acquisition Module	2,950	1,950
91P16	25MHz Pattern Generator Module	2,840	1,900
91S16	50MHz 16Ch Pattern Generator	4,200	2,100
DAS9129	Color Digital Analysis System	13,995	3,000
DAS9129+	Color DAS/DC100/2PS/GPIB/RS232	13,195	3,000
P6452	Data Acquisition Probe	730	450
P6455	TTL/mod Pattern Gen Probe	575	150
P6464	Pattern Generator Probe	1,350	500
P6465	Pattern Generator 8Ch 50MHz	1,680	500
PM1xx	Microprocessor Personality Modules	1,800	300

ZAX

178-68000	10MHz PC-Based Emulator	$ 8,500	$ 5,000
178-8048	8048/49 Emulator	5,500	2,795
178-8086/88	8086/88 PC-Based Emulator	8,500	4,250
278-6809	6809 PC-Based Emulator	5,500	3,300
278-8085	8085 PC-Based Emulator	4,995	1,695
278-V30	V30 PC-Based Emulator	8,995	6,000
278-Z80H	Z80 PC-Based Emulator	5,500	2,795
378-8051	8051/52 PC-Based Emulator	5,995	4,700
378-8086	8086 PC-Based Emulator	8,500	5,100
378-V50	NEC V50 PC-Based Emulator	9,450	6,000
ZICExx	PC Interface S/W for ICD	500	300

Price subject to change without notice. Equipment subject to availability.
* No Warranty ** List Prices vary based on configuration.

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☐ I have rental needs. Please send me, ER's full line multi-reference rental catalog. It includes Workstations, General Purpose, RF/Microwave, Digital Design, Data Products, Telecommunications and Data Acquisition Test Equipment.

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BENEFITS OF RENTING TEST INSTRUMENTATION

Protection Against Obsolescence

Shorter product life cycles and rapidly advancing technology means the state-of-the-art instrument of today is "old-hat" tomorrow. Let us take the risk out of buying the newest equipment ... if it gets outdated, just demand the latest version.

Budget Restraints

Renting test equipment softens the impact on tight budgets. In today's competitive business environment, everyone is trying to get the most "bang" for their buck... rentals conserve capital and stretch your dollars.

Prompt Delivery

With the largest inventory of any company in the business plus 11 computerized local inventory/service centers, we provide equipment immediately for those unforseen demands caused by breakdown or short term projects... when you need it "yesterday".

Short Term Requirements

Special projects or short term needs demanding specific equipment for defined periods are best handled through our short term rentals. Why pay for more or commit to more than you need?

Maintenance Free

No need to worry about the time and money needed to maintain highly sophisticated equipment. If it needs tuning, repair or replacement... we take care of it.

Quality Performance

Our QC standards are tough! Our nationwide network of calibration labs ensures that all equipment works when you turn it on. Our equipment is traceable to the National Institute of Standards & Technology... we also conform to MIL-STD-45662A.

AFFORDABLE FINANCIAL ALTERNATIVES

- **Straight Rentals**
- **Rentals with purchase option**
- **Finance and operating lease**
- **Flexible finance terms on purchase of used gear**

We'll work directly with you to provide you the best in electronics--Affordably.

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FOR SALE...

APPLIED MICROSYSTEMS

MODEL	DESCRIPTION	LIST PRICE	SALE PRICE
EM-18xx	8 Bit Diagnostic Emulator Series	$ **	$ 1,200
ES-68000/8B	68000/08 Emulator Control Board	3,550	2,000
ES-68000B	68000 Emulator Control Board	3,550	1,300
ES-68000P	10MHz 68000 Emulator Probe	3,195	1,000
ES-68008B	68008 Emulator Control Board	3,550	1,500
ES-68008P	10MHz 68008 Emulator Probe	3,195	1,100
ES-68010B	68010 Emulator Control Board	3,550	1,500
ES-68010P	10MHz 68010 Emulator Probe	3,195	1,100
ES-68020B	68020 Emulator Control Board	3,550	1,875
ES-68020P	16MHz 68020 Emulator Probe	3,195	1,500
ES-80186P	80186 Emulator Probe	4,095	1,500
ES-80188P	80188 Emulator Probe	3,195	1,500
ES-8086B	8086/88/186/188 Emulator Ctrl Bd	3,550	2,000
ES-8086P-86	10MHz 8086 Emulator Probe	3,195	1,500
ES-8086P-88	10MHz 8088 Emulator Probe	3,195	1,500
ES-GPB	Gene-Probe	1,995	1,200
ES-LA	Logic State Analyzer	895	495
ES-RO-128	128K RAM Overlay	3,800	2,200
ES-RO-32	32K RAM Overlay	1,500	550
ES-RO-64	64K RAM Overlay	2,500	1,200
ES1800SY100	Satellite Emulator Mainframe	4,350	2,895
PC-ES	PC Driver Software for ES1800	500	225

DATA I/O

29B-20700	29B Programmer/128K/SRC/CRC	$ 4,495	$ 2,100
29B-X0600	29B Programmer/64K/SRC/CRC	4,495	1,500
303A-001	Signetics/TI IFL Adaptor	495	150
303A-006	TI Programmer/Test Adaptor	395	100
303A-007	Harris CMOS Prog/Test Adaptor	495	325
303A-009	CMOS Adaptor	395	125
303A-011B	PLCC/SOIC Generic Module	1,195	1,050
303A-ECL+	ECL Programmer/Test Adaptor	795	675
351A-xxx	PROM Programmer Adaptors	175	100
950-0059	Unipak II	2,575	700
950-0077	Gang Pak	1,750	1,300
950-0099	Unipak	2,200	600
990-0003-01	22A PROM Programmer	4,320	600
990-0004-01	22B PROM Programmer	2,595	600
990-0029-67	System 29/64K Memory/SRC/CRC	4,575	600
990-0121-17	Model 121A Gang Programmer	10,500	2,000
MODEL21A	Personal EPROM Programmer	1,450	500
MODEL22A	Model 22A PROM Programmer	3,795	1,200
MODEL22B	MOS Device Programmer	1,995	895
MODEL280	64K Gang Programmer	1,995	1,200
MODEL60	64K RAM Logic Programmer	3,485	1,200
USITE-OPT1P	Pin Driver Card	435	375
USITE-OPT4	Chipsite SOIC/PLCC Module	3,000	2,800
USITE40/2/3	Usite w/512K Dual Floppys	11,995	10,000

GOULD/BIOMATION

K-101D	Logic Analyzer	$ 19,750	$ 4,000
K-102D	Logic Analyzer	15,750	3,000
K-115	Logic Analyzer Mainframe 32/64 Ch	5,505	2,000
K-20	Logic Analyzer 24 Channel	2,650	1,000
K-205-048	48Ch Hi-Speed Logic Analyzer	17,750	5,500
K-205-148	48Ch Hi-Speed Logic Analyzer w/Disk	19,750	6,000
K-450	Logic Analyzer Mainframe	8,550	4,000
K-450-248	64Ch Logic Analyzer w/Disk Drive	10,800	5,000
K-500D	Logic Analyzer 8Ch 500MHz	17,500	10,000
RTE-68000	RTE Disassembler	700	150
RTE-8085A	RTE Disassembler 8085A	700	150
RTE-Z80B	RTE Disassembler Z80B	700	150

HEWLETT PACKARD

10269A	Probe Interface for 1630	$ 460	$ 295
10269A-xx	Personality Modules	**	250
10269B	Probe Interface for 1630G	460	150
103xx	Preprocessors for 1630D/G	**	350
1630D	43 Channel Logic Analyzer	10,800	5,000
1630G	65 Channel Logic Analyer	12,400	5,500
1631D	Logic Analyzer	13,300	7,000
64001S/05D	15MB Winchester Disk	3,050	750
64001S/05H	20MB Winchester Disk	2,390	1,000
64100B/41	Logic Development System	17,920	3,900
64110B/034	Logic Development System	11,350	3,350
64155A	16 Bit Memory Control Board	1,650	500
64161A	128K Memory Board	3,755	1,900
64162A	64K Memory Board	2,580	1,500
64240/243AA	68000 Emulator 12MHz w/asm+linkr	7,000	4,000
64240/243AB	68000 Emulator 12MHz w/asm+linkr	7,200	4,000
64260A/264	8051 Emulator System w/asm+linkr	6,400	1,000
642xx	Emulator System w/asm+linker	**	500
64300A	8 Bit Logic Analyzer	2,130	200
64302A	48 Channel Internal Analyzer	2,945	1,500
64304A	Emulation Bus Preprocessor	1,745	750
64310A/SF	Software Performance Analyzer	3,510	500
64331A	68000 High Level Soft Analyzer	3,520	500
64332A	8086 High Level Soft Analyzer	3,520	500
64600S/F	8 Channel Timing Logic Analyzer	6,880	1000
64620S/011	60Ch State Analyzer w/Overview	7,920	1500
64630S/011	60 Channel GP Probe Kit	4,260	500
6465xx	Microprocessor Interfaces	**	500
647xx	PC-Based Emulators w/asm+linker	**	10,000
8016A	Word Generator 9 x 32 Bit	11,300	3,500
8018A/1	Serial Data Generator	6,415	3,000
8084A	Word Generator	4,280	1,800
8170A/1	Logic Patter Generator 32K Bit	8,780	2,195
8180A	Data Generator	17,800	8,900
8181A	Data Generator Extender	10,500	5,800
8182A/1	Data Analyzer w/3 Option 1	31,500	9,800

HITACHI

*H180AS01	64180 Emulator	$ 6,000	$ 4,000
*H180ASE02	64180 Emulator	10,495	5,000
H680SM01S	256K Memory Expansion Board	1,500	700

INTEL

*DX-225AFDMF	New Version MDS-235 Mainframe	$ 10,505	$ 750
*DX-286AFDMF	New Version MDS-286FD Mainframe	16,905	750
III-110	8MHz 186/188 Emulator w/SW	7,995	2,995
III-110/IBM	8MHz 186/188 Emulator w/SW	7,995	3,995
III-210	6MHz 80286 Emulator Series IV w/SW	11,995	2,995
III-210/IBM	6MHz 80286 Emulator PC-XT	11,995	3,995
III-211	8MHz 80286 I²ICE Series IV	11,995	3,995
III-211/IBM	8MHz 80286 I²ICE IBM PC-XT/AT	9,995	4,995
III-707	128K I²ICE Emulation RAM Memory	3,950	2,000
IMDX-431A	Series IV MDS	24,900	1,000
IMDX-441A	Enhanced Series IV MDS	28,900	1,000
IMDX-456	IMDX Interface Card/Series IV	2,000	800
IMDX-720A	New MDS-720	6,995	750
IPAT86PC	Performance Analysis Tool for I²ICE	4,995	2,000
IPDS	Intel Personal Development System	7,000	700
IPDS-130	Add-on Disk Drive for PDS	995	200
IPDSEMV51	8051 Emulation Vehicle	2,995	350
IPDSEMV51A	8051 Emulation Vehicle	2,995	400
IUP-201U	UPP with V1.4 Software	2,755	250

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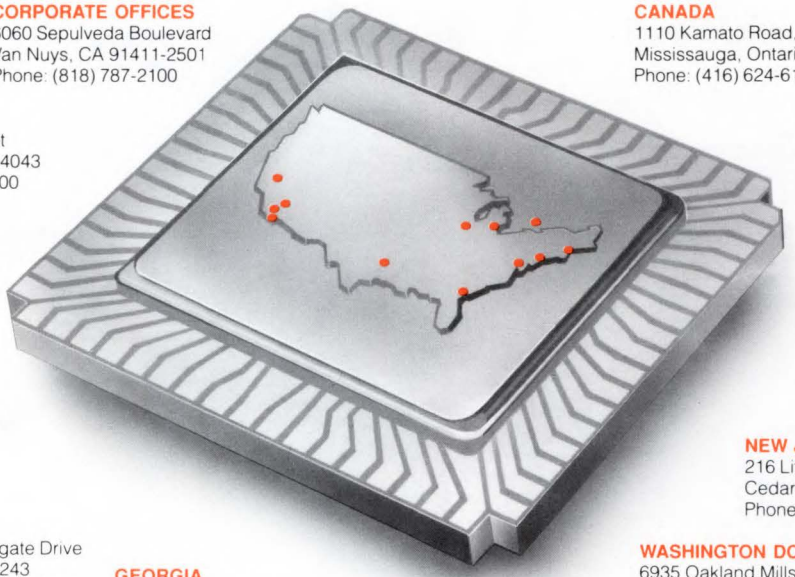

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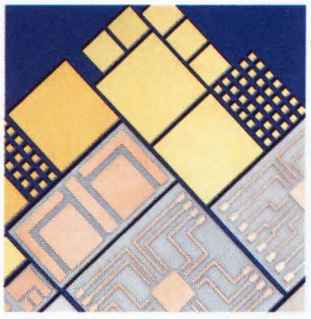
BEAT THE HEAT

with TOKIN AℓN SUBSTRATES

Tokin has developed a film metallization technique for creating AℓN heat sinks with outstanding insulation and heat dissipation properties.

Designing a transistor without the insulation and heat dissipation properties that let you take full advantage of its capabilities is like building a sports car without a cooling system.



That's why we want you to know what TOKIN's AℓN (Aluminum Nitride) substrate material has to offer.

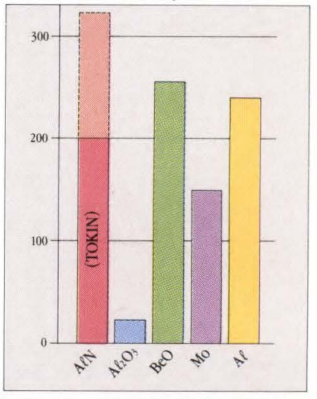
- Thermal conductivity eight times higher than alumina
- Dielectric constant, insulation features, and mechanical strength as high as alumina
- Thermal expansion coefficient comparable to silicon
- Available in 120, 160 and 200 W/mk (RT) thermal conductivity

One note worthy application for AℓN substrate is TOKIN's own line of Static Induction Transistors (SIT). By using SIT in combination with AℓN heat sinks, we are to able provide power levels of 50 W to 3 KW and breakdown voltages ranging to 1500 V. SIT power modules have been used to manufacture 2 MHz, 2 KW RF induction heating generators with a 70% reduction in size and 80% efficiency. And it couldn't be done without AℓN substrate.

So don't leave the job half done. Discover how TOKIN's AℓN can give a dramatic boost to transistors or power circuits (including those for auto ignitions).

It's truly an idea worth celebrating.

Thermal conductivity (W/mK) RT



AℓN Properties		TOKIN AℓN			$AℓN_2O_3$ (96.0%)	BeO (99.5%)
		T-120	T-160	T-200		
Density	g/cm³	3.2			3.8	2.9
Thermal conductivity	W/mK (RT)	120	160	200	20	260
Thermal expansion coefficient	(×10⁻⁶/°C) (RT~400°C)	4.3			6.7	7.5
Dielectric strength	KV/mm (RT)	15			15	10
Volume resistivity	Ω-cm (RT)	$>10^{13}$			$>10^{13}$	$>10^{13}$
Dielectric constant	(1 MHz. RT)	8.9			8.9	6.7
Dielectric loss	(1 MHz. RT)	3			4	3

TOKIN

Tokin Corporation
Hazama Bldg., 5-8, Kita-Aoyama 2-chome, Minato-ku, Tokyo 107, Japan
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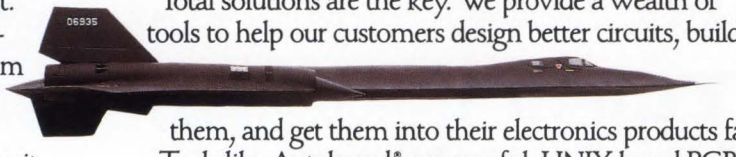
WE JUST INCREASED

In the electronics industry, if you don't get your product to market first, you might as well get there last.

That's why more electronics manufacturers, from makers of sound systems to makers of aerospace assemblies and printed circuit boards, are turning to Prime. Our ability to integrate design and engineering–to get teams of people working simultaneously on a single project–helps our customers minimize development time, and get their ideas to market first.



Total solutions are the key. We provide a wealth of tools to help our customers design better circuits, build them, and get them into their electronics products fast.

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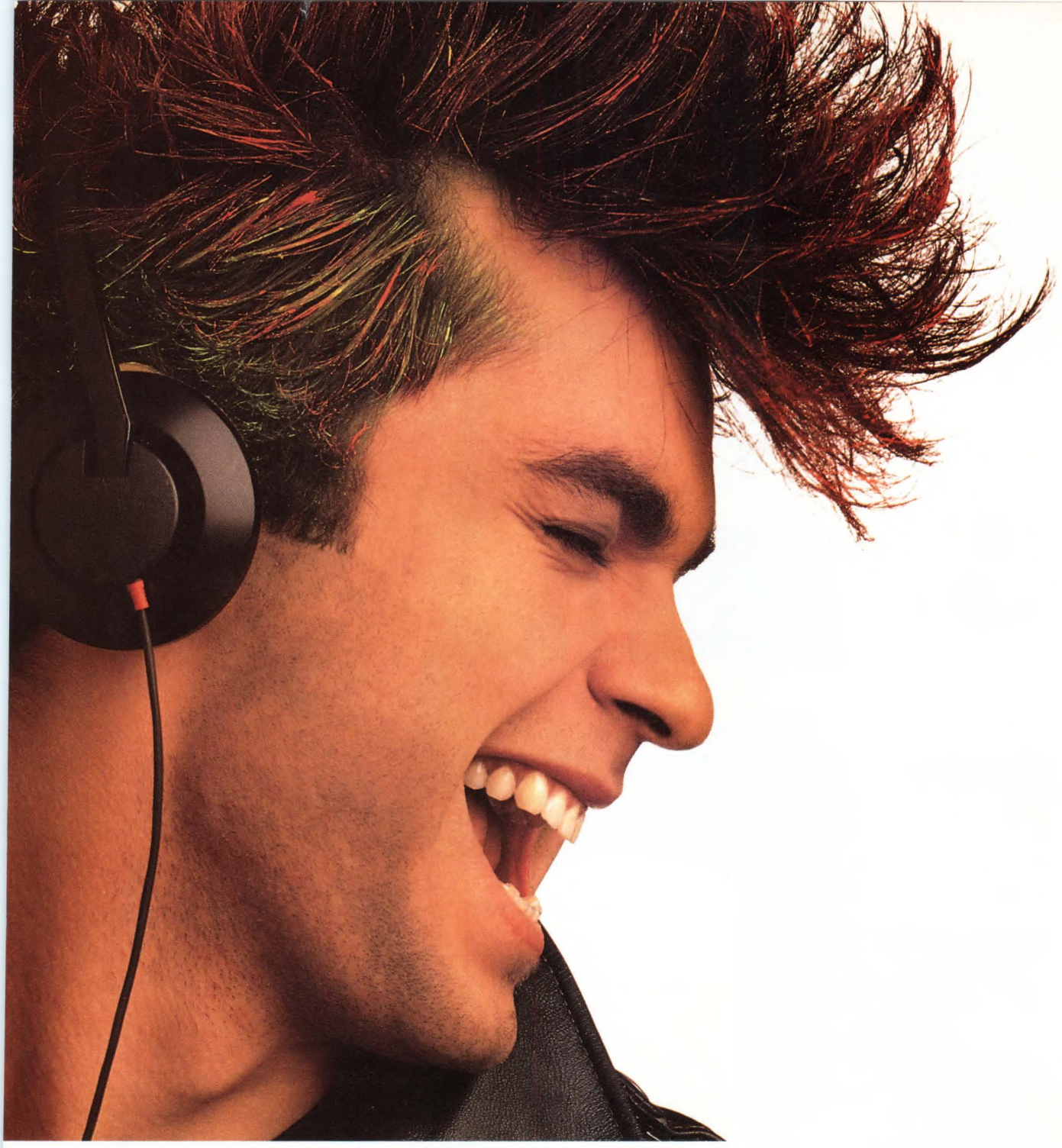
And Schematic Design, a powerful electronics circuit design system that comes with a comprehensive library



THE SPEED OF SOUND.

of thousands of parts and simulation models.

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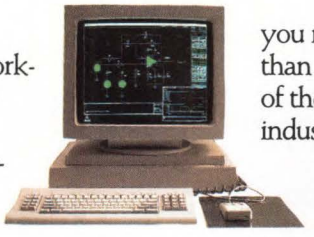
And CADDS® 4X software, one of the most powerful 3D modeling packages available. It will facilitate the packaging of your electronics products quickly and easily.



The list goes on. In fact, nobody offers you more CAE/CAD/CAM solutions than Prime. Maybe that's why we're one of the largest suppliers to the electronics industry.

For more information on how we help our customers get to market first, call 1-800-343-2540 (in Canada call 1-800-268-4700). Or write to us at Prime Computer Inc., 100 Crosby Dr., Bedford, Massachusetts 01730.

Prime®

CIRCLE NO 130

High performance filters off the shelf.

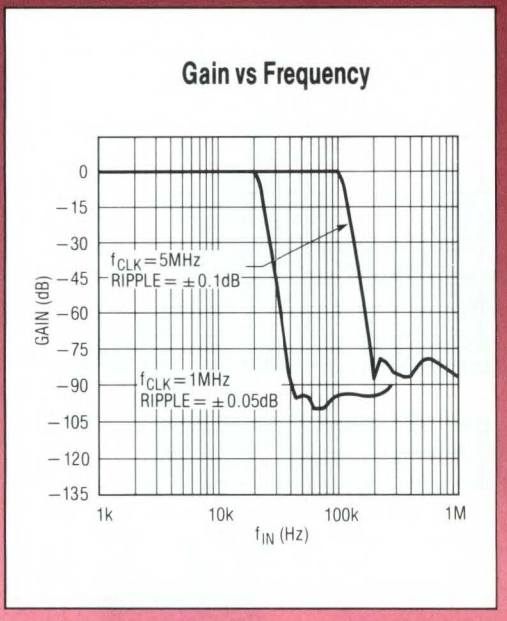
An exciting new series of accurate 8th order filters.

Take your pick. We have the performance low pass filter you want.

By the bin.

The LTC1064 makes a switched-capacitor filter competitive with the performance of active rc filters for the first time. Four independent high performance second order filter sections are in a single 24-pin DIP allowing an eighth order filter. This new filter has outstanding speed, with cutoff frequencies as high as 100kHz, as well as broad dynamic range, low noise, clock tunability, frequency and "Q" accuracy.

The LTC1064 uses external resistors to configure the filter. We make designs even easier with options that put these programming resistors on the chip. The result is a symphony of features: smaller package size, 14-pin DIP, increased speed, low noise, and guaranteed performance. Check out the classic of your choice: Cauer. Butterworth. Bessel. They're available now right off the shelf.



For volume applications, you can specify custom internal thin-film resistor arrays for your filter.

Typical applications for the LTC filters include: sonar/radar, ultrasound, telecom, process control, power supply monitoring, cellular telephones, satellite transceivers, and anti-aliasing filters for data acquisition.

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CIRCLE NO 131

EDITED BY CHARLES H SMALL

Debugger uses coprocessor socket

Noor S Khalsa
EG&G, Los Alamos, NM

The IBM PC debugger in **Fig 1** plugs into the PC's math-coprocessor socket. You can mount all the components in **Fig 1** on a chip carrier. The 8288 bus controller, IC_1, regenerates control signals from the processor's status signals, S_0, S_1, and S_2. The Reset LED, D_1, lights if Reset is active and holding the processor. The Clock status LED, D_3, indicates that the processor is receiving a toggling clock signal. The address-decode logic detects when the processor is doing a jump-on-reset to the PC's BIOS ROM. The Halt LED, D_2, latches on when the BIOS's power-on self test has detected a fatal error and halted the processor. EDN

To Vote For This Design, Circle No 746

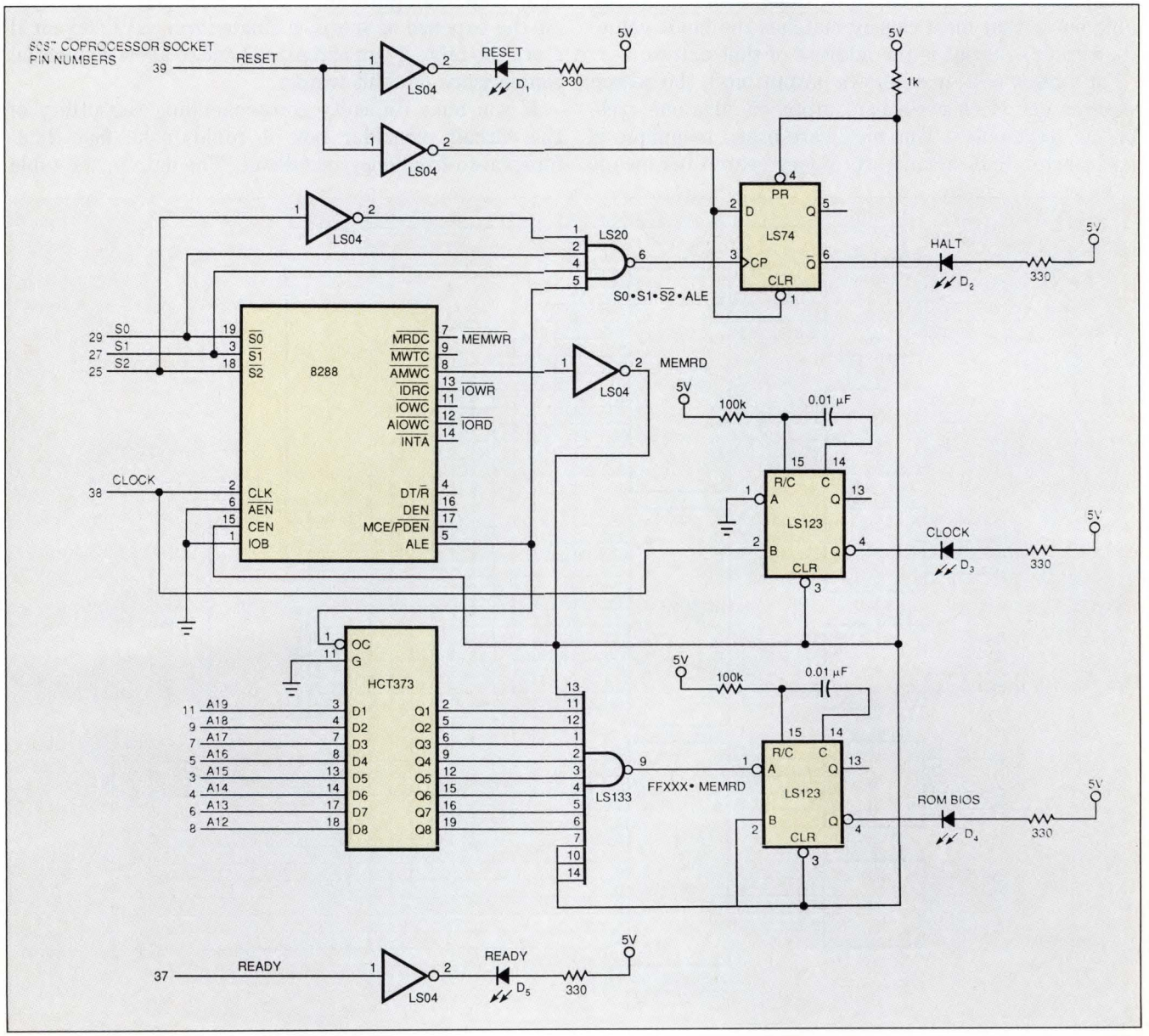

Fig 1—This simple debugging tool plugs *into the math-coprocessor socket of an IBM PC.*

Register performs binary search

James C Vandiver
UAH Research Institute, Huntsville, AL

You can team an AMD SAR2504 successive-approximation register (SAR) with a digital-comparator circuit to perform a fast and efficient binary search of an EPROM-based table. The circuit can also function as a content-addressable memory if the data are in numerical order. The circuit in **Fig 1**, when given an input value and a start pulse, performs successive approximations to the 24-bit input value until it finds the table entry that most closely matches the input value. The circuit's output is the address of that datum.

For a table of 2^n numbers (n output bits), the search requires one clock cycle per output bit plus one cycle for the start pulse. This hardware-based technique is much faster than a software binary search because it avoids the wasted time of loading data and instructions that a μP-based search would require. The 12-bit output word is available in both serial and parallel forms.

The circuit in **Fig 1** shows a table of 4096 24-bit numbers. You can easily scale the circuit to handle different table lengths and word widths by short cycling or cascading SARs and using different EPROMs. Substituting RAMs or EEPROMs for the EPROMs would let you change the table dynamically. For time-critical applications, you could cascade the comparators in a "tree" configuration to reduce propagation delays. At the expense of speed, a single large EPROM could store the table if you add extra logic to allow sequential comparisons on 8-bit words.

If you have difficulty comprehending the utility of this circuit, consider how it could make fast time-interval-to-frequency inversions. The data in the table

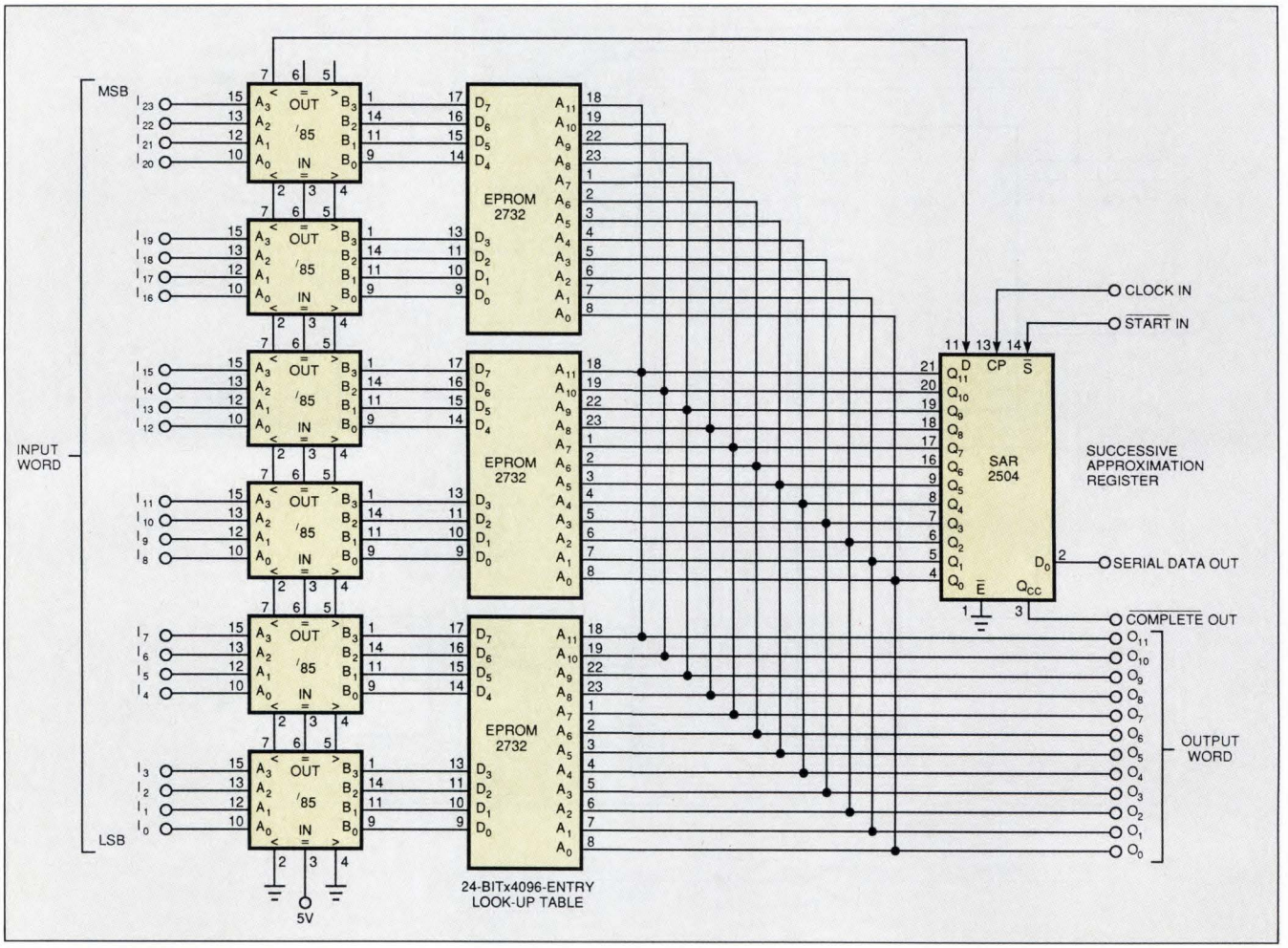

Fig 1—This successive-approximation circuit *performs a binary search for an n-bit number in n+1 clock cycles.*

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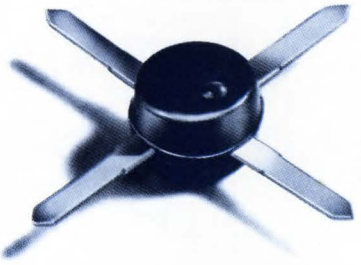

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MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

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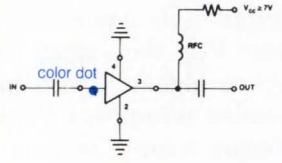

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would be time intervals, which would be compared to measured inputs; their addresses would be the corresponding frequencies. To load the table, you would calculate the inverse of the addresses, scale the inverse values over the expected range of inputs, and load them into the EPROM table. In operation, the circuit would find the nearest match to a given input interval in its table. The address of that datum in the table would then be, in this example, the corresponding frequency. EDN

To Vote For This Design, Circle No 747

Single shots reside in PLDs

Jim Honea
AGL Corp, Jacksonville, AR

By using three external components and three to five pins of a CMOS PLD, you can create a retriggerable monostable multivibrator (one-shot) that can provide timing intervals from milliseconds to seconds. The key to the circuit's operation **(Fig 1)** is a 3-state output that discharges the timing capacitor, C, when a trigger pulse occurs and then lets it recharge through a resistor, R.

When the circuit is in its quiescent state, the flip-flop's output, Q_1, is low; OUTRDC is disabled; and C is charged to within a diode drop, V_D, of V_{CC}. When the Trigger input goes high, it clocks a logic one through the flip-flop. Consequently, the output, Out, goes high, and OUTRDC goes low, which discharges C toward ground. When the potential on C is a diode drop, V_D, below the PLD's input-logic threshold, V_{TH} (about 1.6V for Altera parts), the internal feedback signal, FB_2, goes from low to high. This clears the flip-flop, which in turn puts OUTRDC in its high-impedance state.

With OUTRDC disabled, C charges through R and D toward V_{CC}. When the potential on C equals V_{TH}, the internal feedback signal, FB_1, goes from high to low, thus driving Out low and ending the timing cycle. If the Trigger input sees another high-to-low transition before the circuit times out, the circuit begins another timing cycle.

The purpose of the diode, D, is to ensure that the capacitor, C, discharges to a fixed voltage, V_D, below V_{TH}. Assuming that C discharges to exactly $V_{TH} - V_D$, the timing period is

$$T = -RC \times \ln(1 - (V_{TH}/(V_{CC}-V_D))).$$

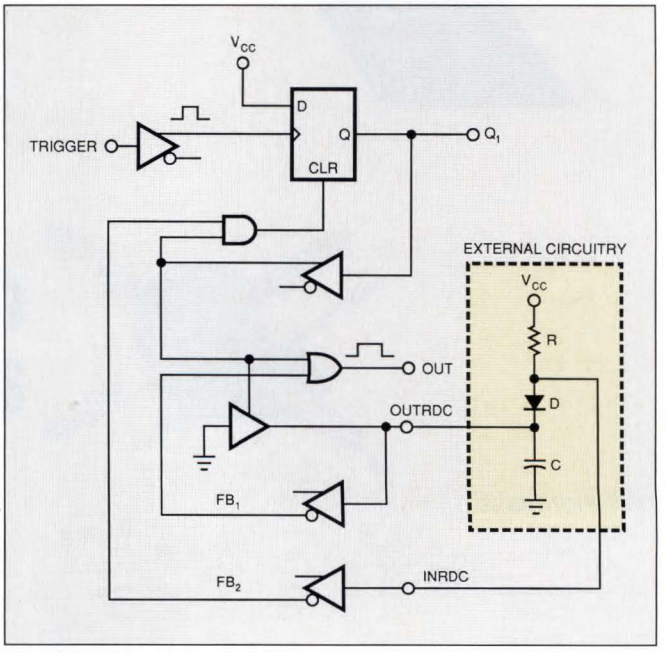

***Fig 1—An external RC-timing** network lets you add the one-shot function to your PLD repertoire.*

If the Trigger signal comes from other circuitry within the PLD and you don't need the Out signal, you can reduce the number of pins required from five to three or four.

Because the voltages at the FB_2 and OUTRDC pins are not confined to the normal logic levels of V_{CC} and GND but can be at or near V_{TH}, the supply current that the PLD draws may be higher than expected, especially if you use a so-called zero-power PLD. The worst-case current draw occurs when C is larger than 1 nF and you retrigger the one-shot frequently. EDN

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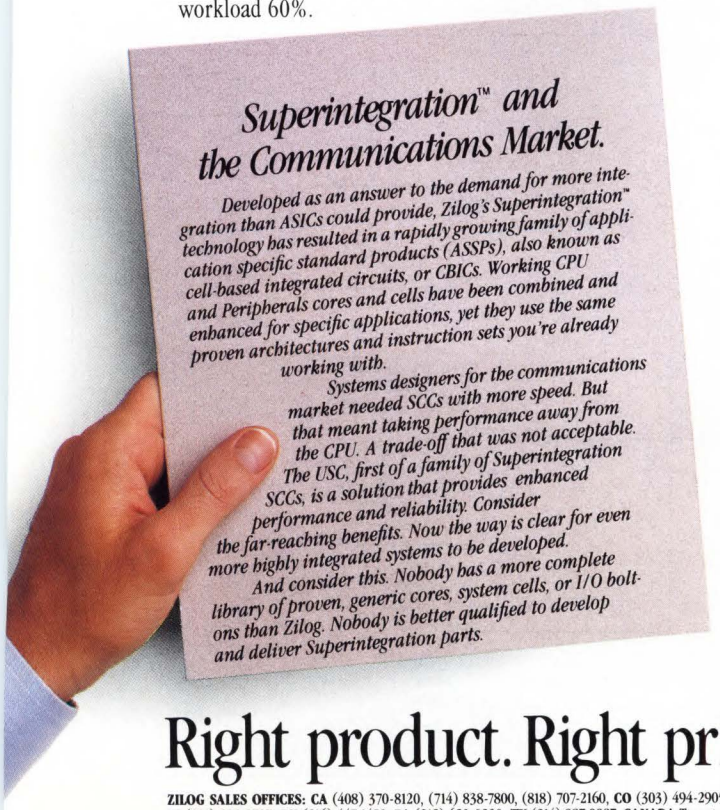

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CIRCLE NO 133

Triacs preregulate HV supply

Héctor Gellon
San Luis University, San Luis, Argentine

The circuit of the high-voltage power supply in **Fig 1** requires detailed study before it reveals its true nature as a digital version of the venerable Variac variable autotransformer. In operation, one of the control circuitry's triacs selects the tap on the main transformer, T_1, which provides the proper, preregulated voltage to the secondary regulator. T_2 and its associated components comprise the secondary regulator. Such preregulation makes this high-voltage supply more efficient and stable.

The ADC 0804, IC_1, digitizes a voltage-feedback signal from the secondary regulator's output. The MC1415 demultiplexer, IC_2, decodes the digitizer's output. IC_2, in turn, drives T_1's optoisolated triacs via the 74LS240 driver chip, IC_3, and associated optoisolators (see the insert in **Fig 1**).

Transformer T_3 samples the circuit's current output. The auxiliary, 12V winding on T_1 ensures no-load starting. The combination of op amp IC_5 and the inverting transistor, Q_1, square this current signal. The output of Q_1 is the $\overline{CLK}$ signal, which triggers one-half of the one-shot, IC_{4A}, to begin the circuit's A/D conversion. The one-shots' periods are set to time out within ½ cycle of the ac input.

Upon completion of its A/D conversion, IC_1's $\overline{INTR}$ output triggers the other half of the one-shot, IC_{4B}, which enables the converter's data outputs.

The rising edge of the $\overline{CLK}$ signal resets the one-shot and latches the new conversion value into IC_2. The latch and the associated driver and optoisolator trigger a selected triac according to the latest value of the voltage-feedback signal, V_O. EDN

To Vote For This Design, Circle No 749

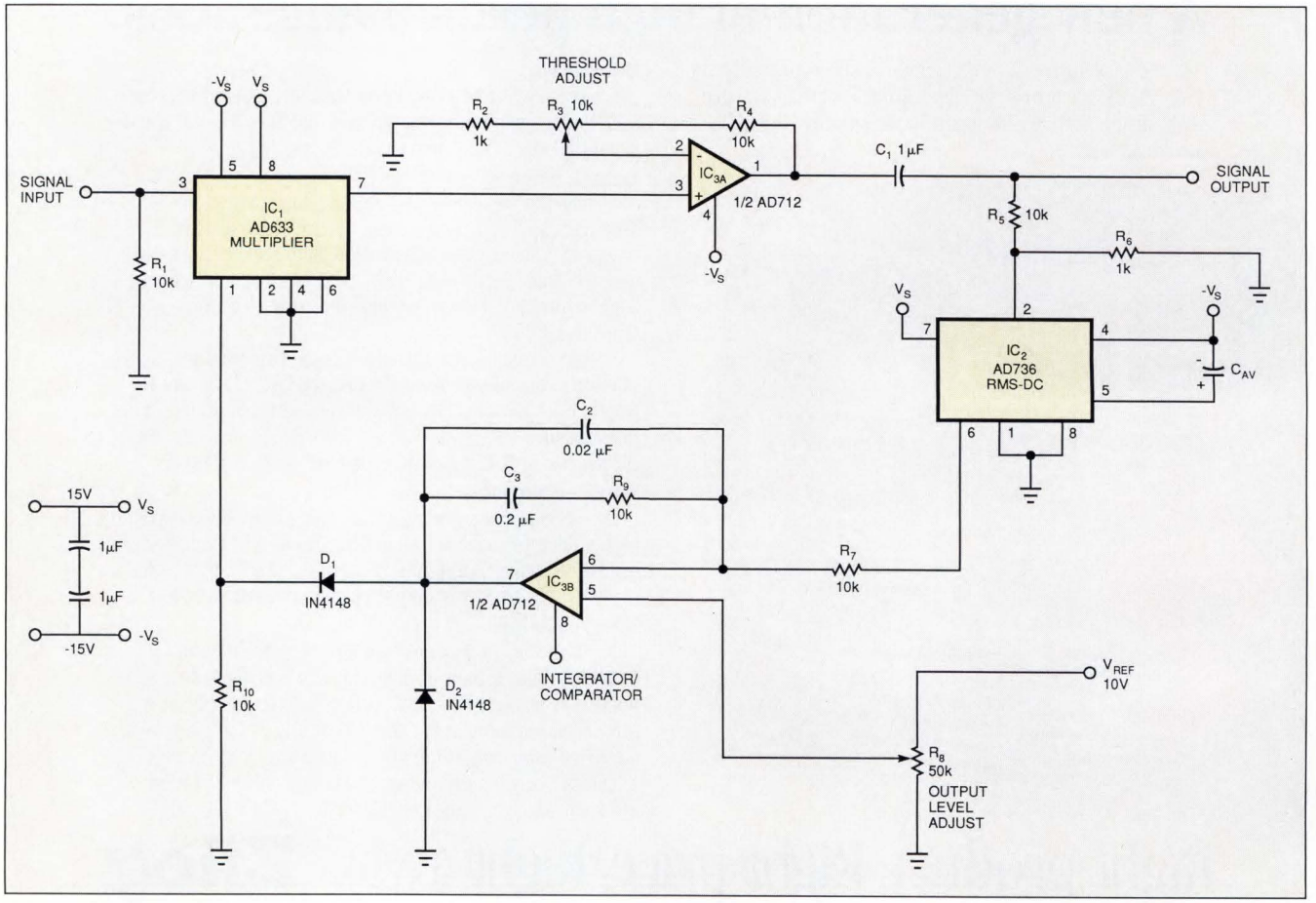

Fig 1—This high-power preregulator *acts as an electronically controlled variable autotransformer.*

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CIRCLE NO 134

True-rms AGC provides constant power

Mark Murphy
Analog Devices, Wilmington, MA

The automatic-gain-control (AGC) circuit in **Fig 1** maintains a constant output level over a 65-dB input range. With a 70-dB signal-to-noise ratio, it provides constant power to a load over a 40-dB input range. The keys to the circuit's superior dynamic range and frequency response are an analog multiplier functioning as a voltage-controlled amplifier and a true-rms converter in the AGC feedback loop. The chip cost is $9.25. You can extend the AGC range to 85 dB by rescaling R_2 or R_4.

In operation, the input signal goes to one input of the analog multiplier, IC_1. One-half of the dual op amp, IC_{3A}, scales the multiplier's output. The rms-to-dc converter, IC_2, converts the op amp's output to a dc level that is proportional to the input signal's rms value. The resistive divider, R_5 and R_6, divides the op amp's output by a factor of 10 to make IC_1, a 1V full-scale device, compatible with IC_2, a 10V full-scale device.

The averaging capacitor, C_{AV}, sets the time constant of the true-rms converter. The other portion of the dual op amp, IC_{3B}, compares and integrates the scaled output of the true-rms converter with a reference level. R_8 varies the reference level and thereby sets the circuit's output level.

After a delay determined by the RC network, C_2, C_3, and R_9, the output of the comparator/integrator appears at pin 1 of the multiplier. This signal sets the gain of the multiplier. Diodes D_1 and D_2 ensure that the output of the comparator/integrator remains positive; a negative voltage would cause it to latch.

The threshold control, R_3, sets the lowest input-signal level at which the AGC loop begins to work. For input signals below this threshold, the signal output tracks the input; above this threshold, the signal output remains constant.

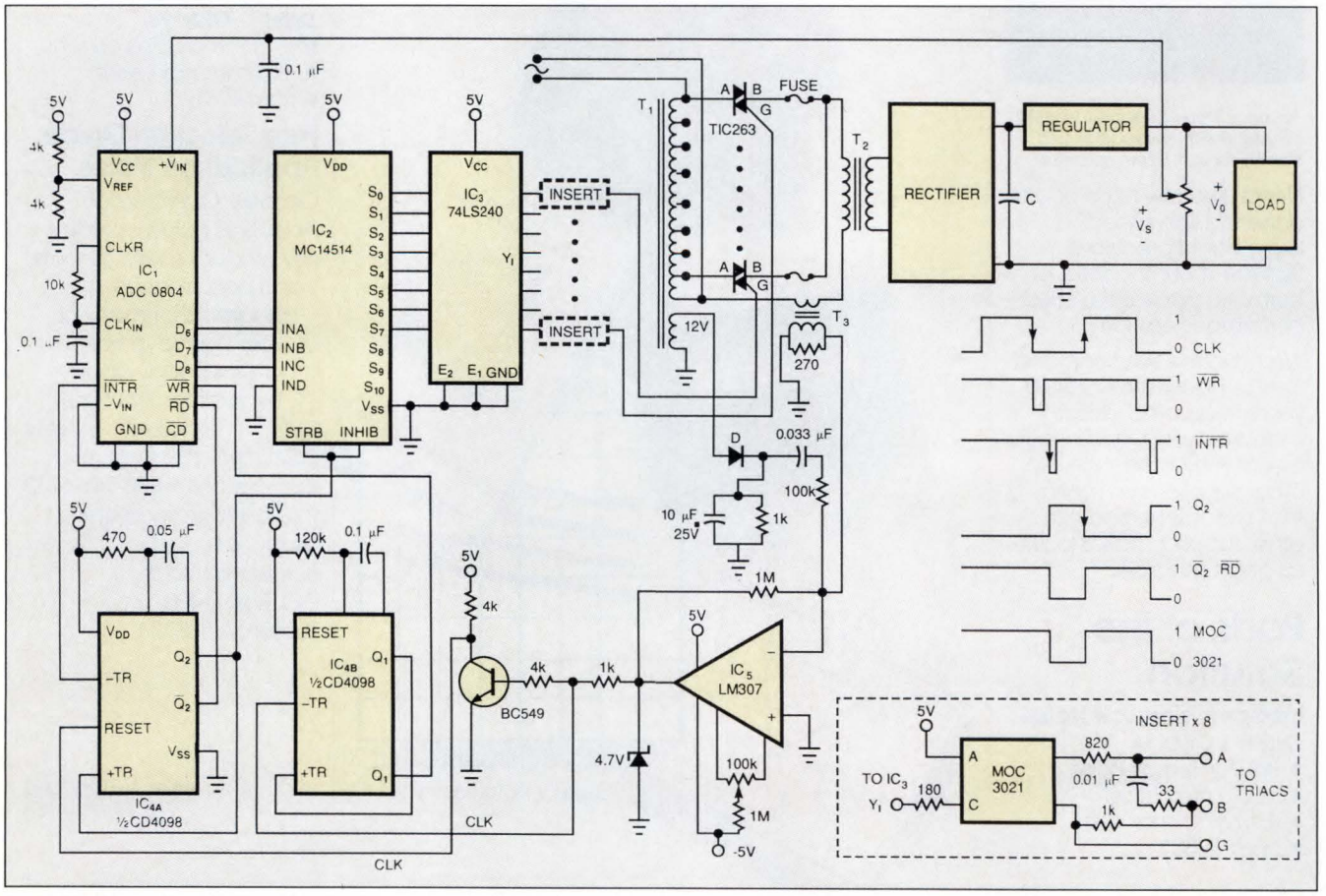

Fig 1—The true-rms converter *in this AGC's feedback loop gives improved frequency response and leveling compared with average or peak-detecting schemes.*

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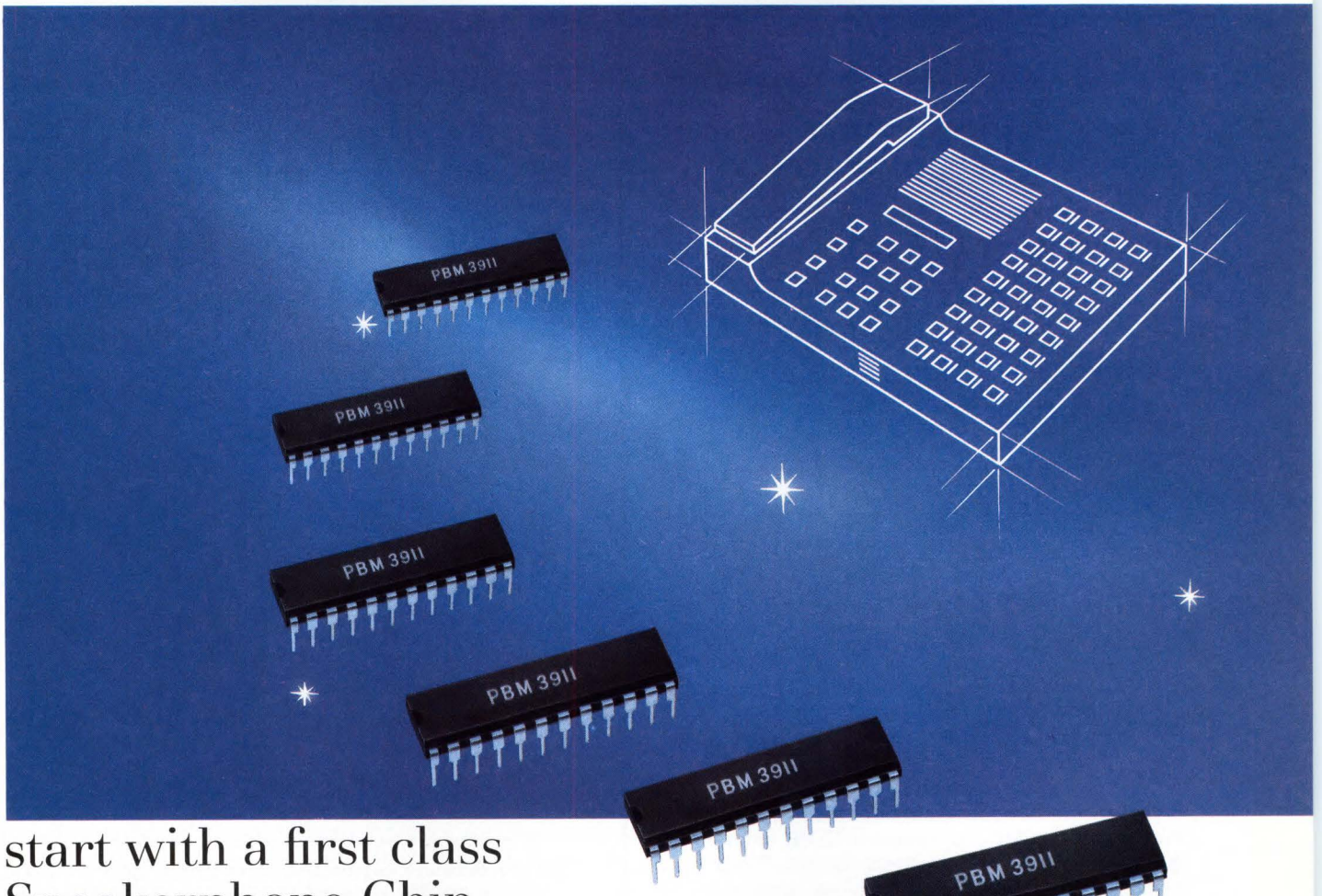

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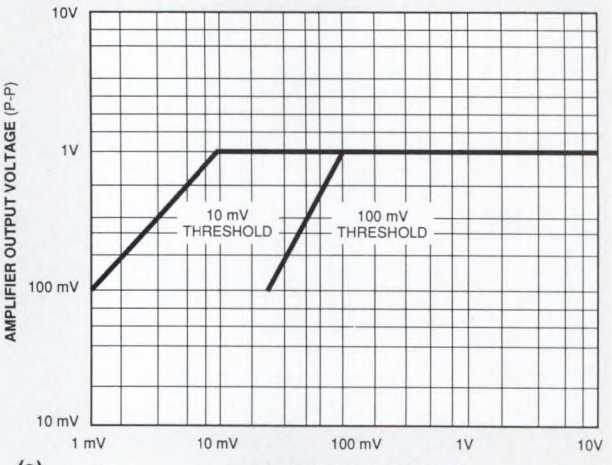

(a)

MINIMUM THRESHOLD	MAXIMUM THRESHOLD	AGC RANGE	SIGNAL-TO-NOISE RATIO	BANDWIDTH
60 mV	25V	52 dB	57 dB	320 kHz
100 mV	25V	48 dB	60 dB	300 kHz
150 mV	25V	44 dB	65 dB	260 kHz
200 mV	25V	42 dB	67 dB	220 kHz
250 mV	25V	40 dB	70 dB	212 kHz

(b)

Fig 2—Performance specifications show that *the AGC limits output levels to 1V* ***(a)****. The specs also illustrate the relationship between AGC range and bandwidth* ***(b)****.*

You can extend the AGC range of this circuit either by increasing the value of resistor R_2 beyond its nominal 1-kΩ value or by decreasing R_4 below its 10-kΩ value. These measures increase the gain of the multiplier. Unfortunately, increasing the AGC range decreases the signal-to-noise ratio. EDN

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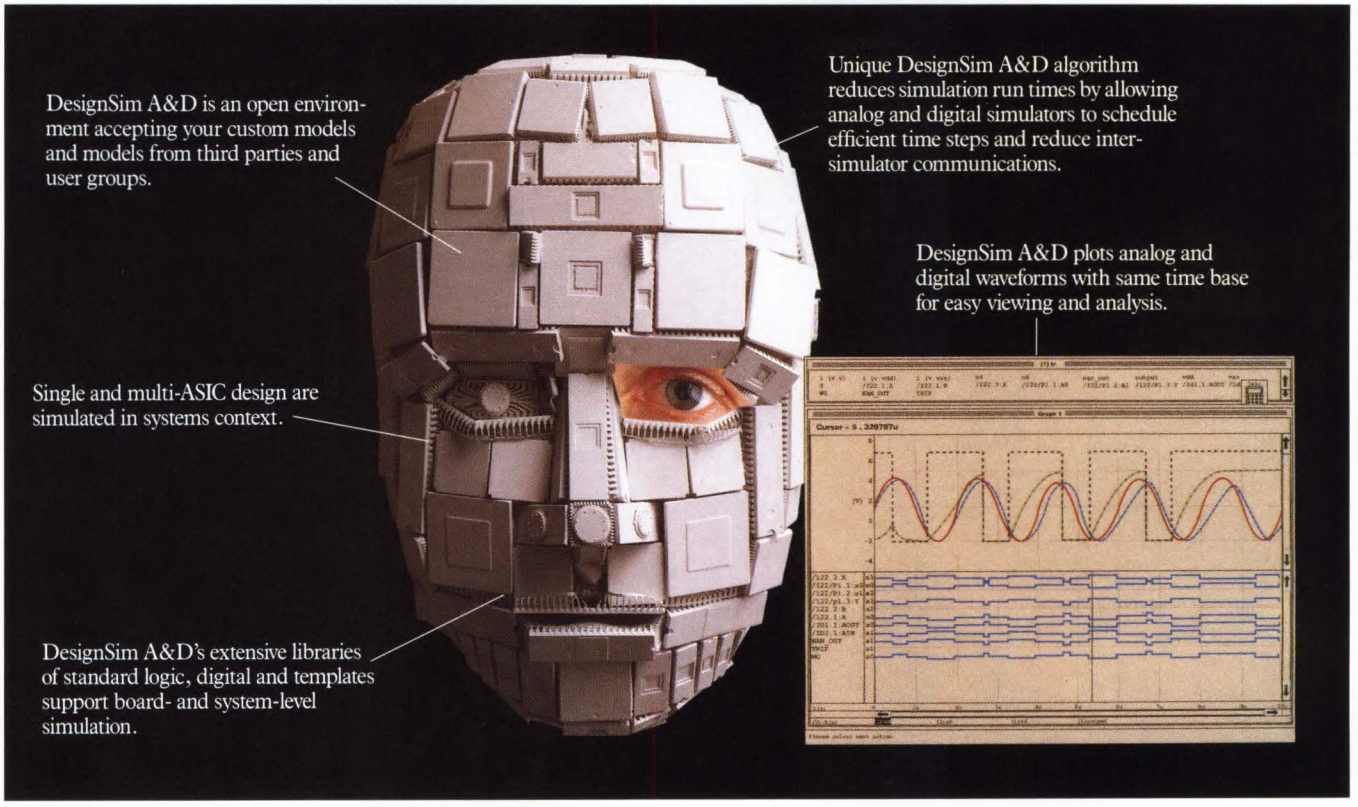

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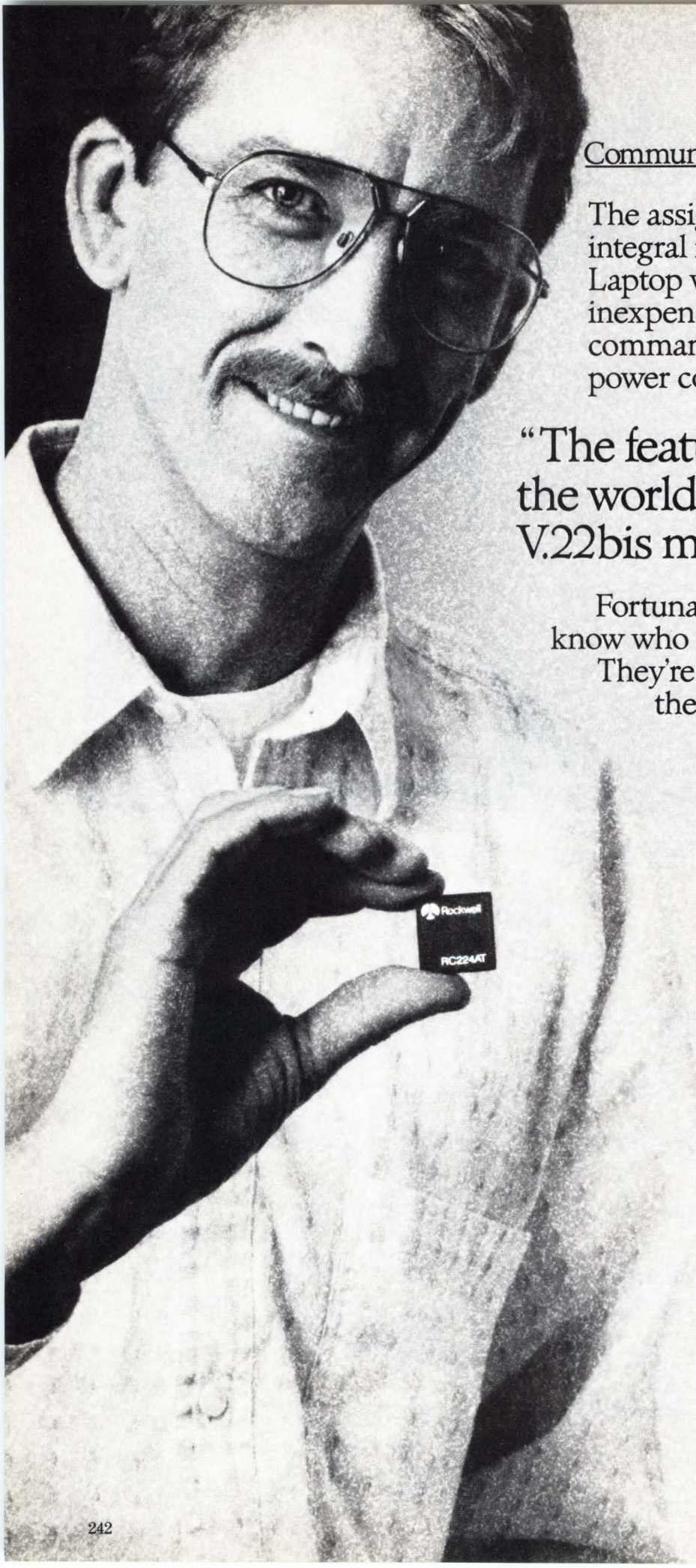

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A Rockwell technical advisor explains that it's the only chip set with Quad capability that meets CCITT V.22bis, V.22A/B, V.21 and V.23 requirements, as well as Bell 212A and 103 standards. He adds that the RC2324SME offers capabilities optimized for Europe, including MNP 5™ and V.25bis.

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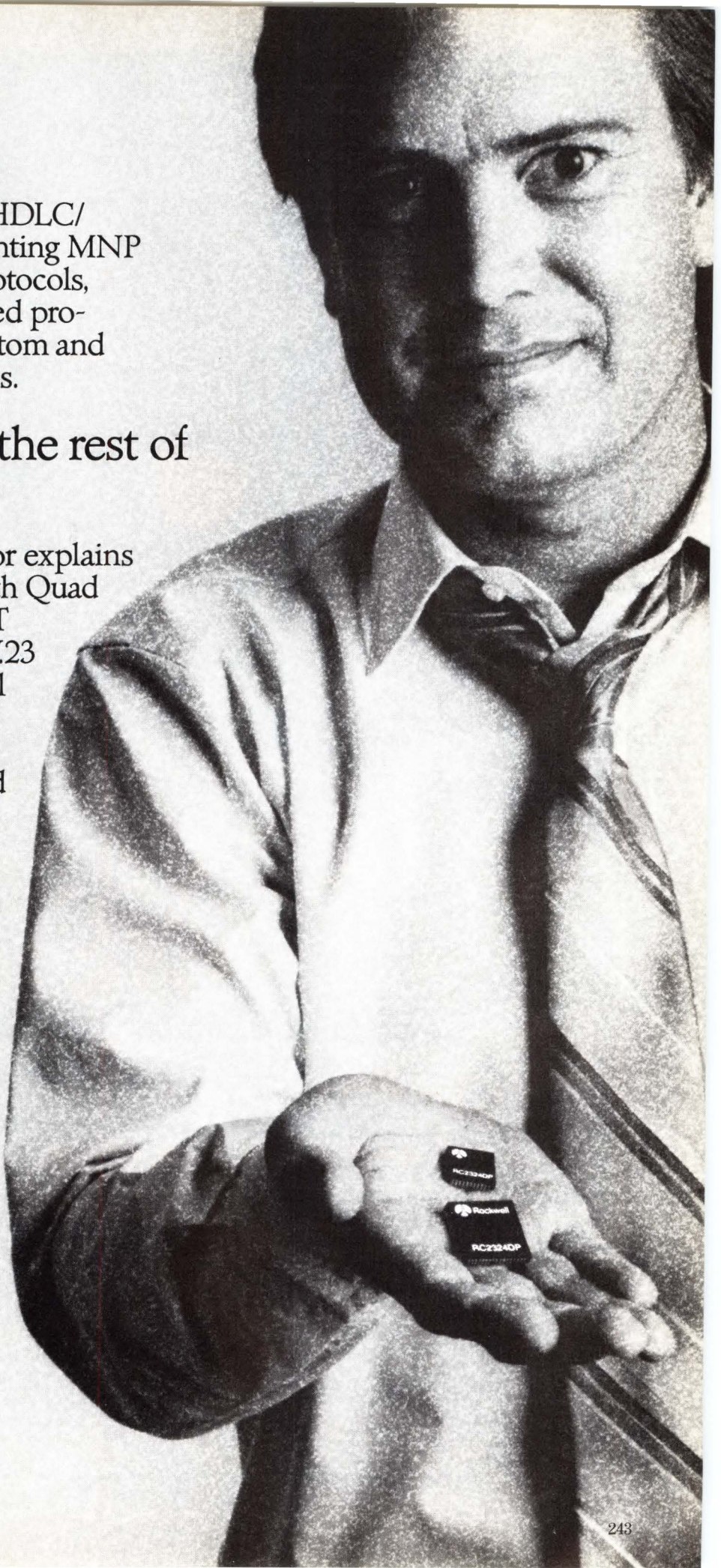

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Digital Electronics Corporation, 31047 Genstar Road, Hayward, CA 94544-7831 (415) 471-4700

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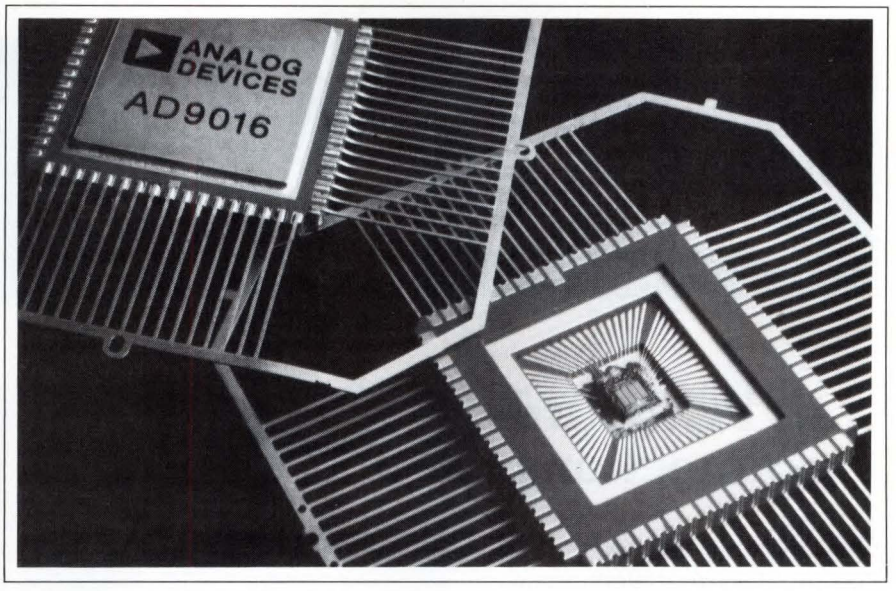
NEW PRODUCTS

INTEGRATED CIRCUITS

6-BIT ADCs

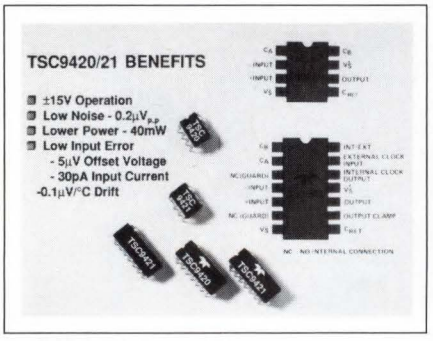
- *Sample at rates to 500 MHz*
- *Have input bandwidths of 200 MHz*



The AD9006 and AD9016 ADCs directly digitize RF signals operating at sample rates to 500 MHz and input bandwidths of 200 MHz. With a 200-MHz input frequency, the ADCs have a minimum 29-dB signal-to-noise ratio, corresponding to 4.4 effective bits. The AD9006 has a single 6-bit output latch; the AD9016 has two 6-bit latches for demultiplexed operation. Demultiplexing reduces the speed requirements for external logic because data is read out at half the sample rate. Both ADCs accommodate a ±1V full-scale input. Maximum integral and differential nonlinearities are 0.5 LSB, with no missing codes guaranteed over the specified temperature range. Dynamic specifications include a typical 1.2-nsec aperture delay and 3-psec aperture jitter. Maximum input capacitance is only 10 pF. The AD9006 and AD9016 operate from 5V and −5.2V supplies and dissipate 1.7W and 2W, respectively. From $200 (100).

Analog Devices, 7910 Triad Center Dr, Greensboro, NC 27409. Phone (919) 668-9511.

Circle No 351



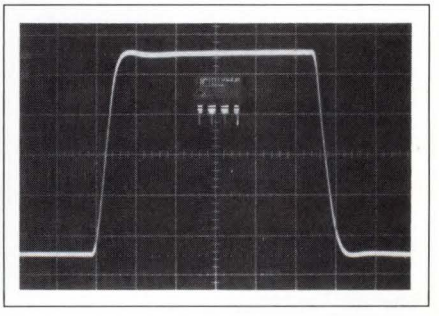
CMOS OP AMPs

- *Operate from ±15V supplies*
- *Offset voltage is only 5 μV*

Able to operate from ±15V supplies or a single supply of 7 to 32V, the TSC9420/21 CMOS op amps can replace lower-performance bipolar devices in precision amplification and signal-conditioning applications. The op amps feature a maximum offset voltage of only 5 μV and an offset-voltage drift of 0.1 μV/°C. Over a 10-Hz bandwidth, noise is 2.1 μV p-p. On-chip nulling circuitry operates over the full temperature range of −40 to 85°C, significantly reducing temperature-induced errors. Open-loop gain is 120 dB min with a 10-kΩ load. The TSC9420 comes in an 8-pin DIP; the TSC9421 comes in a 14-pin DIP. The TSC9421 has an output clamp that minimizes overload recovery time, and you can disable its internal chopper clock for external clock operation. $2.06 (10,000).

Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (800) 888-9966.

Circle No 352



HIGH-SPEED OP AMP

- *Slew rate is 2600 V/μsec*
- *Bandwidth is 165 MHz*

The CLC404 monolithic op amp features an extremely high slew rate of 2600 V/μsec and a full-power (5V p-p) bandwidth of 165 MHz. The CLC404 provides this performance with a supply current of only 11 mA and a power dissipation of only 110 mW. Because of its high slew rate, the op amp operates in a linear mode in virtually all circuit configurations and signal levels. Other features include a typical settling time of 10 nsec to 0.05%, differential gain of 0.07%, and differential phase of 0.03°. Commercial/industrial versions (−40 to +85°C) in 8-pin DIP or 8-pin SOIC packages, $9.35 (1000).

Comlinear Corp, 4800 Wheaton Dr, Fort Collins, CO 80525. Phone (303) 226-0500.

Circle No 353

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2. QUALIFIED TO D55302
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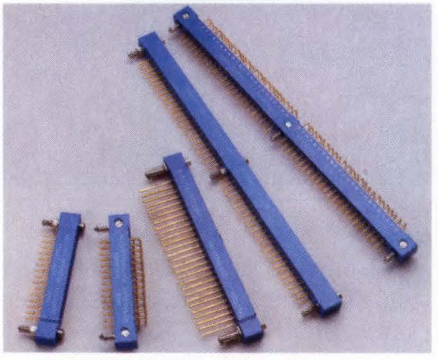
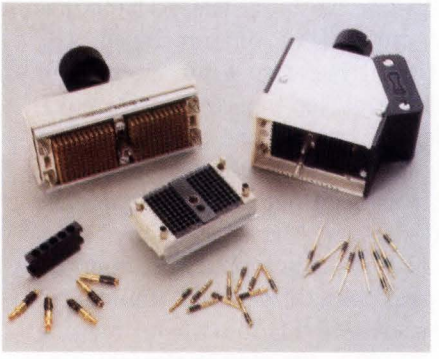
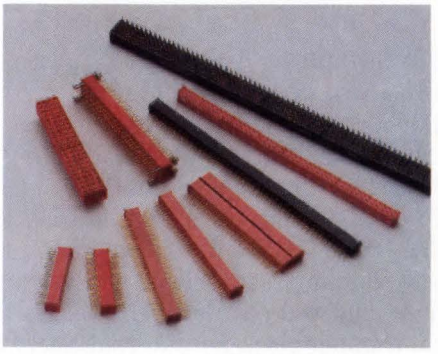


KA Series: *17-490 Contacts with D55302-Listed Qualified Models.*



N Series: *70-700 Position Connectors with Ratings to 9 Amps.*



KG Series: *22-90 Position Board Stacking for .240 or .480 Heights Between Boards.*

Y Series: *3-500 Amp Discrete Pins and Mating Sockets.*

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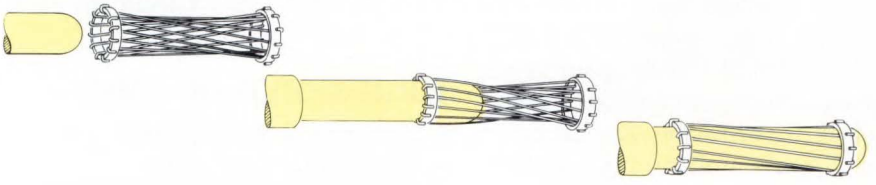

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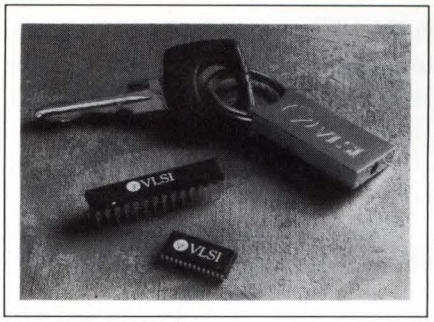


STATIC RAM

- *Organized as 32k × 8-bits*
- *Has access/cycle times of 35- or 45-nsec*

The VT62832 is a 256k-bit static RAM organized as 32,768 words by 8 bits. The device is available with access and cycle times of either 35 or 45 nsec. Power consumption is only 300 mW in the active mode, 100 μW in the standby mode, and 15 μW in the CMOS standby mode. The VT62832 is available in a 28-pin, 300-mil DIP and a 28-pin, 300-mil SOJ package. DIP version of the 35-nsec VT62832, $75; SOJ version, $86.25 (100).

VLSI Technology Inc, 1109 McKay Dr, San Jose, CA 95131. Phone (408) 434-3000.

Circle No 354

PALETTE DAC

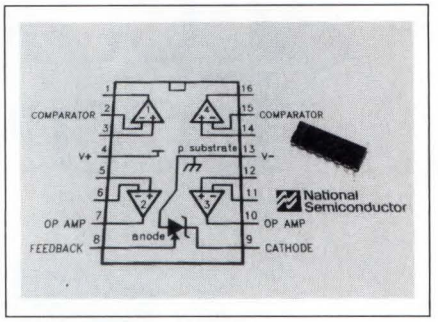
- *Supports 256-color displays*
- *Compatible with IBM PS/2 computers*

The NCR 77C171 D/A converter supports all of the Palette DAC functions in IBM PS/2 computers, and it is fully compatible with VGA display controller outputs and pin-compatible with the Inmos IMS-G171/176 chip. The 77C171 allows the simultaneous display of 256 colors (from a palette of 262,144 colors) via its 256 × 18-bit palette RAM (color look-up table) and three 6-bit D/A converters. The 36-MHz 77C171 chip supports 800 × 600-pixel formats and 132-column displays. The chip provides full video blanking and also includes a bidirectional μP interface for loading and reading the palette RAM. The

77C171's red, green and blue analog outputs are compatible with the RS170 video standard and are capable of driving 0.7V full scale into a 37.5Ω load. 28-pin DIP, $8.25 (1000).

NCR Corp, 1700 Patterson, Dayton, OH 45479. Phone (800) 525-2252.

Circle No 355



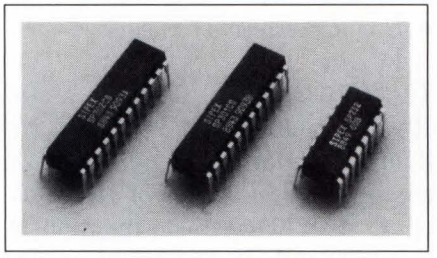
MULTIFUNCTION ICs

- *Contain multiple analog functions on a single chip*
- *Offer higher reliability and lower cost*

The first four members of the company's Super-Block family of monolithic ICs contain multiple analog functions on a single monolithic chip and feature higher reliability and lower costs than single-function devices. The LM604 multiplexes four differential-input channels to a single op amp, and it has a bistate output that drives a 600Ω load. You can use the LM604 in 5V logic systems or in ±15V analog circuits. The LM611 is a single-supply op amp and an adjustable micropower reference. The LM613 is a dual op amp and dual comparator with an adjustable micropower reference. The LM614 is a quad op amp and an adjustable micropower reference. The op amps used in this family of ICs are enhanced versions of the LM324 Series with an improved slew rate and a wider power bandwidth. The LM613's dual comparators allow differential-input voltage swings of ±36V. LM604 (18-pin DIP), $2.30; LM611 (8-pin DIP), $0.84; LM613 (16-pin DIP), $1.30; LM614 (16-pin DIP), $1.22 (100).

National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (408) 721-2274.

Circle No 356



DRIVERS/RECEIVERS

- *Provide RS-232C/RS-432 interface*
- *Functions are pin selectable*

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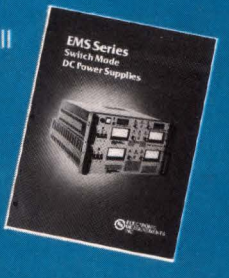

ELECTRONIC MEASUREMENTS INC.

405 Essex Road, Neptune, NJ 07753
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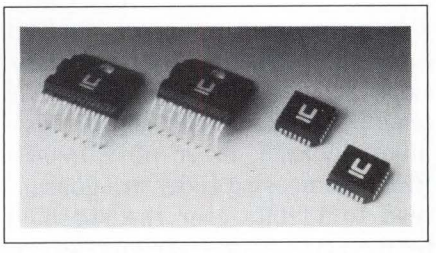
CIRCLE NO 143

of the MAX230 through MAX239 RS-232C devices, Sipex has announced its SP301 and SP302 BiCMOS devices, which combine RS-232C and RS-432 interfaces in one package. The SP301 and SP302 provide pin-selectable interfaces that let you set the RS-232C function, the RS-432 function, or a combination of both. The SP301 and SP302 include an internal loopback mode; this mode is controlled by a single input pin that provides the controlling system with a self-test capability of its transmit and receive circuitry. The SP301 contains 2-channel drivers and receivers for both RS-232C and RS-432 standards. The SP302 contains 4-channel RS-232C and 2-channel RS-432 drivers and receivers. Both devices use 3-state outputs for the drivers and handle receiver input levels of ±15V. The SP301 and SP302 come in a 24-pin DIP and operate from 5V and ±12V supplies. SP-XXX replacements for the MAX230-239 line, from $2.30 to $8.50. SP301, $12.00; SP302, $13.25 (100).

Sipex Corp, 6 Fortune Dr, Billerica, MA 01821. Phone (508) 663-7811.

Circle No 357



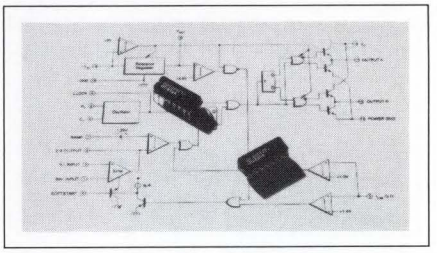
MOTOR-CONTROL IC

- *For 3-phase brushless motors*
- *Provides low-loss linear control*

The UC3655 is used with external Hall sensors and provides the commutation logic for driving each of the IC's three output phases. The IC controls the motor current in 3-phase, dc brushless motors in response to commands based on speed, position and torque. The UC3655 uses external pnp transistors selected for low-saturation voltage as high-side drivers. Internal to the IC are low-saturation, low-side npn drivers. The result is a total source/sink saturation-voltage drop of less than 1V at 1A load current. The UC3655 uses only a 5V supply with a current requirement that is proportional to motor current. When the IC's outputs are off, quiescent supply current is less than 10 mA. Other features include 60° phasing with pin-selectable forward, reverse and inhibit functions, undervoltage lockout, current limiting, and thermal shutdown. UC3655V (15-pin, 25W package), $5.28; UC3655Q (28-pin PLCC), $5.08 (1000).

Unitrode Integrated Circuits Corp, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410.

Circle No 358



CURRENT-MODE PWM

- *Delivers 1.5A peak drive currents*
- *Has 1.5-MHz oscillator capability*

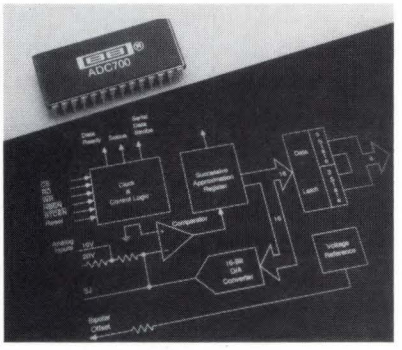
The SG1815 PWM controller offers several improvements over earlier devices. It is fabricated in a linear Schottky process, which exhibits very short propagation delays through the current limit comparator, logic circuitry, and output drivers. The IC has no pulse-width instability at cold temperatures, and it offers lower start-up current and higher ground-noise tolerance than the industry standard. Included in the controller are a 5.1V precision reference trimmed to ±1%, a programmable soft-start function, an oscillator-frequency capability of 1.5 MHz, a fast current-limit com-

INTEGRATED CIRCUITS

parator, full double-pulse suppression logic, and dual 1.5A (peak) totem-pole drivers. Other features include a wideband, low-impedance error amplifier and an undervoltage lockout function with hysteresis. The SG1825 is specified over the military temperature range, the SG2825 over the industrial range, and the SG3825 over the commercial range. SG3825, $7.65 (100).

Silicon General, 11861 Western Ave, Garden Grove, CA 92641. Phone (714) 898-8121.

Circle No 359

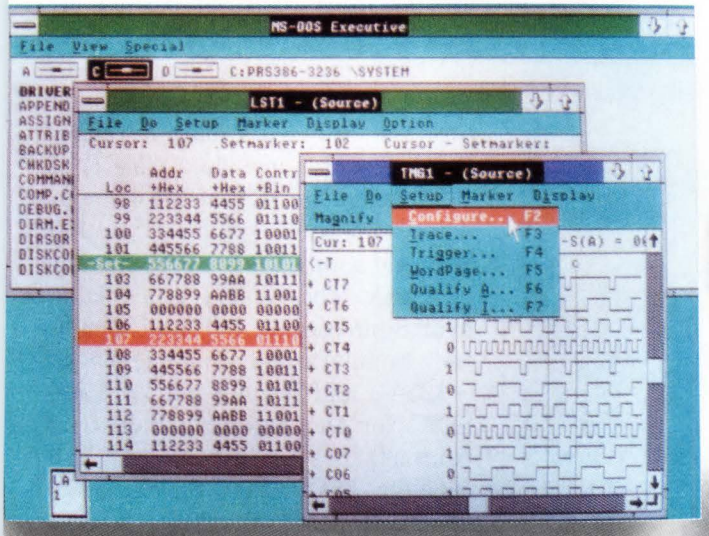


16-BIT ADC

- *Includes μP interface*
- *Has 17-μsec conversion time*

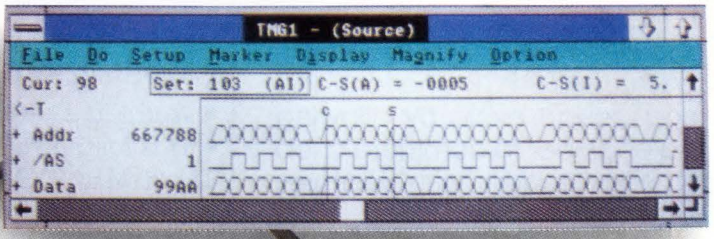
Packaged in a 28-pin, hermetic ceramic DIP, the ADC700 combines a 16-bit A/D converter with a clock, a laser-trimmed reference, and an 8-bit μP interface. Key specifications include 16-bit resolution, a 17-μsec conversion time, and a maximum linearity error of ±0.003% FSR. No missing codes are guaranteed to 14 bits over the specified temperature range (commercial, industrial, or military). Other features include output data in either serial or parallel form and a serial-data interface that includes a data-strobe output with 16 edges appropriately timed for direct loading of shift registers. Parallel data is available in two 8-bit bytes from TTL-compatible, 3-state output buffers. The ADC700 has a 50-nsec bus-access time and a 70-nsec bus-relinquish time. Internal scaling re-

Finally. A High Performance Logic Analyzer That Doesn't Defy Human Logic.

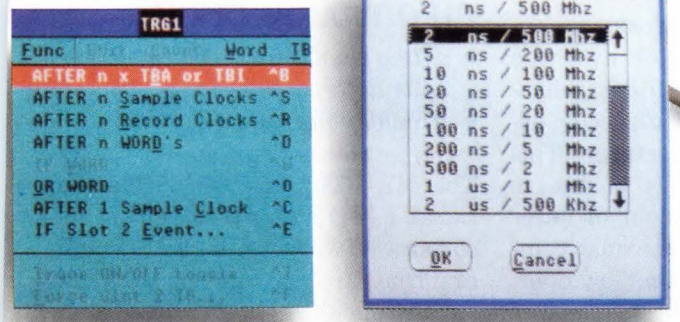


With Microsoft Windows and MS-DOS,™ you get full command of the PL1000's power without losing command of your senses.

The PL1000 supports disassembly of all popular 8-, 16- and 32-bit microprocessors.



An exclusive clustered channel feature simplifies the display, so you always know exactly where you are on your address bus, at a glance.



Pull-down menus let you click through time base choices, trigger functions, or any other parameters.

Just point and click your way through the first time, and every time.

The new PL1000 makes perfect sense the first time you use it. And doesn't have to be relearned the second time.

You get uncompromised high performance (up to 192 channels at 100 MHz synchronous, or 96 at 200 MHz asynchronous; up to 144 channels at 500 MHz asynchronous, or 72 at 1 GHz) with a friendly, familiar MS-DOS Windows interface.

All the heavy-duty features are here, too. A complete line of application-specific accessories. 100 MHz synchronous analysis. High performance active probes —2 MOhm/5 pF. Optional 50-MHz pattern generator.

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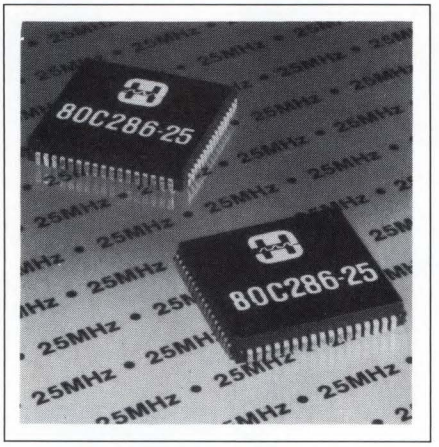
KONTRON ELECTRONICS (800) 227-8834 630 Clyde Avenue, Mountain View, CA 94039-7230

sistors provide a choice of 0 to 5V, 0 to 10V, 0 to 20V, ±2.5V, ±5V, and ±10V input ranges. Prices start at $74 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132.

Circle No 360



CMOS 80286 μP

- *Rated at 25 MHz*
- *Has low operating current*

The 25-MHz 80C286 μP is the latest in a series of performance increases of the original 12.5-MHz CPU. Operating at the same frequency, the 80C286 has shown performance increases as high as 20% over the 80386 when executing 16-bit, industry-standard 8086 or 80286 code, according to the manufacturer. This performance advantage is due to the 80C286's requirement of fewer clock cycles to execute many instructions. Because of its low operating current, the 80C286 is well suited for laptop and portable computers operating from battery power. Other manufacturers, including Chips and Technologies (Milpitas, CA) and Austek Microsystems (Mountain View, CA), plan to offer support circuits rated for 25-MHz operation that will allow maximum system throughput. 80C286-25, $142 (1000).

Harris Semiconductor, Box 883, Melbourne, FL 32901. (407) 724-3800.

Circle No 361

PRECISION OP AMP

- *Ultra-low offset voltage*
- *High open-loop gain*

The OP-177 precision op amp features offset voltage of only 10 μV max at room temperature and 20 μV max over the full military temperature range. Moreover, the low offset-voltage drift of 0.1 μV/°C max eliminates the need for external trimming. The op amp's open-loop gain of 12V/μV is maintained over the full ±10V output range. Other features include a CMRR of 130 dB min, a PSRR of 120 dB min, noise voltage of 118 nV (1 to 100 Hz), and a maximum supply current of 2 mA. The OP-177 is available in an 8-pin ceramic DIP for the military temperature range (−55 to +125°C) and in an 8-pin DIP and SOIC for the extended industrial temperature range (−40 to +85°C). DIP, $1.00; SOIC, $1.50; ceramic DIP, $9.00 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222.

Circle No 362

FIFO/TRANSCEIVERS

- *Allow asynchronous or synchronous data transfer*
- *Provide four different FIFO-buffer status flags*

The MK-45264 and -45265 bidirectional FIFO-buffer/transceivers incorporate two 64×5-bit FIFO buffers that are configured to allow asynchronous, bidirectional, parallel data transfers between two μP-based systems. The devices also contain a bidirectional transceiver so that you can transfer data synchronously from one system to another. The FIFO buffers are automatically disabled when the transceiver is activated. Both devices output two FIFO status flags. The MK45264 has FIFO-full and FIFO-empty flags, and the MK45265 provides FIFO-almost-full and FIFO-almost-empty flags that indicate when a particular port's transmit or

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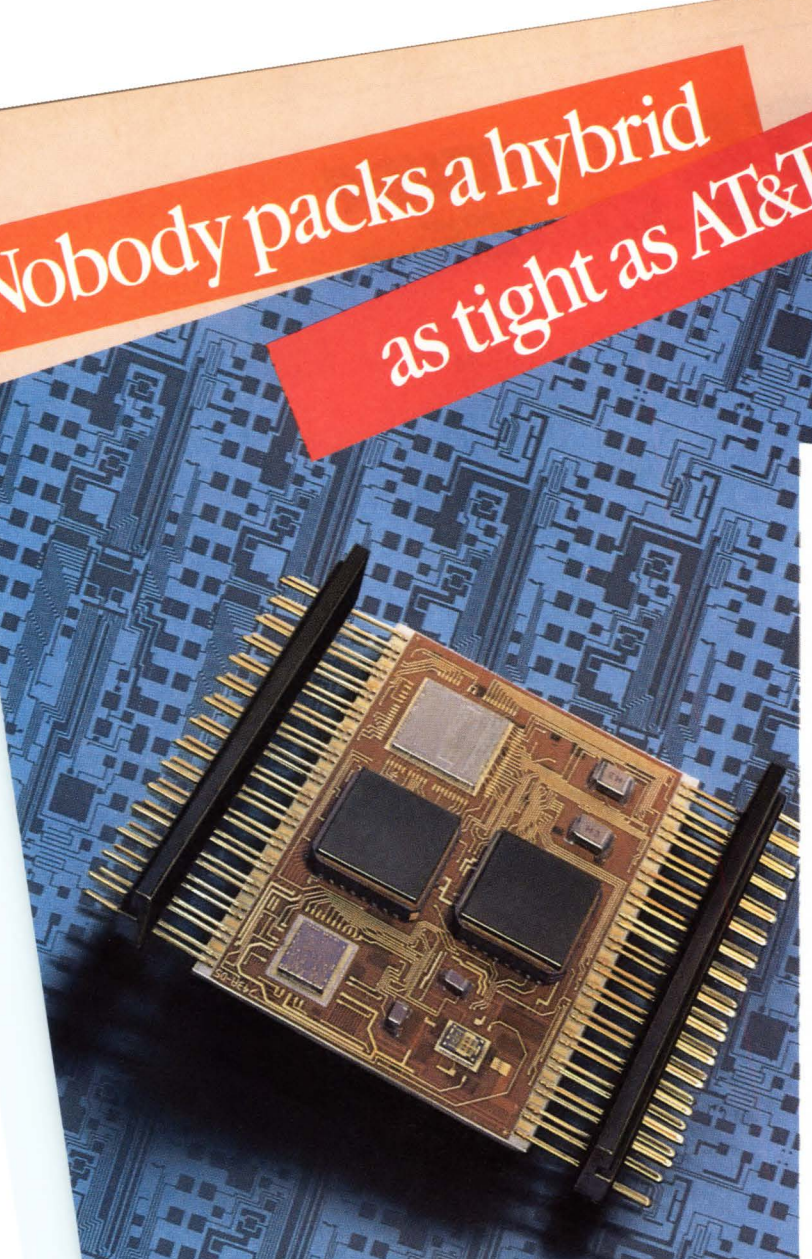

Based on its fully integrated capabilities and new substrate technology, AT&T offers hybrid ICs with record-breaking density.

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CIRCLE NO 149

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HIGHEST OUTPUT POWER PER IN² MOUNTING SURFACE

[HEIGHT — .64 up to .81″]

INPUT: 18-36 VDC

SINGLE OUTPUT: UP TO 90W

SIZE: 4.24 x 2.13 x 0.67″

Model	V/A
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7007/2	12/6.5
7007/3	15/6
7007/4	24/3.75

SINGLE OUTPUT: UP TO 200W

SIZE: 5.91 x 3.54 x 0.81″

7030/1	5/30
7030/2	12/16.5
7030/3	15/13
7030/4	24/8
7030/5	28/7

DUAL OUTPUT: UP TO 120W

SIZE: 5.91 x 2.81 x 0.81″

8001	±5/8
8002	±12/4.5
8003	±15/4
8004	±24/2.5

TRIPLE OUTPUT: UP TO 180W

SIZE: 5.51 x 4.49 x 0.81″

8506	5/12, ±12/4.5
8606	5/12, ±15/4

INPUT: 170-360 VDC

SINGLE OUTPUT: UP TO 150W

SIZE: 5.12 x 2.91 x 0.81″

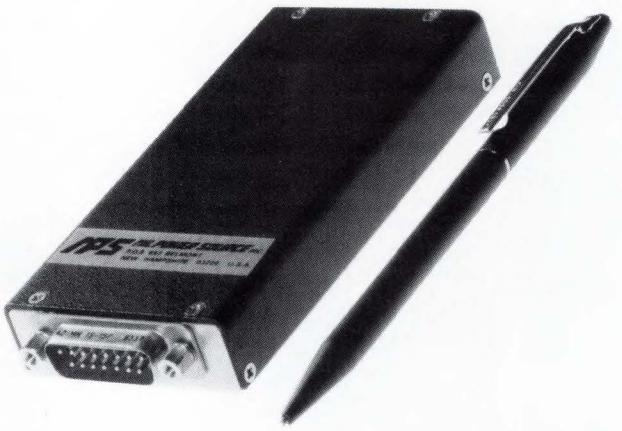
7701/1	5/20
7701/2	12/12.5
7701/3	15/10
7701/4	24/6
7701/5	28/5.5

INPUT: 115 VAC 3-PHASE

SINGLE OUTPUT: UP TO 500W

SIZE: 6.57 x 6.00 x 1.57″

020	5/100
021	12/42
022	15/34
023	24/21



NOTES:

1. INPUT PROTECTION: MIL-STD-1275AT, MIL-STD-704A/D
2. LINE LOAD REGULATION: ±1%
3. RIPPLE & NOISE: 30mv p-p TYPICAL
4. OVERVOLTAGE & CURRENT LIMITING
5. EFFICIENCY: 75-85%
6. EMI/RFI: MIL-STD-461/2
7. ENVIRONMENTAL: MIL-STD-810C
8. TEMP: -54º/+90ºC BASE PLATE
9. **Q.A. SYSTEM MIL-Q-9858A, MIL-I-45208A**
10. **DESIGN/WORKMANSHIP UP TO DOD-2000**

FULL STANDARD LINE AVAILABLE

MPS MILPOWER SOURCE, INC.

BELKNAP INDUSTRIAL PARK
RTE. 106, P.O. BOX 657
BELMONT, NEW HAMPSHIRE 03220, U.S.A.
TEL: (603) 267-8865, FAX: 267-7258

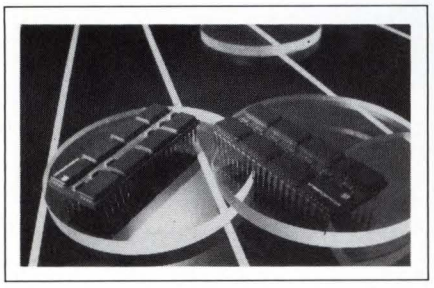
receive FIFO buffer is within four locations of being full or empty. By using one or more MK-45264 and -45265 devices in parallel, you can produce FIFO buffers of various data widths that generate all four status flags. Both devices are packaged in 24-pin, 300-mil-wide DIPs. Approximately $13 (1000).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 363

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 364



STATIC RAM MODULE

- *Provides 1M bit of static RAM in a 40-pin package*
- *Is user configurable to provide 4-, 8-, or 16-bit wide memory*

You can configure the MS1664BCX 1M-bit static RAM module as a 64k×16-bit, 128k×8-bit, or 256k×4-bit memory. It is available with access-time ratings of 25, 35, 45, or 70 nsec. The 40-pin hybrid device comprises 16 64k×1-bit SRAMs surface mounted on a ceramic substrate with decoupling capacitors. Active power consumption for the 25- and 35-nsec versions is 2.28W max; the 45- and 70-nsec versions have a greater maximum power dissipation of 4.8W. Standard versions have a 160-mW standby power dissipation. A low-power version is also available with a standby power dissipation of only 8 mW. The MS1664BCX measures 55.9×22.9×5.6 mm and is optionally available screened to full military requirements. 45-nsec mil part, approximately £500.

Hybrid Memory Products Ltd, Elm Rd, W Chirton Industrial Estate, N Shields, Tyne and Wear NE29 8SE, UK. Phone 091-258-0690. TLX 53206. FAX 091-259-0997.

Circle No 365

Mosaic Semiconductor Inc, 7420 Carroll Rd, Suite 200, San Diego, CA 92121. Phone (619) 271-4565. FAX 619-271-6058.

Circle No 366

ECL RAM

- *Has an access time of 3.5 nsec*
- *Is available with synchronous or asynchronous I/O ports*

The GxB100474A 1k×4-bit ECL static RAM has an access time of 3.5 nsec and is available with either asynchronous or synchronous input and output ports. The synchronous mode device has input and output latches that synchronize input and output data to a common clock input. Input data is latched on the high state of the clock input, and output data is latched on the low state of the clock. In addition, the synchronous device has an on-chip write-pulse generator so that it can self-time write operations. You can clock the synchronous device at frequencies as high as 200 MHz. Both versions have inputs and outputs that are compatible with ECL 100K devices. Approximately $30 (1000).

Siemens AG, Zentralstelle fur Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 367

Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500.

Circle No 368

NEW PRODUCTS

COMPONENTS AND POWER SUPPLIES

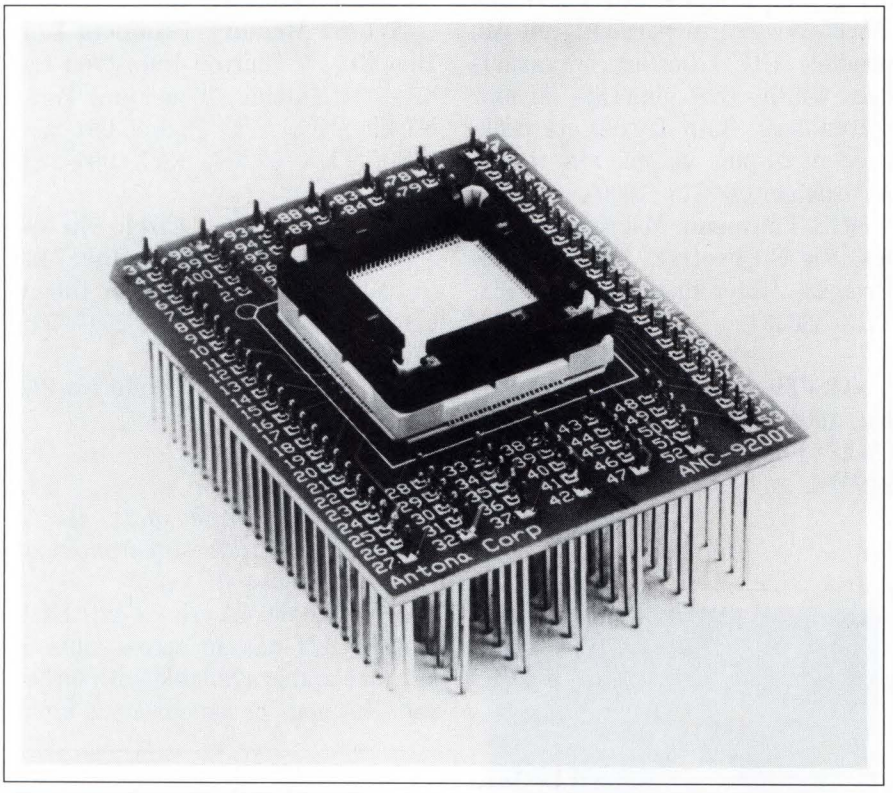
ADAPTER

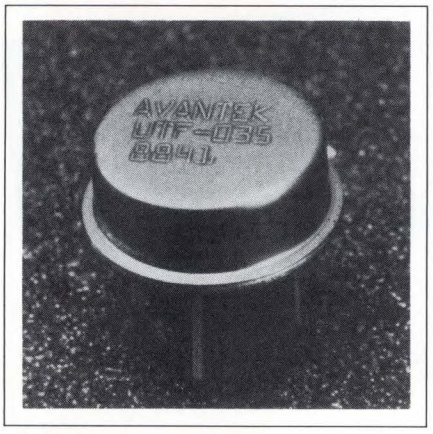
- *Eases prototype wire-wrapping task*
- *Features labeled test points*

The Model ANC-9200 eases the task of wire wrapping prototypes. Available with 3-level wire-wrap pins, the adapter bridges the gap between leadless quad plastic flatpacks and the prototype stage of circuit development. The unit occupies just 6 in.^{2} of board space and provides labeled test points for each of the 100 pins. The adapter pins are on 0.3-in. centers, allowing the unit to be used on a variety of prototype boards. A user's manual includes a template that you can use as a signal-to-pin designation guide. $82.

Antona Corp, 1643½ Westwood Blvd, West Los Angeles, CA 90024. Phone (213) 473-8995.

Circle No 369





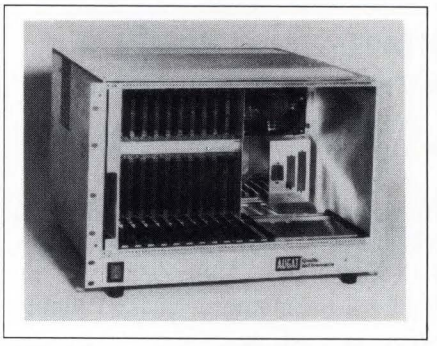
ATTENUATOR

- *Housed in a TO-8 package*
- *Offers single-supply operation*

The UTF-035 unit comprises a 50-to 2000-MHz PIN-diode voltage-variable attenuator combined with a voltage-to-attenuation linearizer circuit in a TO-8 package. It features a 2- to 25-dB attenuation range and a voltage-to-attenuation linearity of ±0.6 dB. The total switching time equals 5 μsec. The unit operates from a 15V supply and features an overall control range of 0 to −10V for maximum to minimum attenuation. The operating range spans −55 to +85°C. $200 (100).

Avantek Inc, 481 Cottonwood Dr, Milpitas, CA 95035. Phone (408) 943-3038.

Circle No 370



POWERED CHASSIS

- *Designed for VMEbus applications*
- *Features three 100-cfm fans*

The Model 70-AVME945 powered chassis is an alternative to the Motorola MVME945A-1. Designed for convenient packaging of Motorola VME board-level products, the unit includes a rear bay for loading 80-mm Motorola I/O transition modules. The front bay accepts Motorola MVME833 or MVME834 mass-storage modules adjacent to the 12-slot, J1/J2 monolithic backplane. A 400W power supply and three 100-cfm fans complete the packaging system. All power and cooling components are totally wired and ready to go. You can use the unit on a table top, or you can mount it in a 19-in. rack. An attractive enclosure is available to provide a finished look. $2949.

Augat Inc, Interconnection Products Group, Box 779, Attleboro, MA 02703. Phone (508) 222-2202. FAX 508-222-0693.

Circle No 371

DC/DC CONVERTER

- *Has a 15W output*
- *Efficiency equals 80% min*

The Model 12S5.3000XC dc/dc converter accepts any input between 9 and 29V and produces a 5V/3A output. Switching frequency equals 70 kHz and efficiency measures 80% min. Internal thermal limiting shuts the unit down if the case temperature exceeds specified limits. Key specs include a 0.2% line-and-load regulation, a 30-mV p-p output noise, and a 0.3%/1000-hour long-term stability. Input-to-output isolation equals 500V dc, and the operating range spans −25 to +80°C. Filter circuits provide conducted-noise protection for both the input and output. A logic shutdown pin serves to minimize converter power consumption. $120.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. FAX 415-932-6017.

Circle No 372

PHOTOSENSOR

- *Utilizes optical triangulation techniques*
- *Has a built-in amplifier*

The MQ photoelectric sensor utilizes optical triangulation techniques that allow users to eliminate background interference by simply twisting a dial. The unit is available in sensing ranges from 1 in. to more than 6 ft. The sensor is insensitive to any changes in color or reflecting surface conditions on the objects being detected. The unit features a built-in amplifier and has a maximum switching speed of 250 operations/sec. $100 (100).

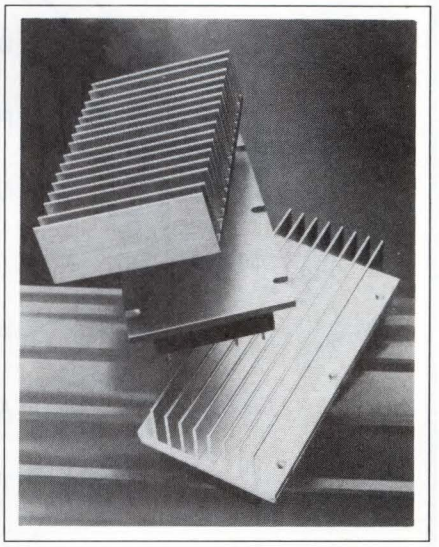
Aromat Corp, 629 Central Ave, New Providence, NJ 07974. Phone (800) 228-2350; in NJ, (201) 464-3550. FAX 201-464-8513.

Circle No 373

HEAT SINKS

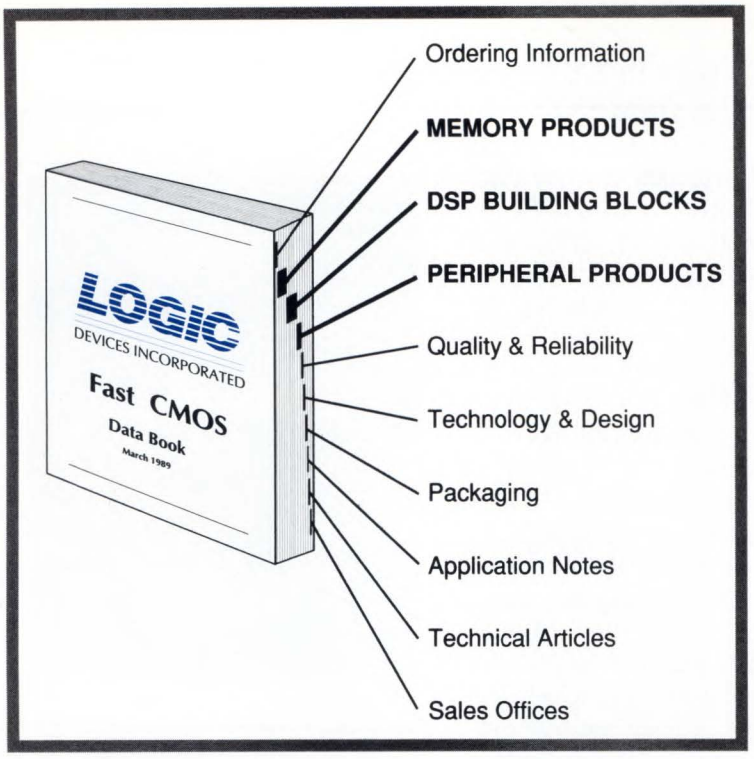
- *Designed specifically to cool dc/dc converters*
- *Available in two models*

These heat sinks are designed specifically to cool 2.4×4.6-in. dc/dc converters. The devices are available in two versions—Model 410011, which features lengthwise fins, and Model 410111, which has crosswise fins. Under natural convection, thermal-resistance values equal 3.5 and 3°C/W for the 410011 and 410111 models, respectively. The thermal resistance under forced-air convection for the two models at 100 and 1000 linear ft/minute, respectively, is as follows:



The 410011 ranges from 0.6 to 2°C/W, and the 410111 ranges from 0.5 to 1.5°C/W. The heat sinks are made of aluminum alloy and come in gold chromate or black anodized finishes. Model 410011, $4.21; Model 410111, $4.23 (1000). Deliv-

Text continued on pg 261



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Please send me:

- ❑ Fast CMOS Data Book
- ❑ SRAM Samples

Part number (even a competitors') _____

Configuration	**Speed**	**Package**
❑ 16K x 1	❑ 12 ns	❑ Plastic DIP
❑ 4K x 4 Sep. I/O	❑ 15 ns	❑ Hermetic DIP
❑ 4K x 4 Com. I/O	❑ 20 ns	❑ CerDIP
❑ 2K x 8	❑ 25 ns	❑ Ceramic LCC
❑ 64K x 1	❑ 35 ns	❑ Plastic SOIC (Gull-wing – 0.3 wide)
❑ 16K x 4 Sep. I/O	❑ 45 ns	❑ Plastic SOIC (Gull-wing – 0.331 wide)
❑ 16K x 4 Com. I/O	❑ 85 ns	❑ Plastic SOJ
❑ 8K x 8	❑ Other _____	❑ Other _____
❑ Other _____		

❑ **I need a quotation — call me**

Name: _____
Title: _____
Company: _____
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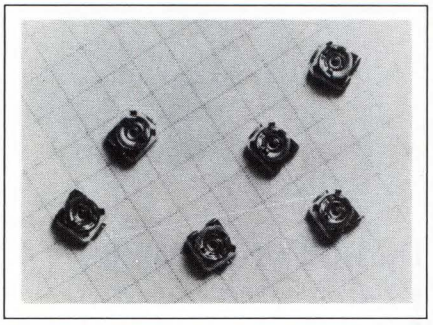
628 East Evelyn Avenue
Sunnyvale, CA 94086
(408) 720-8630

FAX NO: (408) 733-7690

ery, stock to six weeks ARO.

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400. FAX 603-528-1478. TWX 510-298-1127.

Circle No 374



TRIMMER

- *Designed for surface-mount applications*
- *Features a −55 to +125°C operating range*

Measuring only 3×3.1×1.3 mm, the MVR 32 trimmer is designed for surface-mount applications. Employing thick-film technology, the unit offers resistance values ranging from 100Ω to 1 MΩ. The trimmer has a 25V max voltage rating and a 1/16W power rating at 70°C. The unit operates over a −55 to +125°C range and has a ±25% tolerance. The trimmer can accommodate solder reflow processes and is available in tape-and-reel packaging. $0.16 (1000).

Rohm Corp, 8 Whatney, Irvine, CA 92718. Phone (714) 855-2131. TWX 910-595-1721.

Circle No 375

MIXERS/AMPLIFIERS

- *Operate over a 50-MHz to 5-GHz range*
- *Feature single-supply operation*

IAM-81018 and AM-82018 active mixers/amplifiers operate with RF input signals of 50 MHz to 5 GHz and with IF outputs from dc to 1 GHz and dc to 2 GHz, respectively. Both models operate from a 5V supply. The IAM-81018 provides typical RF-to-IF conversion gain of 15

dB, operating from a 0-dBm local-oscillator level. The devices are housed in surface-mount packages that feature gold-plated leads and are fully compatible with conventional 50Ω microstrip systems. IAM-81018, $16; IAM-82018, $25 (1000).

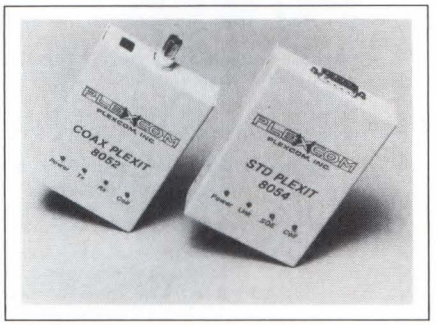
Avantek Inc, 481 Cottonwood Dr, Milpitas, CA 95035. Phone (408) 943-3038.

Circle No 376

TRANSCEIVER

- *Offered in two configurations*
- *Designed for Ethernet*

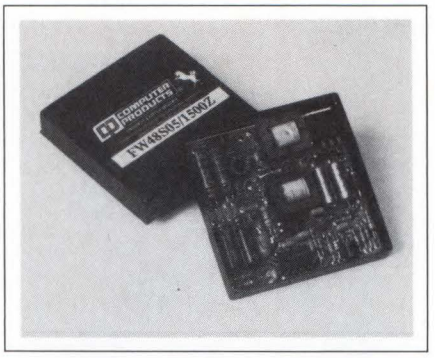
The 10Base-T-Plexit transceiver simplifies the task of implementing the IEEE-802.3 10Base-T twisted-pair interface on an Ethernet controller. In addition to the transmit, receive, and logical-collision-detect functions, the transceiver features power, receive, transmit, collision,



jabber, and link-test LED output controls. Strap-selectable transmit equalization provides flexibility in controlling transmitted wave shape. The transceiver is available in two configurations—the software-reprogrammable 8054 and the hardware-masked 8052. The 8054 has one RJ-45 jack and a male 15-pin attachment-unit interface port; the 8052 features an RJ-45 jack and a BNC connector. 8052, $225; 8054. $295.

Plexcom Inc, 65 Moreland Rd, Simi Valley, CA 93065. Phone (805) 522-3333. FAX 805-583-4764.

Circle No 377



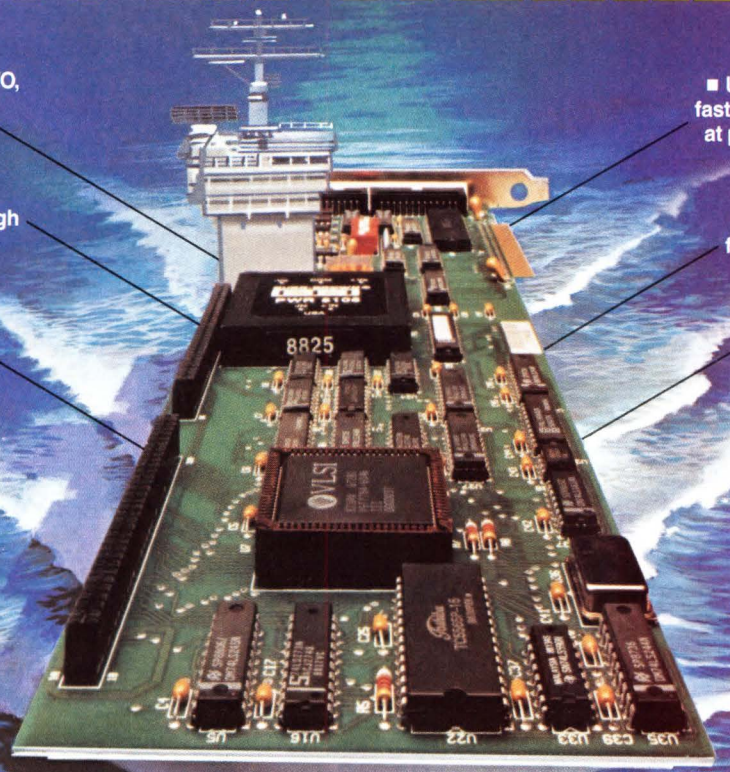
DC/DC CONVERTERS

- *Have a 600,000-hour MTBF*
- *Accuracy equals 4%*

FW Series 7.5W dc/dc converters operate over a 36 to 72V input range and produce single outputs of 5 or 12V. The units feature an 83% efficiency and have a total output accuracy of 4% max for all line-and-load conditions over the full 0

SUPER CARRIER

- 16/8 analog inputs, 16 digital I/O, and 2 16-bit counters (16/32 bit operation)
- Powerful expandability through plug-in modules
- All functions software programmable (SE/Diff, ranges, and gains)
- Unique burst generator allows fast channel-group measurements at programmable sampling rates
- Timebase/rate generator/ frequency-period measurement
- DMA, interrupt driven, or polled modes



More PC Data Acquisition Firepower than any other board.

Burr-Brown has revolutionized PC data acquisition, test, measurement and control with one board. One Super Carrier board that gives you unequalled capability and expandability at a price that blows the competition out of the water.

The software-programmable Super Carrier comes with 16 single-ended/8 differential analog inputs and 16 digital I/O channels on board. Burr-Brown plug-in modules allow expansion to 80 analog inputs, 80 digital I/O channels or 16 analog outputs.

Plus you can add trigger/alarm, simultaneous sample/hold, additional counters, and more. Super Carrier is also supported by a full range of software.

For more information about one of the single most powerful data-acquisition tools you can own, plus a free 288-page Burr-Brown PCI-20000 modular system handbook, call **(602) 746-1111** or write Burr-Brown, 1141 W. Grant Road, MS131, Tucson, AZ 85705.

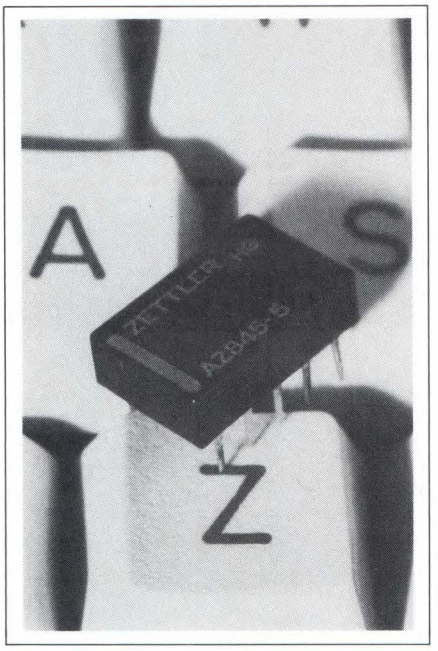
BURR-BROWN®

CIRCLE NO 156

to 71°C operating range. Input-to-output isolation of 500V allows you to develop either a negative or positive output or series-stack the converters to develop higher output voltages. All units feature overvoltage and short-circuit protection. Designed to meet UL94V-0 flammability requirements, the pc-board-mountable converters have bottom standoffs on the package to accommodate aqueous cleaning operations. $44 (1000).

Computer Products, 7 Elkins Ave, Boston, MA 02127. Phone (617) 268-1170.

Circle No 378



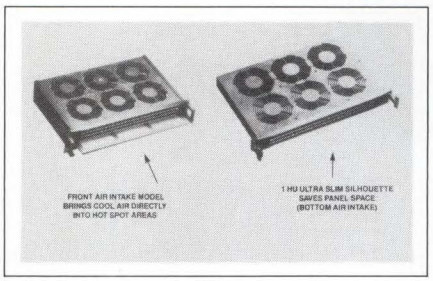
RELAY

- *Provides two 1A changeover contacts*
- *Has a mounting height of only 4 mm*

The AZ 845 dual-in-line relay provides two changeover contacts in a 14 × 9-mm footprint package with a mounting height of only 4 mm. The gold palladium double contacts have 5-μm gold plating to ensure high contact reliability and low contact resistance even with very low contact currents. The contacts can carry a continuous current of 1A and can switch a maximum load of 30W or 60 VA. They have a maximum switching voltage rating of 125V dc or ac. The isolation test voltage between the contacts and between the relay's coil and contacts is 1 kV. The relay is available as a monostable or bistable relay; they respond at a coil power as low as 100 and 150 mW, respectively, for a 2.5 msec pulse. The relays are available with a range of nominal coil voltages from 3 to 24V dc. They are washproof to DIN 40050 protection class IP67 requirements. Approximately DM 7.5 to DM 9 (1000).

Zettler GmbH, Postfach 202626, D-8000 Munich 2, West Germany. Phone (089) 849056. FAX 089-8414942.

Circle No 379



FAN TRAYS

- *You have a choice of air-intake options*
- *All models come prewired*

The Airmatic 300 line of 19-in. fan trays now includes three additional models—the 1HU bottom air-intake model and the 2HU and 3HU front air-intake models. The 1HU is available in versions offering 6, 9, 12, and 15 fan positions. The 2HU and 3HU models include a removable filter and can be located anywhere along the vertical panel of a cabinet. All three models feature fans with a 79.5-cfm capacity, and all three are constructed from two structural foam halves that provide individual fan compartments to isolate noise and vibration. Each compartment comes prewired whether it holds a fan or not. Each fan is plug terminated to ease field maintenance. Unused positions come with a foam and metal insert. 6-position 1HU model with 1 fan, $173.29.

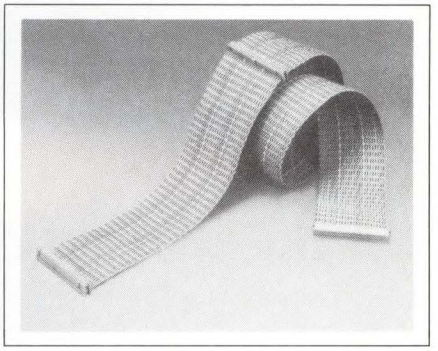
Dacobas Inc, 1890 N Voyager Ave, Simi Valley, CA 93063. Phone (805) 526-7733. FAX 805-584-8371.

Circle No 380

WOVEN CABLE

- *Offers as many as 64 conductors*
- *UL and CSA approved*

The Econo-Mizer IDC-compatible flat-woven cable employs stranded conductors to provide longer flex life in applications involving repeated bending. The cable is designed to accept IDC (insulation displacement connector) terminations without the need for special tools. The cable is available with 16 to 64 conductors spaced on 50-mil centers. Alternating conductors feature a red/blue color code. Available in 300-ft reels, the cable is UL and CSA approved. $0.9964 (1000 ft) for a 26-conductor cable.



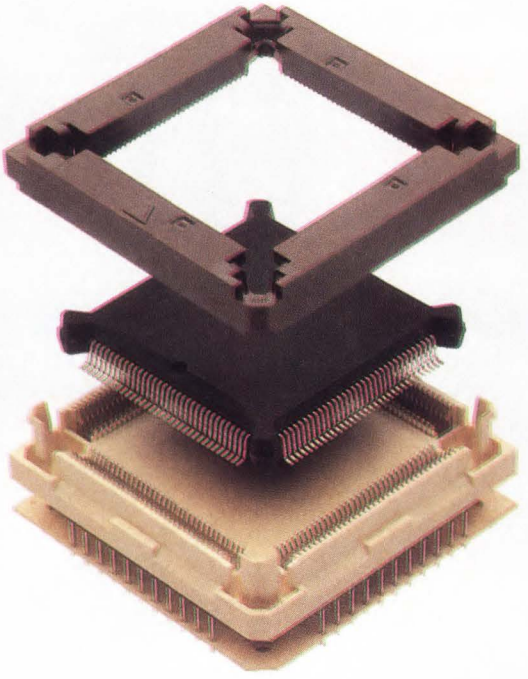
Woven Electronics, Box 667850, Charlotte, SC 28266. Phone (803) 963-5131. TWX 810-287-2091.

Circle No 381

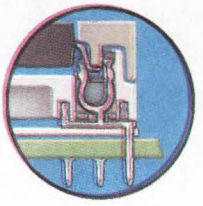
One small step for PQFPs. One giant step for service

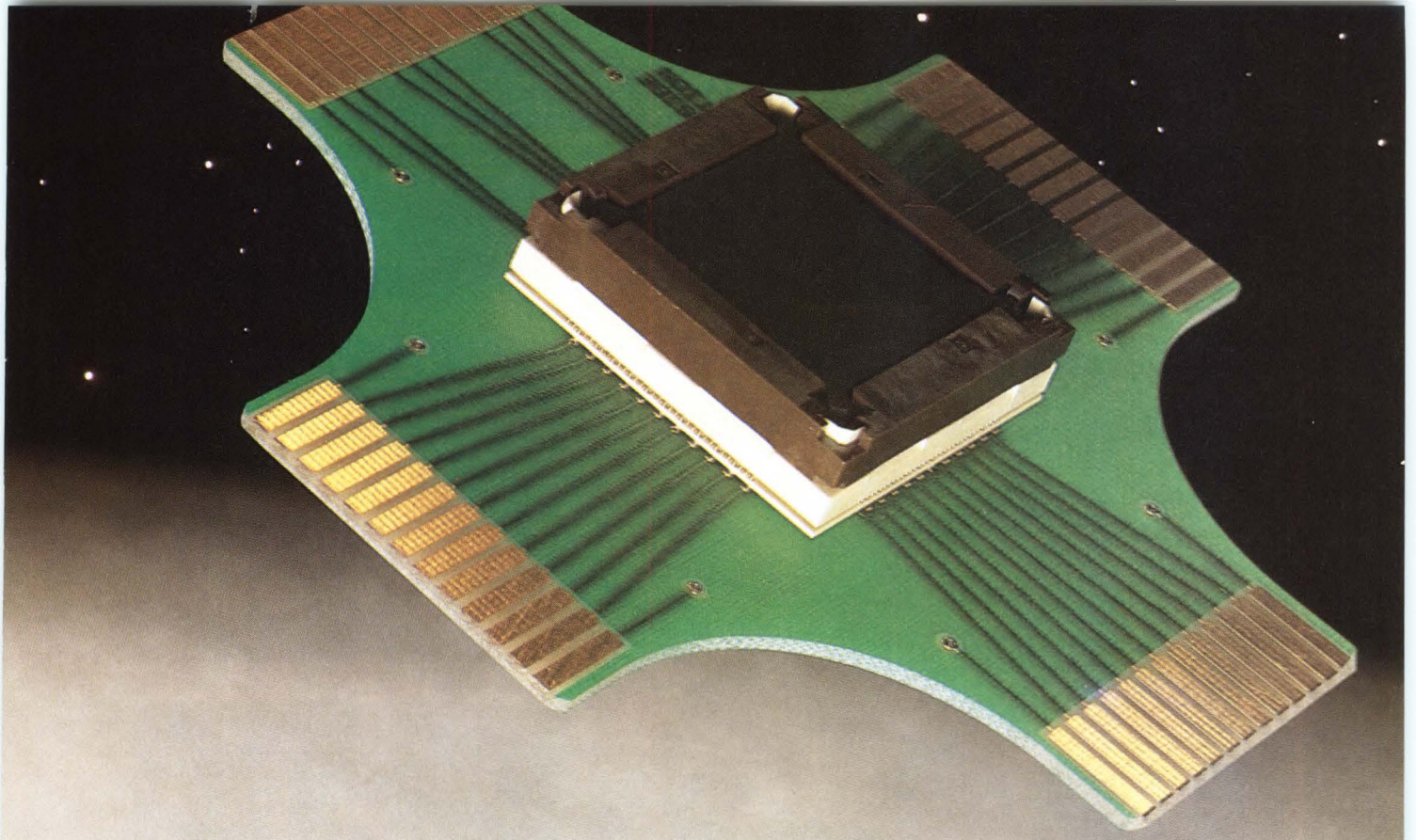
Introducing the right technology at the right time—our two-piece Micro-Pitch sockets for JEDEC plastic quad flat pack ICs.

Our patented low-profile (.400″) Micro-Pitch sockets are a remarkably simple, safe way to mount high-speed, high-performance PQFPs. And their simplicity—in engineering, and in the minimum use of material—brings them to you at a remarkably low price.



PQFP as easy as 1-2-3. .025″ centerline Micro-Pitch sockets ease handling, automate readily. High-speed contacts provide oxide cleaning wipe action, 200 grams normal force for positive mating. Footprint on .075″ x .100″ three-row grid.





and manufacturing.

The cover aligns IC leads for easy insertion into the base. It also protects the leads during handling. In fact, your PQFP supplier can insert chips into covers at his site, and send completed units to you. Result: hands-off installation.

Our high-speed tin-plated contacts provide .020″ to .030″ of contact cleaning wipe during insertion, and a normal mating force of 200 grams on each contact. Very positive engagement. And just the kind of quality engineering you can count on from AMP.

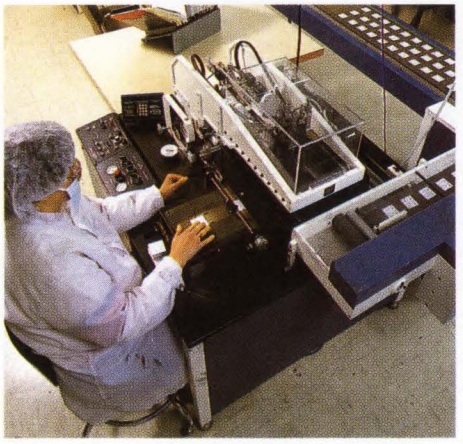
Micro-Pitch sockets have been designed with automation in mind, as well. They're fully polarized cover-to-base, and base-to-board, and compatible with vacuum pickup, for fast robotic implementation.

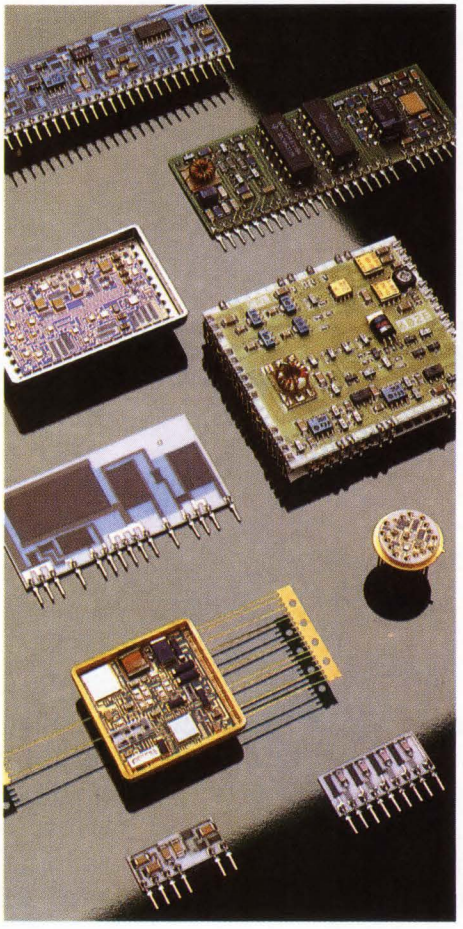
With today's chip costs, and with the high quality and low installed cost AMP is known for, this is one option you'll want to pick up. Fast.

For technical literature and more information, call the AMP Product Information Center at 1-800-522-6752 and ask about Micro-Pitch Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

Application-Specific Hybrid Packaging Solutions.





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For our Capabilities Catalog, write to: Philips Circuit Assemblies, A Division of North American Philips Corporation, Corporate Advertising, 2001 W. Blue Heron Blvd., P.O. Box 10330, Riviera Beach, FL 33404.

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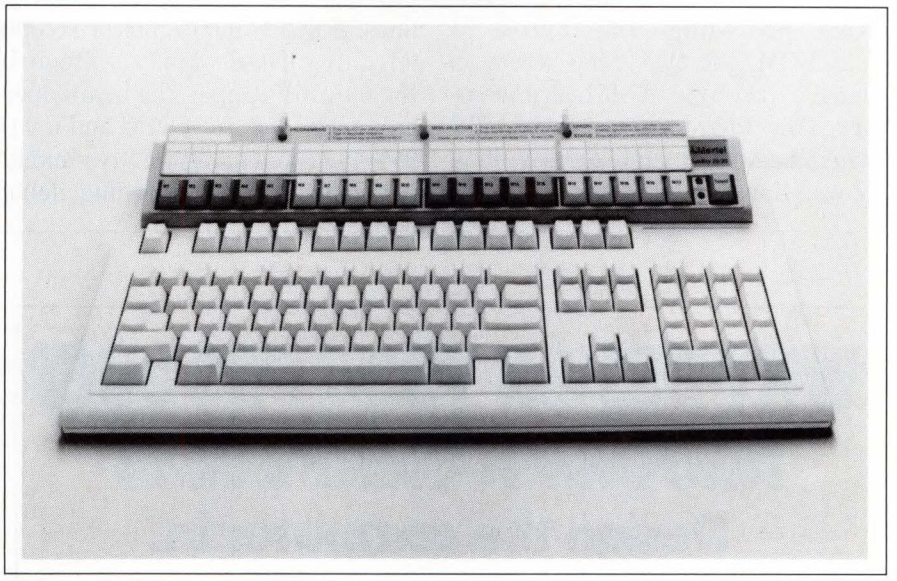
NEW PRODUCTS

COMPUTERS AND PERIPHERALS

MACRO STORAGE

- *System stores 8000 keystrokes*
- *Compatible with IBM PC, PC/XT, PC/AT, and PS/2*

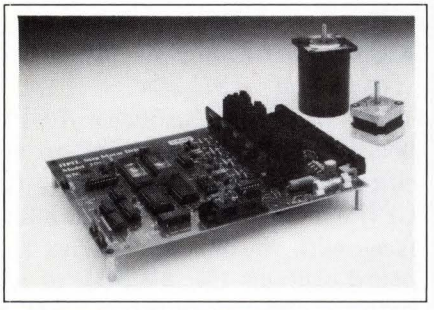
The AutoKey 20/20 data-entry device provides 400 programmable function keys for an IBM PC, PC/XT, PC/AT, or PS/2 compatible keyboard. The unit mounts in the upper portion of the keyboard. The device contains a μP and lithium-battery-backed memory, which stores as many as 8000 keystrokes. When you press the select key the unit memorizes a series of keystrokes without program interruption. Pressing a macro storage key saves the keystroke sequence in memory for as long as 10 years. Pressing the macro key again sends the keystroke sequence to the computer as if you typed it. The unit stores as many as 400 sequences.



A flip-down legend lets you document each macro sequence in memory. The unit operates with DOS, OS/2, and Unix operating systems. AutoKey 20/20, $289; AutoKey 40, reduced-capacity version, $139.

Mextel Inc, 159 Beeline Dr, Bensenville, IL 60106. Phone (312) 595-4146. FAX 312-595-4149.

Circle No 401



STEPPER DRIVER

- *Drives 4-phase motors from 0.15 to 4000 steps/sec*
- *Controls four motors requiring 24V and 5A*

The Model 201 stepper-motor driver board conforms to the requirements of the Hewlett Packard Interface Loop (HPIL). The HPIL permits 31 devices to operate from one driver, allows loop distances of 100m, and requires electrical isolation via pulse transformers. The unit can drive as many as four 4-phase stepper motors requiring 24V and 5A running at speeds from 0.15 to 4000 steps/sec. It controls each motor one at a time via onboard selection drivers. You can control the stand-alone board from a computer with an HPIL port or an IEEE-488 controller with an adapter. The hardware consists of a stepper motor indexer, a translator, a driver, a home function, and a step-counting function. $895. Delivery, stock to 60 days.

Interloop, 706 Charcot Ave, San Jose, CA 95131. Phone (408) 922-0520. TWX 910-240-0128.

Circle No 402

OPTICAL DISKS

- *Erasable and rewritable and store 644M bytes*
- *Compatible with Hitachi's OD112-1 optical-disk drive*

The two models of this erasable and rewritable optical disk are available for Hitachi's OD112-1 optical-disk drive. Each magneto-optical 5¼-in. disk can store 644M bytes of data on both sides. The model OC112G-2 has a glass substrate, and the model OC112P-2 has a plastic polycarbonate substrate. The disks achieve a high S/N ratio and a high degree of reliability through the use of a multilayer recording film. The disks have a track capacity of 17.4k bytes, a track density of 16,000 tpi, and a linear density of 24,000 bpi. Each disk has 18,751 tracks with 17 sectors/track. OC112G-2, $400; OC112P-2, $250.

Maxell Corp of America, 22-08 Route 208, Fairlawn, NJ 07410. Phone (201) 794-5900.

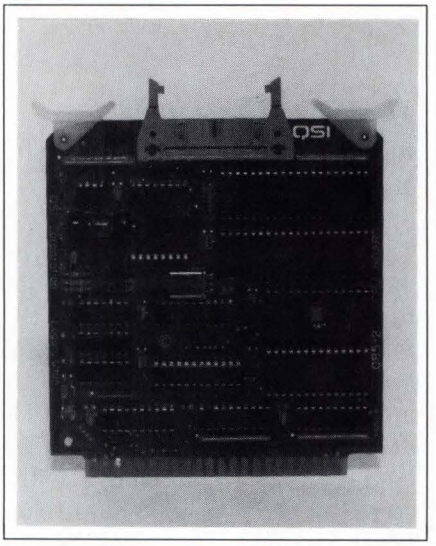
Circle No 403

C-44 CPU BOARD

- *Has a 6-MHz 80C85 μP and 64k bytes of memory*
- *Provides 22 digital I/0 lines and two serial communications lines*

The Q85-2 stand-alone CPU board for the C-44 bus is compatible with any expansion or peripheral board for the C-44 bus. The board con-

tains a 6-MHz 80C85 μP and 64k bytes of memory—32k bytes of EPROM and 32k bytes of RAM. Also providing 128 bytes of EEPROM, the Q85-2 can access as much as 1M byte of off-board memory. The board consumes 96 mW when operating and 24 mW in a power-down mode. Other board features include 22 digital I/O lines, a 14-bit timer, and a UART that provides two serial communications lines. A switching regulator accepts an unregulated supply voltage in the 6 to 16V range. The board operates from −40 to +85°C and a 0 to 98% noncondensing relative-humidity range. Board, including debug monitor and floppy-disk drive with source code, $290.



QSI Corp, 1740 Research Park Way, Logan, UT 84321. Phone (801) 753-3657. TLX 887430. FAX 801-753-3822.

Circle No 404

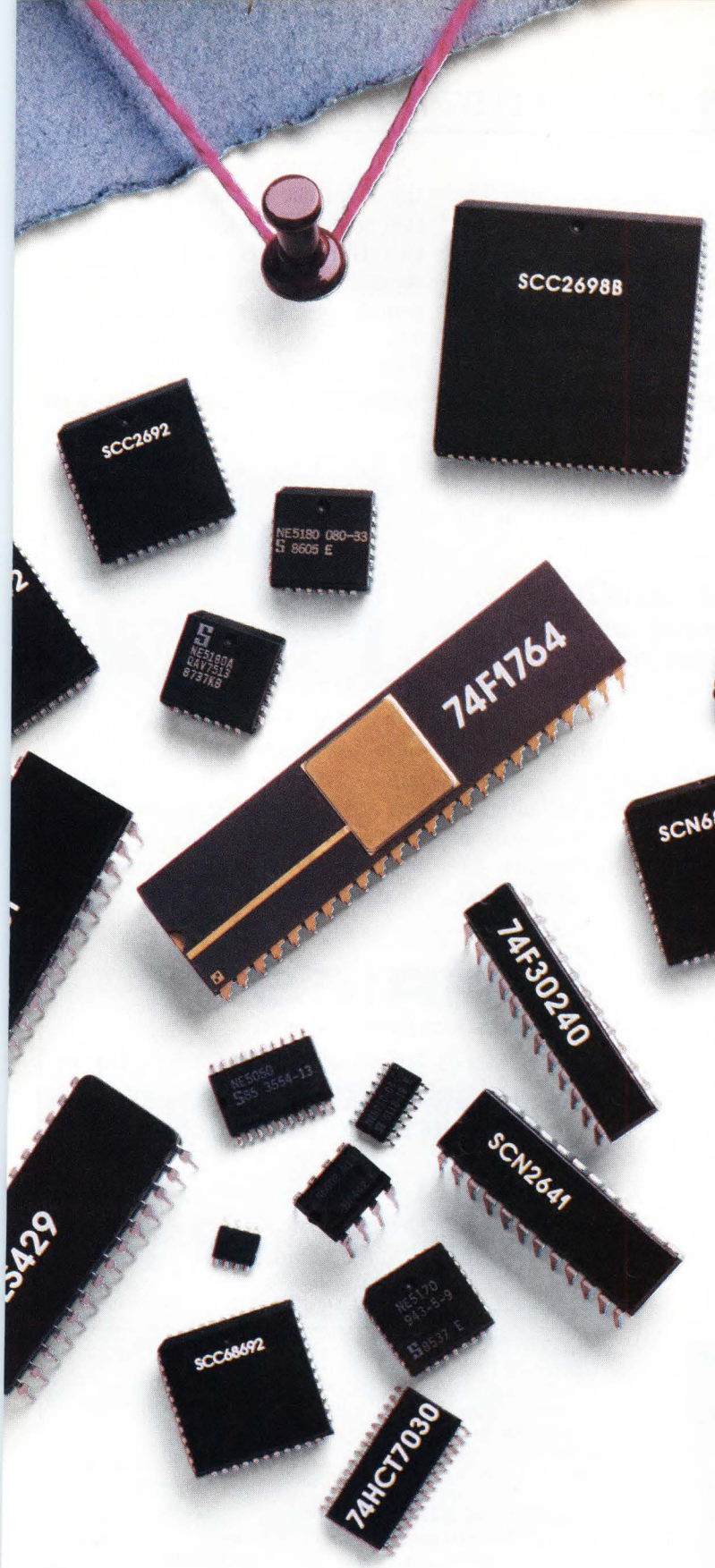
80386SX CPU BOARD

- *Runs at 16 MHz*
- *Contains as much as 8M bytes of DRAM in SIMMs*

The SCX386-16 is an 80386SX CPU board for an industry-standard architecture passive backplane. Its CPU operates at 16 MHz and interfaces with the bus at 8 MHz. The board contains 1M, 2M, 4M, or 8M bytes of 100-nsec dynamic RAM in SIMMs. You can configure the RAM for either page-mode access or in a 2-way interleave arrangement. It comes with either the Phoenix or Award BIOS, and it has a socket for an optional 80387SX coprocessor. The device consumes 35W and has an onboard buzzer or connections for an external speaker. It comes with a 2-year limited warranty. With 1M byte of RAM, $700 (OEM qty).

Mylex Corp, 47650 Westinghouse Dr, Fremont, CA 94539. Phone (415) 657-7667. FAX 415-656-7857.

Circle No 405



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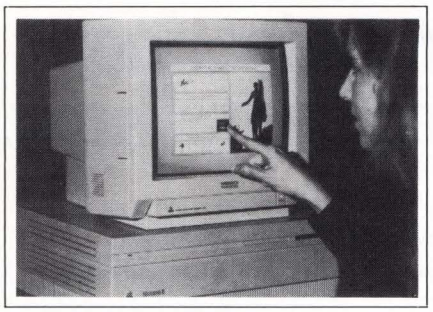


TOUCH MONITOR

- *Displays 256 colors from palette of 16M colors*
- *Provides 640×480-pixel resolution*

The Mac 'n Touch, a touchscreen monitor for Mac II, MacIIx, and Mac IIcx, comes with a controller, a cable, and a software driver, allowing it to be used with all Macintosh software, including HyperCard. The monitor interfaces with the Mac II through the Apple Desktop bus and can display 256 colors from a palette of 16M colors with a resolution of 640×480 pixels. The 14-in. display has a 0.29-mm dot pitch and sits on a tilt-and-swivel stand. The monitor uses analog capacitive sensing to provide 1024×1024 touch points and can convert 60 touch points/sec. $1545.

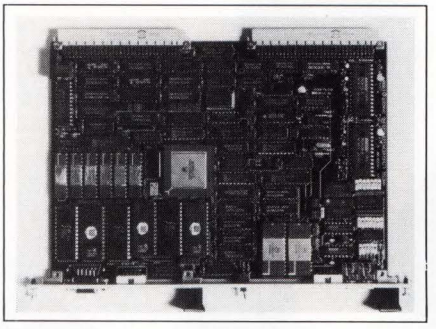
MicroTouch Systems Inc, 10 State St, Woburn, MA 01801. Phone (617) 935-0080. TLX 530264. FAX 617-935-0133.

Circle No 406

VME DSP BOARD

- *Uses a 20-MHz 56001 DSP chip and 8k words of RAM*
- *Contains two 16-bit ADCs and two DACs*

The 56001 VME Board, a 6U DSP board for the VMEbus, has Motorola's 20-MHz 56001 DSP chip, 8k words of RAM, and 8k words of EPROM. Both memories are expandable to 32k words. In addition, the 56001 has two analog inputs and two analog outputs that connect to two 16-bit ADCs and two DACs, respectively. The converters can sample as fast as 200 kHz/channel. The board also contains two 56200 FIR filter processors, which are configurable as independent FIR



filters or adaptive filters. The board comes with Sun 3 Unix device drivers and monitor/debugger software that communicates with an IBM PC via an RS-232C port. The company provides Motorola's Assembler/

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Working with Small AlphaNumeric (SAN) displays used to impose certain compromises.

You had to put up with the high power consumption and heat dissipation of bipolar technology, which required expensive heat sinks and PCB designs. And you paid dearly for the high cost of ceramic packaging and the lack of price competition.

Now the company that brought you the first CMOS SANs expands the family of Siemens Advanced Model SAN (SAMSAN) displays in a plastic package. These pin-for-pin replacements for Hewlett-Packard SANs offer a wider range of operating temperatures than HP's commercial bipolar ceramic device. For as little as half the price.

And SAMSAN LED displays are built with CMOS technology. So their lower power consumption and heat dissipation make thermal management simple.

Siemens Components, Inc. Optoelectronics Division, 19000 Homestead Road, Cupertino, CA 95014. (408) 725-3423.

SAMSAN Features

- .15" and .20" character heights in red, HER, green, and yellow.
- Commercial plastic package: −40°C to +85°C.
- Drop-in replacement for many existing ceramic applications.
- CMOS driver offers 30% lower power consumption and 25 times less quiescent power than bipolar. Heat sink not required for most applications.
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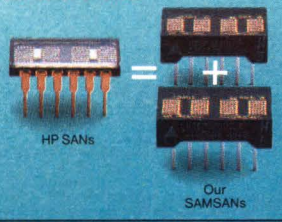
Siemens Super SAN Display Swap.

We're sure you'll agree that our SAMSANs are the perfect replacement for HP SANs. So sure that if you'll send us a ceramic HDSP 2000 type display, we'll send you *two* plastic SAMSANs to replace it. Mail your request on your letterhead to R. Waltonsmith. Be sure to specify your color choice.



Distributors: Advent Electronics, Inc., Almo Electronics, Hall-Mark, Insight Electronics, Marshall, Summit, Western Microtechnology.

Siemens...
Practical Solutions by Design.

Linker + Simulator separately, as well as a C compiler for the IBM PC and Sun 3 Unix systems. Board and software, $5995.

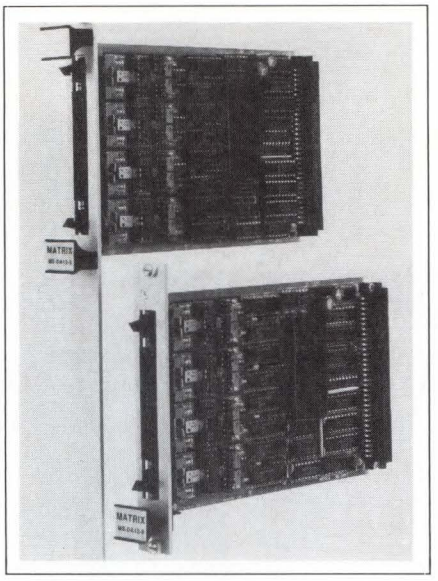
Spectrum Signal Processing Inc, 460 Totten Pond Rd, Waltham, MA 02154. Phone (800) 323-1842; in MA, (617) 890-3400. FAX 617-890-0976.

Circle No 407

VME DACs

- *Two, four, six, or eight analog output channels*
- *12-bit resolution and 25-μsec settling time*

The MS-DA12 Series 12-bit D/A converter boards for the VMEbus come with two, four, six, or eight analog voltage outputs. An optional voltage-to-current adapter configures the output as current loops. An onboard jumper selects a 0 to 5V, 0 to 10V, ±5V, or ±10V output range. You can use an external reference of ±10V between 0 and 8 kHz as a multiplier for the boards. The settling time is 25 μsec typ and 30 μsec max to reach ½ LSB of the full-scale step value. The devices are compatible with revision C.1 of the VMEbus specification, and they respond either as A16:D16 or as A16:D08 slaves. You can configure the boards to respond to either or both the short nonprivileged access (AM code $29) or short supervisory access ($2D) code. From $395; 2-channel voltage-to-current adapter, $95.



Matrix Corp, 1203 New Hope Rd, Raleigh, NC 27610. Phone (919) 833-2000. FAX 919-833-2550.

Circle No 408

ARCNET BOARD

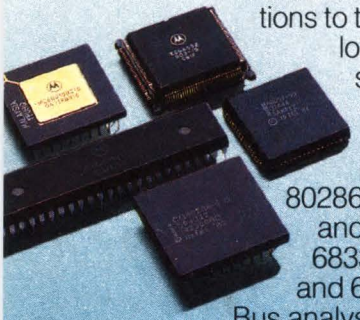
- *Interfaces PCs to Arcnet LANs*
- *Has a 2k-byte data buffer, and a switch- or software-controlled node identifier*

The ARC250 Arcnet LAN card for the IBM PC, PC/XT, PC/AT or compatible computers allows you to select the network node identifier via switches that are accessible on

Text continued on pg 278

TEK'S $2995 LOGIC ANALYZER. NOW WITH SUPPORT FOR MORE THAN 20 MICROPROCESSORS.

Only the Tek 1230 lets you start with an entry-level logic analyzer—then, as time goes on, add channels and draw from a comprehensive list of 8- and 16-bit micro support.

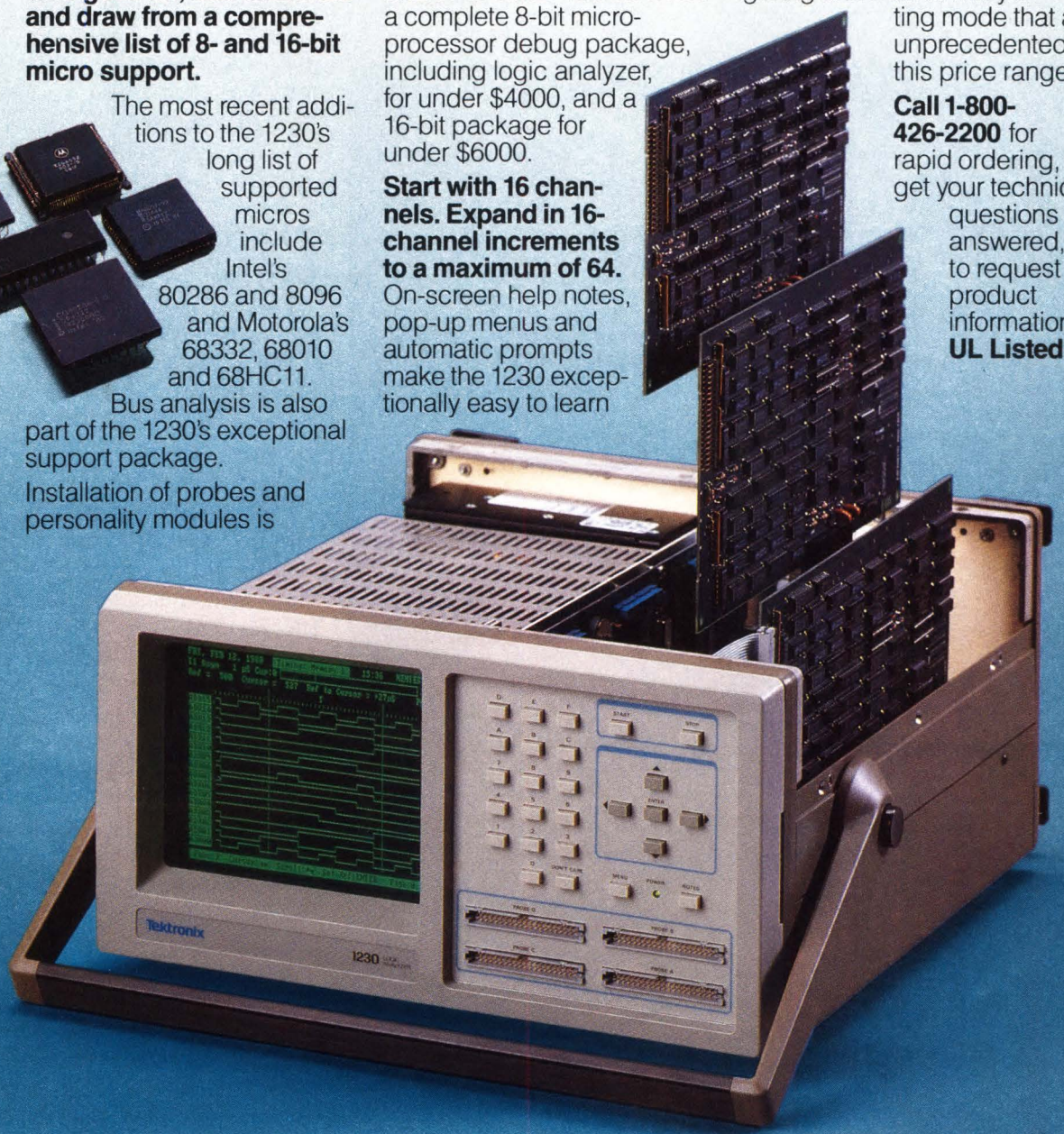


The most recent additions to the 1230's long list of supported micros include Intel's 80286 and 8096 and Motorola's 68332, 68010 and 68HC11. Bus analysis is also part of the 1230's exceptional support package.

Installation of probes and personality modules is effortless; the disassembly itself is more complete and informative than anything else in its class. You can have a complete 8-bit microprocessor debug package, including logic analyzer, for under $4000, and a 16-bit package for under $6000.

Start with 16 channels. Expand in 16-channel increments to a maximum of 64. On-screen help notes, pop-up menus and automatic prompts make the 1230 exceptionally easy to learn and use. Yet you can access features like four 2K deep memories, sophisticated triggering and built-in babysitting mode that are unprecedented in this price range.

Call 1-800-426-2200 for rapid ordering, to get your technical questions answered, or to request product information. **UL Listed**



To order now, call (800) 426-2200. VISA, MasterCard accepted.

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Circle 7 for literature

Circle 8 for sales contact

the card's rear panel or via software control. The card also incorporates LEDs to indicate the network status and the transmission of network data. The card uses Standard Microsystems' COM9026 Arcnet controller and has a 2k-byte RAM to buffer data before transmission or after reception. This buffer RAM is dual-ported to the COM9026 controller and the PC bus. The board also has three byte-wide EPROM sockets that can hold boot software for diskless systems or special networking software. A PAL-controlled memory-mapping scheme allows you to jumper-select the board's address decoding so that the card occupies between 16 and 64k bytes of the PC's address space. By using custom PALs, you can extend the board's memory address space to 128k bytes. To eliminate ground-loop problems, the board's Arcnet transceiver connects to the Arcnet LAN via a BNC connector that has an isolated ground connection. Approximately £295.

DSP Design, Unit 1, Apollo Studios, Charlton Kings Rd, London NW5 2SB, UK. Phone 01-482-1773. FAX 01-482-1779.

Circle No 409

MEMORY CONTROLLER

- *Uses one ISA bus slot for three different disk drives*
- *Its μP and pipelined data path transfer data at 2.5M bps*

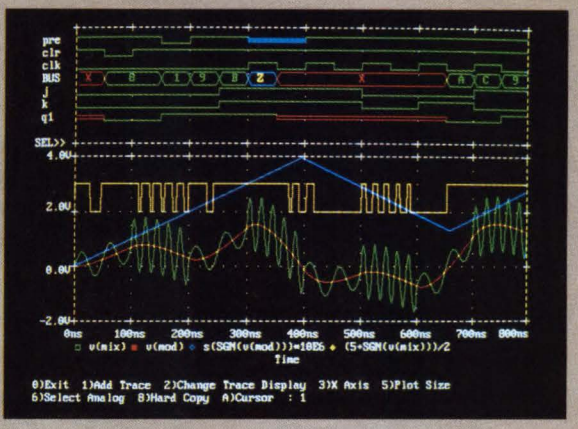
The HyperStore 816 mass-storage controller for the 16-bit ISA bus can control two 3½- or 5½-in. floppy-disk drives and two ST506/412 MFM-compatible hard-disk drives. The unit can also support optical-disk drives and magnetic-tape devices using a daughter board called the Mediadapter. The controller contains a 16-bit, 10-MHz Z280 μP and from 512k to 4M bytes of cache memory. This combination provides an elastic buffer between the host and the drives, allowing them to transmit data at their natural speeds. The host can transfer data using the 8- or 16-bit path provided by the extension connector on the ISA bus. The CPU's 3-stage pipeline architecture transfers data to a drive at 2.5M bytes/sec. The board can also tolerate five different types of faults, ranging from bit errors to media damage. Board with 512k bytes of cache memory, $849; Mediadapter with MFM encoding, $395; Mediadapter with RLL 2,7 encoding, $435.

Perceptive Solutions Inc, 1509 Falcon, Suite 104, DeSoto, TX 75115. Phone (800) 343-0903; in TX, (214) 224-6774. FAX 214-228-1430.

Circle No 410

PSpice

The Standard for Analog Circuit Simulation



Mixed-mode waveform display from Probe

Two years ago, MicroSim introduced the technology for simulating mixed analog/digital circuits. Now, this capability is available in the Digital Simulation extension for PSpice. It does true mixed-mode simulation of circuits — including feedback loops between analog and digital sections.

At the core of the Digital Simulation extension is a multi-state, event-driven logic processor. It efficiently calculates logic transitions and propagation delays — there are no performance compromises to do mixed-mode simulation. Also included with the option is a model library of standard TTL and CMOS logic devices.

Once the simulation is finished, viewing the results is easy. As you can see from the photo above, the Probe option for PSpice can display analog and digital waveforms together.

Introduced five years ago, MicroSim's PSpice is used by more engineers, and has more copies sold, than all other SPICE programs combined. Here are some of the features which have made PSpice so popular:

- Standard parts libraries of over 2200 analog models: diodes, bipolar transistors, small-signal JFET's, power MOSFET's, opamps, voltage comparators, and transformer cores.
- GaAs MESFET devices, BSIM MOS model.
- Non-linear transformers modeling saturation, hysteresis, and eddy current losses.
- Ideal switches for use with, for example, power supply and switched capacitor circuit designs.

Besides Digital Simulation, these other PSpice options are also available:

- Analog Behavioral Modeling, which allows arbitrary transfer functions for devices, either by formula or look-up table. This can be done in both the time and frequency domains. In time domain the devices may be non-linear as well as linear.
- Monte Carlo analysis calculates the effect of parameter tolerances on circuit performance. This includes statistical, sensitivity, and worst case analyses.
- The Probe "software oscilloscope" provides interactive viewing of simulation results and post-processing data reduction (see photo above).
- The Parts parameter extraction program, allows you to extract a device's model parameters from data sheet information.

PSpice is available on these computers:

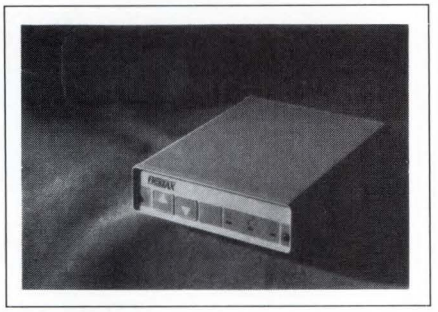
- The PC family, including the PS/2, and including both DOS and OS/2.
- The Macintosh II.
- The Sun 3 and Sun 4 workstations.
- The Apollo DN3000 and DN4000 workstations.
- The VAX/VMS family, including the MicroVAX.

Each copy of PSpice comes with our extensive product support. Our technical staff has over 100 years of experience in CAD/CAE and our software is supported by the engineers who wrote it.

For our free information packet, including a PSpice demo diskette, call us at (714) 770-3022 or **toll free** (800) 826-8603. Find out for yourself why PSpice has become the standard in circuit simulation.

MicroSim Corporation **20 Fairbanks • Irvine, CA 92718 USA • Telex 265154 SPICE UR**

CIRCLE NO 168



FAX MODEM

- *Sends and receives a fax at 9600 bps*
- *Compatible with CCITT Group 3 and AppleFax protocols*

The FlexFAX fax modem for the Macintosh II, Plus, and SE computers is 100% compatible with the AppleFax fax modem. It can automatically select AppleFax, CCITT Group 3, or FlexFAX protocols and send and receive a fax at 9600 bps. The modem provides automatic fallback to V.29, V.27ter, and V.21 data rates. The unit operates in the "background" without host intervention. A pass-through mode liberates the modem port for use by other peripherals. Other features include storage for fax directories, transmission of multiple documents to multiple locations, and diagnostic capability. The unit operates as a 2400-, 1200-, or 300-bps modem conforming to the CCITT V.22bis, V.22, V.21, and Bell 212A/103 specifications. As a data modem, it can transmit data half or full duplex using the Hayes AT command set. $1095.

Circuit Research Corp, 4 Townsend W, Suite 3, Nashua, NH 03063. Phone (603) 880-4000.

Circle No 411

VME SBC

- *20-MHz RTX-2000 μC on a single-height board*
- *64k bytes of EPROM and 64k bytes of battery-backed SRAM*

The V401 single-height, single-board computer for the VMEbus contains a 20-MHz Harris RTX-2000 microcomputer, 64k bytes of EPROM, and 64k bytes of battery-backed CMOS SRAM. Because the μC offers a 100-nsec 16×16-bit multiplier, a 400-nsec interrupt latency, and a 2-μsec context switching time, the board is well suited for real-time applications. The board also has a 16-bit parallel I/O port, two RS-232C ports, and a VMEbus master and interrupt handler. The data-transfer rate is 6M bytes/sec to the VMEbus and 20M bytes/sec to the parallel I/O port. V401-0, $1308; V401-1, $963 (100); development package with Forth operating system, optimizing compiler, real-time debugger, and monitor, $1195.

VME Inc, 542 Valley Way, Milpitas, CA 95035. Phone (408) 946-3833. FAX 408-945-1173. TWX 910-240-9707.

Circle No 412

PRINTER ADAPTER

- *Interfaces Q Bus to Tektronics 4693D printer*
- *Q Bus board compatible with DEC LPV11 software*

The GT361T adapter board for DEC's LSI-11 and MicroVAX-11 Q Bus computers provides a parallel interface for the Tektronix 4693D color-image printer. The board contains a configuration register and a line-printer data buffer and is compatible with DEC LPV-11 software. The device also supports four levels of interrupts and 22-bit addressing with selectable vector and base addresses. The printer generates an interrupt when it's ready for the next character or to signal an error such as no paper, a bad connection, or a mechanical fault. The single dual-height board measures 5.2×8.9 in. and draws 2A from the 5V supply. $395.

Computer Products Inc, Measurement & Control Div, 2900 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-5500. TWX 510-956-9895. FAX 305-979-7371.

Circle No 413

APPLICATION SPECIFIC PLASTICS FROM PHILLIPS 66

CONNECTING VALUE WITH PERFORMANCE

Performance and value. You can get both with Aspect™ TPPE from Phillips 66. This engineering thermoplastic polyester gives you:

- Improved flow and processability to help you mold complex, intricate parts—easily and precisely, at low injection pressures.
- Long-term thermal performance —retaining over 50% tensile strength after 17 weeks at 220° C.
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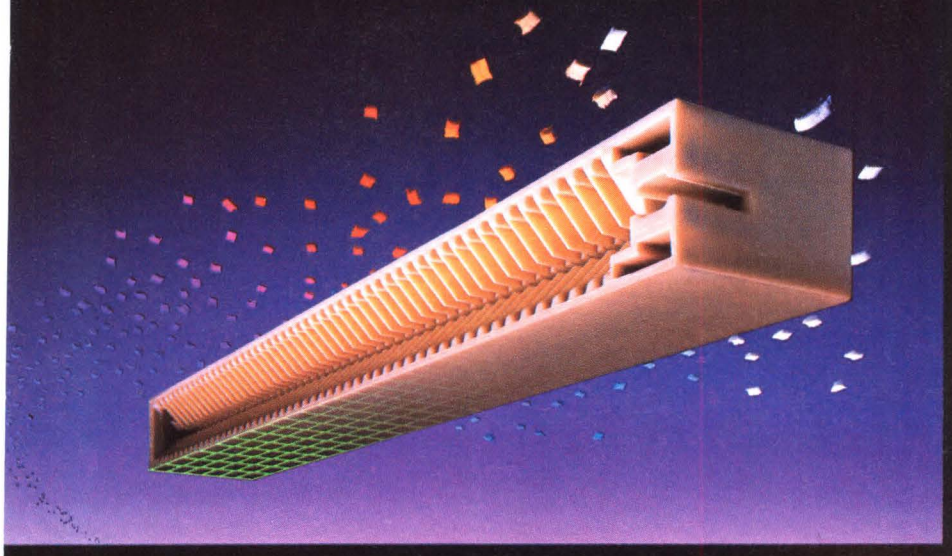
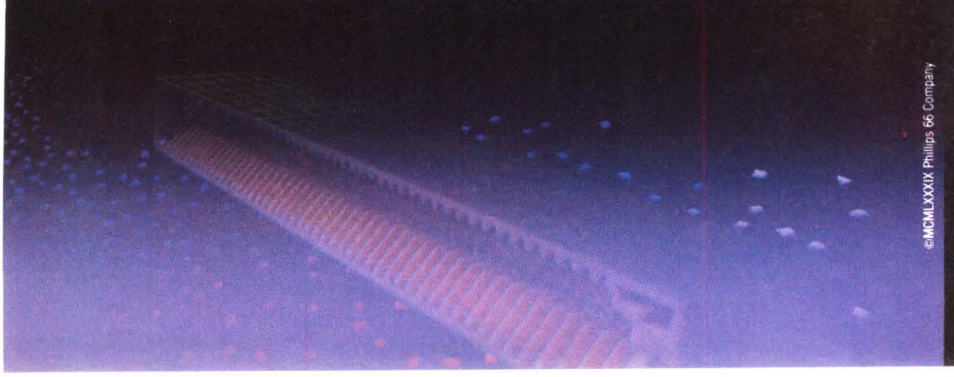
Aspect™ TPPE is ideal for applications such as high density interconnectors; thin, intricate and hard-to-mold bobbins; terminal blocks; and fuse holders.

With Application Specific Plastics such as Aspect™ TPPE from Phillips 66 you can take advantage of the expertise of the Phillips 66 Plastics Technical Center . . . its research and development and advanced molding facilities, the computer-aided design capabilities, the experienced staff, and more.

Phillips 66 offers other Application Specific Plastics for your electrical/electronic needs: Ryton® PPS, Ryton® S PPSS, and Crystalor™ PMP. For more information call toll free ***1-800-53-RESIN***. Or Telex #492455.





ASPECT™ TPPE

PLASTICS WITH POWER TO WIN™

PHILLIPS 66

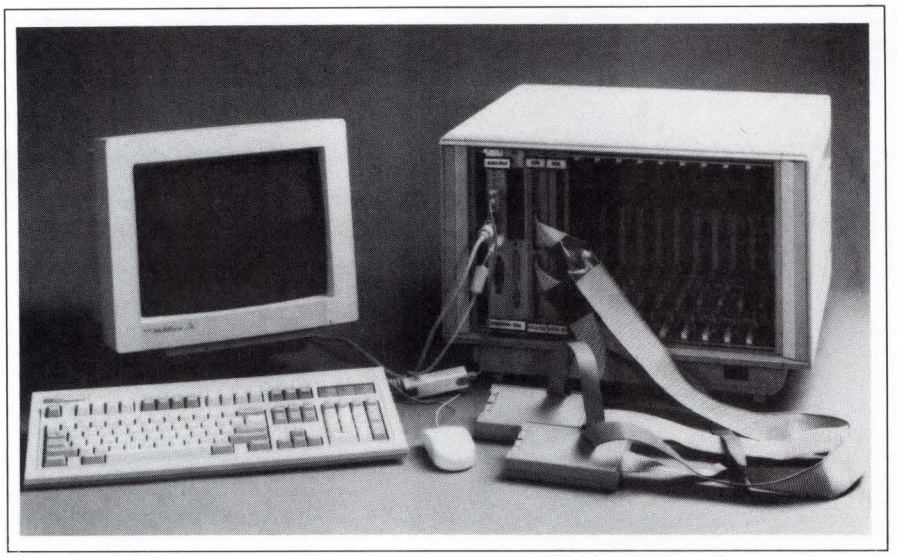
CIRCLE NO 167

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

VXI-BASED TESTER

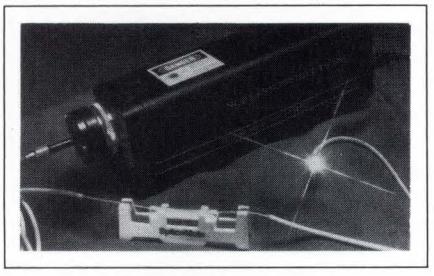
- *Performs stimulus/response testing on 96 channels or more*
- *Has 32k bits of RAM per channel and 50-MHz clock rate*



Based on the VXI Bus (VME eXtensions for Instrumentation), the Final Analysis system is a modular stimulus/response tester for pc boards and ASICs. The vendor has integrated a module especially designed for the system with a VXI card cage and an 80386-based computer in a VXI module. The computer includes a 3½-in. 1.44M-byte floppy-disk drive, a 40M-byte hard disk, two serial ports, a parallel port, an IEEE-488 port, and a VGA color monitor. The computer also performs "slot-0" control functions for the bus. The test module includes 96 bidirectional channels, each of which is backed by 32k bits of RAM that you can expand to 64k bits. The maximum clock rate is 50 MHz; the maximum data rate is 25 MHz. You can expand the system to 384 channels by adding test modules. From $32,000. Delivery, 90 days ARO.

Kikusui International Corp, 19601 Mariner Ave, Torrance, CA 90503. Phone (800) 545-8784; in CA, (213) 371-4662.

Circle No 420



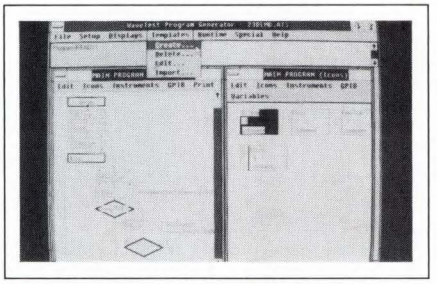
FIBER INSPECTOR

- *Provides visual indication of optical-fiber faults*
- *Uses low-power HeNe laser*

The Fiber Visualizer focuses red light from a compact, low-power helium-neon laser onto an optical-fiber connector. The Class II laser is safe provided you don't stare into the beam. You can use the 1.1-lb. unit to tell whether fibers are correctly aligned at a splice: When they are not, you see a red glow; when alignment is correct, the glow disappears. You can also use the instrument to test whether a cable is correctly installed in a connector, to locate breaks and microscopic bends in a fiber, and to trace individual fibers within bundles. The vendor supplies different versions of the unit for various connector types. $1195.

Norland Products Inc, Box 145, North Brunswick, NJ 08092. Phone (201) 545-7828.

Circle No 421



IEEE-488 SOFTWARE

- *Includes database of more than 100 instruments*
- *Automatically generates test programs and documentation*

Version 2.5 of the Wavetest software package runs under Microsoft Windows on IBM PC/ATs and compatible computers. This package permits you to operate IEEE-488-based instruments, and, without programming expertise, to design and document programs that control the instruments. A code generator within the program creates code that you can execute with only a run-time version of the program resident. Beginning with this version, the software supports 8087 and 80287 math-coprocessor chips and allows programs as large as 2M bytes. It also allows you to create, import, and link subroutines. The software explicitly supports more than 100 IEEE-488-based instruments from a number of vendors. You can add support for additional instruments. $3990; run-time version, $1500; upgrade for users of earlier versions, $495.

Wavetek Corp, 9045 Balboa Ave, San Diego, CA 92123. Phone (619) 279-2200.

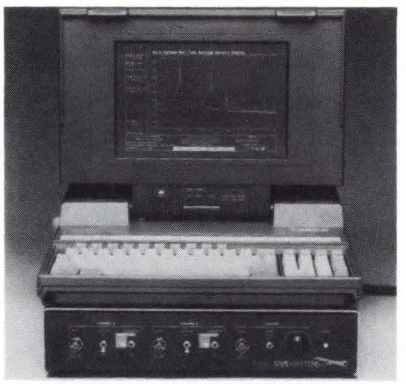
Circle No 422

Oops... You Just Keyed The Transmitter Into Your Spectrum Analyzer

Costly and time consuming repairs due to accidental overload of your spectrum analyzer are now history. Rest easy...Marconi's 2382 uniquely features 50 watt front end protection. It also features full automatic self calibration, providing the industry standard for total level accuracy of +1 dB... including the integral tracking generator. That's right — you can count on this level of accuracy anywhere on the screen. To find out all the features of the 400 MHz and 4.2 GHz 2380 series spectrum analyzers, or to arrange for a demo, call toll-free 800 233-2955, in NJ (201) 934-9050 or write Marconi Instruments, 3 Pearl Ct., Allendale, NJ 07401.

CIRCLE NO 169

TEST & MEASUREMENT INSTRUMENTS



FFT ANALYZER/SCOPE

- *Simultaneously acquires two channels at 20M samples/sec*
- *Displays 1024-point FFTs at a rate of 10/sec*

The R45 is a complete portable 2-channel scope and FFT spectrum analyzer whose input sensitivity scales from 10 mV to 50V/division. The unit consists of a laptop PC to which the vendor attaches an instrumentation module. The PC is based on a 12-MHz 80286. The R45 has a bandwidth of 10 MHz and acquires data simultaneously on two channels at 20M samples/sec. It can store 128k samples/channel and can display 10 1024-point FFT spectra per sec. Under the control of menu-driven software, the unit can store and retrieve data to and from disk, average spectra, and save spectra either in scalar form (magnitude only) or in complex form. $7995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. FAX 206-548-0322. TLX 265017.

Circle No 423

AUTORANGING SCOPE

- *Offers three 100-MHz channels*
- *Permits display of six traces through alternate sweep*

The handheld VP-5610P scope has a 100-MHz bandwidth and three channels; it can display six traces, using alternate sweeps. The unit can also display two X-Y patterns simultaneously. The scope features

New Instruments

µP-based Programmable E/I dc Calibrator Model 521

The new Model is a micro-processor based, IEEE-488 (GP-IB) controlled, Voltage and Current DC Calibrator. One of its important applications is an imbedded standard as used in Data Acquisition and Process Control Systems.

An important feature of the new microprocessor that has been installed is that the programming of this instrument is transparent with respect to the programs written for the earlier 520, 520/A and even the older 501/J (GP-IB version).

The height is only 3½", and features current mode outputs from 10 nanoamperes (nA) to 110 milliamperes (mA), in two ranges, with extraordinary compliance of 100 Vdc. Even with this power, ideal for transducer instrument testing (4-20 and 10-50 mA), the accuracy is ± 0.005% of setting.

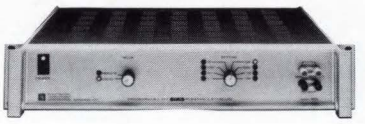
The voltage has three ranges with outputs from 100 nV to 100 Vdc and optional to 1100 Vdc. Compliance current is 100 mA. The one-year accuracy is ± 0.002% of setting.

All ranges and both modes resolve to 1 ppm. A crowbar zero provides a reference for this essential value.

Price: $3,150.
Engineering Contact: **Bob Ross**
Tel: (617) 268-9696 • FAX: 268-6754

CIRCLE NO 171

Programmable Resistance Calibrator Model 620/A



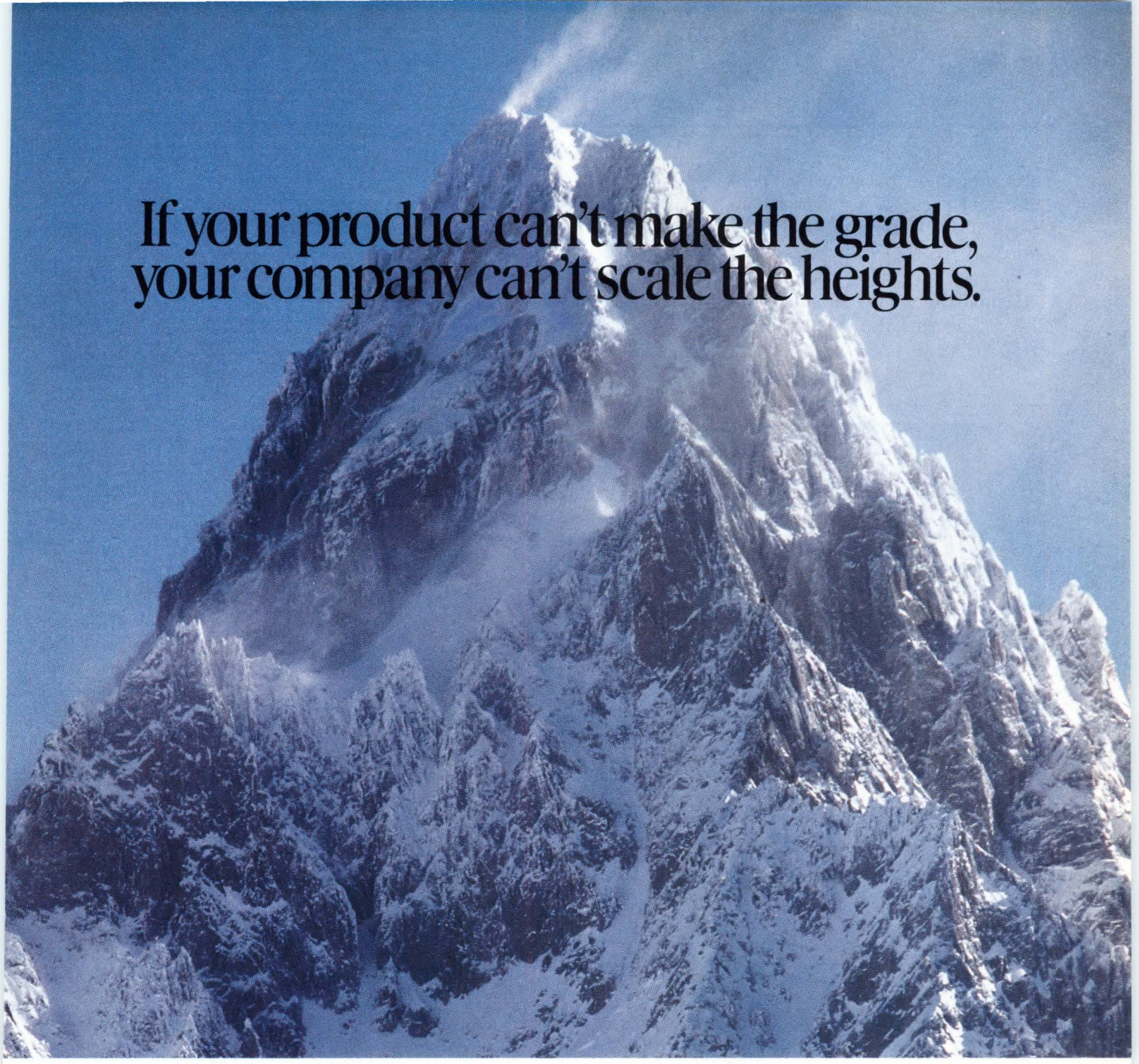
The Model 620/A is a programmable IEEE-488 resistance calibrator which features eight cardinal resistance points. It eliminates need to switch leads for various ranges. Ideal for use with both non-smart DVM's and DMM's.

Features:
Front Panel Manual Controls
Accuracies 0.002% to 0.0125%
2 or 4 wire connections
True passive resistance

Specifications:
Temp: 0°C to 50°C
Relative Humidity: 70%
Setting: 1 to 10 meg
Accuracies: 0.0125% (at 1) to
0.002% (at 10 meg)
Accuracy: Valid and guaranteed for 12 months

Price: $1,530
Engineering Contact: **Bob Ross**
Tel: (617) 268-9696 • FAX: 268-6754
CIRCLE NO 172

ELECTRONIC DEVELOPMENT CORP.
11 Hamlin St., Boston, MA 02127



AT&T's testing services provide comprehensive laboratory services and product evaluations, so you get the precise test data, reports and analysis you need.

Whether you're designing a product or manufacturing it, you need guarantees it can stand up to customer demands.

Which means you need accurate testing, as well as test data that's totally dependable.

Exactly what you'll get from AT&T's testing services.

In fact, they're the same services that continually place our own products at the top of the industry.

Our test site facility contains over 3,000 pieces of test equipment. All continually calibrated, certified and updated to assure accurate test data, reports and analysis.

Our extensive laboratory services include acoustics, chemical, environmental, electronic, and more.

Over 200 engineers specialize in specific product categories, and our in-house design groups develop and build custom test fixtures and automated test systems.

All to assure your product's performance—as well as your position—in the marketplace.

Put quality to work.

For more on how AT&T's Quality Management and Engineering Services will put your product to the test, call our sales office at 1 800 521-3399, or in NJ, 201 851-3333.

AT&T
The right choice.

autoranging on both vertical and horizontal axes. It includes an on-screen alphanumeric display and, optionally, an IEEE-488 interface. $1895.

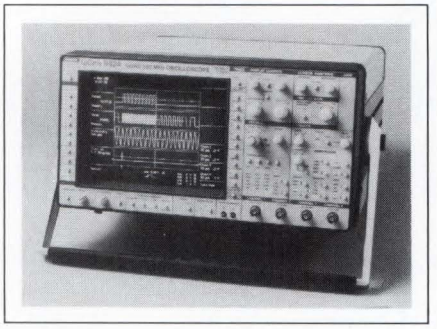
Panasonic, 50 Meadowland Pkwy, Secaucus, NJ 07094. Phone (201) 392-4050. FAX 201-392-4482.

Circle No 424

DSO

- *Has four 350-MHz-bandwidth channels*
- *Also provides X-Y displays*

The 9424 is a 4-channel, 350-MHz-bandwidth, portable digital storage oscilloscope. For repetitive phenomena, the effective sampling rate exceeds 10G samples/sec. For single-shot events, the unit takes 100M samples/sec. Its X-Y display capability is not commonly found in DSOs. The unit uses independent 8-bit flash A/D converters on each channel and has a nonvolatile memory that can store 50k samples/channel, allowing the DSO to sample single-shot events at its maximum rate for much longer periods than can most competitive instruments. This ability, coupled with the ability to magnify waveform segments, lets you see otherwise invisible details in rather long-duration transients. $19,900.



LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 578-6072. FAX 914-425-8967. TWX 710-577-2832.

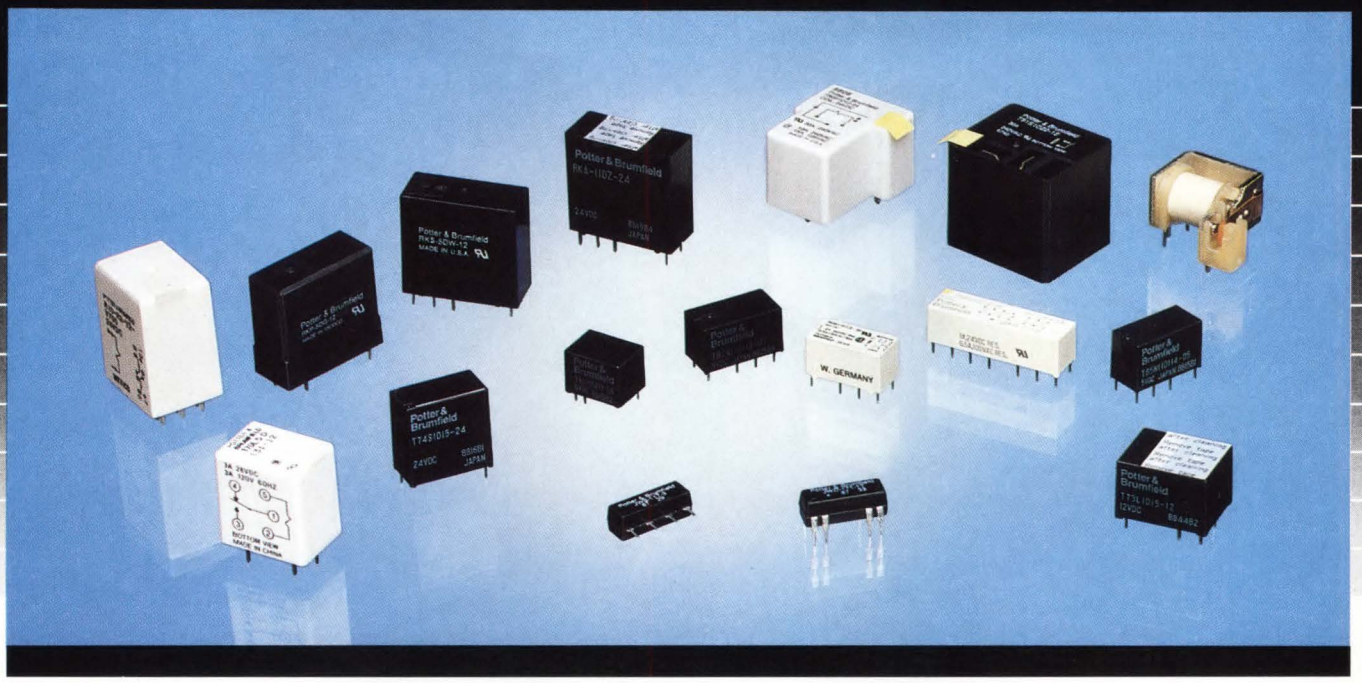
Circle No 425

DSO

- *Has two 300-MHz bandwidth channels*
- *Also displays two channels of computed data*

The PM 3323 digital storage oscilloscope has two inputs, but it can simultaneously display four waveforms, two of which it derives by performing mathematical operations on the input signals. The inputs have a 300-MHz bandwidth,

Specify P&B for dry circuit to 30A load switching on your P.C. board.



New Models Expand Offering

Potter & Brumfield's expanded line of printed circuit board relays provides the features you need – whether you're switching dry circuits or 30A loads. New products, traditional P&B quality and unbeatable service combine to help solve your toughest relay design-in problems in telecommunications, appliance, industrial control and other applications.

Miniature Relays Switch 1mA to 10A

New T73 and T74 series miniature P.C. board relays join the T70 series as Potter & Brumfield's low-cost SPDT units for general purpose applications. Various contact materials permit these immersion cleanable relays to switch from 1 mA through 10A. Sensitive coil models are available.

Expanded Line of 4,000V Isolation Relays

Extensions to the line of RK series relays feature 8mm coil-to-contact spacing for 4,000V isolation. SPDT models switch loads to 20A, while DPDT models switch up to 5A. Both sealed and unsealed types are now offered with either AC or DC coils.

T90 & T91 – 30A Workhorses

T90/T91 series relays have SPDT contacts for loads to 30A. The DC coil T90 is offered as an open-style or sealed relay. The T91 is available with a DC coil, and it's offered with quick connect terminals for load connections. An AC coil T91 will be available soon.

More Models for Low Signal Switching

The growing line of P&B low-signal relays features units with single or multiple contacts to provide dependable switching of 2A and under loads. Both polarized and non-polarized units are offered in various coil sensitivities. Included are immersion cleanable DIP and SIP types.

Stock Availability

Many models are available off-the-shelf from your authorized P&B distributor. Of course, distributor stock is backed by Potter & Brumfield's extensive factory inventory.

Find Out More

Contact us today for information on our complete line of P.C. board relays. Potter & Brumfield, A Siemens Company, 200 S. Richland Creek Drive, Princeton, Indiana 47671-0001.

Call toll-free 1-800-255-2550 for the P&B authorized distributor, sales representative or regional sales office serving your area.

Potter & Brumfield A Siemens Company

8905

NEED BROAD-BAND COAXIAL RELAYS? FROM 2 TO 24 THROW, MATRIX HAS THE ANSWER

Our versatile 7000 series of coaxial relays have band-widths from DC up to 800 MHz. They're available from 2 to 24 throw. And by using our 9000 series cross-straps, switching matrices of any size can be configured.

Why have Matrix broad-band relays become the industry standard? Because we construct them of precision machined anodized aluminum alloy, all signal shield paths are silver plated, and basic switch elements are hermetically sealed in nitrogen filled gas envelopes with rhodium plated contacts to insure non-stick operation.

The end result is extremely low crosstalk, EMI and VSWR. Another plus, all switchpoints are individually field replaceable.

The units are plug compatible with Matrix 6100A and 1600 Series Logic Modules for compatibility with RS-232, RS-422 and IEEE-488 Interface busses as well as 16 bit parallel.

Non-blocking Matrix configuration may be easily assembled using our self-terminating relays and 5100A series power dividers. Built-in Video/RF amplifiers allow zero insertion loss designs.

So if you're looking for broad-band relays, it pays to deal with Matrix. After all, we've been designing state-of-the-art reed relay and semiconductor switching systems for over 18 years.

Our customers include government agencies, defense contractors, the TV industry, ATE and telecommunications companies—and more.

MATRIX
SYSTEMS CORPORATION

5177 NORTH DOUGLAS FIR ROAD
CALABASAS, CALIFORNIA 91302
(818) 992-6776 · TWX 910-494-4975

For free catalog, phone, write, FAX or TWX Matrix today.

CIRCLE NO 176

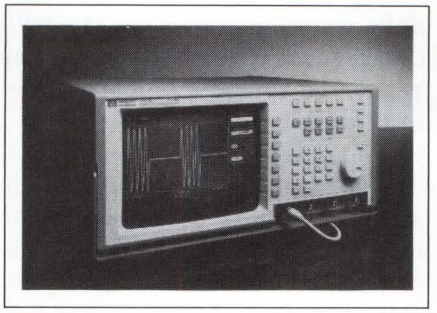
and the scope takes 500M 10-bit samples/sec on each channel, allowing it to resolve single-shot signals with durations as short as 2 nsec. Input offset lets you suppress dc voltages equivalent to 1000× the height of the screen, thereby permitting you to use the ADC's full resolution on the dynamically changing portion of the signal. The scope can calculate and display histograms, and optionally can compute a 4096-point FFT in 13 sec. From $10,900. Delivery, eight weeks ARO.

John Fluke Mfg Co Inc, Box C-9090, Everett, WA 98206. Phone (800) 443-5853; in WA, (206) 347-6100. TWX 910-445-2943.

Circle No 426

Philips Test and Measurement, Building HKF, 5600 MD, Eindhoven, The Netherlands. Phone local office.

Circle No 427



DSOs

- *HP 54503A has four 500-MHz-bandwidth channels*
- *Cost less than closely equivalent analog scope*

The HP 54503A digital storage oscilloscope digitizes repetitive signals that contain 500-MHz components. This frequency range is higher than that handled by most portable DSOs. The scope can also display four input signals simultaneously, and its price is lower than that of an analog scope with similar characteristics. The 54503A can't display wide-bandwidth single-shot phenomena, something analog scopes can do, albeit normally only with the aid of a camera. The Model 54502A, which the vendor is announcing at the same time, does handle wideband single-shot events. It has two channels, a 100-MHz single-shot bandwidth, and a 400-MHz repetitive-signal bandwidth. 54503A, $4950; 54502A, $6450. Delivery, 12 weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No 428

PROGRAMMERS

- *Operate as gang, set, and PLD programmers*
- *Support 24-, 28-, and 32-pin devices (40 pins optionally)*

The 135H-E duplicates EPROMs and EEPROMs. It also functions as

a gang programmer, simultaneously programming identical information into as many as eight devices, and a set programmer, simultaneously programming data as wide as 32 bits into multiple devices. In addition to performing all of these functions, the 135H-U model also programs PLDs. Both units can handle DIP devices with 24, 28, or 32 pins. As an option, the vendor can supply the units configured to program EPROMs and microcomputers that have 40 pins. The programmers, which operate in stand-alone mode or connected to a computer's RS-232C port, include a RAM that expands to 4M bytes. From $1495.

Bytek Corp, 508 NW 77th St, Boca Raton, FL 33487. Phone (407) 994-3529. FAX 407-994-3615. TLX 4998369.

Circle No 429

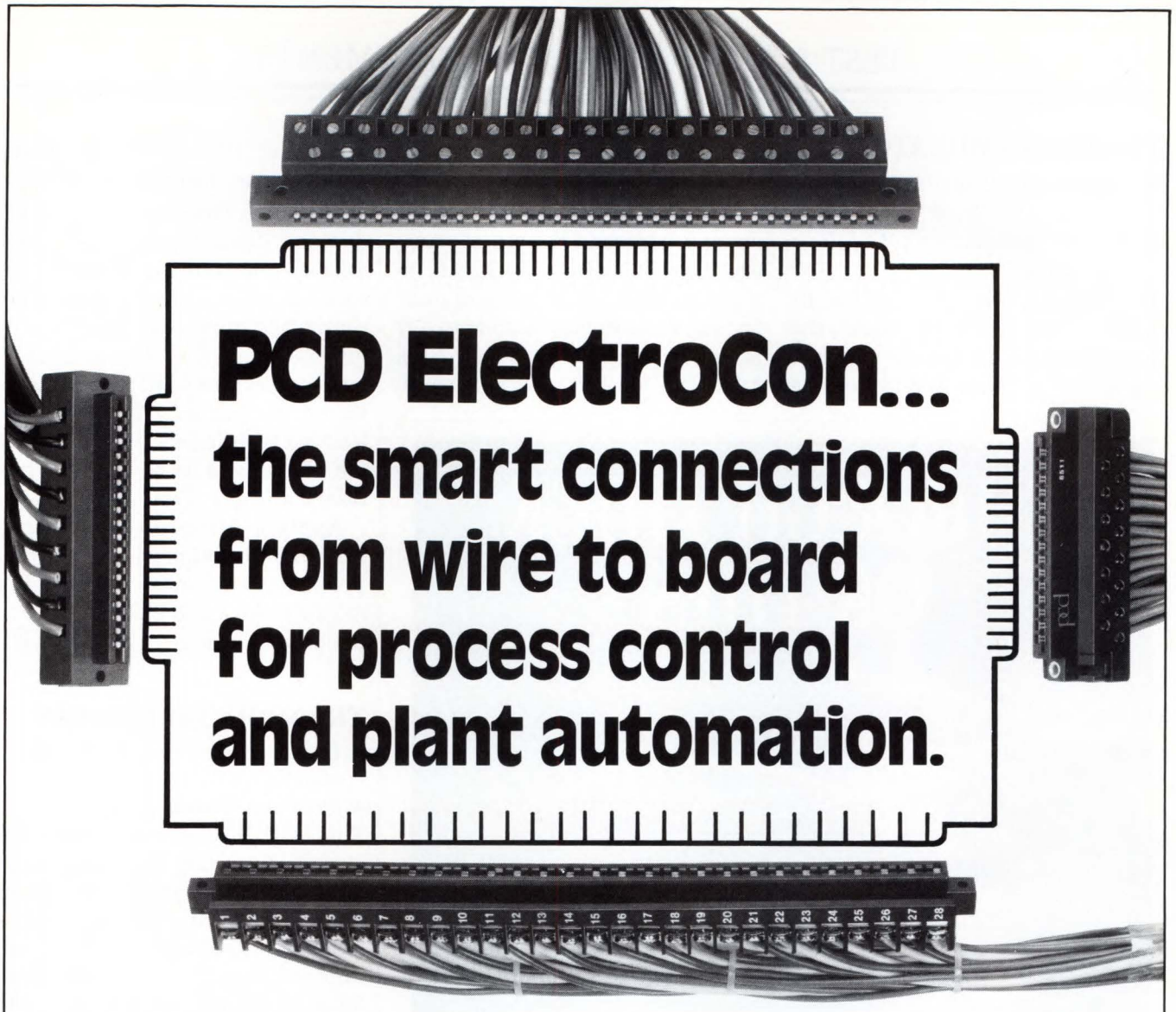
MACINTOSH II BOARDS

- *Acquire analog data at 1M samples/sec*
- *Can transfer data to memory at 29M bytes/sec*

The NB-A2000 and NB-DMA2800 are Nubus-based boards for Apple Computer's Macintosh II series. The NB-A2000 is a 4-channel, 12-bit-resolution data-acquisition board that includes four S/H circuits and a single ADC. The NB-DMA2800 is a 32-bit block-mode DMA interface with eight DMA channels, eight counter/timer channels, and eight interrupt channels. Without interfering with the operation of the Macintosh's own CPU, it can transfer data to and from contiguous locations anywhere in the Nubus's 32G-byte address space at a rate of 29M bytes/sec. The vendor supplies several coaxial adapters and cables to simplify bringing signals into the data-acquisition board. The vendor also provides a set of software drivers, collectively named NB LabDriver, that permits the boards to work with its $1995 Labview instrument-control software package. NB-A2000, $2995; NB-DMA2800, $1595; NB LabDriver, $295. Delivery, August 1989.

National Instruments Corp, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 433-3488; in TX, (512) 794-0100. FAX 512-250-9319.

Circle No 430



PCD ElectroCon... the smart connections from wire to board for process control and plant automation.

PCD ElectroCon screw barrier/edgecard connectors join the electrical world to the electronic with more reliability and in the tightest spacing around for individual or gang wire-to-board termination. Now, PCD has expanded its ElectroCon connector system to a complete family of the smartest connectors available for plant automation, programmable/process controllers, instrumentation I/O and other discrete wire-to-board interconnect applications.

ElectroCon connectors are now available with contact spacings of .375″, .200″ and .156″—in a variety of configurations. PCD has even designed special ElectroCon connector systems to .100″. And whether its a standard model or something special, every member of the ElectroCon family gives you better board contact, with better wire termination, than any other screw barrier/edgecard connector.

PCD: the connector connection
PCD is, and always has been, a *connector* company. We know what it takes to make a good connection. And it shows in the ElectroCon's design. These connectors feature precision-engineered, high normal force beam contacts, and more reliable, more durable board contact.

The selectively plated ElectroCon beam contact provides more consistent board contact and eliminates possible board damage inherent in tuning fork contacts. It provides reliable contact over the entire range of board thicknesses and after repeated insertion/withdrawal cycles.

The ElectroCon/375 features a separate steel wire retention nut for greater wire termination strength and reliability while eliminating the possibility of thread stripping. The ELD/200 and ELB/156 models employ a new floating vise clamp that assures direct, high-pressure interconnection between contact and wire. And since the rotating captive screw doesn't contact the wire, there's no possibility of strand damage.

Make smarter connections
If you're looking to use connectors smarter, PCD's ElectroCon family offers you high reliability, high density, isothermal equalization and cold reference junction capability—all in the same compact connector. You can't beat the performance or economy. Call or write PCD, Inc., 2 Technology Drive, Centennial Park, Peabody, MA 01960. (508) 532-8800. FAX (508) 532-6800.

pcd
PRECISION CONNECTOR DESIGNS, INC.

The smart connector company

Z180/64180 EMULATOR

- *Supports the Z180 and the PLCC version of the 64180*
- *Allows emulation at μP's full clock speed*

In addition to the Z80 and the R-Mask version of the HD 64180, the EL 800 in-circuit emulator now supports the Z Mask version of the 64180 in PLCC (plastic leaded chip carrier) packages and the equivalent Z180. The latter two devices directly address 1M byte of memory. The emulator, which can include as much as 2M bytes of overlay RAM, performs nonintrusively at the processors' maximum clock rate. The EL 800 software, which runs on an IBM PC/AT computer, includes such features as movable and sizeable windows; a watch window for viewing registers, symbol values, and address locations as code executes; a strobe option that continually updates all windows; an expression analyzer that accepts C language expressions; and 10 hardware-test routines. A file window lets you save specific configurations (or all configurations except symbols and trace). From $3500.

Applied Microsystems Corp, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; in WA, (206) 882-2000. FAX 206-883-3049.

Circle No 431

TRANSDUCER DISPLAY

- *Usable with strain gauges and load cells*
- *Resolves 100,000 counts*

The MVD2630 panel-mounted instrument excites, conditions, and displays the output of strain gauges, load cells, and other resistive-bridge transducers. The measurement error is <0.01% and resolution is 100,000 counts. The unit, which sports a 6-digit display, employs a 6-wire input and minimizes drift and noise through the use of a 600-Hz carrier system. Splash-proof membrane switches let you control many measurement and alarm functions, including six limit-switch levels and their hysteresis ranges. You can also operate the unit via an RS-232C interface and use it to control other equipment via external relays. $2200.

Hottinger Baldwin Measurements Inc, 19 Bartlett St, Marlboro, MA 01752. Phone (508) 624-4500.

Circle No 432

KEPCO INDUSTRIAL GRADE 150KHz FET-BASED SWITCHING POWER SUPPLIES

SERIES RAX™

New Reduced Prices!*

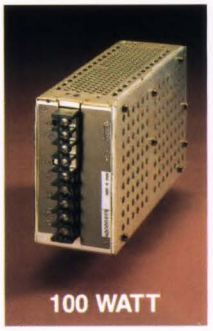
KEPCO®
THE POWER SUPPLIER™

* Unit prices shown.
Quantity discounts available.

KEPCO INDUSTRIAL GRADE 150KHz FET-BASED SWITCHING POWER SUPPLIES, SERIES RAX™

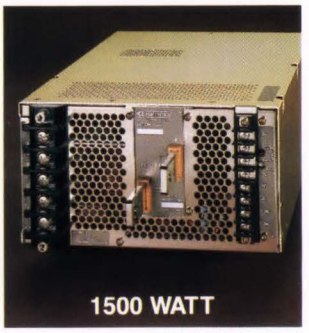
4.3 INCHES HIGH


50 WATT


100 WATT


175 WATT


300 WATT


1500 WATT

RAX MODEL TABLE

SPECIFICATION	OUTPUT VOLTAGE		OVP SETTING	OUTPUT CURRENT			CURRENT LIMIT	RIPPLE				NOISE (SPIKE)	EFFICIENCY
Unit	Volts		Volts	Amps			Amps	mV				mV	Percent
Condition	Factory set(1)	Adjustment range	Nom. input, 25°C	50°C	60°C	71°C	25°C Rectangular Fixed	Source p-p typ	Source p-p max	Switching p-p typ	Switching p-p max	d-c to 50MHz p-p max	max load typ
50 WATT MODELS							Size: 4.3" H x 1.8" W x 7.5" D				Net weight: 1.80 lb.		
RAX 5-10K	5	4.0~ 5.5	6.0~ 6.9	10.0	7.0	4.0	10.5~ 11.0	5	10	25	40	100	75%
RAX 12-4.2K	12	8.4~13.2	13.7~15.7	4.2	2.9	1.7	4.5~ 4.8	15	30	25	50	170	
RAX 15-3.4K	15	12.0~16.5	17.0~19.5	3.4	2.4	1.4	3.6~ 3.9	15	30	25	50	200	
RAX 24-2.1K	24	16.8~26.4	27.0~30.5	2.1	1.5	0.8	2.3~ 2.5	25	40	25	60	290	
RAX 28-1.8K	28	19.6~30.8	32.0~35.0	1.8	1.3	0.7	2.0~ 2.2	30	60	25	60	330	
RAX 48-1K	48	32.6~52.8	55.0~63.0	1.0	0.7	0.4	1.1~ 1.3	35	90	25	60	530	
100 WATT MODELS							Size: 4.3" H x 2.6" W x 7.9" D				Net weight: 2.90 lb.		
RAX 5-20K	5	4.0~ 5.5	6.0~ 6.9	20.0	14.0	8.0	22.0~ 24.0	5	10	25	40	100	78%
RAX 12-8.3K	12	8.4~13.2	13.7~15.7	8.3	5.8	3.3	9.1~ 10.0	15	30	25	50	170	
RAX 15-6.6K	15	12.0~16.5	17.0~19.5	6.6	4.6	2.6	7.3~ 8.0	15	30	25	50	200	
RAX 24-4.2K	24	16.8~26.4	27.0~30.5	4.2	2.9	1.7	4.7~ 5.1	25	40	25	60	290	
RAX 28-3.5K	28	19.6~30.8	32.0~35.0	3.5	2.5	1.4	4.0~ 4.2	30	60	25	60	330	
RAX 48-2K	48	32.6~52.8	55.0~63.0	2.0	1.4	0.8	2.3~ 2.5	35	90	25	60	530	
175 WATT MODELS							Size: 4.3" H x 3.9" W x 8.7" D				Net weight: 3.96 lb.		
RAX 5-35K	5	4.0~ 5.5	6.0~ 6.9	35.0	24.5	14.0	36.8~ 38.5	5	10	25	40	100	79%
RAX 12-14K	12	8.4~13.2	13.7~15.7	14.0	9.8	5.6	14.7~ 15.4	15	30	25	50	170	
RAX 15-11K	15	12.0~16.5	17.0~19.5	11.0	7.7	4.4	11.8~ 12.1	15	30	25	50	200	
RAX 24-7.2K	24	16.8~26.4	27.0~30.5	7.2	5.0	2.9	8.0~ 8.3	25	40	25	60	290	
RAX 28-6.2K	28	19.6~30.8	32.0~35.0	6.2	4.3	2.5	7.0~ 7.3	30	60	25	60	330	
RAX 48-3.6K	48	32.6~52.8	55.0~63.0	3.6	2.5	1.4	4.3~ 4.5	35	90	25	60	530	
300 WATT MODELS							Size: 4.3" H x 5.1" W x 8.7" D				Net weight: 5.50 lb.		
RAX 5-60K	5	4.0~ 5.5	6.0~ 6.9	60.0	42.0	24.0	65.0~ 70.0	5	10	25	40	100	77%
RAX 12-25K	12	8.4~13.2	13.7~15.7	25.0	17.5	10.0	28.0~ 30.0	15	30	25	50	170	
RAX 15-20K	15	12.0~16.5	17.0~19.5	20.0	14.0	8.0	22.0~ 24.0	15	30	25	50	200	
RAX 24-12K	24	16.8~26.4	27.0~30.5	12.0	8.4	4.8	13.2~ 14.4	25	40	25	60	290	
RAX 28-10K	28	19.6~30.8	32.0~35.0	10.0	7.5	4.3	12.0~ 15.0	30	60	25	60	330	
RAX 48-6K	48	32.6~52.8	55.0~63.0	6.0	4.2	2.4	6.8~ 7.4	35	90	25	60	530	
1500 WATT MODELS							Size: 4.3" H x 8.0" W x 12.6" D				Net weight: 17.60 lb.		
RAX 5-300K	5	4.0~ 5.5	6.0~ 6.9	300.0	210.0	120.0	315.0~350.0	5	20	50	120	200	79%
RAX 12-125K	12	8.4~13.2	13.7~15.7	125.0	87.5	50.0	130.0~140.0	15	30	60	150	250	82%
RAX 24-65K	24	16.8~26.4	27.0~30.5	65.0	45.5	26.0	68.0~ 72.0	25	40	60	150	300	83%
RAX 48-30K	48	32.6~52.8	55.0~59.0	30.0	21.0	12.0	32.0~ 35.0	35	90	70	150	500	84%

(1) Nominal input, maximum load, 25°C

For complete specifications send for Switcher Catalog 146-1605

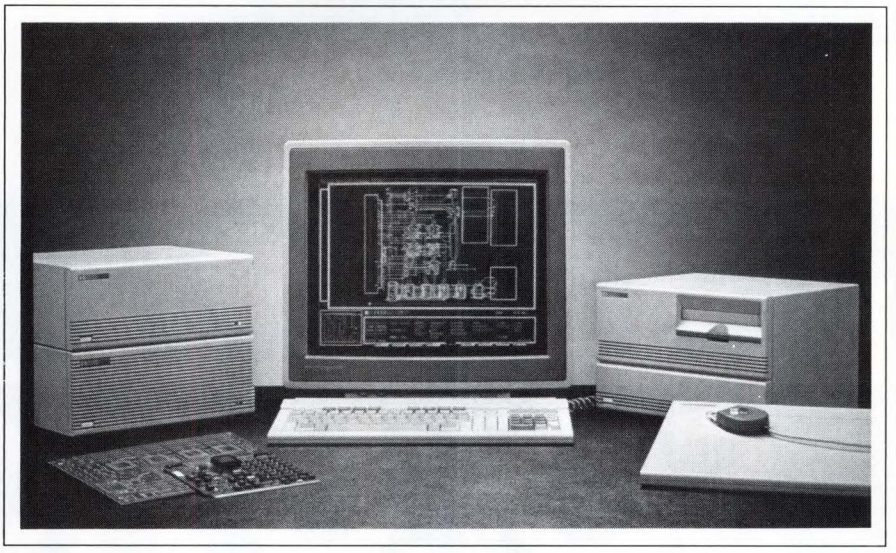
KEPCO, INC. • 131-38 SANFORD AVENUE • FLUSHING, NY 11352 USA • (718) 461-7000 • FAX: (718) 767-1102 • Easylink (TWX): 710-582-2631

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

SMT-BOARD DESIGN AID

- *Provides interactive placement and routing features*
- *Ability to flip board sides for viewing and plotting*



The HP PCDS 2.0 Printed Circuit Design System provides interactive placement and routing features that are especially suitable for designing dense 2-sided surface-mount boards. The system performs automatic placement on both sides of the board, but lets you select one side on which you can specify device placement by device class. The program lets you use metric or English units, or a mixture of both. You can flip the display from one side of the board to the other in order to view and check the plotting; the program uses different-colored pads on the two sides so you can identify the side you are viewing. To obtain higher completion rates, the program provides routing to off-grid parts and SMD breakouts. For tighter manual control over interactive tasks, you can stretch, rubberband, snap, or angle-lock traces, or remove them if redundant. You can also color-code power-supply and logic lines and turn this color coding on or off at will. The system runs on the vendor's HP 9000 Models 340, 360, 370, and 835 computers. From $15,000 to $37,000. Delivery, 12 weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

Circle No 388

POWER-SUPPLY DESIGN

- *Library includes models of PWMs*
- *Allows Saber simulator to handle linear and nonlinear magnetics*

The Power Supply Design Package allows the vendor's Saber general-purpose analog simulator to handle integrated magnetic components. According to the vendor, modeling and algorithm enhancements provide as much as a 35× increase in simulation speed. The modeling library includes behavioral PWMs, cores, transformers, power-MOS devices, and digital switches. Core models include the Ferroxcube family of ferrite cores. The program allows you to switch back and forth between linear (ideal) and nonlinear (real) models. An optimization feature allows you to enter parameter information from data books into the model, which then computes the optimal internal-parameter settings and creates an accurate nonlinear model of the core and automatically adjusts for effects of both temperature and frequency. The Power Suppy Design Package is an add-on to the Saber simulator. Annual subscription, $3600.

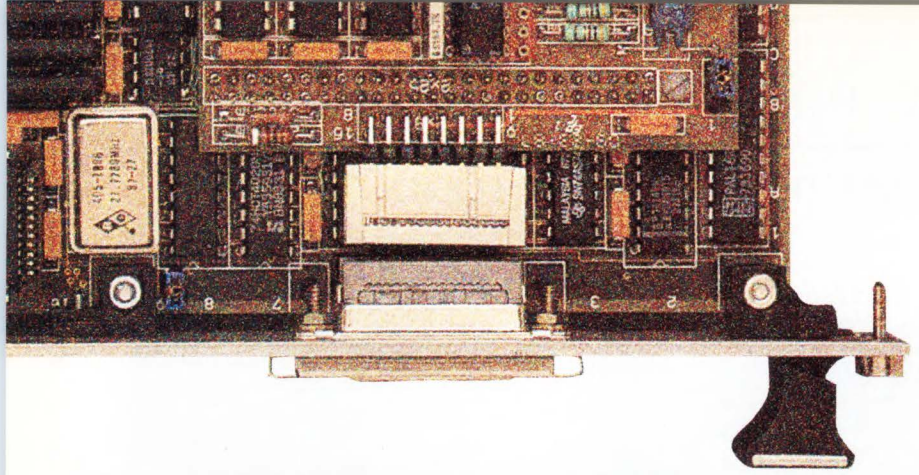
Analogy Inc, 9205 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-9700.

Circle No 389

LOGIC SIMULATOR

- *Allows verification of board-level logic designs*
- *Allows real-time manipulation of simulated test instruments*

Digital Design Lab is an interactive, PC-based logic simulator package that allows you to verify board-level logic designs. The package includes the software equivalents of a logic analyzer, an oscilloscope, a digital word-generator, a current-sniffer probe for locating bus conflicts, ROM and PLA programmers, an in-circuit emulator, and a μP development system. The interactive simulation lets you stop and restart simulation at any time; add, change, or delete test patterns; alter timing delays; patch μP code; and alter circuit connections or add parts without leaving the program. All of the virtual instruments are mouse-driven and are accessible through pop-up windows. The models are written in machine code rather than interpreted code and, in conjunction with the proprietary simulation algorithms, yield a simulation speed of as high as 200,000 gates/sec on an IBM PC/AT. The package comes with libraries of TTL and CMOS parts; optional libraries cover ECL, PAL/PLD/EPLD, Xilinx, RAM/ROM, VLSI, and μP families. The package works with the vendor's Associate Designer or Master De-



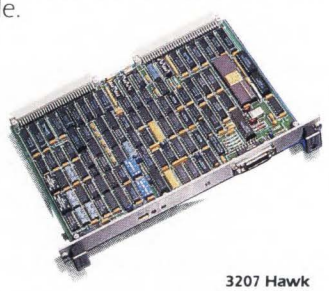
NETWORKING SOLUTIONS

ETHERNET SOLUTIONS FOR VMEbus

Ethernet can be frustrating. No one likes putting up with an Ethernet link that has low throughput. And for the system or network designer, the real price of a slow network is staggering. Just think about the productivity lost when almost every node is idly waiting for the network.

Often, the culprit is not the network itself, but slow, poorly-designed node controllers. Now, Interphase gives you solutions that are measurably better.

Interphase has a connectivity strategy for a wide range of VMEbus-to-Ethernet applications. The solution is two new products: the V/Ethernet 3207 Hawk and V/Ethernet 4207 Eagle.



3207 Hawk

HIGH-PERFORMANCE NODE CONTROLLERS

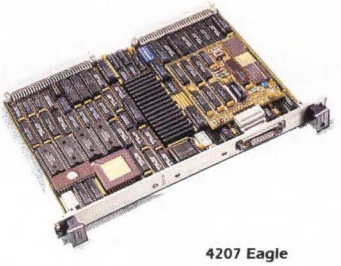
An elegantly partitioned architecture and powerful 16 MHz 68020 processor give the Eagle plenty of power for on-board protocol processing, yet provide outstanding throughput in link level applications. In fact, the Eagle is able to continuously saturate the Ethernet cable even with packets as small as a few hundred bytes. The other side of the performance question is the VMEbus interface. Here the Eagle has Interphase's exclusive BUSpacket Interface℠ which transfers data over the VMEbus at more than 30 megabytes per second.

LOW COST-PER-NODE SOLUTION

Our V/Ethernet 3207 Hawk offers a cost-effective approach to network access and node control. The Hawk has high-speed, dual-ported memory, innovative memory mapping capabilities, and a set of pipeline registers which prevents the bus from being monopolized during network access. For link-level performance at a surprisingly low cost, the Hawk can't be beat.

NETWORK LEADERSHIP

Interphase has consistently led the industry in high-performance peripheral controllers. It should be no surprise that our advanced technology has been applied to these two Ethernet controllers.



4207 Eagle

NETWORKING SOLUTIONS

Interphase provides the high-performance Ethernet solutions you need today. And just as we have for our first 15 years, we continue to set trends in technology and standards for performance that others follow. With Interphase as your technology partner, you gain a valuable member of the team that always keeps you...

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CIRCLE NO 181

signer systems. To run the program, you'll need an IBM PC/AT, PS/2, or compatible, having at least 640k bytes of RAM and 2M bytes of free space on a hard-disk drive. $1850.

P-CAD, 1290 Parkmoor Ave, San Jose, CA 95126. Phone (408) 971-1300.

Circle No 390

SPICE FOR 386

- *Can accept data from many schematic-capture programs*
- *Includes library of 2000 components*

The PC386 HSpice analog-circuit simulator runs under DOS 3.3 or later on the 80386-based IBM PC/AT and compatibles. To run the simulator, you need 4M bytes of RAM and an 80387 numeric coprocessor. The simulator works with a variety of video systems, including Hercules, CGA, EGA, and MCGA, and includes drivers for Epson, NEC, Okidata, HP DeskJet, and HP LaserJet printers. It conforms to standard Spice 2G conventions and accepts input data generated by the schematic-capture modules of many popular CAE systems. The program comes with a library of more than 2000 standard analog components and software that lets you create models of new components. $4000.

Meta-Software, 50 Curtner Ave, Suite 16, Campbell, CA 95008. Phone (800) 346-5953; in CA, (408) 371-5100. FAX (408) 371-5638. TWX 910-350-4928.

Circle No 391

ADA CROSS-DEVELOPER

- *Runs on IBM 370/VM or 370/MVS hosts*
- *Generates code for MIL-STD-1750A or 68000 family targets*

The vendor has released its TeleGen2 Ada Cross-Development Systems in four additional configurations for IBM mainframes: 370/VM to MC680X0 and MIL-STD-1750A; and 370/MVS to MC680X0 and MIL-STD-1750A. Each package includes the cross-compiler, Ada run-time system, and a set of development tools consisting of a global optimizer, a library manager, a library tool set, and other utility programs. The compiler itself is written in Ada and employs advanced error-recovery techniques to assist you in your development tasks. The global optimizer provides optimization across independently compiled modules, and allows you to optimize either for execution speed or for minimum code size. An on-line help facility documents all the system components and provides help in using them. Among the utility programs are an Ada Source-dependency Lister, an Ada Source Formatter, and a cross-referencer for symbolic names. From $17,660 to $155,000. Delivery, 60 days ARO.

TeleSoft, 5959 Cornerstone Ct W, San Diego, CA 92121. Phone (619) 457-2700. TLX 855300. FAX 619-452-1334.

Circle No 392

MATH FOR MAC

- *Palettes let you enter operator symbols easily*
- *Integrates equations, text, and graphics in one document*

MathCAD is an engineer's scratchpad that formats equations as you type them and quickly calculates and displays the results. The program was formerly available on IBM PCs and other workstations, and this new version runs on Apple (Cupertino, CA) Macintosh Plus, SE, or II computers that have at least 1M byte of RAM. Special palettes for the Macintosh make it easy for you to enter operator symbols and Greek letters in equations, and allow easy and fast manipulation of mathematical expressions. The program lets you perform comprehensive matrix arithmetic, trigonomet-

Analogic Announces...

The World's Highest Performance Arbitrary Waveform Synthesizer

At 800 Megapoints per second, the new Analogic/Data Precision Models 2040 and 2045 outperform the competition, delivering 4 times the data rate of the fastest polynomial waveform synthesizers.

With the Analogic Models 2040 and 2045, you can define and create any periodic or transient waveform.

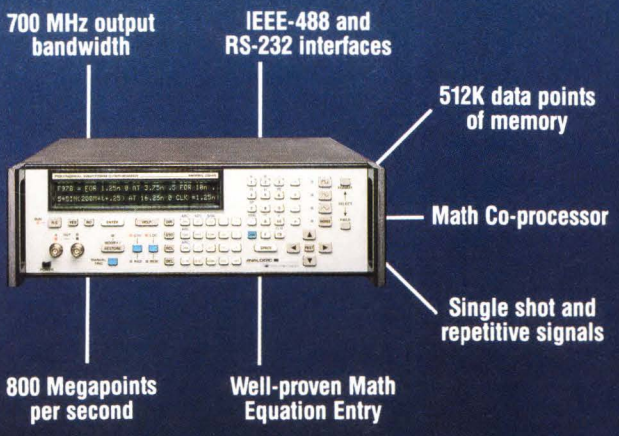
You can use Analogic's well-proven ME² Math Equation Entry approach, entering any equations in the form Y = f(t) from the keyboard. Or, you can download waveforms created on computers, graphic tablets, or oscilloscopes.

And, you can capture real-world transients with the Analogic Model 6100 Universal Waveform Analyzer, transfer their waveforms to the 2040/2045, and modify as desired.

The Model 2040 offers two outputs, each 1 V p-p, in phase opposition to provide both single-ended and differential outputs at a bandwidth of greater than 700 MHz.

The Model 2045 provides one low level output (1 V p-p/50 ohms) at a full 700 MHz bandwidth and another output channel at 5 V p-p/50 ohms, 200 MHz bandwidth and 8 bits resolution over the full dynamic range.

To discover how to use the new Analogic/Data Precision 2040 and 2045 for your most complex waveform generator applications, call Analogic today at 1-800-343-8333.



ANALOGIC®

The World Resource for Precision Signal Technology

Analogic Corporation
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CIRCLE NO 183

ric, and hyperbolic functions, and compute integrals and derivatives. Other features include facilities for real and complex FFTs, a random-number generator, a wide variety of statistical functions, cubic splines, and Bessel and gamma functions. The program can also compute solutions of simultaneous linear or nonlinear equations. Plotting facilities include automatic or manual scaling, linear and log plots, and 3-D surface plots. $495.

MathSoft Inc, 1 Kendall Sq, Cambridge, MA 02139. Phone (617) 577-1017. FAX 617-577-8829.

Circle No 393

VISION OS

- *Provides multiwindow control of all functions*
- *Lets you create command files for automatic sequencing*

The VOS/DVOS icon-based operating system runs on the IBM PC, PC/XT, PC/AT, and compatibles and gives you full control of microcomputer-based imaging applications. The icon-based user interface lets you set up hardware, manage the screens, define touch zones, and, using DVOS, lets you create or change icons. The system provides camera functions, frame-grabber functions, disk functions, and access to user-defined functions written in C. The imaging functions let you define the kernel and perform convolution, and define and execute bit-mapped operations. The on-line help facility provides a guide to all VOS functions. In the Record mode, the system stores all point-and-click operations in a disk file that you name; you can repeat the same sequence of operations by recalling and executing this file. VOS, $99; DVOS, including VOS, libraries, and icon-editing facilities, $499.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX 508-880-0179. TLX 503989.

Circle No 394

OS SWITCH

- *Allows both OS/2 and PC-DOS on the same hard disk*
- *Lets you switch from one operating system to the other*

MultiBoot provides quick and easy access to either OS/2 or PC-DOS at boot time, allowing you to install both systems on the hard disk and select one of them as the default; that system boots from the hard disk at turn-on time and whenever you press CTRL-ALT-DEL to reboot. However, before the boot is complete, the program pauses, displaying a prompt that allows you to select the operating system you want to use; if you ignore the

prompt, the default-system boot continues; if you press the Caps Lock key in response to the prompt, MultiBoot abandons the default-system boot and boots the alternative operating system. The program works with all versions of OS/2 and with PC-DOS version 3.0 and higher. Because the program is a boot record and is resident only during a boot, it cannot interfere with any application programs or system utilities. The vendor supplies the program on 5¼-in. or 3½-in. disks. $49.95.

Bolt Systems Inc, 4340 East-West Hwy, Bethesda, MD 20814. Phone (301) 656-7133. FAX 301-907-8736.

Circle No 395

GRAPHICS TOOL

- *Conforms to PHIGS*
- *Makes graphics applications written in Fortran or C portable*

The Figaro and Figaro+ device- and computer-independent implementations of the Programmer's Hierarchical Interactive Graphics Standard allow you to develop portable graphics application programs written in Fortran or C. These applications can make full use of features such as event-input programmable triggers and soft-input devices such as screen buttons and sliders. You can move an application from one machine to another by merely relinking the application to a Figaro library on the new machine. Figaro tools and libraries are available for more than 20 different computers, from the Convex and Alliant supercomputers at the upper end, to HP, IBM, DEC, Sun, Apollo, and 80386-based machines in the workstation category. Figaro provides all the facilities you need for common 2-D and 3-D applications; Figaro+ provides the same features with the addition of sophisticated lighting, shading, and depth-cuing capabilities needed for more complex graphics applications. Figaro, from $3500; Figaro+, from $4500.

Template Graphics Software Inc, 9685 Scranton Rd, San Diego, CA 92121. Phone (619) 457-5359. FAX 619-452-2547.

Circle No 396

CONTROL SYSTEM

- *Provides tools for developing industrial controls*
- *Provides multitasking kernel and operator interface*

The RPCore software package runs on IBM PC/ATs, PS/2s, or compatibles, and provides not only a multitasking kernel for embedded systems, but also all the routines you need for developing the software and a graphics operator interface for an industrial process-control system. The facilities allow you to develop process-control software, complete with a graphical operator interface, debug it, and download it to an embedded system. Because the system supports a wide variety of I/O controllers based on STD, VME, and Multibus standards, you can also use the host computer as the control center for multiple controllers connected to each other and to the host by RS-232C, RS-485 Multidrop, or ArcNet communications links. From $18,750.

Realtime Performance Inc, 491 Macara Ave, Suite 1001, Sunnyvale, CA 94086. Phone (408) 245-6537. FAX 408-245-6547.

Circle No 397

CASE TOOL

- *Lets you develop prototype screen displays and reports*
- *Data dictionary ensures data consistency*

Pose-SRP, the ninth module in the Pose computer-aided software-engineering system, is a screen and report prototyper that lets you develop screen displays, reports, and system simulations. This module is tightly integrated with the Pose

NOW PUT A LITTLE AVANTEK MAGIC IN YOUR SYSTEM

Avantek MagIC™ High Speed ICs Enable Superior System Designs

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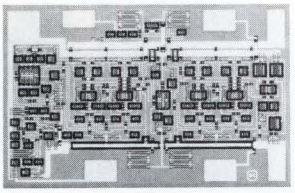
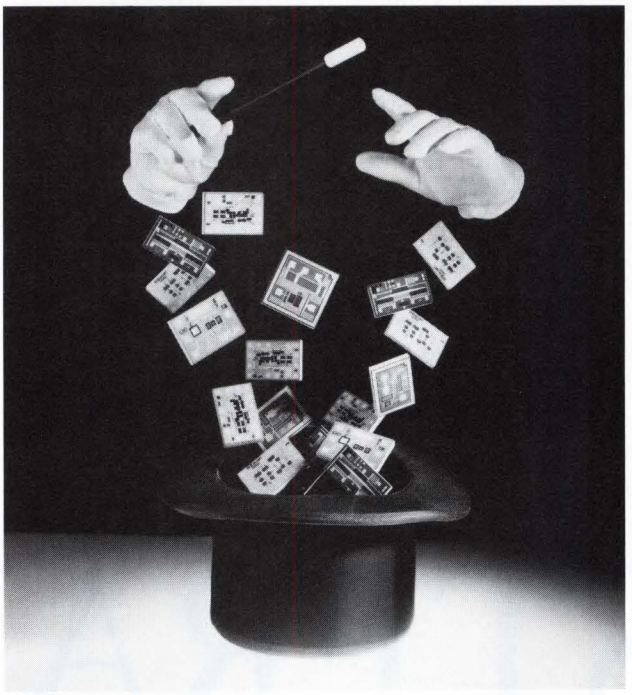
The new MagIC™ series of silicon bipolar MSI integrated circuits offer the best performance available from silicon ICs yet. The broadband, high frequency performance of these high-speed silicon ICs make them cost-effective alternatives to more expensive GaAs ICs. Avantek MagIC silicon ICs are manufactured with Avantek's proprietary 10-15 GHz F_t, 25 GHz F_{max} Isosat™ process for unsurpassed integration and performance at microwave frequencies. Avantek's MagIC series ICs presently consists of four product families: low noise amplifiers, active mixers, variable gain control amplifiers, and prescalers. These low-cost, high-speed silicon ICs are Avantek's magic solutions to your RF, microwave and lightwave system performance and cost problems.



High Performance, High Speed, Low Cost...

The INA-series of two-stage low-noise amplifiers presently consists of three models, offering:

- 3 dB bandwidths to 2.8 GHz
- Gains as high as 32 dB
- Noise figures as low as 1.7 dB
- Prices as low as $22.00 each* in hermetic 70 mil surface mount package



The IAM-series of active mixer/amplifiers presently consists of two models, offering:

- RF and LO frequency range of .05 to 5.0 GHz
- Conversion gain as high as 15 dB
- LO power as low as −10 dBm
- Prices as low as $16.00 each* in hermetic 180 mil surface mount package

The IVA-series of variable gain control amplifiers presently consists of two models, offering:

- 3 dB bandwidths to 3.0 GHz
- 30 dB gain control range
- Gains as high as 26 dB
- Prices as low as $28.50 each* in hermetic 180 mil surface mount package

The IFD-series low phase noise static prescalers offer:

- Divide-by-4 to 5 GHz
- Low 125 mW Power Consumption
- Prices as low as $18.50 each* in hermetic 100 mil surface mount package

*Price for 1000 piece quantities

MagIC™ ICs Are Available in Quantity for Volume Applications

Avantek presently produces more than 1,000,000 MMICs per month. So you can be assured the MagIC high speed ICs you need will be available to support your volume production programs. And, all MagIC silicon ICs are in stock at your local Avantek distributor.

For additional information, or the name and address of your local distributor, contact the regional sales office nearest you.

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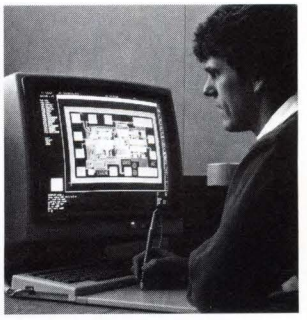
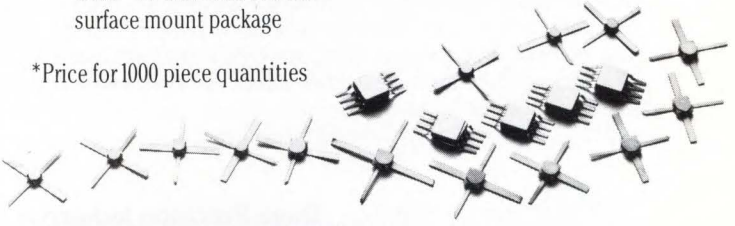
European: (44) 276-685753





Magic Solutions in Silicon

AVANTEK

CIRCLE NO 186

data dictionary to ensure data consistency. You can use the screen-painter facility to create the screen image and define the fields; you can also specify edit checks and repeating fields, and control the flow from one screen to another. The report-generation facility lets you produce mock-ups of the reports that the system will generate, complete with the titles, headers, labels, and data-output pictures. The prototyping facility shows you how the screens would appear during execution of the system under design, and how they would interact with other screens. The complete Pose system runs on the IBM PC, PC/XT, PC/AT, PS/2, and compatibles and consists of nine modules. Each module, $495; 4-module system, $885; complete 9-module system, $2265.

Computer Systems Advisers Inc, 50 Tice Blvd, Woodcliff Lake, NJ 07675. Phone (201) 391-6500.

Circle No 398

TEST SOFTWARE

- *Allows you to loop-test power supplies*
- *Can control auxiliary test equipment*

The Cycletest software package runs on the company's Micro Series PC-based power-supply ATE systems, allowing you to continuously loop-test power supplies. The software, which is an addition to the company's Powerstar software library, can monitor one or more power-supply parameters and log the results on the disk. You can analyze the accumulated data, using standard statistical-analysis formulas, and you can include tolerance limits on tests, which can then be used to condense the test results. Cycletest can produce a range of reports for use by development engineers, manufacturing and quality-assurance departments, or incoming inspection departments. In addition, the software allows you to drive auxiliary equipment, such as burn-in ovens, via the ATE's digital I/O ports. For present owners of the Powerstar software library, £200.

Intepro Systems Ltd, Plassey Technological Park, Castletroy, Limerick, Ireland. Phone (061) 332233. FAX 061-332584.

Circle No 399

Intepro Systems Inc, 450 Bedford St, Lexington, MA 02173. Phone (617) 863-9500. FAX 617-861-1957. **Circle No 400**

SIMPSON UNIVERSAL FREQUENCY COUNTERS.

COUNT ON US FOR ACCURACY.

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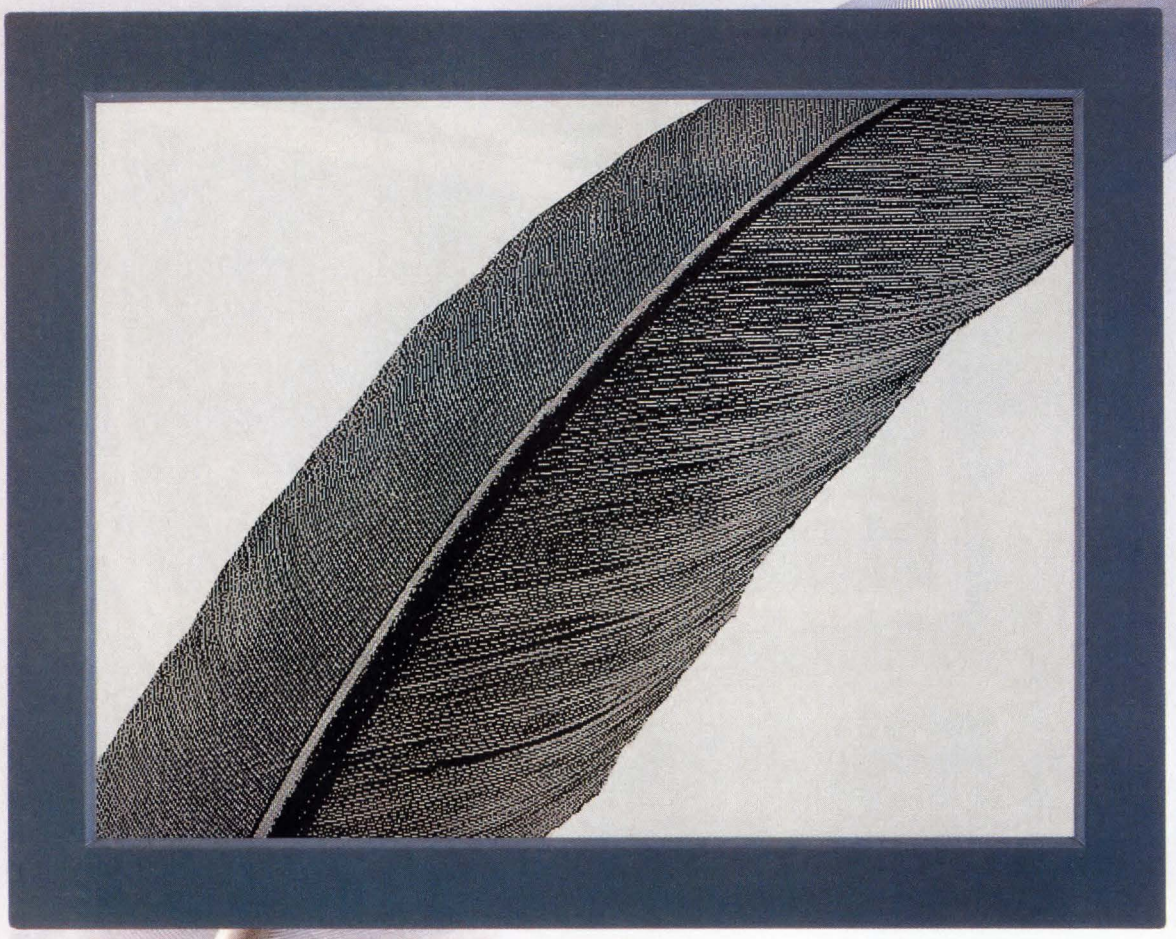

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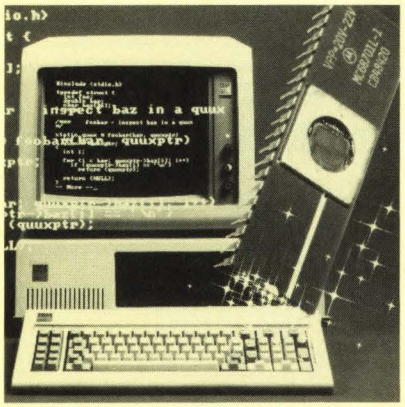

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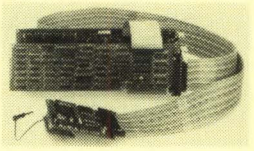

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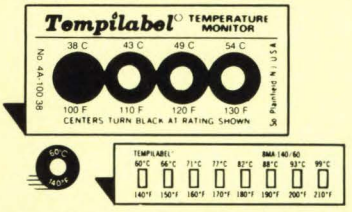

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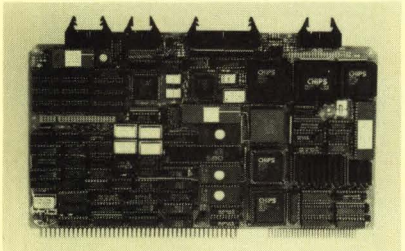

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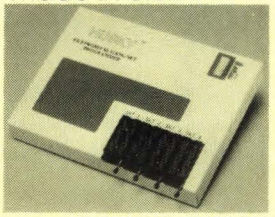

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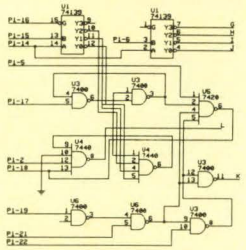

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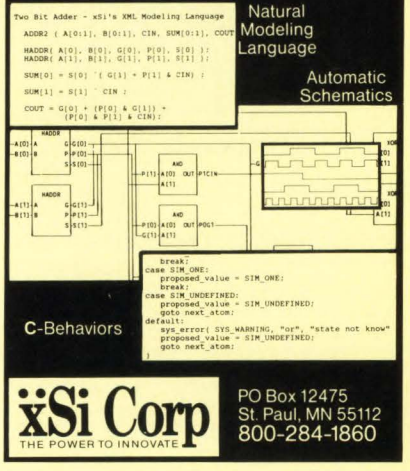

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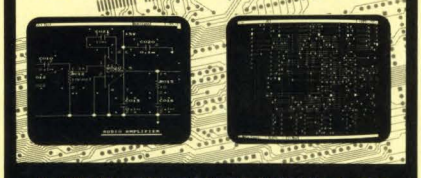

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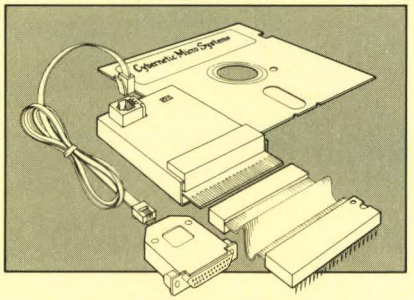

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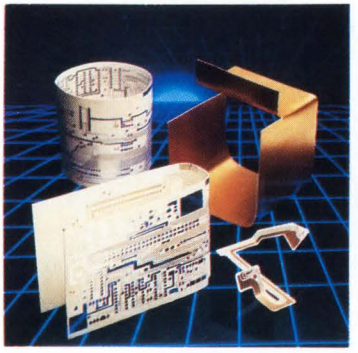

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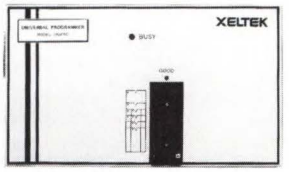

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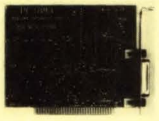

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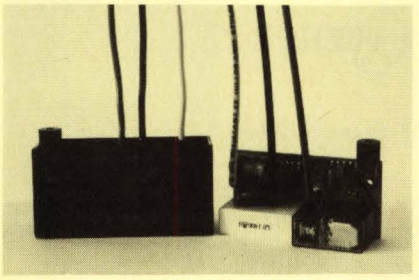

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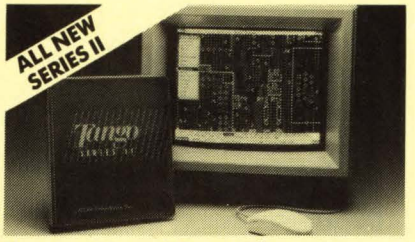

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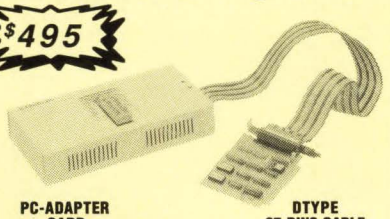

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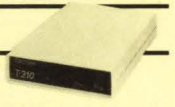

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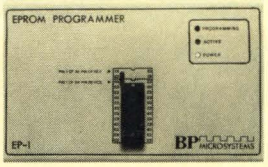

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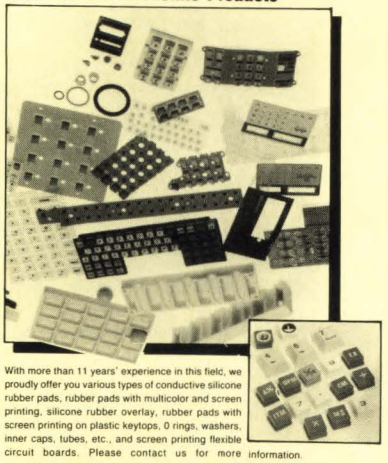

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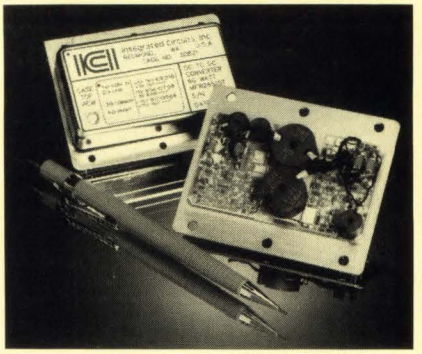

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ICI announces the addition of the MFW series of 50-70 watt DC-DC converters to its line of HI-REL devices. Up to 88% efficient, these converters are avail in 5, 12, 15 V single, dual & triple output configurations. For MIL & other HI-REL applications, 125°C T_C is possible with derated power output. Additional environment screening is avail.

Interpoint, 10301 Willows RD., Redmond, WA, 98052, 800/822-8782

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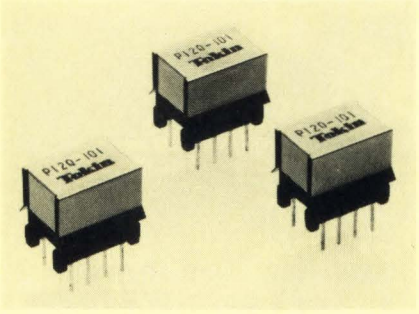

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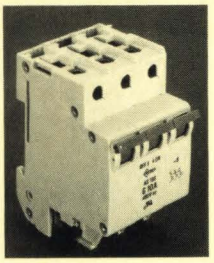

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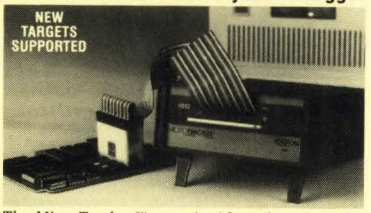

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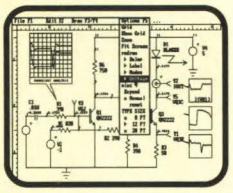

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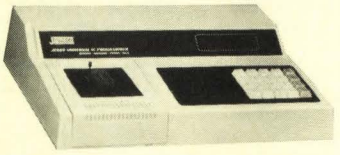

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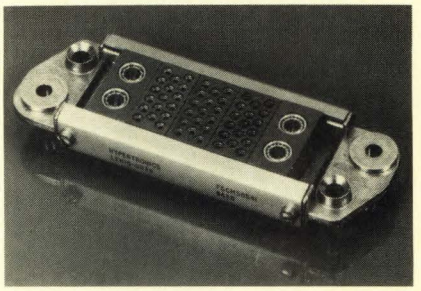

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Compilation time	*12 sec*	*18 sec*	*17 sec*
Linkage time	*29 sec*	*9 sec*	*6 sec*
Execution time	*11.46 sec*	*9.00 sec*	*1.08 sec*
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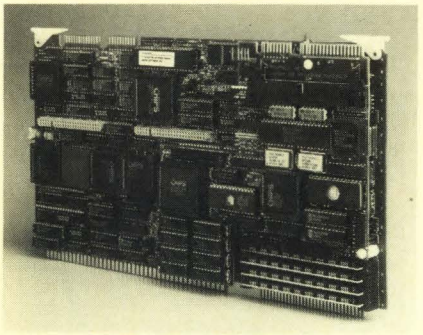

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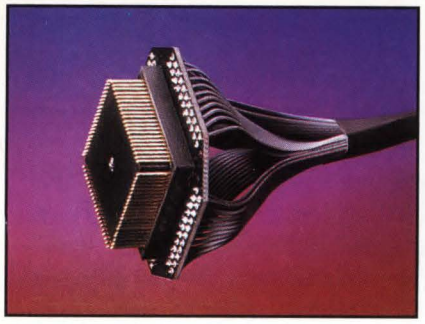

Easy Emulator Pods & Adapters

- Plug your PLCC and LCC packages into your PC board in minutes, with these easy-to-use adapters.
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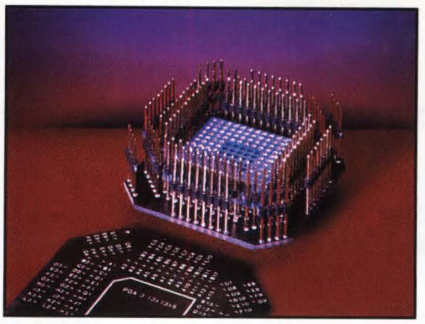

Complete Line of Debug Tools

- Famous Bug Katcher™ makes it easy to attach test leads to ICs in LCC, PLCC, PGA, PQFP, and DIP packages.
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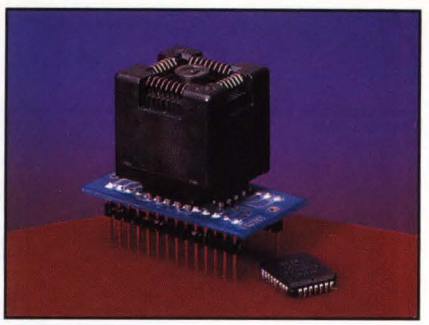

PAL/PROM Programmer Adapters

- Any EPROM programmer designed for DIPs can be converted to accept LCC, PLCC, and SOIC sockets in seconds!
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Now you can connect any VLSI or surface mount circuit to any other type of circuit—or test equipment—thanks to our complete line of adapters, connectors, and test clips. Solve *your* "wrong prong" problem—contact us today for a *free catalog!*

Wrong Prong?

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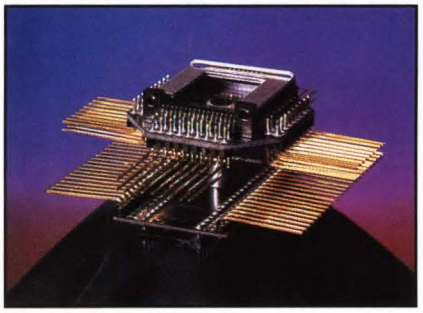

Quick, Fast Socket Conversion

- Convert-A-Socket™ makes it a snap to convert a production socket to a test socket and vice-versa.
- Complete line of male/female sockets for LCC, PLCC, PGA, PQFP, and DIP circuits.
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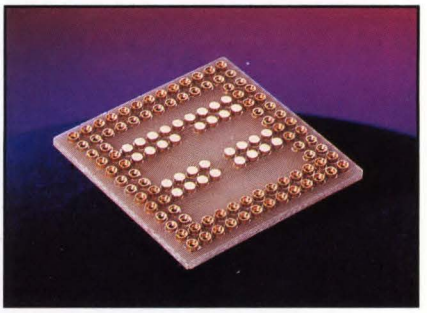

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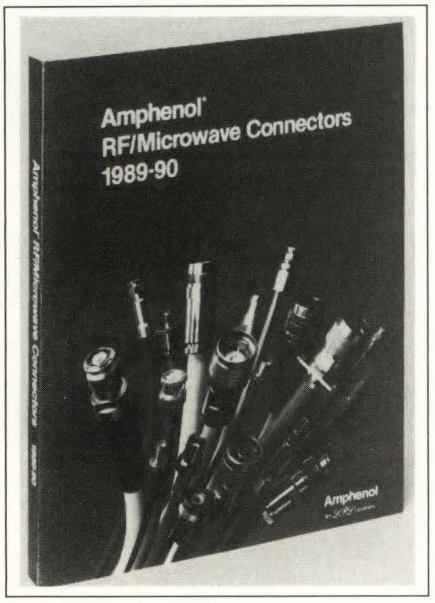


Catalog presents RF/microwave connectors

This 326-pg catalog details 34 connector series consisting of more than 4000 coaxial, triaxial, and twinaxial cable connectors, receptacles, terminations, adapters, and related products for RF/microwave and data-transmission system interconnections. Using the selection guide for RF/microwave connectors, which has a cable-to-connector index, you can start with the cable you want to use and look over the connector series options, configurations, and affixment types. Also included are indexes of pc boards and hermetic coaxial connectors, as well as 210 between-series adapters and more than 500 MIL-STD-C-39012 and MIL-STD-A-55339 connectors.

Amphenol Corp, 1 Kennedy Ave, Danbury, CT 06810.

Circle No 414

Newsletter for VXI Bus users

The VXI Newsletter keeps you up to date on new VXI products and provides show reports, user reports, and news of companies that have decided to adopt VXI. It reports on IEEE-P1155 and what's happening toward the adoption of this standard, and it describes action within the VXIbus consortium. The publication also provides an independent analysis of how VXI is going and what's ahead. Annual subscription in US and Canada, $195; overseas, $235.

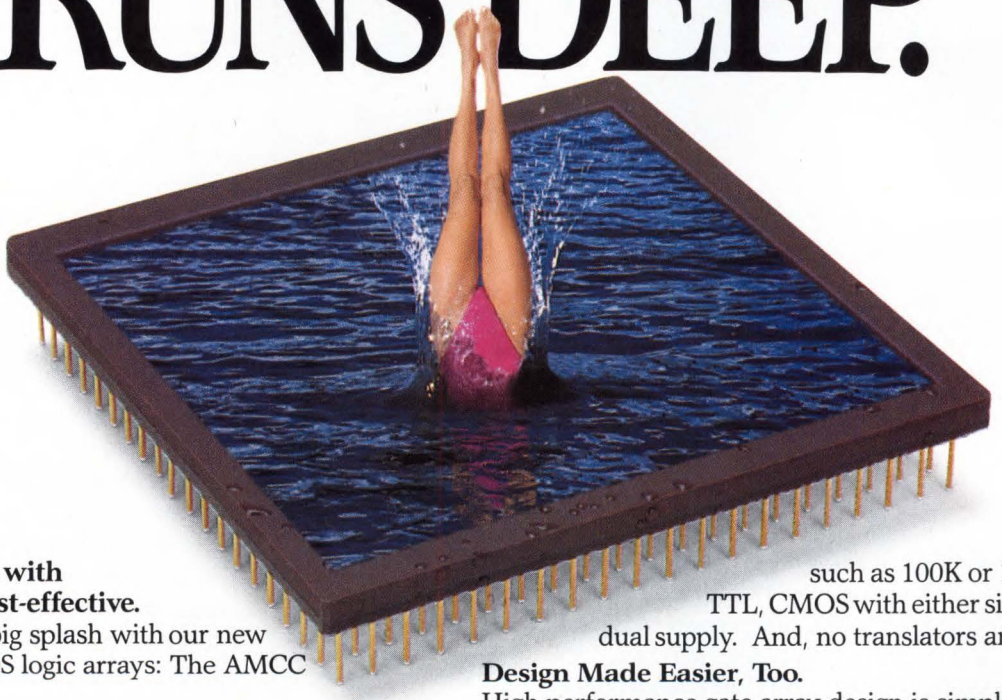
Bode Enterprises, 8380 Hercules Dr, Suite P3, La Mesa, CA 92042.

INQUIRE DIRECT

How to avoid shocking experiences

This Spring/Summer 1989 catalog (*Control ESD and avoid a shocking experience!*) covers products that direct static buildup away from your components and workplace. The 32-pg booklet describes such instruments as a wrist-strap tester,

OUR SEA OF CELLS™ PERFORMANCE RUNS DEEP.



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Equivalent Gates	2160	5760	9072	13,440
Gate Delay* (ns)	.7	.7	.7	.7
Maximum I/O Frequency (MHz)	180	180	180	180
Utilization	95%	95%	95%	95%
Power Dissipation (W)	.5 - 2.0	1.0 - 2.8	2.0 - 4.0	1.4 - 4.4
I/O	80	132	160	226
Temperature Range	COM, MIL	COM, MIL	COM, MIL	COM, MIL

*(2 loads, 2 mm of metal)

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High performance gate array design is simplified because of embedded bipolar drivers in each macro. And, with only 25 ps per fanout load degradation, critical paths are less affected by metal routing and fanout. In addition, the bipolar drivers yield symmetrical loading degradation for rising and falling edges. Less pulse width shrinkage.

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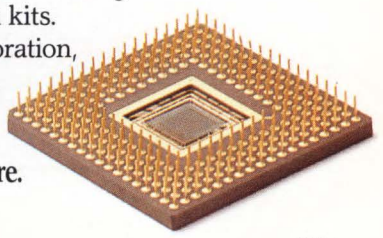

A Better BiCMOS Array is Here.

AMCC

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a charge-guard wrist strap, and a workstation grounding kit. Also included in the product section are lead formers and cutters, soldering equipment, work holders, storage bins, tool kits, and test equipment.

HMC, 33 Springdale Ave, Canton, MA 02021.

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Handbooks provide 1-stop reference for µPs and µCs

A set of 1989 reference handbooks are divided into three major product groups: super chips, embedded controllers, and microcomputer systems. Some of the subjects include microprocessors and peripherals; microcommunications; 8-, 16-, and 32-bit controllers; embedded-control applications; and OEM boards and systems. $18 to $26. A 160-pg product guide is available free of charge.

Intel Corp, Box 58130, Santa Clara, CA 95052.

INQUIRE DIRECT

Guide to in-circuit emulators

Development Tools Selection Guide details a complete line of in-circuit emulators and associated support software. Included in the list of products are 14 8-bit and 16-bit emulators, as well as source and symbolic debuggers. In addition, an application note explains the trade-offs involved in selecting languages and debuggers.

Softaid Inc, 8930 Route 108, Columbia, MD 21045.

Circle No 416

Voluminous listing of linear-power IC products

This 720-pg catalog covers more than 100 devices, listing the vendor's complete line of linear-power-management ICs. The combination catalog and design guide contains 13 chapters covering power-supply, motion-control, power-driver, and interface circuits; op amps and comparators; core memory; automotive circuits; and other devices. A collection of application notes details a range of topics from designing with integrated regulated PWMs to a tutorial on power-switch drivers for switched-mode power supplies.

Silicon General, 11861 Western Ave, Garden Grove, CA 92641.

Circle No 417

Surplus goods cataloged

This 72-pg catalog lists electronic and computer parts, as well as equipment and assembled products. The book explains that sources for the goods include manufacturer surplus, distributor excess, importer

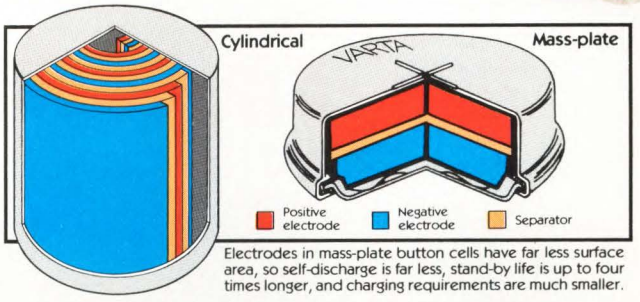
Why our button makes the better rechargeable.

Today, Varta leads the world in making cells for the smaller NiCd batteries. The reason lies in understanding the two ways cells are made. One is Varta's original development: the mass-plate NiCd button cell. Its electrodes are thick, solid masses with small surface areas. Result: a very low self-discharge which provides up to four times longer stand-by life and reduced charging current.

In the other cells, the long, thin, sintered electrodes, which are wrapped around in a cylindrical shape, have a large surface area. Result: cylindrical cells with an inherently fast self-discharge. Most of these NiCd batteries have a useful stand-by life of less than 3 months and, in use, require more frequent charging with "heavier" charging current.

Better operational characteristics. Mass-plate construction results in NiCd batteries with no "memory" effect, so they can be trickle-charged long-term without reduction in effective capacity. They have a longer, 1000-cycle life, according to IEC 509. And they can be stored in any state of charge for over five years without significant performance loss.

Safer, tougher. Mass-plate design protects against overcharge and/or overdischarge. Mass-plate cells perform better under vibration, as shown by MIL STD 810C. Key cell sizes are UL-recognized. They can be wave-soldered for up to 10 seconds in a fully charged state.

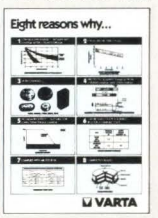


Electrodes in mass-plate button cells have far less surface area, so self-discharge is far less, stand-by life is up to four times longer, and charging requirements are much smaller.

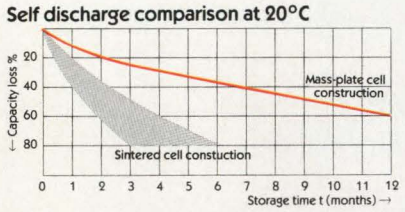
More sizes and types for any application. Mass-plate cells range from 4 mAh (world's smallest) to 1000 mAh. Taking up to 40% less space, batteries are available flat or stacked with all types of connections. Safetronic and Mempac batteries are pin-equipped for easy plug-in.

New "high-temperature" types. The Varta DKT Series can operate up to 65°C, 15° higher than before.

Most cost-effective. Despite their advantages, mass-plate buttons are competitively priced. For more information, on Varta button cells and batteries, please ask for our booklet "Eight Reasons Why....". Call 1-800-431-2504, Ext. 260, or write below.



Self discharge comparison at 20°C



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VARTA Batteries, Inc., 300 Executive Blvd., Elmsford, NY 10523, USA, Tel. 1-800-431-2504, Ext. 260
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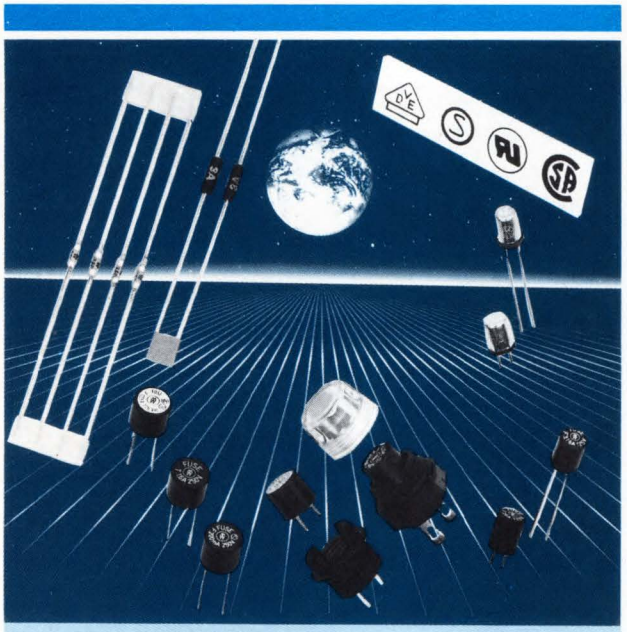

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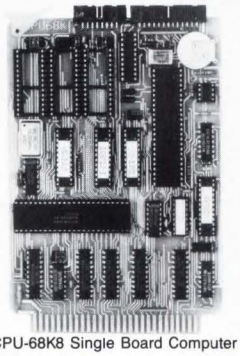

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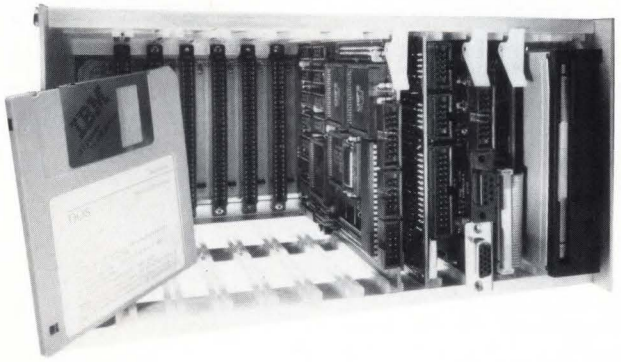

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CIRCLE NO 195

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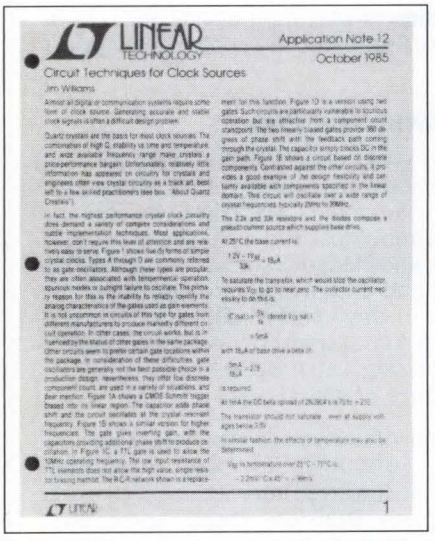
Packet of CASE information

The company's brochure and seven inserted data sheets describe TestCASE, a software-development package that integrates computer-aided software engineering (CASE) tools and functional testing for automatic test equipment. In addition to a product overview, the data sheets discuss SigmaSeries control tools, the TestPlan generator, TestBasic and programming tools, the standard template library, and the revision control system.

Summation Inc, 11335 NE 122nd Way, Kirkland, WA 98034.

Circle No 418


LINEAR TECHNOLOGY

Application Note 12

October 1985

Circuit Techniques for Clock Sources

Jim Williams

Examining alternate oscillators for clocks

The application note, *AN12: Circuit Techniques for Clock Sources,* looks at a number of clock oscillator circuits that can replace gate oscillators to achieve more reliable performance, greater accuracy, and lower drift with time and temperature. Some of the linear circuits described and presented in schematic form are an oven-controlled crystal oscillator, 10- and 25-MHz crystal oscillators, a temperature-compensated crystal oscillator, a voltage-controlled crystal oscillator, a reset-stabilized oscillator, and a stable RC oscillator.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle No 419

CAREER OPPORTUNITIES

1989 Editorial Calendar and Planning Guide

EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News Edition
July 20	June 29	Product Showcase — Volume II, Components	Closing: July 21 Mailing: Aug. 10
Aug. 3	July 13	Integrated Circuits, Computer Boards	
Aug. 17	July 27	Military Electronics, Special Issue Military Software	Closing: Aug. 4 Mailing: Aug. 24
Sept. 1	Aug. 10	Test & Measurement, Integrated Circuits	Closing: Aug. 18 Mailing: Sept. 7
Sept. 14	Aug. 24	Industrial Product Showcase, Digital ICs	Closing: Aug. 30 Mailing: Sept. 21
Sept. 28	Sept. 7	Integrated Circuits, Computer Peripherals	Closing: Sept. 15 Mailing: Oct. 5

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Duties and Accomplishments: Industry of Current Employer:

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Reason for Change: _____

PREVIOUS POSITION:

Job Title: _____

Employer: _____ From: _____ To: _____ City: _____ State: _____

Division: _____ Type of Industry: _____ Salary: _____

Duties and Accomplishments: _____

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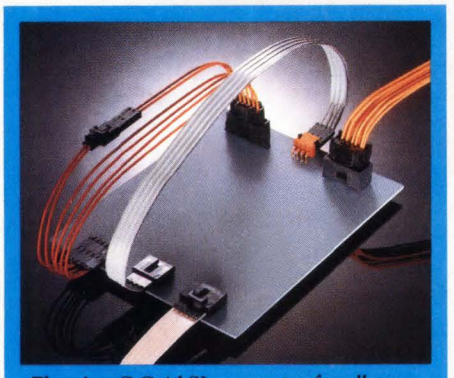

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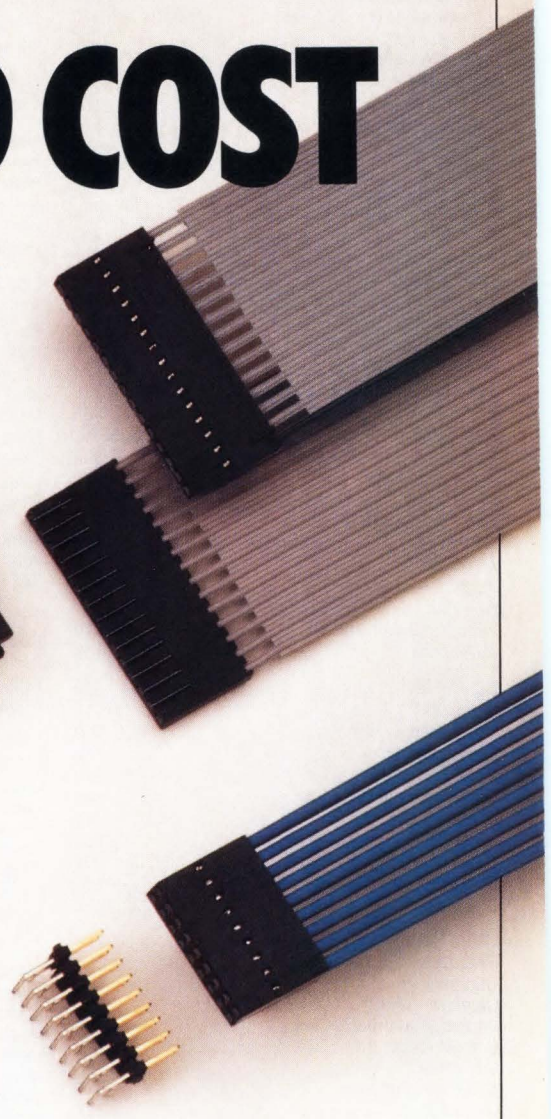

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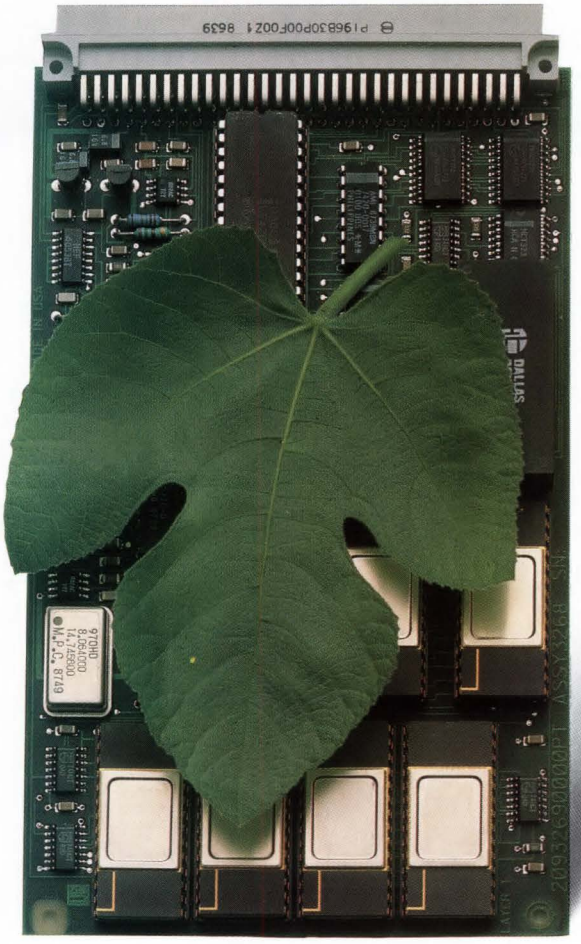

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For the bare facts about technical details and quantity pricing, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/721-8000; Telex 752602 UDS HTV.

Universal Data Systems

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Beyond that, Signal has a full line of superior low power *PC board transformers*, as well as the smaller-than-ever *"2-4-1" Series*, competitively-priced *rectifier power transformers*, *chokes* and industrial-grade step-up and step-down power isolation transformers.

We maintain significant levels of our stock transformers and sell direct – without a middleman to slow things down...or mark prices up. Even better, we can ship to you in quantity within 24 hours. We call it our *PRONTO* service.

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Signal offers you the products, the service and dependability you need. Sure, you could buy a cheap knock-off. But why would you?

For the complete free catalog on the American Originals contact: Signal Transformer, 500 Bayview Avenue, Inwood, NY 11696.

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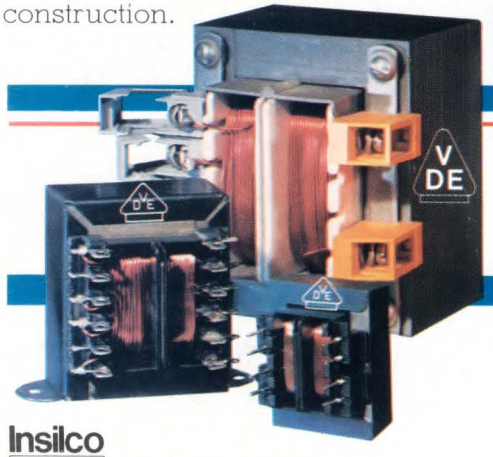

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