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AUGUST 2, 1990

EDN®

Engineering in Poland

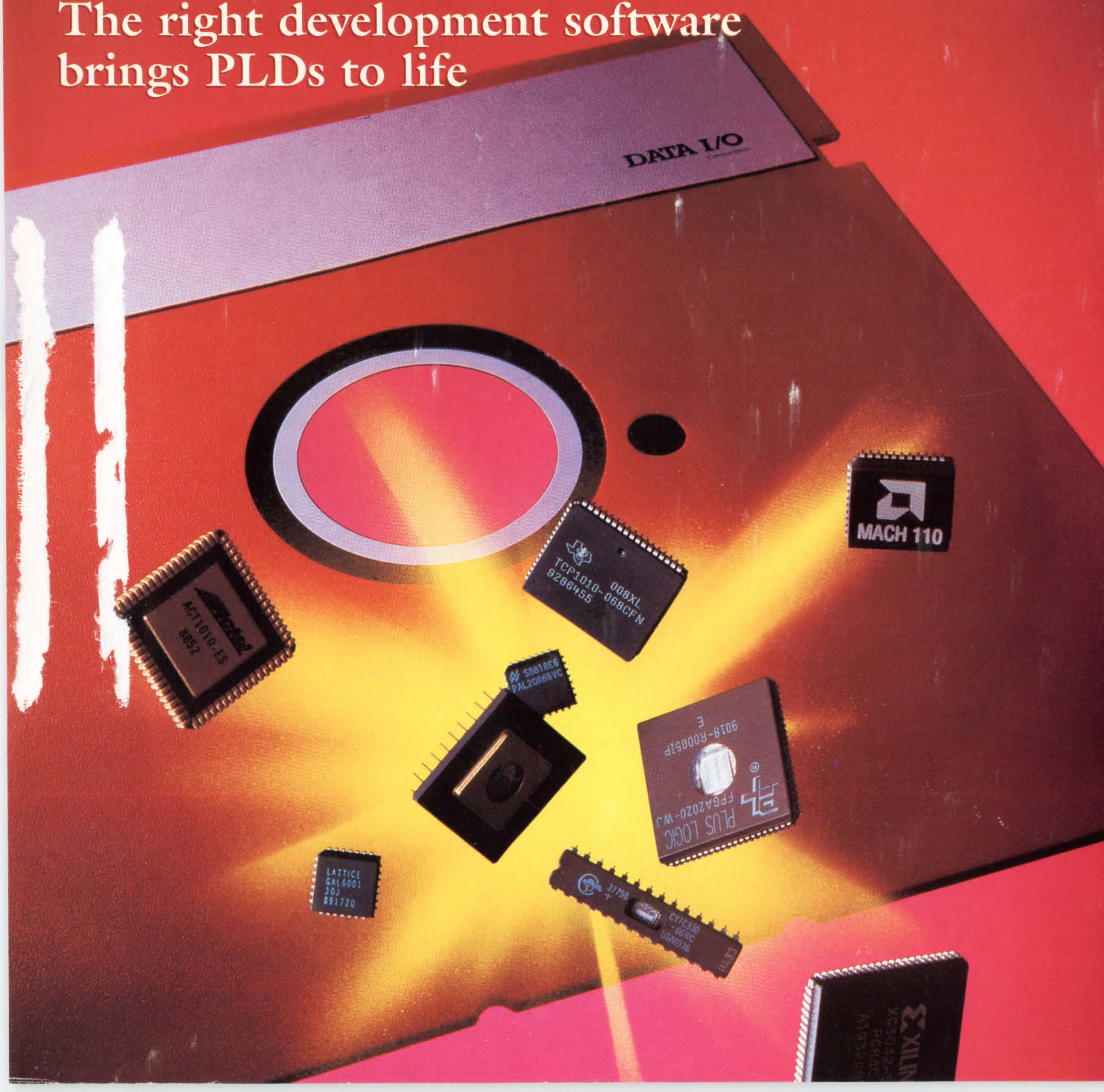
TIGA 340X0-based intelligent graphics boards

JTAG boundary-scan test eases pc-board testing

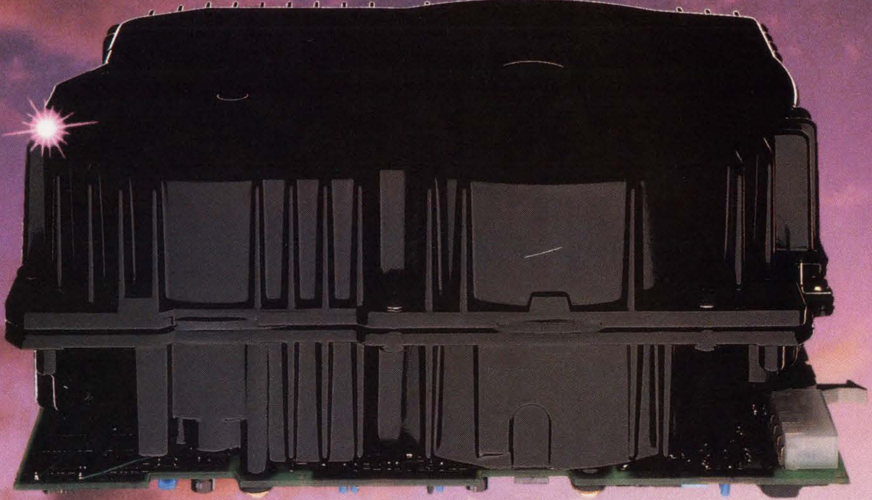
Switched-capacitor filter subtleties affect design

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report:
The right development software brings PLDs to life



HITACHI'S DK515, 5¼", 780 MB WINCHESTER



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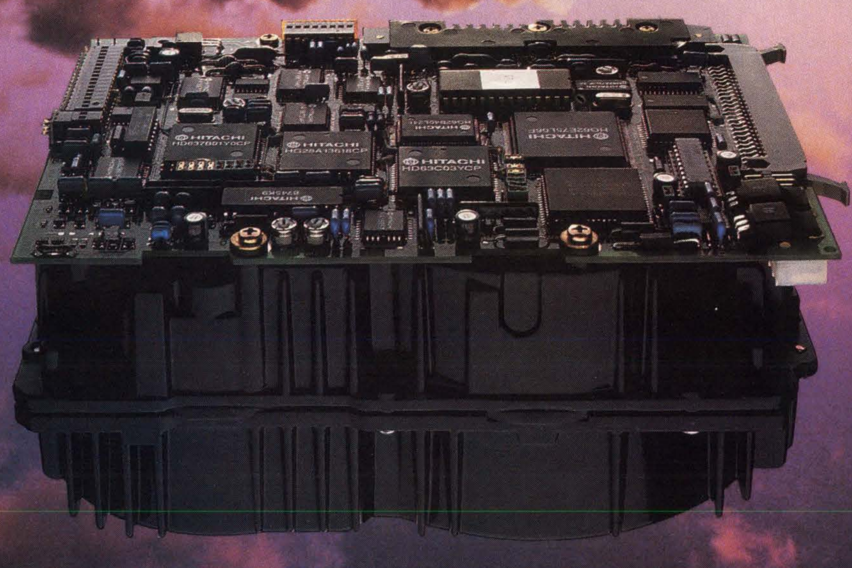

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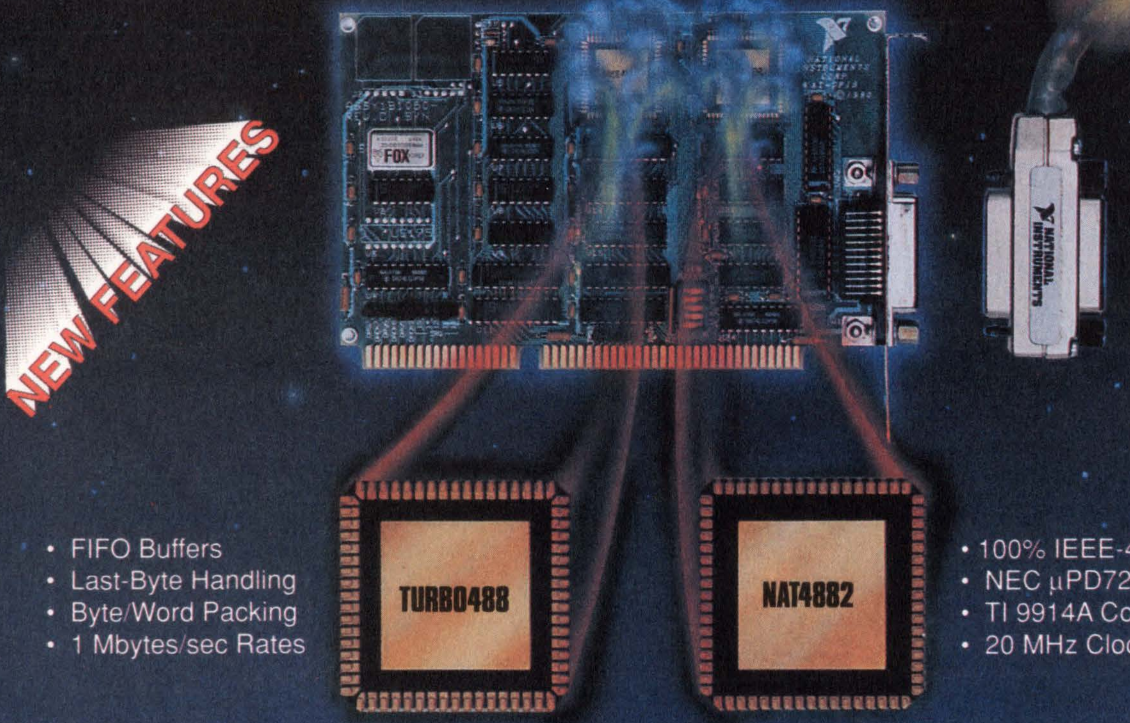

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The AT-GPIB

Custom Chips – Bringing state-of-the-art technology to you is why we've been the leader in the IEEE-488 (GPIB) market for over 14 years. Our latest AT-GPIB board for the PC/AT computer combines the functionality of our new IEEE-488.2 controller chip, the NAT4882™, and the performance enhancements of our Turbo488™ ASIC to provide 100% IEEE-488.2 compatibility, 1Mbytes/sec read and write data rates, and significantly reduced software overhead.

Enhanced Software – The performance and functionality of our NI-488 software has made it the *de facto* industry standard. The new NI-488.2 is compatible with NI-488 when using either Hewlett-Packard commands or high-level functions with popular compiled languages. A complete 488.2 controller command set, dynamic configuration, and compatibility with extended memory are but a few of the enhancements.

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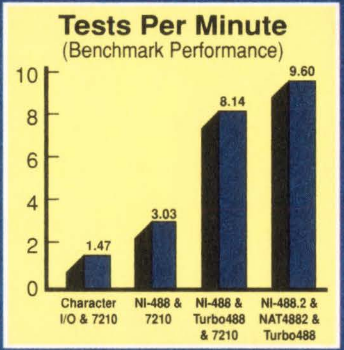

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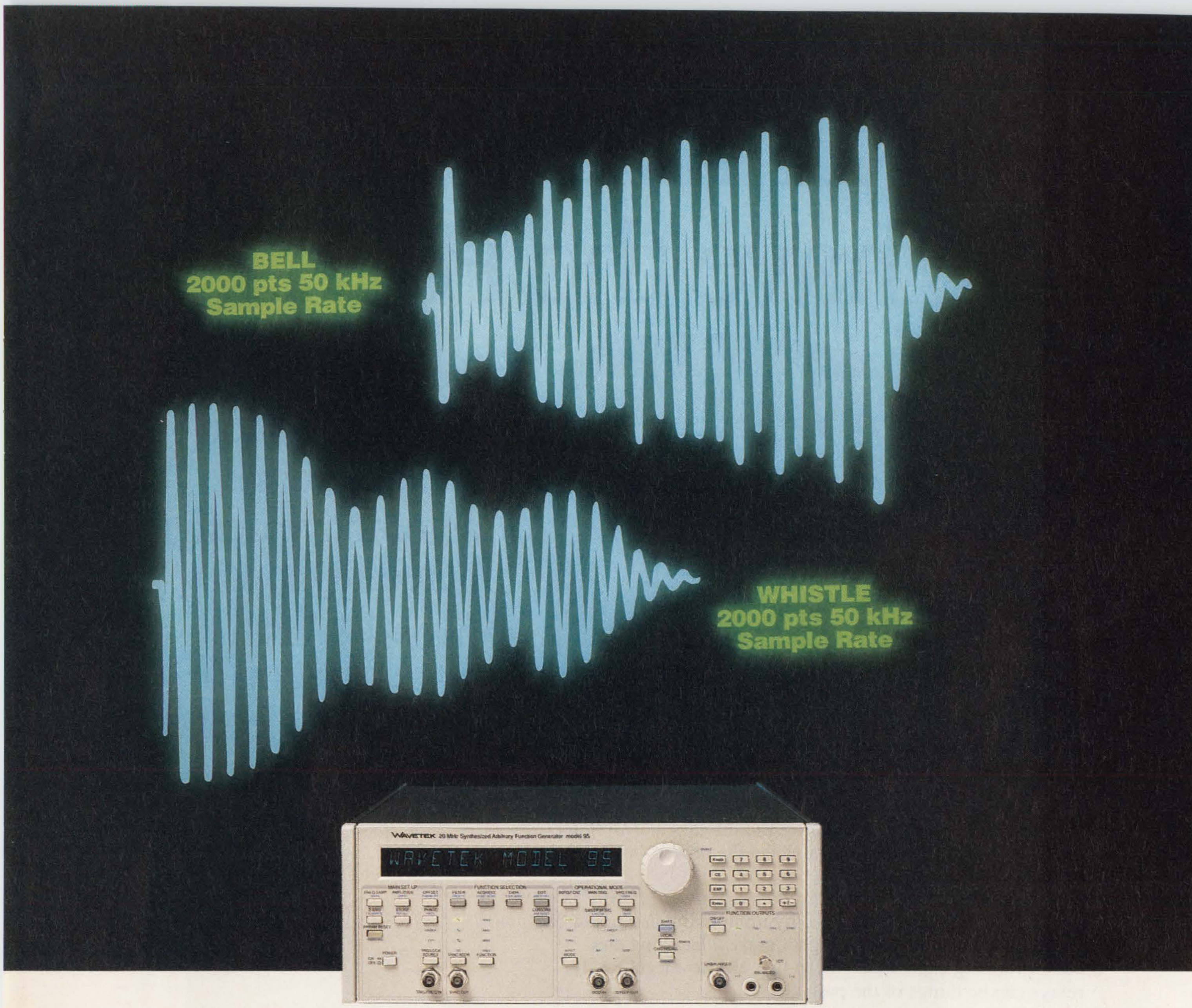

Our new function generator has all the bells and whistles.

In fact, it has any kind of waveform you can imagine. Because the Model 95 combines a high performance function generator with a powerful arbitrary generator.

As a function generator, Model 95 produces remarkably pure square waves, triangles and sines, from 1 mHz to 20 MHz with synthesized accuracy up to 0.001%. It has the power to output 15 Vp-p into 50Ω, and includes sweep, pulse and modulation modes plus four user-selectable output impedances. There's even an internal trigger generator for trigger, gate and burst.

If you'd rather be arbitrary, Model 95 gives you up to 128k of waveform memory to work with, and a sample rate of 20 MHz. Four different editing modes help you produce even the most complicated wave shapes quickly and accurately, while analog and digital filters allow you to create the purest output possible.

For information about all the other bells and whistles you'll find on the Model 95, call Wavetek San Diego, Toll Free at **1-800-874-4835** today.

Circle 34 for Literature

Circle 35 for Demonstration

WAVETEK®

Volume 35, Number 16

EDN Magazine Edition

August 2, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Choosing the right development software is as crucial to PLD-based circuitry design as choosing the right PLDs. See the Special Report on pg 100. (Photo courtesy Data I/O Corp; design by Doug Hansen Design)*

SPECIAL REPORT

DESIGN FEATURE

Continued on page 7

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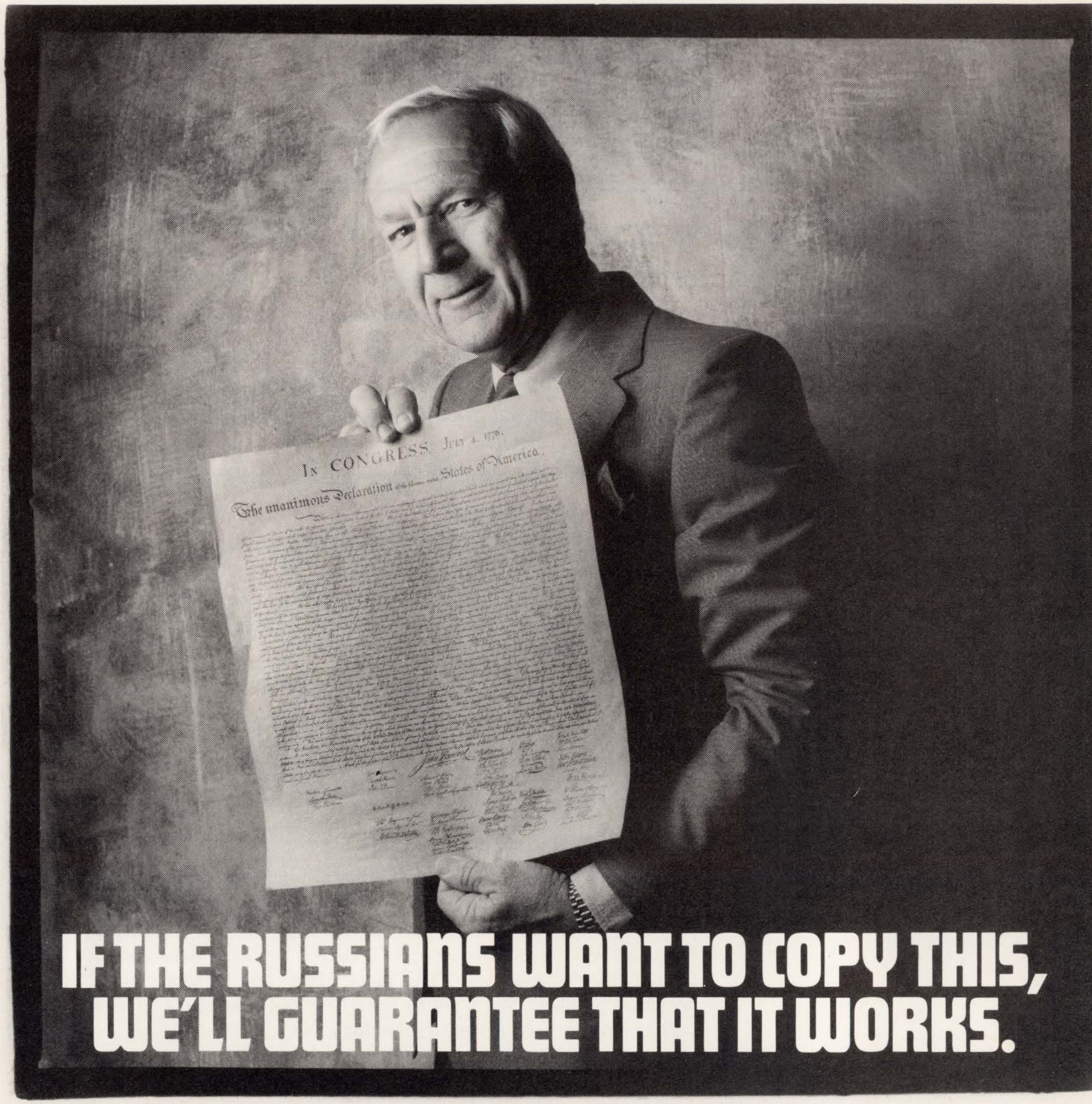
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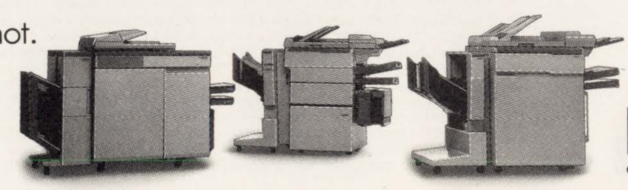
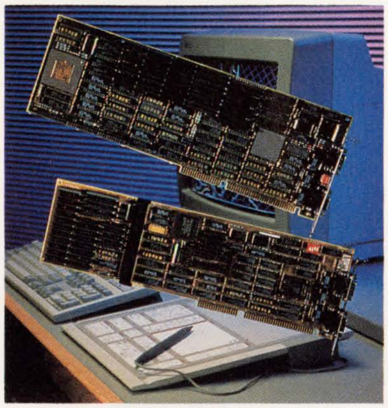


Continued from page 5



Intelligent graphics boards *based on Texas Instruments microprocessors give you workstation-quality graphics on a PC (pg 81).*

TECHNOLOGY UPDATES

INNOVATION™ Driving Electronic Technology Into The Next Century

EDITORS' CHOICE

DESIGN IDEAS

Continued on page 9

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

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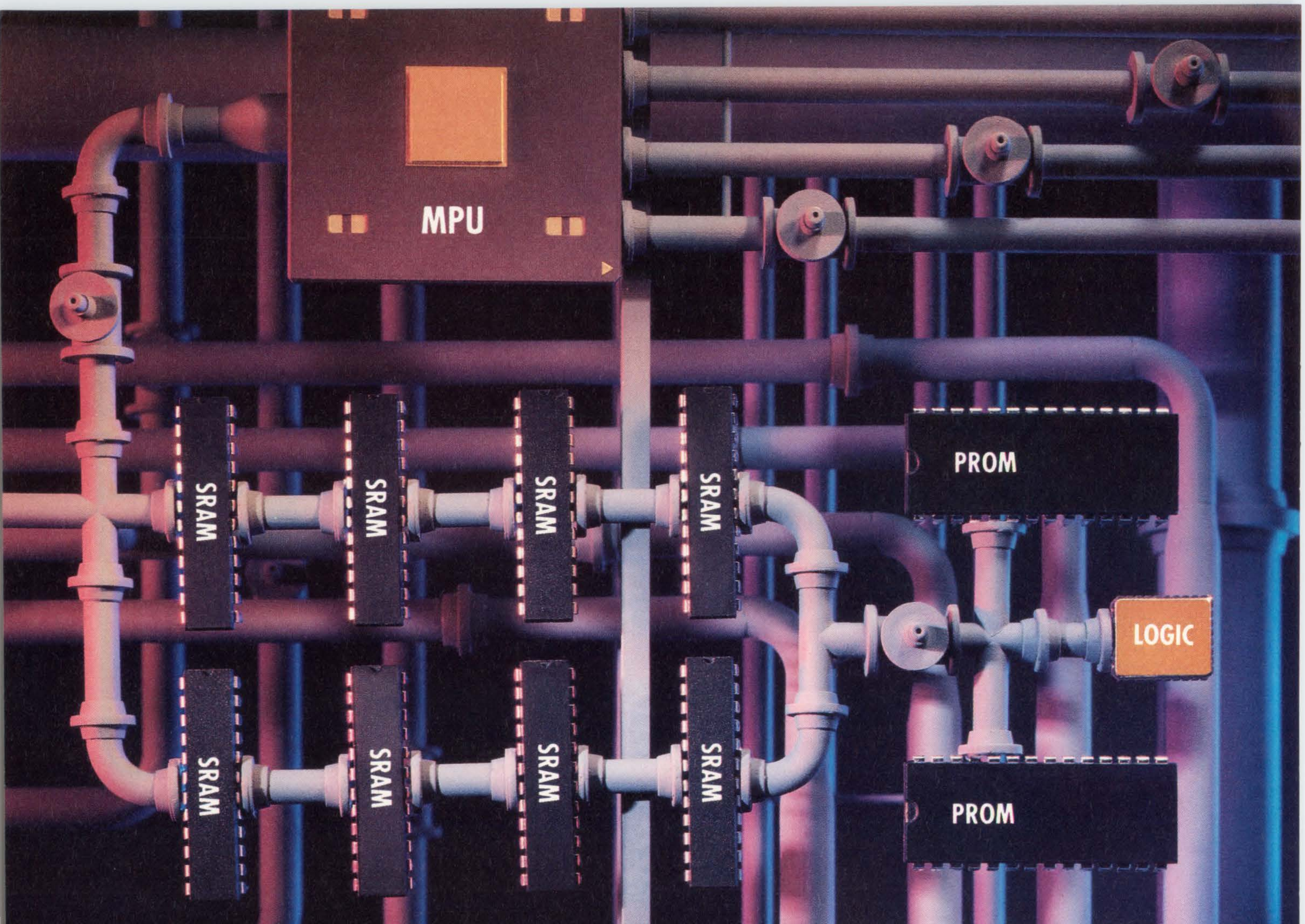
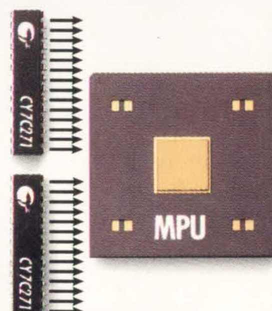


There's a much faster way around all this.

New Ultra-Fast 256K PROMs:
At 35 ns, these 300-mil parts are so fast you can run code right from PROM, eliminating SRAM and logic expense. You cut space and cost requirements significantly.



For applications such as embedded control, where space is at a premium, these new high density, high performance PROMs let you build a smaller system, or pack more functions into your existing space.

256K PROM.

You save on more than space and SRAM part costs.

You save on power, because all these PROMs are in our proven, high performance, low power CMOS.

They are available in a wide variety of packaging, including plastic DIP, CERDIP, and PLCC.

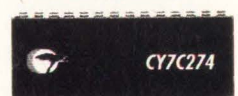
They are erasable. That lets us test every part 100% before shipping, and lets you specify windowed, reprogrammable versions.

So if you need more memory in less space with less power, go direct with our ultra-fast 256K PROMs.

256K Registered CMOS PROM. 30 ns.

256K Registered CMOS PROM. 35 ns.

Call the Hotline for your free Data Book and get the full info on all our PROMs. 1-800-952-6300.*
Ask for Dept. C4H



32 K x 8 Power Switched CMOS EPROM. 35 ns.

256K Power Switched CMOS PROM. 35 ns.

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NEW PRODUCTS

DEPARTMENTS

What's new in EDN

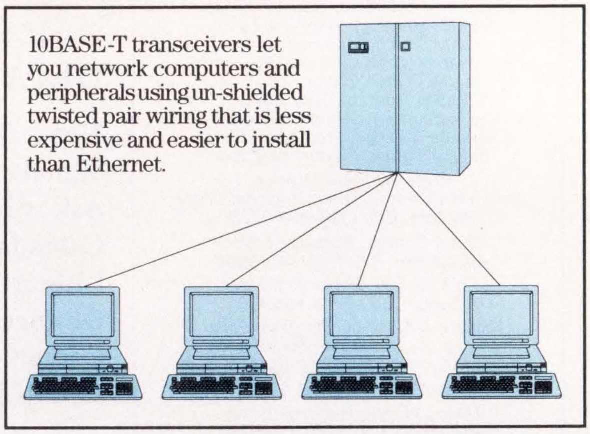
In this issue, EDN Magazine introduces a new department called Ask EDN (pg 35). In this section, EDN's editors help you solve design problems, locate parts and manufacturers, and interpret spec sheets. We'll answer as many of your questions as we can. And if EDN doesn't have the answers, we'll look for experts who can provide them or print your letter and ask our readers for their ideas. If you've got a nagging problem or a difficult question, write to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS.

The newest tw

Finally, a plug and play 10BASE-T network.

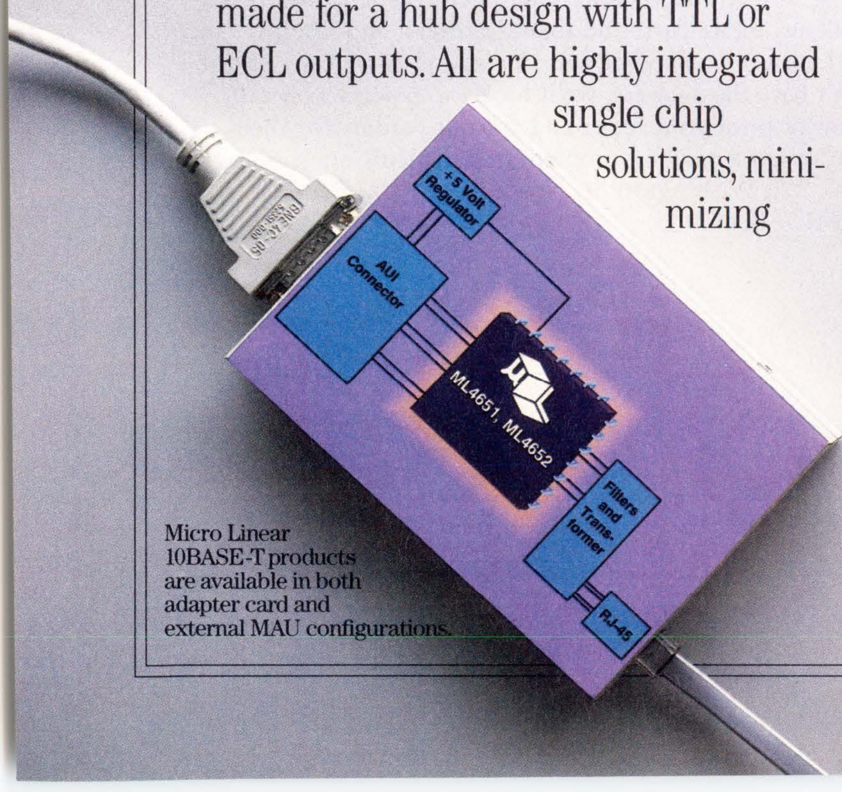
With our new ML4650 family of Single Chip 10BASE-T transceivers, you're covered all across the LAN. Because we have single chip twisted pair solutions for both ends, hub to node. Available now. In quantity. Giving you a fast, no hassle 10BASE-T solution.

On the PC side, the ML4651 and ML4652 transceivers incorporate AUI interfaces designed for both Ethernet adapter cards and external MAUs. On the hub side, the ML4654 is tailor-made for a hub design with TTL or ECL outputs. All are highly integrated single chip solutions, minimizing the number of external components required. So your design-in process is much easier. And faster.



On-chip current driven transmitters are less sensitive to noise and power supply variations. So you get superior jitter performance and low noise outputs that help you easily pass FCC requirements. And the receiver includes an intelligent squelch that rejects cross-talk noise commonly found coupling from the phone wires into the LAN. There's no external crystal oscillator required either, and devices use 5 volts only power supplies.

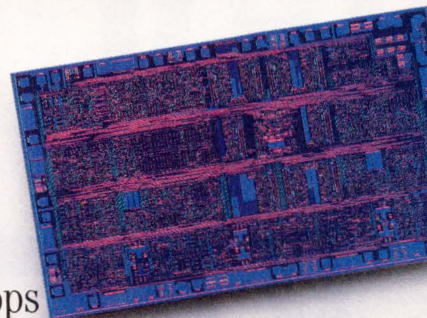
Parts are available in 20- and



Micro Linear 10BASE-T products are available in both adapter card and external MAU configurations.

ist in 10BASE-T.

24-pin skinny DIPs and 28-pin PLCCs. There's even an ML4621 Fiber Optic Inter-Repeater Link (FOIRL) receiver available to satisfy 10 Mbps fiber optic Ethernet requirements.



Semi-standard options of the standard 10BASE-T circuits are possible simply by modifying the metal mask on the FB3651 tile array.

And, unlike much of the technology you've been hearing about, these are products of experience. We've been shipping twisted pair transceivers since 1987, as part of Synoptics' LattisNet network.

Semi-standard options.

We're one of the first to market for one simple reason. Our 10BASE-T family is based on our standard FB3651 bipolar tile array. So we were able to quickly modify our "standard" product to satisfy the rapidly-emerging IEEE 802 standards.

And, for the same reason, they can be easily modified with semi-standard capability to give you proprietary product advantages. Like functional or performance modifications. Or special screening packaging or reliability levels to meet your specific network requirements. Whether it's an on-board AUI device. Or a multi-port repeater (MPR) designed to achieve that critical time-to-market advantage you've been looking for.

Call us on it.

If you'd like to turn your 10BASE-T idea into a deliverable product, just call Charles Yager today at (408) 433-5200 and ask him for the complete story on our ML4650 family of single chip 10BASE-T transceivers. Or ask for a free sample. It could add a whole new twist to your networking scheme.

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A GRAPHIC EXAMPLE OF WHY APPLE CHOSE THE AMD 29K.


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"I came here because linear leadership. I stay here vision of the linear future."

HOW NATIONAL SEMICONDUCTOR IS HELPING YOU DESIGN HIGH-PERFORMANCE SOLUTIONS WITH ADVANCED LINEAR TECHNOLOGIES.

Dennis Monticelli, National Semiconductor's Design Manager, Analog Division, talks about pushing the performance limits of linear-IC design.

Building the world's first high-speed, high-power monolithic op amp.

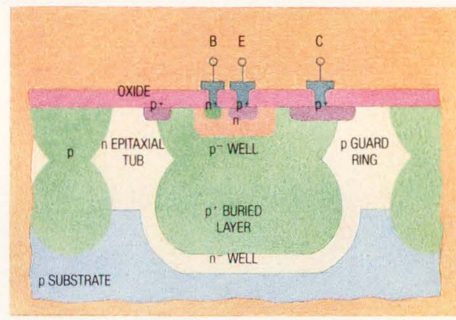
"No one in the world has ever done this before. Our LM6313 delivers a 250V/μs slew rate, yet can drive a 50-ohm load directly with a 20V swing. Before this, you'd need a separate op amp and buffer or an expensive hybrid. We did it in one device using a unique bipolar technology we call 'Vertically Integrated PNP' or 'VIP.' It's a junction-isolated complementary bipolar process. And we were the first in the industry to do it."

Setting the standard in high-resolution CRT design.

"Today's CRT designs have run out of gas. Only integrated solutions can deliver high speeds without bandwidth losses due to discrete board layouts. So we created the LM1201 video preamp. One chip. 16 pins. Replaces 40 components. Put it with our CRT driver, and you can design a 1280 x 1024 display with a 6ns pixel rate. Without the EMI. Without the real estate."

Delivering bipolar performance in CMOS op amps.

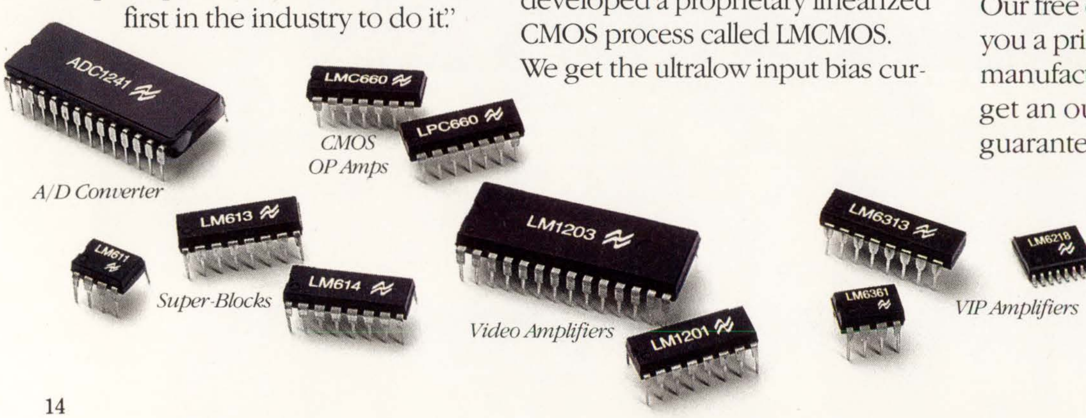
"Single-supply 5V systems need optimized op amps. So we developed a proprietary linearized CMOS process called LMCMOS. We get the ultralow input bias cur-



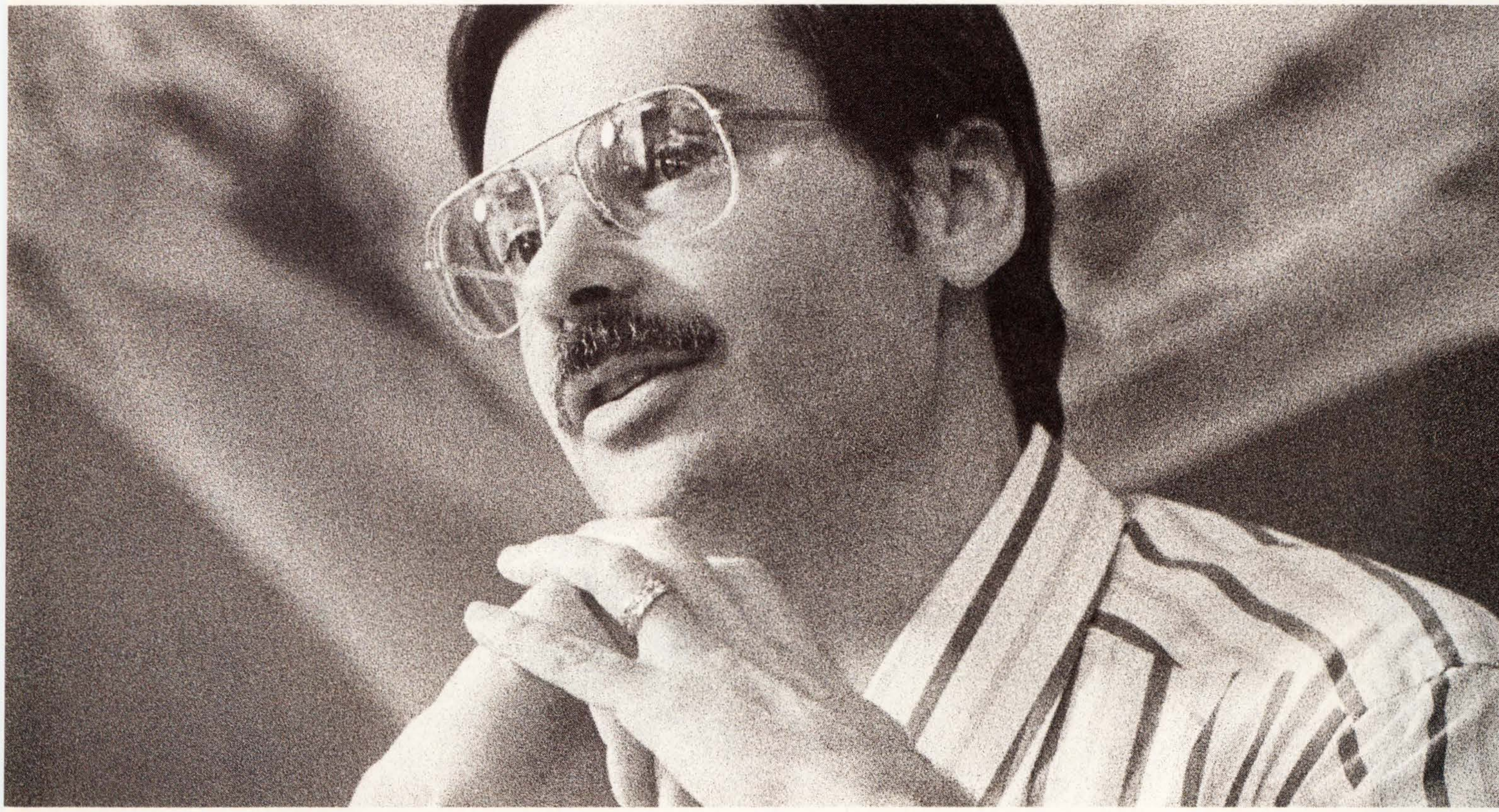
rent and frugal power consumption of CMOS with the driving power and input precision of bipolar. Our new LMC660/662 op amps, for example, can drive 600-ohm loads rail-to-rail. With input bias current of 40 *femto*amps. Remarkable."

Making switching-power-supply design truly simple.

"Switching regulators are efficient and versatile, but you need a PhD in Power Conversion to design one. Not anymore. Our new Simple Switcher family makes it easy. Our free design software even gives you a printed schematic and a manufacturers' parts list. And you get an output voltage that's guaranteed to be within ±5%



National has a heritage of because we also have a clear



regardless of line, load, temperature, and external component tolerances. Simple, right?"

Integrating three technologies to make power devices smarter.

"We've actually packed CMOS, bipolar, and DMOS onto the same chip in our new LMD18200 H-Bridge. It's rated at 55V at 3A, and delivers 150W continuous and 300W peak power to the load. All under the command of CMOS-logic-level inputs. And since R_{ON} of each FET is just 0.3 ohms, even if you draw peak current of 6A, that still leaves 50V for the motor. So it's perfect for printers, plotters, industrial controls, whatever. Now that's smart."

Putting the pride of National to work for you.

"I've spent my entire design career here at National. We have a long heritage of linear leadership. We have a clear vision of the linear future. And we have some of the best linear designers in the world, pardon my modesty. If I were in the market for advanced linear, I'd call National. Period."

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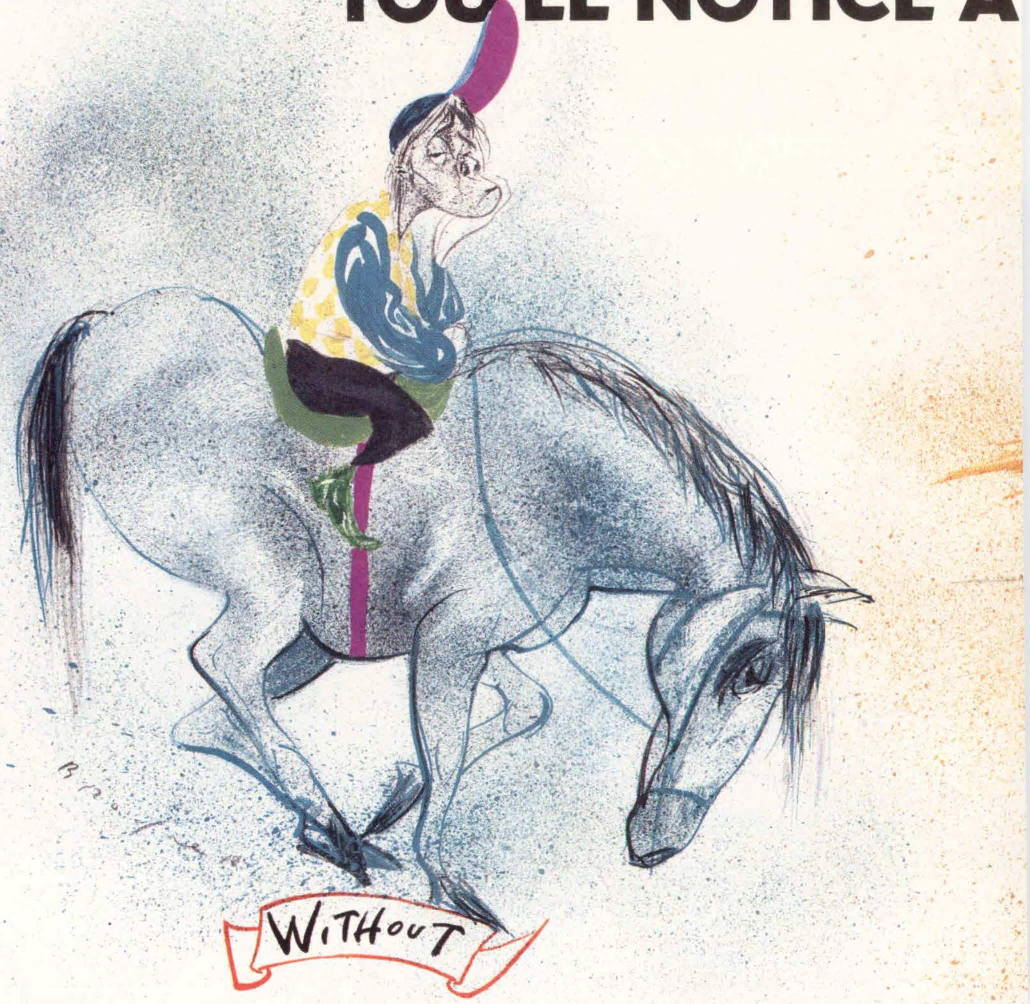
SAMSUNG NOW

68040 SYSTEMS EQUIPPED YOU'LL NOTICE A



Systems utilizing the new Samsung 84C31 take off. They run like Triple Crown-winning thoroughbreds. They blaze, scorch, and leave others in their dust.

In a word, they are fast.

And they make even speedy 68040 systems that *don't* use the 84C31, look like they're not in motion.

The 84C31 was designed with the close cooperation of Motorola. It is the *only* DRAM controller designed specifically for Motorola's powerful 68040 and 68030 microprocessors.

SAMSUNG'S DRAM CONTROLLER FOR THE 68040 AND 68030

Part Number	*RAMs Supported*	*Package*
KS84C31-33CL	256K, 1Mb	68-pin PLCC
KS84C32-33CL	256K, 1Mb, 4Mb	84-pin PLCC

Samples and production available now.

Like the extremely successful earlier-generation Samsung System Accelerators,™ the part is highly integrated and inherently fast. And as the cutting edge in memory control, it can help you simply and economically enhance even 68040 performance.

The 84C31 supports both the burst and non-burst modes of the 68040. It also provides a direct interface

WITH OUR DRAM CONTROLLER: CERTAIN IMPROVEMENT.

to the microprocessor. Which saves you dollars, board real estate, and

68030 PERFORMANCE SUMMARY

Access Clocks	*DRAM Speed*	*Frequency (Mhz)*
4-2-2-2	70 ns	20
5-2-2-2	120 ns	20
5-2-2-2	80 ns	25
6-2-2-2	120 ns	25
6-2-2-2	80 ns	33
7-2-2-2	100 ns	33

68040 PERFORMANCE SUMMARY

Access Clocks	*DRAM Speed*	*Frequency (Mhz)*
3-2-2-2	80 ns	25
5-2-2-2	100 ns	25
6-2-2-2	120 ns	25
5-2-2-2	80 ns	33
6-2-2-2	100 ns	33

design time, since it means you don't need additional glue logic.

Ease of design is another advantage. As a glance at our System Design Guides will show, it's an unusually simple chip to design in.

All in all, we believe the 84C31 is the best memory controller solution available today.

For details on using it to make *your* designs take off, contact DRAM Controller Marketing, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134. Or call 1-800-669-5400, or 408-954-7229.

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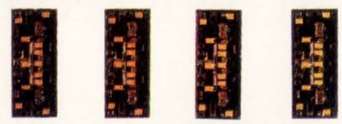
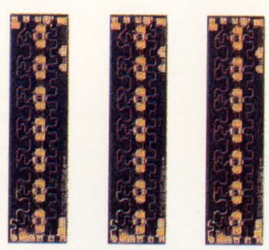
What a GaAs.

GaAs beam lead Schottky diodes optimized for 26-60GHz.

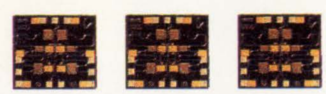


GaAs MMIC DC-50GHz voltage variable attenuator.



GaAs MMIC traveling wave amplifiers.

New Product



GaAs MMIC SPDT switches.

New Product

Products shown 10 times actual size.

Want some great news about GaAs? Check into HP. We've got a full line of GaAs high-performance products.

For openers, consider our new GaAs MMIC attenuator. The only device in the world operating from DC-50GHz.

Its wide attenuation range, exceptional bandwidth and fast switching speed make it ideal for automatic gain control, amplitude and pulse modulation switching.

Our line of GaAs Schottky diodes is optimized for 26-60GHz. But they deliver outstanding performance through 100GHz.

Along with low series resistance and low capacitance. Which ensures a high cut-off frequency and solid performance through 100GHz.

If you're looking for the right general-purpose switch, switch to HP. Our new broad-band GaAs MMIC SPDT devices offer low insertion loss and high isolation for improved system performance from DC-6GHz.

Plus they're available in both 8- and 7-lead packages for versatile drop-in replacement.

HP's great GaAs news also includes a family of high-gain, high-power MMIC traveling wave amplifiers.

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NEWS BREAKS

EDITED BY SUSAN BUREAU

TWO FIRMS OFFER NO-SLOT IEEE-488 INTERFACES

If you need to use an IBM PC-compatible computer to control a group of IEEE-488 instruments, but your PC has no open I/O slot to hold the bus-controller card, you don't have to purchase another PC. Instead, look to Cleveland, OH; two companies in that city offer solutions. IOtech's ((216) 439-4091) LPTalk488 cable plugs into a computer's Centronics-compatible I/O port and couples with the IEEE-488 bus. The $195 cable uses a parallel-port connector to mate with the connectors on PCs. Keithley Instruments ((216) 248-0400) offers the $299 500-Serial, a unit no larger than the shell of a DB-25 connector that mates with a standard RS-232C port. This unit, which plugs into and draws power from an RS-232C interface, also connects to the IEEE-488 bus. An adapter lets the device mate with the 9-pin connector used by many PCs. Both vendors include IBM PC-based software with their hardware.
—Dan Strassberg

EEPROMs SHED VOLUME

A pair of slimmed-down EEPROMs from Intel Corp (Santa Clara, CA, (408) 987-8080) should help you fit nonvolatile data storage into very small places. The 1M-bit 28F010 and 2M-bit 28F020 feature surface-mount packages measuring 20×8×1.2 mm. The 200-nsec devices cost $17.95 for the 1M-bit version and $45.20 (10,000) for the 2M-bit version.—Steven H Leibson

MILITARY-PRODUCT DATABASE INCLUDES EDIF CAE INFORMATION

Although several component-database systems exist, none except the Component Information System from Expert Views Inc (Waltham, MA, (617) 890-0333) lets you transfer MIL-spec component data to your CAE system. The database supplies graphical-symbol information and specifications to CAE systems in both ASCII format and EDIF 2 0 0. A symbol compiler lets companies convert graphics information to comply with company-wide graphics standards. The system operates on networked computers running Unix or VMS operating systems and costs $50,000 for a 1-year license, including quarterly updates. The company provides two $40,000 software packages for the system. View Master, a parts-access software package, lets users examine components and specifications. A control software package called Component Manager lets managers customize the database by eliminating some products, adding specifications for others, and including special or customized components.
—Jon Titus

CONTACTLESS SENSOR DETECTS MOTION AND POSITION

The Optometer, a contactless detector from Heimann GmbH, a subsidiary of Siemens Corp (Iselin, NJ, (800) 222-2203), provides large-area motion and position detection. The device detects alternating light and dark areas, in either a linear or circular configuration. When activated by a vertical light beam, the photodiodes produce a binary signal that indicates the moving object's position. The sensor is unaffected by noise and irregular signal levels. It offers resolutions of 0.05 to 5 mm and ranges of 50 to 200 mm. Prices are $60 to $250, depending on the features you choose.—Susan Bureau

NEWS BREAKS

PLD PROVIDES HIGH-SPEED WIDE-ADDRESS DECODING

Most high-speed PLDs give you the speed you need for address decoders in high-performance systems but not the decoding width you want. The PHD48N22-7 from Philips Components-Signetics (Sunnyvale, CA, (408) 991-2000) offers both these features by providing a 7.5- to 8-nsec propagation delay and 36 dedicated input leads for wide-address decoding. The 68-lead device also has 10 dedicated output leads, so you should be able to satisfy all the chip-enable requirements in your design with one IC. In case you need wider-address decoding or more chip enables, the device has 12 bidirectional lines that you can use as input or output pins. If you use all the lines as inputs, you can resolve a 48-bit address to a single location. The PLD costs $22 (1000); the company's Amaze version 1.9 software for programming the device is free to qualified customers.—Steven H Leibson

TEST-PROGRAM SYNTHESIS LINKS VENDORS

To automatically create tester-specific test programs, ExperTest Inc (Mountain View, CA, (415) 965-2000) and TSSI (Beaverton, OR, (503) 645-9281) plan to share their technology. ExperTest's Test Design Expert (TDX), scheduled for release in the fourth quarter, will create high-fault-coverage test patterns from behavioral and structural circuit descriptions. TSSI's Test Development Series (TDS) software will use the patterns to produce programs for more than 60 ASIC verifiers as well as component and in-circuit testers. The TDX package price starts at $150,000, and the TDS software starts at $20,000.—Michael C Markowitz

GLOBAL HIGH-TECH DEVELOPERS CONVERGE ON HAWAII

Long a melting pot for people from countries rimming the Pacific basin, Hawaii will be the setting for a conference on high-technology development in Pacific-rim countries in the 1990s. The High-Technology Development Corp (Mililani, HI, (808) 625-5293), which is administratively linked with the state's government, is sponsoring its seventh annual Governor's Symposium on High Technology. The 3-day conference will include panels and speakers discussing critical software-industry issues, strategic alliances, displays and imaging, artificial intelligence, competition between Pacific-rim and European countries in 1992, and information ethics. The symposium will take place November 13 to 15 at the Kauai Hilton Hotel.—Steven H Leibson

LOW-SKEW CLOCK BUFFER OFFERS MULTIPLE PHASES

The GA1110 clock buffer from Gazelle Microcircuits (Santa Clara, CA, (408) 982-0222) uses an internal 500-MHz phase-locked loop to match the output clock, which serves as a feedback signal to the incoming clock. You don't need external components to set the loop-filter parameters. The six TTL-compatible output signals can drive as much as $+-24$ mA.

If you use an unmodified output signal as the feedback, the input and output clocks will match within 500 psec. You can alter this value by inserting additional logic delays between the output and feedback pins. You can choose from four sets of clock output phases, including combinations of inverted signals and phase shifts of $+-2$ and -4 nsec. By using different output phases for the feedback, you can obtain phase shifts as great as $+-6$ nsec. Available with 25-, 33-, and 40-MHz speeds, the clock comes in a 16-pin DIP and costs approximately $35 in sample quantities.
—Richard A Quinnell

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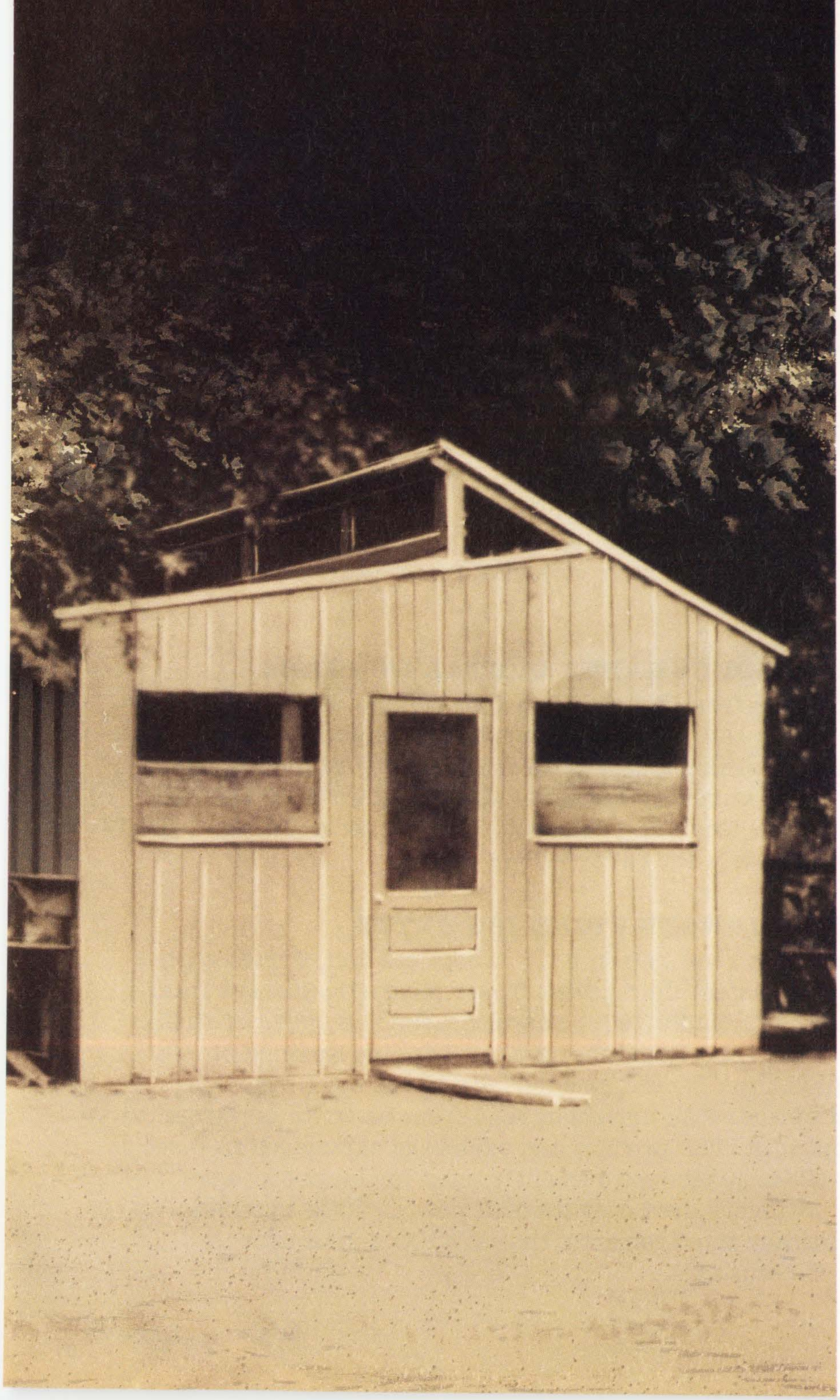

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NEWS BREAKS

COMBINING FRAMEWORKS TO PROMOTE ORDER

Bringing order out of chaos is the goal of a 3-year agreement between Digital Equipment Corp (Maynard, MA, (508) 467-3589) and Cadence Design Systems (San Jose, CA, (408) 943-1234). The companies are attempting to combine their tool-integration and design-management frameworks with standards such as the CAD Framework Initiative's framework specification, the Open Software Foundation's Motif, and the X Window System. Under the agreement, Cadence can sell the DEC Powerframe framework to its customers immediately.—Michael C Markowitz

ADA DEVELOPMENT SYSTEM RUNS ON PCs

It's not exactly the low-budget language compiler that many programmers have come to expect for PCs, but at $1815, FirstAda from Alsys Inc (Burlington, MA, (617) 270-0030) is relatively cut-rate for a validated Ada development system. This price gets you an optimizing compiler that generates 8086/8 or 80286 code, a debugger, an automatic-recompilation utility, a cross-reference generator, a source-code reformatter, and a high-speed syntax checker. You also get a text editor and a beginner's guide to Ada. The package runs under DOS and requires a 640k-byte machine with at least 2M bytes of extended memory and 7M bytes of space on your hard disk. —Steven H Leibson

TWO CMOS FAMILIES MEET ESA RADIATION-IMMUNITY SPEC

SGS-Thomson Microelectronics (Phoenix, AZ, (602) 867-6100) supplies two families of rad-hard (radiation absorbed dose) CMOS logic chips for military, aerospace, and similar applications. The 100k-rad CMOS 4000B family meets the European Space Agency's (ESA) 50k-rad radiation-immunity specification for high-speed CMOS logic. The company expects the ESA to approve their second CMOS family, the HSCMOS line, in the first quarter of 1991. Both logic families come in a variety of ceramic packages, including dual in-line and chip-carrier versions. Prices start at $40 (500). —Susan Bureau

STD BUS CARD OFFERS 144 HIGH-CURRENT DIGITAL I/O LINES

The ZT88CT72 Digital I/O interface from Ziatech (San Luis Obispo, CA, (805) 541-0488) can sink 12 mA on each of its 144 I/O lines. Competing products usually have only 48 channels and 3-mA current-sinking capabilities. The company made these improvements in channel count and current sinking by designing an ASIC instead of using standard off-the-shelf parts. The STD bus card operates over a −40 to +85°C range. The unit is available immediately for $495.—Doug Conner

12-IN. OPTICAL DRIVE AND CHANGER STORE 28G BYTES

For extremely large on-line storage requirements, 12-in. optical-disk drives with jukebox disk changers provide the fastest data access. Laser Magnetic Storage International Co (Colorado Springs, CO, (719) 599-7900) has increased the speed of these drives further with its 28G-byte LF 4500 RapidChanger, a 12-in., write-once optical-disk drive with a 5-cartridge magazine. Each disk cartridge stores 5.6G bytes on 2-sided media, and the integral optical-disk drive can read from or write on either side of a cartridge without flipping it. The product can exchange cartridges in 3 sec or less—much faster than the 12-in. jukeboxes currently used for large storage applications. The $16,000 unit transfers data over its SCSI port at 700k bytes/sec. For applications with smaller storage requirements, the LD 4100 1-disk unit is available for $12,000.—Steven H Leibson

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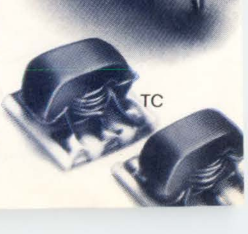
case styles
T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593



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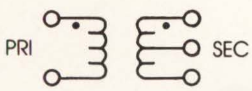
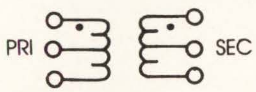
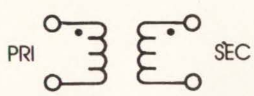
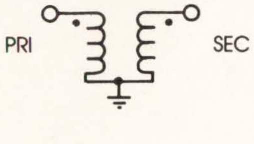
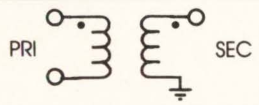
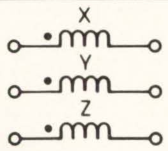
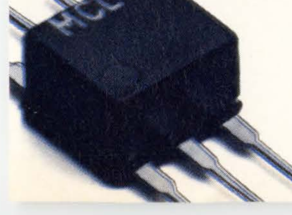
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

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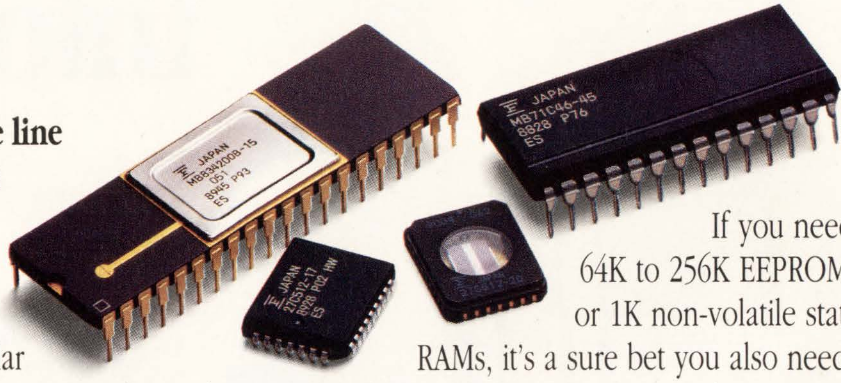

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Like the growing need for personal communication devices and for ICs in desktop and portable computing. As well as devices for computer networking with compatibility across platforms. And for ICs that meet the need for robotics and automation in manufacturing.

We're also drawing from nearly a century of Philips innovation to apply our consumer technologies to the business world. Including digital video and high-density compact disc storage.

In fact, wherever your design needs take you, Signetics will be there with complete families of devices to meet emerging computing, communications and control needs.

Philips Components

you've put so much
it perfect.

OF ICs, YOU GET OUT OF IT WHAT YOU PUT INTO IT.

COMPUTING		COMMUNICATIONS		CONTROL	
APPLICATION	PRODUCT	APPLICATION	PRODUCT	APPLICATION	PRODUCT
Workstations	• Advanced BiCMOS Logic • High Speed ASICs • Futurebus Chip Set • High Speed PAL®-type Devices • High Performance MCUs • SRAMs	Cellular Communications	• Cellular Chip Set • Frequency Synthesizers	Automotive Control Systems	• 8-bit 80C51-based MCUs • OTP EPROMs • Linear/Digital/Mixed Mode ASICs
		Mobile Telephony	• Paging ICs • Frequency Synthesizers		
Personal Computers	• High Density ASICs/PLDs • DRAM Controllers • OTP EPROMs • FLASH Memory	FAX/Modems/ Features Phones	• 8-bit 80C51-based MCUs • E^2PROM • LCD Drivers • Dialers • Speech Circuits • RF Chip Set	Consumer Appliances and Entertainment	• A/D MCUs • LCD Displays • Audio Circuitry • Dolby Noise Reduction • Frequency Synthesizers
Desk Top Video	• A/D Converters • Digital Color Decoders	DataComm LANs	• Ethernet Chip Set • 100-Mbit Fiber • High Speed PLDs • Advanced BiCMOS Logic	Industrial Control & Robotics	• Advanced BiCMOS Logic • UV/OTP EPROM MCUs • Real-Time Bus Communications Controller
Peripheral Products	• 8-bit 80C51-based MCUs • Zero Power PLDs • Programmable Sequencers • 3-State ECL Transceivers	Multi-Protocol	• Dual Universal Serial Controller • UARTs and DUARTs	Portable Instrumentation	• Low Voltage/Power MCUs • Advanced CMOS Logic • LCD Drivers

As illustrated above, we're listening to customer needs and developing products in three focused areas: computing, communications and control.

This includes products based on our advanced BiCMOS technology, QUBiC. Developed from our strength in bipolar technology and fully integrated with our sub-micron CMOS technology, QUBiC gives you nearly twice the speed of previous-generation bipolar ICs. With CMOS power savings. We're incorporating QUBiC into all our product families, creating a new class of high-performance devices.

Philips Components-Signetics is committed to the military market, with over 80% of our ICs meeting MIL-SPEC certification. This commitment is evident in our Class S domestic assembly plant and DESC-certified wafer fabs.

To learn how Philips Components-Signetics helps you make the perfect design, call today for more information: 800-227-1817, ext. 711D.

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Signetics

EXTENDING THE DIMENSIONS OF PERFORMANCE

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CIRCLE NO. 78

SIGNALS & NOISE

On abbreviations and communications

The purpose of my discussion of abbreviations is twofold:

1. As EDN and other publications are vehicles to educate and inform engineers, I feel very strongly about keeping communication lines open and uncluttered as our industry grows more diverse daily. Journals keep the industry communication lines open by disseminating information across engineering boundaries.

2. Our young engineers just starting on this exciting road of electronics are confused enough already. This journal should be an example for these engineers to learn and copy from.

The standards we transmit to readers today will shape the future of intercommunication in the industry, bringing understanding to many. [This understanding] may help solve problems today or help bring forward the discoveries of tomorrow.

In Anne Swager's article (EDN, March 29, 1990, pg 59) on analog-to-digital converters (ADCs), I seemed to have gotten tangled in more than 40 undefined or mixed abbreviations. I haven't been a long-time reader of your journal; however, I've been reading technical journals of similar caliber for many years. I note that unexplained abbreviations are usually a professional trait that hides ignorance or tries to impress—and succeeds in doing neither.

Even the military has noted, as a documentary necessity, that there are standards and etiquette for using abbreviations. This etiquette [dictates] writing out the meaning of abbreviations in full at the first occurrence, with the abbreviation following in parentheses. In the article by J D Mosley (EDN, March 29, 1990, pg 79), FDDI was handled in exactly this way.

Anne's article was of interest, but its inconsistency was distracting. Please explain what the first sentence, fourth paragraph on pg 59 was trying to say. Aren't hybrids integrated circuits? Also in the same paragraph, is the "sample-and-hold function" the same as S/H?

On pg 61, I think what was meant is that "The HDAS-75 and -76 75-kHz hybrids *typically* dissipate 500 mW" [rather than 500 mW typ]. Lastly, I do not think the number of pins determines the interface type (serial or parallel) as the fifth paragraph on pg 64 would suggest. As a magazine dedicated to inform and educate, I am pleased in general with the level of communication your journal offers.

Chris Gidden
Crag Consultants Ltd of St Helier
Jersey Channel Islands
Gardena, CA

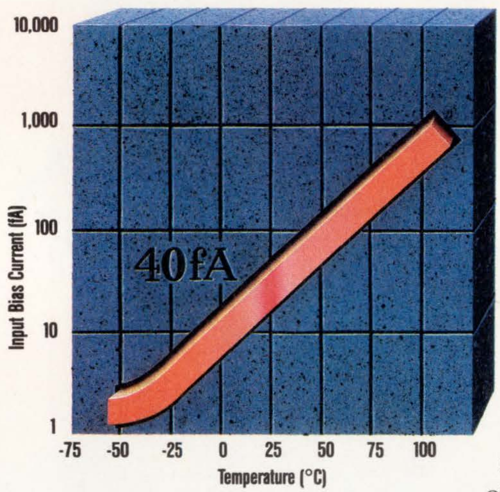
(Ed Note: EDN acknowledges that the electronics industry is full of acronyms, and we strive to invent none of our own. However, we do maintain a list of what we believe are commonly understood abbreviations. That "S/H" stands for "sample and hold" and "ADC" for "analog-to-digital converter" are just two examples of abbreviations we expect most of our readers to be familiar with. When we use less common abbreviations, we do spell them out on first use.

Rather than use monolithic IC and hybrid IC throughout the entire article, the author chose the common usage of IC as monolithic and hybrid for a hybrid IC. As far as this article is concerned, the words "sample and hold" simply refer to the function, and "S/H amplifier" refers to the physical device.

Chris Gidden correctly points out that the number of output pins in and of itself does not determine a device's interface type. However, because monolithic ICs are typically smaller than hybrid packages (and therefore don't have the space for a large number of output pins), most manufacturers design these monolithic data-acquisition ICs with serial interfaces.) EDN

National Semiconductor

National's family of CMOS op amps rises to a new all-time low: 40 femtoamps.



INPUT BIAS CURRENT VS. TEMPERATURE: 40 fA AT 25°C

TAKING IT TO THE LIMITS WITH ULTRA-LOW INPUT BIAS CURRENT.

National's new quad/dual CMOS op amps, the LMC660/662 and the LPC660/662, feature an extremely low input bias current of 40 fA typical. You can't go much lower.

FEATURING RAIL-TO-RAIL OUTPUT SWING.

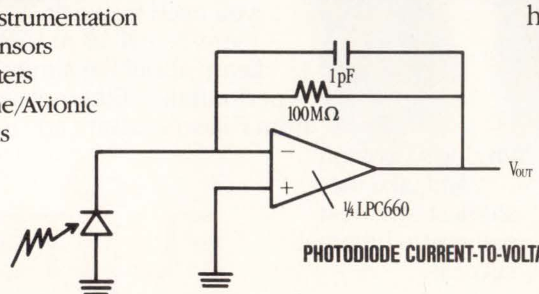
With a newly patented double feed-forward circuit architecture, National's op amps provide an output swing that extends from one supply rail to the other. You can't swing any more than that.

Use the LMC660/662 and LPC660/662 to drive rail-to-rail input A/Ds, or take advantage of the LMC's fully specified 600 Ω load capability to process audio in telecom and cellular radio applications. Other typical applications include:

- Handheld meters
- Medical instrumentation
- Remote sensors
- Electrometers
- Spaceborne/Avionic subsystems

NATIONAL REDEFINES SINGLE-SUPPLY OPERATION.

In the past, a single-supply op amp was an amplifier whose input common-mode range included ground. But in today's +5V systems, you need op amps that take advantage of every last volt that the supply provides, and whose outputs swing fully from rail-to-rail. National was the first to deliver rail-to-rail performance with the LMC660 and now has a complete family— all in CMOS.



PHOTODIODE CURRENT-TO-VOLTAGE CONVERTER

POWER UP WITH LOW POWER AND MICROPOWER.

If you're looking for low power, there's the LMC660/662, which operate at 375 μA/amplifier. Or if your application calls for 40 μA/amplifier, we offer the LPC660/662, micropower versions of the popular LMC series. In either case, you get lower power dissipation and a longer lasting battery.

LMC660/LPC660 VS. THE COMPETITION

	LMC660AI	LPC660AI	TLC274AI
Output Swing ($V^+ = +5V$)	**0.15V to 4.82V**	**0.03V to 4.97V**	**0.05V to 3.2V**
V_{OS} (max)	3 mV	3 mV	5 mV
I_b (typ)	40 fA	40 fA	600 fA
Supply Current (typ)	375 μA/amp	40 μA/amp	675 μA/amp

GET THE LOWDOWN.

For more information on our new CMOS op amps and growing family of high-performance amplifiers, including VIP,™ Bi-FET,™ Super-Blocks,™ and precision, call or write us today: 1-800-624-9613, Ext. 66. In Canada: 1-800-548-4529, Ext. 66. National Semiconductor Corporation, P.O. Box 7643, Mt. Prospect, IL 60056-7643. And find out how we can help take your designs to new heights.

National Semiconductor

ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Have you been stumped by a design problem so long that you don't know who to turn to? Are you having trouble locating parts? Finding companies? Can't interpret a spec sheet? Ask EDN.

This department will serve as a forum to solve nagging problems and answer difficult questions. EDN's editors will provide the solutions. If we can't solve a problem, we'll find an expert who can, or we'll print your letter and ask your peers for help. We can't answer every question, but we'll try to publish the ones that will help you most in your job.

Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS.

Reader seeks frequency converter

Can you tell me where I can purchase a 6A frequency converter that will take 120V ac, 60-Hz input and allow 100 to 120V ac, 50-Hz output? My company needs such a converter for the in-house testing of products used in foreign countries.

If you do not know of such equipment, have you published information on an electrical circuit for such purposes?

I J Rocklin
General Manager
Rocklin Manufacturing Co
Sioux City, IA

We found more than 20 companies that offer frequency converters with the specs that Mr Rocklin is looking for. The list includes

Abacus Controls Inc
85 Readington Rd
Somerville, NJ 08876
(201) 526-6010

Industrial Test Equipment Co
21 Yennicock Ave
Port Washington, NY 11050
(516) 883-1700

Power Star Inc
17346 Eastman St
Irvine, CA 92714
(714) 261-5377.

Senior Editor Charles H Small offers this piece of advice:

"As a former engineer at an uninterruptible-power-supply company, I have some simple advice that may surprise you: Make a motor/generator set. Get a 60-Hz motor and a generator rated for 50 Hz. Mount appropriately sized pulleys on the generator and motor shafts and connect the pulleys with a V belt.

"Such a setup is easy to cobble up from readily available components. The generator output will be a clean, isolated sine wave. The setup is robust; if you add properly sized circuit breakers, the setup will survive any conceivable insult. You can't say the same for small solid-state converters."

Reader in the dark about light pens

Where can I find light pens?

A Banerjee
Research and Development Engineer
Orphic Systems Inc
Philadelphia, PA

Among the dozen or so companies that offer light pens are

Design Technology
5710 Ruffin Rd
San Diego, CA 92123
(619) 268-8194

Opto Technology Inc
562 Chaddick Dr
Wheeling, IL 60090
(312) 537-4277

Rehlander Associates
118A Bridge St
Beverly, MA 01915
(617) 922-5961.

Help locate software company

I am hoping that one of your readers can help me locate a software program once advertised in your magazine. The program is "Partlister" from Livewire Software, Pacific Palisades, CA. I have tried for several months to contact them, but they seem to have either moved or gone out of business.

If anyone can help me find a copy of this program, I would certainly appreciate their help.

Jon Sanserino
Technical Director
Datawave Inc
Van Nuys, CA

We called the phone number on the advertisement that Mr Sanserino included with his letter, but the number is now that of a private citizen, to whom we apologize for bothering. If any reader knows the whereabouts of this company, please drop Ask EDN a line.

EDN

You Can Only Go to a

Oki's New 0.8μm ASICs

If your ASIC vendor's 1.0μm product is at the end of its shrink, your anxieties are justified. When they'll get to the higher speeds and densities you need for next-generation products is a good question.

Oki's there now. Our new family of *true* 0.8μm drawn sea-of-gates offers the migration path you need to 0.6μm, 0.5μm, and beyond. With 200 ps to 400 ps gate delays and 500 MHz flip-flops, these new CMOS 5-Volt SOGs provide the high-speed performance your systems require now—and in the future. Manufactured on a proven, high-volume production line, they also provide the guaranteed quality and reliability your systems demand.

Choose from a range of products—4K to 92K usable gates—and JEDEC metric packages, including QFP and PGA. Our automatic test vector generation (ATVG) capability using scan macros allows you to achieve greater than 95% fault coverage. And it's easy to design with Oki ASICs. We support many popular industry-standard platforms and offer industry-standard in-house tools such as Verilog® and Explorer Rene.™

Start easing your ASIC anxieties today. Call 1-800-654-6994 and schedule a consultation. We'll analyze your ASIC needs and provide the complete design support you need for today's high-density systems—and for those even higher performance systems you've thought about, but couldn't design. Now you can—with Oki.

Transforming technology into customer solutions

Shrink for So Long

0.8µm Oki ASIC Product Family

Family[1]	Estimated Usable Core Gates[2]	No. of I/O Pads	Package Types PLCC	QFP	PGA
MSM10S01XX	4K	100	68, 84	60 to 100	88 to 108
MSM10S03XX	12K	160	68, 84	80 to 144	88 to 132
MSM10S05XX	22K	208		120 to 208	108 to 208
MSM10S09XX	36K	272		144 to 272*	108 to 256
MSM10S11XX	47K	304		144 to 304*	132 to 301
MSM10S18XX	72K	384		144 to 304*	208 to 340
MSM10S23XX	92K	424		144 to 304*	240 to 340

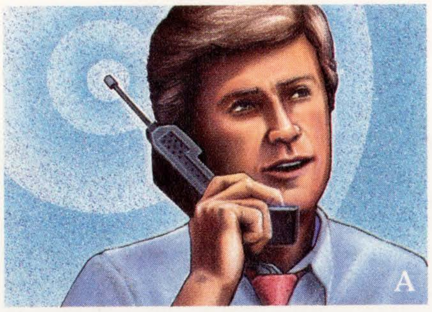
[1]Other products are under development
[2]Up to 100% utilization increase with 3-layer metal, memory, and other regular blocks
*JEDEC metric packages

OKI
Semiconductor

785 North Mary Avenue
Sunnyvale, CA 94086-2909
Telephone 1-800-654-6994

Verilog is a registered trademark of Cadence Design Systems, Inc.
Explorer Rene is a trademark of Mentor Graphics Corporation.

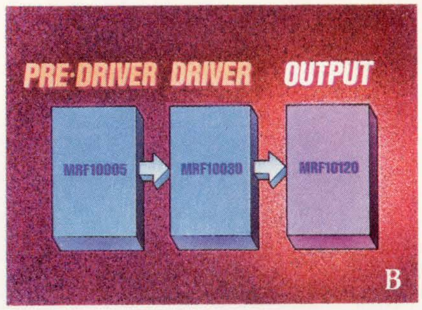
Motorola Discrete



High gain power modules for mobile cellular radios.

From the industry leader in power modules comes a new high gain improvement. The industry standard, the MHW806A, now comes in a 0-dBm version as the MHW807 Series. Instead of the previous power requirement of 30 mW, the new series requires only 1 mW to obtain 6W of output power, thanks to two new gain stages.

The MHW807 Series is perfect for all cellular radio applications. They offer controllable, stable performance over more than the 35 dB range in Po that's needed. Two different frequency models are available: 820 to 850 MHz and 870 to 905 MHz.



Long pulse microwave power transistor.

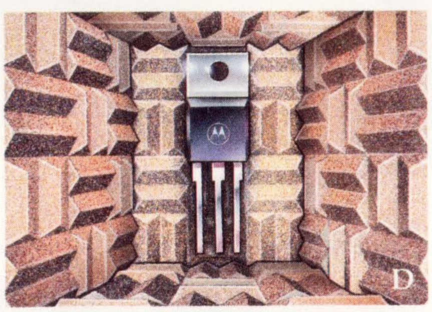
Motorola continues to expand its long pulse microwave power transistor portfolio with the introduction of its new 120 watt L-Band transistor, the MRF10120. This output device completes the lineup consisting of the pre-driver MRF10005 and the MRF10030 driver.

The MRF10120 operates on a power supply of 36 volts and delivers 120 watts of peak power for typically less than 15 watts of peak RF input power. It's designed for common base amplifier applications such as JTIDS (military) and Mode S (commercial) transmitters. The frequency of operation extends from 960 to 1215 MHz.

Satellite microwave power transistors.

Three new microwave power transistors are available for large-signal output and driver amplifier stages for satellite up/down links. The MRA1600-2, MRA1600-13 and MRA1600-30 are designed for Class C, common base amplifiers that operate in the 1600-1660 MHz frequency range. They provide 2.2, 12.7 and 30 watts of minimum power respectively.

These devices offer the highest in reliability and performance. They feature gold metalization, diffused ballast resistors and internal compensation for impedance matching control. All this is offered in a low-cost microwave package for cost efficiency.

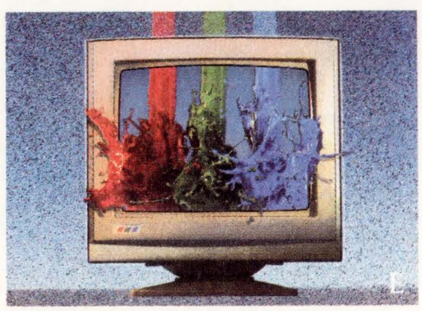


Special TRIACS offer high noise immunity.

The MAC219 series of TRIACS is designed specifically for applications in industrial areas where high noise immunity is required. These TRIACS have voltage ratings from 200 to 800 volts and current ratings of 8, 12, 15 and 20 amps.

All of the devices in the MAC219 series have a noise immunity of 500 volt/microsecond minimum value. This critical rate of rise of off-state voltage is five times that of standard devices with equivalent specifications.

They're perfect for exceptionally demanding applications in AC power control where noise immunity is essential to successful operation of the TRIAC. Use them in appliance controls, industrial controls and AC power circuits involving motors and other inductive loads.



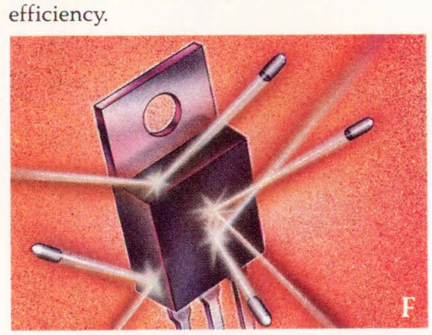
Make a splash in high resolution CRTs.

The SCANSWITCH™ family of semiconductors offer simple answers to horizontal deflection and video amplification problems in high resolution and ultra high resolution CRT applications. The SCANSWITCH family consists of application specific horizontal output transistors, damper diodes and video amplifiers.

Single-chip control ICs are also available for personal computer monitors to reduce design complexity and overall system cost.

All the devices are designed to improve performance in monochrome and color CRT monitors with horizontal scan frequencies of 50 kHz or greater. They offer reduced power dissipation and the ability to work over a wide range of frequencies.

For horizontal output, video amplifiers and multimode horizontal, vertical and video processors, the SCANSWITCH family of semiconductors is the answer.



New high-voltage EFETs.

There's some new additions to Motorola's advanced line of Bulletproof™ EFETs. The new devices have gate voltage ratings of 40 volts and have avalanche energy capability specified. These two characteristics make them essentially indestructible from transients on the gate or drain when used within their specified ratings.

These high voltage EFETs offer breakdown ratings from 400 volts to 1000 volts in the industry's standard TO-218 and TO-200 plastic package. They allow the design of line operated circuits such as motor controls, power supplies and lamp ballasts and other high voltage circuits with a higher degree of reliability.

Many other EFETs are available with smaller size die housed in both metal and plastic packages, including isolated Full Paks.™

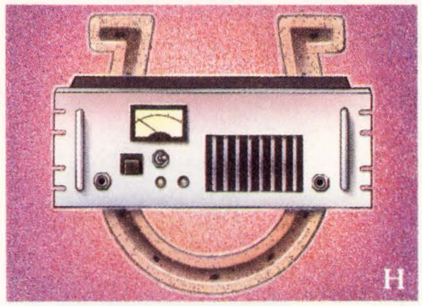
Design News

Low pressure transducer for critical applications.

This new low pressure, temperature compensated, fully calibrated sensor provides a very accurate and very linear voltage output directly proportional to pressure differentials. Its accurate range is from 0 to 1.5 PSI.

The MPX2010D pressure sensor is calibrated for a full-scale span of 25 mV, with a linearity error of less than 1.0 percent, due to laser trimming of critical on-chip components. Even with temperature variations from 0 to 85°C, typical span error is only ±1.0 percent.

A variety of package options make it perfect for applications in automotive, industrial, medical, and many more.

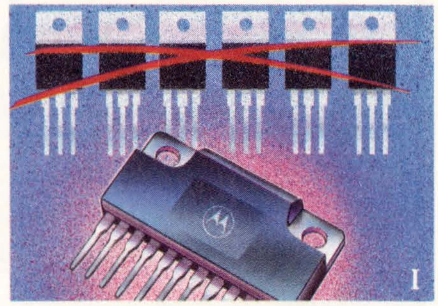


A new breed of workhorse.

Now you can have the same rugged workhorse you've enjoyed for your high-power applications in a medium-power, broadband amplifier. The PAA series of broadband amplifiers are bred to outwork and outlast the competition.

They're ruggedly built with the same power components as our high-power PAA Series including MIL-STD capacitors and resistors, gold-plated connectors, MIL-SPEC plating and painting, EMI/RFI input filter, heavy-duty machined housings with stainless steel hardware, and teflon-coated wire.

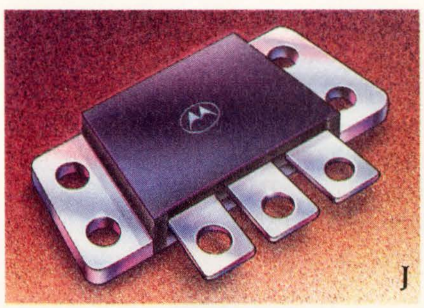
For high-reliability performance you can depend on in a medium-power amplifier, Motorola's PAA Series is the answer.



ICePAK™ TMOS Power Modules for brushless motor control.

Just one ICePAK™ power module replaces 6 power MOSFETS in brushless motor applications. Motorola's MPM3003 power module can handle high surge of up to 25 amps at motor startup. It's a complete three-phase bridge with three N-channel MOSFETS in the lower legs and P-channel MOSFETS in the three upper legs.

This power module is rated at 60 volts to 100 volts at 8 to 10 amps. It offers high dissipation capability and a mechanically rugged, isolated, space-saving package.



Switchmode power rectifier with dual Schottky barrier.

These new high current, dual Schottky rectifiers are available in an electrically-isolated low profile package. Less hardware and tooling is required for mounting than with conventional stud-mounted rectifiers. Both reverse avalanche energy and dv/dt are specified.

Their low inductive package is of obvious advantage in high frequency switching applications. And the platinum barrier metal technology creates optimum forward voltage drop and low reverse leakage current.

The MBR16035CT, MBR16055CT and MBR16050CT Schottky barrier rectifiers are rated at 160 amps continuous, with a non-repetitive peak surge current of 1200 amps. V_{rrm} is rated at 35, 45 and 50 volts minimum respectively.

They're here. High volume, small-footed Optoisolators.

There's a new, reliable, UL-recognized optoisolator for designers who need the time and space savings of opto coupling in small outline, surface mount packages—the MOC200 Series.

Motorola supplies all MOC200 devices in the industry-standard SOIC-8, eight pin packages. And, they're available in tape-and-reel option, conforming to EIA standard RS481A. These devices offer a variety of output configurations:

- 30 & 70 volt transistors @ IF=10mA
- 30 volt transistors @ IF=1mA
- PhotoDarlington detectors

Each of the 12 small-footprint types in the series is packaged with a stable, long-life infrared emitting diode, and features high input-output isolation of 2500 vac(rms), minimum.

Get more information.

To get more information on any of the Motorola products shown here, contact your local Motorola sales office, complete and return the coupon below to Motorola Semiconductor Products, Literature Distribution Center, P.O. Box 20912, Phoenix, AZ 85036. Or call toll-free any weekday, 8:00 a.m. to 4:30 p.m. (MST) 1-800-521-6274.

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Please send me more information on:

A ☐ MHW807 Power Modules	G ☐ Low Pressure Transducers
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D ☐ TRIACS	J ☐ Switchmode Power Rectifiers
E ☐ SCANSWITCH™	
F ☐ High-Voltage EFETs	K ☐ Surface-Mount Optoisolators

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CALENDAR

Surface Mount Manufacturing (short course), Bethlehem, PA. National Training Center for Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethlehem, PA 18017. (215) 861-5486. FAX (215) 861-5060. August 6 to 8.

SIGGRAPH '90: 17th International Conference on Computer Graphics and Interactive Techniques, Dallas, TX. SIGGRAPH '90, Conference Management, 111 E Wacker Dr, Suite 600, Chicago, IL 60601. (312) 644-6610. FAX (312) 938-1232. August 6 to 10.

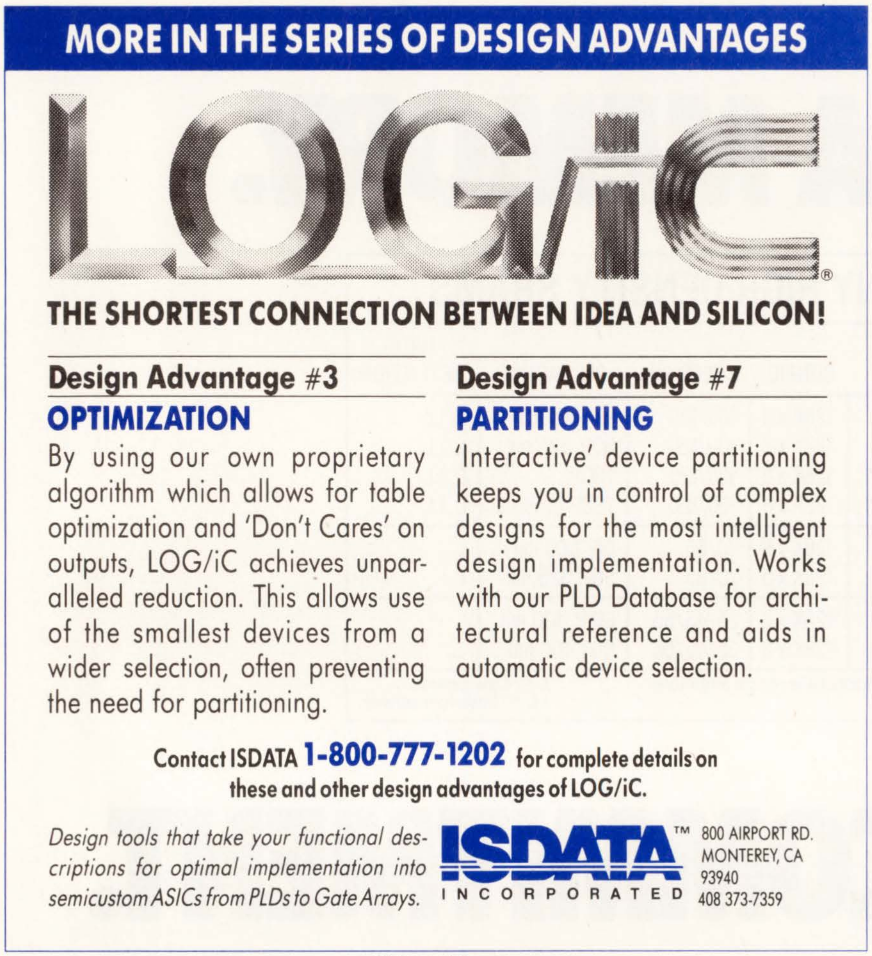
Upgrading, Troubleshooting, and Maintaining your NetWare LAN (seminar), Newport Beach, CA. Center for Advanced Professional Development, 1820 E Garry St, Suite 110, Santa Ana, CA 92705. (714) 261-0240. August 9 to 10.

Controlling the SMT Process (short course), Bethlehem, PA. National Training Center for Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethlehem, PA 18017. (215) 861-5486. FAX (215) 861-5060. August 13 to 15.

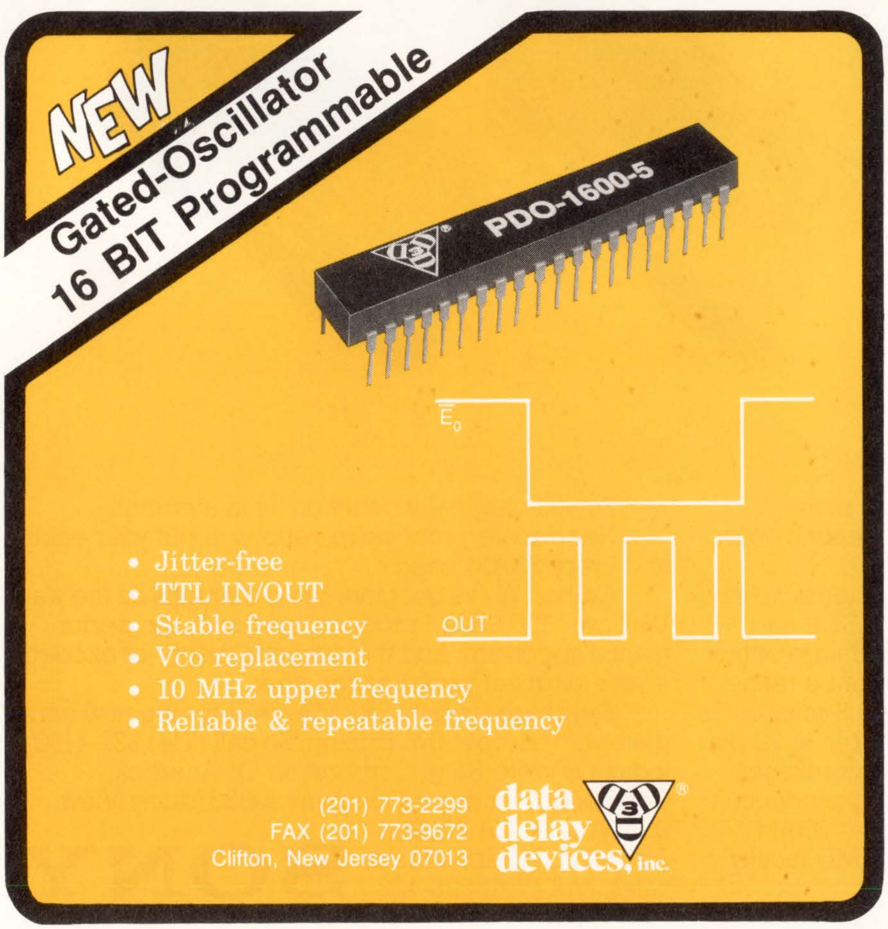
Transient Voltage: Risk, Principles, and Solutions (seminar), Tampa, FL. GSI Educational Services, 2001 W 10th Pl, Tempe, AZ 85281. (800) 776-8358. August 14.

Software Quality Assurance and Testing (short course), San Diego, CA. Learning Tree International, 6053 W Century Blvd, Los Angeles, CA 90045. (800) 421-8166; in CA, (213) 417-8888. FAX (213) 410-2952. August 14 to 17.

High Volume Electronic Printing: User Needs and Vendor Solutions (conference), Boston, MA. BIS CAP International, Research Publications and Conferences Div, Box



CIRCLE NO. 4



CIRCLE NO. 5

CALENDAR

68, Newtonville, MA 02160. (617) 893-9130. FAX (617) 894-5093. August 15 to 17.

Image Processing on PCs (seminar), Marlboro, MA. Data Translation, 100 Locke Dr, Marlboro, MA 01752. (508) 481-3700. FAX (508) 481-8620. August 16 to 17.

SMT Workmanship Standards, Inspection, Rework and Repair (short course), Bethlehem, PA. National Training Center for Microelectronics, Northampton Community College, 3835 Green Pond Rd, Bethlehem, PA 18017. (215) 861-5486. FAX (215) 861-5060. August 16 to 17.

ICEC-IEEE Holm Conference on Electrical Contacts, Montreal, Quebec, Canada. IEEE Holm Conference Registrar, Box 1331, Piscataway, NJ 08855. (201) 562-3863. August 20 to 24.

1990 IEEE International Symposium on Electromagnetic Compatibility, Washington, DC. IEEE 1990 EMC Symposium, Box 19342, Washington, DC 20036. (703) 521-6336. August 21 to 23.

Surface Mount '90, Boston, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. August 28 to 30.

Adaptive Signal Processing (short course), Garmisch Partenkirchen, West Germany. CEI-Europe/Elsevier, Box 910, S-61201 Finspong, Sweden. +46(0)122-17570. FAX +46(0)122-14347. September 3 to 7.

Second International Connection Congress, Tarpon Springs, FL. Worldwide Convention Management Co, Box 159, Libertyville, IL 60048. (708) 362-8711. FAX (708) 362-3484. September 5 to 7.

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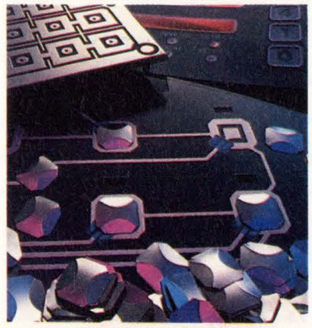

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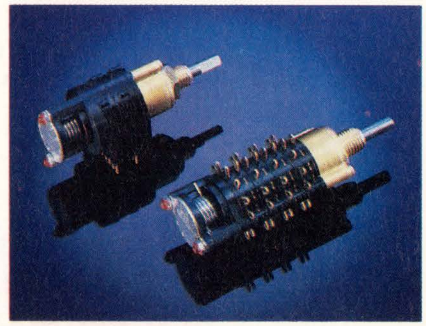

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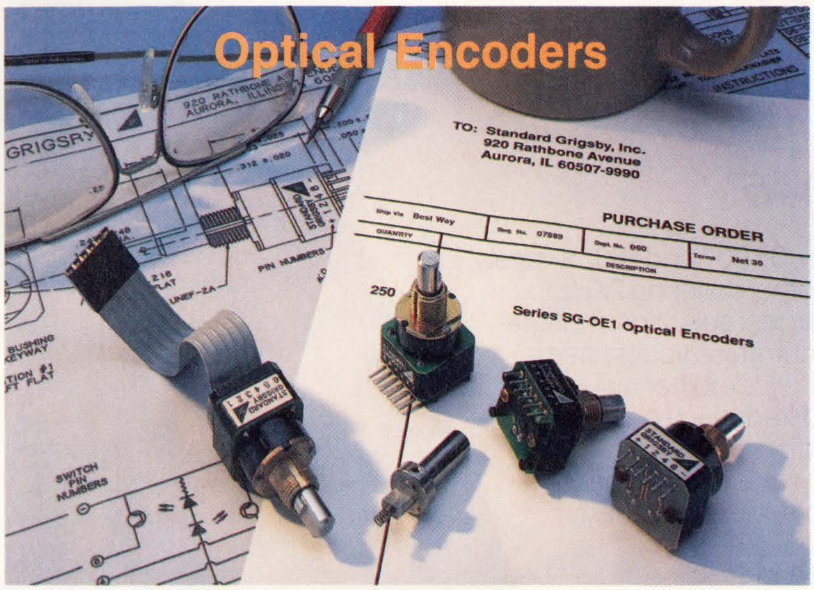

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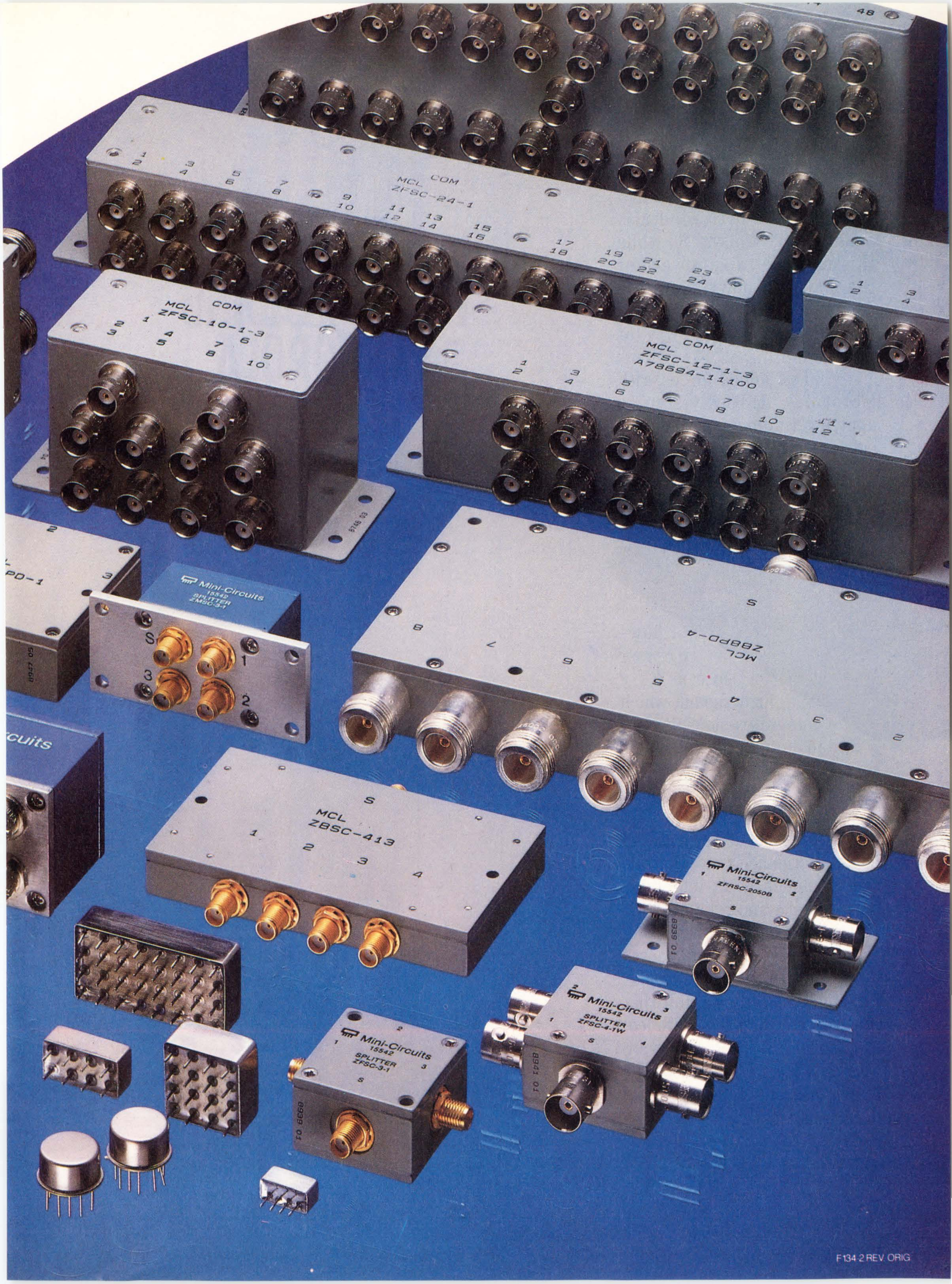

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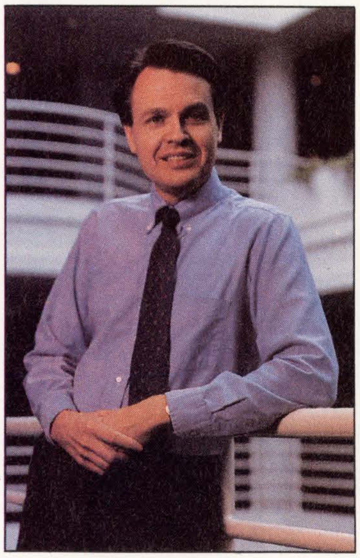
EDITORIAL

The "truth" about Eastern Europe



Kevin Bryan

Facts don't always tell the truth. Just consider this popular image of Eastern Europe: The cities are drab and joyless. Nothing works. Incentive has been destroyed by 45 years of socialism. Technology, what there is of it, is terribly outdated.

This image is basically true, but somewhat distorted. I know; I've been to Eastern Europe twice recently, to Poland and to Hungary. My first surprise was that the cities are not all that drab. Warsaw has many beautiful parks, and Budapest has the majestic Danube. Both cities are alive with activity. And most things do work reasonably well. Even the phone systems, with all their well known shortcomings, aren't as terrible as you may have heard or read.

But mostly, I was surprised by the spirit of the people, especially engineers, in Eastern Europe. Socialism has not destroyed incentive. Most people in Hungary work 60 or 70 hours a week; many have built their own homes and small vacation cottages. In both Poland and Hungary, plenty of engineers seek out challenging, creative work for the sheer joy of it. (See page 52 for a report on electronics in Poland. Our next issue features a report on electronics in Hungary, and future issues will concentrate on electronics in other countries.)

Technology in Eastern Europe certainly does lag technology elsewhere, but not by as much as you might think. In Poland, for example, IC design and production trail the state of the art by 10 years or so, but the use of ICs in design is much more up to date. Eastern European countries have well educated work forces, too. In Poland, 98% of the population is literate. In both Poland and Hungary, engineering education stresses a solid grounding in the sciences and lots of hands-on lab experience. Eastern European engineers are actively recruited for high-tech jobs in Western Europe and elsewhere.

Still, the image of Eastern Europe as a sluggish technological backwater lingers on. This image is not without foundation, but it's misleading because it doesn't show the whole picture. To see only the risks of doing business in Eastern Europe—of which there are many, admittedly—is a mistake. A better approach is to carefully consider those risks while looking at the possibilities: a well-educated work force, technical talent, and potentially lucrative markets.

Gary Legg

Gary Legg
Special Projects Editor

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ELECTRONICS IN POLAND

Learning to cope with capitalism

The celebrations of democracy are over. The bright Solidarity banners no longer fly above cheering crowds. A year after its populace swept aside a lumbering old Communist regime, Poland still faces the difficult job of installing a workable system in Communism's place. It is not an easy task. It is an especially daunting task for the country's outdated electronics industry.

Accustomed to central planning, government subsidies, and guaranteed Eastern Bloc markets for most of its products, Poland's electronics industry hasn't yet learned to think for itself, let alone do for itself.

TEXT AND PHOTOGRAPHS BY GARY LEGG, SPECIAL PROJECTS EDITOR

ELECTRONICS IN POLAND

This telecommunications agency building reflects the grim status of Poland's telecommunications system.

When Poland moved from a controlled economy to capitalism in the space of one day—January 1 of this year—the consequences for electronics were enormous.

Suddenly, by government decree, the subsidies were gone. Monopolies were abolished; markets were no longer guaranteed. Managers accustomed to receiving orders from bureaucrats were suddenly responsible for making decisions themselves. All of a sudden the cold reality of capitalism was at hand: Be profitable or perish. Languishing on the trailing edge of technology, electronics in Poland now has no choice but to become competitive.

Almost without exception, plans to restructure Poland's electronics industry involve joint ventures with foreign firms. Industry managers know that much of their technology is not competitive globally, and they hope to improve it through cooperative arrangements. They also realize that impoverished Poland must get its working capital from abroad. Anatol Zmijewski-Szmit, sales manager for Unitra Commercial and Industrial Company, puts it bluntly: "Joint ventures are the future of our country."

What Poland has to offer in return for technology and capital is a well-educated work force accustomed to low wages. The average Polish worker earns about $75 a month, and the average engineer earns only a little more. Many managers in Polish electronics companies suggest that their industry can do in the 1990s what Taiwan's did in the 1970s and 1980s: start by providing manufacturing services, gradually acquire competitive technology, and finally move into independent design and development.

Barriers stand in this road to progress, however. One is the lack of a solid commercial infrastructure. Commercial banking, for example, is almost nonexistent in Poland, and without a banking system, foreign investments are slow in coming. Telecommunications is also a problem. Poland's outmoded and inadequate phone system makes even an ordinary business call a questionable proposition.

The Polish economy is another obstacle: Inflation last year was between 700 and 900%. Although the annual rate had dropped to 48% by April of this year and has continually declined since, inflation is still a problem to contend with. The Solidarity-led government hopes for a "normal" rate of approximately 10% by year's end.

For Polish workers, the shift to market economics brings another problem—unemployment. Practically nonexistent under socialism, unemployment is now increasing rapidly as companies trim their staffs or even go out of business. Harvard economics professor Jeffrey Sachs, who advises the Polish government, predicts that between five and ten percent of the work force will be jobless by the end of the year. That would mean between one and two million people out of work in a society that has never really had to cope with unemployment.

A positive—if harsh—effect of unemployment is that Polish workers are motivated like never before to perform well to keep their jobs. Sachs notes that in the first week of "shock therapy" capitalism, worker absenteeism dropped 75%. Soaring prices add to workers' anxiety. Under capitalism, prices of previously subsidized consumer items such as food and energy have floated to their natural levels. In January alone, the price of coal rose 600%. For the few engineers who can afford a car, a tank of gas now costs about a week's salary.

This article is part of an occasional series on electronics engineering in Europe.

Much of the new unemployment in Poland results from trimming deadwood that would never have accumulated in companies under capitalism. Engineer Grzegorz Marzantowicz claims, for example, that of the 1000 employees at the state-run telecommunications company where he works, some 300 are administrators. Deadwood is not unknown in technical departments, either. Tadeusz Jarosinski, an engineer who left Poland for the United States last year, says he was frequently one of two or three Polish engineers doing all the work on a project, while a dozen or so coworkers did little more than sit around and read newspapers.

If socialism provided little incentive for hard work or innovation, Poland's new market system provides incentive with a vengeance. As soon as capitalism became the official policy, enterprising Poles began selling consumer items that simply weren't available before. On Warsaw's busy Marszalkowska Street, vendors now stand elbow-to-elbow selling everything from clothing to tropical fruit to electronic equipment. Operating right in front of the dreary department stores they compete with, the vendors feature brighter displays, wider selections, and prices that are 10 to 15% lower.

Polish engineers are responding to their country's political and economic changes with a mixture of enthusiasm, optimism, and anxiety. Some now perform engineering work as sidelines to their regular jobs. Others are taking their first look at private companies as possible employers. But many, perhaps most, engineers still fear the uncertainties of a market economy. Their fears are exacerbated by the knowledge that Polish electronics lags state-of-the-art technology by as much as 15 years in some areas. Still, most Polish engineers say they are well trained and capable of narrowing the technology gap with experience. Much of the gap, they say, is a result of technology import restrictions, not lack of knowledge or ability.

Sidewalk shops now abound in Poland. Last year's consumer goods shortages and long lines have been replaced with plentiful supplies and few people who can afford them.

Poland's economy—not its economic system or the state of its technology—is electronics engineers' biggest concern. The big question is whether the country will regain enough economic health to support private industry, especially in the mercurial field of electronics.

On a personal level, engineers wonder if they can continue to make ends meet on $100-a-month salaries while newly freed prices continue to soar. Although they're happy with their country's turn to democracy and proud of its leadership role in Eastern Europe's denunciation of Communism, they're also concerned about their own financial futures. As one Polish engineer says, "We are living in such an interesting time, but it would be so much better to live in such an interesting time with some money."

Making it by moonlighting

Capitalism is nothing new to this Polish couple. His income from a part-time engineering business more than doubles their regular salaries.

On most weeknights, the living-room table in the two-room Warsaw apartment of Grzegorz and Zosia Marzantowicz is covered with the documents of a surprisingly capitalistic activity—private business. Since 1984—long before Communist rule ended and capitalism became Poland's official policy—Grzegorz Marzantowicz has been a private engineering consultant.

The part-time business is a venture that Marzantowicz didn't plan, or even anticipate. In 1981, after earning a master's degree in electronics at the Technical University of Warsaw, he began a career as a telecommunications engineer for a government-owned agency. There, he found that ability and hard work did not bring advancement. "You could only advance with age," he says, "not your knowledge."

The situation led to what Marzantowicz calls a "war" between the older and younger engineers. "The younger designers worked much faster," he says. "I could do a project in a week that other designers would need a month for, and in my free time I would look for more work." Marzantowicz's boss was only too glad to provide the extra work, but his hands were tied when it came to providing more money. Even now, with nine years of engineering experience, Marzantowicz earns only 1.2 million zlotys a month—about $125—from his regular job with the telecommunications agency.

So when one of the agency's customers offered him some work on the side, he accepted. Although he had some misgivings about circumventing his full-time employer, "In Poland, I must if I want to make money." Now, six years later, Marzantowicz's income from part-time projects is roughly twice that from his regular job. To earn it, though, he says, "I am working 25 hours in 24."

Long hours are not the only price Marzantowicz pays. Because private customers need to contact him during business hours and he's not yet ready to give up his regular job, Marzantowicz has had to cut his agency supervisor in on the action. "I have to pay my boss money," he says, "and he sleeps on the job." But, by funneling some of his private work through the agency, Marzantowicz makes his supervisor look far more productive than he really is, thus solidifying the supervisor's—and his own—position. Marzantowicz pockets only 20% of the fees for the shared jobs, but there are plenty of other jobs that his boss never finds out about.

Most of those jobs involve designing office-building installations such as burglar alarms, access-control systems, telephone networks, paging systems, and closed-circuit TV. Marzantowicz has arrangements with ten companies that contract for such installations. He usually gets 60% of the contract fee, and the contractor keeps 40% for administration.

The work is relatively low tech. "My projects use very simple techniques," Marzantowicz says. "Mostly, I use a typewriter and a

pen. I also have a small personal computer, an Atari 800 with a disk drive and a printer. I would like to buy a plotter, but it's too expensive."

The greatest difficulties with Marzantowicz's consulting work result from shortages of time and work space. He often works far into the night, sometimes taking short naps on the living-room sofa. He usually spends Saturdays at installation sites. "Sunday," he says, "belongs to God." Every two months, he spends a week in Vienna undergoing training at one of the companies he consults for.

The living-room table where Marzantowicz works also serves as the family dining table, so he can't leave his work spread out for long. Nor is there any other work space; the apartment's two rooms are home not only for himself and his wife, but also for their four-year-old son, Mateusz, and Marzantowicz's mother. In fact, Marzantowicz's parents lived there when he was born; it's the only home he's ever known.

Marzantowicz and his wife would like more space, but with Warsaw apartments selling for $10,000 to $20,000, they're not likely to get it anytime soon. Nevertheless, Poland's turn toward capitalism after 45 years of Communism has started people dreaming—not just of increasing their meager incomes as Marzantowicz has, but also of possessing some modest material objects. For now, the grim economic situation makes many of these goals unrealizable, but still the dreams persist. "My dream," says Marzantowicz, "is to buy a flat with an extra room where I can have a computer and work."

Making it in tough times

After a long struggle for success under socialism, a 44-year-old engineer ponders an uncertain future in Poland's new market-based economy.

Life has not been easy for Anatol Zmijewski - Szmit. Since his birth in Siberia in 1945, he has faced one challenge after another.

Zmijewski provides few details of his beginnings. He says only that his mother was Polish, his father half German and half Russian, and that if you've read Aleksandr Solzhenitsyn's *Gulag Archipelago*, "then you understand." When he was three, he and his mother made their way to her native Warsaw, which had been almost completely reduced to rubble in the war. He avoids mentioning his father, except to say that he remained in the Soviet Union.

At the age of 19, Zmijewski went to work in a Warsaw electronics factory, where he quickly encountered socialism's dark side. He was working too hard, an older worker told him menacingly, and making everyone else look lazy. If he didn't slow down, he would receive a beating.

Zmijewski went on to earn a master's degree in electrical engineering at the Technical University of Warsaw in 1969. He became a teaching assistant, but quit after a year because the pay was so low. After another academic job that lasted two years, he became a design engineer for Unitra Unima, a manufacturer of electronic test and production equipment.

Designing test equipment such as multimeters and signal generators gave Zmijewski the greatest fulfillment of his professional life, but the satisfaction lasted only four years. When a new manager at the company wanted his own hand-picked design team in place, he used a combination of firings and harassment to remove anyone in his way. Zmijewski was in his way.

Next, Zmijewski parlayed his facility in languages, particularly Russian, into a job with Unitra Unima's parent company, Unitra. The giant state-owned foreign trading company dealt solely in electronics and almost exclusively in the sphere of the Soviet Union. Zmijewski quickly acquired knowledge of importing and exporting to add to his electronics expertise, and from 1982 through 1986, he and his family—wife, son, and mother—lived in Moscow.

Since returning to Poland, Zmijewski has traveled and conducted business in virtually every country that is, or was, Communist. As an international sales manager with 15 people reporting to him, his career appeared set.

But last year's political upheaval and this year's economic transformation have pushed Poland—and Unitra and Zmijewski—into a state of uncertainty. Under Poland's Solidarity-led government, Unitra no longer enjoys the monopoly on foreign electronics trade that it held for so long. Small companies, much leaner than Unitra, now compete for business. In addition, many companies, such as Unitra, that previously received government subsidies lost all such preferential treatment when Poland implemented a shock-therapy switch to a market-based economy. Now, Unitra must either be profitable or perish.

Unitra's loss of favored status has changed Zmijewski's job. Previously involved only with electronics, Unitra now scrambles to maintain profitability by dealing in everything from butter and potatoes to dresses. "I know electronics," says Zmijewski. "I can sell electronic products. But now I have to learn about everything else." The situation is further complicated by the fact that many of Unitra's new clients are companies much smaller than the old ones. Zmijewski has to maintain many more contacts and participate in many more negotiations just to keep sales figures level.

The new political and business environment creates opportunities as well as difficulties, but the changes in Poland make new undertakings risky. Changing jobs in a country where many of the companies that exist are new and unproven and the economy is in shambles is a crap shoot. Few job openings are available anyway. And starting your own company requires capital, which is practically nonexistent.

Friends and associates encourage Zmijewski to become an international marketing consultant, applying his knowledge of electronics, trade, and Polish manufacturing and consumption. Thus far, he has been reluctant. He figures he would need six months of operating expenses just to get started, and even that much money is hard to come by. Worse, the money could easily be lost.

So, Zmijewski works harder and harder and hopes for the best. Unitra is all right for now, he says, so he has some time for things to work out. But just in case, he's taking an advanced course in economics to learn more about marketing, banking, and foreign trade. The extra knowledge, he figures, will help him meet this latest challenge.

"If I had thought that in two or three years the situation in Poland would improve so that I could carry out my projects, my dreams, then I would have stayed, but it obviously wasn't true. I realized I have only one life, and if I lose my best ten years or my energy or my enthusiasm, I will never get them back."

Those are the words of Tadeusz (Tad) Jarosinski, a 32-year-old electronics engineer who left Poland last year to pursue high-tech goals in America. Solidarity-backed candidates had just dominated Poland's first free elections in four decades, but Jarosinski thought the climate for electronics would not be healthy for a long time, maybe ten years or more. He left Warsaw not knowing when he would next see his wife, his three-year-old daughter, and his four-month-old son. He came to the United States without a job and without much money. His English, while passable, still left a lot to be desired.

Making it in America

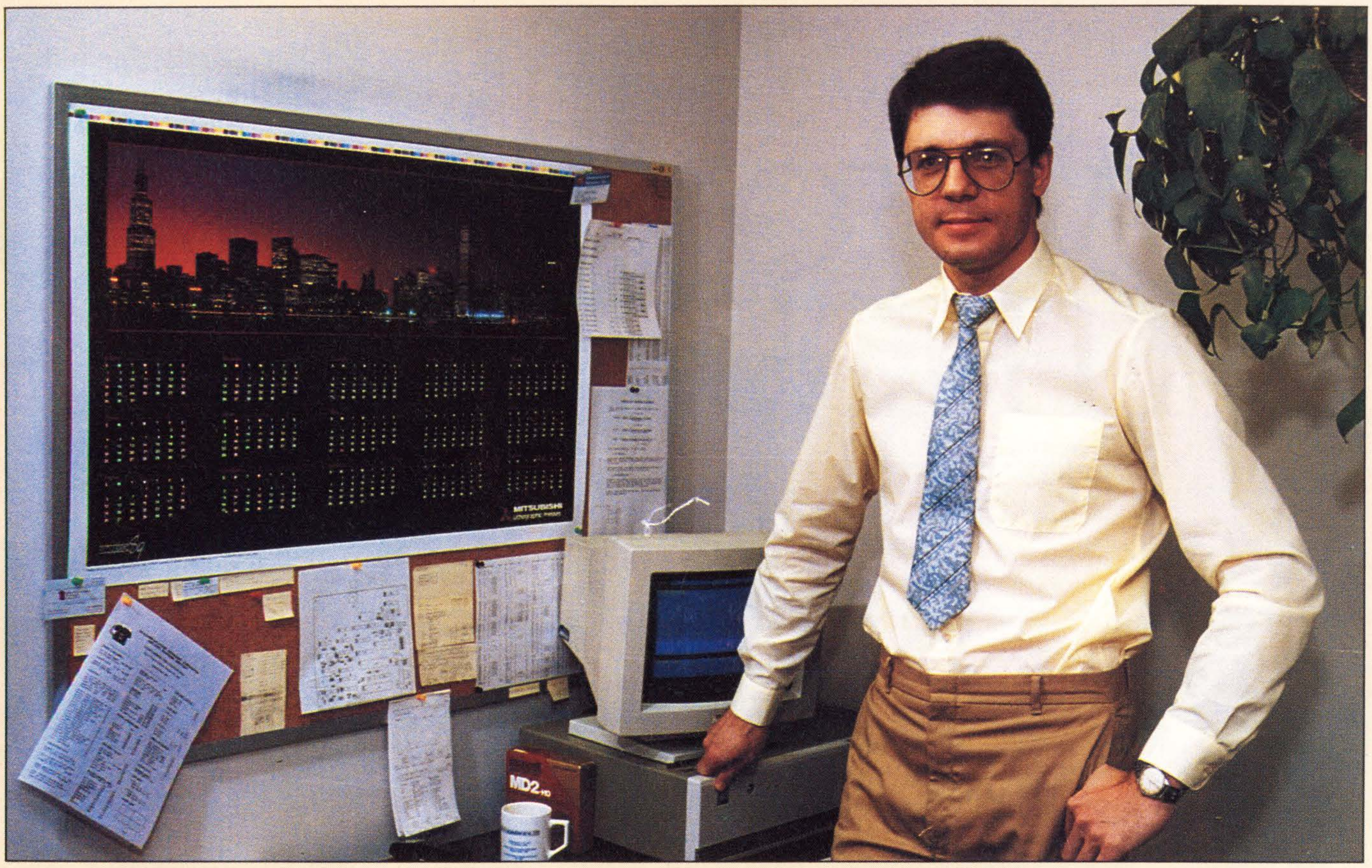
Frustrated by limited opportunities, this Polish engineer looked abroad. Now he's working in Maryland.

But what Jarosinski did have when he arrived in America—on the Fourth of July—was an impressive resume and a burning desire to do creative engineering. He started mailing out his resume and soon had plenty of interviews, although few companies were willing to tackle the paperwork necessary to get him a US work permit. He had a job in Chicago within three or four months, although he soon left it for a better opportunity. He now works as a combination hardware and software engineer for Telecommunications Techniques Corp (TCC) in Germantown, Maryland.

Before he left Poland, Jarosinski had chalked up eight years of electronics experience with one state-owned company and two private ones. He had designed hardware and software for everything from the 8048 microcontroller to the 80286 microprocessor. The work had been frustrating, however, because few designs ever went into production. "The whole infrastructure [in Poland] is so complicated," he says, "that to actually complete an ambitious project is very, very difficult. You can't rely on other contractors. Even if projects are properly done by the hardware and software engineers, they're not completed because of a lack of screws, a lack of boxes, a lack of ABS material, or something like that."

On his own, however, Jarosinski had taken several projects to completion. He designed and built an EPROM programmer and an 8051 emulator. The projects gave him not only good experience, but also engineering tools that he wouldn't otherwise have been able to own. "I couldn't afford to buy even a simple emulator from Nohau for about $2000," he says. "That's a lot of money in Poland."

Another of Jarosinski's projects was a reverse-engineered computer that was software-compatible with an IBM PC/XT. High component costs forced him to use a noncompatible backplane and, therefore, deviate from the IBM hardware spec. He couldn't afford a hard disk either, so he borrowed floppy-disk drives from the Technical Univer-



sity of Warsaw. He ordered chips from a company in Jamaica, and when the company stopped supplying the Eastern Bloc under pressure from the Reagan administration, he turned to sources in West Berlin. He eventually finished the computer and used it to run Microsoft's C compiler, design programs from Autocad and OrCAD, and various other software packages.

But Jarosinski's regular employment was becoming more frustrating. Working for Plastomed, a West German firm with an office in Warsaw, he thought for a time that he could actually take a project to completion. However, the company had so many problems dealing with Polish internal affairs that "They had to concentrate more on getting screws than developing software." It was the last straw. "I had bet on this company," Jarosinski says. "It was my last chance to do something real in Poland."

Now, after only a year in the US and barely six months at TTC, Jarosinski is gratified that his hardware and software designs for T1 test equipment are actually going into production. He's also happy to have development equipment, such as his Hewlett-Packard 9000 workstation, that he didn't have to build himself.

After a nine-month separation from his wife and children, Jarosinski was able to bring them from Warsaw to rejoin him in April. The family plans to stay in America indefinitely, but the thought of returning to Poland is never completely out of mind.

"I think it can be very profitable for my country," Jarosinski says, "if I can go back after ten years or so and give some knowledge to the next generation of electronics engineers." To have stayed in Poland would have been a mistake, Jarosinski says, because in the current economic climate, he would be unable to accomplish anything of significance. "The Polish economy is very weak," he says. "It doesn't profit from people who stay there and do nothing." EDN

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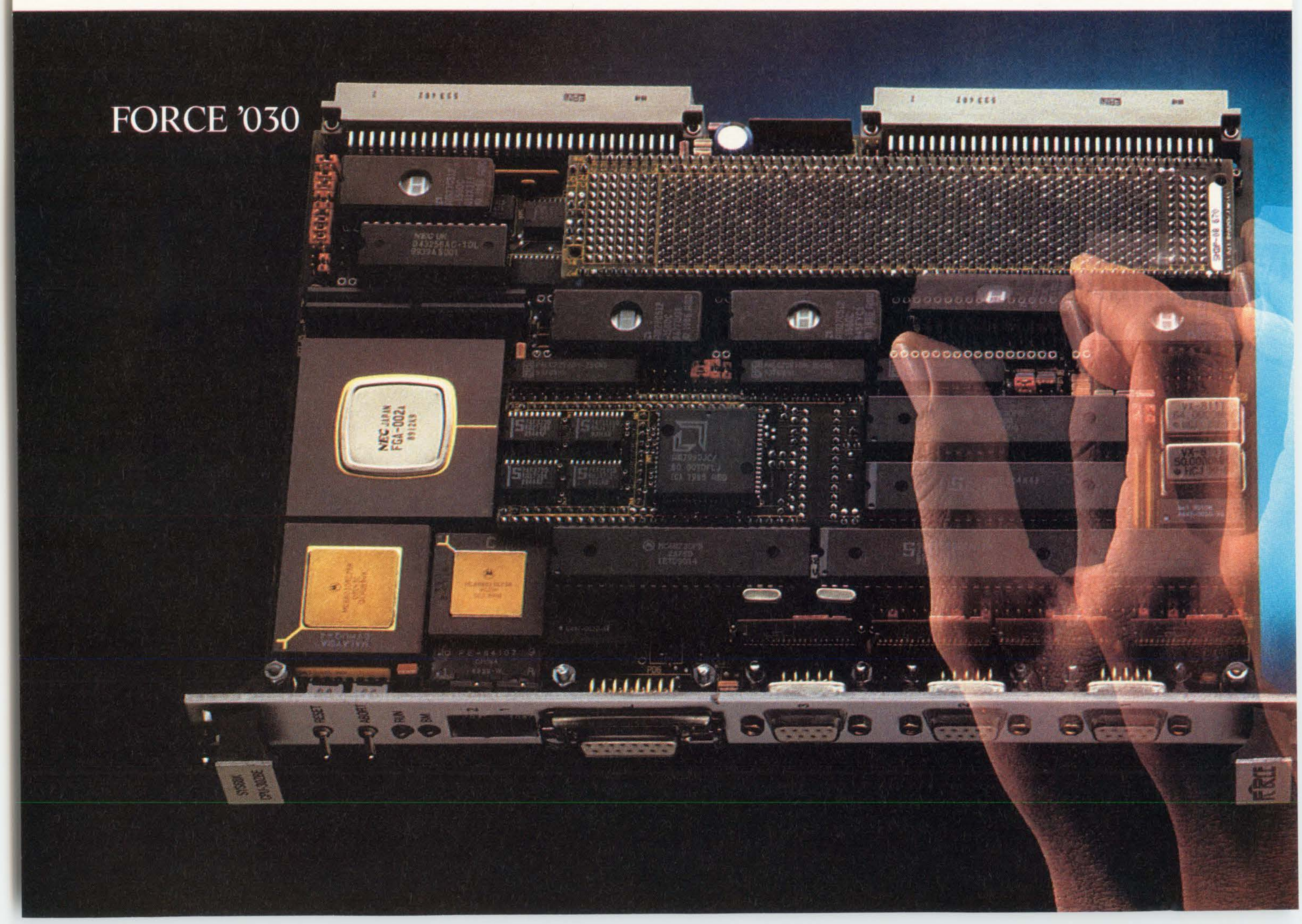

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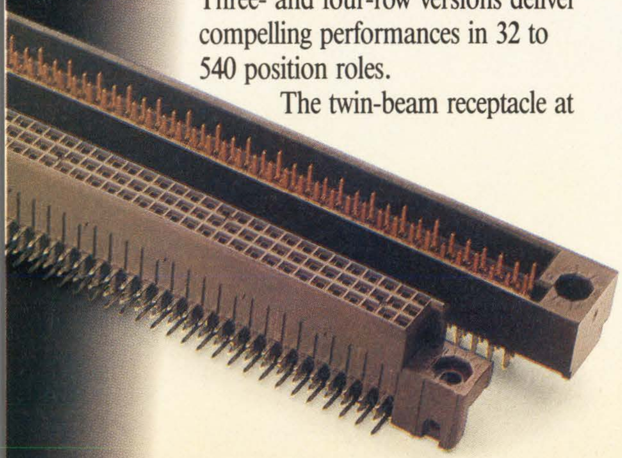

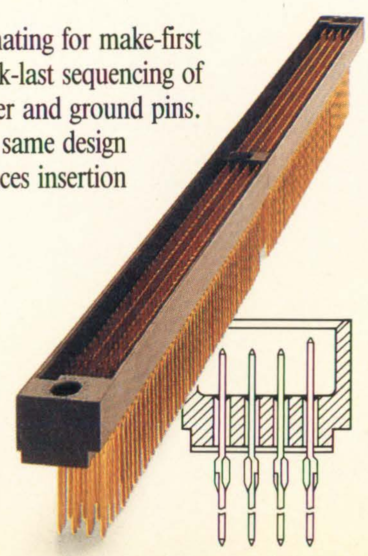

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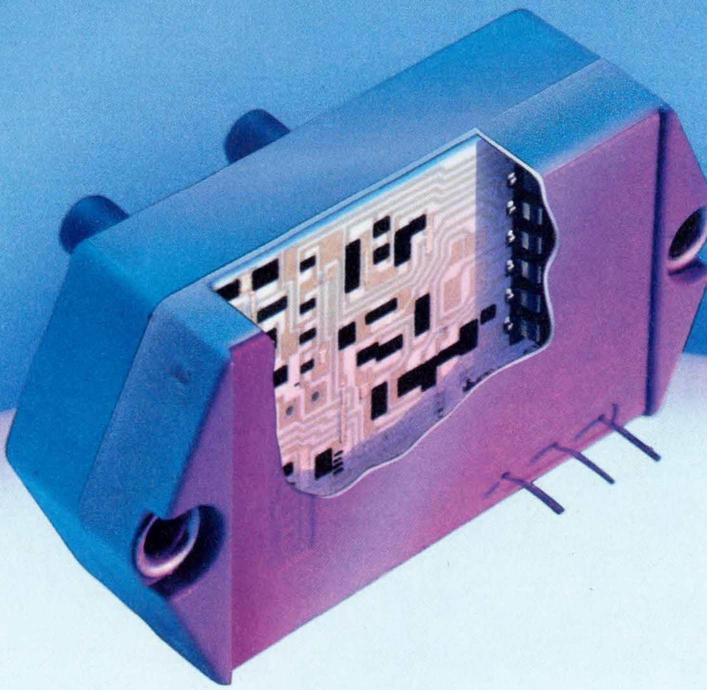

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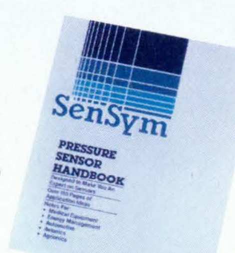

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JTAG BOUNDARY-SCAN TEST

Adding testability also aids debugging

The JTAG boundary-scan technique makes testing pc boards and systems easier. For the knowledgeable designer, the technique also offers benefits during debugging.

Richard A Quinnell,
Regional Editor

As circuits continue to increase in complexity and package density, designing for testability will become more than just a good idea—it will become a requirement. One test technique that helps you debug your design as well as aid production testing is the boundary-scan technique developed by the Joint Test Action Group (JTAG). Soon to be issued as IEEE Standard 1149.1, the technique is now gaining industry support in the form of tools and scannable standard ICs.

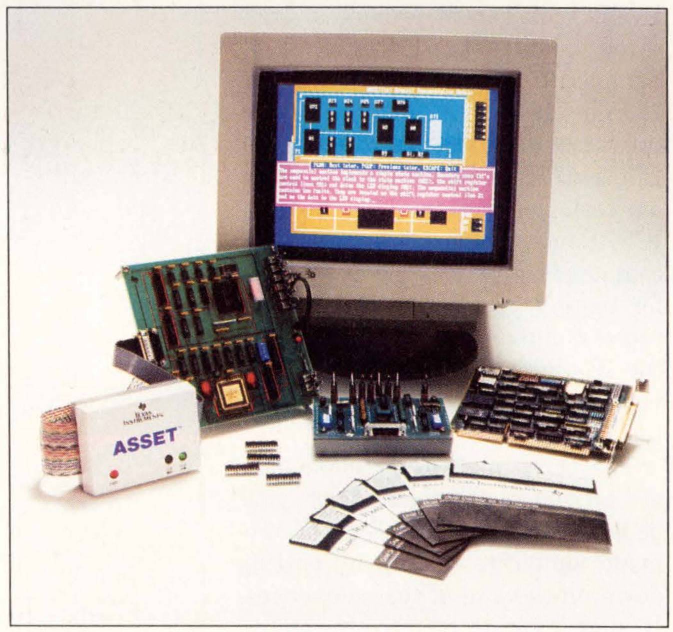
The roots of the JTAG boundary-scan technique lie in the difficulty of testing surface-mount pc boards. The high component density and fine lead sizes of surface-mount components make testing with traditional bed-of-nails probes difficult at best. When components are mounted on both sides of the board, or when circuit traces lie entirely on internal board layers, probing methods become wholly inadequate.

Anticipating that surface-mount pc boards will get even harder to test, the JTAG committee developed a probeless test technique that requires a 4-wire serial test bus. The test bus comprises four signals: Test Data In (TDI); Test Data Out (TDO); Test Mode Select (TMS); and Test Clock (TCK).

TDI and TMS assume a logic-high state if not actively driven, ensuring that the test circuitry always receives a known value on these lines. TDO is a 3-state signal that is active when you are shifting data through the IC. At all other times, it is a high-impedance signal.

The test bus allows you to examine or change the state of all I/O pins on a component, hence the name "boundary scan." By wiring together the TMS and TCK on all ICs and connecting TDO of one IC to TDI on the next, you can test your entire board with a single bus.

Fig 1 gives an overview of the JTAG boundary-scan technique's circuit architecture. All scannable ICs have the three scan registers shown: the instruction register; the bypass register; and



Providing a complete package for testing your boundary-scan design, *the Asset system from Texas Instruments includes a scan-test controller, C++ compiler, software tutorials, and debugging utilities.*

JTAG boundary scan

the boundary-scan register chain. Data passes through these registers under the Test Access Port's (TAP) control, moving from TDI to TDO. The technique gives the IC designer the option of providing additional scannable registers. These extra registers may provide scan paths for testing internal logic, reading a device-specific ID code, or accessing optional built-in test circuits.

The TAP, a state machine that clocks and controls the various registers and multiplexers, is built into every scannable IC. The TMS signal directs the port's state changes, which occur on the rising edge of TCK. Depending on the TAP's state, the test circuits may sit idle or pass data through a register without affecting the IC's normal operation. They may also execute the test command stored in the instruction register. (See **box,** "Controlling your boundary-scan test.")

Standard defines test commands

Any IC claiming compliance with IEEE 1149.1 must provide at least three commands: External Test; Sample/Preload; and Bypass (**Ref 1**). The IC may, at the manufacturer's option, provide a variety of additional commands, such as internal test, self-test, and reading the IC's identity code. The mandatory commands give you the basic tools for testing your pc board. The optional commands allow you to test the ICs individually as well as give you more powerful pc-board-test tools.

The three mandatory commands are all you really need to test your pc board's wiring. The Bypass command simplifies testing by cutting down on the size of test sequences. It allows you to effectively remove an IC from the test loop, routing test data through the 1-stage bypass register. You can then restrict the length of your test sequences to that required by only the ICs you're interested in.

You can best understand the operation of the other two commands by referring to the circuit in **Fig 2**. The Sample/Preload command causes register R1 to capture the state of the IC's I/O line while loading register R2 with the data previously held by R1. The multiplexer M2 allows the system data to pass through, so that your circuit's normal operation is unaffected. You can thus use the Sample/Preload command to take a snapshot of your circuit's normal operation or to prepare register R2 for the next test command.

The External Test command causes the boundary-scan register to behave in one of two ways, depending on the type of signal line the register connects to. A register connected to an IC's output or I/O control line will use R2's output value to replace the IC's normal output signal. A register connected to an IC's input line will capture the line's state on the edge of TCK following the External Test command. The result of this dual function is that you can use a single Ex-

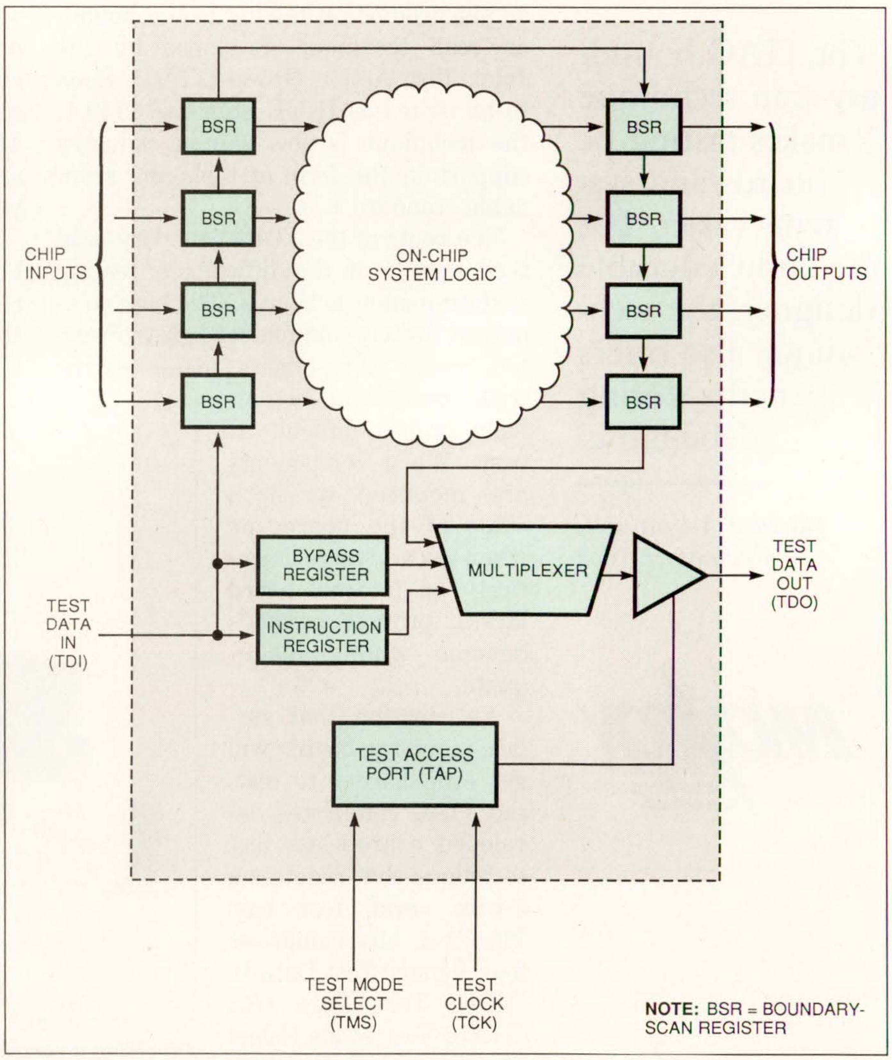


Fig 1—A JTAG boundary-scannable IC *allows you to read and control all of the IC's normal I/O signals with only four additional signals.*

Controlling your boundary-scan test

To control the boundary-scan test circuits, you must manipulate both the Test Data Input (TDI) and Test Mode Select (TMS) lines. You use the TDI line to enter instructions and data into circuits. You use TMS to control the Test Access Port (TAP). A succession of TMS values moves the TAP through its various states **(Fig A.)**

A typical test sequence would begin with the TAP at Test-Logic-Reset. The TAP enters this state at power-up. It will also enter and remain in this state following a sequence of at least five "1s" on TMS.

While in the Test-Logic-Reset state, the TAP allows the IC to operate normally; the test logic is inactive. The TAP also forces the current instruction to the Bypass command or, when implemented, the optional ID Code read command. By forcing the instruction, the TAP ensures that a glitch on TMS has no effect on your circuit. The TAP would return to Test-Logic-Reset within three clocks without executing any instructions.

When the TAP clocks in a "0" on TMS, it moves from the Test-Logic-Reset state to the Run-Test/Idle state. In Run-Test/Idle, the test logic remains inactive, but the TAP no longer forces the instruction's value. You can, therefore, safely park the TAP in this state after loading an instruction that you wish to use repeatedly, such as Sample/Preload.

From the Run-Test/Idle state you can move the TAP to the Select-DR-Scan or the Select-IR-Scan state. Both states have no effect on the test logic; they are simply gateways into their respective scan sequences. One sequence controls the boundary-scan and optional data registers; the other routes serial data through the instruction register. The two sequences are otherwise identical, and the corresponding states have similar effects.

The Capture states transfer data into a serial shift register to be clocked out through TDO. In Capture-DR, the test circuits sample the IC's I/O lines if the current instruction is Sample/Preload. If the current instruction specifies one of the optional test registers, the captured data will be device-specific.

In Capture-IR, the captured data represents the status of the IC. All but the two least significant bits of data are device-specific. That is, the IEEE 1149.1 specification does not restrict their value or meaning. The two least significant bits, however, must be "01." Having this known value to shift through the scan path aids you in debugging your circuit.

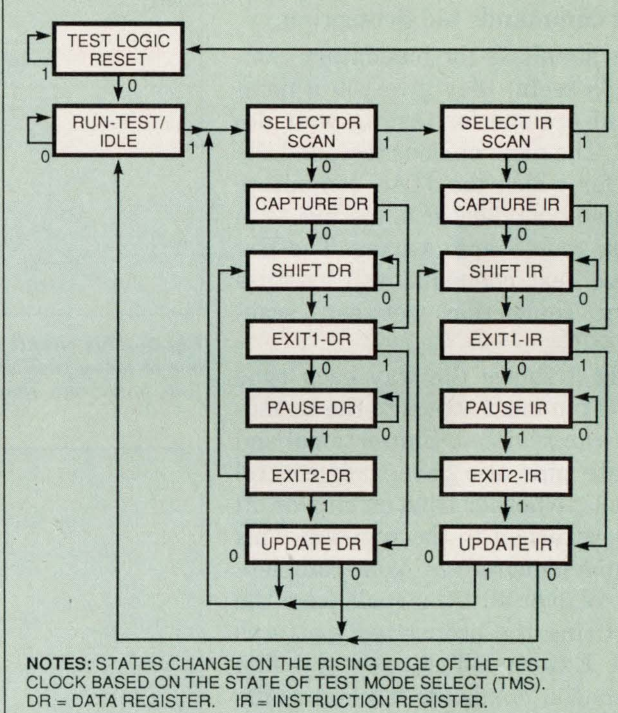


Fig A—The behavior of the JTAG test circuits derives from the Test Access Port's state. *Notice that a sequence of five "1s" will move the port to Test-Logic-Reset from any other state.*

The Shift states allow the Test Clock (TCK) to move data through the IC from TDI to TDO. The data advances one step each rising edge of TCK while TMS is held low. The instruction register determines which path is active during Shift-DR. Shift-IR always uses the instruction register.

The Exit states simply provide gateways to other states. They do not affect the test circuit's operation. The Pause states do have a function, however. They allow you to suspend data shifting, then resume without altering the data. The Pause state is handy when you must wait in the middle of loading a test pattern to retrieve the rest of the pattern.

The Update transfer stores the newly shifted-in data values into the appropriate register. Changing the current instruction and latching test data into the output lines of the boundary-scan register both occur in an Update state.

JTAG boundary scan

ternal Test command to set an IC's output signals, then verify the receipt of those signals at other ICs.

Test commands aid debugging

As simple as the mandatory commands seem, they give you a number of options for testing your design. The most obvious test, and the one for which the JTAG committee created boundary-scan testing, is to check your board's wiring. The External Test command will exercise every connection between scannable ICs.

Fig 3 shows the way each type of I/O pin must attach to the boundary-scan register. Bidirectional and 3-state pins also have their control signals, whether from on chip or off chip, attached to the register. This arrangement gives you complete control over all I/O signals from the IC. Using the proper test patterns with External Test, you can find all shorts, opens, or stuck-at faults on the signal lines.

To test your entire board's wiring, though, all of the ICs on the board must be scannable. Even then, TMS and TCK signals must be testable by external probing.

A corollary to Murphy's Law warns that the built-in test circuits will be the first to fail, and the JTAG boundary-scan circuits are not immune to failure. Only TMS and TCK will need to be probed, however. If they are properly wired, you can check out the remaining circuits by reading the instruction registers of all devices. The two least significant bits of each IC's instruction register must read "01." If the expected pattern doesn't show up when you scan the instruction registers, you need only count bits backward to find out where the fault occurred.

The Sample/Preload command gives you a picture of your entire system at a given moment, rather

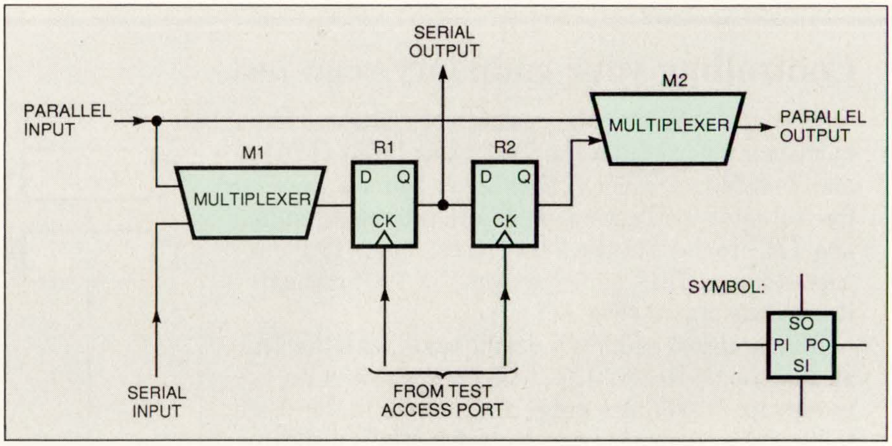


Fig 2—This circuit showing the basic features of a JTAG boundary-scan register cell *is one of many possible implementations. The cell can capture the state of its parallel-input line, provide an alternate output signal, and shift data in and out of adjacent cells.*

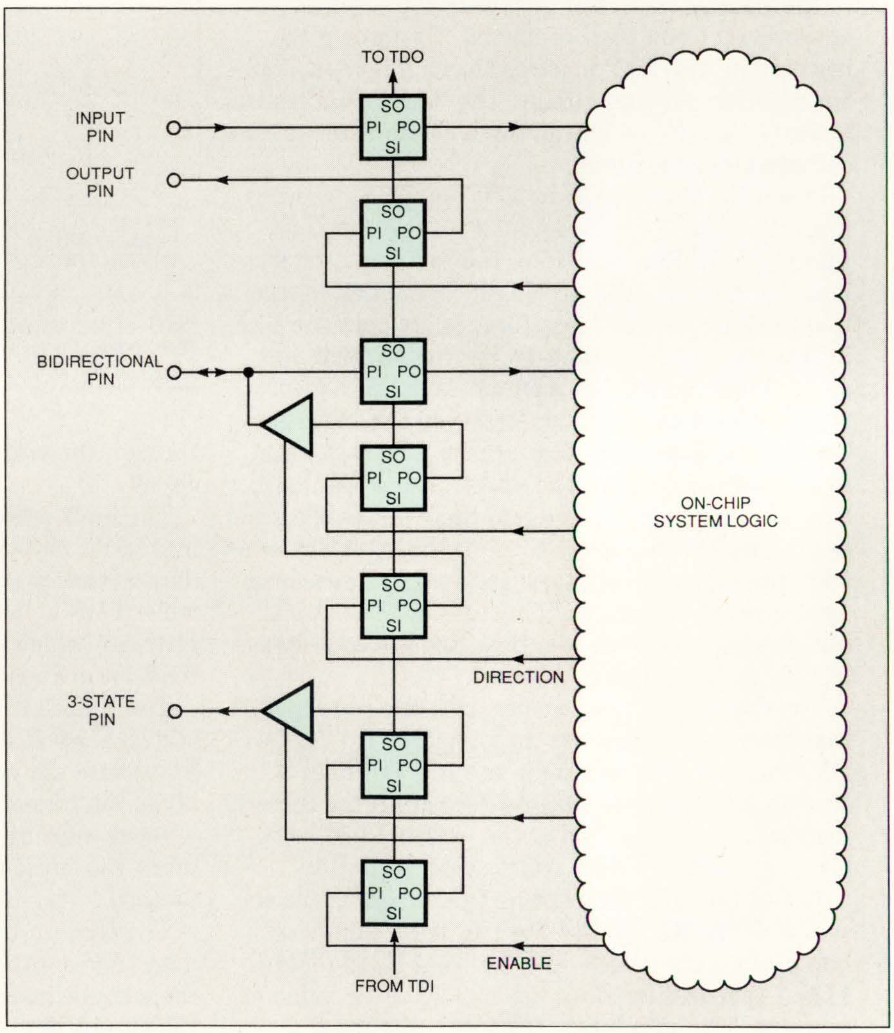


Fig 3—In order to provide complete control over an IC's I/O lines, *the boundary-scan registers must connect to I/O control lines as well as signal lines.*

JTAG boundary scan

like having a many-hundred-bit wide, 1-word-deep logic analyzer. If you can put your system into a repetitive loop, you can then take a succession of such pictures, timed to provide a sequential look at your circuit's operation. Tedious work, it's true, but a lot of capability from a mere four wires.

In large circuits the length of the scan path may become unwieldy. There is, however, nothing restricting you to a single scan path through your circuit. You can just as easily break the test path into multiple paths, running them independently or sharing various signals. **Fig 4** shows several possible scan-path configurations.

Using the Bypass command in conjunction with the External Test command also lets you test your board in sections. You can bypass the ICs that you want to function normally, then use the External Test command to set up and read their boundary conditions. The same scheme allows you to perform functional tests on devices or logic blocks that aren't scannable.

At present, ICs that aren't scannable vastly outnumber the ones that are. Any ASICs you create can certainly be made scannable; many ASIC vendors have JTAG boundary-scan circuits in their libraries. Scannable standard logic, on the other hand, is still fairly rare.

There are some exceptions. Texas Instruments has introduced the first four members of its Scope 74BCT8xxx family of JTAG boundary-scannable logic devices. The four members are 20-MHz octal latches and drivers, functionally similar to the industry-standard 74LS244, -245, -373, and -374 devices, but with the addition of the JTAG test bus. They range in price from $4.33 to $4.55 (1000).

More complex scannable devices are also available. The TMS320C50 fixed-point DSP μP from Texas Instruments provides the JTAG test bus. The chip costs $135 in sample quantities. The ADSP21000 floating-point DSP μP from Analog Devices, which should appear later this year, will also provide the test bus.

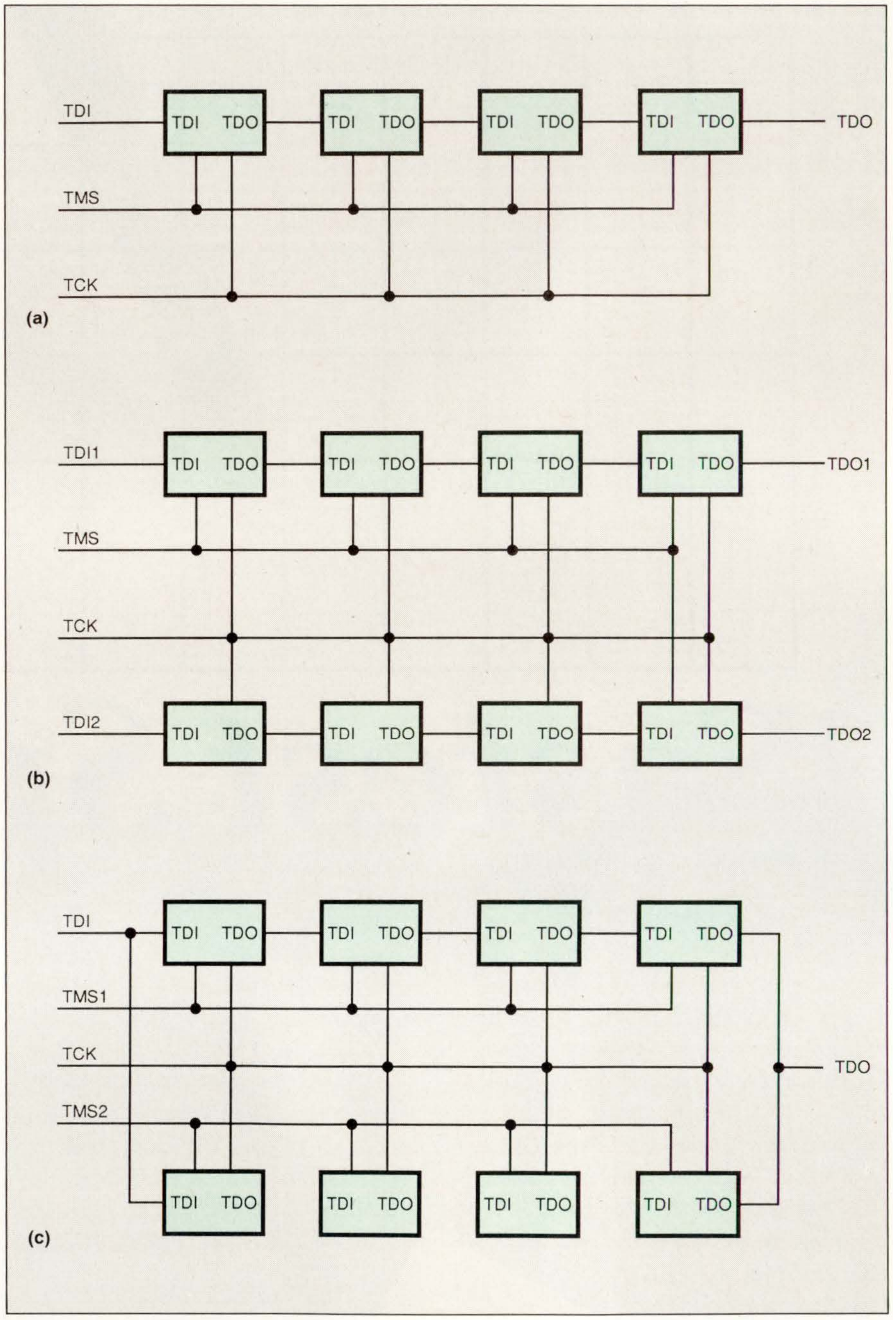
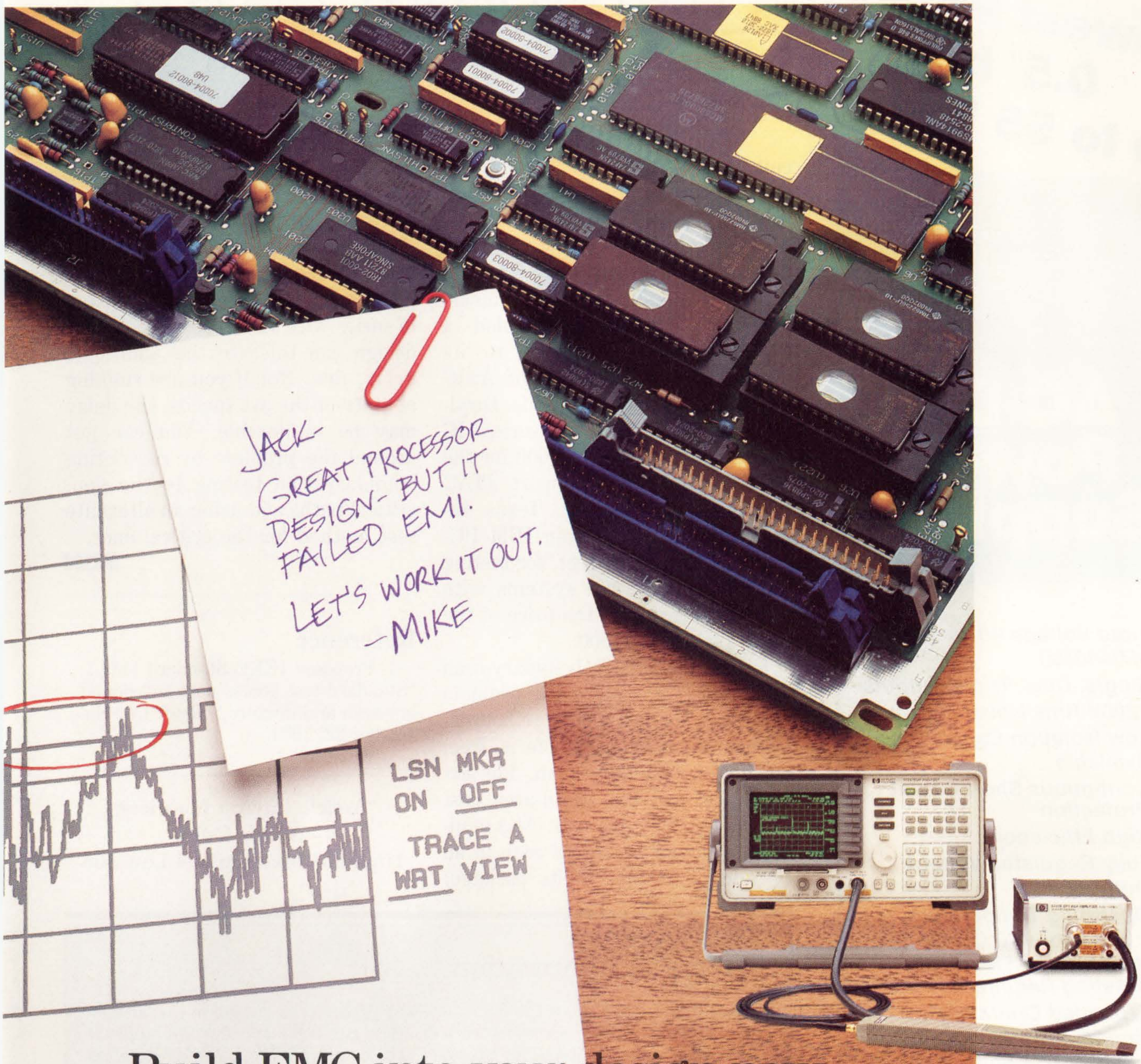


Fig 4—Breaking up is easy to do *if a single scan path through your circuit* ***(a)*** *is too long. You can, for example, create parallel scan paths* ***(b)*** *that operate simultaneously. You can also utilize TDO's 3-state nature to parallel paths* ***(c)*** *that operate independently.*

For the most part, however, JTAG boundary scan is something you'll have to add to your own ICs. Tools to make that addition easier are already on the market. Racal-Redac's SilcSyn 2.0, for example, offers automatic boundary-scan cir-



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Tools to help you test your boundary-scan design are also becoming available. Integrated Measurement Systems has added a $33,000 scan-test module to its Logic Master XL series of ASIC test and verification systems. Hewlett-Packard's HP82000 series IC evaluation systems ($75,000 for the basic system) also support JTAG boundary-scan testing. Texas Instruments is offering an IBM PC-based tool, called Asset, for testing both pc boards and systems with the JTAG test bus; the price of the basic system is $7500.

Using the JTAG boundary-scan technique helps solve the problem of testing surface-mount pc boards. Of course, nothing in life is free; neither is boundary scan. For example, there is a board-area cost for the extra signal lines. At a minimum, putting boundary scan in an IC adds four pins to its package. For large devices the additional pins may not dictate a package size increase, but smaller devices will jump up one size.

There may also be a performance penalty caused by the multiplexers in series with all I/O signals. If your design can tolerate the additional delay, fine. But if you are running at state-of-the-art speeds, the delay may be intolerable. You can get around the problem by restricting boundary-scan testing to the non-critical paths and using an alternate test method for the critical ones.

EDN

Reference

1. Proposed IEEE Standard 1149.1, "Standard test access port and boundary-scan architecture," Draft D6, November 22, 1989.

Article Interest Quotient
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For more information . . .

For more information on the boundary-scan products discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service Card, or use EDN's Express Request service. When you contact any of the manufacturers directly, please let them know you saw their products in EDN.

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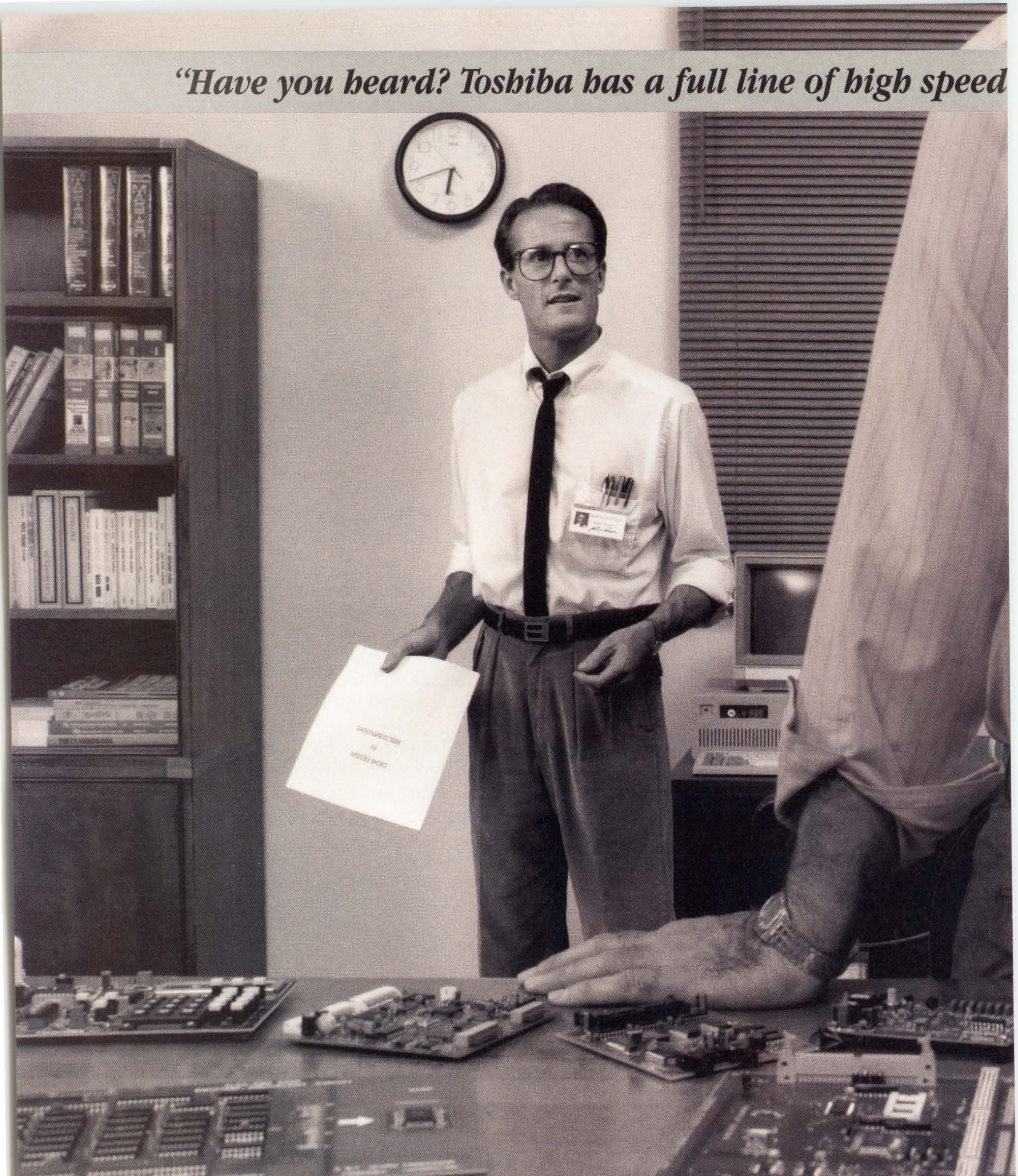

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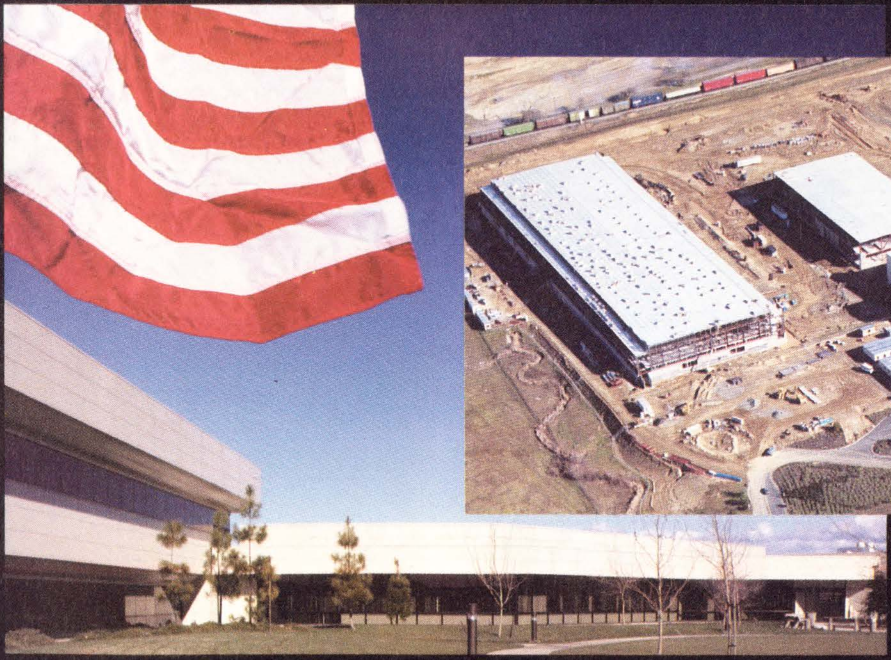

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Intelligent cards display megapixels

Boards based on the TI 34010 and 34020 chips offer the performance and compatibility that users of graphics-intensive CAE and business applications need.

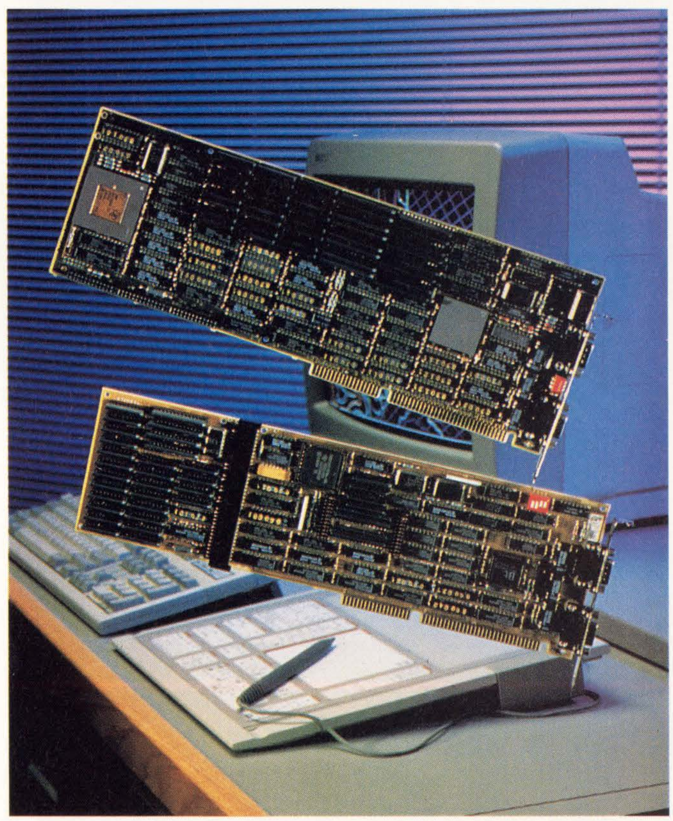
Maury Wright,
Regional Editor

Users of 80X86-based "personal computers" for CAE or other graphics-intensive applications need no longer take a back seat to "workstation users." Intelligent graphics boards based on the Texas Instruments 34010 and 34020 μPs can offload graphics responsibility from your host CPU and greatly accelerate graphics applications and graphics environments such as Microsoft Windows. Furthermore, the 340X0 boards offer compatibility with a wide base of software via the TIGA (Texas Instruments Graphics Architecture) and DGIS (direct graphics interface standard) graphics standards.

The lack of graphics standards at and above the megapixel range has certainly hampered the use of graphics-intensive applications on personal computers. Typically, you need to find graphics software that meets your needs and then buy a graphics board that the software supports. What's more, you're often stuck with a system that runs only a specialized application or two, or one that requires multiple monitors and video cards.

IBM's VGA card provides a standard way to display 640×400 pixels. Subsequently, super and extended VGA cards from third-party vendors now offer a somewhat standard way to achieve 800×600- and even 1024×768-pixel resolution. And although the VGA cards depend on the host CPU to perform the graphics manipulations, today's 33-MHz 80386 and 80486 systems have power aplenty.

Graphics-intensive applications require a more elegant video subsystem



***The 50-MHz 34010 and 25-MHz 34020** intelligent graphics controllers from Hewlett-Packard offer users a price/performance choice. The $2495 Intelligent Graphics Controller 20 is one of the first boards to use the new 34020 processor that implements features such as fast area fills and accelerated text generation. Users on a budget may prefer the $995 Intelligent Graphics Controller 20.*

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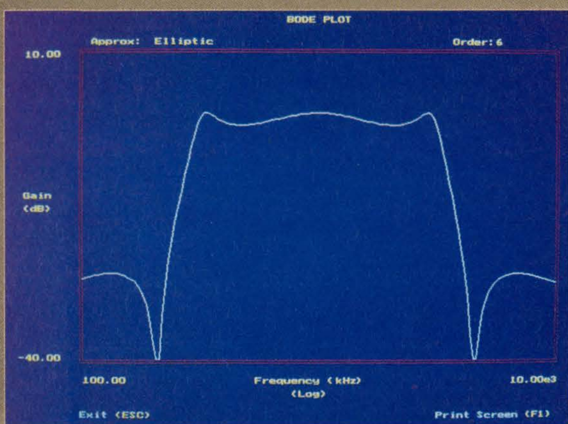

Filter Designer Bode Plot

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than that offered by VGA, though. Almost two years ago, IBM started shipping the 8514/A board, which includes some dedicated circuitry, to offload some graphics primitives from the host. Over the summer, third parties began shipping 8514/A clones. Thus far, the 8514/A occupies less than an industry-standard position because there are some compatibility problems that have to be worked out (see **box,** "TIGA 340X0 vs 8514/A: fact and fiction"). The 8514/A boards also fail to offer the performance that a processor-based board can offer in accelerating a graphics application.

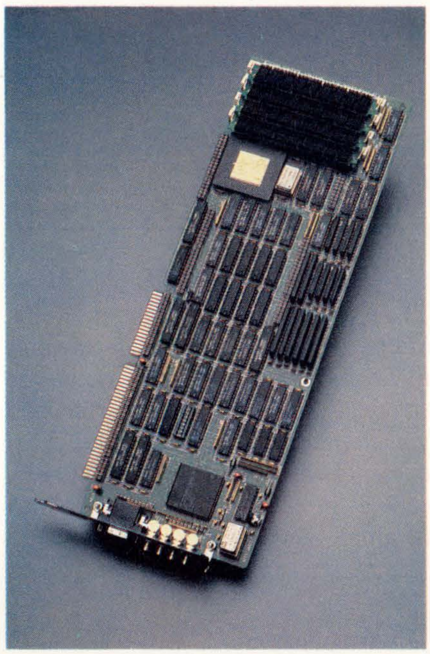
Boards become standard

Intelligent graphics boards that support megapixel resolution have been available for as long as five or six years. The 340X0 boards represent the first semblance of an industry standard, however. TI began shipping the 34010 about four years ago and the 34020 last year. Currently, around 50 vendors offer 340X0 boards for IBM-compatible personal computers, including IBM PC/AT, EISA (Extended Industry Standard Architecture), and Micro Channel Architecture (MCA) bus models. Furthermore, the offerings support resolutions ranging from 640×400 to 4M×4M pixels and offer choices from monochrome to 24-bit color.

According to Doug Crawford, marketing manager for computer video products, TI will soon ship its one millionth 34010. Crawford also estimates that between 70 and 80% of the chips sold go into IBM-compatible personal-computer applications. He expects the company to sell half a million chips this year and to double shipments each year afterward.

Much of the 340X0's success can be traced to TIGA. TI defined TIGA to act as a hardware-independent applications-software interface for 340X0-based boards. In fact, TIGA acts as a graphics operating system that runs on such a board. And any software that includes a TIGA driver can run on a board that hosts TIGA. Board vendors license the graphics standard from TI.

About 50 software applications currently support TIGA. Among them are Microsoft Windows and OS/2 Presentation Manager. Therefore, the hundreds of Windows applications will also run on TIGA boards. And the performance that 340X0 boards offer help most in graphics environments such as Windows. The graphics environment called Halo from Media Cybernetics (Silver Springs, MD) also includes a TIGA driver. And Halo adds support for a couple of hundred more applications.



***Support for 1600×1200-pixel resolution** makes the Artist XJS 34020-based board from Artist Graphics suitable for high-end CAE applications. The board supports 16 colors at its maximum resolution, and you can use the board in a 1280×1024-pixel resolution mode with 256 colors.*

To further embellish compatibility, TI developed a version of the 8514/A AI (adapter interface) for TIGA boards. IBM developed the AI to provide software developers with a hardware-independent software interface to 8514/A boards. Currently, all but about a half dozen applications that support the 8514/A do so via the AI and therefore will run on TIGA boards. You can expect more applications in the future, however, that write directly to 8514/A hardware registers.

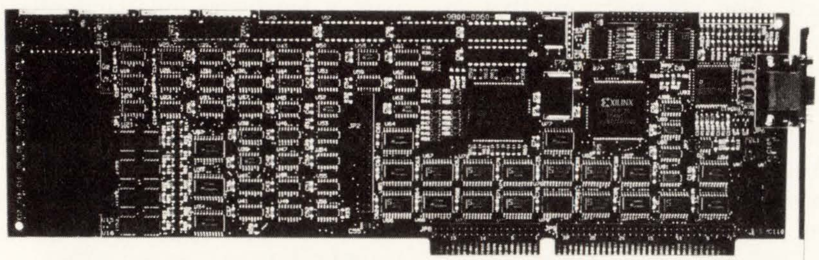
Third-party vendors have also added compatibility to 340X0-based boards. GSS (Graphics Software Systems), for example, licenses its DGIS graphics standard for use on 340X0 boards. The company includes DGIS with its AT1000 and AT1050 boards. The standard adds support for approximately 50 other packages as well. Other well-known vendors of 340X0 boards that support DGIS include Hewlett-Packard, NEC, and Sota Technology. In all, more than 30 vendors of 340X0 boards offer DGIS.

When you consider buying a 340X0 based board, the most important things to examine are performance, price, compatibility, resolutions and colors supported, and upgradeability.

As you might expect, performance is the toughest criterion to judge. Processor-speed rating could give a clue to performance, but most of the newer 34010 boards include 50-MHz processors. For example, the $995 AT1050 and $1495 AT1000 from GSS include 50-MHz μPs. GSS actually only sells the boards on an OEM basis; it also sells manufacturing rights and complete manufacturing kits. NEC sells the products to end users under the name Multisync Graphics Engine.

A few companies offer boards with faster processors. Number Nine Computer Corp sells its Pepper Pro 1024 with a 60-MHz processor, but the board costs $2495. Vermont Microsystems' Cobra family of

Intelligent graphics boards



The programmable frequency output *of the GSS 34010-based AT1050 video card allows it to support virtually any monitor—including adjusting to nonstandard scanning frequencies. The $995 board includes software support for Microsoft Windows and all DGIS-compatible applications.*

boards also uses a 60-MHz processor. The boards start at a base price of $3395. Number Nine's newest board, the #9GRX, uses a 60-MHz chip and has a base price of only $895.

Hewlett-Packard has led the charge to move to the next-generation 34020 μP in search of performance. Carla Klein, an HP product manager, claims that the $2495 Intelligent Graphics Controller 20 based on a 30-MHz 34020 offers about triple the performance of a 34010-based board and 15 times the performance of a VGA board. The company also offers the 34010-based $995 Intelligent Graphics Controller 10.

Jim Cochell, GSS' director of new products, claims GSS achieved 34020-like performance on its boards by designing a custom graphics accelerator IC to complement the 34010. The IC performs fast fills, accelerates text generation, and includes hardware dithering—all enhancements that the 34020 offers. Cochell doesn't think the 34020 is cost effective yet for the mainstream market.

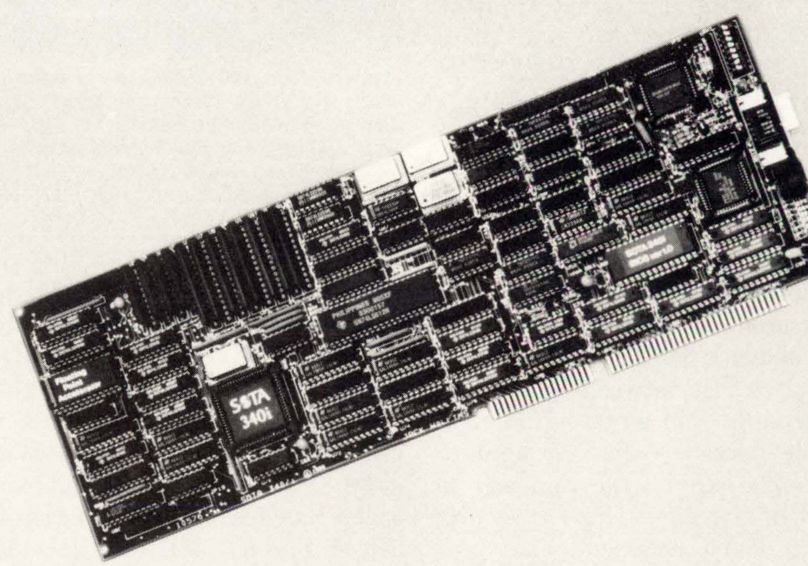
Ultimately, performance depends on a manufacturer's software expertise as much as it does on hardware. TIGA and DGIS implementations affect performance, but you can't measure such effects quantitatively. To find the best performer, you should run your suite of applications on each board you consider.

The price of 34010 boards has dropped considerably in the last year. In addition to Number Nine's #9GRX, GSS/NEC, Hewlett-Packard, and Sota Technology all have boards priced under $1000. TI's Crawford expects to see prices approach $500 by the end of the year. He also thinks that 34020 boards will reach the $1000 level by year's end.

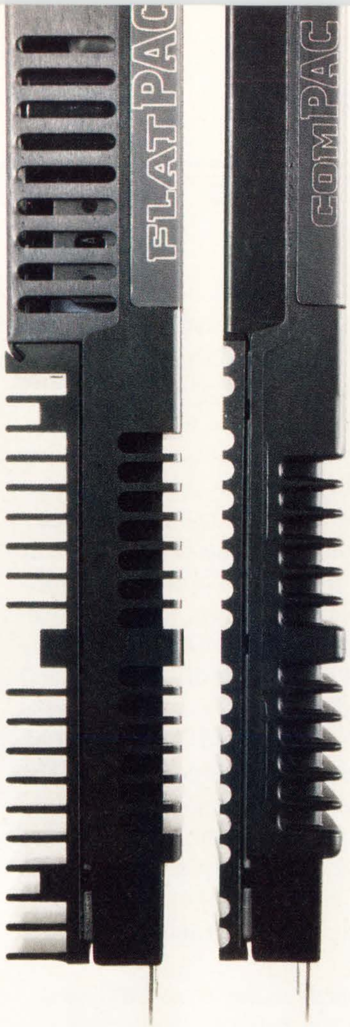
The cost of 34010 boards compares favorably with 8514/A boards. And your monitor will probably cost you substantially more than the video board. Monitors capable of 1024×768-pixel resolution start at about $1000. A 19-in. unit capable of displaying 1280×1024 pixels will cost you at least $2500.

Despite the success of TIGA and DGIS and the growing popularity of Windows, software compatibility is still a problem. You should certainly make sure that your key applications will run on the board you choose. Furthermore, some type of VGA compatibility will ensure that you can run virtually any application as long as you use a

Text continued on pg 88



Resolutions to 1280×1024 pixels *and support for 256 colors make the Sota Technology 340i a flexible choice. You can buy the basic unit for $995 and expand the video RAM frame buffer later.*



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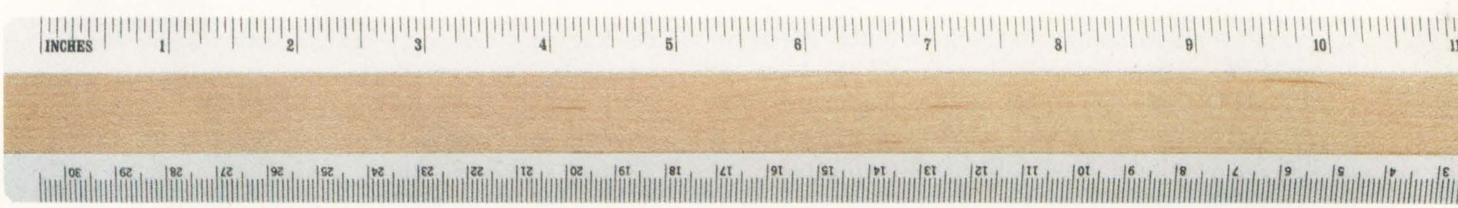

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CIRCLE NO. 46

TIGA 340X0 vs 8514/A: fact and fiction

At the recent Spring Comdex in Atlanta, GA, purveyors of 8514/A-compatible boards waged an all-out verbal war against boards based on the Texas Instruments 34010 and 34020 graphics processor chips. Sifting through the rhetoric, you will find some truths, some half truths, and some outright lies. You should certainly consider both board styles if you need a high-end graphics controller for CAE or other applications on your personal computer. But make sure you compare the technologies on a level playing field.

Designers of IBM-compatible personal-computer graphics boards depend on the competing 8514/A and 304X0 technologies to make a step up in graphics performance from VGA. Vendors offer boards in the 1024×768-pixel resolution range (and higher) based on both. Both technologies have merit, and they may eventually coexist in the marketplace. Boards based on the TI ICs have a huge lead in terms of shipments and availability, however.

IBM began shipping the 8514/A video card almost two years ago. Third-party vendors have only begun production shipments this summer. IBM's 8514/A board includes dedicated circuitry to offload some graphics operations from the host CPU. All prior IBM PC graphics standards required the host CPU to handle the video frame buffer. The board offers 1024×768 resolution and displays 16 (standard) or 256 (optional) colors on interlaced monitors.

Boards based on the TI 34010 have been available for almost four years; 34020 models have emerged over the last year. The 340X0 ICs are actually full-fledged 32-bit μPs with specialized graphics instructions added to a typical μP instruction set. Code written for the 34010 will run unchanged on the 34020. TI also defined the TIGA (Texas Instruments Graphics Architecture) standard to provide a hardware-independent software interface to 304X0 boards.

Weigh many factors

When you examine boards based on the 340X0 with 8514/A boards, consider compatibility, performance, resolution and display quality, cost, and availability.

Compatibility always proves important in choosing a video board. Standard advice includes the tip to choose your software first and then choose a video board that works with all of it. Traditionally, IBM-invented video standards (MDA, CGA, EGA, and VGA) have been safe choices because all software developers support the IBM standards. The 8514/A adds a hitch to assured compatibility, however. IBM intended software vendors to write applications compatible with a hardware-independent software interface called the AI (adapter interface), which was defined for the 8514/A and subsequent video boards. The AI would eliminate the problem of supporting many different displays in application software. Software developers, however, like to write code that communicates directly with the graphics hardware and therefore wrings all of the potential performance out of a video board.

IBM refused to release a detailed description of the 8514/A registers, forcing developers to use the AI. Third-party vendors reverse-engineered the IBM board and custom ICs, however, and the hardware is now well defined. Still, only a handful of applications software currently supports the 8514/A at the hardware level. Most applications that include a driver exploit the AI.

Vendors of 8514/A boards other than IBM that tout performance, however, refer to performance achieved with direct hardware support in applications. Such third-party boards have just become available. The level of hardware compatibility they offer, among each other and with IBM, is yet to be determined. Several vendors at Comdex used proprietary drivers to demonstrate the prowess of their 8514/A boards on applications such as AutoCAD. The necessity of hardware-dependent drivers for good performance paints a different picture than the plug-and-play image championed by the 8514/A vendors.

Boards have many applications

TI 340X0-based boards enjoy no status as an IBM standard. However, they work with many more applications than 8514/A vendors would have you believe. Most of the boards support TIGA, which acts as a graphics operating system on a 340X0 board. A TIGA-compliant board can run any software that includes a TIGA driver. TI currently lists almost 50 popular software packages that include TIGA drivers. That list includes the Microsoft GUIs (graphical user interfaces)—Windows and OS/2 Presentation Manager—and a graphics environment called Halo from Media Cybernetics (Silver Springs, MD). Therefore, TIGA boards will run several hundred other applications through these environments.

Other companies, such as GSS, Hewlett Packard, and NEC, support DGIS (direct graphics interface standard) and TIGA on their boards. Between Windows, Halo, and DGIS, you will find few new graphics applications that the 340X0 board can't run. TI also includes an 8514/A AI driver for TIGA. The 340X0 boards also support AI applications as well as any 8514/A board.

Check before you buy

Performance claims will take the most effort to sort out. The IBM 8514/A includes dedicated circuitry to accelerate three basic graphics functions: line drawing; filled rectangles; and bitblts (bit block transfers). Other graphic operations require help from the host. Furthermore, vendors of 8514/A clones must implement similar architectures to provide register-level and AI compatibility with the original. Even Doug Crawford, TI's marketing manager for computer video products, concedes that the dedicated circuitry of an 8514/A can perform such operations on a par with or faster than a 340X0 board.

Effectively running CAE applications or GUIs such as Windows requires much more than executing a couple of graphics primitives, though, and 340X0 boards can accelerate an entire graphics environment. TI and Microsoft, for example, offload the entire "Windows engine" to the 340X0 in the TIGA Windows driver. No 8514/A boards currently come close to 340X0 boards in the overall acceleration of such an environment. TIGA also allows any application to download code into the graphics board, allowing software developers to customize graphics primitives that speed up their applications.

In addition to good performance, users of high-end personal computers demand resolution in the megapixel range. The IBM 8514/A board displays 1024×768 pixels, 256 colors, and only supports interlaced monitors that are subject to an annoying flicker. Vendors of 8514/A boards argue that the IBM board included undocumented support for 1280×1024 resolution, noninterlaced monitors, and full color. All of the 8514/A clone vendors plan to offer such extended support, but it remains to be seen how the extensions impact hardware or AI compatibility.

TIGA and the 340X0 offer a resolution-independent graphics standard. The board designer can choose to support any monitor type and resolution desired. In fact, you can currently purchase TIGA boards that range in resolution from 640×400 (VGA resolution) to 4M×4M pixels, and that offer support from monochrome to 16.7 million colors.

Cost of a megapixel display subsystem ranges from $1500 to more than $10,000. The 8514/A vendors believe that they will offer boards that cost substantially less than 340X0-based products. In comparing the two types of boards, however, you will find a similar list of components. Both types of boards require similar dynamic RAM or video RAM frame buffers, D/A converters, and look-up tables to support similar resolutions. The 8514/A boards employ a custom chip that implements the graphics functions. The TIGA boards use the TI 34010 or 34020 μP.

Many factors influence cost

The cost of 8514/A boards will depend on the price of the custom chip and therefore largely on the number of boards each vendor can sell. Currently, no one other than IBM has sold many. TI, meanwhile, has sold almost a million 34010 μPs. The chip suits applications ranging from laser printers to workstations. The company expects to ship half a million this year. The TIGA boards, however, do have the added cost of program storage memory because the 340X0 is a μP.

Currently, a few 8514/A boards have street prices approaching $500, although retail prices remain around $1000. TIGA boards feature similar retail prices, and TI's Crawford expects TIGA boards to near the $500 retail level by the end of the year.

Monitor prices, however, contribute more to the cost of a megapixel display subsystem. Both 8514/A and TIGA offerings require monitors that range from a minimum of $1000 for an interlaced unit to $2500 minimum for a 19-in. noninterlaced 1280×1028-pixel unit. In fact, the monitor price makes the small difference in video-board price less significant.

Availability of TIGA boards abounds for the IBM PC/AT, EISA, and MCA buses. Approximately 50 vendors currently ship such boards over a price range of $900 to $5000. Until recently, only IBM shipped 8514/A boards—and only for MCA bus machines. The 8514/A clone vendors finally began to ship units for IBM PC/AT bus machines over the summer—a year later than originally promised.

Intelligent graphics boards

multiple-frequency monitor.

Most of the boards for Micro Channel systems include a "pass-through" connector to VGA. IBM includes VGA on the mother board of its PS/2 systems and introduced the pass-through concept on its 8514/A board. The pass-through circuit allows the VGA controller to drive the monitor when necessary. It connects two video controllers to the same monitor.

The PC/AT bus boards from Hewlett-Packard, Number Nine, and Sota Technology include pass-through capability that works with standard PC/AT bus VGA cards. GSS includes a similar feature on its AT1050 card and actually includes the VGA circuitry along with the 34010 on its AT1000 offering. Adding a CGA (color graphics adapter) or an MDA (monochrome display adapter) simulator on a 34010 board is another workable, but less desirable, compatibility solution that some manufacturers offer. The Number Nine #9GRX includes a VGA pass-through and MDA emulation.

All of the boards discussed here support 1024×768-pixel resolution and noninterlaced monitors at a minimum. Most also can support lower resolutions such as 800×600 that are more suitable for 14-in. monitors. Typically, resolution and number of colors are subject to the amount of frame buffer memory a board includes.

Sota Technology's $995 340i, for example, comes standard with a 512k-byte video-RAM frame buffer and supports 1024×768-pixel resolution and 16 colors. You can upgrade the board for $200 to 1M-byte of video RAM, in which case the board then supports 1280×1024-pixel resolution and 16 colors, or 256 colors at lower resolutions. Likewise, the #9GRX from Number Nine offers 1024×768-pixel resolution with 16 colors as a base and can be expanded to support 256 colors and 1280×1024 resolution.

The GSS AT1050 includes a programmable-frequency output feature that allows you to adjust the board to support nonstandard resolutions. The board supports 1024×768 pixels maximum, but you can set it to a resolution of 900×700 pixels, for example. Such a feature can come in handy in exploiting the maximum noninterlaced resolution a monitor offers.

For higher-resolution CAE requirements, consider the Artist XJS board from Artist Graphics. The 34020-based board supports 1600×1200-pixel resolution and costs $4295. You can also buy a VGA module for the board, and the company plans to offer Micro Channel and EISA versions later this year.

Overall, the boards discussed here certainly offer workstation-level graphics performance—one of the shortcomings pundits believe distinguishes workstations from personal computers. The performance that the 340X0 boards offer certainly can serve the X-Windows market as well as they do Microsoft Windows. You can expect to see widespread X-Windows support emerge for these boards. In fact, expect personal computers equipped with 340X0 boards to completely upstage the demand for dedicated "X terminals"—and industry observers expect a huge demand for X terminals. **EDN**

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For more information . . .

For more information on the graphics boards discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Food for naught.

It should come as no surprise that you'll save money eating where the locals eat. Good and reasonably priced restaurants can be found in department stores and the basements of office buildings. At lunch, ask for *teishoku.* It means special of the day, and includes rice, miso soup, salad, meat or fish, and dessert—all for around five dollars. *Ramenya* and *sobaya* (noodle shops) are perfect places for a quick and tasty meal.

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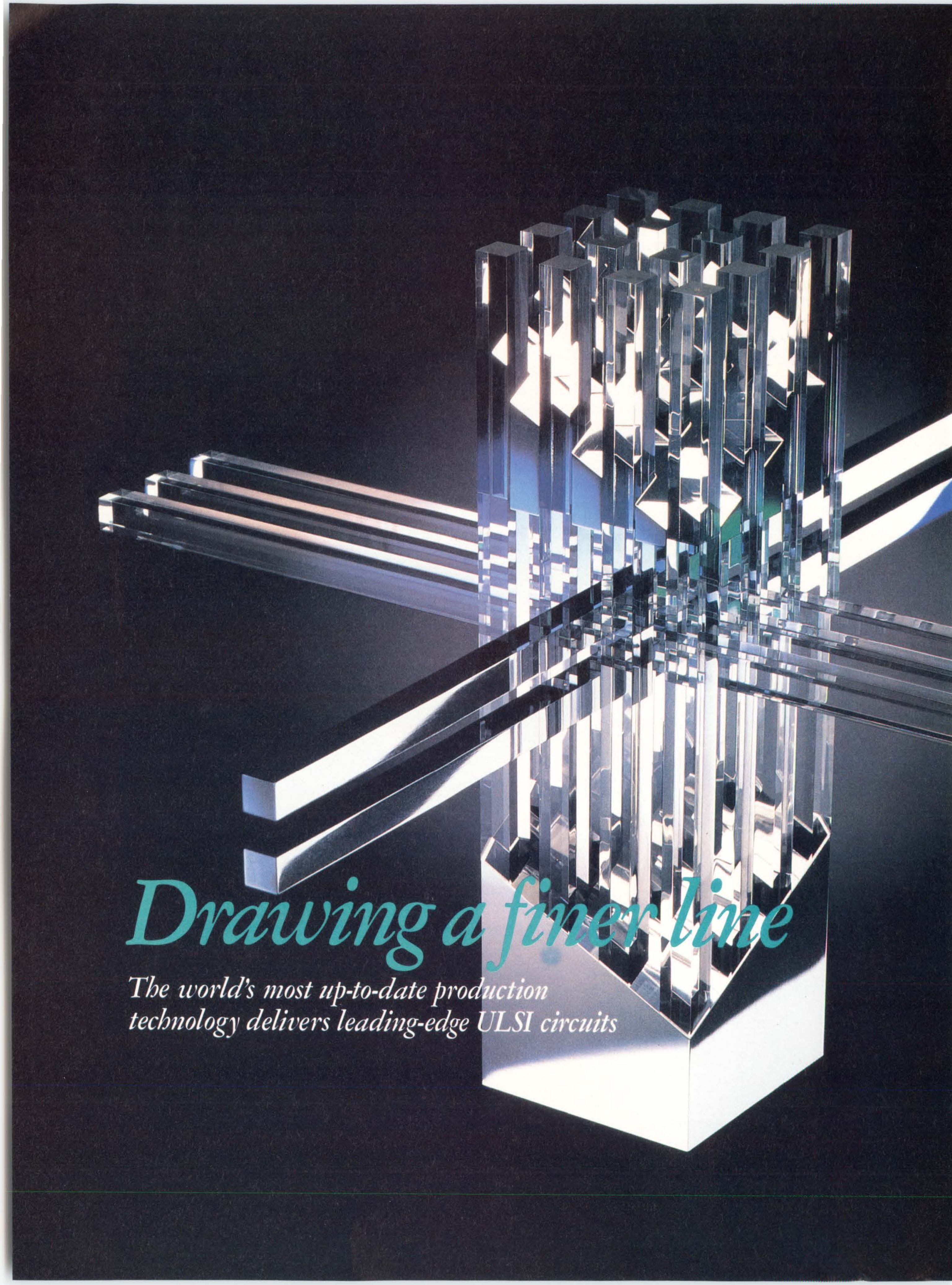

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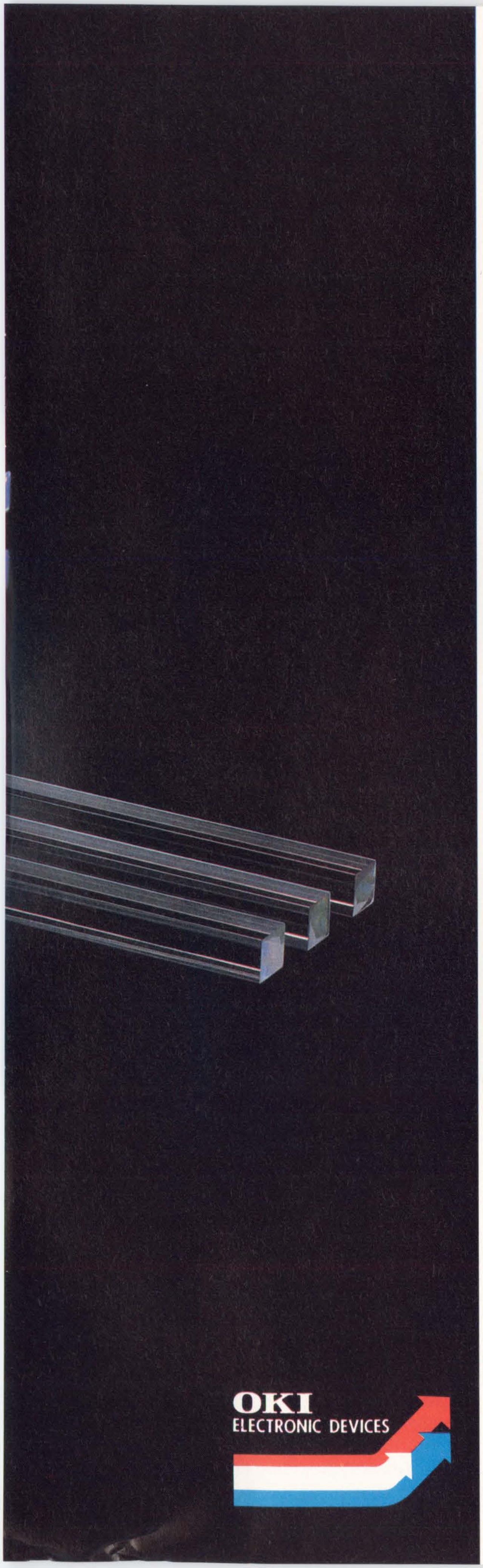

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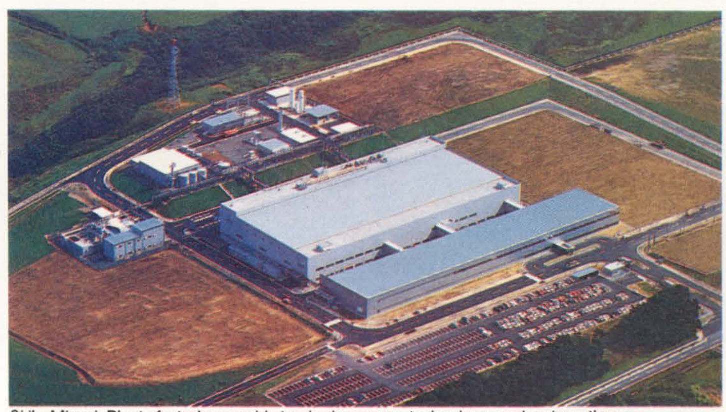

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West Germany
■ Tel: 2101-15960 ■ Fax: 2101-103539
■ Telex: 8517427 OKI D

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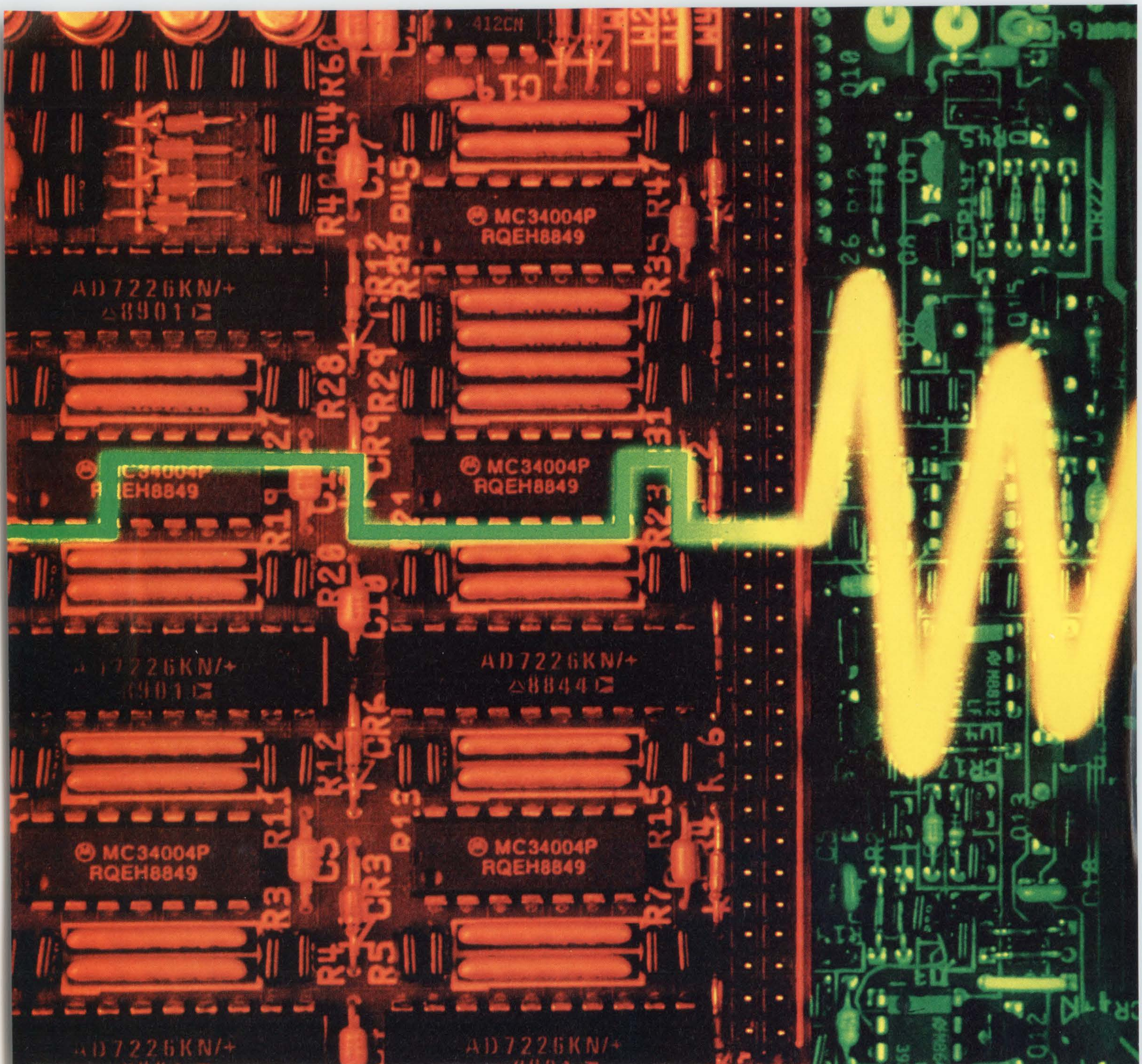

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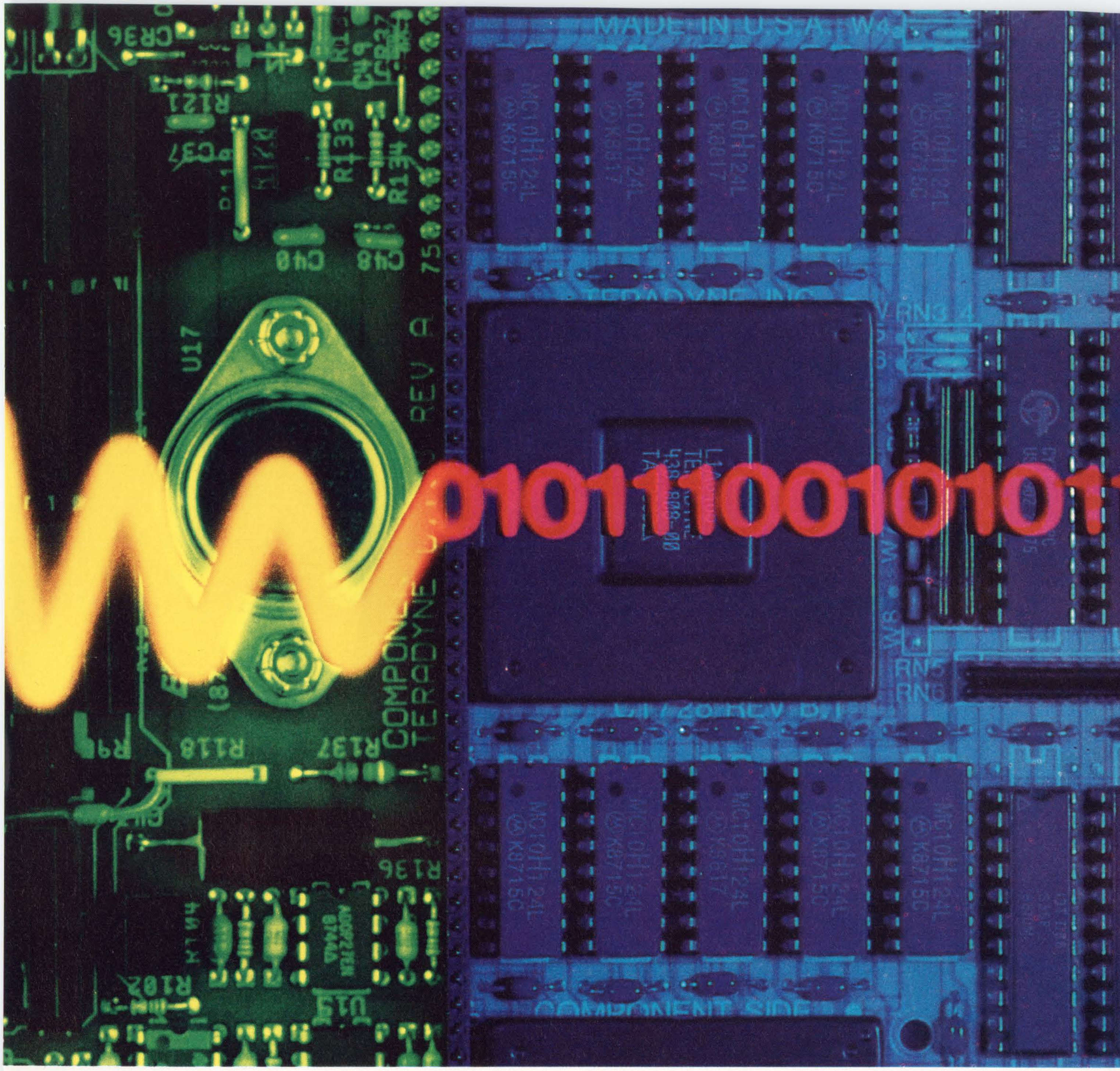

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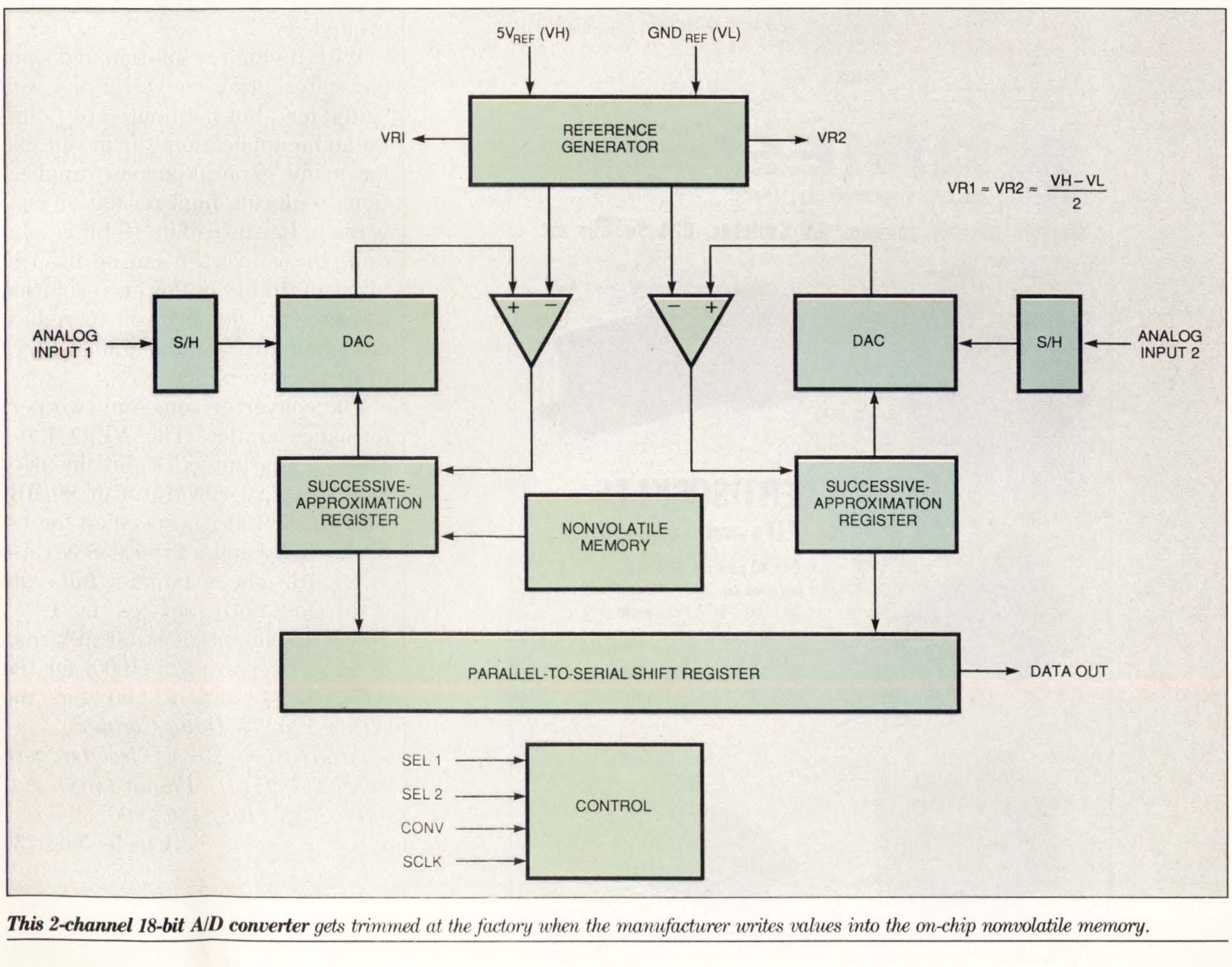
Monolithic single-supply ADC converts to 18 bits in 10.4 μsec

Operating from a 5V supply, the monolithic AT76-C120 18-bit A/D converter can convert 96k samples/sec on each of its two channels. The converter includes dual sample-and-hold circuits that sample both channels simultaneously. Using a successive-approximation technique, the chip converts and then outputs the data from both channels serially on a single-output port. This data is in 2's complement format.

The converter is unprecedented in its use of nonvolatile memory for factory trimming. The on-chip memory allows the manufacturer to compensate for linearity errors by adding correction factors to the digital values. Trimming is performed by the manufacturer and is transparent to the user.

The converter requires two clocks for operation. The conversion clock (CONV) controls the internal S/H function and initiates the output of data after conversion. You can obtain the conversion clock by dividing the system clock (SCLK) by 64. The system clock regulates the conversion and synchronizes the output of individual data bits at the data-output port.



***This 2-channel 18-bit A/D converter** gets trimmed at the factory when the manufacturer writes values into the on-chip nonvolatile memory.*

EDN EDITORS' CHOICE

Two select pins control the converter's operation. The first select pin (SEL1) lets you specify whether channel one or channel two is output first at the single serial-output port. The second select pin (SEL2) controls whether the converter outputs 18 bits or reduces the output to 16 bits. You might select 16-bit operation when extra resolution is not needed so that the data will fit in two bytes instead of three. Sixteen-bit operation does not affect the overall conversion speed.

The converter requires a stable 5V reference for proper operation. A reference-generation block provides ac ground references (VR1, VR2) for signals that swing below ground.

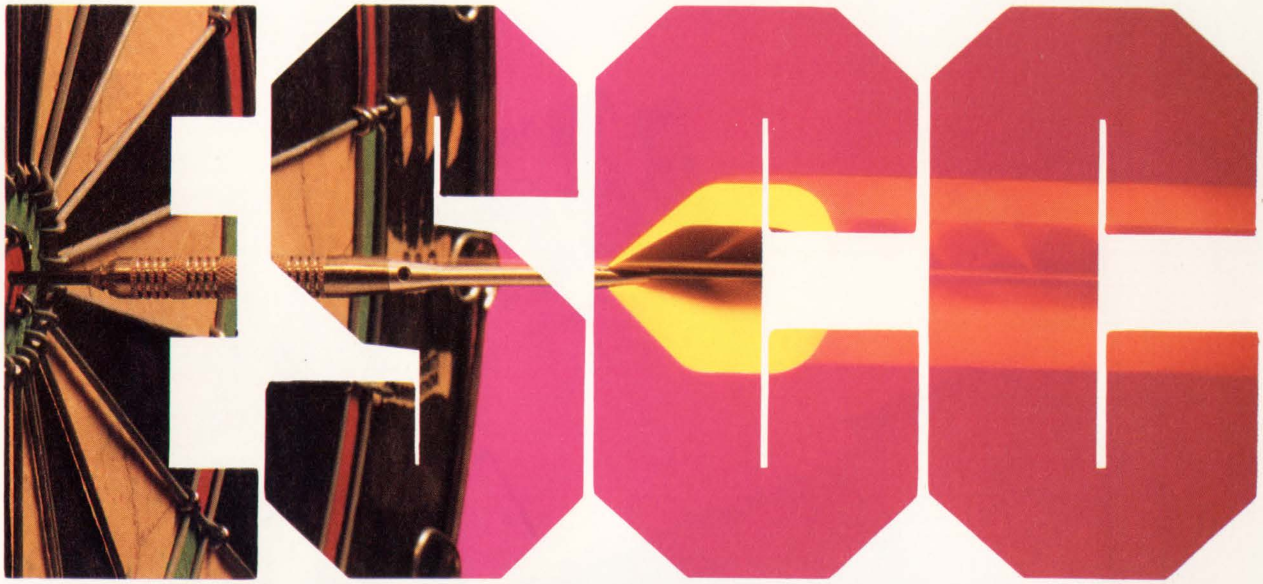
With its high resolution and sample rates, the converter is well suited for—but not limited to—digital-audio applications. It is suitable for many general-purpose applications requiring high-resolution conversion. Because of its 18-bit resolution, the converter can be used in place of 16-bit or lower resolution converters, allowing you to reduce or eliminate variable-gain stages prior to conversion.

The converter comes in two performance grades. The AT76C120-1 offers a guaranteed 15-bit linearity and a typical S/N ratio of 90 dB. The AT76C120-2 is specified for 13-bit linearity and a typical S/N ratio of 84 dB. The maximum full-scale error for both devices is 1.5%. Power consumption is 50 mA max at 5V. Prices are $25 (1000) for the AT76C120-1 and $23.50 for the AT76C120-2.—***Doug Conner***

Atmel Corp, 2125 O'Nel Dr, San Jose, CA 95131. Phone (408) 441-0311. FAX (408) 436-4200.

Circle No. 730

Z I L O G



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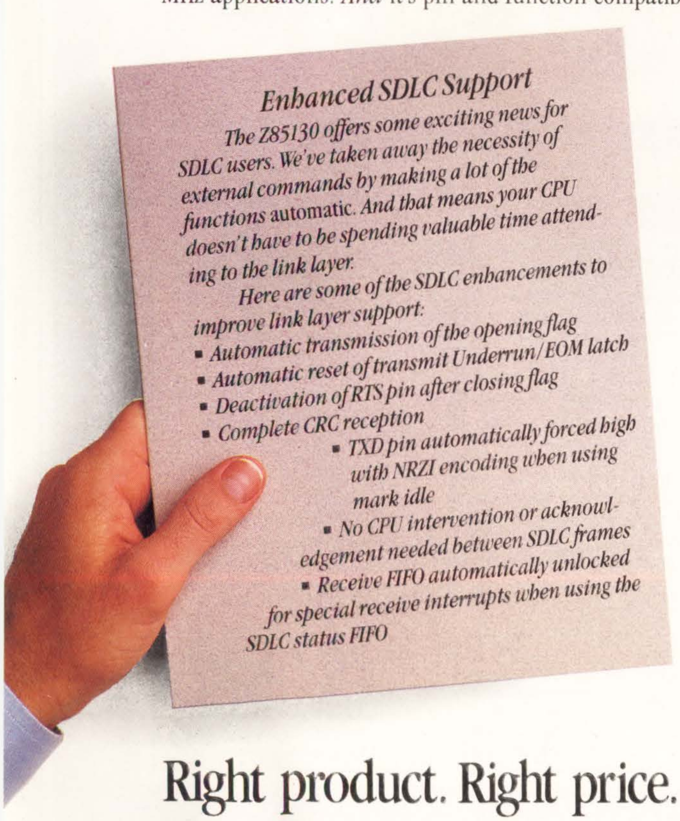

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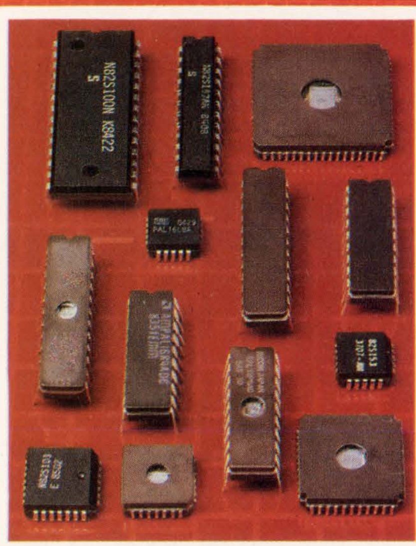

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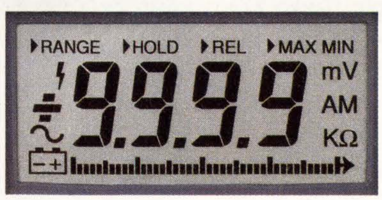

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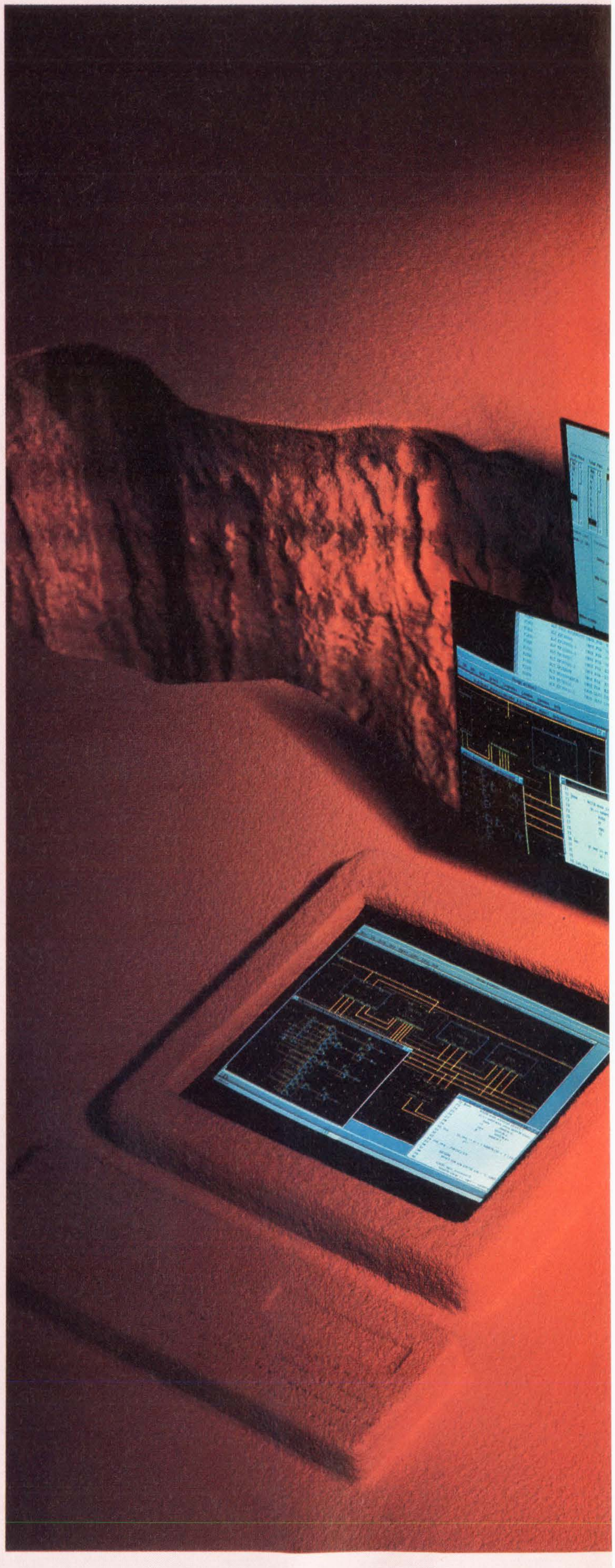
PLD development software

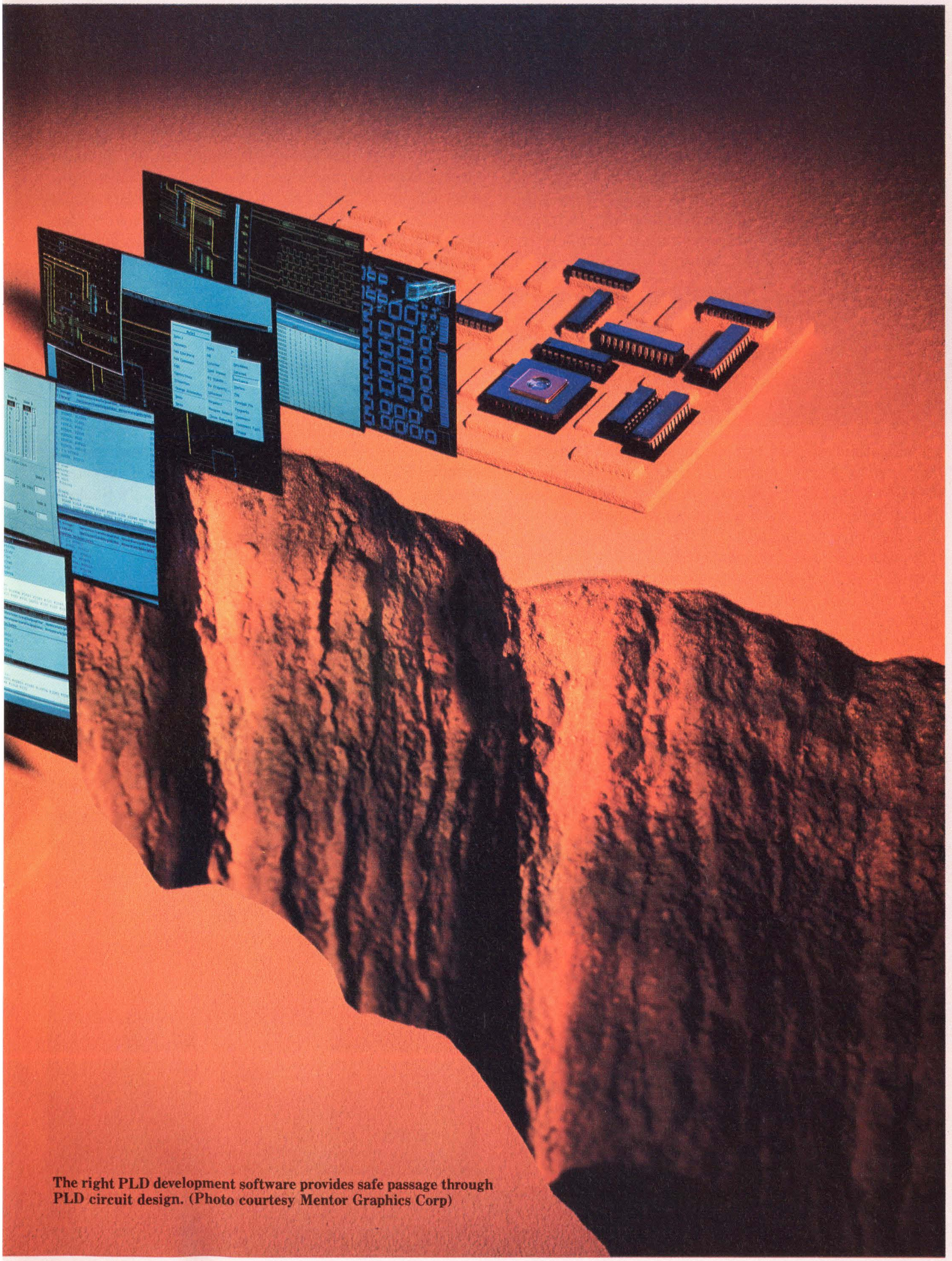
You can't use PLDs in your designs unless you also use the right development software. Choosing that software can be just as important as picking the proper device for your design. The right PLD and the right software will make your job much easier; the wrong choices will stop your project cold.

Steven H Leibson, *Senior Regional Editor*



PLDs and their associated development software form an inseparable team. You can't design PLD-based circuitry without both. Software-development tools for PLDs comprise three types—compilers, simulation products, and test software—and you need all three to complete the job. PLD compilers convert your design into a PLD fuse map. Simulation products, including simulators and device models, allow you to test your design before programming a PLD to make sure that your design is right. They can also save you precious development time. Test software, which includes fault graders and automatic test-pattern generators, helps you keep things right in production.

Many PLD compilers allow you to create a design without regard to any particular device architecture. Sometimes, though, you may wish to use a specific part. If you always have a particular



The right PLD development software provides safe passage through PLD circuit design. (Photo courtesy Mentor Graphics Corp)

PLD in mind when you start a design, almost any PLD compiler will suffice. Early PLD compilers required you to specify the target device in the source-definition file, making device-independent design impossible. Many of the compilers now available allow you to postpone device selection until much later. Compilers that allow device-independent design also accept a device specification, so you can be satisfied in all cases. In fact, you may well elect to use both device-specific and device-independent design methods at different times. Sometimes your requirements are sufficiently general, in which case many PLDs will meet your design needs. For other designs, you may wish to use a special feature that is available in only one vendor's PLD. There's little need to postpone device selection in such instances.

Simulation can save you precious development time. Test software helps you keep things right in production.

Device specificity introduces one of the first criteria you should consider when selecting a PLD compiler: device support. Some vendors offer universal compilers that can generate fuse maps for many PLD types. Other vendors, generally the PLD manufacturers themselves, offer device-specific compilers for their own PLDs. Most PLD programmers accept JEDEC Standard No. 3A fuse-map files, and because most PLD compilers generate such files, you can use most PLD compilers with almost any PLD programmer. **Tables 1** and 2 list several representative universal and device-specific PLD compilers. Note that in each table, only general PLD types are listed under the "PLDs supported" column. Some of these products generate fuse maps for dozens of different PLD architectures and thousands of individual devices, and are therefore virtually impossible to catalog. For an up-to-date, complete device listing, contact the individual compiler vendors.

Do not construe the listing of a supported PLD family in **Tables 1** and **2** to mean that all devices of that family are supported by that compiler. Some of the compilers listed do indeed support every available PLD in the families listed. Other compilers support only a few devices in each family. The list of supported devices for each compiler grows regularly.

You must obtain a compiler that creates fuse maps for all of the PLDs you plan to use. Although that may seem an obvious statement, it has deep implications. Once you select a compiler, you will invest quite a bit of your time learning the idiosyncrasies of the product you pick; you'll not enjoy adopting another compiler later without a strong reason for doing so. Unlike high-level languages for µPs, no standard language exists for PLD source files. Consequently, the source languages for the various PLD compilers vary widely even at the simplest level.

Table 3 demonstrates the diversity among PLD compilers by listing the Boolean, arithmetic, and relational operators for several of the compilers listed in the first two **tables**. If you try to master several PLD compilers, you can easily become confused trying to remember one compiler's symbol for the exclusive-OR operator or whether another compiler supports arithmetic operations. Incidentally, you should not underestimate the value of relational and arithmetic operators for defining PLDs. You can use these additional operators in several applications that formerly used only Boolean operators. For example, if you're defining an address decoder that decodes the address space from hexadecimal address F000 to F7FF, you might write

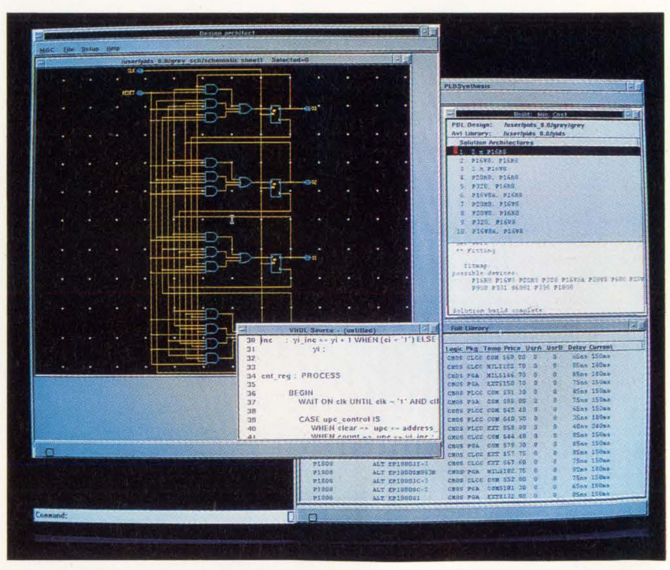
!ENABLE = A15 & A14 & A13 & A12 & !A11

which will work fine. However, using relational operators you can write the same equation as

!ENABLE = (ADDRESS >= F000) & (ADDRESS <= F7FF)

which generates the same function but gives a much better description of what you're really trying to do.

New PLDs appear all the time. The devices you use



***Multiple entry methods** for PLD designs, such as schematic drafting, VHDL descriptions, and traditional Boolean equations, allow you to match your design style to the problem. (Photo courtesy Mentor Graphics Corp)* today may not be the parts you'll use next year. Data I/O Corp claims that more than 250 PLD architectures and 3000 individual devices already exist. More are on the way. Many universal compiler vendors, including Data I/O, try to add device support to their products as soon as possible, but the PLD vendors don't always cooperate. Some PLD vendors keep the tools for their architectures as proprietary as their PLDs. If you must use a brand new PLD architecture, then a device-specific compiler such as those listed in **Table 2** may be your only choice. All of the PLD vendors that offer development tools for their devices do so to support their IC products. Some fear that the universal compilers won't adequately support the special features of their unique PLD architectures.

An example of the potential mismatch between a universal compiler and a PLD arises with flip-flops in some of the newer PLDs, such as Altera's EPLDs (erasable PLDs). You can configure the output registers in some of these devices as JK, T, and SR flip-flops, in addition to the more common D type. But some universal compilers can only create equations for D flip-flops. Your design may work better (fit more efficiently into the PLD) if you use a non-D type flip-flop to create the macrocell equations. The resulting inefficiency in generating product terms may mean the difference between a design that fits in a particular device and one that does not. That's one reason why

Table 1—Representative universal PLD compilers for IBM PC and compatible computers

Manufacturer	Product	Price	Entry Methods: Boolean Equation	Truth Table	State Machine	Waveform	Schematic	Logic Minimizer	Editor	PLDs Supported (nonexhaustive)
Accel Technologies	Tango-PLD	$495	Yes	Yes	Yes	No	Yes	Espresso	Optional	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs, Atmel ATV
Advanced Micro Devices	Palasm 90	$70	Yes	No	Yes	No	No	Yes	Yes	PALs, FPLSs
Data I/O	ABEL	$1995	Yes	Yes	Yes	No	Optional	Presto, Espresso	No	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs
Inlab	proLogic	$249	Yes	Yes	Yes	No	No	No	No	EPLDs
ISDATA	Log/iC	$1480 to $2280	Yes	Yes	Yes	No	Optional	Fact, Bruno	No	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs, Atmel ATV
Logical Devices	CUPL	$1495	Yes	Yes	Yes	No	Optional	Redundancy minimization, Presto, Espresso, Quine-McCluskey	Yes	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs, Atmel ATV
Minc	PLDesigner	$1950 to $4500	Yes	Yes	Yes	Yes	Yes	Sum-of-Products, Espresso, Quine-McCluskey	Yes	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs
	PGADesigner	$2500 to $6000	Yes	Yes	Yes	Yes	Yes	Sum-of-Products, Espresso, Quine-McCluskey	Yes	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs, Altera MAX, Actel ACT-1, Xilinx
National Semiconductor	Plan II	Free	Yes	No	No	No	No	No	No	PALs, GALs
Omation	Schema-PLD	$495	Yes	Yes	Yes	No	Yes	Quick-min, Presto, Quine-McCluskey, proprietary method	No	PALs, GALs
OrCAD Systems	OrCAD/PLD	$495	Yes	Yes	Yes	No	Yes	Quine-McCluskey, McBoole	No	PALs, GALs, EPLDs
Pistohl Electronic Tool	SP11	$295	Yes	No	No	No	No	No	Yes	GALs, EPLDs

Altera offers device-specific development tools for its parts.

No matter which compiler type you pick, your next choice is the design-entry method. With early PLD compilers, you had no choice—Boolean equations. You can live with that one technique for virtually any design you can imagine. However, Boolean equations do not provide the best possible entry method in every instance, so compiler vendors introduced many more options. The five most common design-entry methods, which are listed in **Tables 1** and **2**, are Boolean equations, truth tables, state-machine design, schematic entry, and waveform entry.

> Device specificity introduces one of the first criteria you should consider when selecting a PLD compiler: device support.

Boolean equations and truth tables use text files for the design specification. You can use your favorite text editor to create these source files. Also, many compiler vendors provide text editors either as an option or as an integral part of their compiler. One vendor, Accel Technologies, adopted a well-established, PC-based text editor as the preferred mate for its Tango-PLD compiler. The text editor, called Brief, is available for $199. Brief, a product of Solution Systems (South Weymouth, MA, (617) 337-6963), performs as both text editor and user interface for Tango-PLD.

If you are creating state machines with PLDs, you should seriously consider using a compiler that supports such designs with an entry method tailored to the task. Some PLD compilers that permit you to design using a special state-machine notation support both the Mealy and Moore state-machine models; some support only one model. Unless you are a dedicated advocate of one model, you should be able to build the state machine you want with either form.

All of the state-machine entry methods for the compilers listed in **Tables 1** and **2** employ text-based source files, even though the manuals often illustrate examples with graphic state-machine representations. However, Hewlett-Packard's 74150A PLD Design System and PLD Master from Dazix allow you to draw your state machines. The PLD Design System lets you draw state diagrams with a special editor and troubleshoot those designs with an interactive debugger. The PLD Design System runs on HP's Model 9000 Series 300 workstations and costs $13,700. The compiler's device library includes PALs, GALs, PEELs, FPLAs, FPLSs, and EPLDs (for an explanation of these abbreviations, see **Glossary**). PLD Master, a $5000 module, employs a graphic state-machine representation that resembles a software flowchart.

The last two common design-entry methods are schematic entry and waveform entry. Schematic entry is a natural choice for PLD designs. Using schematic representations of gates, flip-flops, and registers, you can easily create a design that will fit into a PLD's primitive elements: gates, flip-flops, and registers. Some of the compilers accept files from several schematic editors; some will accept schematic files with a little help.

Table 2—Representative device-specific PLD compilers for IBM PC and compatible computers

Manufacturer	Product	Price	Entry Methods: Boolean Equation	Truth Table	State Machine	Waveform	Schematic	Logic Minimizer	Text Editor	PLDs Supported (nonexhaustive)
Altera	PLDS-Encore	$9995*	Yes	Yes	Yes	No	Yes	Yes	No	All Altera EPLDs
Cypress Semiconductor	PLD Toolkit	Free to $395	Yes	No	No	No	No	No	No	Cypress PALs, 7C330 family
Intel	iPLDS II	$1995*	Yes	Yes	Yes	No	Yes	Espresso	No	Intel EPLDs
International CMOS Technology	Place I	$695	Yes	No	Yes	No	Yes	Yes	Yes	PEELs
Programmable Logic Technologies	LogicLab	$499*	Yes	No	No	No	No	Yes	Yes	GALs
Signetics	Snap 1.4	$795	Yes	Yes	Yes	Yes	Yes	Yes	No	PLC42VA12, PLHS501, PLHS502, PLHS601, PML2552, PLUS105, PLUS405, PLUS153, PLUS173
Texas Instruments	proLogic	Free	Yes	Yes	Yes	No	No	No	No	EPLDs

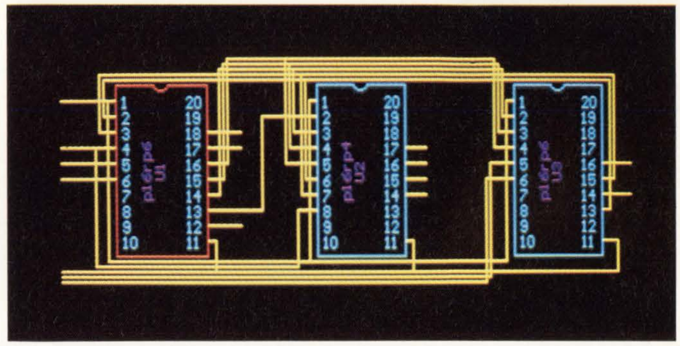
Note: * = Price includes a device programmer.

For example, Data I/O's $250 On-CUPL package translates schematic files generated by several PC-based schematic editors into text files containing CUPL equations.

Ideally, you'd like to mark an arbitrary block of circuitry on your schematic and ask the compiler to design the appropriate PLD. Such a feature would allow you to experiment with different design approaches. Unfortunately, the PLD compilers' ability to work with schematic files remains somewhat crude. You must often use an entire schematic to define the PLD, although some compilers allow you to isolate the PLD to one schematic sheet or hierarchical level. If schematic entry is important to you, check to make sure that the compiler you're considering is compatible with your preferred schematic editor.

Very few PLD compilers currently accept waveforms as PLD source files—but this design-entry method is indeed very handy. Many specifications you work with, such as a μP's bus cycle or the SCSI bus handshake protocol, are specified as waveforms. Using waveform entry, you can copy the waveforms that you plan to apply to the PLD's inputs, add the waveforms you wish to obtain from the PLD's outputs, and then ask the compiler to figure out what circuitry should go in between. Without waveform entry, you must manually convert the waveforms into some other format so that you can enter the design data using a different entry method. Any sort of mental conversion is subject to translation errors due to human error, so waveform entry is valuable for certain designs. The compilers from Minc and HP support waveform entry. More should.

Other entry methods exist beyond the five mentioned here. For example, OrCAD/PLD version 1.1 introduced an entry method called "streams," which



After partitioning your design, *Logical Devices' PLPartition software draws a partial schematic to show you how to connect the selected PLDs.*

Table 3—Operators for selected universal PLD compilers (noninclusive list)

Product	ABEL	CUPL	LOG/iC	OrCAD/PLD	Palasm 90	PLDesigner	Plan II	Tango-PLD
Boolean operators								
AND	&	&	&	&	*	*	* or &	&
NAND				&'		/*		!&
OR	#	#	+	#	+	+	| or +	|
NOR				#' or !#		/+		!|
Exclusive OR	$	$	$	## or $	:+:	(+)	^, $, :+:	^
Exclusive NOR	!$			##'	:*:	/(+)		!^
NOT	!	!	/	' or !	/	/	! or /	!
Arithmetic operators								
Add	+ +	+		+				
Subtract	– –	–		–				
Multiply	* *	*		*				
Divide	/ /	/		/				
Modulus	% %	%		\				
Exponent	**	**		**				
Relational operators								
Equal	= =	:		= =		=		= =
Not equal	!=			/=	< >	< >		!=
Greater than	>			>	>	>		>
Greater than or equal	> =			> =	> =	> =		> =
Less than	<			<	<	<		<
Less than or equal	< =			< =	< =	< =		< =

allows you to specify output values using an implicit sequence of input states. For example, you could write

```
Stream: Step[3~0] -> Y
{ 0, 0, 7(0,1) }
```

which defines a 16-state waveform with two states of a low output signal followed by a 14-state square wave. Note that this method gives you a shorthand method for specifying repetitive waveforms. The parameter 7(0,1) specifies seven consecutive groups of the sequence (0,1). This method works well if you want to create an arbitrary output waveform using very few characters.

Don't underestimate the value of relational and arithmetic operators for defining PLDs.

Looking to the future, when more input methods become available, Data I/O has rewritten ABEL so that the front-end design (design specification and minimization) and the back-end design (fitting and fuse-map generation) are separated by a well-defined interface (**Fig 1**). That interface takes the form of an extended Berkeley Espresso PLA file format, which ASIC vendors commonly use. This de facto standard file format allows other tool vendors to replace ABEL's front-end tools so that you can describe your design using entry methods not supported by ABEL, such as VHDL (VHSIC Hardware Description Language) descriptions or waveforms. ABEL's fitter and fuse-map generator can then create your PLD's JEDEC file.

You can also replace ABEL's back-end tools so that

Glossary

ASIC (application-specific integrated circuit): An IC that is customized for a particular application. The term ASIC usually refers to nonprogrammable devices (devices configured by the semiconductor vendor) but occasionally is used to refer to PLDs as well.

Boolean equations: Behavioral descriptions of a digital circuit's operation using logical (AND, OR, NAND, NOR, exclusive OR, and NOT) notation.

Buried registers: Registers inside a PLD that cannot drive the device's output pins. Buried registers are generally used to implement state machines or to store values.

Design verification: Simulation of the logical operation of a PLD to confirm that a design works properly. You supply the input vectors and the expected output vectors. The design verifier then tells you if you're going to get what you expect.

EPLD: Erasable programmable logic device—a type of PLD. EPLDs are available from Altera, Cypress Semiconductor, Intel, and Texas Instruments.

Fault: A circuit node in the PLD that is stuck high or low so that the attached circuitry cannot operate correctly.

Fault grading: The evaluation of a set of input vectors to determine how many potential faults the vectors can identify. Usually expressed in a percentage, such as 99.9% coverage.

Fitter: A PLD compiler module, program, or subprogram that matches the logical operations of a design to the physical capabilities of a PLD.

FPLS: Field-programmable logic sequencer—a type of PLD. FPLSs are available from Signetics and Advanced Micro Devices.

Functional simulation: A simulation method that simulates a circuit using logic equations and behavioral descriptions rather than device characteristics. This technique is faster but less accurate than timing simulation.

Fuse map: A description that indicates how the programmable elements of a PLD are to be programmed. Unlike today's devices, early PLDs used fuses almost exclusively. But today, some PLDs use EPROM or EEPROM cells to program the internal logic. Nevertheless, for historical reasons, the portion of a file that describes the programming of such a PLD is still called a fuse map.

Fuse mapper (mapper): The PLD compiler module, program, or subprogram that generates a PLD's fuse map by matching the desired interconnections and macrocell configurations to the appropriate programmable elements in the device.

GAL: Generic array logic—a type of PLD. GALs are available from Lattice Semiconductor (Hillsboro, OR, (503) 681-0118), National Semiconductor, and SGS-Thomson Microelectronics (Phoenix, AZ, (602) 867-6259).

Initializable circuit: A circuit that can be forced into a known state after power is applied. Initializable circuits are easier to test than circuits that your PLD design can easily become an ASIC simply by shipping the PLA file to an ASIC vendor. Thus you can prototype a circuit using ABEL to create PLDs and then convert your designs into an ASIC without redesigning the part. Looking at it from another perspective, you can now use ABEL to design ASICs. Data I/O plans to ship this latest version of ABEL (4.0) this month.

Minimization buys you more silicon

Once you've entered your PLD design in some way, your next step is to create the fuse map. Early PLD compilers took this step in one jump. Direct translation of a design file into a fuse map is certainly fast and remains a viable option for simple designs. However, this approach loses its lure for large PLDs. If you want to make efficient use of a PLD, you must use some sort of minimization or reduction algorithm to compress the design so that it fits the available macrocells. If you don't minimize, you may need to buy a bigger, more expensive PLD.

PLD compilers use a variety of minimization algorithms to perform this task. The most popular minimization algorithms are Espresso, Presto, and Quine-McClusky, all of which were developed originally as ASIC design tools but have been adopted for PLD compilers. Many PLD compilers also reduce terms by using deMorgan's theorem. They try both positive- and negative-true logic and select the approach that uses the fewest product terms. Each minimization method offers some advantage (usually speed or efficiency), and several PLD compilers now offer a choice of several methods, as indicated in **Tables 1** and **2.** Some PLD compilers, such as ABEL, also allow you to apply minimization algorithms on a pin-by-pin basis, in case you want to keep redundant terms in some of your combina-

---

can't be initialized.
PAL: Programmable array logic—a type of PLD. PALs are available from Advanced Micro Devices and many other alternate sources.
Partitioning: Decomposition of a design into smaller modules that will each fit in one PLD.
PEEL: Programmable, electrically erasable logic—a type of PLD. PEELs are available from International CMOS Technology.
Macrocell: A configurable logic element within a PLD that can perform several different operations.
Minimization: The removal of redundant logic terms from the functional description of a digital circuit or gates from the circuit itself. Minimization and reduction are frequently used interchangeably.
PLD: An all-encompassing term for logic devices that can be configured in a device programmer. Programmable memory ICs such as EPROMs, EEPROMs, and PROMs are not generally considered to be PLDs.
Preloadable device: An IC that can be placed in any desired state, usually by jamming the desired value into the device's internal registers. Contrast this term with the "initializable circuit," which can be initialized, but perhaps not to any desired state but only one state.
Reduction: See minimization.
Simulator: A software program that mimics some facet of a circuit's operation so that you can verify various aspects or your design without building the circuit or programming a PLD.
Test vectors: Sequences of 1s and 0s that describe a stimulus and how a circuit should react to that stimulus. Part of the text vectors constitute input vectors to be applied to the device under test and the remaining portions of the test vectors indicate the expected response from the device.
Timing simulation: A simulation that uses device propagation delays to produce an accurate estimate of circuit performance.
Truth table: A tabular method for describing logical equations. This method provides a sort of shorthand notation and allows you to simply type the input and output conditions without describing the equations that relate the two. The compiler then generates the equations from your table.
Uninitializable circuit: A logic circuit that cannot easily be placed in a known state after power is applied. Such a circuit is tough to test and should be avoided whenever possible to avoid alienating the manufacturing department.
Unit-delay simulation: A form of idealized timing simulation that uses delay increments of one dimensionless unit instead of nanoseconds or picoseconds. Unit-delay simulation is faster than timing simulation but not as accurate.
Universal PLD compiler: A software product that converts source files to fuse maps for PLDs from a variety of manufacturers.

torial output equations to avoid output glitches. Reduction of state-machine terms usually causes no problems because the clocked nature of the state machine makes it insensitive to the resulting glitches.

The minimization step produces a compacted representation of your design. Until this point, you need not have specified a PLD architecture. Some PLD compilers allow you to take these first steps without selecting a specific PLD. Other compilers force you to declare a target PLD in your source file up front. One way or another, you need to select a device that has the physical resources necessary to implement your reduced equations. This step is called "fitting." If you've had a specific device architecture in mind all along, you can simply turn the compiler's fitter loose and see if your design fits.

> If you don't minimize, you may need to buy a bigger, more expensive PLD.

Some compilers, such as Minc's PLDesigner and HP's PLD Design System, will partition your design by trying single- and multiple-PLD solutions to create the "best" fit. PLDesigner allows you to define what is best for your design through a table of weighted parameters. These parameters include propagation delays, power dissipation, and device cost. You select what factors are important and PLDesigner will generate alternatives, rank them according to your values, and then list the ten best solutions. You can pick one of these solutions and generate the appropriate fuse maps or go back and change your weightings to investigate alternative solutions.

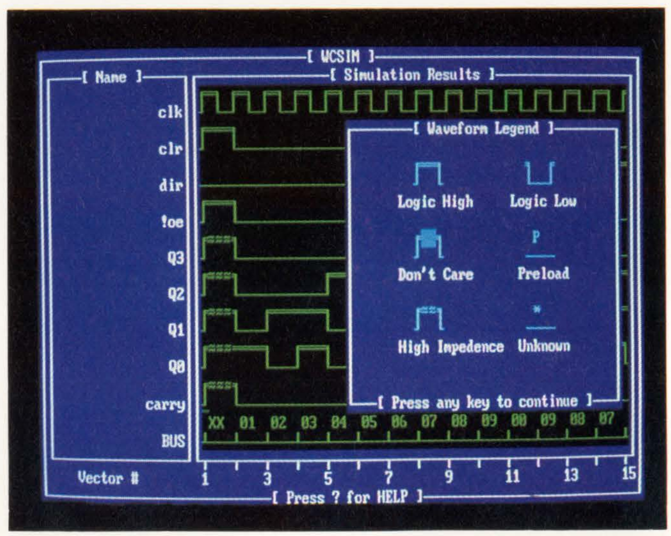
Logical Devices offers two separate programs that add a partitioning ability to the company's CUPL compiler. The $495 PLAdvisor solicits your design criteria and then generates a list of candidates from its PLD library. The $995 PLPartition accepts the list generated by PLAdvisor or a list of devices that you supply and then partitions your design to fit in one or more of the candidate parts. You don't need PLAdvisor to use PLPartition.

Save time by narrowing the choices

You usually won't want a partitioner to consider every PLD in its library during the partitioning phase. PLDesigner's library manager allows you to create your own device library, which can be a subset of the parts that Minc's compiler supports. For example, you may want to create subset libraries that contain just the PLDs in your lab stock, the PLDs on your company's approved-parts list, or the PLDs in your manufacturing inventory. Creating a reduced library speeds up partitioning by eliminating obviously useless choices.

Some engineers like automatic partitioning because they aren't familiar with the hundreds of PLD architectures available. They appreciate a compiler's ability to explore alternative design solutions. Other engineers already know what PLDs they want to use; they aren't interested in this feature. Even if you are already familiar with all the devices you wish to consider, partitioning software can explore many more possibilities in far less time than you can by hand. Furthermore, if you want total control over device selection, compilers with partitioning modules usually allow you to pick the target device when you must.

Tables 1 and **2** list PLD compilers that run on IBM PC and compatible computers. These compilers use a variety of user interfaces on the PC, ranging from line-oriented to menu-driven schemes. For Apple Macintosh fans, Capilano Computing offers MacABEL, a $2350 version of the ABEL compiler. Macintosh users can also purchase MacABEL in a package with Capilano's schematic editor and simulator for $2995. Several of the PLD compilers in **Tables 1** and **2** are also available for workstations.



A waveform display *from the device simulator allows you to see how your PLD design will perform. (Photo courtesy Logical Devices Inc)*

Many vendors of workstation-based CAD and CAE products offer PLD compilers as part of their tool sets. Dazix's PLD Master incorporates Advanced Micro Devices' PALASM compiler and works with ABEL and ISDATA's LOG/iC. Intergraph's Synthesis Engineer Series includes multiple compilers such as custom versions of Data I/O's ABEL ($3000) and Minc's PLDesigner ($14,000). Mentor Graphics and Valid Logic Systems also offer PLD compilers based on PLDesigner. However, these CAE software companies don't just repackage and sell other companies' PLD compilers; they integrate the software into their CAE environments so that you can use the same entry methods and simulation tools for PLD design that you use to design other types of circuitry.

For example, Mentor's $14,900 PLDSynthesis package uses Minc's compiler, partitioning and fitting, algorithms, and its PLD libraries, but not its user interface. Instead, Mentor changed the compiler's user interface to conform with its Software Release 8.0 framework. Further, it connected its schematic editor, VHDL design tools, and Quicksim II simulator to the PLD compiler and thus integrated PLDSynthesis into the company's entire package of design tools. You can design a circuit board with Mentor's schematic editor and other design tools and define your PLDs within the context of your overall design using either Mentor's tools or Minc's text-based input methods. (Although it uses much of Minc's design, Mentor has deferred support for waveform entry until it develops a unified waveform editor for all of its CAE tools. Intergraph's version of Minc's compiler supports waveform entry.) Once you have designed all of your circuitry, you can verify the entire design's operation using Mentor's Quicksim II simulator.

Most PLD compilers include some sort of simulation capability. The simulators with the least capabilities accept input and output vectors that you create and simulate your logic equations (independent of the PLD you select) to ensure that the equations produce the results you expect. Vendors sometimes call these programs functional verifiers instead of simulators.

More complex simulators use a model of your target PLD to create a simulation that reproduces the behavior you specify. For this type of simulation, you specify the input vectors, and the simulator generates output vectors or waveforms. You check these results to see

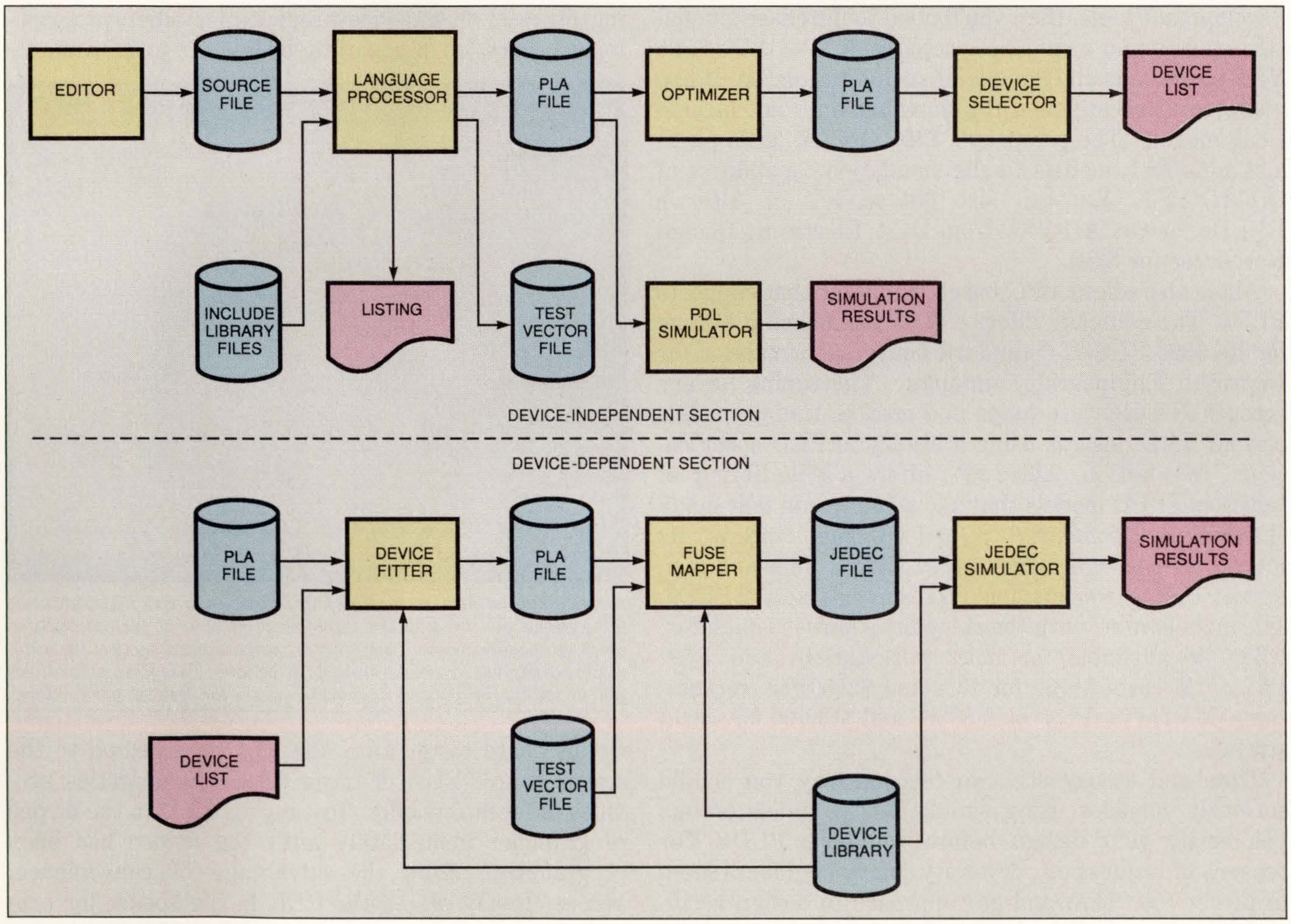


Fig 1—By splitting the latest version of its PLD compiler, *CUPL 4.0, into a device-independent design section and a device-specific fitting and mapping section, Data I/O has produced a tool that can accept design information created by other design tools. Because the front-end design section generates files commonly accepted by ASIC vendors, you can use this product to design ASICs as well as PLDs.*

if your design works as expected. Thus, you find out how the circuit will behave instead of guessing and then verifying your guess. However, you cannot perform these device-level simulations without models for the PLDs you're using.

If you're using an integrated design environment like Mentor's, then you already have a simulator on hand. All you need is the models. Logic Automation, a company that creates device models, has agreed to supply Mentor with device models for all PLDs that PLDSynthesis supports. If you're using PC-based PLD development tools, then you'll need to purchase simulation models and a simulator separately. OrCAD's $995 VST package is an example of such a simulator. It can model simple gates and flip-flops but does not include PLD models. The company's $495 OrCAD/MOD package adds PAL models to the simulation capabilities of OrCAD/VST. You can also get models of Altera's EPLDs for OrCAD/VST from DGA Electronic Design Resources for $395.

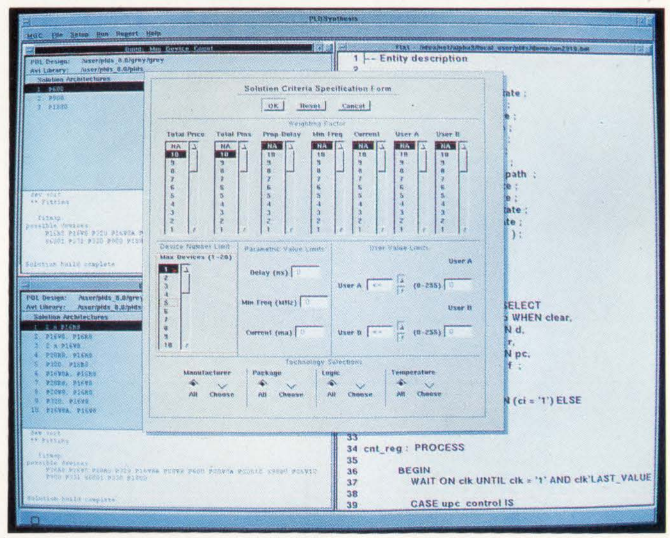
> One way or another, you need to select a device that has the physical resources necessary to implement your reduced equations.

Aldec also offers a PC-based simulator that supports PLDs. The company offers a $995 PLD timing library for its $995 SUSIE (Standard Universal Simulator for Improved Engineering) simulator. The timing library accepts JEDEC fuse maps and creates timing models of your PLD designs using a library of PLD specifications. In addition, Aldec also offers a $795 library of functional PLD models that allow you to run unit-delay simulations. Similarly, Quad Design offers its PAL2TIM package, which takes JEDEC files and generates timing models for PAL devices and EPLDs. The models work with the company's Motive simulator, which is available for both workstations and PCs. PAL2TIM costs $1760 for PCs and $2750 for workstations. Motive for PCs costs $8600 and $13,000 for workstations.

Time and money are two reasons why you should seriously consider using simulation. A simulator lets you verify your design before you burn PLDs. For reasons of laziness or perversity, many engineers seem to prefer the "blow-and-go" approach to design verification and ignore simulation. Their reward is a pile of useless devices, which are usually heaped on the lab bench in an unceremonious and unsightly pile. With 5-nsec PAL devices selling for more than $20 in small quantities and complex PLDs costing even more, this approach can become a costly habit in short order. The price for using a simulator for simple PLDs is usually no more than a few minutes to create some input vectors that will verify your design's logical operation. Even for complex PLDs that require many test vectors, you might still save time by using a simulator, because troubleshooting such complex parts also takes a bit of time.

If you've finished your design, verified that your design works by simulating it, and the prototype circuit is built and operating, you may think that your job is finished. Think again. The manufacturing department is going to build that design of yours, and you can help them by creating test programs for your PLDs and your board. Test software specifically created for PLDs can aid you in performing this task. **Table 4** lists a variety of software packages that create PLD test programs.

You can test PLDs at three points in the manufacturing process: on a device programmer when programming occurs; on a separate IC tester; and on an in-circuit board tester after the PLD is attached to the circuit board. Each of these three opportunities provides different benefits. Testing the PLD in the device programmer immediately after the device has been programmed offers the advantage of convenience. You've already placed the PLD in the socket for programming, so you need only allocate a few extra seconds for testing.



A specification form, *part of Mentor Graphics Corp's PLDSynthesis tool, allows you to rank the importance of several factors such as price, propagation delay, and current consumption so that the automatic partitioner can make suitable selections. This form also allows you to set maximum and minimum values for critical parameters.*

All device programmers verify that the PLD's fuses, EPROM cells, or EEPROM cells have been properly programmed. You don't need test vectors for this test. But if the PLD's programming circuits are faulty, your programmer can program the wrong fuse and be unable to detect that problem because the same on-chip circuitry that programs the device also reads and verifies the programmed fuse map. Chances are good that the faulty circuitry that caused the wrong fuse to blow will tell you that everything is OK when you read the fuse's status. This level of testing also does not check the PLD's input and output circuits, which are not used during programming and fuse-map verification. For the same reason, fuse-map testing cannot determine if you've programmed the right part. The fuse maps of PLDs such as the 16L8 and 16R8 look alike to the device programmer.

Most PLD programmers allow you to exercise a PLD's I/O circuitry through test vectors. The JEDEC 3A file format accommodates test vectors, so in one file you can transfer the test data and the programming data to the device programmer. PLD compilers allow you to incorporate your design-verification vectors into the PLD's fuse-map file for use by the device programmer. In addition, PLD test software can often accept JEDEC fuse maps and append additional test vectors to the JEDEC file for more complete tests.

However, device programmers generally cannot perform parametric testing. For example, they can't tell you if your 5-nsec PAL device really meets its 5-nsec propagation delay spec. They also cannot determine the timing skew between a PLD's outputs. For that sort of information, you need an IC tester. Because they're not dedicated to just PLDs, IC testers don't normally accept test vectors in the JEDEC 3A format. So if you're going to create test vectors for an IC tester, you'll need an appropriate piece of software. Similarly, if you want to test the PLD once it has been placed on a circuit board, you'll need to generate test vectors in the appropriate in-circuit board tester format. Testing PLDs on the circuit board provides the advantage of ensuring that the device still works after enduring manufacturing steps such as device placement, soldering, and cleaning.

Test for failure, not success

It's relatively simple to create a few test vectors that only test for a PLD's proper operation. You defined the device's function by designing it, so you know how it's supposed to work. However, creating a set of test vectors to test for all possible device faults can be a much harder problem, because you may need a lot of vectors. Yet you need to test for those faults,

Table 4—Representative automatic test-pattern-generation software for PLDs

Manufacturer	Product	Price	Tester(s) Supported	PLDs Supported (nonexhaustive)
Acugen Software	ATG 510	$495	PLD programmer	PALs
	ATG 520	$2495	PLD programmer	PALs plus the 22V10
	ATG 521	$3300	PLD programmer	PALs, GALs
	ATG 530	$4950	in-circuit tester	PALs, GALs
	ATG 531	$6950	in-circuit tester	PALs, GALs, EPLDs
	ATG 540	$4950	PLD programmer, IC tester	PALs, GALs
	ATG 541	$6950	PLD programmer, IC tester	PALs, GALs, EPLDs
	ATG 550	$6950	PLD programmer, IC tester, in-circuit tester	PALs, GALs, PEELs, FPLAs, FPLSs
	ATG 560	$9950	PLD programmer, IC tester in-circuit tester	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs
Data I/O	PLDtest Plus 2000	$1995	Device programmer	PALs
	PLDtest Plus 6000	$4995	IC tester	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs
Hewlett-Packard	74153A Advanced PLD Utilities	$4100	PLD programmer	PALs, GALs, FPLAs, FPLSs, EPLDs
ISDATA	LOG/iC Functional Verifier[1]	$995	PLD programmer	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs, Atmel ATV
Logical Devices	TESTPLA	$1995	PLD programmer	PALs, GALs, PEELs, FPLAs, FPLSs, EPLDs
Teradyne	Circuit Breaker	$50,000[2]	IC tester	PALs, GALs, FPLAs, FPLSs, EPLDs

Notes: 1. The LOG/iC Functional Verifier is an optional module for ISDATA's LOG/iC PLD compiler.
2. Price includes a license for Teradyne's Lasar Version 6 simulator.

as they could cause your circuit to operate incorrectly. Unless you plan to make a career out of writing test vectors, you should consider purchasing test software that includes an automatic test-pattern generator. Several software products for creating PLD tests appear in **Table 4**.

PLD test software can start with the vectors you created to verify your design. Working with those test vectors, a fault grader can evaluate your design-verification vectors to determine how much fault coverage they provide. If your vectors can detect every possible fault in the device, you've achieved 100% fault coverage. More than likely, however, your test vectors will only exercise a small part of the PLD. An automatic

Manufacturers of PLD development software

For more information on PLD development software such as the products described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Accel Technologies Inc
6825 Flanders Dr
San Diego, CA 92121
(619) 554-1000
FAX (619) 554-1019
Circle No. 650

Acugen Software Inc
427-3 Amherst St
Nashua, NH 03063
(603) 891-1995
Circle No. 651

Adams-Macdonald Corp
800 Airport Rd
Monterey, CA 93940
(408) 373-3607
FAX (408) 373-3622
TLX 882141
Circle No. 652

Advanced Micro Devices Inc
Box 3453
Sunnyvale, CA 94088
(408) 732-2400
Circle No. 653

Aldec
3525 Old Conejo Rd, #111
Newbury Park, CA 91320
(805) 499-6867
FAX (805) 498-7945
TLX 239447
Circle No. 654

Altera Corp
3525 Monroe St
Santa Clara, CA 95051
(408) 984-2800
FAX (408) 248-6924
TLX 888496
Circle No. 655

Arctos Systems Corp
300 March Rd, 4th Floor
Kanata, Ontario
Canada K2K 2E2
(613) 591-3084
Circle No. 656

Atmel Corp
2125 O'Nel Dr
San Jose, CA 95131
(408) 441-0311
FAX (408) 436-4200
Circle No. 657

Bytek Corp
508 NW 77th St
Boca Raton, FL 33487
(407) 994-3520
FAX (407) 994-3615
Circle No. 658

Capilano Computing Systems Ltd
501-1168 Hamilton St
Vancouver, British Columbia
Canada V6B 2S2
(604) 669-6343
Circle No. 659

Cypress Semiconductor Corp
3901 N First St
San Jose, CA 95134
(408) 943-2600
FAX (408) 943-2741
TLX 821032
Circle No. 660

Data I/O Corp
Box 97046
Redmond, WA 98073
(206) 881-6444
FAX (206) 882-1043
TLX 152167
Circle No. 661

Dazix
Box 7006
Mountain View, CA 94039
(415) 960-0123
FAX (415) 960-6933
TLX 858262
Circle No. 662

DGA Electronic Design Resources
155 West St
Wilmington, MA 01887
(617) 935-3001
FAX (617) 270-3723
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Exel Microelectronics Inc
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Semiconductor Div
2300 Buckskin Rd
Pocatello, ID 83201
(208) 233-4690
Circle No. 665

Hewlett-Packard Co
Customer Information Center
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Bldg 49AW
Cupertino, CA 95014
(800) 752-0900
Circle No. 666

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(303) 460-0103
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Intel Corp
Box 58065
Santa Clara, CA 95052
(408) 765-8080
Circle No. 668

Intergraph Corp
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Huntsville, AL 35894
(205) 772-2000
FAX (205) 730-2461
TWX 810-726-2180
Circle No. 669

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test-pattern generator can take your test vectors as a seed and create additional vectors to make the test's fault coverage more complete. Automatic test-vector generators can develop test vectors without your verification vectors, but they'll perform more quickly if you give them those clues to your design's operation. Thus, you have yet another reason for using simulation and verification in the early design stages.

After power is applied to a PLD, it will be in an unknown state, which makes it difficult to test. If you can initialize the part, perhaps using a reset line, your test can proceed immediately. Otherwise, you'll have to somehow put the PLD into a known state. Many PLDs allow a tester to jam a value directly into its

Manufacturers of PLD development software *(continued)*

ISDATA Inc
800 Airport Rd
Monterey, CA 93940
(408) 373-7359
FAX (408) 373-3622
Circle No. 671

ISDATA GmbH
Haid-und-Neu-Strasse 7
D-7500 Karlsruhe
West Germany
Circle No. 672

Lattice Semiconductor Corp
Box 2500
Portland, OR 97208
(503) 681-0118
FAX (503) 681-3037
TLX 277338
Circle No. 673

Logic Automation Inc
19545 NW Von Neumann Dr
Beaverton, OR 97006
(503) 690-6900
Circle No. 674

Logical Devices Inc
1201 NW 65th Pl
Fort Lauderdale, FL 33309
(305) 974-0967
FAX (305) 974-8531
TLX 383142
Circle No. 675

Mentor Graphics Corp
8500 SW Creekside Pl
Beaverton, OR 97005
(503) 626-7000
FAX (503) 626-1268
TLX 160577
Circle No. 676

Minc Inc
6755 Earl Dr, Suite 200
Colorado Springs, CO 80918
(719) 590-1155
FAX (719) 590-7330
Circle No. 677

National Semiconductor Corp
Box 58090
Santa Clara, CA 95052
(408) 721-5000
Circle No. 678

Omation Inc
801 Presidential Dr
Richardson, TX 75081
(214) 231-5167
FAX (214) 783-9072
Circle No. 679

OrCAD Systems Corp
3175 NW Aloclek Dr
Hillsboro, OR 97124
(503) 690-9881
FAX (503) 690-9891
TWX 910-240-2090
Circle No. 680

Phase Three Logic Inc
1600 NW 167th PL
Beaverton, OR 97006
(503) 645-0313
FAX (503) 645-0207
Circle No. 681

Pistohl Electronic Tool Co
22560 Alcalde Rd
Cupertino, CA 95014
(408) 255-2422
FAX (408) 255-2436
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Programmable Logic Technologies
Box 1567
Longmont, CO 80501
(303) 772-9059
FAX (303) 772-5617
Circle No. 683

Quad Design
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Camarillo, CA 93010
(805) 988-8250
FAX (805) 988-8259
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Signetics Co
Box 3409
Sunnyvale, CA 94088
(408) 991-2000
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321 Harrison Ave
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TWX 710-321-1055
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Texas Instruments Inc
Semiconductor Group (SC-971)
Box 809066
Dallas, TX 75380
(800) 232-3200 x700
Circle No. 687

Valid Logic Systems Inc
2820 Orchard Pkwy
San Jose, CA 95134
(408) 432-9400
Circle No. 688

Viewlogic Systems Inc
313 Boston Post Rd W
Marlboro, MA 01752
(508) 480-0881
FAX (508) 480-0882
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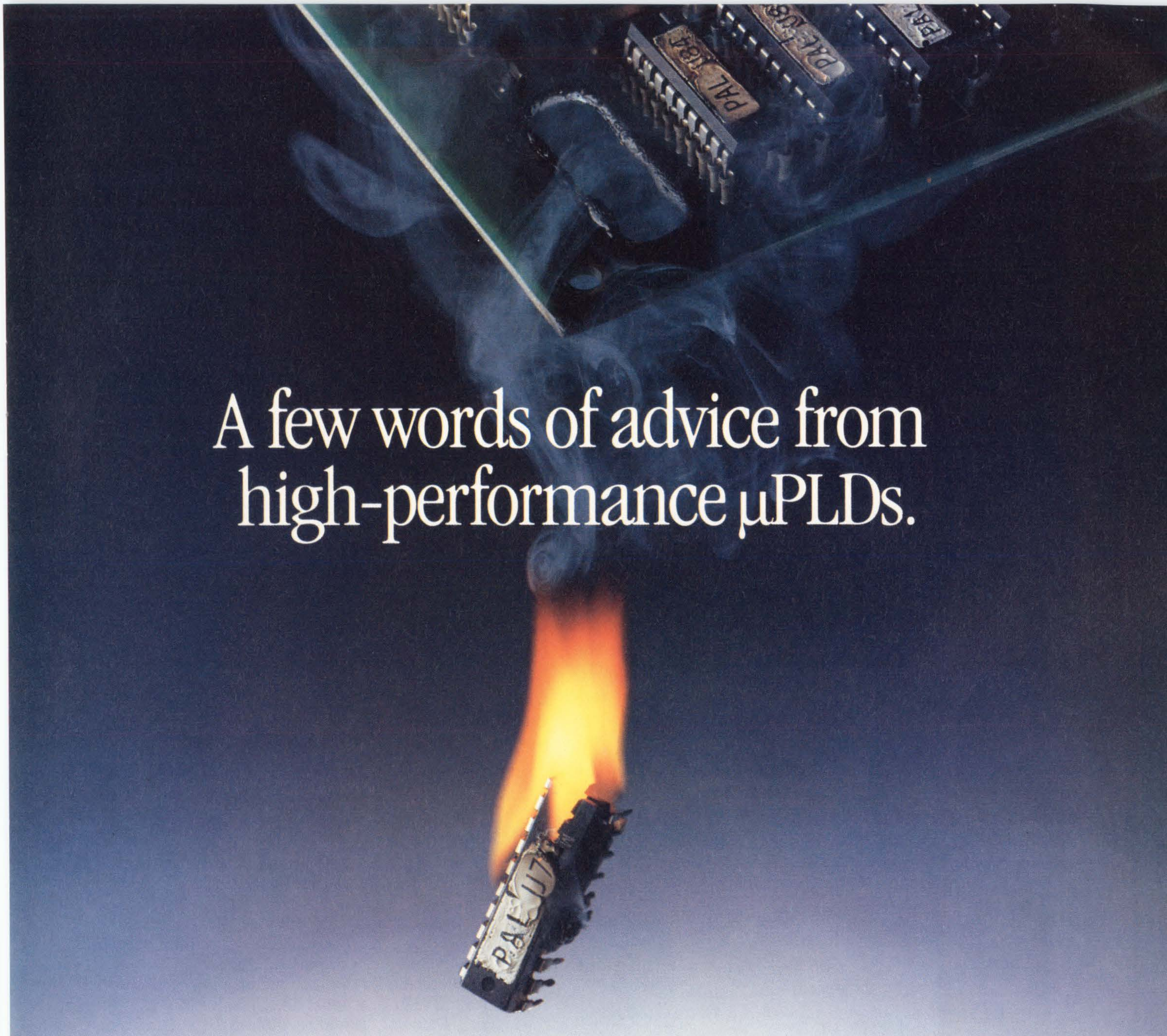

A few words of advice from high-performance µPLDs.

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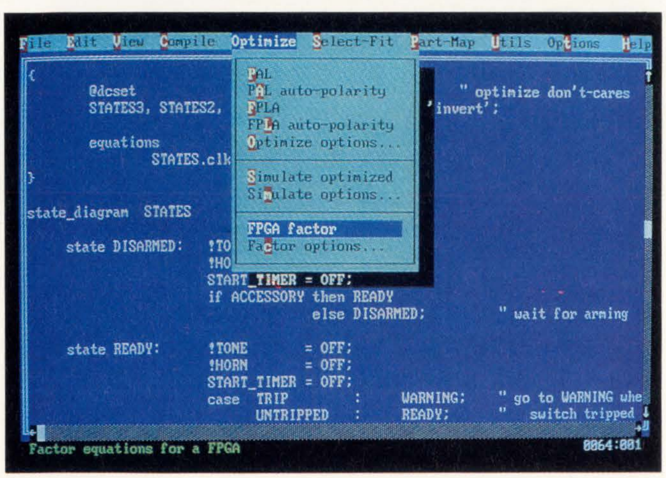
registers. This "preload" feature is usually activated by applying a "supervoltage"—substantially higher than 5V—to one of the PLD's pins. Consequently, you probably won't want to use the preload feature on a PLD once it's placed on a circuit board, because the supervoltage can easily destroy other circuitry on the board. However, programs that create vectors for IC testers can use a PLD's initialization or preload features to reduce the number of test vectors needed to test the device.

> Testing PLDs on the circuit board ensures that the device still works after enduring manufacturing steps such as device placement, soldering, and cleaning.

Once the PLD's registers are in a known state, the test can proceed. Be aware that PLDs with the same architecture but made by different manufacturers may use different preload algorithms. That situation may cause problems when your purchasing department switches PLD vendors, because you'll need a different test for the new PLDs. (This same problem arises for PLD programming as well. PLDs from different vendors, and even different-speed PLDs from the same vendor, use different programming algorithms.)

A test program can also place a PLD into a known state by applying a set of initialization vectors to the PLD's input pins that will force the device into a known state no matter what its initial state is. From there, the test can proceed just as it would if the device's state had been preloaded. This approach requires that the tester apply more vectors than the preload method but it may be the only alternative available to you unless you plan to run your PLD tests on an IC tester.



***Improved user interfaces** for PC-based PLD design tools mark the software products' transition from minimal, batch-oriented implementations to interactive programs that help you refine your design more efficiently. (Photo courtesy Data I/O Corp)*

You can certainly use just a compiler to create PLDs and leave design verification and device testing to the fates. Engineers and their employers take this low-ball approach all the time. One wonders what they're trying to save. They won't save time unless the engineers always create perfect designs the first time. (Those same people probably work crossword puzzles in ink.) Consequently, they don't save money, because time is more valuable than money in the electronics industry. An engineer's time, including overhead, can cost nearly $100/hour; the time to market is priceless. Even the most expensive development tools can quickly become bargains if you keep these realities in mind. EDN

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CIRCLE NO. 51

Knowledge of subtleties aids switched-capacitor filter design

Switched-capacitor filters are in essence sampled-data systems. By recognizing the effects—such as aliasing—these systems can have on the filtering process, you'll have a better understanding of your filter's anomalies. THD, clock jitter, and noise are other potential problems you need to recognize and take steps to avoid.

Richard Markell, *Linear Technology Inc*

Armed with a basic knowledge of switched-capacitor filter design—how to choose filter types and pole/zero locations, for example—you can achieve optimal performance from these filters by recognizing some of their subtleties. The most prominent effect of the sampled-data nature of switched-capacitor filters is the potential for aliasing and imaging of continuous-time signals. Also, recognizing system-level constraints such as clock feedthrough, clock jitter, noise, and filter sensitivity helps you maximize filter performance. If your filter is involved in spectrum analysis, THD is an important specification to evaluate. For any application, layout and power-supply features are critical for getting the best performance out of your switched-capacitor filter (see **box,** "Checklist helps filters work the first time.")

Because the switched-capacitor filter uses a switching capacitor to generate variable filter parameters, this type of filter is by definition a sampled-data device. Like all other such devices it is subject to aliasing and imaging. The mathematical explanation of these complex effects is the subject of many paragraphs in textbooks (**Ref 1**). However, the system designer needn't go through rigorous mathematics to get a meaningful handle on the subject. A series of spectrum-analyzer views displays theoretical and measured responses of both switched-capacitor filters and active RC filters.

Fig 1a shows the basic frequency-domain response for both a theoretical eighth-order elliptic filter and a sampled-data system. **Fig 1a**'s theoretical sampled-data system's response is the same for any sampled-data system, whether it's a sample-and-hold amplifier, a sampled A/D converter, or a switched-capacitor filter. The switched-capacitor filtering process—a form of sampling—effectively multiplies the theoretical elliptic-filter response by the sampled-data response in **Fig 1a**. The final result of this sampling and filtering process with an input frequency of f_{IN} is the filter response in **Fig 1b**. Notice the image-frequency components around the clock frequency, f_{CLK}. These components aren't the result of aliasing, but are an artifact of the nature of a sampled-data system.

Fig 2 shows two segments of the output spectrum of an 8-pole elliptic switched-capacitor test filter. This test filter's cutoff frequency is 500 Hz, and the ratio of the clock frequency to the cutoff frequency—f_{CLK}/f_{CUTOFF}—is 100:1. **Fig 2a** shows the response from 10 to 510 Hz to a 500-mV (−6 dBV) 100-Hz sine-wave input. **Fig 2a** displays the input signal plus the second harmonic that the filter introduced. The amplitude of the second harmonic is −75 dBV.

The most prominent effect of the sampled-data nature of switched-capacitor filters is the potential for aliasing and imaging of continuous-time signals.

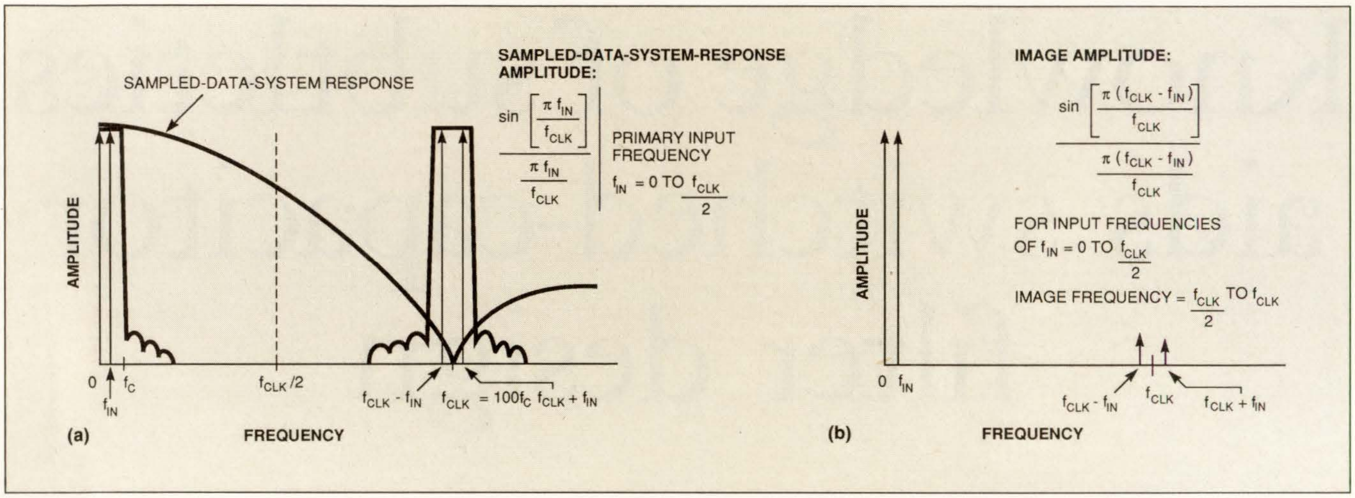


*Fig 1—Switched-capacitor filters are a type of sampled-data system. The overall switched-capacitor filter's response in **b** is the product of the theoretical sampled-data-system response and the theoretical elliptic filter's response in **a**. The image components that occur at multiples of the clock frequency result from the filter's sampling nature and aren't an anomaly of the filter.*

Fig 2b shows the output spectrum around 50 kHz, which is the clock or sampling frequency. The center signal results from clock feedthrough, which is not affected by the sampled-data system's (sin x)/x response. This signal's level is about 890 μV rms. The other two signals are the images of the 100-Hz input frequency at about −55 dBV (−61 dBV − the input's −6 dBV) below the input signal. The amplitude of these signals is almost exactly as the theory predicts when you use the formula in **Fig 2a**.

These images may not be important if the clock frequency is much higher than the frequency band of interest. However, without prefiltering, aliasing can occur, and worse, it can cause out-of-band signals to show up in the passband. When using switched-capacitor filters, aliasing is something you need to take pains to prevent.

All sampled-data systems are prone to aliasing when

Checklist helps filters work the first time

Standard precautions can steer you clear of most problems when you're testing and using your switched-capacitor filters:

Utilize good breadboarding techniques. Avoid building your filters on protoboard or wire-wrap boards. Instead, build the filter on prototype pc boards or on a piece of double-sided copper-clad board. Treat your filter as an analog component more than a digital one. That is, take layout precautions so that the clock doesn't interfere with the operation of the analog parts of the circuit. Even though your input frequency may be in the kilohertz range, you should follow RF layout techniques.

Use a linear power supply. If this is impossible, use a clean switcher. Properly bypass the supply.

Be prepared to deal with aliasing. Bandlimit! Pre- and post-filter if necessary.

Check your filter's time-and frequency-domain performance. Although not discussed in detail in this article, the ultimate response in the frequency domain is often not the ultimate response in the time domain and vice versa. Look at both responses on the bench before committing a filter to either a pc board or silicon.

Evaluate the relative importance of THD and S/N ratio. Understand the cases in which one spec limits the other.

Provide a stable, clean clock to the switched-capacitor filter. This will help you avoid problems caused by too much clock jitter.

input signals exceed one half the clock or sampling frequency. These aliasing effects lead to the ADC user's creed: Don't present signals to the converter at frequencies exceeding one half the clock frequency. If you ignore this warning, aliasing will occur. Remember also that the system can't tell if the signal is an alias or if it's real.

A good way to examine the aliasing phenomena is to imagine that the frequency spectrum folds around one half the clock frequency (the sampling frequency). The spectrum folds back on itself like a piece of paper with the fold representing the sampling frequency. Therefore, a 49.9-kHz input signal to a system whose clock frequency is 50 kHz appears folded back to 100 Hz. Similarly, a 30-kHz input appears folded back to 20 kHz.

The switched-capacitor filter passes or attenuates whatever signal you input to it, whether it's a real or aliased signal. Thus, an input signal of 49.9 kHz aliases into the previous filter's passband and appears at the filter's output unattenuated at 100 Hz. A spectrum plot for this input frequency is identical to the plot in **Fig 2a**. A 30-kHz input appears folded back to 20 kHz. However, 20 kHz is well out of the passband of this 500-Hz lowpass filter, and this signal is attenuated to the floor of the filter, about 75 dB.

When using switched-capacitor filters, remember that signals above one half the sampling frequency may fold over into your filter's passband. Without any prefiltering, these folded signals would be only slightly attenuated, as dictated by the (sin x)/x response. As a result, the filter passes signals between 0 and 500 Hz, whether they're real or aliased signals, without attenuating them. The filter attenuates signals at 30 kHz by approximately 75 dB. The moral of the aliasing story is that you must bandlimit your switched-capacitor filter's input signals. A simple RC filter will do.

Small size and other advantages

One of the great advantages of the switched-capacitor filter is the lack of discrete capacitors, which exhibit tolerance and stability limitations. An active RC filter with real-world capacitors that you design using theoretical capacitor values has problems with repeatability and stability. The switched-capacitor filter also has small errors in both the cutoff frequency, f_0, and Q, but they are easier to deal with than those of the active RC filter.

Manufacturing realities of the semiconductor business also affect the switched-capacitor filter design.

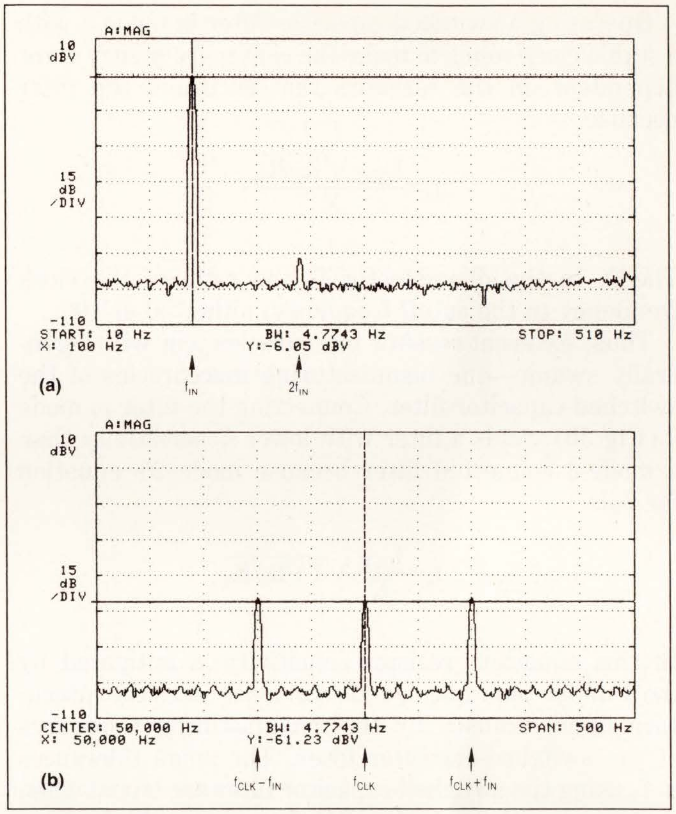


Fig 2—Spectrum-analyzer output plots display *the main signal and second harmonic* ***(a)*** *of an eighth-order switched-capacitor filter (LTC1064-1). Image and clock-feedthrough signals appear at the switched capacitor's clock frequency* ***(b)***.

Although this inaccuracy is much less than the inaccuracy of a comparable active RC filter, it does exist. Switched-capacitor filters are available from manufacturers with center frequency tolerances of generally 0.4 to 0.7%. Be aware that these numbers are only true if you use an accurate and stable clock.

In addition to the effects of the manufacturing process on the filter, the way you use filters also determines many of their characteristics. For instance, if you're using a universal switched-capacitor-filter building block that requires external resistors, the different ways of connecting those resistors (the modes) have various advantages and disadvantages. The state-variable biquad-circuit configuration, known as mode 3 **(Fig 3a)** allows you to achieve lowpass, bandpass, and highpass filter functions. This configuration also enables you to design high-Q filters that have low sensitivity to component tolerances. (For a strict mathematical analysis of the sensitivity of the state-variable biquad filter, see **Ref 2**.)

The moral of the aliasing story is that you must bandlimit your switched-capacitor filter's input signals. A simple RC filter will often do.

Operating a switched-capacitor filter in mode 3 with a stable clock tends to make the center-frequency error dependent on the resistors that surround the filter because

$$f_0=\frac{f_{CLK}\sqrt{R_2/R_4}}{X}.$$

The X in the denominator is the ratio of the clock frequency to the cutoff frequency, either 50 or 100.

Thus, external resistor inaccuracies join with—generally swamp—the manufacturing inaccuracies of the switched-capacitor filter. Connecting the filter in mode 2 (**Fig 3b**) yields a filter with lower f_0 sensitivity than a mode-3 connected filter because mode 2's equation for f_0 is

$$f_0=\frac{f_{CLK}}{X}\sqrt{1+R_2/R_4}.$$

In this equation, resistor sensitivity is mitigated by the 1 under the radical, and so in most cases the inaccuracy is only caused by the manufacturing tolerances of the switched-capacitor filter. The small tolerances in f_0 using the switched-capacitor filter are trivial when compared with an active RC filter. An elliptic filter built with resistors, capacitors, and op amps requires a lot of trimming. Changing the cutoff or center frequency is even more impractical.

One of the most common uses of filters is for antialiasing prior to A/D conversion. Antialiasing filters bandlimit the signal at the input to a DSP system. A critical concern is the filter's S/N ratio. If a filter has a maximum output swing of 2V rms and noise of 100 μV rms, it has an S/N ratio of 86 dB. A filter with these characteristics would certainly be a candidate for the antialiasing filter prior to a 14-bit A/D converter, a component which requires an S/N ratio of approximately 84 dB.

S/N ratio isn't the only important consideration, however, especially if you're trying to resolve every spectral component in a band of interest. THD is a measure of the unwanted harmonics that are introduced by nonlinearities in the system. Unfortunately, system and filter designers often ignore the subtleties of THD.

You can understand the effects of S/N ratio and THD, and how they inter-relate, by considering a system whose goal is to digitize a 4-kHz signal to 14 bits of accuracy. In this case, the filter has an S/N ratio of 86 dB, but let's suppose its THD is only −47 dB. Ultimately, both the 4-kHz signal and its harmonics will be digitized. Thus, the 4-kHz pure tone will come out looking like 4 kHz + 8 kHz + 12 kHz, and so on. The A/D converter will digitize these signals, thereby adding errors to the data-acquisition process. Ultimately, you won't be able to tell the real signals from the erroneous harmonics.

Fig 4 illustrates that THD in a real filter is often not as good as the S/N-ratio specification. This figure shows a THD-vs-input-amplitude plot of an 8-pole Butterworth lowpass filter. A second horizontal scale labels S/N ratio. The graph shows that the THD and S/N ratio of 1.5V-rms inputs are below −70 dB and −85

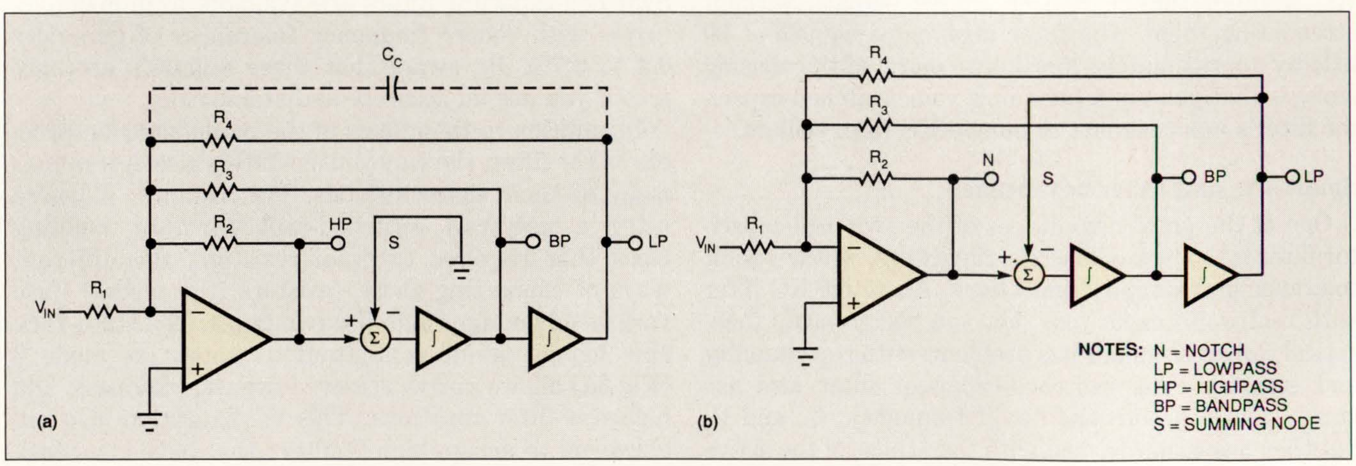
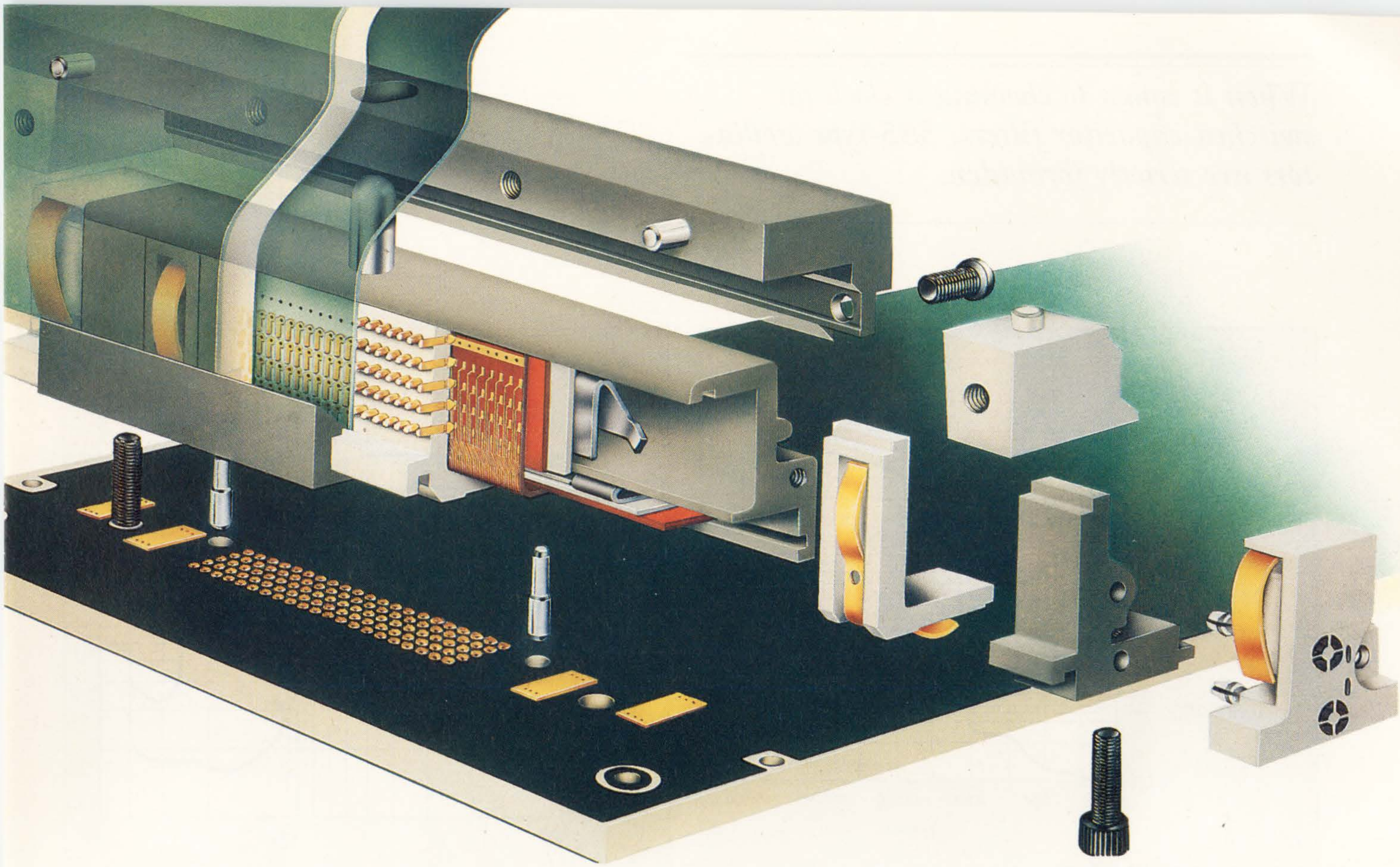


Fig 3—The major sources of a filter's error *can depend on the way you configure the filter. Connecting a universal filter building block in mode 3* ***(a)*** *will produce a filter whose errors stem mainly from external resistors. Filter errors connected in mode 2* ***(b)*** *depend more on the quality of the part itself.*



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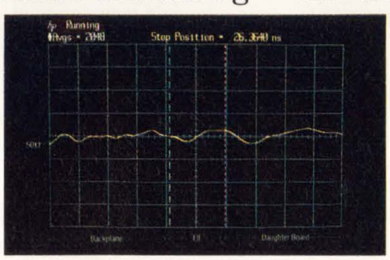

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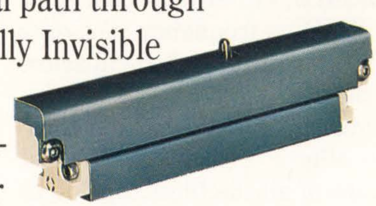

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When it comes to choosing a clock for switched-capacitor filters, 555-type oscillators are strictly forbidden.

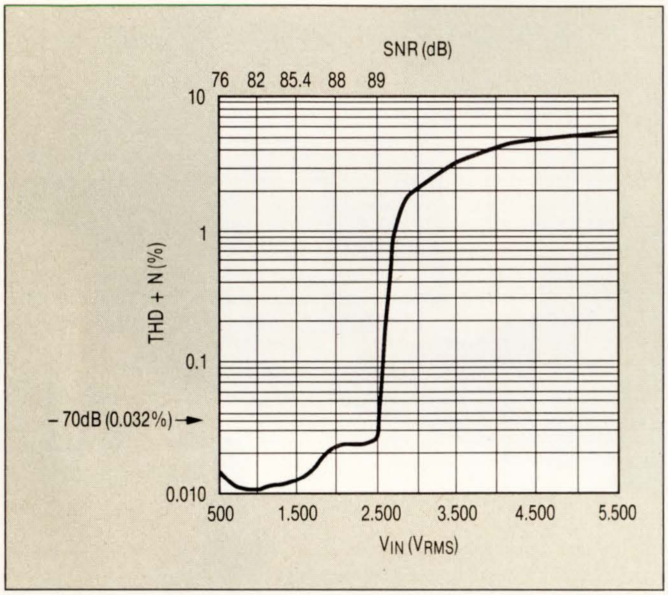

Fig 4—For spectrum-analysis applications, *THD is what ultimately limits digitization accuracy. Data from a real switched-capacitor filter reveals that, although the S/N ratio is 85 dB when $V_{IN}=1.5V_{RMS}$, THD is around −75 dB.*

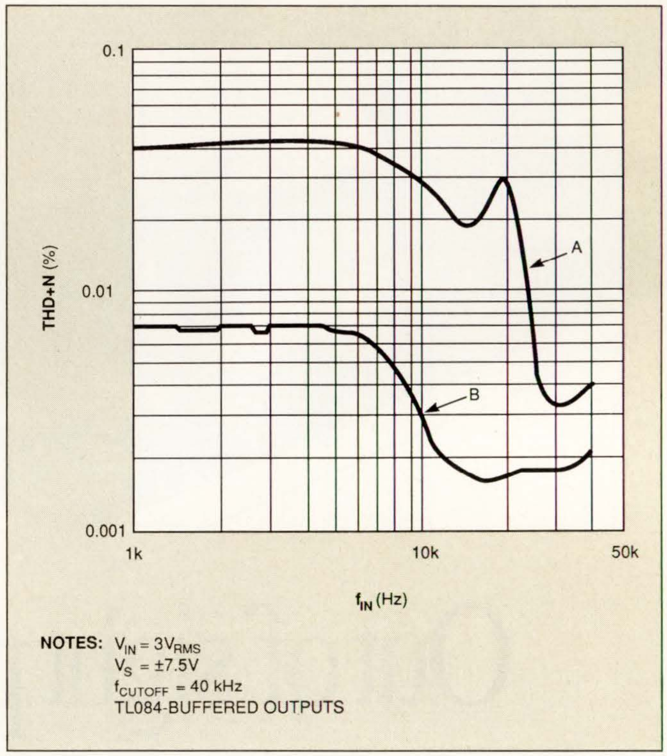

Fig 5—Switched-capacitor filters have many advantages *in size and price over active RC filters, but active RC filters have slightly better THD performance (trace **B**) than do switched-capacitor filters (trace **A**).*

dB, respectively. Thus, all the harmonics of the 4-kHz input signal are below −70 dB. However, your system's real digitization accuracy is now 70 dB and *not* the dynamic range of 85 dB.

THD generally limits the digitization accuracy of spectrum-analysis applications, not S/N ratio. If your system must be able to resolve multiple-frequency components, don't overlook THD's importance. It does no good to have a filter or any black box that has an 85-dB S/N ratio without the equivalent THD. Distortion is a complicated phenomenon, and its potential causes are not explicitly known. Some possible causes are the charge transfer inherent in the switching capacitors, the output drive, and the swing internal to the switched-capacitor filter.

THD varies with filter type

Many engineers who use filters generally assume that the THD of active RC filters is superior to that of switched-capacitor filters. Traditional filter textbooks seem to lack data on THD, either in a theoretical or a practical sense. The THD-vs-frequency plot data of the eighth-order elliptic RC and switched-capacitor filters **(Fig 5)** shows that the active RC filter has somewhat better THD performance than the switched-capacitor filter. (Note: The elliptic filters have almost the worst THD specifications of all the filter topologies because of their high-Q sections. Butterworth and Bessel filters have very good THD performance.) The performance of the active RC filter comes with the cost of board space: the active RC filter that produced this data includes 16 operational amplifiers, 31 resistors, and eight capacitors on a board that's about 2.5×6 in.

In many cases, you can optimize the THD of a filter by adjusting its design parameters. For example, you can make a large difference in an eighth-order filter's THD simply by changing the cascade order of the four second-order sections. This process is specialized, and data-sheet THD specifications may not reflect the best achievable performance. Bob Pease may be the Czar of Band Gaps **(Ref 3)**, but sometimes only a Czar of Filters can tweak the minimum THD from a filter circuit.

Noise in switched-capacitor filters has been on the decline since the invention of the device. Many devices currently have noise levels that compete with active RC filters. The noise of the switched-capacitor filter is nearly constant and independent of bandwidth. For

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Active RC filters aren't subject to aliasing, but they require more board area and many more components.

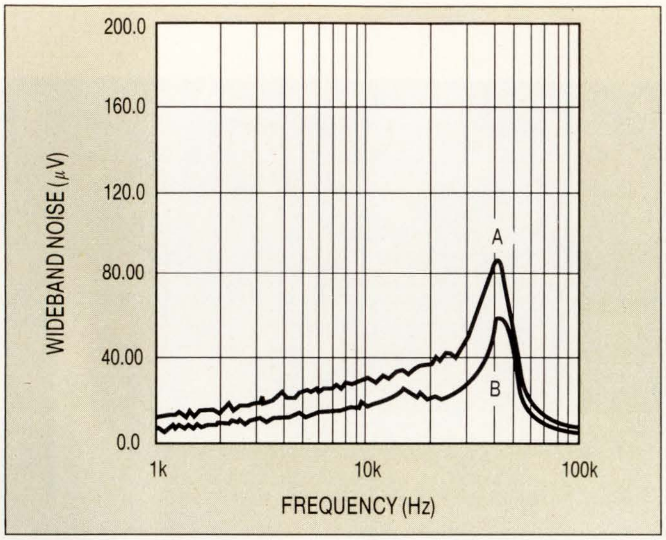

***Fig 6—The noise performance** of elliptic active RC filters (trace B) and switched-capacitor filters (trace A) is quite close.*

example, Linear Technology's LTC1064-2 Butterworth filter has approximately 80-μV rms noise from 1 Hz to 50 kHz (f_0 equal to 50 kHz). It also has 80-μV rms noise from 1 Hz to 10 kHz (f_0 equal to 10 kHz). Because the traditional active RC filter has noise specifications based on so many nV per $\sqrt{Hz}$, the switched-capacitor filter is a better competitor for active RC filters as the filter's cutoff frequency increases. **Fig 6** compares noise between an active RC filter and a switched-capacitor filter. Both curves show typical peaking at the corner frequency. The active RC filter has slightly better noise performance, but the two filters differ at most by 20 μV.

When it comes to bandpass filters, switched-capacitor filters have no better or worse performance than other filter types. **Fig 7a** is the frequency response of an eighth-order Bessel bandpass switched-capacitor filter. This filter has a Q of approximately 9, and a very linear phase response in the passband. The Bessel response is very useful when signal phase is important. Of particular interest to the present discussion is that the noise-band shape of this bandpass filter **(Fig 7b)** is identical to the curve in **Fig 7a**. This is not unusual since the bandpass filter is letting only the noise at a particular bandpass center frequency through the filter. Users of switched-capacitor filters sometimes assume the source of this noise is clock feedthrough, but this assumption is wrong. This noise is not the result of clock feedthrough, and it is not peculiar to the switched-capacitor filter. In an active RC filter, or even a passive LC bandpass filter with these characteristics, noise appears like a signal at the center frequency of

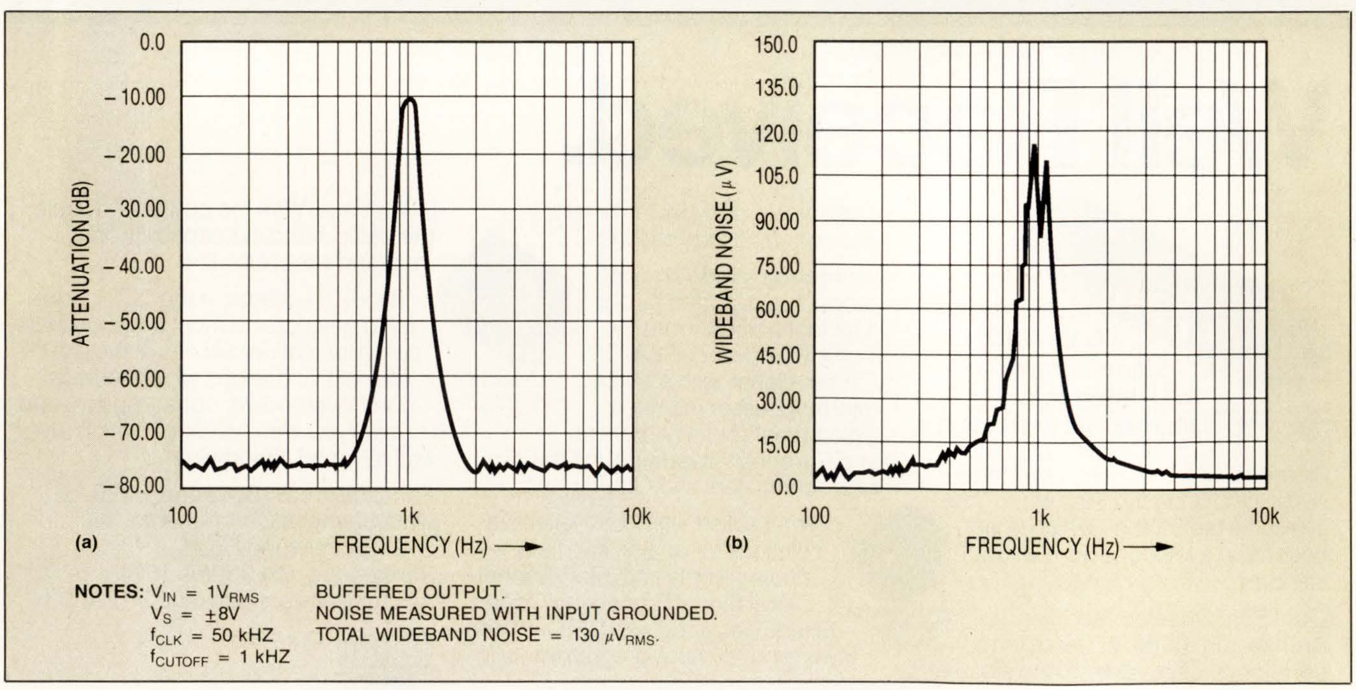

***Fig 7—Don't be surprised if you see noise peaks (b)** in the pass band of a highly selective, high-Q switched-capacitor bandpass filter **(a)**. Often erroneously attributed to switched-capacitor-filter clock feedthrough, all bandpass filter types, including active RC and passive RC types, exhibit noise responses that closely resemble the filter's frequency response.*

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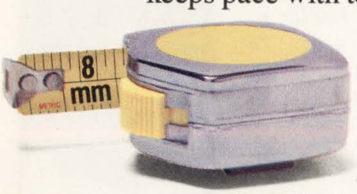

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Switched-capacitor filters are more analog than digital, and using analog-circuit layout techniques ensures proper performance.

the bandpass filter.

Unlike bandpass-filter noise, effects of the clock signal are unique to switched-capacitor filters. You can never take the act of clocking a switched-capacitor filter for granted. A clean, stable clock is required to obtain device performance commensurate with the data-sheet specifications. This requirement implies that 555-type oscillators are strictly forbidden. Often, what appears as insufficient stopband attenuation or excessive passband ripple is in fact the result of poor clocking of the switched-capacitor-filter device.

Fig 8 shows an eighth-order elliptic lowpass switched-capacitor filter that's set up to provide a cutoff frequency of 500 Hz. Modulating the clock (see the top curve measurement) simulates approximately 50% clock jitter. The stopband attenuation at 750 Hz is approximately 42 dB instead of the 68 dB specified by this filter's data sheet at 1.5 times the cutoff frequency. The second curve on the graph shows the situation when a good stable clock is used. Although the 50% jitter situation is somewhat ridiculous, **Fig** 8 provides a good base line as to why clock jitter must be minimized. Similar measurements of the wideband noise indicate the effect of clock jitter on the noise. The wideband noise from 10 Hz to 1 kHz rises when a jittery clock is used from 156 μV rms to 173 μV rms. This is an increase of approximately 11% due only to a poor clocking strategy.

Clock feedthrough has been greatly improved in the recent generation of switched-capacitor filters, but some users still want to further limit this anomaly. It is, of course, easier to postfilter clock feedthrough that is 100 times the cutoff frequency of the filter than for a clock-to-cutoff ratio of 50:1. The design aspects of minimizing clock feedthrough—choosing the clock-to-cutoff frequency ratio, for example—deserves your thought and attention.

Previously, **Fig 2b** showed −61 dB of clock feedthrough at 50 kHz. This is below 0 dB, which in this example was 2V rms. Clock feedthrough here is approximately 890 μV rms. Inserting a simple RC filter whose cutoff frequency is well outside the passband of the filter at the output of the switched-capacitor filter can reduce both the clock feedthrough and the imaging by at least a factor of 10. A simple RC post filter with values of 9.64 kΩ and 3300 pF reduces **Fig 2b**'s clock feedthrough to −82 dB below 1V rms or to 89 μV. If a clock-feedthrough component is out of the band of interest, additional filtering is unnecessary.

Switched-capacitor filters continue to evolve and progress. These filters closely pace the performance of active RC filters and offer the advantages of smaller size, better accuracy, and tunability. To best take advantage of these filters, you must observe good engineering practices and thoroughly understand the types of signals you're filtering, what signals you want to preserve, and finally how much spectral precision is necessary. **EDN**

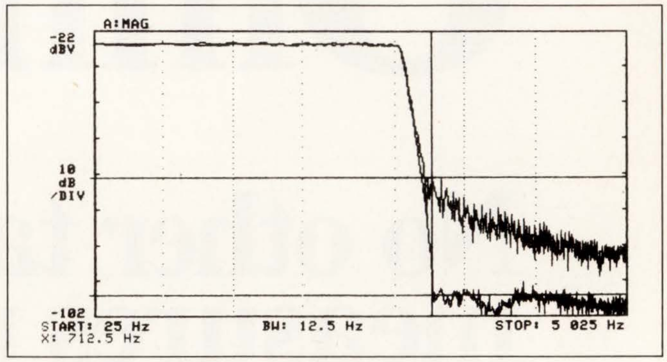

***Fig 8—Clock jitter degrades the performance** of a switched-capacitor filter. The upper trace shows the filter's performance with 50% clock jitter; the bottom trace shows the improvement with a jitter-free clock.*

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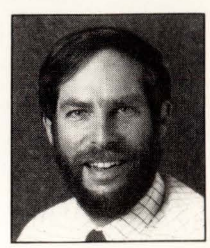
Author's biography



Richard Markell has been an applications manager at Linear Technology Corp (Milpitas, CA) for two years. In addition to writing articles and application notes, Richard recently helped develop switched-capacitor-filter design software. He has a BA in electro-optics from San Jose State University and is a member of the Audio Engineering Society. His hobbies include audio-circuit design, gardening, traveling, and hiking.

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

DESIGN NOTES

Number 38 in a series from Linear Technology Corporation August, 1990

Applications for a New Micropower, Low Charge Injection Analog Switch

Guy Hoover, William Rempfer, Jim Williams

With greater accuracy for both charge and voltage switching, the LTC201A is a superior replacement for the industry standard DG201A. In addition, the micropower LTC201A operates from a single 5V supply, and has lower on-resistance and faster switching speed. These improvements are critical to the operation of the following three circuits.

Micropower V-F Converter

Figure 1 shows a 100Hz to 1MHz voltage-to-frequency converter. This V-to-F operates from a single supply and draws only 90μA quiescent current, rising to 360μA at 1MHz. Linearity is 0.02% over a 100Hz to 1MHz range.

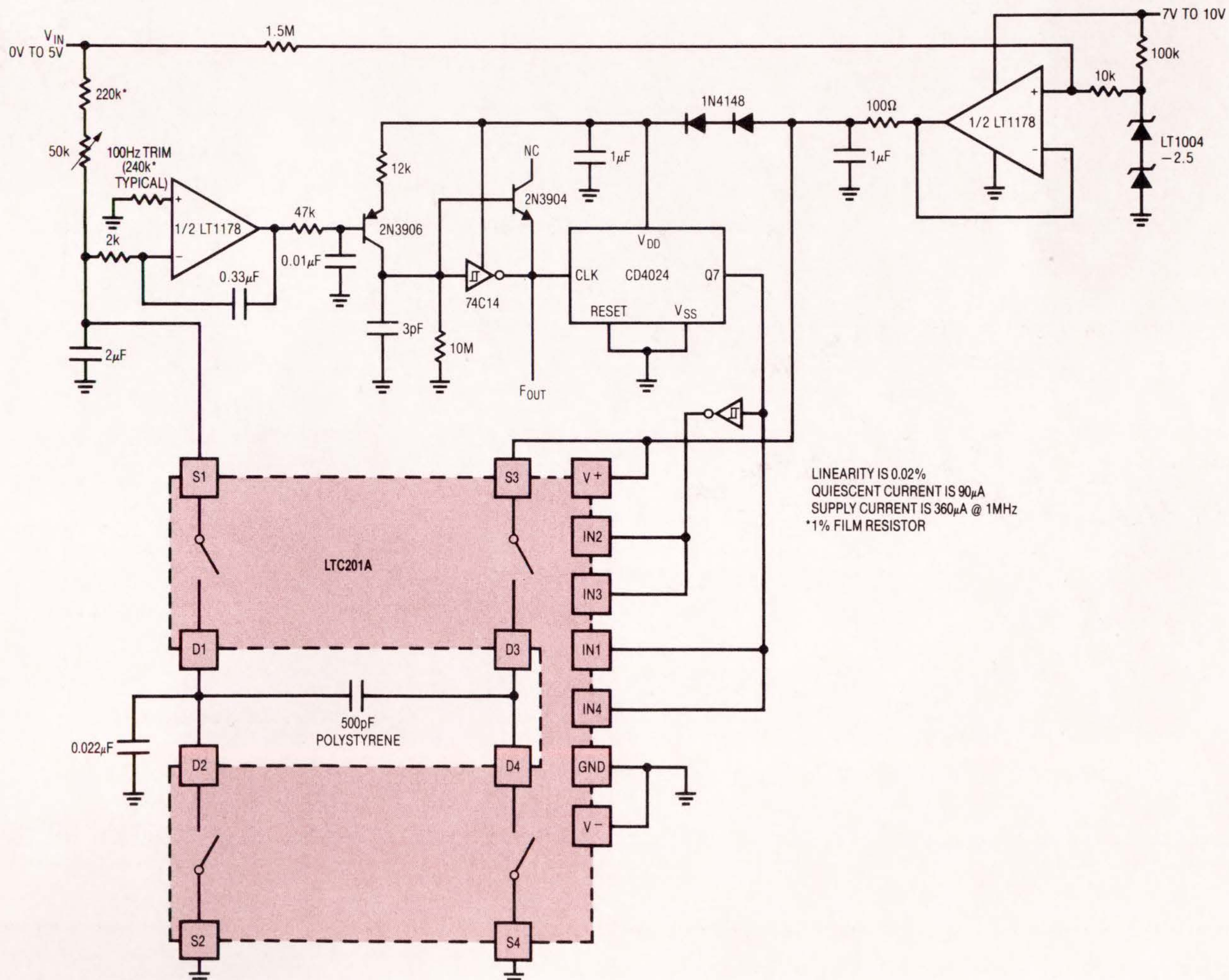


Figure 1. Micropower 100Hz to 1MHz V-to-F Converter

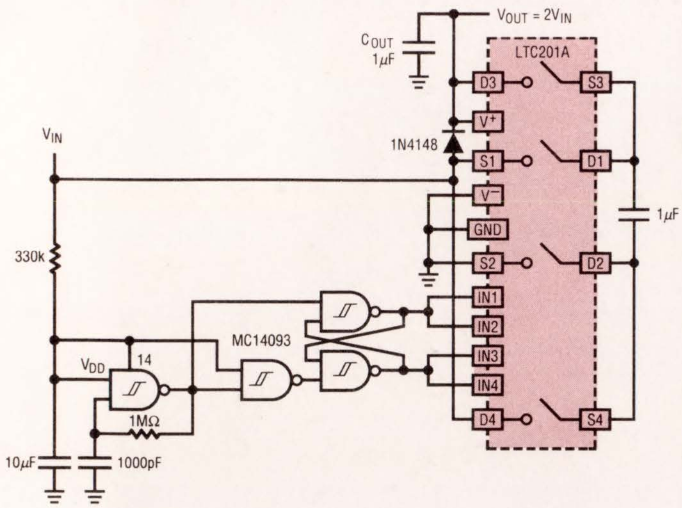


Figure 2. Micropower, 4.5V-15V Input, Voltage Doubler

The circuit consists of an oscillator, a servo amplifier and a charge pump. The oscillator's divided down output is expressed as current (charge per time) by the LTC201A-500pF combination. The input voltage is converted to current by the 220k trimmer pair. The amplifier controls the oscillator frequency to force the net value of the current into A1's summing point to zero.

The 1.5MΩ resistor between V_{IN} and the reference buffer amplifier sums a small input related voltage to the reference, improving linearity. The 0.022μF capacitor prevents excessive negative transitions at LTC201A D1-D2 pins. The series diodes in the oscillator divider supply line lower supply voltage, decreasing current consumption. The 10MΩ resistor at Q8's collector dominates node leakages ensuring low frequency operation by forcing Q8 to always source current.

Precision Voltage Doubler

The precision micropower voltage doubler of Figure 2 has an input voltage range of 4.5V to 15V. The low supply current of the LTC201A allows it to be powered directly from the input voltage. Total no load supply current of the circuit ranges from 20μA at V_{IN} = 4.5V to 130μA at V_{IN} = 15V. Output impedance is only 1.2kΩ at V_{IN} = 4.5V and reduced to 600Ω at V_{IN} = 15V. The accuracy of this circuit is better than 0.2% over the 4.5V to 15V input range.

The MC14093 is used to form an oscillator with complementary non-overlapping outputs. R1 and C1 determine the frequency of oscillation (roughly 1.2kHz at V_{IN} = 4.5V). The oscillator outputs drive two sets of switches in the LTC201A and ensure that one pair of switches shuts off before the other set turns on. C_{IN} is alternately charged to V_{IN} and then stacked on top of V_{IN} to charge C_{OUT}. R2 reduces the supply voltage to the MC14093 which keeps current drain low. The diode ensures latch-free power-up for any input rise time condition.

Quad 12-Bit Sample and Hold

Figure 3's sample and hold uses the low charge injection of the LTC201A combined with the low offset voltage of the LT1014 to produce a sample to hold offset of only 0.6mV. This makes it accurate enough for 12-bit applications. Acquisition time to 0.6mV is 20μs. Aperture time is 300ns (the off time of the LTC201A). Droop rate is 2mV/ms and is limited by the I_B of the LT1014. The input range is 3.5V to −5V with ±5V supplies.

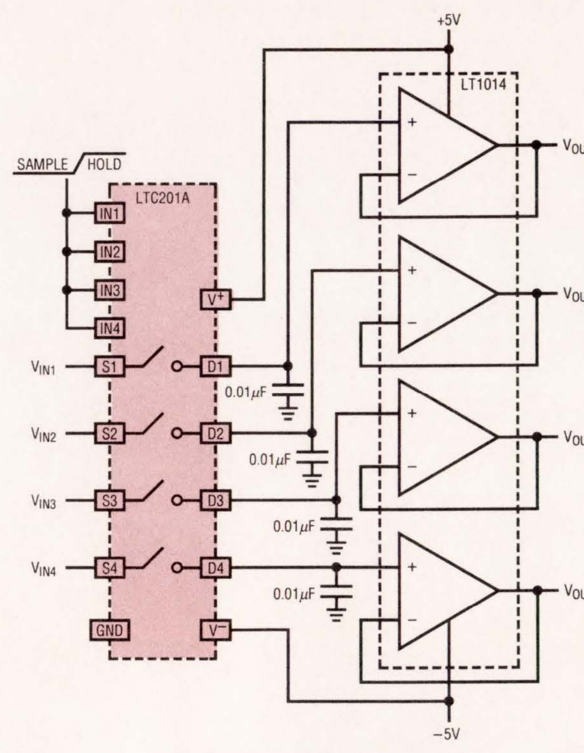


Figure 3. Quad 12-Bit Sample and Hold

For additional literature on LTC201A, call **(800) 637-5545.**
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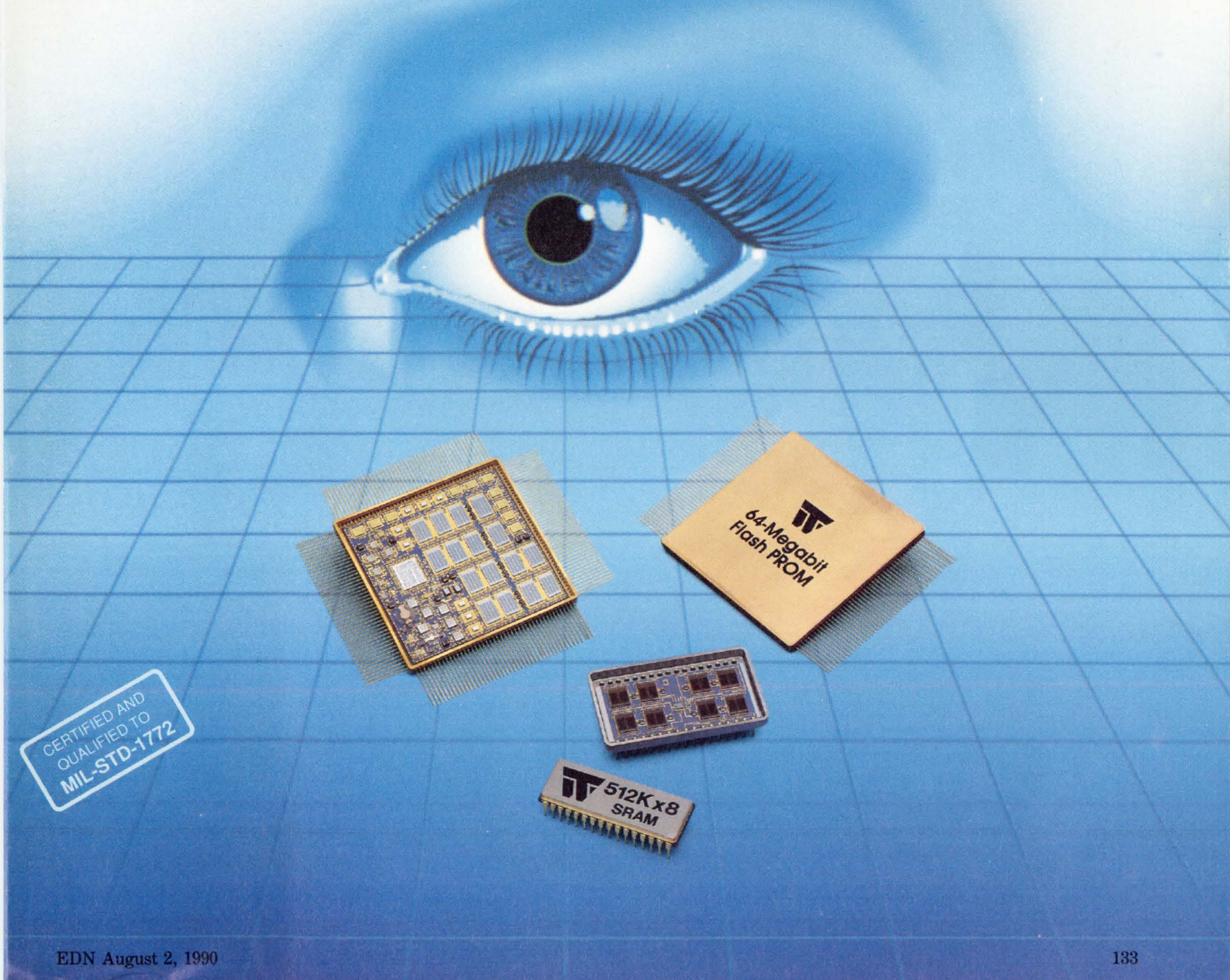

Passive network is totally resistive

Prayson Pate
BNR, Research Triangle Park, NC

The circuit in **Fig 1a** looks trivial, but it isn't. It can provide a resistive termination to a transmission line over a wide bandwidth—much wider than you can achieve with op amps. Further, you can extend the circuit to make multipole lowpass, highpass, and bandpass filters. Note that although the circuit resembles a tank circuit, it doesn't ring. In fact, ringing arising from component mismatch is small for reasonable component tolerances.

To calcuate the circuit's impedance, first let $Z_1 = R \| L$ and $Z_2 = R \| C$. If $\omega_1 = R/L$ and $\omega_2 = 1/RC$, then

$$Z_1 = R/(1 + \omega/\mathbf{j}\omega_1)$$

and

$$Z_2 = R/(1 + \mathbf{j}\omega_2/\omega).$$

Thus the circuit's input impedance equals $Z_1 + Z_2$, or

$$Z_{IN} = R(1 + (\mathbf{j}\omega/\omega_2 + \omega_1/\mathbf{j}\omega) + 1)/(1 + \mathbf{j}\omega/\omega_2 + \omega_1/\mathbf{j}\omega + \omega_1/\omega_2).$$

This expression reduces to simply R if $\omega_1 = \omega_2 = \omega_0$. You can calculate values for L and C simply:

$$L = \omega_0/R = 2\pi/F_0$$

and

$$C = 1/\omega_0 R = 1/2\pi F_0.$$

The circuit's transfer function is then:

$$H(\mathbf{j}\omega) = Z_2/Z_{IN} = 1/(1 + \mathbf{j}\omega/\omega_0),$$

which is the same transfer function as a simple LC lowpass filter.

You can realize more elaborate circuits by various combinations of the RL and RC subcircuits. Swapping the subcircuits in the circuit in **Fig 1a** yields a highpass circuit with the same pole. **Fig 1b** shows a 2-pole lowpass filter, and **Fig 1c** shows a bandpass filter. In **Figs 1b** and **1c**, the resistive input impedance of the second filter stage acts as the parallel resistor for the first stage. You can repeat this arrangement many times. The bandpass filter in **Fig 1c** does have the disadvantage of a 3-dB loss in its passband. EDN

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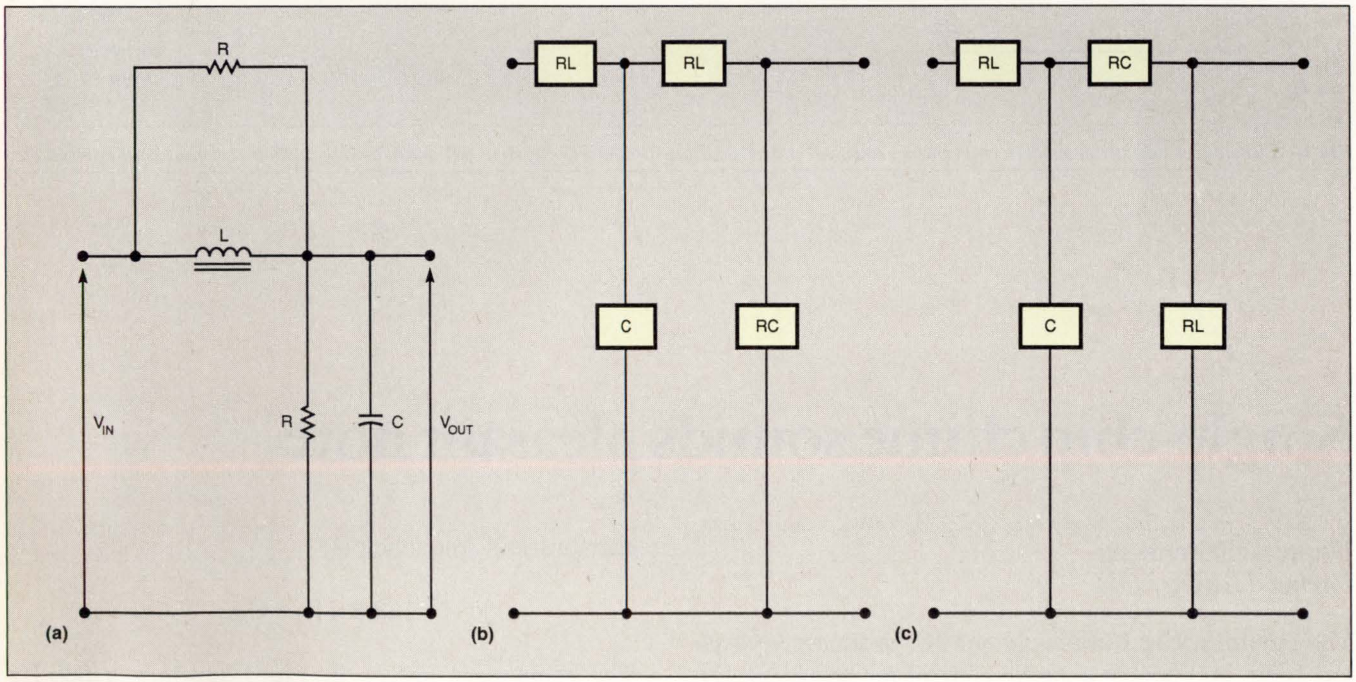

Fig 1—The simple circuit in a *provides resistive termination at all frequencies. Combining and swapping the circuit's elements yields the 2-pole lowpass filter in* ***b*** *and the bandpass filter in* ***c****.*

Watchdog timer sounds alarm

N Kannan
Centre for Development of Imaging Technology
Kerala, India

The watchdog timer in **Fig 1** contains a counter, IC_3, in addition to the usual retriggerable 555 timer, IC_1. The counter will sound an audible alarm if the watchdog timer trys to reset the μP a certain number of times—eight in the case of the counter in **Fig 1**. The alarm indicates that despite numerous resets, the system μP has failed to restart successfully, and the system is truly dead.

A second 555 timer, IC_2, resets the counter, IC_3, for the duration of a manual system restart. You could easily modify the design so that the system μP resets the counter. EDN

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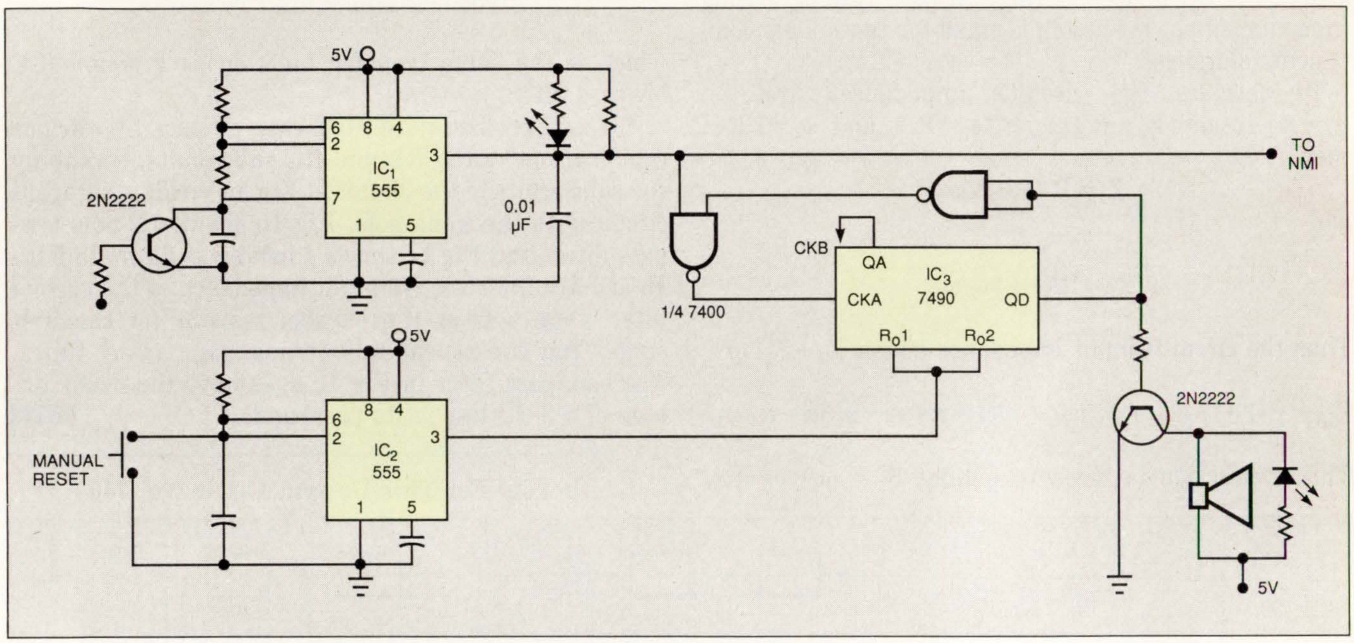

Fig 1—This watchdog timer counts *reset pulses and sounds an audible alarm if the system μP doesn't respond to a certain number of resets.*

Single-chip chime sounds pleasant note

Dennis Eichenberg
Parma Heights, OH

The circuit in **Fig 1** uses only one IC, produces a pleasant tone, and sports a single control for adjusting the tone's chiming rate. IC_{1A} and IC_{1B} form an astable multivibrator, which produces the circuit's basic tone. The multivibrator's frequency is:

$$f=1/(2.2\times R_1\times C_1).$$

The component values in **Fig 1** produce a 668-Hz tone. IC_{1C} buffers the multivibrator's output to the 8Ω speaker. Current-limiting resistor, R_2, determines

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100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
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the speaker's volume. R_2's minimum value is 220Ω.

IC_{1D} and IC_{1E} form an asymmetric, astable multivibrator, which adds a chime effect to the circuit's basic tone. The chime effect's frequency is:

$$t_{LO} = 1.1C_2(R_4 \| (R_5 + R_6))$$

$$t_{HI} = 1.1C_2(R_5 + R_6).$$

R_7 gives this rate multivibrator a slowly varying output signal to produce a pleasant decay for the chime effect. IC_{1F} is an inverting amplifier for the chime multivibrator. EDN

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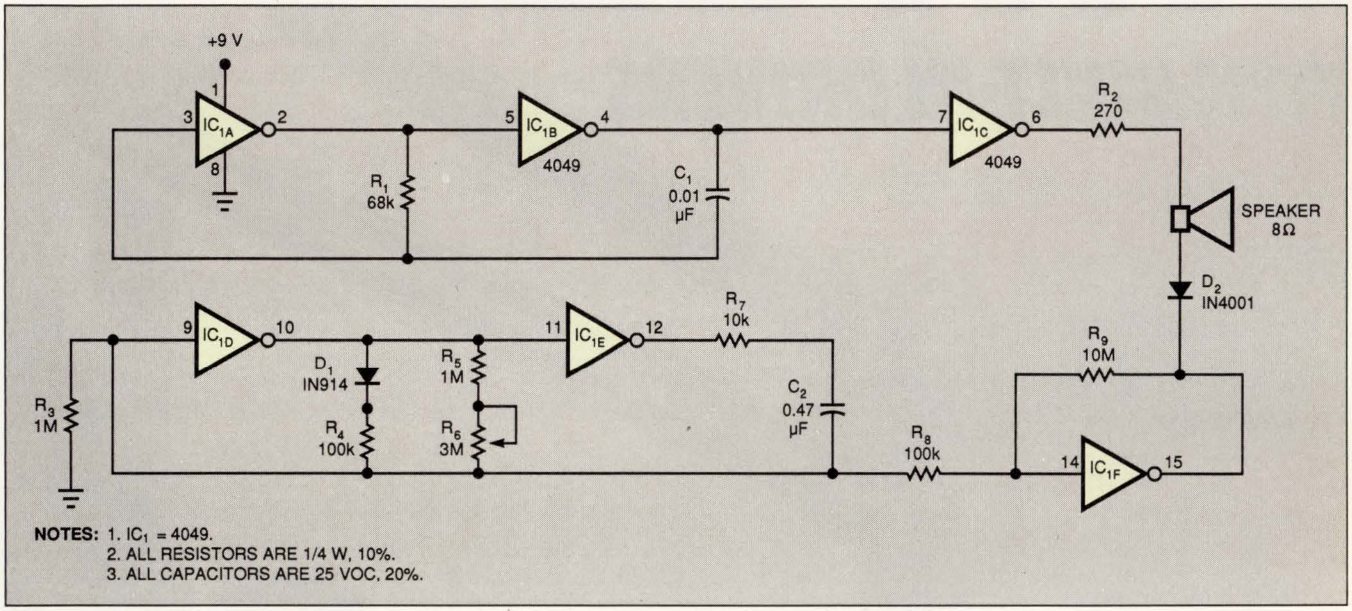

Fig 1—Using only one IC, *this dual multivibrator produces a pleasantly decaying, chime-like sound.*

Diodes stabilize CMOS circuits

Cezary Rudnicki
Institute of Electronics, Warsaw, Poland

The simple diode network in **Fig 1** can stabilize the voltage supplied to CMOS circuitry from a battery.

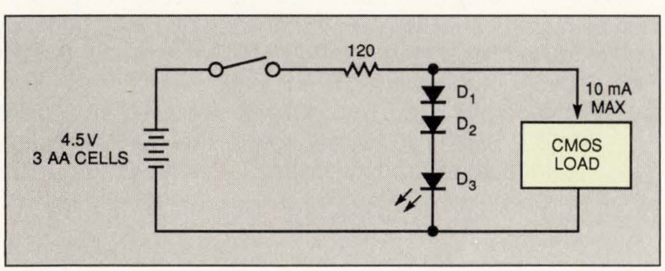

Fig 1—This simple diode network stabilizes *the supply voltage for low-power CMOS circuits running at 3V.*

Table 1—Voltage regulation

Input	4.5V	4V	3.5V	3.2V	3V	2.8V
Output	3.28V	3.21V	3.14V	3.05V	2.94V	2.8V
LED	on	on	on	on	on	off

D_1 and D_2 must have a combined forward-voltage drop of about 1.5V. And D_3 is an LED with a forward-voltage drop of about 1.7V. **Table 1** shows the network's output voltage as the battery's voltage declines. EDN

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Setup tests crystals

Jon Dunn
Bertan Associates, Hicksville, NY

Certain crystals aren't suitable for oscillator circuits that use logic gates (**Fig 1**). If a crystal has more than one series-resonant mode, such a circuit can oscillate indeterminately at one of several frequencies.

With the simple test setup in **Fig 2a**, you can quickly identify crystals with spurious modes on your scope (**Fig 2b**). If you identify unsuitable crystals, your crystal supplier may be able to change its manufacturing methods to eliminate the spurious modes. **EDN**

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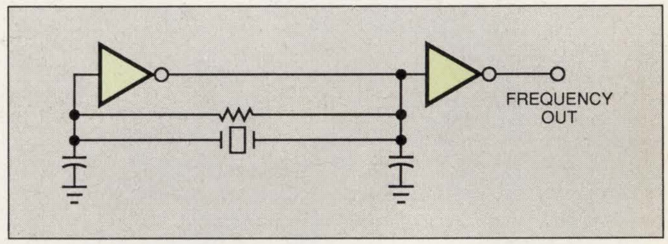

Fig 1—Simple oscillator circuits that employ logic gates *depend on the crystal's series-resonant mode, so a crystal that has more than one series-resonant mode is not suitable for such circuits.*

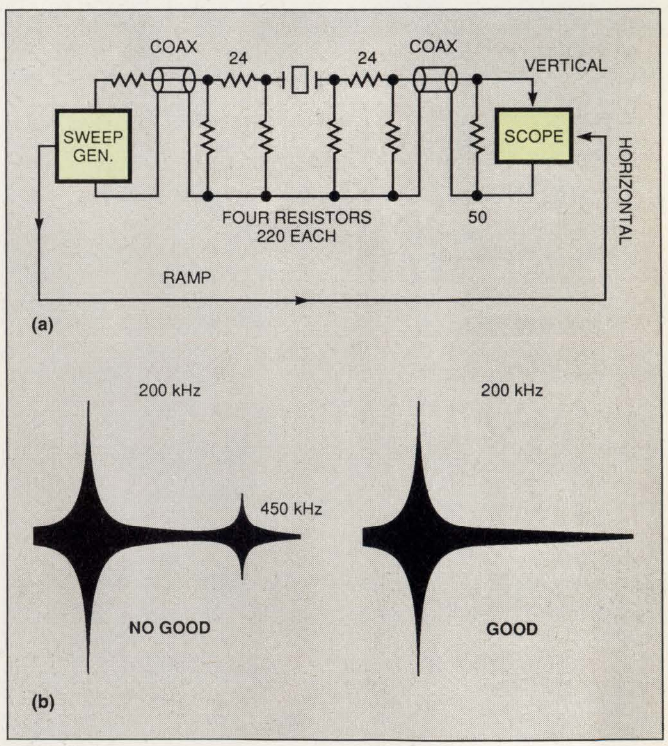

Fig 2—This simple test setup (a) *will quickly ferret out unsuitable crystals* ***(b)****.*