

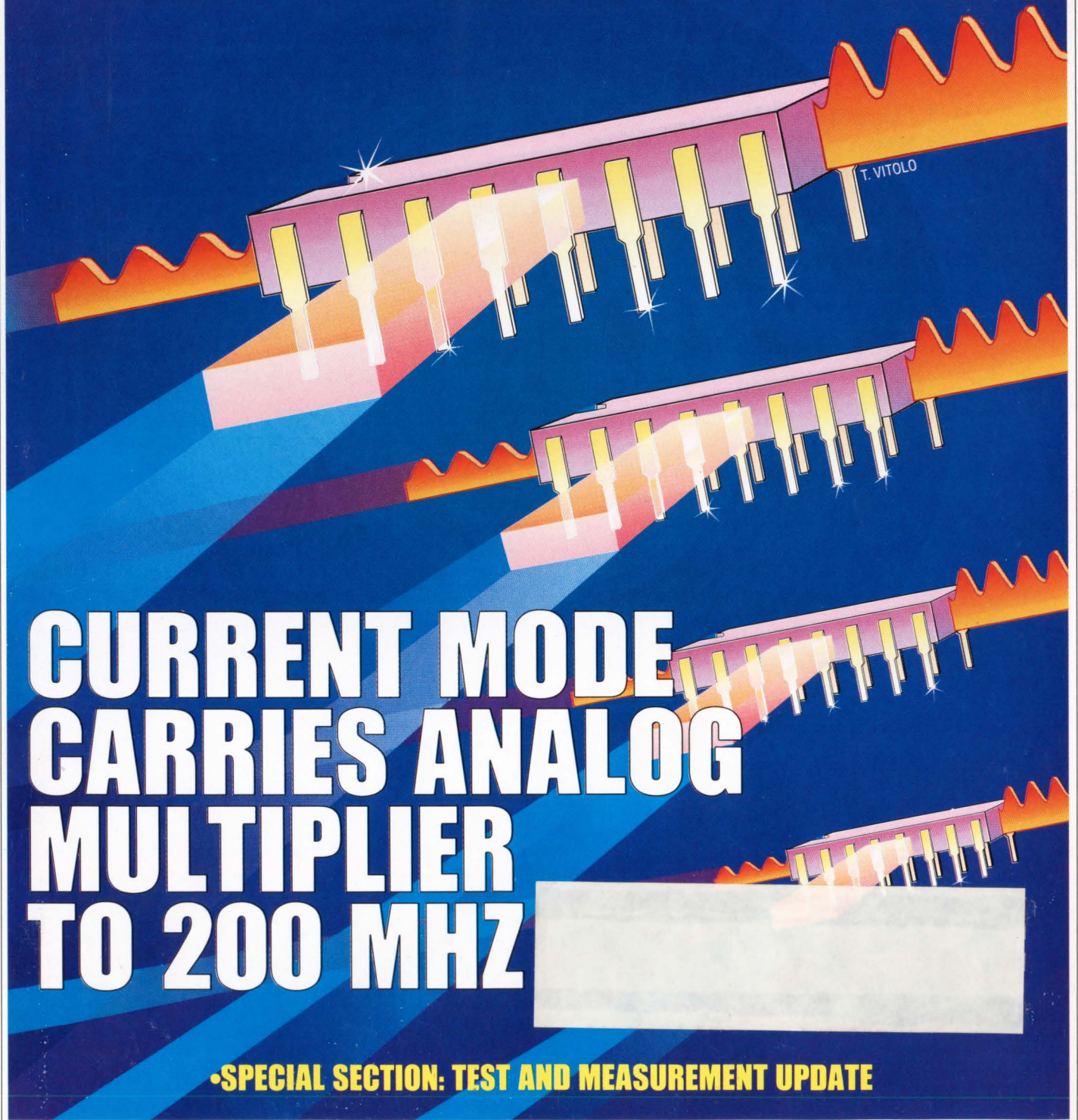
**SYNTHESIS TOOLS OFFER NEW CAPABILITIES**  
**SPECIAL REPORT: EDA TOOLS FOR MCM DESIGNS**

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

# **ELECTRONIC DESIGN**

A PENTON PUBLICATION U.S. \$5.00

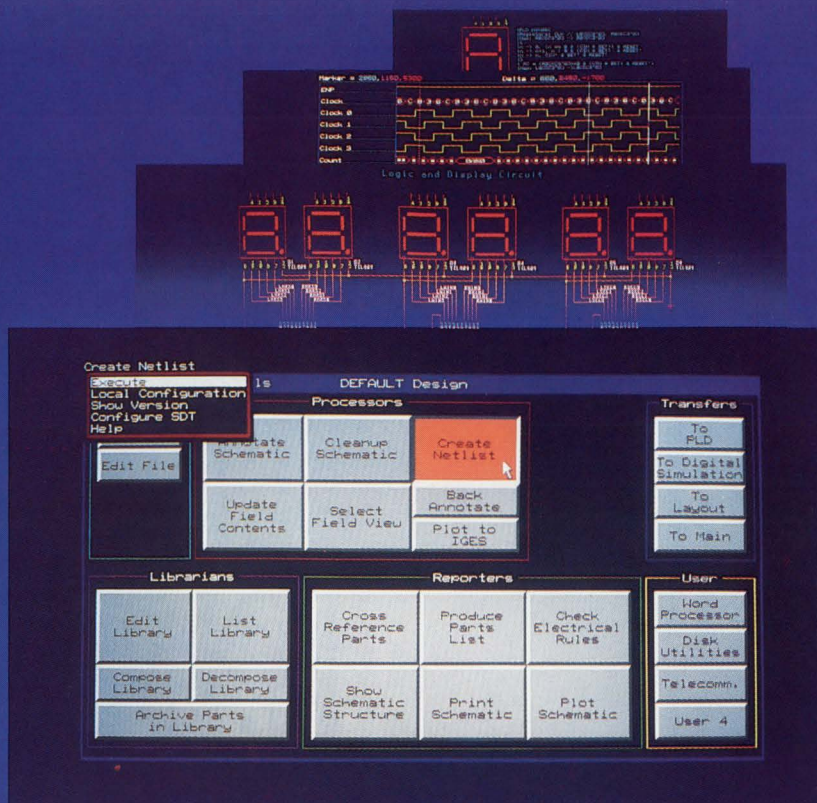
FEBRUARY 28, 1991



## **CURRENT MODE CARRIES ANALOG MULTIPLIER TO 200 MHZ**

**•SPECIAL SECTION: TEST AND MEASUREMENT UPDATE**

# OrCAD presents Release IV



## The limits are gone

OrCAD has introduced the greatest product upgrade in its history. Memory limits, design restrictions, even boundaries between products are all disappearing.

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- Expanded memory capabilities

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ESP is a graphical environment designed specifically for the electronic designer. Software tools appropriate for different stages in the design process are now linked together to form a seamless flow of information. This easy-to-use framework relieves the designer of time consuming tasks and the inconvenience of moving from one tool set to another. You can now spend more time productively designing.

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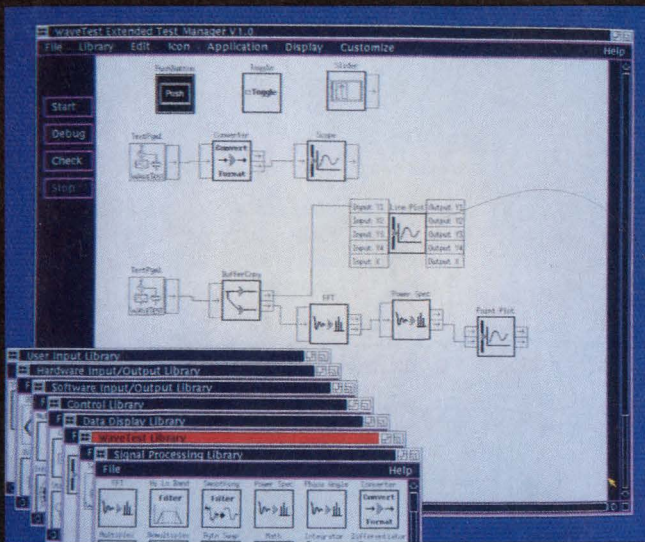
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**OrCAD** 

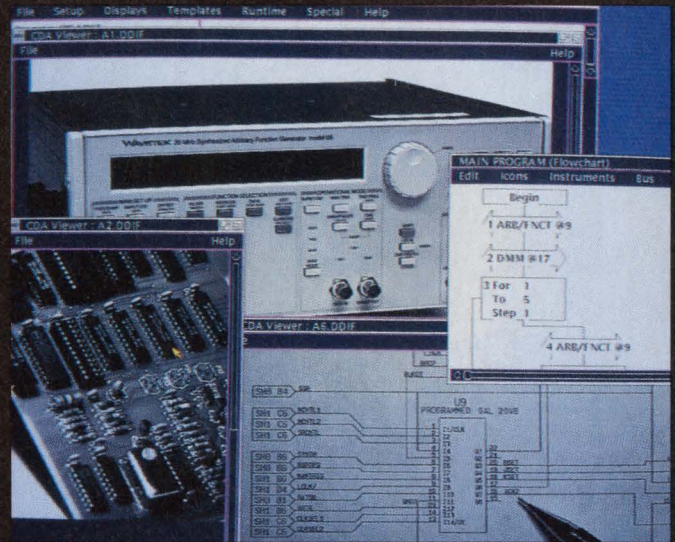
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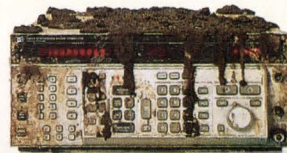
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**CIRCLE 164 FOR LITERATURE  
CIRCLE 165 FOR DEMONSTRATION**

**WAVETEK<sup>®</sup>**

Did you hear about the 74-pounder they  
caught in the Columbia River?





It worked without a snag.

This is a story about the one that got away. And then came back as reliably as ever.

In 1987, bandits stole four HP signal generators from a truck in Spokane, Washington. Luckily, police managed to recover three of them. But the last one disappeared without a trace.

Six months later, a man fishing the Columbia River hauled in a heavy metal box. Well, within a few days, we had the missing signal generator back. There was mud in every nook and cranny.

But rather than clean this catch, one of our Service Engineers decided to plug it in. To his surprise, the instrument emitted a signal. Even more remarkable, it met specifications.

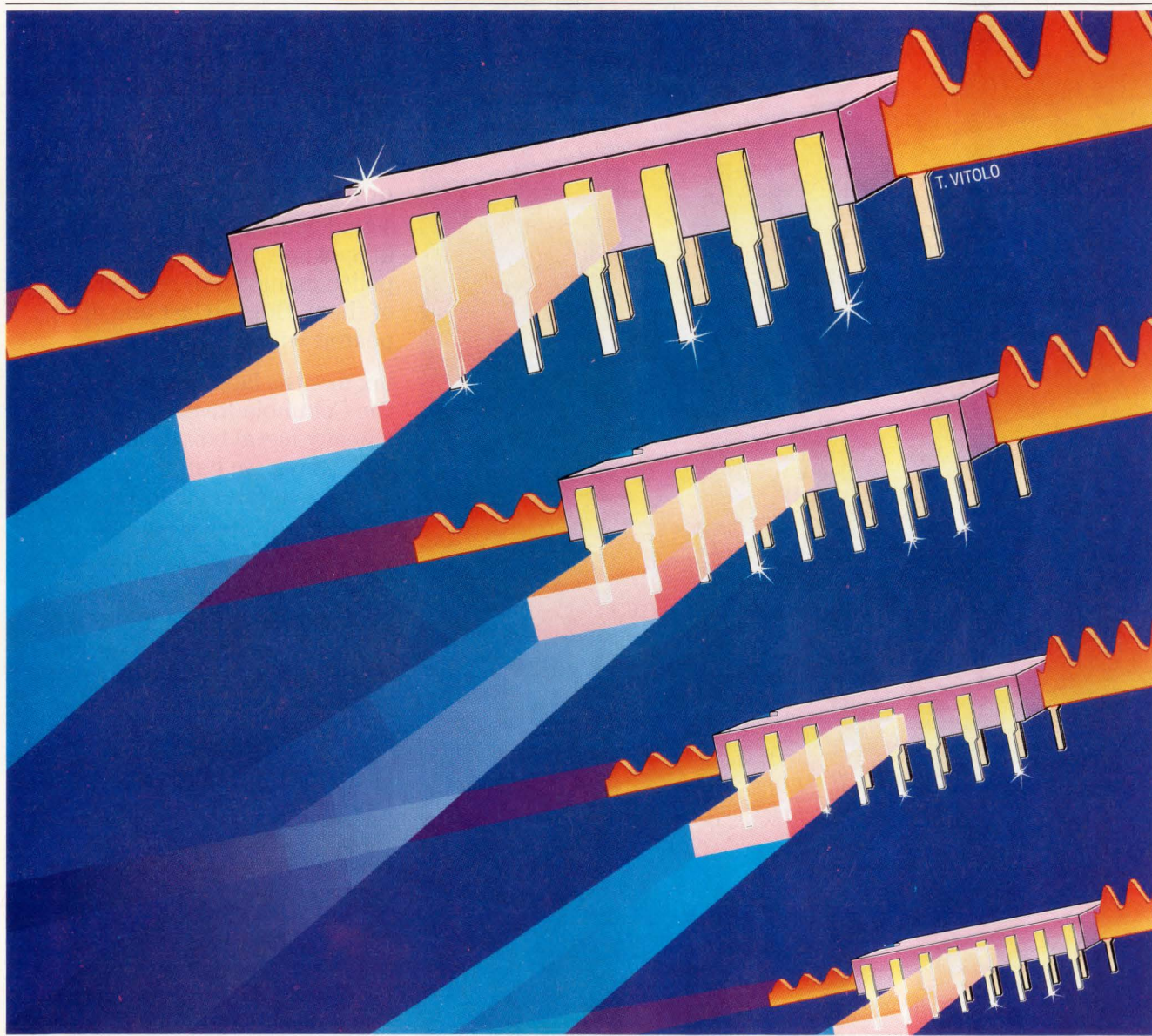
Stories like this underscore why HP rates highest for reliability among engineering managers. We're still not satisfied. In fact, in 1979 we started a Total Quality Control program to increase quality ten-fold in 10 years. We'll reach that goal this year.

It just goes to show you that when design and manufacturing productivity are at stake, there is no reliable substitute for HP. And that sometimes the best fish stories are actually true.

There is a better way.



# ELECTRONIC DESIGN



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Certificate of Merit  
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Jesse H. Neal Editorial  
Achievement Awards

Cover: Tony Vitolo

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- Building SCSI-based redundant disk arrays
- Special Section: Designing for PC systems
- Upgrading an 80386 system to use the i486
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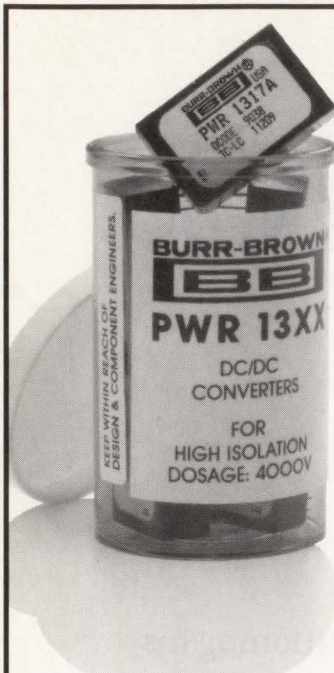
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CIRCLE 82

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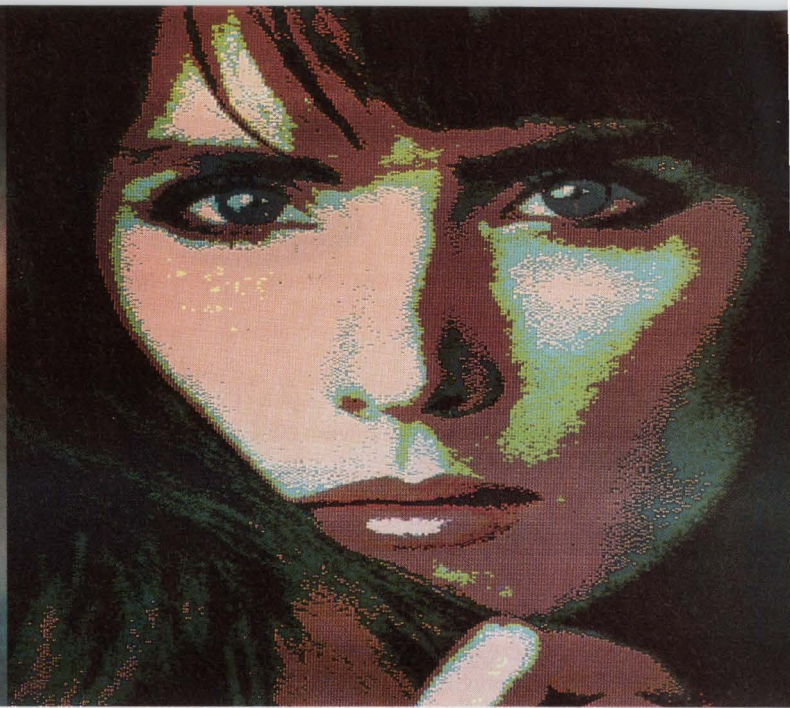
CIRCLE 137

8 ELECTRONIC DESIGN

FEBRUARY 28, 1991



Picture your flat panel display using Cirrus Logic controller chips. They actually add colors to your display capabilities for more realistic shading.



The same panel looks flat without our enhanced VGA capabilities. And it will lose face faster without our optimized power management system.

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Face it. The first thing everybody notices about your newest laptop is the display quality. Is it bright? Are the images clear and well modeled? Are the colors vivid?

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is lower than other solutions for longer battery operation.

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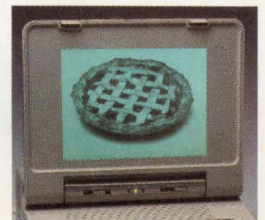
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Cirrus Logic Color LCD Interface Controller Bulletin



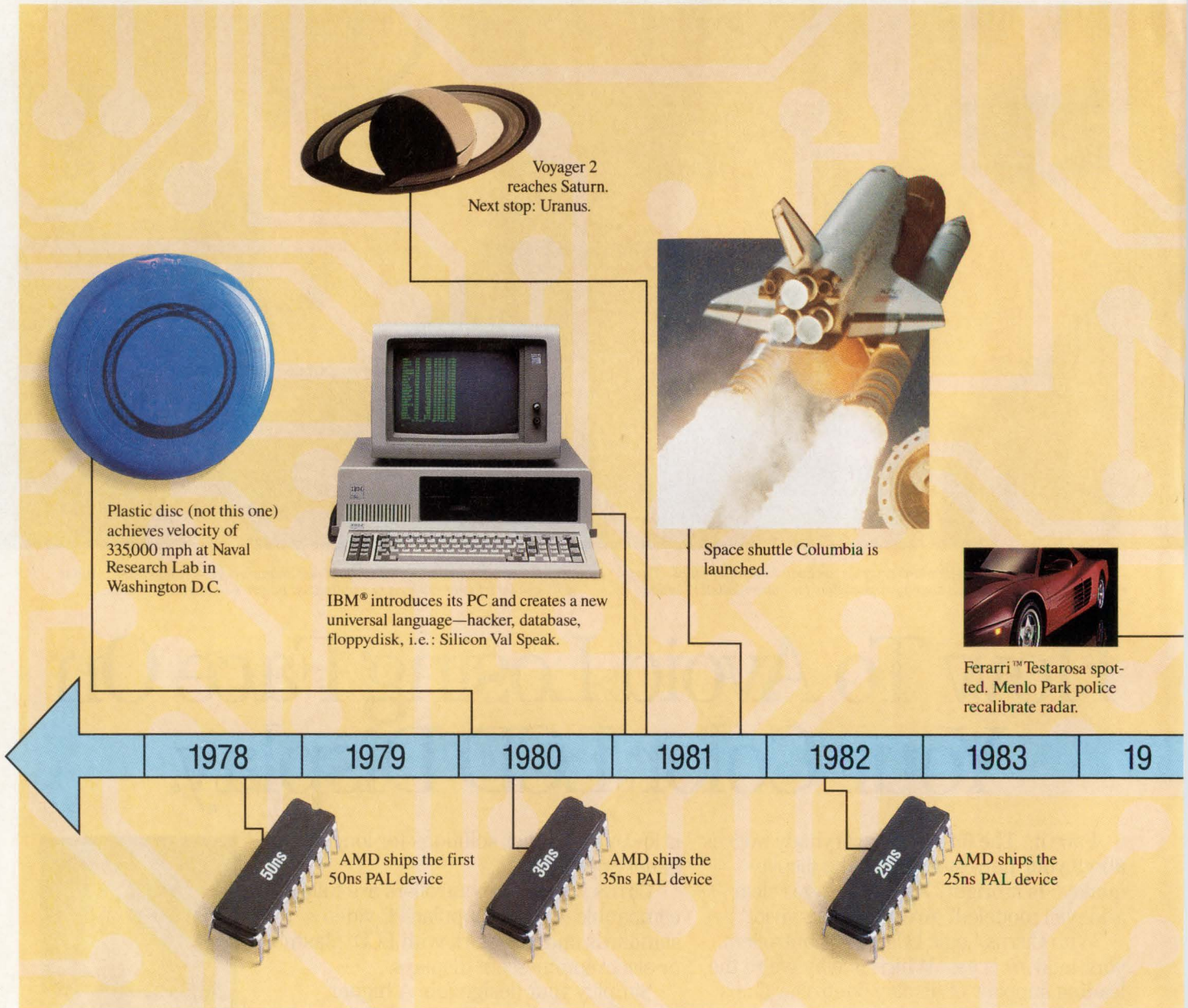
Cirrus Logic monochrome LCD controllers will also make everything from realistic scanned images to business charts look tastier.



CIRRUS LOGIC

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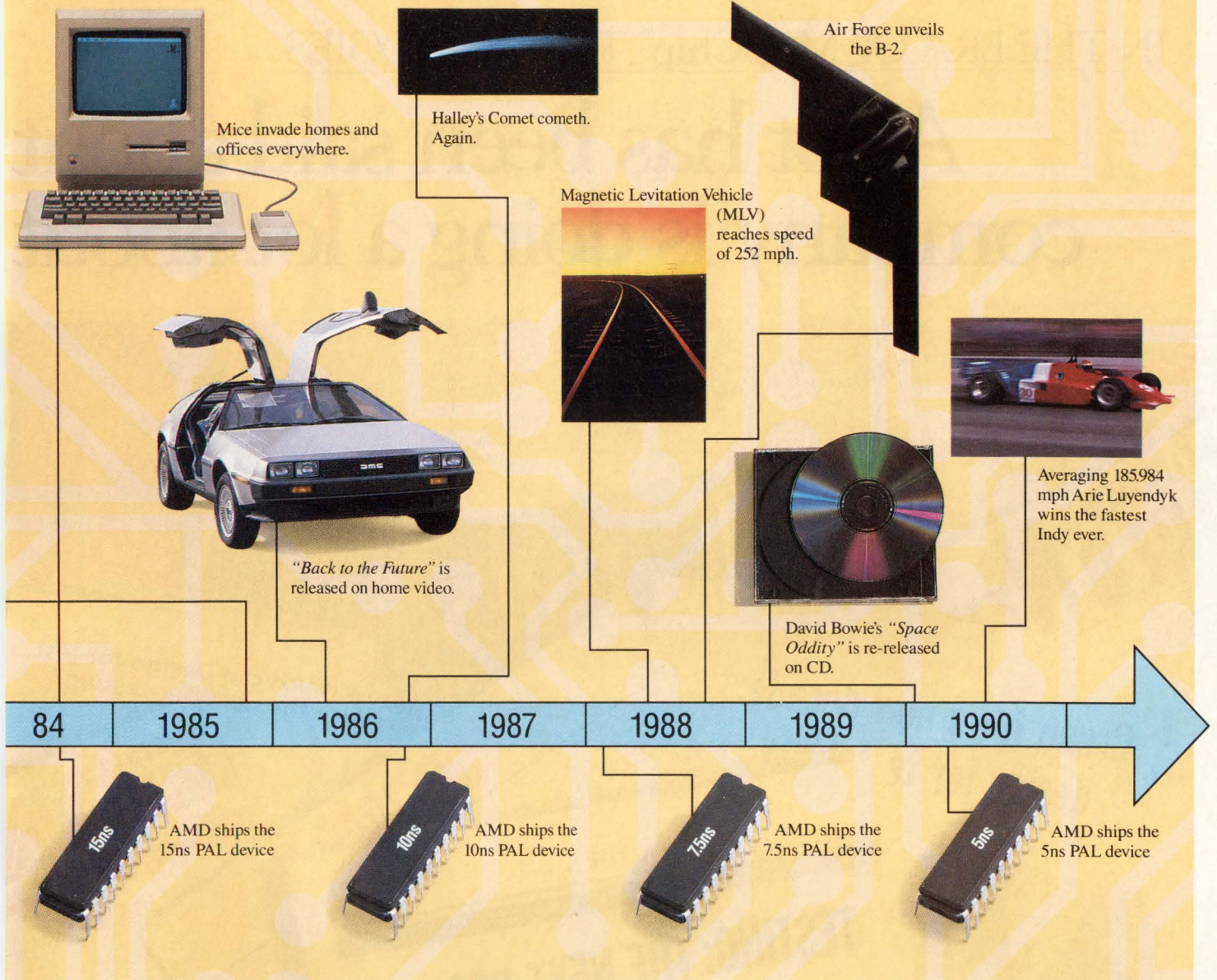
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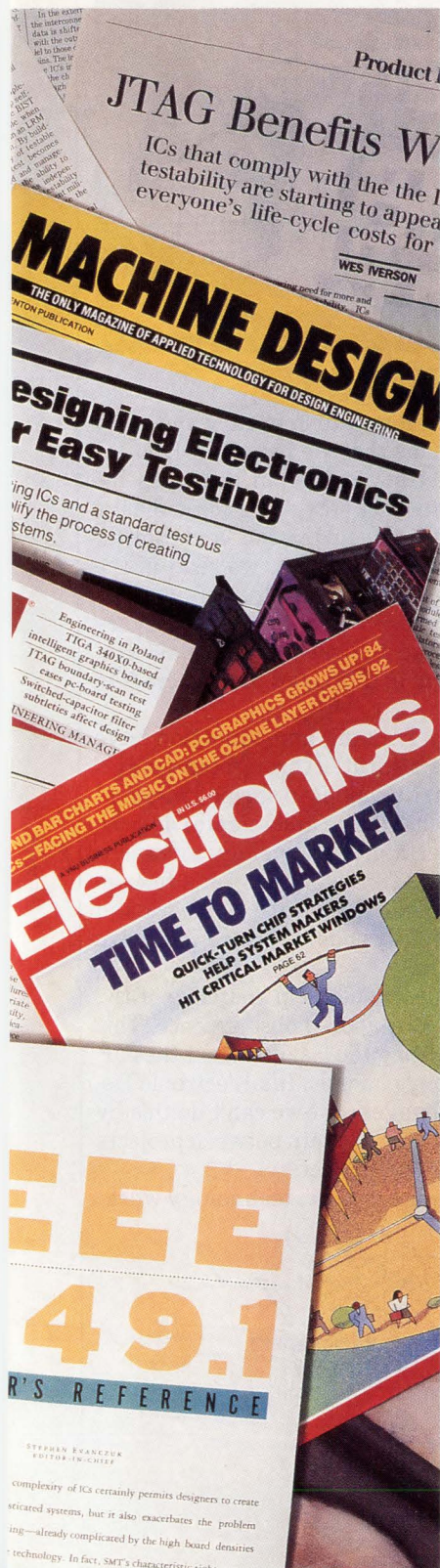
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controllers, and microprocessors with boundary-scan and built-in self-test features.

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As a member of the Joint Test Action Group (JTAG), we contributed to the formulation of the IEEE 1149.1 standard and wholeheartedly support it. We are committed to growing our SCOPE family of products so that designing to the IEEE 1149.1 standard will be like second nature.


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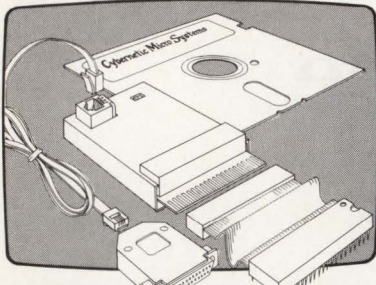
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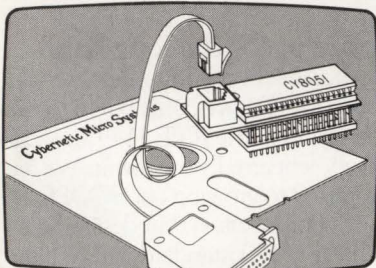
  
**TEXAS  
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## Low Cost 8051 Tools



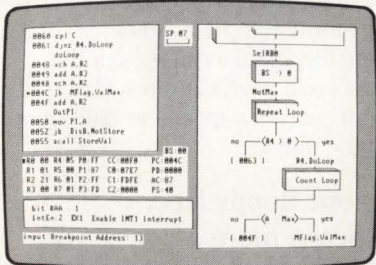
**d<sup>2</sup>ICE-51** \$1250

This Real-Time emulator is low cost and smallest sized full speed 8051 in-circuit emulator. Full access to hardware I/O. Includes all debugging features of Sim and dICE below. Fits in shirt pocket. Cross Assembler incl.



**dICE-51** \$495

This reduced-speed in-circuit 8051 debugger provides full access to I/O but will not run real-time. With the same user interface features as Sim8051 below, dICE-51 generates execution profiles during reduced speed execution. (CMOS and MIL also available.)



**Sim8051** \$395

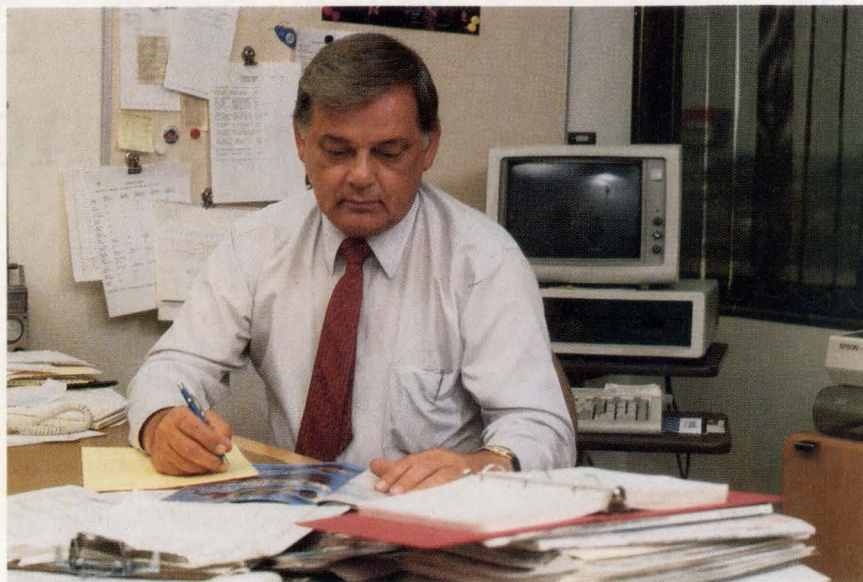
This software Simulator/debugger allows 'no-circuit', debugging of 8051 code on IBM-PCs. All Cybernetics 8051 debug tools offer multi-window source code displays, symbolic access to data, single key commands, breakpoints, trace, full speed and single step execution, execution profiler, and more.

### Other 8051 tools include:

- Cross Assembler \$195
- 8751 Programmer \$195-\$345
- Debugger Demo Disk \$ 39



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PO Box 3000 • San Gregorio CA 94074  
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## KEEPING ENGINEERS ON THE BALL

**T**o those of us who are strictly baseball fans, late February and early March is a special period. First, it means that we have survived another winter, sustained only by television images of collisions between behemoths in shoulder pads and helmets. Second, it means that once again, the sound of bat striking ball is heard in the land: Spring training has begun. And like spring training seasons past, we read in the sports pages that team managers again intend to stress "fundamentals" during this spring training. An interesting concept, spring training. Every year, professional practitioners are subjected to analyses of their past season's performance and given additional training in the basics of their craft to achieve higher levels of athletic quality.

In a way, the same is true for engineering. Training and education have been cited as key parts of the quality programs instituted throughout today's electronics industry. Why not an engineering equivalent to spring training? Engineers could periodically revisit the ever-changing fundamental devices and techniques of electronics technology. Certainly, technology advances are frequent enough to make this worthwhile. After every project's release to manufacturing, the design team should be given the time to look back and analyze its performance. Then, individual members could receive intensive training to help them improve on the next project.

Continually upgrading an engineer's skills also would help allay one of the biggest fears of engineers—almost inevitable, job-imposed obsolescence. This is because they were too deeply involved in finalizing the last details of the current project to keep up with the latest technology changes. It's Electronic Design's purpose to inform our readers of such changes, but we can't do this by ourselves. Employers should let their engineers take a breath between projects to refresh their knowledge before taking on the next project.

It takes skilled people with the latest knowledge to make technology work.

Stephen E. Scrupski  
Editor-in-Chief

...Now, about the New York Mets this year...



# TINY SPDT SWITCHES

## ABSORPTIVE... REFLECTIVE

dc to 4.6 GHz from \$32<sup>95</sup><sub>(10-24)</sub>

Tough enough to pass stringent MIL-STD-883 vibration, shock, thermal shock, fine and gross leak tests... useable to 6GHz... smaller than most RF switches... Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

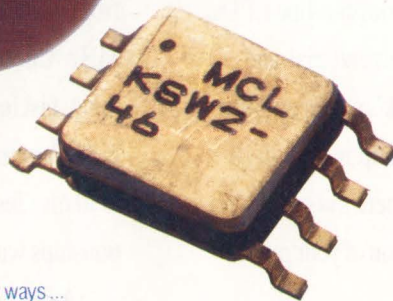
Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only \$32.95, and the KSWA-2-46, at \$48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

**Switch fast... to Mini-Circuits' GaAs switches.**

### SPECIFICATIONS

Pin Model	<b>KSW-2-46</b>		<b>KSWA-2-46</b>	
Connector Version	<b>ZFSW-2-46</b>		<b>ZFSWA-2-46</b>	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ)	ON	1.3:1	1.3	
	OFF	—	1.4	
SW. SPEED (nsec)	rise or fall time		2(typ)	
			3(typ)	
MAX RF INPUT (bBm)	up to 500MHz		+17	
	above 500MHz		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER./STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	<b>\$32.95</b> <b>\$69.95</b>		<b>\$48.95</b> <b>\$79.95</b>	



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**Mini-Circuits**

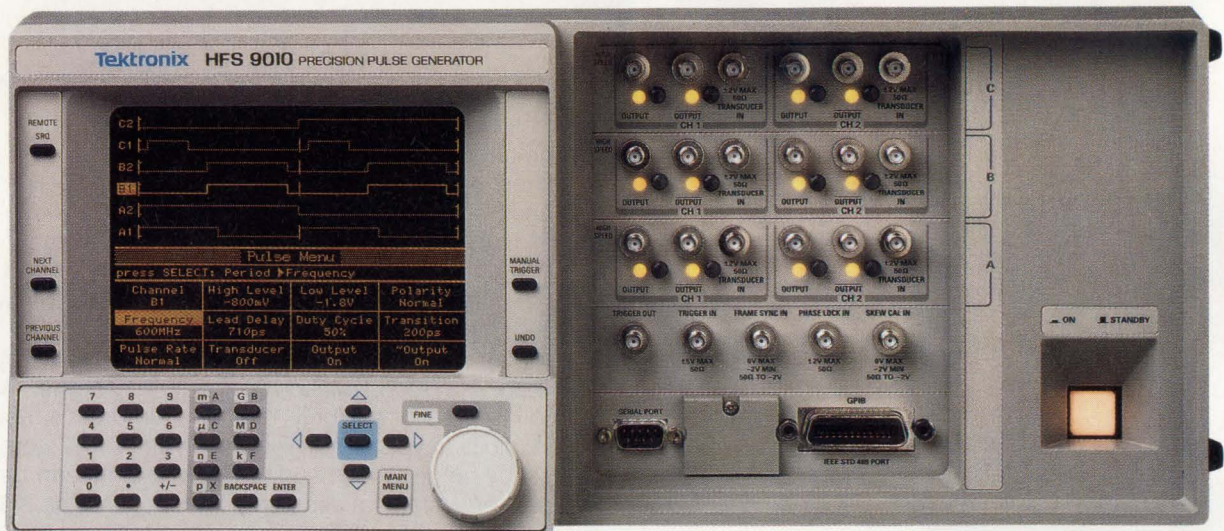
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CIRCLE 107

C 117 REV. G

# Making



**You're looking at the biggest news in signal sources in years: two new families of pulse generators from Tektronix.**

You can already see one reason why Tek's new pulse generators are stirring up so much interest: their what-you-see-is-what-you-get user interface vastly simplifies your life.

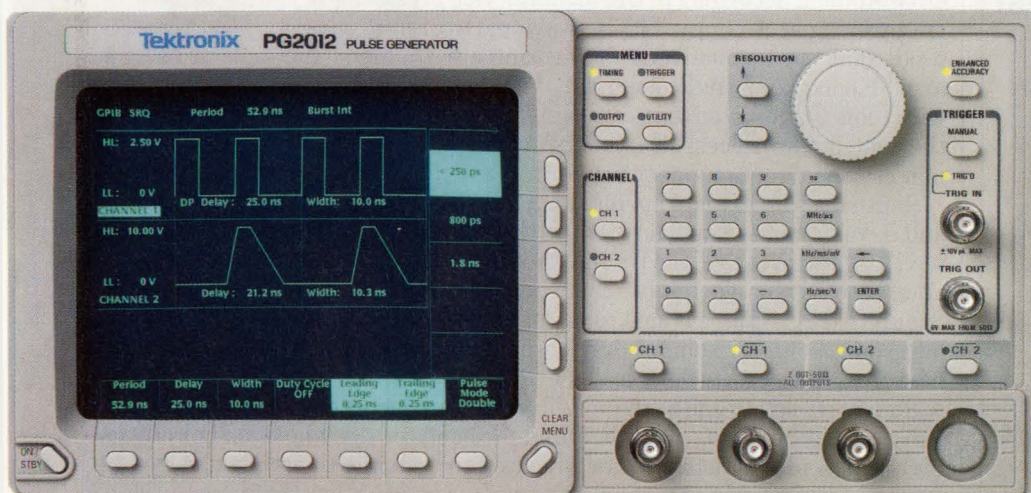
Now you can stop piecing the big picture together from one-line LEDs, blinking error lights and trial-and-error iteration. Tek's new scope-like display lets you set up and modify a whole set of parameters at once, with a true representation of your pulses

and instant, visual feedback.

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Add to all this our popular pulse generator plug-ins from Tek TM500/

# Waves.



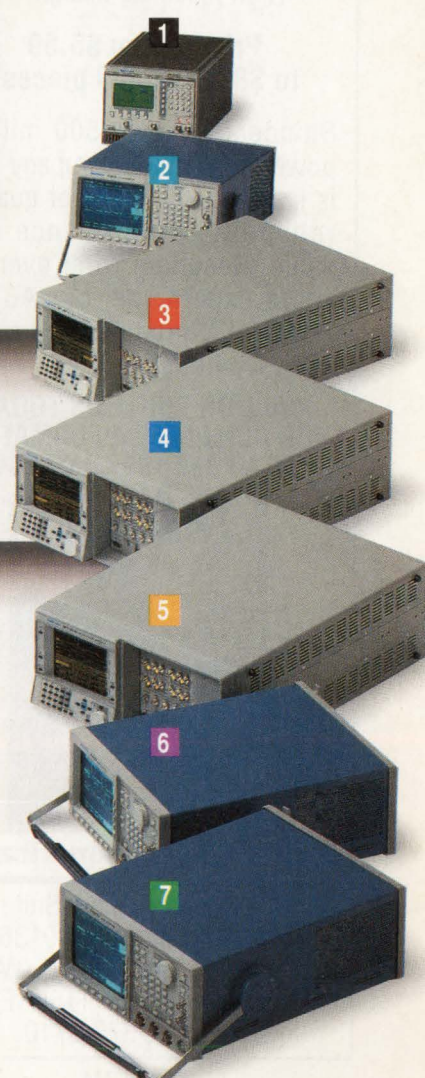
5000 modular instrumentation, and you can see why we're making waves!

Easier to use, more precise and more expandable, Tek's new pulse generators are doing for signal sources what DSOs have done for measurements.

Contact your Tek sales office for a demonstration, or call for more information.

1-800-426-2200

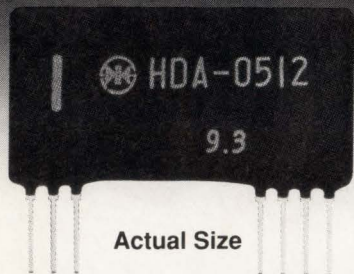
<p>6 PG2010</p> <p>7 PG2012</p> <p>2 PG2011</p> <p>1 PG5110</p>	<p>4 HFS 9010</p> <p>5 HFS 9030</p> <p>3 HFS 9020</p>	<p>FAST LOGIC (<math>&lt; 7</math>ns transitions) ECL, ECLinPS, Sony ECL, GaAs</p> <p>LOGIC (<math>\geq 7</math>ns transitions) TTL, CMOS</p>
MODULES & ASSEMBLIES	COMPONENTS	



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## TECHNOLOGY BRIEFING

### TOOLS PLAY ONLY SUPPORTING ROLE IN CE

The stage is set for concurrent engineering (CE) to be the design methodology of the 1990s. It's becoming obvious that with today's complex systems, creating a testable, manufacturable product requires that engineering teams move away from the traditional sequential design cycle to a more parallel process. Faced with this change, a project manager may wonder what type of sophisticated tools are needed for such a change. The answer? None.

The simple reason is design tools aren't the most important aspect of a successful concurrent-engineering environment, according to David Smith, vice president of engineering at Analogy Inc., Beaverton, Ore. Smith contends that "in a concurrent-engineering environment, the tools are secondary." He explains that concurrent design can be done with today's tools or with tools that existed ten years ago. The tools only increase the efficiency of the concurrent process. Engineers interacting constructively is what really makes concurrent engineering work.

Smith uses an example to illustrate his point. While working in a research and development group, he discovered three types of engineers: the very innovative and creative, the traditionalists who worked to meet specifications, and those who had actually spent some time out on the fabrication line. The group that really knew how to do a good design was the third group. They had spent some time in production and experienced firsthand the requirements of a successful design.

Similarly, says Smith, the engineers in a concurrent-design team must learn each other's jobs to understand the needs of the whole design process. Simply assembling a team of engineers won't change their views. A good IC designer should know the fabrication process and realize that how the chip is designed will affect yield. True concurrent engineering will bring together such disciplines as testing, manufacturing, reliability, design, and software. Each engineer must know enough about all of the other disciplines to recognize that the issues brought up by each team member is important.

In that situation, design tools become a facilitator to give them a common ground of communication. Therefore, they can each perform their own analysis and share results. Tools can also enable team managers to translate their own experience into the language of the people that are working for him. For instance, Analogy is involved in the VHDL and analog HDL efforts because the company sees them as common high-level description methods. Such tools as VHDL can help speed the overall process once the design group decides that they need to communicate and how to communicate.

To be useful, CE tools must provide designers with a way to envision the systems they're designing. Schematics work well at a low level of detail. However, their effectiveness diminishes at the system level. One major reason schematics don't work very well is that engineers can't visualize the problem in the domain they perceive it in. Most schematic systems are set up as a documentation media and not as a design media. For example, once an engineer conceives an idea, he can use schematics to capture the idea and perform further analysis. However, it's difficult to manipulate the idea to improve it. The concurrent environment must have built-in malleability.

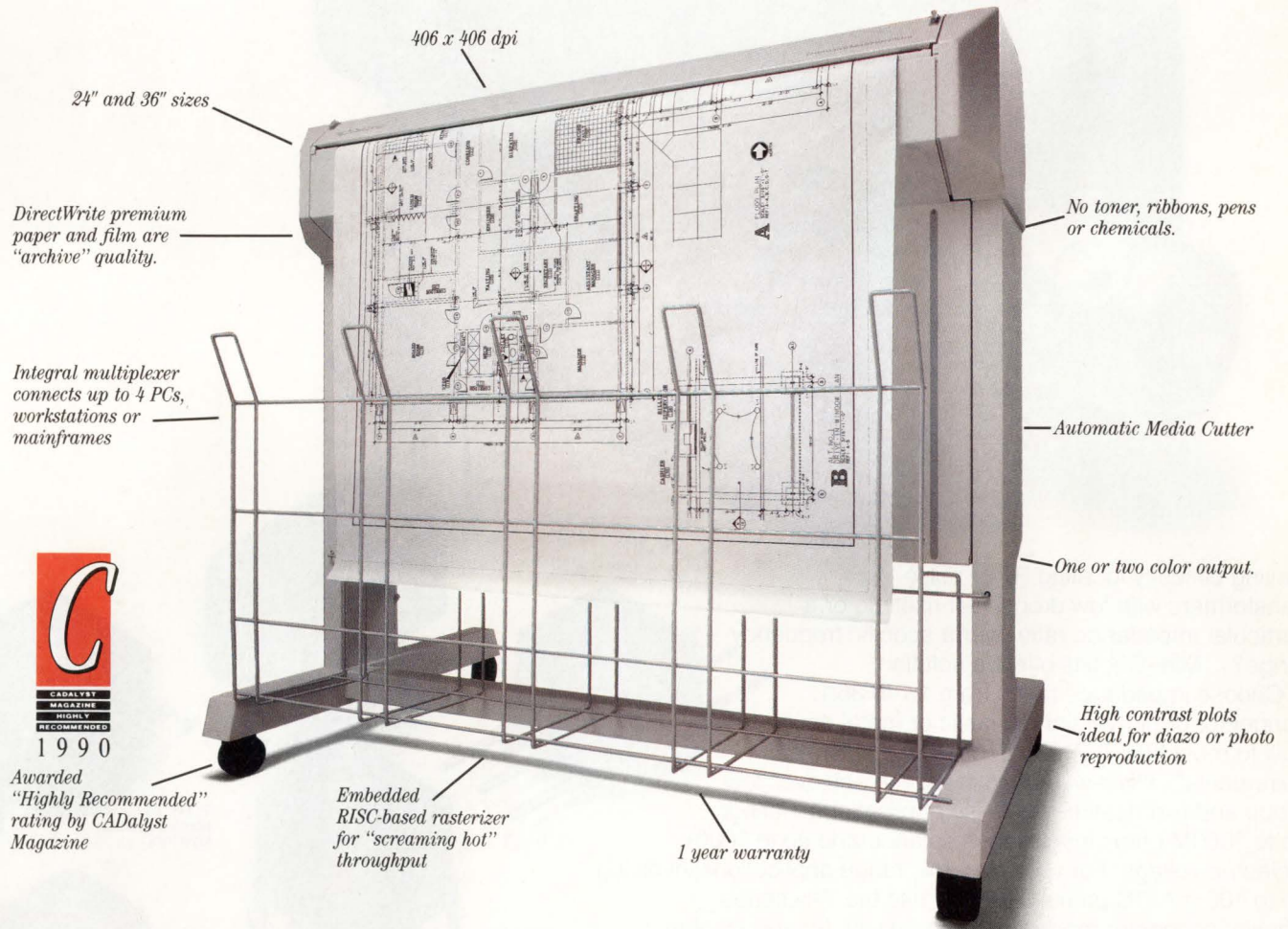
CE also demands tools that produce understandable, visual analyses. Tools must show users where problems exist. Based on that information, they can determine where they need to spend engineering time to make the necessary changes. Present visualization processes involve charts and tables. But the end result is 100 pages of a printed report. What's needed is a way to see where the problems are graphically or in a way that's easy to understand.



LISA MALINIAK  
CAE EDITOR

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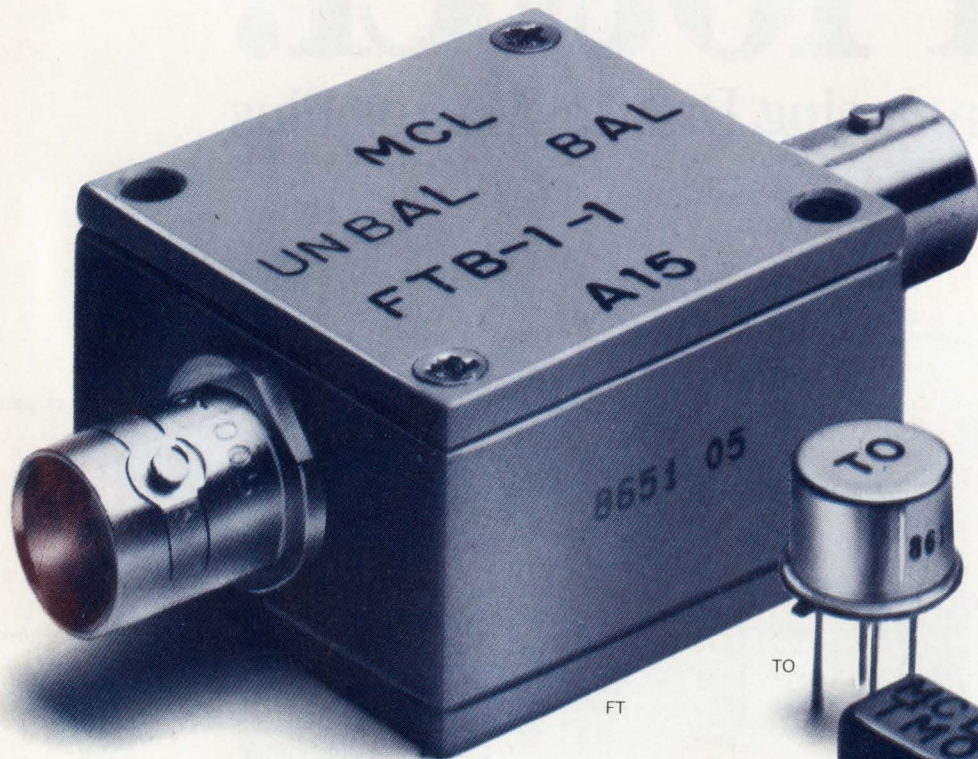
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# RF TRANS

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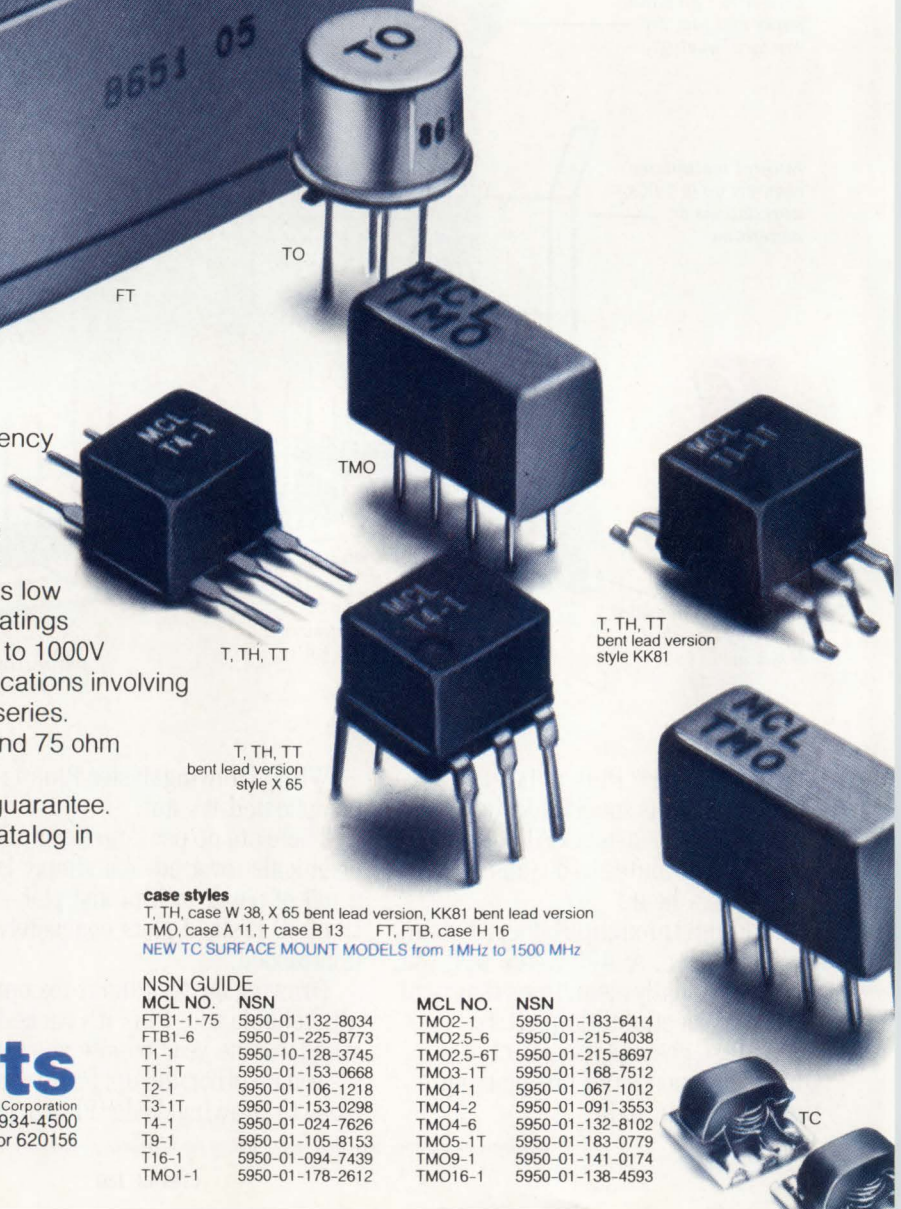


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\*units are not QPL listed



#### case styles

T, TH, case W 38, X 65 bent lead version, KK81 bent lead version  
TMO, case A 11, † case B 13 FT, FTB, case H 16

NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

#### NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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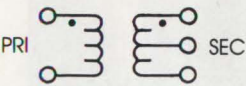
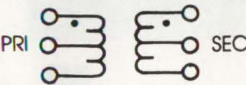
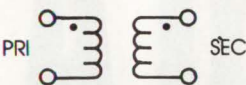
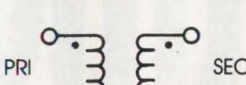
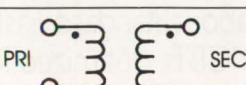
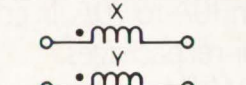
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case style number see opposite page	MODEL NO.	$\Omega$ RATIO	FREQUENCY MHz	INSERTION LOSS			PRICE \$ Qty. (1-9)	
				3dB MHz	2dB MHz	1dB MHz		
<b>A*</b> 	T	T1-1T	1	.05-200	.05-200	.08-150	2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	2-350	2-350	35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	.01-100	4.45
		T5-1T	5	3-300	3-300	6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	.1-60	7.95
		T13-1T	13	3-120	3-120	7-80	.5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
		T4-1H	4	10-350	10-350	15-300	25-200	5.95
		TMO1-1T	1	.05-200	.05-200	.08-150	2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
TMO4-1	4	2-350	2-350	35-300	2-100	6.25		
TMO5-1T	5	3-300	3-300	6-200	.5-100	8.45		
TMO13-1T	13	3-120	3-120	7-80	5-20	8.45		
<b>B*</b> 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	4	.05-200	2-50	2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
		TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
		<b>C</b> 	T	T1-1	1	.15-400	.15-400	.35-200
T1.18-3	1.18			0.01-250	0.01-250	0.02-200	0.03-50	5.65
T1-6	1			.01-150	.01-150	.02-100	.05-50	5.65
T1.5-1	1.5			1-300	1-300	2-150	.5-80	4.45
T1.5-6	1.5			.02-100	.02-100	.05-50	.01-25	5.65
T2.5-6	2.5			.01-100	.01-100	.02-50	.05-20	4.45
T4-6	4			.02-200	.02-200	.05-150	.1-100	4.45
T9-1	9			15-200	15-200	3-150	2-40	3.95
T16-1	16			3-120	3-120	7-80	5-20	4.45
T36-1	36			.03-20	.03-20	.05-10	.1-5	6.95
TO-75	1			10-500	—	10-500	40-250	6.95
T1-1H	1			8-300	8-300	10-200	25-100	5.95
T9-1H	9			2-90	2-90	3-75	6-50	6.45
T16-1H	16			7-85	7-85	10-65	15-40	6.45
TMO1-02	1			1-800	1-800	2-500	—	9.45
TMO1-1	1			15-400	15-400	35-200	2-50	6.25
TMO1.5-1	1.5			1-300	1-300	2-150	5-8	8.45
†TMO2.5-6	2.5			.01-100	.01-100	.02-50	.05-20	7.95
†TMO4-6	4			.02-200	.02-200	.05-150	.1-100	7.95
TMO6-1	6			3-200	3-200	5-150	5-50	7.95
TMO9-1	9			15-200	15-200	3-150	2-40	7.95
TMO16-1	16			3-120	3-120	7-80	5-20	7.95
<b>D</b> 	T	T2-1	2	.050-600	.050-600	1-400	.5-200	3.95
		T3-1	3	5-800	5-800	2-400	—	4.45
		T4-2	4	2-600	2-600	5-500	2-250	3.95
		T8-1	8	15-250	15-250	25-200	2-100	3.95
		T14-1	14	2-150	2-150	5-100	2-50	4.95
		TMO2-1	2	.050-600	.050-600	1-400	.5-200	7.95
		TMO3-1	3	5-800	5-800	2-400	—	8.45
		TMO4-2	4	2-600	2-600	5-500	2-250	7.95
		TMO8-1	8	15-250	15-250	25-200	2-100	7.95
		TMO14-1	14	2-150	2-150	5-100	2-50	8.45
		FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25
FT1.5-1	1.5	1-400	1-400	5-200	1-100	35.95		
<b>E</b> 	FTB	FTB-1	1	2-500	2-500	5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB1-75	1	5-500	5-500	5-300	10-100	36.95
<b>F</b> 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95

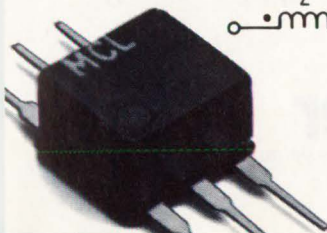
■ Denotes 75 ohm models

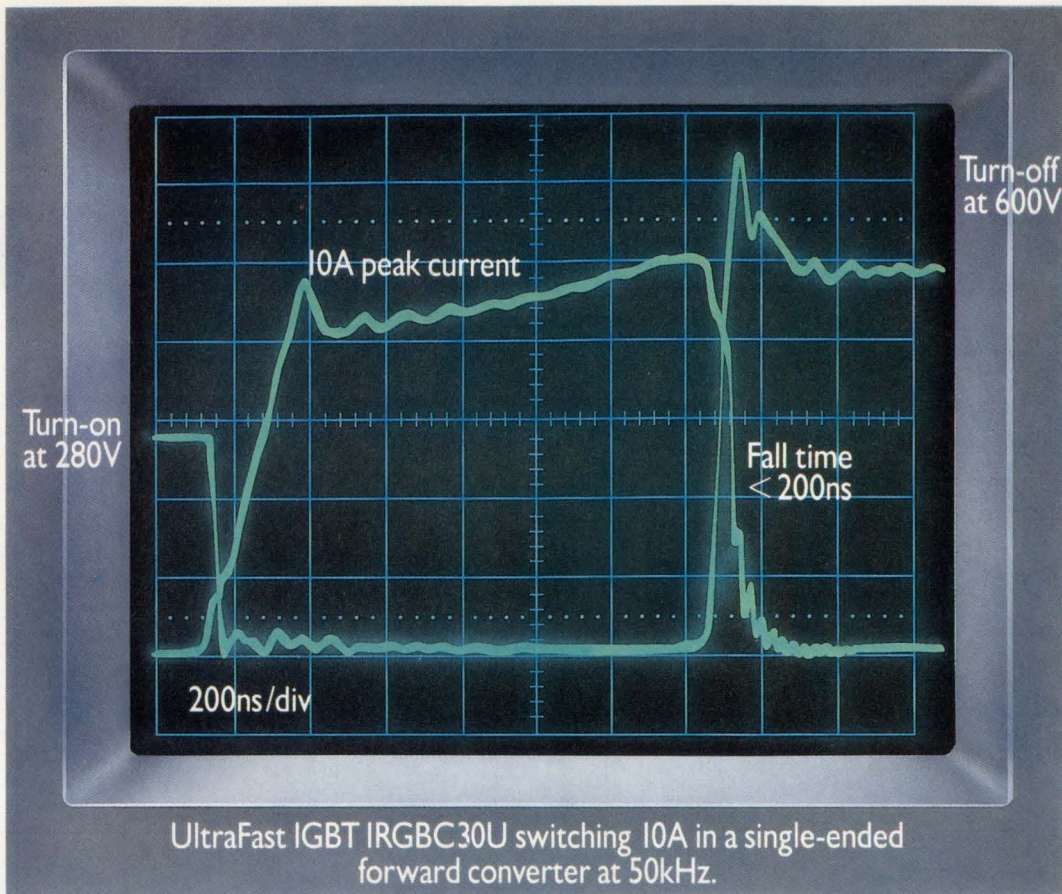
\* FOR A AND B CONFIGURATIONS

Maximum Amplitude Unbalance  
0.1 dB over 1 dB frequency range  
0.5 dB over entire frequency range

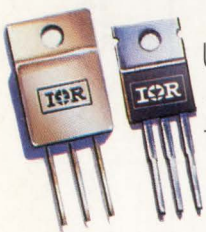
Maximum Phase Unbalance  
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5.0° over entire frequency range

CIRCLE 110





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CIRCLE 134



## ZINC-AIR CELLS TRIED IN LAPTOPS

A battery chemistry with five to eight times the energy density of NiCds is being tried in laptop computers. According to their makers, the zinc-air rechargeable batteries have energy densities of up to 300 Wh/kg compared with 35 Wh/kg for NiCds. The cells have superior energy-to-weight ratio because they use available oxygen from the air to fuel the chemical reaction that releases energy. Other chemistries rely on a heavy, bulky oxidizer within the cell's case. According to Aerobic Power Systems Inc., Atlanta, Ga., two pounds of NiCds will power a typical laptop for 2.4 hours, but three pounds of the company's zinc-air cells will run the same laptop for at least 11.5 hours. Toshiba America Information Systems Inc., Irvine, Calif., is now running beta trials on the zinc-air cells. Call David Dorheim at (404) 952-3375. *DM*

## REAL-TIME OS NOW RUNS ON 24-BIT DSP CHIPS

The first real-time operating system for integer digital-signal processors allows the DSP chips to perform multitasking operations—a key function in most real-time control systems. Jointly developed by Motorola Inc., Austin, Texas, and Ready Systems Corp., Sunnyvale, Calif., the real-time software runs on the 24-bit DSP56000 DSP chips offered by Motorola. It is a derivative of the popular VRTX32 real-time operating system. The active kernel of the VRTX32/DSP56000 software only requires about 3 kbytes of memory, leaving most of the DSP56000's 64-kword memory available for application software. The operating-system kernel takes advantage of the 56000 architecture and performs priority-based scheduling. Built-in intertask communication and synchronization mechanisms free programmers from the problems of synchronizing multiple real-time tasks and enables them to focus development efforts on their application. One of the first cards to implement the real-time operating system is the S-56 from Ariel Corp., Highland Park, N.J. The DSP56000-based card is designed to plug into the one of the S-Bus connectors in a Sun Sparcstation workstation. Contact Jim Ready at (408) 736-2600 regarding the software, and Tim Andre at (201) 249-2900 about the card. *DB*

## TINY PACKAGE HOLDS 20-NS, 1-MBIT SRAM

A leadless chip carrier package measuring just 450 by 550 mils holds the PDM41024L32 static RAM from Paradigm Technology Inc., San Jose, Calif. The package that surrounds the 128-kword-by-8-bit, 20-ns chip is claimed to be about 30% smaller than any other megabit SRAM package available. Thanks to the memory's high speed, high density, and small footprint, it's now easier to design cache memories for compact systems based on the new generation of 30-to-50-MHz RISC processors. Commercial- and military-rated versions are offered with 20-, 25-, and 35-ns speeds. In lots of 100, the 25-ns chip costs \$146 for the commercial version and \$829 for the military version. Delivery is from stock. Call Steven Taylor at (408) 954-0500. *DM*

## TRANSPUTER KIT TEACHES PARALLEL PROCESSING

The Transputer Education Kit is designed for engineers who can program serial machines and want to go on to explore the techniques associated with multiple processing and parallel computing. The kit is the result of cooperative agreements between Computer System Architects (CSA), Provo, Utah; SGS-Thomson's Inmos division, Phoenix, Ariz.; and Logical Systems, Corvallis, Ore. By using the kit, multiple transputers can be cabled together to form arbitrarily large networks of processors. Before the Transputer Education Kit, entry-level transputer development systems were in the \$2000 price range. This kit sells for \$236. It comes with a 20-MHz T400 transputer mounted on a 3/4-size PC add-in board. Also included are an 8-bit PC-bus interface; a T400 C cross compiler; a T400 Occam compiler; example, demonstration, and diagnostic programs; and more than 1500 pages of documentation. The entry-level board comes equipped with 1 or 4 Mbytes of local DRAM. Additional processors can be purchased for \$150 each. For more information, call CSA at (800) 753-4722. *RN*

## MCC CONTRACTS VENDOR TO CREATE MCM TOOL SUITE

The Microelectronics and Computer Technology Corp. (MCC), Austin, Texas, has awarded a \$1.3 million contract to Valid Logic Systems Inc., San Jose, Calif., to develop a suite of tools for multichip-module (MCM) design. Under the two-year agreement, Valid will enhance its Allegro-MCM product in accordance with specifications set forth by MCC's Open Systems Project. Valid was chosen for its strength in high-speed design capabilities, including rules-driven design and floor planning. The company

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CIRCLE 154



is required to add timing-driven and thermal-driven autoplacement, enhancements to transmission-line modeling and Spice-model extraction, expanded rules-driven routing, and new manufacturing interfaces. Technology developed under the contract will be made available to Open Systems participants. Valid can also sell the new products outside of MCC. For more information, contact Valid Logic at (408) 432-9430 or MCC at (512) 343-0978. *LM*

## MULTICHIP MODULES SHRINK TELECOM CIRCUITS

Thanks to a new multichip-module packaging technology, wafer-scale integration has come to telecommunication-system design. The module's high-density interconnections deliver short delays, controlled impedances, low crosstalk levels, excellent thermal conductivity, lower power consumption, and high reliability compared with printed-wiring-board or hybrid-circuit implementations. The PM100 technology, developed by Pacific Microelectronics Centre (PMC), Burnaby, B.C., Canada, can accommodate up to 25 ICs alongside discrete resistors and capacitors. It can also integrate several technologies, including CMOS, GaAs, and bipolar, onto one substrate. Significant benefits have been achieved in transmission-line interfaces, such as T3 and SONET. Multiple channels, complete interfaces requiring a mix of technologies, or fiber-optic interfaces with data rates up to 650 MHz can be implemented in one module. Among the techniques used by PMC to build the modules are wire bonding, multilayer-metal interconnections, polyimide dielectrics, silicon substrates, and advanced design tools. Call Al Kozak at (604) 293-5738. *DM*

## 20,000 LASERS SQUEEZED ONTO A 2-IN. WAFER

Scientists can now mass-produce and test a "semiconductor laser" on a wafer constructed of aluminum gallium arsenide. The researchers, from IBM's Zurich Research Laboratory in Switzerland, have developed a way to build as many as 20,000 tiny lasers on a round semiconductor wafer that's just 2-in. in diameter. Such lasers are now used to read music on compact disks, print output in laser printers, store and retrieve data on computer disks, and transmit information along fiber-optic networks. The IBM scientists expect the new method of laser fabrication to be faster and more effective than conventional methods, while costing about 50% less. They also feel the lasers can be integrated with other electronic components to form optoelectronic chips that use both light and electric current to carry information. The key to the fabrication is the etching process that forms laser mirrors coated with a semireflective material. The mirrors direct the path of light that's emitted when current travels through the chip. The mirrors can be formed in either straight, concave, or convex shapes to bend the path of light. *RN*

## SBUS EXTENSION BOOSTS SYSTEM-I/O PERFORMANCE

The industry's first 64-bit specification for a desktop input/output interconnection has been finalized. The extension of the SBus architecture will help system and add-in card developers improve the performance of SBus-based systems. The SBus specification revision B.0 features a 64-bit transfer protocol which, in anticipation of higher bandwidth requirements from I/O devices, will permit 64 bits of data to be transferred with each clock cycle. This results in a peak bandwidth of 160 to 200 Mbytes/s. The architecture extension is the first modification of the original SBus specification to be released by the Public SBus Specification Committee, which was formed in September 1990 by Sun Microsystems, Mountain View, Calif., and several third-party SBus vendors. Contact the SBus Technical Support Group at (415) 336-3558. *DM*

## POLYMER CIRCUITRY SOLVES DESIGN PROBLEM

In the course of designing its next generation of powerful, compact 80386-based laptop computers, Compaq Computer Corp., Houston, Texas, had problems working out the space and positioning for the computer's LED disk-drive indicator. Initially, the indicator had to be attached to the pc board with an awkward arrangement of cables and connectors and a discrete-wiring package. But by using flexible polymer circuitry from Poly-Flex Circuits, Cranston, R.I., Compaq's engineers eliminated the discrete wiring, connectors, and all but one cable. Poly-Flex's additive-polymer-circuitry technology enables the conductors to be screen-printed directly onto the polymer substrate and the components to be surface mounted to the substrate as well. Compaq's costs fell to \$0.50 per unit compared with \$2 for the discrete alternative. The resulting unit was also lighter and easier to position and assemble. Call David Vieau at (401) 463-3180. *DM*

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CIRCLE 123

## THIRD COMPANY JOINS COPROCESSOR FRAY WITH 80387 REPLACEMENT

Computer-system performance can usually be improved if more hardware is used to tackle the problem at hand. Similarly, on an integrated circuit, additional transistors can be employed to do more every clock cycle. That approach is taken by newcomer ULSI Systems Technology Inc., San Jose, Calif., in its design of a floating-point math coprocessor. The coprocessor directly replaces the Intel 80387, delivering higher throughput while consuming about half the power. Designers at ULSI estimate that their implementation of the coprocessor will run an average 20 to 30% faster than the 80387.

To verify the improved performance, some benchmark tests were run on a 33-MHz 80386 computer with an 80387-33 Intel coprocessor and the US83C87-33 coprocessor. The first test was a wire-frame drawing rotation without erasing, in which the wire frame is rotated 3 degrees at a time over the 360-degree field. The second test consisted of a Mandelbrot fractal image. And a third test was a set of benchmarks established by the PC Labs group of PC Magazine.

In the first test, the ULSI chip rotated the image 18% faster. In the second test, the chip showed a 26% speed increase. And in the third test, it delivered a 29% improvement.

The ULSI chip, which puts about twice the number of transistors to work as the 80387, employs a radix-16 multiplier that can

perform a 64-bit multiplication in four cycles. That multiplier can also handle matrix computations more rapidly than the logic on Intel's chip. One key architectural improvement inside the arithmetic unit is a three-cycle adder that has hardware assists to perform format conversions. That extra hardware saves time when switching between number formats.

During the chip's design, much attention focused on the coprocessor

interface and ways to reduce bus overhead so that operations can be started sooner. Unfortunately, due to software compatibility issues, just minor tweaks were possible. Internal buses are 80-bits wide to handle the full 80-bit extended double-precision numbers. In contrast, Intel's math unit uses narrower buses and requires multiple cycles to transfer full 80-bit numbers.

Though the chip from ULSI will use more transis-

tors, it will consume less power than the 80387 according to its designers, because it's implemented with static logic. The static design lowers the standby power and enables the chip, to some extent, to perform its calculations with lower power consumption. Furthermore, designers at ULSI believe that no patent litigation issues exist on its design versus the Intel approach, and that they should be able to deliver a steady flow of math chips.

For more information, contact George Hwang, (408) 943-0562.

DAVE BURSKY

## LAPTOP PC DRIVES nV/M ELECTRIC FIELDS

A Compaq battery-powered laptop PC lies at the heart of a system that simulates small nV/m underwater electric fields. The system was used in a biological experiment to study the behavior of marine life, by Dr. Timothy Tricas of the Washington University School of Medicine, St. Louis, Mo., and Scott Michael, a graduate student at the University of Nebraska. The simulator includes a 12-bit multiplying digital-to-analog converter (DAC) and an isolation am-

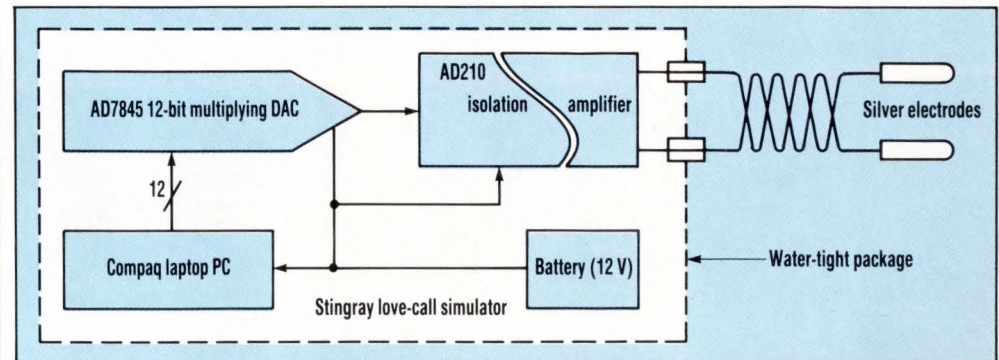
plifier, both from Analog Devices, Norwood, Mass. All of the equipment was enclosed in a water-tight plastic case.

Tricas and Michael used their electric-field synthesizer to obtain information on the behavior of round male and female stingrays found in shallow waters off the Mexican Gulf coast. They recorded, and then played back bioelectric "calls" made by the stingrays. These calls are part of what researchers believe is a sixth sense possessed by sharks, sting-

rays, and skates (known collectively as Elasmobranchii), which enables them to perceive minute electric fields and respond.

The very weak field generated by stingrays has a mean intensity of 500 nV/m. In contrast, the mean field intensity of the earth at sea level varies between 100 and 300 V/m, and can rise to 10,000 V/m during electric storms. Mimicking the female ray's field demands that the low-level signal is accurately reproduced in sea water several meters deep, while still maintaining the field's complex spatial features.

Previously recorded calls were digitized and







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### 10-bit A-to-D Converters.

There's three new 10-bit A-to-D Converters which offer five to eleven channels of input with on-board S/H. These are SAR-type converters with a serial interface that permits a 8, 10 or 16-bit data transfers, making them completely SPI compatible. Reference voltages down to 2.5 volts are accommodated.

### New LED Display Driver.

Motorola's newest LED Display Driver is configurable to drive individual lamps, seven-segment displays or a combination of both. Each of these cascable ICs drives five digits plus decimals. They also offer a serial interface and a variable current source to easily vary the display's brightness.

### Advanced Video Circuits.

New additions to our video circuits portfolio include an Enhanced Comb Filter and Video Op Amps for video signal processing in TVs and VCRs. Our Comb Filter minimizes common comb-filter problems such as dot crawl and cross color.

As a companion to our filter, Motorola has introduced Dual Video Amplifiers. These video op amps have a

guaranteed bandwidth of 10 MHz, are capable of directly driving 150 Ohm loads and have a gain of 10 dB at 5 MHz.

### Dual PLLs for cordless telephones.

Motorola Dual Phase-Locked Loop frequency synthesizers designed for cordless telephones have a maximum frequency of 60 MHz with a supply range of three to five volts. They synthesize up to 15 channel pairs.

Motorola also has a new general purpose dual PLL that's designed to interface with both VHF and UHF dual modulus prescalers.

### Single-chip VHF PLL Frequency Synthesizer.

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stored on the PC's hard disk. For playback, the calls were fed to the multiplying DAC, and then to silver electrodes through the isolation amplifier (see the figure).

For a better understanding of the properties of the electric field that "stimulate" male stingrays, both amplitude and frequency were varied. Field intensity was varied with an Analog Devices AD7845 multiplying DAC, while frequency control was maintained by the host PC. This allowed the researcher to study the stingray's response to both strong electric fields (field-intensity control) and fast signals (frequency control).

The multiplying DAC had two variable inputs: a digital word that corresponds to the playback of the female stingray from the computer, and an analog reference that determines the output signal's magnitude. With the DAC, the researchers could control the output current to the isolation amplifier accurately in the range of 4 to 8  $\mu$ A. This in turn produced field intensities near the electrodes on the order of nV/m.

The secret of the system, however, was the AD210 isolation amplifier. It galvanically isolated (to 2500 V) from input to output and input power from output power. It interrupted ground loops and leakage paths and allowed operation from the host's battery. Most importantly, the isolation amplifier rejected common-mode noise by up to 120 dB. This noise would have significantly distorted the amplifier's output to the electrodes.

FRANK GOODENOUGH

## AIRBORNE EXPERIMENTS STUDY SUPERCONDUCTERS AT ZERO GRAVITY

The electrical properties of high-temperature superconducting (HTSC) materials depend on their microstructure—that is, the size and shape of the materials' crystals and how they interlock. A factor that affects the microstructure is gravity, or the lack of it, as the material is formed.

To study gravity's effects in the production of HTSC materials, researchers from Space Industries International Inc., Houston, Texas, and the Los Alamos National Laboratory, Los Alamos, N.M., are using a computer-controlled furnace aboard NASA's KC-135 parabolic-flight aircraft. The furnace melts the material being studied, which then resolidifies as the aircraft spends about 20 seconds in near-zero-gravity.

A recently discovered class of HTSC materials are polycrystalline ceramics, according to Donald Pettit, a research scientist at Los Alamos. Because polycrystalline materials contain crystals of different densities, gravity plays a role in the materials' microstructure. "As this kind of material solidifies in gravity, crystals segregate according to their density," notes Pettit.

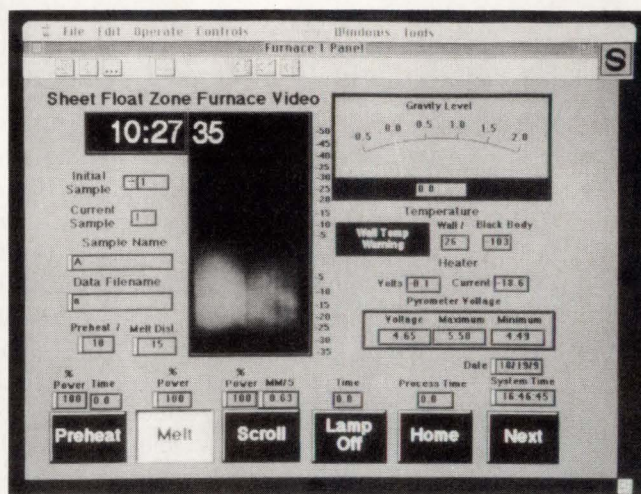
A zero-gravity environment may enable composite materials, such as mixtures of superconducting ceramics and silver, to be produced. In zero gravity, they can be brought to a full melt and maintain a fine dispersion of silver within the matrix of the superconducting material.

The project uses the Sheet Float Zone Furnace designed by Space Industries. It uses four movable quartz halogen lamps to focus heat on a sample up to 2.5-in. by 4-in. by 0.1-in.

Typically, a sample is preheated as the modified KC-135 performs a 2-G

tosh IIX running LabView 2 software from National Instruments Corp. The computer sends signals to a programmable stepper-motor system that controls heater movement, and to an SCR power controller that regulates the heater.

Paul Brannon, manager



pull-up. During this phase, the heaters move along the material, bringing it close to melting. As the plane's nose is pushed over, establishing a near-zero-gravity environment, the heaters are brought closer together, doubling the heat at the center of the sample and establishing the melt. The heaters then move slowly apart to spread the melt along the sample's length.

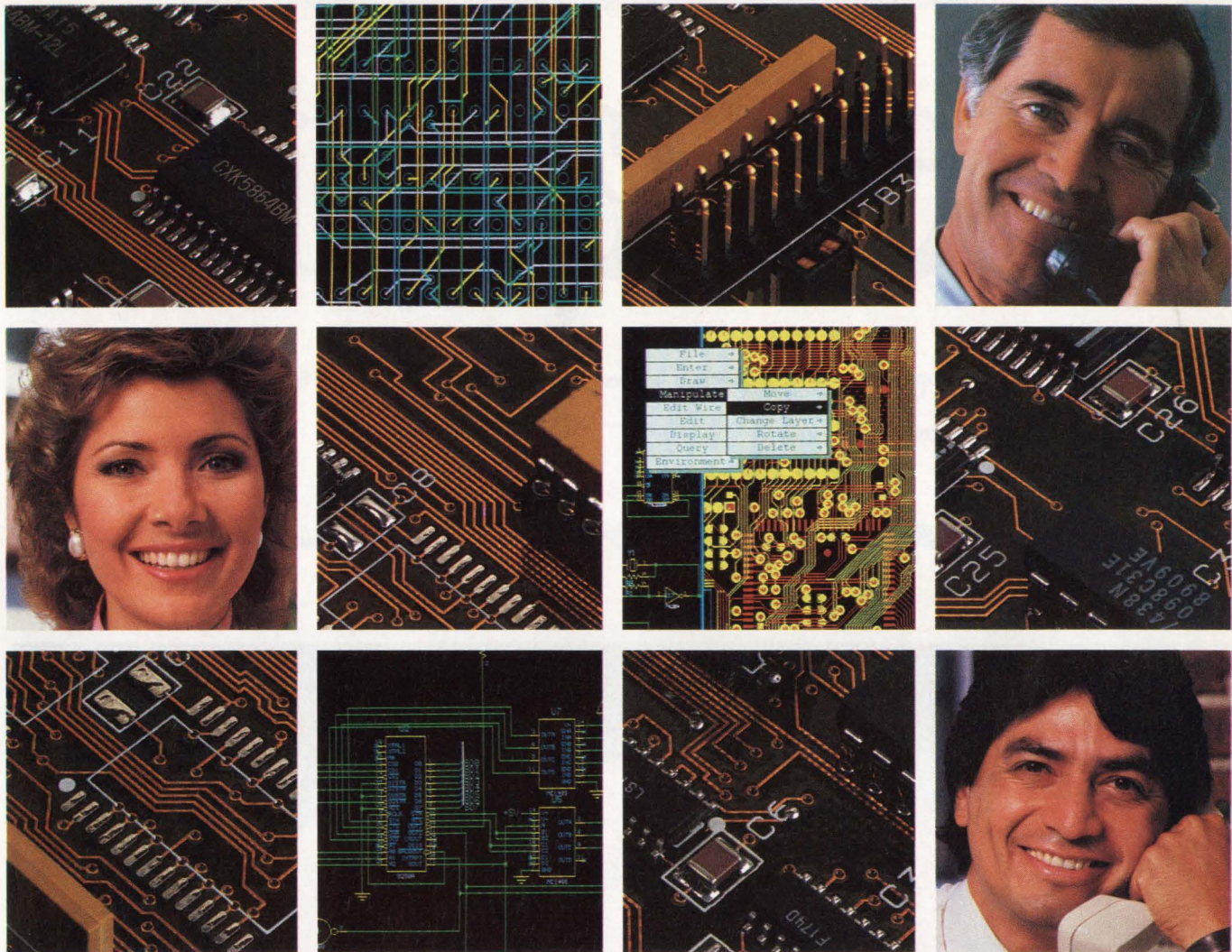
As soon as the focused energy leaves an area, the material begins to resolidify. Solidification occurs between two separate melt fronts, an area called the float zone. About five seconds before gravity returns, the lamps are shut off to allow the material to completely solidify.

The process is controlled by an industrialized Macin-

formation systems at Space Industries, was the primary developer of the LabView application program. To make the system easy to use in flight, Brannon designed a graphical front panel for use with a touch screen. The large "buttons" on the virtual-instrument panel make the furnace easy to control during the airplane's maneuvers (see the figure).

To help researchers analyze the data from the experiments, Brannon added an off-the-shelf video camera and a VCR to the system. As the furnace operates, the camera's video image is displayed on the LabView 2 screen display, along with numerous processing parameters and the control switches.

JOHN NOVELLINO



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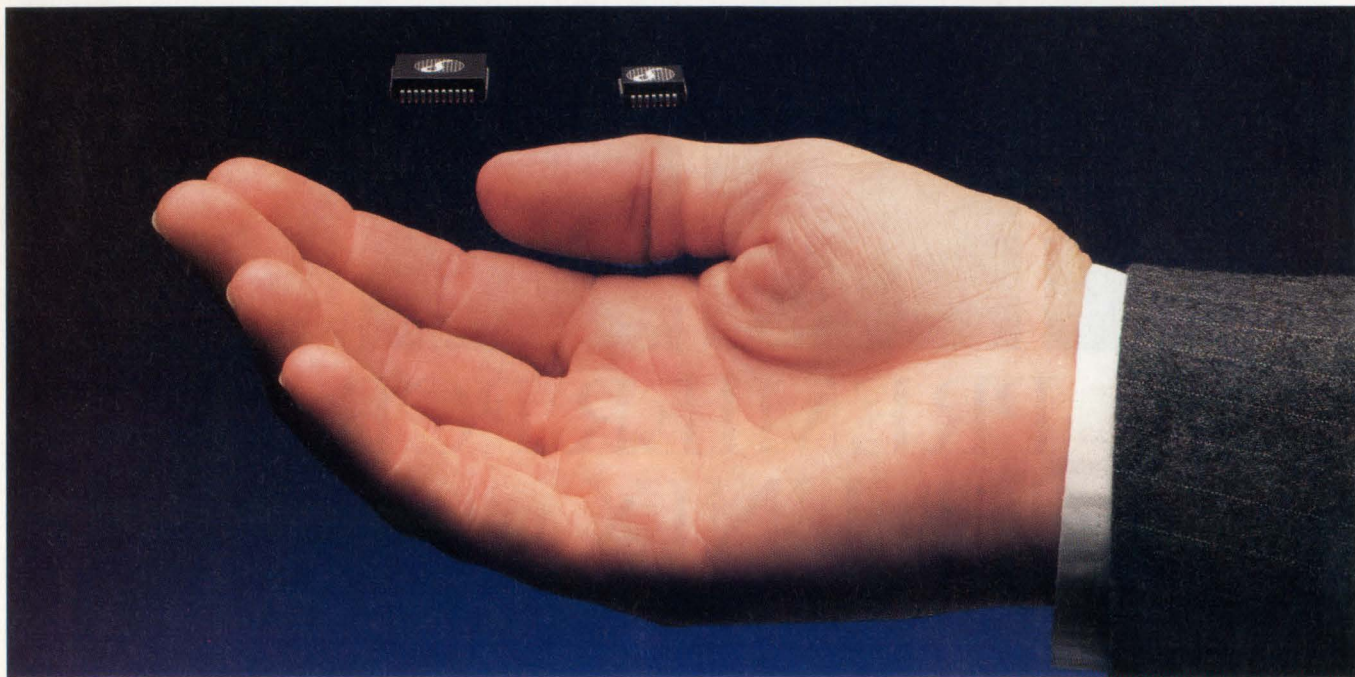
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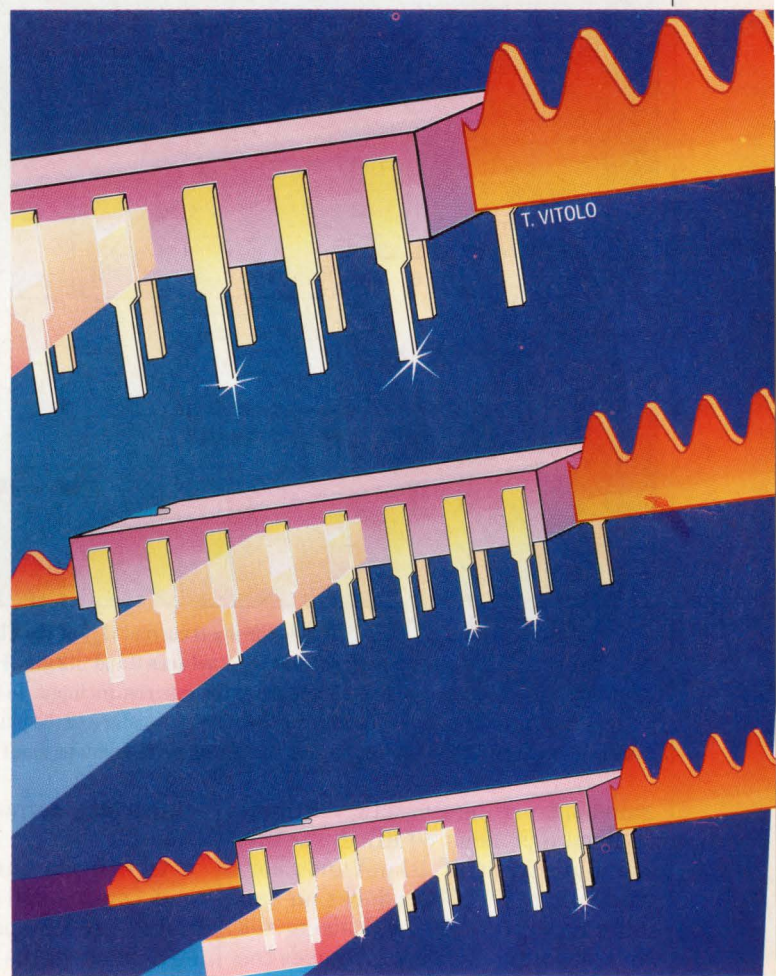
# ANALOG MULTIPLIER IC WORKS FROM DC TO 200 MHz

FRANK GOODENOUGH

**A**long with op amps, analog multipliers represent the basic IC building blocks at the heart of analog signal processing. Though they go back to the birth of AM radio, most analog multipliers today are based on the four-quadrant, voltage-mode multiplier circuit patented by Barrie Gilbert (then of Tektronix and now of Analog Devices). Known as the Gilbert cell, it offers high accuracy but sacrifices some of that accuracy at wider bandwidths. Now, Barry Harvey of Elantec has come up with a two-quadrant, current-mode, multiplier architecture that extends bandwidth while maintaining accuracy. The new architecture debuts in Elantec's EL2082.

While earlier IC multipliers were relatively slow and expensive, the EL2082 sports a full-power bandwidth of 150 MHz and goes for under \$6 each in hundreds. The multiplier also offers greater accuracy than several recent and expensive high-frequency variable-gain amplifiers. By considering all of these factors, it appears that wideband analog multiplier/variable-gain amplifier/mixer ICs are a wavelet of the future as can be seen by several recent product announcements. This trend is illustrated by the fact that at least four multiplier circuits were described in technical presentations at the past International Solid State Circuits Conference (ELECTRONIC DESIGN, Feb. 14, p.67).

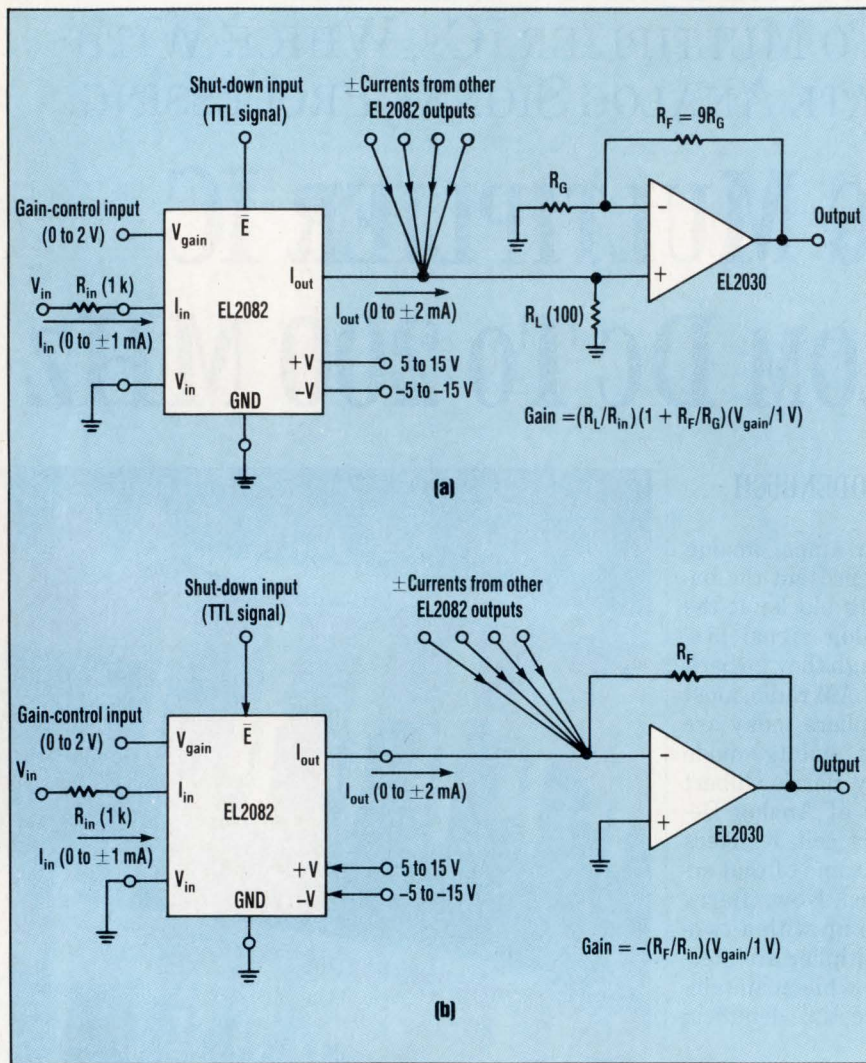
The EL2082 is a two-quadrant multiplier that uses current steering to achieve its wide signal bandwidth. In fact, its front-end resembles that of a current-feedback amplifier (see "Current steering controls gain/attenuation," p. 37). An input current ( $I_{in}$ ), between 0 and  $\pm 1$  mA, produces a linearly relat-



ed output current ( $I_{out}$ ) of 0 to  $\pm 2$  mA,  $\pm 0.4\%$  (see the figure). Just one resistor,  $R_{in}$ , connected between a voltage signal and the current input, converts the voltage signal to a current.

Applying 0 to +2 V at the gain-control input  $V_{gain}$  varies the current gain through the chip from zero to maximum. The result is a gain-control range of at least 50 dB with a calibrated accuracy within 5%. The complete

# 200-MHz TWO-QUADRANT ANALOG MULTIPLIER



**APPLYING 0 TO  $\pm 1$  mA** to the input current ( $I_{in}$ ) of the EL2082 wideband IC multiplier produces an output current ( $I_{out}$ ) between 0 and  $\pm 2$  mA. The output current is a direct linear function of 0 to 2 V applied to the gain-control input. To create an output voltage, the IC's output current can either drive a resistor and the plus input of a follower-connected op amp (a), or the op amp's summing point or minus input (b).

gain-control range, practical in many applications, runs 80 dB. Basically, an input current of  $\pm 1$  mA and a control voltage of 1 V produces an output current of  $\pm 1$  mA. Raising the control voltage to 1.5 V increases the output current to  $\pm 1.5$  mA. Two volts of control voltage creates  $\pm 2$  mA of output current.

Because it's a two-quadrant multiplier, zero or a negative voltage on the control pin shuts it off. Input-to-output isolation then runs 80 dB at 10 MHz. Applying a TTL signal to the shut-down pin  $\bar{E}$  provides similar isolation and creates a high impedance

state at the output (so-called analog tristate).

As with its current-feedback op-amp cousin, full-power (input current of 1 mA pk-pk) and small-signal 3-dB bandwidths of the multiplier aren't that different from each other, being 150 and 200 MHz, respectively. And small-signal response is flat—within  $\pm 0.1$  dB—to 40 MHz. The output current's compliance voltage is within 3 V of the positive and negative supply rails.

Since the IC runs off  $\pm 5$  to  $\pm 15$  V, it can push its  $\pm 2$ -mA output into a 6-k $\Omega$  load, developing  $\pm 12$  V. But that

output swing can't be pushed to 200 MHz because stray capacitance across the resistor severely limits bandwidth.

While a smaller resistor, say 100  $\Omega$ , should do the trick, full-scale output will be limited to just  $\pm 200$  mV. However, this can be applied to the plus input of a fast op amp, such as Elantec's current-feedback EL2020, EL2030, 2070, or 2071 (depending on the bandwidth needed), and gained up at least ten times (see the figure again, a). Alternatively, the multiplier's output can drive the minus input of the op amp directly (see the figure again, b).

## WHO NEEDS 'EM?

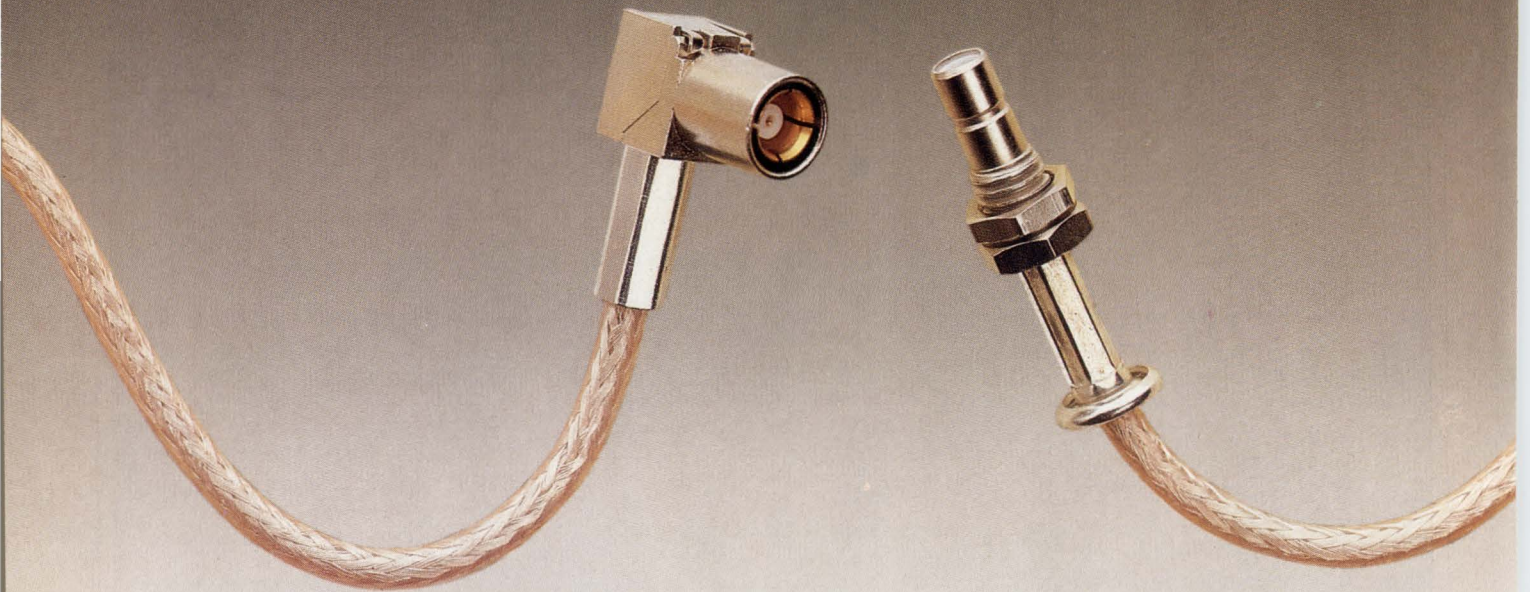
The EL2082 can be considered a low-cost device that brings all but the most-precise multiplier applications to video-bandwidth signals. Differential gain and phase with 3.58-MHz NTSC test signals are typically 0.14% and 0.05°, respectively, for  $\pm 0.35$ -mA input signals. At 30 MHz, differential gain and phase rise to 0.2% and 0.12°, respectively. Due to its wide bandwidth, the chip can also be located in the feedback loop of a fast op amp, reducing distortion (improving differential gain) by a factor of 3 to 5 (9 to 15 dB), but limiting the gain-control range to about 10 dB. However, a fader circuit can be built with two multipliers in the feedback loop of one op amp. The circuit offers the same reduced distortion while maintaining 80 dB of gain control.

Other homes for the multiplier range from manual gain control of wideband/fast-slewing signals, particularly at a point remote from the manual control itself, to changing the frequency response of active filters. Like any multiplier, the EL2082 makes for a good modulator and demodulator.

It's a natural in AGC circuits and can take advantage of the full 80-dB gain-control range. The current inputs and outputs lend themselves to tuned circuits, such as IF amplifiers and filters.

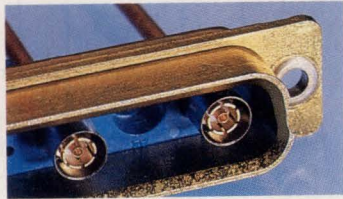
The combination of current output and the shut-down pin adapts the IC to mixing and/or multiplexing multi-





# What's

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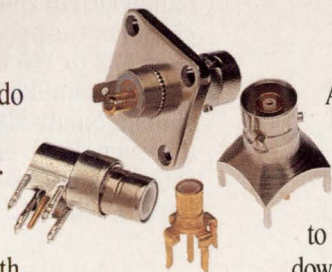






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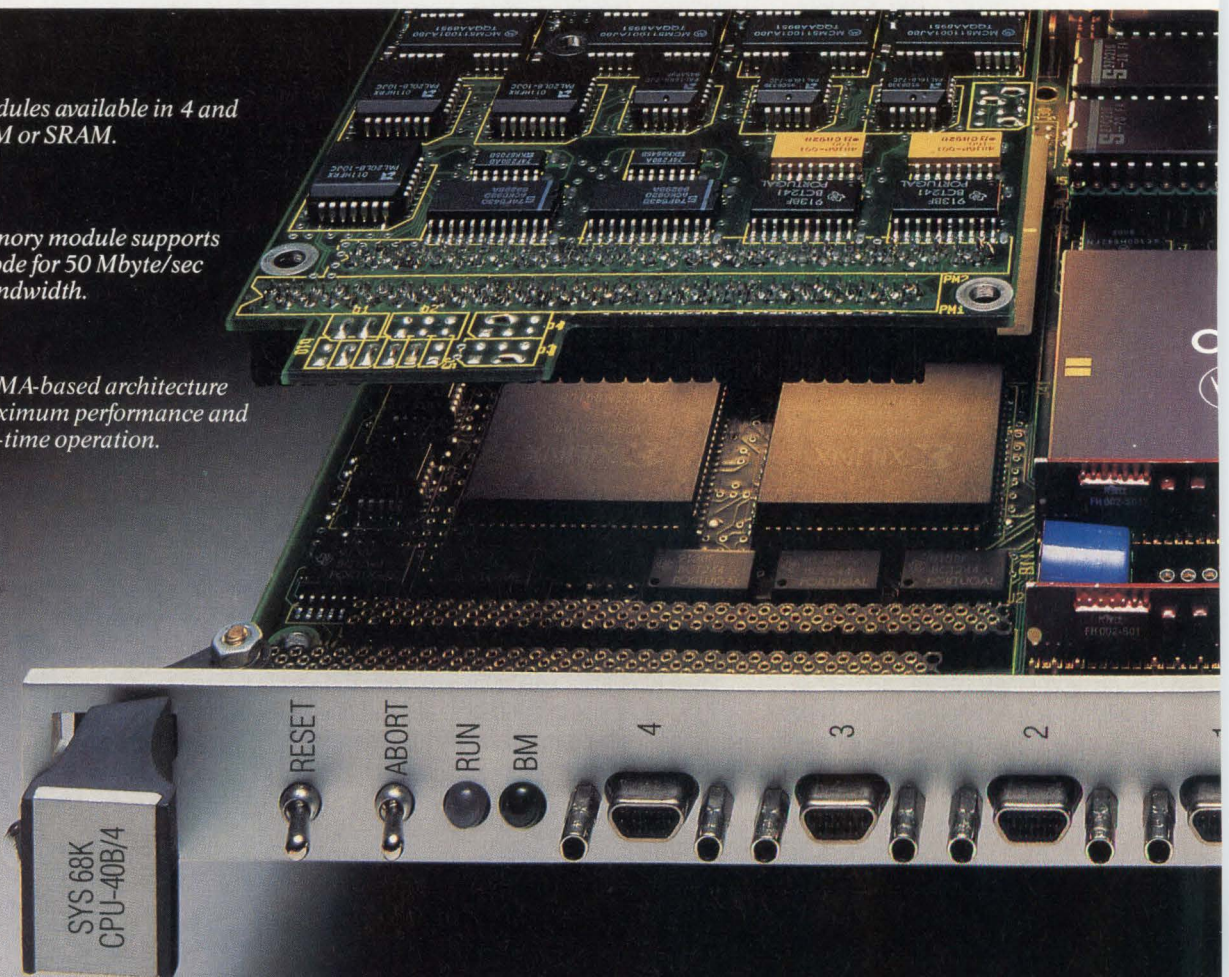
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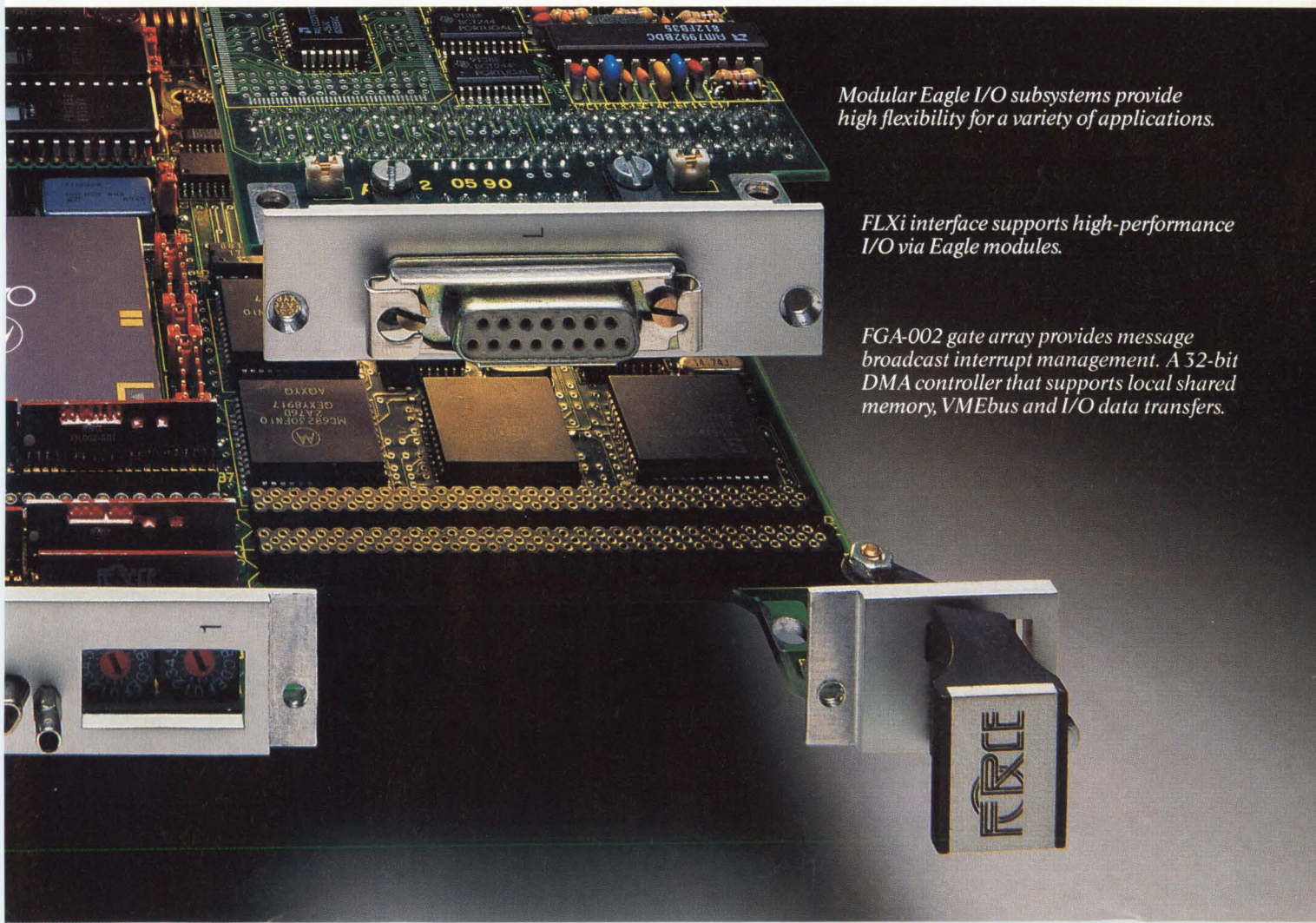
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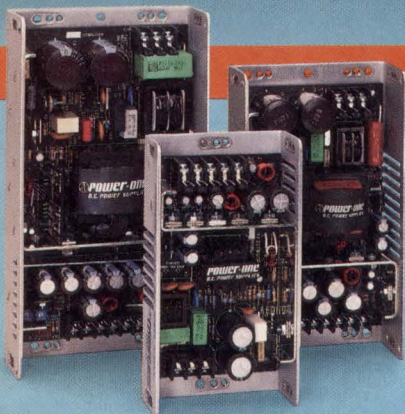


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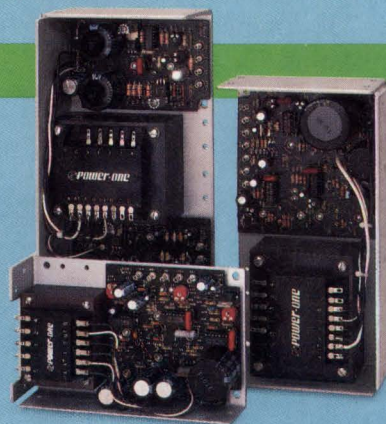
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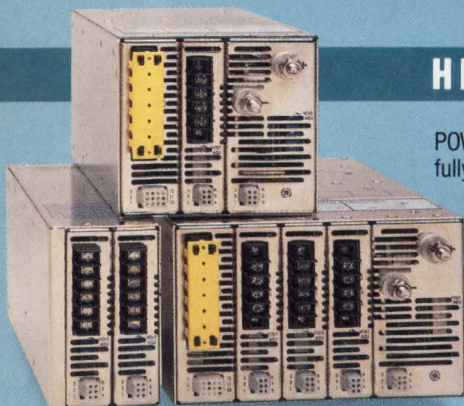
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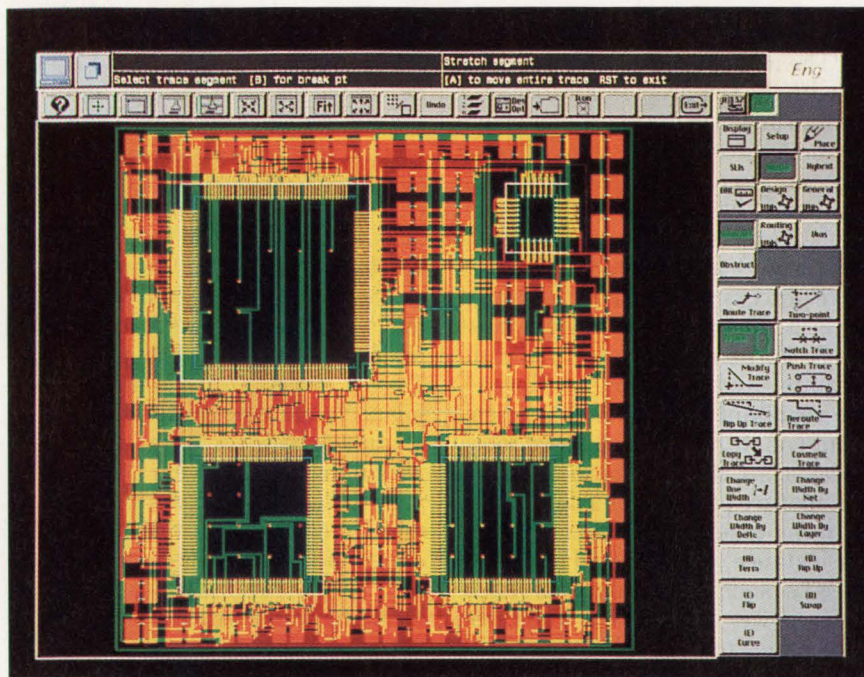
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LISA MALINIAK

## IC AND PC-BOARD DESIGN SOFTWARE BLEND TO FILL THE NEEDS OF AN EMERGING TECHNOLOGY.

have characteristics of both pc boards and ICs. Consequently, they can approach the problem from several directions. Most vendors involved with MCMs have chosen to modify existing pc-board or hybrid

design tools. Several companies, though, are approaching MCMs from the IC side. Others feel that the best solution is to combine elements of both pc-board and IC design tools.

Pc-board-based MCM design tools work well now because most of the early MCM technology is based on pc-board technology. In the future, however, engineers will create much denser designs and MCM technology will migrate toward IC technology (see "Semiconductor manufacturers meet MCM needs," p. 47). IC technology yields finer line widths, better controlled geometries, and higher densities. "MCMs should be considered as a large ASIC and not as a miniature pc board," claims Patrick Scaglia, director of research and development for the MCM program at Cadence Design Systems Inc., Santa Clara, Calif. Scaglia explains that this is because MCMs are considered as a single function, just as an ASIC. In addition, manufacturing techniques and testing problems are very close to IC technology.

There isn't a firm definition as to what an MCM really is. Mike Bare, a product marketing manager at Intergraph Corp., Huntsville, Ala., states that "An MCM ranges from a silicon-on-silicon structure to a small, dense pc board. We must supply a design tool that's open for about anything."

Intergraph has a tool called MCM Engineer that covers a range of technologies falling under the MCM umbrella (see opening photo). MCM Engineer encompasses three technologies: ceramic packaging (hybrids), silicon on silicon (ASICs), and laminated technology (pc boards). What the tool will be focused on in the future will depend on how the MCM industry unfolds.

In developing MCM Engineer, Intergraph conferred with MCM designers on their particular needs. The fact that Intergraph has been in the hybrid industry for five

# EDA TOOLS EVOLVE TO SUIT MCM DESIGNERS

**M**ultichip modules (MCMs) are fast becoming a popular way to build lighter, smaller, high-speed digital systems. Using MCM technology reduces the size of multichip systems because IC dies are mounted directly on a substrate. And because interconnect lengths are shorter than on pc boards, MCM speeds are expected to go into the gigahertz range. Designing an MCM, however, isn't an easy task. For instance, a typical MCM may have several high-speed ASIC dies with 256 pins each, all interconnected on a few square inches of substrate. Electronic-design-automation (EDA) vendors have just begun to introduce design tools to support this emerging technology.

A problem arises for EDA vendors because MCMs

## MCM DESIGN TOOLS

years helped because they got lots of feedback from hybrid designers who made the progression to MCMs.

The best way for EDA vendors to determine what's needed in MCM design tools is to work closely with MCM designers. nChip Inc., San Jose, Calif., an MCM supplier, is one of the partners working with Cadence Design Systems on the company's MCM tools program. The role of nChip is to provide direction and input to Cadence as to what the technology's requirements are, from both a designer's and manufacturer's point of view.

Cadence Design Systems is developing their MCM tools on the company's IC framework. "This was because MCM designers looked more like ASIC designers than pc-board designers," explains Phil Arana, director of marketing for Cadence. The MCM tools are being built from modifications of the Amadeus toolset. For instance, Cadence plans to create different routing algorithms for the various MCM technologies.

In another example of vendors working closely with designers, the Microelectronics and Computer Technology Corp. (MCC), Austin, Texas, has an Open Systems satellite program doing research on MCMs. According to the project's leader, Marshall Andrews, the program's goal is to "drive the domestic infrastructure to support the introduction of MCMs." MCC and the program's member companies looked at what's missing for MCM acceptance. One area found to be lacking was effective CAD tools.

The group determined which existing tools weren't adequate and why. A list of required MCM design tools was listed in order of importance, and specifications were set for the top four tools. The four tools are: a component placement tool; an interconnect routing tool; an extraction tool to take data off the design for additional simulation, enabling designers to use the simulation tool they typically use; and a timing analyzer. Tool users essentially formulated the list. MCC has contracted with Valid Logic Systems Inc., Chelmsford, Mass., to develop these

tools over the next year and a half.

"The main purpose behind coming up with the requirements is to build a system in which the users don't have too many iterations," states Hector Moreno, a senior member of the technical staff at MCC. Today, most designs are placed and routed, and then run through analysis tools. This iterative process goes on until the design is right. The proposed system must work through user-defined constraints. And according to Moreno, the resultant tools should have elements of both IC and pc-board tools, because MCMs could be looked at as a miniature pc board or a large chip.

In the case of the placement tool, for instance, users should be able to specify such constraints as maximum power dissipation. Then, the placement tool should come back with a recommendation on decisions; for example, whether or not thermal vias are needed. And if thermal vias must be used, the placement tool should place them.

### LOOK AHEAD

The placement tool must tell users in advance that with a certain placement and type of interconnect, the MCM ought to have a certain number of layers. Essentially, it must look ahead and not only do the placement, but it should also be aware that the components are placed with the idea that they will be connected. Consequently, the net list must be available to this tool.

The placement tool should know some of the electrical characteristics of the chips. Therefore, if groups of pins on the chips are electrically equivalent, the tool can take advantage of it. It should work with the idea that the placement is there to make the interconnection simpler. In addition, it must give a rough estimate of whether or not the thermal, interconnect, and overall timing requirements will be met. That way, users won't have to route an entire MCM to find out their constraints weren't obtained.

Constraint-driven tools act together to achieve a user's goals. But many times the goals are contradictory. For instance, users don't want

too much thermal dissipation on the MCM, but on the other hand they'd like to have all of the chips together for performance reasons. There will be conflicts between goals, and the placement tool must help make difficult engineering decisions. "The most important MCM constraints involve timing," says Moreno, "because the main reason that users move from a pc board to an MCM is higher speed." According to Shiv Tasker, director of pc-board marketing at Valid Logic Systems Inc., constraint-driven tools should arrive within the next two years.

Silvar-Lisco, Sunnyvale, Calif., is an EDA company that's had years of experience with IC layout and routing. After carefully studying the MCM market, Marc Swinnen, a product marketing manager at the company, concludes that in the long run, the IC approach is much better than the pc-board approach. Swinnen points out that one big difference in the two approaches is placement and routing. IC place-and-route tools work with much finer geometries, and design-rule violations are stricter and more complex. Furthermore, the number of IC layers is much smaller: a pc board can have up to 22 layers while an IC router must typically work within three routing layers. These features, Swinnen points out, more closely match the needs of MCM technology than do pc-board tool features. Silvar-Lisco is currently working with several companies to determine specifications for MCM tools that will meet their needs.

According to the MCC project, an important routing-tool feature is its restartability. Different users have different requirements for MCM interconnections. For instance, in some technologies, they may want to daisy-chain certain pins, or may want to control the length of the stubs the router creates. They may even have their own algorithms for these requirements. Other users, however, may have a different idea for an interconnect. In that case, it may be necessary to invoke a different algorithm. What users need are various tools that can be called interchangeably. There must be the ability to



stop one and call another. It would also be helpful to limit the routed module's area. For instance, channeled routing is used in one area while a maze router is employed in other places.

Users want routing that completes to 100%. It's far too difficult in MCM design to do the last dozen or so wires by hand, mainly because of the density. Also, the MCC group determined that the router must handle at least ten signal layers and accept pads with arbitrary shapes.

In the future, there will be a move toward correct-by-construction design methods, such as constraint-driven routing. Specific constraints include thermal requirements and delay minimization per net. Delay minimization per net means the router must understand that for some

nets, the delay can't be more than this number or less than that number. In addition, the router should be able to constrain the number of routing layers and the maximum number of vias or junctions from layer to layer on a specific net.

Traditionally, routers try to minimize net length and achieve 100% completion. IC routers do consider timing delay. Some companies even have timing-driven layout and routing. In this case, not only net length is minimized, but users can also specify desired timing so that critical nets are routed correctly. On MCMs, that concept will be extended to more electrical parameters than just timing. Because of the devices' high speed, every line will have to be modeled as a transmission line. This requires that the router look at more

parameters than just net length and delay. Today, high-speed routing technology exists for chips, but not for chip-to-chip routing.

Both an IC and pc-board router are used by nChip to design its MCMs. Dick Lang, director of CAD for nChip, feels that a good router is an important factor in MCM design. He states that "they both have strengths, but both lack something when it comes to MCMs." His ideal router would have more constraint-based routing and a much better understanding of noise. For instance, the router would know when noise is building up and would avoid having too much noise in the first place.

A good delay model would also help. Right now, the delay models in most packages are simply a function of length. In reality, the function is

## SEMICONDUCTOR MANUFACTURERS MEET MCM NEEDS

**A**s the multichip-module (MCM) industry matures, it will be faced with demands for increased component density and higher clocks. Semiconductor manufacturers will be best suited to meet these demands with their IC-based MCM technology.

Semiconductor manufacturers have the know-how that's needed to fabricate multilayer MCM substrates. These substrates are often built up on a silicon-wafer base to eliminate the differential thermal expansion between the substrate and the mounted die. It's even possible to integrate peripheral passive or active components directly on the silicon substrate.

The basic process of layer deposition and photolithographic patterning is identical to IC processing. Other steps in MCM manufacturing, from die testing through bonding and packaging, are already part of a typical semiconductor production flow.

Semiconductor technology can achieve the necessary high densities and fine tolerances. Component packing densities will be limited by the achievable routing

density, as is already the case with VLSI chips. To control the characteristic impedance of long, high-speed lines in a multilayer environment, it's necessary to create precise, 3D geometries (strip lines for example).

There are a number of aspects that differentiate MCM from IC manufacturing: thermal analysis and transmission-line qualification add more constraints to MCMs. In addition, MCM multi-part assembly and final system testing will be quite different from the standard IC processing flow. There may be changes in the materials used, possibly substituting copper for aluminum and adding layers of insulation other than SiO<sub>2</sub>. Also, some features' dimensions, such as oxide thickness, may be an order-of-magnitude larger on MCMs.

These technological issues will need considerable research and development work to be resolved. Nevertheless, they're mostly evolutionary progressions from current IC techniques.

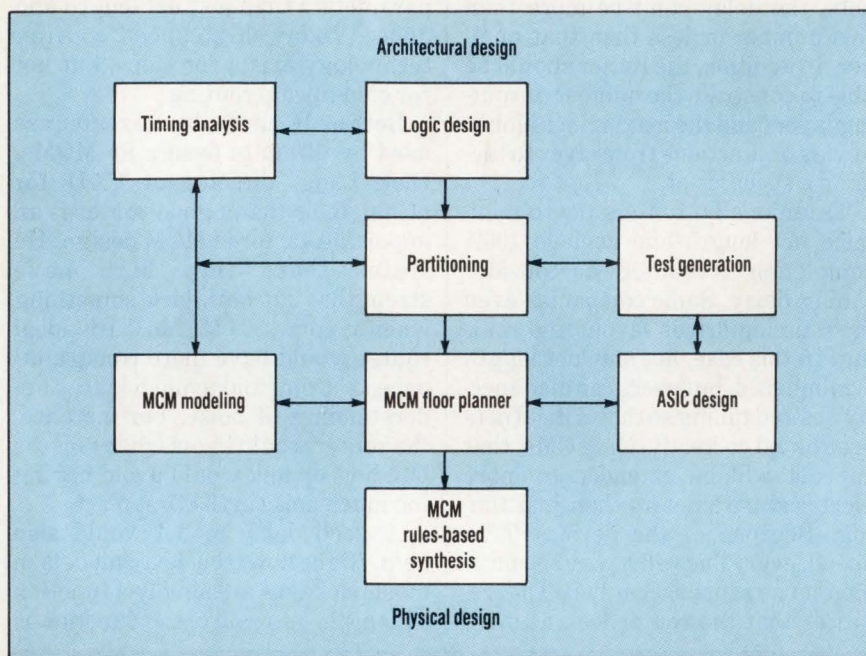
In addition, consider that IC dies will require special treatment by the semiconductor vendor before mounting on an MCM (bump-

ing of I/O pads, ruggedizing, TAB leadframe), and it becomes clear that MCM manufacturing is a natural extension to today's semiconductor business. Already, some of the major, vertically integrated semiconductor manufacturers in the United States, Japan, and Europe are gearing up to compete in this rapidly growing market segment.

Finally, it's important to note that semiconductor houses have long experience with the IC-based software tools that will be essential for the automatic placement and routing of increasingly complex and timing-critical MCM designs. Typical designs being completed today seldom have more than 100 placeable objects, and routing resources seem to be adequate. This will change in time, however, and users will demand more competent tools as they did in the pc-board and IC markets.

*Contributed by Marc Swinnen, product marketing manager at Silvar-Lisco, Sunnyvale, Calif. He has a MSEE and a master's degree in industrial management from the Catholic University of Leuven, Belgium.*

## MCM DESIGN TOOLS



**1. PARTITIONING IS A KEY STEP** in the MCM design flow because it lets engineers break systems into MCMs and ASICs. Linking the MCM floor planner with ASIC design, partitioning, and MCM modeling helps designers choose between various design alternatives. The layout is based on the constraints generated at the floor-planning stages.

one of material type or layer type, length, load capacitance, driver output impedance, and other factors. The width that the router uses should be a function of which net it's routing and what layer it's using.

Testing MCMs will be difficult, so users should design with testability in mind. In Moreno's opinion, the testing problem is closer to pc-board testing problems, but has very reduced dimensions. An MCM design-for-testability tool needs to be developed because a critical area in MCM design is how to test it. For example, should it be tested one layer at a time, and should engineers use IC production testers? Right now, designers don't know the best mechanism for MCM testing.

A partitioning and/or floor-planning tool is also needed. Users should have the ability to map their system to a module or a few modules (*Fig. 1*). After sections of logic are mapped into particular parts, users still must decide what technology to use. Tools should help partition according to the technology available and the goals that have been set. The floor-planning tools should be cou-

pled with analysis tools, such as thermal analysis. That way, users can explore trade-offs and possibly back-annotate that information to the schematics.

"Important MCM design-tool features are hierarchy and partitioning," according to Marc Swinnen at Silvar-Lisco. If a tool has no hierarchy, it can lose the distinction between what's on the chip and what's between the chips. Designers need tools that can recognize and reorganize the hierarchy. MCM tools must take one large design and spread it among two or three chips, then place and route those chips individually, and finally place and route the whole MCM with those chips.

In addition, flexibility of the tool will be needed. The design rules and the detailed methodologies used on the chips will undoubtedly be different than they will be on the MCM. Possibly, the chips may be of different technologies: a CMOS processor with several bipolar chips around it for drive, for example. The problem is, if the tool is going to handle that in any unified way, it must manage these different technologies and

must see the hierarchy and change its design rules.

The MCM tool suite must combine a number of areas. In addition to the physical-layout tools, such as place and route, MCM design will require extensive analysis software. "The physical layout packages are really only a small portion of solving the problems," says Shiv Tasker of Valid Logic Systems. "Analysis and simulation are an integral part of the MCM design process." For instance, with many ICs crammed onto a few square inches of substrate, thermal analysis becomes a necessity. Many of the analysis tools that are needed are available today, but not as an integrated MCM package. Today, it's up to the user to integrate the appropriate tools.

EDA vendors must decide if they will modify existing tools to suit MCM design, or whether they will create the MCM tools from scratch. Don DiMatteo, product marketing manager for Valid Logic Systems, points out that the current solution is expanding the capabilities of the existing tools to conform to the new materials used by MCMs. For example, a tool vendor may use a database to expand an existing tool's capabilities. Not all existing tools, however, have architectures that are flexible enough for this expansion.

Valid's MCM tool, called Allegro-MCM, was created by modifying the company's existing Allegro pc-board software (*Fig. 2*). All math functions were changed from integer to double-precision floating-point arithmetic to obtain the accuracy that MCMs require. In addition, the company had to remove all pc-board types of assumptions for such things as vias. Valid maintained Allegro's user interface and editing capabilities. Allegro-MCM, introduced last June, has three major components: a set of design tools to place and route MCMs, analysis tools, and the interface to manufacturing.

The three major ingredients for MCM CAD tools, according to Jacob Ben-Meir, product marketing manager for Mentor Graphics Corp.'s pc-board division, Beaverton, Ore., are place and route, physical analysis,



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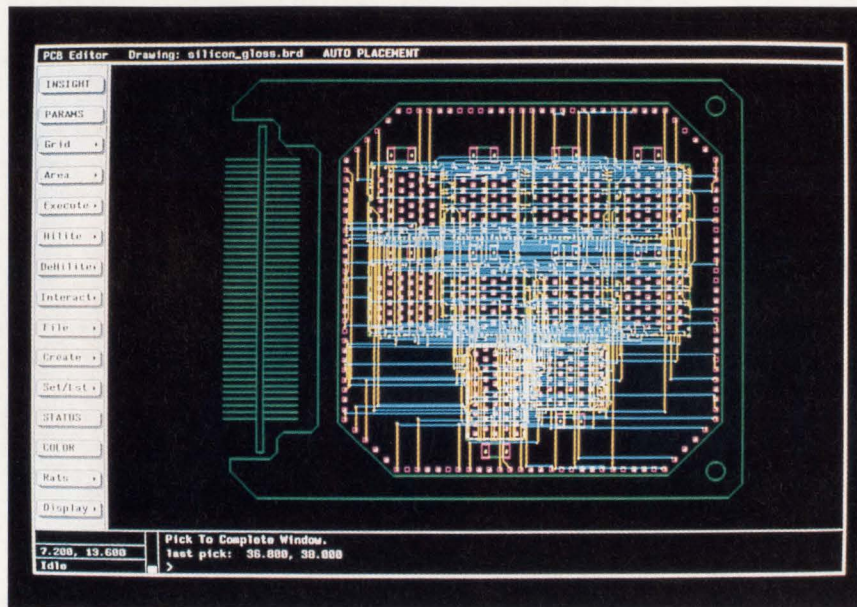
and thermal analysis. Ben-Meir states that today's tools are designed to solve constraints within the chip itself. Tool vendors must expand those constraints to handle multiple chips interconnected on one substrate. A big concern is how to blend physical analysis tools with router technology to meet the requirements up front.

Many good analysis tools are available today. For instance, Quad Design Technology Inc., Camarillo, Calif.; Quantic Labs Inc., Winnipeg, Canada; and Swiftlogic Ltd., Glasgow, Scotland; all have pc-board analysis tools that work well in analyzing crosstalk and transmission-line effects in MCMs.

nChip chose to go with the Cadence IC-oriented tool mainly because there's a much stronger suite of verification tools with chip design than with pc-board tools. The company has done well using those verification tools (they have a 100% success rate). Dick Lang of nChip considers verification to be the most essential, but not the most difficult, aspect of MCM design. He feels that IC tools do an adequate job of verification, except in electrical verification. With MCMs, electrical verification requires analyzing nets, including information about the drivers and loads on those nets. The company uses pc-board analysis tools for electrical verification.

Thermal-analysis tools are available today. Thermal analysis is important because many MCMs are heavily populated with surface-mounted parts. The surface-mounted parts sit much closer to each other so the heat dissipation is greater. Designers need to decide whether to use air or liquid cooling. The thermal tools should perform power calculation for the individual chips and for the entire system. The tools must ensure thermal stability by understanding whether or not the cooling method will work based on the placed-and-routed design.

Crosstalk and transmission-line effects, like overshoot and undershoot, run rampant in MCMs. The analysis tools must determine whether or not the design meets the



**2. THIS MCM IS CREATED** using Valid's Allegro-MCM tools. It consists of a two-signal-layer pc board that has ultrafine lines and embedded power and ground planes.

allocated noise margin. In addition, it should help determine how much of the noise margin will be used up by each type of transmission-line effect, such as ringing and reflection. The analysis results should be back-annotated into static-timing verification and simulation tools for post-route verification.

MCM tools will need strong links between the analysis and layout tools to achieve this back-annotation. Users will need to simulate on the actual physical layout vs. simulating on just the schematic. High-speed circuitry dictates that the tools simulate timing associated with trace lengths, and the tools must feed trace capacitance and delays back into the simulator to make sure the circuit is going to actually work.

Overall integration is also important, because the necessary tools don't all come from the same vendor. No one vendor has all of these analysis capabilities. Interfaces are needed to keep the designer within one framework. One framework is essential because the typical system designer is working between chips, MCMs, boards, and backplanes, and needs to have the flexibility to partition between those elements. Dick Lang at nChip asserts that floor-planning tools that help predict cost

and performance at a reasonably high level of abstraction are important, especially when designing chips specifically for MCMs.

Don DiMatteo at Valid thinks the future will see IC tools and MCM tools becoming more tightly integrated. Engineers designing their own ASICs will want to change them on-the-fly to improve the routing on the MCM. In most of today's systems, it takes two different tools and two different processes to do this. For example, most IC designers aren't concerned with the pinouts on the IC and the I/O pad locations. Those can be critical on an MCM. Moving a pad from one side of the chip to the other may help an engineer bring components closer together, and that in turn will improve MCM routing. The future MCM design environment will have constant updates from the ASIC or IC layout. The ability to go back and forth and back-annotate that data is going to be critical. A closer-knit environment, says DiMatteo, can be achieved with a good framework. □

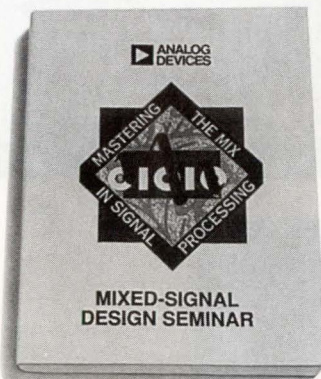
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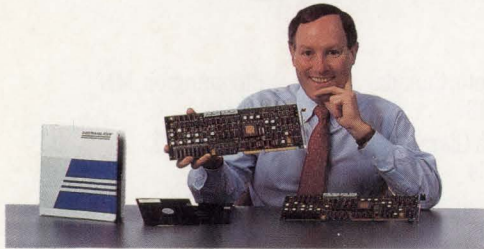
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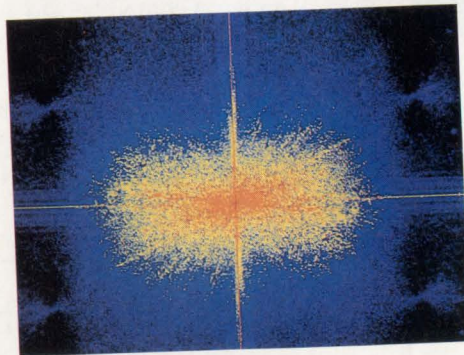
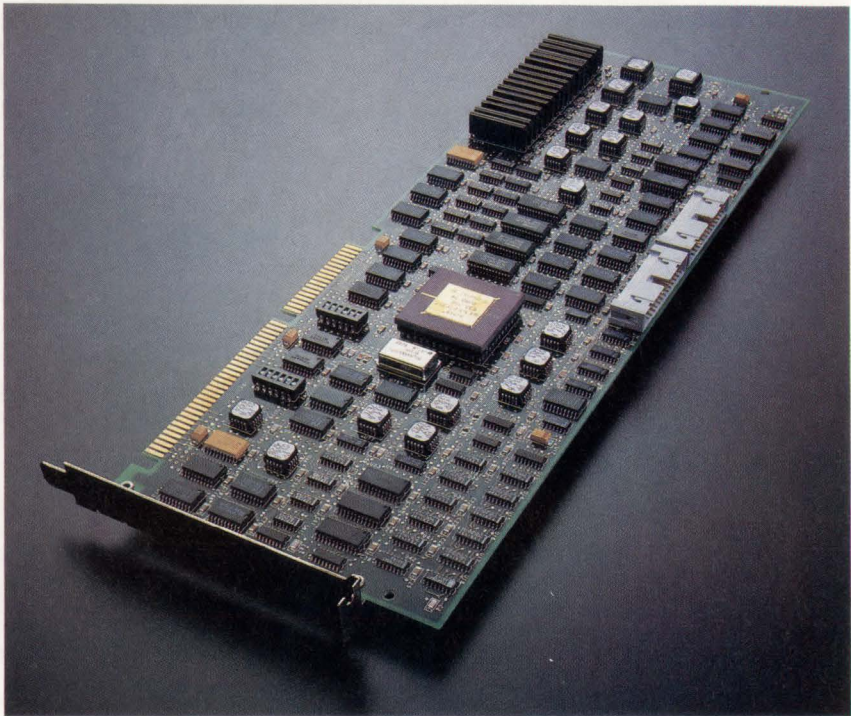
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# TEST & MEASUREMENT

A SPECIAL EDITORIAL FEATURE

## Additions to the VXIbus standard will enhance operating performance

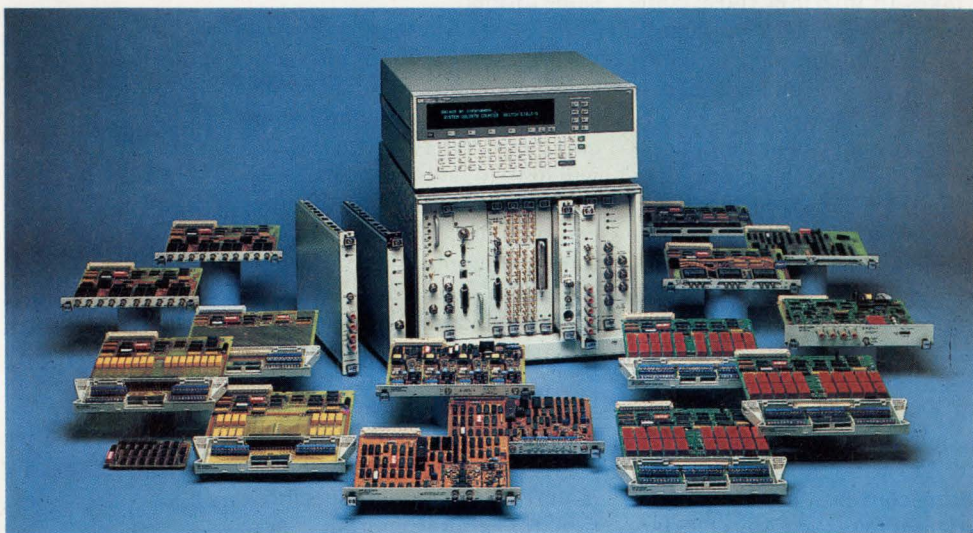
*The consortium that created card-modular VXIbus instrumentation is still hard at work.*

BY JOHN NOVELLINO

**A**lthough the VXIbus standard is more than three-and-a-half years old, the work of the VXIbus consortium is far from over. Though no big changes are emerging, several minor additions to the standard aim at ensuring interoperability and enhancing performance. Moreover, members continue to test actual products for their interoperability, as well as the standard's robustness.

The current version of the document, 1.3, defines certain items more vigorously to eliminate interpretations that caused some initial interoperability problems. These problems primarily dealt with the VXIbus resource manager in identifying, at power-up, all of the devices in the system and what specific features they support. The added language leaves less room for module manufacturers to interpret the standard differently, therefore ensuring compatibility between devices.

But consortium members have done extensive testing and believe the basic standard will now hold up in its current form. Product testing continues, however, both to increase confidence in the specification's robustness and to monitor how manufacturers are reading and understanding the document. Makers of VXI devices needn't submit their products for interoperability testing, but most of the ma-



major players feel such testing is in their best interests. To accommodate the testing, the consortium holds interoperability meetings every three months, or as needed.

One area that has caused some debate in the past year is the original standard's shared-memory protocol. The shared-memory option aimed at speeding up data transfers and allowing modules to communicate outside of the typical commander-servant relationship. But testing to ensure the protocol's completeness devoured more time than originally thought. So shared memory was dropped from revision 1.3 and is now included in a separate, rather thick document that probably will be

added as an appendix.

In practice, that appendix may never be used by most engineers implementing VXIbus test systems. Other simpler ways of greatly boosting data transfer rates—the primary goal of users interested in shared memory—are available. The consortium is codifying these methods in a document that should be approved very shortly.

**A**ccording to John Graff, VXI product manager at National Instruments, Austin, Texas, “The problem was that the shared-memory protocol being developed by the consortium was a very high-level transport protocol. It was very detailed and very elaborate, but not

## ■ VXIBUS PERFORMANCE ENHANCED ■

something the typical user could grasp easily." More likely, module manufacturers would use the protocol to allow their devices to communicate together, he said.

Because most users only need a faster way to transfer large blocks of acquired data, the consortium separated that goal from the desire to break down the commander-servant relationship, says Larry DesJardin, VXIbus technical program manager at Hewlett-Packard's Loveland Instrument Div., Colo. In fact, because VXI uses high-level commands, the time it takes to interpret those commands is more of a bottleneck than the time needed to handshake those commands across the bus.

The result is what the consortium is calling the block data format. "What we decided to do is describe where and how you put block binary data into memory and then agree on a few number formats," says DesJardin. These formats include 8-, 16-, and 32-bit integer and 32- and 64-bit real formats, all IEEE standards.

"We just put some byte-ordering conventions on where the different bytes go," says DesJardin. "All we did was document standard practices."

The plan is to have every device reading or writing data in the user's chosen format, whether the devices are message- or register-based, or even if they're VME cards. Ideally, the format will be the same as that used by the computer controlling the VXI system. Then as the computer receives the data, it will be ready for immediate processing without the need for any additional conversion.

The result is that the VXIbus system's theoretical bandwidth should be the same as that of the VMEbus, or 40 Mbytes/s. The system can run as fast as the VMEbus drivers without being slowed down by a handshake protocol.

The next revision of the VXI-

bus specification will also contain several relatively minor additions that will make the standard more useful and easier to implement. One is the definition of extended register-based devices. The added registers can hold module serial numbers and other information. Another is the inclusion of some new word-serial commands oriented around device identification. And some common ASCII resource-manager commands will enable users to ask a manager what devices are in a system. All managers will respond in the same format.

**T**he consortium is also adding some standard mnemonics to speed up the use of common VXI resources. Users will have to know only one set of these codes for all manufacturers' modules. The VXI consortium will submit these mnemonics to the consortium working on the standard commands for programmable instruments (SCPI). The VXI group is working on the VXIbus-specific portion of the SCPI standard.

Also close to approval is a mainframe extender specification for multi-mainframe systems. On the VXIbus side of the extender cable, the consortium agreed to use the National Instruments MXIbus implementation for multi-mainframe systems. The cable side of the interface will be left open so that users can employ any medium they desire, even fiber-optic hardware for long runs between mainframes.

A major trend in VXIbus is the move to higher-performance modules. To get the industry off to a fast start, many manufacturers initially introduced VXI modules leveraged off the companies' discrete instruments. Although these products fulfilled VXI's promise of downsized systems and interoperability, their performance was basically the same as their discrete counterparts, a fact that did not go

unnoticed by many prospective VXI users.

But that uninspired performance is starting to change. One example is the VX4240 waveform digitizer/analyzer from Tektronix/Colorado Data Systems, Englewood, Colo. The C-size module uses a 12-bit 10-MHz analog-to-digital converter (ADC) and a RISC transputer to capture waveforms to 5 MHz and perform extensive analysis and signal conditioning on them.

Another high-performance unit is the 2351-EMD time-interval analyzer from Racal-Dana Instruments, Irvine, Calif. The instrument, which fits into a double-wide C-size module, contains a 68020 processor and a math coprocessor for near-real-time signal analysis. Measurement resolution is 8 ps.

Another point of contention with users is VXIbus cost, according to Lou Klahn of Tektronix/CDS. His company's answer includes two full-function Slot 0 controllers priced under \$2000. But Klahn also notes that many candidates for VXIbus don't realize that they don't have to change their whole existing system to take advantage of the standard. Engineers upgrading their test setup can replace a portion of it with VXIbus instruments that will work with the remaining discrete units.

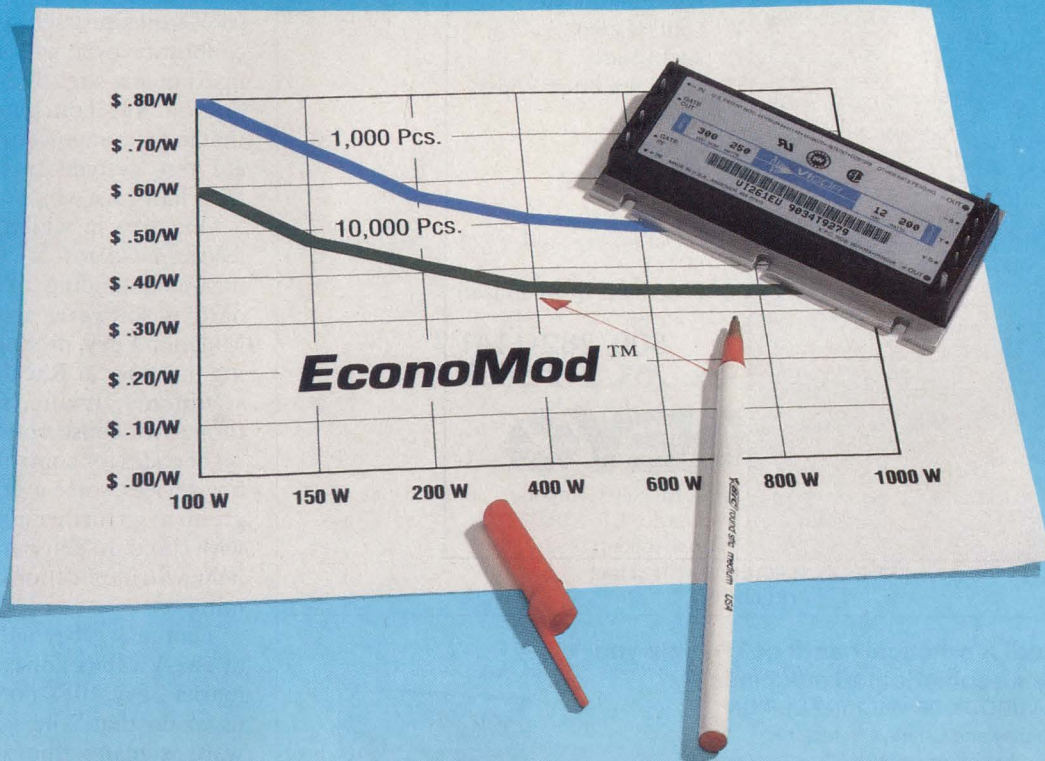
**A**ccording to Klahn, that realization is part of a larger education problem manufacturers face. Furthermore, they must show potential users that VXI means more than downsizing. "What you're really dealing with is a predictable, closed environment for instrumentation that allows you to get your arms around a lot of traditional system-type problems that nobody could get their arms around before," says Klahn.

A prime example is in the calibration of large, multi-instrument systems. In such setups, Klahn notes, tolerance build-up

**Many candidates for VXIbus don't realize that they don't have to change their whole existing system to take advantage of the standard.**



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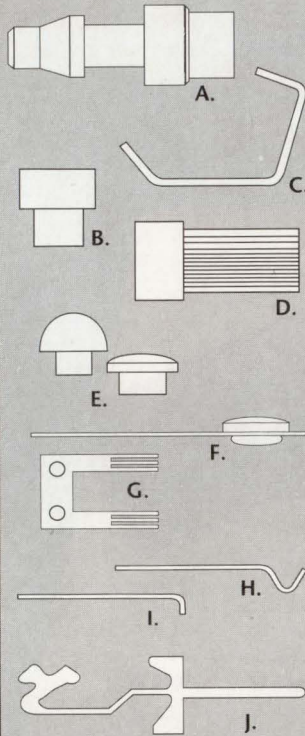


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can cause the system as a whole to be out of calibration, even though each individual instrument is within limits. On the other hand, a properly integrated VXIbus test setup can be in calibration even with individual instruments slightly out of calibration. As Klahn puts it, telling that to most engineers who operate test systems would make their hair turn white.

One area in which customer feedback seems to indicate a misunderstanding of the standard is software, according to Malcolm Levy, product marketing manager at Racal-Dana Instruments, Irvine, Calif. Although the consortium defined a set of codes for controlling VXIbus devices, some users want the group to go further and come up with standard software that will help with applications programming.

That task is beyond the scope of the VXIbus consortium, remarks Levy. "It's not really for us to do that," he says. "Software is many things to many people. We feel that the first step is to make sure that we can all communicate with each other and not to have to some sort of test-software architecture fully defined. That would take the whole thing into another realm."

Levy also says that engineers should be aware that VXI is not just for low-frequency applications, a misconception some still believe. He notes that Racal-Dana introduced a microwave VXI chassis and prototyping cards. Also EIP Microwave Inc., Milpitas, Calif., has introduced a microwave frequency counter in a three-slot-wide C-size module.

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# Configuring your first VXIbus test setup

*A step-by-step process eases the novice user's way to a successful system.*

BY LARRY DESJARDIN

Hewlett-Packard Co., Loveland Instrument Div., P.O. Box 301, Loveland, CO 80539; (303) 679-3207.

The extremely wide range of possible applications and the multiple-manufacturer intent of the VXIbus architecture preclude products from arriving precisely preconfigured for every application. Users, therefore, must determine the final system configuration before operation. First, the proper instrument modules should be selected. Next come any additional system modules and, finally, the mainframe. Users can then determine the system configuration and install the modules. Once this point is reached, application programming can begin (Fig. 1).

To configure any test system, VXIbus or otherwise, test engineers must first detail the system's measurement requirements, typically in terms of source, sensor, and switching functionality. They can then scan catalogs and data sheets from various manufacturers to find the optimum module set for these measurement needs.

To facilitate this search, the VXIbus standard requires every manufacturer to specify the system attributes of its VXI products. For instrument modules, this includes module size, number of slots, power and cooling requirements, and the module's intelligence (whether it's message or register based). Typically, manufacturers will also describe VXIbus subsystem requirements (10-MHz or 100-MHz clock, SYNC100 or STARXY triggering, P2/P3 connectors, etc.), as well as any other modules needed for a practical system. Users must note this information for each instrument module before selecting the system modules and mainframe.

**TABLE 1: TYPICAL INSTRUMENT MODULE DOCUMENTATION**

MODULE SIZE, NUMBER OF SLOTS: B, 2		
CONNECTORS: Required: P1 Optional: P2		
COOLING REQUIREMENTS: Watts/slot: 6 Airflow/slot: 0.5 liter/second at 0.25 mm H <sub>2</sub> O for 10°C rise		
POWER REQUIRED:		
	Current	
Voltage	Dc-peak (I <sub>Pm</sub> )	Dynamic (I <sub>Dm</sub> )
+5 V	1.0 A	15 mA
+12 V	20 mA	0.1 mA
-12 V		
+24 V		
-24 V		
-5.2 V	1.0 A	20 A
-2 V		
+5 V stby	100 μA	10 μA
INTELLIGENCE: Device type: Register based Memory required: 1 Mbyte, A24 Commander: Acme 123 or Acme 456 Commander required for ASCII communication. Fully documented register map for register-based communication.		

Documentation is typically noted on a VXIbus product's data sheet. Table 1 shows an example. The module is a 2-slot B-size unit. It requires at least a P1 connector on the mainframe, but also accesses a P2 connector if provided. At 6 W per slot, the module dissipates 12 W. The data sheet also provides a detailed air-cooling specification for precise mainframe matching.

The dc-peak current, I<sub>Pm</sub>, consumed by the module will be used to determine the current capacity required of the mainframe.

Dynamic current, I<sub>Dm</sub>, specifies an equivalent ripple current for the module. This figure ensures that the power-supply ripple voltage is within the specified VXIbus ripple limits.

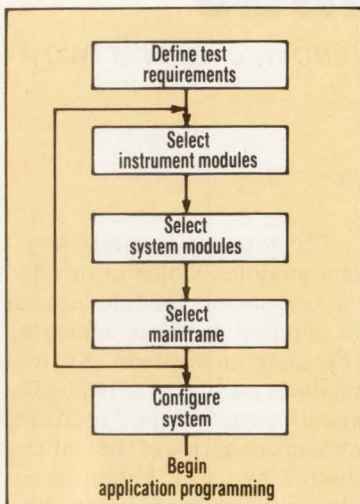
The next step is selecting system modules, which in this discussion are any modules needed in addition to those delivering the instrumentation. System modules may be required by the specific instrument modules chosen or because of the features desired by users. Examples include the VXIbus Slot 0 module, interfaces to the host computer (for example, IEEE-488 or RS-232), command interpreters, extenders, internal computers, and so forth.

The VXIbus standard defines the Slot 0 module. This card delivers the 10-MHz clock on the CLK10 VXIbus lines and accesses the module identification pins of the other modules. In the largest D-size systems, the Slot 0 module may also include the 100-MHz clock as well as the precision trigger features of SYNC100 and STARXY.

Users should check the instrument modules to determine what Slot 0 functions are required. They must also note any other required specifications, such as clock accuracy or jitter. From this information, users can verify that a particular Slot 0 module meets all system requirements. Typically, instrument module manufacturers will list particular Slot 0 modules that meet their products' requirements. At least one of these units should do the job for all of the selected instrument modules.

Because the Slot 0 module plays a unique role in a VXIbus system by being a common system-resource module, many of these cards include other functions that can be used by other system components. For instance, typical Slot 0 modules include an IEEE-488 interface,

# VXIBUS CONFIGURATION



1. Developing a VXIbus test system should be viewed as a step-by-step procedure. In this process, early decisions should affect later selections of equipment.

the VMEbus system controller (bus arbiter), the resource manager, and possibly embedded firmware that allows register-based instruments to communicate as message-based instruments. Such a combination is commonly referred to as a command module.

If an external host computer is to control the VXIbus instruments, there must be a link from the host to the VXIbus system. Initially, the most common link will be IEEE-488 (GPIB), but the user may also select a local-area network (LAN), an RS-232, or a direct VME interface such as MXIbus.

Once the interface type is known, the user may select the corresponding VXIbus interface module, or save a slot position by choosing a Slot 0 module with an interface. Documentation that's typically found on a data sheet for an IEEE-488 VXIbus interface module is shown in table form (Table 2).

The specification defines two types of modules that will be common implementations for instruments: register-based devices and message-based devices. Command interpreters are needed to communicate in high-level instrument language to the simpler of the two basic types of VXIbus modules.

Typically, register-based devices will be simple modules that

respond to binary register reads and writes over the backplane. These modules tend to be small, inexpensive, and because of the direct binary register access, extremely fast. Examples of likely register-based devices include switches, digital I/O cards, and simple ADCs and DACs.

On the other hand, message-based devices follow the VXIbus word-serial communication protocol. They're typically intelligent devices with embedded microprocessors that receive and execute ASCII commands. Most sophisticated instrument modules will be message-based devices, although they may also contain register access for applications in which throughput is important.

To program a register-based module with a high-level ASCII command language—for instance, the Standard Commands for Programmable Instruments (SCPI)—a message-based module is needed. The message-

based device will serve as the register-based unit's commander and transparently translate the high-level command language into register reads and writes. Manufacturers of register-based devices will specify message-based modules that can perform this task.

The translator module may stand alone, or it may be combined within a command module. Often a manufacturer will specify a message-based module that can translate for all of the company's register-based instruments, making them appear from any host to be message-based. This makes it possible for users to choose between convenience (ASCII English-like commands such as SCPI) and performance (direct binary register access).

To maximize system speed, users may want to communicate with a register-based device at its register level. If so, the interface module must have the register access capability needed to do this. This simple capability is included on nearly all interface modules.

After the instrument and system modules are selected, users can choose a mainframe. Considerations include module size (A, B, C, or D), number of slots, power dissipation for each supply voltage, cooling capability, and VXIbus backplane implementation (P1, P2, and/or P3).

The size of the largest module will determine the mainframe size required. If smaller cards are to be inserted into a larger mainframe, users should acquire the proper adapter fixtures. These will typically be bus extenders or carriers. Larger systems with many modules will need multiple mainframes. These can be configured by employing backplane extenders or by placing an interface module to the host computer in each mainframe.

Modules that will be coupled to each other using the trigger or

TABLE 2: TYPICAL INTERFACE MODULE DOCUMENTATION

IEEE-488-TO-VXIbus DATA SHEET			
- Single-primary, multiple secondary GPIB addressing			
- Secondary address determined by five most significant bits of module's logical address			
- Full resource manager capability at secondary address 0			
- Slot 0, VMEbus system controller capability			
- Full register access capability			
MODULE SIZE, NUMBER OF SLOTS:			
C, 1			
CONNECTORS:			
Required: P1, P2			
COOLING REQUIREMENTS:			
Watts/slot: 12			
Airflow/slot: 1.0 liter/second at 0.25 mm H <sub>2</sub> O			
POWER REQUIRED:			
Voltage	Current		Dynamic (I <sub>Dm</sub> )
	Dc-peak (I <sub>Pm</sub> )		
+5 V	2.0 A		15 mA
+12 V	20 mA		0.1 mA
-12 V			
+24 V			
-24 V			
-5.2 V	100 mA		10 mA
-2 V	50 mA		5 mA
+5 V stby			
INTELLIGENCE:			
Device type: Message-based commander, resource manager, Slot 0			
Memory required: 64 kbyte, A24			
Commander: of Acme 100 series register-based instruments			

## ■ VXIBUS CONFIGURATION ■

sumbus lines should be placed inside the same mainframe. The mainframe's power supply must be able to handle the total of the modules' individual dc-peak currents and the total of the dynamic currents.

Next, users must ensure that the mainframe's cooling capacity is sufficient. A quick check suitable for many applications is to compare the worse-case power dissipation of any module against the mainframe's abbreviated cooling specification. This specification will typically be in units of watts/slot.

Different manufacturers, however, use different assumptions when specifying mainframe cooling capabilities in units of watts/slot. Consequently, this figure should be used to verify compatibility only when the mainframe manufacturer's abbreviated cooling specification exceeds that of the highest power-density module by at least a factor of two.

For more precise verification, mainframes and modules must specify cooling in terms of airflow rate versus back pressure (Fig. 2). This more detailed check is recommended whenever the module power dissipation is within 50% of the mainframe's cooling capacity.

A- or B-size modules, however, are only half as deep as their larger counterparts. Consequently, in a C- or D-size mainframe, an A- or B-size module will receive only half the airflow of C- or D-size modules. To ensure compatibility, users should convert a smaller module's specifications to equivalent C- or D-mainframe values. That's done by doubling the module's watts/slot and airflow volume figures (but not the back-pressure specification).

For instance, if a B-size module specifies:

watts/slot: 15  
airflow/slot: 0.1 liter/second at 0.05 mm H<sub>2</sub>O for a 10°C rise,  
then an equivalent specification

TABLE 3: MAINFRAME SELECTION PROCESS		
Define mainframe requirements:		
Module size: Largest of any module. (A, B, C, or D, from small to large)		
Number of slots: Sum of slots specified by each module. (May require multiple mainframes. Maximum VXibus subsystem chassis is 13 slots, Slot 0 plus 12 instrument slots.)		
Power supply: Sum current needed for each supply voltage by all modules.		
	Peak current	Dynamic current
+5 V	5.0 A	4.0 A
+12 V	3.0 A	3.0 A
-12 V	1.0 A	1.0 A
-5.2 V	10 A	10 A
-2 V	4.0 A	3.0 A
+24 V	0.5 A	0.5 A
-24 V	0.25 A	0.5 A
Backplane: P1, P2, or P3? (P1 mandatory, P2, P3 optional depending on modules.)		
Cooling: Abbreviated: use highest watts/slot of any module. Detailed: Compare module flow rate versus back pressure against mainframe specifications.		
Choose mainframe that meets all the identified size, power, backplane, and cooling requirements.		

for a C- or D-size mainframe would be:

watts/slot: 30  
airflow/slot: 0.2 liter/second at 0.05 mm H<sub>2</sub>O for a 10°C rise.

Sometimes a test system can tolerate larger temperature rises. For example, if the test station's ambient intake air temperature is low, a larger rise may be allowed.

If a larger temperature rise is permitted, users can determine cooling requirements by multiplying the module's airflow/slot volume and back pressure values by the ratio of the module's specified temperature rise to the revised temperature rise. For instance, if airflow/slot = 0.5 liter/second at 0.2-mm H<sub>2</sub>O for a 10°C rise, then airflow/slot = 0.25 liter/second at 0.1-mm H<sub>2</sub>O for a 20°C rise.

For mainframes with temperature-controlled variable-speed fans, users can compare the largest airflow curve (highest temperature) against the module's nominal 10° rise specification. The mainframe manufacturer already takes temperature rise

into account for the lower-temperature fan speeds.

Finally, users must specify whether the system needs the P1, P2, or complete P3 backplane. Most mainframes will offer the maximally configured backplane for the module size.

The mainframe selection process can be easily codified into a step-by-step procedure (Table 3). In reality, the procedure can be further simplified. The process can usually start with the mainframe recommended by the manufacturer of the largest number and highest power-density modules. And if users prefer a particular mainframe, they may opt for smaller and less power-consuming modules. This is particularly common if the preferred mainframe is only marginally underpowered, or if one large module originally forced the need for a larger mainframe.

Once the modules and mainframes are selected and delivered, users can configure the system. The primary task at this point is to set the proper logical addresses for each module. VXibus devices will have logical addresses ranging from 0 to 255, which are typically set by switches on the module.

Logical address 0, which is reserved for the resource manager (typically the Slot 0 card), should be set first. Address selection for the remaining modules is left to the user, and is constrained only by commander-servant relationships and a requirement for uniqueness. A commander is a module that controls one or more other modules, called servants. The commander may be a message-based device that translates for register-based devices, or an IEEE-488 interface module that controls the internal instruments. Embedded controllers are also commanders.

The VXibus specification describes a simple algorithm that unambiguously defines which

**The VXibus mainframe selection process can be easily codified into a step-by-step procedure.**

## ■ VXIBUS CONFIGURATION ■

modules, based on their logical addresses, will be servants to a particular commander. Essentially, each commander has a servant pointer switch that's set by the user. The switch defines the maximum number of servants a commander may have, starting with the next logical address. For instance, if a commander at address 10 has a servant pointer of 5, the commander may control devices at addresses 11 through 15.

If another commander lies within this "servant space," the first commander can control the second commander as well. But modules in the second commander's servant space can be controlled only by the second commander.

In other words, a commander may be a servant to another commander in a hierarchical system. Likewise, if a module is in the servant space of more than one commander, that module will only be the servant to the commander with the greatest logical address.

**O**ne way to assign logical addresses for a system is to list all servant-only modules vertically on a piece of paper, grouped by common commanders. Then users can insert the commander for each group above its block of servants. Any higher layers of commanders can go just above the commanders they control. The resource manager heads the list. Users then number each module consecutively, starting with zero for the resource manager. These numbers correspond to the modules' logical addresses.

To allow for system growth, users can occasionally skip a number, or number by twos or threes. Most commonly, the interface module being used will define an address-mapping scheme that will naturally spread the logical addresses. For instance, instrument logical addresses are typically configured to a multiple of eight, because

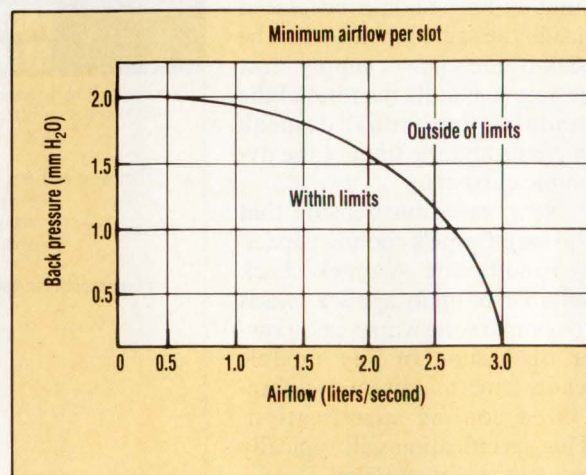
most command modules map the five most significant bits of the logical address into the GPIB secondary address, while the three least significant bits are set to zero.

To determine the servant-pointer value for each commander, users locate the servant module with the highest logical address (lowest on the page) that belongs to each commander. Subtracting the logical address of the commander module from that of the servant module yields the value of the servant pointer. The modules' logical addresses and servant pointers can now be set.

With the commander-servant hierarchy decided, the last configuration task is to determine the system's interrupt structure. Interrupts are an optional way for a servant to communicate to its commander. The VXI backplane has seven interrupt lines, and a commander will typically monitor one particular line for all of the commander's servants. The commander then is called an "interrupt handler," and each of its servants may be an "interrupter."

Interrupt capability is optional; many devices don't have it. Message-based devices using the signal register don't need interrupt capability at all, eliminating this part of the configuration process. However, if there are interrupters, the system must be configured so that there's only one interrupt handler per line, and servants must only interrupt on their own commander's interrupt line.

As in the case of the commander-servant hierarchy, a simple configuration algorithm exists. First, list all commanders that have a servant interrupter. Then sequentially assign an interrupt-line number to each listed commander, from 1 to a maximum of 7. This list sets the proper interrupter level on the servant modules, and the proper interrupt handler level on the commander modules.



2. When the total power dissipation of the system's modules gets to within 30% of a mainframe's cooling capacity, system designers should check more detailed specifications. This graph of back pressure versus airflow gives more precise guidance.

If any of the modules support programmable interrupter or handler levels instead of having module switches, the resource manager will program the proper levels. The user, however, must report the interrupt line of each interrupt handler to the resource manager. Typically, this is done through a command or a nonvolatile memory. The procedure will be described in the resource manager's manual.

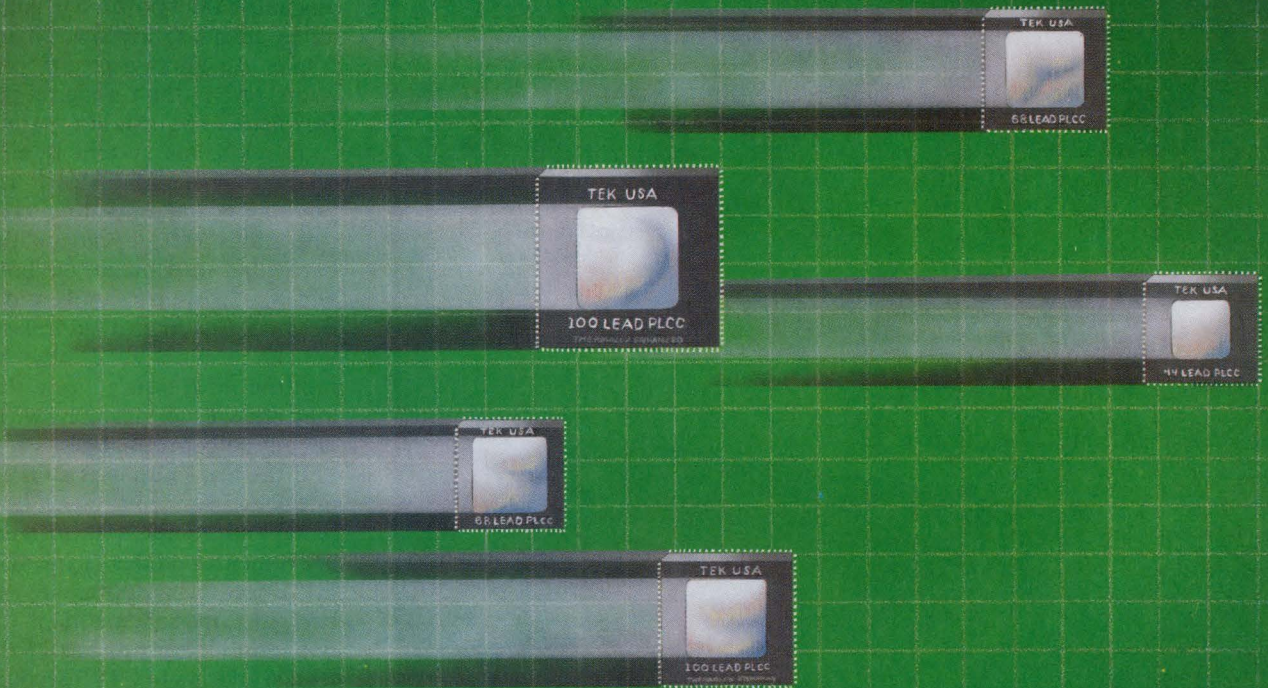
The configuration's design is now complete. The user can set the logical address of each module and the servant pointer on each commander, as well as the interrupter and handler levels.

At this point, the modules are ready to be inserted into the mainframe. Slot 0 modules should be placed into their positions, and the remainder of the modules placed in adjacent slots starting at Slot 1.

**P**lacing modules in adjacent slots maintains the five daisy-chain signals of the VMEbus backplane. If modules aren't placed in adjacent slots, the VMEbus daisy chains must be maintained using jumpers on the backplane, or jumper modules inserted from the front.

Recently introduced mainframes (such as the HP E1400B) include self-jumpering connectors that configure the backplane automatically, eliminating this one configuration task completely. As a final step, some

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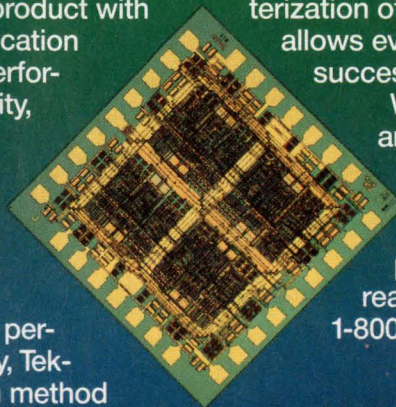
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mainframes may require faceplate modules to be inserted into any unused slot position to guarantee adequate airflow. Mainframes using pressurized air plenums often don't require the faceplates to be installed.

The VXIbus system is now ready to program. Most programming and operating considerations will depend on the particular instrument modules and the system's application. Because the logical addresses, not slot numbers, determine the module addressing, modules may change slot positions without any software changes.

If the test setup uses a GPIB interface, users must check how it maps addresses to the internal instrument modules. Typically, GPIB secondary addressing will be used. This scheme maps the five most significant bits of the logical address to GPIB secondary addresses. Multiple primary addresses, as well as textual addressing embedded in a message, are also allowed.

Specific testing applications may require other system topologies. But they're essentially variations of the above configuration process expanded to address some unique feature or capability.

*Larry DesJardin is the VXIbus technical program manager at Hewlett-Packard's Loveland Instrument Div. He is the company's representative to the VXIbus Consortium and received the John Fluke Sr. Memorial Award for his contribution to the creation of the VXIbus standard. DesJardin received his BS in engineering from the California Institute of Technology in Pasadena and his MSEE from Stanford University.*

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## VXIBUS PRODUCTS

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The 73A-155 RM/488 interface module is a high-performance Slot 0 device with advanced triggering, comprehensive resource management capabilities, and an IEEE-488 interface. The module permits external or internal trigger generation, trigger fan-out, trigger protocol translation, and automatic time/pacer functions. Slot 0 functions include a 10-MHz differential ECL clock driver for the backplane and transceivers for the VXibus MODID lines. Built-in test equipment executes a self test at power-up, on direction of a VXibus

hard reset, or on command. The 73A-155 costs \$2800. Delivery is within 6 weeks from receipt of an order.

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### ▼ 2-SLOT MODULE CAPTURES SIGNAL NONLINEARITIES

Frequency nonlinearities on swept and CW signals can be measured with the 2351-EMD. The 2-slot, C-size VXI module incorporates a 68020 processor and a math coprocessor

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**▼ IMPROVED DRIVER WORKS WITH ADDITIONAL SYSTEMS**

Version 2.0 of the NI-VXI software driver for VXIbus systems runs under OS/2, Windows, and SunOS operating systems in addition to DOS, SCO XENIX, SCO Unix, ISC 386/ix, AIX, and Macintosh OS. The driver



includes functionality for various multitasking and nonmultitasking software environments. Functions are now structured so that multitasking and nonmultitasking implementations have the same function-level interface. Newly added functions make it possible for the system computer to operate as a servant. The NI-VXI software is packaged with National Instruments' embedded controllers and interface kits. Prices range from \$3800 to \$16,860, depending on host platform and operating system.

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**▼ SOFTWARE CREATES VXI PROGRAMS AUTOMATICALLY**

With WaveTest/VXI (WaveTest Version 2.6), test-system programmers can generate VXI and GPIB test programs automatically using flowcharts or modules. The icon-based programming environment is syntax-free and runs under Microsoft Windows. The software makes the VXI or GPIB interface transparent, allowing direct control of the instruments through computer-generated front panels. After initial configuration setup, WaveTest/VXI handles all communication protocols and details. VXI and GPIB instruments can be supported in one system using one controller. WaveTest/VXI includes an instrument database library and instrument library generator to characterize new VXI or GPIB instruments or to customize libraries. WaveTest/VXI costs \$1995 and is available from stock.

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**▼ MEMORY, DISK OPTIONS ENHANCE CONTROLLERS**

A 16-Mbyte system memory and two disk options enhance the performance of the EPC-2 and EPC-2e C-size embedded controllers. The two 386-based computers come with 40-Mbyte hard disks, but can now be ordered with 100- or 200-Mbyte options. The larger drives have average access times of 15 ms and are compatible with all standard PC programs, including Unix software. The 16-Mbyte RAM option is available on both the 16- and 20-MHz versions of the controllers. In addition, the EPC-2e Ethernet-compatible controller now works with standard Unix, TCP/IP, and DECnet software. The 100- and 200-Mbyte disk options cost \$800 and \$1600, respectively. The 16-Mbyte RAM goes for \$4060. All are available immediately. The price of the standard 16-MHz EPC-2 was recently dropped to \$5995.

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**Racal-Dana Instruments Inc.**  
4 Goodyear St.  
Irvine, CA 92718  
(714) 859-8999  
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**Westinghouse Electric Corp.**  
Integrated Logistics Support Div.  
111 Shilling Rd.  
Hunt Valley, MD 21030  
(301) 584-5700  
► **CIRCLE 349**

**NEWSLETTER AVAILABLE**  
The **VXIbus Newsletter** is published 10 times a year by Fred Bode, who helped develop the specification as an original member of the VXIbus consortium. The newsletter covers all aspects of VXI, including new products, technical papers, and changes and additions to the specification. It also follows the ATE industry in general to monitor the standard's adoption and progress. Sample copies are available from Bode Enterprises, 8380 Hercules Dr., Suite P3, La Mesa, CA 91942; (619) 697-8790.

## VXIBUS PRODUCTS

### ▼ VXIBUS COUNTERS WORK TO 170 GHz

The EIP 1230A pulse/CW microwave frequency counter covers 100 Hz to 26.5 GHz, with optional extensions to 170 GHz. The 3-slot-wide, C-size module measures pulse widths down to 50 ns and pulse periods as short as 250 ns, as well as carrier frequency. Frequency extension is achieved using remote sensors that eliminate the disadvantages associated with high-frequency cabling. A companion product, the 1231A, covers up to 20 GHz. The counters use digital averaging. The 1230A and 1231A cost \$17,000 and \$12,700, respectively, with delivery 12 weeks after receipt of an order.

#### **EIP Microwave Inc.**

1589 Centre Pointe Dr.

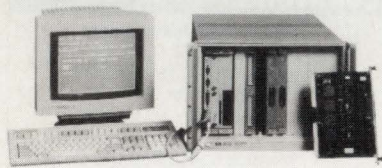
Milpitas, CA 95035

(800) 232-3471 or (408) 945-1477

► CIRCLE 376

### ▼ FUNCTIONAL TESTER USES ADVANCED PIN CARDS

The VXI 2000 performs core analog and digital functional testing using two specially developed pin electronics cards and artificial-intelligent



system software. The Universal Pin Electronics card supplies four channels of analog and digital stimulus and response capability to 25 MHz without switching. The channels are reconfigurable under software control and are actually virtual instruments. The Digital Pin Electronics card is a 96-channel word generator/receiver that supplies TTL apply, expect, and mask signals at rates to 5 MHz. Controlling the hardware is the Diagnostic Workbench package, which transfers diagnostic information on the unit under test directly from the CAD environment to the test environment. System prices range from \$50,000 to \$80,000.

#### **Giordano Associates Inc.**

44 Rt. 46

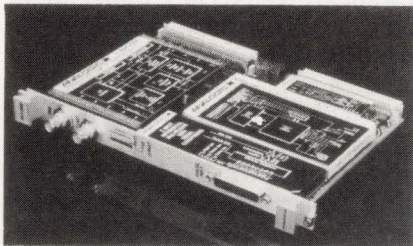
Pine Brook, NJ 07058

(201) 808-8500

► CIRCLE 377

### ▼ B-SIZE CARD COLLECTS FAST 16-BIT DATA

With its 16-bit resolution and 400,000-conversions/s speed, the DVX 2503 is suitable for real-time data acquisition in both VXI and VME systems. The B-size (6U VME card) module offers 8 differential analog input channels that are multiplexed to an instrumentation ampli-



fier followed by a programmable-gain amplifier. Amplifier gain is selected dynamically on a channel-by-channel basis without degrading the system's accuracy or measurement rate. Common-mode rejection ratio is better than 100 dB at 60 Hz. A 1000-word FIFO memory stores the collected data temporarily, guaranteeing continuity despite transfer gaps caused by processor and DMA latencies. The DVX 2503 costs \$4500 and is available 8- to 10-weeks after receipt of an order. Quantity prices are available.

#### **Analogic Corp.**

8 Centennial Dr.

Centennial Industrial Park

Peabody, MA 01961

(508) 977-3000

► CIRCLE 378

### ▼ INTERFACE SYSTEM MAKES TIGHT CONNECTIONS

An interface system for VXIbus mainframes offers a single, highly reliable connection between the mainframe and the unit under test. Two major components make up the system: an Interconnect Adapter and an Interlocking Receiver. The adapter connects the VXI card to two connector modules so that the entire module—including the card, the adapter with wiring, and the connector modules—can be easily inserted and removed from the mainframe. Connections are completed with signal paths as short as 4 in. The receiver hinges downward for easy access to the VXI modules in the mainframe. When closed, the receiver positions the connector modules auto-

matically. The module is priced at \$2800, with delivery within 6 weeks from receipt of an order.

#### **Virginia Panel Corp.**

1400 New Hope Rd.

Waynesboro, VA 22980

(703) 949-8376

► CIRCLE 379

### ▼ 32-RELAY MATRIX CARD CAN BE SPLIT OR COMBINED

Designed for either VXIbus or CDSbus systems, the 53A-365 matrix relay card contains 32 independently controlled DPDT relays that can be configured as either a 2- or a 4-wire matrix in various combinations. Users can open or close the relays randomly by transmitting ASCII characters from the system controller. A split-matrix switch enables the card to be configured as either one matrix or as two independent matrices of equal size. Using the card's front-edge D-connectors, modules can be chained together to create larger matrices. The 53A-365 sells for \$750 and is available within 6 weeks of ordering.

#### **Tektronix/Colorado Data Systems Inc.**

3301 W. Hampden

Englewood, CO 80110

(800) 237-2831 or (303) 762-1640

► CIRCLE 380

### ▼ MULTICHANNEL COUNTER HAS 2-NS RESOLUTION

In a single-width C-size card, the HP E1420A universal counter supplies two 200-MHz channels and an optional 1.3-GHz channel. The unit boasts a 2-ns time interval resolution (200 ps with averaging) and rise/fall time measurements down to 15 ns. Besides the typical universal counter measurements of frequency, period, time interval, totalize, and ratio, the module automatically measures rise and fall times, pulse width, and ac/dc voltage. Up to 40 measurements/s are possible for a sequence of different measurements. A single type of measurement can be made 60 times a second. The HP E1420A costs \$3450 and is available within 6 to 8 weeks.

#### **Hewlett-Packard Co.**

Loveland Instrument Div.

P.O. Box 301

Loveland, CO 80539-0301

(800) 752-0900 or (303) 679-5000

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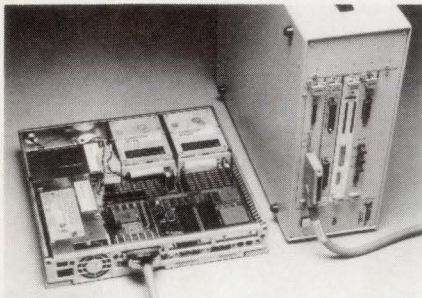
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CIRCLE 112

## VXIBUS PRODUCTS

### ▼ KIT TURNS SPARCSTATION INTO A VXI CONTROLLER

With the VXI-SB2020 interface kit, users can control VXIbus systems from any Sun Sparcstation employing an SBus slot. The kit gives the Sparcstation the equivalent capability of an embedded VXI controller that plugs directly into a VXIbus slot. The VXI-SB2020 comes with the integrated NI-VXI software, which includes intuitive tools to control VXI devices, driver software for



VXI programming, and support for multiple mainframe systems. Hardware includes a 32-bit board that plugs into one SBus slot, a C-size Slot 0 module, and a 2-m cable. The kit costs \$3700, with delivery in 30 days.

**National Instruments**  
6504 Bridge Point Pkwy.  
Austin, TX 78730-5039  
(800) 433-3488 or (512) 794-8411  
► CIRCLE 382

### ▼ SHIELDED MAINFRAME HANDLES RF APPLICATIONS

Special shielding features and a low-noise power supply make the Model 1261E C-size VXI chassis ideal for RF and microwave applications. The mainframe incorporates double-skin construction and an easily removable shielded door for excellent attenuation of external signals. Cables enter the chassis through front and rear escutcheon plates, both of which are fully gasketed. A low-noise, low-ripple power supply ensures that measurements are unaffected by power-line noise. The chassis can handle 35 W/slot, thanks to a high-capacity cooling system with variable-speed fans that automatically provide the needed cooling with minimum noise.

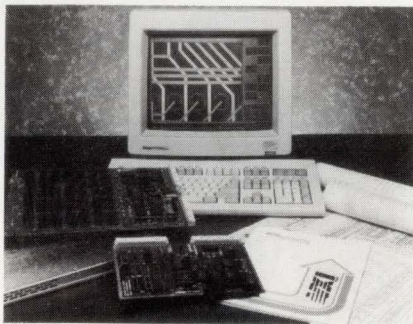
**Racal-Dana Instruments Inc.**  
4 Goodyear St.  
Irvine, CA 92718-2002  
(714) 859-8999  
► CIRCLE 383

### ▼ B-SIZE CHASSIS BOASTS FULL VXI COMPATIBILITY

The VXI-B series consists of a portable 12-slot chassis, a VXI Slot 0 controller, and a 386SX- or 386-based PC-compatible embedded computer. Included with the system are MS-DOS and Windows/386, as well as the RadiSys EPConnect/VXI software, which contains the VXI resource manager, the bus probe, and the bus monitor. The chassis and software accommodate both VXI and VME modules. The systems offer full dynamic-configuration capability and a complete VXI backplane, including trigger lines, local bus, MODID lines, and an ECL clock. The VXI-B1, with a 16-MHz 386SX computer, costs \$9995. The VXI-B2, which has a 25-MHz 386-based computer, goes for \$12,285.

**RadiSys Corp.**  
19545 NW Von Neumann Dr.  
Beaverton, OR 97006  
(503) 690-1229  
► CIRCLE 384

### ▼ BOARDS HELP INTRODUCE DESIGNERS TO VXIBUS



Designers new to the VXIbus can use the Quick-Start program to speed up the design of original VXI modules and the reconfiguration of existing instruments. The package includes the VXI-5500 prototyping card, a C-size board that handles all VXI byte and word protocols. Two-thirds of the board is blank with insertion holes on 0.1-in. centers for easy component mounting. The VXI-5523 interface card contains the same circuitry on a card one-third the height of a C-size module. The card can be mated by a right-angle DIN connector to a user's existing circuit. A companion hardware kit is a VXI-standard capsule designed for component cooling and RFI/EMI control. The VXI-5500 costs \$975; the

VXI-5523, \$700; and the hardware kit, \$200. Delivery is in two weeks.

**ICS Electronics Corp.**  
2185 Old Oakland Rd.  
San Jose, CA 95131  
(408) 432-9009  
► CIRCLE 385

### ▼ SYNCHRO/RESOLVER HAS BROAD FREQUENCY RANGE

The VXI 5388 combines synchro/resolver, angle-position indicator, and simulator functions in a one-slot C-size module. The simulator portion of the card has a resolution of 0.001° with an accuracy of  $\pm 0.003^\circ$ . Operating frequency ranges are 47 Hz to 2 kHz and 360 Hz to 10 kHz, and the line-to-line output range is 2 to 90 V rms. The card can simulate a transducer rotating at up to 1000°/second and can drive a load of up to 6 VA at 400 Hz. The card's indicator function accepts stator line-to-line inputs from 20 to 90 V over a range of 47 Hz to 10 kHz. The VXI 5388 costs \$6795 and is available 10 to 12 weeks after receipt of an order.

**North Atlantic Industries Inc.**  
60 Plant Ave.  
Hauppauge, NY 11788-3890  
(516) 582-6060  
► CIRCLE 386

### ▼ VXI MODULES CUSTOMIZE FUNCTIONAL TESTER

The Testar System 5000 (TS5000) is a mixed-signal, functional, automatic-test-equipment system using VXIbus B- and C-size modules running under the proprietary Testar Test Executive (TSEXEC). In addition to VXIbus instruments, the TS5000 supports a wide range of VME and IEEE-488 instruments. TSEXEC, a software kernel, offers an interactive and comprehensive set of application development tools and screens. The software acts as an interface between applications programs and the operating system. Functional diagnostics to the component level are provided. The company offers application engineering services, including maintenance support and applications programming. Prices start at less than \$100,000.

**Proteus Corp.**  
5827 S. Rapp St.  
Littleton, CO 80120  
(303) 795-5944  
► CIRCLE 387

# NEWS

ABOUT  
1553 DATA BUS  
SYNCHRO CONVERSION  
A/D & D/A CONVERSION  
POWER HYBRIDS  
SOLID-STATE POWER CONTROLLERS

**DDC**  
ILC DATA DEVICE  
CORPORATION

## TEST A 1553 RT IN 20 SECONDS!

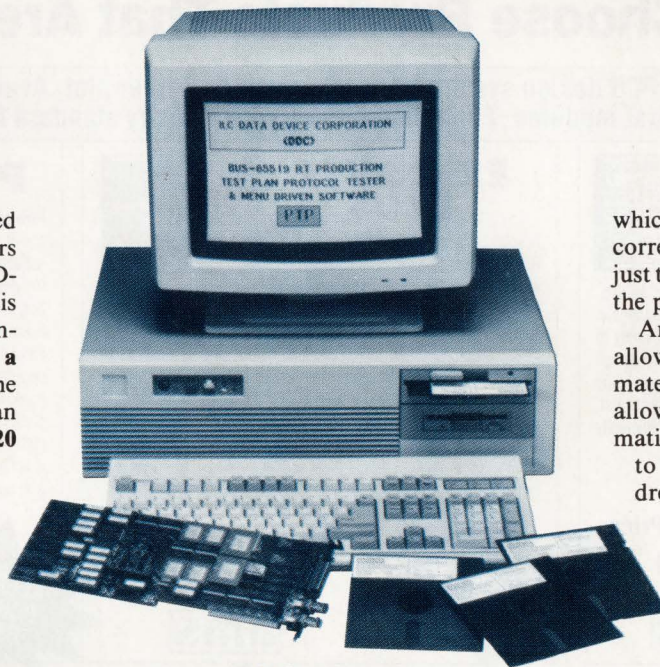
The BUS-65519 was designed to make life simpler for engineers tasked with testing MIL-STD-1553 Remote Terminals. This turnkey system allows an engineer to **completely test a 1553 RT**, in accordance with the SAE RT Production Test Plan (protocol tests), **in less than 20 seconds!**

The BUS-65519 comes complete with menu driven software. The user simply answers a series of questions regarding the operation of the Unit-Under-Test (UUT). The BUS-65519 automatically generates the executable code required to implement the test. **The user does not need to write a single line of code!**

In addition, when not being used for production test, the BUS-65519 can be used as a general purpose MIL-STD-1553 tester/simulator!

The test software generated by the BUS-65519 is not limited to use on the factory floor. The use of the SAE Production Test Plan insures that the 1553 RT correctly handles MIL-STD-1553 protocol. It is perfect for the following applications:

1. Incoming Inspection of Components;
2. RT Design Verification;
3. Production Test.



### **BUS-65519** **PRODUCTION TEST PLAN TESTER AND SOFTWARE**

The BUS-65519 consists of an IBM PC/XT/AT® compatible board with user friendly, menu driven software. Default values support complete MIL-STD-1553B compliance. Most variables need only be modified if the specific RT does not support all MIL-STD-1553 message formats. This keeps set-up time to a minimum.

The characteristics of the particular UUT are saved to disk. Once the user selects "RUN" from the Main Menu, the BUS-65519 issues the required 1553 messages and evaluates the response from the RT. A report is automatically generated indicating whether the RT passed or failed.

#### **AUTOMATIC TEST REPORT**

If the unit fails, the report will indicate the specific tests to

which the RT did not respond correctly. The user can rerun just those tests, in order to debug the problem.

An optional 16 bit I/O card allows the user to further automate the test procedure. This allows the BUS-65519 to automatically control discrete inputs to the UUT—such as RT address, status bits, and Power-On Reset—simplifying the user's test fixture.

#### **BONUS— GENERAL PURPOSE TESTER CAPABILITIES!**

When not being used for RT Production Testing, the BUS-65519

can be used as a general purpose 1553 tester. It has all the capabilities of the popular BUS-65517II card.

This includes simultaneous simulation of BC, multiple RT's, and intelligent Bus Monitor. Error injection capabilities include word count, bit count, zero crossing, gap, and RT response errors.

Whether your needs are for Incoming Test, Design Verification, or Production Test—the BUS-65519 provides an inexpensive, easy-to-use solution.

Order yours today! For additional product or application information, contact Fabio Stanzini, Applications Engineer, at 1-800-DDC-1772, x206.

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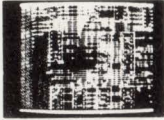
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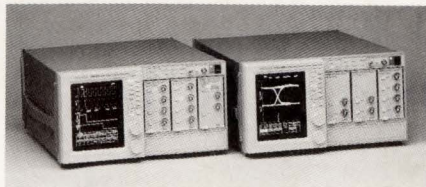
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31200 LaBaya Drive Westlake Village, CA 91362

ED228



▼ **DIGITAL SCOPE FEATURES  
ADVANCED PROCESSING**



With fast-Fourier-transform capability, the 11403A digitizing oscilloscope can convert time-domain acquisitions into the frequency domain for spectral analysis. Users can select from six FFT windowing functions: rectangular, triangular, Hamming, Hanning, Blackman, and Blackman-Harris. Other waveform processing capabilities include pass/fail testing and simultaneous measurements on multiple waveforms. The modular scope can accommodate up to 12 acquisition channels that have dual independent time bases and vertical resolution of 14 bits, with averaging. The 11403A costs \$18,950, with delivery 4 weeks after receipt of an order.

**Tektronix Inc.**  
P.O. Box 19638  
Portland, OR 97219-0638  
(800) 426-2200

► **CIRCLE 388**

▼ **DYNAMIC SIGNAL ANALYZER  
FITS 7-LB. PACKAGE**

Weighing only 7 lbs., the notebook-size HP 3560A dynamic signal analyzer offers time- and frequency-domain analysis from dc to 40 kHz. The 2-channel, FFT-based instrument makes a broad spectrum of complementary measurements typical of larger benchtop units. Complete alias protection and digital zoom allow high-resolution measurements, and an antialias filter can be adjusted for fast-edge, time-domain measurements. The analyzer works for 6 hrs. on its internal battery. For spectrum measurements, dynamic range is 70 dB and amplitude accuracy is  $\pm 0.5$  dB. Network measurement accuracy is  $\pm 0.2$  dB and  $\pm 5^\circ$ . The HP 3560A costs \$7500, and delivery is estimated at 4 to 6 weeks.

**Hewlett-Packard Co.**  
Lake Stevens Instrument Div.  
8600 Soper Hill Rd.  
Everett, WA 98205-1298  
(800) 752-0900

► **CIRCLE 389**

▼ **4-CHANNEL DIGITAL SCOPE  
HAS 100-MHZ BANDWIDTH**

The DL1200A 4-channel digital oscilloscope features a 100-MHz analog bandwidth. Maximum sampling rate is 100 Msamples/s on one channel and 20 Msamples/s on four channels. Vertical resolution is 8 bits, and record length is 128 ksamples (32 ksamples/channel in 4-channel operation). Features include automatic setup, go/no-go decision making, automatic waveform measurements, and a dynamic accumulate mode. Users can capture four signals with long time intervals using one trigger event. Prices start at less than \$5000, with delivery in 8 weeks.

**Yokogawa Corporation  
of America**  
2 Dart Rd.  
Newnan, GA 30265-1094  
(404) 253-7000

► **CIRCLE 390**

▼ **I960CA EMULATOR WORKS  
TO 33 MHZ IN REAL TIME**

With an operating speed of 33 MHz, the Express Plus offers nonintrusive, real-time in-circuit emulation for Intel's i960CA. To eliminate potential interference from high-speed signals traveling along cable connec-



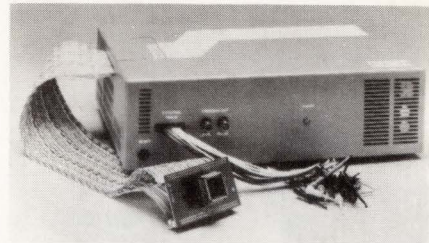
tions, the target processor remains in the circuit. Then, while the system executes code, the Express Plus passively monitors all i960CA bus activity and records it in trace memory. The emulator reconstructs programs executing from the processor's cache by using all of the control information supplied by the processor and special emulator software. The Express Plus costs \$28,750, with delivery in 60 days.

**Step Engineering Inc.**  
661 E. Arques Ave.  
Sunnyvale, CA 94088-3166  
(800) 538-1750 or (408) 733-7837

► **CIRCLE 391**

▼ **EMULATORS ADD  
68332 SUPPORT**

The HMI-200 series emulators have added support for the Motorola 68332 microprocessor. The instrument offers real-time emulation, four complex break and trigger points, and two 4-kword-by-104-bit trace buffers, including 16 external trace bits and 32 bits of time-tag information. Standard emulation



memory is 256 kbytes, with 1, 2, or 4 Mbytes optional. The 200-series emulators are integrated with SourceGate, a window-driven high-level language debugger that supports C, Pascal, PL/M, and Ada compilers. The 68332 version of the HMS-200 sells for \$16,000. SourceGate for the IBM PC family is \$1500.

**Huntsville Microsystems Inc.**  
4040 S. Memorial Pkwy.  
Huntsville, AL 35802  
(205) 881-6005

► **CIRCLE 392**

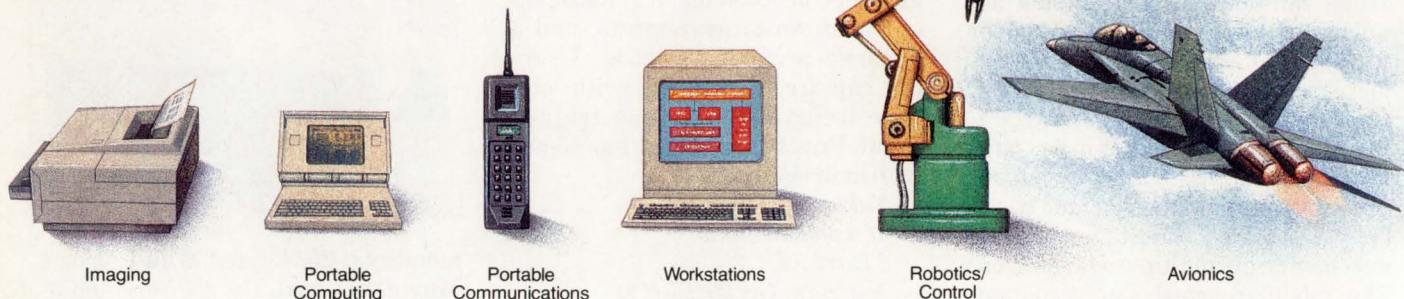
▼ **PROGRAMMING SOFTWARE  
AUTOMATES SCOPE TESTS**

Software for the 400-series digital oscilloscopes makes it possible for users to write customized programs for automating analysis and test tasks. The Tact software consists of a learn function, a Basic language subset, and an editor. Custom menus and operator prompts can be created for automated testing, without the need for an external computer or an interface. Using an AT-style keyboard and the software's full-screen editor, users can create or modify Tact programs on the scope. Conditional testing, branching, variable storage, and disk and printer output are available, as well as extensive waveform analysis. The programs are stored on a floppy disk, hard disk, or 44-Mbyte disk cartridges.

**Nicolet Test Instruments**  
5225 Verona Rd.  
Madison, WI 53711  
(800) 356-3090 or (608) 273-5008.

► **CIRCLE 393**

# From LaserJets® to fighter jets, our high-performance FACT QS and FCTA set the pace in logic.



Delivering high performance to a broader range of applications.

Whether it's a printer churning out 8 PPM or an F-18 scorching the sky at Mach 2+, your application requires advanced logic solutions that deliver low power. Which is exactly what you get with our low-noise FACT Quiet Series and high-speed FACT FCTA families.

Together, these devices provide innovative solutions to the distinctly different needs of a broad spectrum of high-performance applications.

Needs that range from the ultra-low power of battery-operated

systems to the searing speeds dictated by RISC processing. To guaranteed 50-ohm dynamic drive for low-impedance bus environments (something that reduced-output swing ACMOS technologies and BCT can't do). To the 64mA low-level static drive required of VME-type termination schemes.

## Silencing noise with advanced circuitry.

Beyond speed, power, and drive there's the issue of noise. Our USC™ (Under-Shoot Corrector) and patented GTO™ (Graduated Turn-On Output) circuits enable our devices to offer the lowest ground bounce of any ACMOS family. And their split-ground bus results in the best dynamic noise margins of *any* logic technology.

Plus, with controlled output edges and negligible ringing, FACT QS generates lower spectral content than BCT and non-standard-pin-out ACL families.\*

## Producing a complete family of ACMOS logic.

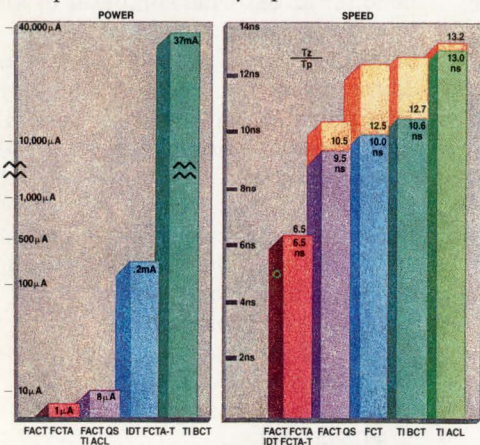
With our high-performance FACT QS and FACT FCTA devices, we've enhanced our multi-functional, broad-based line of ACMOS logic devices, which already includes standard FACT and FCT. What's more, FACT is available with Standard Military Drawings, JAN 38510 level B, and S-level processing. So regardless of your application, we have the solution.

## Keep pace with the leaders in logic.

For more information, including datasheets and samples, on our ACMOS families, call or write us today.

We'll get you up to speed in no time at all.

1-800-NAT-SEMI, Ext. 111  
National Semiconductor Corp.  
P.O. Box 7643  
Mt. Prospect, IL 60056-7643



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\*From a 1990 study conducted by Washington Labs Inc., a subsidiary of Violette Engineering Corporation.

# IEEE-488



Control any IEEE-488 (HP-IB, GP-IB) device with our cards, cables, and software for the PC/AT/386, EISA, MicroChannel, and NuBus.

bit, 5-MHz sampling converter with an 83-dB spur-free dynamic range. Software included is the ZPA1000 dynamic signal-analysis test software and DSPlay XL development software. The system comes with a 50-MHz digital-signal-processing board that uses the AT&T WE DSP32C processor. Single-quantity price is \$13,100 for one channel and \$17,200 for two channels. Delivery is from stock to 6 weeks.

**Burr-Brown Corp.**  
P.O. Box 11400  
Tucson, AZ 85734  
(800) 548-6132 or (602) 746-1111  
▶ **CIRCLE 395**

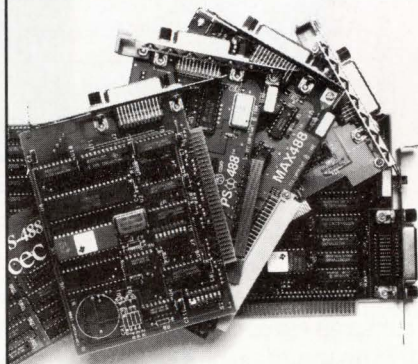
## ▼ AUTOHANDLER PROGRAMS, TESTS, MARKS ICs

The Quality Automation Autolaser 3100 is a standalone handler system that programs, tests, and marks ICs in one operation. The permanent marking, which is performed by a built-in laser, is unaffected by solvents or high temperatures used in board manufacturing. The system supports plastic leadless chip carriers, dual in-line packages, and small-outline packages. Print densities are available in eight pitches with proportional spacing. The pick-and-place technology used by the Autolaser 3100 is designed to prevent lead damage to surface-mounted devices. The chips move gently down a track of air and are transported through the system by hydraulically operated vacuum cups under microprocessor control.

**Data I/O Corp.**  
10525 Willows Rd. NE  
Redmond, WA 98073-9746  
(206) 881-6444  
▶ **CIRCLE 394**

## ▼ SYSTEM EVALUATES, TESTS, DEVELOPS ADC CIRCUITS

Designers can test, evaluate, and develop applications for Burr-Brown's very high-performance analog-to-digital converters using the DSP-SYS604. The system, which is PC-based, was specifically designed for the ADC604 ADC. Included with the system is a single or dual analog-input system and one or two 64-kword input buffer boards. The input system uses the ADC604, which is a 12-



You get fast hardware and software support for all the popular languages. A software library and time saving utilities are included that make instrument control easier than ever before. Ask about our no risk guarantee.

## ▼ POD EMULATES XXC528-SERIES MICROCONTROLLERS

The POD-C528 allows the EMUL51-PC in-circuit emulator to support the Philips Components-Signetics 80C528, 83C528, and 87C528 microcontrollers. The unit accommodates all of the microcontrollers' features, including their extended RAM and power-control modes at all speeds. The EMUL51-PC employs a flexible modular architecture consisting of a PC plug-in emulator board and an optional plug-in trace board. The POD-C528 costs \$895 and the EMUL51-PC goes for \$2390.

**Nohau Corp.**  
51 E. Campbell Ave.  
Campbell, CA 95008  
(408) 866-1820  
▶ **CIRCLE 397**

## ▼ PC/AT CARD CHASSIS HAS 200-W POWER SUPPLY

A 10-in. portable PCXI chassis has six slots for PC/AT-based function cards. The PX1020 chassis comes with the PX1570, a 200-W switching power supply. In addition, the chassis has six 16-bit PC/AT bus connectors on the backplane. Cooling is accomplished by positive-pressure airflow from a 72-cfm positive-pressure fan. Termination resistors are provided on clock, address, and data lines. The PX1020 chassis costs \$995.

**Rapid Systems Inc.**  
433 N. 34th St.  
Seattle, WA 98103  
(206) 547-8311  
▶ **CIRCLE 398**

## ▼ DMM INCLUDES BRIGHT LED DISPLAY

A 0.5-in. bright LED display makes the Model 2831A digital multimeter (DMM) easy to read in all lighting conditions. The 3-1/2-digit DMM features 0.1% dc voltage accuracy and ac voltage response to 40 kHz. The meter measures current to 20 A, voltage to 1200 V dc or 1000 V ac, and resistance to 20 MΩ. It also has a diode test capability. All functions are overload protected. The Model 2831A is priced at \$295.

**B&K-Precision**  
6470 W. Cortland St.  
Chicago, IL 60635  
(312) 889-1448  
▶ **CIRCLE 399**



Free:  
Informative  
catalog 800-234-4232  
Applications help (617) 273-1818



**Capital Equipment Corp.**  
Burlington, MA. 01803

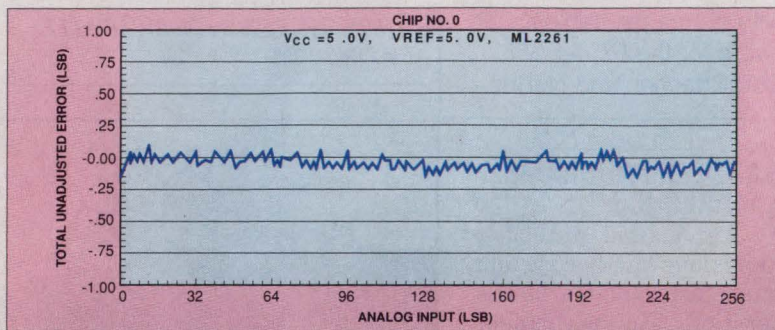
CIRCLE 151

# Our new ML2261 8-bit A/D converter takes speed and accuracy to an entirely new level: 670ns.

Latch onto Micro Linear's new ML2261. Without question, the fastest, most accurate micro-processor-compatible 8-bit A/D converter on the market. With performance features that'll leave most microprocessors in a no-wait state.

By utilizing half-flash techniques, the ML2261 achieves A/D conversion times of 670ns over temperature and  $V_{CC}$ . It quickly converts an analog 0V to 5V sine wave at 500 kHz to its digital representation with 48 dB signal-to-noise ratio. Digital error correction is used to achieve a total unadjusted error of better than  $\pm 1/4$  LSB. (Total unadjusted error includes the sum of linearity, zero scale and full scale errors).

It's also easier to use, because the ML2261's differential architecture provides superior power supply rejection. The analog input is 0V to 5V with a 5V power supply. And because



*Built-in digital error correction delivers true 8-bit accuracy, with typical unadjusted error of less than  $\pm 1/4$  LSB.*

inputs can withstand at least 25 mA, you can achieve better latch-up immunity on analog inputs. The digital interface is also designed to keep up with the fastest microprocessors and appears as a memory location or I/O port to the microprocessor. In addition, no external clock is required and power dissipation is a mere 75 mW. All parameters are guaranteed over the supply tolerance and temperature range.

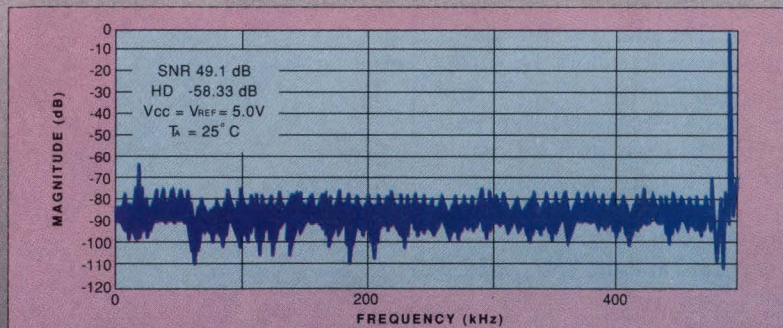
Combined, the ML2261 gives you the fastest, most accu-

rate, easiest to use 8-bit converter for a wide range of applications including disk drives, medical instrumentation and signal processing. With a price/performance ratio that's significantly lower than comparable converters.

Devices are now available in standard 20-pin DIP or surface-mount PCC packages, with 100-unit prices beginning under \$9.00.

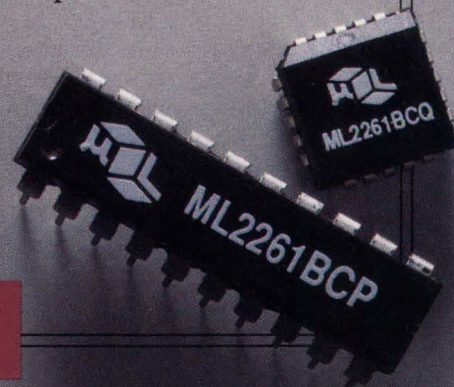
#### For more information.

To find out more about how you can quickly convert your new product design to the ML2261, just call (408) 433-5200. Or write to: Micro Linear, Dept. TFA, 2092 Concourse Drive, San Jose, CA 95131. We'll send you all the specs. In a flash.



*The ML2261 maintains ideal signal-to-noise ratios independent of increasing analog input frequencies to 500kHz.*

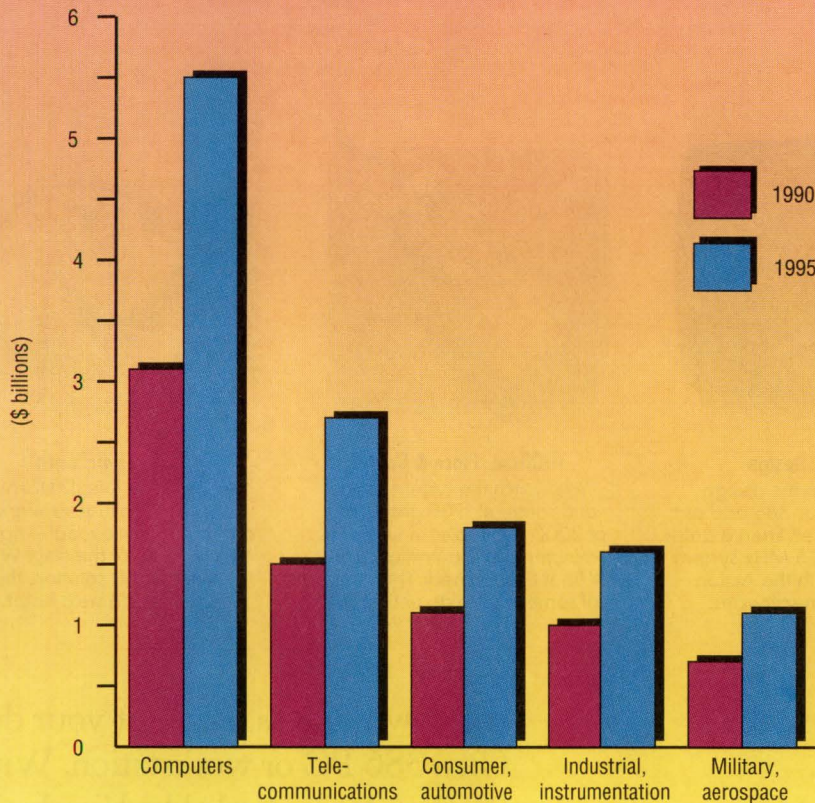
 **Micro Linear**



# ELECTRONIC DESIGN QUICK LOOK

EDITED BY SHERRIE VAN TYLE

## ASICs, PROGRAMMABLE ICs KEEP SURGING



Source: Electronic Trend Publications

## MARKET FACTS

**S**ales of application-specific ICs and programmable chips are flourishing. Revenues from ASICs and programmable devices will grow from \$7.3 billion last year to \$12.6 billion in 1995. But as costs skyrocket more specialized ICs are being fabricated in CMOS, according to predictions from Electronic Trend Publications.

The Saratoga, Calif., market researcher tracks the ASIC market by gate arrays, standard cells, and full custom ICs. Programmable ICs comprise programmable logic devices, erasable programmable logic devices, and field-programmable gate arrays. Sales of full custom devices are expected to drop off by 25% by 1995 as users opt for gate arrays and FPGAs, which have lower development costs. ASICs are expected to grow 10% a year until 1995, propelled by their use in portable cellular phones and other compact equipment.

Programmable ICs should see an 11% increase overall by 1995. EPLDs and FPGAs are expected to double their market share, to 6% by mid-decade. About 80% of these chips will be built in CMOS through 1995, says Electronic Trends. Still, use of gallium arsenide and biCMOs is expected to grow at least 10% as users seek greater speed.

## EYE CATCHER

Bleak outlook: The U. S. share of the worldwide market for computers—mainframes, minicomputers, workstations, and PCs—is steadily dropping. Meanwhile, Japanese market share is gaining, with Japan expected to overtake the U. S. as market leader by 1993. So forecasts the Semiconductor Industry Association. Japan's semiconductor sales eclipsed those of the U. S. in 1986. Also eroding is U. S. market share vs. Japan in semiconductor equipment and ICs, including DRAMs, microprocessors, microcontrollers, peripheral logic, and ASICs.

### Computer Segment

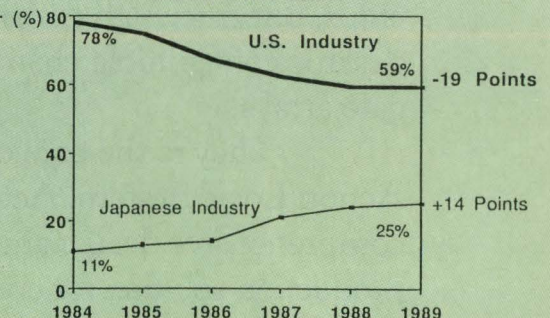
(Mainframes, Midranges, Workstations and PCs)

#### Top 10 Manufacturers

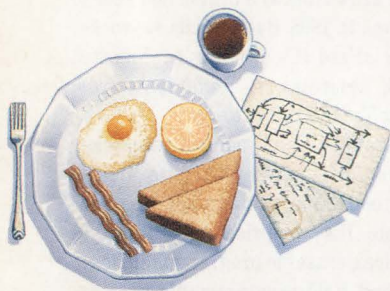
1984	1989
IBM	IBM
DEC	DEC
Burroughs	NEC
Sperry	Fujitsu
Fujitsu	Unisys
Control Data	Hitachi
NCR	HP
HP	Groupe Bull
NEC	Siemens
Siemens	Olivetti

Source: Datamation, SIA Estimates

#### Shares of WW Market

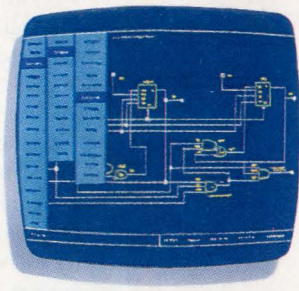


# Be Brilliant At In Production



## 7:05 am: Breakfast

Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



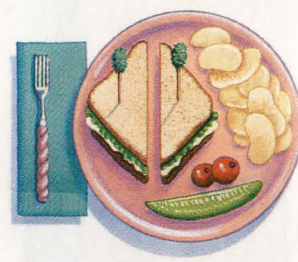
## 8:50 am: Design

You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.



## 11:00 am: Place & Route

You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



## 12:00 pm: Lunch

Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

## Actel Field Programmable Gate Array Systems.

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL® or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

They're the core of the Action Logic System, Actel's comprehensive design and production solution for creating

your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic™, OrCAD™, and Mentor™.

And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus

100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

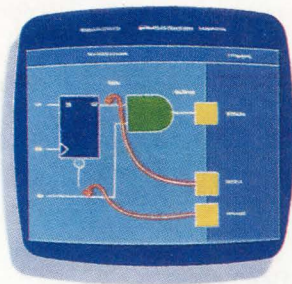
Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

# Breakfast And n By Dinner.



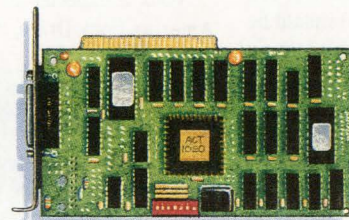
#### 1:15 pm: Program

You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.



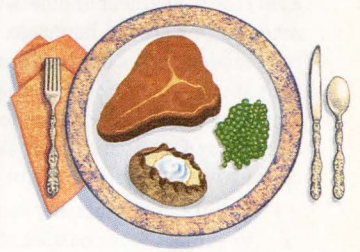
#### 1:25 pm: Test

You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



#### 4:00 pm: Production

Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished way ahead of schedule! Better think of something to do until 5:00.



#### 6:00 pm: Dinner

Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

In fact, the only thing you'll give up is the NRE you pay with full masked arrays. You can get started with an entry level Action Logic System for under \$5000. Guaranteed.

And Actel FPGAs are even 883 mil-spec compliant.

You can be brilliant right now

with 1200- and 2000-gate devices, and a whole new family of 8000-, 4000- and 2500-gate parts are on the way. Call 1-800-227-1817, ext 60 today for a free demo disk and full details about the Action Logic System.

It could make your whole day.



Risk-Free Logic Integration

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## 1-MINUTE OPINIONS

*What do you think about the education that young engineers receive these days?*

**E**ngineering education really begins in elementary school with the teaching of math and science. Although technical material is important, engineers do need other skills such as writing, speaking, and managerial know-how.

Someone once suggested that (at the college level) engineers take managerial courses and that management students take engineering courses. The foreign-language idea presented by Alain Beaulieu, Ottawa, Ontario, is very timely [Oct. 25, 1990, p. 85]. Everybody (engineer or otherwise) should be schooled in a second language. The economy is becoming increasingly global and to prepare young people for the competitive marketplace, we must teach them technical, managerial, and communication skills. **Robin A. Schwartz, Huntington, N. Y.**

**T**he burden of educating young engineers in subject areas outside of engineering should be shared by the students themselves and the industry that is employing them. As a young engineer (25) who graduated from college three and a half years ago, I have a fairly up-to-date perspective on the issue. I completed my BSE in computer systems engineering in five years, attending school full time for the first three and part-time (while working as a full-time engineer) the second two. In order to complete the curriculum in four years, an engineering student is expected to take course loads of 18 hours a semester.

Before curriculum changes will have any effect, engineering students will have to realize the benefits of using the humanities courses in a productive manner instead of taking the known courses for the easy A. Sadly, the emphasis is too much on keeping abreast of the most up-to-date technology; the job market is competitive and employers are concerned more with what computer languages a student knows or what types of digital design courses he or she has taken. Until employers start placing a value on a well-rounded education, the average engineering student will not bother pursuing it. **Mark Fogle, Chandler, Ariz.**

*What's your opinion on the education of today's young engineers? Fax your opinion to (201) 393-0637 or mail to Electronic Design, Reader Opinions, 611 Route 46 West, Hasbrouck Heights, NJ 07604.*

## HOT PC PRODUCTS

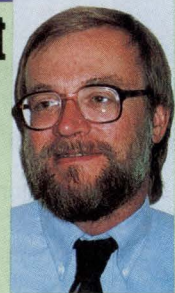
**T**he video and PC worlds should work more easily together with a low-cost video controller from Sony. With the Vbox, PCs users can control Sony video equipment, including 8-mm camcorders and VCRs, from their computers. Underlying the link of PCs to video is the proliferation of video boards for PCs, which convert computer (RGB) signals to TV (NTSC) signals. The Vbox relies on proprietary controller chips. For presentations, Vbox simplifies printing to video—transferring PC graphics and other images to 8-mm videotape. It also simplifies integrating full-motion video into multimedia presentations. Up to seven Vbox controllers can be daisy-chained and connected to a PC through one serial port. That way, several video devices can be cued and controlled during a multimedia presentation.

The controller uses ViSCA, the company's video system control architecture. ViSCA is a machine control protocol, a set of platform-independent command codes. Apple Computer is developing a ViSCA device driver and toolkit, to be offered to application developers at no charge. Farallon Computing, of Emeryville, Calif., and Macromind, of San Francisco, will support ViSCA in their multimedia software.

Vbox is expected to be available in the spring. List price is \$250. Contact Sony Corp. of America, Sony Drive, Park Ridge, NJ 07656; (201) 930-6432.

## K M E T S K O R N E R

### ...Perspectives on Time-to-Market



#### BY RON KMETOVICZ

President, Time to Market Associates Inc.  
Cupertino, Calif.; (408) 446-4458

**I**f you followed my suggestions in the Jan. 31 column, you can use the project model you've developed with your team of modelers and planners to help select computer tools and software. You'll find this approach far superior to the often-followed alternative of selecting tools first and then trying to develop models that satisfy tool requirements. Let's look at the three most important parameters in selecting tools:

- Supports hierarchical tree-planning techniques

Software manufacturers often employ two techniques (actual hierarchical trees and outlines) to support hierarchical planning. Both are effective, so selection is a matter of personal preference. However, of the two, an actual tree structure provides the best visualization of the project's structure and makes it extremely easy to move about within the model.

- Functions effectively on more than 1000 tasks

A typical synthesis of a cross-functional plan generates a model that consists of hundreds of tasks and milestones. It becomes very easy to visualize how the initial model could grow in complexity as more becomes known about the project. Project/program modeling software must be able to handle many tasks on the initial effort and provide the reserve for projected needs. For many projects, 1000 is a modest number. Whatever the task and milestone count for your initial model, allow for a two- to three times expansion. Knowing this number speeds decisions.

- Used by horizontal and vertical decision makers

Your model was developed by a horizontal and vertical team. Logically, you would want those who contributed to model development to be capable of using the model as a decision-making tool once it is available in electronic form. As a result, the hardware and software selected should be of such variety that it can be made available to the entire decision-making team. Network implementations are often of considerable value where project teams are separated physically and geographically. Access to the same project database enables decision makers to assess cause-and-effect relationships of various choices. These three criteria should pare your hardware and software choices. Use your project's model as a benchmark to determine what tools are best for your situation.



## OFFERS YOU CAN'T REFUSE

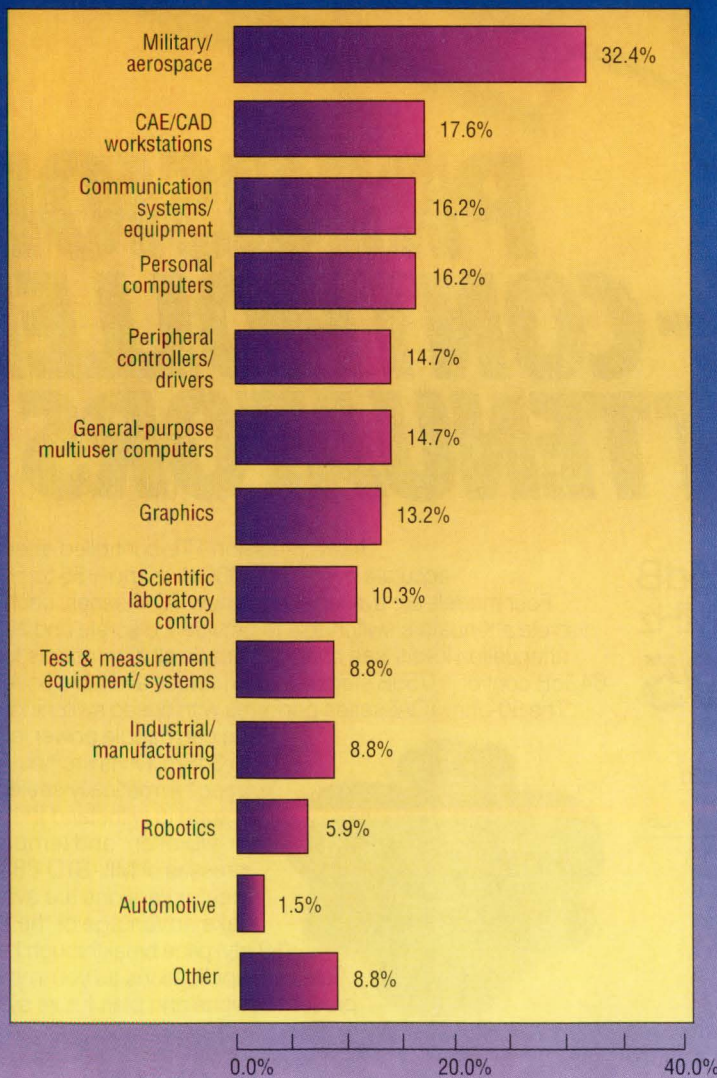
**A**n optical encoder design guide is free from BEI Motion Systems Co. The 16-page booklet gives information on absolute and incremental encoder operations. It explains the use of tachometer and quadrature outputs and describes various count multiplication techniques. There is also a section of selecting encoders for industrial environments and a glossary.

Contact the company's Industrial Encoder Division, 7230 Hollister Ave., Goleta, CA 93117-2891; (805) 968-0782; fax (805) 968-3154.

**E**ngineers can tour an IC manufacturing facility without leaving their chairs. Sand to Circuit, a videotape from Texas Instruments, shows how raw silicon becomes packaged circuits. The VHS tape covers silicon crystal growth, wafer fab, and quality control. The 40-minute tape, at \$90, is available from TI's Semiconductor Group (SC-9105), P. O. Box 809066, Dallas, TX 75380-9066; (800) 336-5236, ext. 700; (214) 242-0864.

## MICROPROCESSOR SURVEY

### WHAT ARE THE PRIMARY APPLICATIONS FOR YOUR 32-BIT DESIGNS?



A. WHITE

Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

## TIPS ON INVESTING

**T**he following checklist suggests some ways that engineers can prepare for investing in the 1990s.

•**Reassess future needs and goals.** Milestones such as marriage, children, and retirement may signal a need to change investment strategies.

•**Adjust portfolio to changes in the market.** Just as investment goals can change fundamentally over time, so can the long-term prospects of individual investments be affected by war in the Mideast and recession, for example.

•**Maintain a long-term perspective.** Long-term investing tends to smooth out the short-term fluctuations of the financial markets. Long-term investors are likely to profit from long-term trends, which have always been positive for stocks, bonds, and many other investments.

•**Monitor investments regularly.** Investing for the long-term does not mean buying an investment and forgetting about it.

•**Take advantage of global opportunities.** One significant investment trend of the 1990s is globalization—the emergence of worldwide financial markets.

•**Understand the effect of changes in the tax laws.** In 1990, Congress enacted legislation that will raise federal taxes and curtail deductions for many Americans. Many states are considering similar increases.

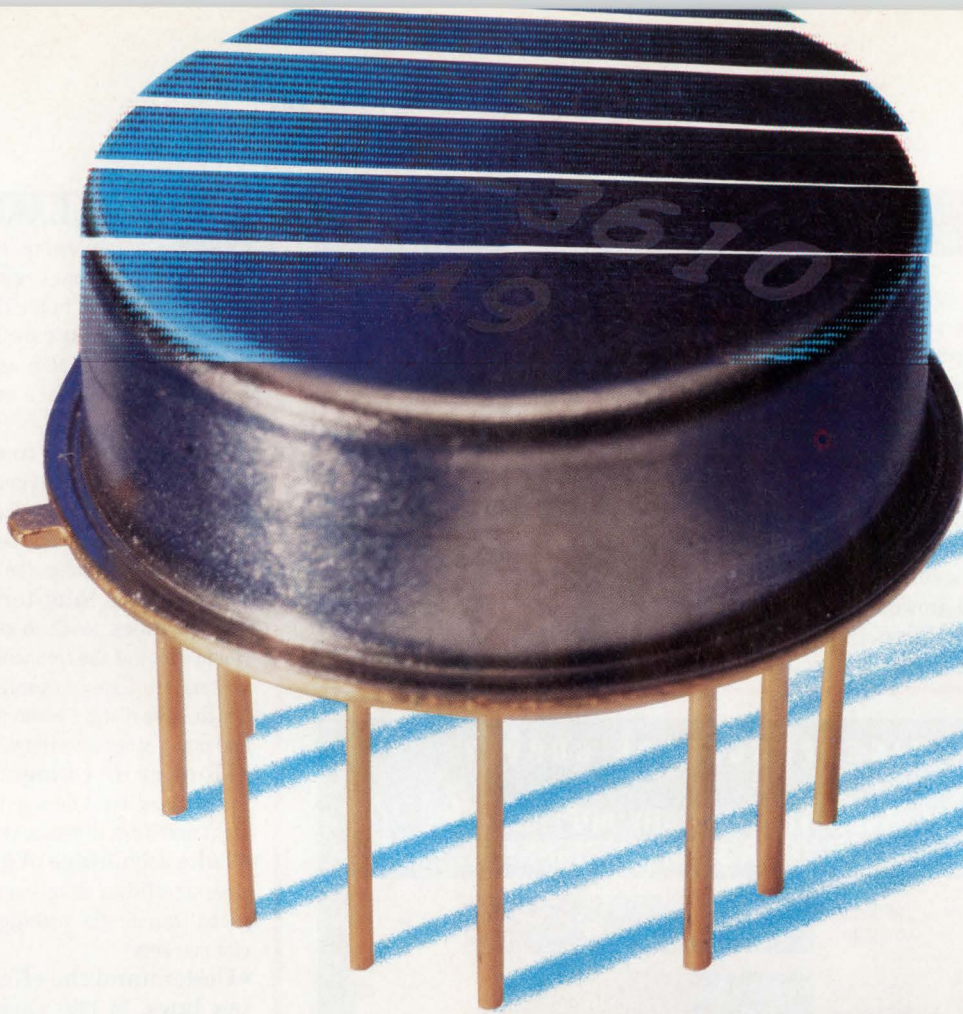
•**Look for quality in long-term investments.** Quality is the hallmark of the long-term investment. Many fixed-income investments are assessed for quality by independent rating firms such as Moody's and Standard & Poor's.

•**Fighting inflation over the long term.** Preserving capital doesn't mean just holding onto assets, it means preserving a lifestyle. Even the most conservative, income-oriented investor needs to include a growth component in his or her portfolio to compensate for the effects of inflation over the long term. This is particularly true for mature investors who rely on retirement income.

•**Protect your capital from catastrophe.** An engineering investor must be prepared for financial emergencies that may arise because of poor health, especially for older investors.

•**Leave a financial legacy for children, grandchildren, or other heirs.** Ensuring that an estate is left for heirs is another critical component of an engineer's financial plan.

*Henry Wiesel is a financial consultant with Shearson Lehman Brothers Inc. and a qualified pension coordinator with the Private Client Group. Wiesel invites questions and comments, which should be addressed to him at Shearson, 1040 Broad St., Shrewsbury, NJ 07702, (800) 631-2221; (800) 221-0073 in N. J.; (908) 389-8300 outside the U. S.*



# PRECISION TTL-CONTROLLED ATTENUATORS

up to 35dB  
10 to 1000MHz  
only **\$59.95**

TOAT-R512 Accuracy (dB) (+/-dB)		TOAT-124 Accuracy (dB) (+/-dB)		TOAT-3610 Accuracy (dB) (+/-dB)		TOAT-51020 Accuracy (dB) (+/-dB)	
<b>0.5</b>	<b>0.12</b>	<b>1.0</b>	<b>0.2</b>	<b>3.0</b>	<b>0.3</b>	<b>5.0</b>	<b>0.3</b>
<b>1.0</b>	<b>0.2</b>	<b>2.0</b>	<b>0.2</b>	<b>6.0</b>	<b>0.3</b>	<b>10.0</b>	<b>0.3</b>
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
<b>2.0</b>	<b>0.2</b>	<b>4.0</b>	<b>0.3</b>	<b>10.0</b>	<b>0.3</b>	<b>20.0</b>	<b>0.4</b>
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

**bold faced values are individual elements in the units**

Now...precision TTL-controlled attenuators accurate over 10 to 1000MHz and -55 to +100°C. Four models are available in the new TOAT-series, each with 3 discrete attenuators switchable to provide 7 discrete and accurate attenuation levels (see chart). Cascade all four models for up to 64.5dB control in 0.5dB steps. Custom values available on request.

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## Mini-Circuits

CIRCLE 109

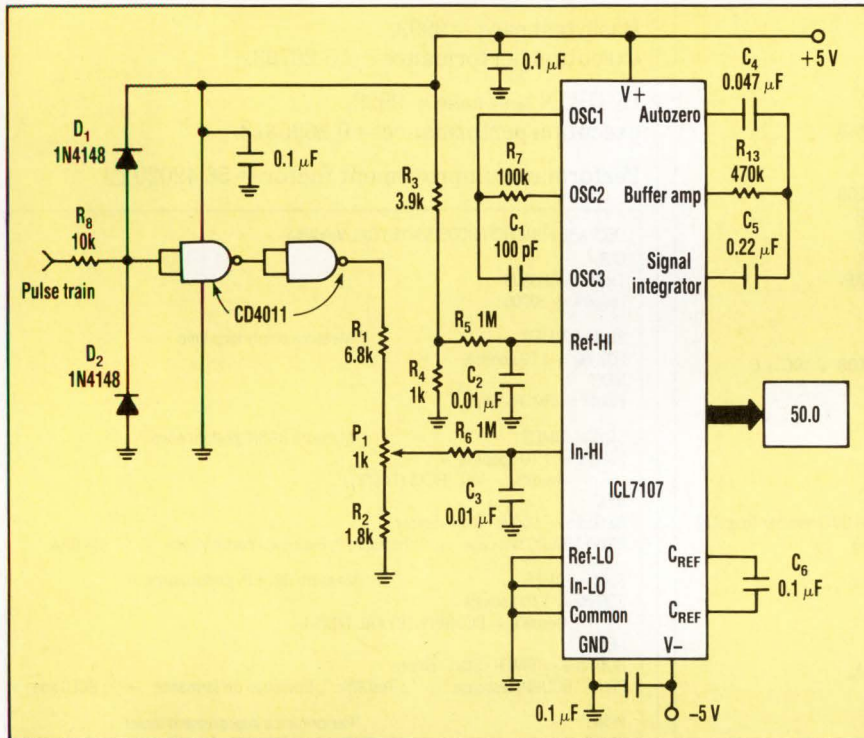
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# CIRCLE 521 MEASURE DUTY CYCLE To 0.5% ACCURACY

M.S. NAGARAJ

ISRO Satellite Centre, Digital Systems Div., Airport Rd., Viminapura P.O., Bangalore 560017 India.



**THIS CIRCUIT MEASURES DUTY CYCLE** to 0.5% accuracy and then displays the percentage. The input pulse is converted to a constant height by the AND gates. The voltage divider, consisting of  $R_1$ ,  $P_1$ , and  $R_2$ , scales down the input to  $V_{REF}$  and sends it to the In-HI of the ADC. Then,  $V_{in}$  is divided by  $V_{REF}$  to get the duty cycle.

**P**ulse-width modulators are commonly used in switched-mode power supplies and dc motor-speed controllers. To test the modulators, the pulse trains' duty cycles at their outputs need to be measured. To find the duty cycle ( $\eta$ ), the pulse width ( $t$ ) and the pulse period ( $T$ ) should be measured using a high-frequency clock. Then the ratio of  $\eta = t/T$  can be computed.

By adding two CMOS gates to a standard display circuit configured around an Intersil 7107 3-1/2-digit analog-to-digital converter (ADC), the pulse train's duty-cycle percentage can be exhibited (see the figure). The circuit can compute, with reasonable accuracy, the duty cycle of a

# CIRCLE 522 CONVERT BCD 56 TIMES FASTER

STEVEN B. LEELAND

Fairchild Data Corp., 350 N. Hayden Rd., Scottsdale, AZ 85257; (602) 949-1155.

**A** highly interactive interpreted language, such as Quick Basic, offers a nearly ideal environment for PC-based test equipment. However, due to the massive amounts of data conversion that might be required, even Quick Basic's performance can be limiting. An assembly-language function that can be called from within Quick Basic improves BCD-

train with a pulse rate as low as 100 pulses/s. However, accuracy increases to better than 0.5% for a pulse rate ranging from 1 to 250 kHz.

The CMOS gates convert the incoming pulse train into pulses of constant height ( $V_m = 5$  V). Note that for CMOS parts, the output voltage swing closely approaches  $V_{DD} - V_{SS}$ . Difference voltages  $V_{DD} - V_{OH}$  and  $V_{OL} - V_{SS}$  have maximum values of 10 mV according to the specifications, but are usually close to 1 mV.

The voltage divider formed by  $R_3$  and  $R_4$  supplies a reference voltage ( $V_{REF}$ ) of about 1 V at the ADC's Ref-HI input. The height of the pulse train is also scaled down to  $V_{REF}$  by the voltage divider formed by  $R_1$ ,  $P_1$ , and  $R_2$ , which is then fed to the ADC's In-HI input. The pulse train's mean average value =  $\eta \times V_{REF}$ .

The 7107 chip displays the ratio of the voltages at its In-HI and Ref-HI inputs. The display reading =  $V_{in} / V_{REF} = (\eta \times V_{REF}) / V_{REF} =$  duty cycle. The right decimal point in the tens position is turned on so that the display reads the duty cycle as a percentage. □

### Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

to-binary conversions by a factor of 56 (Fig. 1).

Four-digit binary-coded decimal (BCD) values can be collected directly from test-equipment hardware or from a general-purpose instrumentation bus, such as the GPIB or IEEE-488. When an application requires massive amounts of conversions of this data, user delays can be lengthy. Using the assembly-lan-

```

; DECLARE SUB BCDBIN% (BYVAL bcdval%)
NAME BCDBIN
PUBLIC BCDBIN
BCDVAL EQU WORD PTR [BP + 6]
BC__TEXT SEGMENT WORD PUBLIC 'CODE'
ASSUME CS:BC__TEXT

BCDBIN PROC FAR
PUSH BP
MOV BP, SP
MOV AX, BCDVAL ;AX = 4d digit BCD number (e.g.ABCD)
MOV CL, AL ;CL = CD
MOV AL, AH ;AL = AB
CALL BCDBYT ;AL = 10A + B
MOV BH, AL
MOV AH, 0 ;AX = 10A + B
MOV BL, AH ;BX = 2560A + 256B
ADD AX, AX ;AX = 20A + 2B
ADD AX, AX ;AX = 40A + 4B
SHR BX, 1 ;BX = 1280A + 128B
SHR BX, 1 ;BX = 640A + 64B
ADD AX, BX ;AX = 680A + 68B
SHR BX, 1 ;BX = 320A + 32B
ADD BX, AX ;AX = 1000A + 100B
MOV AL, CL ;AL = CD
CALL BCDBYT ;AL = 10C + D
MOV AH, 0 ;AX = 10C + D
ADD AX, BX ;AX = 1000A + 100B + 10C + D
MOV SP, BP
POP BP
RET 2

BCDBIN ENDP

BCDBYT PROC NEAR
MOV AH, AL ;AH = AL = 2 digit BCD number (e.g. AB)
AND AX, 0F00FH ;AH = 16A, AL = B
SHR AH, 1 ;AH = 8A
ADD AL, AH ;AL = 8A + B
SHR AH, 1 ;AH = 4A
SHR AH, 1 ;AH = 2A
ADD AL, AH ;AL = 10A + B
RET ;Result returned in AL

BCDBYT ENDP

BC__TEXT ENDS
END
    
```

## 1. THIS ASSEMBLY-LANGUAGE FUNCTION

performs BCD-to-binary conversions. One place that requires these conversions is in test equipment, where massive amounts of data are collected. The function can be called from Quick Basic.

# CIRCUIT SENSES 523 POWER-DOWN

ROBERT SPREITZHOFFER

Alcatel Austria AG, Dep. GTC, Scheydgasse 41 A1210, Vienna, Austria.

**D**esigners working with switched-mode power supplies sometimes need to detect a power-down condition at the mains input as quickly as possible. This gives the system time to switch to a backup battery or generate a power-fail interrupt. In most cases, the system is floating with respect to the mains. This can turn

fault sensing into a cumbersome task, especially because transformers can behave erratically during power-down conditions. Sense circuitry at the mains side must be powered from a high voltage with a high power loss. Moreover, timing is difficult to manage concerning load variations.

This circuit, which has a low part

guage function shown in figure 1, performance improves considerably. This routine could also be adapted to interface with other high-level languages.

A program that invokes the assembly-language function can measure the execution time of the BCD conversions either with or without the function (*Fig. 2*). This is done using the built-in timer function. When running this program on a 20-MHz 386 processor with a 387 math coprocessor, the following results are achieved:

Basic test case = 9999,  
execution performance = 15.20703.

BCDBIN test case = 9999,  
execution performance = 0.2695313.

Performance improvement factor = 56.42029. □

```

DECLARE FUNCTION BCDBIN% (BYVAL Value%)
CLS
Test% = &H9999
Loops% = 30000

Start = TIMER ;'Measure empty loop time
FOR i% = 1 TO Loops%
NEXT
Empty = TIMER - Start

Start = TIMER ;'Measure BASIC performance
FOR i% = 1 TO Loops%
Result% = VAL (HEX$ (Test%))
NEXT
BasTime = TIMER - Start - Empty
PRINT "BASIC test case = "; Result%; ", Execution performance = "; BasTime

Start = TIMER ;'Measure BCDBIN performance
FOR i% = 1 TO Loops%
Result% = BCDBIN% (BYVAL Test%)
NEXT
BCDTime = TIMER - Start - Empty
PRINT "BCDBIN test case = "; Result%; ", Execution performance = "; BCDTime

PRINT ;'Performance improvement factor
PRINT "Performance improvement factor = "; BasTime / BCDTime
    
```

## 2. THIS PROGRAM INVOKES

the assembly-language function that performs the conversions. The program uses Quick Basic's built-in timer function to measure the conversions' execution time with or without the assembly-language function.

count and no isolation problems, offers an easy solution for some cases (*see the figure*). All pulse-width-modulator regulating principles adjust the circuit's duty cycle as the ratio from the input to the output voltage. During typical execution, the output voltage stays relatively constant so that the duty cycle is directly proportional to the input voltage. The duty cycle can easily be sensed at either side of the transformer as well as from the pulse-width modulator itself.

For an early warning in case of a power-fail condition, the absolute value of the voltage is of no importance. However, the increasing duty

# That Was Then...

## Quality Comes Through

### Company Delivers On Its Promise Of 12-ns SRAMs

By Hugh G. Willett

SANTA CLARA, CALIF. — Silicon Valley start-up Quality Semiconductor Inc. this week will fulfill its plan to move into high-performance static RAMs. Quality Semiconductor will introduce a line of five 16-kilobit  $\times$  4 SRAMs, implemented in 1-micron CMOS, capable of access speeds as fast as 12 ns. The SRAMs follow by one month the debut of

the company's first product line of standard logic devices, and by two weeks its introduction of high-speed first-in first-out (FIFO) memories.

The new SRAMs are designed for the fast-access primary and secondary cache requirements of high-performance RISC- and CISC-based systems, said Sunneel Rajpal, director of marketing at Quality Semiconductor, Santa Clara, Calif.

"These SRAMs are targeted at systems with clock rates of at least 25 MHz," he said. "Our fast CMOS process lets us add value through performance

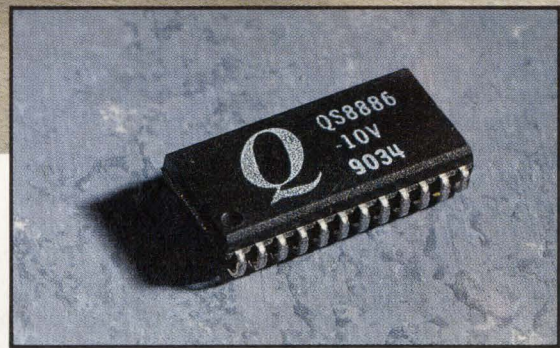
(to page 22)

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Article shown was published in Electronic Buyers News, May 7, 1990

CIRCLE 120

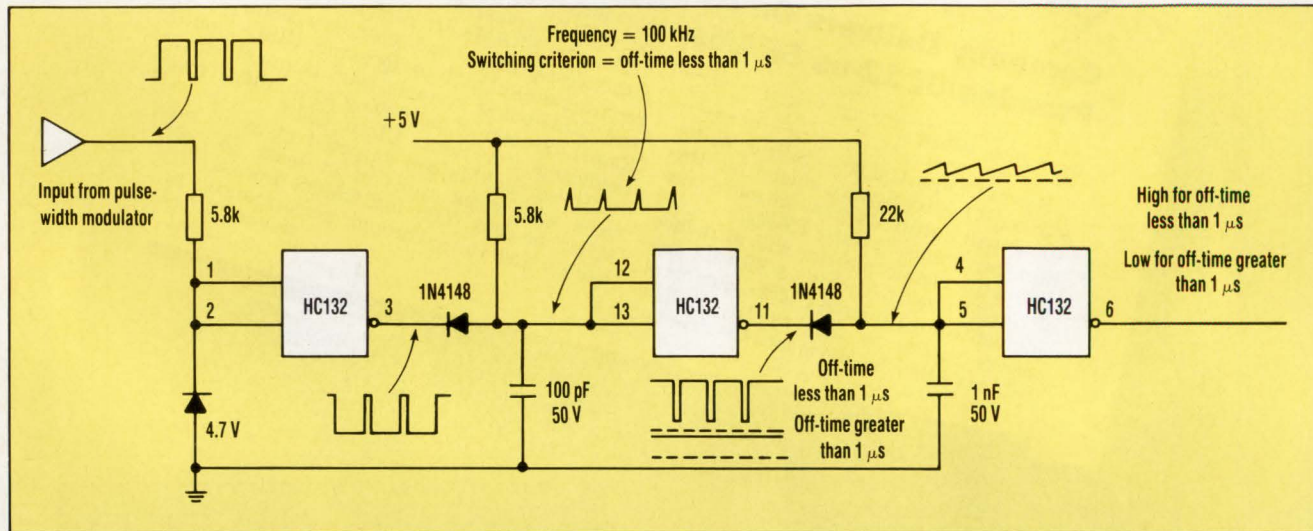
## IDEAS FOR DESIGN

cycle can easily be measured. The circuit indicates a duty cycle with more than 90%, leaving some room for increase before the real power-

down occurs.

The circuit switches to a backup battery with very little delay when the 90% duty cycle is reached, re-

gardless of the reason for the increase. Also, the loss of regulation capability is seen as a power-down condition. □



**THIS CIRCUIT GENERATES** an early power-fail indication by sensing when a pulse-width-modulated regulator's duty cycle reach 90%. The HC132 quad NAND gate's output will be high for an off-time of less than 1  $\mu\text{s}$  and low for an off-time of greater than 1  $\mu\text{s}$ .

### To Electronic Design:

I am writing to express my concern about an Idea for Design that appeared in the Dec. 27, 1990 issue of *Electronic Design* titled "Detect Earth-Line Leakage Current." The circuit does indeed detect earth-line leakage current. It does not, however, protect against shock hazard as the text states.

The schematic shows a connection to a 220-V ac circuit consisting of line, neutral, and safety ground. Typically, utility companies don't provide this type of service, so I'll address the more common 277/480-, 120/240-, and 120/208-V services. The following remarks also apply to the type of service specified in the article, should it be available somewhere.

The problem arises because the service's neutral conductor is grounded. That is, it's connected to a copper rod that's driven into the earth. For this reason, the National Electric Code requires that certain circuits or receptacle outlets be equipped with ground-fault protection to prevent a circuit fault from occurring. The fault current returns to the source through a high-impedance ground path rather than the neutral conductor or the safety-ground wire. An example of such a high-impedance path is a building's cold-water pipe, which is in immediate contact with the earth outside the building.

Should such a high-impedance ground fault occur in equipment using the circuit described in the article, the fault current would return to the source by a path other than the safety-ground wire. The circuit can't detect the condition, nor can it protect against a shock

hazard.

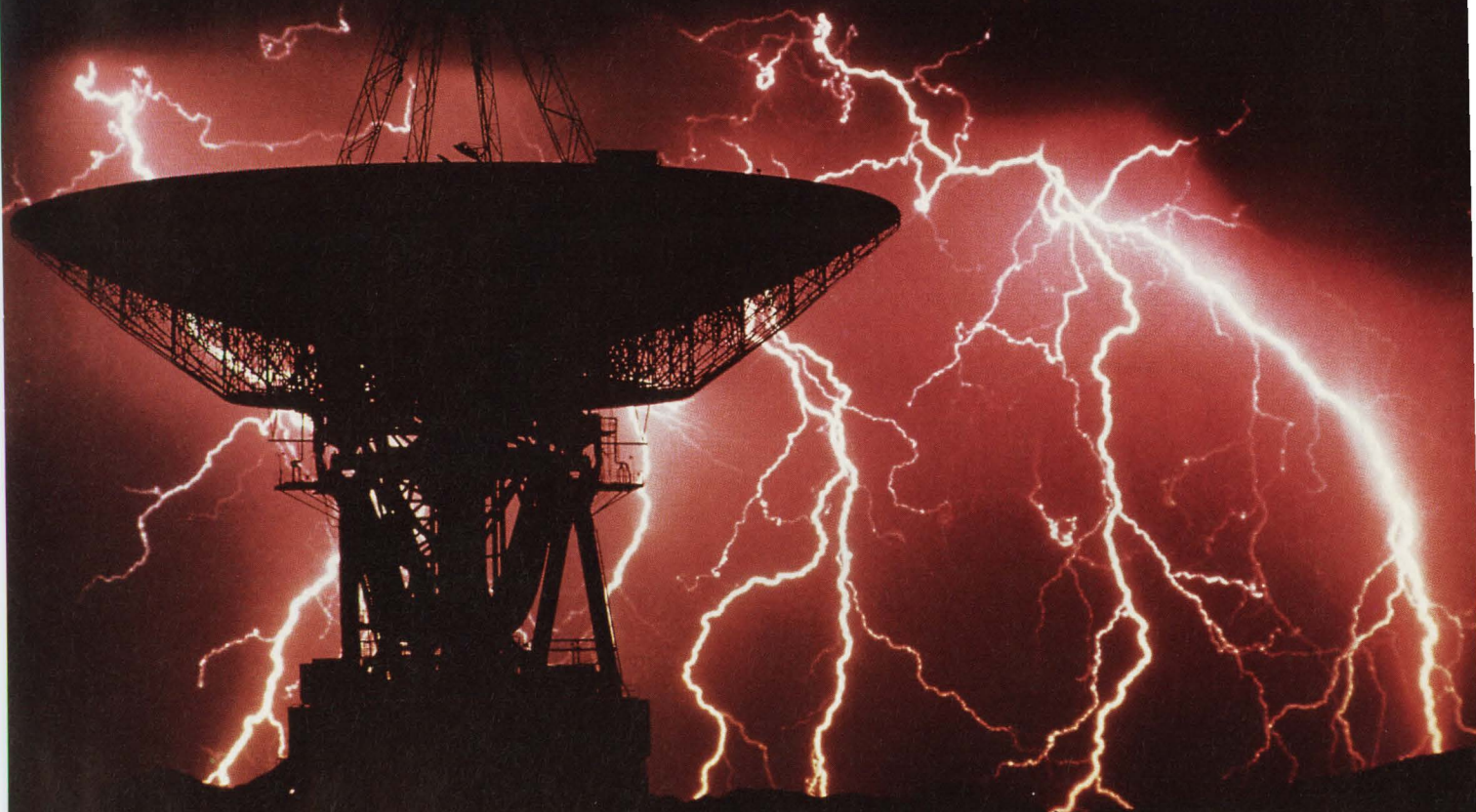
The circuit in the article detects a current in the safety-ground wire caused by, for example, shorting the hot conductor of a single-phase 120-V circuit to a machine frame or some type of electronic apparatus. It'll then trip the breaker, opening the neutral conductor. This won't de-energize the circuit. The hot conductor is still energized with a return path through the safety-ground wire. The circuit would only de-energize by an upstream fuse or by a circuit breaker tripping due to overcurrent in the hot conductor. Anyone using the circuit described in the article for protection against shock hazard is likely to incur substantial product liability for improper design leading to injury or death.

A ground-fault circuit interrupter typically senses the difference between the currents in the hot and neutral conductors. If this current isn't zero, a current must return to the source through a path other than the neutral conductor, and the ground-fault protection should be activated. Usually, a fault current in the safety-ground wire is large enough to trip the branch-circuit protection. If not, the ground-fault protection detects this, opening the circuit, eliminating the hazard.

The circuit described in the article won't protect against a high- or low-impedance fault and shouldn't replace UL-recognized ground-fault circuit protection.

Sincerely,  
Thomas H. Hoover, P.E.

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# WHAT'S ALL THIS COST-ACCOUNTING STUFF, ANYHOW?

Once upon a time, I was down at Lewis' Restaurant in Norwood, Mass., waiting in line to order a Lewisburger, which was a fantastic hamburger with blue-cheese dressing and potato salad and ham. A voice came booming across the noisy restaurant, "Hi Bob." I replied, "Hello Maurice, what's new?" Maurice wandered over and said, "How come you are still using the wrong formula, the *old formula*, for Factory Cost?" Old formula? I never heard of a new formula. You mean the formula of Parts Cost + 450% of Labor Cost is obsoleted? Maurice said, "Oh, that's been obsolete for months. Didn't anybody tell you? The *new* Factory Cost is  $2 \times$  Parts Cost +  $3 \times$  Labor Cost." Well, I ordered my Lewisburger, and ate lunch and bantered with my friends. But on the way back to my office, the wheels began going around in my head. How could they change the formula for Factory Cost and not inform people? How could they accept that, after "a few months," people were still using the incorrect formula, but it was no big deal?



**BOB PEASE**  
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

And they wouldn't bother to tell a guy unless they happened to bump into him at a restaurant? So I went to

see my boss, Richard Randlett, to ask him if he knew what was going on.

He said, yes, he had heard about the new formula, but he didn't know it was officially in effect. And, besides, he didn't want to bother us with unimportant details. We should keep on engineering our designs using good judgment, as usual, and not worry about this "New Factory Cost Formula," and other academic things like that. Not a big deal. Well, okay, I went back to work. But within an hour, I was back at Richard's office.

"Hey, Richard, you know that low-cost converter I am working on?" Yeah. "Well, I was going to use a double-sided pc board, but with the new formula in effect, it would be cheaper to use a single-sided board and a few jumpers. The parts cost will go down quite a bit, but the labor will only increase a little."

Richard sat there. He thought about it for a few seconds. Then he saw red! "No, don't make that change!!" I replied, "But Richard, the new Factory Cost Formula says it's wise to add a few seconds of labor to save a lot on parts cost." But Richard pointed out that even though that was what the bean counters were telling us to do to save money, it would be wrong. He told me to keep on optimizing the costs, assuming that Labor Costs would be multiplied by 4.5 compared to the Parts Cost. Meanwhile, he would try to get this resolved, and get the formula changed back to a reasonable proportion. He'd get me an answer within a month.

Well, one month later, Richard

was still trying to get the problem resolved. Two months later he was gone, and three months later, I resigned. So to this day, I don't know how this was ever worked out. But I did know that I could not do my job if nobody would tell me the rules, and if the rules kept changing to contradict themselves. One set of rules told me that it was wise to add jumpers instead of plated through holes. And a second set of rules told me that was foolish and costly, and I should do it the other way. And if no one could tell me which rules were valid—hey, that's a problem. I needed to solve that problem, but nobody could help me resolve it. So I voted with my feet and left that company, and I haven't worried about that kind of problem. Until recently.

Of late, I was collaborating on a small regulator chip where we wanted to trim the output to high accuracy. That would take about 10 Zenerzap trims. And those would tend to take up lots of die area—probably a 50% increase over the circuit area.

Conversely, if we put in laser trims, that would keep the die size small, but the cost for trimming each die would rise considerably. How much would it rise? We did not have the cost data. And when we got the cost data, it was kind of outdated, and we did not *entirely* believe it. But the time for trimming with 10 laser cuts would basically take an extra second, due to the need to get the laser aligned with the die. And the cost of testing on a tester with a laser is about double—about 4 cents/second—versus 2 cents/second on a tester without a laser.

That is true, even for the tests when you're not using the laser. This is because the whole machine must be paid for, even if you're not utilizing all of the tester. So, 3 seconds  $\times$  4 cents/second is noticeably different than 2 seconds  $\times$  2 cents/second. For an 8-cent difference, you can pay for a much bigger die area!! So that convinced us there was probably a cost advantage if we could avoid laser trimming.

But those considerations were overruled by a more important con-

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## PEASE PORRIDGE

sideration: The need to fit the die in a small package. There were some small plastic packages that the larger (cheaper) die would not fit into. Still, we realized that in the future, we will be sharpening up our pencils more often. What is the right way to keep the costs low? What are the rules in our business? We're not sure, but we're trying to get some of these rules nailed down. Then when it is important, we will have the rules available—and believable. And that's not a trivial statement.

What are the rules in your business? Do you know what they are? Do you believe them? Are they ever subjected to thoughtful scrutiny, or are they so old and dusty that you know darned well that nobody has thought about them for many years? Do people change them without understanding all of the ramifications and repercussions? Maybe it's time for a sanity check.

All for now. / Comments invited! /  
 RAP / Robert A. Pease / Engineer

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### LETTER TO BOB

Dear Bob:

*The most disturbing thing to me about Spice is that many companies have adopted a philosophy of going directly from Spice to board design. You know, and I know, that analog design has too many subtle traps—breadboards must also be built.*

*I've seen too many simulations where the problem wasn't lack of convergence, getting error messages, weird results, or weird waveforms; but rather something even more disturbing: Getting good simulation results on circuits that I knew, or that breadboarding later showed, did not and could not work worth a darn.*

**JERRY STEELE,**  
 Applications Engineer  
 Apex Microtechnology Corp.  
 Tucson, AZ



School of American Ballet student performance: Merrill Ashley. Copyright: Martha Swope, 1967.

## Thanks to the Library, American dance has taken great leaps forward.

American dance is more popular than ever, and one of the reasons is The New York Public Library's Dance Collection.

Choreographer Eliot Feld says the Library at Lincoln Center is "as vital a workroom as my studio." Agnes de Mille says, "the revival of any work is dependent on access to the Library's Dance Collection."

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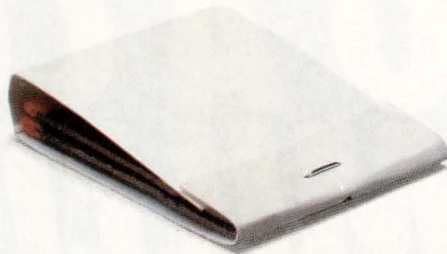
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**The New York Public Library**

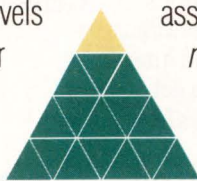
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ENHANCED LOGIC-SYNTHESIS TECHNOLOGY CREATES DESIGNS WITH OVER 20K GATES USING INNOVATIVE OPTIMIZATION AND MAPPING ALGORITHMS.

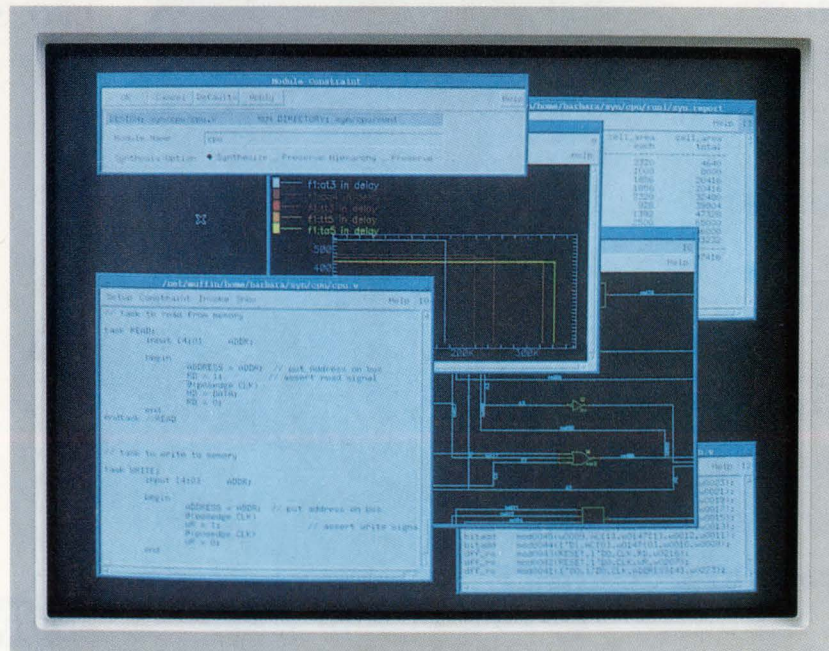
# SYNTHESIS TOOLS COMPLETE FRONT-TO-BACK EDA SYSTEM

LISA MALINIAK

**T**

he second generation of logic-synthesis technology has arrived with the addition of enhanced synthesis capabilities to Cadence Design Systems' toolset for the design of ICs, ASICs, and PLDs. The introduction of the Improvisor and Optivisor synthesis tools spotlights the first commercially available design-synthesis technology developed specifically as an integral part of framework-based electronic-design-automation (EDA) systems. The synthesis technology is integrated into Cadence's Amadeus System Design Series and Opus IC Design Series operating under the Design Framework II.

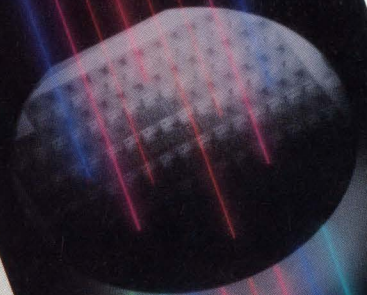
The two new synthesis products have capabilities unavailable with previous synthesis products. These abilities include the synthesis of designs over 20k gates; one library for all simulation, verification, and analysis functions; timing-driven constraints throughout the entire design cycle;



**BOTH THE IMPROVISOR AND OPTIVISOR** tools run under Cadence's Design Framework II. The trade-off curve, shown in the middle window on the screen, displays multiple results of synthesized circuits based on a range of timing or area goals.

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## LOGIC-SYNTHESIS TOOLS

and the leverage of Cadence's ASIC vendor relationships.

The Cadence synthesis technology creates gate-level circuits from hardware-description-language (HDL) files. Initial releases will support 100% of the Verilog HDL. VHDL versions of the synthesis products are planned for release in the second half of this year. In addition, future releases will support testability, FPGAs, and ECL technology.

One major benefit of the Cadence synthesis technology is its tight integration with a proven design environment. This includes existing libraries, mixed-level design entry, simulation documentation, and physical-layout and verification tools. These familiar tools furnish consistency across all stages of the hardware-design process. In addition, the tight integration means that users have a common technology data source for the entire design cycle.

Tracking timing constraints through various abstraction levels and between design tasks has traditionally been a manual process. Cadence's common delay-calculation capabilities, however, automate this function. Timing constraints are transferred through levels of abstraction and between design tasks.

Another benefit of the synthesis tools' integration with the Cadence environment is the access to the full suite of the company's physical-layout tools. This access permits forward and backward transfer of data between logic and physical design. Consequently, designs can be resynthesized if errors or constraints are discovered at the back-end of the design cycle.

The same language format is used for simulation and synthesis. A unified library is employed for all analysis tasks. Using one library ensures consistent results across all analyses within a design, and provides access to Cadence's entire suite of certified ASIC libraries.

Improvisor generates gate-level descriptions from mixed-level HDL inputs. It can explore design alternatives early in the design process: The Improvisor draws a trade-off curve to display multiple results based on a

range of timing or area goals (*see the figure*). Users aren't forced to commit to specific ASIC technology or even a specific ASIC technology until an optimal result is achieved. Once a desired format is decided upon, results can be directed to optimization and mapping capabilities for implementation as custom ICs, ASICs, or PLDs.

Optivisor is a synthesis technology that optimizes the gate-level circuits generated by the Improvisor. Therefore, it requires at least one Improvisor as a prerequisite. Optivisor has optimization and mapping capabilities for automating much of the traditional manual processes involved in producing fully optimized results. It accepts gate-level descriptions and automates low-level design decisions by finding an optimal implementation in a given library based on users' constraints.

The tool's timing-optimization algorithms were developed to handle large designs without sacrifices in speed. The tool uses partitioning techniques that preserve optimization opportunities based on recognized relationships between circuit elements. These relationships include complex operators such as adders and subtractors. A proximity-driven technique explores timing-optimization alternatives. Intelligent-mapping algorithms produce circuits that are mapped to models and ready for layout. The proximity-driven technique combined with intelligent-mapping algorithms results in an optimization capability that can handle larger designs (bigger than 20k gates). □

### PRICE AND AVAILABILITY

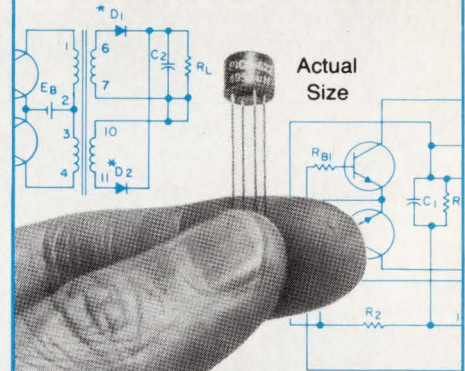
*Pricing for the Improvisor and Optivisor starts at \$15,000 and \$35,000, respectively. The synthesis products, which run on Unix-based workstations, will be available next month.*

*Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. CIRCLE 512*

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**C**ommunications-system designers are often faced with the job of implementing different interfaces in the same piece of equipment. These may be serial interfaces to wide-area networks, as well as serial interfaces of a more local nature, such as for asynchronous terminals, printers, modems, and other peripherals. However, within that single piece of equipment, all of these interfaces must operate side-by-side, placing a great demand on choosing a suitable serial communications controller that's both flexible and is relatively inexpensive.

Until now, this demand has fallen short of expectations because no available controllers offer the needed versatility. To be sure, there are low-cost controllers, but these can be used only for asynchronous data transfers. Others are dedicated solely to telecommunications uses and are ill-suited for local data-communications applications. Still others are too slow for many of today's exacting demands. Moreover, because the controllers come from different manufacturers, they're not mutually software compatible.

This is where a new serial multiprotocol communications controller from Germany's Siemens AG steps in. The SAB 82532 finally lets designers implement all serial interfaces for both data and telecommunications applications by using a single controller type and uniform software. The device offers two independent full-duplex serial channels and can control synchronous and asynchronous data transfers at rates up to 10 and 2 Mbits/s, respectively.

Made from Siemens' 1- $\mu$ m CMOS process, the controller features 64-byte transmit and receive first-in, first-out (FIFO) buffers per channel. Furthermore, it has an 8-/16-bit microprocessor interface for Motorola and Intel bus architectures (*see the figure*). Power consumption is only 50 mW at 2 Mbits/s.

The new controller's two full-duplex serial channels are independent of each other. This independence facilitates the task of software design. Either of the device's two channels supports various data-communications protocols. These protocols include asynchronous data transfers (for instance, through the RS-232 or V.24 interfaces), as well as synchronous character- or byte-oriented transfers. They also include diverse bit-oriented HDLC (high-level data-link control)-based data-transfer protocols.

The device offers special functions, such as back-to-back, or shared-flag, transmission, which is necessary for high-speed data communications. It can be programmed for four different operating modes: auto, non-auto, transparent, and extended-transparent. The extent of protocol support in each case depends on the operating mode that's selected.

Where applicable, some of the functions supported in the auto mode reduce the amount of protocol software

# MULTIPROTOCOL COMMUNICATIONS CONTROLLER

required considerably. These include protocol handshaking, programmable timeout, or retransmission functions.

Further reduction of protocol software is possible thanks to the 82532's checking of maximum packet size, and its maskable address-recognition feature with HDLC transfers. Savings in device-supporting software are achieved by cyclically transmitting the multiprotocol controller's FIFO contents, which is possible in the extended-transparent mode.

For maximum versatility when linking to different transmission media, the 82532 multiprotocol controller IC supports all common data-encoding and decoding schemes. Among these schemes are nonreturn-to-zero (NRZ), NRZ-I (inverted), biphasic space and biphasic mark, and Manchester techniques.

Either channel of the multiprotocol controller device has a fast digital phase-locked loop circuit to recover the synchronous bit clock from the incoming data streams at a data rate up to 4 Mbits/s, without the need for any separate sync information on

auxiliary lines. Clock recovery can also be supported with an optional one-bit insertion. Because of fast clock recovery, the controller chip can also be employed in optical data-transmission systems.

For synchronization, the 82532 sends a programmable preamble with a selectable number of repetitions (up to eight times). It also performs functions like interrupt-request generation at transmit-frame end or time-slot assignment, functions which until now could be realized only with the use of complementary glue logic.

The device's 16-bit data bus has a direct access to all FIFO buffers and registers. Because there's no recovery time necessary between two consecutive CPU accesses to the 82532 multiprotocol controller IC, both 8- and 16-bit accesses are possible. The microprocessor interface is extremely fast and permits excellent data throughput to occur on the system side.

The throughput can be increased further by data exchange in the direct-memory-access (DMA) or interrupt modes. This, together with the

large 64-byte FIFO buffer for each channel as well as transfer direction, decouples the 82532 from the CPU. The CPU is thus relieved from critical reaction times and from any excessive loading by the serial interface side.

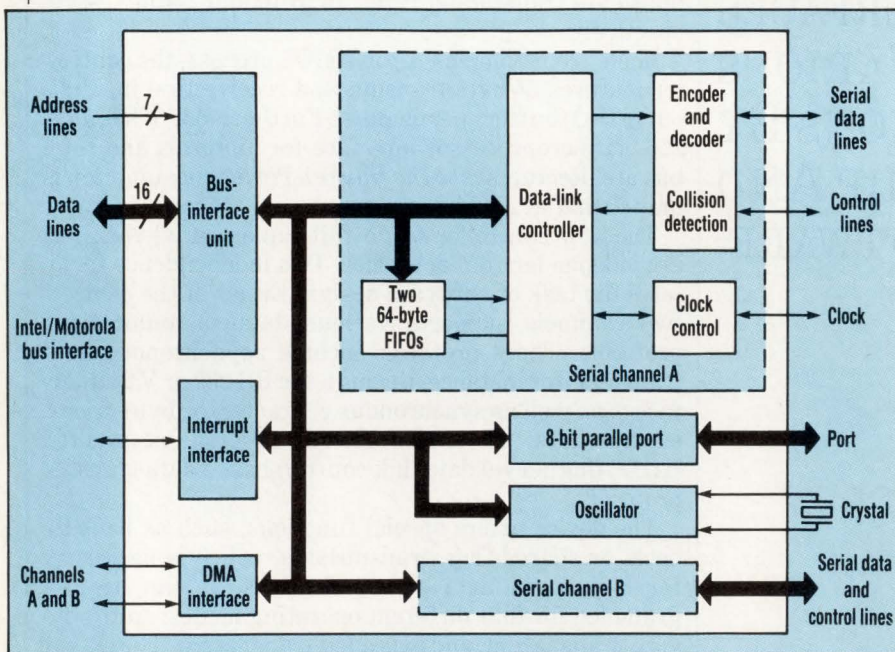
The Siemens 82532 multiprotocol communications controller IC supports fast interrupt handling with relatively simple software. That's because aside from non-vectorized interrupts, it also uses vectored interrupts with on-chip vector generation. Interrupt cascading is possible in both the daisy-chain and slave configurations. This capability considerably simplifies the necessary interrupt hardware.

DMA transfers to and from the 82532 communications controller are supported by a four-channel DMA interface with one request line for each transmitter and receiver of both serial channels. Furthermore, the device offers a programmable, bidirectional 8-bit parallel input/output port for optional use. In many applications, this parallel I/O facility cuts hardware costs.

## AN APPLICATIONS MIX

The 82532 is well-suited for various datacom and telecommunications tasks. Datacom applications include office computers, workstations with the X.25 interface, and synchronous terminal clusters. In large systems, the controller can be used for internal communications between subsystems. Other datacom applications include multiprotocol communication cards for general networking, primary-rate interface cards, bridges and gateways, telemetry systems, terminal multiplexers and servers, and various multimaster configurations.

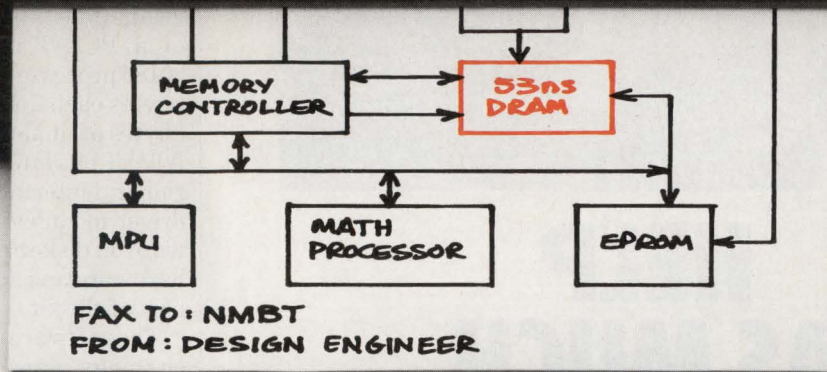
In the telecommunications sector, the 82532 performs such functions as data-packet assembly/disassembly and central signaling in public switched networks. It also handles many tasks in private networks using time-slotted packet transfer. In primary-rate interfaces, it can transfer signaling data or implement serial data channels. It can also be used in integrated-services digital-net-



**WITH TWO INDEPENDENT CHANNELS**, the Siemens SAB 82532 multiprotocol communications controller links to various data and telecommunications applications with uniform software. A large 64-byte FIFO buffer for each channel facilitates data transfers.

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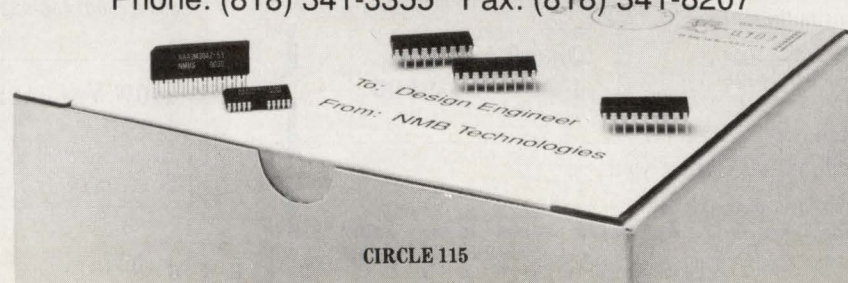
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## MULTIPROTOCOL COMMUNICATIONS CONTROLLER

work (ISDN) terminals as well as in base stations for digital mobile radio.

To facilitate the 82532's system integration, Siemens offers an inexpensive design tool, the Easy532 evaluation kit. The Easy532 consists of a PC/AT add-on card with an 80186 processor, the 82532 itself, 128 kbytes each for RAM and EPROM, 2 kbytes of dual-port RAM, a fast 8-bit AT/XT bus interface, and a serial peripheral interface to connect diverse driver modules. The necessary software on diskettes and the associated hardware and software manuals are part of the kit.

The software contains, among other things, a menu utility that introduces the programming of initialization routines and data transfer, and protocol handling. The user software can be designed on a PC and then downloaded to the add-on card by way of download routines. These routines are part of the Easy532 software. Furthermore, the software also includes a macro library for C language and a local-area-network analysis program.

In addition to the two-channel 82532, Siemens will have the software-compatible 8-channel version, the SAB 82528. It integrates four SAB 82532s on one chip. The device cuts board space and minimizes power consumption to only -120 mW for eight channels. □

### PRICE AND AVAILABILITY

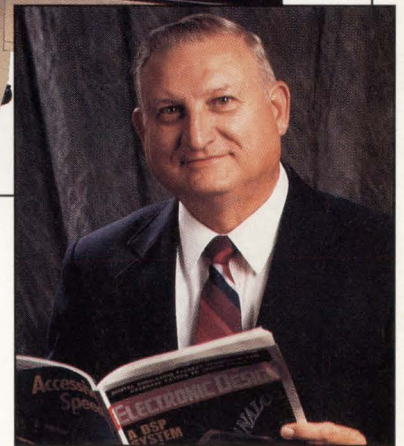
*Housed in a compact 68-pin plastic-leaded chip carrier for surface mounting, the SAB 82532 is now available as engineering samples. Large quantities can be had by early summer this year. By 1992, the 2-Mbit/s version will sell for \$13 each and the 10-Mbit/s type for \$19.50 each in 10,000-unit lots. The Easy Evaluation Kit, already available, costs \$750. As for the 8-channel SAB 82538, engineering samples will be offered in the fall of 1991. For the 2-Mbit/s version, the expected price in 1992 will be around \$70 each in 1000-unit lots.*

**Siemens AG, Semiconductor Div., P.O. Box 801709, D-8000 Munich 83, Germany; (089) 4144-3728. Siemens Components Inc., 2191 Laurelwood Rd., Santa Clara, Calif. 95054; (800) 456-9229. CIRCLE 513**

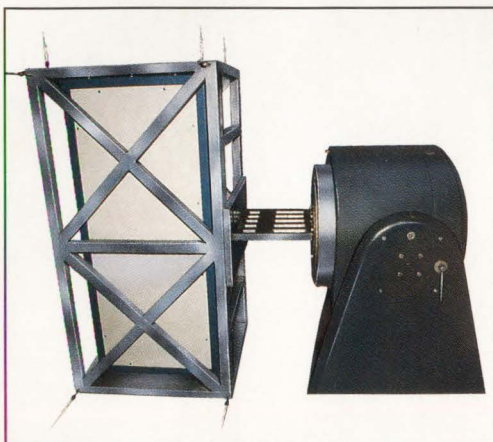
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# BUS-MASTER CHIPS SIMPLIFY SMART NETWORK CARD DESIGN

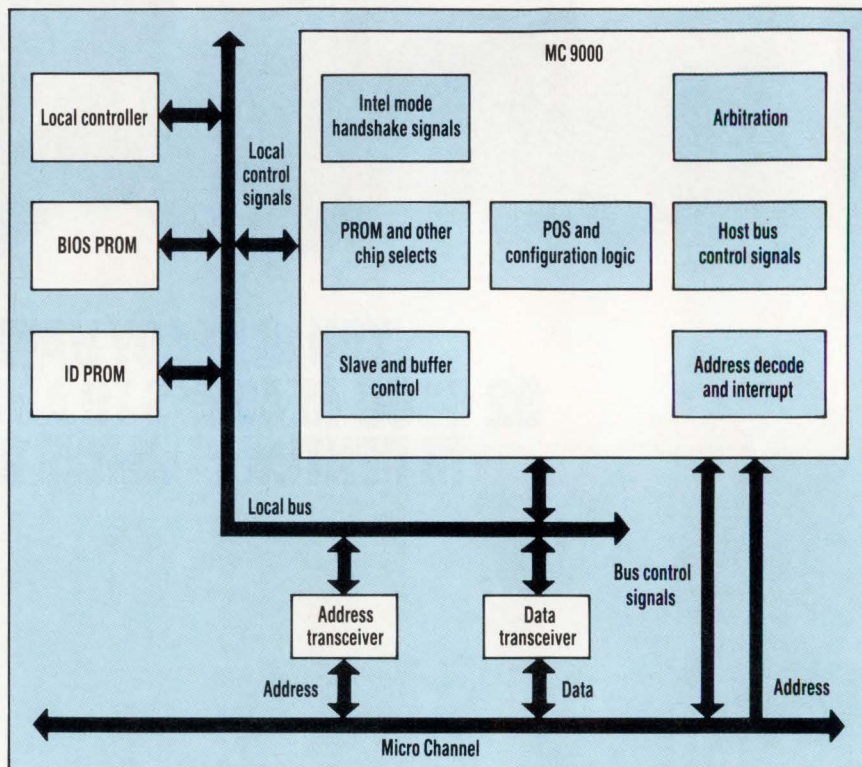
DAVE BURSKY

A family of interface chips, the 90X0 series, has been designed to simplify implementing bus-master cards for the IBM Micro Channel and AT (ISA) buses, as well as the extended ISA (EISA) bus. The chips, developed by PLX Technology, come in a "generic" option and in versions designed to tie into specific peripheral chips—various company's network controllers.

The first application-specific versions of the 90X0 family will tie directly into popular local-area network support chips from Intel (the 82596), National Semiconductor (the DP83932), and Texas Instruments (the TMS380C16/4). They will considerably reduce the complexity and cost of a bus-master network card by eliminating many of the simpler chips that clutter the card.

Generic versions of the 90X0 series of interface chips—the 9000—are available for either the ISA, EISA, or Micro Channel buses. Included on the bus-master interface chip are various handshake control signals for the logic on the bus-master card, various control and arbitration circuits for the host-bus interface, system configuration logic, and slave and buffer control circuits.

The 128-lead bus-master interface chip puts all of the necessary control functions as well as some optional bus logic onto one chip. With the architecture selected by PLX, the local-area network controllers can use their own FIFO buffers and DMA controllers, while also implementing a complete bus-master interface, including the EISA burst mode and the Micro Channel streaming data mode. In contrast, bus-master chips offered by other companies typically include their own DMA controllers, which force designers to bypass the DMA blocks and FIFO buffers that are on the network controllers, such as what Intel and National Semiconductor offer in bus-master chips. That, in turn, would lower overall



system throughput.

All of the bus versions of the 90X0 chips have identical sets of configuration registers. As a result, Node ID software, BIOS software, and features like chip-select addresses can all be reused, with minor changes, as the core of multiple driver programs—each written for a specific platform. Similarly, most of the board's physical design can be reused as well. Configuration registers can be employed with either static or dynamic programming of board ID information, four interrupt request levels, number of wait states, address device levels, port selection information, and four user-definable programmable configuration bits.

The generic version of the controller, the AT 9000, ties directly to an AT bus and provides all of the local control for the on-board function as well as the AT bus control signals. Similar versions of the generic chip are available for the Micro Channel

and EISA buses. The more application-specific versions are the AT 9010, MC 9010, and EISA 9010, all for the National DP83932 local-area network controller; the AT, MC, and EISA 9020 for the Intel 82596 local-area network controller; and the AT, MC, and EISA 9030 for the TI TMS380C16. The MC series parts can perform 40 Mbyte/s transfers by using the streaming state mode, while the EISA chips will transfer 33 Mbytes/s. AT-bus versions support single-cycle adapter-to-memory transfers.

Samples of most of the 90X0 series of bus-master chips are immediately available, with all the chips expected to be ready in the second quarter. Prices in 10,000-unit lots start at \$12.50 each for the AT version and go up to about \$17 each for the MC or EISA versions.

*PLX Technology Inc., 625 Clyde Ave, Mountain View, CA 94043. Gaylord Galiher, (415) 960-0448.*

CIRCLE 361



## CMOS DOUBLE-PRECISION FP CHIP HITS 100 MFLOPS

A family of floating-point processors—the W4X64 family—achieves peak throughputs of 100 MFLOPS, the highest yet for a CMOS processor. It achieves this performance by integrating all of the major functions required for the implementation of double-precision floating-point computations.

The functions integrated on the chip include the register file, independent floating-point ALU and multiplier/divider blocks, and the control logic. The Weitek processors run at a maximum clock rate of 50 MHz, and because the ALU and multiplier blocks are independent, two floating-point operations can occur simultaneously. As a result, the chip has a computation throughput of twice the clock rate.

Furthermore, because the chips are implemented in a 0.8- $\mu$ m CMOS pro-

cess, they won't require any special cooling arrangements. All versions of the chip consume between 2 and 3 W of power.

In addition to the four basic floating-point math functions, each chip also performs 32-bit integer, square-root, reciprocal, and reciprocal square-root operations. All of the chip's floating-point math operations are IEEE-754 compatible, ensuring that the results will match those obtained on large computers that are IEEE compatible.

A key aspect of the math chips is an on-chip multiplexed 32-word-by-64-bit register file that supplies operands and holds results for both the ALU and the multiplier/divider block. The W4164 has an eight-ported register file, while the 4364's file requires nine ports. The multiple ports permit simultaneous loading and storing so that both the ALU and multiplier/divider blocks can

run independently.

There are two versions of the math chip. The 4164, which has one 64-bit I/O port, is suited for coprocessor applications at the moderate-to-high performance levels needed by the lower tier of scientific and technical desktop systems. The 4364, which has three 64-bit ports, delivers a much higher throughput, making the chip well suited for vector-processing operations.

The math and ALU blocks do a full computation every clock cycle. However, the chips have a three-cycle register-to-register latency for all operations. Samples of the 207-lead pin-grid-array housed single-port chip will be available next quarter, while the 447-lead PGA-housed triple-port version will be sampled in September. In 1000-unit quantities, the W4164 sells for \$575 each, while the 4364 goes for \$625 each.

*Weitek Corp., 1060 E. Arques Ave., Sunnyvale, CA 94086; (408) 739-4374.*

**CIRCLE 362**

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### Digitizing Oscilloscopes

From the opening shots of an abacus, slide rule, and other measurement tools that time has passed by, the premise of this video is clear: digitizing oscilloscopes have made their analog brethren obsolete. The 12-minute presentation illustrates many of the benefits that the company's state-of-the-art family of HP-54500 digitizing oscilloscopes provide, such as self-test capabilities, high accuracy, advanced display modes, and full computer compatibility. The video concludes with a brief look at the characteristics of the three current members of the 54500 series, each offering different price/performance combinations. **Free Video.**

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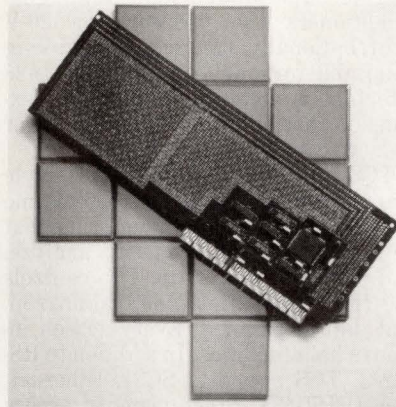
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## PROTOTYPE BUS-SPECIFIC BOARDS UP TO 100 MHz

Designers can get help developing Eurocard and bus-specific circuit boards with the Vectorbord 50 prototyping-board family. The family, available from Vector Electronic Co., works with the latest high-speed CMOS, ECL, RISC, and Sparc-based microprocessors. The operating frequencies of the prototype boards can range from 50 to 100 MHz. Using the Vectorbord 50, applications for test equipment, graphics, communications, or advanced DSP can be prototyped at actual operating frequencies. The prototyped boards can either be shipped as a final product or the design can easily be converted to full-production boards. The initial release is an EISA product; all popular buses will be supported later.

The boards take advantage of the company's Vectorwire technology. Vectorwire uses embedded-polyimide insulated discrete wires and plated through-holes for circuit interconnection. The round wires supply high-quality signal transmission-line properties, and the insulation lets them cross without shorting. This feature eliminates the need for vias, providing high density with just two levels of wire. And



routing is simplified because of the independence of each wire and the elimination of the vias.

The EISA product comes with an Intel bus-master interface chip and glue logic installed and connected. This gives designers the ability to incorporate their application according to the EISA bus standard with a guaranteed compatibility. The board is available now. Prices depend on configuration.

**Vector Electronic Co., 510 Broadhollow Rd., Melville, NY 11747; (516) 293-6300. CIRCLE 365**

■ RICHARD NASS

## 40-MHz MILITARY BOARD PUSHES 3.6 MIPS

Designed for the military market, the PaceRunner/1750AE VMEbus board comes in 20-, 30-, and 40-MHz versions. The single-board computer offers a sustained throughput of 3.6 MIPS. The board is based on Performance Semiconductor's Pace1750AE chip set and microprocessor. The 16-bit processor is designed for floating-point and integer arithmetic with real-time support. It supplies 13 addressing modes, including direct, indirect, indexed, and based, and it can access 4 Mbytes of segmented memory space. The board comes with 256 kwords of high-speed static RAM, an on-board monitor program, and a built-in system test program. Connection to the board is done through two serial ports, a VMEbus interface and a development system port. All three boards are available immediately. The 30- and 40-MHz versions cost \$13,120 and \$16,400, respectively.

**Performance Semiconductor Corp., 610 E. Weddell Dr., Sunnyvale, CA 94089; (408) 734-8200. CIRCLE 366**

## 386 AT COMPUTER FITS ON COMPACT EUROCARD

Built around a 16- or 20-MHz 80386SX microprocessor and an 80387SX math coprocessor, the GESMPU-38 PC/AT board from Gespac fits on a single-height 160- by 100-mm Eurocard. The board includes the functionality of page-address registers, a timer, interrupt control, a real-time clock with battery-backed RAM, and a keyboard controller.

It also comes with two serial ports, a bidirectional parallel printer port, a floppy-disk controller, and a hard-disk bus interface.

The GESMPU-38 is expandable through a bus interface to any of over 400 I/O modules from Gespac and other third-party vendors. The board can run MS-DOS, Unix, OS 9000, and other operating systems for applications needing real-time or multitasking environments. The GESMPU-38 is available now for \$2195 with 1 Mbyte of on-board RAM.

**Gespac Inc., 50 W. Hoover Ave., Mesa, AZ 85210; (602) 962-5559. CIRCLE 367**

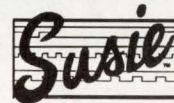
## CAPTURE IMAGES ON A PC

Designed as a video-image capture system for IBM XT/AT and compatible PCs, the Supervision/8 board consists of a frame-grabber board and its accompanying image-capture software. The board allows images to be captured from any RS-170 source, including a camera, a video tape, or even a live broadcast.

The image is captured with a resolution of 256 pixels, using 256 shades of gray. The resulting picture can be displayed on any standard PC-type monitor that supports Hercules monochrome, CGA, EGA, or VGA graphics standards. The image can also be adjusted, then stored or printed on a dot-matrix or a laser printer.

The board is available from stock in single quantities at a price of \$269.95 each. Large-quantity discounts are also available.

**IDEC Inc., 1195 Doylestown Pike, Quakertown, PA 18951; (215) 538-2600. CIRCLE 368**



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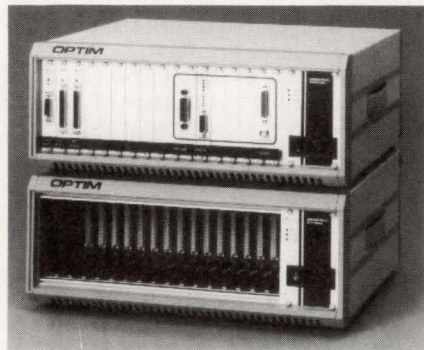
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CIRCLE 80

## MODULAR DATA ACQUISITION SYSTEM INCLUDES POWERFUL SOFTWARE

The Megadac 3000 series data acquisition systems feature a 16-bit analog-to-digital converter, 25,000-sample/s speed, and a 128-kbyte memory (expandable to 2 Mbytes). Included is Optim's Test Control Software (TCS), which speeds system setup and operation.

The basic mainframe, the 3008AC, comes with the ADC and an 8-channel analog input module, leaving eight empty slots. Users can choose from a large selection of analog, digital, and



thermocouple input modules and signal conditioners. The 3008 works on 120-V ac or, optionally, 12-Vdc power, making it suitable for mobile use. An IEEE-488 interface is included. The 0016AC expansion chassis adds 15 slots for larger or more complex applications.

TCS is driven by an index-card-style menu. The software boasts real-time graphics plotting and monitoring that help users collect, convert, analyze, and plot measured data. TCS controls the filter, amplifier gain, calibration, and digital balance. Every screen includes help facilities. In addition to RS-232-C, TCS supports SCSI, Ethernet, and IEEE-488 direct memory access transfers between the 3008 and the host computer.

An entry level 3008 system, including the ADC and TCS software costs \$7995 and is available on a 6-to-8-week delivery schedule.

*Optim Electronics Corp., Middlebrook Technical Park, 12401 Middlebrook Rd., Germantown, MD 20874; (301) 428-7200. CIRCLE 369*

■ JOHN NOVELLINO

## MODULATION ANALYZER DISPLAYS FREQUENCY, TIME-INTERVAL DATA

With its ability to display continuous frequency and time-interval measurements, the HP 53310A modulation-domain analyzer lets designers of a wide range of complex circuits characterize them quickly, visually, and directly.

A modulation-domain analyzer plots frequency and time-interval measurements versus time, just as an oscilloscope shows voltage versus time. Such capability helps designers understand potential sources of jitter and other forms of undesired modulation in ICs, video and compact disk systems, and digital communications systems. Additionally, the analyzer's statistical functions offer insight into the operation of a variety of spread-spectrum applications.

Measurements are available from dc to 200 MHz, with a 2-GHz option, at measurement rates up to 2 MHz. The display updates 20 times a second, and standard memory is 16 ksamples, expandable to 64 ksamples. An autoscale feature permits one-button setup, and

the rest of the operation is menu-driven. The instrument can trigger on frequency or time-interval value or on an external trigger.

The analyzer combines measurements and processing functions on one IC. The HP-designed universal-counter IC keeps track of data events and time through the use of zero-dead-time counters. It computes results on the fly, enabling them to be updated and displayed graphically 20 times a second. Additionally, the circuit's speed allows the HP 53310A to trigger on user-specified frequency or time-interval values, eliminating the need for an external trigger.

The HP 53310A modulation-domain analyzer costs \$9500. An optional third channel costs \$1450, and an oven-controlled time base is priced at \$1600. Delivery is estimated at 4 weeks after receipt of an order.

*Hewlett-Packard Co., Santa Clara Div., P.O. Box 58059, Santa Clara, CA 95052-8059; (800) 752-0900.*

CIRCLE 370

■ JOHN NOVELLINO

## ADVANCED SOFTWARE EASES TEST PROGRAMMING

Because it uses the Rational Systems Inc. DOS/16M DOS extender and virtual memory manager, LabWindows 2.0 offers many features previously not possible. One, the User Interface Library makes it easy to create graphical



interfaces and integrate them into applications programs. Users can make full-color panels with elaborate graphs, strip charts, and input and output controls. Also, the software development system can now dynamically load external libraries and objects written in C into the Interactive Program. As a result, programmers can use their own external libraries and C code as if they were standard LabWindows libraries. The package requires an 80286-, 386-, or 486-based PC running MS-DOS 3.0 or later, and 2 Mbytes of RAM. LabWindows costs \$495 and an Advanced Analysis Library sells for \$895. Together, the packages sell for \$1295.

*National Instruments Inc., 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. CIRCLE 371*

## EMBEDDED CPUS GET DEVELOPMENT TOOLS

Adding to its extensive line of microprocessor development tools, Hewlett-Packard has released emulation and analysis tools for the Series 32000 embedded processors from National Semiconductor Corp. The new tools will support the 32FX16, 32CG160, 32CG16, 32GX320, and 32GX32 imaging processors, as well as the 32525 general-purpose microprocessor. The tools are part of the HP 64700 family of development tools and provide real-time, nonintrusive emulation with analysis of the processor's address, data, and status buses. The software permits symbolic debugging and code-coverage testing. Optionally available is a 25-MHz state or 100-MHz timing analyzer. Prices start at \$23,000 and delivery is in 4 weeks.

*Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. CIRCLE 372*

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**P**rogrammable gain amplifiers (PGAs), both software controlled and pin-strapped, typically offer gains of 1, 2, 4, and 8, or 1, 10, 100, and 1000. If finer control is needed, it basically comes down to a "do-it-yourself" process. However, a new family of wideband software-controlled PGAs from Frequency Devices gives you additional options. Called the 830PGA Series, its three members—the 830PGA-20, 830PGA-40, and 830PGA-60—offer programmable gains of 0 to 20, 0 to 40, and 0 to 60 dB, respectively. Also, their gain-steps run 0.5 dB, 1.0 dB, and 2.0 dB, respectively. This fine-resolution gain control is combined with high-impedance (1-M $\Omega$ ) differential inputs, a full-power bandwidth of 100 kHz for a  $\pm 10$ -V output across 1000  $\Omega$ , and dc response.

Aimed at a wide range of applications, the amplifiers enhance a system's dynamic range. A multichannel

data-acquisition system, which must bring all channels close to full-scale prior to digitization, represents a typical job. Test systems are a natural. By changing gains, a host computer brings the input signal (or signals) up to a reference level for analysis and, in the process, determines its precise amplitude. The gain tolerance of each amplifier is  $\pm 0.02$  dB, and gain and phase match between devices of 0.04 dB and 0.5°, respectively (from 1 Hz to 100 kHz), support such applications. Total harmonic distortion runs just 0.003% at 1 kHz and 0.02% at 90 kHz, while common-mode rejection is more than 60 dB from 10 Hz to 100 kHz. In quantities of 100, the amplifier modules cost \$140 each. Differential outputs that simplify driving balanced lines, such as shielded twisted pair, are a no-charge option.

*Frequency Devices Inc., 25 Locust St., Haverhill, MA 01832; Frank DeGiso, (508) 374-0761. **CIRCLE 373***

■ FRANK GOODENOUGH

### WIDEBAND AMPLIFIER RUNS ON LOW POWER

Most know that op amps with full-power bandwidths beyond even a few megahertz are power hogs. However, the latest current-feedback IC op amp from Comlinear—the CLC406—belies such "conventional wisdom." Running off  $\pm 5$ -V supplies at a closed loop gain of 6 (15 dB) and putting 5 V pk-pk across 100  $\Omega$ , the op amp sports a minimum 3-dB bandwidth of 95 MHz and its response is flat within 0.6 dB at 50 MHz. But it draws less than 5.5 mA from the supply rails with no load—that's just 50 mW. Linear gain and phase are 0.04% and 0.04°, respectively, for both NTSC and PAL TV video signals. For a 2-V pk-pk output driving 100  $\Omega$  at 20 MHz, second- and third-harmonic distortion run -42 and -43 db, respectively. Time-domain specifications reflect those of the frequency domain. Slew rate runs a minimum of 1200 V/ $\mu$ s and the output settles in under 15 ns (maximum) to 0.05% of final value for a 2-V step. Applications range from video distribution and photodiode transimpedance amplifiers to high-speed DAC output amplifiers and driving flash ADCs. To top it off, the CLC406 is inexpensive, just \$4.24 each in hundreds.

*Comlinear Corp., 4800 Wheaton Dr., Fort Collins, Colo. 80525; Tom Baldwin, (303) 226-0500. **CIRCLE 374***

### DUAL DAC GIVES 8-BIT ACCURACY AT 15 MHZ

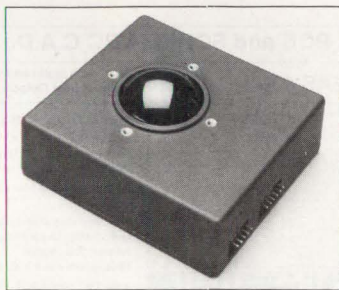
The standard 7528, dual digital-to-analog converter (DAC) was never intended for video applications. However, improved versions of the 7528—the MP7429A/B from Micro Power Systems—are at home with video. Their required write-pulse is just 30 ns and their output current settles to 8-bit accuracy in similar time. These specifications are half and about 1/6, respectively, of that of available devices. A and B versions of these multiplying current-output DACs operate respectively from 15- and 5-V rails. Applications range from audio mixers to pixel correction in video digitizers. Total harmonic distortion runs -95 dB (15 bits). A proprietary bit-decoding technique reduces the maximum binary-weighted current developed by resistors and switches. It aids the DACs' speed and low glitch-impulse, which is just 10 nV-s (nanovolt-seconds)—an order of magnitude below that of the 7528. Three accuracy grades offer best-case differential nonlinearity and gain error of  $\pm 1$  LSB and a relative accuracy of  $\pm 1/4$  LSB (the latter was until now unavailable). In their 14-pin plastic DIPs, pricing starts at \$4.34 each in 100s.

*Micro Power Systems, 3151 Jay St., Santa Clara, CA 95054; (408) 727-5350. **CIRCLE 375***

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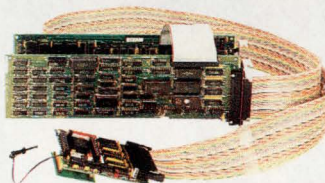
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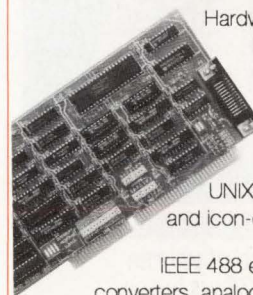
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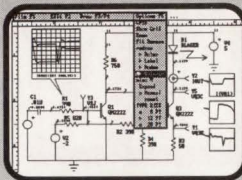
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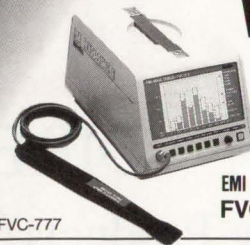


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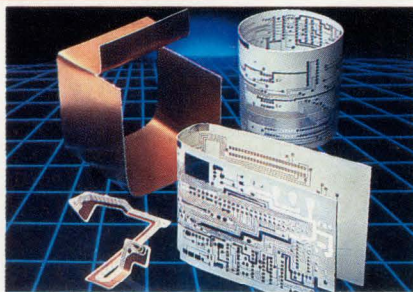
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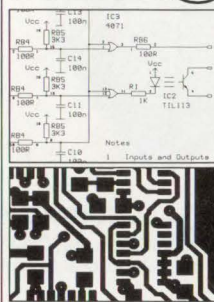
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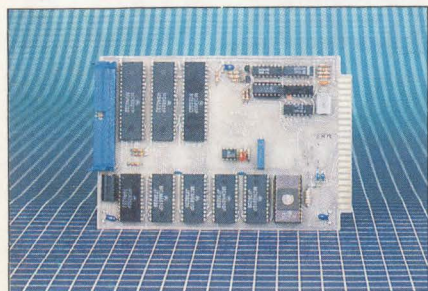
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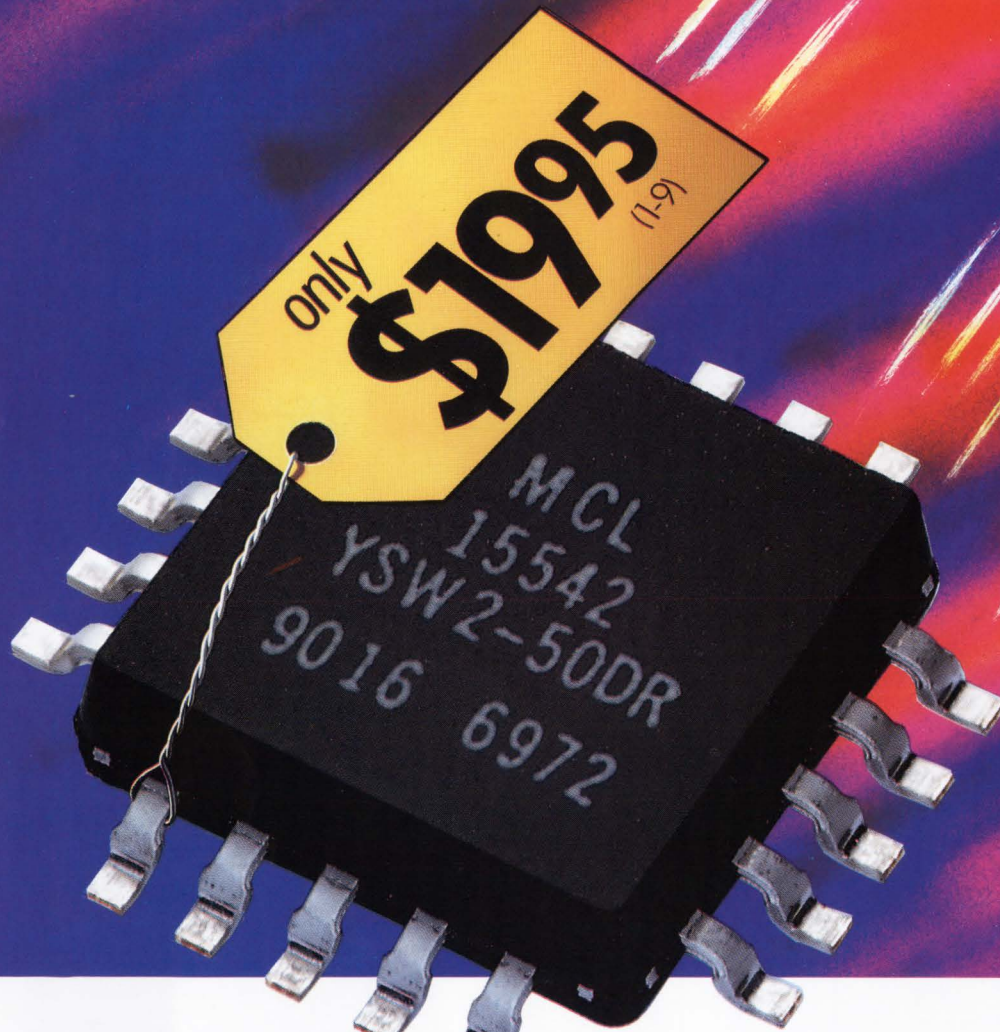
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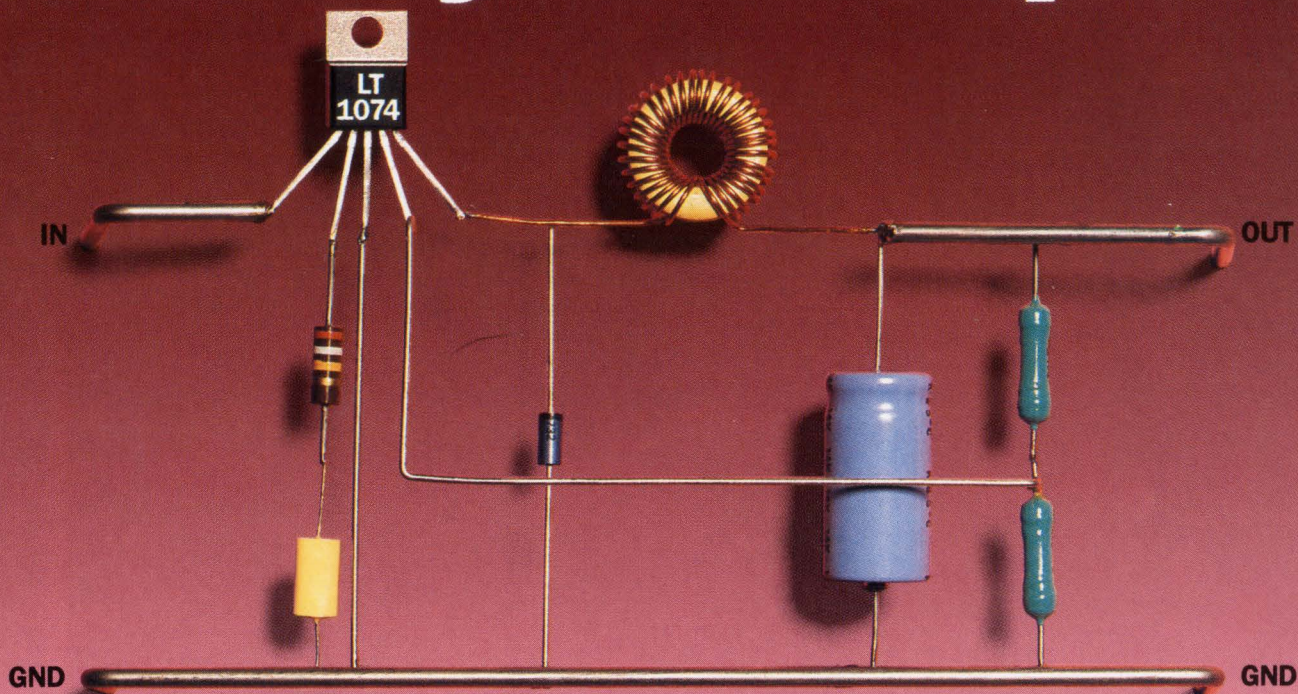
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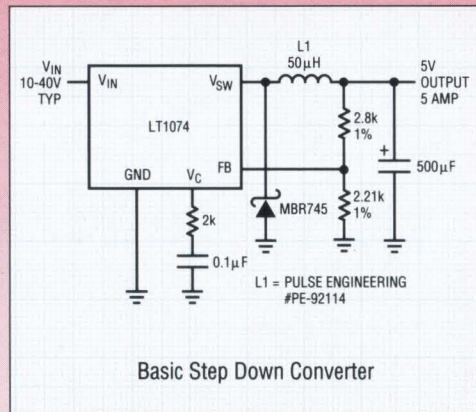
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