MAINTENANCE MANUAL
VOLUME II

LINC-8

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

LINC-8
MAINTENANCE MANUAL

VOLUME II

November 1967

VOLUME II

LINC-8 ENGINEERING DRAWINGS

This volume of the LINC-8 Maintenance Manual contains instruction timing-flow diagrams, engineering drawings, and module schematics not found in other related documents. These drawings cover the basic LINC-8 system described in Volume I and are listed below.

Instruction Timing-Flow Diagrams

Engineering Drawings

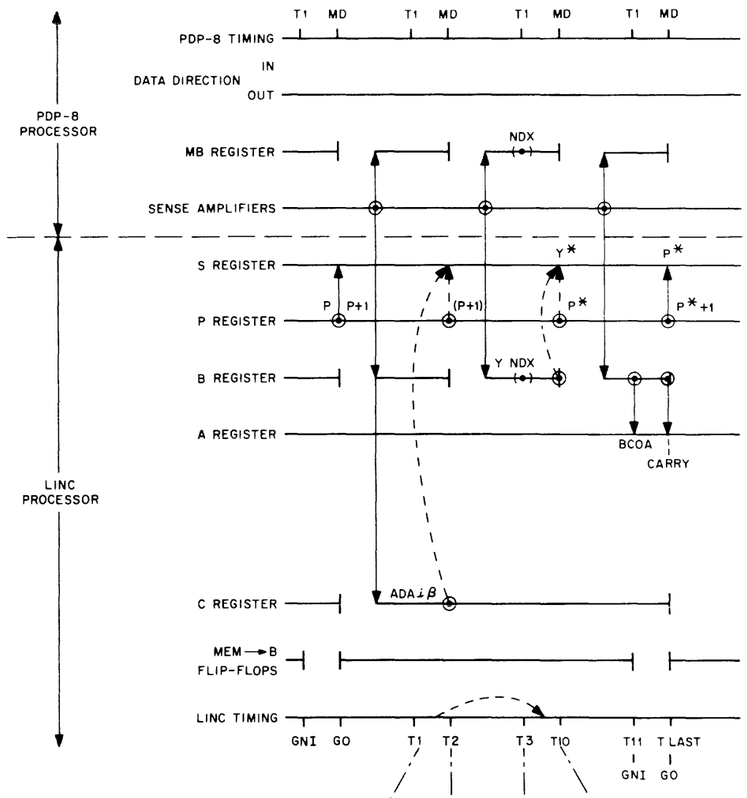
Engineering Drawings (cont)

Engineering Drawings (cont)

Module Schematics

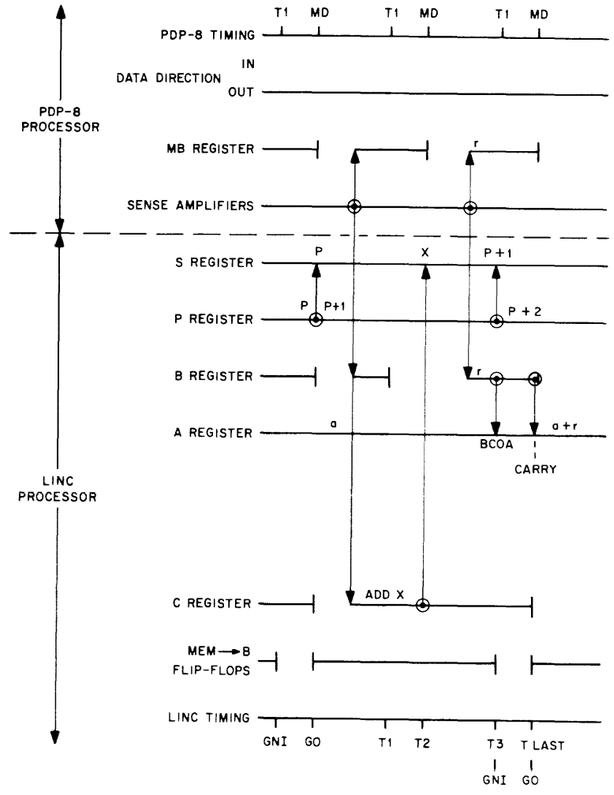
Module Schematics (cont)

ADA $i\beta$

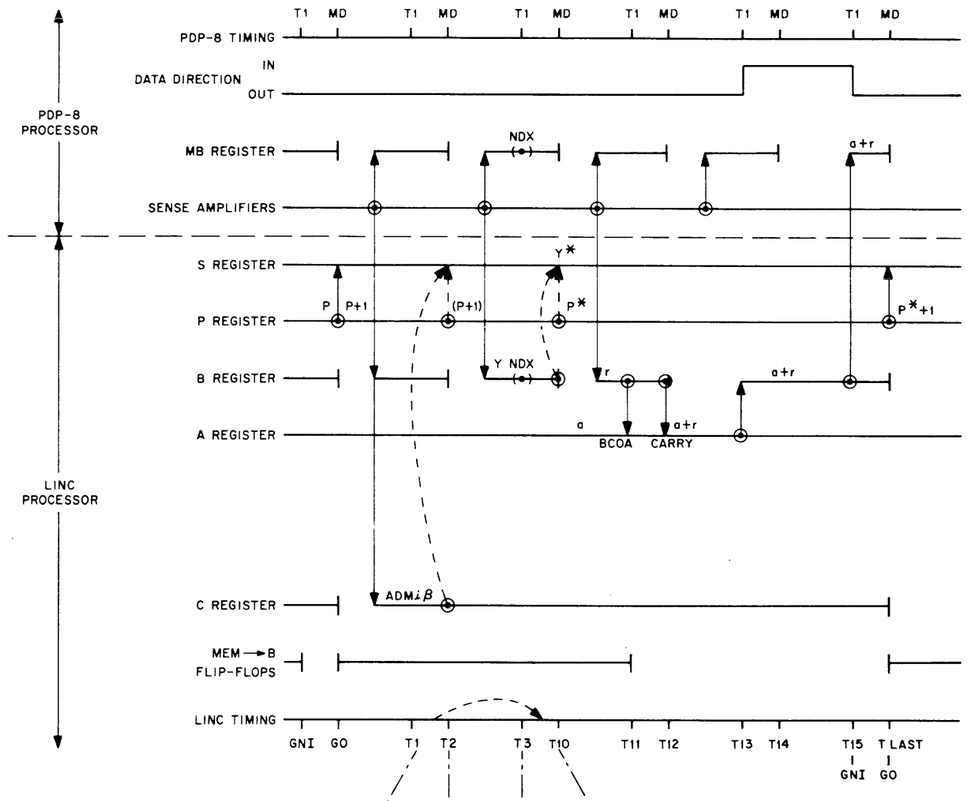


CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

ADD X

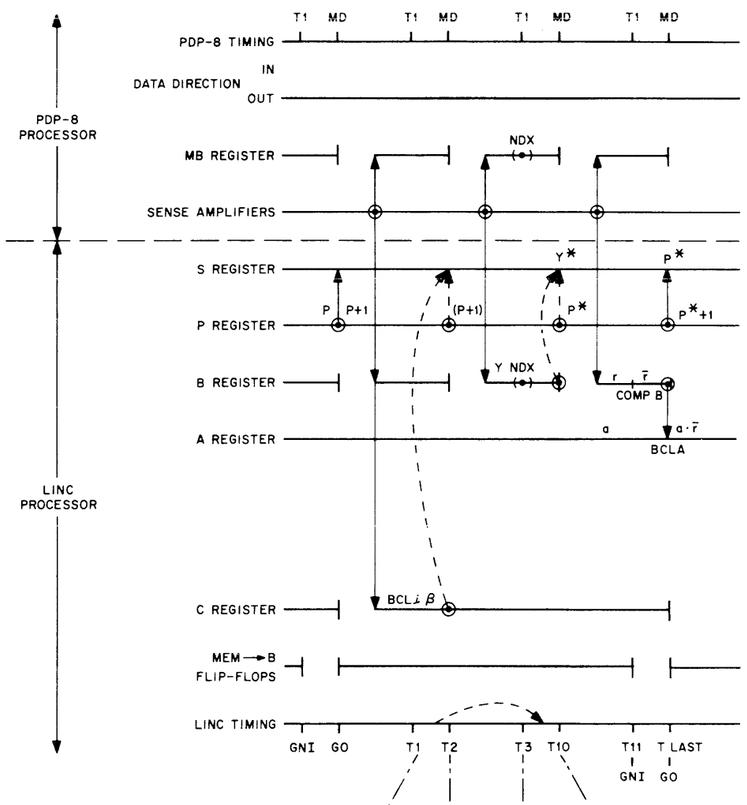


ADM $i\,\beta$



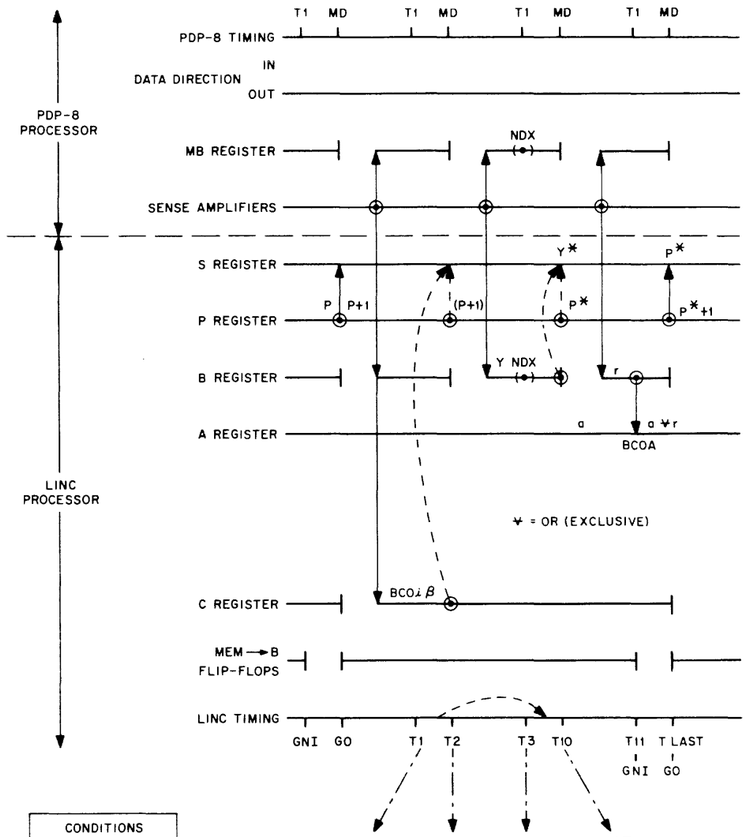
CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

BCL $i\,\beta$



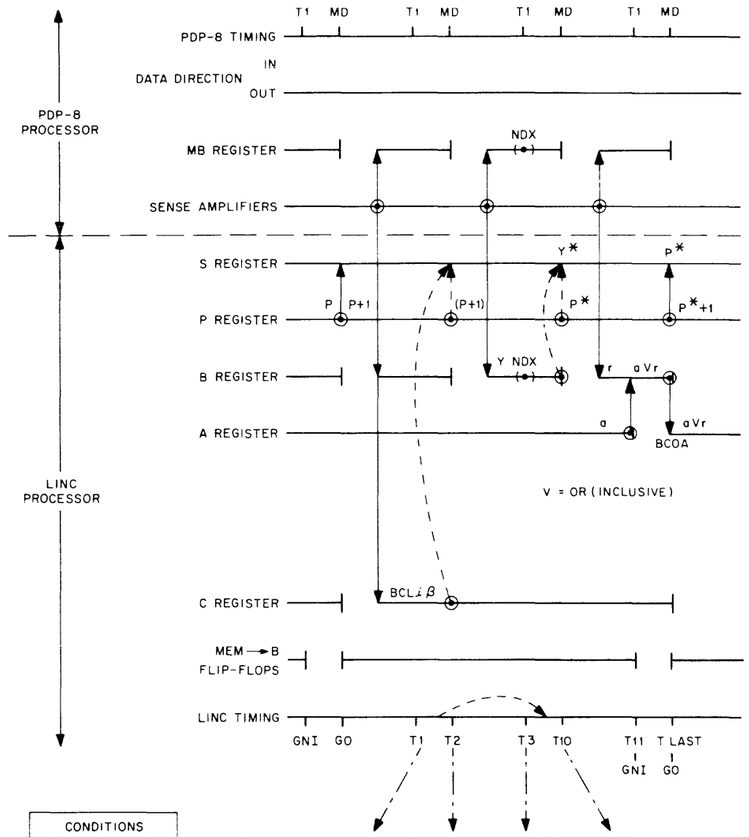
CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

BCO $\iota\beta$



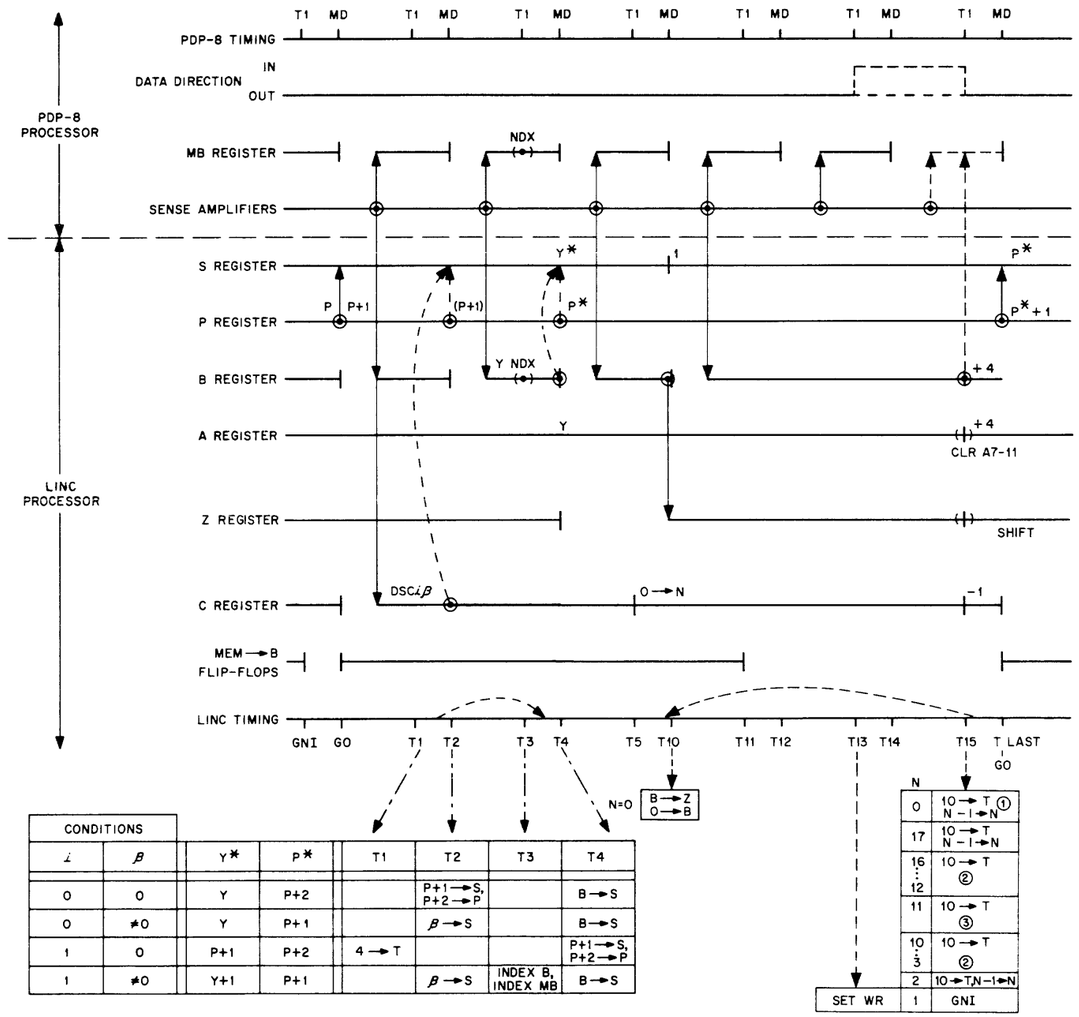
CONDITIONS							
ι	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

BSE $\iota\beta$



CONDITIONS							
ι	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

DSC↓β

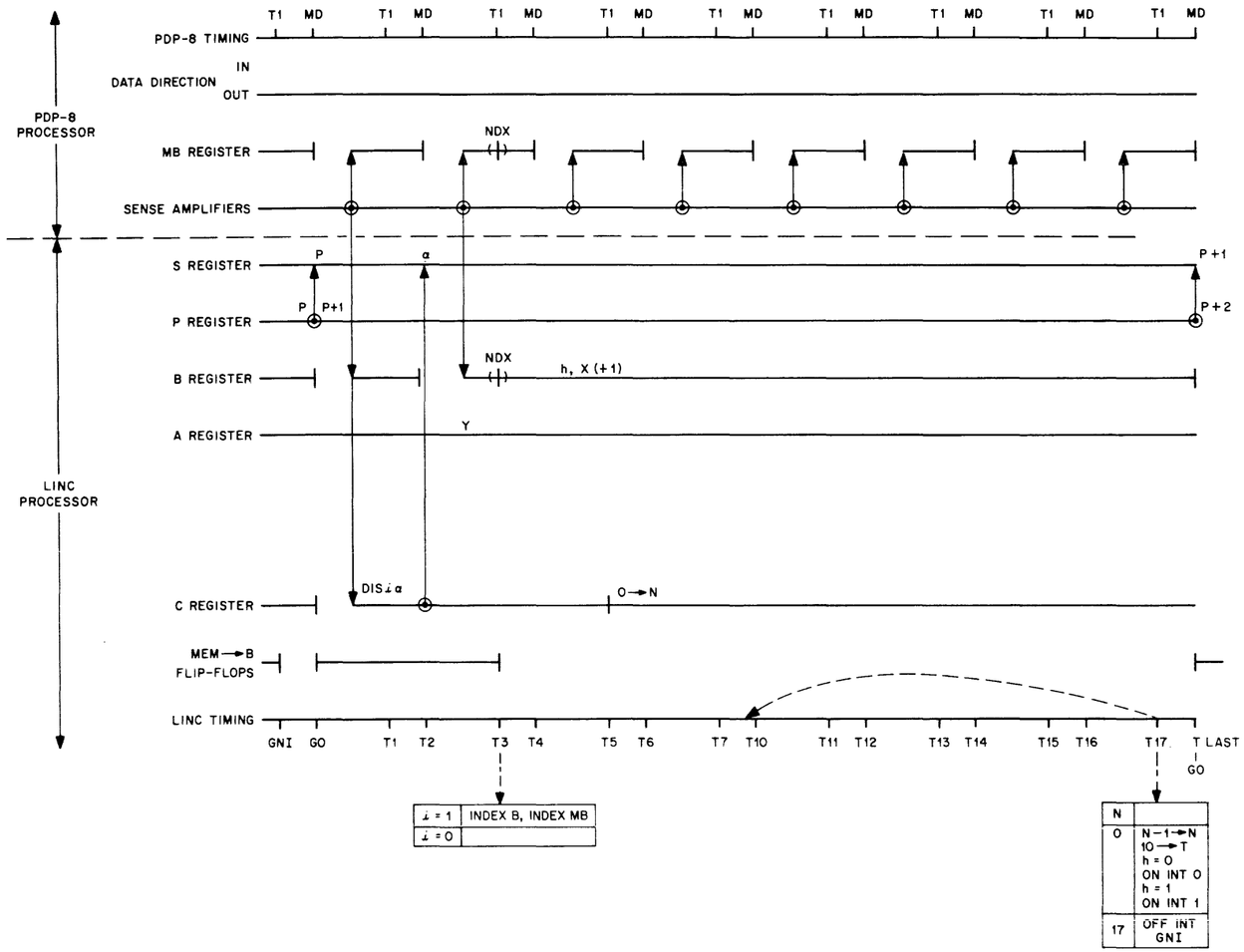


CONDITIONS		Y*	P*	T1	T2	T3	T4
↓	β						
0	0	Y	P+2		P+1→S, P+2→P		B→S
0	≠0	Y	P+1		β→S		B→S
1	0	P+1	P+2	4→T			P+1→S, P+2→P
1	≠0	Y+1	P+1		β→S	INDEX B, INDEX MB	B→S

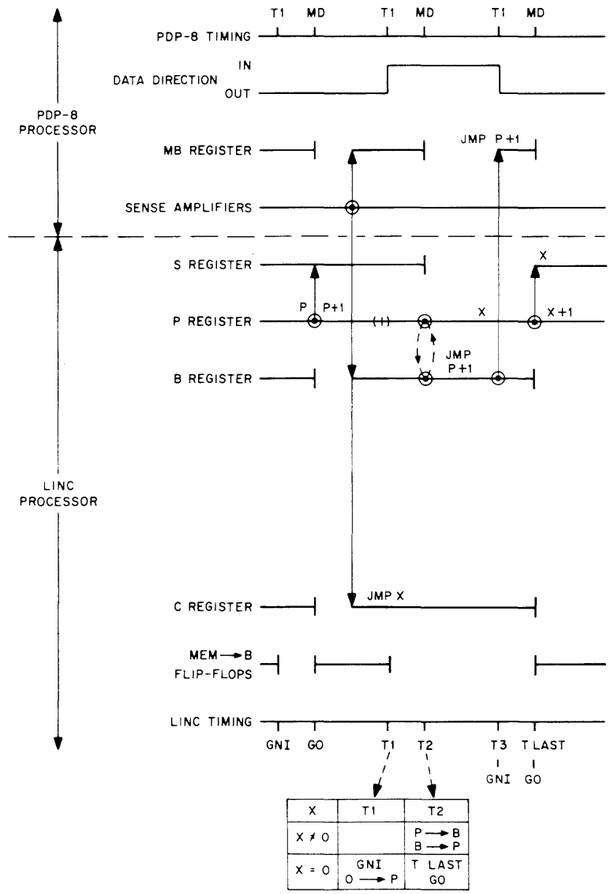
N	
0	10→T ① N−1→N
17	10→T N−1→N
16 ⋮ 12	10→T ②
11	10→T ③
10 ⋮ 3	10→T ②
2	10→T, N−1→N
1	GNI

①	0→A 7-11 B+4→B
②	IF Z11=1, THEN ON INTENSITY, 0→Z11
	IF Z11=0, THEN OFF INTENSITY, A+4→A, N−1→N AND ZSHR
③	IF Z11=1, THEN ON INTENSITY, 0→Z11
	IF Z11=0, THEN 0→A7-11, B+4→B, N−1→N, OFF INTENSITY, AND ZSHR

DIS ↓ α

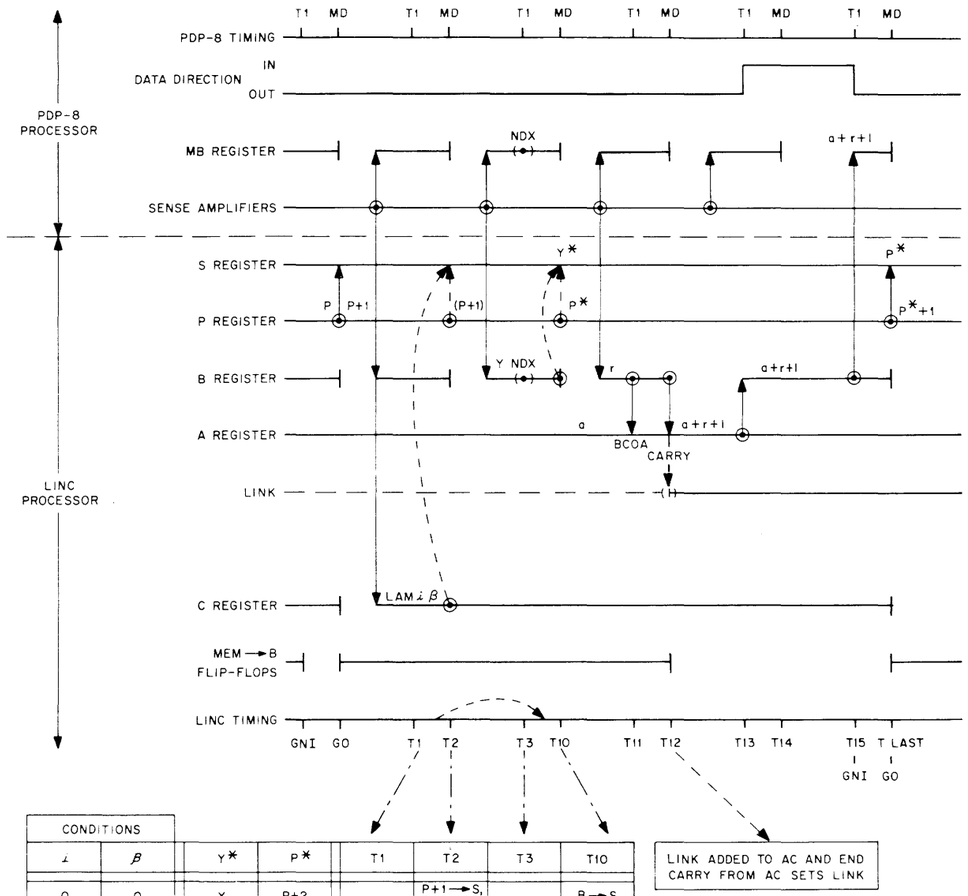

T1 MD
PDP-8 TIMING
DATA DIRECTION
IN
OUT
PDP-8 PROCESSOR
NDX
MB REGISTER
SENSE AMPLIFIERS
S REGISTER
P
α
P+1
P REGISTER
P+2
B REGISTER
h, X (+1)
A REGISTER
Y
LINC PROCESSOR
C REGISTER
DIS ↓ α
0→N
MEM→B FLIP-FLOPS
LINC TIMING
GNI GO T1 T2 T3 T4 T5 T6 T7 T10 T11 T12 T13 T14 T15 T16 T17 T LAST
GO
↓ = 1 INDEX B, INDEX MB
↓ = 0
N
0 N−1→N 10→T h = 0 ON INT 0 h = 1 ON INT 1
17 OFF INT GNI

JMP X



X	T1	T2
X ≠ 0		P → B B → P
X = 0	GNI 0 → P	T LAST GO

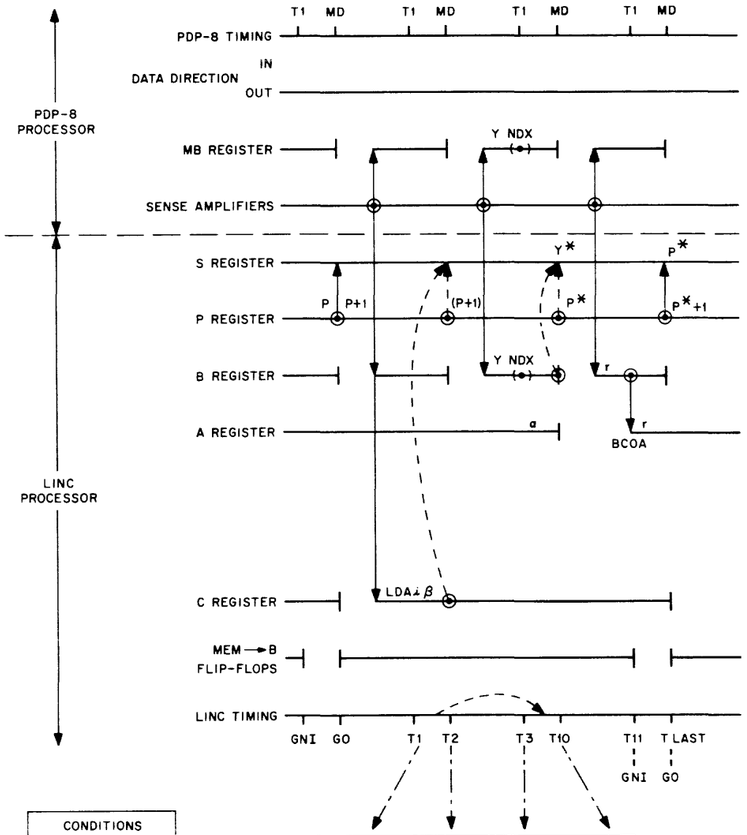
LAM $i\beta$



CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

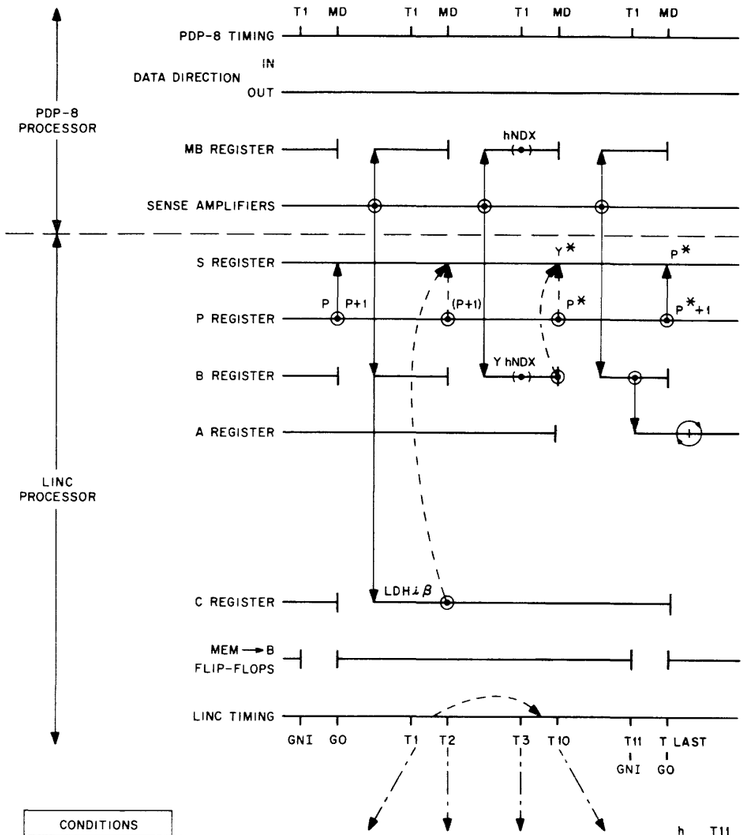
LINK ADDED TO AC AND END CARRY FROM AC SETS LINK

LDA i β



CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

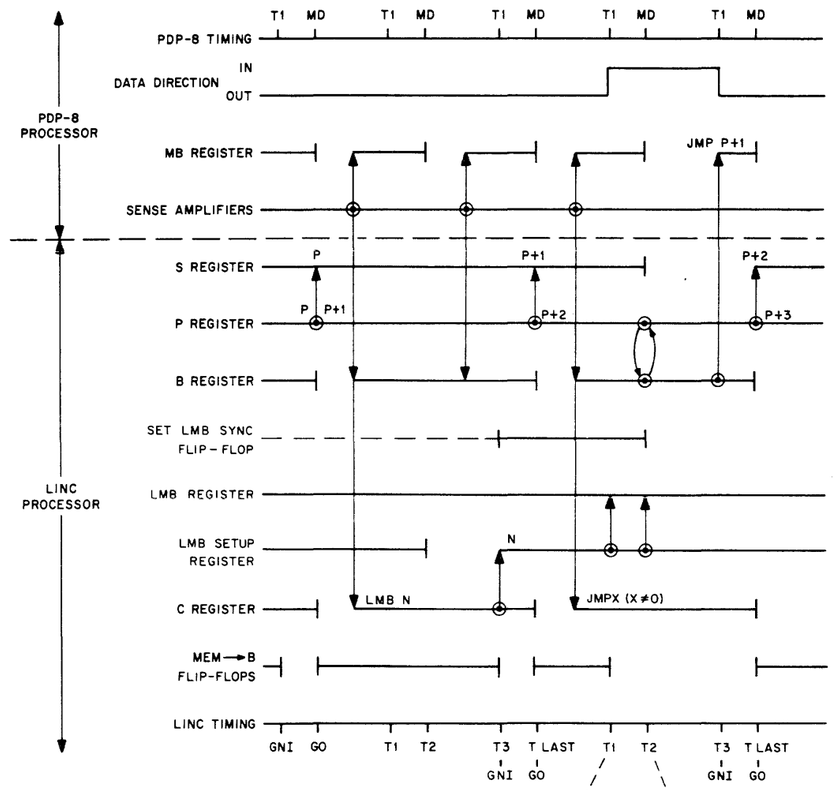
LDH i β



CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	h INDEX B h INDEX MB	B → S

h	T11	T LAST
0	BCOAL	$A_R \rightarrow A_L$
1	BCOAR	

LMB N

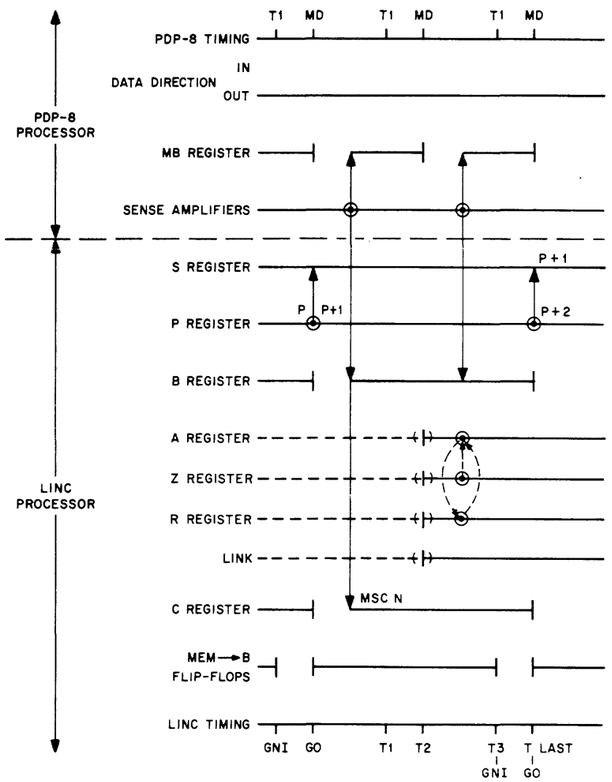


THE JMP INSTRUCTION IS SHOWN BECAUSE COMPLETION OF AN LMB INSTRUCTION COMES DURING THE JMP INSTRUCTION. A JMP MUST OCCUR SOMETIME AFTER, BUT NEED NOT BE THE NEXT INSTRUCTION FOLLOWING AN LMB INSTRUCTION.

CHANGE LMB 0-2

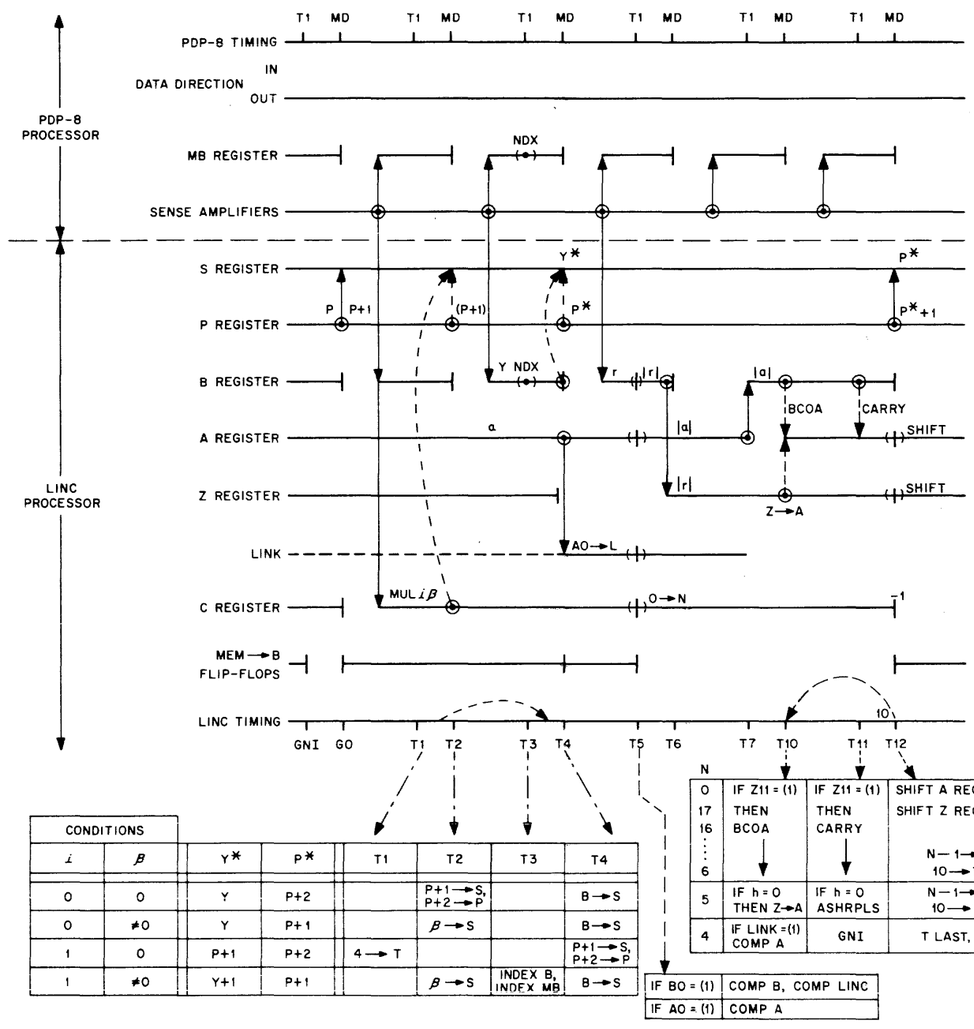
CHANGE LMB 3-4

MSC N



N	MNEM	T2	T3
0	HLT	Ø→RUN INT Ø→AUTO FF	
5	ZTA	Z → A	ASHRPLS
11	CLR	0→A, 0→L	0 → Z
14	ATR	0→R	A → R
15	RTA	0 → A	R → A
16	NOP		
17	COM	$\bar{A}$ → A	

MUL $i\beta$

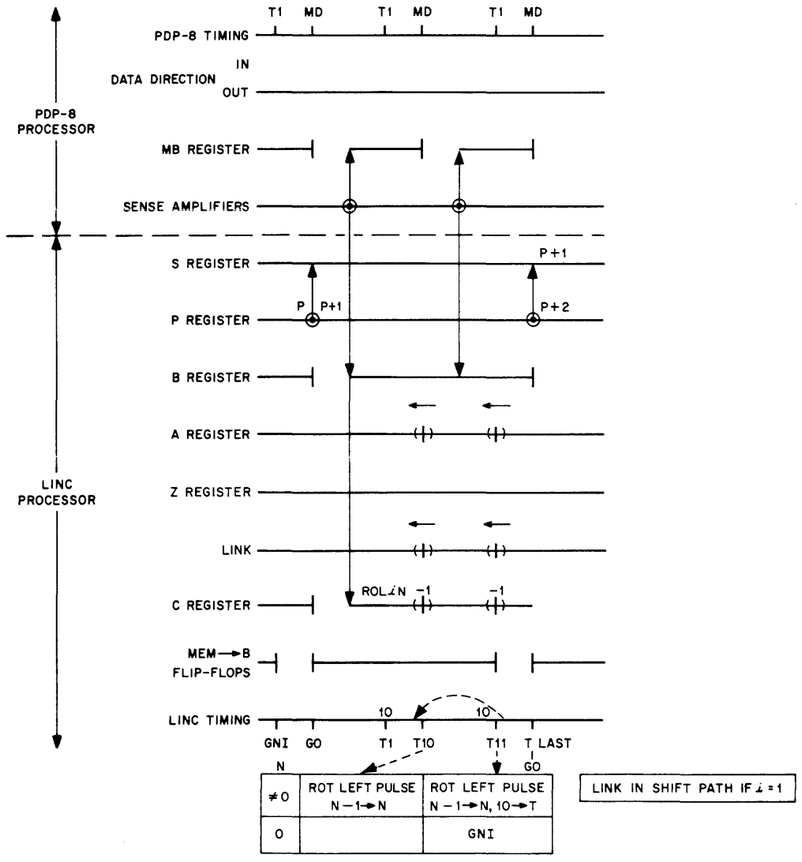


CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T4
0	0	Y	P+2		P+1→S, P+2→P		B→S
0	≠0	Y	P+1		β→S		B→S
1	0	P+1	P+2	4→T			P+1→S, P+2→P
1	≠0	Y+1	P+1		β→S	INDEX B, INDEX MB	B→S

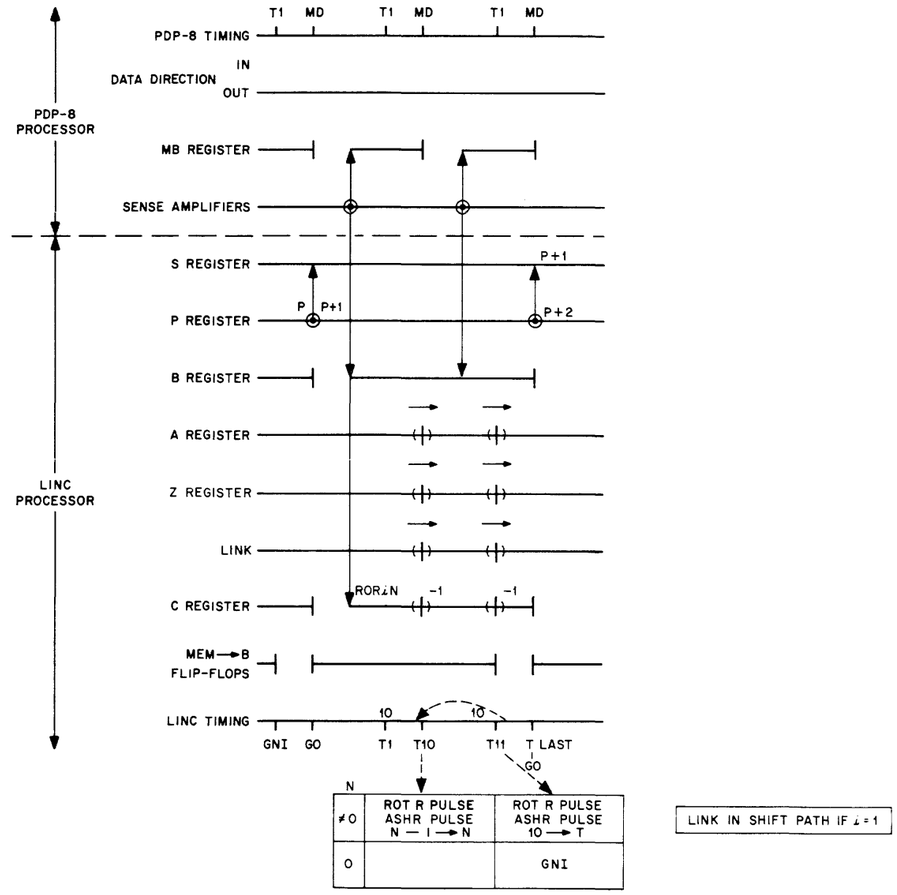
N			
0	IF Z11 = (1)	IF Z11 = (1)	SHIFT A REGISTER
17	THEN	THEN	SHIFT Z REGISTER
16	BCOA	CARRY	N−1→N
⋮	↓	↓	10→T
6			
5	IF h = 0 THEN Z→A	IF h = 0 ASHRPLS	N−1→N 10→T
4	IF LINK = (1) COMP A	GNI	T LAST, GO

IF BO = (1)	COMP B, COMP LINC
IF AO = (1)	COMP A

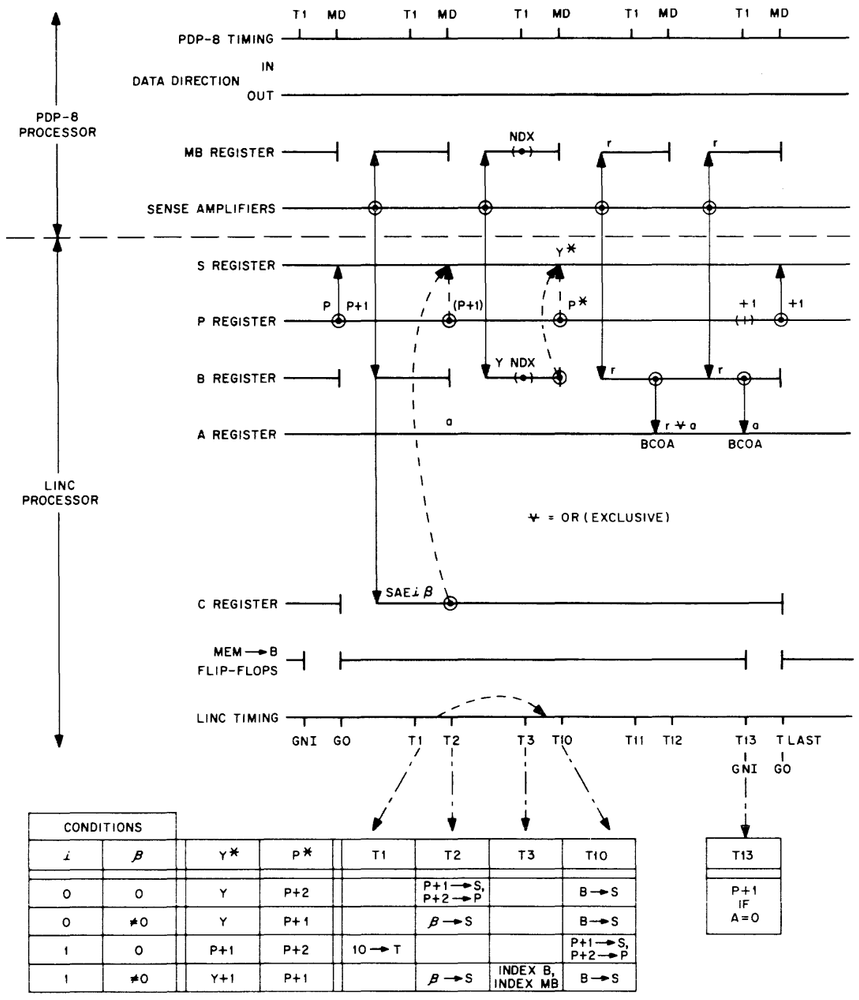
ROL ∠ N


T1 MD T1 MD T1 MD
PDP-8 TIMING
DATA DIRECTION
IN
OUT
PDP-8 PROCESSOR
MB REGISTER
SENSE AMPLIFIERS
S REGISTER
P+1
P REGISTER
P P+1
P+2
B REGISTER
A REGISTER
LINC PROCESSOR
Z REGISTER
LINK
C REGISTER
ROL∠N -1 -1
MEM→B FLIP-FLOPS
LINC TIMING
10 10
GNI GO T1 T10 T11 T LAST
GO
N
≠0
ROT LEFT PULSE N−1→N
ROT LEFT PULSE N−1→N, 10→T
0
GNI
LINK IN SHIFT PATH IF ∠=1

ROR ∠ N


T1 MD T1 MD T1 MD
PDP-8 TIMING
DATA DIRECTION
IN
OUT
PDP-8 PROCESSOR
MB REGISTER
SENSE AMPLIFIERS
S REGISTER
P+1
P REGISTER
P P+1
P+2
B REGISTER
A REGISTER
LINC PROCESSOR
Z REGISTER
LINK
C REGISTER
ROR∠N -1 -1
MEM→B FLIP-FLOPS
LINC TIMING
10 10
GNI GO T1 T10 T11 T LAST
GO
N
≠0
ROT R PULSE ASHR PULSE N − 1 → N
ROT R PULSE ASHR PULSE 10 → T
0
GNI
LINK IN SHIFT PATH IF ∠=1

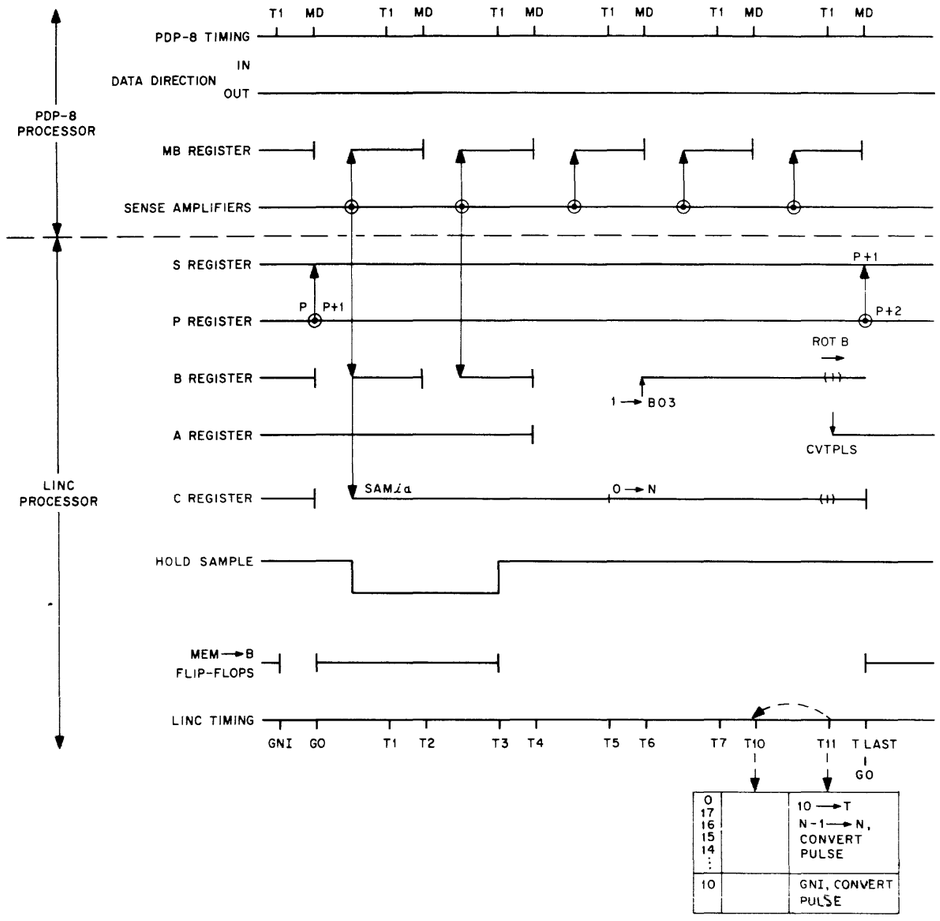
SAE i β



CONDITIONS							
i	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

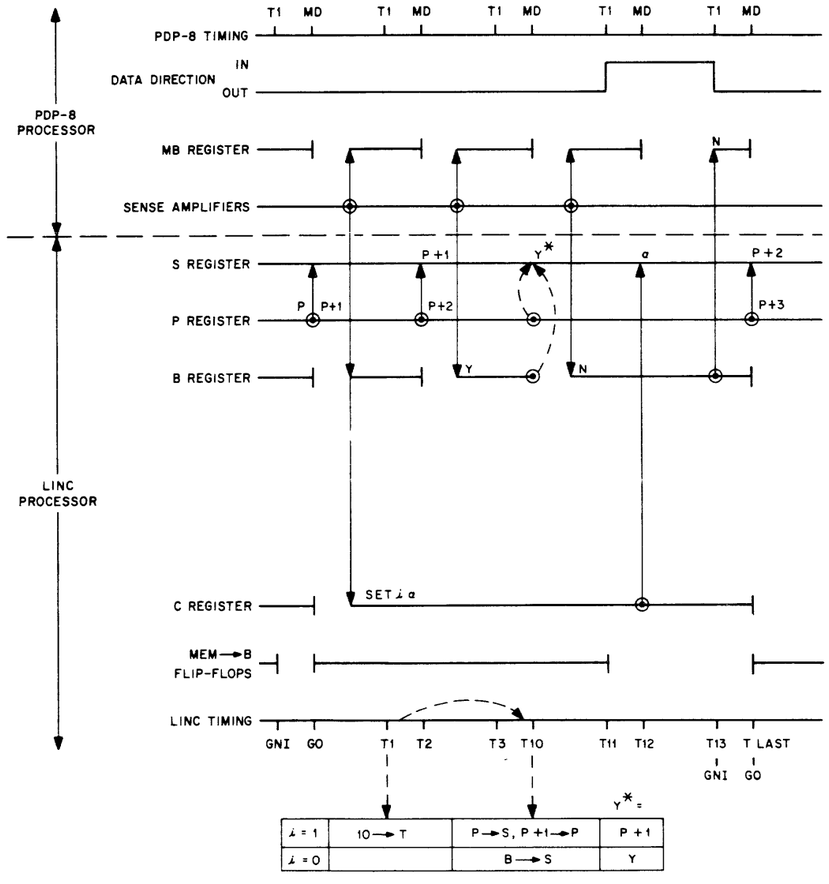
T13
P+1 IF A=0

SAM i a

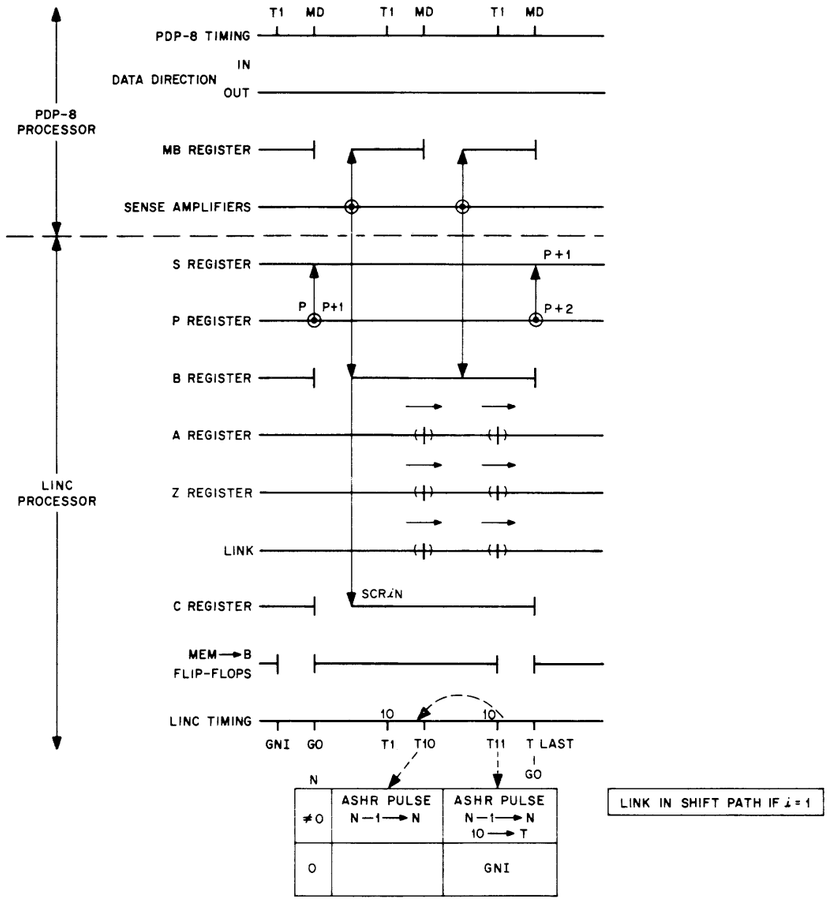


0 17 16 15 14 ⋮		10 → T N-1 → N, CONVERT PULSE
10		GNI, CONVERT PULSE

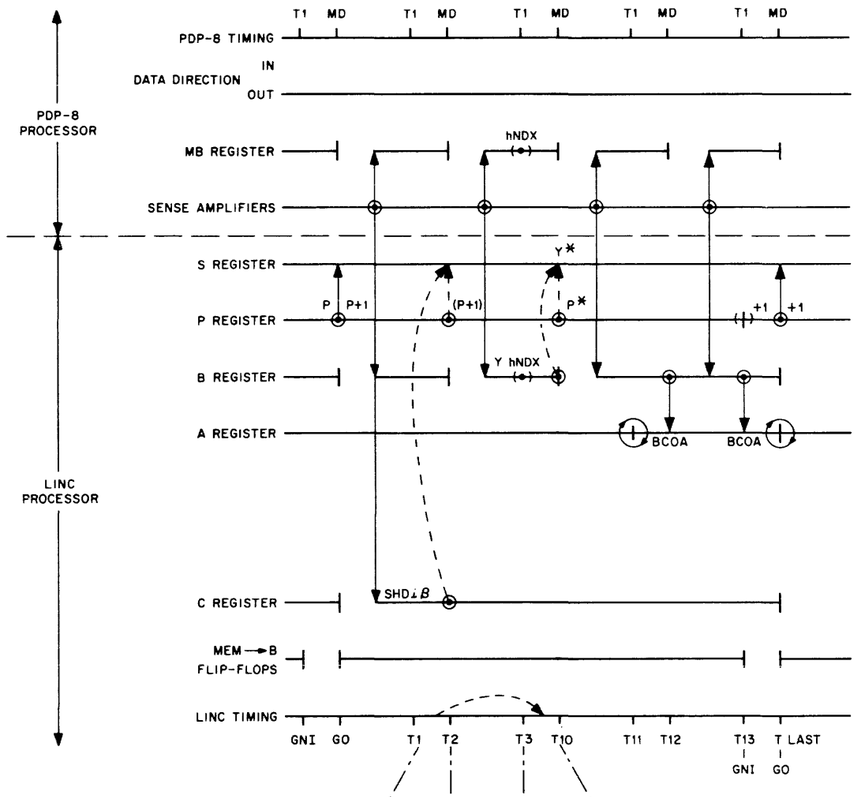
SET ⌟ α


PDP-8 PROCESSOR
LINC PROCESSOR
T1 MD T1 MD T1 MD T1 MD T1 MD
PDP-8 TIMING
DATA DIRECTION
IN
OUT
MB REGISTER
SENSE AMPLIFIERS
S REGISTER
P REGISTER
B REGISTER
C REGISTER
MEM → B FLIP-FLOPS
LINC TIMING
P
P+1
P+2
P+3
Y*
Y
N
α
SET ⌟ α
GNI GO T1 T2 T3 T10 T11 T12 T13 T LAST
GNI GO
Y* =
⌟ = 1 | 10 → T | P → S, P+1 → P | P+1
⌟ = 0 | | B → S | Y

SCR ⌟ N


PDP-8 PROCESSOR
LINC PROCESSOR
T1 MD T1 MD T1 MD
PDP-8 TIMING
DATA DIRECTION
IN
OUT
MB REGISTER
SENSE AMPLIFIERS
S REGISTER
P REGISTER
B REGISTER
A REGISTER
Z REGISTER
LINK
C REGISTER
MEM → B FLIP-FLOPS
LINC TIMING
P
P+1
P+2
SCR ⌟ N
10
GNI GO T1 T10 T11 T LAST
GO
N
≠0 | ASHR PULSE N−1 → N | ASHR PULSE N−1 → N, 10 → T
0 | | GNI
LINK IN SHIFT PATH IF ⌟ = 1

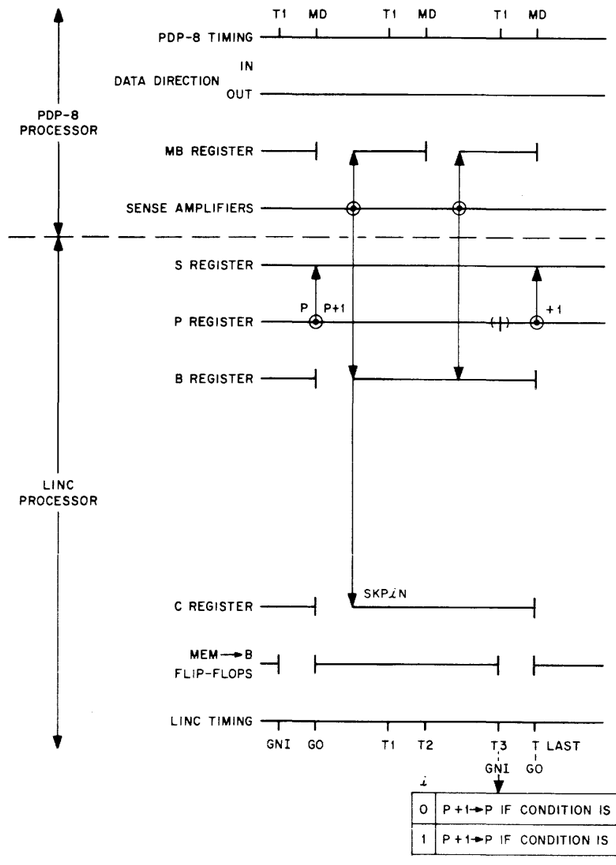
SHD ∠ β



CONDITIONS							
∠	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	h INDEX B h INDEX MB	B → S

h	T12	T13	T LAST
0	AR ⇄ AL	AL ≠ 0 P+1 → P	AR ⇄ AL
1		AR ≠ 0 P+1 → P	

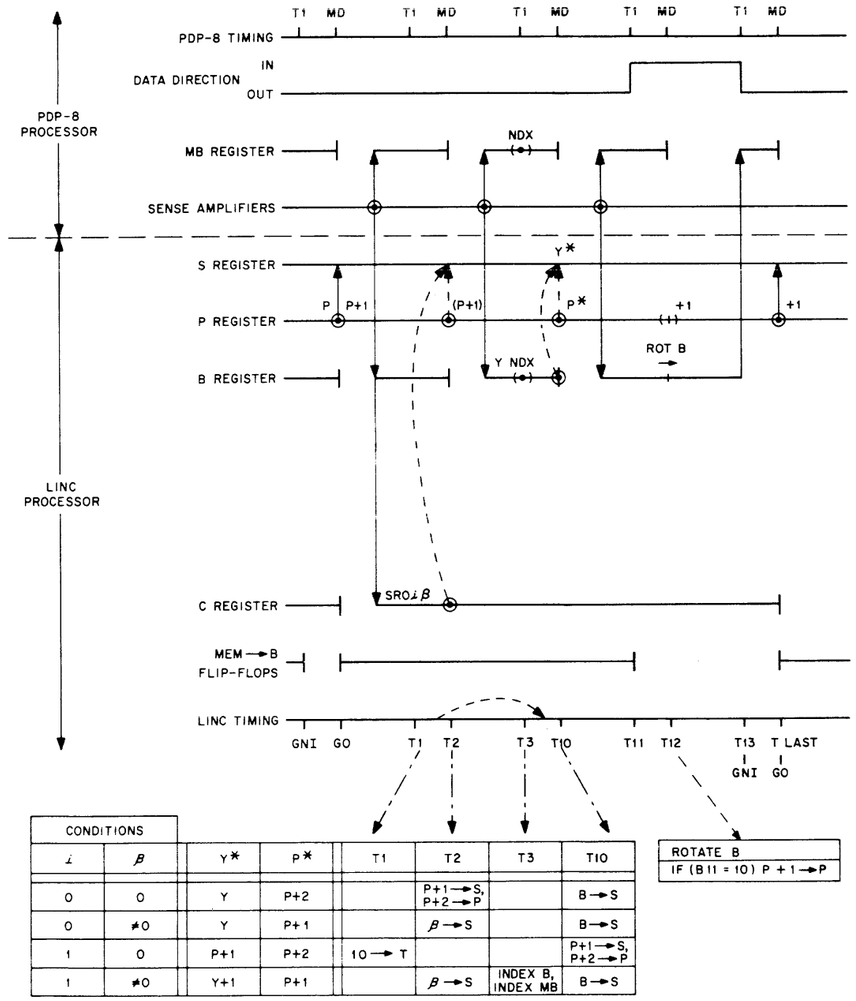
SKP ∠ N



N	CONDITION	MNEM
0	SS 0 = (1)	
1	SS 1 = (1)	
2	SS 2 = (1)	
3	SS 3 = (1)	
4	SS 4 = (1)	
5	SS 5 = (1)	
6		
7		
10	|A| = 0	AZE
11	AO = (0)	APO
12	LINK (0)	LZE
13	1 B MARK	IBZ
14	FLO (1)	FLO
15	Z11 = (0)	ZZZ
16		
17		

∠	
0	P+1 → P IF CONDITION IS TRUE
1	P+1 → P IF CONDITION IS NOT TRUE

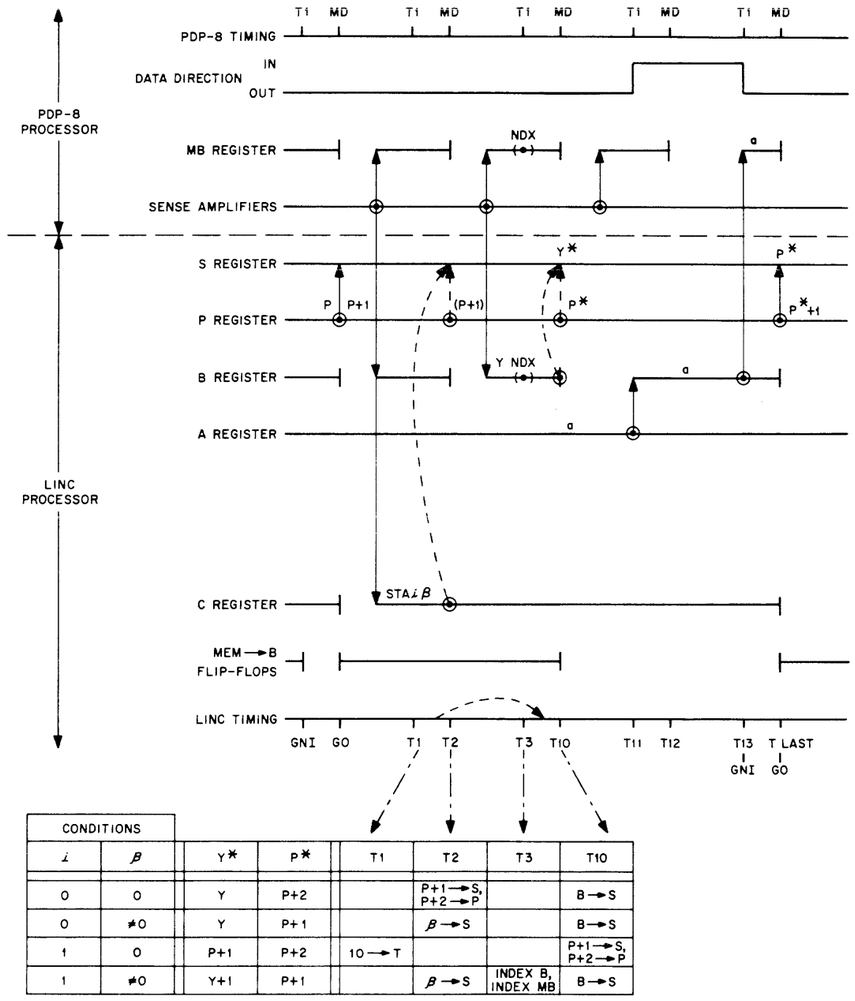
SRO $\angle\beta$



CONDITIONS							
$\angle$	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

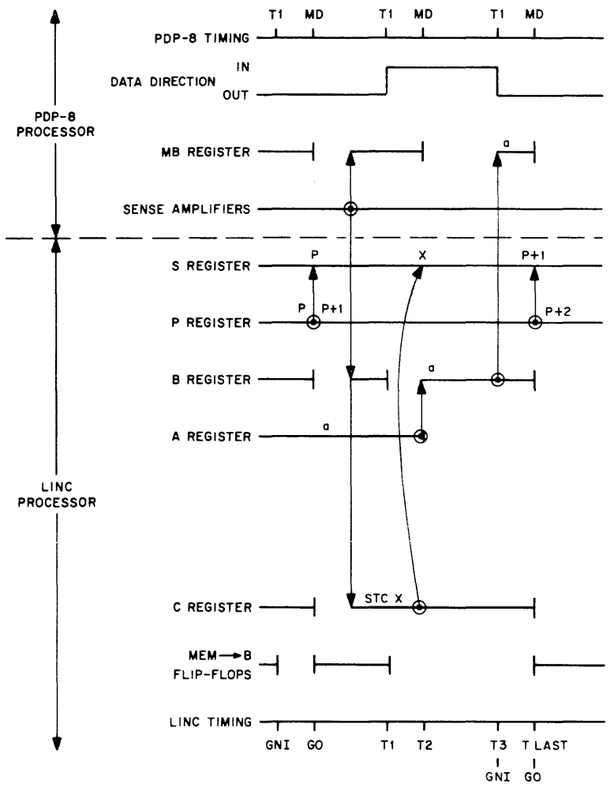
ROTATE B
IF (B11 = 10) P + 1 → P

STA $\angle\beta$

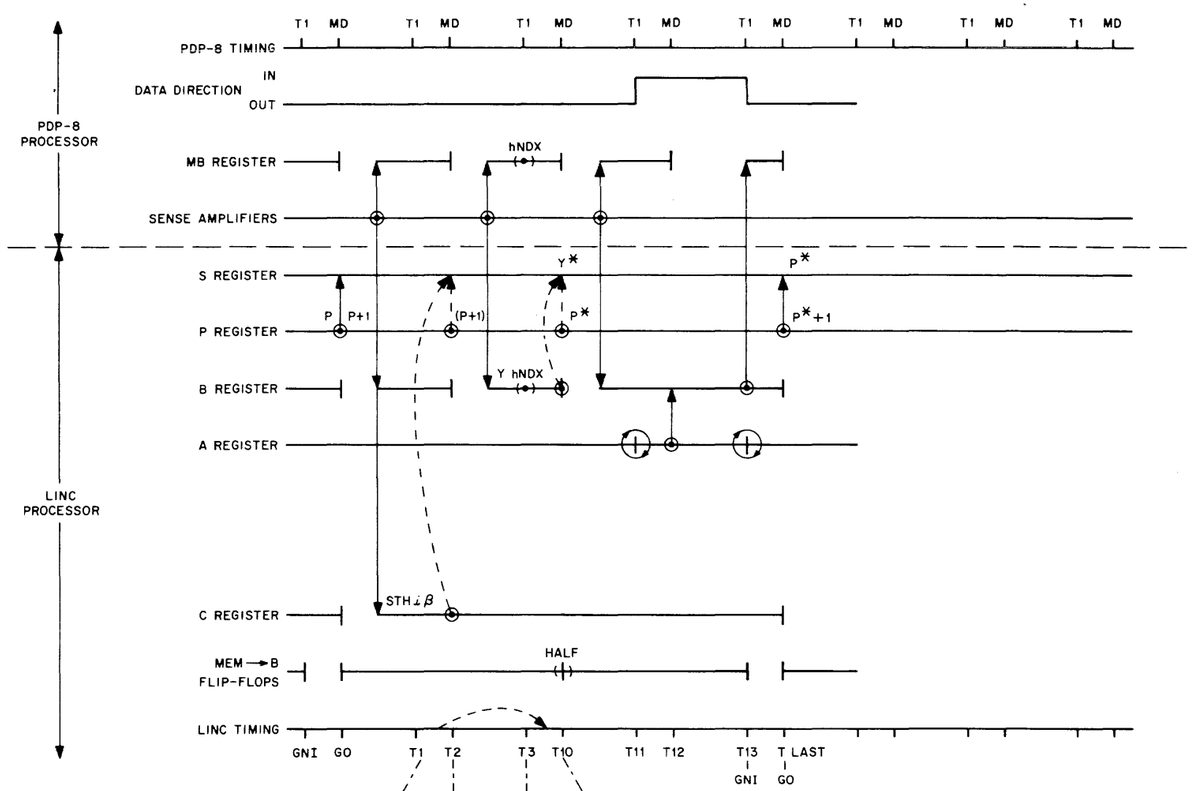


CONDITIONS							
$\angle$	β	Y*	P*	T1	T2	T3	T10
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	INDEX B, INDEX MB	B → S

STC X



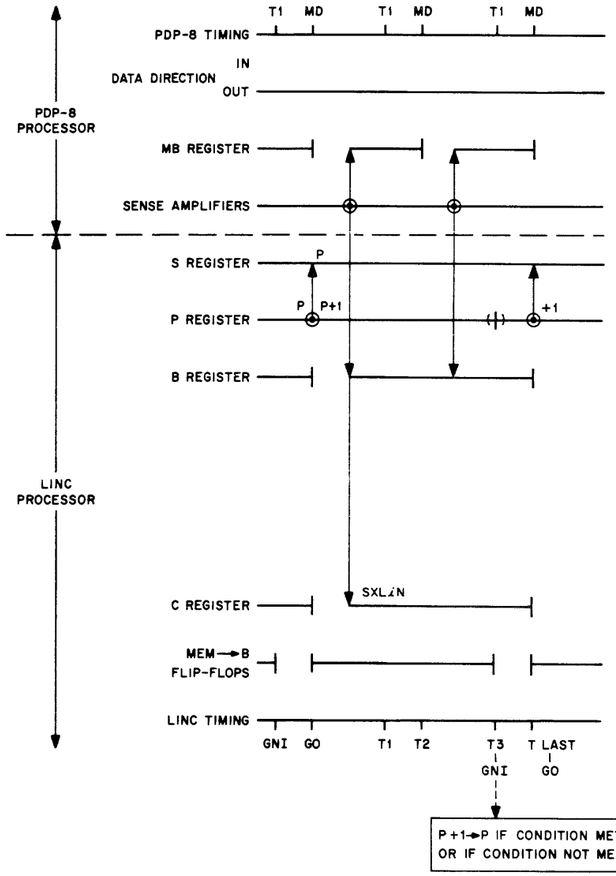
STH i β



CONDITIONS							
i	β	Y*	P*	T1	T2	T3	
0	0	Y	P+2		P+1 → S, P+2 → P		B → S
0	≠0	Y	P+1		β → S		B → S
1	0	P+1	P+2	10 → T			P+1 → S, P+2 → P
1	≠0	Y+1	P+1		β → S	h INDEX B h INDEX MB	B → S

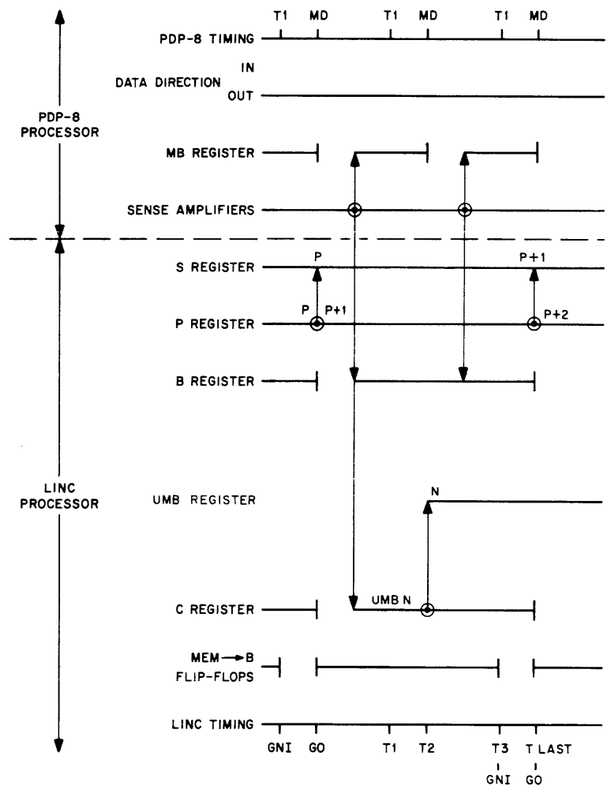
h	T10	T11	T12	T13
0	OFF MEMORY LEFT HALF	AR → AL	AL → BL	AR → AL
1	OFF MEMORY RIGHT HALF		AR → BR	

SXL i N

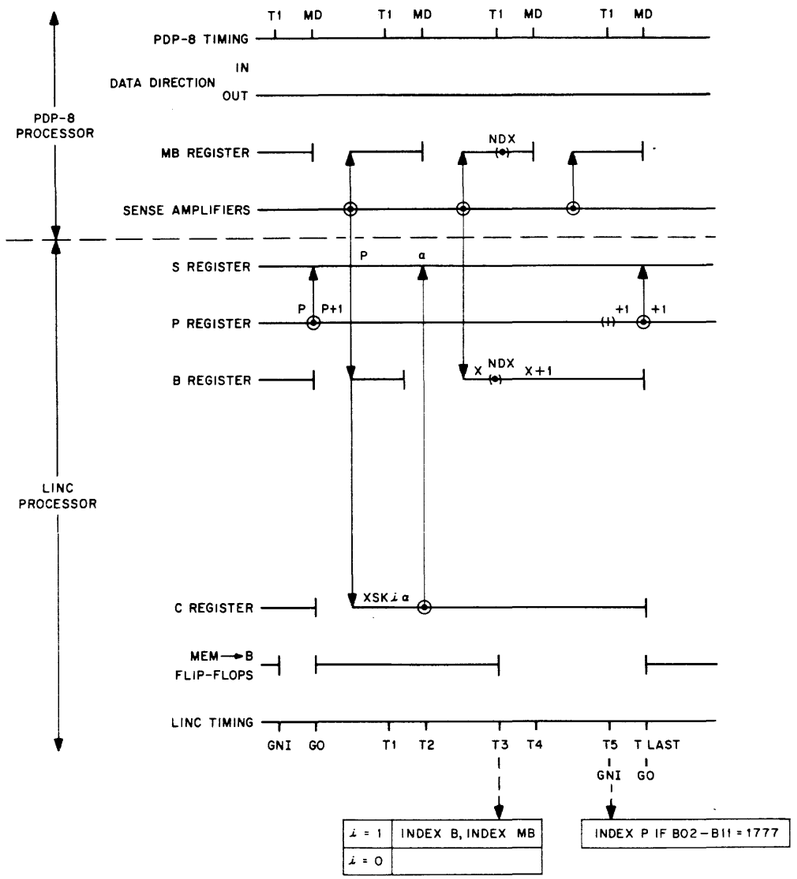


N	CONDITION	MNEN
0	XL0	
1	XL1	
2	XL2	
3	XL3	
4	XL4	
5	XL5	
6	XL6	
7	XL7	
10	XL10	
11	XL11	
12	XL12	
13	XL13	
14		
15	KST (1)	KST
16		
17		

UMB N

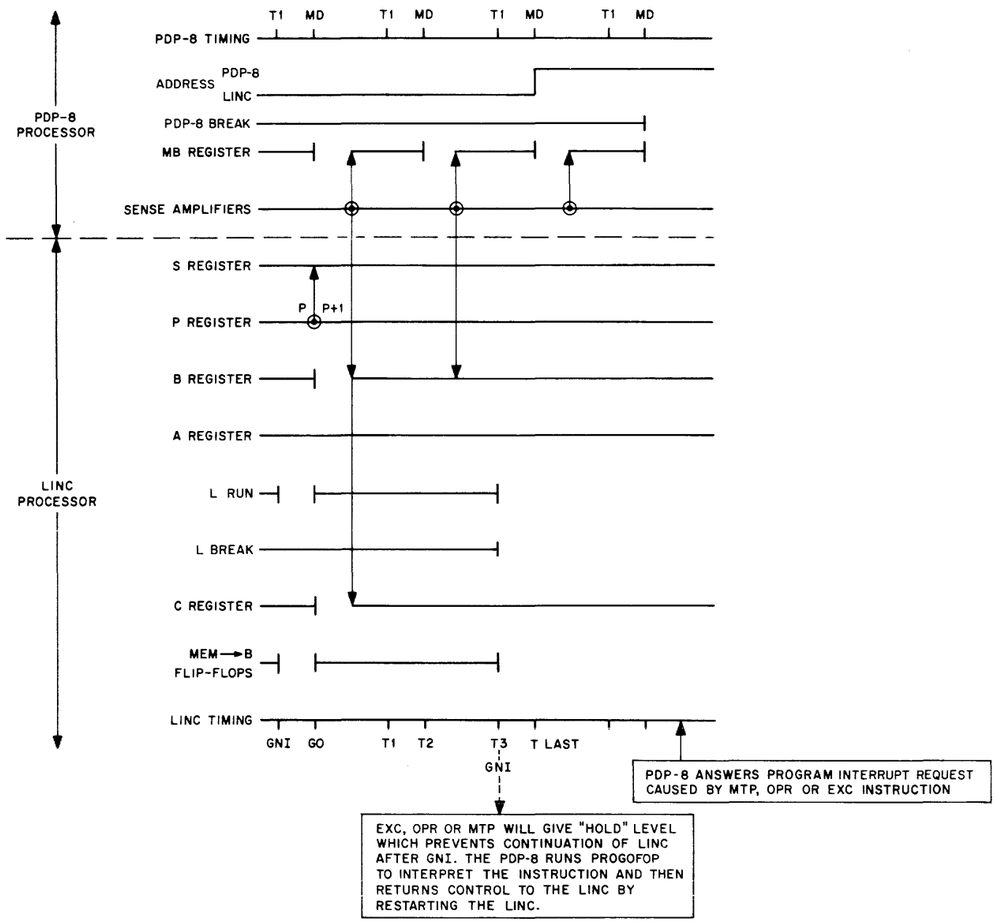


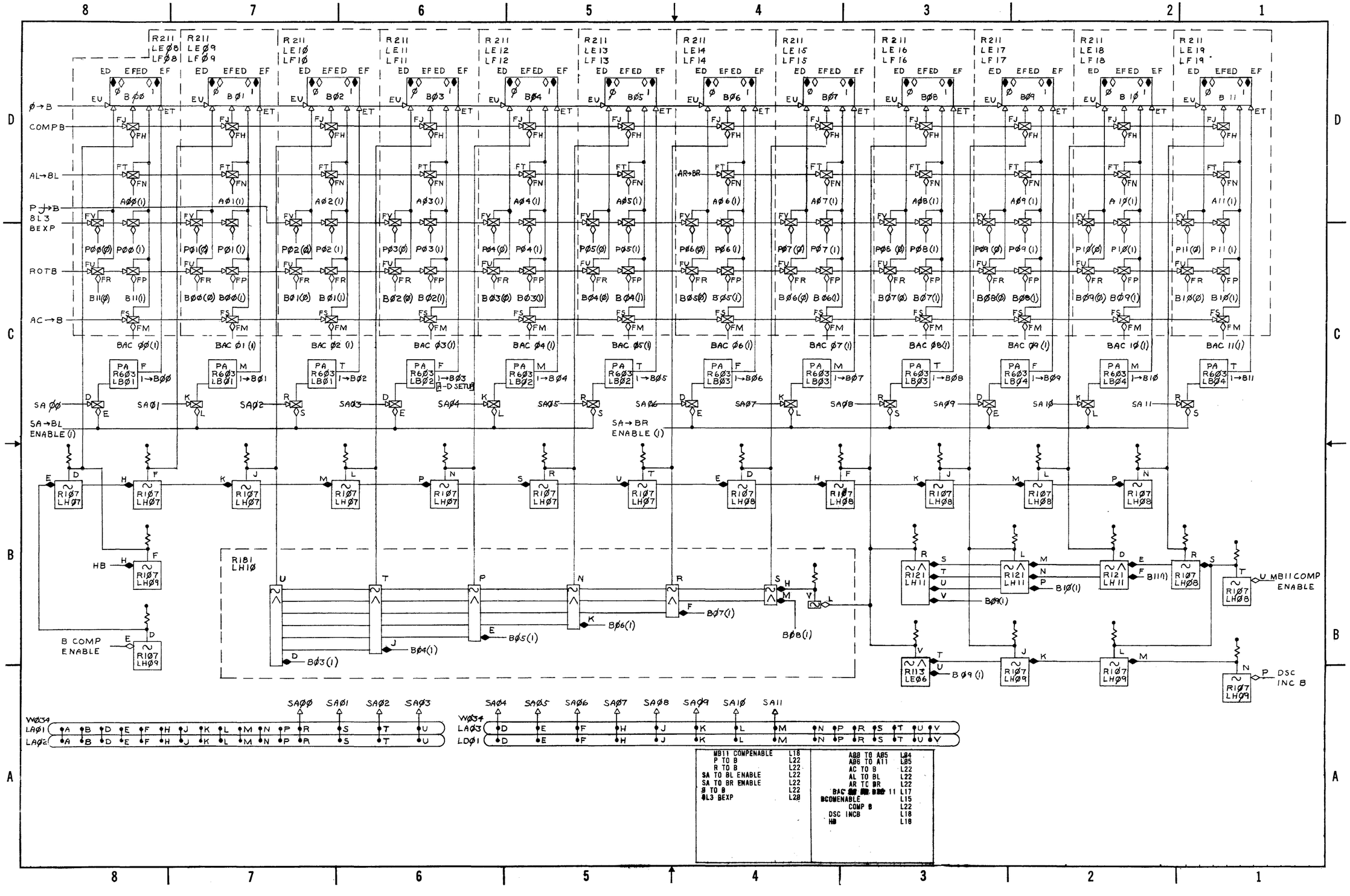
XSK𝑖α



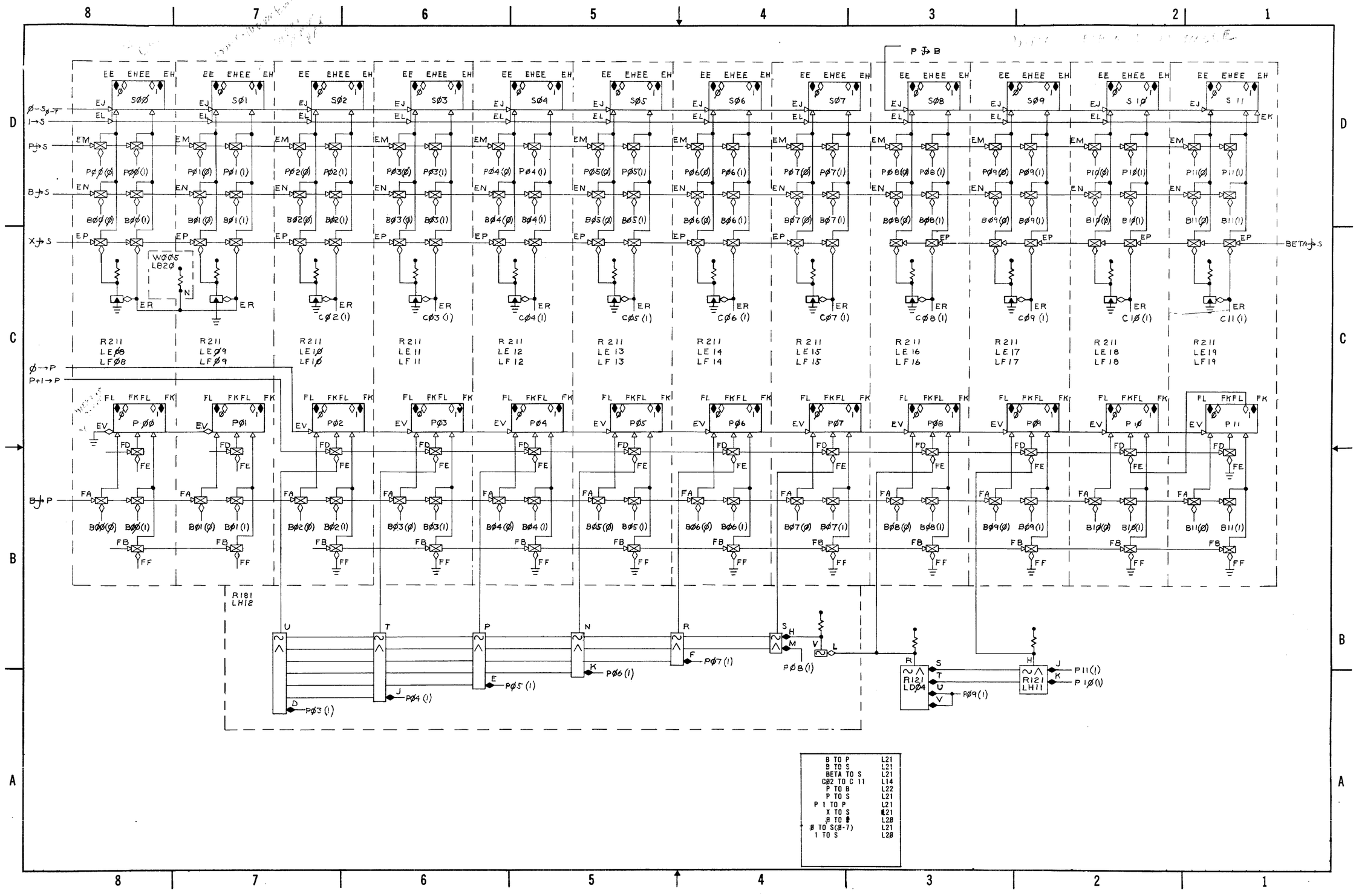
8 EXECUTE CLASS

MTP
OPR
EXC

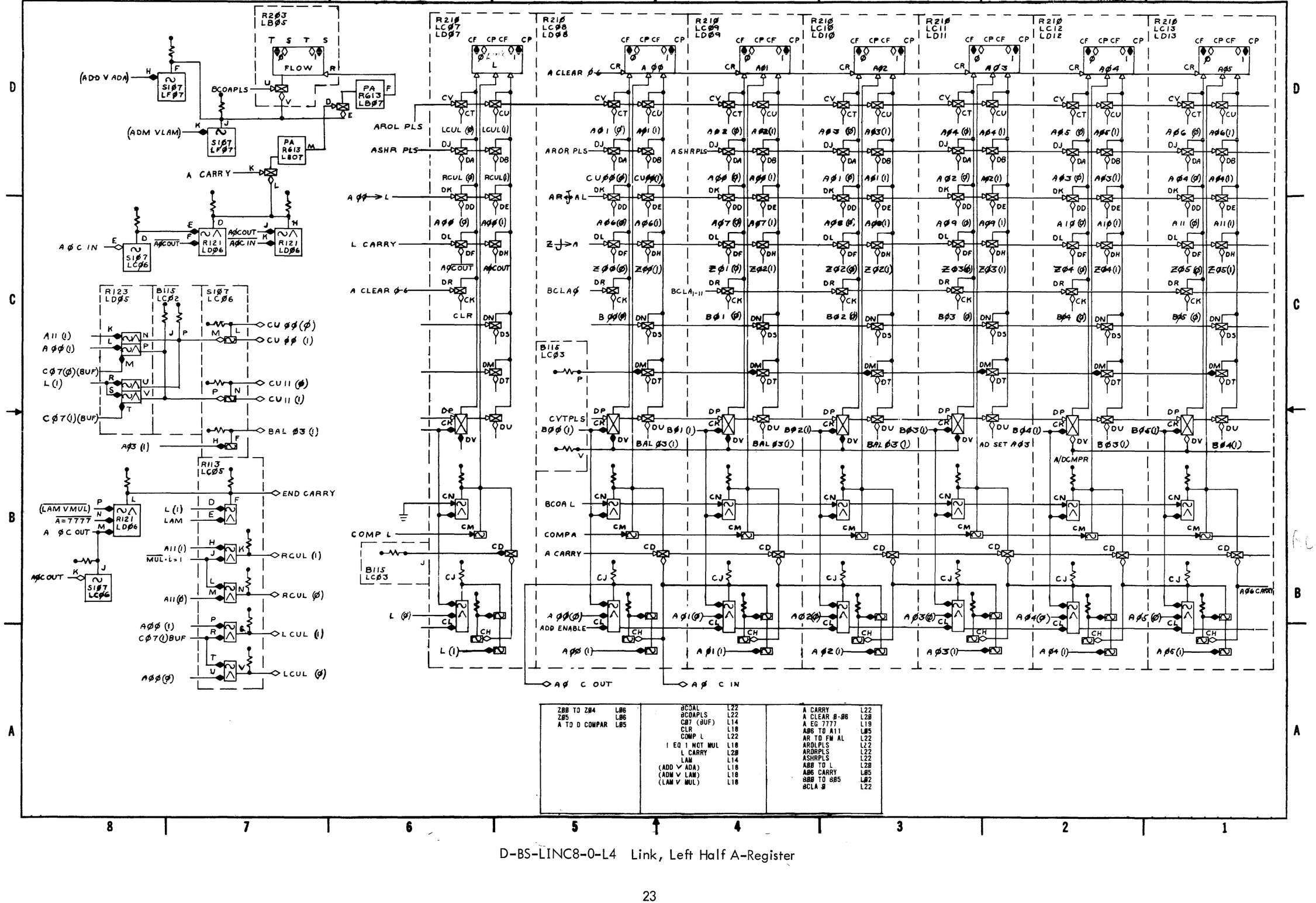




D-BS-LINC8-0-L2 B-Register

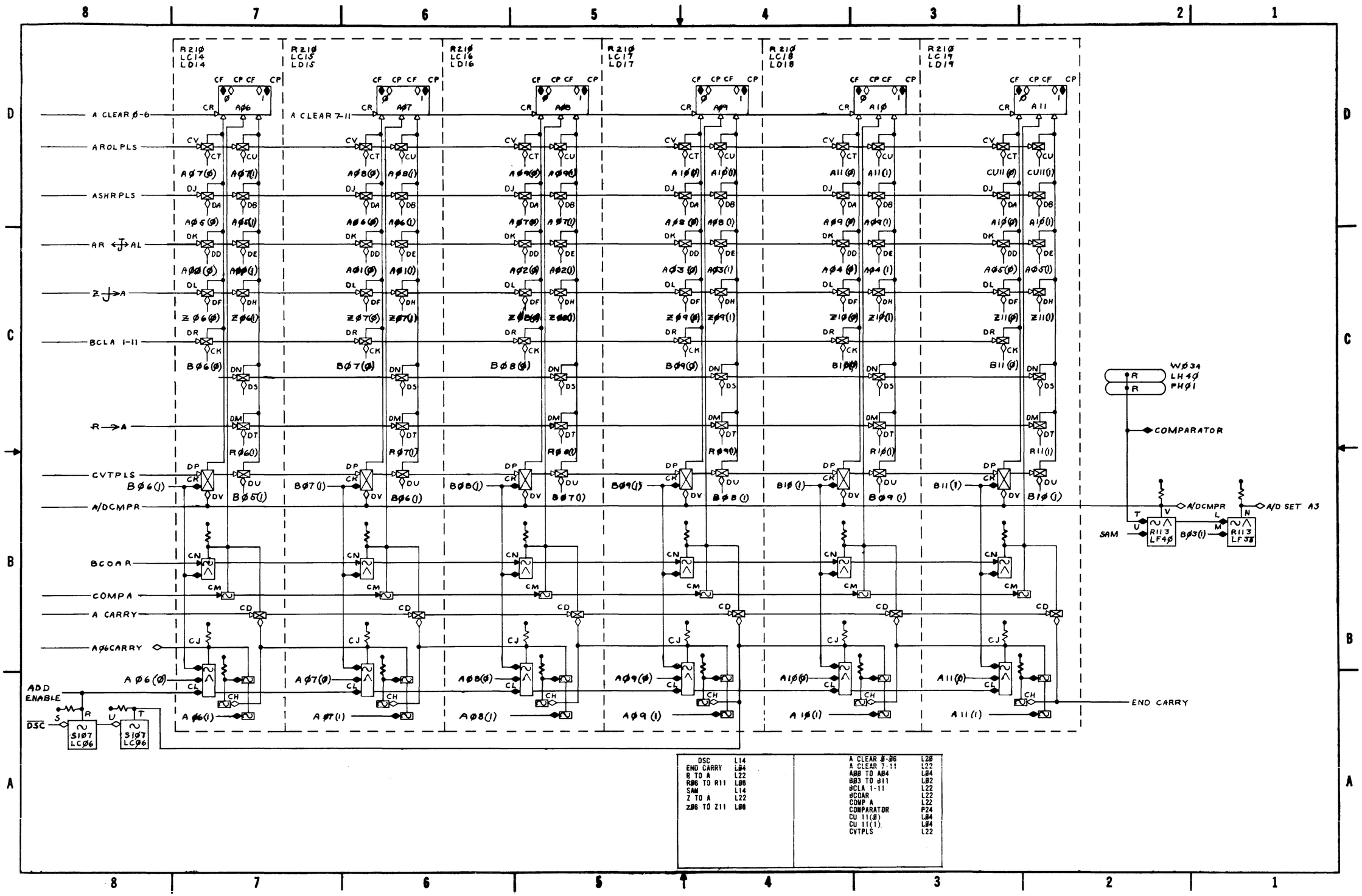


D-BS-LINC8-0-L3 S and P Registers



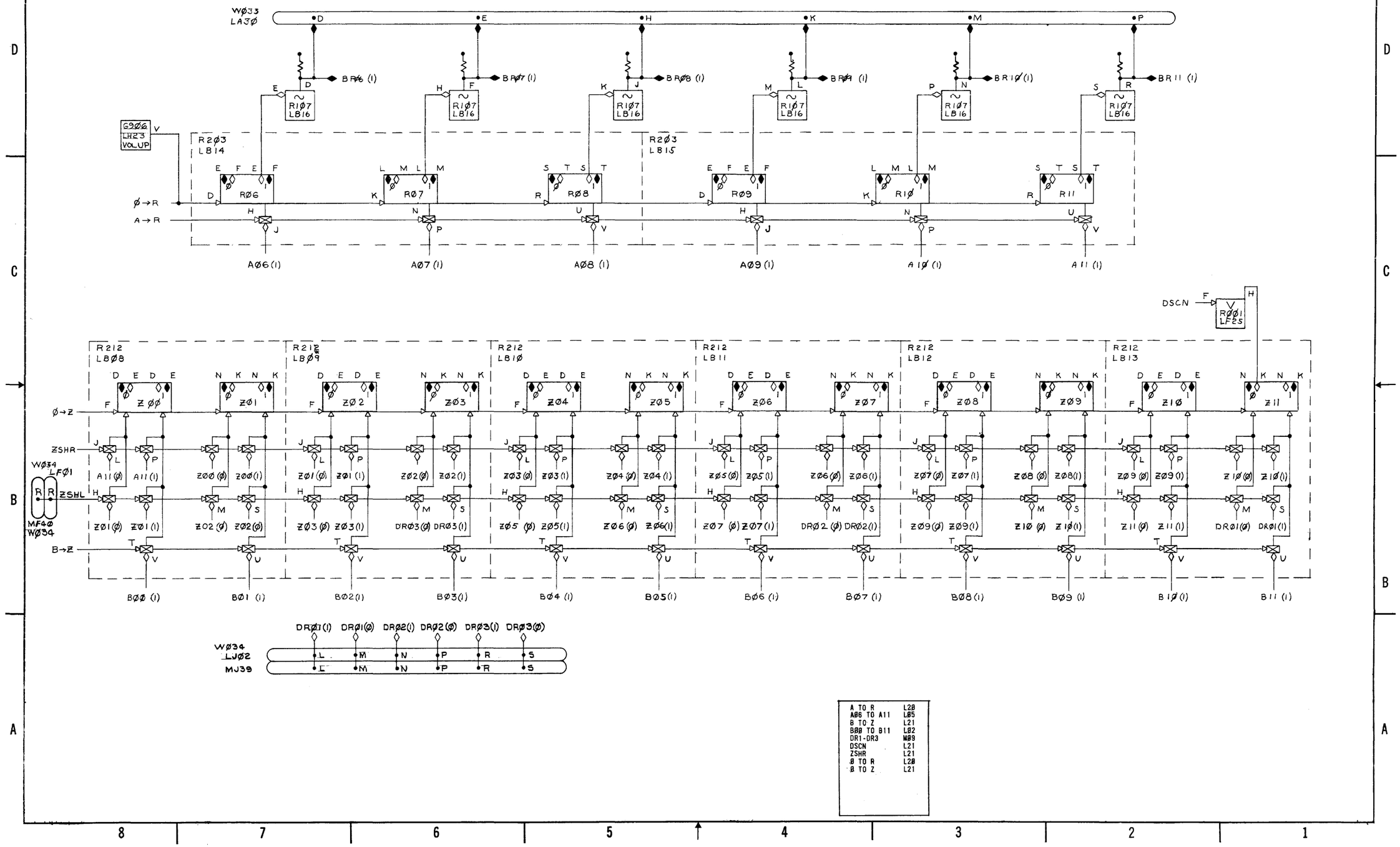
Z88 TO Z84 L86	BCOAL L22	A CARRY L22
Z85 L86	BCOAPLS L22	A CLEAR Ø-86 L28
A TO D COMPAR L85	CØ7 (BUF) L14	A EG 7777 L19
	CLR L18	A86 TO A11 L85
	COMP L L22	AR TO FM AL L22
	I EQ 1 NOT MUL L18	ARDLPLS L22
	L CARRY L28	ARDRPLS L22
	LAM L14	ASHRPLS L22
	(ADD V ADA) L18	A88 TO L L28
	(ADM V LAM) L18	A86 CARRY L85
	(LAM V MUL) L18	B88 TO B85 L02
		BCLA Ø L22

D-BS-LINC8-0-L4 Link, Left Half A-Register

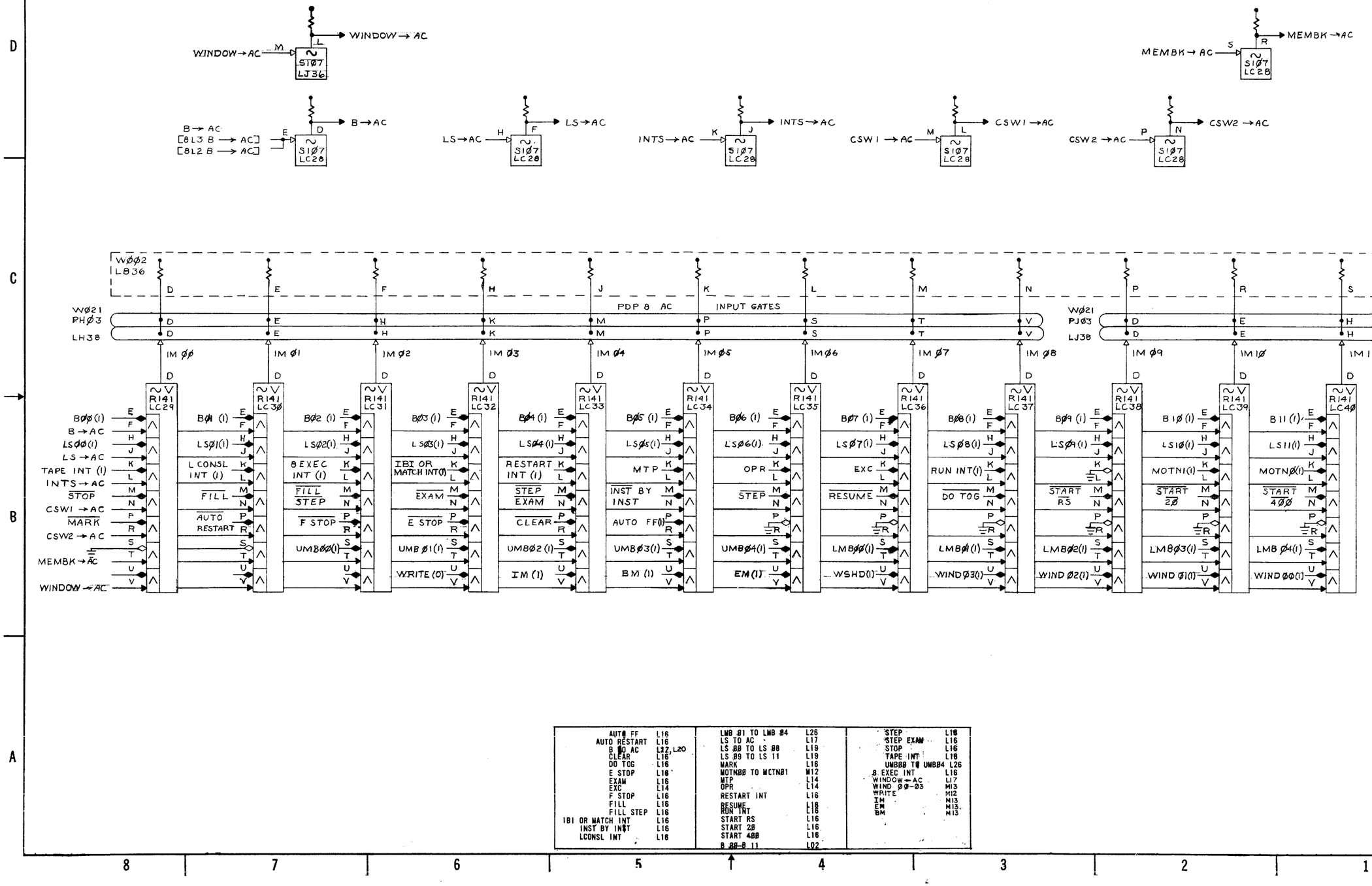


DSC	L14	A CLEAR Ø-Ø6	L28
END CARRY	L84	A CLEAR 7-11	L22
R TO A	L22	AØØ TO AØ4	L84
RØ6 TO R11	L86	BØ3 TO Ø11	L82
SAM	L14	BCLA 1-11	L22
Z TO A	L22	BCOAR	L22
zØ6 TO Z11	L86	COMP A	L22
		COMPARATOR	P24
		CU 11(Ø)	L84
		CU 11(1)	L84
		CVTPLS	L22

D-BS-LINC8-0-L5 Right Half A-Register

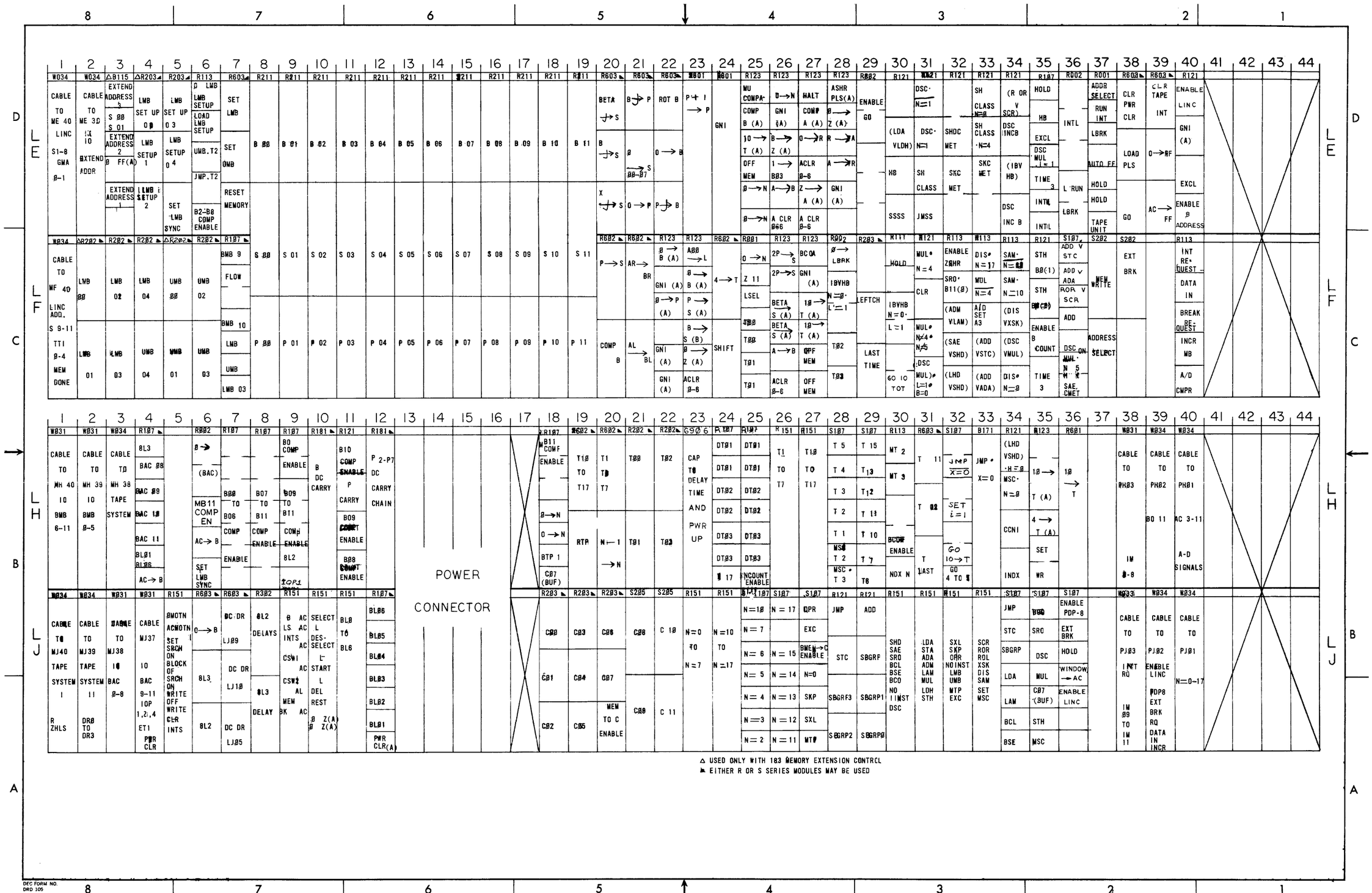


D-BS-LINC8-0-L6 R and Z Registers

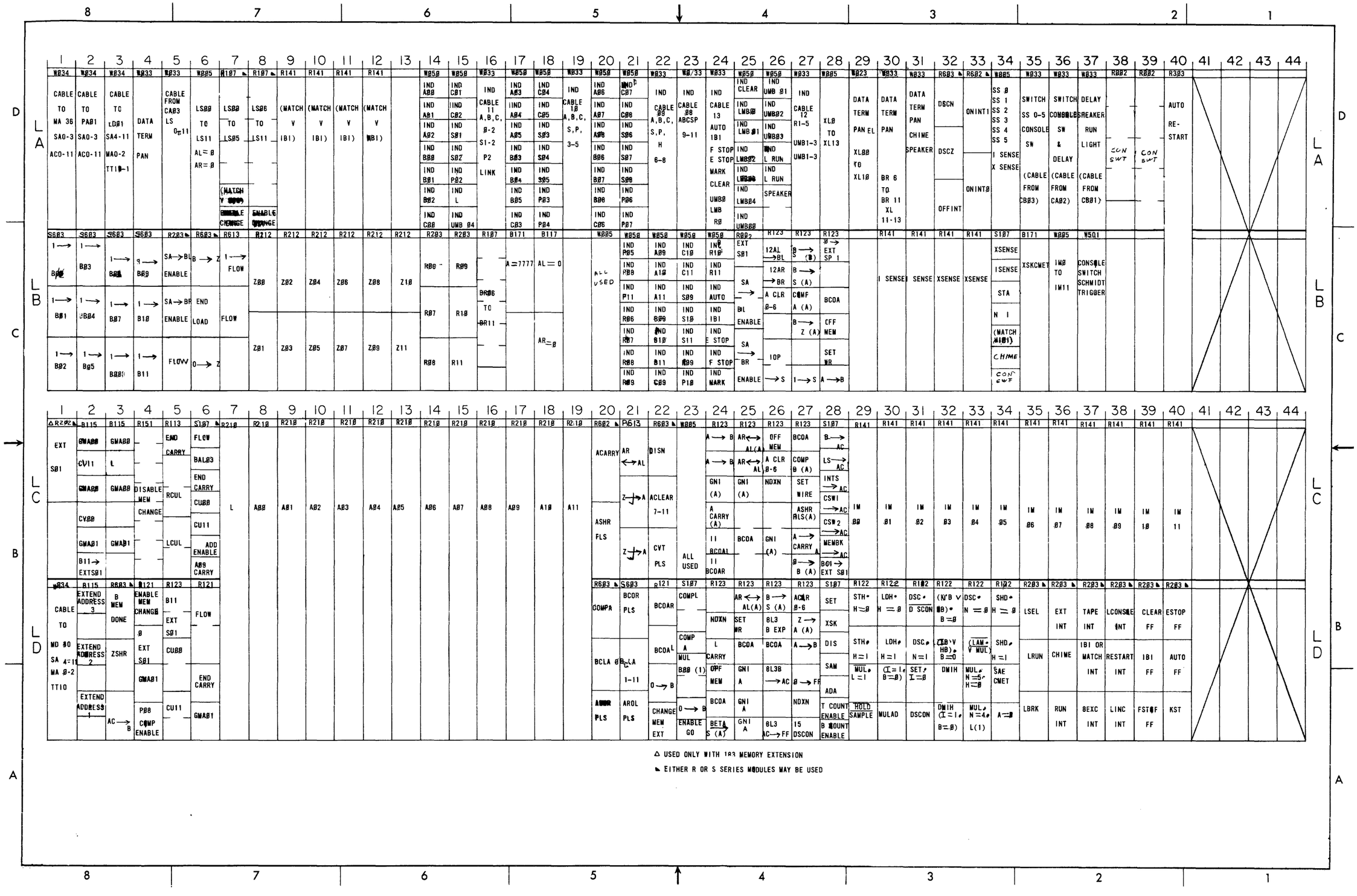


AUTO FF	L16	LMB Ø1 TO LMB Ø4	L26	STEP	L16
AUTO RESTART	L16	LS TO AC	L17	STEP EXAM	L16
B TO AC	L17, L20	LS Ø8 TO LS 08	L19	STOP	L16
CLEAR	L16	LS Ø9 TO LS 11	L19	TAPE INT	L16
DO TOG	L16	MARK	L16	UMBØØ TO UMBØ4	L26
E STOP	L16	MOTNØØ TO MOTNØ1	M12	8 EXEC INT	L16
EXAM	L16	MTP	L14	WINDOW → AC	L17
EXC	L14	OPR	L14	WIND ØØ-Ø3	M13
F STOP	L16	RESTART INT	L16	WRITE	M12
FILL	L16	RESUME	L16	IM	M13
FILL STEP	L16	RUN INT	L16	EM	M13
IBI OR MATCH INT	L16	START RS	L16	BM	M13
INST BY INST	L16	START 2Ø	L16		
LCONSL INT	L16	START 4ØØ	L16		
		B 08-B 11	L02		

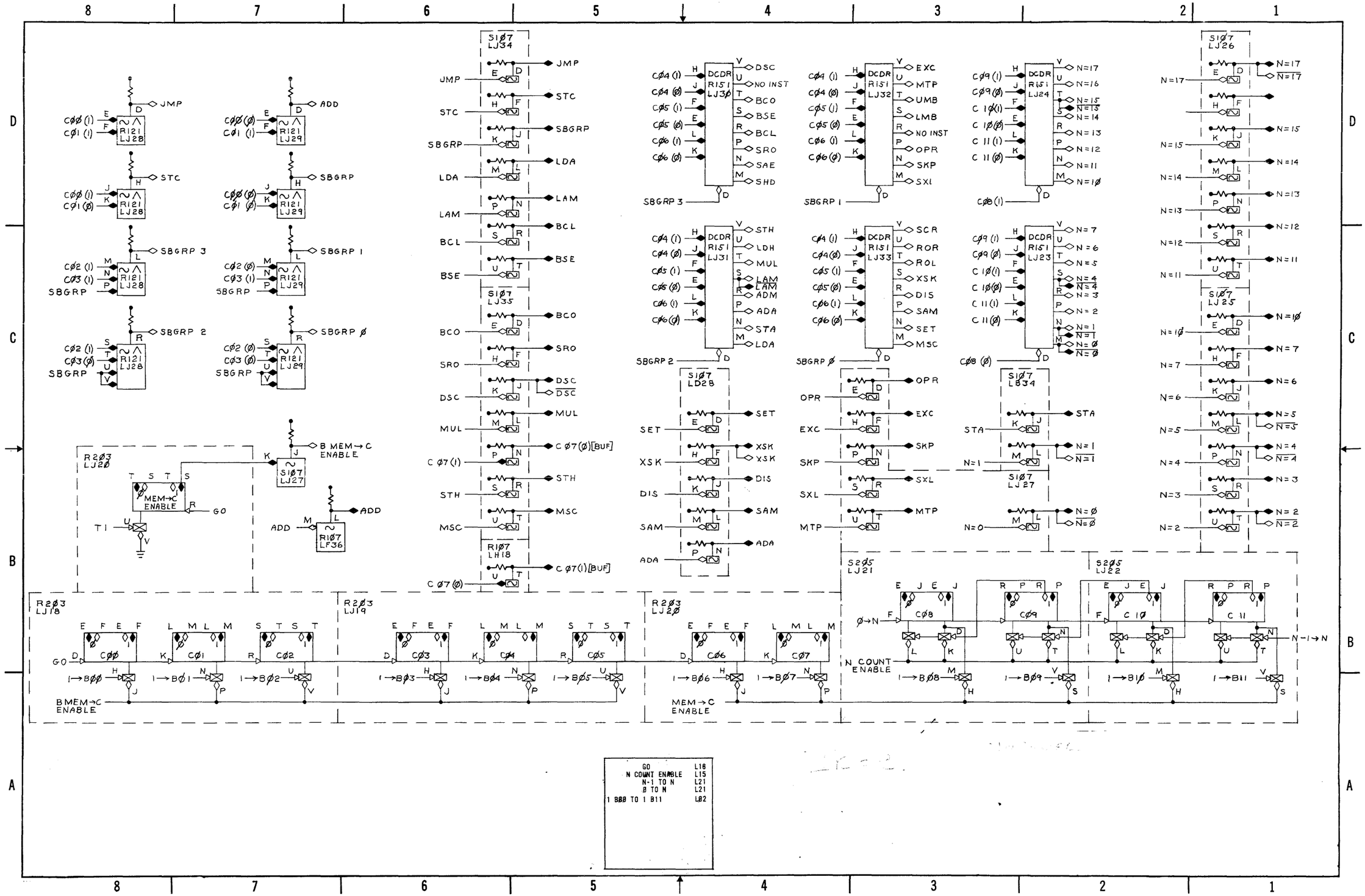
D-BS-LINC8-0-L7 PDP-8 AC Input Gates



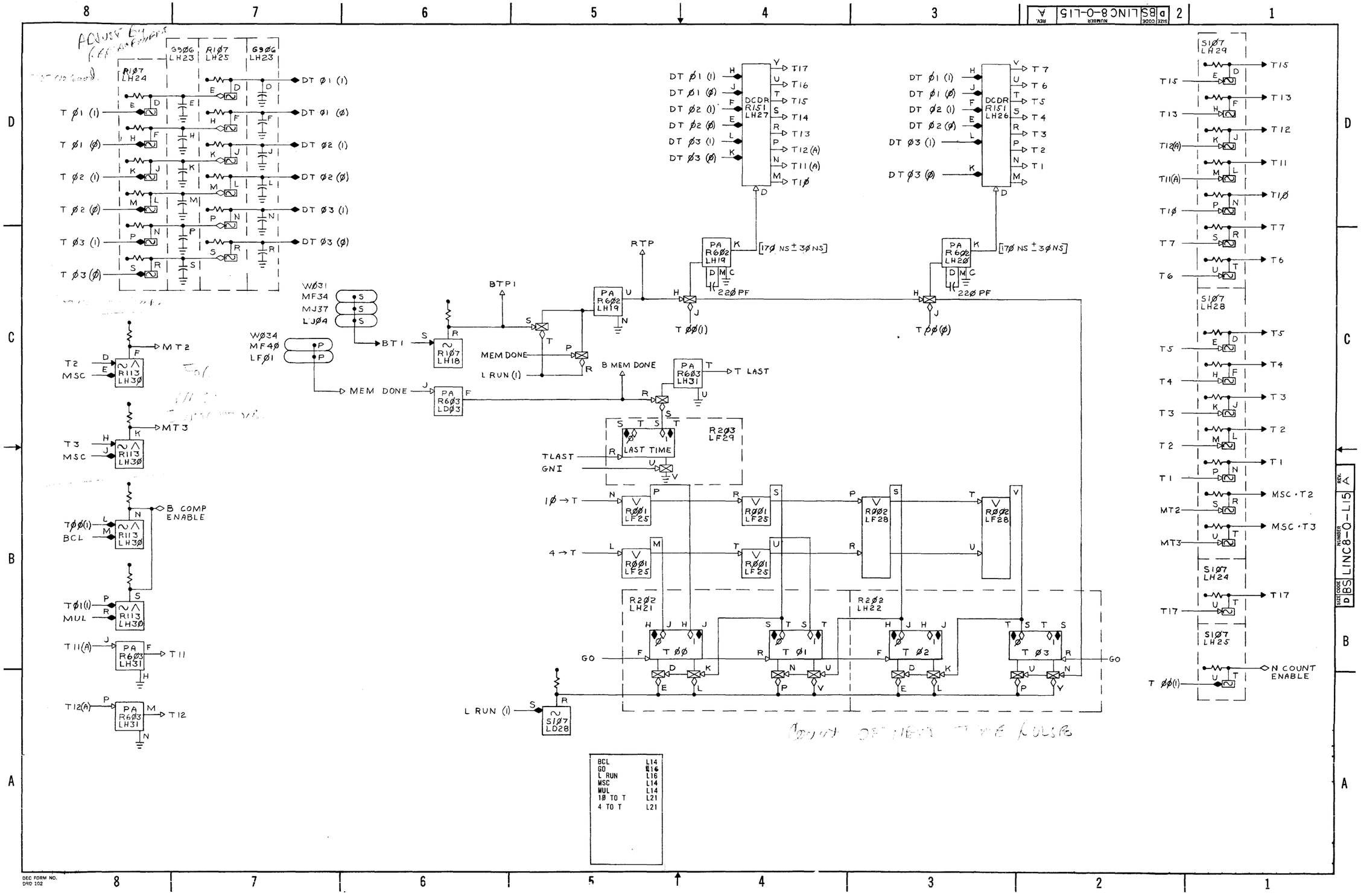
D-MU-LINC8-0-L10 LINC8 UML, LE-LJ



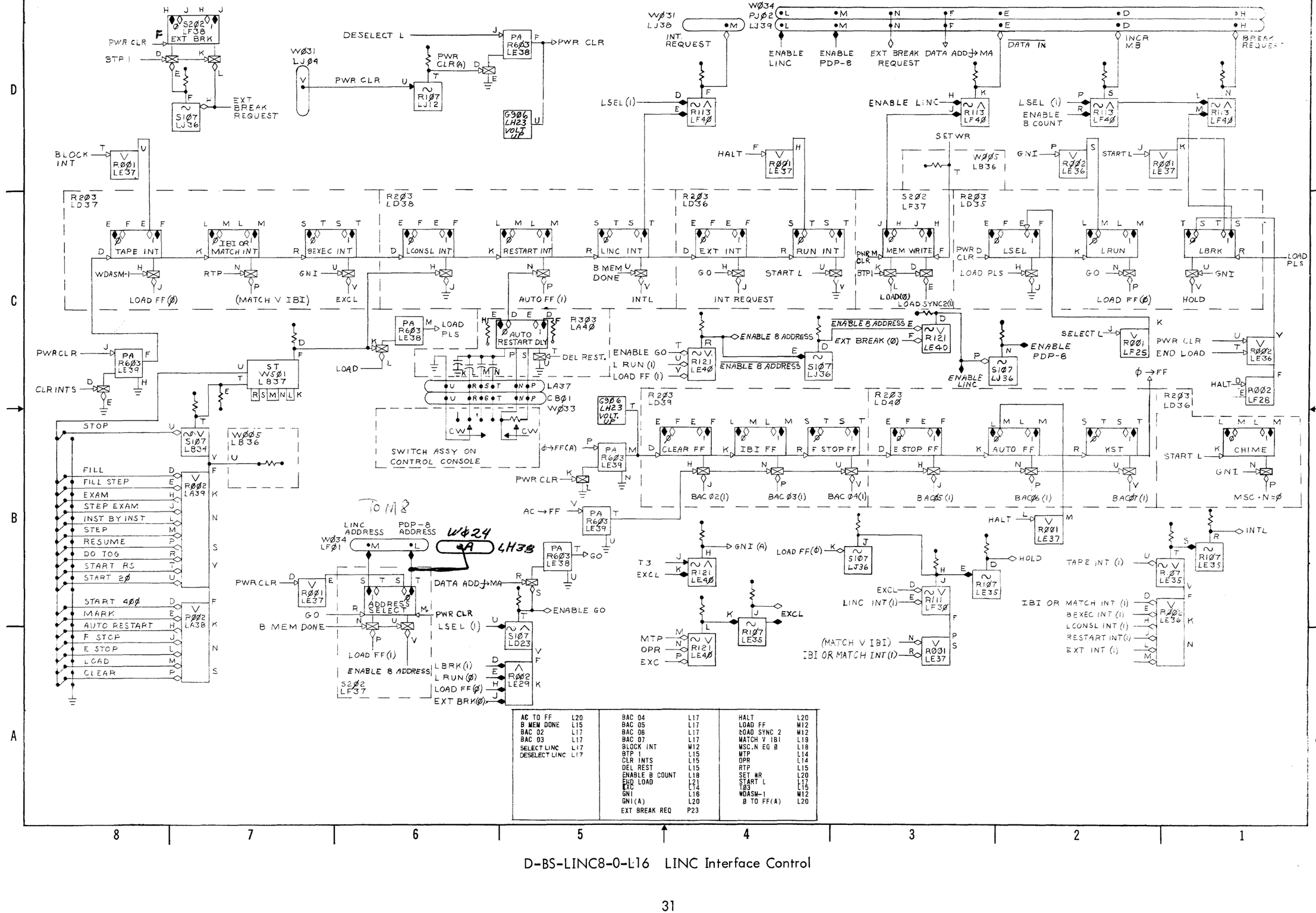
D-MU-LINC8-0-L11 LINC8 UML, LA-LD



D-BS-LINC8-0-L14 Control Register and Instruction Decoders

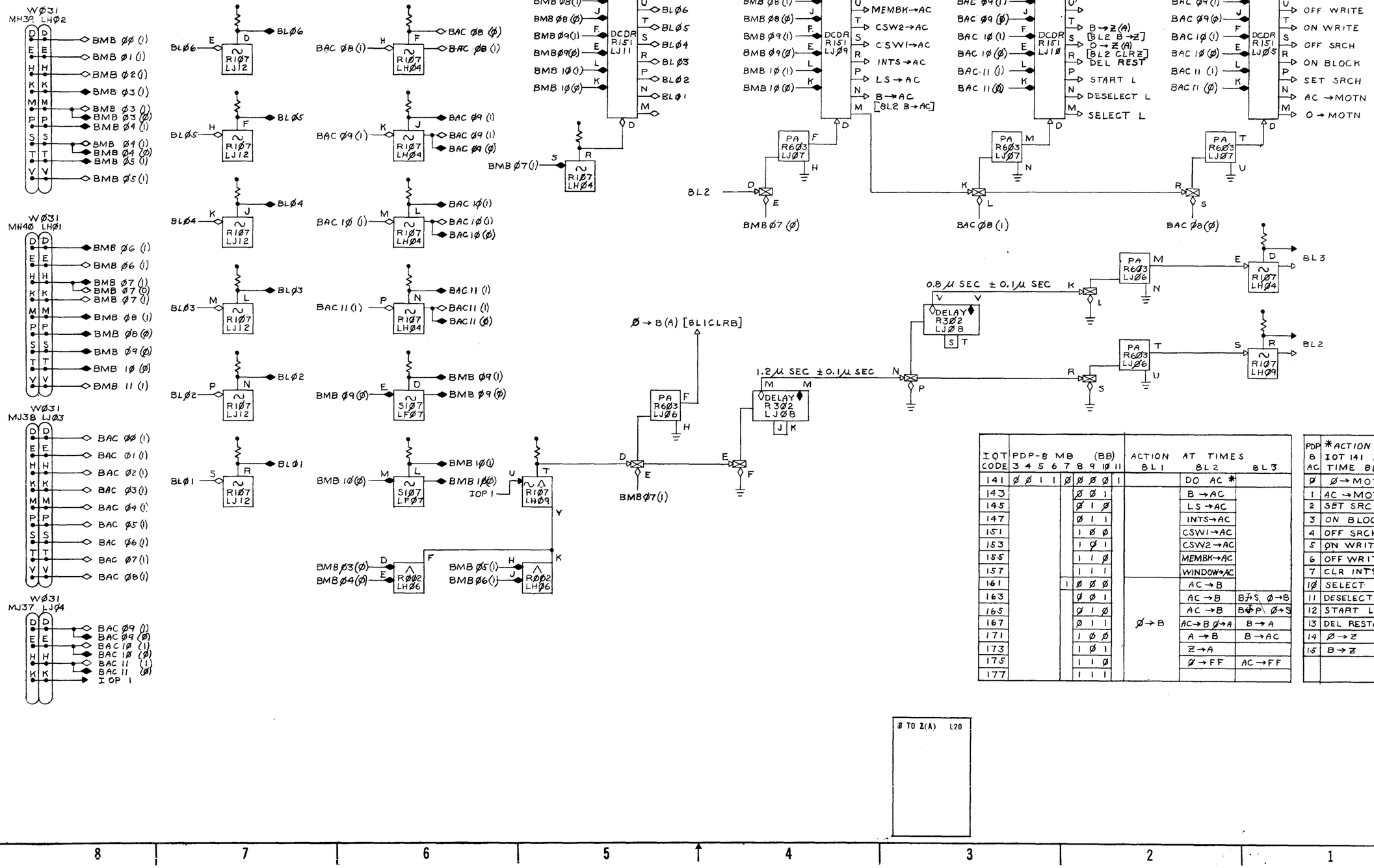


D-BS-LINC8-0-L15 Time Pulse Distributor



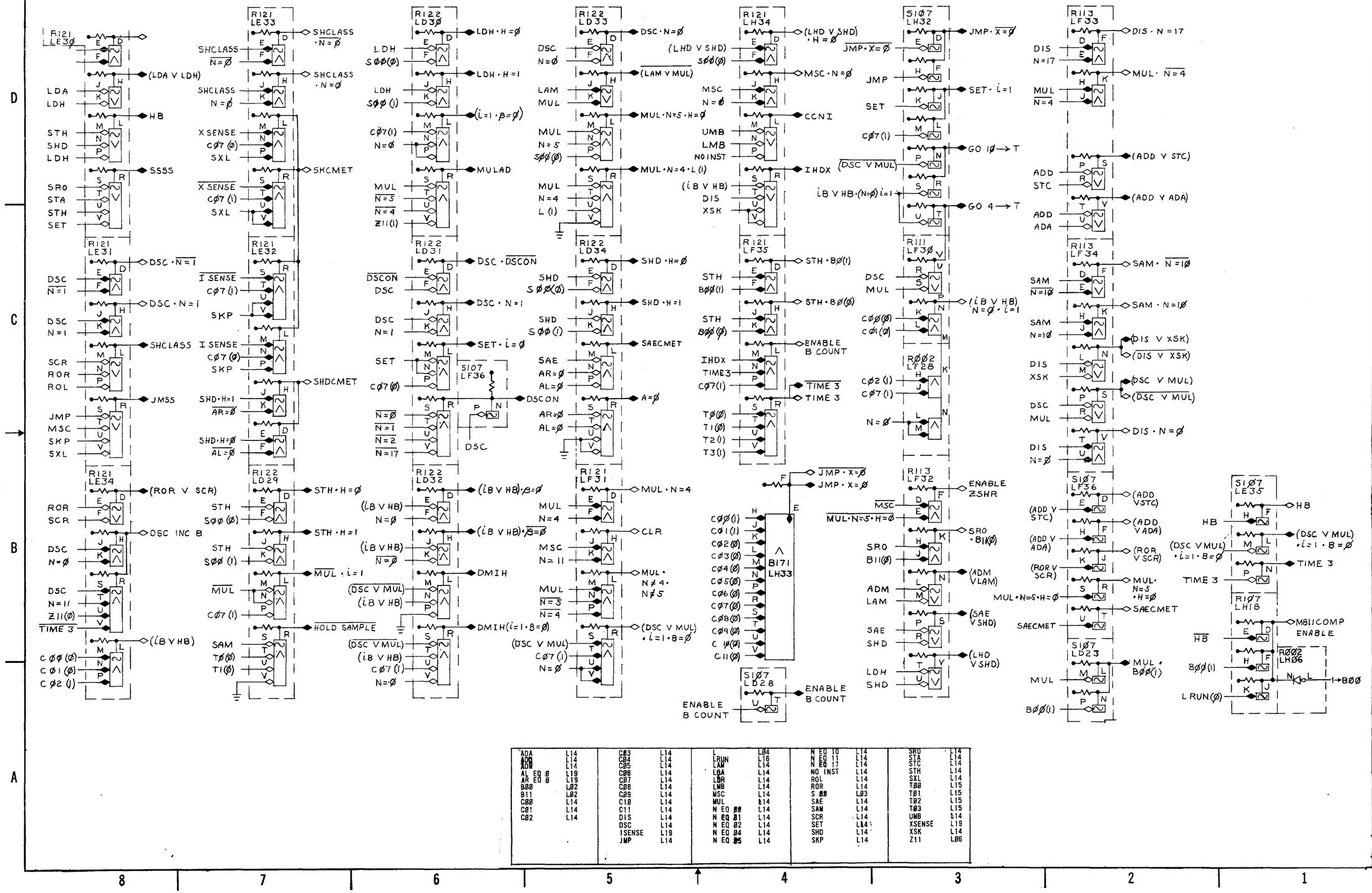
AC TO FF	L20	BAC 04	L17	HALT	L20
B MEM DONE	L15	BAC 05	L17	LOAD FF	M12
BAC 02	L17	BAC 06	L17	LOAD SYNC 2	M12
BAC 03	L17	BAC 07	L17	MATCH V IBI	L19
SELECT LINC	L17	BLOCK INT	M12	MSC.N EQ Ø	L18
DESELECT LINC	L17	BTP 1	L15	MTP	L14
		CLR INTS	L15	OPR	L14
		DEL REST	L15	RTP	L15
		ENABLE B COUNT	L18	SET WR	L20
		END LOAD	L21	START L	L17
		EXC	L14	T03	L15
		GNI	L16	WDASM-1	M12
		GNI(A)	L20	Ø TO FF(A)	L20
		EXT BREAK REQ	P23		

D-BS-LINC8-0-L16 LINC Interface Control

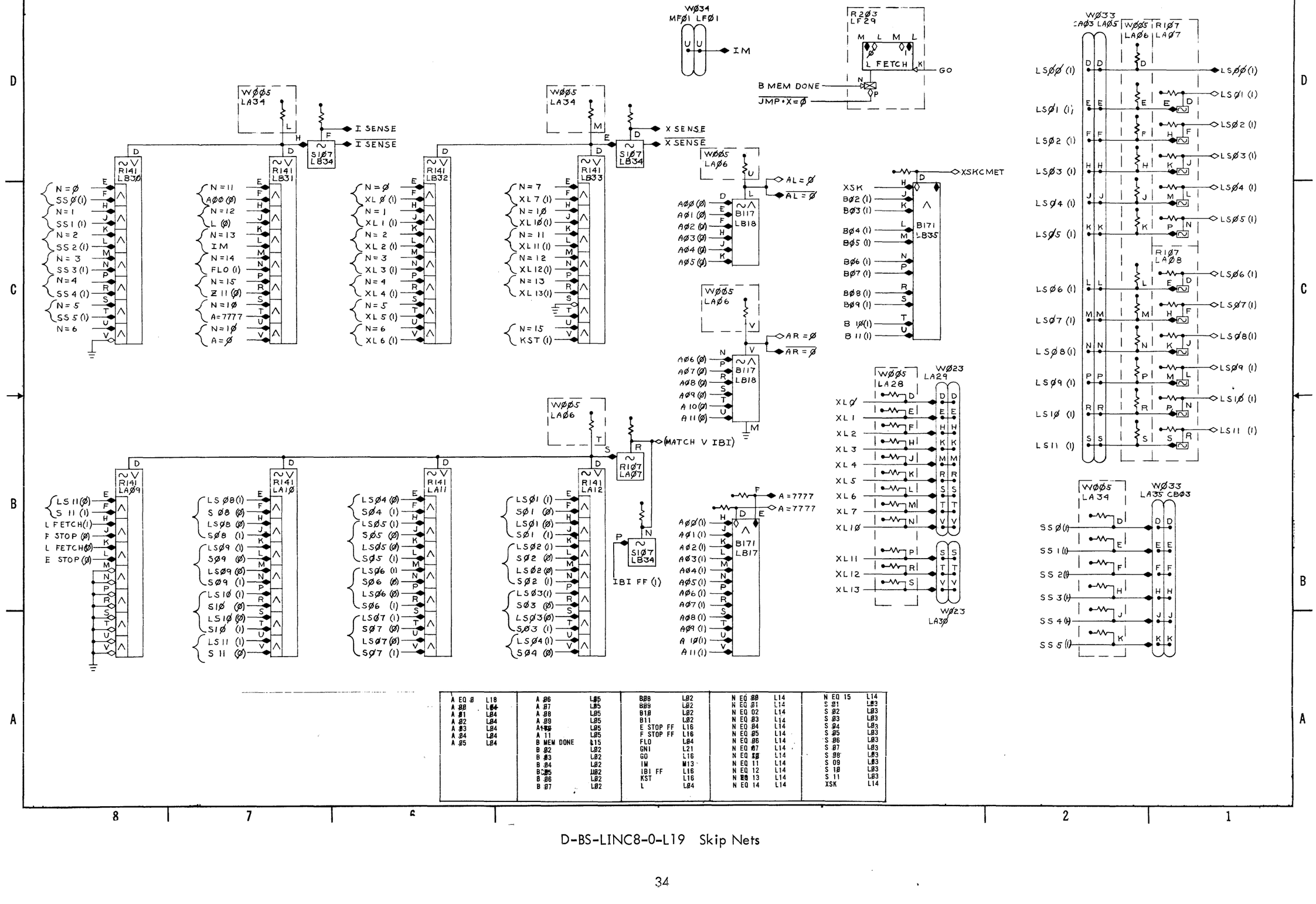


IOT CODE	PDP-8 MB (BB) 3 4 5 6 7 8 9 10 11	ACTION AT TIMES BL1	BL2	BL3
141	Ø Ø 1 1 Ø Ø Ø Ø 1		DO AC *	
143	Ø Ø 1		B →AC	
145	Ø 1 Ø		LS →AC	
147	Ø 1 1		INTS→AC	
151	1 Ø Ø		CSWI→AC	
153	1 Ø 1		CSW2→AC	
155	1 1 Ø		MEMBK→AC	
157	1 1 1		WINDOW→AC	
161	1 Ø Ø Ø		AC →B	
163	Ø Ø 1		AC →B	B→S, Ø→B
165	Ø 1 Ø		AC →B	B→P\ Ø→S
167	Ø 1 1	Ø→B	AC→B Ø→A	B→A
171	1 Ø Ø		A →B	B→AC
173	1 Ø 1		Z→A	
175	1 1 Ø		Ø→FF	AC→FF
177	1 1 1			

PDP 8 AC	*ACTION ON IOT 141 AT TIME BL2
Ø	Ø→MOTN
1	AC →MOTN
2	SET SRCH
3	ON BLOCK
4	OFF SRCH
5	ON WRITE
6	OFF WRITE
7	CLR INTS
1Ø	SELECT L
11	DESELECT L
12	START L
13	DEL RESTART
14	Ø→Z
15	B→Z

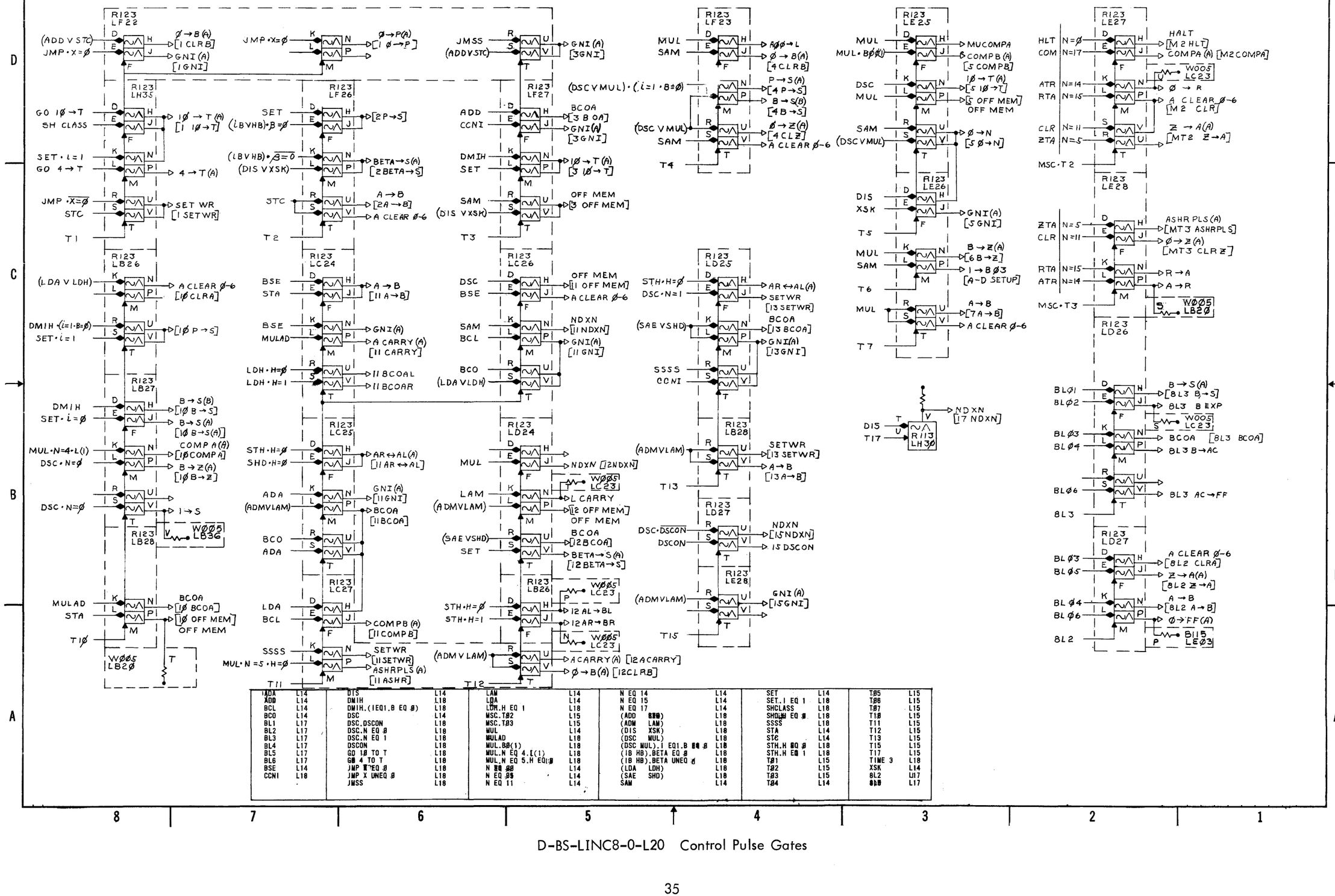


D-BS-LINC8-0-L18 Control Function



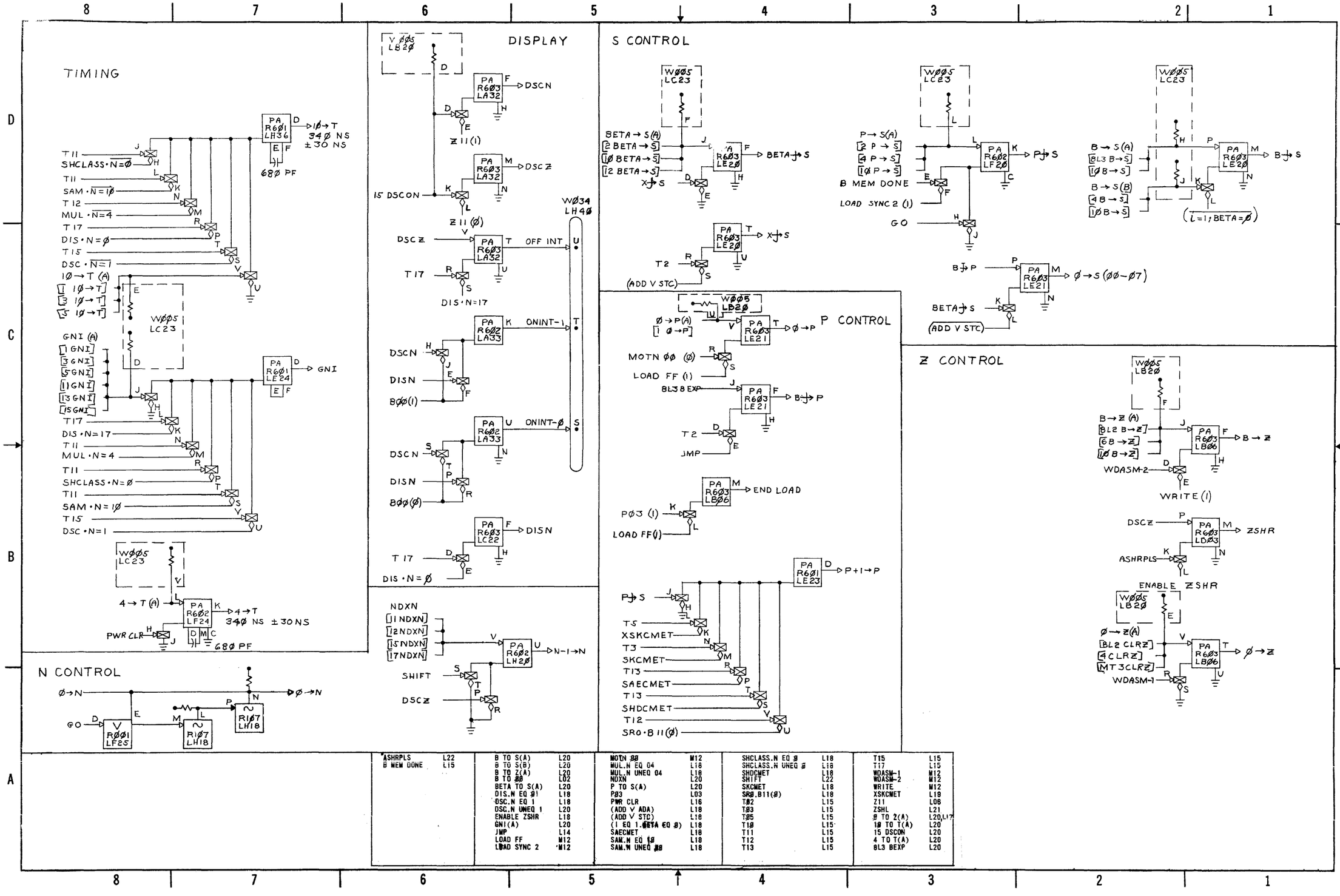
A EQ 0	L18	A 06	L05	B00	L02	N EQ 00	L14	N EQ 15	L14
A 00	L04	A 07	L05	B01	L02	N EQ 01	L14	S 01	L03
A 01	L04	A 08	L05	B10	L02	N EQ 02	L14	S 02	L03
A 02	L04	A 09	L05	B11	L02	N EQ 03	L14	S 03	L03
A 03	L04	A 10	L05	E STOP FF	L16	N EQ 04	L14	S 04	L03
A 04	L04	A 11	L05	F STOP FF	L16	N EQ 05	L14	S 05	L03
A 05	L04	B MEM DONE	L15	FLO	L04	N EQ 06	L14	S 06	L03
		B 02	L02	GNI	L21	N EQ 07	L14	S 07	L03
		B 03	L02	GO	L16	N EQ 08	L14	S 08	L03
		B 04	L02	IW	M13	N EQ 11	L14	S 09	L03
		B 05	L02	IBI FF	L16	N EQ 12	L14	S 10	L03
		B 06	L02	KST	L16	N EQ 13	L14	S 11	L03
		B 07	L02	L	L04	N EQ 14	L14	XSK	L14

D-BS-LINC8-0-L19 Skip Nets



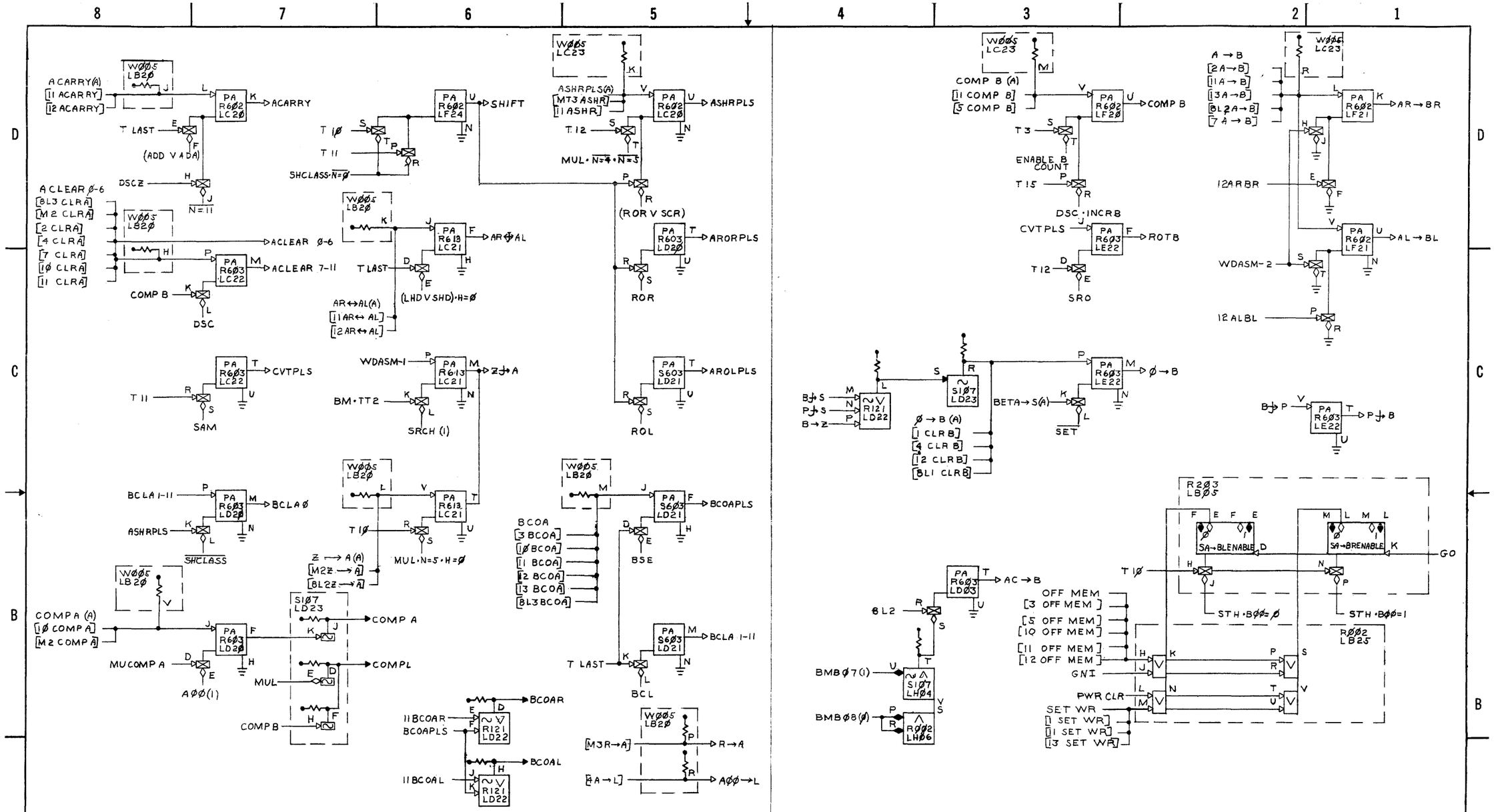
ADA	L14	DIS	L14	LAM	L14	N EQ 14	L14	SET	L14	T#5	L15
ADD	L14	DMIH	L18	LDA	L14	N EQ 15	L14	SET.I EQ 1	L18	T#6	L15
BCL	L14	DMIH.(IEQ1.B EQ Ø)	L18	LDM.H EQ 1	L18	N EQ 17	L14	SHCLASS	L18	T#7	L15
BCO	L14	DSC	L14	MSC.T#2	L15	(ADD SUB)	L18	SHD.H EQ Ø	L18	T1Ø	L15
BL1	L17	DSC.DSCON	L18	MSC.T#3	L15	(ADM LAM)	L18	SSSS	L18	T11	L15
BL2	L17	DSC.N EQ Ø	L18	MUL	L14	(DIS XSK)	L18	STA	L14	T12	L15
BL3	L17	DSC.N EQ 1	L18	MULAD	L14	(DSC MUL)	L14	STC	L14	T13	L15
BL4	L17	DSCON	L18	MUL.B#(1)	L18	(DSC MUL).I EQ1.B EQ Ø	L18	STH.H EQ Ø	L18	T15	L15
BL5	L17	GO 1Ø TO T	L18	MUL.N EQ 4.I(1)	L18	(IB HB).BETA EQ Ø	L18	STH.H EQ 1	L18	T17	L15
BL6	L17	GO 4 TO T	L18	MUL.N EQ 5.H EQ Ø	L18	(IB HB).BETA UNEQ Ø	L18	T#1	L15	TIME 3	L18
BSE	L14	JMP X EQ Ø	L18	N EQ Ø5	L14	(LDA LDH)	L18	T#2	L15	XSK	L14
CCNI	L18	JMP X UNEQ Ø	L18	N EQ 9	L14	(SAE SHD)	L18	T#3	L15	8L2	L17
		JMSS	L18	N EQ 11	L14	SAM	L14	T#4	L14	8L8	L17

D-BS-LINC8-0-L20 Control Pulse Gates



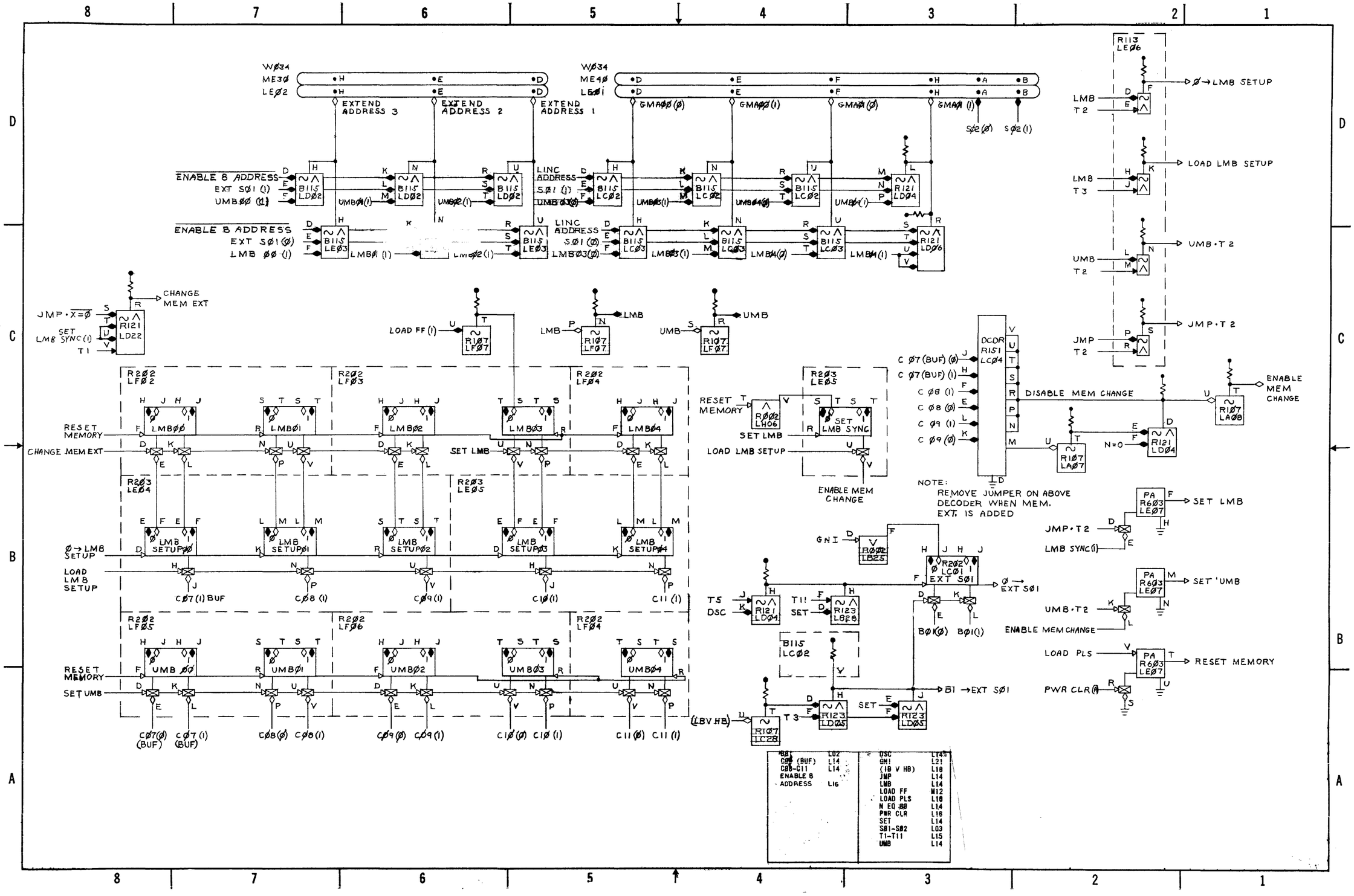
ASHRPLS	L22	B TO S(A)	L20	MOTN ØØ	M12	SHCLASS.N EQ Ø	L18	T15	L15
B MEM DONE	L15	B TO S(B)	L20	MUL.N EQ Ø4	L16	SHCLASS.N UNEQ Ø	L18	T17	L15
		B TO Z(A)	L20	MUL.N UNEQ Ø4	L18	SHDCMET	L18	WDASM-1	M12
		B TO ØØ	L02	NDXN	L20	SHIFT	L22	WDASM-2	M12
		BETA TO S(A)	L20	P TO S(A)	L20	SKCMET	L18	WRITE	M12
		DIS.N EQ Ø!	L18	PØ3	L03	SR0.B11(Ø)	L18	XSKCMET	L18
		DSC.N EQ 1	L18	PWR CLR	L16	T02	L15	Z11	L06
		DSC.N UNEQ 1	L20	(ADD V ADA)	L18	TØ3	L15	ZSHL	L21
		ENABLE ZSHR	L18	(ADD V STC)	L18	TØ5	L15	Ø TO Z(A)	L20,L17
		GNI(A)	L20	(1 EQ 1.BETA EQ Ø)	L18	T1Ø	L15	1Ø TO T(A)	L20
		JMP	L14	SAECMET	L18	T11	L15	15 DSCON	L20
		LOAD FF	M12	SAM.N EQ 1Ø	L18	T12	L15	4 TO T(A)	L20
		LOAD SYNC 2	M12	SAM.N UNEQ ØØ	L18	T13	L15	BL3 BEXP	L20

D-BS-LINC8-0-L21 S, P, Z, T, N and Dis. Cont. Pulses



A CLEAR Ø-Ø6	L20	AØØ TO L	L20	DSC	L14	R TO A	L20	T1Ø	L15
A TO B	L20	B TO P	L21	DSCINCB	L18	ROL	L14	T11	L15
A ØØ	L04	B TO S	L21	DSCZ	L21	ROR	L14	T12	L15
AR TO FM AL(A)	L20	B TO Z	L21	ENABLE B COUNT	L18	(ADD V ADA)	L18	T15	L15
		BCL	L14	GNI	L21	(LHD V SHD), H ØØ Ø	L18	WDASM-1	M12
		BCOA	L20	GO	L16	FROM V SCR)	L18	WDASM-2	M12
		BETA TO S(A)	L20	MUCOMPA	L20	SAM	L14	Z TO A(A)	L20
		BMB Ø7	L17	MUL	L14	SET	L14	11 BCOAL	L20
		BMB Ø8	L17	MUL.N EQ 5.H EQ Ø	L18	SET WR	L20	11 BCOAR	L20
		BM.TT Ø2	L18	MUL.N UNEQ 4.N UNEQ 5	L18	SHCLASS.N UNEQ Ø	L18	12 AL TO BL	L20
		BSE	L14	N EQ 11	L14	SRCH	M12	12 AR TO BR	L20
		COMP A(A)	L20	OFF MEM	L20	SRO	L14	8L2	L17
		COMP B(A)	L20	PWR CLR	L18	T LAST	L15	P TO S	L21
								Ø→B(A)	L17, L20

D-BS-LINC8-0-L22 A and B Register Control Pulses



D-BS-LINC8-0-L26 Memory Extension

ALL INDICATOR INPUTS COMING FROM FLIP FLOPS COME FROM THE 1 NEG. SIDE (I.E. AØØ(1)→)

W05Ø LA14: AØØ IND A ØØ; A Ø1 IND A Ø1; A Ø2 IND A Ø2; B ØØ IND B ØØ; B Ø1 IND B Ø1; B Ø2 IND B Ø2; C ØØ IND C ØØ

W05Ø LA15: C Ø1 IND C Ø1; C Ø2 IND C Ø2; S Ø1 IND S Ø1; S Ø2 IND S Ø2; P Ø2 IND P Ø2; L IND L; UMB Ø4 IND UMB Ø4

W05Ø LA17: A Ø3 IND A Ø3; A Ø4 IND A Ø4; A Ø5 IND A Ø5; B Ø3 IND B Ø3; B Ø4 IND B Ø4; B Ø5 IND B Ø5; C Ø3 IND C Ø3

W05Ø LA18: C Ø4 IND C Ø4; C Ø5 IND C Ø5; S Ø3 IND S Ø3; S Ø4 IND S Ø4; S Ø5 IND S Ø5; P Ø3 IND P Ø3; P Ø4 IND P Ø4

W05Ø LA20: A Ø6 IND A Ø6; A Ø7 IND A Ø7; A Ø8 IND A Ø8; B Ø6 IND B Ø6; B Ø7 IND B Ø7; B Ø8 IND B Ø8; C Ø6 IND C Ø6

W05Ø LA21: C Ø7 (BUF) IND C Ø7; C Ø8 IND C Ø8; S Ø6 IND S Ø6; S Ø7 IND S Ø7; S Ø8 IND S Ø8; P Ø6 IND P Ø6; P Ø7 IND P Ø7

W05Ø LB22: A Ø9 IND A Ø9; A 1Ø IND A 1Ø; A 11 IND A 11; B Ø9 IND B Ø9; B 1Ø IND B 1Ø; B 11 IND B 11; C Ø9 IND C Ø9

W05Ø LB23: C 1Ø IND C 1Ø; C 11 IND C 11; S Ø9 IND S Ø9; S 1Ø IND S 1Ø; S 11 IND S 11; P Ø9 IND P Ø9; P 1Ø IND P 1Ø

W05Ø LB21: P Ø5 IND P Ø5; P Ø8 IND P Ø8; P 11 IND P 11; R Ø6 IND R Ø6; R Ø7 IND R Ø7; R Ø8 IND R Ø8; R Ø9 IND R Ø9

W05Ø LB24: R 1Ø IND R 1Ø; R 11 IND R 11; AUTO FF IND AUTO; IBI FF IND IBI; E STOP FF IND E STOP; F STOP FF IND F STOP; MARK FF IND MARK

W05Ø LA25: CLEAR FF IND CLEAR; LMB ØØ IND LMB ØØ; LMB Ø1 IND LMB Ø1; LMB Ø2 IND LMB Ø2; LMB Ø3 IND LMB Ø3; LMB Ø4 IND LMB Ø4; UMB ØØ IND UMB ØØ

W05Ø LA26: UMB Ø1 IND UMB Ø1; UMB Ø2 IND UMB Ø2; UMB Ø3 IND UMB Ø3; L RUN IND L RUN; L RUN IND L RUN; AØØ SPEAKER; AØØ

TO DAT TERMINAL PAN. W033 LA31: -15 V; +10 V; SPEAKER; CHIME; CHIME FF(1) S; R; SIØ7 LB34

W033 LA16 IND11: PWR -15V; GND; IND C Ø2; IND L; IND A Ø2; IND LMB 4; IND B Ø2; IND UMB 4; IND S Ø2; IND B ØØ; IND P Ø2; IND AØØ; IND C Ø1; IND C ØØ; IND A Ø1; IND S Ø1; IND B Ø1

W033 LA19 IND1Ø: IND C Ø5; IND P Ø3; IND A Ø5; IND S Ø3; IND B Ø5; IND B Ø3; IND S Ø5; IND A Ø3; IND P Ø5; IND C Ø3; IND C Ø4; IND P Ø4; IND A Ø4; IND S Ø4; IND B Ø4

W033 LA22 IND Ø9: IND C Ø8; IND P Ø6; IND A Ø8; IND S Ø6; IND B Ø8; IND B Ø6; IND S Ø8; IND A Ø6; IND P Ø8; IND C Ø6; IND C Ø7; IND P Ø7; IND A Ø7; IND S Ø7; IND B Ø7

W033 LA23 IND Ø8: IND C 11; IND P Ø9; IND A 11; IND S Ø9; IND B 11; IND B Ø9; IND S 11; IND A Ø9; IND P 11; IND C Ø9; IND C 1Ø; IND P 1Ø; IND A 1Ø; IND S 1Ø; IND B 1Ø

W033 LA24 IND13: IND AUTO; IND IBI; IND UMB ØØ; IND E STOP; IND LMB ØØ; IND F STOP; IND R Ø6; IND MARK; IND CLEAR

W033 LA27 IND12: IND R Ø7; IND R Ø8; IND R Ø9; IND LMB Ø1; IND UMB Ø3; IND UMB Ø1; IND LMB Ø3; IND R 1Ø; IND UMB Ø2; IND R 11; IND LMB Ø2

W033 LA05 CA03: LS ØØ(1); LS Ø1(1); LS Ø2(1); LS Ø3(1); LS Ø4(1); LS Ø5(1); LS Ø6(1); LS Ø7(1); LS Ø8(1); LS Ø9(1); LS 1Ø(1); LS 11(1)

W033 LA35 CB03: SS ØØ(1); SS Ø1(1); SS Ø2(1); SS Ø3(1); SS Ø4(1); SS Ø5(1); AUTO RESTART; CLEAR; E STOP; EXAM; FILL; FILL STEP; F STOP; INST BY INST

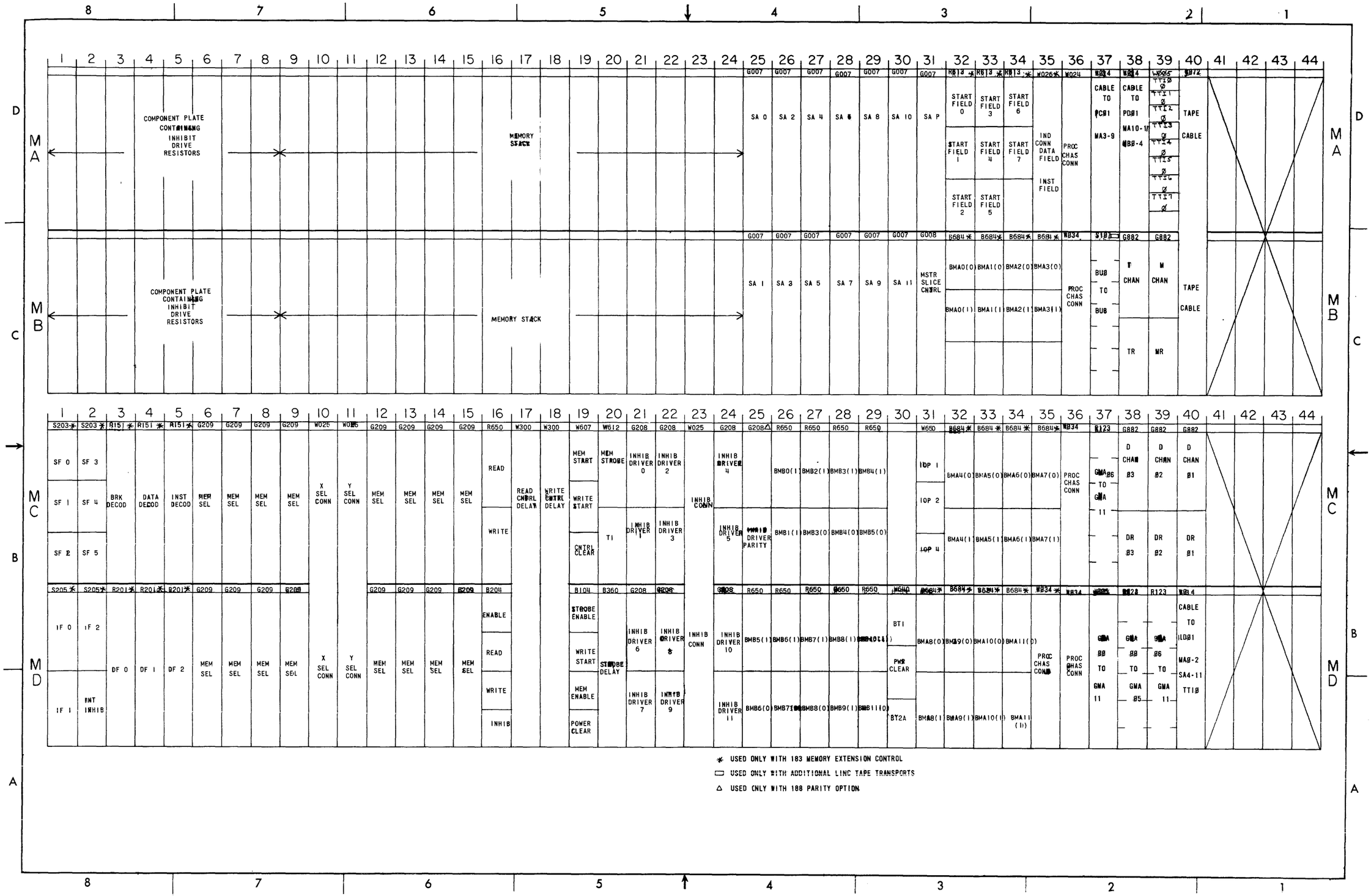
W033 LA36 CA02: MARK; RESUME; LOAD; START RS; START 2Ø; START 4ØØ; STEP; STEP EXAM; STOP; DO TOG; LB37U (-3V SUPPLY)

W033 LA37 CB01: IND L RUN; SPEAKER; CHIME; DELAY POT; DELAY CAP; ON CONT. PAN.

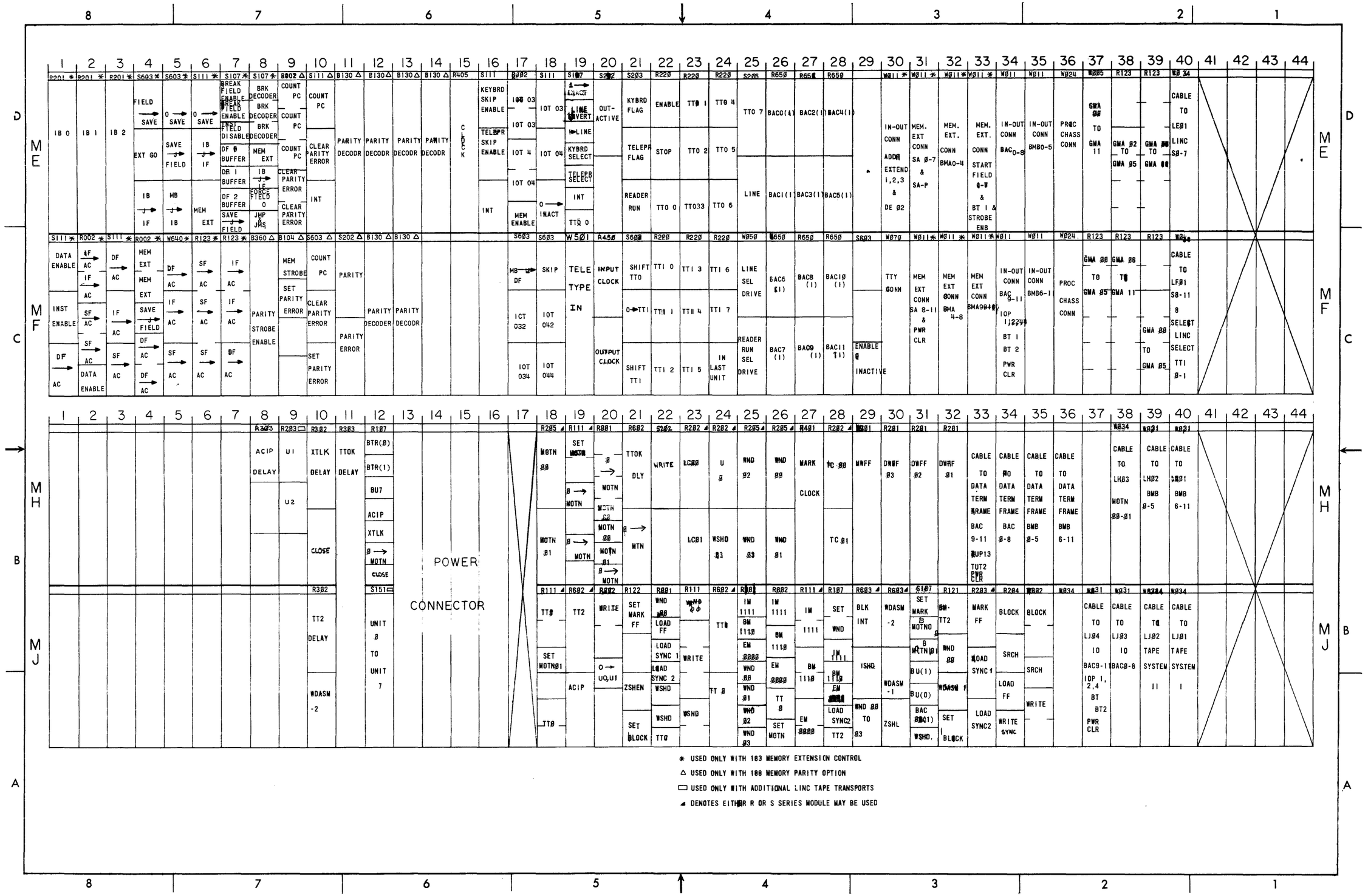
P02 TO P11	L03
R06 TO R11	L06
S01 TO S11	L03
UMB ØØ TO UMB Ø4	L16

AØØ TO A05	L04
A06 TO A11	L05
AUTO FF	D16
BØØ TO B11	L02
CØØ TO C11	L14
E STOP FF	L16
F STOP FF	L16
IBI FF	L16
L	L04
LMB ØØ TO LMB Ø4	L26
MARK FF	M12

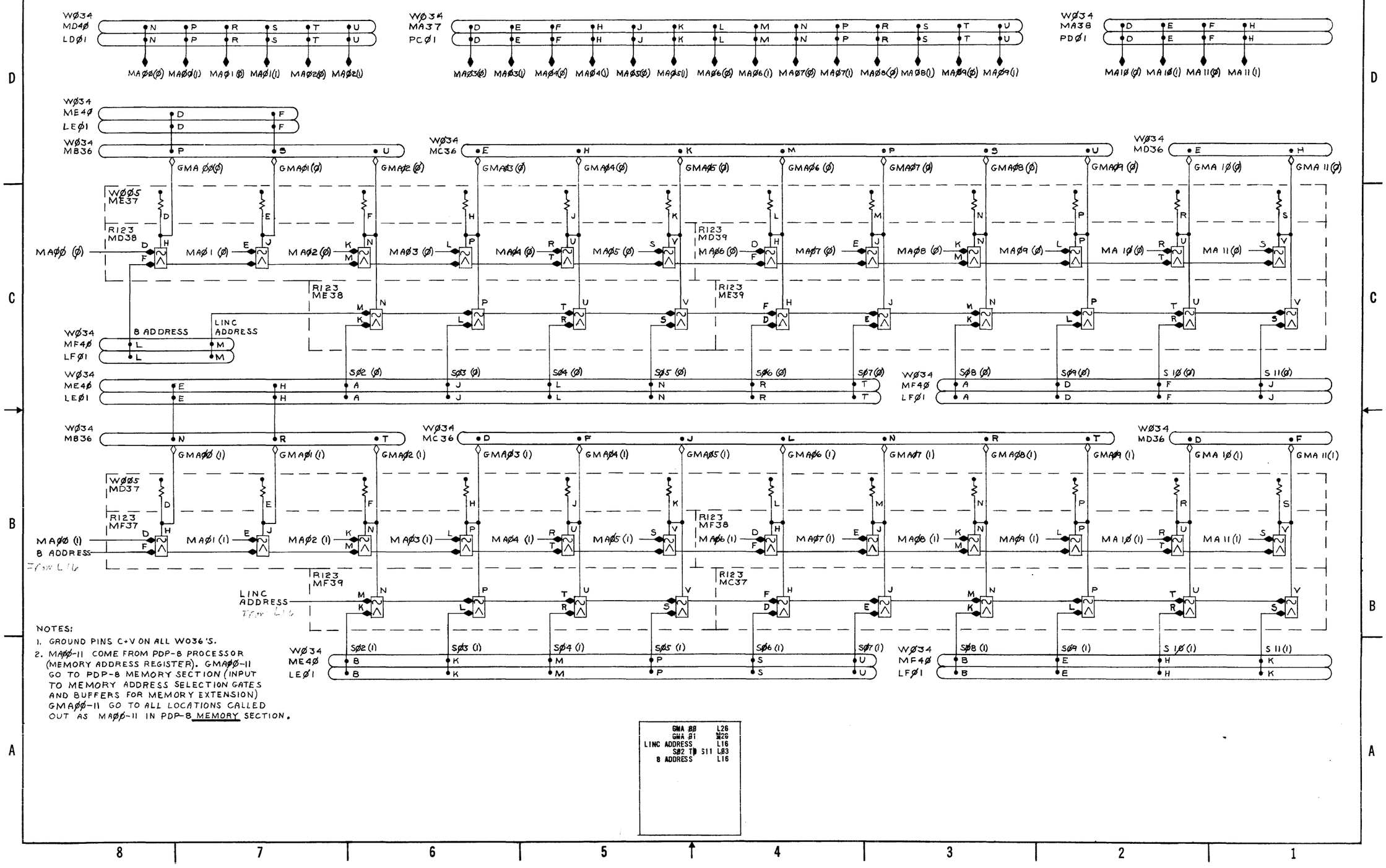
D-BS-LINC8-0-L28 LINC Switches and Indicators



D-MU-LINC8-0-M3 LINC-8 UML, MA-MD



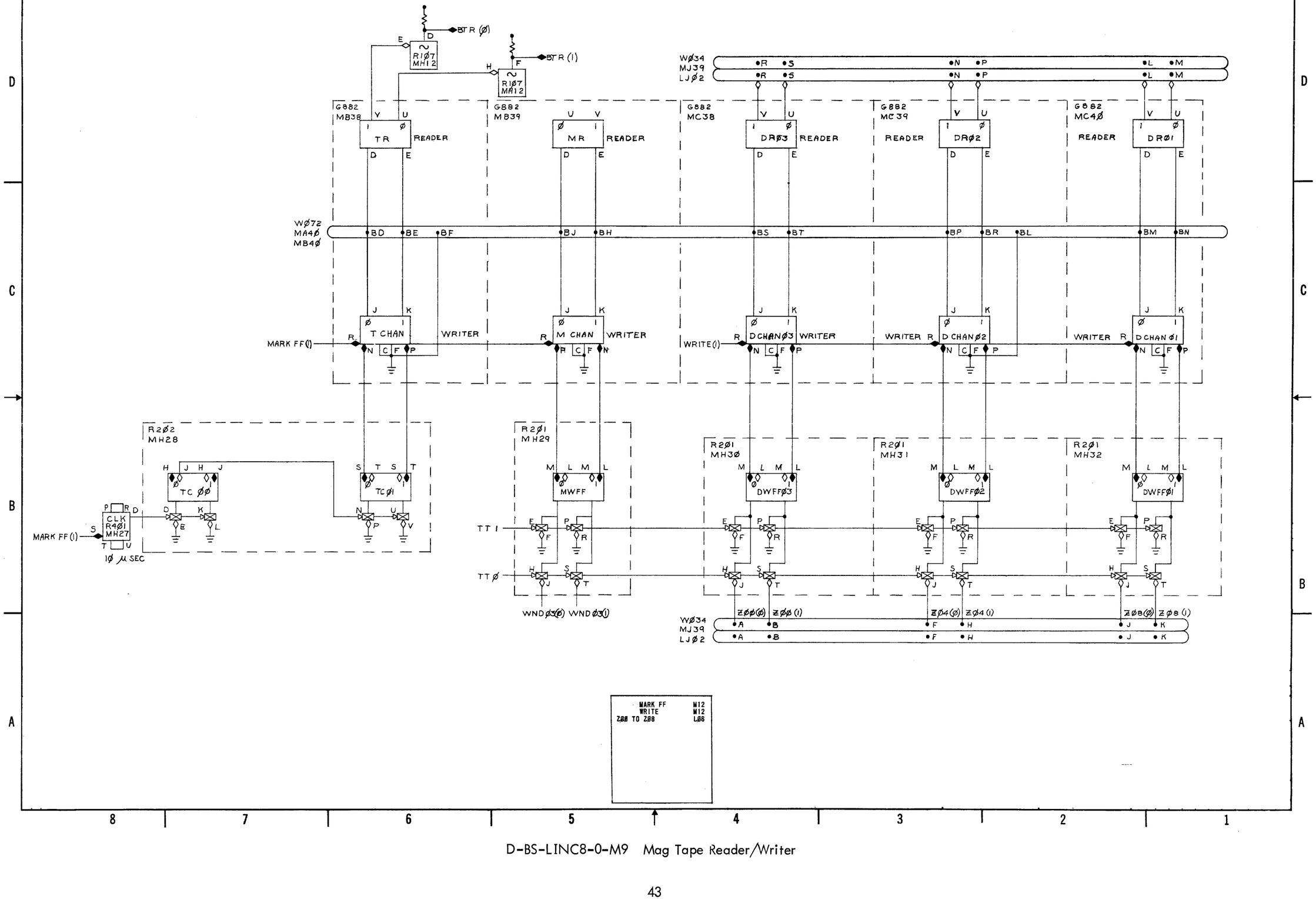
D-MU-LINC8-0-M4 LINC-8 UML, ME-MJ



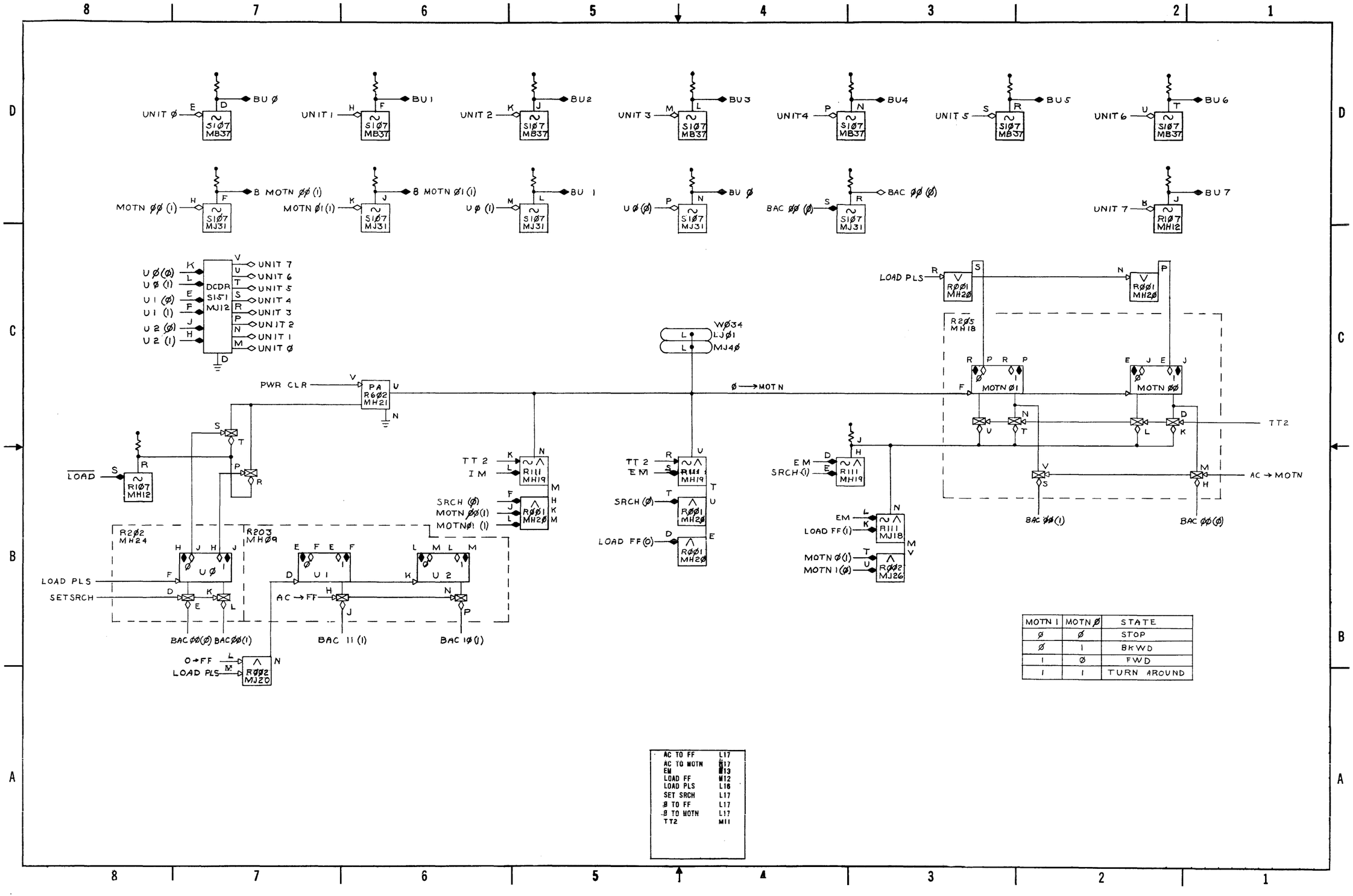
NOTES:

1. GROUND PINS C+V ON ALL W036'S.
2. MA00-11 COME FROM PDP-8 PROCESSOR (MEMORY ADDRESS REGISTER). GMA00-11 GO TO PDP-8 MEMORY SECTION (INPUT TO MEMORY ADDRESS SELECTION GATES AND BUFFERS FOR MEMORY EXTENSION) GMA00-11 GO TO ALL LOCATIONS CALLED OUT AS MA00-11 IN PDP-8 MEMORY SECTION.

D-BS-LINC8-0-M8 PDP-8 ADDR Input Gates



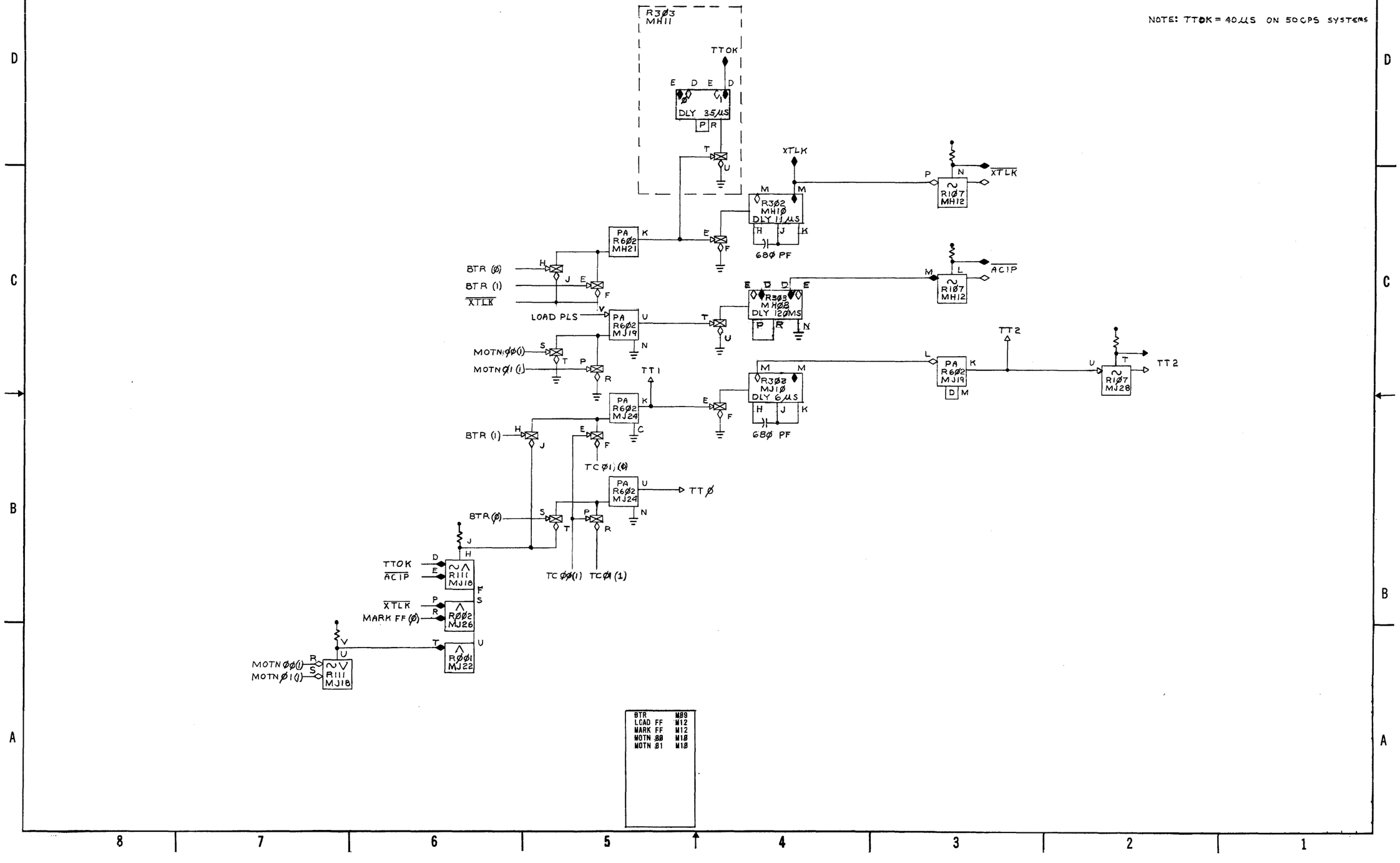
D-BS-LINC8-0-M9 Mag Tape Reader/Writer



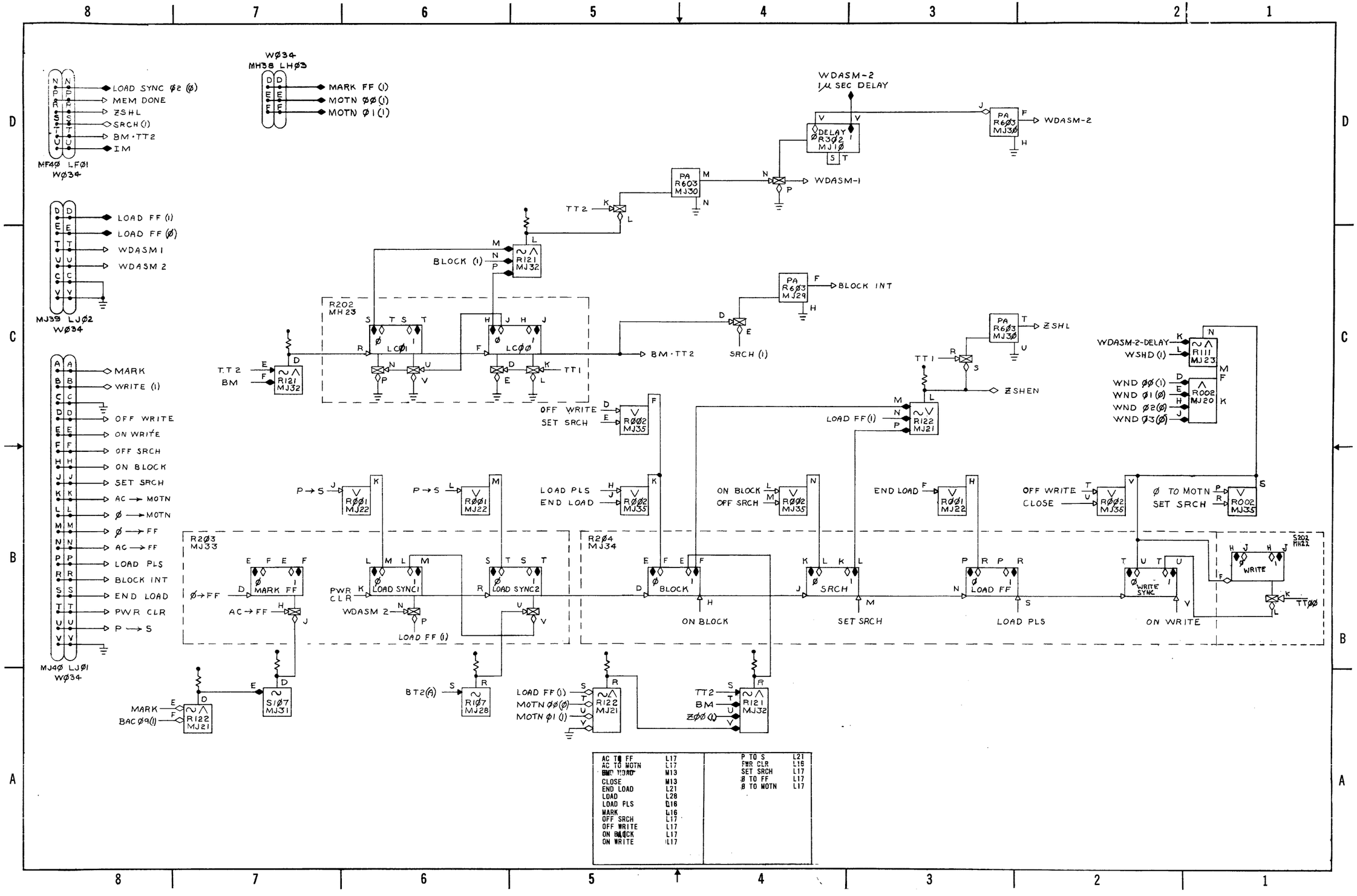
MOTN 1	MOTN Ø	STATE
Ø	Ø	STOP
Ø	1	BKWD
1	Ø	FWD
1	1	TURN AROUND

AC TO FF	L17
AC TO MOTN	M17
EM	M13
LOAD FF	M12
LOAD PLS	L16
SET SRCH	L17
B TO FF	L17
B TO MOTN	L17
TT2	M11

D-BS-LINC8-0-M10 Mag Tape Motion Control

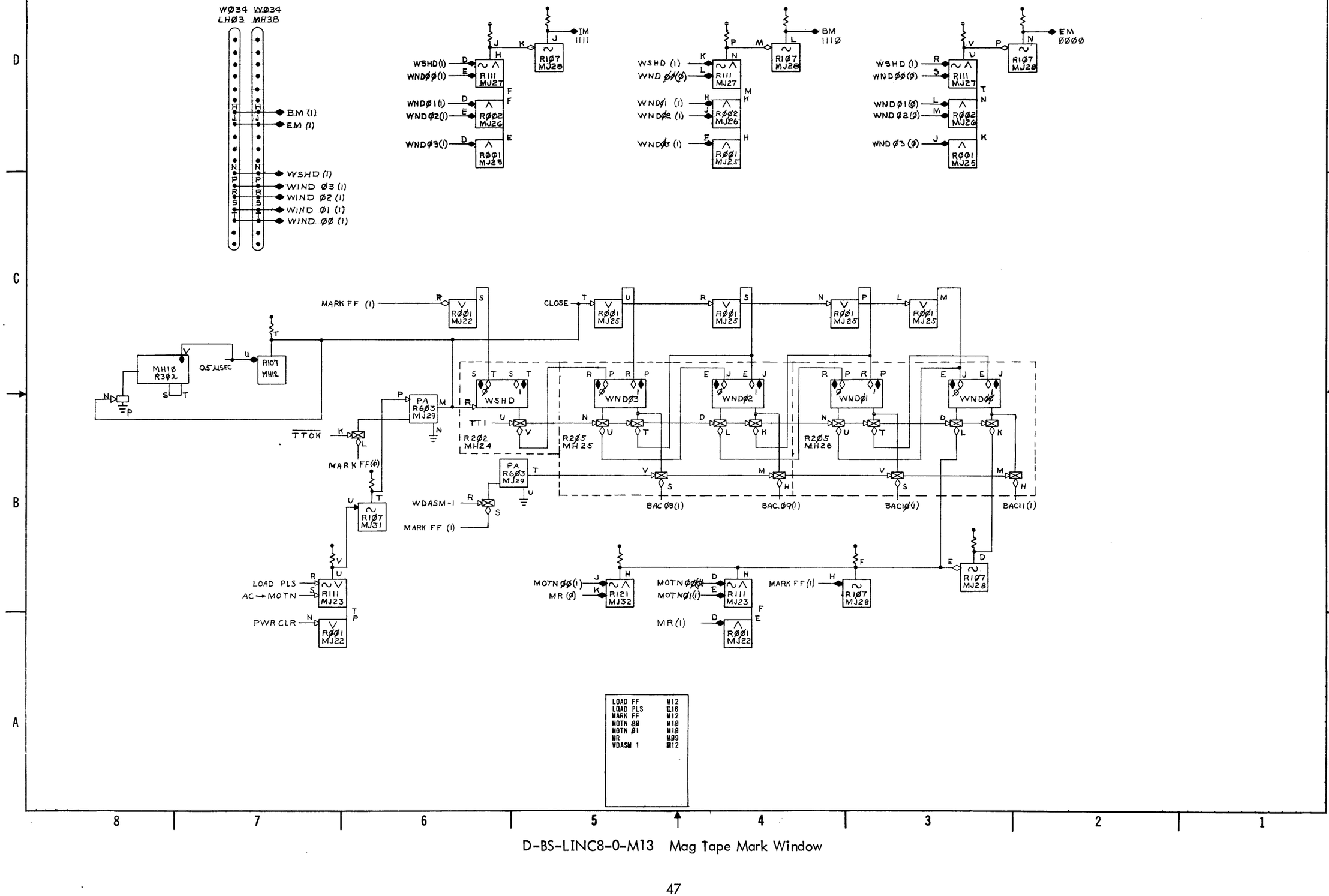


D-BS-LINC8-0-M11 Mag Tape Timing Generator

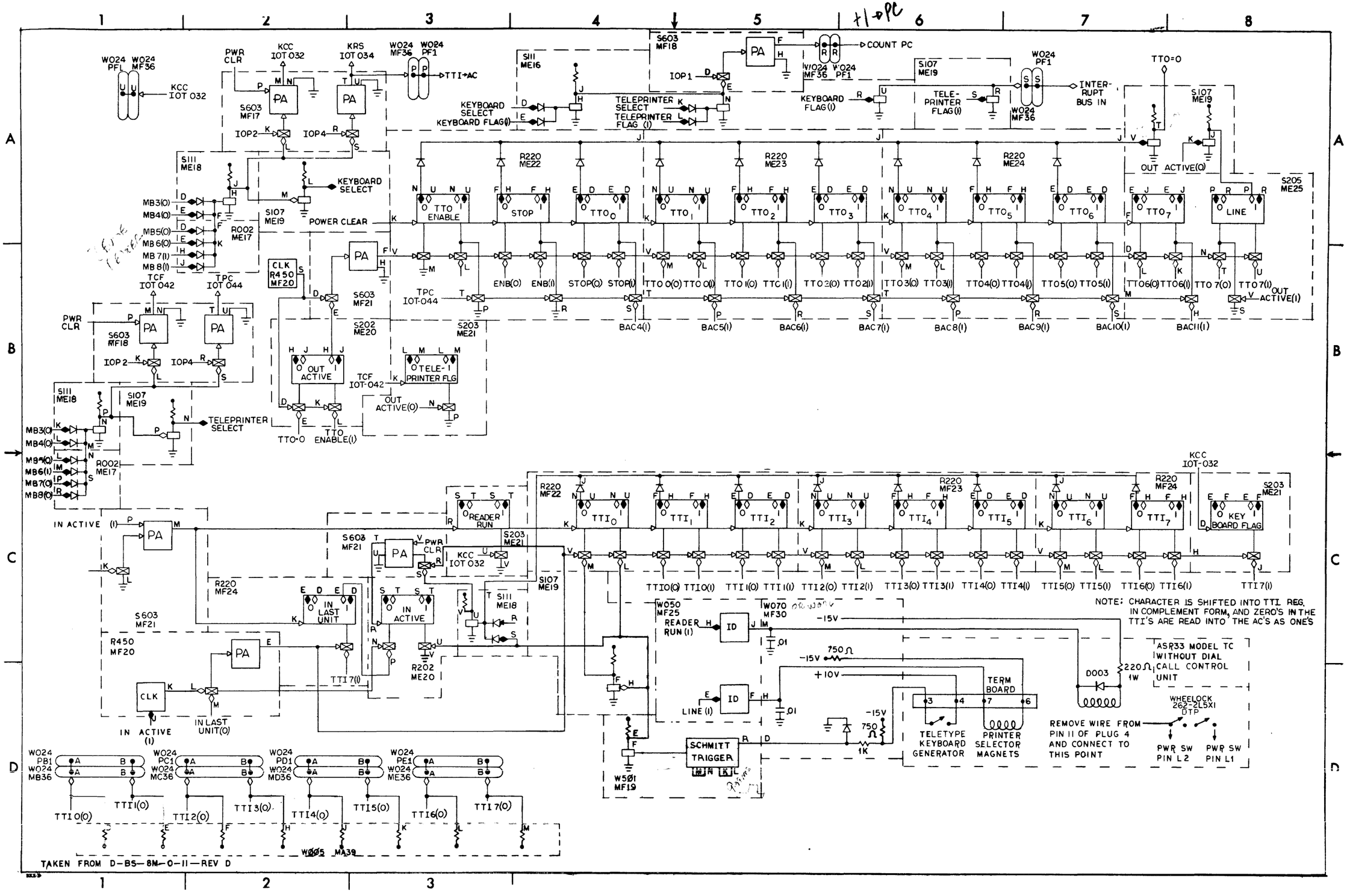


AC TO FF	L17	P TO S	L21
AC TO MOTN	L17	PWR CLR	L16
BAD TO AD	M13	SET SRCH	L17
CLOSE	M13	Ø TO FF	L17
END LOAD	L21	Ø TO MOTN	L17
LOAD	L28		
LOAD PLS	L16		
MARK	L16		
OFF SRCH	L17		
OFF WRITE	L17		
ON BLOCK	L17		
ON WRITE	L17		

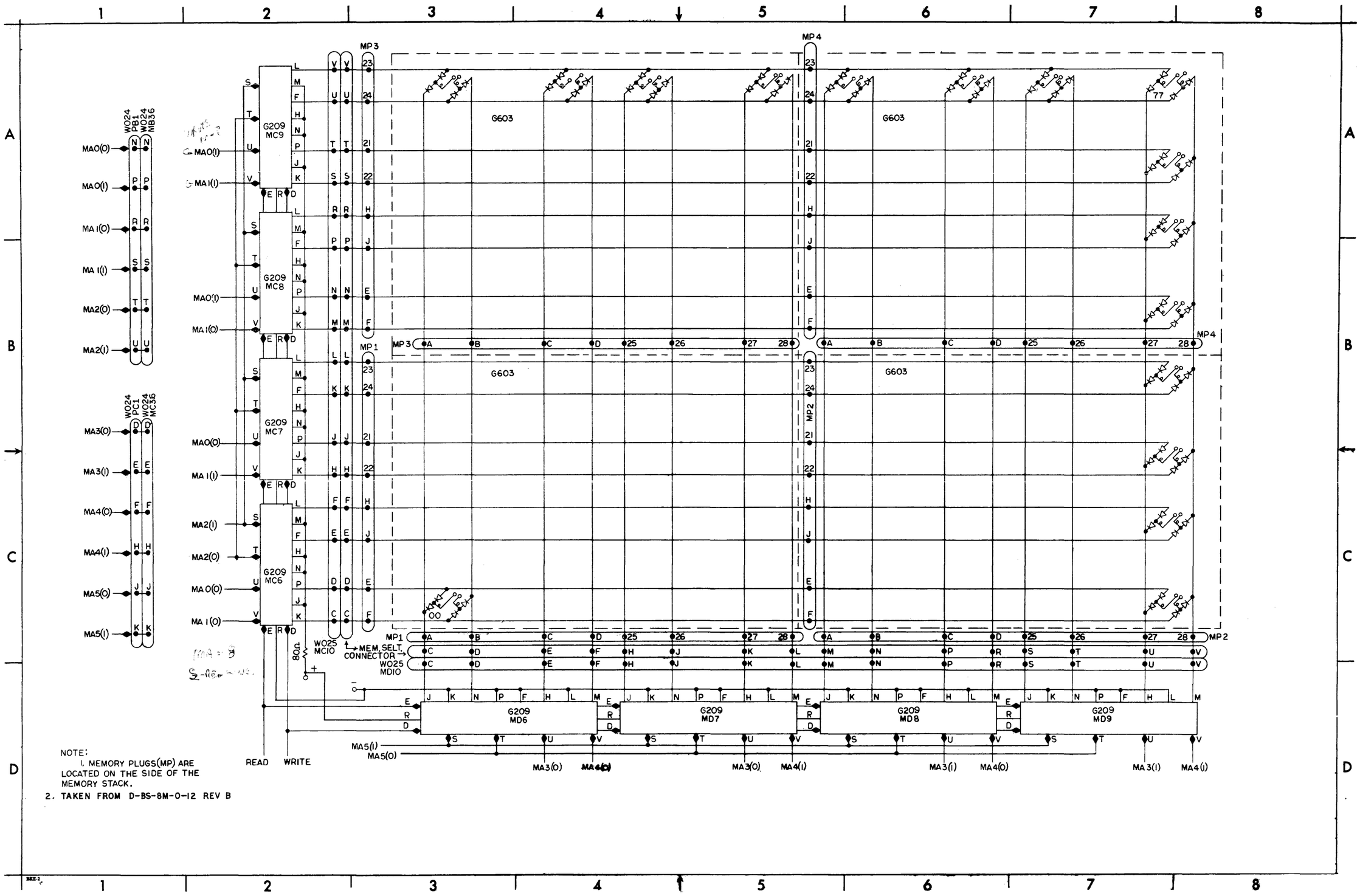
D-BS-LINC8-0-M12 Mag Tape Mode Control



D-BS-LINC8-0-M13 Mag Tape Mark Window

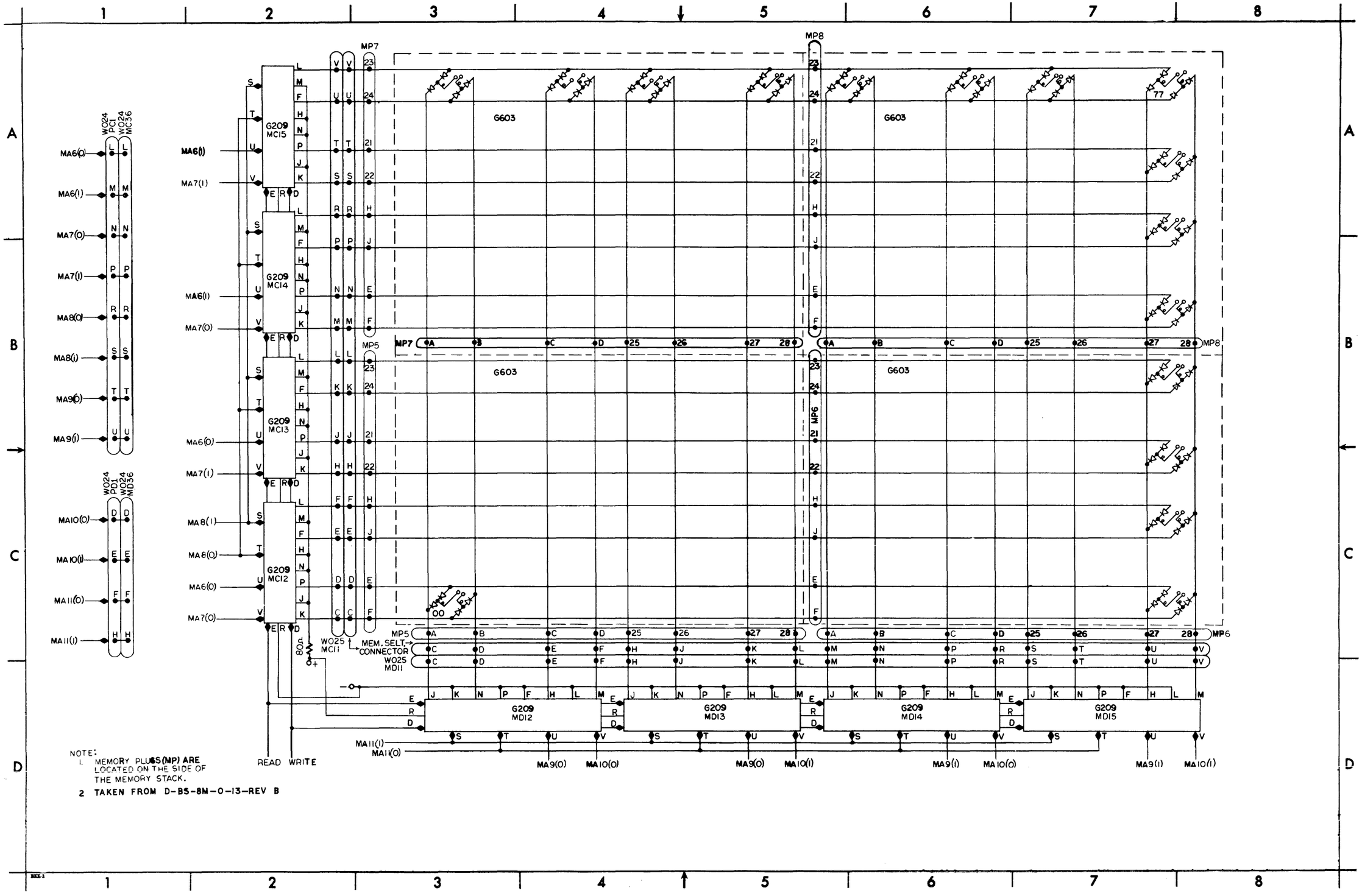


D-BS-LINC8-0-M111 Teleprinter

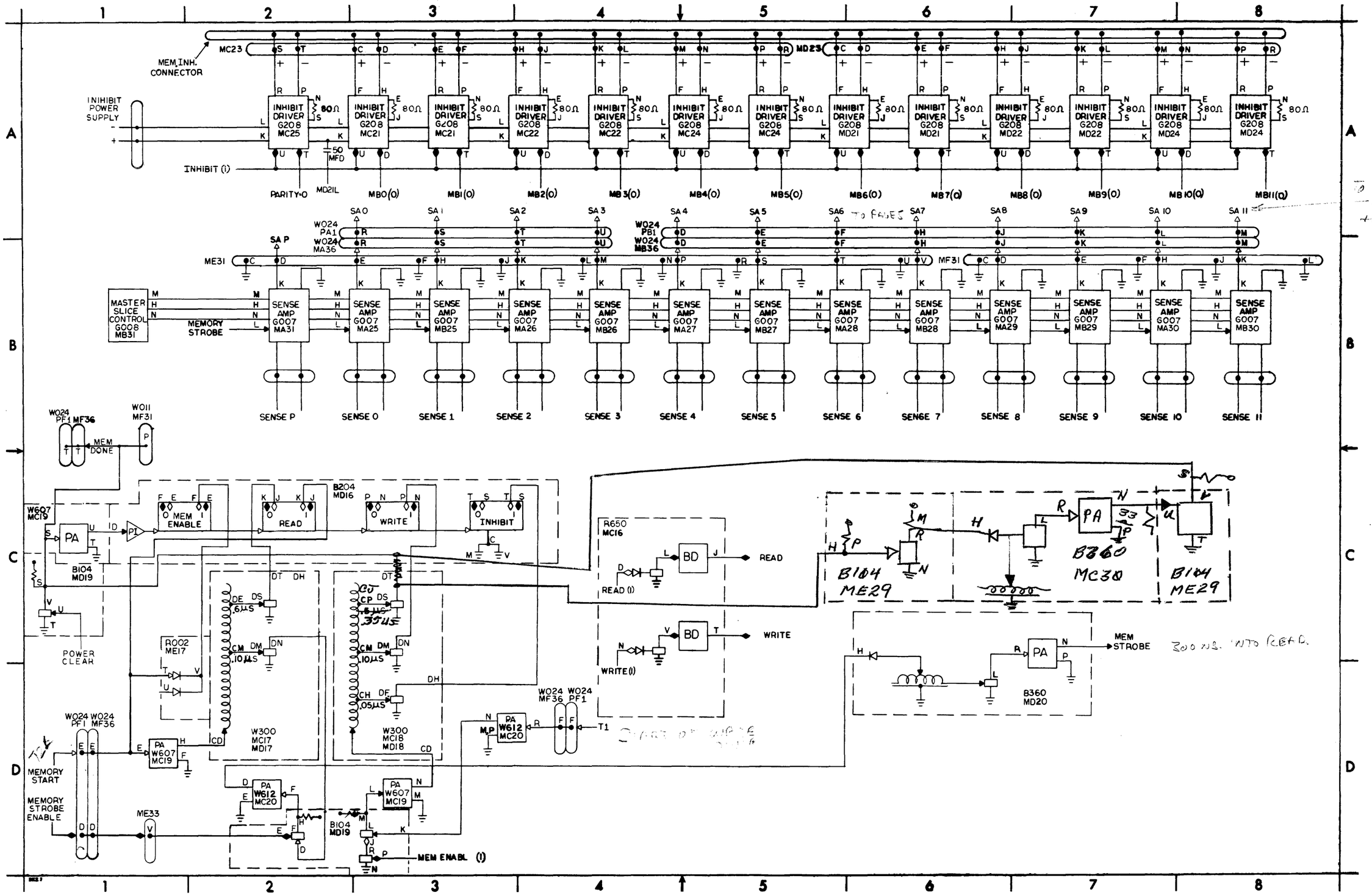


NOTE:
1. MEMORY PLUGS(MP) ARE LOCATED ON THE SIDE OF THE MEMORY STACK.
2. TAKEN FROM D-BS-8M-0-12 REV B

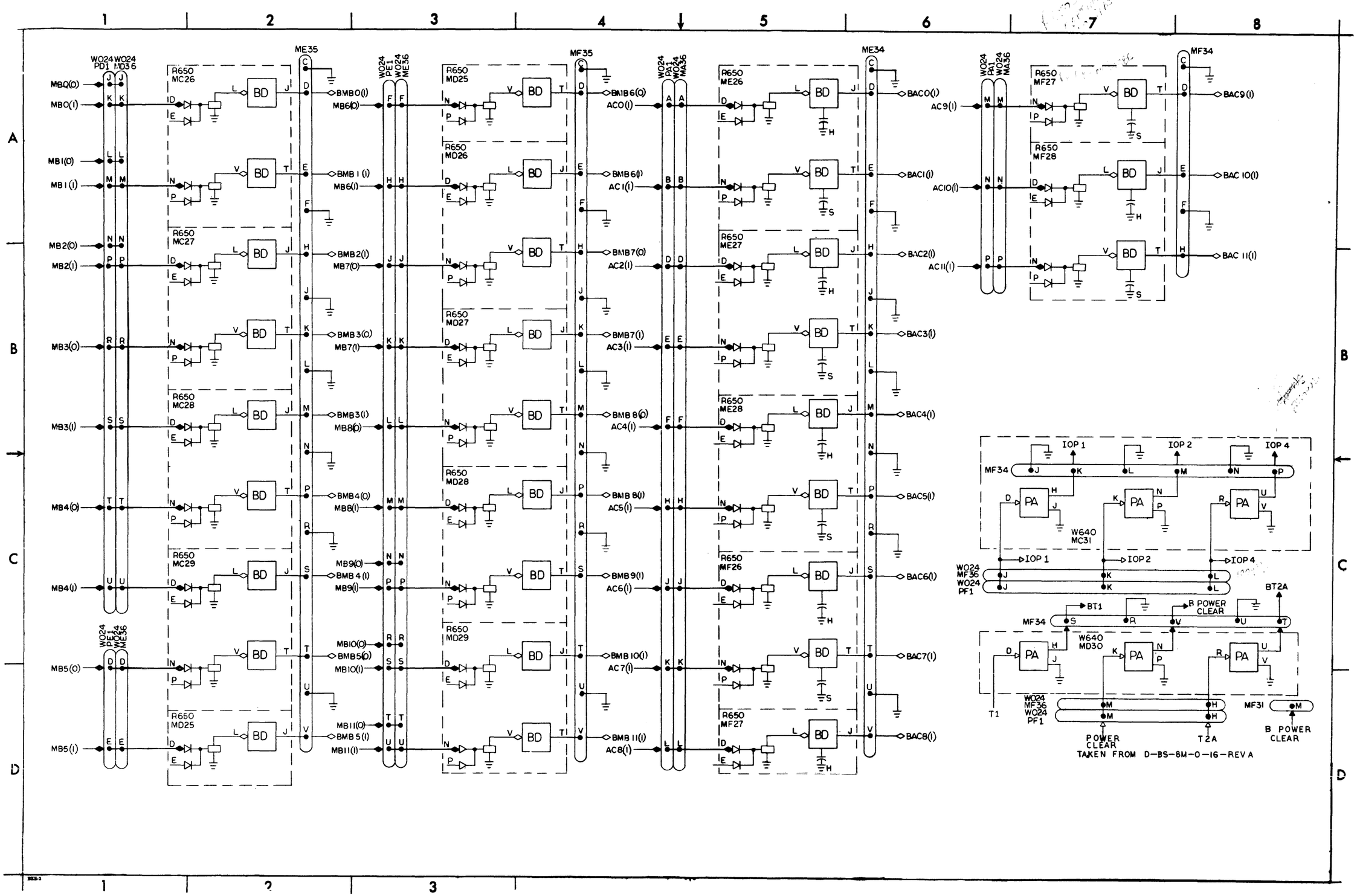
D-BS-LINC8-0-M112 X-Axis Selection



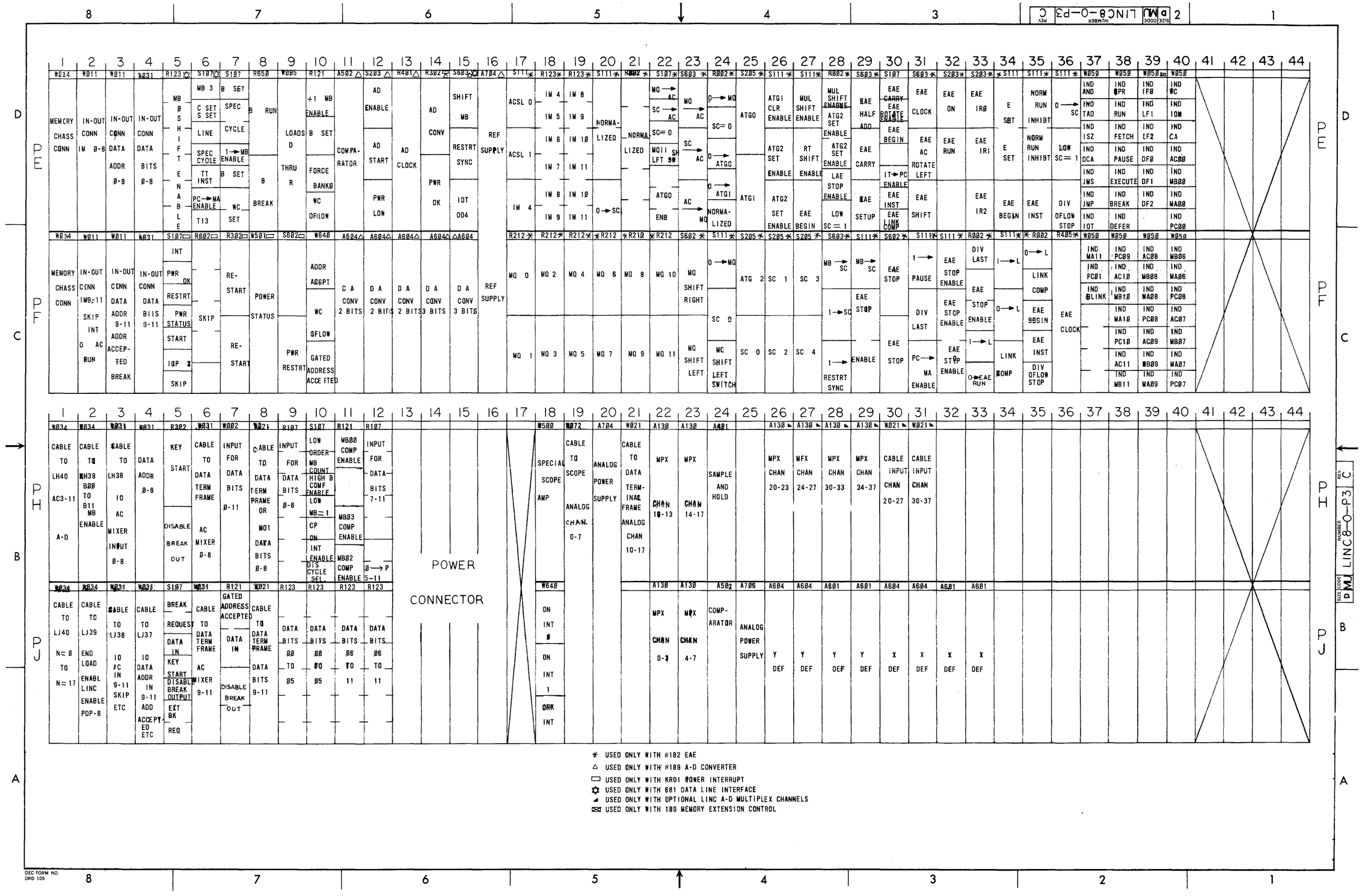
D-BS-LINC8-0-M113 Y-Axis Selection



D-BS-LINC8-0-M115 Sense Amps, Inhibit Drivers, Mem. Cont.

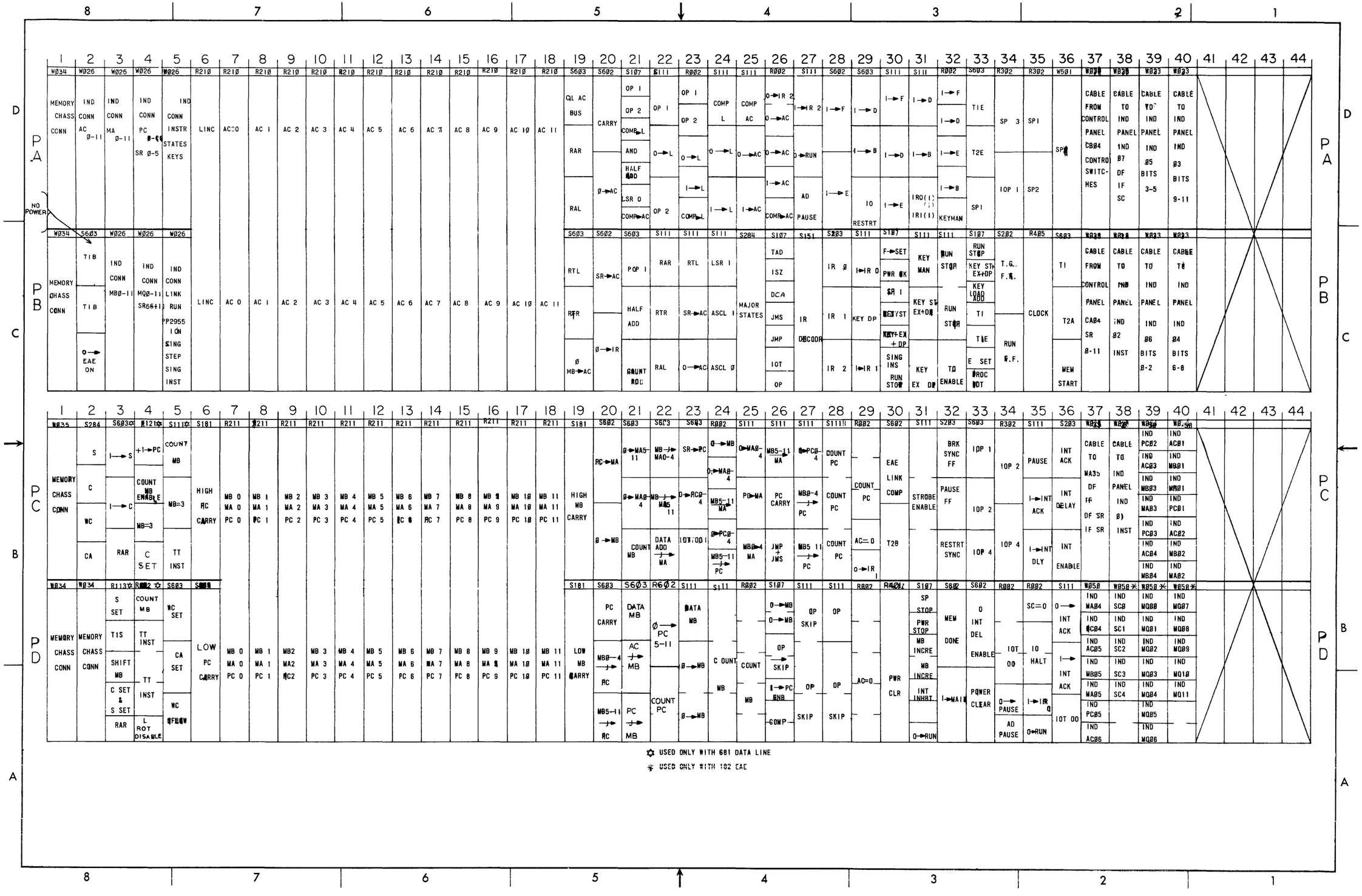


D-BS-LINC8-0-M116 In Out Buffers

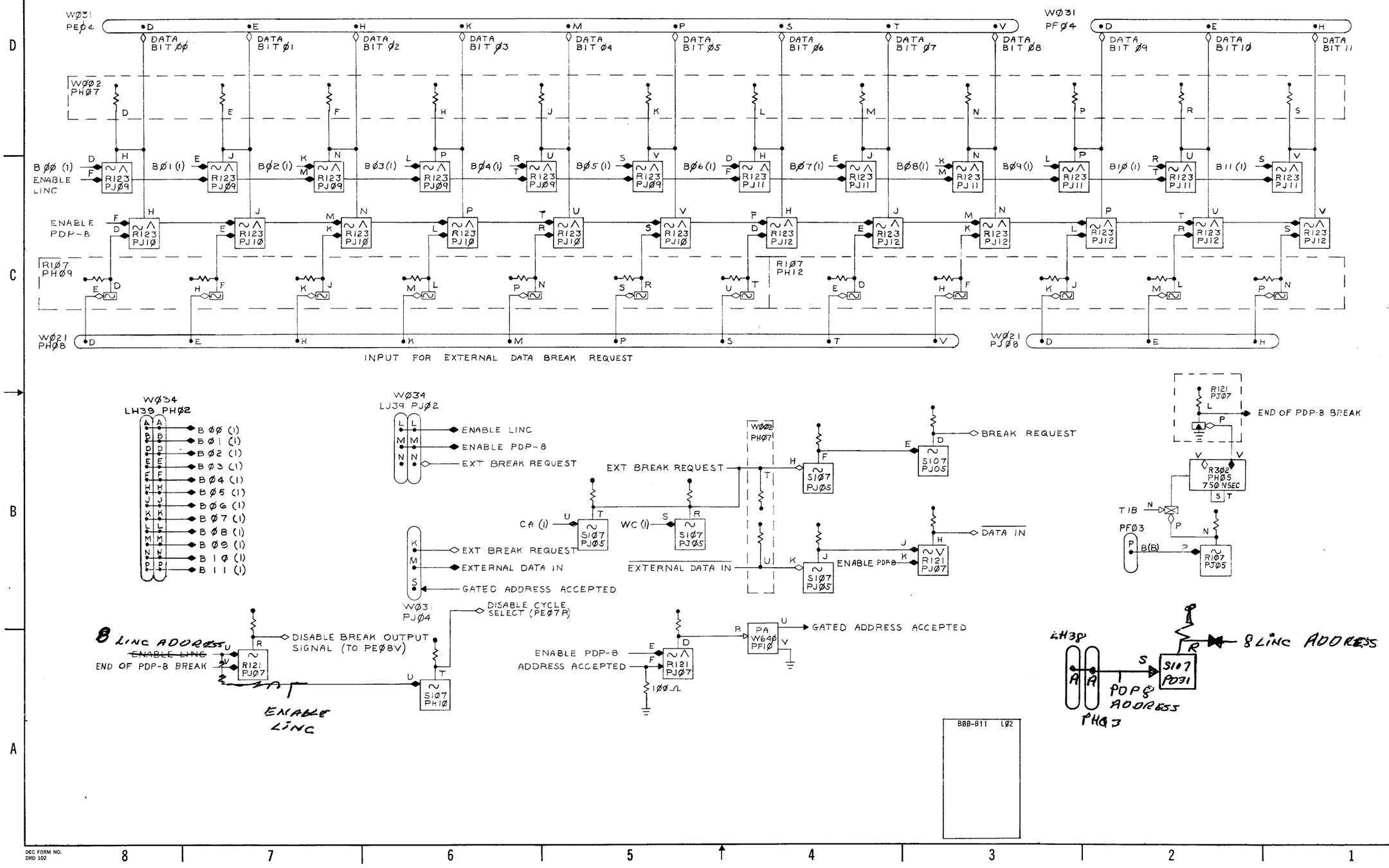


DEC FORM NO. DRD 105

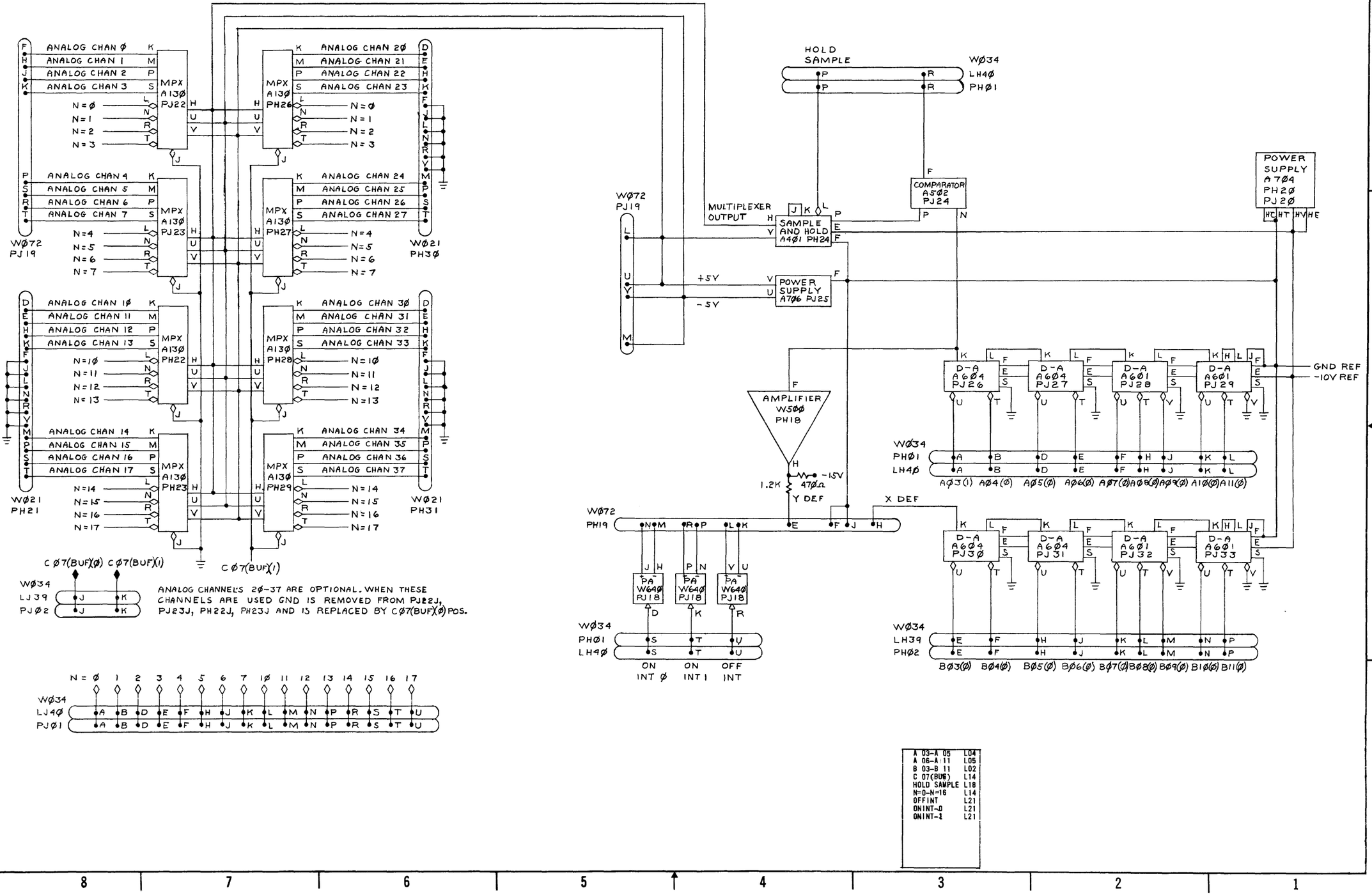
D-MU-LINC8-0-P3 LINC8 UML, PE-PJ



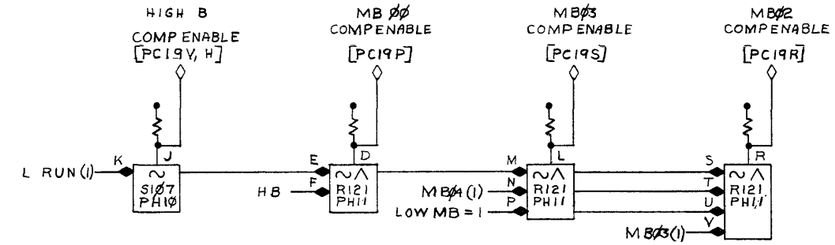
D-MU-LINC8-0-P4 LINC8 UML, PA-PD

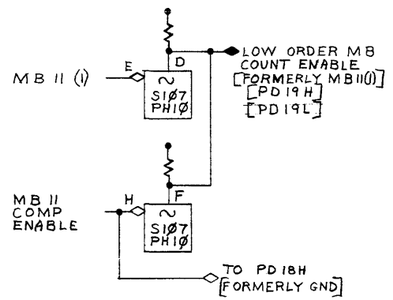


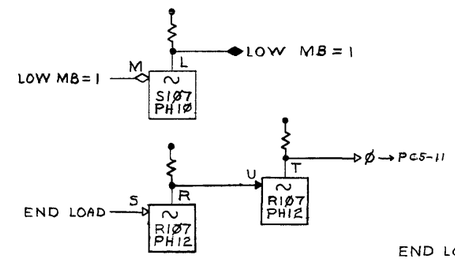
D-BS-LINC8-0-P23 Data Bits, 00-11 Gates

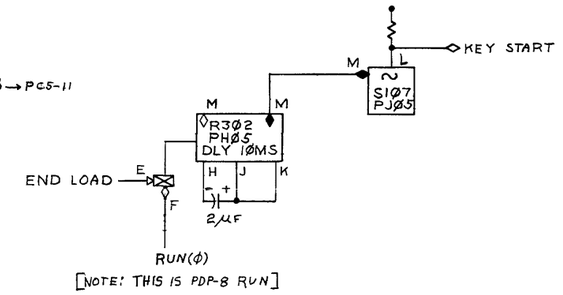


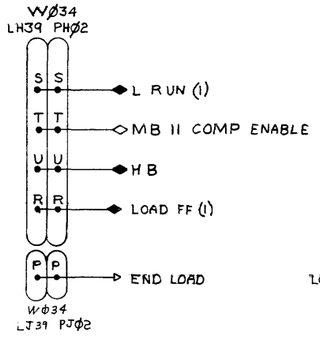
D-BS-LINC8-0-P24 Analog System

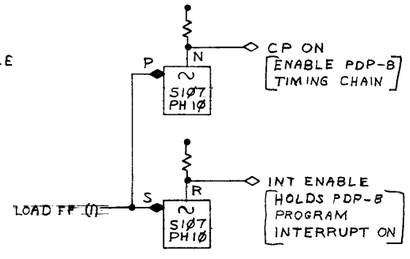












END LOAD	L21
HB	L18
L RUN	L16
MB 11 COMP ENABLE	L18

D-BS-LINC8-0-P25 MB & Load Mods in PDP-8

ALL INDICATOR INPUTS COMING FROM FLIP FLOPS COME FROM THE 1 NEG SIDE. (I.E. AØØ(1)—●)

W05Ø PE4Ø: WC, INT ENABLE, CA, AC ØØ, MB ØØ, MA ØØ, PC ØØ → IND WC, IND ION, IND CA, IND ACØØ, IND MBØØ, IND MAØØ, IND PCØØ

W05Ø PC4Ø: ACØ1, MBØ1, MAØ1, PCØ1, ACØ2, MBØ2, MAØ2 → IND ACØ1, IND MBØ1, IND MAØ1, IND PCØ1, IND ACØ2, IND MBØ2, IND MAØ2

W05Ø PC39: PCØ2, ACØ3, MBØ3, MAØ3, PCØ3, ACØ4, MBØ4 → IND PCØ2, IND ACØ3, IND MBØ3, IND MAØ3, IND PCØ3, IND ACØ4, IND MBØ4

W05Ø PD37: MAØ4, PCØ4, ACØ5, MBØ5, MAØ5, PCØ5, ACØ6 → IND MAØ4, IND PCØ4, IND ACØ5, IND MBØ5, IND MAØ5, IND PCØ5, IND ACØ6

W05Ø PF4Ø: MBØ6, MAØ6, PCØ6, ACØ7, MBØ7, MAØ7, PCØ7 → IND MBØ6, IND MAØ6, IND PCØ6, IND ACØ7, IND MBØ7, IND MAØ7, IND PCØ7

W05Ø PF39: ACØ8, MBØ8, MAØ8, PCØ8, ACØ9, MBØ9, MAØ9 → IND ACØ8, IND MBØ8, IND MAØ8, IND PCØ8, IND ACØ9, IND MBØ9, IND MAØ9

W05Ø PF38: PCØ9, AC1Ø, MB1Ø, MA1Ø, PC1Ø, AC 11, MB11 → IND PCØ9, IND AC1Ø, IND MB1Ø, IND MA1Ø, IND PC1Ø, IND AC 11, IND MB11

W05Ø PF37: MA11, PC 11, LINK → IND MA11, IND PC 11, IND 8 LINC

W05Ø PE37: AND, TAD, ISZ, DCA, JMS, JMP, IOT → IND AND, IND TAD, IND ISZ, IND DCA, IND JMS, IND JMP, IND IOT

W05Ø PE38: OPR, RUN, FETCH, PAUSE, EXECUTE, BREAK, DEFER → IND OPR, IND RUN, IND FETCH, IND PAUSE, IND EXECUTE, IND BREAK, IND DEFER

W05Ø PE39: IF Ø, IF 1, IF 2, DF Ø, DF 1, DF 2 → IND IF Ø, IND IF 1, IND IF 2, IND DF Ø, IND DF 1, IND DF 2

W05Ø PD39: MQ ØØ, MQØ1, MQØ2, MQØ3, MQØ4, MQØ5, MQØ6 → IND MQ ØØ, IND MQØ1, IND MQØ2, IND MQØ3, IND MQØ4, IND MQ Ø5, IND MQ Ø6

W05Ø PD4Ø: MQØ7, MQØ8, MQØ9, MQ1Ø, MQ11 → IND MQØ7, IND MQØ8, IND MQØ9, IND MQ1Ø, IND MQ11

W05Ø PD38: SC Ø, SC1, SC2, SC3, SC4 → IND SC Ø, IND SC 1, IND SC 2, IND SC 3, IND SC4

W033 PA38 IND Ø7: PWR −15V, GND, IND 8 LINC, IND IF 2, IND DF Ø, IND SC 4, IND SC Ø, IND IF 1, IND DF 1, IND SC 3, IND SC 1, IND IF Ø, IND DF 2, IND SC 2

W033 PB39 IND Ø6: IND MQØ2, IND PCØØ, IND ACØ2, IND MAØØ, IND MBØ2, IND MBØØ, IND MAØ2, IND ACØØ, IND PCØ2, IND MQØØ, IND MQØ1, IND PCØ1, IND ACØ1, IND MAØ1, IND MBØ1

W033 PA39 IND Ø5: IND MQØ5, IND PCØ3, IND AC Ø5, IND MAØ3, IND MBØ5, IND MBØ3, IND MAØ5, IND ACØ3, IND PCØ5, IND MQØ3, IND MQØ4, IND PCØ4, IND ACØ4, IND MAØ4, IND MBØ4

W033 PB4Ø IND Ø4: IND MQØ8, IND PCØ6, IND ACØ8, IND MAØ6, IND MBØ8, IND MBØ6, IND MAØ8, IND ACØ6, IND PCØ8, IND MQØ6, IND MQØ7, IND PCØ7, IND ACØ7, IND MAØ7, IND MBØ7

W033 PA4Ø IND Ø3: IND MQ11, IND PCØ9, IND AC11, IND MAØ9, IND MB11, IND MBØ9, IND MA11, IND ACØ9, IND PC 11, IND MAØ9, IND MQ11, IND PC 1Ø, IND AC 1Ø, IND MA1Ø, IND MB1Ø

W033 PB38 IND Ø2: IND AND, IND OPR, IND TAD, IND IOT, IND ISZ, IND JMP, IND DCA, IND JMS

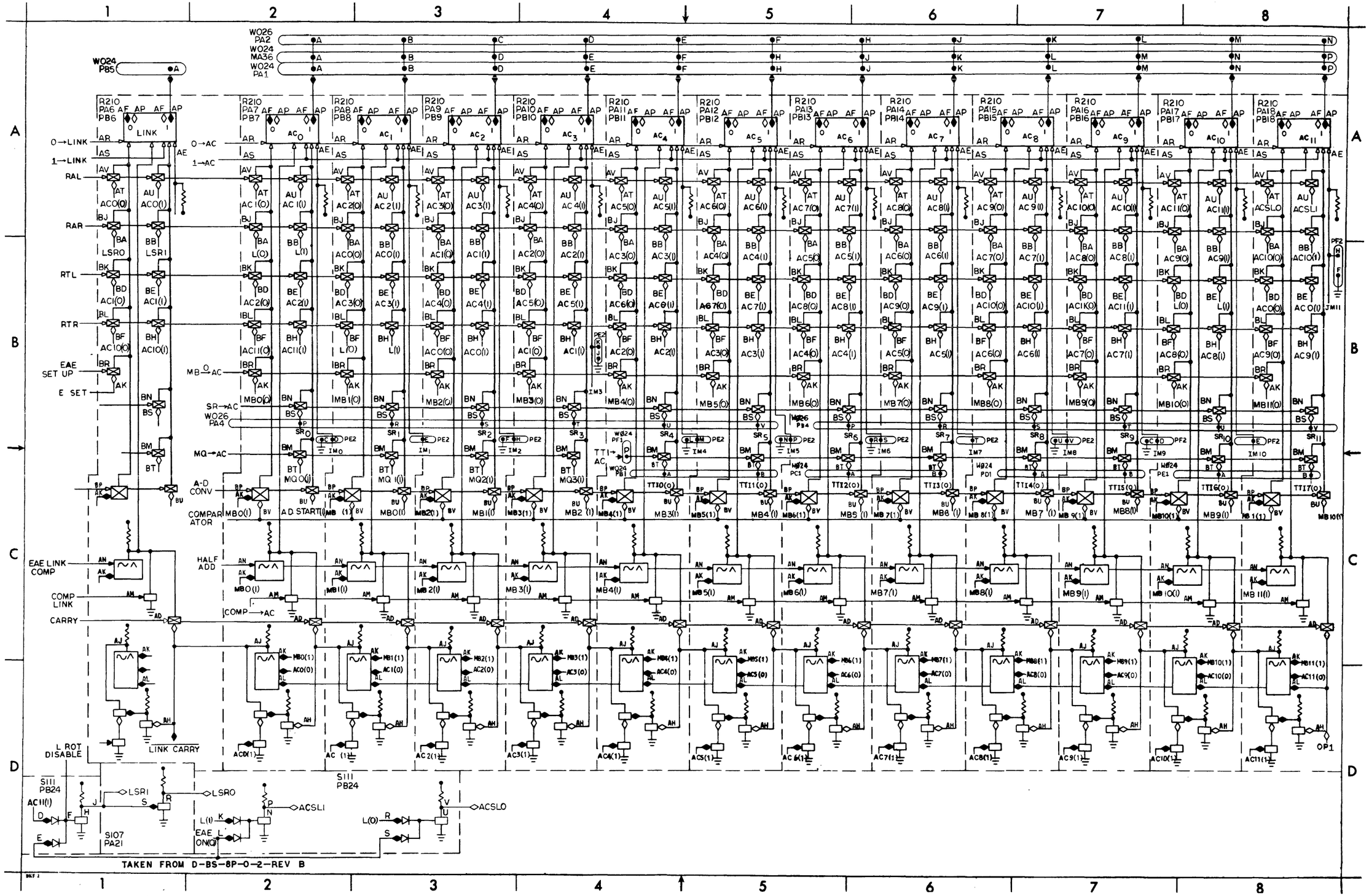
W033 PC38 IND Ø1: IND RUN, IND FETCH, IND PAUSE, IND EXECUTE, IND BREAK, IND DEFER, IND WC, IND ION, IND CA

W033 PB37 CAØ4: SRØØ, SRØ1, SRØ2, SRØ3, SRØ4, SRØ5, SRØ6, SRØ7, SRØ8, SRØ9, SR1Ø, SR 11

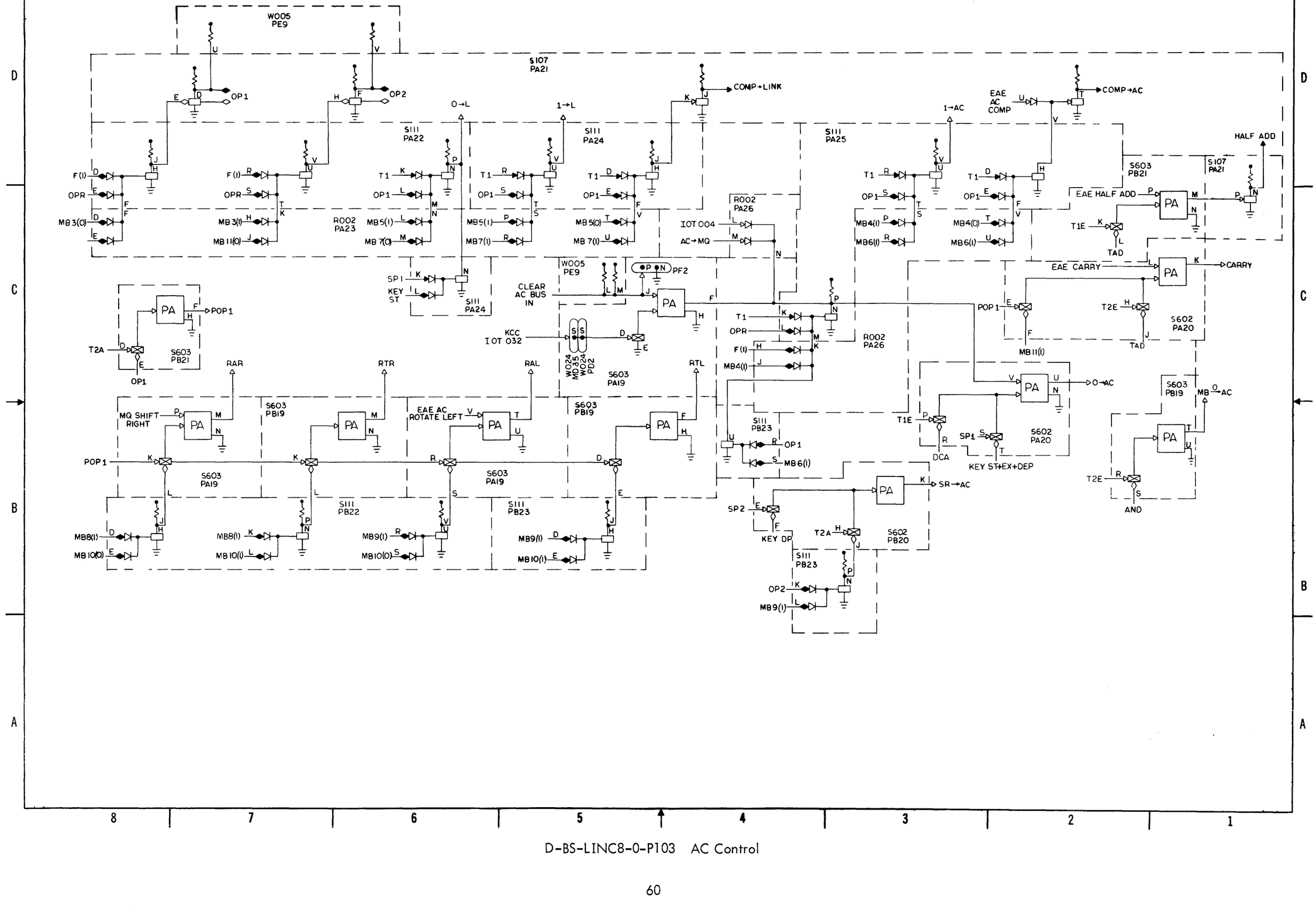
W033 PA37 CBØ4: KEY LOAD ADDR, KEY DP, KEY EX, KEY CONT, RUN STOP, KEY START, RUN STOP, SINGLE INST, DF SRØ, DF SR 1, DF SR 2, IF SRØ, IF SR 1, IF SR 2

W033 PC37 MA35: DF Ø, DF 1, DF 2, IF Ø, IF 1, IF 2, DF SRØ, DF SR1, DF SR 2, IF SRØ, IF SR 1, IF SR 2

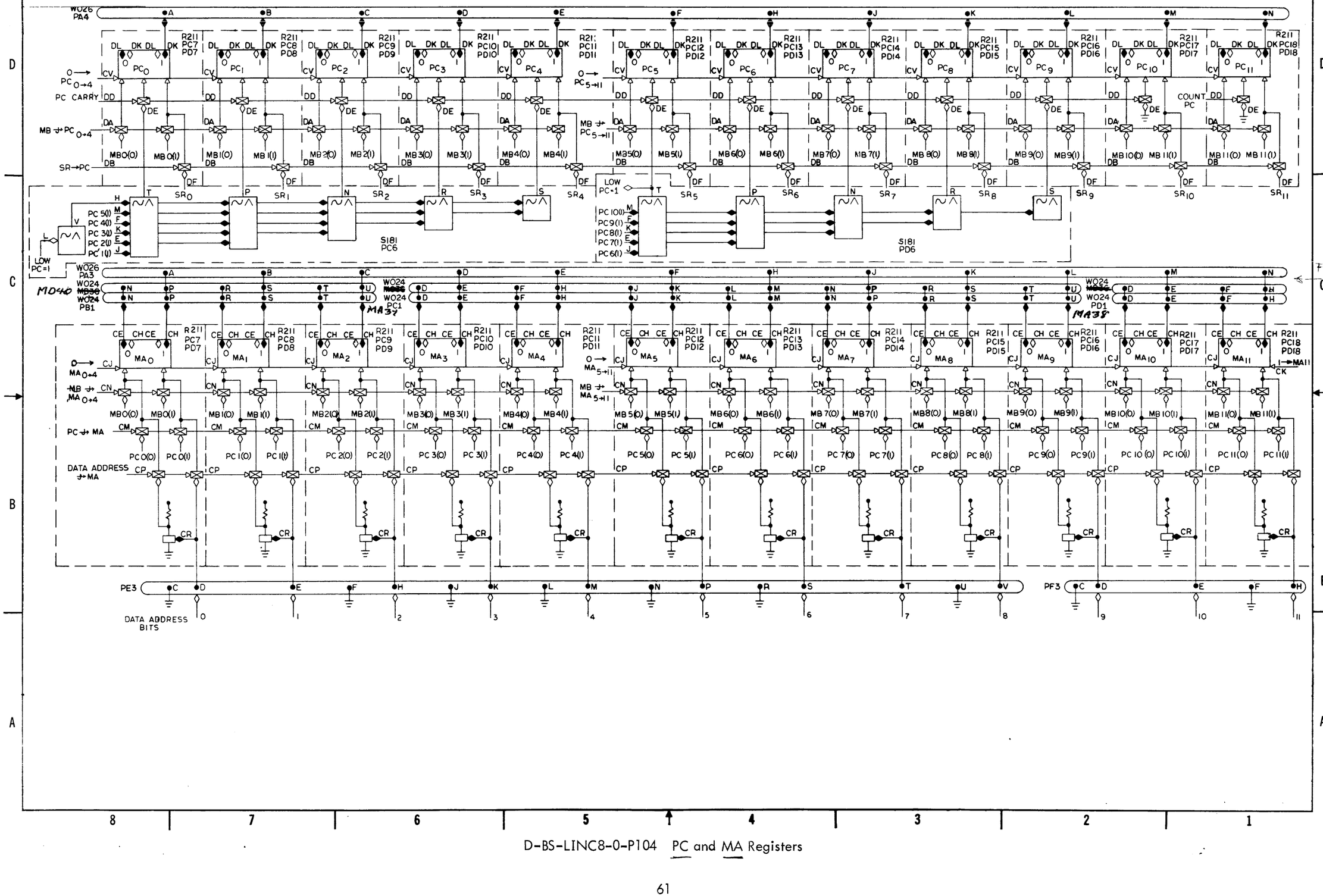
D-BS-LINC8-0-P27 PDP-8 Switches and Indicators



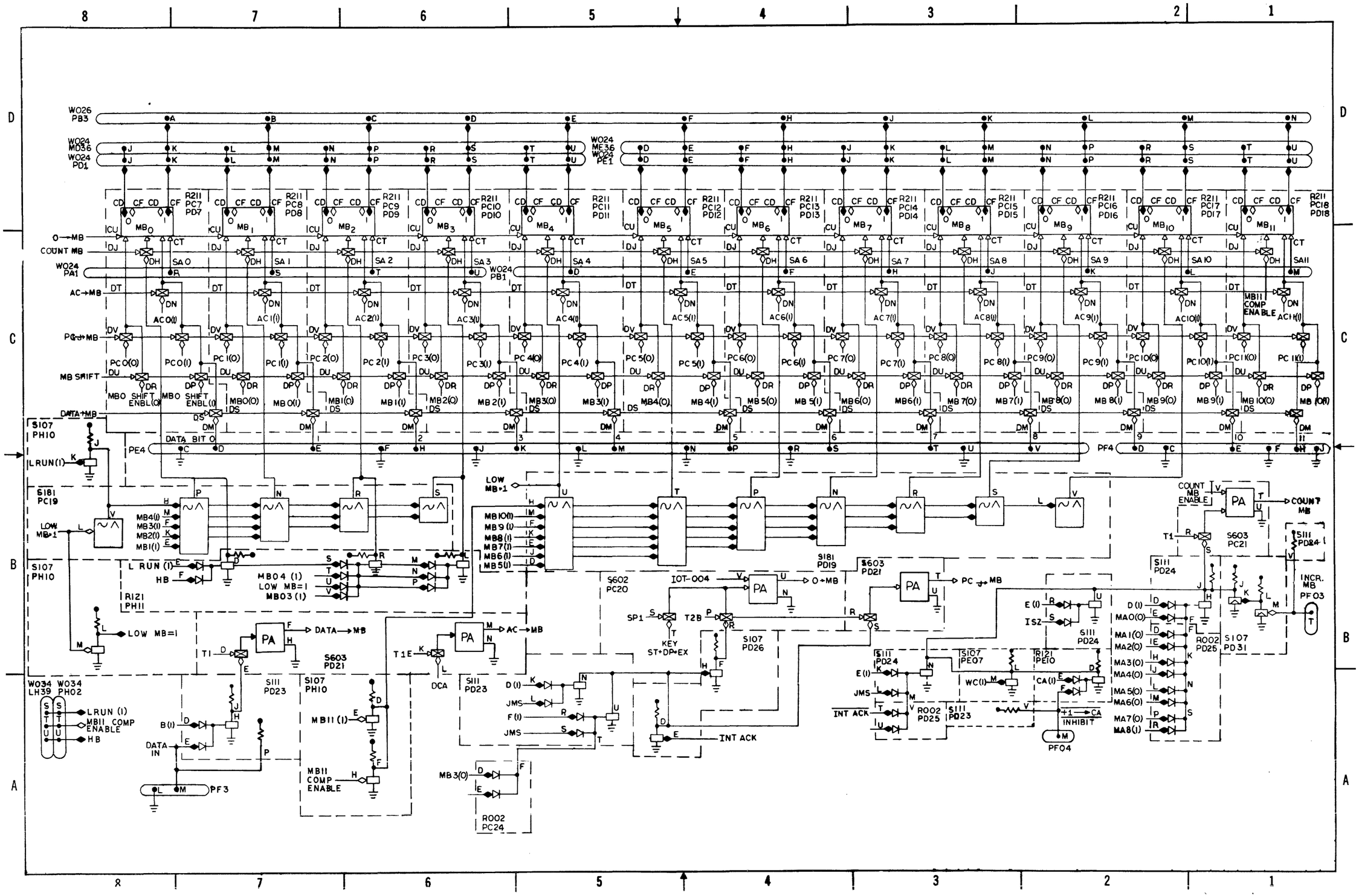
D-BS-LINC8-0-P102 Accumulator



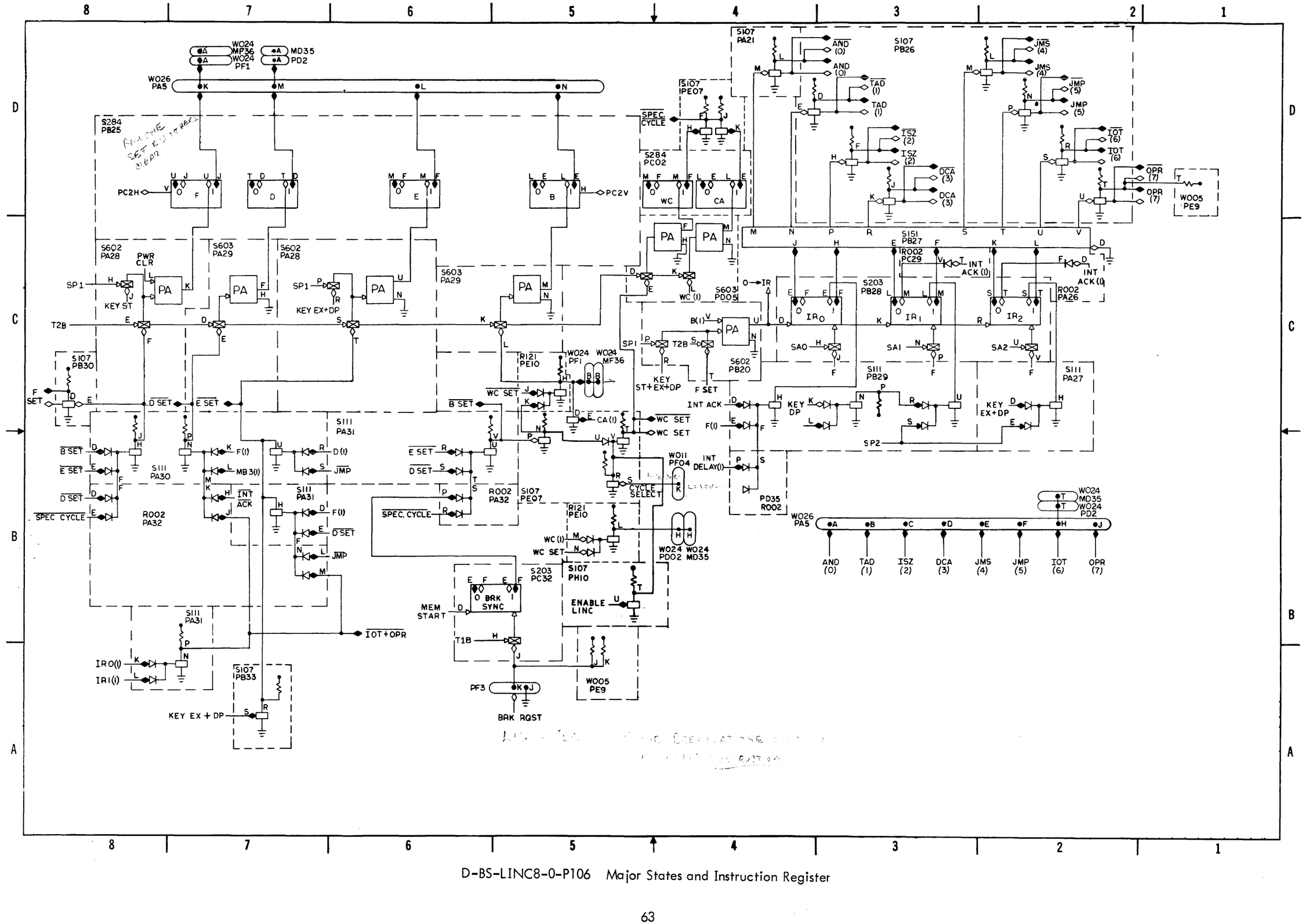
D-BS-LINC8-0-P103 AC Control



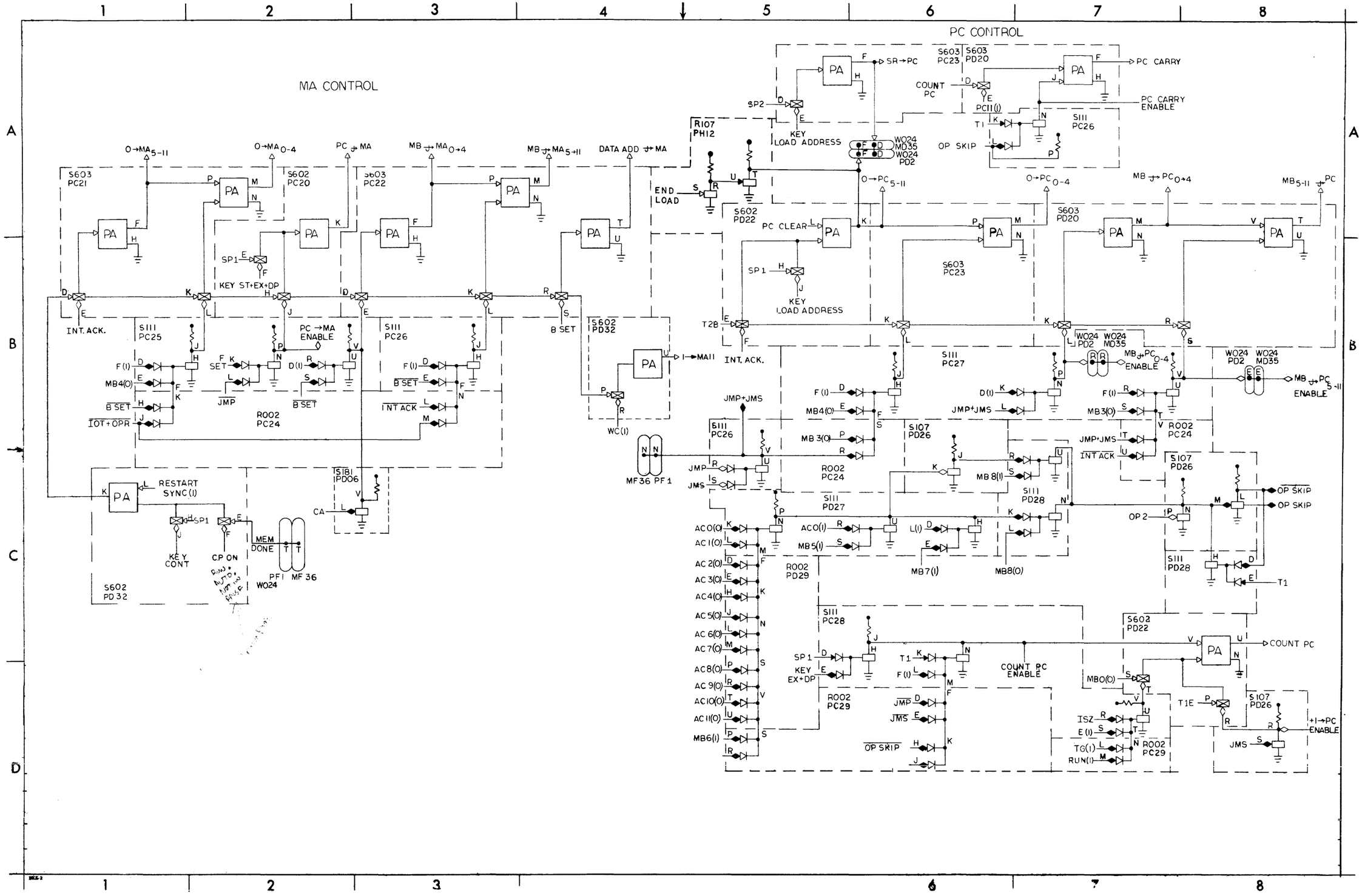
D-BS-LINC8-0-P104 PC and MA Registers



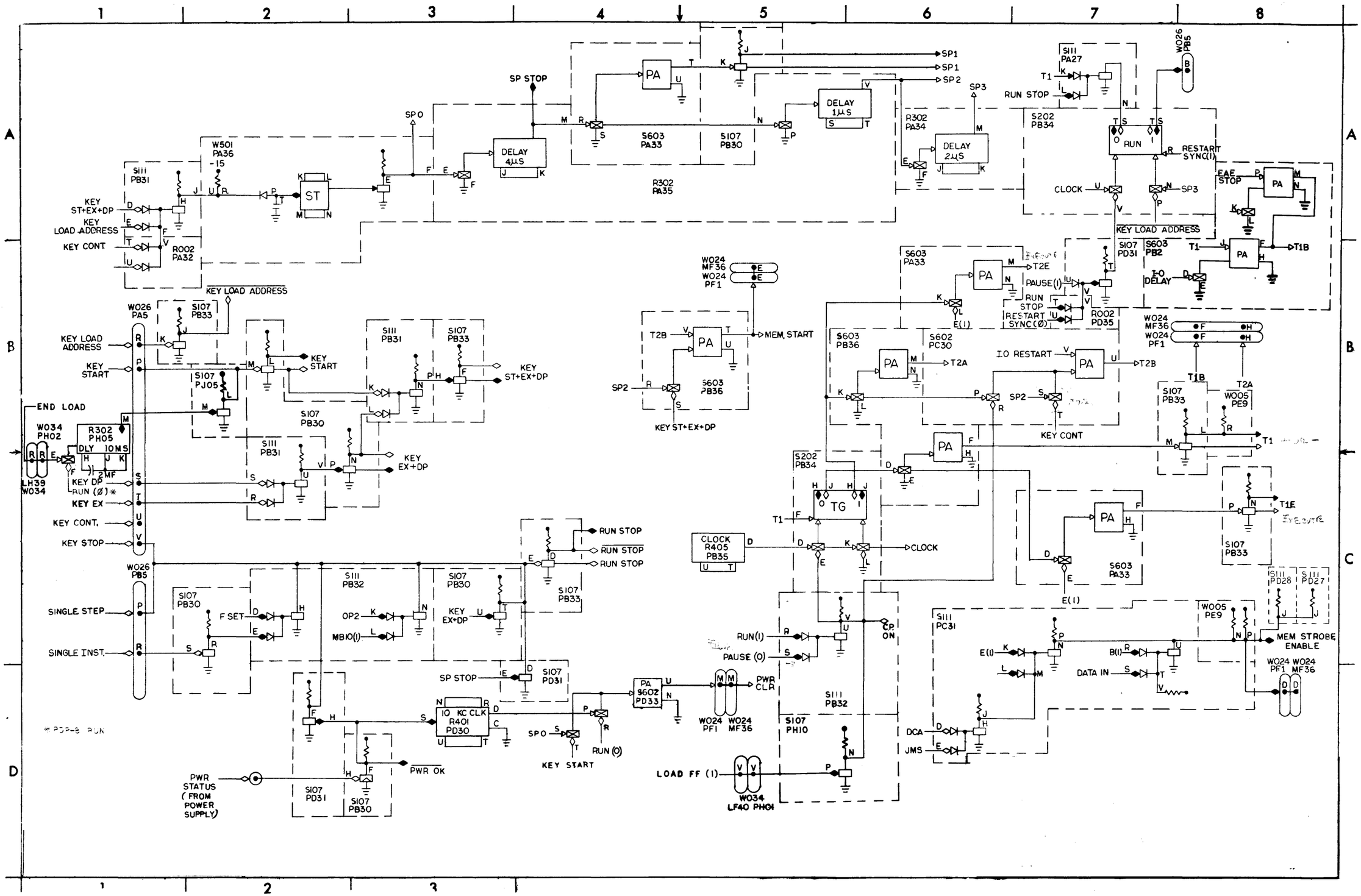
D-BS-LINC8-0-P105 MB Register and Control



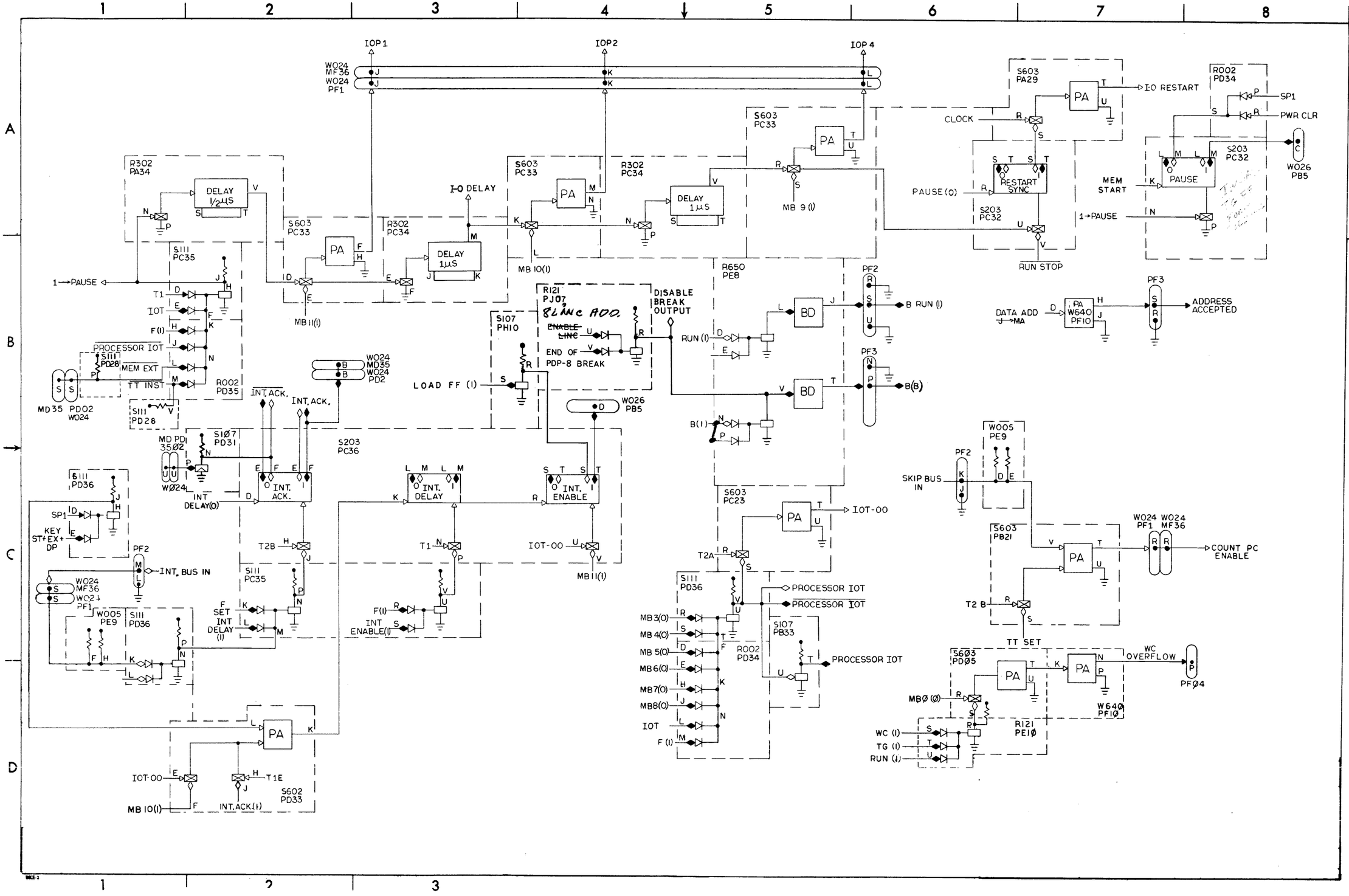
D-BS-LINC8-0-P106 Major States and Instruction Register



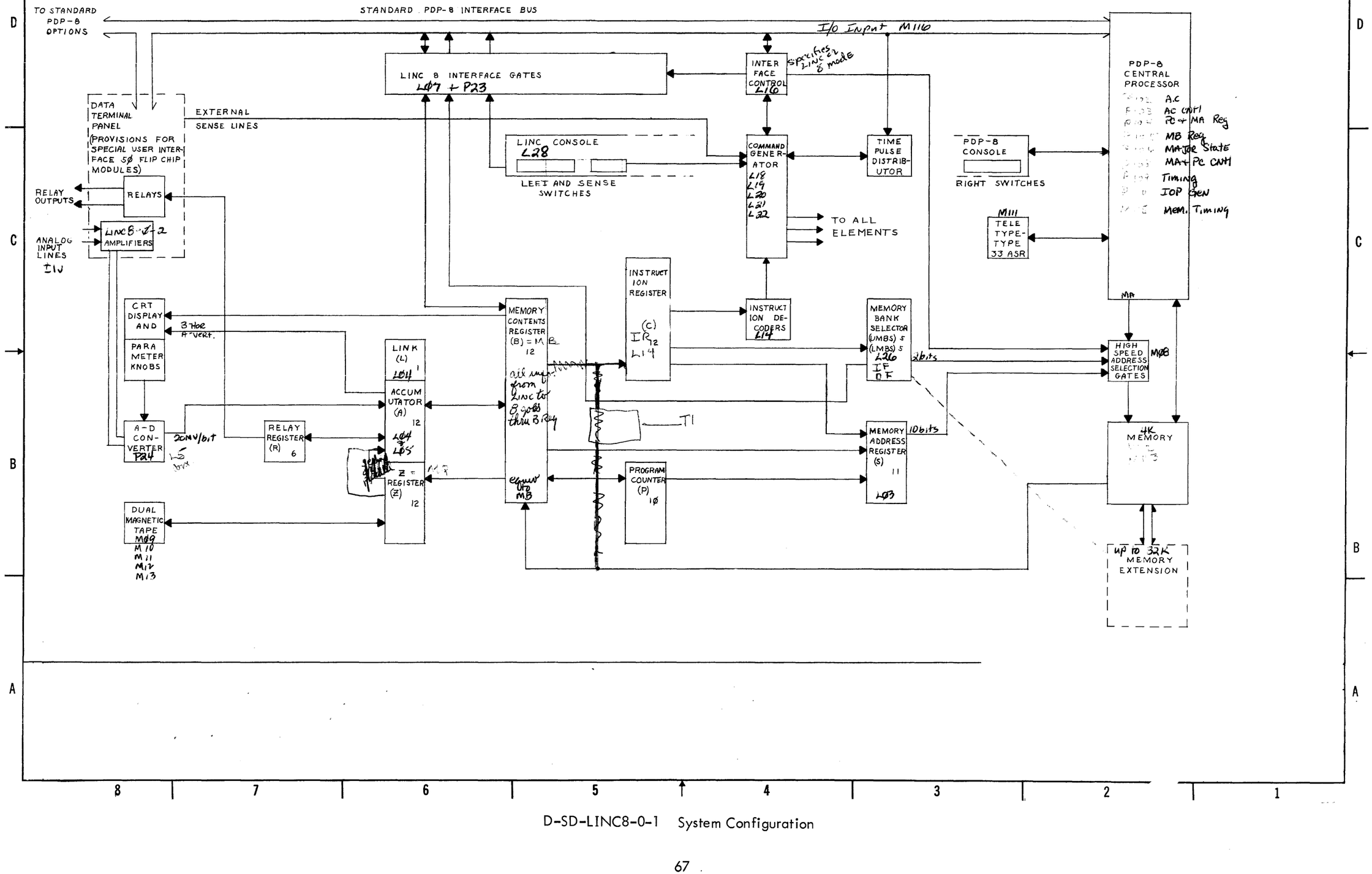
D-BS-LINC8-0-P108 MA, PC Control



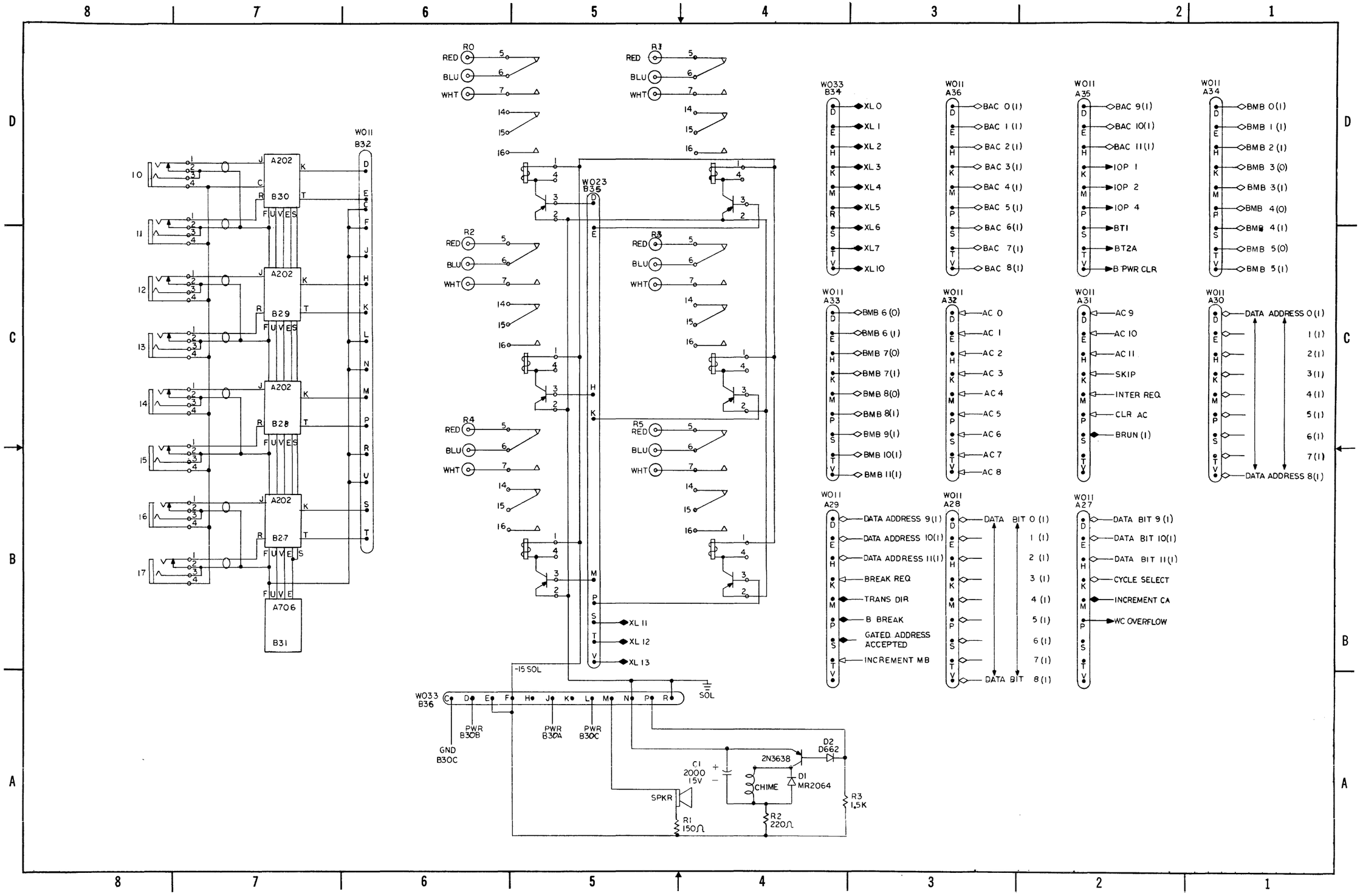
D-BS-LINC8-0-P109 Timing Keys, SWS and Run



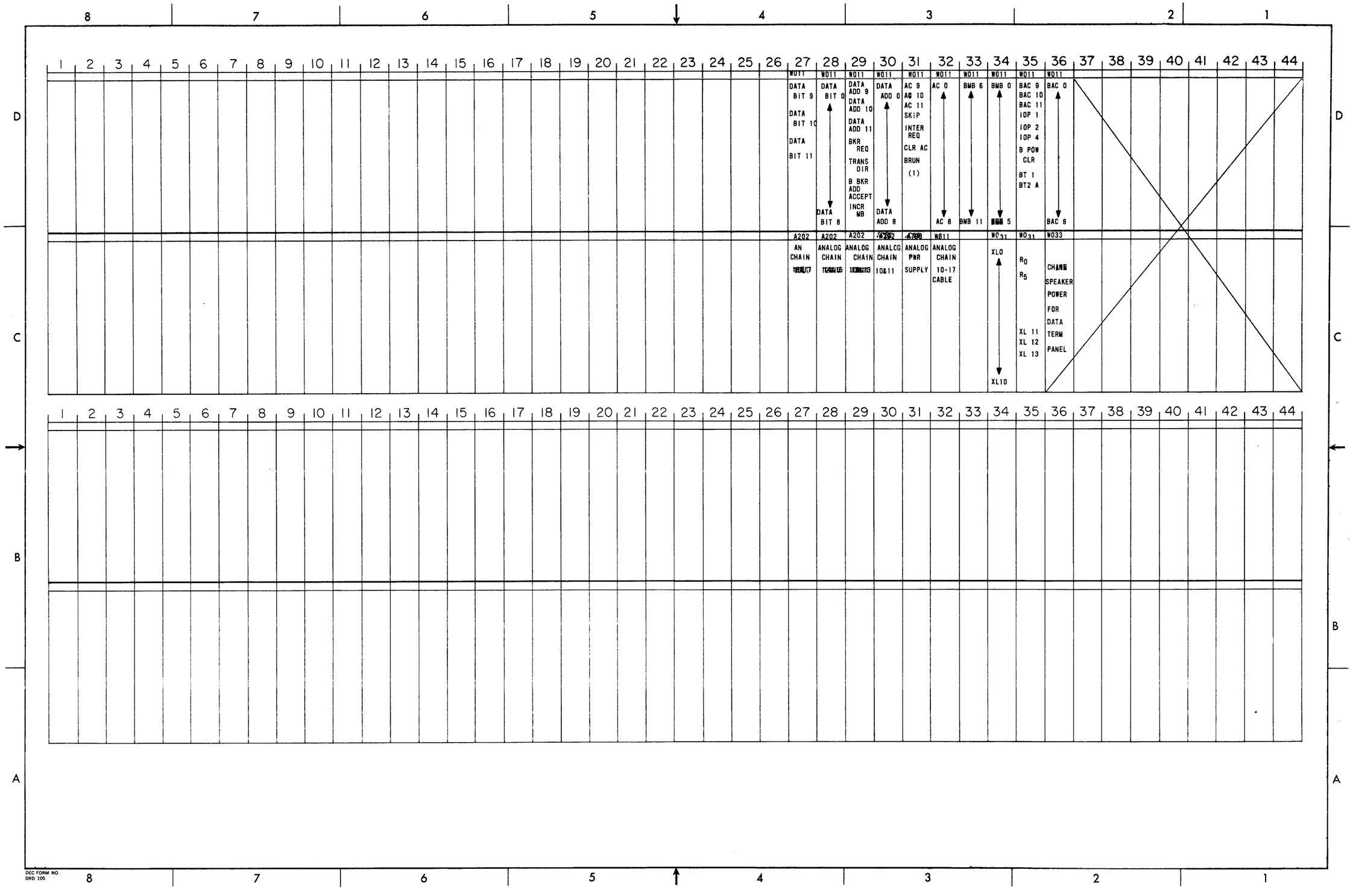
D-BS-LINC8-0-P110 Input/Output Control



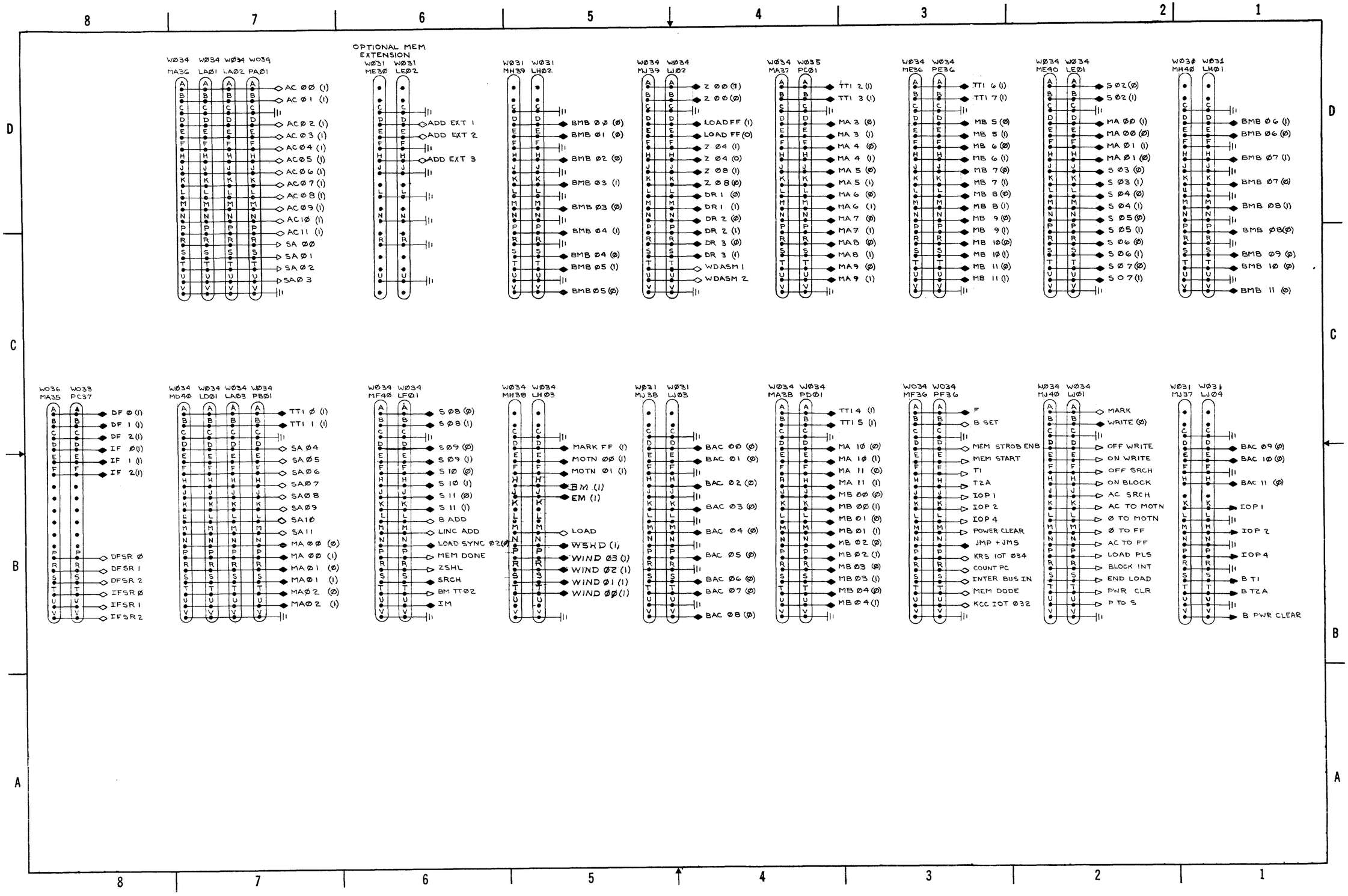
D-SD-LINC8-0-1 System Configuration



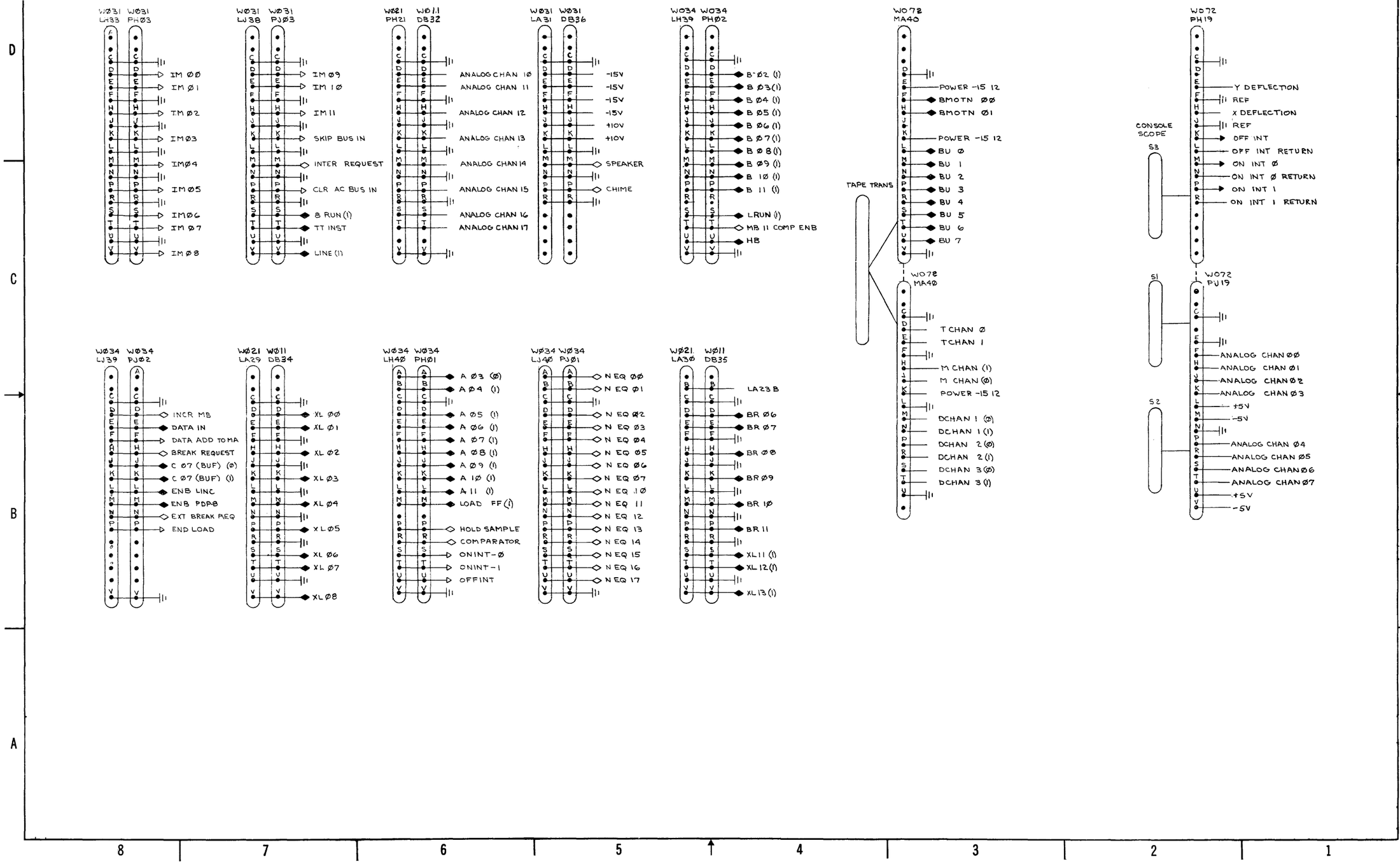
D-BS-LINC8-0-2 Data Terminal Panel Logic



D-MU-LINC8-0-3 Data Terminal Panel UML



D-IC-LINC8-0-4 Cables, LINC-8 (Sheet 1)



D-IC-LINC8-0-4 Cables, LINC-8 (Sheet 2)

SIGNAL	SYMBOL	INTERF CONN	DATA TERM PNL	MODULE TERMINAL	MODULE TYPE
PROGRAMMED DATA TRANSFER INPUT SIGNALS					
AC 0		PE2D	DA32D	PA7E	R210
1		E	E	8E	
2		H	H	9E	
3		K	K	10E	
4		M	M	11E	
5		P	P	12E	
6		S	S	13E	
7		T	T	14E	
8		PE2V	DA32V	15E	
9		PF2D	DA31D	16E	
10		E	E	17E	
AC 11		H	H	18E	R210
CLEAR AC		P	P	PA19J	S603
INTERRUPT REQUEST		M	M	PD36K	S111
SKIP		K	DA32K	PB21V	S603
PROGRAMMED DATA TRANSFER OUTPUT SIGNALS					
BAC 0(1)		ME34D	DA36D	ME26J	R650
1(1)		E	E	ME26T	
2(1)		H	H	ME27J	
3(1)		K	K	ME27T	
4(1)		M	M	ME28J	
5(1)		P	P	ME28T	
6(1)		S	S	MF26J	
7(1)		T	T	MF26T	
8(1)		ME34V	DA36V	MF27J	
9(1)		MF34D	DA35D	MF27T	
10(1)		E	E	MF28J	
BAC 11(1)		H	H	MF28T	R650
IOP 1		K	K	MC31H	W640
2		M	M	MC31N	W640
IOF 4		ME34P	DA35P	MC31U	W640
BMB 3(0)		ME35K	DA34K	MC27T	R650
3(1)		M	M	MC28J	
4(0)		P	P	MC28T	
4(1)		S	S	MC29J	
5(0)		T	T	MC29T	
5(1)		ME35V	DA34V	MD25J	
6(0)		MF35D	DA33D	MD25T	
6(1)		MF35E	E	MD26J	
7(0)		H	H	MD26T	
7(1)		K	K	MD27J	
8(0)		M	M	MD27T	
8(1)		MF35P	DA33P	MD28J	R650
DATA BREAK TRANSFER INPUT SIGNALS					
DATA ADDRESS 0(1)		PH04D	DA30D	PC7R	R211
1(1)		E	E	8R	
2(1)		H	H	9R	
3(1)		K	K	10R	
4(1)		M	M	11R	
5(1)		P	P	12R	
6(1)		S	S	13R	
7(1)		T	T	14R	
8(1)		PH04V	DA30V	15R	
9(1)		PJ04D	DA29D	16R	
10(1)		E	E	17R	
DATA ADDRESS 11(1)		PJ04H	DA29H	PC18R	R211
DATA BIT 0(1)		PH08D	DA28D	PH09E	S107
1(1)		E	E	H	
DATA BIT 2(1)		PH08H	DA28H	PH09K	S107

SIGNAL	SYMBOL	INTERF CONN	DATA TERM PNL	MODULE TERMINAL	MODULE TYPE
DATA BIT 3(1)		PH08K	DA28K	PH09M	S107
4(1)		M	M	P	
5(1)		P	P	S	
6(1)		S	S	PH09W	
7(1)		T	DA28T	PH12E	
8(1)		V	DA28V	H	
9(1)		PJ06D	DA27D	K	
10(1)		E	27E	M	
11(1)		PJ08H	27H	PH12P	
BREAK REQUEST		PJ04K	29K	PJ05H	
TRANSFER DIRECTION		04M	29M	PJ05K	S107
INCREMENT MB		04T	29T	PD31M	S107
CYCLE SELECT		08K	27K	PE7S	S107
INCREMENT CA		PJ08M	DA27M	PE10F	R121
DATA BREAK TRANSFER OUTPUT SIGNALS					
BMB 0(1)		ME35D	DA34D	MC26J	R650
1(1)		E	E	26T	
2(1)		H	H	27J	
3(1)		M	M	28J	
4(1)		S	S	MC29J	
5(1)		ME35V	DA34V	MD25J	
6(1)		MF35E	DA33E	MD26J	
7(1)		K	K	27J	
8(1)		P	P	28J	
9(1)		S	S	28T	
10(1)		T	T	29J	
11(1)		MF35V	DA33V	MD29T	
B BREAK		PJ04P	DA29P	PE8T	R650
ADDRESS ACCEPTED		PJ04S	DA29S	PF10U	W640
WC OVERFLOW		PJ08P	DA27P	FF10N	W640
MISCELLANEOUS INPUT SIGNALS					
ADDR EXTENSION 1		ME30D	ME8K, MC3K		S107, S151
2		E	ME8H, MC3E		S107, S151
ADDR EXTENSION 3		ME30H	ME8E, MC3J		S107, S151
MISCELLANEOUS OUTPUT SIGNALS					
B RUN (1)		PF2S	DA31S	PE8J	R650
DATA FIELD 0(1)		ME30K		ME7L	S107
1(1)		M		ME7N	
DATA FIELD 2(1)		ME30P		ME7R	S107
BT 1		MF34S	DA35S	MD30H	W640
BT 2A		T	T	U	
B POWER CLEAR		MF34V	DA35V	MD30N	W640

*DIRECTION IS INTO PDP-8 WHEN SIGNAL IS -3v, OUT OF PDP-8 WHEN GROUND POTENTIAL.

**THE INCREMENT MB INPUT TO THE PDP-8 MUST BE THE OUTPUT OF A GATING CIRCUIT THAT ENABLES GENERATION OF THE GROUND LEVEL SIGNAL ONLY WHEN THE B BREAK SIGNAL IS PRESENT.

CABLE NO	TYPE	FROM-TO	FUNCTION REMARKS
7405554-1-0	W034 W034	MA36-LA01	PDP-8 MEM-PROC I (11)
7405559-4-0	W034 W035	MA37-PC01	PDP-8 MEM-PROC III
7405554-4-0	W034 W034	MA38-PD01	PDP-8 MEM-PROC IV (9)
-5-0		ME36-PE01	LINC ADDRESS I (9)
-5-0		MF36-PF01	LINC ADDRESS II
-1-0		MD40-LD01	PDP-8 MEM-PROC II (11)
-1-0		ME40-LE01	PDP-8 MEM-PROC V
7405554-3-0	W034-W034	MF40-LF01	PDP-8 MEM-PROC VI
7405554-2-0	W034-W034	MH38-LH03	TAPE SYSTEM III
7405552-2-0	W031-W031	MH39-LH02	BMB 0-5
-1-0		MH40-LH01	BMB 6-11
-2-0		MJ37-LJ04	BAC 9-11 IOP 1,2,4, ETC.
7405552-2-0	W031-W031	MJ38-LJ03	BAC 0-8
7405554-1-0	W034-W034	MJ39-LJ02	TAPE SYSTEM II
7405554-1-0	W034-W034	MJ40-LJ01	TAPE SYSTEM I
7405555-1-0	W033-W036	MA35-PC37	OPTIONAL MEM EXT SW & IND (4&6)
7005187-0-0	W073	MA40 TAPE MB40 UNIT	TAPE TRANSPORT CABLE (10)
7405552-3-0	W031-W031	ME30-LA02	OPTIONAL EXT DAT ADD
7005186-0-0	W072	PH19 PJ19 SCOPE	SCOPE DISPLAY
7405552-2-0	W031-W031	LH38-PH03	INPUT MIXER (AC 0-8)
4-1-0	W034-W034	LH39-PH02	B0-11 & A 0-2
4-1-0	W034-W034	LH40-PH01	A 3-11 & A-D SIGNAL
7405552-2-0	W031-W031	LJ38-PJ03	INPUT MIXER (AC 9-11) ETC.
7405554-1-0	W034-W034	LJ39-PJ02	MISC BREAK & A-D SIGNAL
-1-0		LJ40-PJ01	N00-N17
-3-0		LA02-PA01	PDP-8 MEM-PROC I
7405554-3-0	W034-W034	LA03-PB01	PDP-8 MEM-PROC II
			DATA TERMINAL,PANEL
7405556-7-0	W021-W011	MH33-DA35	PDP-8 IO BAC 9-11 IOP (5)
		MH34-DA36	PDP-8 IO BAC 0-8 (5)
		MH35-DA34	PDP-8 IO BMB 0-5 (5)
		MH36-DA33	PDP-8 IO BMB 6-11 (5)
		PH04-DA30	PDP-8 IO DATA ADD 0-8 (5)
		PJ04-DA29	PDP-8 IO DATA ADD 9-11 (5)
		PH06-DA32	PDP-8 IO INPUT MIXER 0-8 (5)
		PJ06-DA31	PDP-8 IO INPUT MIXER 9-11 (5)
		PH08-DA28	PDP-8 IO DATA BITS 0-8 (5)
		PJ08-DA27	PDP-8 IO DATA BITS 9-11 (5)
7405556-7-0	W021-W011	PH21-DB32	LINC ANALOG CHAIN 10-17 (5)
7405553-7-0	W033-W033	LA31-DB36	LINC CHIME POWER SPEAKER
7405556-7-0	W021-W011	LA29-DB34	LINC XL-0-10
7405556-7-0	W021-W011	LA30-DB35	LINC RELAYS XL 11-13
			INDICATOR CABLES
7405553-6-0	W033-W033	IND01-PC-38	PDP-8 RUN FETCH ETC. (1)
-5-0		02-PB-38	PDP-8 INSTRUCTIONS (1)
-4-0		03-PA40	PDP-8 BITS 9-11 (1)
-4-0		04-PB40	PDP-8 BITS 6-8 (1)
-3-0		05-PA39	PDP-8 BITS 3-5 (1)
-3-0		06-PB39	PDP-8 BITS 0-2 (1)
-2-0		07-PA38	PDP-8 INST-FIELD & DATA FIELD (1)
-2-0		08-LA23	LINC BITS 9-11 (1)
-2-0		09-LA22	6-8 (1)
-2-0		10-LA19	3-5 (1)
-2-0		11-LA16	LINC BITS 0-2 (1)
-2-0		12-LA27	LINC UMB, R LMB (1)
7405553-1-0	W033-W033	IND13-LA24	LINC AUTO IBI ETC (1)

CABLE NO	TYPE	FROM-TO	FUNCTION REMARKS
			CONTROL CONSOLE
7405553-1-0	W033-W033	CA02-LA36	LINC CONTROL SWITCHES (1)
-1-0		CB02-LA37	DELAY; AUDIO CHIME (1)
-1-0		CA03-LA05	LEFT SWITCH (1)
7405553-1-0	W033-W033	CB03-LA35	LINC SENSE SW& CONTROL SW (1)
7405555-2-0	W036-W033	CA04-PB37	PDP-8 RIGHT SWITCH (2)
7405555-2-0	W036-W033	CB04-PA37	PDP-8 CONTROL SWITCH (3)
			STANDARD IO CABLE TO PERIPHERAL
	W021	ME34	BAC 0-8
		MF34	BAC 9-11 IOP
		ME35	BMB 0-5
		MF35	BMB 6-11
		PE02	INPUT MIXER 0-8
		PF02	INPUT MIXER 9-11
		PH04	DATA ADD 0-8 (8)
		PJ04	DATA ADD 9-11 (8)
		PH08	DATA BITS 0-8 (8)
	W021	PJ08	DATA BITS 9-11 (8)
7005423-0-0	TAPE UNIT TO TAPE UNIT		LINC 8 TAPE EXTENSION CABLE (10)

M = MEMORY SECTION
L = LINC SECTION
P = PROCESSOR SECTION
D = DATA TERM PANEL
IND = INDICATORS
C = CONTROL SWITCHES

NOTES:

1- JUMPER PIN "B"

2- JUMPER PIN "B" OF W033, JUMPER PIN "B" & "C" OF W036, 100 OHM PINS P-V OF W036

3- JUMPER PIN "B" OF W033, JUMPER PIN "B" & "C" OF W036, 100 OHM ON PINS: D-H,K & M-V 10 OHM ON PINS: J & L OF W036

4- D664 DIODES PINS A-N, 100 OHM RESISTORS PINS P-V OF W036
JUMPER PINS A & B OF W033

5- COAX CABLE

6- OPTIONAL FOR EXTENDED MEMORY

7- OPTIONAL FOR EAE

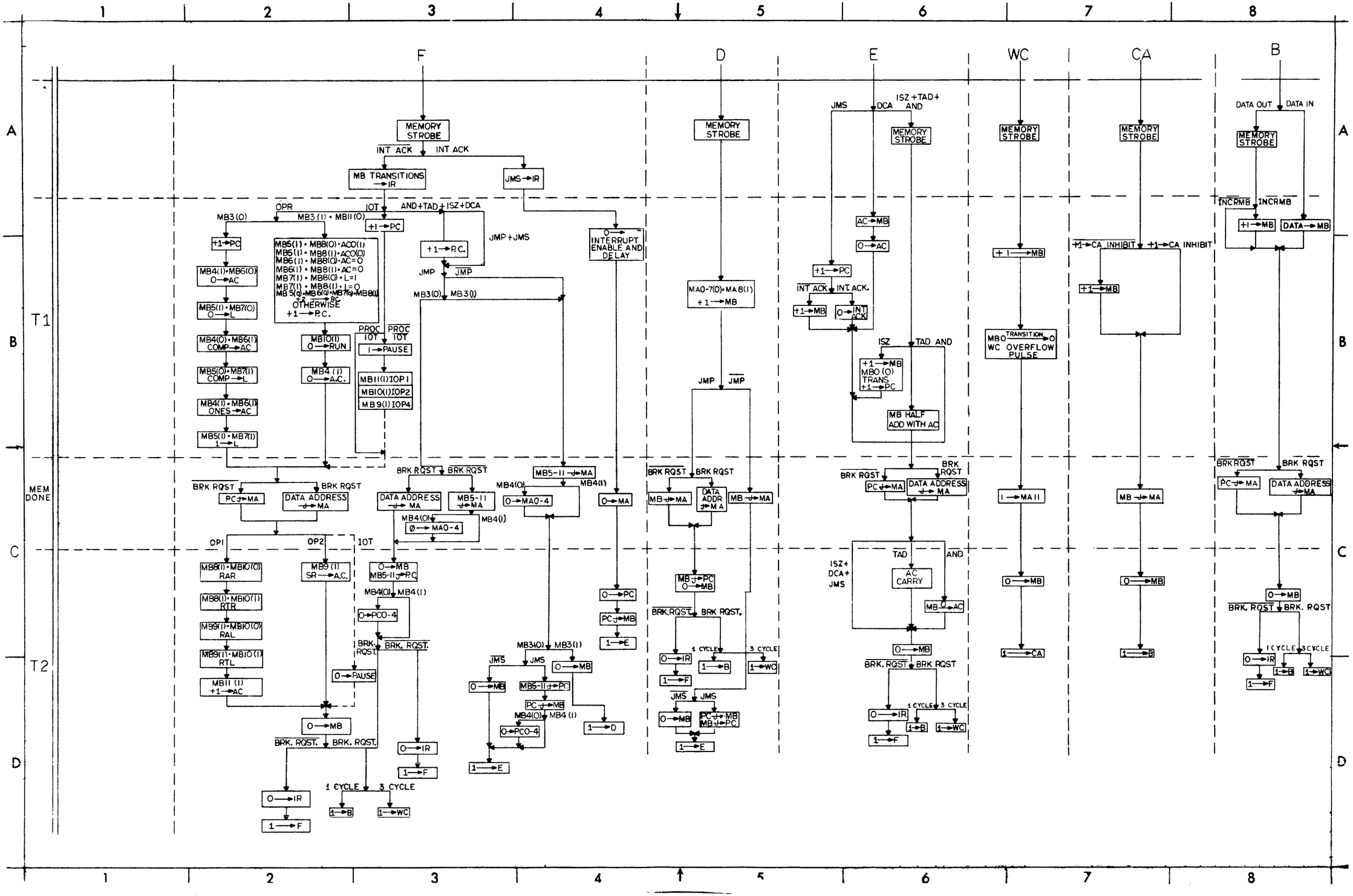
8- ONLY ONE BREAK DEVICE IS ALLOWED UNLESS DW01 (MULTIPLEXER) IS USED THEREFORE EITHER DATA TERM PANEL OR PERIPHERAL BREAK DEVICE MAY BE USED.

9- 220 OHM RESISTORS IN MEMORY END OF CABLE 100 OHM RESISTORS IN PROCESSOR END OF CABLE.

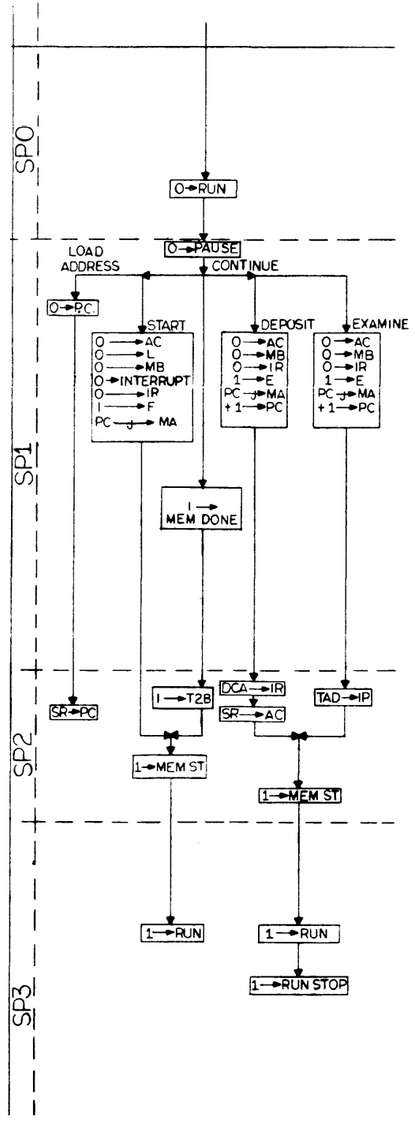
10- ONE CABLE ADDITIONAL FOR EACH ADDITIONAL DUAL TAPE UNIT.

11- 100Ω RESISTORS IN SERIES WITH PINS A AND B IN BOTH ENDS OF THE CABLE.

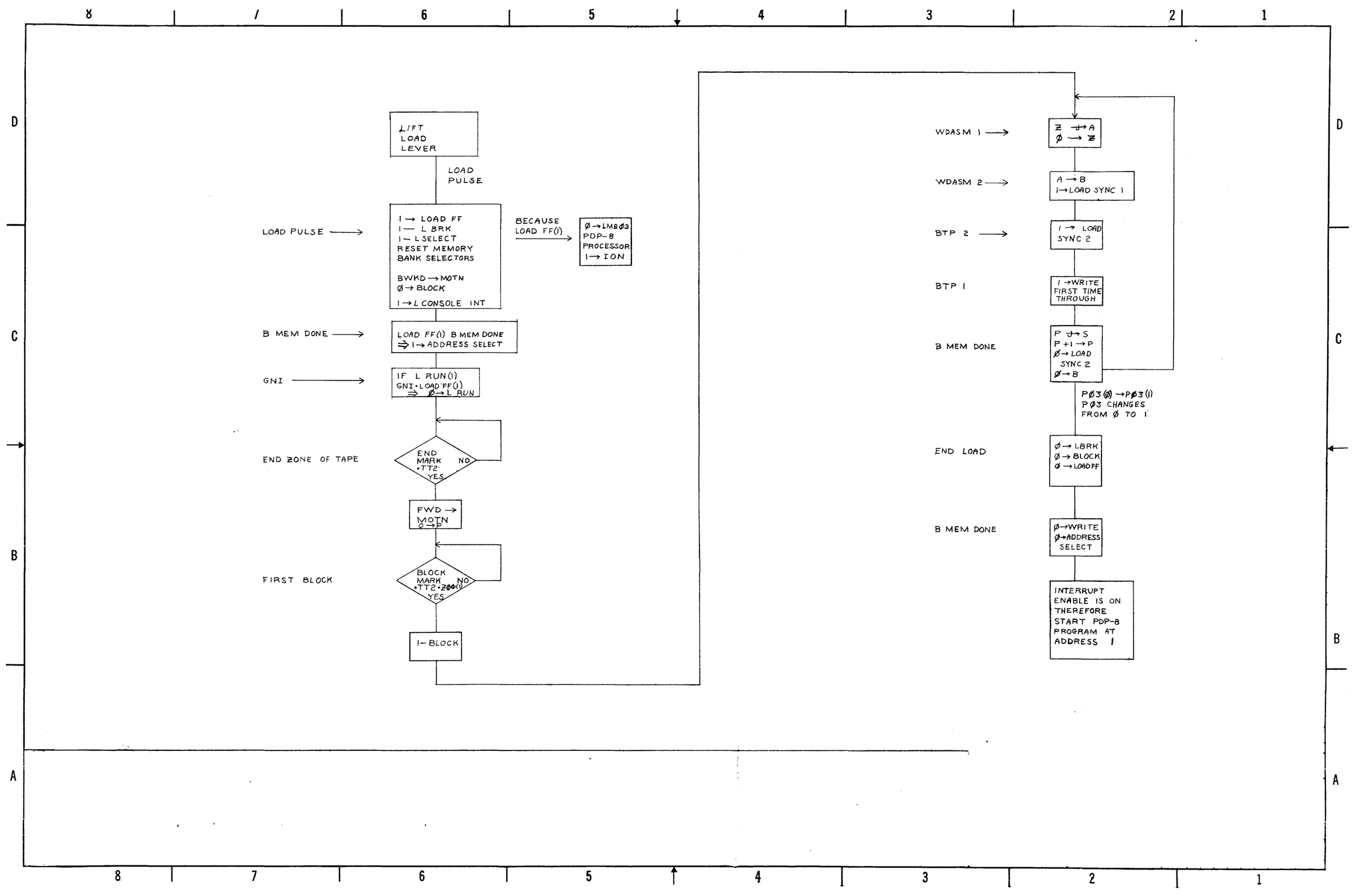
D-IC-LINC8-0-6 Cable List



D-FD-LINC8-0-9 Flow Diagram, Automatic Operations



D-FD-LINC8-0-9 Flow Diagram, Manual Operations

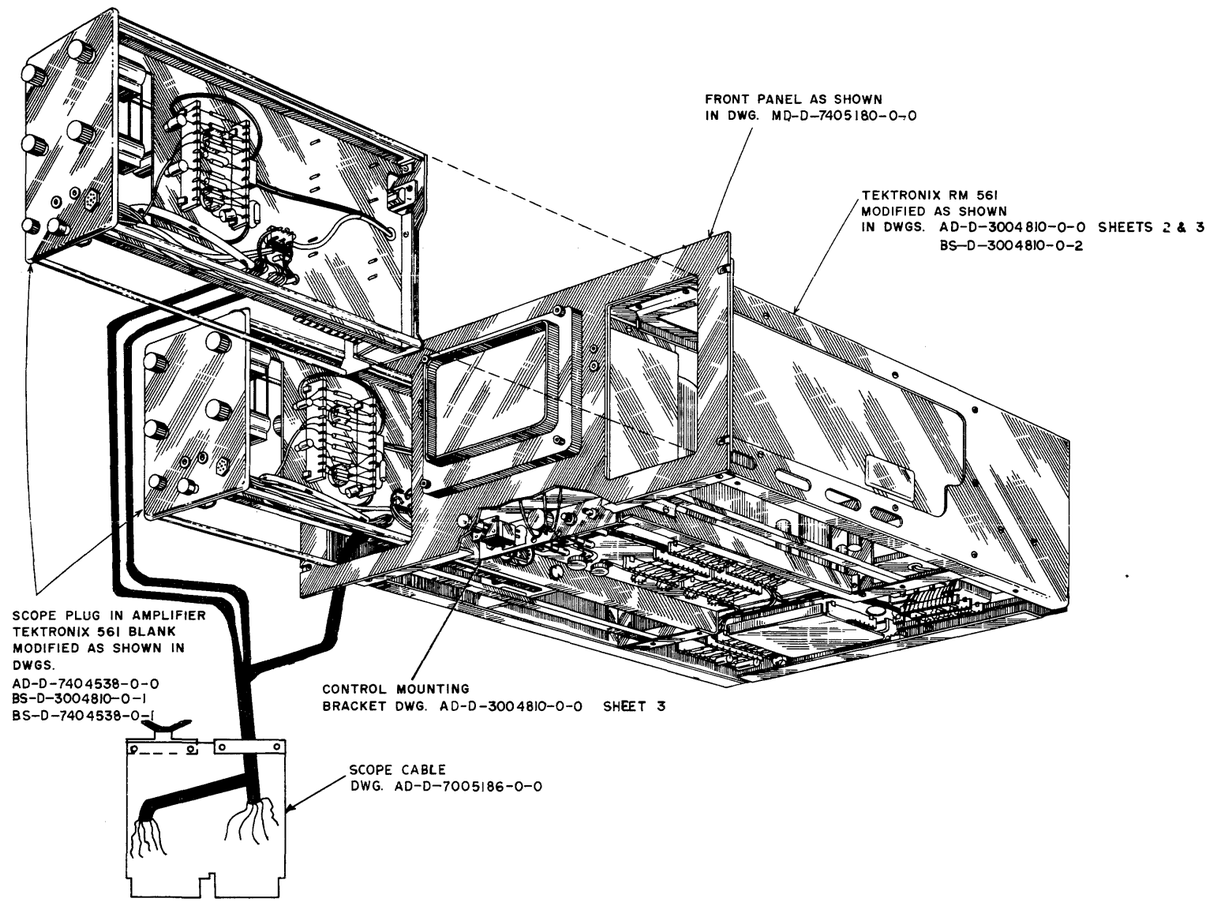


D-FD-LINC8-0-30 Flow Diagram, Load

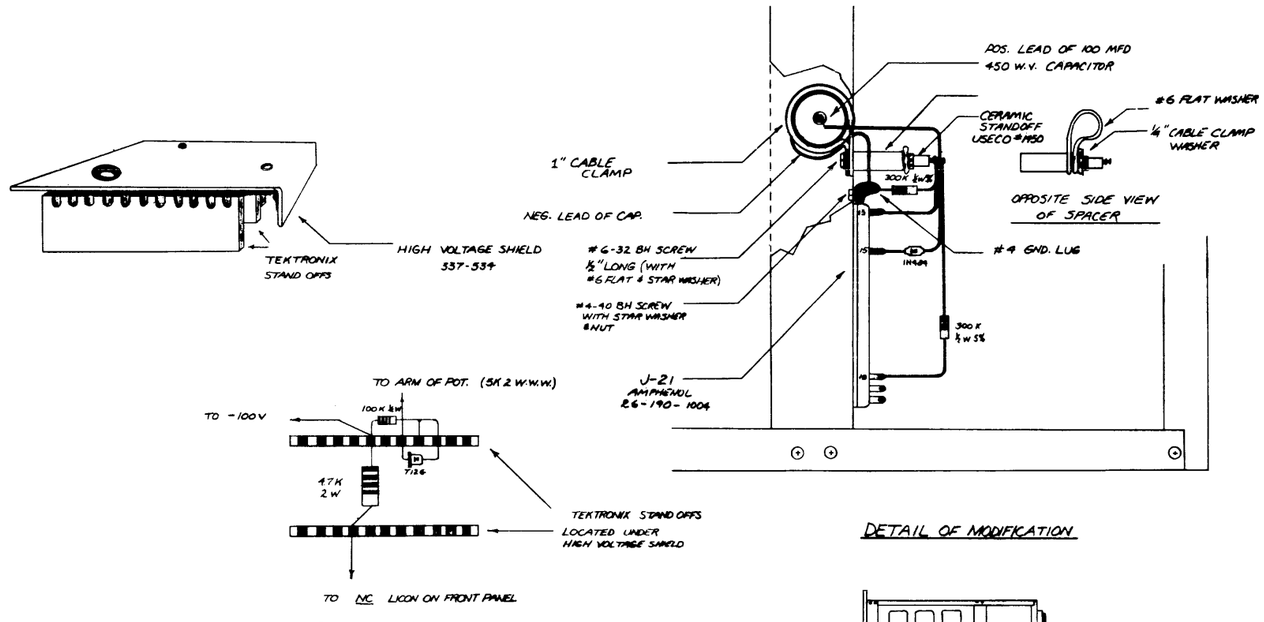
SEE NOTE 1 #		
	D-AD-3004810-1-0	60 CYCLE
	D-AD-3004810-2-0	50 CYCLE

NOTES:

1. 60 CYCLE UNIT IDENTICAL TO 50 CYCLE UNIT EXCEPT FOR INTERNAL WIRING. REFER TO INSTRUCTION MANUAL.

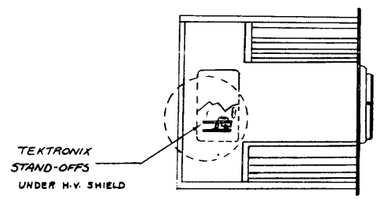


D-AD-3004810-0-0 Console Scope Overall (Sheet 1)

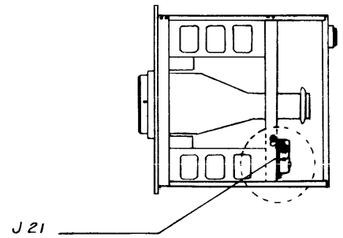


DETAIL OF MODIFICATION

TOP VIEW OF STAND-OFFS



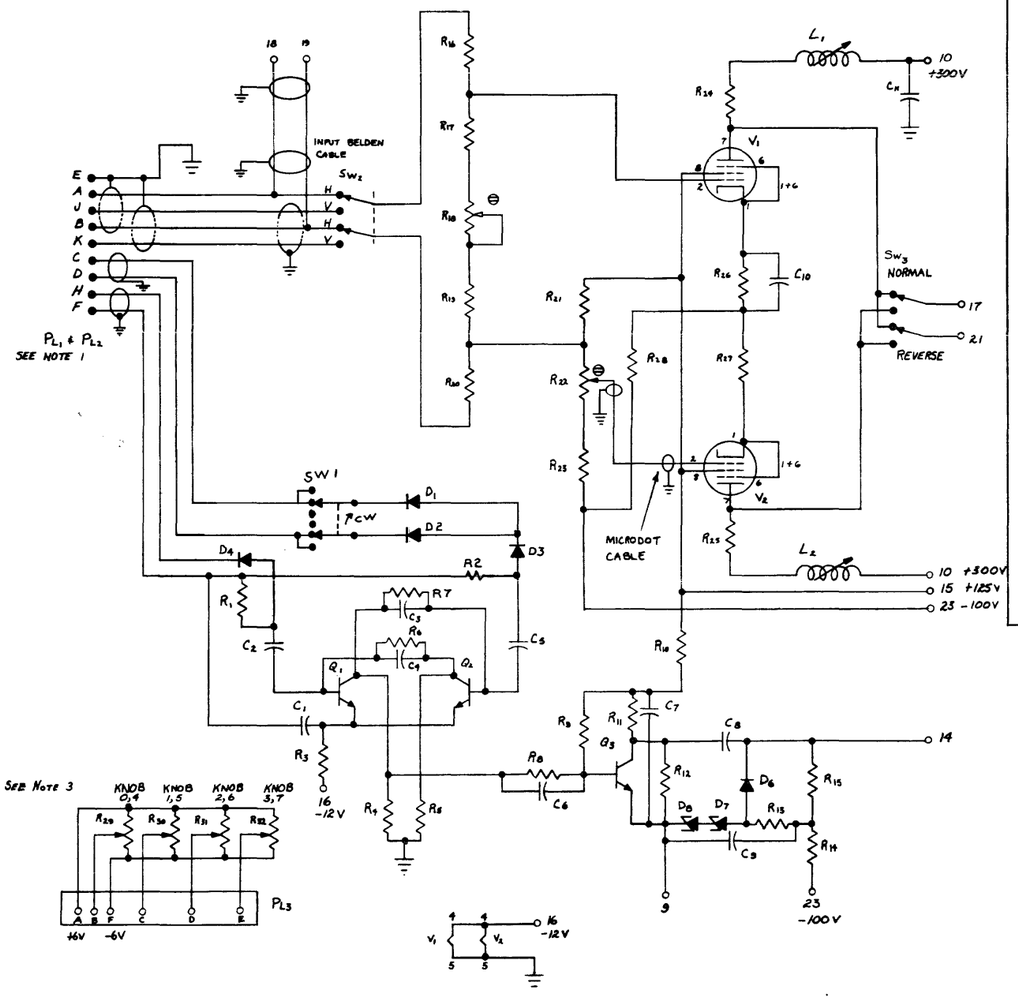
BOTTOM VIEW OF SCOPE CHASSIS



TOP VIEW OF SCOPE CHASSIS
SHOWING POSITION OF MOD.

NOTES:

D-AD-3004810-0-0 Console Scope Inten (MTG Mode) (Sheet 4)



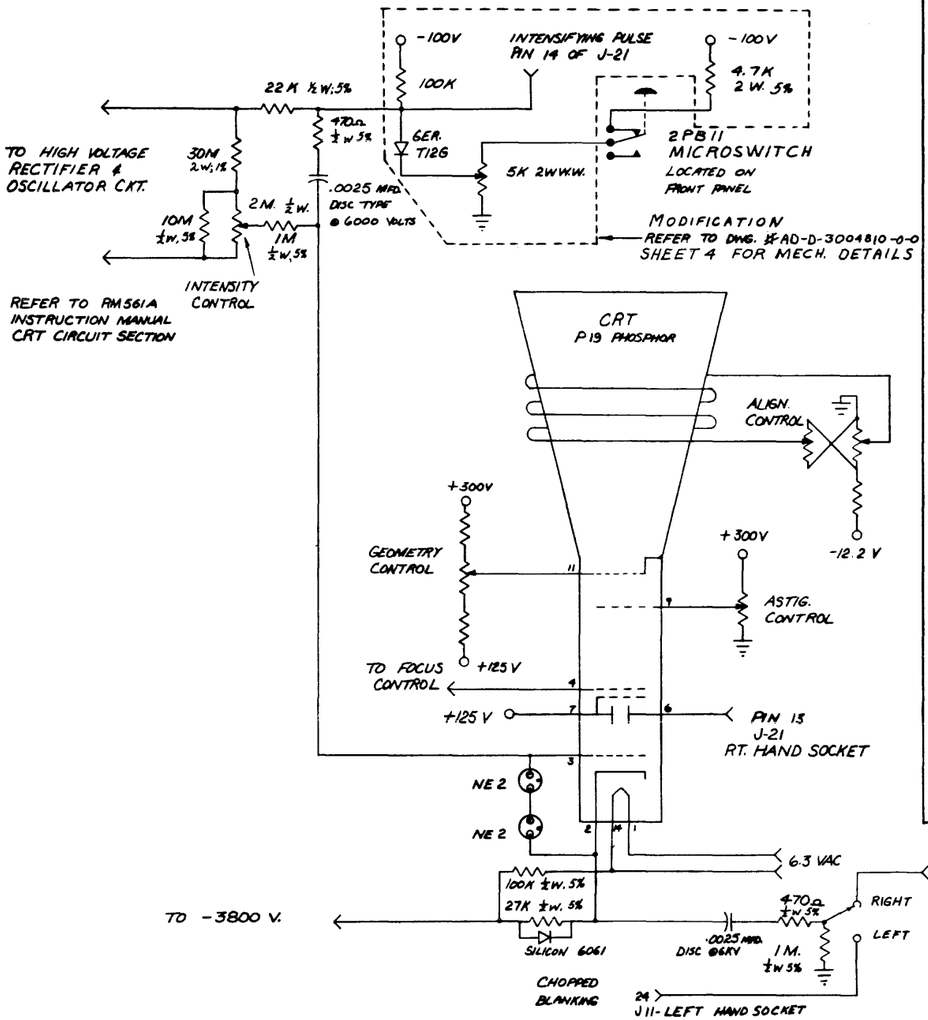
PARTS NUMBER KEY

C_1	1000pf. CD DIPPED SILVER MVA	1ea
$C_2 C_5$	100pf. CD DIPPED SILVER	2ea
$C_3 C_4$	30pf. CD DIPPED SILVER MICA	2ea
C_6	10pf. CD DIPPED SILVER MICA	1ea.
$C_7 C_9 C_{11}$	.1 MF. DISC @ 600WV SPRAGUE	3ea.
C_8	.1 MF. TUBULAR 300WV AEROVOX	1ea.
C_{10}	.1MF. 100WV 6000-ALL X663F	1ea.
$D_1 D_2 D_3 D_4 D_5$	IN276 CLEVITE	5ea.
D_6	IN484 FAIRCHILD	1ea.
D_7	IN3038 MOTOROLA	1ea.
D_8	IN3030B MOTOROLA	1ea.
L_1, L_2	8.3 MH – 1MH DELEVAN 200-56/R	2ea.
PL_1	9 PIN AMPHENOL #126-219	1ea.
PL_2	9 SOC AMPHENOL #126-221	1ea.
PL_3	7 PIN AMPHENOL #126-197	1ea.
$Q_1 Q_2$	2N708 FAIRCHILD	2ea.
Q_3	2N1893 FAIRCHILD	1ea.
$R_1 R_2 R_{16} R_{20}$	5.1K A/B ½ W 5%	4ea.
$R_3 R_{10} R_{19}$	100Ω A/B ½ W 5%	3ea.
$R_4 R_5 R_8$	1 K A/B ½ W 5%	3ea.
$R_6 R_7 R_{12} R_{17} R_{18}$	10K A/B ½ W 5%	5ea.
R_9	47K A/B ½ W 5%	1ea.
R_{11}	6.2K A/B 2W 5%	1ea.
R_{13}	15K A/B 2W 5%	1ea.
R_{15}	33K A/B 2W 5%	1ea.
R_{16}	250K VAR. A/B ½ W TYPE Q	1ea.
R_{21}	125k ½ W 1%	1ea.
R_{22}	5 k VAR. A/B ½ W TYPE G	1ea.
R_{23}	95.3k ½ W 1%	1ea.
$R_{24} R_{25}$	20K 5 W WARD LEONARD	2ea.
$R_{26} R_{27}$	33Ω A/B ½ W 5%	2ea.
R_{28}	8.2 K 5W CHIMITE # AG5I	1ea.
$R_{29} R_{30} R_{31} R_{32}$	5 K, 3 TURN RT CLAROSTAT #110-6326	4ea.
SW_1	3 POL 3 POS CENTRALAB #PS-10B	1ea.
$SW_2 SW_3$	DPDT SLIDESWITCH SA STACKPOLE	2ea.
$V_1 V_2$	12.BV7 SYLVANIA	2ea.

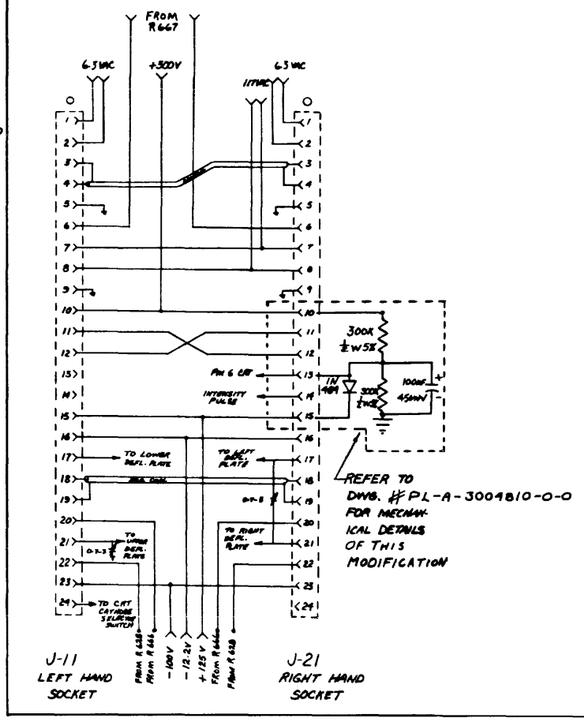
NOTES:

1. PL_2 IS MOUNTED ON FRONT OF AMPLIFIER AND IS WIRED IN PARALLEL WITH PL_1.
2. NUMBERED PINS REFER TO PL_4. 24 PIN CONNECTOR PROVIDED IN TEKTRONIX BLANK PLUG IN UNIT.
3. KNOBS ARE TO BE ENGRAVED AS SHOWN IN DWG #AD-D-3004810-0-0 SHEET 2. (ONE PLUG IN 0-3, OTHER PLUG IN 4-7).

D-BS-3004810-0-1 Display Amplifier Intensifier Circuit



REFERENCE - TEKTRONIX PRELIMINARY MANUAL RM-561A.

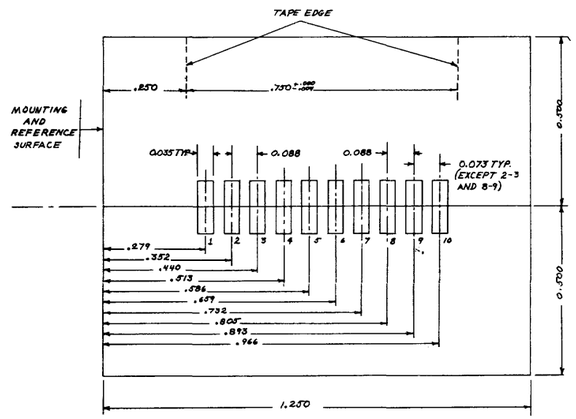


NOTES:

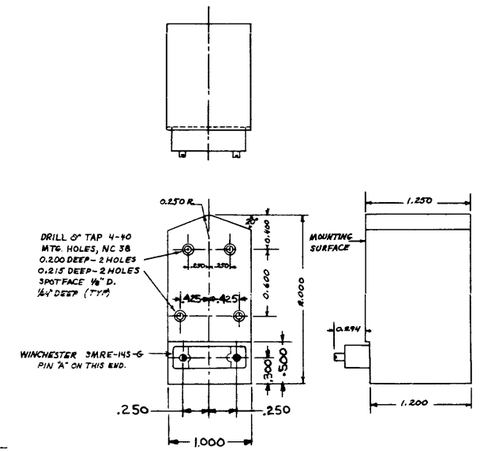
D-BS-3004810-0-2 Console Scope Elec. Mod.

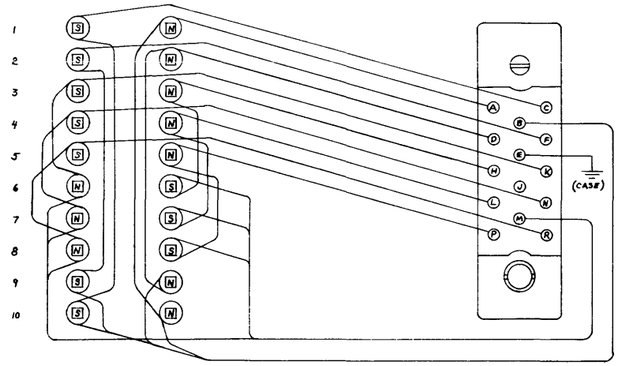
NOTES:

1. ALL BURRS TO BE REMOVED FROM MTG. SURFACE BY GRINDING OR LAPPING AFTER DRILLING, TAPPING & SPOTFACING.
2. TAPE HEAD TO BE PURCHASED FROM INSCO CORP.



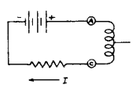
GAP WIDTH - 500 MICROINCHES
GAP SCATTER - ± 50 MICROINCHES
GAP LINE PERPENDICULARITY - 100 MICROINCHES
SKEW BETWEEN TRACKS 1&10.
SHIELD LOCATIONS - AS REQUIRED TO MEET CROSSTALK SPECIFICATIONS.





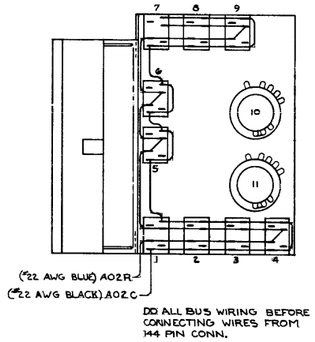
VIEW OF EXPOSED RECEPTACLE OF WINCHESTER 3MRE-143-G

NOTE: POLE PIECES ARE SHOWN AS VIEWED FROM END OF HEAD WHICH CONTACTS TAPE. "N" & "S" DESIGNATE NORTH-SEEKING & SOUTH-SEEKING POLES RESPECTIVELY, WHEN PINS A, D, H, L & P ARE CONNECTED TO A POSITIVE SOURCE & C, F, K, M & R ARE CONNECTED TO THE NEGATIVE RETURN.

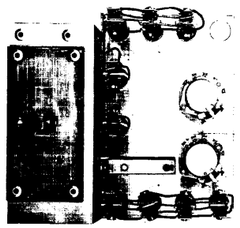


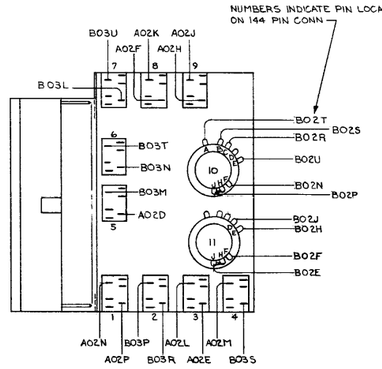
WIRING

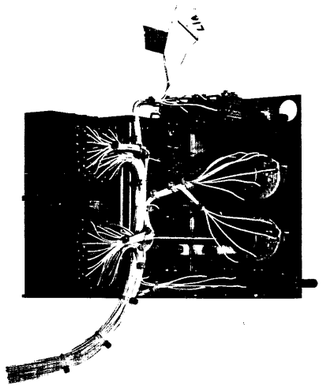
D-SC-340460-0 Tape Head



STEP 1







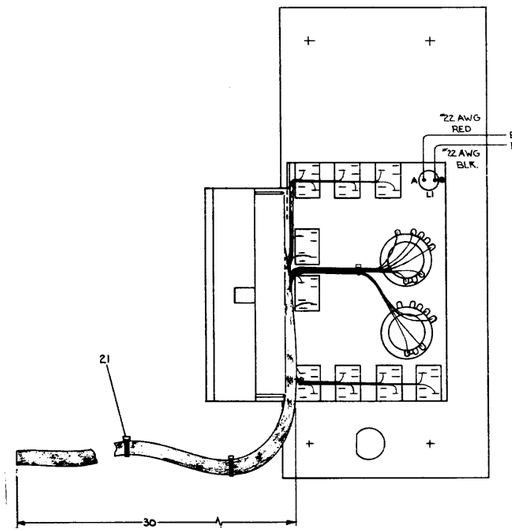
STEP 2

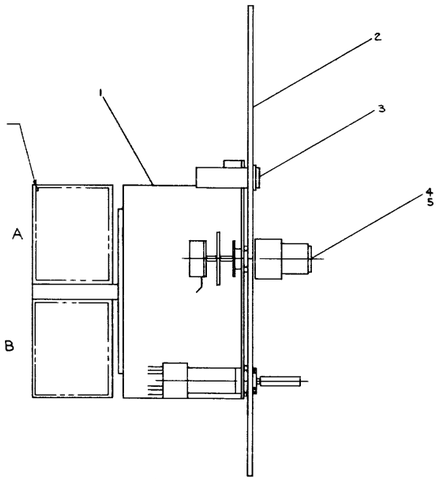
NOTES:

1. ALL WIRE TO BE WHITE #22 AWG STRANDED TEFLON INSULATED UNLESS OTHERWISE SPECIFIED.
2. ~~INSTALL ACC WIRES ON 144 PIN CONN. & LABEL ENDS THE CORRECT NUMBER PER WIRING TABLE PER COLUMN LABELED "144 PIN CONN".~~
3. ASSEMBLE CONTROL BOX (#1) & FRONT PANEL (#2) AFTER ALL WIRING IS COMPLETE ON CONTROL BOX.
4. INSTALL INDICATOR LAMP IN #2 (FRONT PANEL) & CONNECT WIRES

WIRING TABLE

LENGTH OF WIRE	NAME	144 PIN CONN	SW NO PIN LTR
10 IN	GND	A02C	1F
"	-3VSUP	A02R	1D
	DO TO G	A02P	1E
	STOP	A02N	1B
	FILL	B03R	2E
	EXAM	B03P	2B
	RESUME	A02E	3E
	STEP	A02L	3B
	FILL STEP	B03S	4E
	EXAM STEP	A02M	4B
	MARK	A02D	5E
	CLEAR	B03M	5B
	E STOP	B03N	6E
	F STOP	B03T	6B
	AUTO RESTART	B03L	7E
	INST BY INST	B03U	7B
	LOAD	A02F	8E
	START 40B	A02K	8B
	START RS	A02H	9E
	START 20	A02J	9B
	DELAY 7	B02T	10A
	DELAY 6	B02S	10B
	DELAY 5	B02R	10C
	DELAY 3	B02U	10E
	DELAY 1	B02N	10F
	DELAY 2	B02P	10J
	CHIME 1	B02J	11D
	CHIME 2	B02H	11E
	SPEAKER	B02F	11F
	SPEAKER	B02E	11J
"	LINE HUM	B02D	L1A
10 IN	-15V	B02B	L1B
30 IN	GND	B03C	12A
"	SENSE 0	B03D	12B
	SENSE 1	B03E	13B
	SENSE 2	B03F	14B
	SENSE 3	B03H	15B
	SENSE 4	B03J	16B
	SENSE 5	B03K	17B
	L.SW.0	A03D	18B
	L.SW.1	A03E	19B
	L.SW.2	A03F	20B
	L.SW.3	A03H	21B
	L.SW.4	A03J	22B
	L.SW.5	A03K	23B
	L.SW.6	A03L	24B
	L.SW.7	A03M	25B
	L.SW.8	A03N	26B
	L.SW.9	A03P	27B
	L.SW.10	A03R	28B
	L.SW.11	A03S	29B
	DATA F. 0	B04N	30D
	GND	A04C	30C
	DATA F. 1	B04P	31B
	DATA F. 2	B04R	32B
	INST F. 0	B04S	33B
	INST F. 1	B04T	34B
	INST F. 2	B04U	35B
	R.SW. 0	A04D	36B
	R.SW. 1	A04E	37B
	R.SW. 2	A04F	38B
	R.SW. 3	A04H	39B
	R.SW. 4	A04J	40B
	R.SW. 5	A04K	41B
	R.SW. 6	A04L	42B
	R.SW. 7	A04M	43B
	R.SW. 8	A04N	44B
	R.SW. 9	A04P	45B
	R.SW. 10	A04R	46B
	R.SW. 11	A04S	47B
	GND	B04C	48A
	START	B04K	48B
	GND	B04B	49C
	LOAD	B04D	49B
	DEPOSIT	B04E	50B
	EXAM	B04F	51B
	CONT	B04H	52B
	STOP	B04J	53B
"	SING STEP	B04L	54B
3C IN	SING INST	B04M	55B



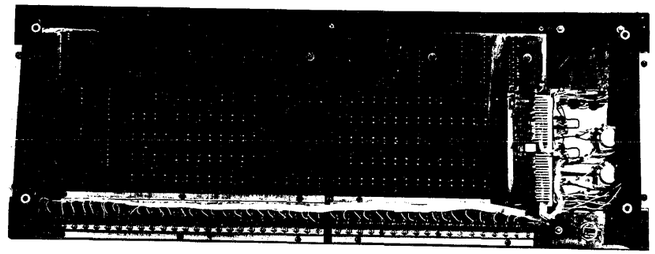


STEP 3

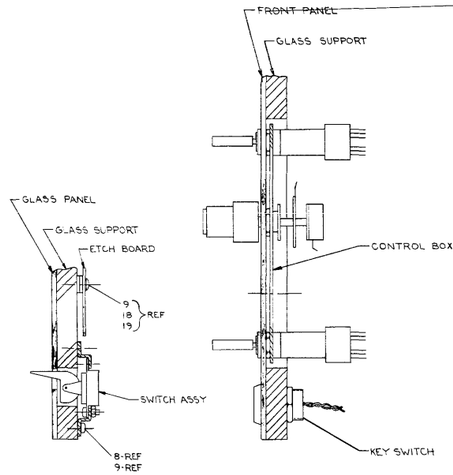
TYP TERM LTRS FOR SWITCHES #1 THRU #9

E-AD-7005114-0-0 Control Panel (Sheet 1)

NOTES:
1. *25 (GLASS PANEL) WELL NOT BE ASSEMBLED TO *20 (GLASS SUPPORT) UNTIL CONTROL PANEL IS MOUNTED IN LINC 8 CABINET



REAR VIEW



SECTION A-A

SECTION B-B

ASSEMBLY PROCEDURE:

STEP 1. FASTEN *17 (ETCH BOARD) TO *20 (GLASS SUPPORT) USING *18 (SCREW), *9 (WASHER), & *19 (NYLON WASHER

STEP 2. FASTEN *7 & *16 (SWITCH ASSY'S) TO *20 (GLASS SUPPORT) USING *8 (SCREW) & *9 (WASHER)

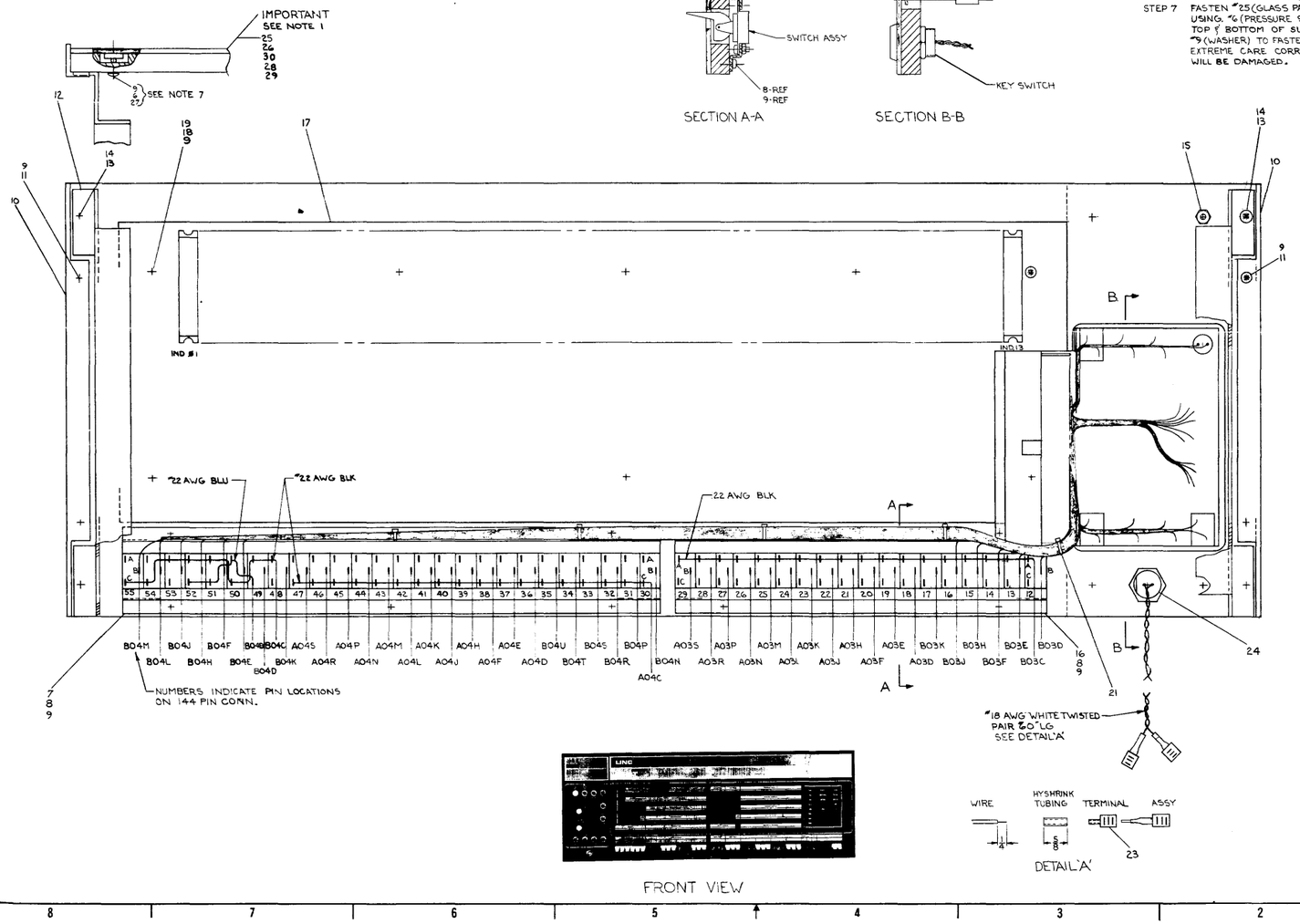
STEP 3 INSERT *1 (CONTROL BOX) & WIRE THRU GLASS SUPPORT FASTEN WITH *15 (KEPS NUT) & SOLDER WIRES TO INDICATED SWITCHES

STEP 4 INSERT *24 (KEY SWITCH) THRU *2 (FRONT PANEL) & *20 (GLASS SUPPORT) FASTEN WITH SUPPLIED HARDWARE SOLDER ON WIRE (WHT & WHT TW. PR.)

STEP 5 FASTEN *10 (SIDE TRIM) TO GLASS SUPPORT USING *11 (SCREW)

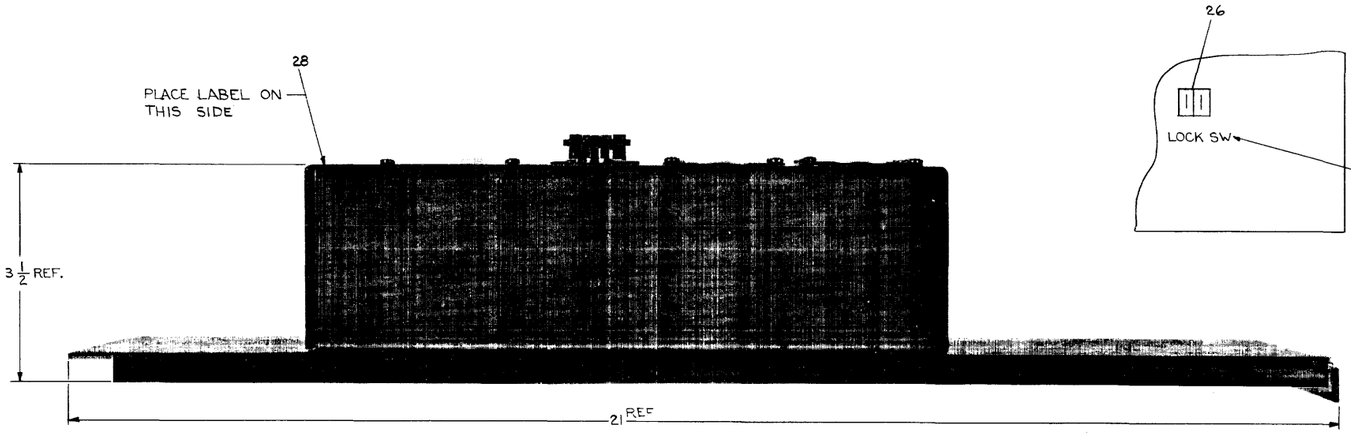
STEP 6 FASTEN *12 & *31 (MTG BRKT) TO GLASS SUPPORT USING *14 (SCREW) & *13 (WASHER)

STEP 7 FASTEN *25 (GLASS PANEL) TO *20 (GLASS SUPPORT) USING *6 (PRESSURE SENSITIVE ADHESIVE *464) ACROSS TOP & BOTTOM OF SUPPORT. ALSO USE *27 (SCREW) & *9 (WASHER) TO FASTEN IN PLACE. WHEN TIGHTENING USE EXTREME CARE. CORRECT LENGTH IS USED OR GLASS PANEL WILL BE DAMAGED.



FRONT VIEW

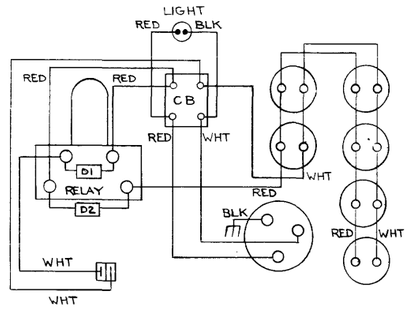
E-AD-7005114-0-0 Control Panel (Sheet 2)



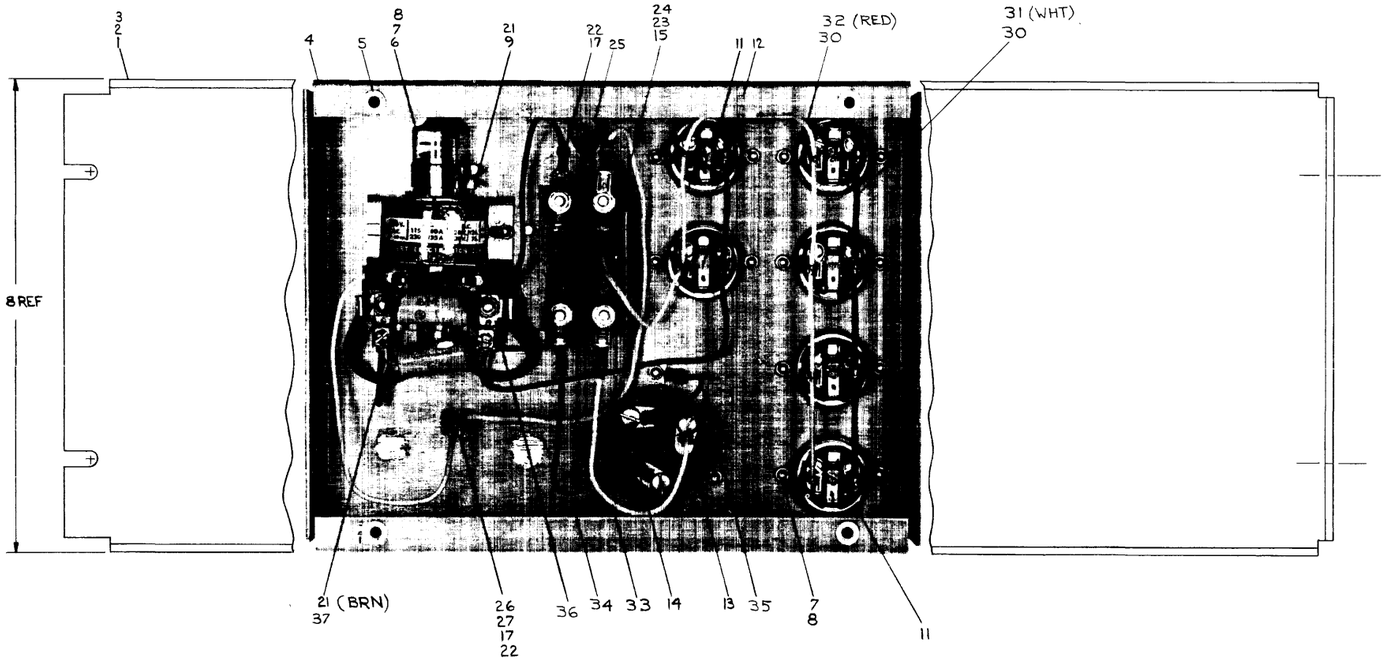
NOTES:

~~1. WIRE USED FOR BUSSING TO BE #14 AWG SOLID UNLESS OTHERWISE SPECIFIED.~~

2. WIRE WITH SCREW DOWN LUGS OR QUICK DISCONNECTS TO BE #14 AWG STRANDED & TEFLON INSULATED UNLESS OTHERWISE SPECIFIED.



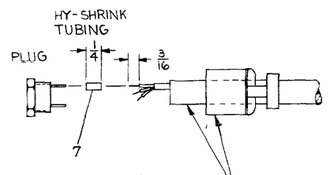
CIRCUIT SCHEMATIC

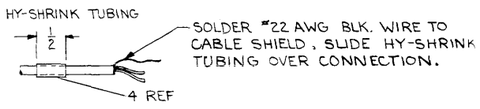


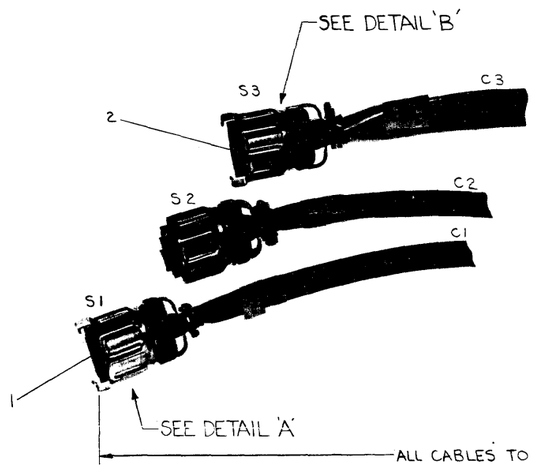
WIRING INCORRECT IN THIS VIEW
SEE CIRCUIT SCHEMATIC.

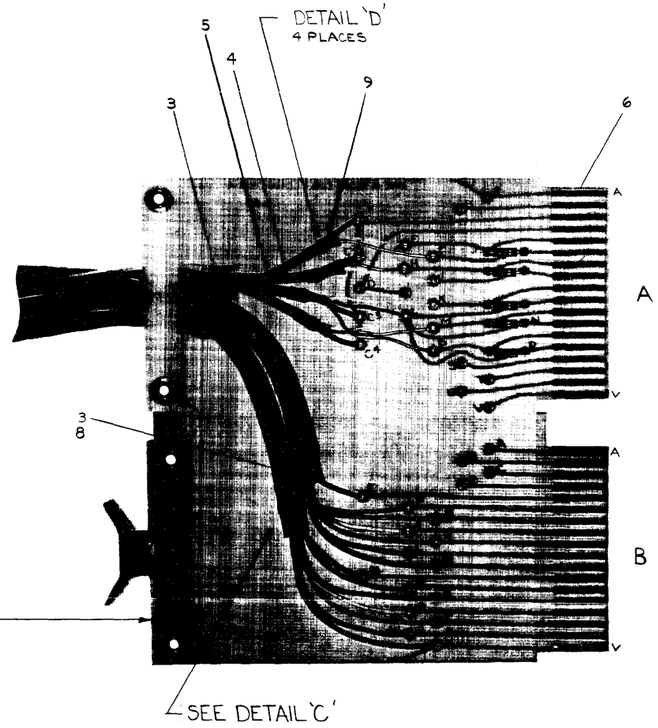
D-AD-7005164-1-0	60 CYCLE
D-AD-7005164-2-0	50 CYCLE

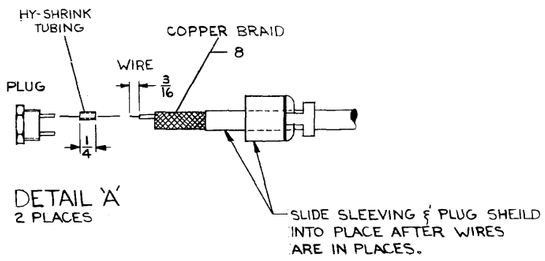
D-AD-7005164-0-0 Power Input Panel Assy.

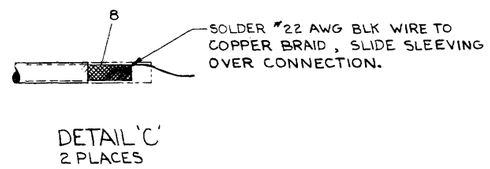










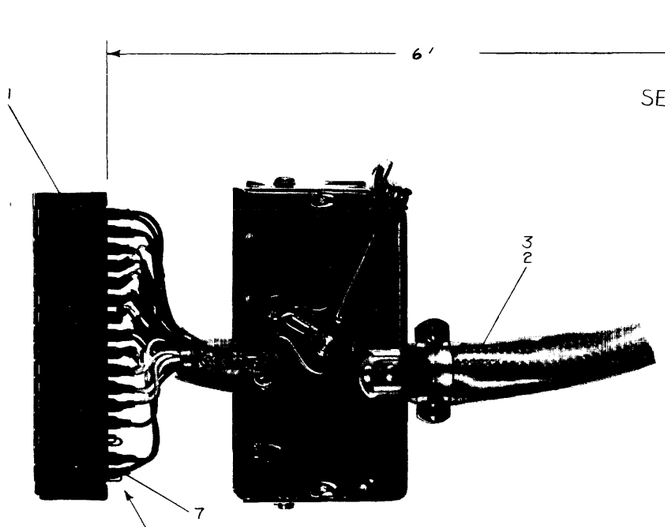


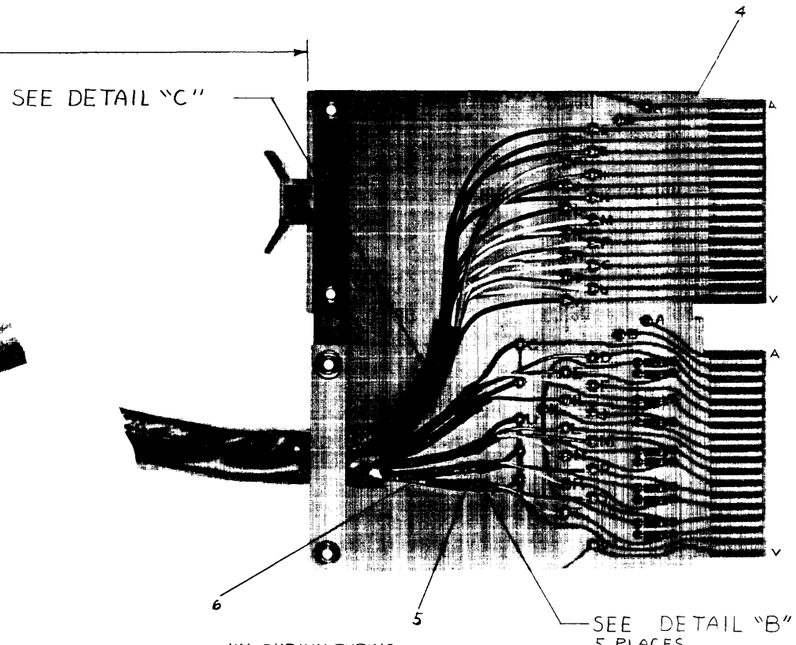
NOTES:

1. ALL WIRE TO BE #22 AWG. SINGLE STRAND TEFLON INSULATED UNLESS OTHERWISE SPECIFIED.
2. EYELETS & NYLON CLAMP TO BE INSTALLED AFTER CABLES HAVE BEEN SOLDERED TO BOARD.

WIRING LEGEND				
CABLE NO	PLUG PIN LTR	W072 PIN LTR	COLOR	WIRE
C1	S1-A	B-L	BRN	22 AWG
↓	S1-B	B-F	RED	↓
	S1-C	B-H	ORN	
	S1-D	B-J	YEL	
	S1-E	B-K	GRN	
↓	S1-F	B-M	BLU	
C1	CABLE GRD	B-E	BLK	
C2	S2-A	B-U	BRN	
↓	S2-B	3-P	RED	
	S2-C	B-R	ORN	
	S2-D	B-S	YEL	
	S2-E	B-T	GRN	
↓	S2-F	B-V	BLU	↓
C2	CABLE GRD	B-N	BLK	22 AWG
C3	S3-A	A-E	WHITE	MICRO-DOT
↓ 1	S3-B	A-F	RED	CABLE
	CABLE GRD	A-C1	BLK	22 AWG
	S3-J	A-H	RED	MICRO-DOT
2	S3-K	A-J	WHT	CABLE
	CABLE GRD	A-C2	BLK	22 AWG
	S3-C	A-M	WHT	MICRO-DOT
3	S3-D	A-P	RED	CABLE
	S3-F	A-L	BLUE	
	CABLE GRD	A-C3	BLK	22 AWG
	S3-E	A-D	RED	MICRO-DOT
↓ 4	S3-H	A-K	WHITE	CABLE
C3	GRD CABLE	A-C4	BLACK	22 AWG

3	CABLE 2 CONDUCTOR x6 FT. LG MICRODOT		9
2	COPPER BRAID 1/4 DIA X 6 FT. LG.		8
22	HY SHRINK TUBING #18 X 1/4 LONG (RED)		7
1	LINC 8 SCOPE CABLE CONN W872 FLIP CHIP	W872	6
4	HY SHRINK TUBING #14 X 1/2 LG (RED)		5
1	CABLE 3 CONDUCTOR X 6 FEET LG MICRODOT		4
3	SLEEVING VINYL EXTRUDED BLK ASTRA 703/105 SIZE NO 1/4 X 6 FEET LG		3
1	HEX CONN (9 CONTACTS) 126-222 AMPHENOL	S3	2
2	HEX CONN (7 CONTACTS) #126-196 AMPHENOL	S1,S2	1





NOTES:

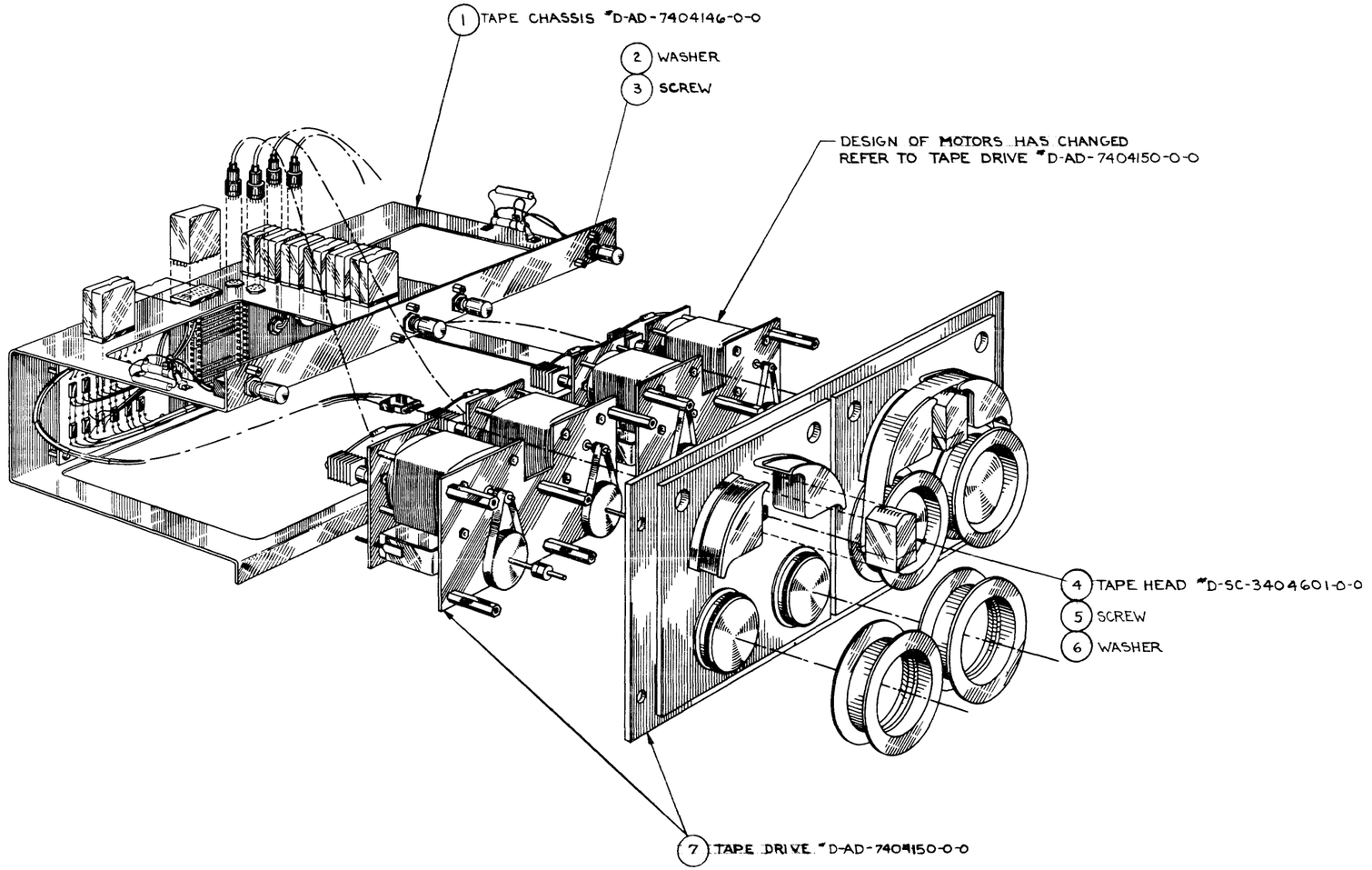
1. ALL WIRE TO BE #22 AWG SINGLE STRAND TEFLON INSULATED UNLESS OTHERWISE SPECIFIED.
2. EYELETS & NYLON CLAMP TO BE INSTALLED AFTER CABLES HAVE BEEN SOLDERED TO BOARD.

WIRING LEGEND

CABLE NO	PLUG PIN LTR	W073 PIN LTR	COLOR	WIRE
C1	P-13	A-J	BLU	22 AWG
	P-1	A-C	GRN	
	P-17	A-D	RED	
	P-32	A-E	ORN	
	P-3	A-F	YEL	
	P-24	A-H	GRN	
	P-31	A-K	VIO	
	P-9	A-L	GRY	
	P-25	A-M	WHT	
	P-10	A-N	WHT-BRN	
	P-26	A-P	WHT-RED	
	P-11	A-R	WHT-ORN	
	P-27	A-S	WHT-YEL	
	P-12	A-T	WHT-GRN	
	P-28	A-U	WHT-BLU	
		A-V (GND)	BLACK	22 AWG
1	P-2	B-D	WHITE	MICRO-DOT
	P-18	B-E	BLU	CABLE
	P-4	B-F	RED	
2	P-3	B-H	WHT	
	P-19	B-J	BLACK	
3	P-20	B-L	WHT	
	P-5	B-M	BLUE	
	P-21	B-N	RED	
4	P-6	B-P	WHITE	
	P-22	B-R	BLACK	
5	P-7	B-S	WHITE	MICRO-DOT
C1 5	P-23	B-T	BLACK	CABLE

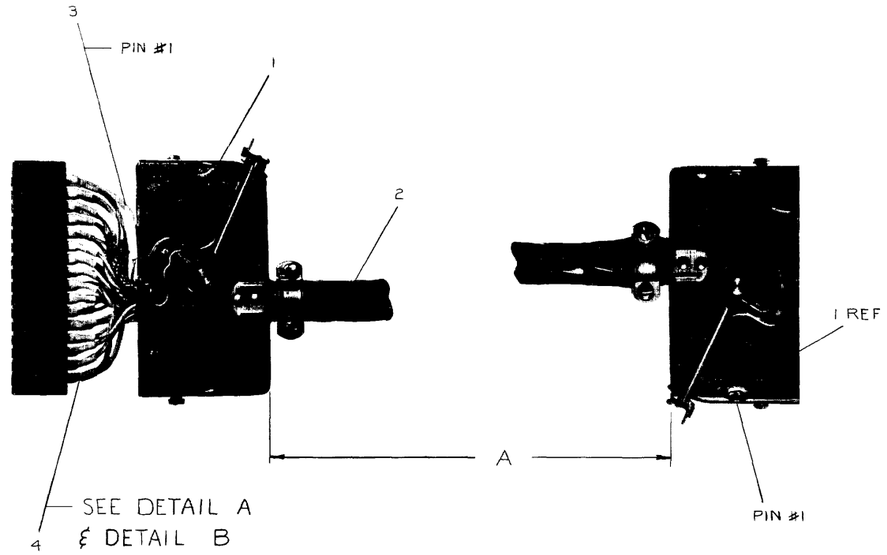
27	HY SHRINK TUBING #14 X 1/2 LG		7
5	CABLE, 3 CONDUCTOR X 6 FEET LONG		6
5	HY SHRINK TUBING #18 X 1/2 LG		5
1	W073 CABLE CONNECTOR FLIP CHIP	W073	4
1	SLEEVING VINYL EXTRUDED ASTRA 703/105 SIZE NO 1/2" X 6 FT LG		3
1	COPPER BRAID 3/8 DIA X 6 FT LONG		2
1	BLUE RIBBON CONN #26-4303-32S AMPHENOL		1

D-IA-7005187-0-0 LINC Tape Unit Cable



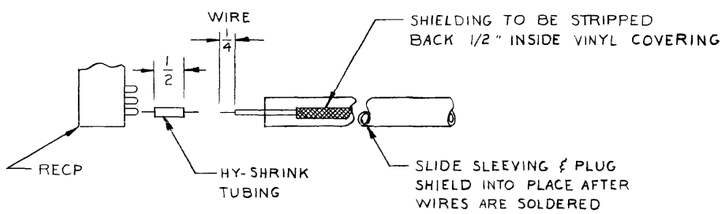
D-UA-7005260-0-0 Tape Transport

LEGEND	
NUMBER	"A" DIM
D-IA-7005423-1-0	18
D-IA-7005423-2-0	48

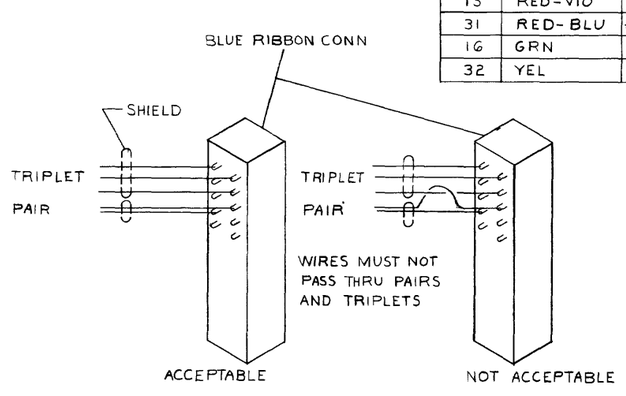


	PIN#	COLOR	WIRE
	1	SHIELD	#18 AWG
	17	ORN-YEL	#18 AWG
PAIR DOUBLE SHIELD TRIPLET DOUBLE SHIELD	2	BLK-ORN	#22 AWG
	18	BLK-YEL	↑
	3	BLU	
	19	VIO	
	4	GRY	
TRIPLET	20	RED-BRN	
	5	BRN-ORN	
	21	BRN-YEL	
PAIR	6	BLK-BRN	
	22	BLK-RED	
PAIR	7	BRN-VIO	
	23	BRN-GRY	
PAIR	8	BLK	
	24	BRN	
PAIR	9	BLK-GRN	
	25	BLK-BLU	
PAIR	10	RED	
	26	ORN	
PAIR	11	BRN-GRN	
	27	BRN-BLU	
PAIR	12	BLK-VIO	
	28	BLK-GRY	
	13	RED-YEL	
	29	RED-GRN	
	14	RED-GRY	
	30	RED-ORN	
	15	RED-VIO	↓
	31	RED-BLU	#22 AWG
	16	GRN	#18 AWG
	32	YEL	#18 AWG

NOTES:



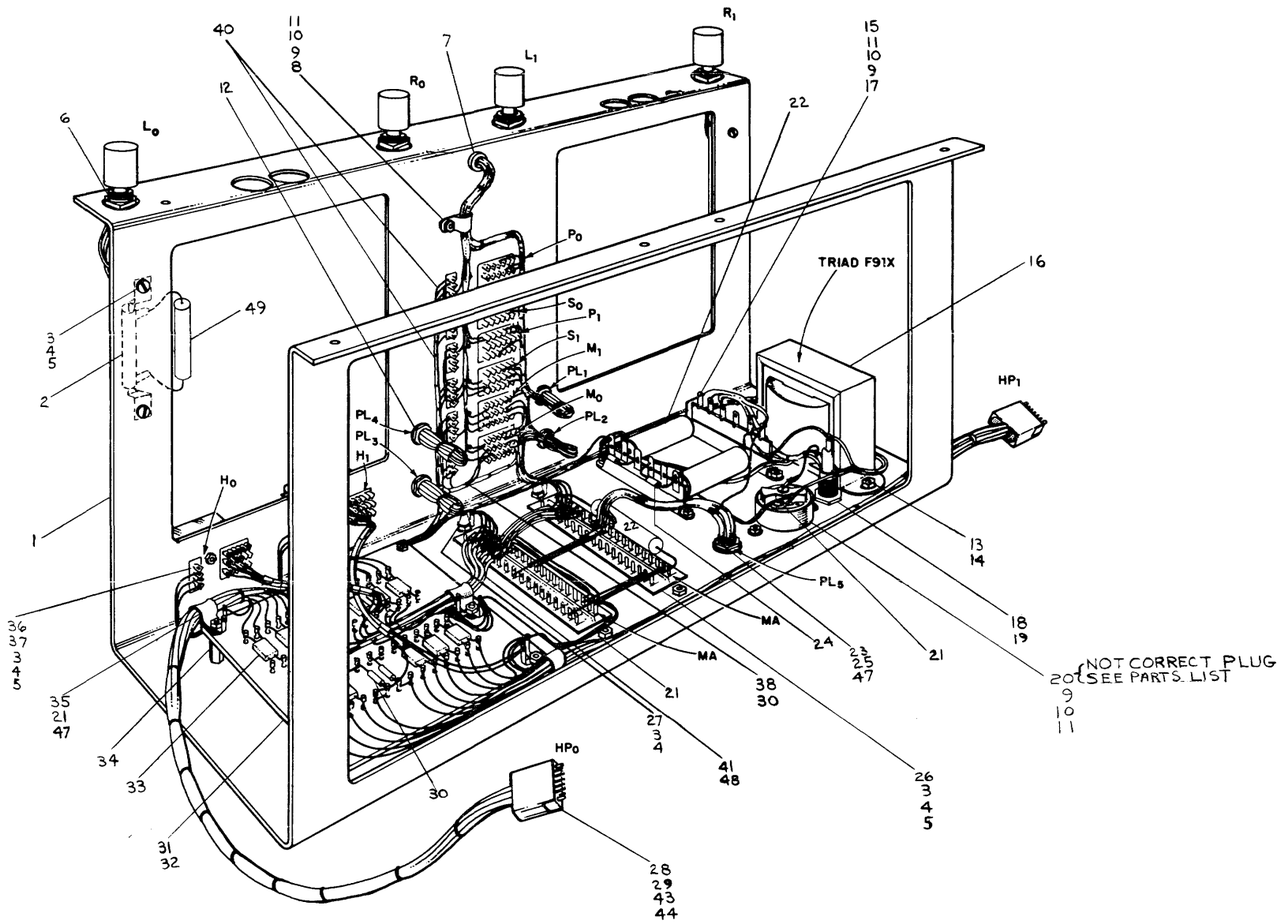
DETAIL "A"



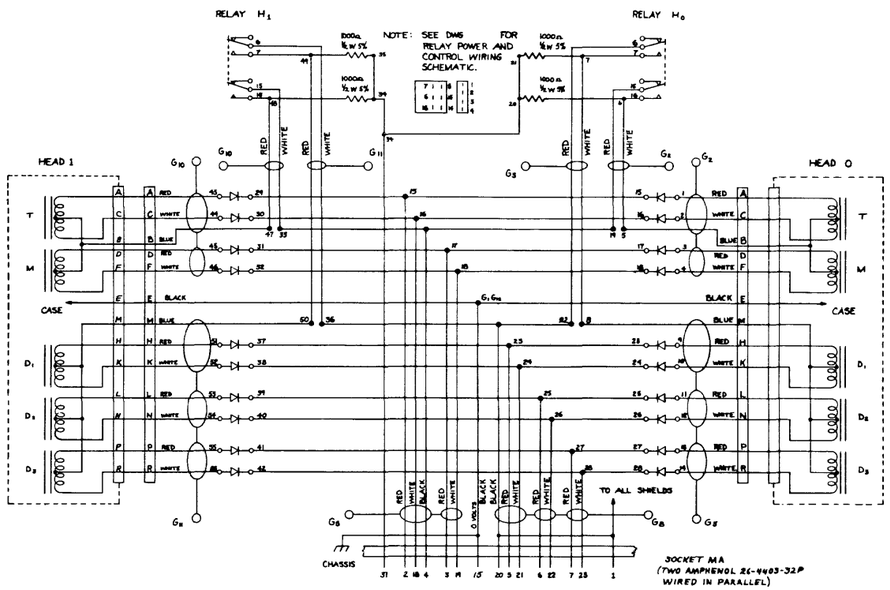
DETAIL "B"

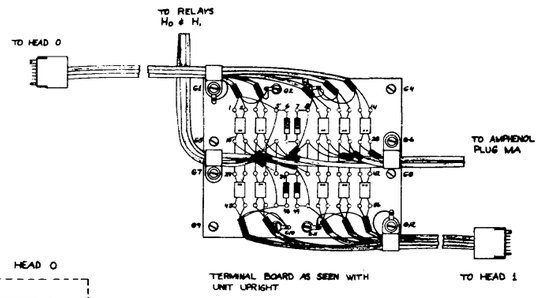
64	HY-SHRINK TUBING WHITE 1/2 LG		4
2	SLEEVING WHITE VINYL #18 AWG 2 LG		3
A/R	LINC SHIELDED CABLE DEC 9105605		2
2	BLUE RIBBON CONN #EG-4303-325 AMPHENOL		1

D-IA-7005423-0-0 LINCtape Extension Cable



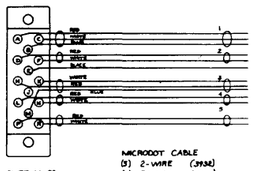
D-AD-7404146-0-0 Tape Chassis (Sheet 1)





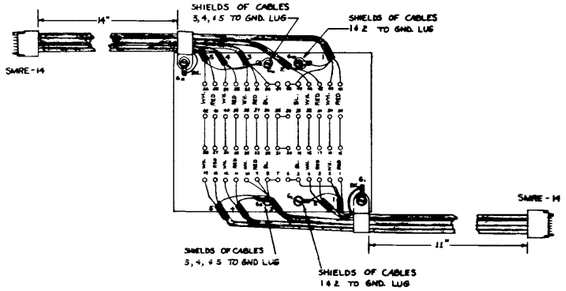
D-AD-7404146-0-0 Tape Chassis (Signal Wiring) Sheet 3

TAPE HEAD CABLE ASSEMBLY



MICRODOT CABLE
(2) 2-WIRE (3934)
(2) 3-WIRE (3937)
(1) # 26 STRANDED WIRE WITH BLACK TEFLON INSULATION

1. MAKE 2 PER CHASSIS. ONE WITH 18" CABLE & ONE WITH 16" CABLE.
2. SHIELDS MAY NOT CONTACT ONE ANOTHER AT CONNECTOR END OF CABLE.
3. FOR CONNECTOR END, USING MODIFIED WINCHESTER SMRE-14 H HOOD WITH ENLARGED CABLE OPENING.
4. DO NOT STRIP OTHER END OF CABLE.
5. ALL CABLE CLAMPS 5/8"



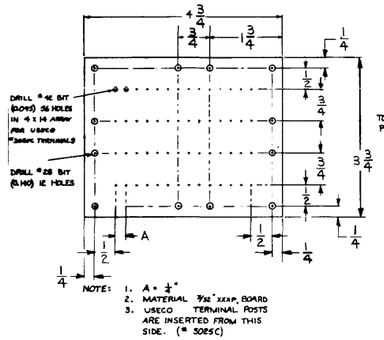
JUMPERS AND CONNECTIONS ON LOWER LANDS OF TERMINALS.

NOTES ON PREPARATION OF ENDS OF MICRODOT SHIELDED CABLE.

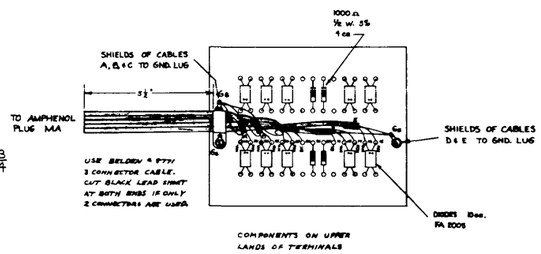
1. STRIP OUTER INSULATION BACK ABOUT 1" LEAVING SHIELD EXPOSED.
2. STRIP OFF ABOUT 3/16" OF SHIELD
3. WRAP EXPOSED SHIELD WITH 4 TURNS #24 AWG SOLDER, BEING OUT END OF WIRE WRAP ABOUT 3" IF REQUIRED.
4. INSULATE WRAPPED SHIELD WITH SHRINK FIT TUBING AND INSULATE #24 WIRE WITH SLEEVING.

NOTES ON PREPARATION OF BELDEN SHIELDED CABLE.

1. STRIP OUTER INSULATION BACK AS REQUIRED AND REMOVE FOIL.
2. USE DRAIN WIRE FOR SHIELD GROUND CONNECTION WHEN REQUIRED.
3. INSULATE SHIELD END AND DRAIN WIRE AS ABOVE.

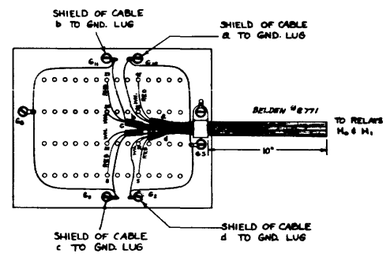


NOTE: 1. A = 1/2"
2. MATERIAL 3/32" XXXP, BOARD
3. USECO TERMINAL POSTS ARE INSERTED FROM THIS SIDE. (# 3085C)



USE BELDEN # 8771 3 CONNECTOR CABLE. CUT BLACK LEAD SHORT AT BOTH ENDS IT ONLY 2 CONNECTIONS ARE USED

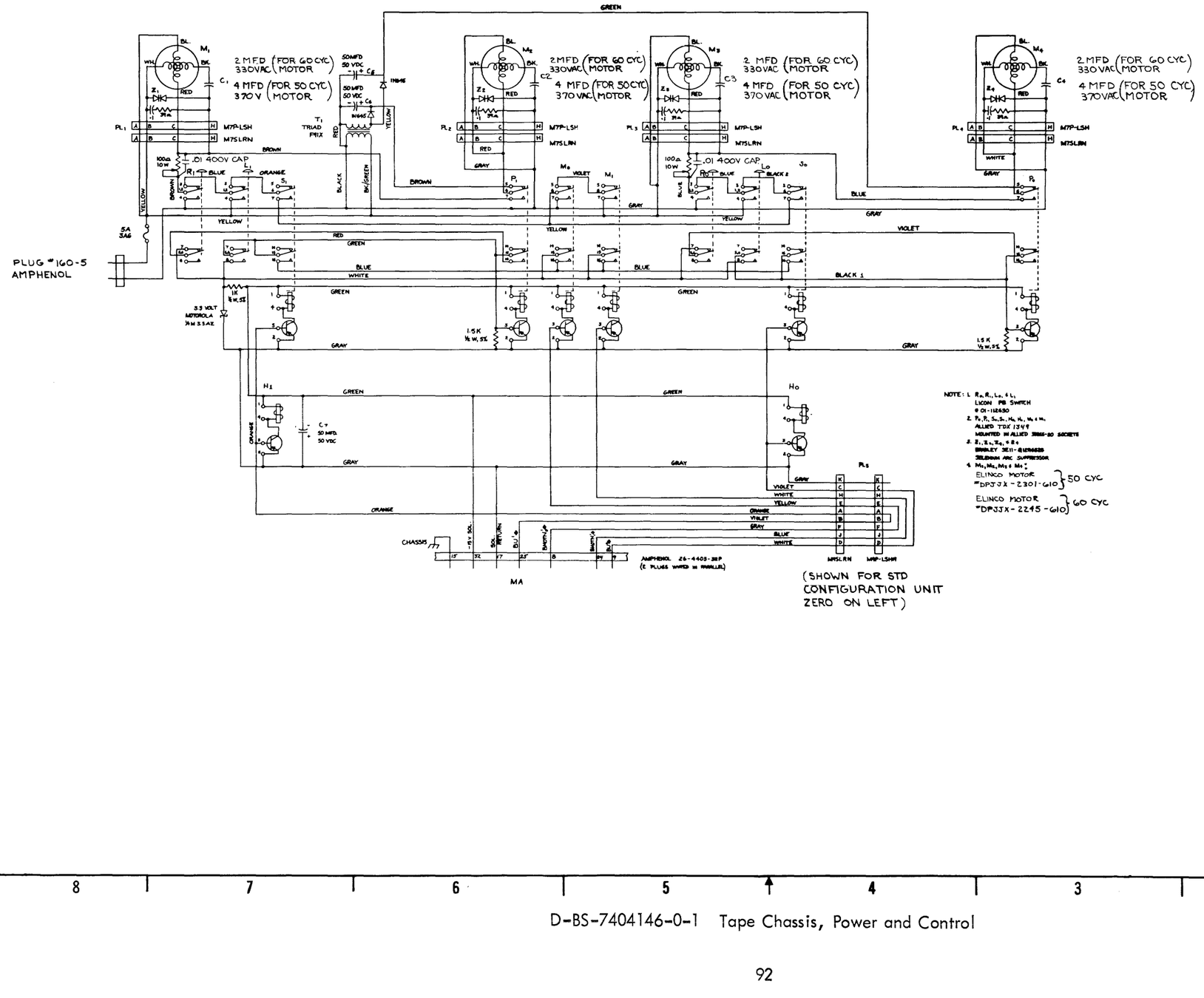
COMPONENTS ON UPPER LANDS OF TERMINALS



NOTE: OBSERVE SHIELD AND GROUND CONNECTIONS ACCURATELY.

DEC FORM NO.
DRD 100 (ELLCOVEL 103 PLAIN)

D-AD-7404146-0-0 Tape Chassis (Signal Wiring) Sheet 4

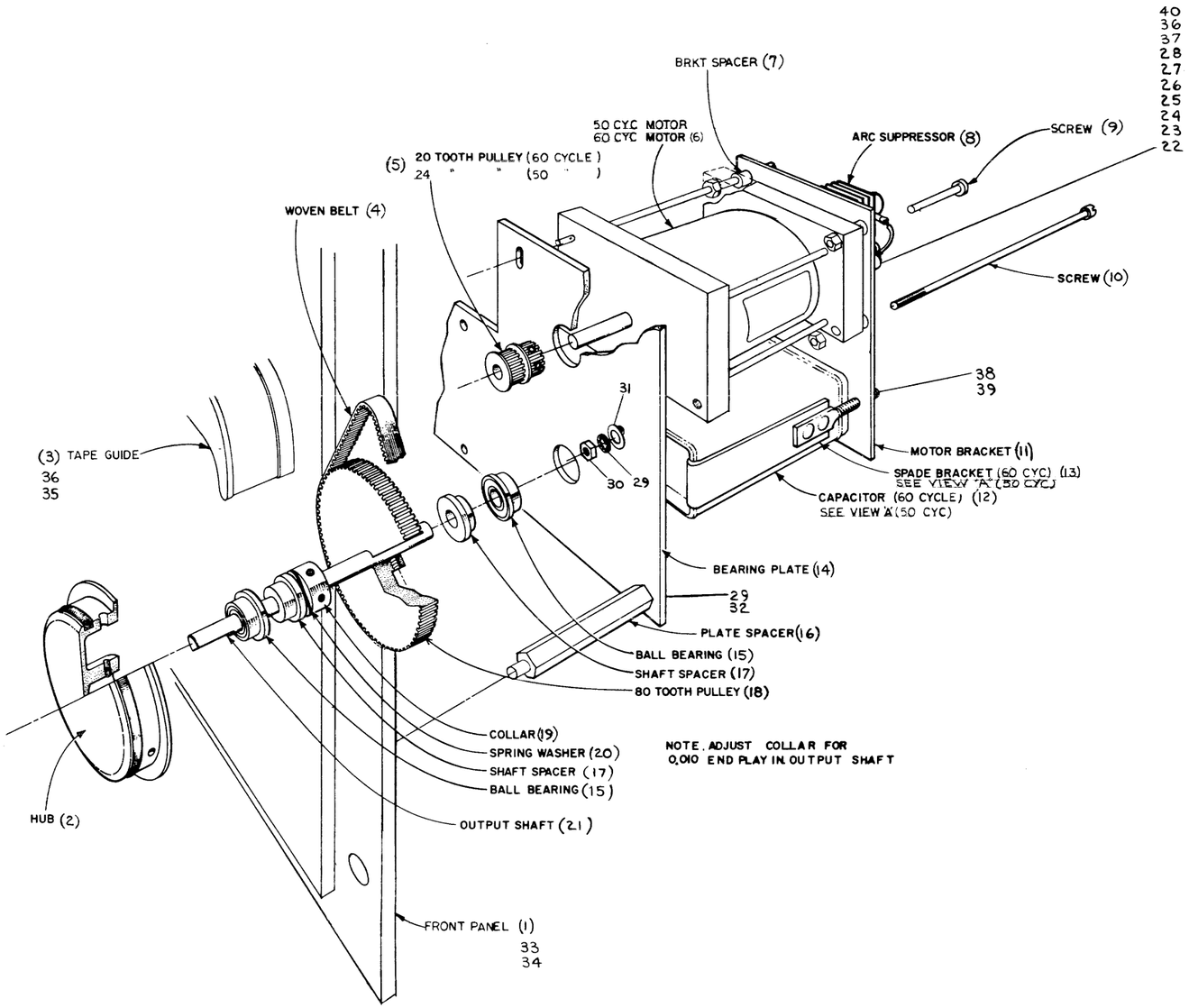


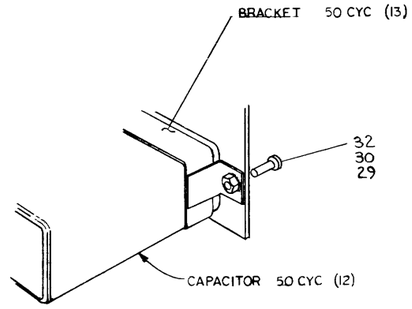
D-BS-7404146-0-1 Tape Chassis, Power and Control

NOTES:

1 USE STAINLESS ST. SET SCREWS IN A— PULLEYS & BEARINGS.

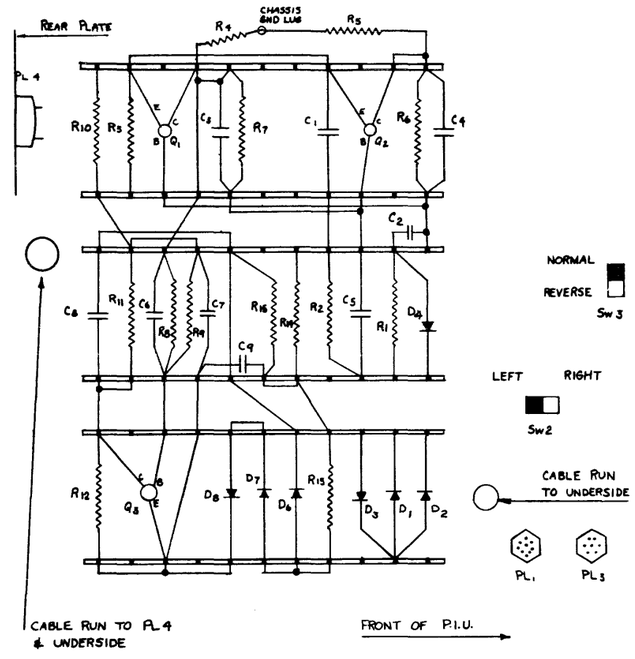
D-AD-7404150-1-0	60 CYCLE UNIT
D-AD-7404150-2-0	50 " "

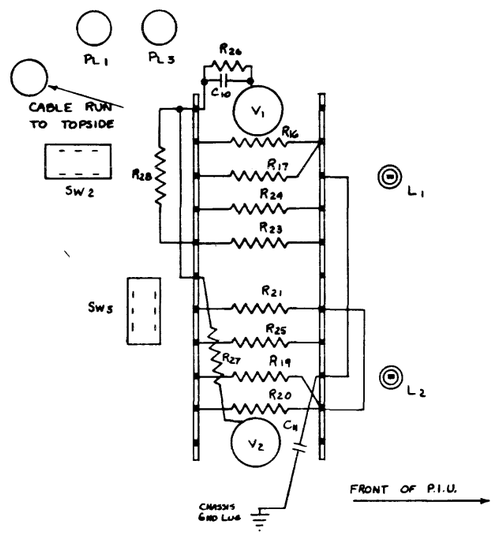




VIEW "A"

D-AD-7404150-0-0 Tape Drive (LINC8)

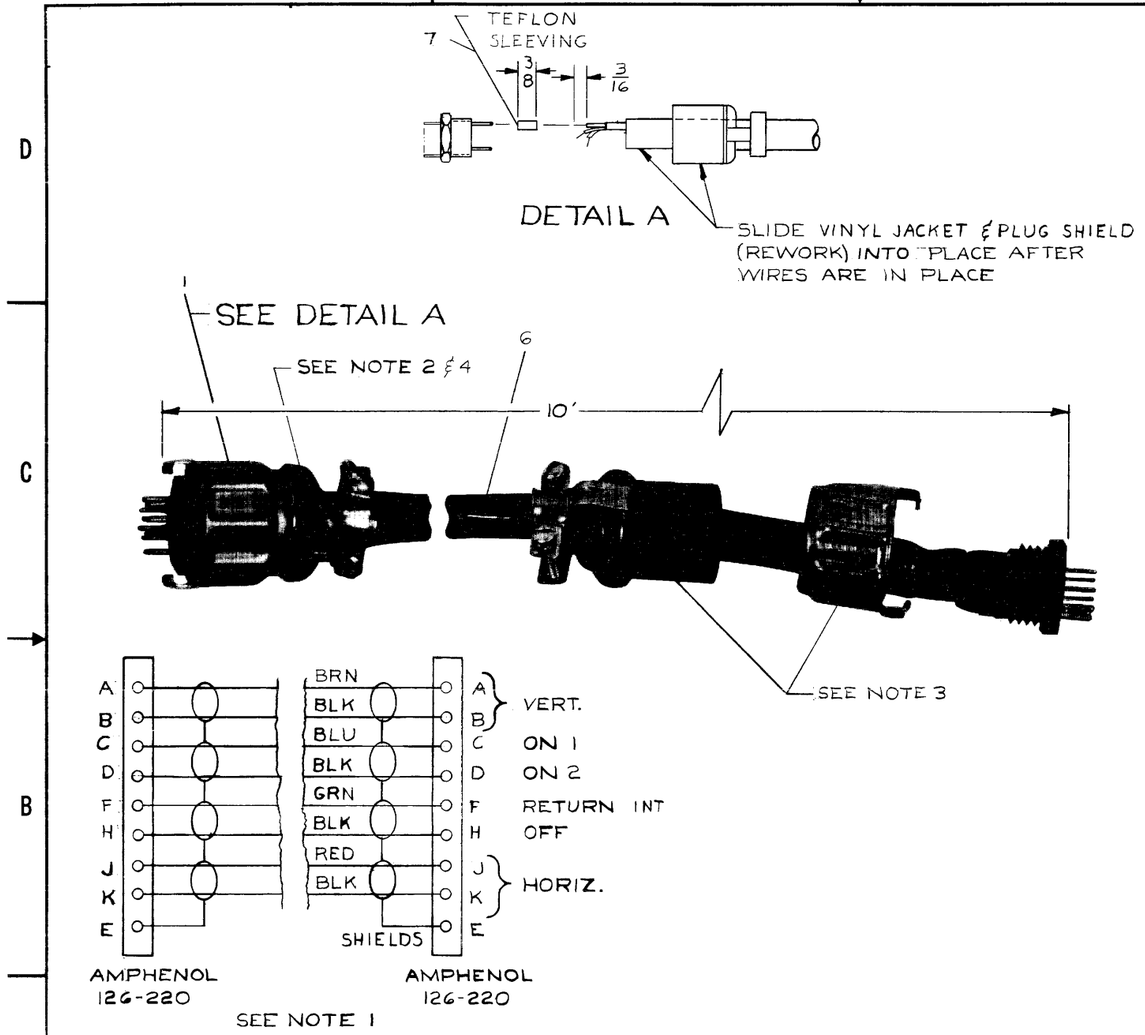




NOTES:

1. PART NUMBERS REFER TO PART NUMBER KEY DWG. # BS-D-3004810-01
2. CABLE RUNS SHOWN IN LAYOUT DWG. # AD-D-7404538-0-0 SHEET 4.

D-BS-7404538-0-1 Scope Plug-In (Component MTG)



NOTES:

1. THIS CABLE IS USED TO CONNECT THE REMOTE SCOPE TO THE CONSOLE SCOPE WHEN THE REMOTE SCOPE IS USED AS A DISPLAY SCOPE. IT IS CONNECTED TO THE CONSOLE SCOPE AT PL_2 ON FRONT OF THE RIGHT PLUG IN AND TO THE REMOTE SCOPE AT PL_2 ON THE RIGHT PLUG IN.
2. DRILL 13/32 HOLE IN BACK OF BOTH PLUGS TO INSURE PROPER INSERT OF CABLE.
3. PLUG SHOWN APART FOR CLARITY IN ASSEMBLING ONLY.
4. ONLY FOUR OF THE SIX PAIRS OF WIRE IN THIS CABLE ARE USED. THE TWO UNUSED PAIRS ARE CUT OFF 1-1/2" ABOVE THE WIRES USED.

A/R	TEFLON SLEEVING 1/16 OD		7
1	CABLE BELDEN 8778		6
~~1~~	~~CABLE,3COND x 10 FT #202-4007 MICROBOT~~		5
~~3~~	~~CABLE,2COND x 10FT #202-3938MICRO~~		4
~~18~~	~~HYSHRINK TUBING #18 x 1/4(RED)~~		3
~~A/R~~	~~SLEEVING VINYL BLK 3/8 ID~~		2
2	HEX CONN(9COND) 126-220 AMPHENOL		1

C-IA-7405611-0-0 Cable, Scope (Remote)

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-LINC8-0-0		3	LINC8 ASSEMBLY
A-PL-LINC8-0-0		8	LINC8 PARTS LIST
B-OD-LINC8-0-13		1	OUTLINE DRAWING
	A		
D-FD-LINC8-0-30	L	1	FLOW DIAGRAM, LOAD
	W		
D-SD-LINC8-0-1	A	1	SYSTEM CONFIGURATION
	Y		
A-MDL-LINC8-0-L	S	1	LINC 8
A-MDL-LINC8-0-P	U	1	LINC 8 PROCESSOR
	S		
A-MDL-LINC8-0-M	E	1	LINC 8 MEMORY
D-BS-LINC8-0-2	L	1	DATA TERM. PANEL LOGIC
	A		
D-MU-LINC8-0-3	T	1	MODULE UTILIZATION LIST
A-PL-LINC8-0-3	E	1	MODULE PARTS LIST
	S		
D-IC-LINC8-0-4	T	2	CABLES FOR LINC8
D-IC-LINC8-0-5	R	1	I/O LISTINGS
	E		
D-IC-LINC8-0-6	V	1	CABLE LISTING
	I		
A-CP-LINC8-0-7	S	1	EXTERNAL COMPONENT LIST
	I		
D-FD-LINC8-0-9	O	2	MANUAL & AUTO OPERATIONS
	N		
A-PL-LINC8-0-8	S	18	MODULE PARTS LIST
D-IC-LINC8-0-10		1	POWER WIRING AC & DC
D-IC-LINC8-0-11		1	CABLE LAYOUT OF CONTROL PANEL
A-IC-LINC8-0-12		1	AC CABLES

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. D. ANDRUCHOW DATE 10-1-6
CHK'D. DAIGNEAULT DATE 10-1-66
ENG. R.J. Clayton DATE 10-1-66
PROJ. ENG. R.J. Clayton DATE 10-1-66
PROD. R.J. Clayton DATE 10-1-66
FIRST USED ON LINC 8
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
LINC 8

SIZE	CODE	NUMBER	REV.
A	ML	LINC8-0	

DIST.

DEC FORM NO. DRA 103

A-MDL-LINC8-0-0 Master Drawing List

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
RESISTOR	1.2K ¼W		PH18H	PH19E	
RESISTOR	470 Ω		PH18H	PH18B	
AC TERMINATOR	100Ω ¼W RES & .01MFD CAP		PH01U	PH01C	
" "	" "		PH01P	PH01C	
CAPACITOR	2MFD OR 2.2 MFD		PH05H(-)	PH05J(+)	
CAPACITOR	.01MFD 50V		PB30H	PB30C	
RESISTOR	30K ¼W		PH18F	PH20E	
AC TERMINATOR	100Ω&.01 CAP		LB08H	LB08C	
CAPACITOR	680 PF		PF24M	PF24D	
CAPACITOR	680 PF		PH36E	PH36F	
CAPACITOR	680 PF		PH10H	PH10J	
CAPACITOR	680 PF		PJ10H	PJ10J	
AC TERMINATOR	100Ω ¼W RES &.01MFD CAP		MF36F	GND	
" "	" "		MF36H	"	
" "	" "		MF36J	"	
" "	" "		MF36K	"	
" "	" "		MF36L	"	
" "	" "		MF36M	"	

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
A	2/67	11	RJC
B	REVISED & 9/67	REDRAWN 23	RJC

DRN. R.BERNIER DATE 9/66
CHK'D. DAIGNEAULT DATE 10/66
ENG. R.CLAYTON DATE 10/66
PROJ. ENG. R.CLAYTON DATE 10/66
PROD. R.CLAYTON DATE 10/66
FIRST USED ON LINC-8
SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
EXTERNAL COMPONENT LIST
FOR
LINC-8

SIZE	CODE	NUMBER	REV.
A	CP	LINC8-0-7	B

DIST.

DEC FORM NO. DRA 106

A-CP-LINC8-0-7 External Component List (Sheet 1)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
RESISTOR	100Ω ¼W		DA35K	GND	
"	"" "		DA35M	"	
"	"" "		DA35P	"	
"	"" "		DA35S	"	
"	"" "		DA35T	"	
"	"" "		DA35V	"	

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN.		DATE
CHK'D.		DATE
ENG.		DATE
PROJ. ENG.		DATE
PROD.		DATE
FIRST USED ON		
SCALE		
SHEET 2 OF 2		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
EXTERNAL COMPONENT LIST
FOR
LINC-8
DATA TERMINAL PANEL

SIZE	CODE	NUMBER	REV.
A	CP	LINC8-0-7	B

DIST.

DEC FORM NO.
DRA 106

A-CP-LINC8-0-7 External Component List (Sheet 2)

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
K-WL-LINC8-0-L9	H		WIRING LIST
D-MU-LINC8-0-L10	F	1	PANELS LE-LJ
D-MU-LINC8-0-L11	B	1	PANELS LA-LD
D-BS-LINC8-0-L2		1	B REGISTER
D-BS-LINC8-0-L3		1	S+P REGISTER
D-BS-LINC8-0-L4		1	LINC, LEFT HALF A REGISTER
D-BS-LINC8-0-L5		1	RIGHT HALF A REGISTER
D-BS-LINC8-0-L6	A	1	R & Z REGISTERS
D-BS-LINC8-0-L7	A	1	PDP-8 AC INPUT GATES
D-BS-LINC8-0-L14		1	CONTROL REG. + INST DECODERS
D-BS-LINC8-0-L15	A	1	TIME PULSE DISTRIBUTOR
D-BS-LINC8-0-L16	D	1	LINC INTERFACE CONTROL
D-BS-LINC8-0-L17	A	1	IOT DECODERS
D-BS-LINC8-0-L18	A	1	CONTROL FUNCTIONS
D-BS-LINC8-0-L19		1	SKIP NETS
D-BS-LINC8-0-L20	A	1	CONTROL PULSE GATES
D-BS-LINC8-0-L21		1	S P Z T N & DIS. CONT. PULSES
D-BS-LINC8-0-L22	A	1	A&B REGISTER CONTROL PULSES
D-BS-LINC8-0-L26	A	1	MEMORY EXTENSION
D-BS-LINC8-0-L28		1	LINC SWITCHES & INDICATORS
D-AD-7005108-0-0	A	1	BUSS BAR

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
A	11/66	3	R.J.C
B	12/66	6	R.J.C
C	1/67	9	R.J.C
D	2/67	10	R.J.C
E.	2/67	12	R.J.C
F	3/67	14	R.J.C
H	8/67	22	J.S.
J	9/67	24	J.S.

DRN. D. ANDRUCHOW		DATE 10-1-66
CHK'D. DAIGNEAULT		DATE 10-1-66
ENG. R.CLAYTON		DATE 10-1-66
PROJ. ENG. R.CLAYTON		DATE 10-1-66
PROD. R.CLAYTON		DATE 10-1-66
FIRST USED ON LINC 8		
SCALE		
SHEET OF		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
LINC 8
LINC SECTION

SIZE	CODE	NUMBER	REV.
A	ML	LINC8-0-L	J

DIST.

DEC FORM NO.
DRA 103

A-ML-LINC8-0-L Drawing List, LINC Section

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
K-WL-LINC8-0-M2	F		WIRING LIST
D-MU-LINC8-0-M3	C	1	PANELS MA-MD
D-MU-LINC8-0-M4	D	1	PANELS ME-MJ
D-BS-LINC8-0-M8		1	PDP-8 ADDR INPUT GATE
D-BS-LINC8-0-M9		1	MAG TAPE READER/WRITER
D-BS-LINC8-0-M10	A	1	MAG TAPE MOTION CONTROL
D-BS-LINC8-0-M11	A	1	MAG TAPE TIMING GEN.
D-BS-LINC8-0-M12	A	1	MAG TAPE MODE CONTROL
D-BS-LINC8-0-M13	B	1	MAG TAPE MARK WINDOW
D-BS-LINC8-0-M111	C	1	TELEPRINTER
D-BS-LINC8-0-M112		1	X AXIS SELECTION
D-BS-LINC8-0-M113		1	Y AXIS SELECTION
D-BS-LINC8-0-M115	B	1	SENSE AMPS, INHIBIT DRIVERS MEM. CONT.
D-BS-LINC8-0-M116		1	IN-OUT BUFFERS
D-AD-7005110-0-0		4	BUSS BAR

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
A	11/66	2	R.C.
B	12/66	5	R.C.
C	1/67	8	R.C.
D	1/67	8A	R.C.
E	2/67	11	R.C.
F	4/67	16	R.C.
H	6/67	17	R.C.
J	8/67	21	R.C.

DRN. Andruchow DATE 1/66
CHK'D. Daigneault DATE 1/66
ENG. R.Clayton DATE 1/66
PROJ. ENG. R.Clayton DATE 1/66
PROD. R.Clayton DATE 1/66
FIRST USED ON LINC 8
SCALE
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
LINC 8
MEMORY SECTION

SIZE	CODE	NUMBER	REV.
A	ML	LINC8-0-M	J

DIST

DEC FORM NO. DRA 103

A-ML-LINC8-0-M Drawing List, Memory Section

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
K-WL-LINC8-0-P2	E		WIRE LIST
D-MU-LINC8-0-P3	C	1	PANELS PE TO PJ
D-MU-LINC8-0-P4	C	1	PANELS PA TO PD
D-BS-LINC8-0-P23	A	1	DATA BITS ØØ-11 GATES
D-BS-LINC8-0-P24		1	ANALOG SYSTEM
D-BS-LINC8-0-P25		1	MB REGISTER MODS.
D-BS-LINC8-0-P27		1	PDP-8 SWITCHES & INDICATORS
D-BS-LINC8-0-P102	A	1	ACCUMULATOR
D-BS-LINC8-0-P103		1	AC CONTROL
D-BS-LINC8-0-P104		1	PC+MA REGISTERS
D-BS-LINC8-0-P105	A	1	MB REGISTER CONTROL
D-BS-LINC8-0-P106	A	1	MAJOR STATES & INSTRUCTION REG.
D-BS-LINC8-0-P108	A	1	MA, PC CONTROL
D-BS-LINC8-0-P109	B	1	TIMING, KEYS, SWS, & RUN
D-BS-LINC8-0-P110	B	1	INPUT-OUTPUT CONTROL
D-AD-7005109-0-0		1	BUS BAR

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
A	11/66	1	R.J.C
B	11/66	4	R.J.C
C	1/5/67	7	R.J.C
D	4/67	15	R.J.C
E	8/67	18	J.S.
F	8/67	19	R.C.
H	9/67	25	J.S.

DRN.D. ANDRUCHOW DATE 10-1-66
CHK'D. DAIGNEAULT DATE 10-1-66
ENG. R.J. Clayton DATE 10-1-66
PROJ. ENG. R.J. Clayton DATE 10-1-66
PROD. R.J. Clayton DATE 10-1-66
FIRST USED ON LINC 8
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

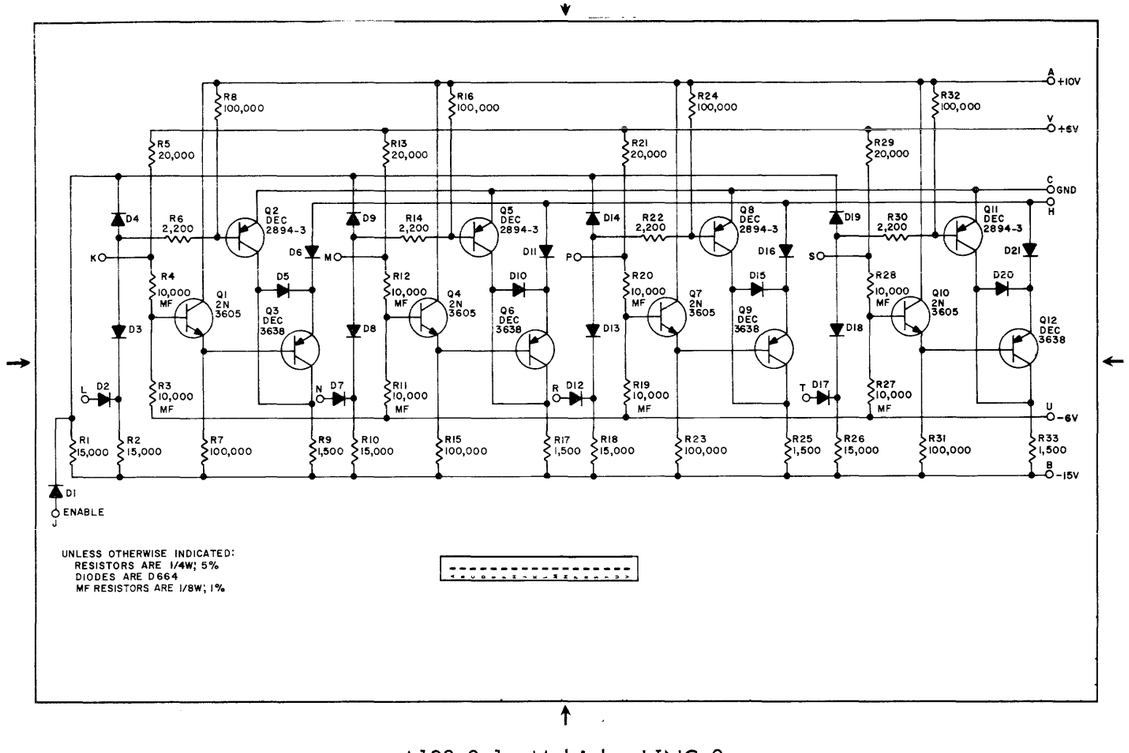
TITLE
LINC 8
PROCESSOR SECTION

SIZE	CODE	NUMBER	REV
A	ML	LINC8-0-P	H

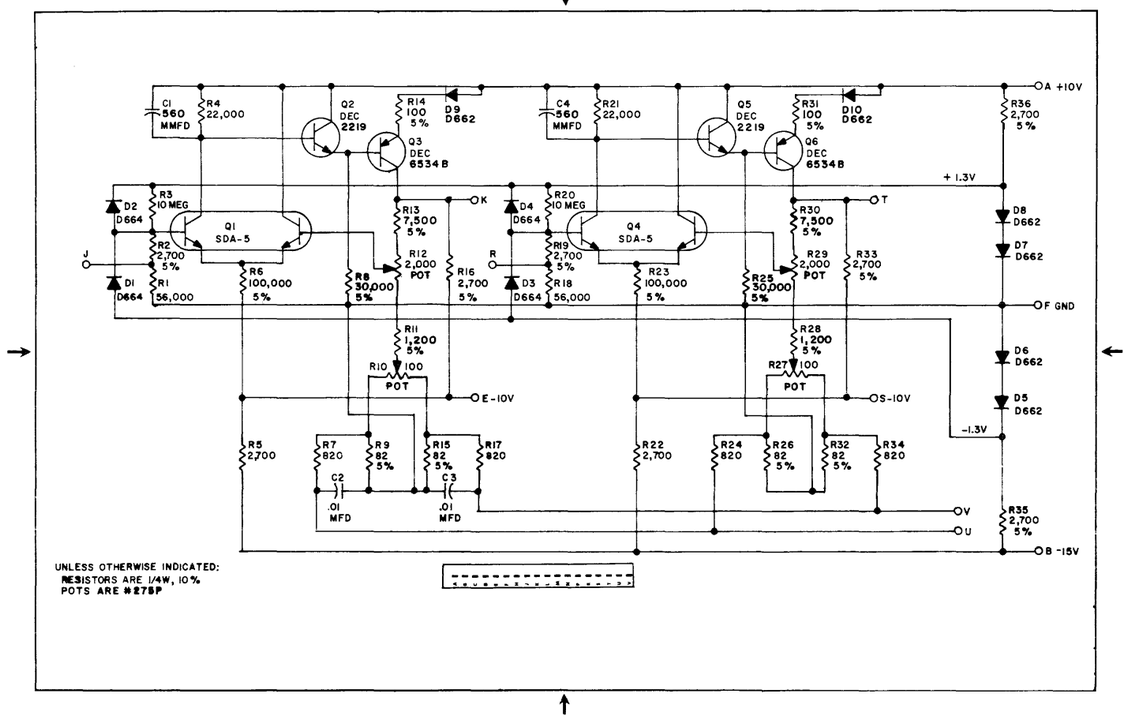
DIST.

DEC FORM NO. DRA 103

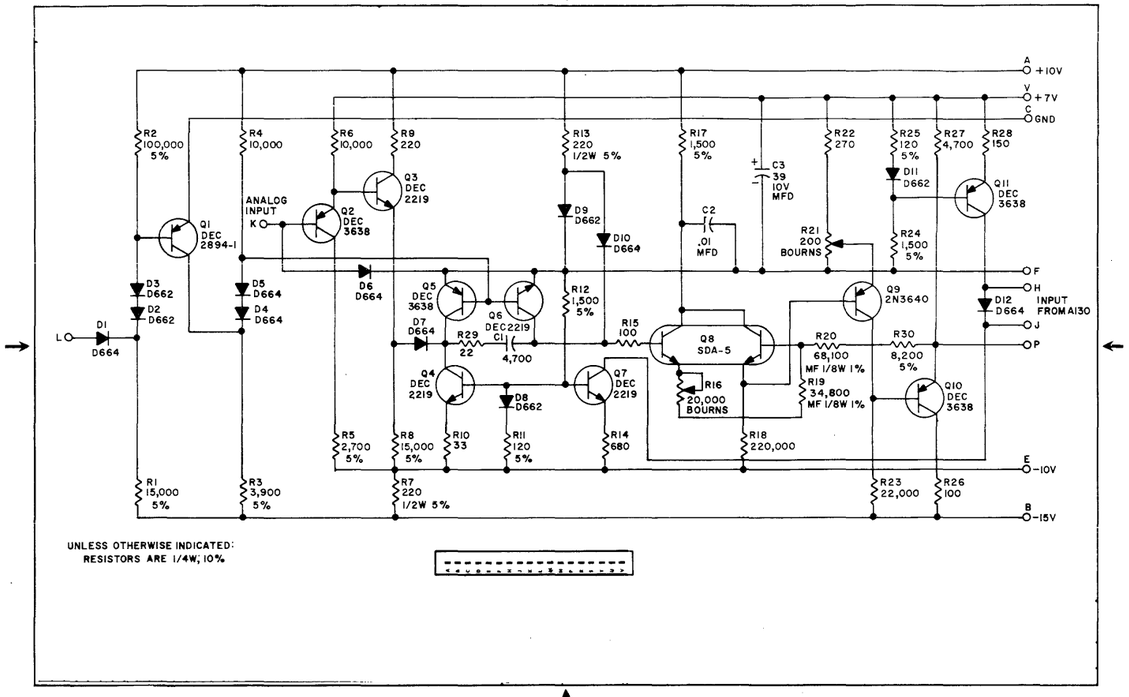
A-ML-LINC8-0-P Drawing List, Processor Section



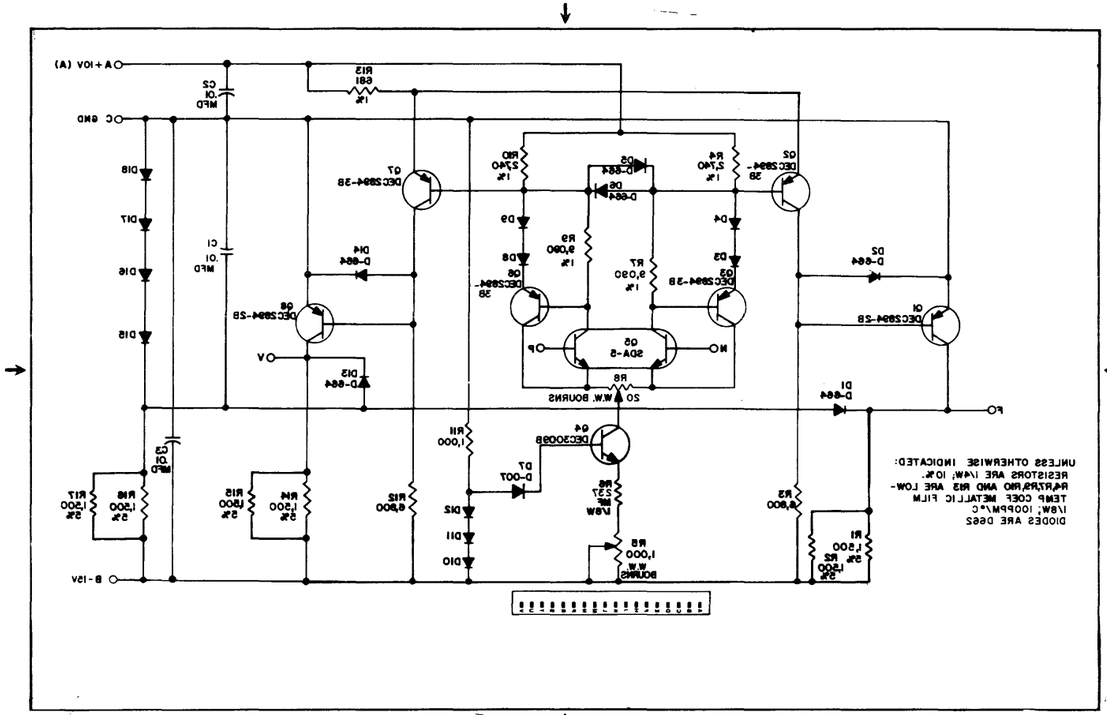
A130-0-1 Multiplex LINC-8



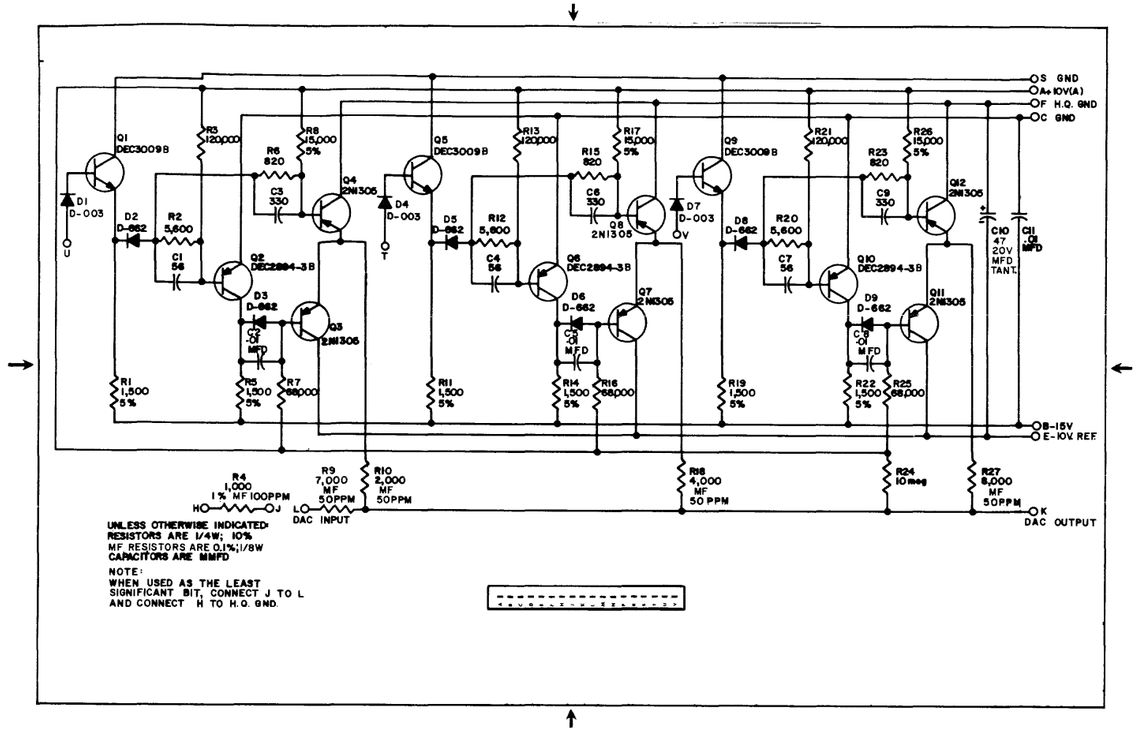
A202-0-1 Two Analog Preamplitiers



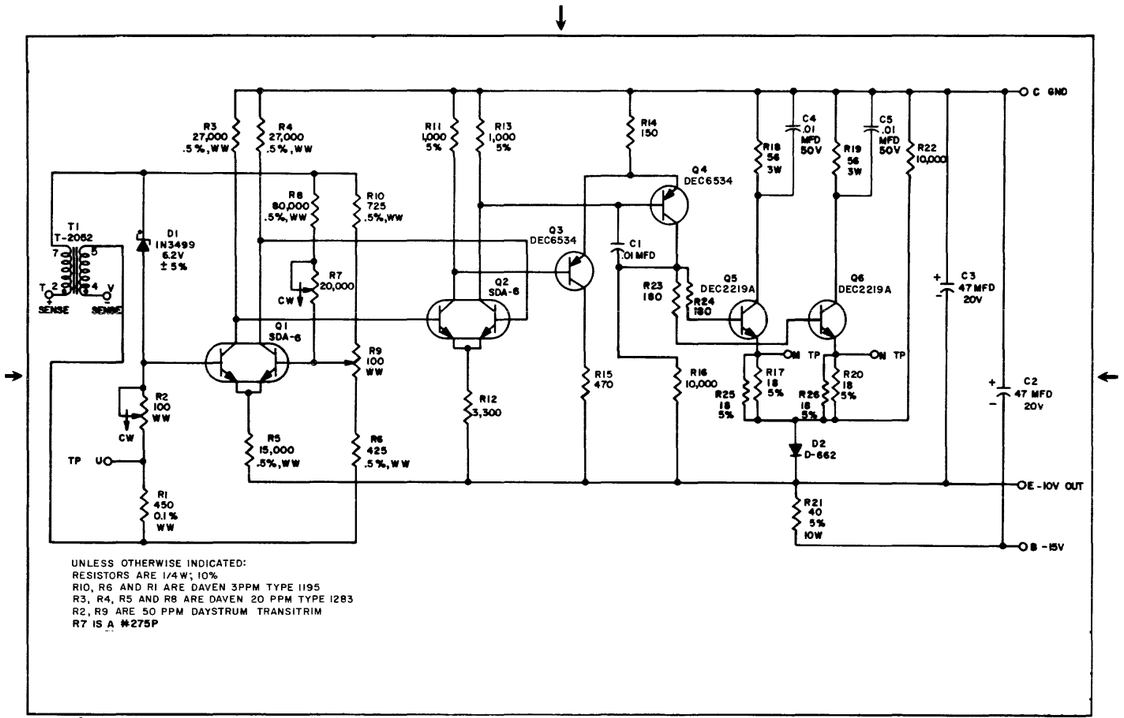
A401-0-1 Sample and Hold



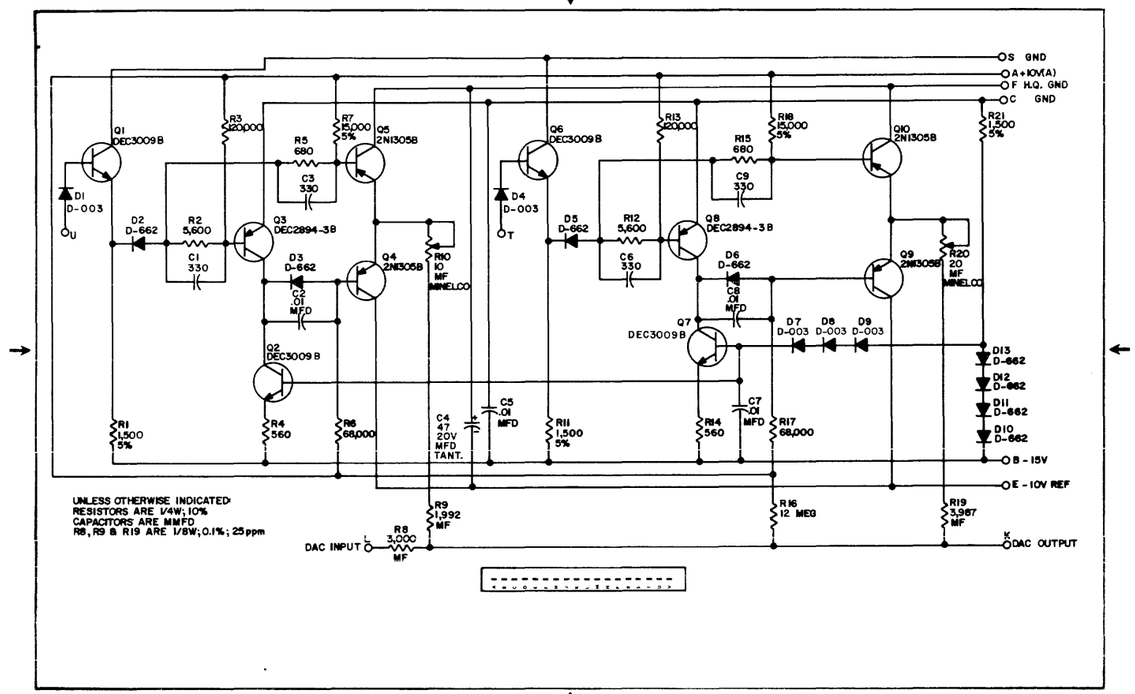
A502-0-1 Difference Amplifier



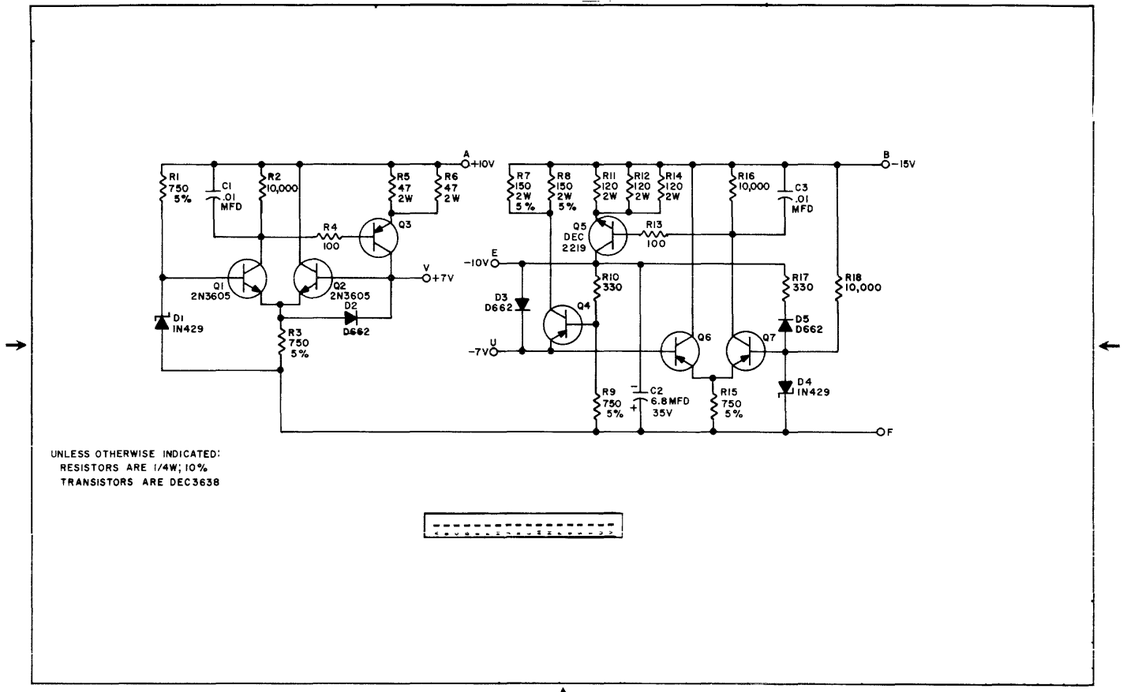
A601-0-1 3 Bit DAC



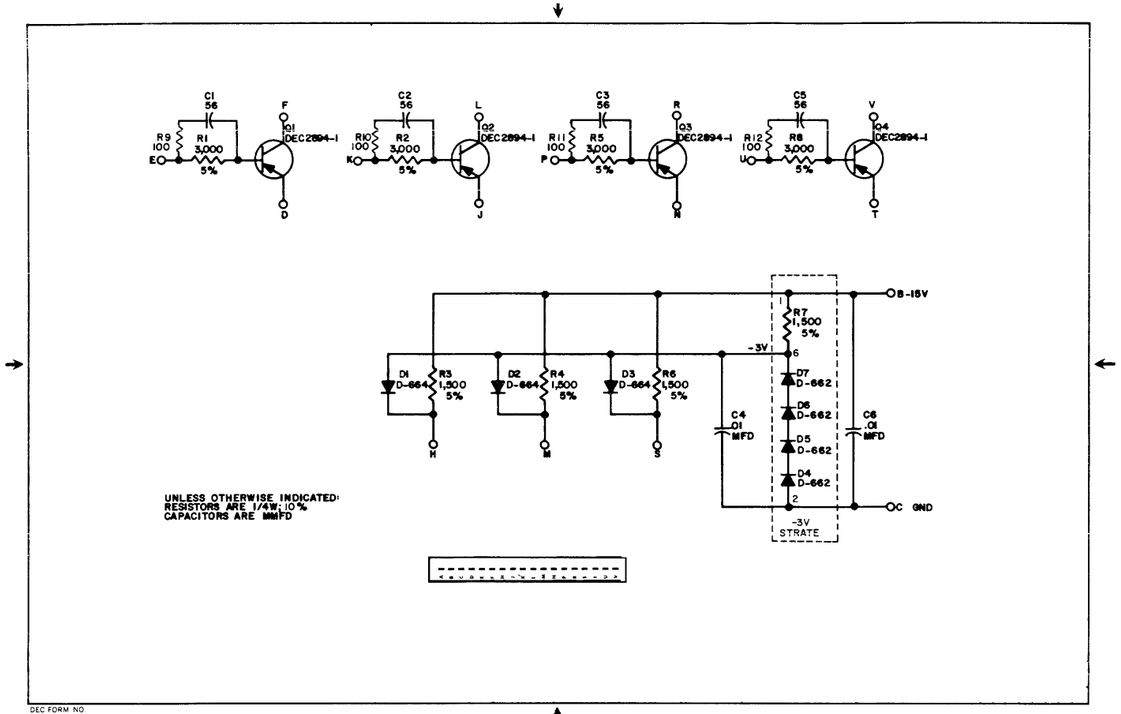
A704-0-1 -10V Precision Power Supply



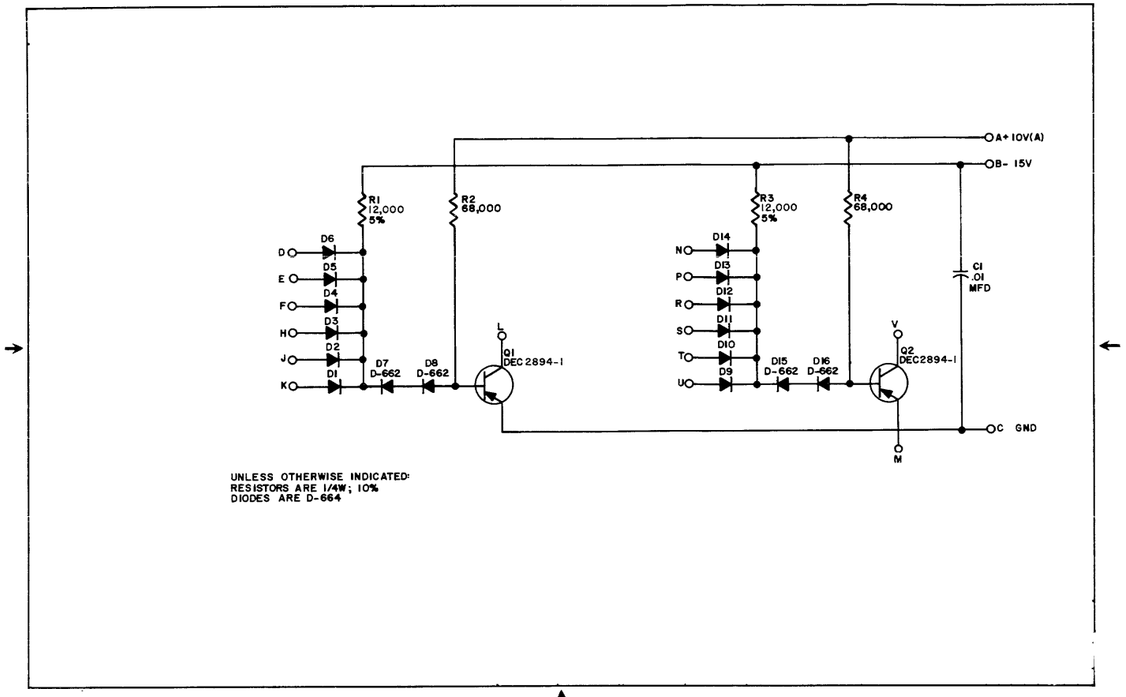
A604-0-1 2 Bit DAC



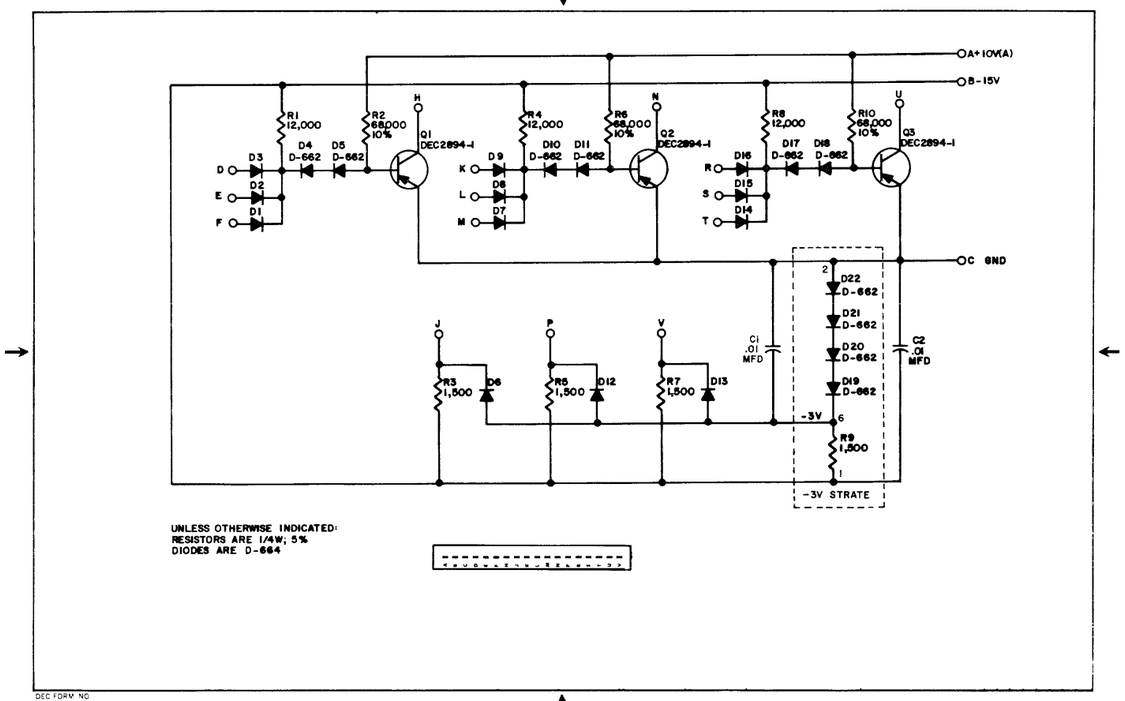
A706-0-1 Power Supply for A202



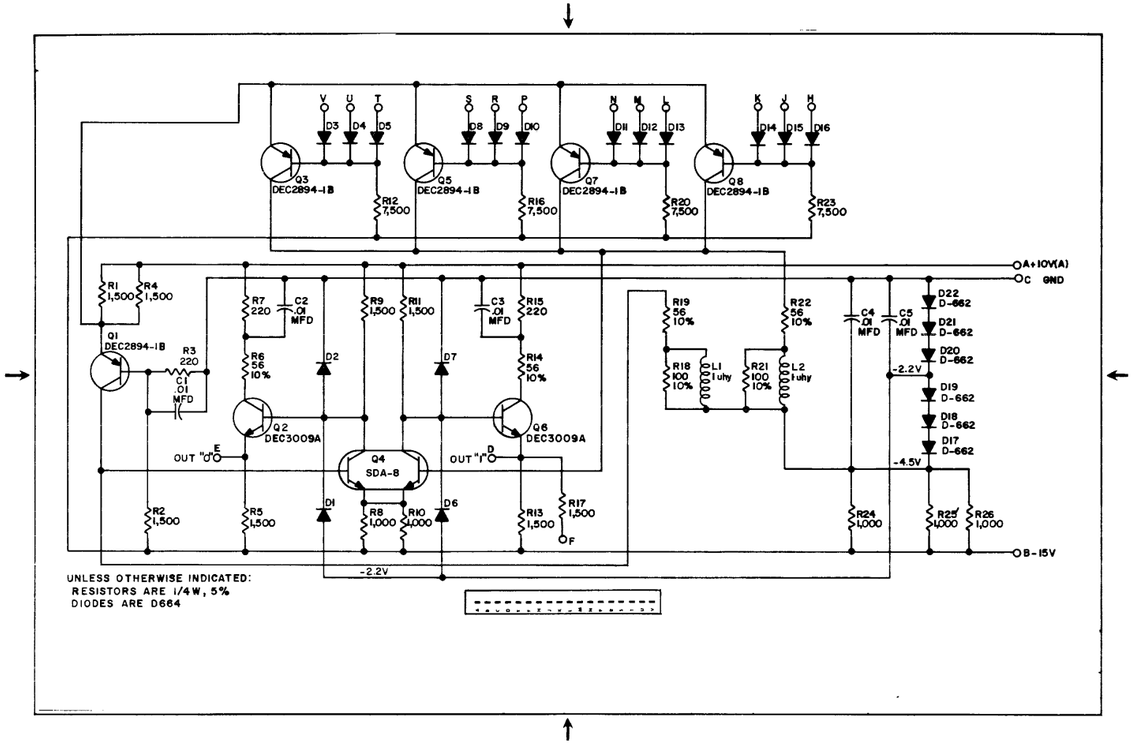
B104-0-1 Inverter



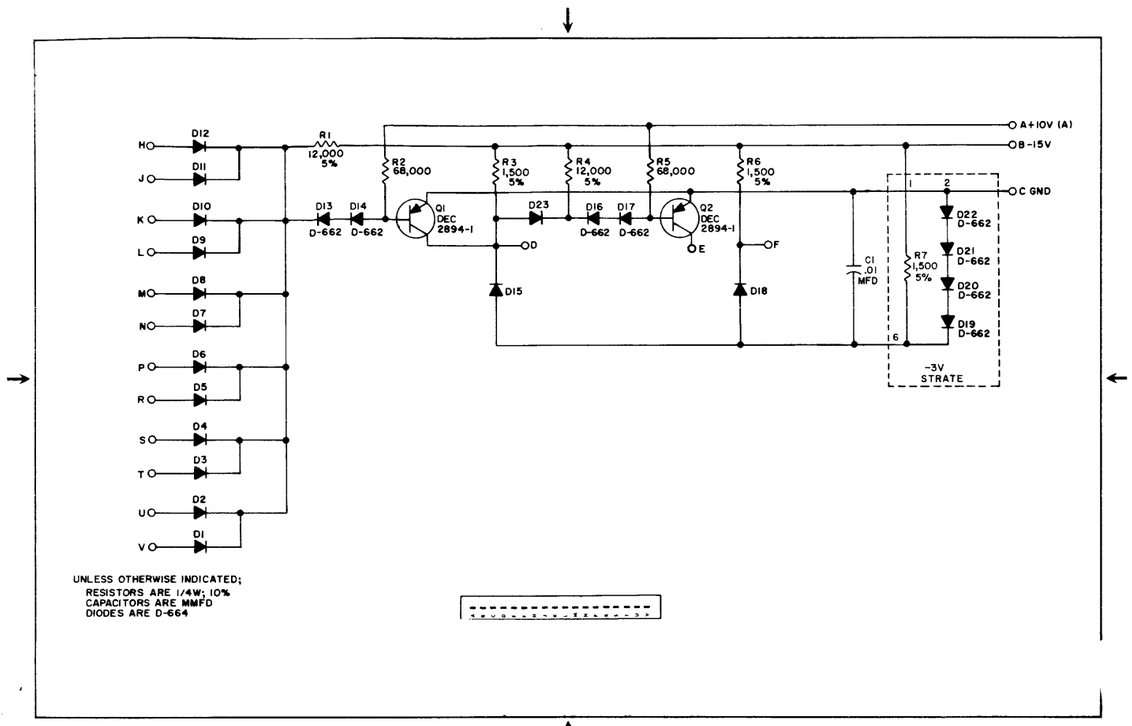
B117-0-1 Diode Gate



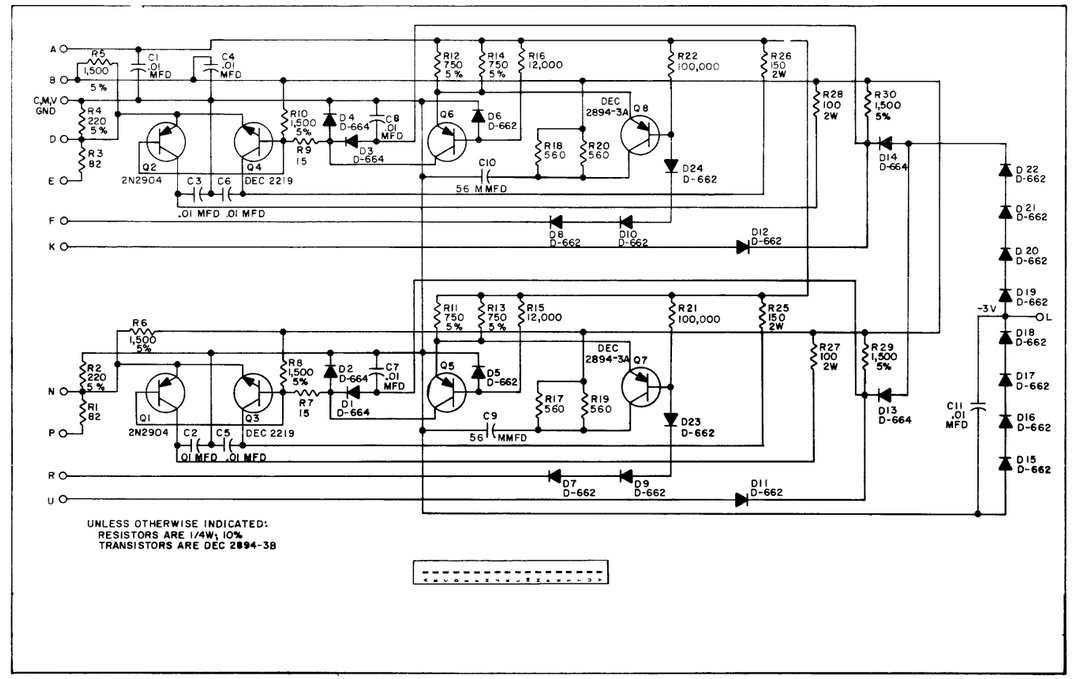
B115-0-1 Diode Gate



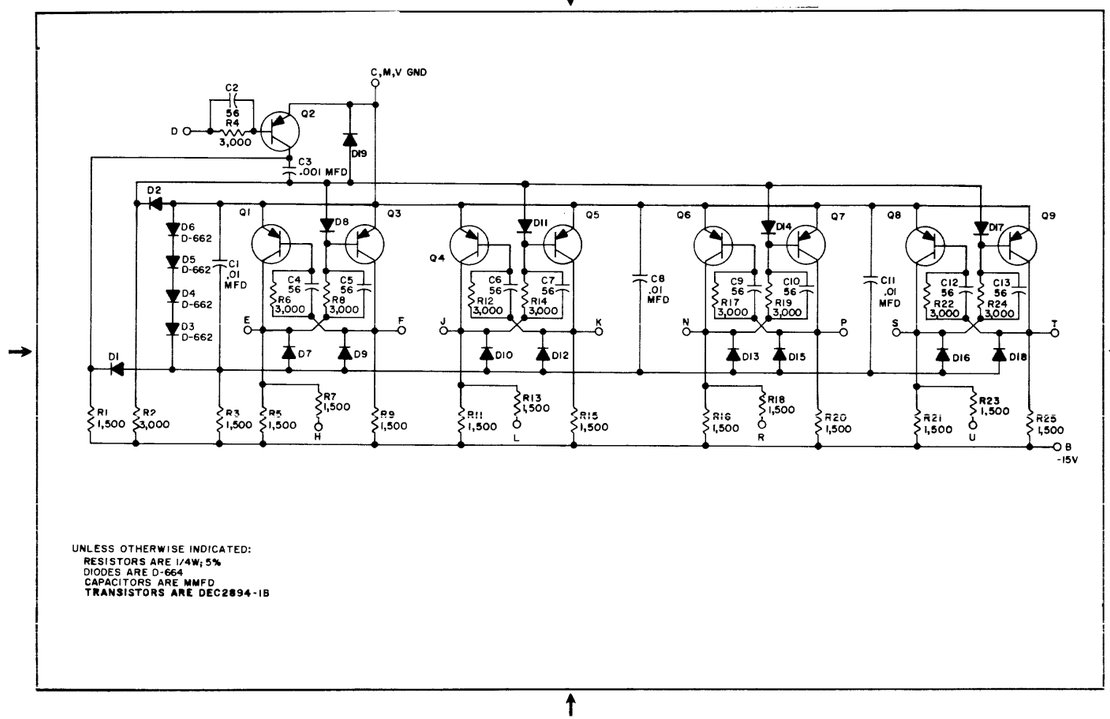
B130-0-1 3Bit Parity Circuit



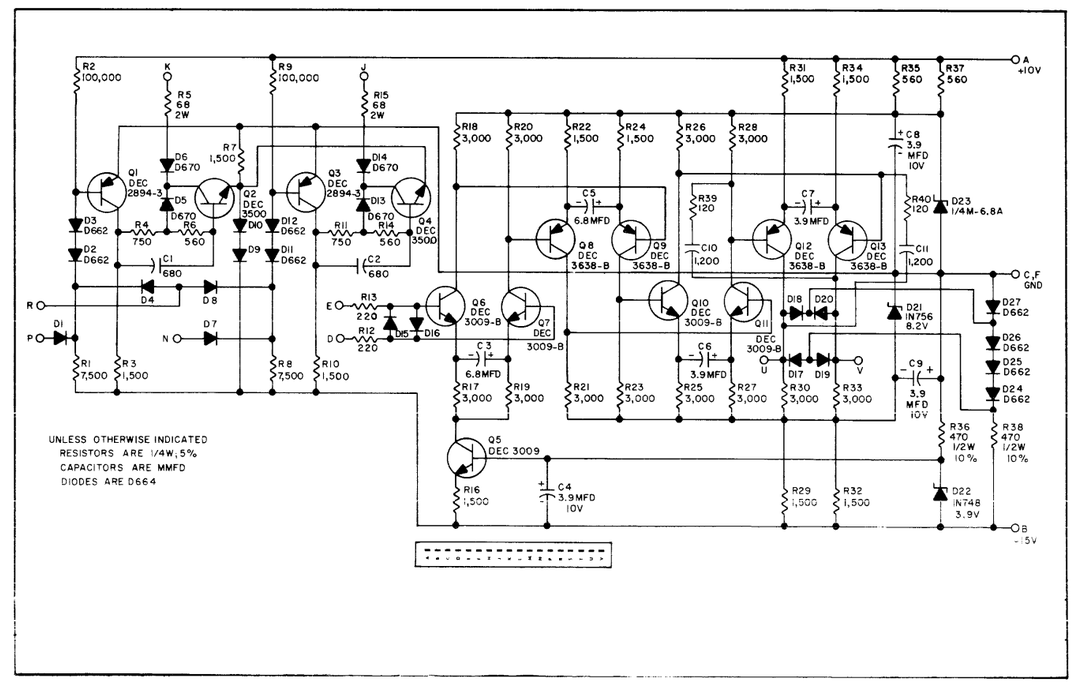
B171-0-1 Diode Gate



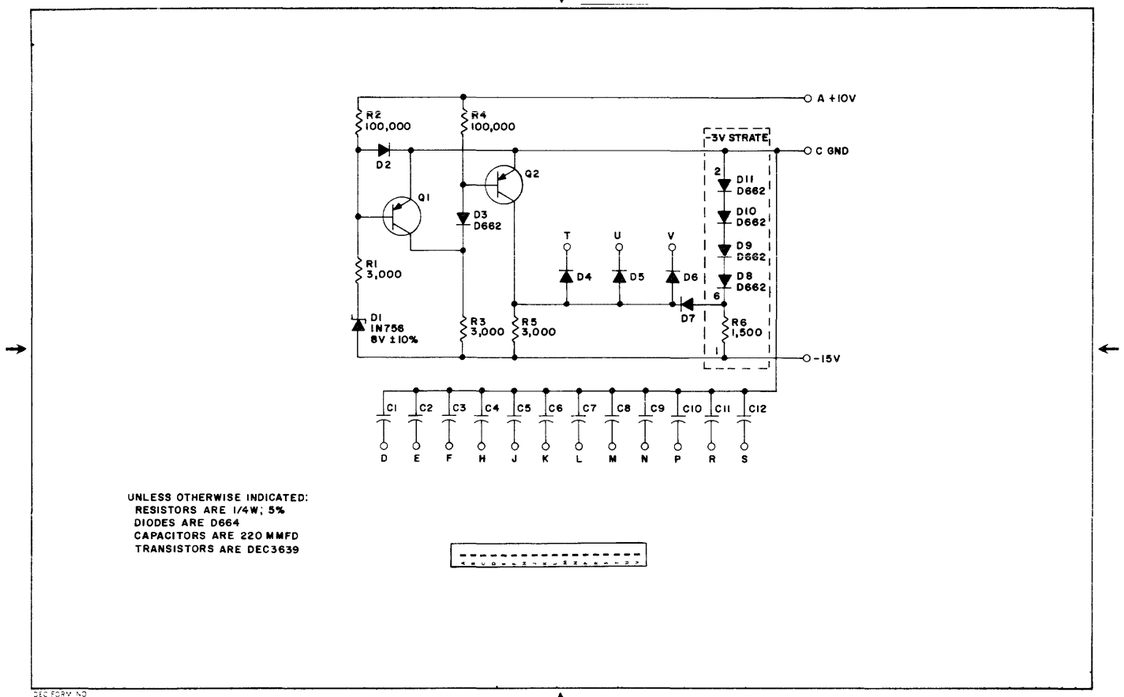
B684 Two Bus Drivers



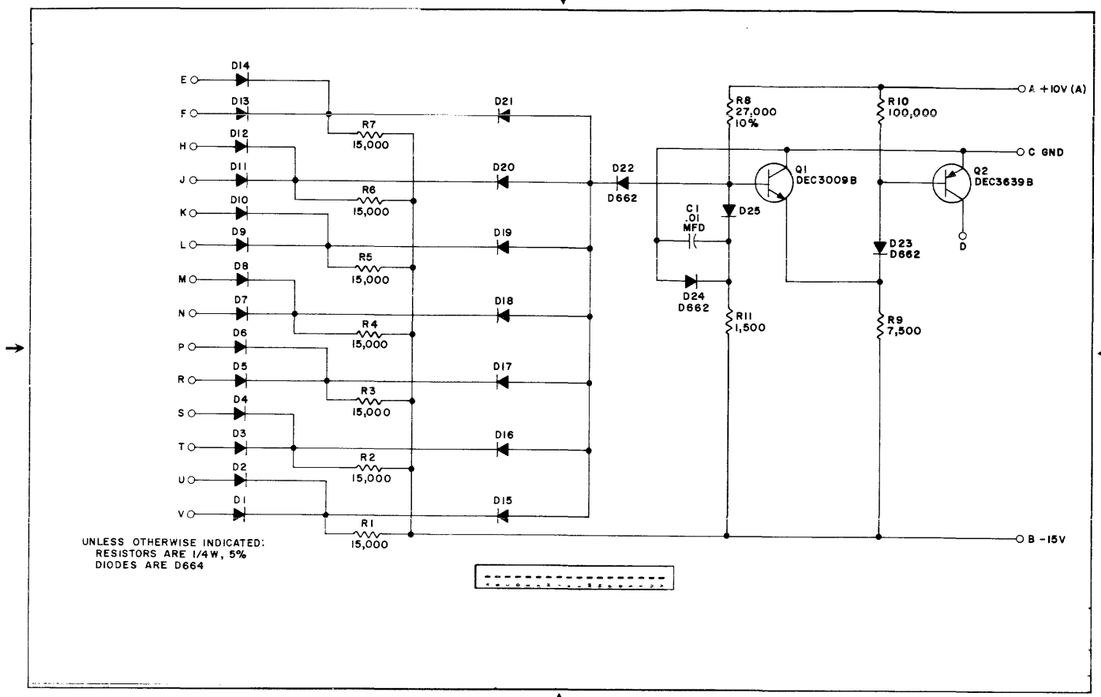
B204-0-1 Four Flip-Flops



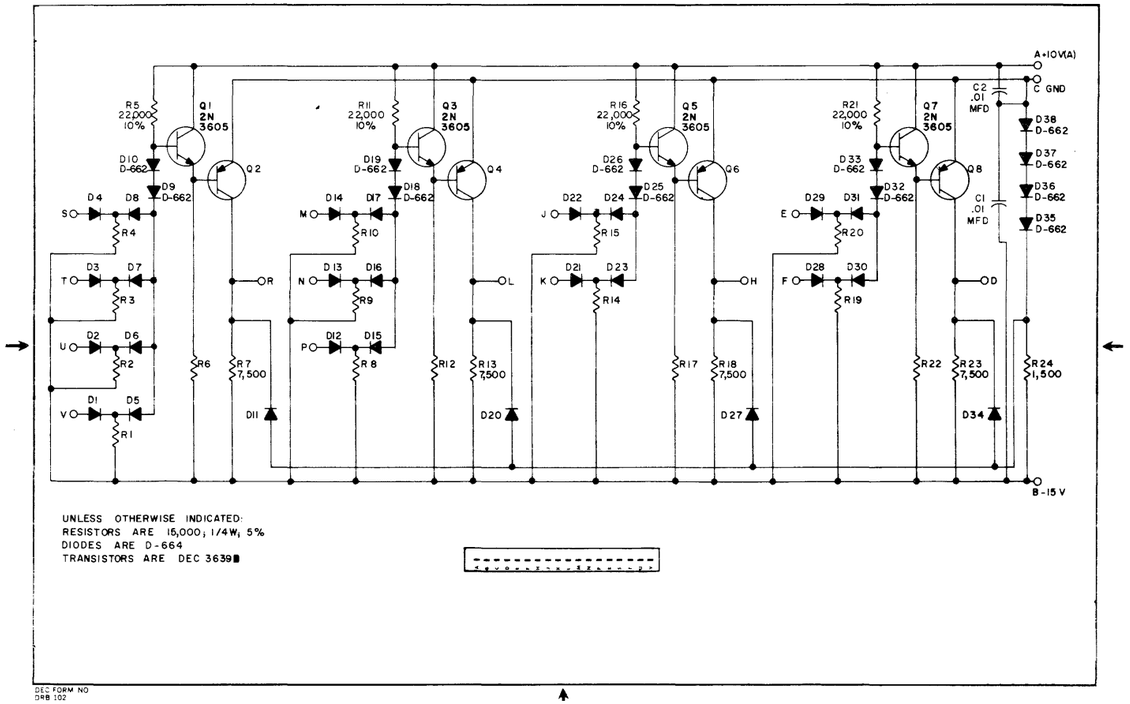
G882 Manchester Reader Writer



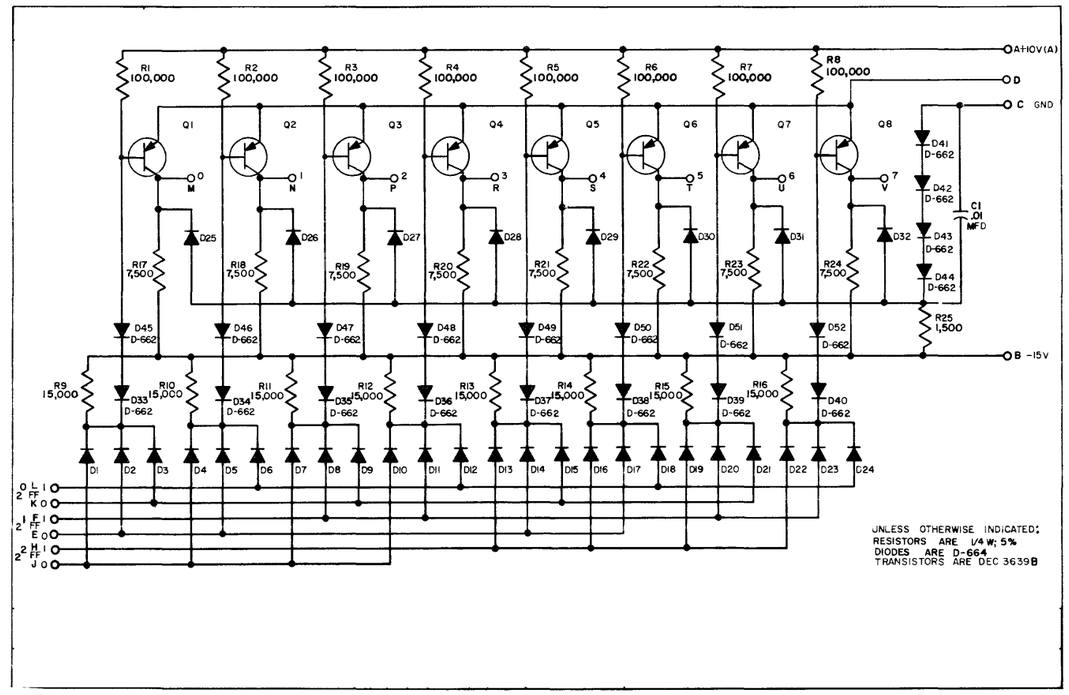
G906-0-1 LINC8 Capacitor and Power Up



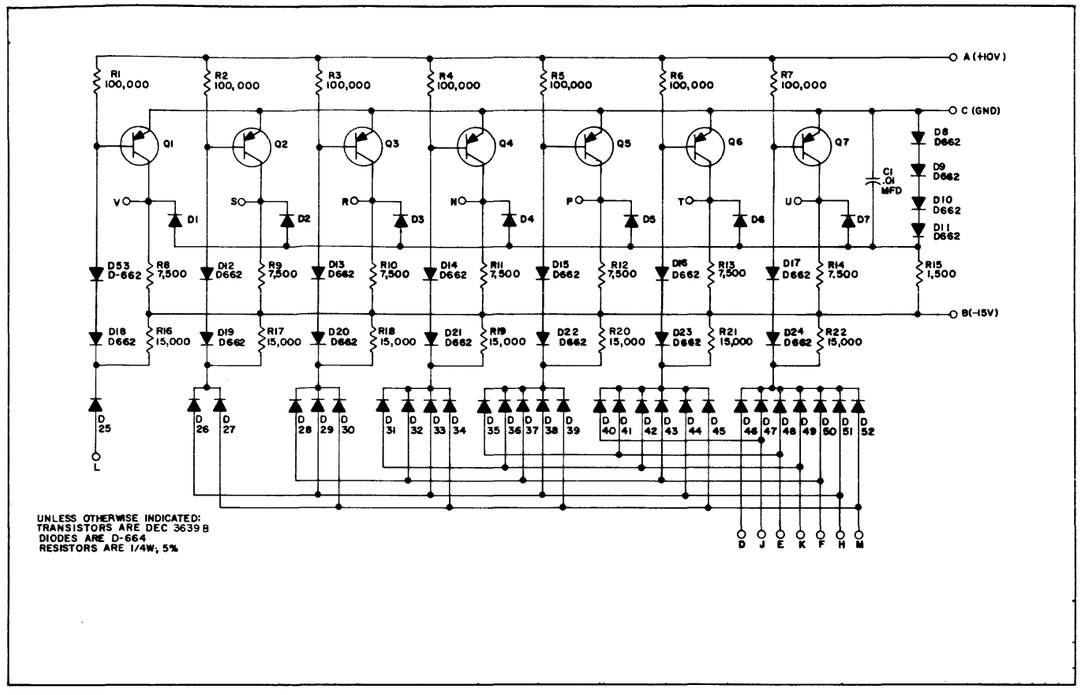
R141-0-1 Diode Gate



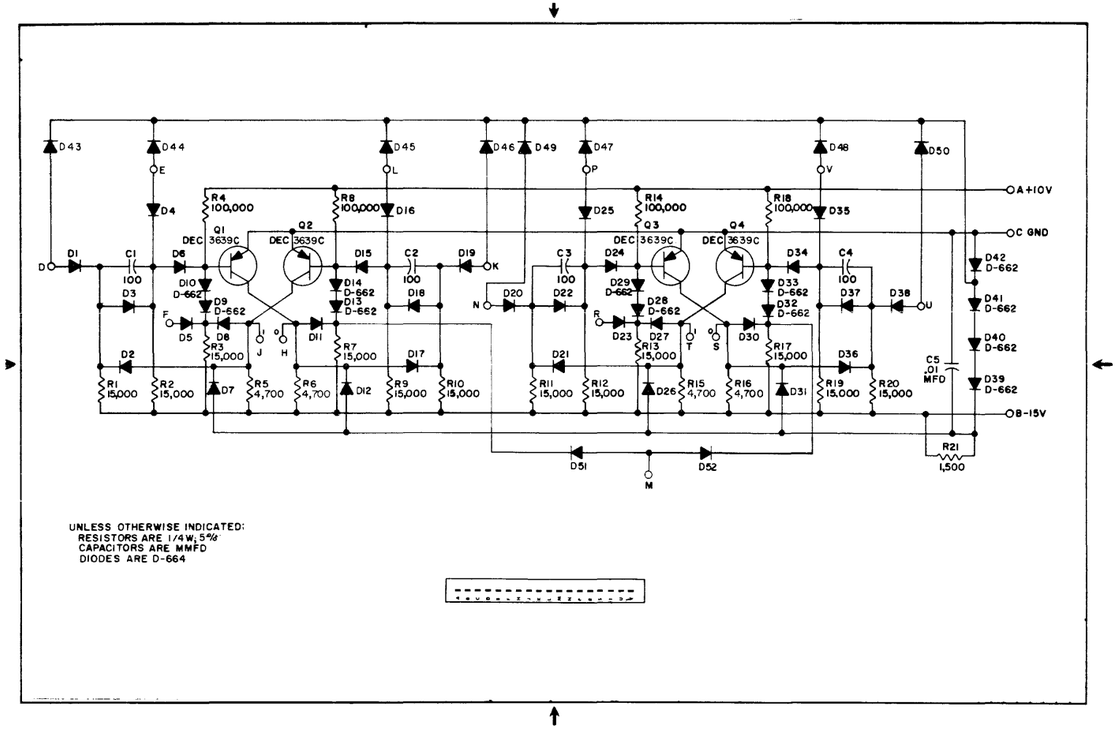
R122-0-1 NOR Gate



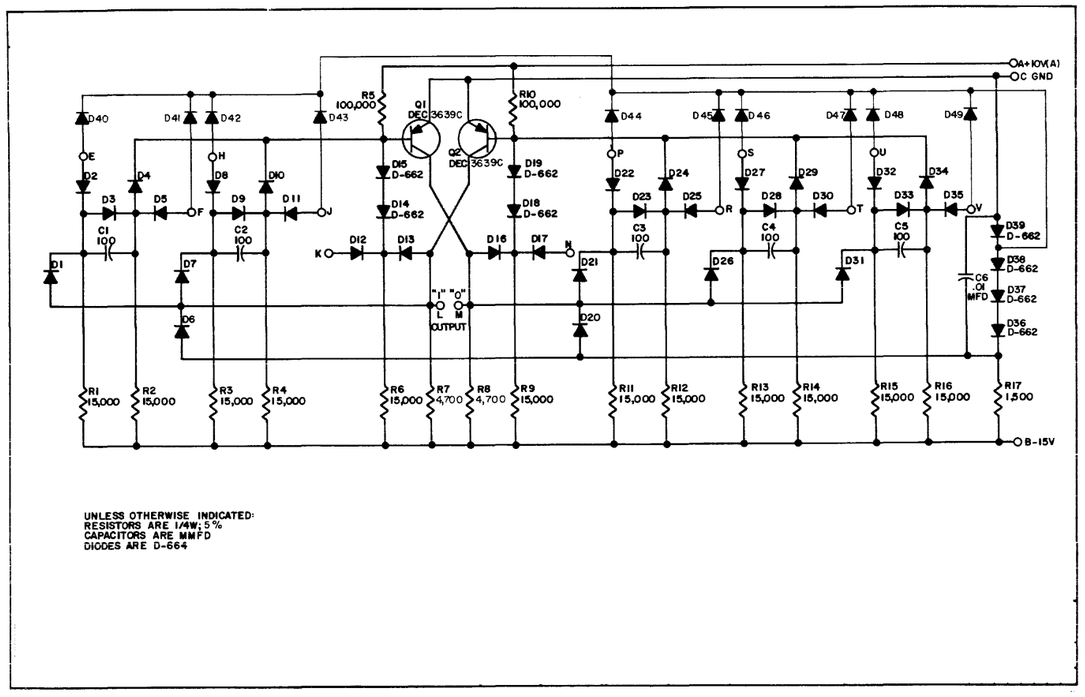
R151 Binary to Octal Decoder



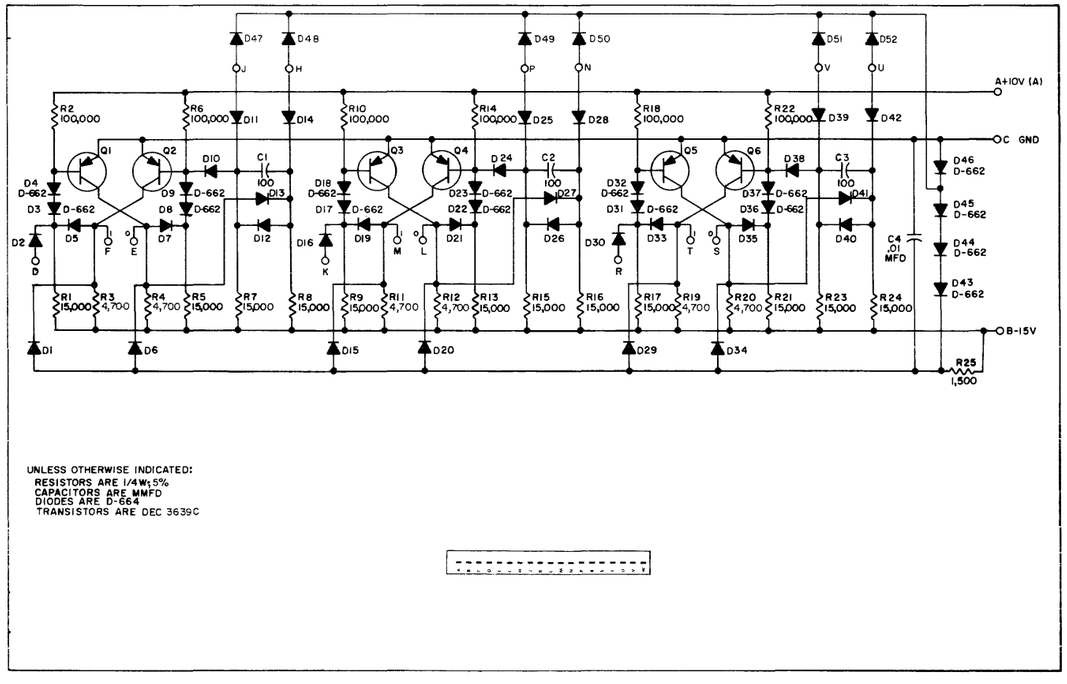
R181-0-1 DC Carry Chain



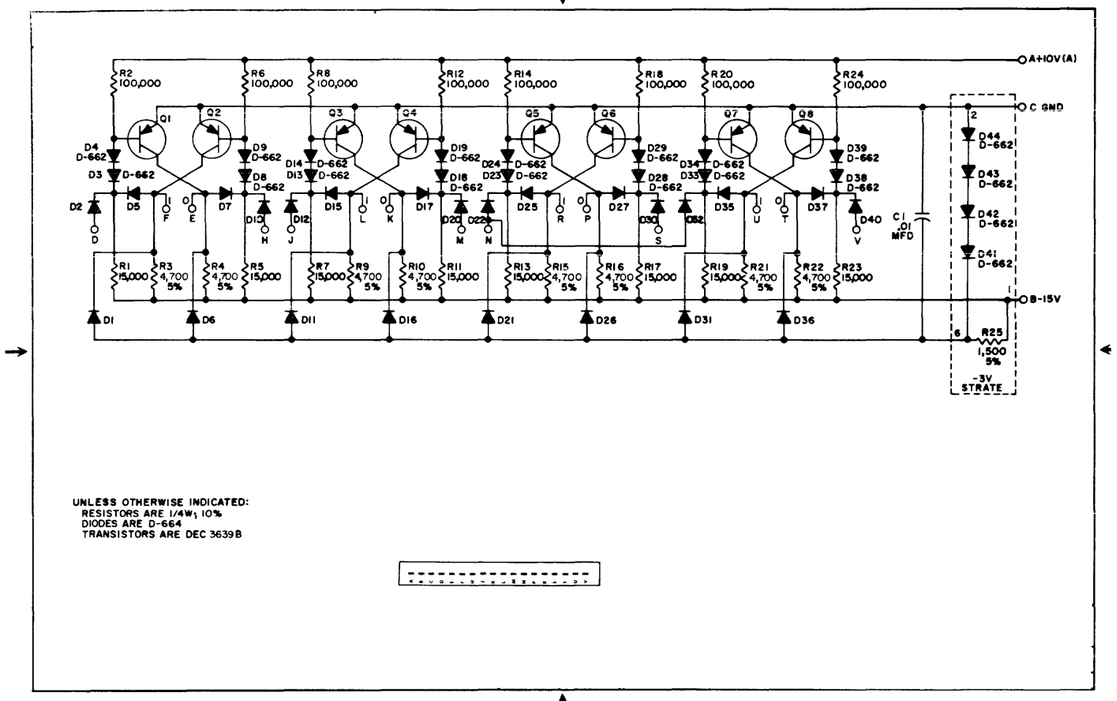
R202-0-1 Dual Flip-Flop



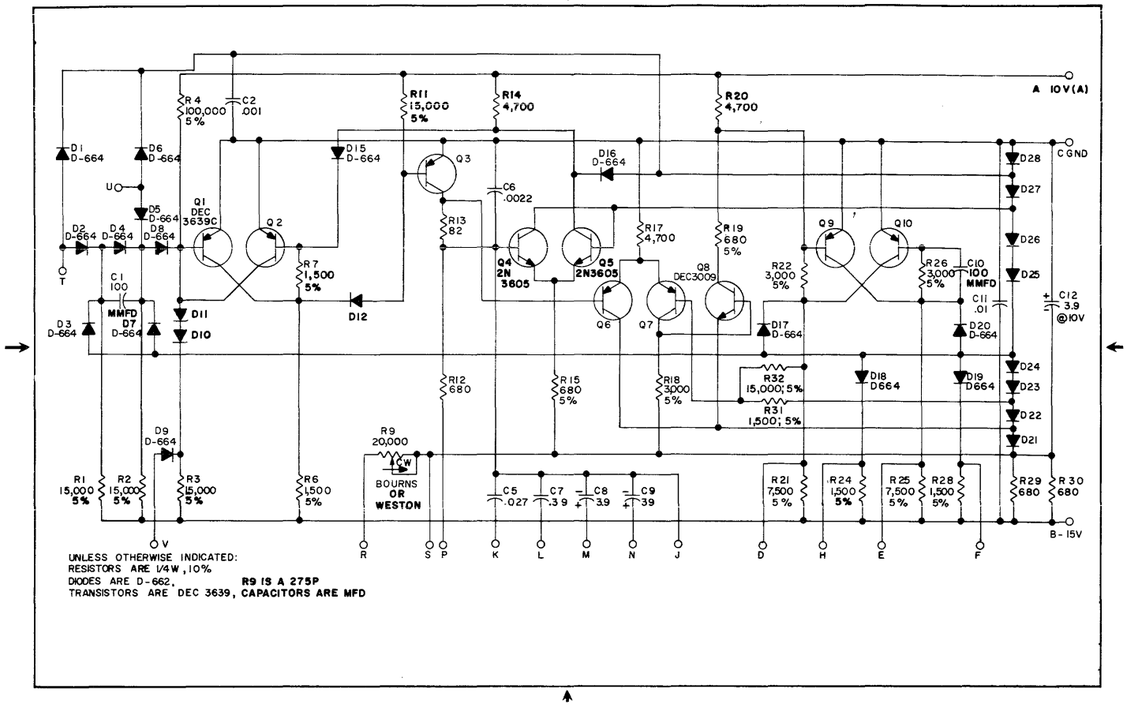
R201 Flip-Flop



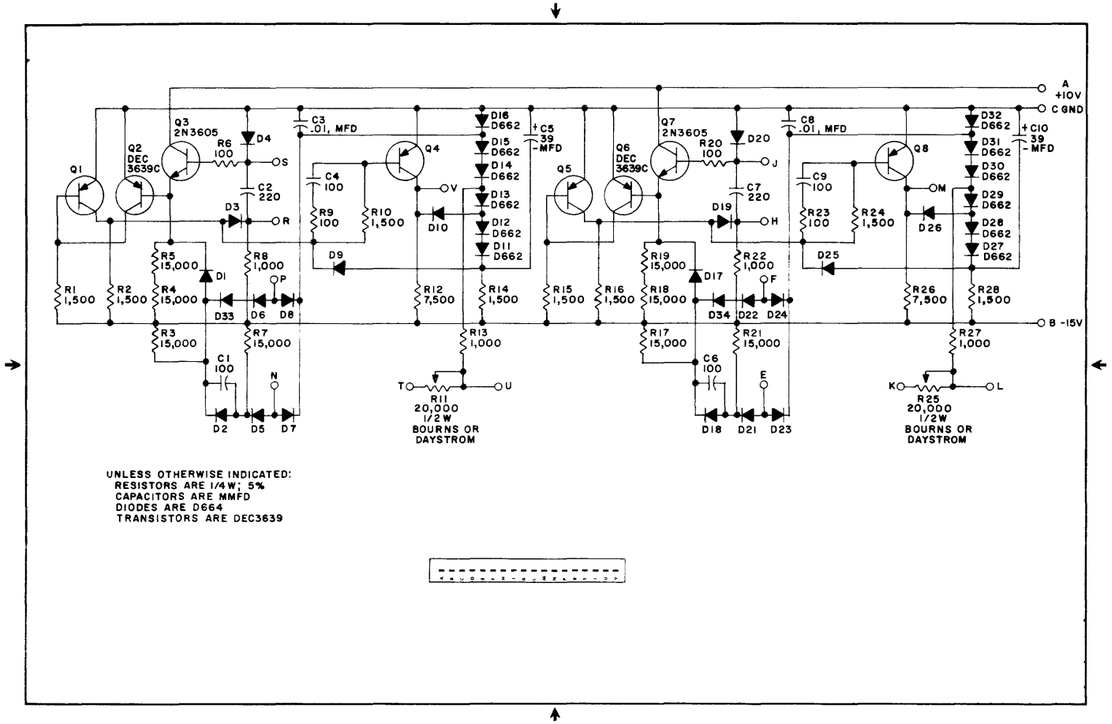
R203-0-1 Triple Flip-Flop



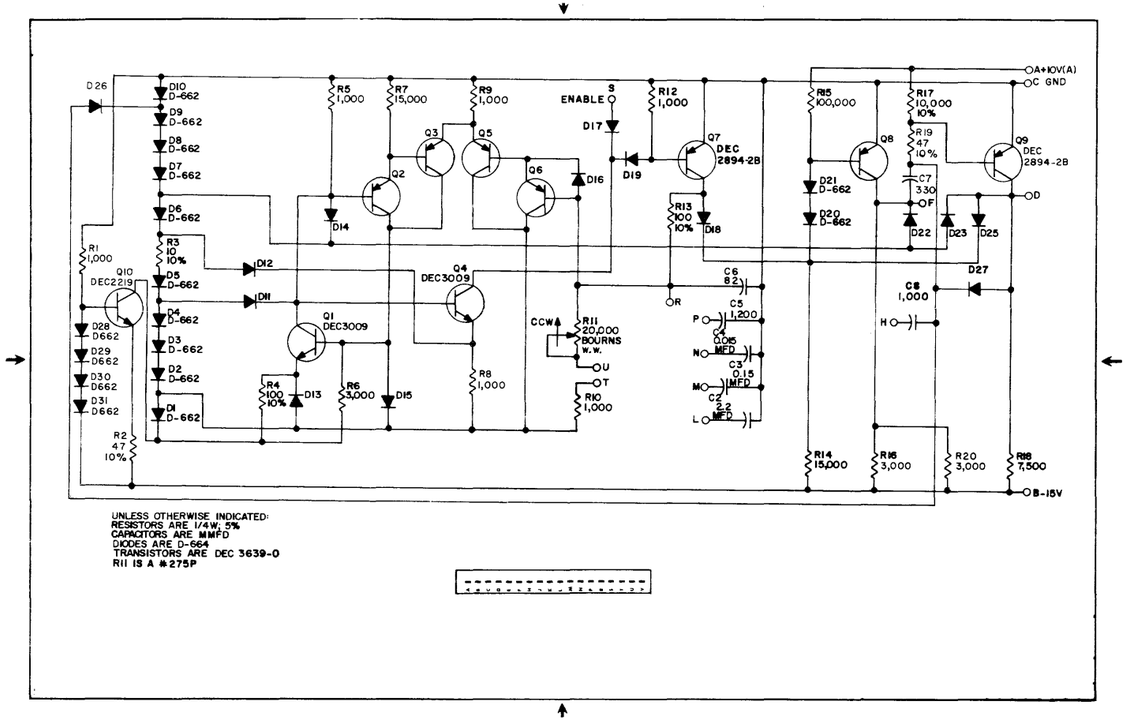
R204-0-1 Quadruple Flip-Flop



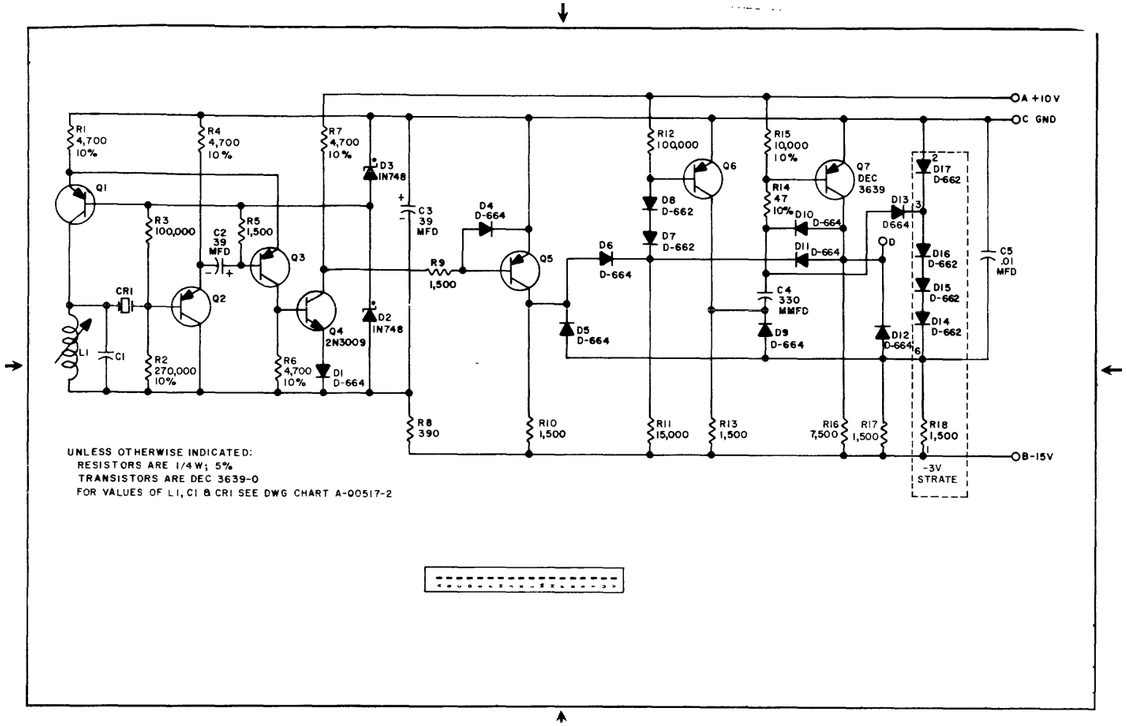
R303-0-1 Integrating One-Shot



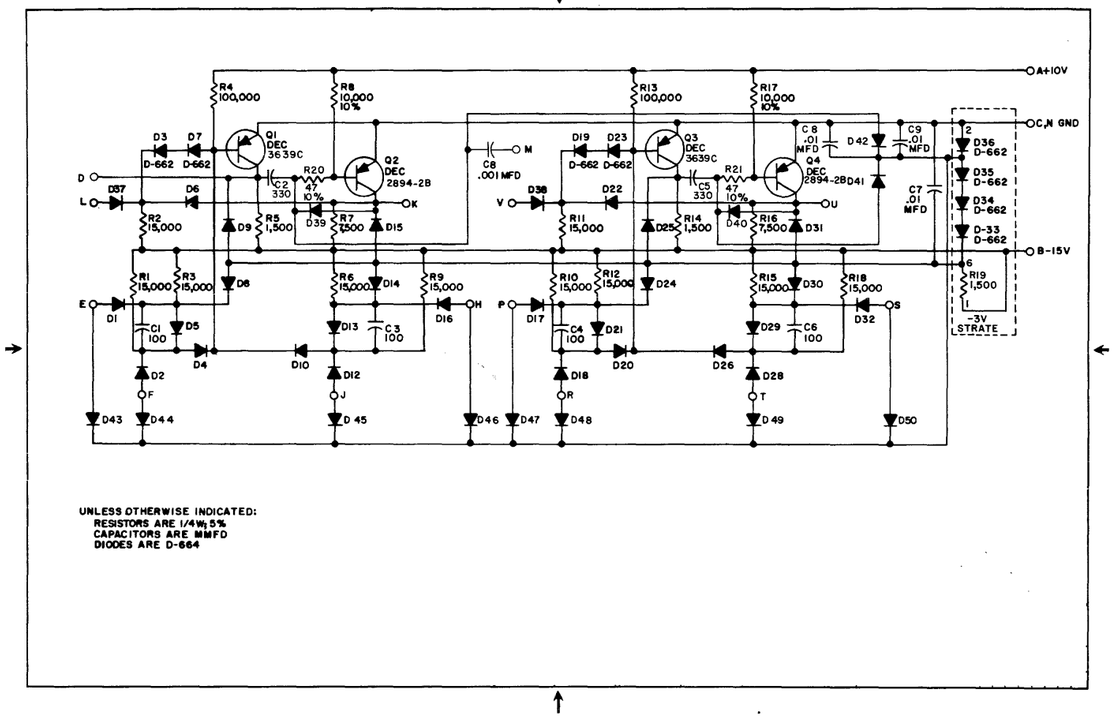
R302-0-1 Delay



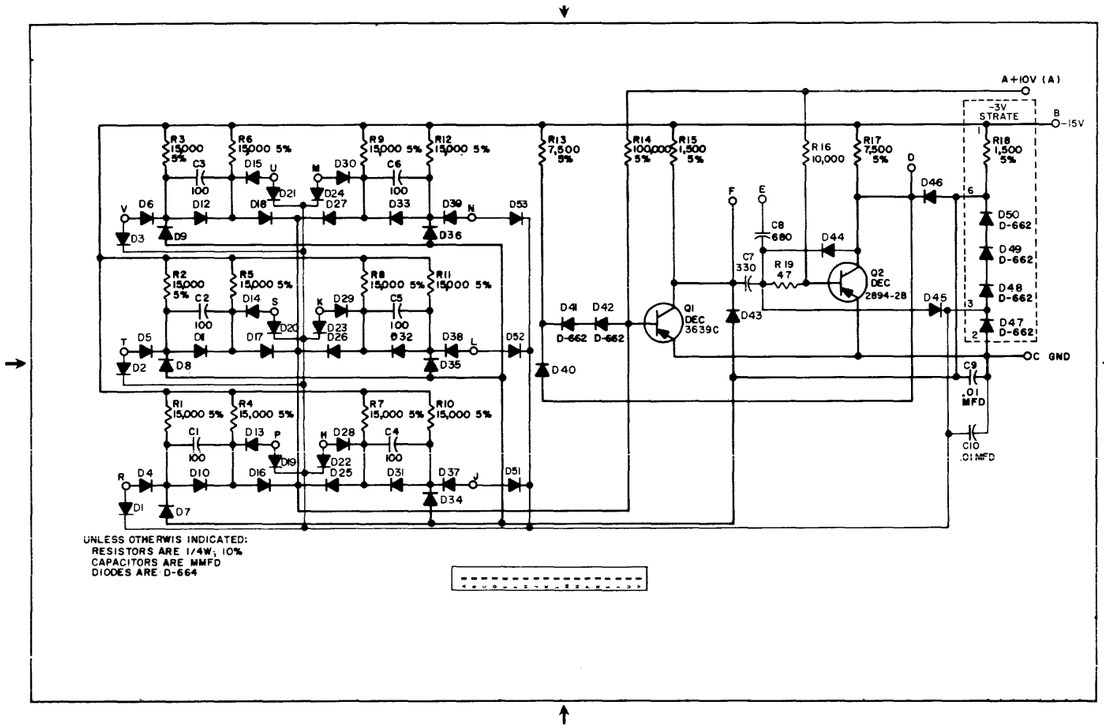
R401-0-1 Clock



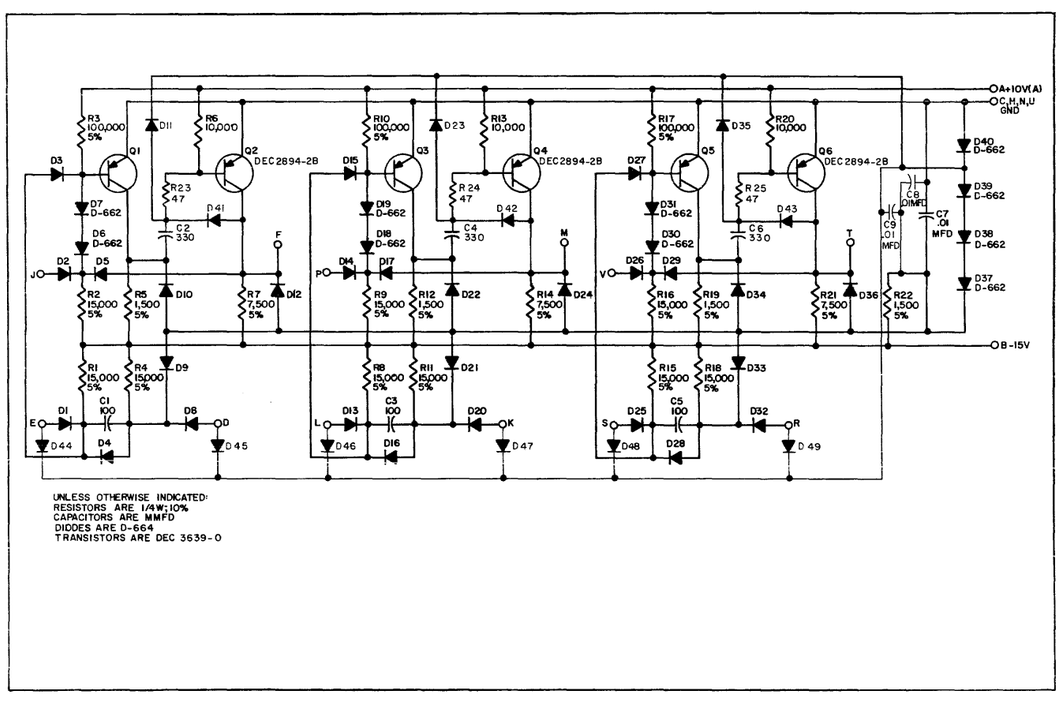
R405-0-1 Crystal Clock



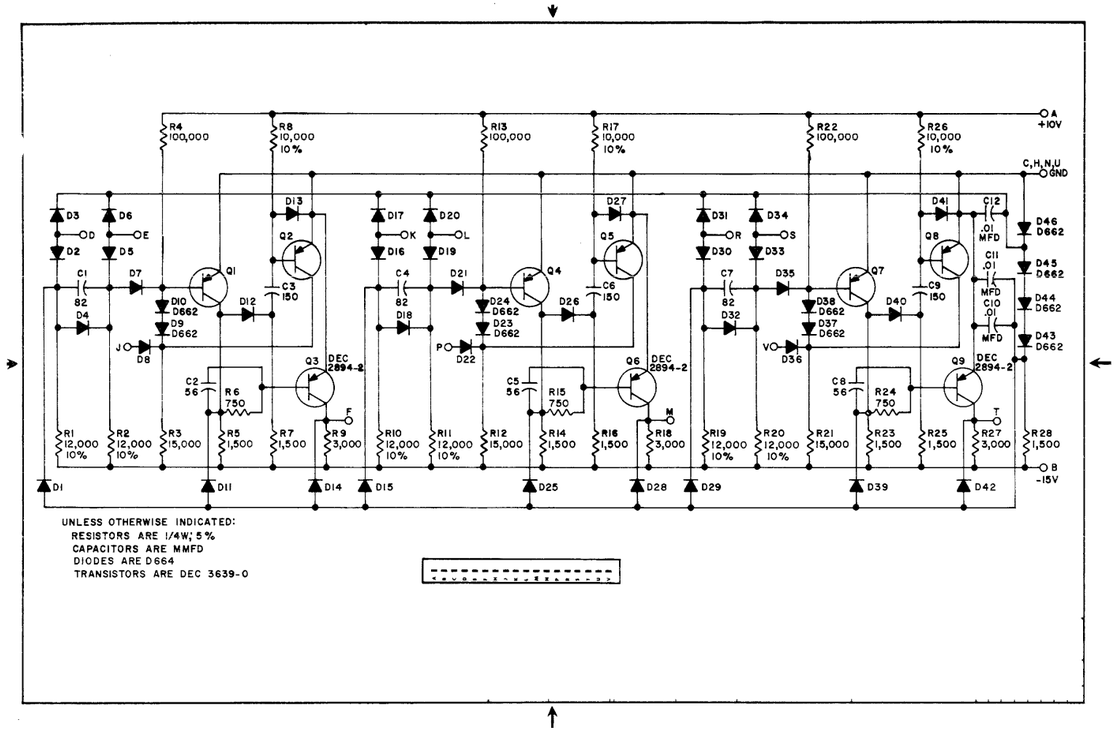
R602-0-1 Pulse Amplifier



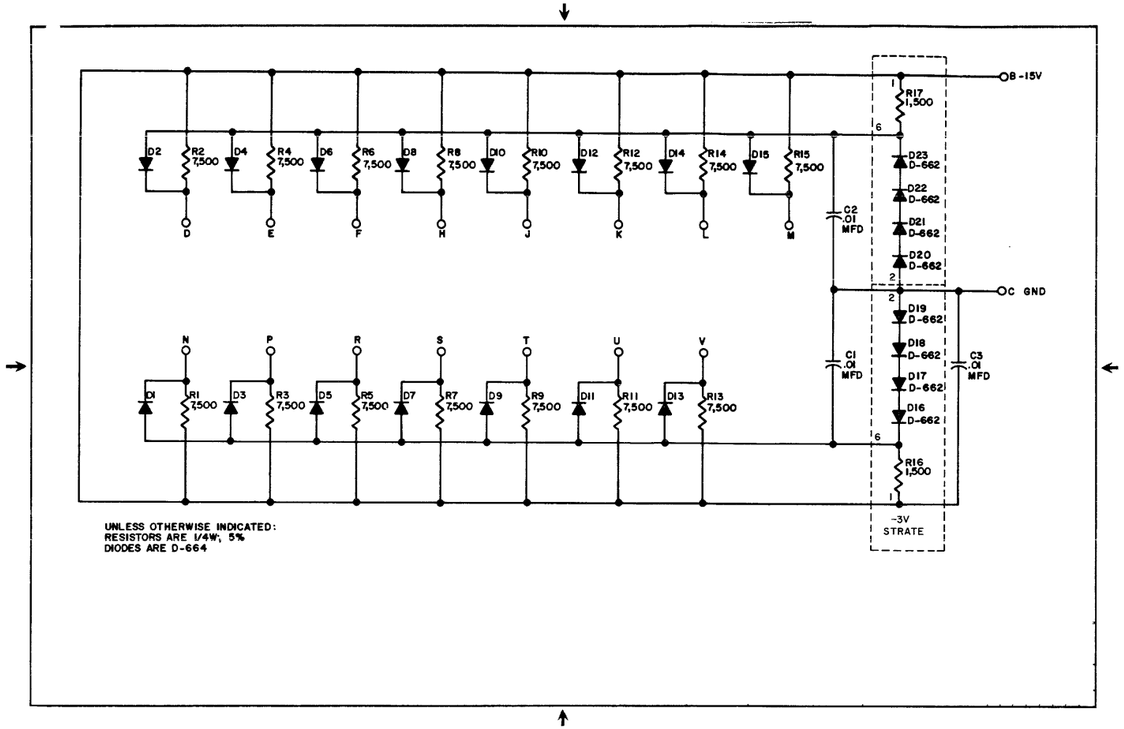
R601-0-1 Pulse Amplifier



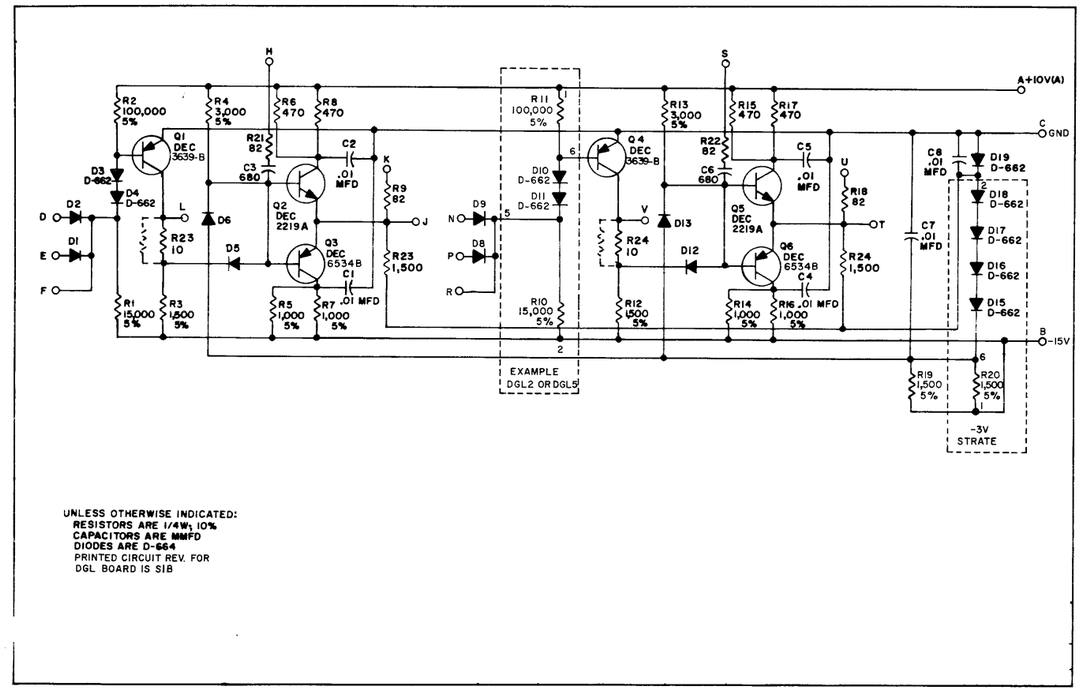
R603 Pulse Amplifier



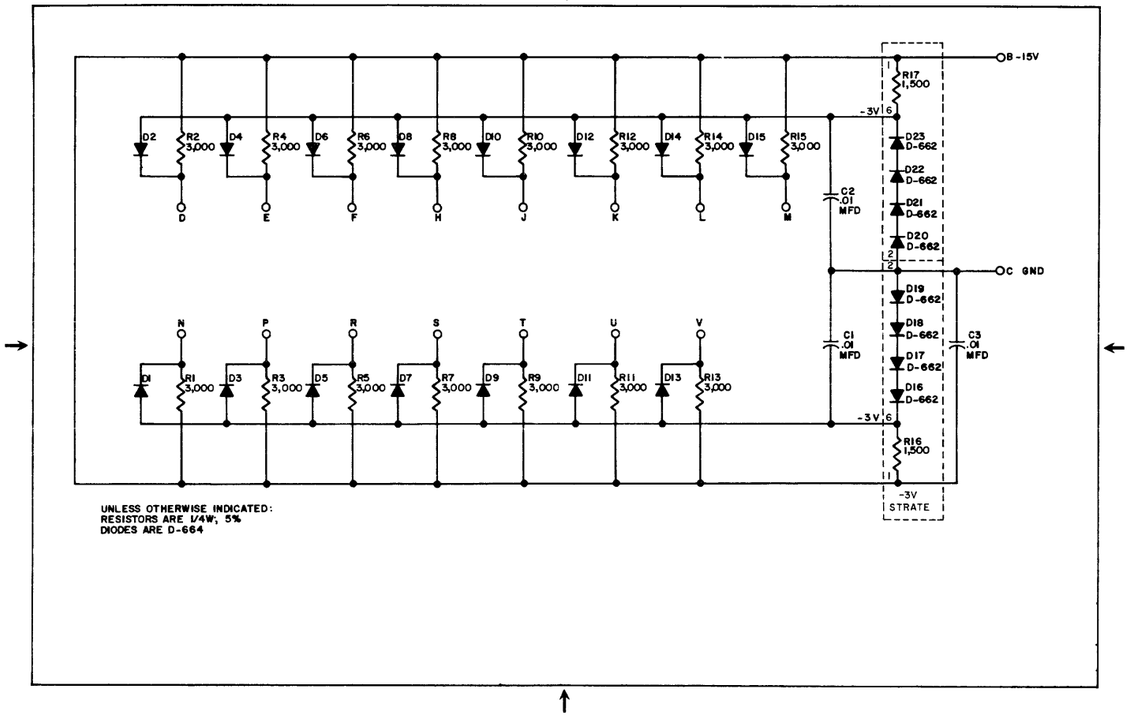
R613-0-1 Pulse Amplifier



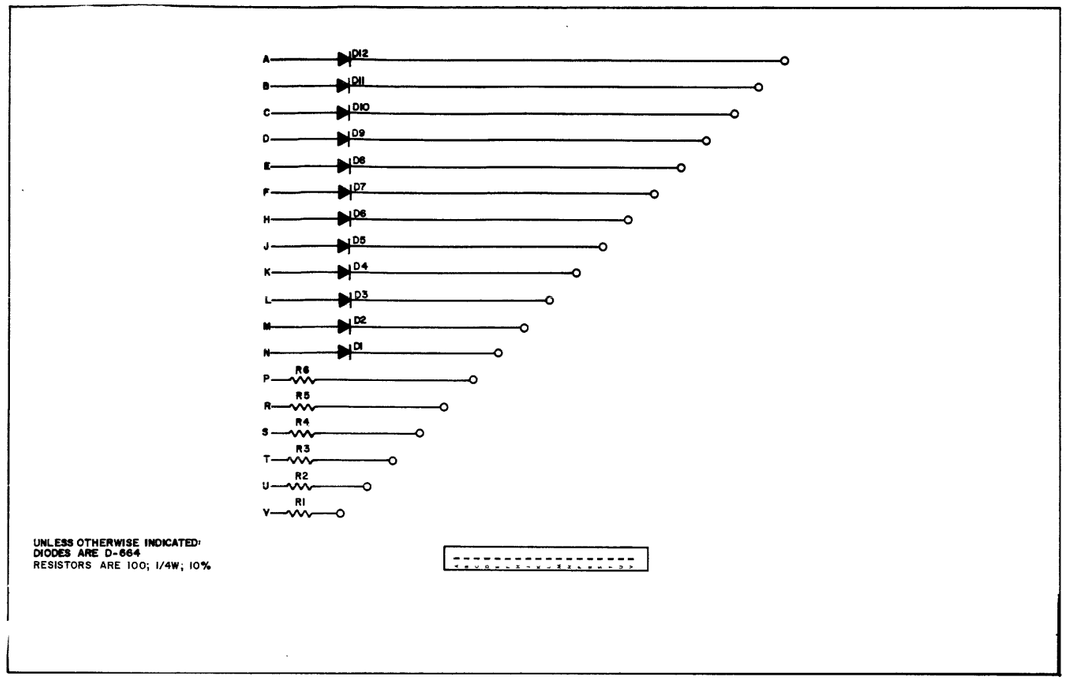
W002-0-1 Clamp Loads



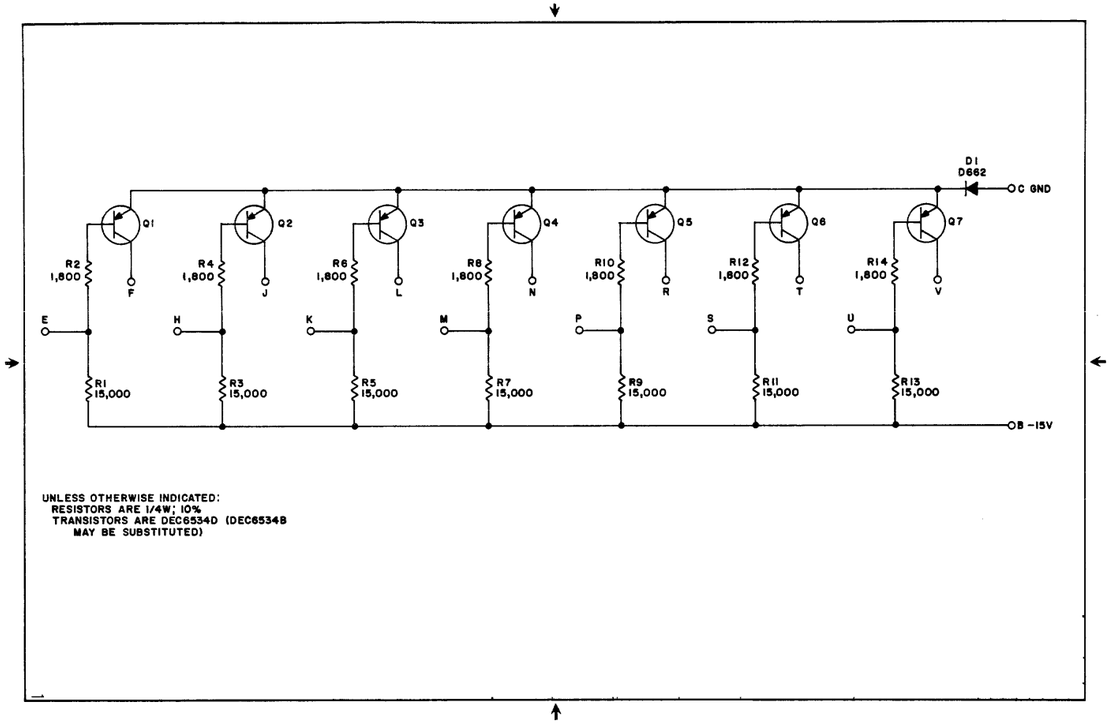
R650-0-1 Bus Driver



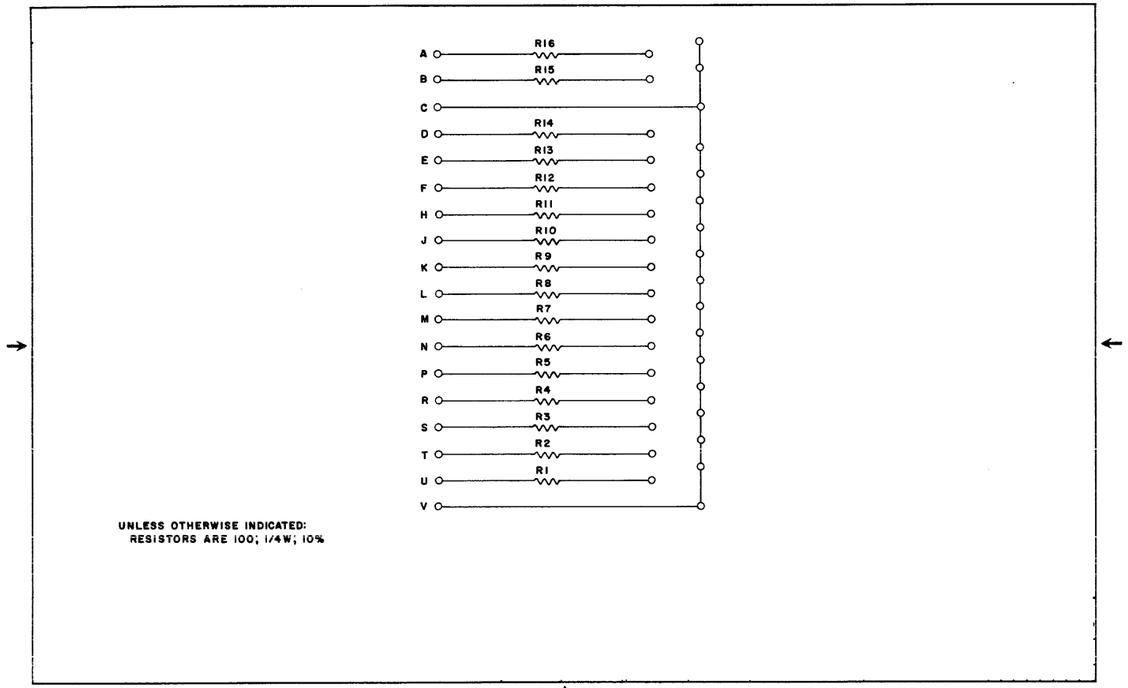
W005-0-1 Clamped Loads



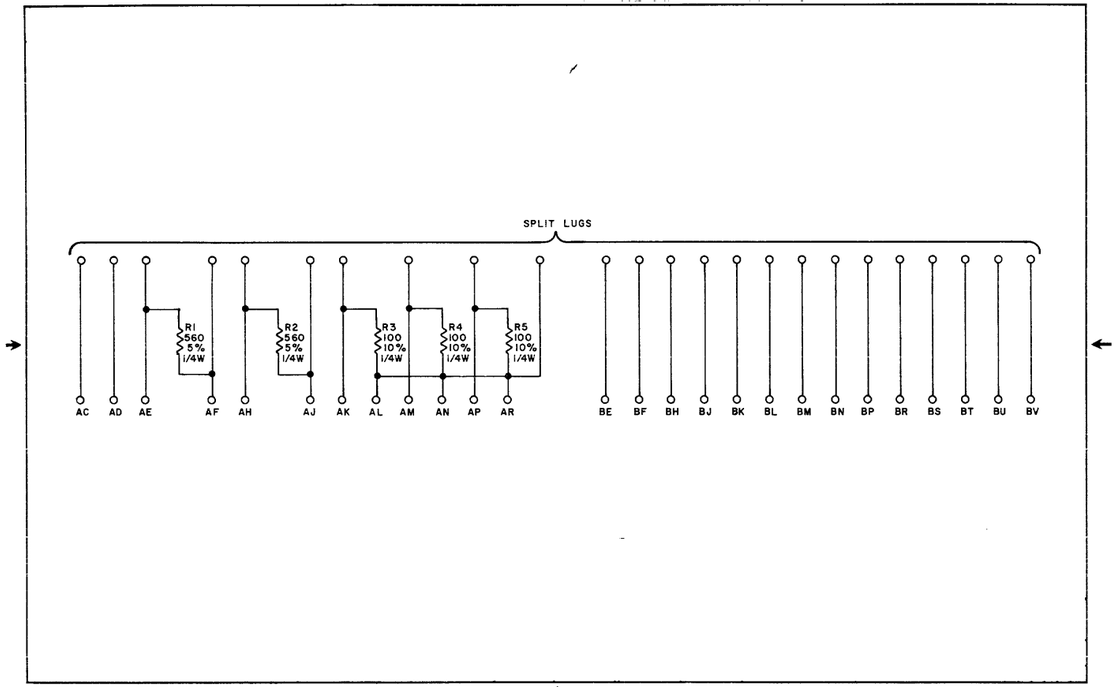
W026 Connector Board



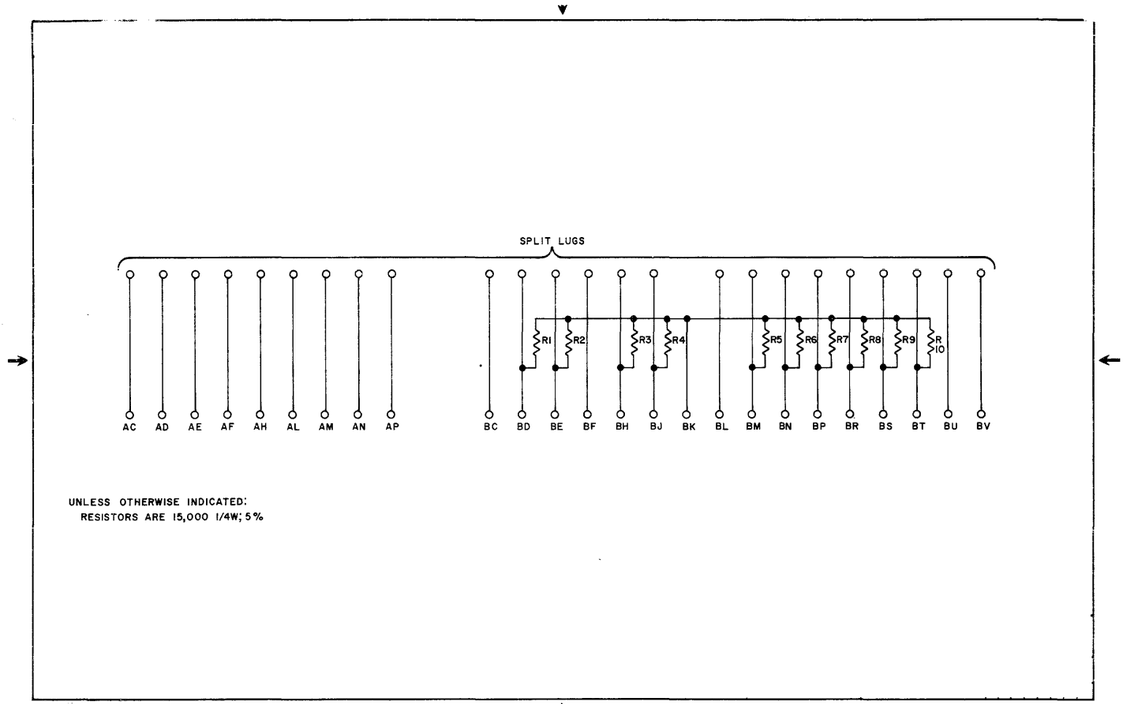
W050-0-1 Indicator Driver



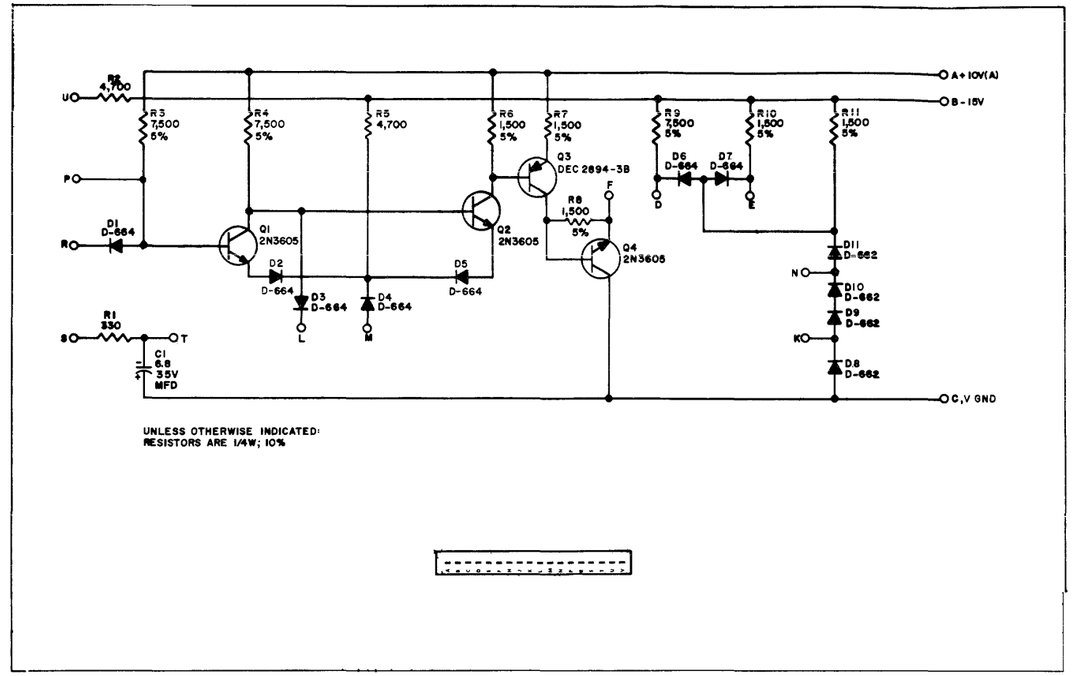
W035-0-1 Cable Connector



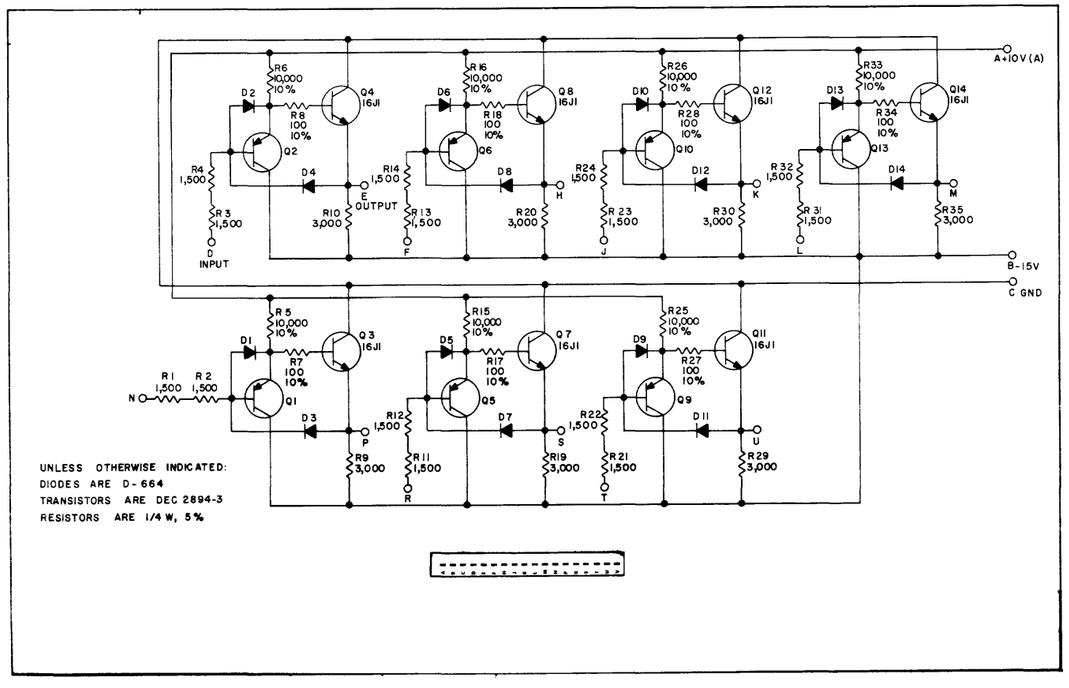
W072-0-1 LINC-8 Scope Cable Connector



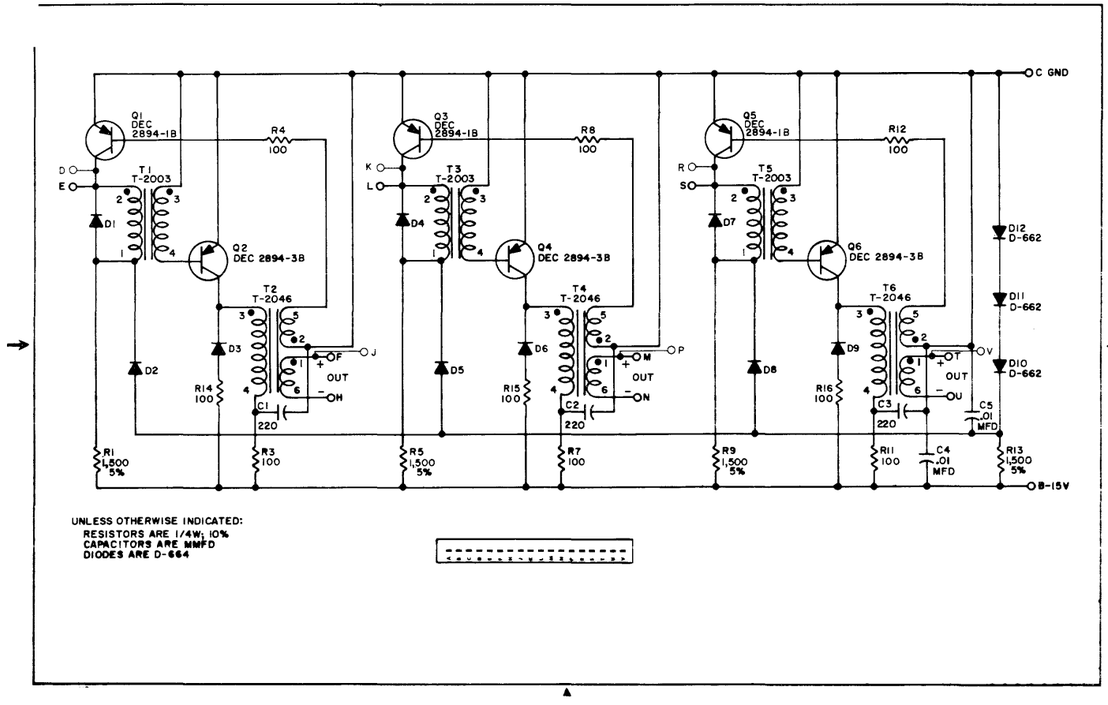
W073-0-1 LINC-8 Tape Cable Connector



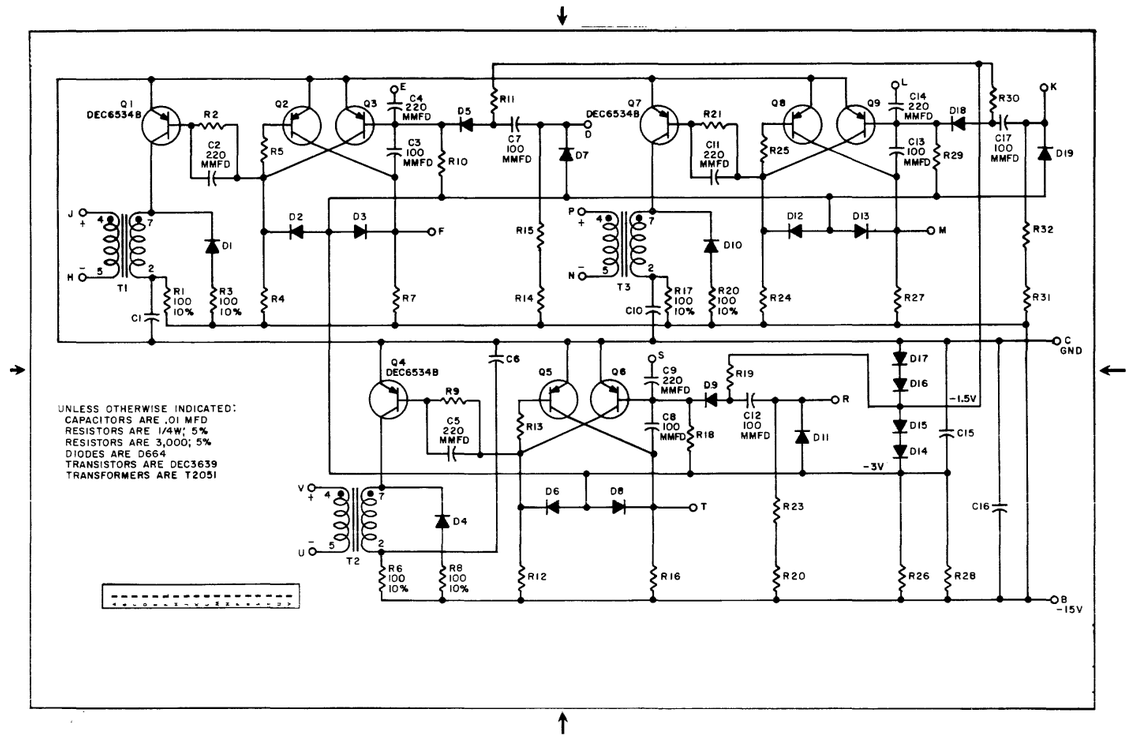
W501 Schmitt Trigger



W500 High Impedance Follower



W607-0-1 Pulse Amplifier



W640-0-1 Pulse Amplifier

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