

## MEMORY BOARD DESCRIPTION

### Learning Objectives

When you have successfully completed this portion of this lesson, you will be able to:

- Describe the major memory functions.
- Identify all major components and special components.
- Identify the available diagnostic tools.

### General Description

The memory boards interface to the Synchronous Intermodule Bus (SIMB). Each memory board is made up of a controller and an array on one board. Each array contains 512k bytes using 64k RAMs. The memory system supports both a 16-bit and a 32-bit data bus. Each board in the memory system inspects 28 address bits and responds to an address range based on its identification code. The identification code is the same as the channel number. Up to two boards can be installed in the system. If two boards are installed, the memory is interleaved, resulting in improved performance. The memory system can buffer a maximum of two memory requests, which results in improved performance. These two requests are Access A and Access B. There are seven functional blocks in a memory board. See figure 7-2 for a functional block diagram of the memory board.

### Memory Array Section

Each memory array on a board is made up of two blocks - 0 and 1. Each block is made up of a data array (MRAY) and a check bit array (CKRAY). Each block is driven by one set of RAS and CAS lines. Each MRAY has 32 RAM chips. Each CKRAY has seven RAM chips. Therefore, each board has a memory array consisting of a total of 78 RAMs. In each case, one chip represents one data bit or check bit. Write and Read operations require an average of four cycles per word for execution.

See figure 7-3 for the physical arrangement of the RAMs and their block and bit assignments.

### Address Section

The Address section, MEMADD, holds address information from the backplane until memory can use it. At that time, it issues the address information to the array and the Control section. It also keeps track of memory refresh.

The Address section of the Memory board is made up of five elements. They are the Address registers, the FROM registers, a FROM code parity generator, the Refresh counter, and the RAS/CAS multiplexer.

How the Series 37 SPU Works

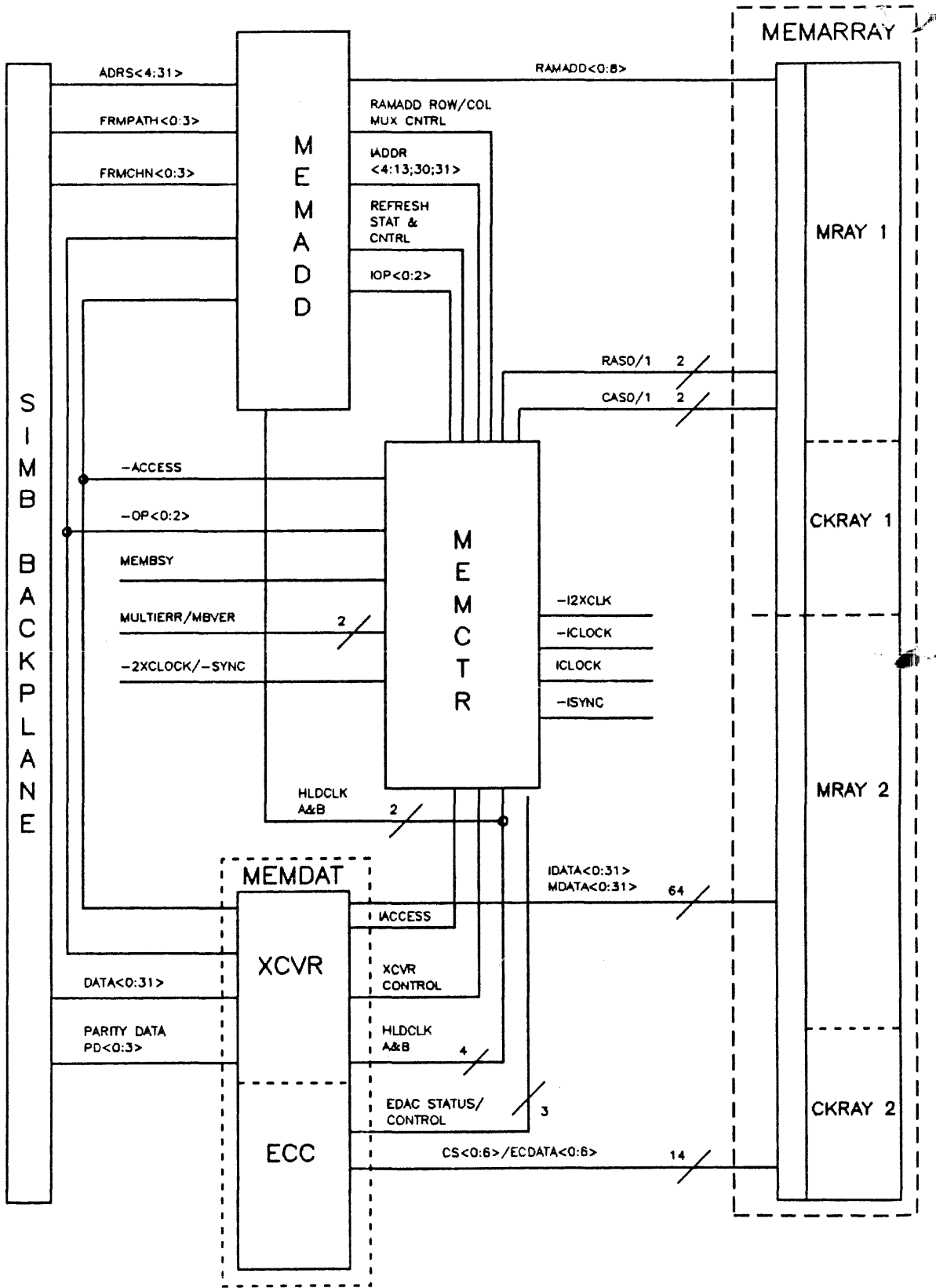


Figure 7-2. Memory Block Diagram

U1002 0/0	U902 1/0	U802 0/8	U702 1/8	U602 0/16	U502 1/16	U402 0/24	U302 1/24	U202 0/C0	U102 1/C0
U1003 0/1	U903 1/1	U803 0/9	U703 1/9	U603 0/17	U503 1/17	U403 0/25	U303 1/25	U203 0/C1	U103 1/C1
U1004 0/2	U904 1/2	U804 0/10	U704 1/10	U604 0/18	U504 1/18	U404 0/26	U304 1/26	U204 0/C2	U104 1/C2
U1005 0/3	U905 1/3	U805 0/11	U705 1/11	U605 0/19	U505 1/19	U405 0/27	U305 1/27	U205 0/C3	U105 1/C3
U1006 0/4	U906 1/4	U806 0/12	U706 1/12	U606 0/20	U506 1/20	U406 0/28	U306 1/28	U206 0/C4	U106 1/C4
U1007 0/5	U907 1/5	U807 0/13	U707 1/13	U607 0/21	U507 1/21	U407 0/29	U307 1/29	U207 0/C5	U107 1/C5
U1008 0/6	U908 1/6	U808 0/14	U708 1/14	U608 0/22	U508 1/22	U408 0/30	U308 1/30	U208 0/C6	U108 1/C6
U1009 0/7	U909 1/7	U809 0/15	U709 1/15	U609 0/23	U509 1/23	U409 0/31	U309 1/31	X	X

Figure 7-3. Memory RAM Location Diagram

## Data Section

The Data section is organized so that either 16-bit or 32-bit bus transactions can take place. Data is accepted and output from the SIMB by six registers for Access A and six registers for Access B.

The Data section, MEMDAT, is made up of three elements - the Read/Write Data transceivers, the Error Correction circuit, and the Data Parity Generator.

The Error Correction circuitry is located on one chip. The Error Detection and Correction (EDAC) chip corrects single-bit errors and detects multiple-bit errors. Under certain error conditions, some error patterns with more than two incorrect bits will not be detected.

The Data Parity Generator generates four parity bits. One bit is associated with each byte of a 32-bit word in memory. Note that data is organized on a 32-bit basis in memory and on a 16-bit basis in the rest of the system.

## Control Section

The Control section determines if an A-Access or a B-Access is being done. It also phases in the Refresh function, provides the timing for the RAMs, and generates all of the control signals for the latches and buffers on the board. The signals are also used for initiating error correction.

The Control section also determines if the address referenced by a pending request resides on the board under its control, the other board, or none of the boards (a memory bounds violation). When two memory boards are installed, the memory system is automatically interleaved. The memory assignments for each board are such that when sequential accesses of memory are made, the accesses switch between boards after each pair of words. Therefore, when interleaved, board selection is controlled by bit 30 of the address. Note that bit 31 is the least significant bit.

The control signals for the latches, buffers, and error correction are implemented in Programmable Logic Arrays (PLA). There are four PLAs in the system.

## Memory Operations

The memory operations are controlled by the opcodes. The functions associated with each memory op code are shown below:

OP CODE	ADDRESS BIT 31	FUNCTION
0	do not care	Read (16-bit)
1	do not care	Write (16-bit)
2	0	*Read error latch
2	1	*Write (16-bit) with old check bits and return new check bits
3	0	Write (32-bit) to initialize check bits
3	1	*Write (16-bit) with old check bits

\* Functions performed for diagnosis

### Read (Opcode = 0)

If a Read operation is specified, data is input into the 32-bit MDATA latch. The data is then put on the IDATA bus. If no errors are detected, then IDATA is latched onto the data bus (DATA) of the SIMB. Only bits 0 through 15 are read by the SIMB. How the data is latched is controlled by the value of address bit 31.

If address bit 31 is set to 0, the upper 16 bits (0 - 15) of memory are mapped into the upper 16 bits (0 - 15) of the SIMB.

If address bit 31 is set to 1, the lower 16 bits (16 - 31) of memory are mapped into the upper 16 bits of the SIMB.

### Write (Opcode = 1)

If a Write operation is specified, data is transferred in the opposite direction from that of the Read operation - from the SIMB to the MDATA latch.

## Refresh

Refresh is accomplished with a divide-by-100 counter. A Refresh operation takes place every 99 cycles. Each refresh operation increments a refresh counter, which rolls over every 256 counts. A 64k RAM is refreshed every two milliseconds for seven address lines.

## Initialization

Before memory can be accessed in a normal manner, a 32-bit Write (opcode 3) operation must be performed to every memory location. This sets the correct syndrome bits for each memory location.

## Memory Logging

Memory logging is a facility that allows MPE to create a file of the most recent memory errors. A single-entry error latch in memory is read by MPE every 10 minutes. Unlike the other HP 3000 systems, the Series 37 cannot save data about more than one error. It can only save the most recent error in the error latch. This facility uses the following programs:

Memory Error Logging Process (MEMLOG)  
 Memory Log Analysis Program (MEMLOGAN)  
 Memory Error Logging Interval Update Program (MEMTIMER)

Refer to the MPE System Utilities Reference Manual for user interface information. The format of each entry in the file created by MPE is shown below.

```

-----
|      ADDRESS      | ERROR TYPE      | ERROR |
-----
| BOARD | ROW | TYPE BIT CHIP | COUNT |
-----

```

**BOARD**            The board ID number is displayed as 0 or 1. Board 0 resides in slot 2 and board 1 resides in slot 3.

**ROW**              This identifies the row in which the faulty RAM is located. It is not displayed if there is a multiple bit error.

**TYPE**             Type of error detected. They are:

Check - Check bit error

Data - Data bit error

Multiple bit - Error in more than one bit error

If a multiple bit error is indicated, no bit or chip information is given.

## How the Series 37 SPU Works

<b>BIT</b>	If TYPE = Check, BIT indicates the failing check bit (0 through 6).  If TYPE = Data, BIT indicates the failing data bit (0 through 31).
<b>CHIP</b>	Indicates the chip on which the error occurred, in the format Un. The variable n indicates the chip number.
<b>COUNT</b>	The number of logging intervals during which this error was detected at least once. It does not accurately indicate the number of times an error was actually detected.

## Memory Diagnostic Tools

The following diagnostic tools are available with this product for diagnosing memory problems.

1. PON selftest
2. Maintenance Mode Selftest - Memory test
3. DUS memory diagnostic (MDIAG37)
4. Memory logging facility