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# Lead Reduction Among Combinatorial Logic Circuits

*The paper provides a description of the behavior of lead reduction among combinatorial logic circuits. Methods by which one may design the lead reduction architecture for modular packaging schemes are developed. The methods are then applied to the design of the lead reduction architecture of an integrated circuit chip and a nine-chip cell.*

## Introduction

The number of circuits required to build a large digital system such as the IBM System/370 Model 168 is much larger than the number of circuits of suitable performance that may be implemented directly on a silicon chip. Therefore, the construction of 370/168-type systems with large-scale-integrated (LSI) chips still requires the design of circuit interconnection schemes composed of modular parts. The silicon masterslice (gate array) is one example of a modular part designed to carry a set of partitions (a group of interconnected logic circuits abstracted from a system) that, when interconnected, constitute the system. Other examples of modular parts are multi-chip modules, printed circuit cards, frames, etc. Several questions arise during the design of modular parts. For example, what distribution of possible partitions, combinations of input/output (I/O), I/O signal requirements, and circuit aggregates are available within a system design? What is a suitable maximum number of circuits for a part whose information signal requirements will be limited by the number of I/O supplied on the part? What are the efficiencies of use of the circuit mounting space and of the I/O terminals on the container? What are the signal I/O requirements for collections of partitions such as multi-chip assemblies? This paper provides methods by which lead reduction architecture may be designed for modular packaging schemes to achieve a required circuit packing efficiency.

## The distribution of partitions in a system

In 1960, E. F. Rent [1] sampled partitions of the logic circuitry of the IBM 1401 and 1410 computers to determine a rule for printed circuit card designers which would state a sufficient number of card pins to service the maximum number of circuits that may be mounted on a card. Sample values of the circuit count $n_c$ and the number of logic signals required to service a partition of $n_c$ circuits, *NIO*, were plotted on a log-log scale. A straight line estimate of the upper bound on *NIO* for partitions of the 1401/1410 systems yielded the rule

$$NIO \leq 4.30 n_c^{0.672}, \tag{1}$$

which was obtained from Rent's table of upper bounds with $100 \leq n_c \leq 500$ circuits per partition. Rules similar to (1) have been derived using data from packaged machines and partitioning experiments [2–4].

Formula (1) represents a risk function and Ref. [1] does not state the probability that a partition may require more *NIO* than the number specified by the formula. In 1965, a 360/30 CPU was examined to determine the distribution of partitions in the 360/30 for partitions of solid logic technology (SLT) modules abstracted from the system [5]. The examination proceeded in the following manner. First a contour was drawn around a constant number of SLT modules, $n_m$, in the system. Modules rather than circuits were counted in order to simplify the selection of contours in the module wiring diagram of the 360/30. Next, trial contours which were uniformly distributed throughout the system were selected. The number of single-wire connections required to connect the partition of $n_m$ modules to the rest of the system was then defined as $N_m$. Figure 1 displays the accumulative probability distributions, $P(N_m \leq N)$, for $n_m = 6$, 12, 24, and 48 SLT modules per partition. Figure 2 displays the data of Fig. 1 plotted as $\log n_m$ *vs.* $\log N_m$ for constant risk factors,

$$P(N_m \leq N; n_m = \text{constant}) = 0.9773, 0.8413. \tag{2}$$

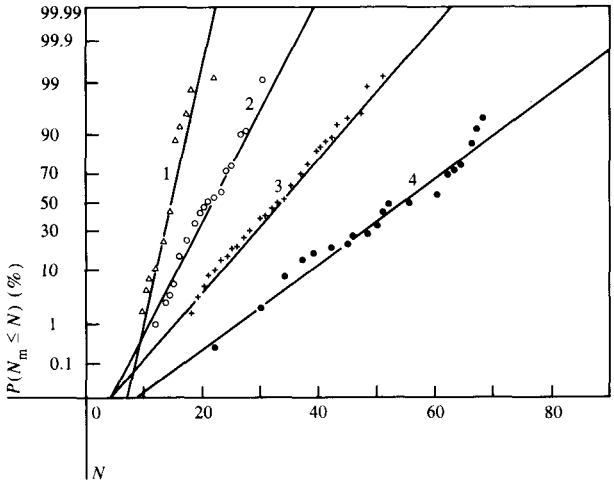


**Figure 1** Observed data, the calculated probability function $P(N_m \leq N)$, as a function of $N$. The lines represent best fits to the calculated data. Curves 1–4 are for constant $n_m = 6, 12, 24$, and 48, respectively. $\langle N_6 \rangle = 14.45, \sigma_6 = 2.02$; $\langle N_{12} \rangle = 21.53, \sigma_{12} = 4.64$; $\langle N_{24} \rangle = 33.05, \sigma_{24} = 7.72$; $\langle N_{48} \rangle = 54.36, \sigma_{48} = 12.13$.

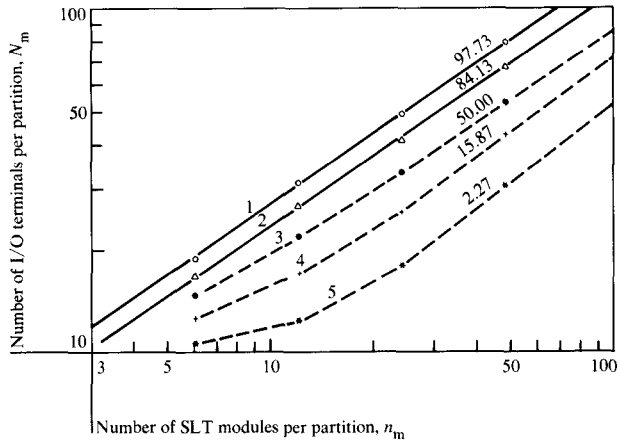


**Figure 2** Experimental constant-risk contours for 360/30 SLT circuitry. Curves 1–5 are for contour values of 97.3% (○, $\langle N \rangle + 2\sigma$); 84.1% (Δ, $\langle N \rangle + \sigma$); 50% (●, $\langle N \rangle$); 15.9% (+, $\langle N \rangle - \sigma$); and 2.3% (*, $\langle N \rangle - 2\sigma$); respectively. For Curves 1 and 2, $NIO = bn_m^{\Gamma}$ was calculated: Curve 1, $b = 5.55 \pm 0.18$ and $\Gamma = 0.682 \pm 0.011$; Curve 2, $b = 4.80 \pm 0.18$ and $\Gamma = 0.680 \pm 0.013$.

A root-mean-square (RMS) fit of the equation,

$$N_m = bn_m^{\Gamma}, \tag{3}$$

to Eq. (2) shows that such an equation fits the upper-bound risk contours (0.9773 and 0.8413) of Fig. 2 reasonably well. In particular, if the random variable

$$b = \frac{N_m}{n_m^{0.680}} \tag{4}$$

for each set of partitions at a constant-risk level is calculated, it is seen that for $12 \leq n_m \leq 48$ modules per partition, $b$ is a quasi-normally distributed variable with $\langle b \rangle$, the average value of $b$, equal to 3.90 and a standard deviation $\sigma_b$ of 0.87. The results of such a calculation are shown in Fig. 3. If this behavior is valid for $n_m >> 48$, the distribution of $b$ could be used to calculate answers to the questions mentioned previously.

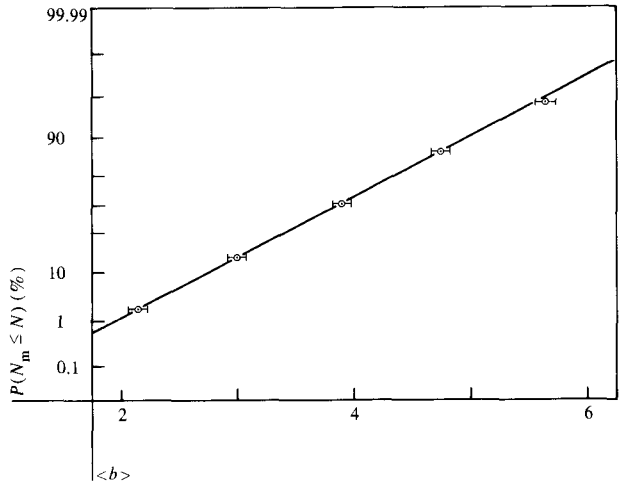


**Figure 3** Distribution of $b$ corresponding to $P(N_m \leq N)$ for $n_m = 12$, 24, and 48 modules; *i.e.*, the mean value of $b$, $\langle b \rangle = \sum(N/n_m^{\Gamma})/3$, where $\Gamma = 0.680$ and $P(N_m \leq N)$ is set to a constant value. The circled data points represent $\langle b \rangle$, while the bars indicate $\pm\sigma_{[b]}$.

Analytical attempts to describe the distribution of possible partitions produced probability distributions similar to the distribution of partitions observed for the 360/30. The random variables used in the analysis can be explained by describing the approximate average value of $NIO$ at constant $n_c$, $\langle NIO; n_c \rangle$, over all possible partitions of $n_c$ circuits:

$$\langle NIO; n_c \rangle \approx n_c \left[ \frac{\langle I_p \rangle}{2 - \langle PIO(n_c) \rangle} \right] \frac{\langle PIO(n_c) \rangle}{2(1 - \langle 1/j_p \rangle)}, \tag{5}$$

where $n_c$ is the number of logic circuits per partition, and $I$ is the number of wires attached to emitter-coupled logic circuits with fan-in less than or equal to four; $2 \leq I \leq 12$. $\langle I_p \rangle$ is the average number of wires attached to a circuit for the circuits in a partition, $j_p(n_c)$ is the number of logic service terminals (LSTs) per net between I/O terminals of partitions of $n_c$ circuits, and $\langle 1/j_p \rangle$ is the average value of the reciprocal of $j_p(n_c)$. $\langle PIO(n_c) \rangle$ is the average probability that a wire attached to a circuit within a partition of $n_c$ circuits must connect to a circuit outside the partition, and $I$, $j_p$, and

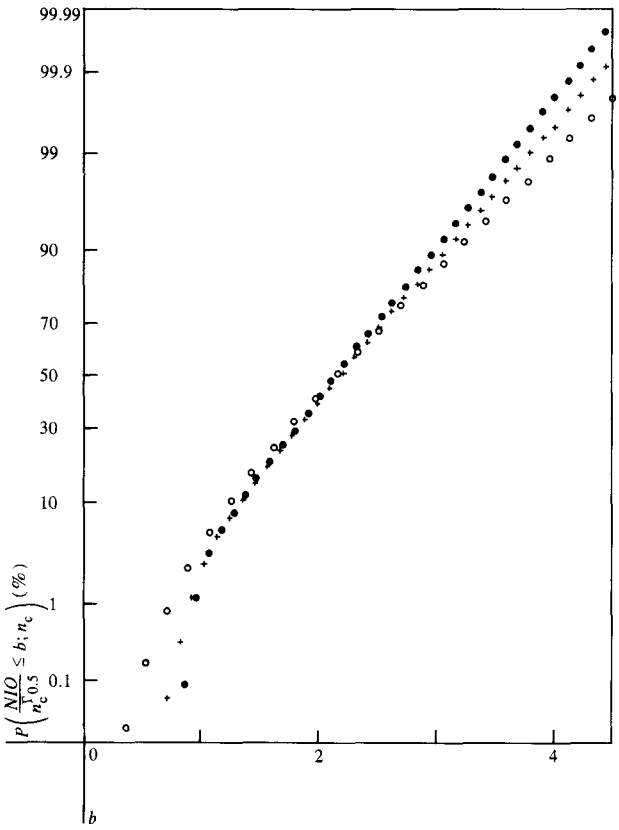


**Figure 4** The distribution of $NIO/n_c^{\Gamma_{0.5}}$ for calculated probability distributions of $NIO$ at constant partition sizes $n_c$ = 40 (○), 400 (+), and 4000 (●), using 360/9X ECL circuitry. $\Gamma_{0.5} = 0.6695 - 0.01059 \log n_c$.

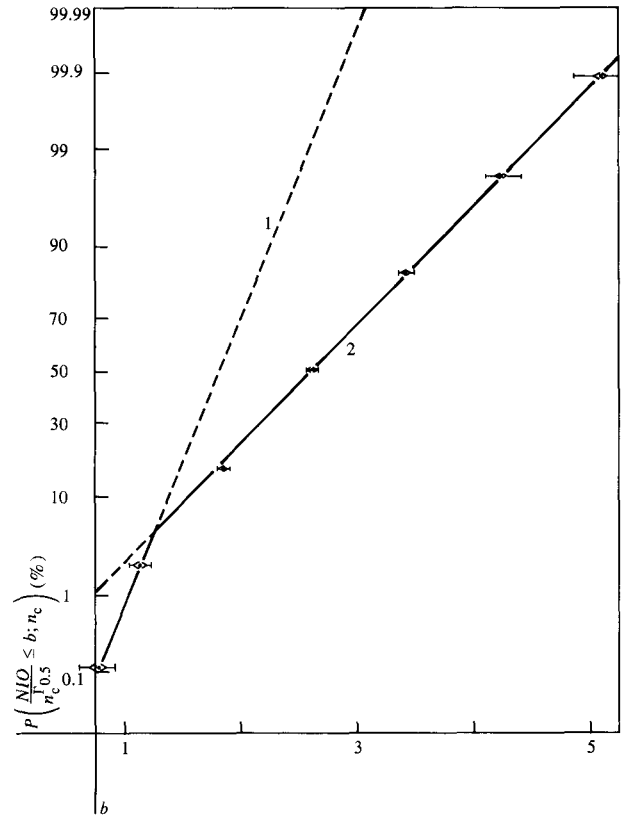


**Figure 5** Composite distributions for $b$ where $20 \le n_c \le 7000$ circuits. Curve 1: $\langle b_1 \rangle = 1.80, \sigma_{b_1} = 0.33375, b < 1.21784$; Curve 2: $\langle b_2 \rangle = 2.6164, \sigma_{b_2} = 0.80180, b \ge 1.21784$. The bracketed data points = $\langle b; n_c \rangle$, while the uncertainty in $b$ ($\pm\sigma$) is represented by the range of the bars on either side of the data points.

$PIO(n_c)$ are random variables. For $n_c = 1$, $PIO(n_c) = 1$, and

$$\langle NIO; 1 \rangle = \frac{\langle I_p \rangle}{2}\left[\frac{1}{2(1 - \langle 1/j_p \rangle)}\right]$$

is the average number of LSTs per circuit. For $n_c \to \infty$, $PIO(n_c) \to \delta << 1$, $\langle 1/j_p \rangle \to 1/2$, and $\langle NIO; n_c \to \infty \rangle \to [n_c\langle I_p \rangle/(2 - \langle \delta \rangle)]\langle \delta \rangle$, which is the average number of terminals required to connect $n_c$ circuits to other circuitry of a large system. The analysis calculates the probability distribution for $NIO$ with constant $n_c$ under the constraints imposed by the probability distributions of the random variables $I$, $j_p$, and $PIO(n_c)$, and also maximizes the variety of interconnection shapes. The details of the calculations require more space than is permitted here and thus are not presented at this time [5].

When the median value of $NIO$ for analytically derived $P(NIO \le NIO^*; n_c) = 0.5$ was plotted against $n_c$, an RMS fit of the median risk contour yielded

$$NIO_{0.5} = 2.616 n_c^{\Gamma_{0.5}};$$

$$\Gamma_{0.5} = 0.6695 - 0.01059 \log n_c. \quad (6)$$

The distributions $P(NIO \le NIO^*; n_c)$ were then transformed via

$$b = \frac{NIO}{n_c^{\Gamma_{0.5}}} \quad (7)$$

to

$$P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} \le b; n_c\right)$$

for $n_c$ = 40–10 000 circuits per partition, where $NIO^*$ is the variable range of $NIO$. Figure 4 displays the results of this transformation for $n_c$ = 40, 400, and 4000. Figure 5 displays the pooled distribution of $b$ and the uncertainty in $b$ for constant

$$P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} \le b; n_c\right).$$

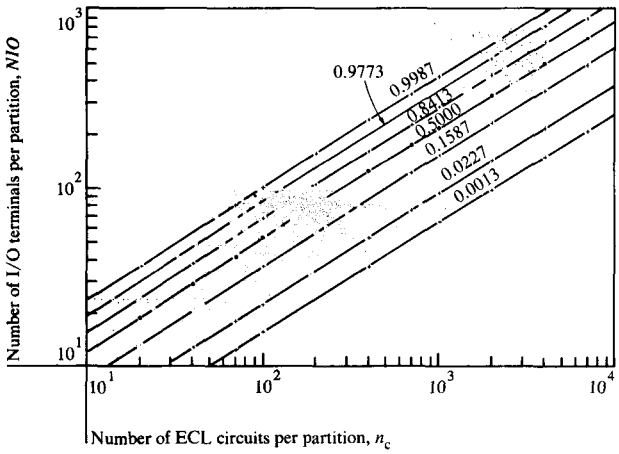


**Figure 6** Distribution of partition states for 360/9X ECL partitions as a function of the observed partitions for ECL parts. The data points are for 360/9X ECL cards and boards, 370/168 ECL cards and boards, and 370/158 4-W cards. Here, $\Gamma = 0.66952 - 0.010593 \log n_c$; $\langle b_1 \rangle = 1.80$, $\sigma_{b_1} = 0.33375$, and $b < 1.2178$; $\langle b_2 \rangle = 2.6164$, $\sigma_{b_2} = 0.80180$, and $b \geq 1.2178$. The numbers on the lines are the cumulative distributions in decimal form.

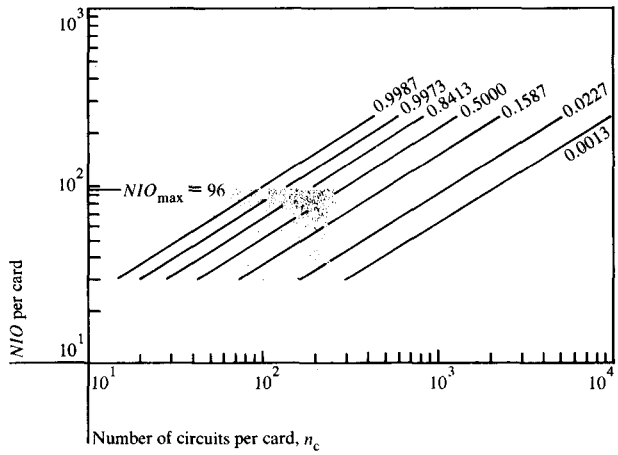


**Figure 7** Mapping of 343 4-W 60 × 72 PAC cards from 360/9X ECL circuitry into 330 unique ECL coordinates. The accumulative distributions for the lines are as in Fig. 6.

The results are similar to the behavior of $b$ for the 360/30 partitions. The droop in $b$ at low risk ($\lesssim 5\%$) is caused by the requirement that $NIO > 0$ for circuitry partitions. We will approximate

$$P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} \leq b; n_c\right)$$

by two piecewise continuous distributions, shown as solid- and dashed-line segments in Fig. 5.

Figure 6 displays constant risk contours (parallel curves) of

$$P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} \leq b; n_c\right)$$

and the $(NIO, n_c)$ coordinates of the physical parts of several systems (360/9X, 370/158 and /168) implemented with circuitry that has attributes similar to the random variables used in the analysis. The distribution of the physical parts corresponds to the region bounded by the risk contours. The risk contours indicate that considerably more circuits might have been mounted on cards with $\leq 96$ terminals, such as those supplied for the 360/9X; see Fig. 7. The module mix for the 360/9X cards did not permit mounting of more than $\approx 280$ circuits per card. The card and module set limited our view of possible partitions to those with $\leq 280$ circuits per card and $NIO \leq 96$ I/O terminals per card. In the case of the System 370/Model 158 (Fig. 8), the module set permitted a wide range of circuit counts of $\approx 60 \leq n_c \leq 1100$ circuits per card. In this case, the view of the possible

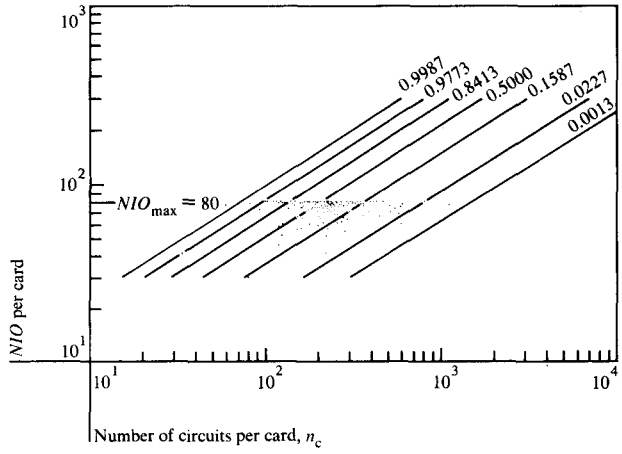


**Figure 8** Mapping of 136 4-W 3-Hi (72 PAC) cards from 370/158 circuitry into 135 unique ECL coordinates. Accumulative distributions are as in Figs. 6 and 7.

partitions is limited to those with $60 \leq n_c \leq 1100$ and $NIO \leq 80$. The distribution of the parts corresponds to the distribution implied by the risk contours. If one interprets the equation,

$$P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} = b; n_c\right)\frac{1}{n_c^{\Gamma_{0.5}}} = P(NIO; n_c), \tag{8}$$

as the probability that $n_c$ circuits will require $NIO$ I/O terminals, then within a contour such as that illustrated in Fig. 9(a), we may calculate

$$P(n_c; \text{within contour}) = \frac{1}{C}\sum_{NIO=NIO_1}^{NIO_2} P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} = b; n_c\right)\frac{1}{n_c^{\Gamma_{0.5}}}; \tag{9}$$

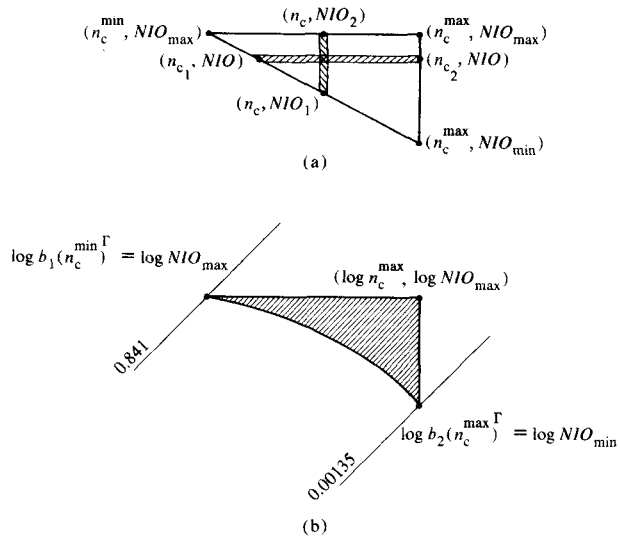


**Figure 9** (a) Partition contour in $n_c$ *versus* $NIO$ space. $NIO = NIO_{max} - \text{slope}(n_c - n_c^{max})$, where the slope $= [(NIO_{max} - NIO_{min})/(n_c^{min} - n_c^{max})]$. (b) Integration contour in log $n_c$ *versus* log $NIO$ space. The parallel straight lines represent risk levels of 0.00135 and 0.841. $b_1 = 4.22$ and $b_2 = 0.80809$.

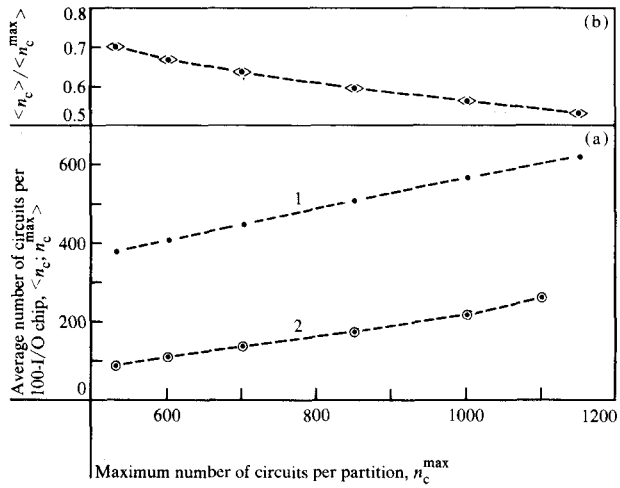


**Figure 10** (a) The average number of circuits per chip as a function of $n_c^{max}$, where $NIO_{max} = 100$ I/O terminals per chip. Curve 1 plots the average number of circuits per chip and Curve 2 plots the standard deviation in the number of circuits per chip. (b) Utilization of circuits on an ECL circuit chip, where $NIO \leq 100$. Note that no corrections have been made for yield fallout of more complex chips in either (a) or (b).

$$P(NIO; \text{within contour}) = \frac{1}{C} \sum_{n_c = n_{c_1}}^{n_{c_2}} P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} = b; n_c\right) \frac{1}{n_c^{\Gamma_{0.5}}}; \quad (10)$$

and

**Table 1** Calculated and observed values of $n_c$ and $NIO$ and their respective standard deviations on the 360/9X and 370/158 systems. For the 360/9X system, $NIO \leq 96$ pins per card and $n_c \leq 280$ circuits per card. For the 370/158, $NIO \leq 80$ pins per card and $n_c \leq 1100$ circuits per card.

| | *360/9X* | | *370/158* | |
|---|---|---|---|---|
| | *Observed* | *Calculated* | *Observed* | *Calculated* |
| $\langle n_c \rangle$ | 168.3 | 172.8 | 245.1 | 234.0 |
| $\sigma_{n_c}$ | 41.5 | 39.1 | 140.4 | 112.0 |
| $\langle NIO \rangle$ | 82.1 | 81.2 | 72.8 | 73.3 |
| $\sigma_{NIO}$ | 12.1 | 12.5 | 10.2 | 10.0 |

$$C = \sum_{n_c = n_c^{min}}^{n_c^{max}} \left[ \sum_{NIO = NIO_1}^{NIO_2} P\left(\frac{NIO}{n_c^{\Gamma_{0.5}}} \neq b; n_c\right) \frac{1}{n_c^{\Gamma_{0.5}}} \right], \quad (11)$$

in order to estimate the efficacy of a partitioning tactic, which is described by a contour containing accessible partitions. Care must be taken that the contour straddles the risk contours $P[(NIO/n_c^{\Gamma}) \leq b; n_c]$ 0.8413 and 0.1587, which contain the greatest density of possible partitions. Then Eqs. (8) and (9) produce distributions of $NIO$ and $n_c$ that correspond to the actual distributions of these variables for packaged logic partitions on the cards of the 360/91 and 370/158. For example, calculated values of $\langle n_c \rangle$, $\sigma_{n_c}$, $\langle NIO \rangle$, and $\sigma_{NIO}$ were obtained by integrating the probability $P(NIO; n_c)$ over the coordinates $(n_c, NIO)$ occupied by the parts. These calculated values are listed with the corresponding observed values in Table 1.

Let us now apply the information we described earlier to the following problem. First, we assume that we have a gate array technology that allows up to 100 I/O or signal connections to a silicon chip, and that the electrical power feed and thermal requirements of the chip can be satisfied over the range of our considerations. We must determine an upper bound, $n_c^{max}$, on the circuits allowed per gate array in order to utilize 67% of the $n_c^{max}$ circuits per chip. Second, we assume that a nine-chip-cell module is proposed as the next packaging level and that we must ascertain how many I/O connections must be supplied in order to maximize the average number of chip cells occupied per module.

First, we carry out the sums in Eq. (8) over the region contained in the contour of Fig. 9(b) for $n_c^{max} = 530$, 600, 700, 850, 1000, and 1150 circuits per partition and $NIO = 100$ signal terminals per partition. Figure 10 displays the average values of circuits per chip and the standard deviation of circuits per chip as $n_c^{max}$ increases. Normally, one takes into account the differences in yield fallout as the

**Table 2** Probability matrix for the module; $u = \Gamma(NIO_m^{max}/\langle NIO_c\rangle)$, an integer, and $j = (n_m - un_c^{min}) + 1$, where $j$ is the circuit count, $u$ is the number of occupied chip cells per module, and $n_m$ is given in circuits per module.

| $n_m$ | *Index of j* | $u$ | $u+1$ | $u+2$ |
|---|---|---|---|---|
| $un_c^{min}$ | 1 | $a_{u1}$ | 0 | 0 |
| $1 + un_c^{min}$ | 2 | $a_{u2}$ | 0 | 0 |
| • | • | • | 0 | 0 |
| • | • | • | 0 | 0 |
| $(u+1)n_c^{min}$ | $K$ | $a_{uk}$ | $a_{(u+1)K}$ | 0 |
| $1 + (u+1)n_c^{min}$ | $K+1$ | $a_{u(K+1)}$ | $a_{(u+1)(K+1)}$ | 0 |
| • | • | • | • | 0 |
| • | • | • | • | 0 |
| $un_c^{max}$ | $J$ | $a_{uJ}$ | $a_{(u+1)J}$ | 0 |
| $1 + un_c^{max}$ | $J+1$ | 0 | $a_{(u+1)(J+1)}$ | 0 |
| • | • | 0 | • | 0 |
| • | • | 0 | • | 0 |
| $(u+2)n_c^{min}$ | $M$ | 0 | $a_{(u+1)M}$ | $a_{(u+2)M}$ |
| $1 + (u+2)n_c^{min}$ | $M+1$ | 0 | $a_{(u+1)(M+1)}$ | $a_{(u+2)(M+1)}$ |
| • | • | 0 | • | • |
| • | • | 0 | • | • |
| $(u+1)n_c^{max}$ | $L$ | 0 | $a_{(u+1)L}$ | $a_{(u+2)L}$ |
| $1 + (u+1)n_c^{max}$ | $L+1$ | 0 | 0 | $a_{(u+2)(L+1)}$ |
| • | • | 0 | 0 | • |
| • | • | 0 | 0 | • |

distribution of partitions that may fit the gate array allows larger and larger circuit assemblies on the chip. We did not do so here because we want only to show how to use the information just presented. Yield effects would cause the average values to fall below Curve 1 of Fig. 10(a). Table 2 displays $\langle n_c\rangle/n_c^{max}$ as a function of $n_c^{max}$, and shows that $n_c^{max} = 600$ uses on the average 67% of the circuits implementable on the emitter-coupled logic (ECL) gate array chip.

The calculations described in Eqs. (8) and (9) must be changed to take into account the fact that the number of circuits that may be placed on a nine-chip-cell module depends on the distribution of the number of circuits that may be placed on a chip. Let $NIO_m^{max}$ be the maximum number of signal terminals allowed per module. Then the integer ceiling ($\Gamma$) of $NIO_m^{max}/\langle NIO\rangle_c$ is approximately the minimum number of chip cells expected to occupy a module; $\langle NIO\rangle_c \approx 88$ terminals for the chip just selected. It is possible that combinations of chips between the minimum and nine chips per module may require more I/O than $NIO_m^{max}$, and therefore must be excluded from consideration. In addition, the absolute maximum number of circuits per module is $9 \times 600 = 5400$. One may thus proceed by computing the distributions of circuits accessible to $x$ chips by calculating the $x$-fold convolution of the probability distribution of the number of circuits per chip, starting with the minimum number of chips and proceeding to the nine-fold convolution. Each $x$-fold convolution produces $P(n_m, x)$, the probability that an aggregate of $x$ chips will add up to $n_m$ circuits per module.

Let $NIO_m^{max}$ be the maximum number of I/O terminals per module,

$$n_m^{max} = 9n_c^{max} < \left(\frac{NIO_m^{max}}{0.8089}\right)^{\Gamma^{-1}},$$

$$n_m^{min} = (NIO_m^{max}/4.22)^{\Gamma^{-1}},$$

and

$$NIO^{min} = 0.8089\,(n_m^{max})^{\Gamma}$$

(in each case, $\Gamma$ is a function of the particular $n_m$ involved) define a contour similar to Fig. 9(b) for the nine-chip-cell module. The quantities in the matrix of Table 2 are calculated as follows over summation strips defined in Fig. 9(a). Let

$$a_{xn_m} = \sum_{NIO_m = NIO_1}^{NIO_2} P\left(\frac{NIO_m}{n_m^{\Gamma}} = b; n_m\right)\frac{1}{n_m^{\Gamma}}P(n_m, x) \qquad (12)$$

and

$$C = \sum_{x=u}^{9}\sum_{j=1}^{J} a_{xj}\,;\; u \approx \left\lceil \frac{NIO_m^{max}}{\langle NIO\rangle_c}\right., \qquad (13)$$

where $J = [(9n_c^{max} - un_c^{min}) + 1]$. The probability of $n_m$ circuits per module is

$$P(n_m; NIO_m^{max}) = \left(\frac{1}{C}\right)\sum_{x=u}^{9} a_{xn_m}. \qquad (14)$$

The probability of $n_{mc}$ chip cells occupied per module is

$$P(N_{mc}; NIO_m^{max}) = \left(\frac{1}{C}\right)\sum_{j=1}^{J} a_{n_{mc}}\, j. \qquad (15)$$

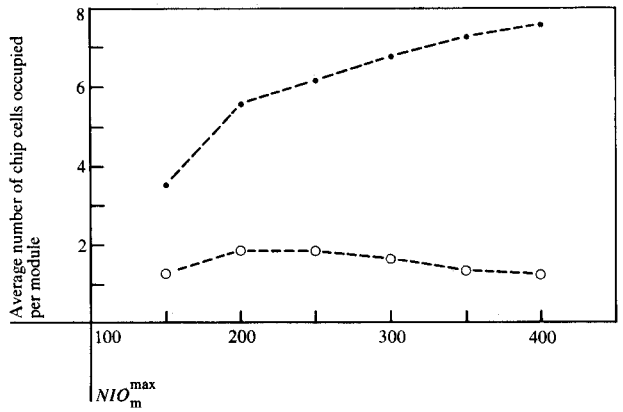


**Figure 11** The average number of chip cells occupied per nine-chip-cell module (●) and the associated standard deviation (○) as a function of the average number of chips mounted per module increase; $n_c \leq 600$ circuits per chip and $\langle n_c \rangle / 600 = 0.66$.

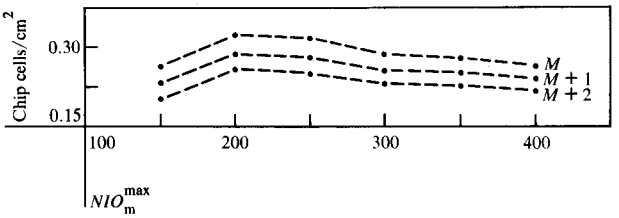


**Figure 12** The density of occupied chips for projected connector areas for a nine-chip-cell module as a function of $NIO_M^{max}$, the maximum number of I/O terminals per module; $d = 2.5$ mm.

A matrix similar to that shown in Table 2 and equations corresponding to (12)–(14) will produce the probability distribution of the use of I/O terminals for the nine-chip module. We leave this exercise to the reader. Figure 11 displays the average number of chip cells occupied per nine-chip-cell module and the standard deviation for the same quantity *versus* the $NIO_m^{max}$ obtained by executing the calculations just described. As we increase $NIO_m^{max}$, the average number of chips mounted per module increases. However, from a systems point of view we desire a module which maximizes the density of occupied chip cells at the packaging level that carries the modules. Let us presume the following in order to facilitate the calculations: 1) The module has a form factor similar to the nine-chip IBM 4300 modules; 2) The power requirements can be satisfied by supplying five I/O pins per chip cell; and 3) We have a printed circuit that can wire the modules together.

The minimum area on a printed circuit for such a module is then

$$A_M = Md^2 \geq (NIO_m^{max} + 45)d^2, \tag{16}$$

where $M$ is the smallest integer that will satisfy Eq. (16) and $d = 0.25$ cm. Equation (16) requires that the modules be brick-walled. If an 0.25-cm space is required between the modules, $A_M = (M + 1)d^2$, etc. Figure 12 displays the average density of occupied chip cells per cm$^2$ at the printed circuit board for $d = 0.25$ cm, for modules on $Md$, $(M + 1)d$, and $(M + 2)d$ *versus* $NIO_m^{max}$. A relative maximum in the chip density is found in the vicinity of $NIO_m^{max} = 190$–$250$.

Thus, considering our constraints on the chip and module choices, a nine-chip-cell module with 256 pins in a 16 × 16-pin array is a reasonable selection from a systems point of view.

## References and notes


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