P. Frasch
K. H. Saremski

Feature Size Control in IC Manufacturing

Until recently, the ever-increasing demand for higher device density in integrated-circuit (IC) designs has been satisfied mainly through device and circuit design ingenuity, increased chip size, and dimensional reduction. To keep pace with dimensional reduction, control of dimensional variations has assumed a more significant role. New IC designs are very dense and performance-oriented, requiring 2-μm lithography ground rules with less than ±0.2-μm variations in circuit-feature dimensions at 3σ. Such small variations are difficult to detect and control with the present-day routine in-line-inspection optical tools. In this article, we present a description of the primary causes of dimensional variations in a typical manufacturing environment and proposals for their control.

Introduction

During the manufacture of chips designed with a low signal-to-noise ratio, *e.g.*, high-density memory chips, partial bit line failures may be detected during electrical testing. Invariably, no physical defects can be found to explain these failures. However, patterns of the failure distributions, when mapped, show a striking resemblance to striation patterns. For example, Fig. 1(a) shows bit line failures on one side of the sense amplifiers on a chip, and Fig. 1(b) shows failures resembling typical striation patterns. Since the only meaningful explanation for the electrical failures is pattern dimension variations, an extensive evaluation program to study the effects of striation on dimensions was begun. During the study, we indeed discovered parameters that influence dimension control. We also found that the measurement methods used in manufacturing were not always adequate for our study for determining small but important dimensional differences at the chip level.

Before we could proceed, therefore, we had to evaluate different measurement techniques to find one adequate for our use. We investigated optical, electrical, and scanning electron microscope (SEM) methods of determining within-chip, chip-to-chip, wafer-to-wafer, and lot-to-lot dimensional variations of resist materials. These investigations are described in Section 1 of this paper.

We next had to define a test for striations which included optical appearance, amplitude, and periodicity. A modified Talysurf turned out to be the key for determining the striation formation of different resists, including diazo-type resists ®AZ-1350J, ®AZ-1450, ®AZ-1470, and HPR204, and a diazonaphthoquinone-®Novolak (DNQN) system [1]. This, together with variations due to the resist application method, is described in Section 2.

A common practice in photolithography is to use exposure time to compensate for and correct image sizes. We investigated over- and underexposure modes, and thus we propose methods to use these effectively in a manufacturing environment in Section 3 of this paper.

Since the use of pellicles as a protective device against mask defects is common manufacturing practice, we had to be sure that their use did not contribute to further dimensional variations. Our findings are discussed in Section 4.

Finally, we experimented with different resist systems for integrated-circuit (IC) manufacturing, checking their performance for dimensional variations, absence of striations, and ease of processing. These experiments are summarized in Section 5. There are other factors that can affect the photolithography, such as exposure uniformity, quality of the optical image, and depth of focus (including wafer flatness and flatness of underlying films). Since these do not vary significantly in our manufacturing setup, the effects of their variance are not discussed here.

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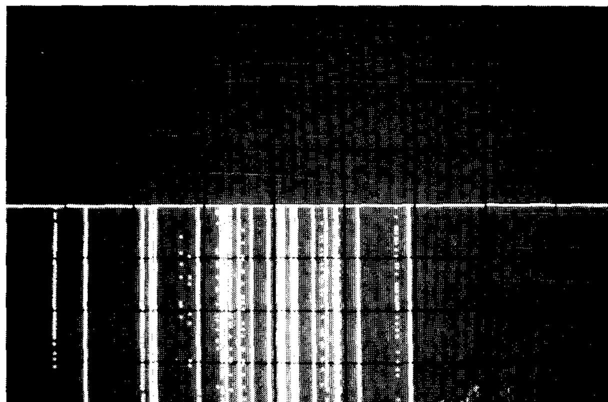
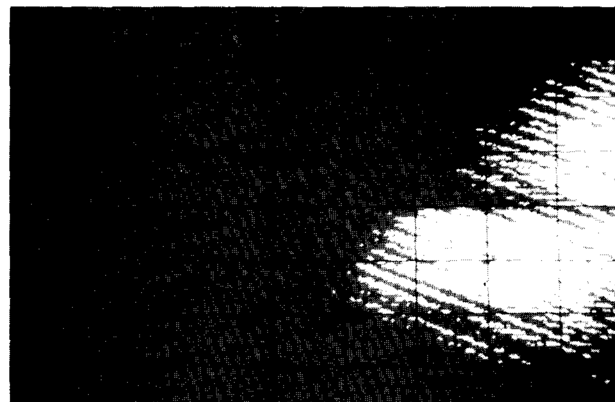
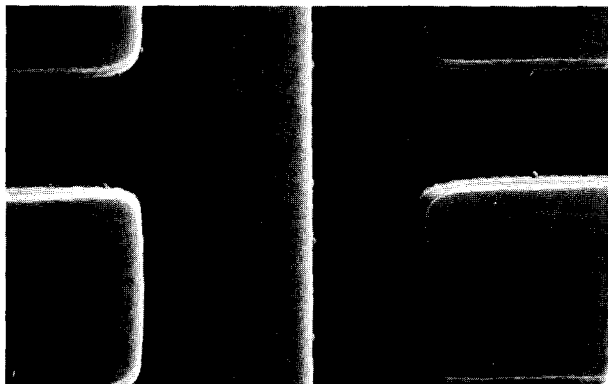


(a)



(b)

Figure 1 (a) Electrical bit failure map showing partial bit line failures. The white spots indicate failing bits. (b) Electrical bit failure map clearly demonstrating striation patterns.



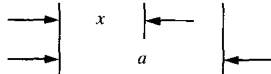


Figure 2 SEM of storage node and bit line of a SAMOS RAM used for pitch measurement. Here a is a known reference pitch, and x is the spacing to be measured.

We conclude that dimension variations causing intolerable circuit asymmetries are mainly due to resist striations, exposure variations, and pellicles. However, dimension control can be maintained in the manufacturing environment through the proper choice of resist, mask design, and exposure compensation. The paper ends with proposals for manufacturing future IC devices using the proper resist systems and measurement methods.

The authors realize that their results may not apply generally. The results are valid for the Perkin-Elmer 1× projection printing system which was used in the experiments [2]. Before using our findings on other tools, it is suggested that similar experiments using the specific tools be conducted.

1. Measurement techniques for small images

With decreasing feature sizes, the measurement of features in the manufacturing environment becomes more difficult. For example, trying to measure printed features in 1.2–1.8-μm-thick resist using today's standard manufacturing projection printing tools gives rise to high resist slopes of 60°–70°, which weakens the ability to distinguish between top and bottom edges and thereby leads to inaccuracies. Newer measurement techniques, such as electrical image size measurements or SEM pitch measurements, may be required.

Optical measurement A Leitz Latimet measurement system [3] is used at the IBM Sindelfingen pilot line for in-line operational control of exposure settings and etch time adjustments. Measurement precision of this tool is ±0.1 μm (3σ). Unless otherwise stated, data in this article were obtained with this device.

Electrical measurement Source drain spacing and gate widths are measured electrically with special monitors on the kerf structure in the SAMOS [4a] technology in a routine manner. The measurement is performed at the first chip test. However, the long lead time between the process step at which the structure is formed and the process step at which it is measured is a big disadvantage. The only real benefit for measurements at this step is the high volume of data which can be obtained in a very short test period.

SEM measurement The most accurate measurement method available today is the SEM, where a known pitch is used as a reference [4b]. Pitch is defined as the distance between two corresponding image edges. This is determined by design and does not change in the process. It is illustrated in Fig. 2. Note that the design pitch can be used as a standard for adjusting the scale on an SEM photograph.

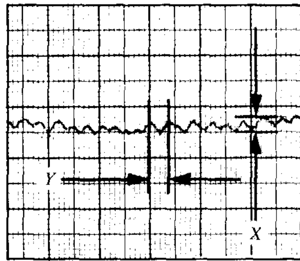


Figure 3 Talysurf diagram of typical striation patterns and the definition of its characteristics. X is the amplitude of striation, averaged from 10 repeating wave measurements. Y is the period of striation, again averaged from 10 repeating wave measurements.

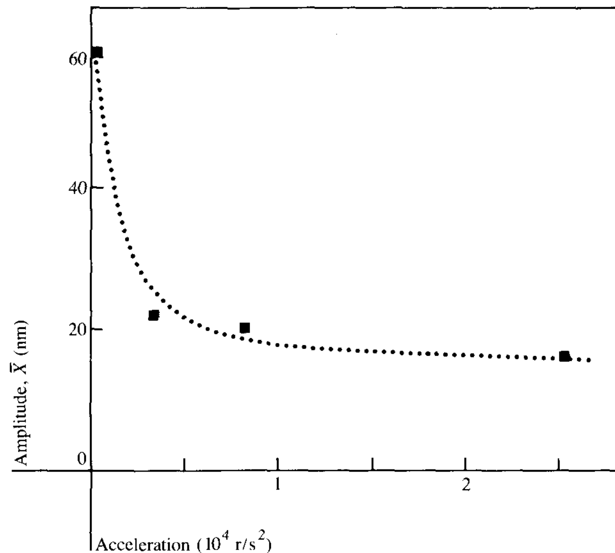


Figure 4 Influence of spin-table acceleration on striation amplitude.

2. Resist striations

Striations are resist-thickness variations generated during the resist-application operation. These variations emanate radially from wafer centers and are also called ripples in the IC lithography literature [5]. Radially distributed striations are a natural consequence of the physics of spinning during the resist application process in which a viscous fluid experiences Newtonian forces. This has been explained by Gazley and Charwat [6] as one of the limitations of resist lithography. However, radial forces causing radial thickness variations, which in turn cause variable resist exposures, can only explain the striations qualitatively.

Striations cause feature size variations within a chip and have been observed to result in asymmetries in structures which should be identical. Striations are resist-system dependent and can be reduced by the use of a proper application process. We have found a good method for determining resist-thickness variations by means of a mechanical surface roughness measurement employing a Talysurf system using a spherical diamond as a pickup.

Standardization of measurement To compare different resists and different resist application techniques, we had to standardize the measurement technique and to define the wafer location at which the measurements were to be taken. After a few experiments we found a fast and conclusive method. All measurements were made at a distance of 15 mm from the wafer edge, traveling across the wafer, with the Talysurf adjusted to a speed of 0.25 mm/s, using a spherical diamond with a sensitivity of 10 nm/mm on trace paper. Figure 3 shows a typical Talysurf plot. We chose to define the amplitude of striation, X, by measuring ten successive waves and then averaging the measurements. Similarly, we defined the period of the striations, Y, by averaging the measurement of the periods of ten consecutive waves.

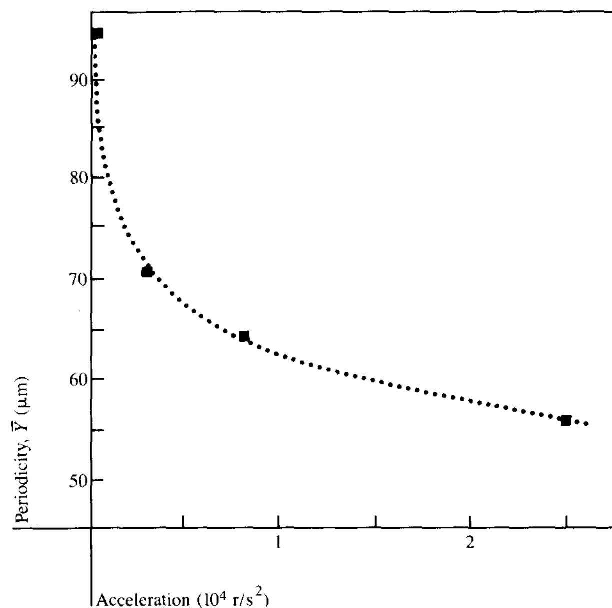


Figure 5 Influence of spin-table acceleration on striation periodicity.

Resist application process To determine the influence of the resist application process on striation, a resist system which is known to have striations (®AZ-1350J, diluted to a viscosity of 0.019 Pa-s) was used in a large-chuck spindle with a nominal spin speed of 3000 revolutions per minute. Measurements were taken with the resist subject to different accelerations. The results are shown in Figs. 4 and 5. With increasing acceleration, amplitude and periodicity of striations decreased. To achieve the best results, we decided to use

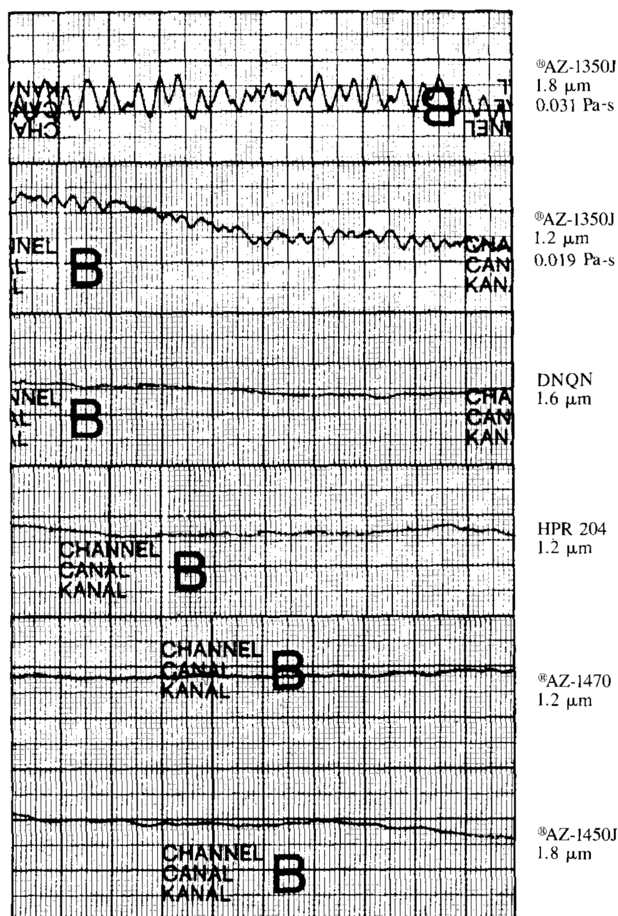


Figure 6 Talysurf diagrams of different resists after the application and baking processes but *prior* to development. The ®AZ-1350J resist shows a distinct ripple striation effect; the others do not.

Table 1 Striation behavior of different resist systems.

Resist system	*Amplitude*		*Periodicity prior to develop.* (μm)
	Prior to develop. (nm)	*Post-develop.* (nm)	
®AZ-1350J 0.019 Pa-s	20	30	70
®AZ-1350J 0.031 Pa-s	50	≥80 (Peaks to 120)	60
®AZ-1470	0	10	—
®AZ-1450	0	≥40 (Peaks to 120)	—
HPR 204	< 5	15	—
DNQN	5	15	—

accelerations greater than 8000 revolutions per second per second (r/s^2). We noted also that striations could not be eliminated by the application process alone. The resist system used also played a very important part, as did the solvents used to make up or dilute the resists (which contributed not only to the evaporation rates but also to the concentrations), the airflow rate, the air speed, and the air temperature in the chuck area, which all influenced the striation.

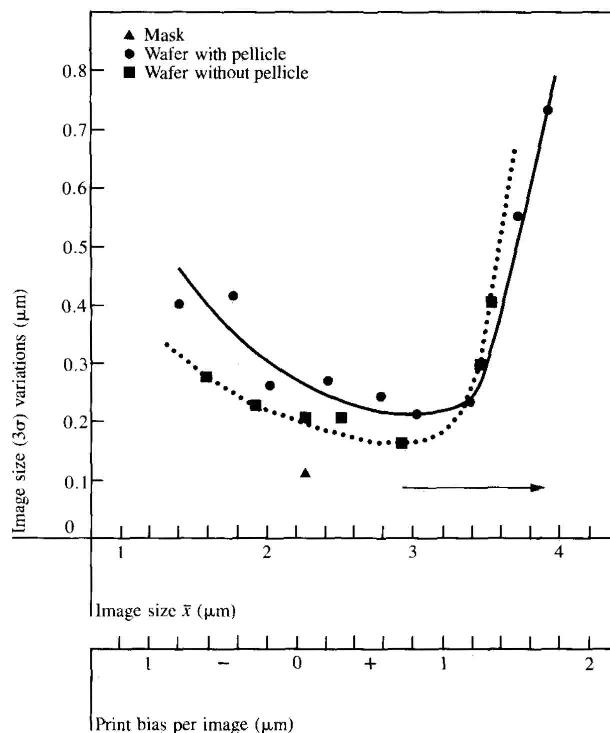
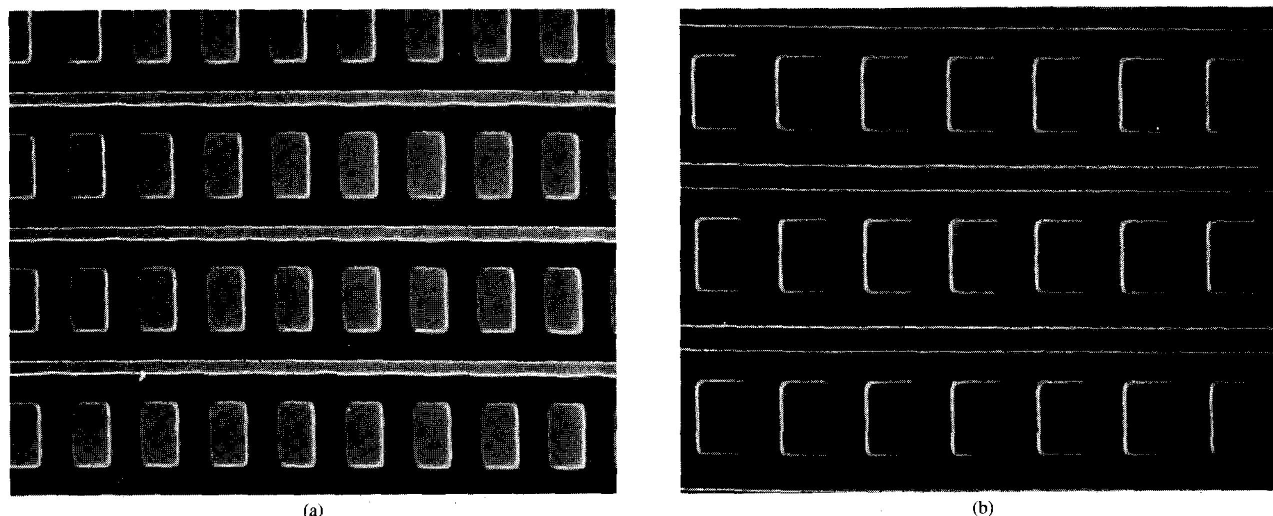


Figure 7 Influence of exposure conditions on chip-to-chip image size variations. Arrow on horizontal axis indicates overexposure direction. Triangle represents 2.2-μm mask feature. Note that the use of the pellicle results in a slight increase in feature size variations.

Resist systems Five different resist systems were investigated regarding striation behavior at nominal resist thickness on both 82-mm and 100-mm wafers. In addition, the influence of the development process using a standard developer was determined. As can be seen from Table 1, the ®AZ-1350J resist displays striations while the others do not. The striation effect was enhanced when the unexposed resist was treated with a developer. The Talysurf curves are shown in Fig. 6. No significant differences were found between the smaller and the larger wafers.

3. Exposure dosage

As image size adjustments are often made by varying the exposure time, it is of interest to determine whether dimensional variations can be influenced by over- or underexposure. Also, since the use of pellicles is required in a manufacturing environment to prevent high defect rates, our investigation of mask/pellicle combinations is mainly of practical



(a) (b)

Figure 8 (a) Waviness of bit lines after etching is completed is due to inadequately controlled exposure of the mask, resulting from the proximity effect. (b) Enlargement of the SAMOS cell patterns and bit lines showing the elimination of the proximity effect through corrected exposure setting on the same mask as in Fig. 8(a).

interest. The mask-without-pellicle investigation was done for comparison purposes. The experiments performed for Fig. 7 were as follows: Five wafers were taken in each exposure batch. Using 5, 7, 9, and 13 units of exposure through the pellicle mask of each, 15 chips per wafer in one position and one chip per wafer in ten different positions were developed and measured. We observed that the dimensional variations decrease with increasing amounts of light arriving at the wafer surface. This confirms earlier findings which suggest a slight overexposure as the manufacturing strategy to follow. For the photolithography to run true despite the overexposure, a 0.5-μm compensation should be made in the mask design (constant development and baking).

As a byproduct of the above experiment, a proximity effect was observed. This can be clearly seen in Figs. 8(a) and 8(b), which contain 2.0–2.5-μm features. The influence of the neighboring storage nodes on the bit linewidths is quite apparent. Again, compensation in the mask design could minimize this effect.

4. Pellicle contributions

Earlier investigations have shown considerable loss of transparency of Mylar pellicles when exposed to ultraviolet (uv) light. Also, because of dispersed inorganic fillers in the commonly used Mylar pellicle material, dimensional differences in very small areas are known to occur. Although the present trend in industry is to use nitrocellulose pellicles which are clearly superior to Mylar, we developed an experiment using mid- and deep-uv light exposure on Mylar pellicle material to determine the influence of transparency loss on

Table 2 Influence of pellicle on image size variations.

Parameter	*Image size variations* (3σ), (μm)	*Sample size*
Mask without pellicle	±0.31	160
Mask with pellicle	±0.42	160

feature size variations [7]. In an experiment, we exposed wafers through a 1× mask as a base. Then we added a pellicle to the mask and repeated the exposures. After aging the pellicle with uv light, we again repeated the exposures. We measured the feature sizes of 40 chips on each wafer, and compared the feature size variations after 1.5, 6, and 27 hours of aging. Table 2 provides the results of this experiment and shows that the feature size variation is 0.11 μm greater if a pellicle is used. However, long exposure to uv light did not provide any significant effect on feature size variations. (We subjected the pellicle material to 27 hours of exposure with a high-pressure mercury lamp. This exposure amounts to approximately 18 000 passes under ordinary manufacturing conditions, and it did contribute to some noticeable loss of transparency, but no noticeable difference in image size variations.)

5. Resist systems

A comparison of feature size variations for different resist systems was obtained by measuring three lots per resist system. We took five measurements per chip of the source-

Table 3 Within-chip feature size variations with different resists.

Resist system	*Average within-chip variations* (3σ), (μm)
®AZ-1350J	±0.55
®AZ-1470	±0.37
HPR 204	±0.26
DNQN	±0.28

Table 4 Chip-to-chip feature size variations with different resists.

Resist system	*Developing technique*	*Chip-to-chip size variations* (3σ), (μm)
®AZ-1350J	®AZ 1:1 developer, tank	±0.90
®AZ-1470	®AZ 1:1 developer, tank	±0.53
HPR 204	®AZ 1:1 developer, tank	±0.60
DNQN	KOH. 1.7%, puddle development	±0.88

to-drain spacing formed in the "A" layer of SAMOS technology wafers taken from the manufacturing line. The results are shown in Table 3. As expected, the worst results were obtained with ®AZ-1350J because this resist could not be used striation-free.

Another comparison, that of chip-to-chip feature size variations, was also made. This time not only the resist but also the development technique affected the outcome. Table 4 shows the results. Again ®AZ-1350J exhibited the worst results. Note also that the DNQN resist did not perform as well as the ®AZ-1470. This is probably due to the different (puddle *vs.* tank) development process used with the single wafers. It should also be noted here that the chip-to-chip measurement includes the wafer-to-wafer (within lot) feature size variation.

6. Conclusions

For future memory chip manufacture using 2-μm lithography, it is necessary to control image sizes much closer than we do today. This is due to the more stringent requirements of the signal sensitivities called for by the chip designs, and the overall electrical sensitivities to feature variations. The experiments we conducted prove that there are ways of controlling feature sizes with a careful mix of resist system, exposure variation, mask design compensation, and development (puddle *vs.* tank) processes. The work presented in this paper is based on the measurements taken on some 1000 wafers processed through the manufacturing line. This huge data base enables us to make the following recommendations for a 2.2-μm ground-rule-optimized photolithography process with adequate dimensional control:

1. The choice of a striation-free resist is the key to good image size control. One major solution to reducing striations is to use a suitable photoresist system. Our measurements clearly identified two groups of photoresists, one with and one without striations.
2. Overexposure with mask design compensation permits a wider process latitude. Overexposure yields additional image improvements. This requires image size compensations in the mask of about 0.5 μm.
3. Pellicle film material can have an effect on dimensional variations. While we found no changes in image size variation under our exposure conditions, we believe the material used should not be sensitive to uv light. Mylar pellicle material does contribute to feature variations on the wafer. We found, however, that aging of that material due to uv light had little or no additional effect. Since our study of only one material may not apply generally, we recommend further studies of pellicle materials since pellicles will undoubtedly continue to be used in manufacturing operations.
4. Current optical measurement techniques seem to be adequate for in-line process control. SEM measurements may be used to calibrate the optical in-line measurement tools. In addition, for long-term adjustment of the manufacturing line, electrical measurements of the key parameters should be continued.

7. Acknowledgments

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References and notes

1. ®AZ is a registered trademark of American Hoechst Corp., Route 202-206 No., Somerville, NJ. Their licensed distributor is the Shipley Corp., Newton, MA. The HPR204 is supplied by Philip A. Hunt Co., Palisades Park, NJ. The DNQN is an experimental resist.
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7. Although slight changes were noted in the optical absorption of the treated pellicles, we found no evidence for any change in the image size variation under our manufacturing process conditions.

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Peter U. Frasch *IBM Germany, P.O. Box 266, 7032 Sindelfingen, Federal Republic of Germany.* Mr. Frasch, a chemical engineer since 1963, joined IBM in 1965 at the Sindelfingen plant material laboratory. He worked on analysis of manufacturing problems and on developing new screen coating materials. Since 1971, he has worked in the field of semiconductor process development. His background is in contamination control. He has received an IBM Invention Achievement Award in the area of lithography and other processes. Mr. Frasch is currently on assignment at the IBM General Technology Division, Burlington facility, Essex Junction, Vermont 05452, where he is the German Team leader.

Karl Heinz Saremski *IBM Germany, P.O. Box 266, 7032 Sindelfingen, Federal Republic of Germany.* Mr. Saremski joined IBM in 1974 and is a product engineer in an integrated circuit processing facility. In 1973, prior to joining IBM, he received his chemical engineering degree from Naturwissenschaftlich-Technische Akademie, Isny, Federal Republic of Germany. Since joining IBM, he has worked in the field of photolithography, especially in the field of new technologies useful for manufacturing processes.