C. H. Stapper

Modeling of Integrated Circuit Defect Sensitivities

Until now only cursory descriptions of mathematical models for defect sensitivities of integrated circuit chips have been given in the yield literature. This paper treats the fundamentals of the defect models that have been used successfully at IBM for a period of more than fifteen years. The effects of very small defects are discussed first. The case of photolithographic defects, which are of the same dimensions as the integrated circuit device and interconnection patterns, is dealt with in the remainder of the paper. The relationships between these models and test sites are described. Data from measurements of defect sizes are discussed.

1. Introduction

Previous papers [1–3] described models used to project and control manufacturing yield of large-scale integrated circuits. These statistical models estimate the number of failures or faults per chip. Such faults are caused if defects occur in those parts of the chip where they result in failures. The purpose of this paper is to investigate the interaction between defects and integrated circuit structures or patterns. As a consequence of this approach it becomes evident that defect densities can be measured with defect monitors.

Defect sensitivities are treated in two parts in this paper. First we investigate very small defects, which often occur in the chip insulators. These are known as dielectric pinholes. The basic concept of critical areas becomes intuitively obvious for these defects.

The second class of defect sensitivities includes defects that have sizes comparable to those of the VLSI patterns. All photolithographic patterns are in this class. The theory needed to deal with these defects must first address the defect sensitivity for each defect size. The second part of the theory must incorporate the size distribution of defects. By combining the size distribution with the defect sensitivities, a theory can be developed for photolithographic defects that is similar to the theory for very small defects. Again, it becomes possible to design defect monitors to determine both the defect densities and the nature of the defect size distribution.

The yield monitoring and yield modeling methods that form the core of this paper make it possible to continually check the self-consistency of the yield models in an actual process. Defect densities and defect size distributions can be evaluated against the actual yield performance of the product. When the parameters do not perform as expected, they can be measured with defect monitors and the model can be adjusted to be an accurate representation of reality.

2. Pinhole defects

One class of defects, known as pinholes, occurs in dielectric insulators such as thin and thick silicon oxides, oxidized polysilicon, chemical vapor deposited insulators, quartz, etc. These defects are usually much smaller than a micrometer. Their occurrence can result in a short circuit between conductors produced at different photolithographic levels. The area in which such defects cause failures is the overlap region between two conductors that cross each other, as shown in Fig. 1. Defects that fall outside these overlap areas cannot cause short circuits. We call the overlap where failures do occur the "critical area." The words "defect-sensitive area" and "susceptible area" have also been used in the same context.

Critical areas of pinholes in most designs can be determined readily as the total overlap area between patterns at different photolithographic levels. When the integrated circuit masks are generated with a computer, algorithms are

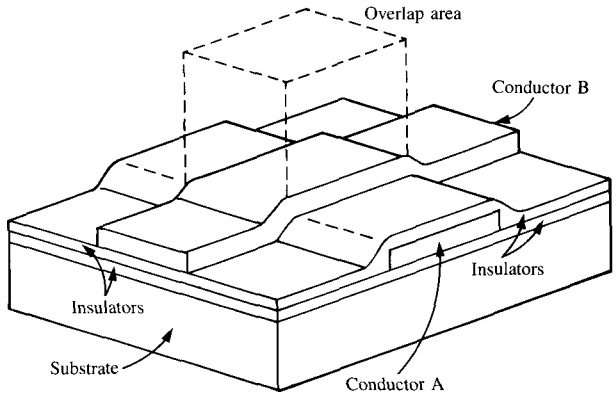

Figure 1 The critical area for pinholes is the overlap area between the two conductors.

often available to determine this area for an entire chip. The result must be less than the total chip area. Let θ be the fraction of chip area A that is sensitive to pinholes. The critical area A_c can then be expressed as

$$A_c = \theta A. \tag{1}$$

The average number of failures or faults caused by the defects can now be calculated by

$$\lambda = A_c D \tag{2a}$$

$$= \theta A D, \tag{2b}$$

where D is the density of defects per unit area. This is the direct relationship between defect densities and the average number of faults that also was discussed in previous papers [1, 2].

Some investigations into the defect densities of dielectric pinholes have shown that the average number of failures per monitor can be proportional to the monitor length [4]. A typical structure where this can occur is shown in the cross section of a charge-coupled device in Fig. 2. Stress effects between the two polysilicon patterns create defects along the edges of the overlap area.

To model these effects one has to count the number of faults that occur along an overlap section of length L. It is then possible to define

$$\lambda = L D_L, \tag{3}$$

where D_L is the density in defects per unit length. This is a model that differs significantly from the area model, since the defect densities are in different units. Yet, if both the area and the length pinhole effects take place in the same chip, their combined number of faults is given by

$$\lambda = A_c D + L D_L. \tag{4}$$

This result demonstrates an important principle in yield modeling: *Faults caused by different failure mechanisms can be added, but defect densities for different failure mechanisms cannot be added.* In this example the defect densities have to be modified by both the critical area and the critical length to become faults.

It is possible at this point to expose a myth that seems to recur constantly in yield models used by the semiconductor industry. This myth assumes that the yield can be modeled with only one critical area and one defect density, regardless of the process complexity. Even though thus far we have discussed only one defect type, namely, pinholes, we already see that such an averaging process is impossible. It should be clear that the introduction of other defect types should make this simplification even less likely. The only simplification possible is the use of the cumulative average number of faults λ to which all these defects contribute.

3. Pinhole defect monitors

The relationship between the average number of faults for area pinholes and the defect density D is a simple proportionality. This simplicity has a useful application. If we have a process without a linear pinhole problem, we can make defect monitors that consist only of a large overlap area between two conductors. By measuring the resistance between the conductors, we can determine when the monitors are short-circuited and fail due to pinholes.

Let us assume that we have made N of these monitors and we find that U of these are short-circuited. The monitor yield Y_m is then given by

$$Y_m = \frac{N - U}{N}. \tag{5}$$

We now want to estimate the average number of faults that cause these failures. Unfortunately, we have no way of knowing how many faults cause a monitor to fail. In most cases it is only one fault, but there can be instances in which two or more defects cause two or more faults. If the defect density is constant in the sample and the defects occur at random, then the distribution of the number of faults per monitor is given by a Poisson distribution [3]. For X faults per monitor this distribution can be written as

$$P(X = x) = \frac{e^{-\lambda_m}(\lambda_m)^x}{x!}, \tag{6}$$

where λ_m is the average number of faults per monitor and $x = 0, 1, 2, \cdots$. The probability of having zero faults is

$$P(X = 0) = e^{-\lambda_m}. \tag{7}$$

But this must be equal to the yield given in (5). It is therefore possible to solve for λ_m and obtain

$$\lambda_m = -\ln Y_m \tag{8a}$$

$$= -\ln\left(\frac{N-U}{N}\right). \tag{8a}$$

With the average number of faults known, it is now possible to determine the defect density with

$$D = -\frac{\ln Y_m}{A_m}, \tag{9}$$

where A_m is the critical area of the monitor.

With the pinhole defect density known, it is possible to calculate the pinhole-limited yield for any product that is made with the same process as the monitors. If the pinhole critical area for such a product is given by A_p, then the pinhole yield is

$$Y_p = e^{-A_p D}, \tag{10}$$

where D is the defect density determined with the monitor. Use of Eq. (9) makes it possible to express the product yield in terms of the monitor yield:

$$Y_p = \exp(A_p/A_m) \ln Y_m \tag{11a}$$

$$= Y_m^{A_p/A_m}. \tag{11b}$$

This is an interesting result, showing that we can scale the monitor yield to the product yield with an exponent given by the critical area ratio. This is often referred to as "area scaling." However, we must remember that it is the ratio of critical areas that must be used here, not the ratio of actual areas of the chip and monitor. The latter is only correct if the probability of failure θ is the same for both the monitor and product.

Since the beginning of integrated circuit manufacturing, it has been clear that most defects do not have the uniformly random distribution required for Poisson statistics [5–8]. Negative binomial statistics have been found to give a better fit to the data in many cases [1, 3, 9, 10]. The yield formula related to these statistics is

$$Y_m = (1 + \lambda_m/\alpha)^{-\alpha}, \tag{12}$$

where α is a cluster parameter. This parameter can be estimated from monitor data as described in [9, 10].

Solving expression (12) for the average number of faults per monitor results in

$$\lambda_m = \alpha(\sqrt[\alpha]{1/Y_m} - 1). \tag{13}$$

The defect density is therefore given by

$$D = \alpha(\sqrt[\alpha]{1/Y_m} - 1)/A_m. \tag{14}$$

Since the yield for the product is given by

$$Y_p = (1 + A_p D/\alpha)^{-\alpha}, \tag{15}$$

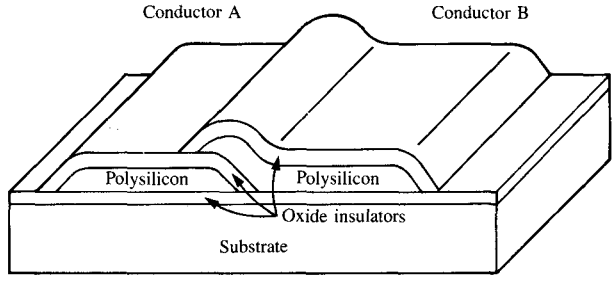

Figure 2 A conductor structure that leads to length defects.

substitution of the expression for D in (14) gives

$$Y_p = [1 + (\sqrt[\alpha]{1/Y_m} - 1)A_p/A_m]^{-\alpha}. \tag{16}$$

Yield scaling with these statistics is not as convenient as it was with (11b), but the greater accuracy of (16) has resulted in its use for integrated circuit chip manufacturing defect measurements. Area pinhole monitors have been used at the IBM plant at Essex Junction, Vermont, since the early seventies. Data from these monitors are scaled to product yield with (16).

The line pinholes can be monitored the same way as the area pinholes, provided only line defects occur in the monitor. The case in which both defect types are present is discussed in the next section. In the case of Poisson statistics, the line defect density can be obtained by

$$D_L = -\frac{1}{L_m}\ln\left(\frac{N-U}{N}\right) \tag{17}$$

$$= -\frac{\ln Y_m}{L_m}, \tag{18}$$

where L_m is the monitor length, N the number of monitors tested, U the number of failing monitors, and Y_m the monitor yield.

Scaling the monitor yield to an equivalent product yield with Poisson statistics gives

$$Y_p = Y_m^{L_p/L_m}, \tag{19}$$

where L_p is the length of the pinhole-sensitive patterns in the product. Notice that in this case the scaling is done by a critical length ratio rather than the ratio of critical areas.

Similarly, the product yield

$$Y_p = [1 + (\sqrt[\alpha]{1/Y_m} - 1)L_p/L_m]^{-\alpha} \tag{20}$$

is the result when negative binomial statistics are used.

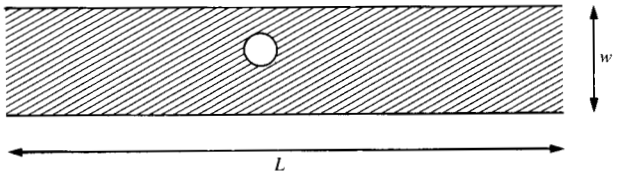

Figure 3 A small defect in a long conductor of length L and width w. If the defects are small enough, they will not cause an open circuit when this conductive line is tested.

4. Defect monitors sensitive to two failure modes

The best strategy is to design defect monitors that fail with one failure mechanism caused by one type of defect. However, this situation may not always be possible in practice. For example, a pinhole monitor might be made with a process that produces a high defect density along the edges of a pattern and a low defect density in the middle. Such a process can still be monitored. What we need in this case is two pinhole monitors, each with a different area to circumference ratio. Let us designate these as monitor 1 and monitor 2, with critical areas and peripheral lengths A_{m1}, A_{m2}, L_{m1}, and L_{m2}. If these monitors are produced side by side, they will be sensitive to the same random defect densities. The average number of faults per monitor should therefore be given by

$$\lambda_{m1} = A_{m1}D + L_{m1}D_L\,, \tag{21a}$$

$$\lambda_{m2} = A_{m2}D + L_{m2}D_L\,. \tag{21b}$$

As was done before, the average number of faults per monitor can be determined from the monitor yield with (8a) and (13).

If the yields of monitors 1 and 2 are given by Y_{m1} and Y_{m2}, then

$$\lambda_{m1} = -\ln Y_{m1}\,, \tag{22a}$$

$$\lambda_{m2} = -\ln Y_{m2}\,, \tag{22b}$$

according to Poisson statistics, and by

$$\lambda_{m1} = \alpha[\sqrt[\alpha]{1/Y_{m1}} - 1], \tag{23a}$$

$$\lambda_{m2} = \alpha[\sqrt[\alpha]{1/Y_{m2}} - 1] \tag{23b}$$

if negative binomial statistics are appropriate. These last expressions assume that the cluster parameter α is the same for both monitors. If this is not the case, the problem becomes more complex and falls outside the scope of this paper.

The defect densities can be determined by solving Eqs. (21a, b) for D and D_L to give

$$D = (L_{m2}\lambda_{m1} - L_{m1}\lambda_{m2})/(A_{m1}L_{m2} - A_{m2}L_{m1}), \tag{24a}$$

$$D_L = (A_{m1}\lambda_{m2} - A_{m2}\lambda_{m1})/(A_{m1}L_{m2} - A_{m2}L_{m1}). \tag{24b}$$

It is clear from these results that solutions exist only if

$$\frac{A_{m1}}{A_{m2}} \neq \frac{L_{m1}}{L_{m2}}\,. \tag{25}$$

The sensitivity of the monitors is greater for a larger difference between the area and length ratios of the monitors.

An area and length model, like the model for pinholes, has also been applied to junction leakage defects. Such defects cause semiconductor junctions to "leak" an excessive amount of "leakage" current when the junction is reverse-biased. Defect monitors capable of evaluating the contributions of leakage current from both area and line defects are used at IBM to evaluate the dielectric integrity and junction qualities of new semiconductor manufacturing processes.

5. Photolithographic defects

Patterns of polysilicon, metal, dielectric insulators, and diffusions in silicon wafer surfaces are used to make and interconnect the transistors, diodes, resistors, and capacitors in integrated circuit chips. Minimum pattern dimensions of a few micrometers are typical for the integrated circuits manufactured today. Dust and dirt particles with similar dimensions, or larger, are the major cause of defects in integrated circuit production. Such particles interfere with the photolithographic processes used to define the patterns. Whether a particle causes a failure depends on its location on a chip or on the photographic mask used in the process. The size of the resulting defect also determines whether the chip will fail. In many cases small defects do not cause chip failures at all.

A theory for mathematically modeling the size dependency of defects was originally developed by R. H. Dennard and P. Cook at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York, in the late 1960s. This theory has subsequently been adapted by Maeder et al. in a yield model used for manufacturing control [11]. Other yield models that make use of this approach have since been applied for yield projection and line control at a number of IBM manufacturing locations [12]. However, until now only a cursory description of the defect size model has been given in the literature [3, 13]. It is the purpose of the next sections to describe the model and derive it from fundamental principles.

6. Critical areas of very long conductors

The effect of defect size on integrated circuit patterns is best approached by first considering a very long straight conductive line. We assume that this conductor is deposited on an insulator and has a length L which is much greater than its width w. This conductive line has to allow an electric current to flow from one end to the other. The failures in this case are

open circuits caused by holes in the conductive material. These holes are referred to as missing photolithographic patterns.

It must be pointed out here that there is a class of open circuits that is caused by minute cracks in the conductive material. This usually occurs where the conductor passes over steps from the edges of the patterns underneath. Such defects can be modeled by counting the number of critical steps in a design. This propensity of steps to cause discontinuities can be measured with defect monitors. These defects are not included in the analysis which follows.

When photolithographic defects are very small, there can be enough conductive material left to allow the line to conduct currents without failure. Such a condition is depicted in Fig. 3. We define the defect size as a maximum defect dimension perpendicular to the line edges.

The width of the defect in the longitudinal or horizontal dimension does not matter. In actual cases it is usually of the same magnitude as the transverse dimension. It has therefore proven convenient to model the defects as circles, as is done in the rest of this paper. The diameter of each circular defect is designated with the Greek letter χ.

The object of our model is to find the mathematical relationship between the critical area and the defect size. We have already seen that for small enough defects the conductor will not fail. We now must consider the maximum amount of conductive material that can be left by a defect and have it still cause a failure. If more than this amount is left, the line will not fail. When less than this amount remains, the line will always fail.

The amount of the conductor that has to be left by a defect in order not to cause a failure during final test depends on the electrical current that flows through the line when it is tested. In this paper we focus attention on models for final test or functional yield of chips. Reliability failures caused by the phenomenon of aluminum migration can be modeled with a similar model but are not treated in this paper. We assume that, during normal operation and final test, the conductor carries enough current to make it "blow" when only a width d of material is left. If the width is greater than d, we assume that the line is not affected, while any amount of material of width d or less always causes a failure.

Thus defects of size $\chi < (w - d)$ leave enough conductive material to keep the conductor operational, and defects of size $\chi \geq (w - d)$ cause the line to fail if they occur in the right location. These conditions are known as the failure criteria. The locus of the center of defects that lead to failure is known as the critical area. The critical area is therefore

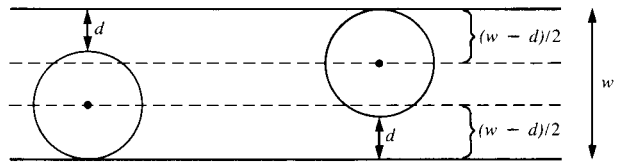

Figure 4 Determination of the critical area for minimum defect size that will cause a conductor to fail.

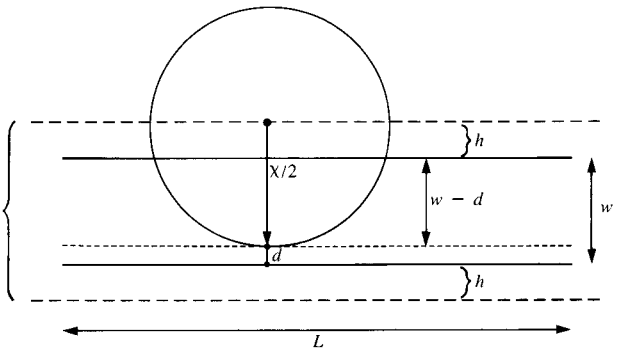

Figure 5 Diagram pertinent to calculating the critical area of a conductive line with length L and width w. An open circuit results when less than an amount d of conductor is left.

defined as *the area in which the center of a defect must fall to cause a failure or a fault.*

Let us first determine the critical area for a defect of size $\chi = (w - d)$. This area is indicated by the dashed lines in Fig. 4. If the center of the defect falls above the upper dashed line, no failure will occur. Similarly, if the defect is centered below the lower dashed line, there will be no fault. In both these cases more than a width d of conductive material is left. With the drawing in Fig. 4 we can determine the distance between either edge of the conductor and its nearest dashed line. This distance is equal to the radius of the defect, which is $(w - d)/2$. The space between the two dashed lines of Fig. 4 is therefore equal to d, the same distance as for the failure criteria. We obtain the critical area by multiplying the line length by the distance to get an area Ld. This is an interesting result. For defects smaller than size $(w - d)$ the critical area was zero. Then all of a sudden at defect size $(w - d)$ we find a critical area equal to Ld. The critical area is therefore discontinuous. This is a direct consequence of the minimum allowable line width assumption used in the derivation of this critical area.

Next we must determine the critical areas for defects that are larger than $(w - d)$. This critical area depends on the defect size. The diagram in Fig. 5 should be helpful in the

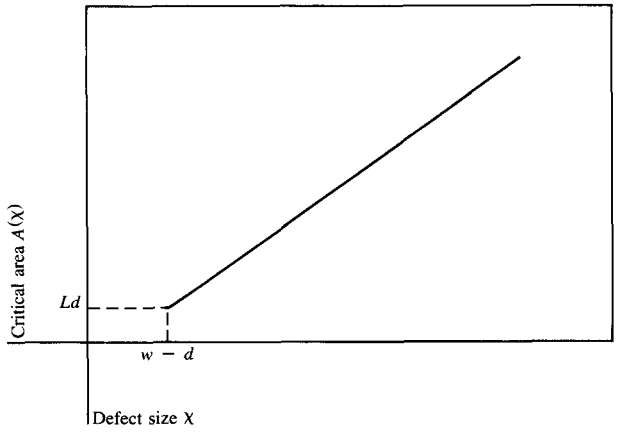

Figure 6 Critical area as a function of defect size for the conductor in Fig. 5. Failure occurs if $<d$ width of the conductor remains.

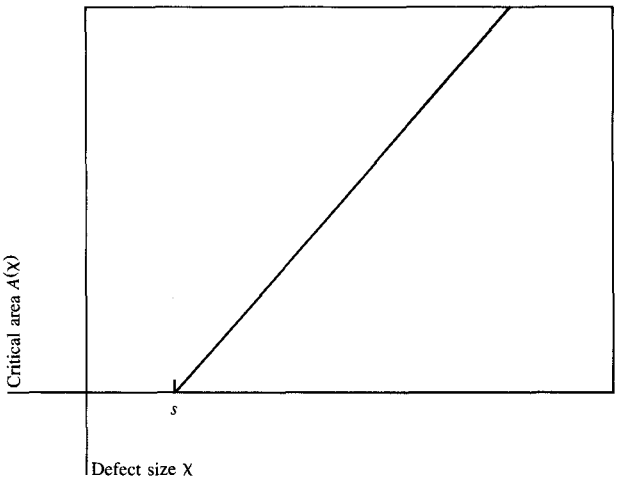

Figure 7 Critical area as a function of defect size for two very long conductors spaced a distance s apart.

analysis of this dependency. A defect shown in this diagram is positioned in the uppermost location where it will cause a fault during test. If it were located just a little higher, it would leave a strip of material that is wider than distance d. In that case no failure would occur during testing.

We can also see that less than a width d would be left if the center of the defect were located a little lower than shown. The dashed line in Fig. 5, therefore, is the upper boundary for the critical area. It is shown a distance h above the edge of the conductor. From the diagram we can deduce that the distance h must be equal to the defect radius minus the distance $(w - d)$, so that

$$h = \frac{\chi}{2} - (w - d). \tag{26}$$

A similar lower boundary for the critical area exists below the conductor. The situation is completely symmetrical, so that we have again a distance h from the conductor edge to this boundary. The critical area is equal to the distance between the two dashed lines times the line length L, or $(w + 2h)L$. By use of (26) we therefore obtain

$$A_c = (\chi + 2d - w)L, \tag{27}$$

which holds for defects of size χ larger than $(w - d)$ and is a function of the size of these defects.

The best way to describe the critical area mathematically is as follows:

$$A(\chi) = \begin{cases} 0 & \text{for } 0 \le \chi < w - d, \quad (28a) \\ (\chi + 2d - w)L & \text{for } w - d \le \chi < \infty. \quad (28b) \end{cases}$$

This discontinuous function is plotted in Fig. 6.

In the analysis of FET memory chip yields it has proven useful to simplify the preceding results. This is done by setting the minimum allowable conductor width d equal to zero. This critical area is then given by

$$A(\chi) = \begin{cases} 0 & \text{for } 0 \le \chi \le w, \quad (29a) \\ (\chi - w)L & \text{for } w \le \chi < \infty. \quad (29b) \end{cases}$$

This function is no longer discontinuous and line width w corresponds to the minimum defect size that will cause a failure. This assumption is used throughout the rest of this paper. The results obtained with this assumption can be readily extended by introducing the offset and minimum defect size requirements of (28).

It must be noted here that in both the preceding cases line length L was much larger than line width w. The case when L and w have comparable dimensions requires different failure criteria, which depend on the circuits in which such a pattern is used. The critical area usually becomes a quadratic function of the defect size. This, however, is beyond the scope of this paper.

The theory for short circuits is identical to the one for open circuits. In this case we can consider two very large conductors separated by a long straight gap with space s. Under the condition where the length of the gap $L >> s$ we obtain the critical area

$$A(\chi) = \begin{cases} 0 & \text{for } 0 \le \chi \le s, \quad (30a) \\ L(\chi - s) & \text{for } s \le \chi < \infty. \quad (30b) \end{cases}$$

In this case there is no equivalent to the distance d for open circuits, since the defect must always touch the two conduc-

tors to cause a short circuit. The resulting critical area as a function of defect size is shown in Fig. 7.

7. Defect size distributions

Finding the critical area of a conductor as a function of defect size is the first step towards a photolithographic yield model. To determine the average number of failures caused by these defects we must next consider the defect size distribution. A number of people at IBM have made studies to determine this distribution. The result from work done by G. F. Guhman at IBM Burlington is shown in Fig. 8. These data were compiled from optical microscope observations of memory chips. Mathematical functions were fitted to these results and given the general designation $D(\chi)$ for a defect size distribution. This distribution has the property that the average defect density $\overline{D}$ is given by

$$\overline{D} = \int_0^\infty D(\chi)d\chi. \tag{31}$$

It is also possible to relate the defect size distribution to a probability distribution function $h(\chi)$ by

$$D(\chi) = \overline{D}h(\chi). \tag{32}$$

The defect size distribution can be combined with the critical area as a function of defect size. To obtain the average number of faults or failures λ we must evaluate

$$\lambda = \int_0^\infty A(\chi)D(\chi)d\chi, \tag{33a}$$

$$= \overline{D}\int_0^\infty A(\chi)h(\chi)d\chi. \tag{33b}$$

The integral in (33b) gives the expected or average value of the critical area with respect to the defect size distribution. We can write this as

$$\overline{A} = \int_0^\infty A(\chi)h(\chi)d\chi. \tag{34}$$

It is therefore possible to reduce (33) to the simplicity of the pinhole defect model:

$$\lambda = \overline{A}\overline{D}. \tag{35}$$

It must be remembered, however, that this simplicity hides the defect size averaging that has been employed.

D. R. Thomas of IBM Burlington used test sites to determine whether the distribution given in (7) was appropriate for use in the photolithographic defect model. His structures consisted of very long narrow conductors with different widths and spacings. Thousands of these test sites were made in an experimental pilot line. The average number of failing lines was determined for each structure with a continuity test. The average defect density is the same for each monitor. Therefore, according to (35) the ratio between the average

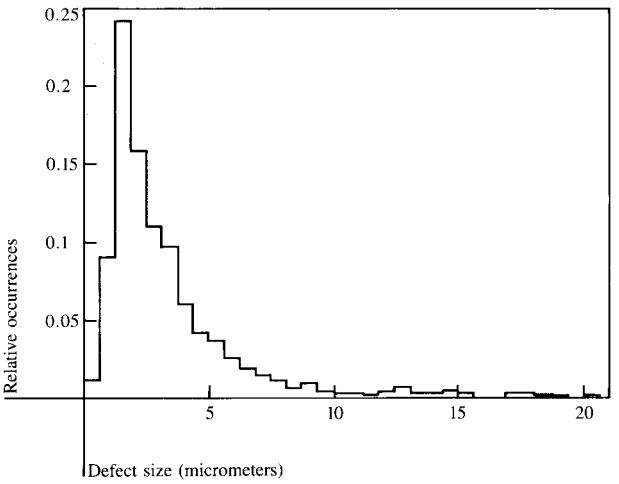

Figure 8 Defect size distribution obtained from counting defects with a microscope.

number of failures of different monitors has to be equal to the ratio of the critical areas of those monitors. Critical areas for Thomas' test sites were calculated by this author using (29), (30), and a mathematical approximation for the defect size distribution of Fig. 8. The results, however, were disappointing. There were far more failures in the narrower conductors than had been anticipated from the calculations. Two reasons for this were discovered. The counting of small defects is very difficult due to the optical limitations of the microscopes that were used. This resulted in inaccurate counts of the smaller defects. The other reason for the discrepancy between calculation and experiment is the difference that exists in the classification of defect sizes between experiment and theory. The experimenters determined their defect size as seen on the photolithographic patterns *after* etching, while the theory uses defect sizes that apply to patterns *before* they are etched.

During the late 1960s work with large photolithographic patterns at the IBM Thomas J. Watson Research Center had indicated that the defect densities decreased with increasing size as $1/\chi^3$. Thomas and Stapper decided to test a distribution that varied as $1/\chi^n$ for large defects. Very small defects were assumed to increase linearly with defect size to a point where the straight line crosses the $1/\chi^n$ curve. The result is shown in Fig. 9. Normalization of this distribution function gave them

$$h(\chi) = \frac{2(n-1)\chi}{(n+1)\chi_0^2} \quad \text{for } 0 \le \chi \le \chi_0, \tag{36a}$$

$$h(\chi) = \frac{2(n-1)\chi_0^{n-1}}{(n+1)\chi^n} \quad \text{for } \chi_0 \le \chi \le \infty. \tag{36b}$$

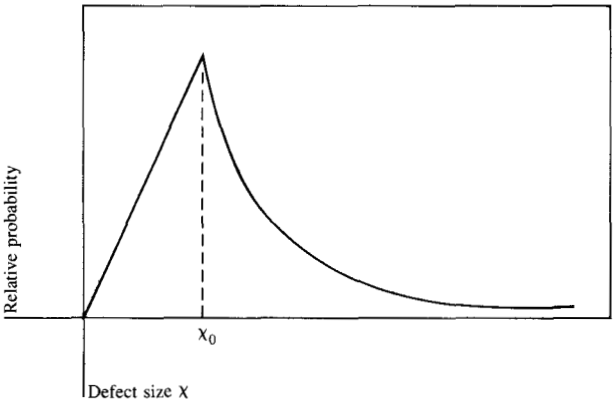

Figure 9 A hypothetical defect size distribution.

The peak of this distribution occurs at defect size x_0. Below this size it is assumed that the photolithographic process cannot resolve the defects well enough. The value of x_0, however, must be smaller than the minimum width or spacing of the defect monitors. This is because the minimum dimensions of the monitors have to be well within the resolving capability of the photolithographic process. Otherwise they cannot be printed. As a result, evaluation of integral (34) with the critical area given in (29) and the defect size probability distribution function (36) only involves (29b) and (36b). Consequently, the average number of faults or failures are found to be given by

$$\lambda = \frac{2Lx_0^{n-1}\overline{D}}{(n+1)(n-2)w^{n-2}}. \tag{37}$$

This expression has been compared with the test site data of Thomas. The results showed that $n = 3$ gave an excellent fit with the measurements made. This appeared to hold for defects causing open and short circuits on monitors consisting of polycrystalline-silicon and metal conductors, as well as diffusions. The observations at the IBM Research Center were therefore verified.

The preceding experiment has been repeated a number of times at various IBM locations. N. Haddad, when working at IBM East Fishkill, showed a long-term average of $n = 2.85$ for missing metal defects causing open circuits. A value of $n = 3.10$ was obtained for extra metal defects causing short circuits. Subsequent statistical tests were also performed on defect monitor data from one of the integrated circuit manufacturing lines at IBM Burlington by D. C. Sullivan. He found the $1/x^3$ size distribution to be a good hypothesis for defects occurring in diffusion and metal patterns. The hypothesis could not be rejected statistically as a model for the data from thousands of monitors.

Using the value ($n = 3$) in (36) gives

$$h(x) = x/x_0^2 \qquad \text{for } 0 \le x \le x_0, \tag{38a}$$

$$h(x) = x_0^2/x^3 \qquad \text{for } x_0 \le x \le \infty. \tag{38b}$$

The average critical area for the long conductive line with critical area (29) becomes

$$\overline{A} = Lx_0^2/2w. \tag{39}$$

Similarly, for the case of short circuits between two very long conductors we find

$$\overline{A} = Lx_0^2/2s. \tag{40}$$

There are no restrictions on chip or circuit sizes in these results. Critical areas can be affected if we limit our observations to the chip or circuit area itself. These considerations, however, fall outside the scope of this paper and are not discussed here.

8. Summary

In integrated circuit manufacturing large numbers of different defects cause yield losses. Each defect type has its own mechanism to cause a chip failure. In this paper defects have been categorized into two classes. Defects for which the defect size is not important are the easiest to model and are considered in the first class, e.g., defects that cause dielectric pinholes and junction leakage. The second class pertains to defects that are comparable in size to the photolithographic patterns. In this case the defect sensitivity depends on the defect size. We have shown a simple example of how this can be handled. All photolithographic defects fall into this category.

Defect monitors tie in very well with defect sensitivity models. Monitor data are used to measure the average number of failures and determine defect densities. For photolithographic defects the monitors have been used to find the defect size distribution and establish the capabilities and limits of photolithographic technologies.

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Charles H. Stapper *IBM General Technology Division, Burlington facility, Essex Junction, Vermont 05452.* Dr. Stapper received his B.S. and M.S. in electrical engineering from the Massachusetts Institute of Technology in 1959 and 1960. After completion of these studies, he joined IBM at the Poughkeepsie, New York, development laboratory, where he worked on magnetic recording and the application of tunnel diodes, magnetic thin films, electron beams, and lasers for digital memories. From 1965 to 1967, he studied at the University of Minnesota on an IBM fellowship. Upon receiving his Ph.D. in 1967, he joined the development laboratory in Essex Junction. His work there included magnetic thin-film array development, magnetic bubble testing and device theory, and bipolar and field effect transistor device theory. He is now a senior engineer in the development laboratory, where he works on mathematical models for yield and reliability management. Dr. Stapper is a member of the Institute of Electrical and Electronics Engineers and Sigma Xi.