Chapter 1

SYSTEM OVERVIEW

1.1 INTRODUCTION

The MAD-1(TM) Personal Workstation is a compact modular state-of-the-art machine that reflects the most advanced computer technology possible. The MAD-1 offers a powerful processing capability compatible with the IBM PC (TM).

The MAD-1, shown in Figure 1-1, runs the industry standard MS-DOS 2.0 and Concurrent CP/M 86 operating systems as well as a vast variety of application programs that are available in the market today. In addition, the MAD-1 can be networked using the field-proven EtherNet or PCNet Local Area Networks (LANs).

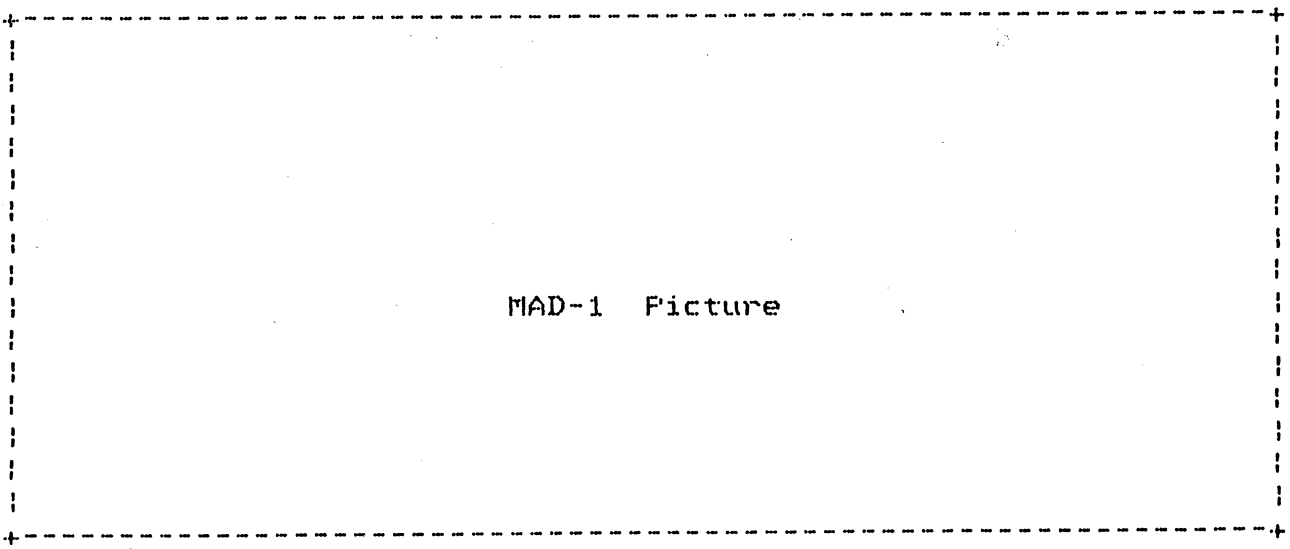


Figure 1-1: MAD-1 System

1.1.1 Standard Configuration

The MAD-1 is currently available in two basic models; one containing two floppy disk units and the other containing one floppy disk and one 10Mb hard disk. The standard configuration for each model is given in the following list:

MAD-1 : With Two Floppy Disks

- An Intel 80186 microprocessor
- 128K bytes of RAM and 16K bytes of EPROM
- Two RS-232C Serial Interface Ports
- One Parallel Interface Port
- One Video Controller with color and monochrome capabilities
- One monochrome Video Display (green or amber) and Keyboard
- Two 360K bytes Floppy Disk Drives
- DOS 2.0 Operating System

MAD-1 : With Hard Disk Option

- An Intel 80186 microprocessor
- 256K bytes of RAM and 16K bytes of EPROM
- Two RS-232C Serial Interface Ports
- One Parallel Interface Port
- One Video Controller with color and monochrome capabilities
- One Monochrome Video Display (green or amber) and Keyboard
- One 360K bytes Floppy Disk Drive
- One 10M bytes Hard Disk Drive
- DOS 2.0 Operating System

1.1.2 Optional Features

The MAD-1 system offers a variety of both hardware and software features that can be easily field-installed. The following list contains the optional features currently available:

HARDWARE

- Expansion Module (4 slots)
- 128K Memory Expansion Kit (Max. of 3)
- Ability to use 32K bytes EPROM (using 27128)
- 10 MB Hard Disk

SOFTWARE

- Operating Systems
  - MS-DOS 2.8
  - CCP/M 3.1
  - VENIX
- Languages
  - GW-Basic
  - Pascal
  - Cobol
  - C

Note: Addition of floppy and/or hard disks will require an Expansion Module.

1.2 SYSTEM COMPONENTS

The MAD-1 Personal Workstation is designed and implemented using advanced and proven technology and built around the concept of modular architecture.

High-speed TTL technology is utilized on multi-layered boards in the implementation of the logical components. The two inner layers of each printed circuit board are connected to the 5 VDC power supply and ground, which provides a contiguous power and voltage plane for the logical components on the board. The outer two layers of the printed circuit board provide discrete connections or bus lines between the various logic components on the board. External connections to other PC boards and assemblies are made via ribbon cables.

The logic portion of the system is partitioned into three separate modules, the computing module, the data module, and the expansion module. In addition, there is the video display and keyboard modules that are used for operator interface. Each module may be configured with additional optional features to give today's sophisticated users an exact and powerful configuration tailored to specific operation.

The overall block diagram of the MAD-1 showing the following five primary components is shown in Figure 1-2.

1. Computing Module
2. Data Module
3. Video Display Module
4. Keyboard Module
5. Expansion Module

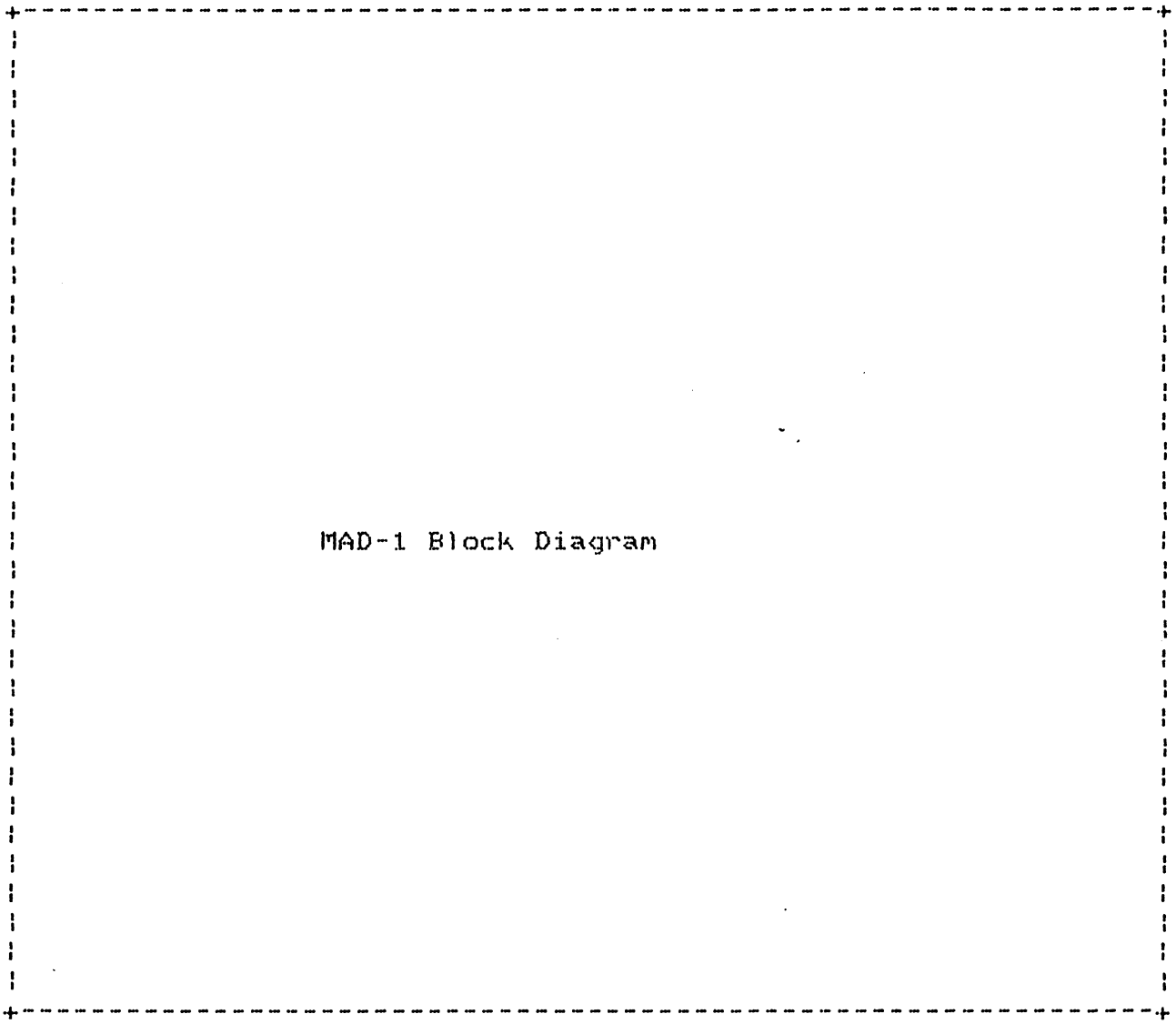


Figure 1-2: MAD-1 Block Diagram

1.2.1 Computing Module

The computing module is a 12.5" X 15.5" X 2.5" hard plastic enclosure containing up to three PC boards, eight external interface connectors, and two sets of internal jumper connections, as shown in the following list:

PC BOARDS:

- o CPU board
- o Video board
- o Expansion board (optional)

EXTERNAL CONNECTORS:

- o Two 37-pin connectors:
  - One for floppy disk connection
  - One for fixed hard disk connection (optional)
- o Three 25-pin connectors:
  - Two for serial communication
  - One for parallel printer interface.
- o One 10-pin connector for DC power in.
- o One 9-pin connector for video display signals.
- o One 6-pin modular telephone-style connector for the keyboard interface.

INTERNAL JUMPER SETS:

- o 22-jumper set for the CPU
- o 11-jumper set for the video board

Each of these items is further described in subsequent chapters of this manual.

1.2.1.1 CPU Board

The CPU board is a multi-layered 11"x14" printed circuit board containing all the processing, communication, timing logic, and all the neccessary interface for the system. It is mounted in the bottom of the computing module and contains the integrated floppy disk controller and a programmable peripheral interface. The physical locations of the components on the CPU board is shown in Figure 2-3.

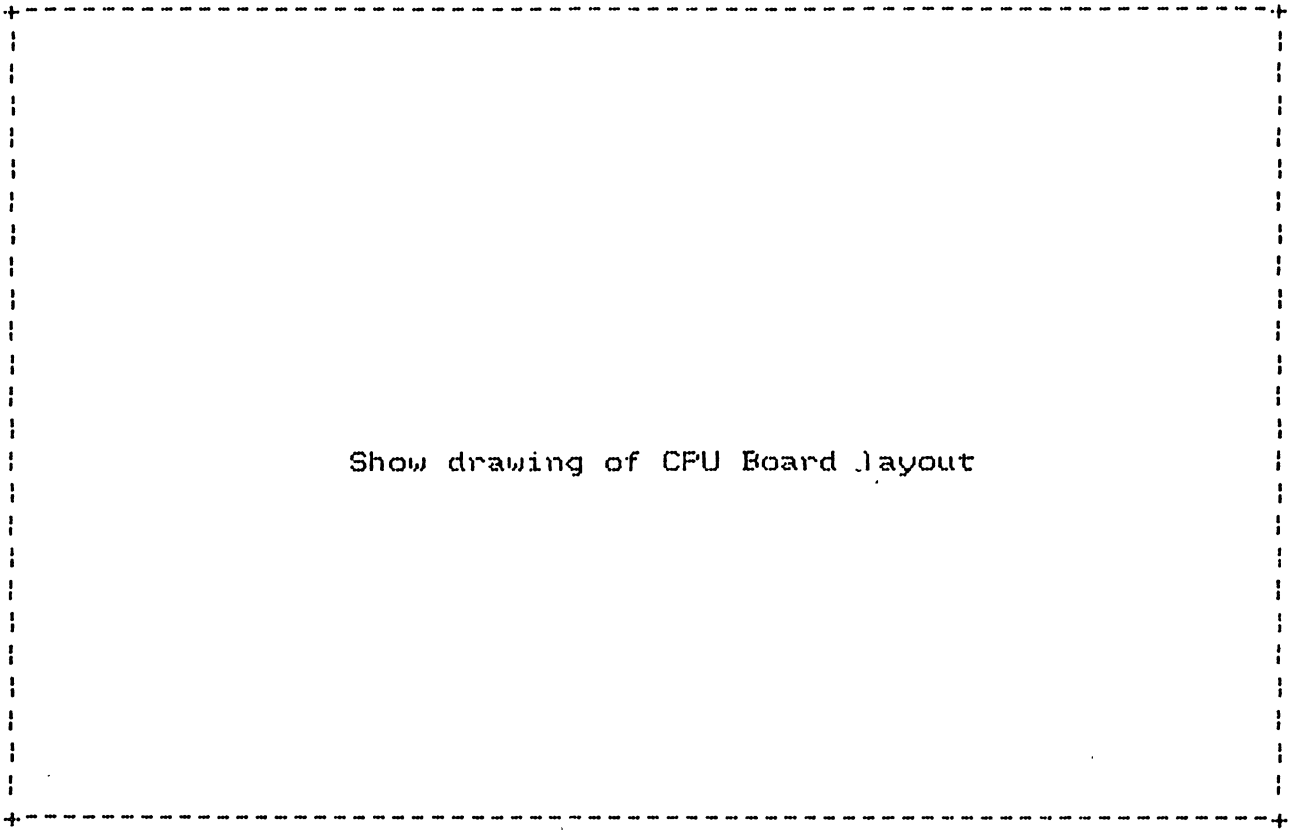


Figure 1-3: Physical Layout of CPU Board

The logical components contained on the CPU board, as shown in Figure 1-3, are given in the following list:

- o Intel 80186 operating in minimum mode.
  - Two internal DMA channels.
  - Three internal timer channels.
- o Four DMA channels (Intel 8237A-5).
- o Three timer channels (Intel 8254).
- o Eight interrupts (Intel 8259A-2).
- o Serial/Parallel communication interface
  - One serial tertiary channel USART (Intel 8274).
  - One serial primary channel UART (Intel 8250)
  - One serial secondary channel UART (Intel 8250)
  - One parallel printer interface
- o Memory control and memory
  - Up to 32K EPROM (using two 2764 or 27128 type EPROMs)
  - Up to 512K RAM
- o Programmable peripheral interface (Intel 8255)
- o Floppy disk controller (Intel 8272-A)
- o Clock/Calendar chip with battery back-up (58321)
- o I/O connectors
  - One 37-pin connector (floppy interface),
  - Three 25-pin connectors (two for serial port and one for parallel port)
- o Speaker circuitry
- o 8-Bit dip-switch for indicating disk, display type, and memory size.
- o Expansion slot for a third party peripheral card or for an additional 128K of memory (optional)

1.2.1.2 Video Control Board

The video board is a 14" X 5-3/4" four layer printed circuit board that is mounted component side down directly above the CPU board in the computing module. It is controlled by the Motorola 6845 CRT control chip and is capable of performing the functions of both the IBM monochrome display adapter and the color/graphic adapter (not including composite color video). Selection of either monochrome display or color/graphics is made via jumper assignments, described in Appendix C of this manual (one channel is operated at a time).

The video board itself, shown in Figure 1-4, contains the following connectors and logical circuitry:

- o 64-pin interface connector to the 16-bit expansion bus.
- o Special 16-pin connector providing the upper byte of the 16-bit data bus.
- o 9-pin D-shaped interface connector to the CRT display.
- o CRT control chip (Motorola 8645)
- o Monochrome and color video circuits

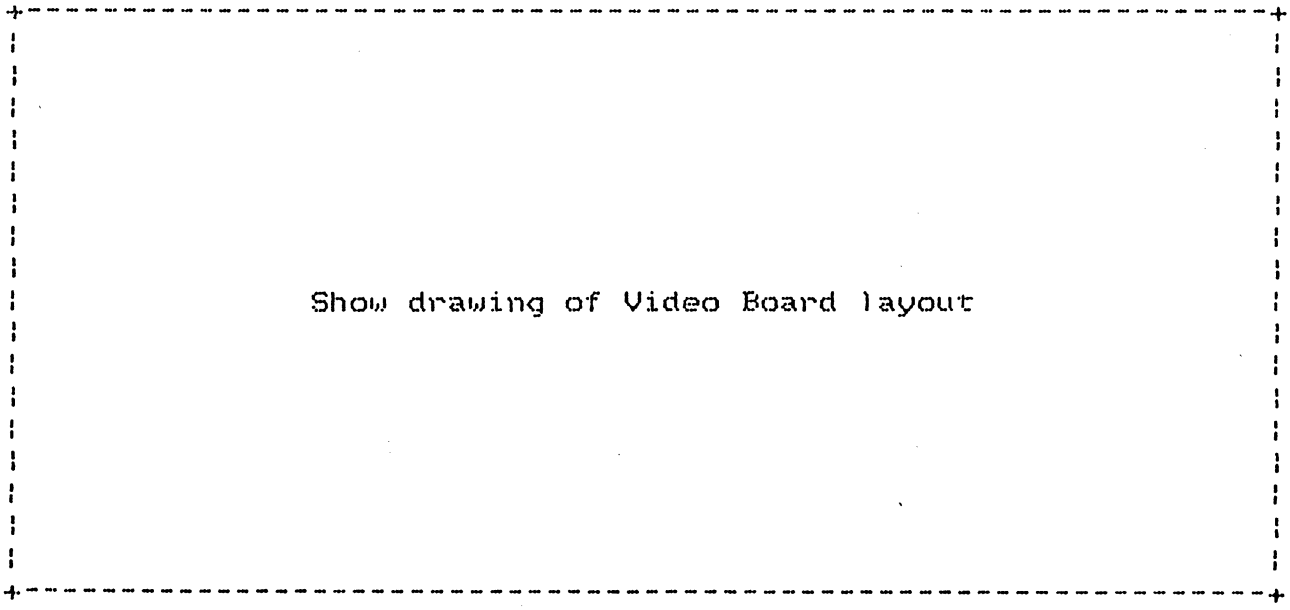


Figure 1-4: Physical Layout of Video Board

1.2.1.3 Memory Expansion Board

The memory expansion board is used to expand main memory from 512K bytes to 640K bytes. It is an optional four-layered printed circuit board that contains the necessary control logic and memory for an additional 128K bytes of Dynamic Random Access Memory (DRAM). The memory expansion board (when installed in the Computing Module) is mounted on a small bracket above the CPU board. Connection between this optional memory board and the CPU board is via one 62-connector and one 16-connector ribbon cable.

1.2.2 Data Module

The data module is identical in size (12.5" X 15.5" X 2.5") and shape to the computing module and contains the following list of components:

- o Up to two floppy disk drives, or one floppy disk and one optional Hard Disk Drive.
- o System's DC power supply.
- o External connector for connection to rest of the system.
  - Two 37-pin connectors; one for the floppy, and one for (optional) fixed hard disk.
  - One 10-Pin connector for DC power out.
- o RESET button
- o One 2-pin connector for video monitor DC power out.

1.2.3 Video Display Module

The video module consists of a standard lightweight 12" monochrome CRT, or an optional IBM compatible color CRT. This module operates in conjunction with the computing module which contains video control logic, and the data module that supplies all the necessary voltage.

1.2.4 Keyboard Module

The MAD-1 keyboard is designed to meet all European ergonomic and DIN standards. It utilizes the Intel 8048 microprocessor and a 64 byte input data buffer. The keyboard contains the standard alphanumeric typewriter keyboard and additional function keys for a total of 85 keys. These keys are arranged to provide optimum usage and reach.

The keyboard interface is located in the computing module with

the connection made via a 6-connector coiled cable.

1.2.5 Expansion Module

The expansion module is a 12.5" X 15.5" X 2.5" ~~optional~~ hard plastic optional enclosure which provides housing for an additional IBM compatible expansion board. This module is shown in Figure 1-5.

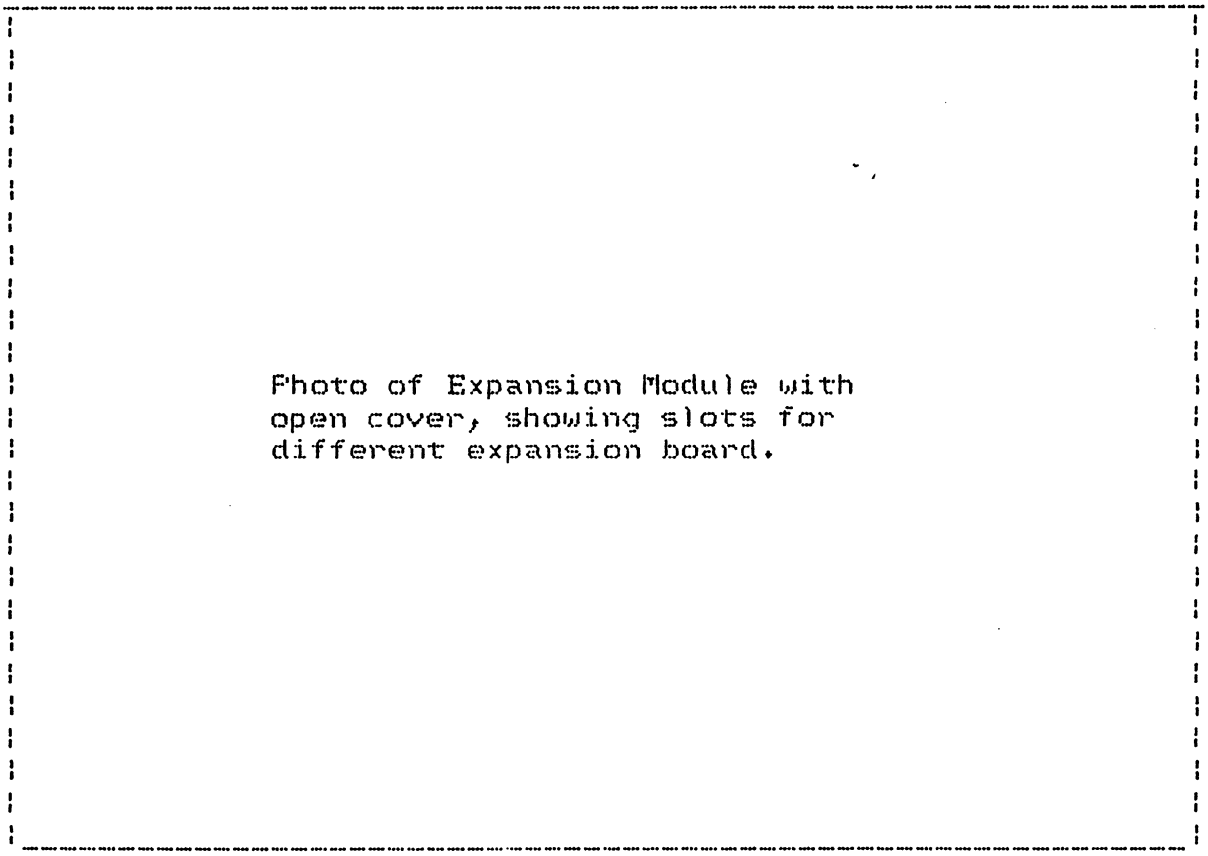


Figure 1-5: Expansion Module

1.2.6 Connectors And Cables

The number of connectors and cables is dependent on the configuration of the system. Figure 1-6 shows the various types of connectors and cables that may be used in the system:

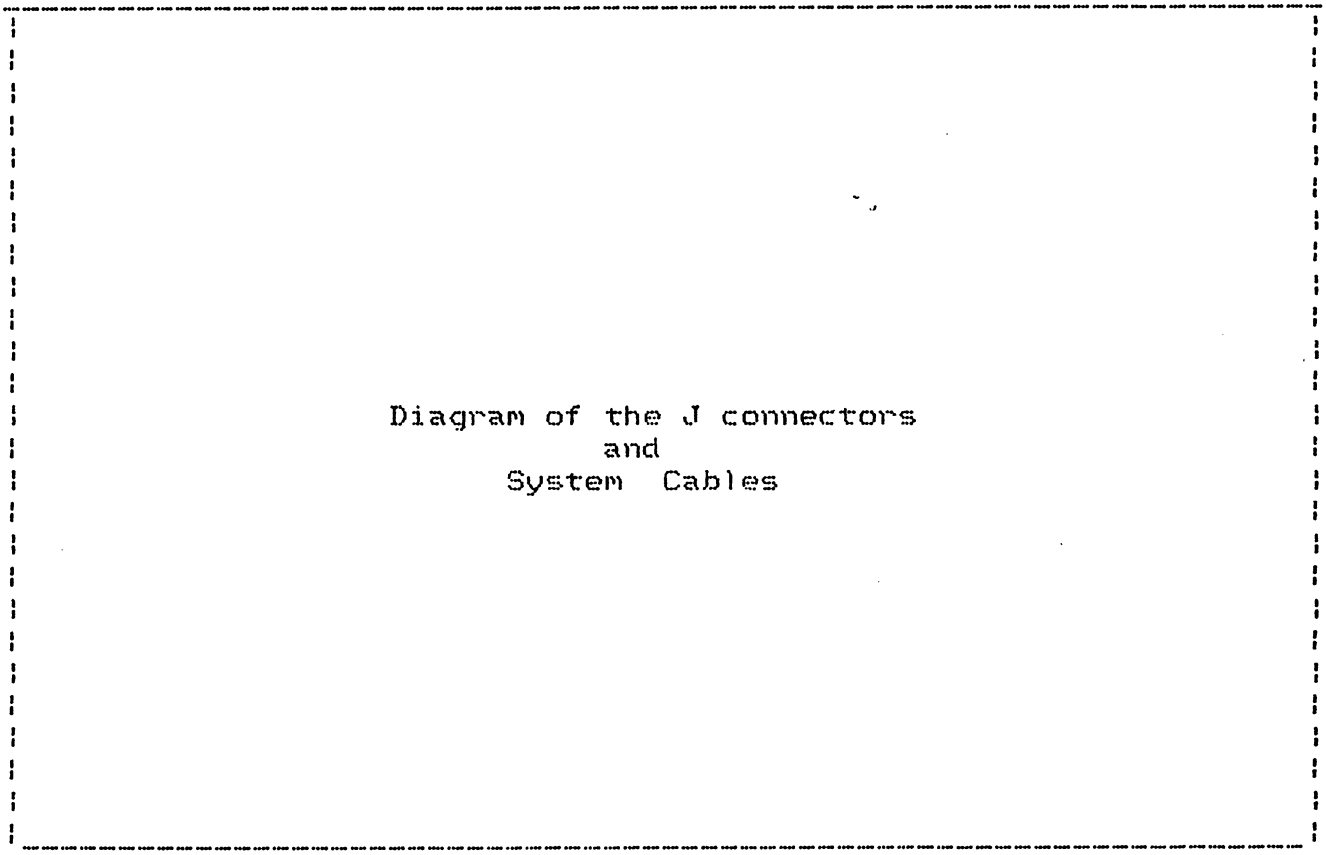


Figure 1-6: System Connectors and Cables

Chapter 2

CENTRAL PROCESSING UNIT

2.1 INTRODUCTION

This section contains a functional and operational description of the Central Processing Unit (CPU) in the MAD-1 ~~computer.~~ Personal Workstation

The MAD-1 CPU utilizes the Intel 80186 microprocessor chip operating in minimum mode. Its operation is such that it maintains complete compatibility with the Intel 8088 and 8086 processors even though it provides a much more extensive and faster instruction set. The 80186 has added many new instructions as well as optimizing several current instructions in order to improve the overall throughput of the processor.

The CPU will support up to one megabyte of dynamic RAM (DRAM) memory. However, to stay compatible with the IBM PC the MAD-1 CPU currently supports only 640K bytes of DRAM memory. The 640K bytes are distributed between the CPU board (512K bytes) and the expansion board (128K bytes). In addition to the dynamic RAM memory support, the CPU card contains 16K bytes of ROM (Read Only Memory).

The CPU interface, shown in Figure 2-1, contains the following logical components:

- Microprocessor, Intel 80186 chip
- Memory and Memory Control
- Direct Memory Access, Intel 8237A-5 chip
- Interrupt Controller, Intel 8259A-2
- Interval Timer, Intel 8254
- Programmable Peripheral Interface, Intel 8255 chip
- Serial Communication Interface, Intel 8274/8250 chips
- Parallel Printer Interface.
- Floppy Disk Controller, Intel 8272 chip

2.2.1 80186 Processor I/O Pin Description

Table 2-1: Processor Pin Descriptions

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
AD15-AD00	10-17 01-08	I/O I/O	Address/Data bus (0-15), time multiplexed memory or I/O address and data bus. The signals on this bus are active high.
ALE/QS0	61	O	Address Latch Enable/Queue Status 0 is an active high signal provided by the 80186 to latch the bus address bits in the address latches.
ARDY	55	I	Asynchronous Ready is an active high signal used to inform the 80186 that the addressed memory space, or I/O device, will complete the on-going data transfer.
A19/S6, A18/S5, A17/S4, A16/S3	65 66 67 68	O O O O	Address Bus Output (16-19) and Bus Cycle status (S3-S6) are high active signal that represent the four most significant bits of the address bus lines. S6 = 0, indicates Processor Cycle S6 = 1, indicates DMA Cycle
-BHE, S7	64	O	Bus High Enable is an active low signal that is used for strobing the eight most significant bits of the data (D15-8) onto the data bus. S7 is an active high signal that represents bit 7 of the status. -BHE A0 Function 0 0 Word Transfer 0 1 Byte Transfer bits D15-D08 1 0 Byte Transfer bits D07-D00 1 1 Reserved

(Continued)

Table 2-1 continued:

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
CLOCKOUT	56	O	Clock Out is an active high signal that provides the system with a 50% duty cycle clock.
-DEN	39	O	Data Enable is an active low signal used to enable the data bus transceivers.
DRQ0 DRQ1	18 19	I I	DMA Request 0/1 are active high signals raised by an external I/O device requesting a DMA transfer operation.
DT, -R	40	O	Data Transmit, Receive is used to control the direction of the data flow.
HOLD	50	I	Hold is an active high signal sent to the 80186 processor to indicate another bus master is requesting the use of the bus.
HLDA	51	O	Hold Acknowledge is an active high signal issued by the 80186 processor in response to the HOLD signal.
INT0 INT1 INT2 -INTA0 INT3 -INTA1	45 44 42 42 41 41	I I I O I O	Interrupt Requests 0-3 are active high signals. INT2 and INT3 may be configured via software to provide an active low Interrupt Acknowledge signal on each of corresponding pins. All interrupt request lines must remain active until acknowledged.
-LCS	34	O	Lower Memory Chip Select is an active low signal issued whenever a memory reference is made to a defined portion of memory (1K-256K).
-LOCK	48	O	LOCK is an active low signal issued by the processor to prevent bus access by other bus masters.
-MCS0 -MCS1 -MCS2 -MCS3	38 37 36 35	O O O O	Mid Range Chip Selects 0-3 are active low signals issued when a memory reference is made to a defined midrange portion of the memory (8K-512K). Signals are software programmable.

(Continued)

Table 2-1 continued:

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
NMI	46	I	Non-Maskable Interrupt is an active high signal that triggers the NMI interrupt when a memory parity error or channel error occurs.
-PCS0,-PCS1 -PCS2,-PCS3 -PCS4	25,27 28,29 30	O O O	Peripheral Chip Selects 0-4 are active low signals issued when a reference is made to a defined peripheral area (64K I/O space)
-PCS5, A1	31	O O O O	Peripheral Chip Select 5 is an active low signal that may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal.
-PCS6, A2	32	O O O O	Peripheral Chip Select 6 is an active low signal that may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A1 signal.
-RES	24	I	Reset is an active low signal that is issued by the operator. This signal, when active, causes the 80186 processor to terminate all ongoing activities.
RESET	57	O	RESET is an active high signal issued by the 80186 to indicate it is being reset. RESET may be used to reset the system.
SRDY	49	I	Synchronous Ready is an active high signal that must be synchronized externally to the 80186.
S0-3	52-54	O	S0-3 are active high signals that provide bus cycle status, as encoded below: S0 S1 S2 — BUS CYCLE INITIATED 0 0 0 — Interrupt Acknowledged 0 0 1 — Read I/O 0 1 0 — Write I/O 0 1 1 — Halt 1 0 0 — Instruction Fetch 1 0 1 — Read Data from memory 1 1 0 — Write Data to memory 1 1 1 — Bus inactive

(Continued)

Table 2-1 continued:

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
-TEST	47	I	TEST is an active low signal examined by the WAIT instruction. If TEST is active, it will cause the execution of the WAIT instruction to be suspended. The WAIT instruction will re-examine TEST, and if not active, it will resume execution. Otherwise WAIT will continue to examine the TEST signal.
TMR IN 0 TMR IN 1	20 21	I I	Timer Input 0 and Timer Input 1 are active high signals that are used as either a clock or control signal, depending on the programmed timer mode.
TMR OUT 0 TMR OUT 1	22 23	O O	Timer Output 0 and Timer Output 1 are active high signals that provide single pulse or continous waveform, depending on programmed timer mode.
-UCS	34	O	Upper Memory Chip Select is an active low signal that is issued whenever a memory reference is made to the defined portion of the memory (256K-512K).
VCC	9,43	I	System Power, provides +5 Vdc to the internal logics of the 80186 processor.
VSS	26,60	I	System Ground
-WR, QS1	63	O	Write Strobe is an active low signal that is used to strobe data on the bus into memory or an I/O device. QS1 is an active high signal that represents Queue Status 1
X1 X2	59 58	I I	Crystal Inputs X1, and X2 are active high signals that provides an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. The X1 input may be connected to the output of an external clock instead of a crystal.

2.2.2 80186 Internal Register Map

The Intel 80186 microprocessor provides 14 internal registers as described below:

X'FE'	RELOCATION REGISTER
X'DA'-X'D0'	DMA DESCRIPTION CHANNEL 1
X'CA'-X'C0'	DMA DESCRIPTION CHANNEL 0
X'A0'-X'A8'	CHIP SELECT CONTROL REGISTER
X'66'-X60'	TIMER 2 CONTROL REGISTER
X'5E'-X58'	TIMER 1 CONTROL REGISTER
X'56'-X50'	TIMER 0 CONTROL REGISTER
X'3E'-X'20'	INTERRUPT CONTROL REGISTER

Figure 2-3: 80186 Internal Register Map

2.3 MEMORY SUBSYSTEMS

Basically, there are three types of memory elements used in the design of the MAD-1 Workstation. They are:

1) **Dynamic Random Access Memory (DRAM)**
High-speed volatile read/write memory for implementing the main memory used by processor and I/O operations. DRAM requires a periodic refresh cycle to retain its contents.

2) **Static Random Access Memory (RAM)**
RAM is a high-speed volatile read/write memory used for buffering display and keyboard data.

3) **Programmable Read Only Memory (PROM)**
PROM is a non-volatile type of memory used for storing system control and system operational instructions that are coded specifically for the MAD-1.

Figure 2-4 shows the physical location of each memory type on the CPU and video board. A more indepth discussion of each one follows the figure.

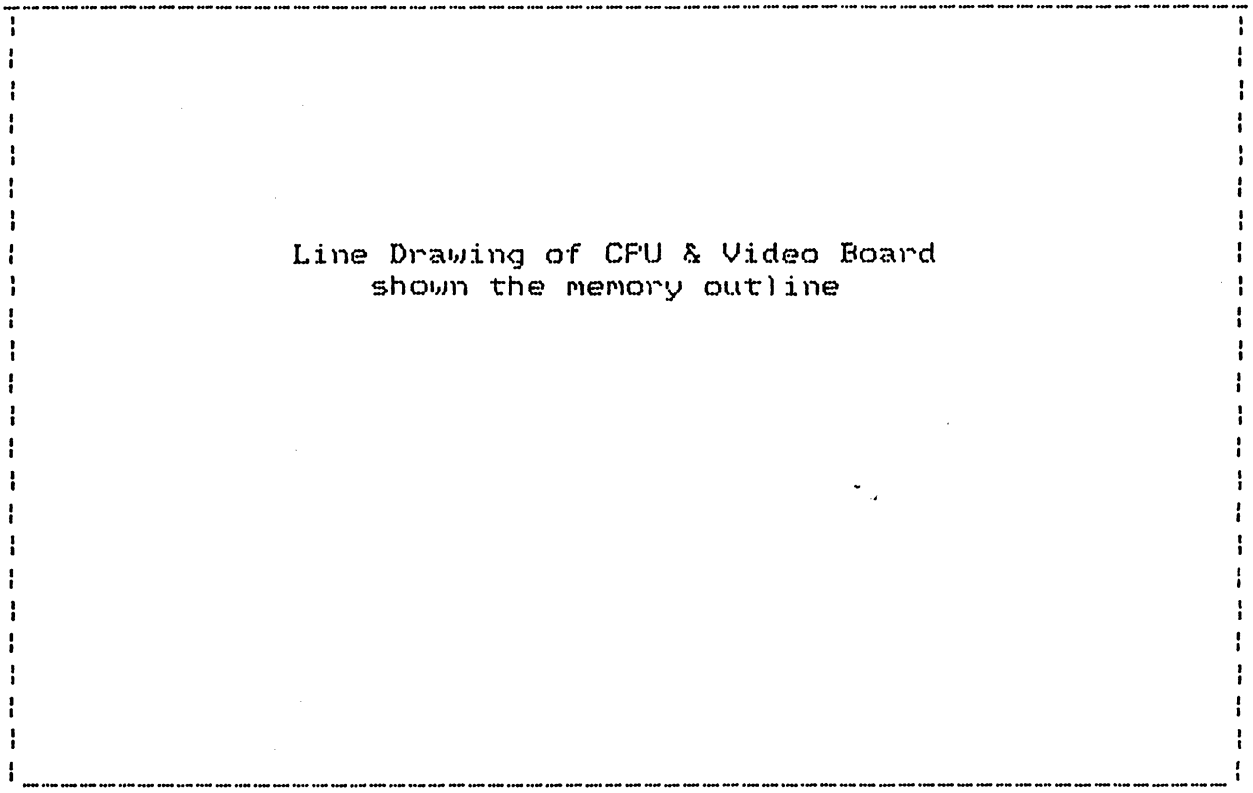


Figure 2-4: CPU/Video Memory Locations

2.3.1 Main Memory

Main memory in the MAD-1 is viewed as a contiguous string of 9-bit bytes (8 data bits plus one parity bit) beginning at memory address x'00'. It utilizes 64K DRAM chips to support a maximum of 640K bytes in increments of 128K bytes. The first 512K bytes of DRAM reside on the CPU board in the computing module and begin with address x'00' through x'7FFFF'. The remaining 128K bytes are located on the memory expansion card, mounted above the CPU card in the computing module, and contain memory addresses x'80000' through x'9FFFF'. An address map of main memory is shown in Figure 2-5. The connection between the memory expansion card and the CPU board is through a 62-pin and a 16-pin I/O extension cable. The DRAM chips in main memory are arranged to provide a 16-bit read-out for a 16-bit CPU transfer operations.

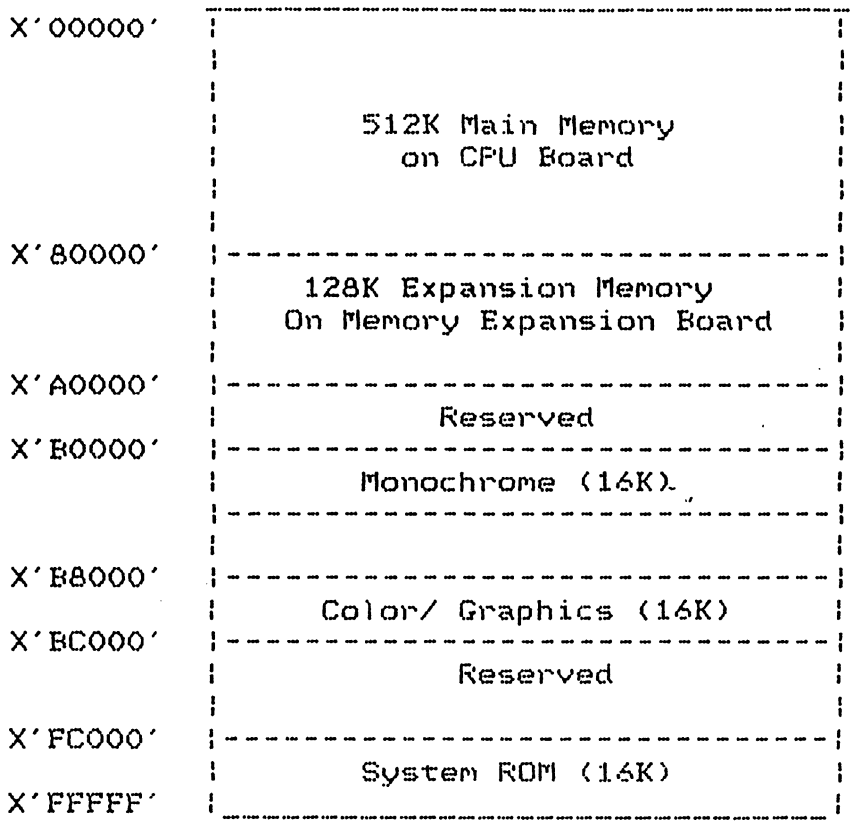


Figure 2-5: Memory Address Map

2.3.1.1 Main Memory Cycle Time

The dynamic RAMs (DRAMs) used in main memory have an access time of 150 nsec. The processor requires four CPU cycles (167 nsec per cycle) to access data from main memory, and a minimum of five CPU cycles for I/O operations. When I/O access occurs, one wait state is automatically inserted and the READY signal is sampled. If the READY signal is false, another wait state may be added. The memory timing diagram is shown in Figure 2-6:

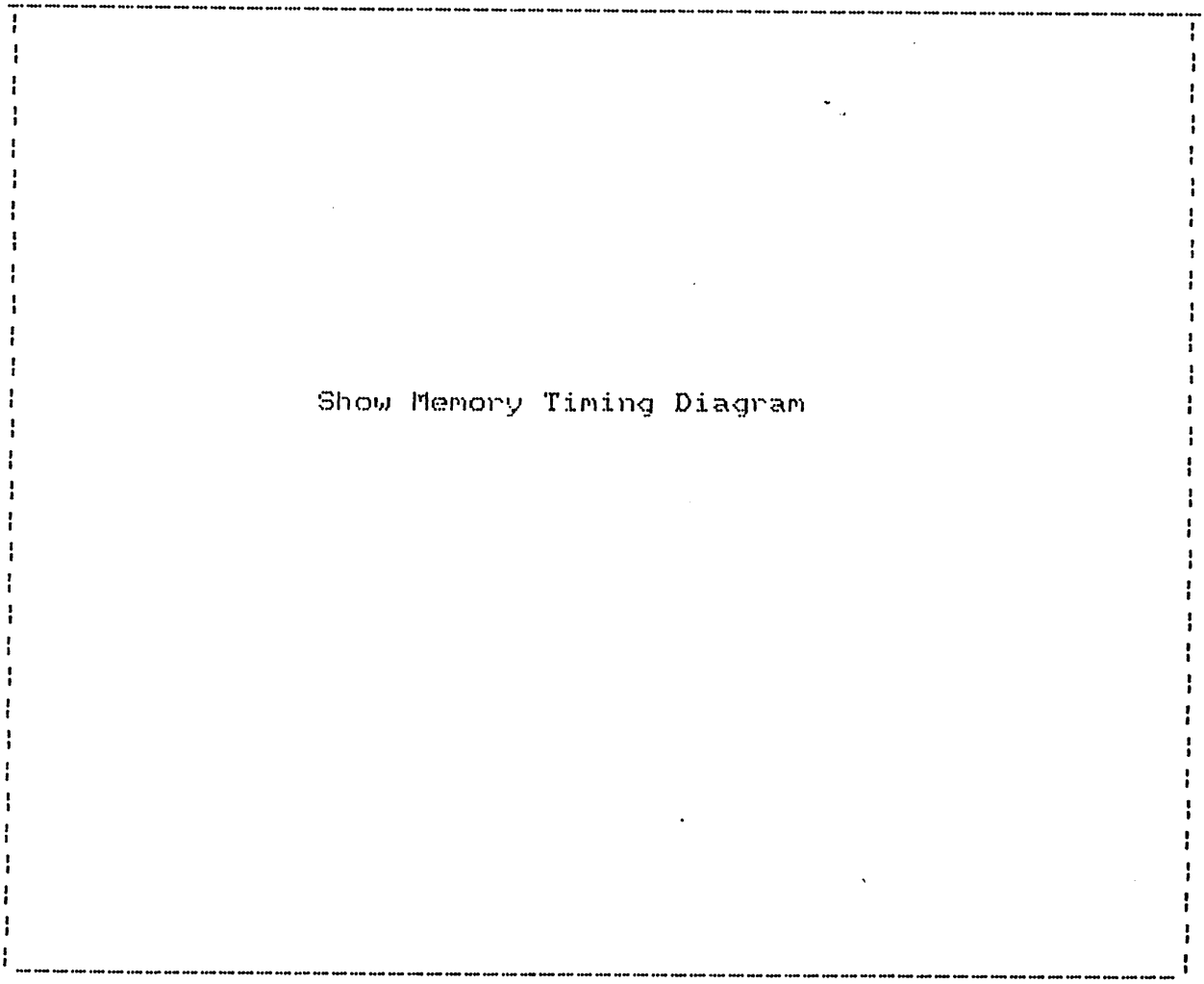


Figure 2-6: Memory Timing Diagram

2.3.1.2 Parity Bit

MAD-1 memory provides one parity bit with each byte of information written or read from main memory, as shown in Figure 2-7. All parity bits are transparent to the user and the programs; they are written during write operations and are checked during read operations. If a parity check occurs, the operation is halted by a level '0' interrupt, referred to as a Non-Maskable Interrupt (NMI). This type of interrupt has the highest priority in the system. For more information on interrupts, see section 2.6, Interrupt Control, in this chapter.

awkward sentence

NOTE: Parity bits may be enabled by jumpering W-09 on the CPU board (see Appendix C for all jumper locations).

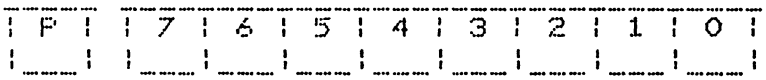


Figure 2-7: Memory Byte with Parity

2.3.1.3 Main Memory Refresh

The dynamic RAMs used by main memory require a periodic refresh (every 2 milliseconds) to sustain the recorded data in the memory cells. The refresh operation is performed by DMA Channel 0 issuing periodic read requests to main memory. The DACK 0 signal is used to enable RAS on all memory chips and inhibit CAS.

2.3.2 Video Display Buffer Memory

The MAD-1 Personal Workstation utilizes static RAM memory, located on the video display board (see Figure 2-4), for its 16K byte video display buffer (8-bit bytes with no parity). This memory space is used to buffer the display information and its attributes. For more information, see Chapter 3 in this manual.

2.3.3 Programmable Read Only Memory (PROM)

Unlike main memory, PROMs are static and do not require a refresh operation. This type memory consists of either a pair of 2764 chips for 16K bytes, or 27128 chips for 32K bytes. The current PROM memory address assignment for 16K bytes begins at location X'FC000' and at X'F8000' for 32K bytes.

The access time of PROM memory is 350 nanoseconds. The processor accesses PROM information the same as main memory information. However, for above memory address x'FBFFF', two wait states are inserted.

time?
way?

2.4 INPUT/OUTPUT (I/O) CHANNEL

The I/O channel is a de-multiplexed buffered extention of the 80186 microprocessor bus with added interrupts, DMA channels, power, and control signals. The I/O channel itself is an 86-pin connector consisting of:

- 20-bit Address Bus
- 16-bit Bi-directional Data Bus
- Six levels of Interrupts
- Three DMA Channels
- Power and Ground for Adapters.
- Control Lines for Memory and I/O Read/Write, Clock, and Timing.
- Four voltage lines, +/-5Vdc and +/-12Vdc, for expansion cards.
- READY Line for operation of slow I/O or Memory Devices

Each I/O operation requires a minimum of five CPU cycles. This includes one automatically inserted wait cycle that is used for sampling the READY line. If the READY signal is not activated during the sample, another wait state (1 cycle at 167 nsec.) is added to allow it to become activated. The READY line will be resampled during the added wait cycle. If the ready line is not activated after two wait states, the watchdog timer will timeout, thus preventing the system from permanently being hung.

I/O devices that are configured to the MAD-1 are addressed via the I/O mapped address spaces.

Parity errors from the memory expansion cards are reported by the channel check line, which is connected to the NMI input of the 80186 processor.

The I/O channel diagram and pin assignments with signal descriptions are shown in Figure 2-9 and Table 2-2.

2.4.1 I/O Channel Diagram

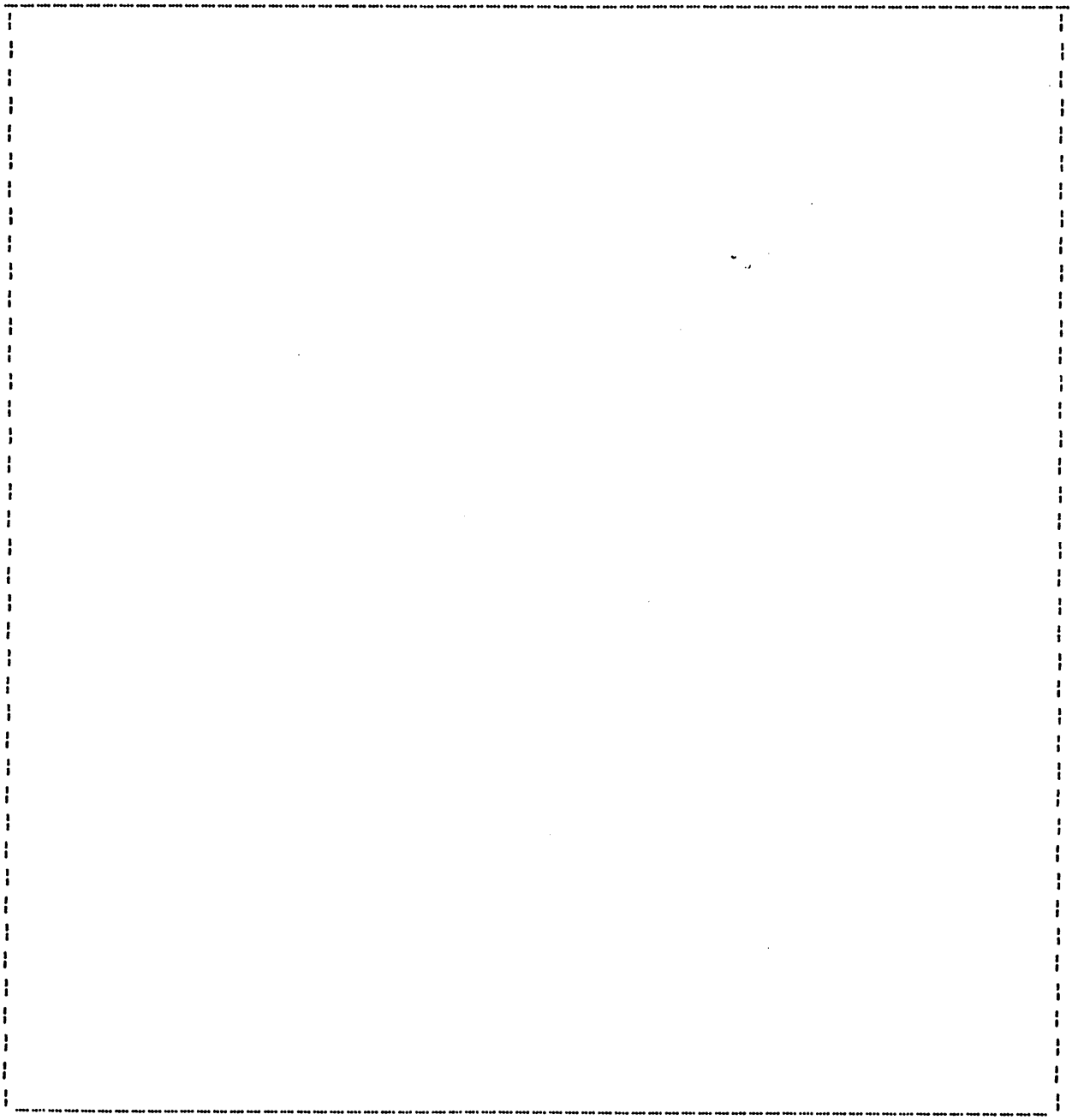


Figure 2-8: I/O Channel Diagram

2.4.2 I/O Expansion Bus

The expansion bus refers to that portion of the I/O channel bus that is extended beyond the IBM I/O Channel Bus. As shown in the I/O Channel Diagram (Figure 2-8), the expansion bus contains 22 lines consisting of the following:

- Eight Data lines for Data Bits D08 thru D15
- Two Lines for Light Pen signals
- Four reserved lines
- Eight lines for Power and Ground signals

No Lightpen!

2.4.3 I/O Channel Signal Description

The MAD-1 I/O Channel is an 86-pin connector numbered A01 through A42 and B01 through B42. The first 31 lines on both sides of the connector are fully compatible with the IBM PC I/O channel bus. Table 2-2 lists all the pin assignments and their functions by pin number:

Table 2-2: I/O Channel Signals

PIN #	SIGNAL	DIR.	DESCRIPTION
A01	-I/O CH CK	O	Channel Check: Active low signal that indicates parity error in memory or devices in the I/O channel.
A02 Thru A09	+D7 - +D0	I/O	DATA BITS 7 - 0: Active high signals. Low eight bits of the 16-bit data bus used to transfer data between the 80186 processor, memory, and I/O.
A10	+I/O CH RDY	I	I/O Channel Ready: Active high signal indicating readiness of the bus. It is pulled low to increase the memory cycle for slow devices attached to the I/O channel to operate properly. Slow device should drive this signal low immediately upon detecting valid address and a read or write command. This line should never be held low longer than 10 clock cycles.

continued

Table 2-2 continued:

PIN #	SIGNAL	DIR.	DESCRIPTION
A11	+AEN	O	Address Enable: Active high signal used to de-gate processor or other attached device from the I/O channel to allow DMA transfer to take place. When +AEN is high the DMA controller has control of the address bus, data bus, read or write and command lines for both memory and I/O.
A12 Thru A31	+A19 - +A0	O	Address Bits 19 - 0: These 20-bit address lines are used by the processor or I/O to address main memory with up to 1M byte of direct memory access.
A32	J9-3	I	Used for the optional Light Pen.
A33	RESERVED		Reserved for future use.
A34	RESERVED		Reserved for future use.
A35 Thru A42	+D8 - +D15	I/O	DATA BITS 8 - 15: Active high signals. High order eight bits of the 16-bit data bus used to transfer data between the 80186 processor, memory, and I/O.
B01	GND		Ground
B02	+RESET DRV	O	Reset Drive: Active high signal used to reset or initialize system hardware logic during power-up. This synchronizes the operation with the falling edge of the system clock.
B03	+5 VDC		+5 Vdc
B04	+IRQ2	I	Interrupt Request Line 2: An active high signal used by an attached device to request attention from the processor. The MAD-1 carries IRQ2, IRQ3, and IRQ5 on the bus for use by the expansion card. IRQ0, IRQ1, IRQ4, IRQ6, and IRQ7 are assigned to the system clock tick, keyboard, primary serial port, floppy disk controller, and printer or secondary serial port, respectively.

Table 2-2 continued:

PIN #	SIGNAL	DIR.	DESCRIPTION
B05	-5 VDC		-5 VDC.
B06	+DRQ2	O	DMA Request Line 2: Active high signal. One of the four asynchronous channel requests used by the peripheral devices to gain DMA access.
B07	-12 VDC		-12 VDC.
B08	-CARD SLCTD	I	Card Select : Active high signal driven by an open collector device and used to signal the CPU board that the expansion card has been selected. The appropriate drivers on the CPU board must read from, or write to expansion slot J8. Connectors J1-J8 are tied together at this pin, however, it is used only for J8.
B09	+12 VDC		+12 VDC.
B10	GND		Ground
B11	-MEMW	O	Memory Write Command: Active low signal driven by processor or I/O to instruct the memory to store data present on the data bus.
B12	-MEMR	O	Memory Read Command: Active low signal driven by the processor or the I/O to instruct memory to drive data onto the data bus.
B13	-IOW	O	I/O Write Command: Active low signal driven by processor or DMA instructing the selected I/O device to read the data present on the data bus.
B14	-IOR	O	I/O Read Command: Active low signal driven by the processor or the DMA, instructing the selected I/O device to write its data onto the data bus.

Table 2-2 continued:

PIN #	SIGNAL	DIR.	DESCRIPTION
B15	-DACK3	O	DMA Acknowledge line 3: Active low signal. -DACK3 is one of the four lines used to acknowledge DMA request.
B16	+DRQ3	O	DMA Request Line 3: Active high signal functioning as an asynchronous channel request used by peripheral devices to gain DMA access.
B17	-DACK1	O	DMA Acknowledge line 1: Active low signal. -DACK1 is one of the four lines used to acknowledge DMA request.
B18	+DRQ1	I	DMA Request Line 1: Active high signal. +DRQ1 is one of four asynchronous channel requests used by peripheral devices to gain DMA access.
B19	-DACK0	O	DMA Acknowledge line 0: Active low signal. This is one of the four lines used to acknowledge DMA requests. This signal is also used in memory refresh operations.
B20	CLOCK	O	System Clock: 'Divide-by-two' output of the 12 MHz oscillator (6MHz) with a period of 167 nsec and a duty cycle of 50%.
B21	RESERVED		Reserved for future use.
B22	RESERVED		Reserved for future use.
B23	+IRQ5	I	Interrupt Request Line 5: Active high signal. One of eight interrupt request lines used to signal the processor that an attached I/O device on the expansion bus requires attention. The MAD-1 carries IRQ2, IRQ3, and IRQ5 on the bus for use by the expansion bus. IRQ0, IRQ1, IRQ4, IRQ6, and IRQ7 are assigned to the system clock tick, keyboard, primary serial port, floppy disk controller, and printer or secondary serial port, respectively.

Table 2-2 continued:

PIN #	SIGNAL	DIR.	DESCRIPTION
B24	RESERVED		Reserved for future use.
B25	+IRQ3	I	Interrupt Request Line 3: Active high signal. One of eight interrupt request lines used to signal the processor that an attached I/O device on the expansion bus requires attention. The MAD-1 carries IRQ3 on the bus for use by an expansion card.
B26	-DACK2	O	DMA Acknowledge line 2: Active low signal. -DACK2 is one of the four lines used to acknowledge DMA request.
B27	+TC	O	Terminal Count: Active high signal used to indicate that the terminal count for any DMA channel is reached.
B28	+ALE	O	Address Latch Enable: Active high signal provided by the Intel 8288 bus controller chip to latch valid addresses from the Processor. For I/O channels, combinations of ALE and AEN indicate a "valid Processor Address".
B29	+5 VDC		+5 VDC supply voltage.
B30	+OSC	O	Oscillator: Active high clock signal with a 14.31818 MHz frequency and 50% duty cycle.
B31	GND		Ground
B32	J9-1		
B33	-LAHE	O	Latched Address High Enable
B34	RESERVED		Reserved for future use.
B34	RESERVED		Reserved for future use.
B36	+5 VDC		+5 VDC
B37	+5 VDC		+5 VDC
B38	+5 VDC		+5 VDC
B39	GND		Ground
B40	GND		Ground
B41	GND		Ground
B42	GND		Ground

2.5 DIRECT MEMORY ACCESS (DMA)

The DMA capability is provided on the MAD-1 to allow access by high-speed communication with peripherals attached to the system. DMA enhances system throughput by handling data transfers between main memory and the peripheral devices without intervention from the 80186 microprocessor.

This feature utilizes the Intel 8237A-5 DMA controller with four channels (CH0 - CH3) operating with 4.0 MHz clock, and these four channels are used for the following functions:

CH0	Memory refresh operation
CH1	Available on the I/O channel
CH2	Assigned to floppy disk controller
CH3	Available on the I/O channel (normally assigned to the hard disk)

In the normal operation of the 8237 controller, a 16-bit memory address is used. However, since the MAD-1 I/O operation uses a 20-bit address for memory operations, additional circuitry is provided for the extra four bits. This additional circuitry includes four DMA page registers used to handle the upper four bits of the 20-bit I/O address.

2.5.1 DMA Registers

The Intel 8237 DMA controller provides 16 registers, with addresses X'000' thru X'00F', that are used for programming the DMA operation. The following list explains the breakdown of these 16 registers:

- Eight 16-bit Read/Write registers (two register for each DMA channel) used for base and current addresses during read operation.
- One 8-bit Command Register.
- One 8-bit Status Register.
- One 8-bit Mark Set/Reset Register.
- One 8-bit Mode Register.
- One 8-bit Clear Byte Pointer Register.
- One 8-bit Temporary Register.
- One 8-bit Clear Mask Register.
- One 8-bit Write All Mask Register.

In addition to these 16 registers, the MAD-1 circuitry provides a

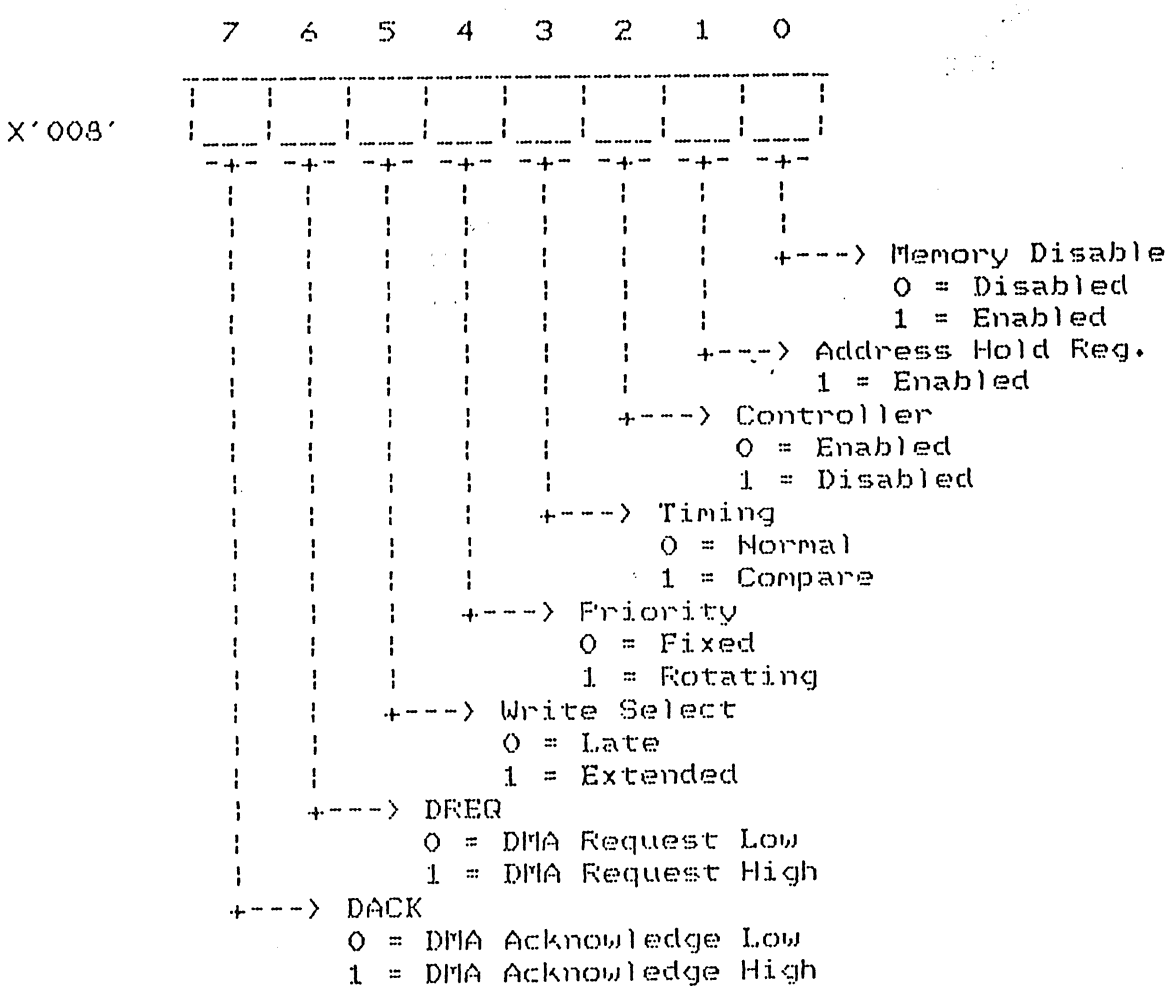
group of four 4-bit DMA page registers used to assist the 8237 controller with the 20-bit I/O address.

2.5.2 DMA Programming Considerations

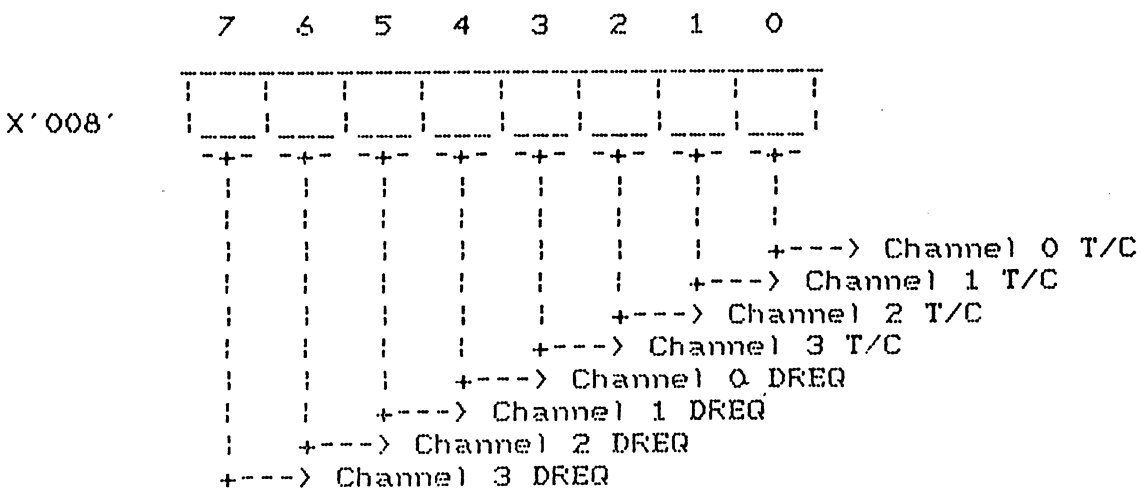
DMA Base & Current Address Registers: There are a total of eight 16-bit registers that are used to address the lower order 16 bits of the I/O memory address during a read operation. Two registers are assigned to each DMA channel and addressed as follows:

- X'000' and X'001' for DMA Channel 0 (CH0)
- X'002' and X'003' for DMA Channel 1 (CH1)
- X'004' and X'005' for DMA Channel 2 (CH2)
- X'006' and X'007' for DMA Channel 3 (CH3)

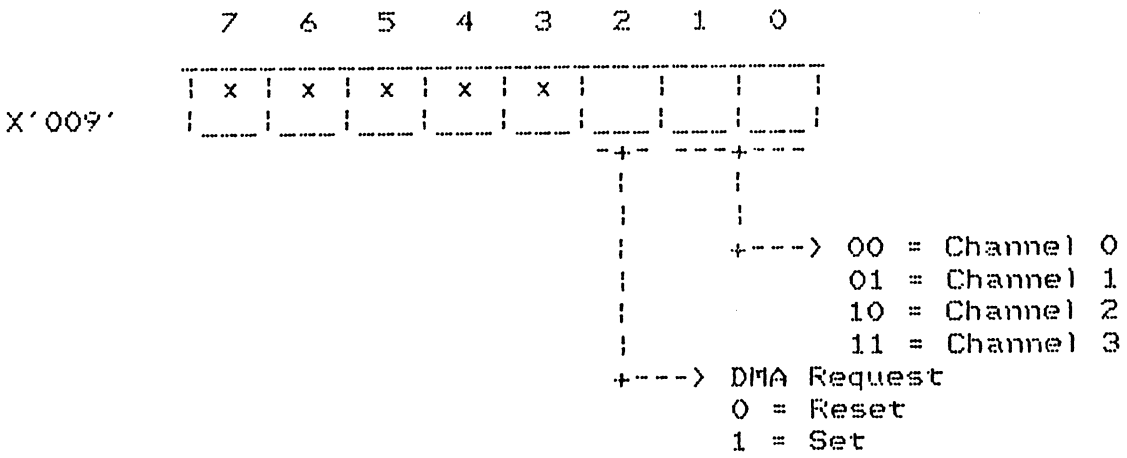
DMA Command Register: This 8-bit register is used as both a DMA command register and a DMA status register. As a command register, it is used by the programmer to write the command information into the register with I/O address X'008', as shown below:



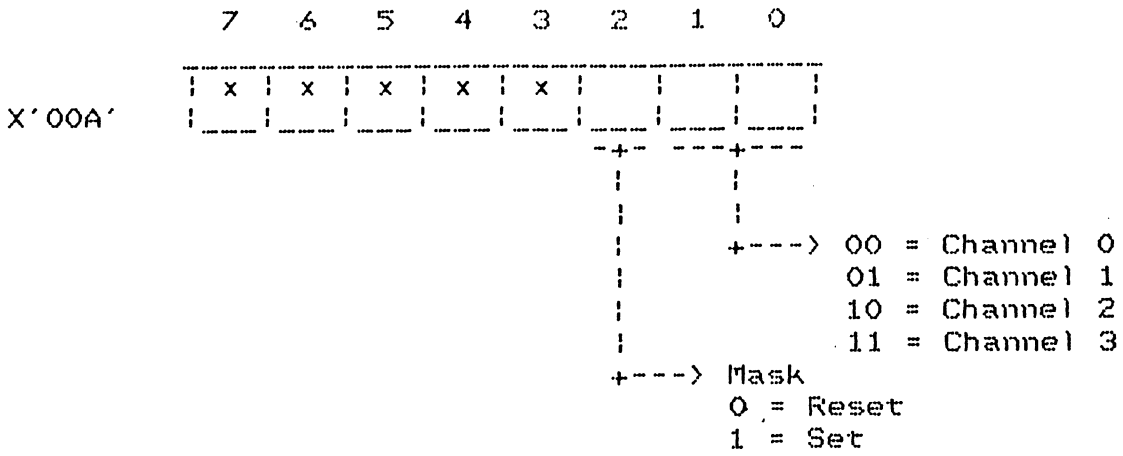
DMA Status Register: The status register is physically the same register as the control register, described on the previous page, but is used to read the status command. The format and status bits are shown in the following figure:



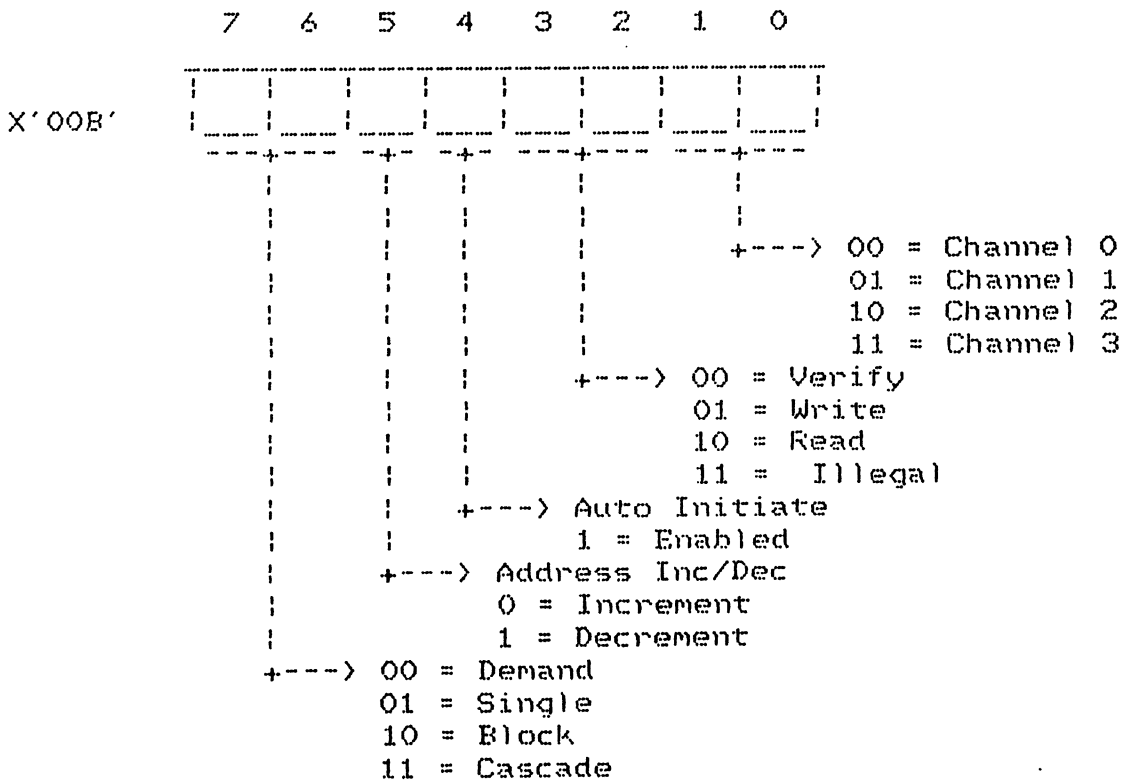
DMA Request Register:



DMA Mask SET/RESET Register:



DMA Mode Register:

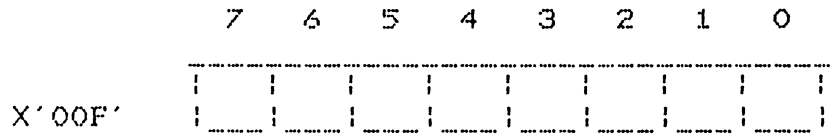


DMA Byte Pointer Register: This is a Write Only flip-flop used to clear the byte pointer bits.

DMA Temporary Register: This is a Read Only 8-bit register used during a Memory-to-Memory transfer to hold one byte of data.

DMA Clear Mask Register: This is a Write Only register used to clear the mask bits.

DMA Write All Mask Register: This is a Write Only register used to clear all the mask bits.



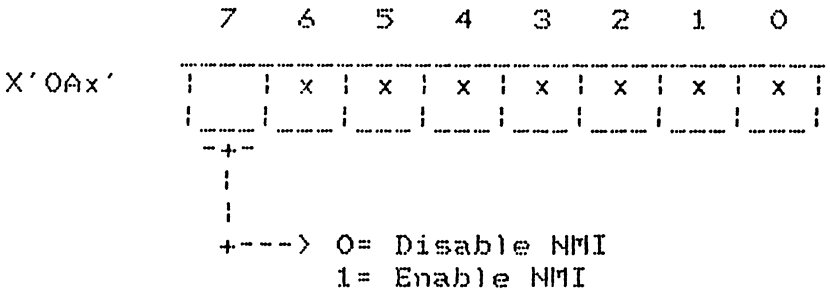
2.6 INTERRUPT CONTROL

Interrupt Control on the MAD-1 Personal Workstation consists of two classes of interrupts. The first class contains the Non-Maskable Interrupt (NMI) which is triggered by the occurence of a memory parity error or channel error. The second class contains eight levels of maskable interrupts, 0 thru 7, which are provided by the Intel 8259A Programmable Interrupt Controller (PIC) chip.

2.6.1 Non-Maskable Interrupt

The NMI logic is provided by the 80186 microprocessor, and is used to indicate parity error in main memory or in the I/O channel.

There are two jumpers provided on the MAD-1 Personal Workstation (W-6 and W-9 on CPU board) to enable/disable NMI via hardware. The NMI can be enabled/disabled under program control by writing X'80' (enable) and X'00' (disable) to I/O address X'0Ax'. During the power-up sequence, the NMI interrupt is masked off regardless of the bit settings in the NMI register. The format of NMI register is shown below: **NMI Register:**



2.6.2 Interrupt Level 0 Through 7

The remaining class of control interrupts in the MAD-1 Personal Workstation contains eight levels of interrupts, INT0-7. These eight lines are provided by the Intel 8259A PIC chip, where level INT0 has the highest priority and level INT7 has the lowest priority. The interrupt requests (IRQ0-7) are queued by priority and automatically transfer control of the program to a designated routine. The interrupt request and interrupt vector are sent to the processor giving the location of the routine to process the

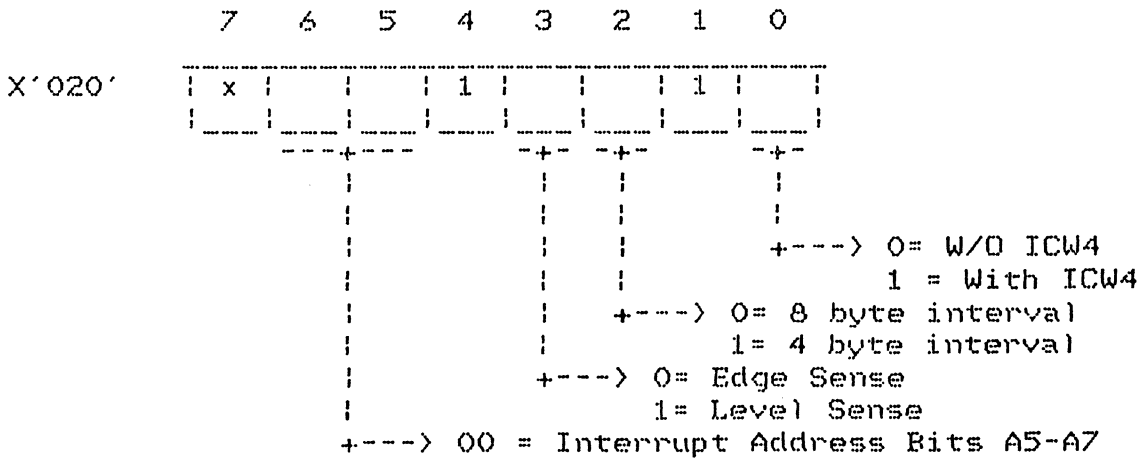
interrupt vector. In the event that there is more than one device requesting an interrupt, the interrupt requests are queued in the order of priority listed below:

IRQ0 = System Clock Tick
IRQ1 = Keyboard
IRQ2 = Expansion Bus
IRQ3 = Expansion Bus
IRQ4 = Primary Serial Port
IRQ5 = Expansion Bus (Optional Fixed Disk)
IRQ6 = Floppy Disk Controller
IRQ7 = Printer or Secondary Serial Port

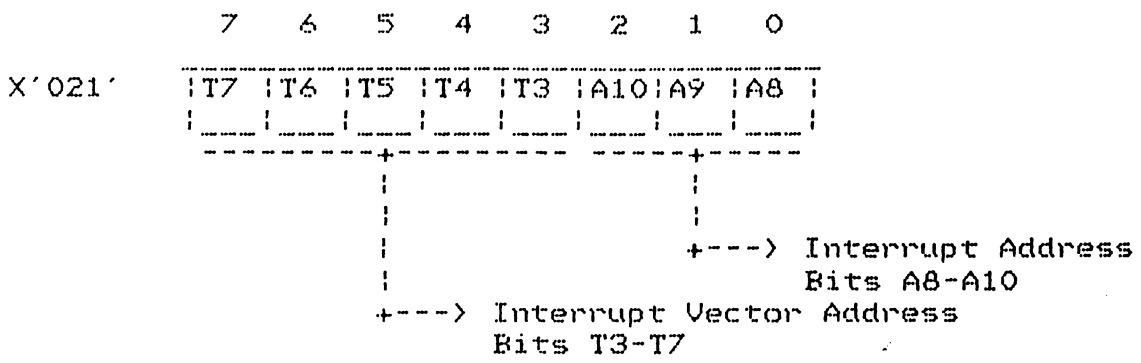
2.6.2.1 Initialization Command Word

The interrupt controller provides four 8-bit Initialization Command Word (ICW) Registers which are used in programming the 8259A PIC chip. The ICW registers are addressable by the program as I/O addresses X'020' and X'021'. The I/O address and format of the ICW registers are shown below:

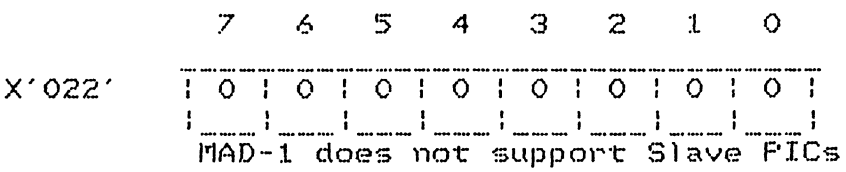
Initialization Command Word1 (ICW1):



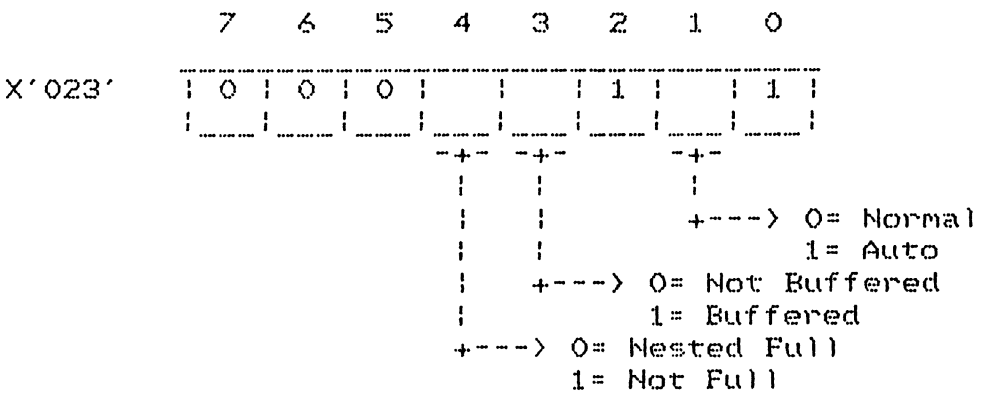
Initailization Command Word2 (ICW2):



Initialization Command Word3 (ICW3):



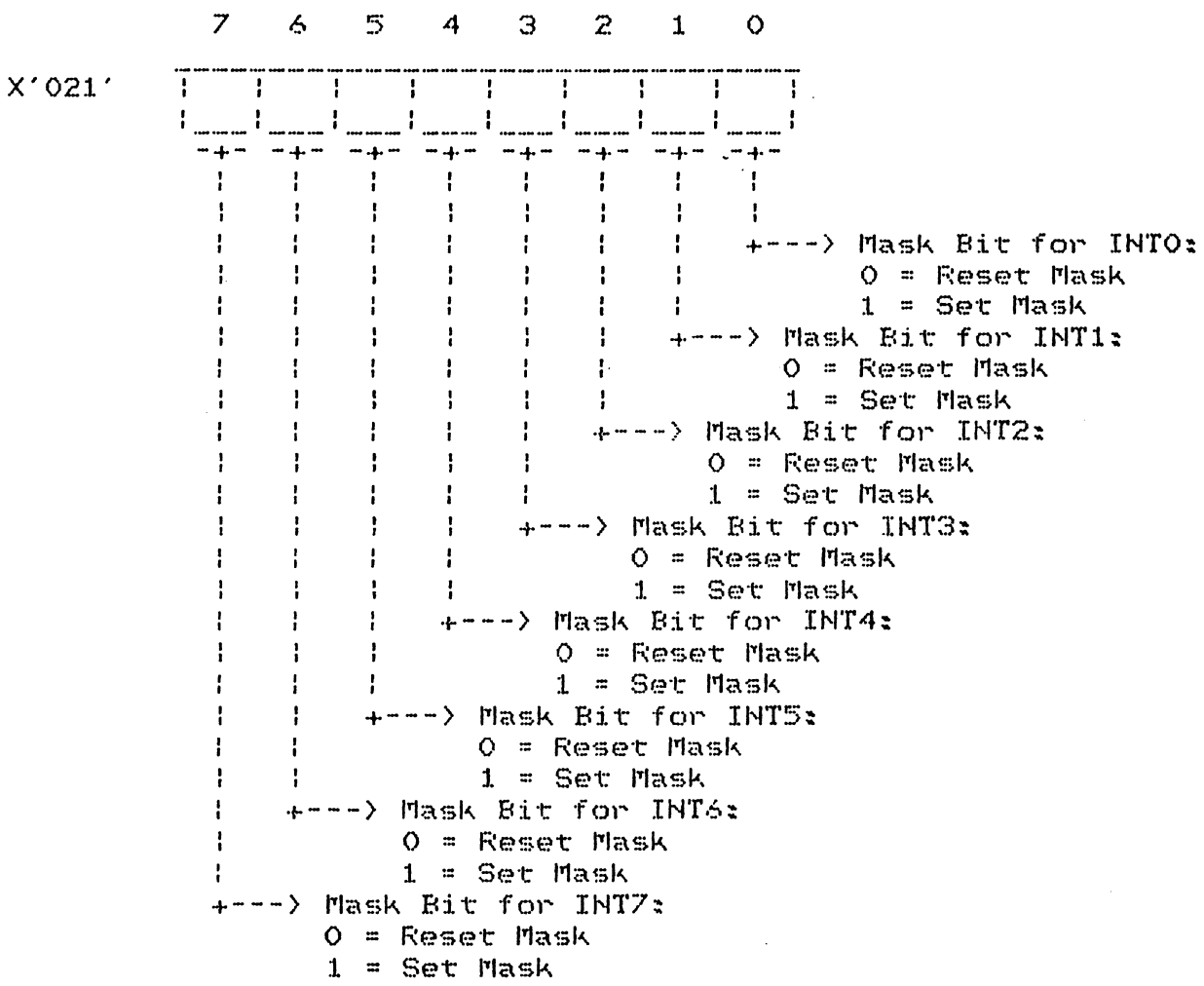
Initialization Command Word4 (ICW4):



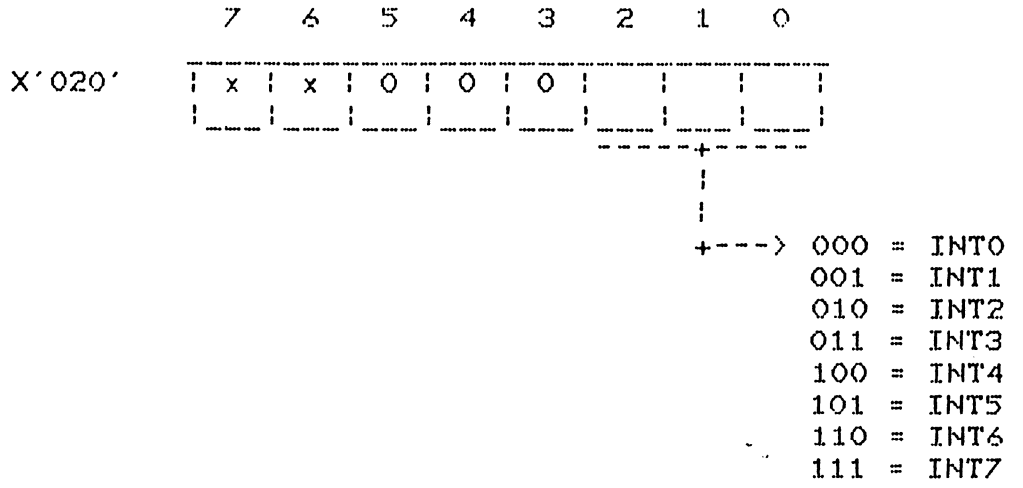
2.6.2.2 Operation Command Word

In addition to the four ICW registers, there are three Operation Command Word (OCW) registers containing the operation control words issued after initialization. The I/O address and format of each OCW register are shown below:

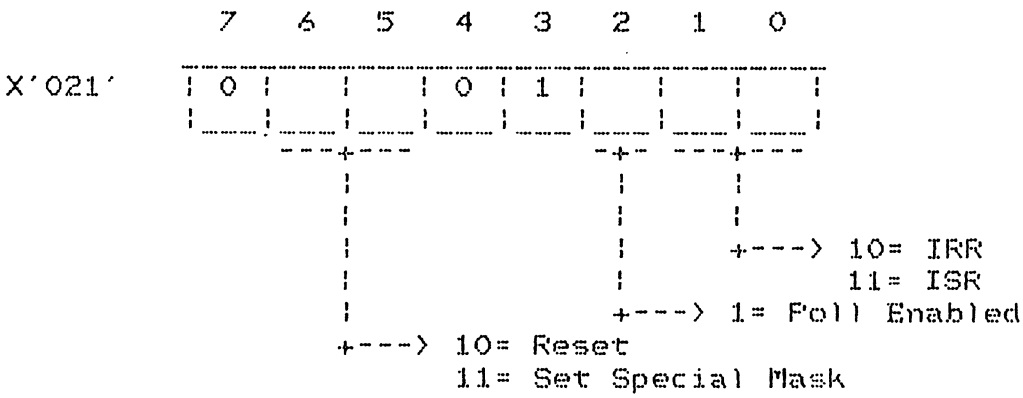
Operation Command Word1 (OCW1): This register is used as an interrupt mask register.



Operation Command Word2 (OCW2): This register is used for the end of an interrupt command and priority rotate.



Operation Command Word3 (OCW3):



2.6.3 Interrupt Programming Consideration

I/O addresses, X'20' and X'21', are used for programming INT0 through INT7, as shown on the previous pages. Each level, as indicated in the following Table, is controlled by the program and may be enabled or disabled by the mask bit under program control. The Non-Maskable Interrupt (NMI) is enabled at all times except during power up. However, NMI's may be enabled or disabled by the program, providing that jumper W-6 is installed. If the jumper is installed, the NMI can be disabled by writing X'00' to I/O location X'0Ax'; and enabled by writing X'80' to I/O address X'0Ax'.

Interrupt Priority	Device Assignment	I/O Address
NMI	Memory Parity Error	X'0Ax'
INT0	System Clock Tick	X'20-21'
INT1	Keyboard	X'20-21'
INT2	Expansion Bus	X'20-21'
INT3	Expansion Bus	X'20-21'
INT4	Primary Serial Port	X'20-21'
INT5	Expansion Bus (Optional Fixed Disk)	X'20-21'
INT6	Floppy Disk Controller	X'20-21'
INT7	Printer or Secondary Serial Port	X'20-21'

2.7 INTERVAL TIMER CHANNELS

The timer facility of the MAD-1 Personal Workstation consists of three internal timer channels (internal to the 80186 and not currently used) and three external timed interval channels (CT0, CT1, and CT2) using the Intel 8254 Timer chip operating at 1.19 MHz.

CT0 is connected to INT0 of the Intel 8259A-2 Interrupt Control chip in order to generate a clock tick. CT1 is used to generate the baud clock for the Intel 8274 USART. CT2 is connected to the speaker circuitry to generate audio signals for the speaker under program control.

2.7.1 Programming Consideration

The Intel 8254 Timer chip is a programmable device which allows each of the three timed interval channels to be programmed to a specific need. There are four 8-bit registers, with I/O addresses of X'040' through X'043', that are used in conjunction with the 8254 timer chip for programming the timer channel. A specific control word is first written into control register (I/O address X'043') to select a specified timer channel, and then data is written into the data register of the selected timer channel.

Timer Channel 0 Data Register:

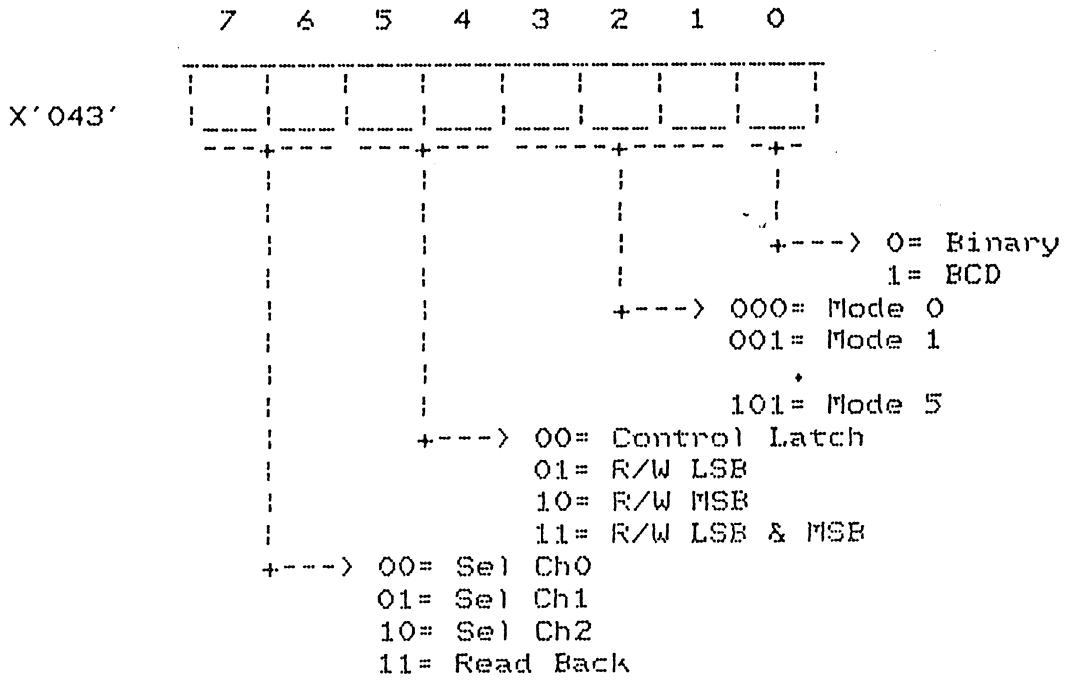
	7	6	5	4	3	2	1	0
X'040'								

Timer Channel 1 Data Register:

	7	6	5	4	3	2	1	0
X'041'								

Timer Channel 2 Data Register:

Timer Channel Control Register:



2.8 PROGRAMMABLE PERIPHERAL INTERFACE

The Intel 8255 Programmable Peripheral Interface (PPI) chip is used for control and interfacing on the CPU board via its three ports, Port A, Port B, and Port C. The following paragraphs describe the MAD-1 PPI port connections:

PORT A: This port is used for reading the keyboard scan code or the configuration switch read out.

PORT B: This port is used to enable the keyboard, to enable parity circuitry, force floppy disk drive motor on, and to program the speaker circuitry.

PORT C: This port is used for returning system status and errors, such as memory parity error.

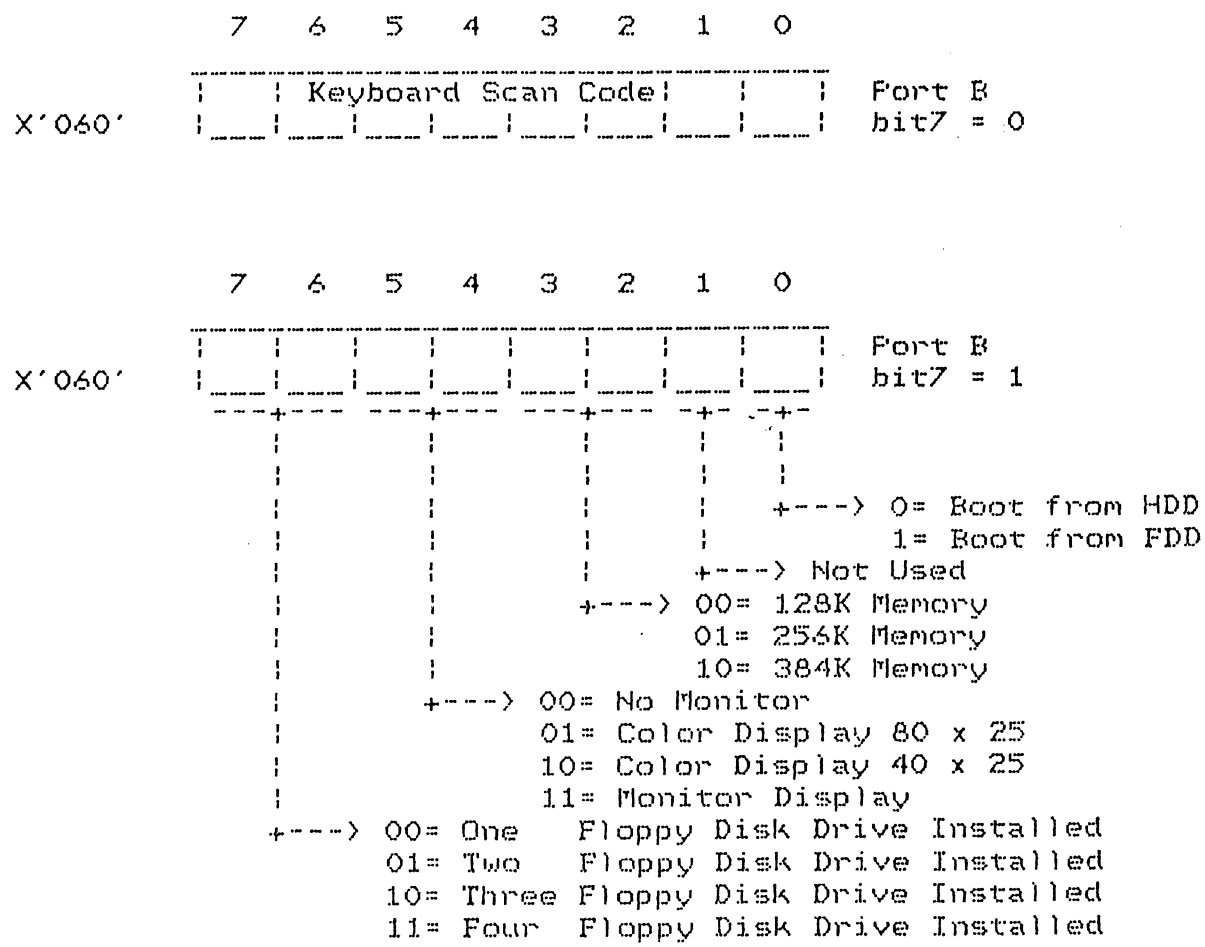
Data, control, and status information are transfered to/from the system bus via an 8-bit buffer provided by PPI. Access to each individual port and its operation is described in the following paragraphs:

2.8.1 PPI Port Operation

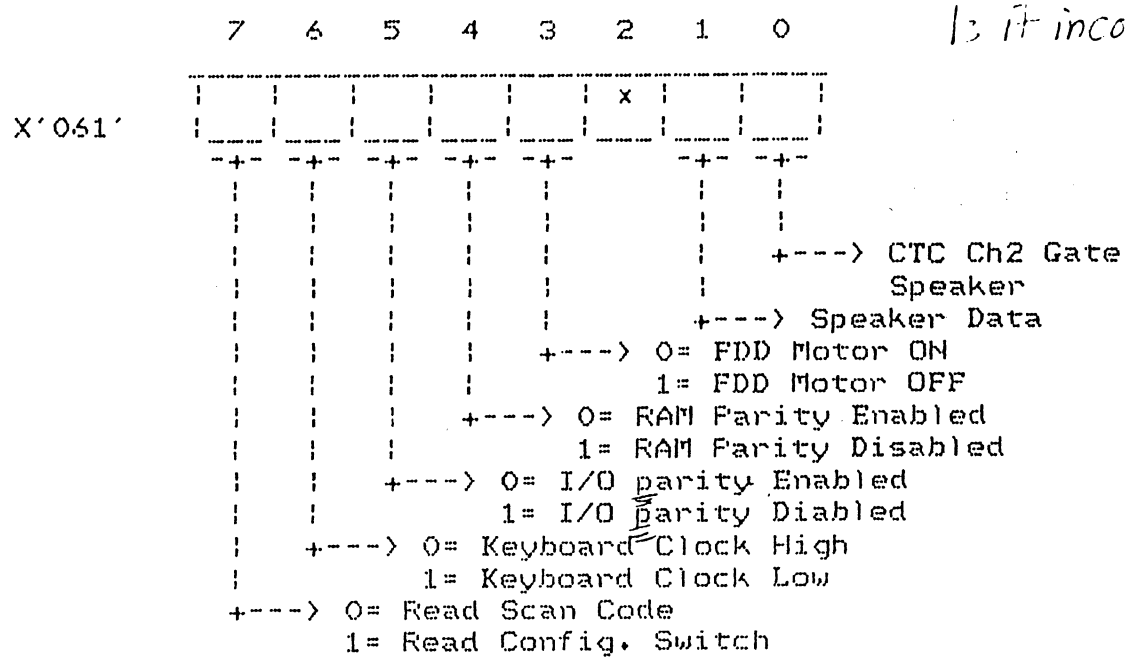
PPI Mode Register: This is a ~~Write Only~~ register.

	7	6	5	4	3	2	1	0
X'063'	1	0	1	1	1	0	0	1

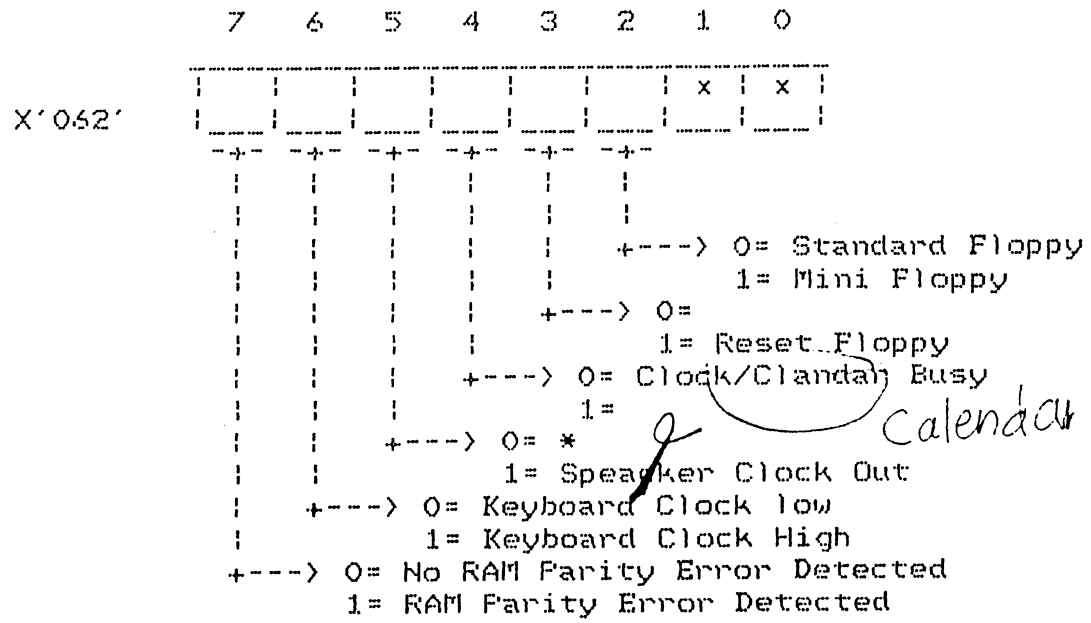
PPI Port A Register: This is a ~~Read Only~~ register and, depending on bit 7 of Port B (Enable bit), contains keyboard scan code, or configuration switch read out.



PPI Port B Register: This is a Write only register. what happened to this line? Is it incorrect



PPI Port C Register: This is a Read Only register.



Calendar

what happened to 2.8.2 – info regarding audio signal?

2.9 SERIAL COMMUNICATION INTERFACE

The MAD-1 provides two serial communication ports supporting three serial communication interfaces:

1. **Primary Serial Communication (COM 0)**
   This is an asynchronous serial communication utilizing the Intel 8250 programmable UART with RS-232C protocol.

2. **Secondary Serial Communication (COM 1)**
   To operate COM 1 serial channel, the serial port address is sent out on the I/O bus for an IBM or an IBM compatible Serial Communication Expansion board.

3. **Tertiary Serial Communication (COM 2)**
   The Tertiary serial channel is a high speed multi-protocol serial channel which supports synchronous, IBM BSC, SDLC, and HDLC protocols. Tertiary serial communication utilizes the Intel multiprotocol 8274 programmable USART chip, and provides either RS-232C or RS-422 interface.

only 2 serial ports — how come these 3 are listed?

The MAD-1 is equipped with a programmable baud rate generator that facilitates operation with a desired baud rate ranging from 50 baud to 9600 baud. The interface logic for the primary and tertiary serial communication interfaces are located on the CPU board in the computing module. I/O signals for the primary and tertiary interfaces are made available at the 25-pin 'D' type connectors J15 and J14, respectively, located on the rear panel of the computing module (shown in Figure 2-9).

what happened to 2.9.1 "serial interface mode of Operation?

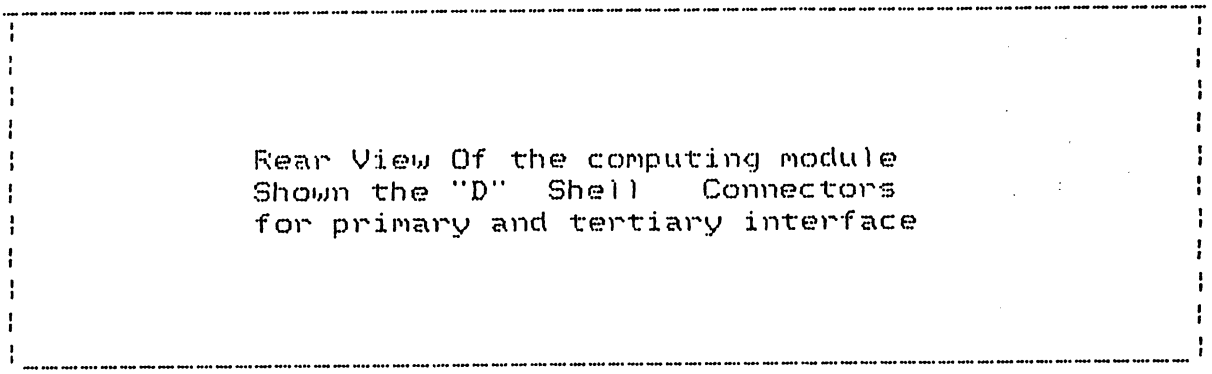
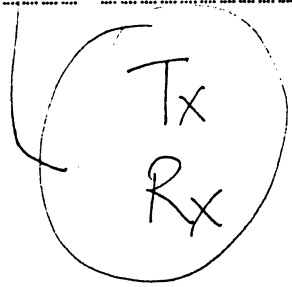


Figure 2-9: Back of Computing Module

Table 2-3: I/O Address Assignments, Primary & Secondary Port

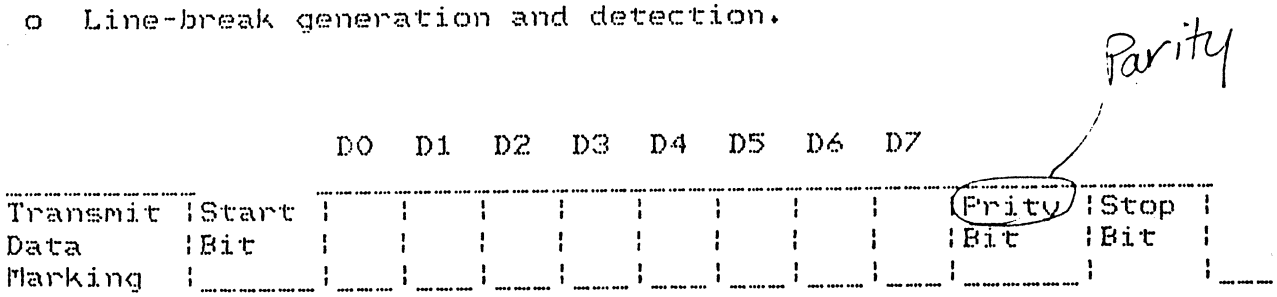
I/O Address (Hex)		Corresponding Register	
Primary	Secondary		
3F8	2F8	TX Buffer	DLAB=0 (Write)
3F8	2F8	RX Buffer	DLAB=0 (Read)
3F8	2F8	Divisor Latch LSB	DLAB=1
3F9	2F9	Divisor Latch MSB	DLAB=1
3F9	2F9	Interrupt Enable Register	
3FA	2FA	Interrupt Identification Register	
3FB	2FB	Line Control Register	
3FC	2FC	Modem Control Register	
3FD	2FD	Line Status Register	
3FE	2FE	Modem Status Register	



2.9.2 Primary Serial Communication, UART

The primary interface is a fully programmable asynchronous communication interface that is capable of adding/deleting start bit, stop bit(s), and the parity bit to/from characters for transmission. It features a programmable baud rate generator that supports variable baud rate operations ranging from 50 to 9600 baud. Primary interface logic is controlled by an Intel 8250 programmable UART which supports:

- o Five, six, seven, or eight bit characters with 1 start bit, and 1, 1-1/2, or 2 stop bits.
- o Fully prioritized interrupts:
  - Transmit Interrupt
  - Receive Interrupt
  - Error Interrupt
  - Line Status Interrupt
  - Data Set Interrupt
- o Diagnostic capability which provides loopback functions of transmit/receive and input/output signals.
- o Full double buffering which eliminates the need for precise synchronization.
- o Independent receiver clock input.
- o Modem control functions:
  - CTS, Clear To Send
  - RTS, Request To Send
  - DSR, Data Set Ready
  - DTR, Data Terminal Ready
  - RI,Ring Indicator
  - Carrier Detect
- o False-start bit detection.
- o Line-break generation and detection.



Data Transfer Format Diagram

is firmware loaded?

Actual communication protocol for the primary serial interface is controlled by communication software. The software is operated by system firmware which is loaded prior to any serial interface operations. A block diagram of the primary communication channel using an Intel 8250 programmable UART is shown in Figure 2-10.

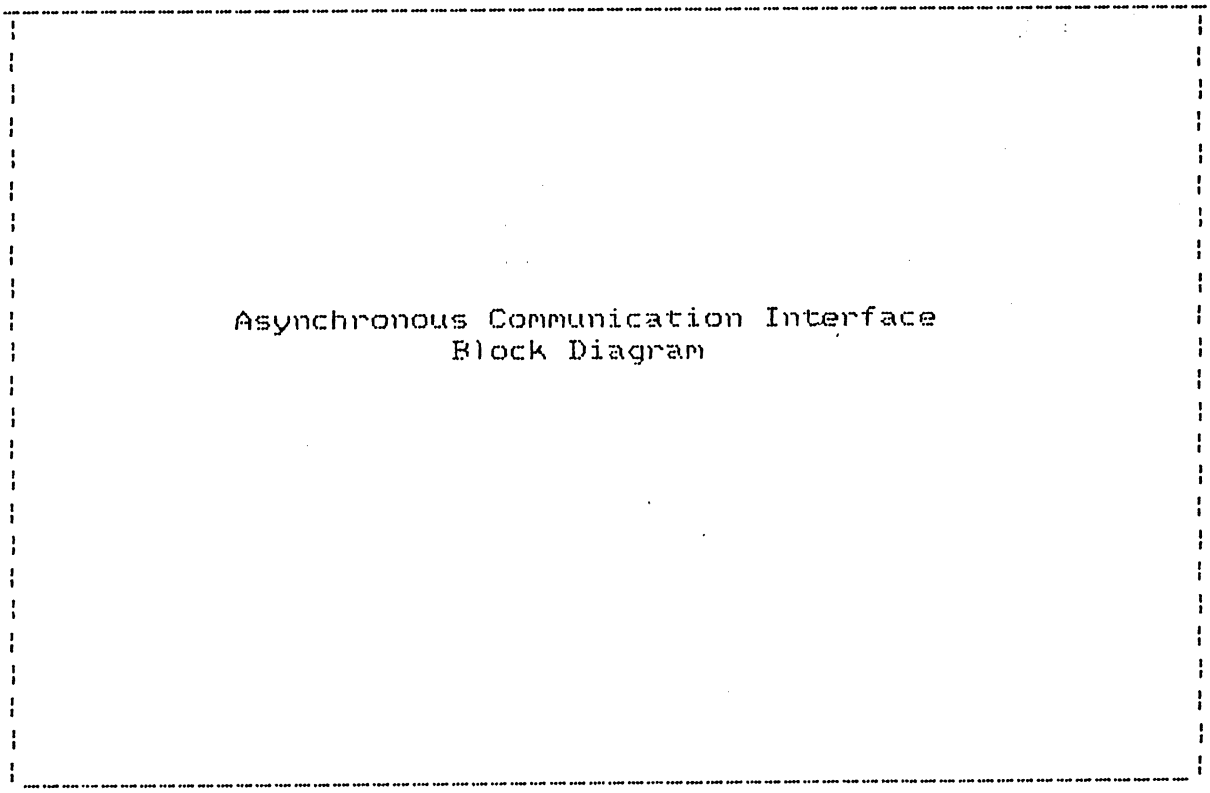


Figure 2-10: Primary Communication Block Diagram

2.9.2.1 Intel 8250 I/O Description

The following table describes the logical state and function of the signals assigned to the 8250 I/O pins:

Table 2-5: 8250 I/O Pin Description

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
+D7 - D0	1 -8	I/O	Data bus bit 7 through bit 0 are used for bidirectional data transfer.
+RCLK	9	I	Receiver Clock is 16 times the baud rate clock for the receiver section of the chip.
+SIN	10	I	This pin is assigned to serial input data from the communication link.
+SOUT	11	O	Composite Serial Output to communication link. Set to marking (logical 1) state upon master reset operation.
+CS0 +CS1 -CS2	12 13 14	I I I	When Chip Select 0 and 1 are high and Chip Select 2 is low, the chip is selected. Chip select signals CS0 - CS2 are latched with the address strobe (-ADS). When chip is selected, communication between the processor and the 8250 is enabled.
-BAUDOUT	15	O	BAUDOUT is 16 times the clock signal used for transmitter section of the 8250. Clock rate equal to main reference oscillator frequency divided by the specified divisor in the baud generator divisor latches.
+XTAL1 +XTAL2	16 17	I/O I/O	External Clock Input/Output used to connect the crystal oscillator to the 8250.
-DOSTR +DOSTR	18 19	I I	When -DOSTR is low or +DOSTR is high (while chip is selected), the processor is allowed to write data or control information into a selected register of the 8250 chip. Note: Only a high +DOSTR or a low -DOSTR is required to allow data transfer from the 8250 during a write.

Continued

Table 2-5 continued:

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
VSS	20		GND (0 Vdc) reference.
-DISTR +DISTR	21 22	I I	When -DISTR is low or +DISTR is high (while chip is selected), the processor is allowed to read status or data information from the registers of the selected chip. Note: Only a high +DISTR or a low -DISTR is required to allow data transfer from the 8250 during a read.
+DDIS	23	O	Driver Disable; used to disable external transceiver except during a processor read.
+CSOUT	24	O	Chip Select Out, when high, indicates that the chip has been selected by active +CS0, +CS1, and -CS2 inputs. No data transfer can be initiated until the CSOUT signal is active high.
-ADS	25	I	When this signal is low, it allows CS0-CS2 and A0 - A2 signals to be latched.
+A0 +A1 +A2	26 27 28	I I I	These three high active input signals are used during a read or write operation to select one of the 8250 registers: DLAB A2 A1 A0 — REGISTER 0 0 0 0 — Rec Buff/Xmit holding 0 0 0 1 — Input enable x 0 1 0 — Interrupt ID (Read only) x 0 1 1 — Line Control x 1 0 0 — Modem Control x 1 0 1 — Line status x 1 1 0 — Modem Status 0 1 1 1 — None 1 0 0 0 — Divisor Latch (LSB) 1 0 0 1 — Divisor Latch (MSB)
+INTRPT	30	I/O	Interrupt signal is used to indicate that either a receive error flag, received data, available, transmitter holding register empty, or modem status interrupt is active. INTRPT is set low upon master reset.

Continued

Table 2-5 continued:

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
-OUT2	31	O	Output 2 is user-designated and can be set to an active state by setting modem control register, bit 3, to "1" .
-RTS	32	O	Request To Send informs the modem, or data set, that the 8250 is ready to transmit data. RTS output signal can be set to active state by setting modem control reg., bit 1, to "1". -RTS signal is set high upon a master reset.
-DTR	33	O	Data Terminal Ready, when low, informs the modem or data set that the 8250 is ready to communicate. The DTR output signal can be set to an active low by software setting bit 0 of the modem control register to a high level. The -DTR signal is set high upon a master reset operation.
-OUT1	34	O	Output 1 is user-designated and can be set to active state by setting modem control reg., bit2, to "1" under program control.
-CTS	36	I	Clear To Send is a modem control input signal tested when the processor reads bit 4 (CTS) of the modem control register. NEW CTS, (bit 0), indicates whether CTS input has changed state since the previous reading of the modem status register.
-DSR	37	I	Data Set Ready signal, when low, indicates the modem or data set is ready to establish a communiation link/data transfer with 8250. DSR is a modem control input signal tested when the CPU reads bit 5 of the modem status reg. NEW CTS (bit 1) indicates whether the DSR input has changed since the last last reading of the modem status register.

Continued

spell out

spell out

spell out

Table 2-5 continued:

SIGNAL NAME	PIN NO.	DIR	DESCRIPTION
-RLSD	38	I	Receiver Line Signal Detect signal, when low, indicates that data carrier had been detected by the modem or data set. The -RLSD is a modem-control function input signal whose condition can be tested by the CPU via reading bit 7 of the modem status register. NEW RLSD (bit 3) indicates whether the RLSD has changed since the last reading of the modem status register.
-RI	39	I	Ring Indicator, when low indicates that a telephone ringing signal has been received by the modem or data set. The RI signal is a modem-control input whose logical condition can be read by the host CPU by reading bit 6 of the modem status register. Signal NEW RI (bit 4) of the modem status register indicates whether the state of the RI signal has changed since the last reading of the modem status register.
VCC	40		+5 Vdc supply

2.9.2.2 Primary Interface, Baud Generator

The Intel 8250 UART contains its own 1.8432 MHz clock and is used for the primary channel. The baud rate for this channel is selected under program control by setting the appropriate clock divisor value, ranging from "1" to "65535", into the divisor latches. The output frequency of the baud generator is 16 X baud rate resulting from the division. The divisor value is two 8-bit bytes that are loaded into the divisor latch (LSB) in I/O address X'3F8' and divisor latch (MSB) in I/O addresses X'3F9'. These values must be loaded during the initialization prior to any serial communication operation. To prevent a long count, the 16-bit baud counter is immediately loaded and begins counting upon loading any of the divisor latches. Since the I/O addresses X'3F8' and X'3F9' are shared registers, and they are also used as TX/RX and interrupt enable registers, to used them as a LSB and MSB of the divisor latches, the bit 7 (DLAB, Divisor Latch Address Bit) of the control register must be set to "1".

The different divisor values used to obtain a desired baud rate are listed in Table 2-6 along with the percentage of error using a clock frequency of 1.8432 MHz:

Table 2-6: Divisor Values

BAUD RATE	DIVISOR VALUE (Hex)	DIVISOR VALUE (Dec)	% ERROR
50	900	2304	-
75	600	1536	-
110	417	1047	0.026
134.5	359	857	0.058
150	300	768	-
300	180	384	-
600	0C0	192	-
1200	060	96	-
1800	040	64	-
2000	03A	58	0.69
2400	030	48	-
3600	020	32	-
4800	018	24	-
7200	010	16	-
9600	00C	12	-

Divisor LSB Latches: This register is time-shared as TX/RX buffer when DLAB = 0, and as an LSB of the divisor when DLAB = 1. As a divisor LSB register, it is used for loading the Least Significant Byte (bits 0 - 7) of the divisor value during system initialization.

	7	6	5	4	3	2	1	0	
X'3F8'	7	6	5	4	3	2	1	0	DLAB = 1

Divisor MSB Latch: This register is time shared as an Interrupt Enable Register when DLAB = 0, and as a MSB of the divisor when DLAB = 1. As a divisor MSB register, it is used for loading the Most Significant Byte (bits 8 - 15) of the divisor value during system initialization.

	7	6	5	4	3	2	1	0	
X'3F9'	15	14	13	12	11	10	9	8	DLAB = 1

2.9.2.3 Primary Port Interface Connector

I/O signals for the primary serial communication interface are brought to the J15 25-pin "D" shell connector located on the back of the computing module. The connection between the system and the external device is made via a standard serial communication cable (interface signals are shown in Figure 2-11). The interface circuitry on the CPU board converts the signals from TTL levels on the CPU board, to EIA voltage level on the cable side, and vice versa. The voltage level for the line should meet the line voltage specification described in section 2.9.6 titled Serial Interface Line Voltage Specification in this Chapter.

****** C A U T I O N ******

To prevent voltage surge on the signal drivers circuitry, the output signals must not be used to drive an inductive device, such as relay.

****

(Standard RS-232C Levels)

	01	(GROUND)	01	
	02	(DATA OUT)	02	
	03	(DATA IN)	03	
	04	(RTS)	04	
	05	(CTS)	05	
	06	(DSR)	06	
	07	(Signal Ground)	07	
SERIAL EXTERNAL DEVICE	08	(CARRIER DETECT)	08	ASYNCHRONOUS COMMUNICATION INTERFACE RS-232C
	09	(Not Connected)	09	
	10	(Not Connected)	10	
	11	(Not Connected)	11	
	12	(Not Connected)	12	
	13	(Not Connected)	13	
	14	(Not Connected)	14	
	15	(Not Connected)	15	
	16	(Not Connected)	16	
	17	(Not Connected)	17	
	18	(Not Connected)	18	
	19	(Not Connected)	19	
	20	(DTR)	20	
	21	(Not Connected)	21	
	22	(RING INDICATOR)	22	
	23	(Not Connected)	23	
	24	(Not Connected)	24	
	25	(Not Connected)	25	

Figure 2-11: Primary Serial Interface (UART) Connector J14

2.9.2.4 Primary Interface Registers and Programming

There are several data, control, and status registers to program the operation of the Intel 8250 UART. These registers are addressable by the program using the assigned I/O addresses shown in the following list:

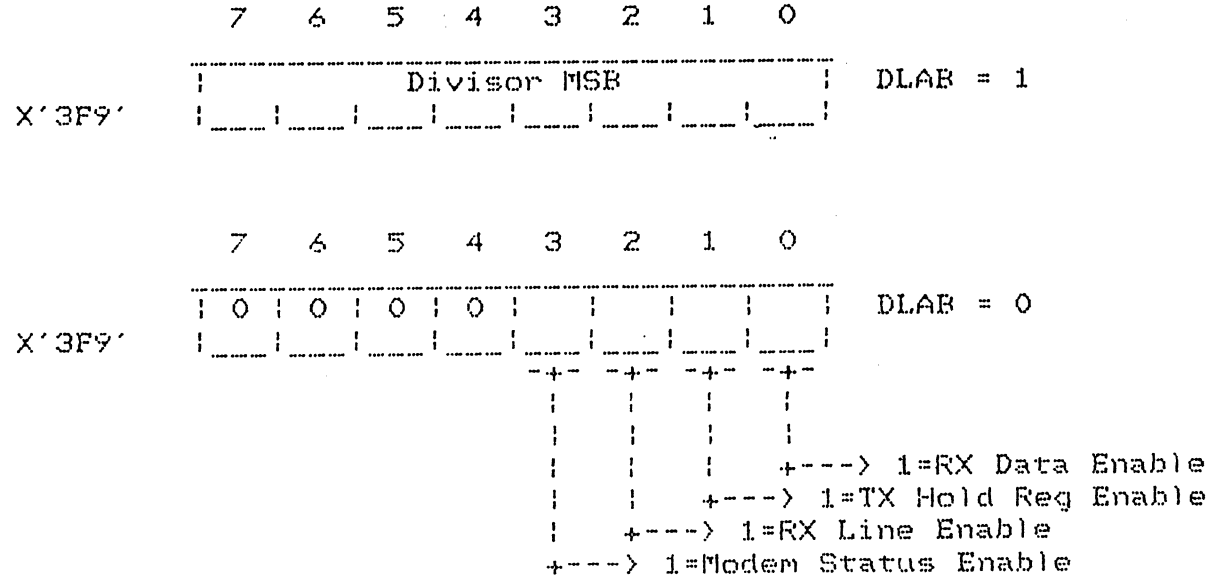
REGISTER	I/O ADDRESS
TX BUFFER (DLAB=0)	X'3F8'
RX BUFFER (DLAB=1)	X'3F8'
DIVISOR LATCH,LSB (DLAB=1)	X'3F8'
DIVISOR LATCH,MSB (DLAB=1)	X'3F9'
INTERRUPT ENABLE REGISTER	X'3F9'
INTERRUPT IDENTIFICATION REG.	X'3FA'
LINE CONTROL REGISTER	X'3FB'
MODEM CONTROL REGISTER	X'3FC'
LINE STATUS REGISTER	X'3FD'
MODEM STATUS REGISTER	X'3FE'

TX/RX Register: This register is time-shared as an LSB of the Divisor Latches when DLAB = 1 (bit 7 of the Control Register), and as a TX Buffer (Transmitter Holding Register) during transmission, and an RX Buffer (Receiver Buffer) during receive when DLAB = 0. The Transmitter Holding Register (TX Buffer) holds 8-bits of the data that are to be serially transmitted. The Receiver Buffer (RX) is used for collecting the eight serially transmitted bits.

	7	6	5	4	3	2	1	0	
	Transmit/Received Data								DLAB = 0
X'3F8'									

Bit 0 is the least significant bit and is the first bit serially transmitted and received.

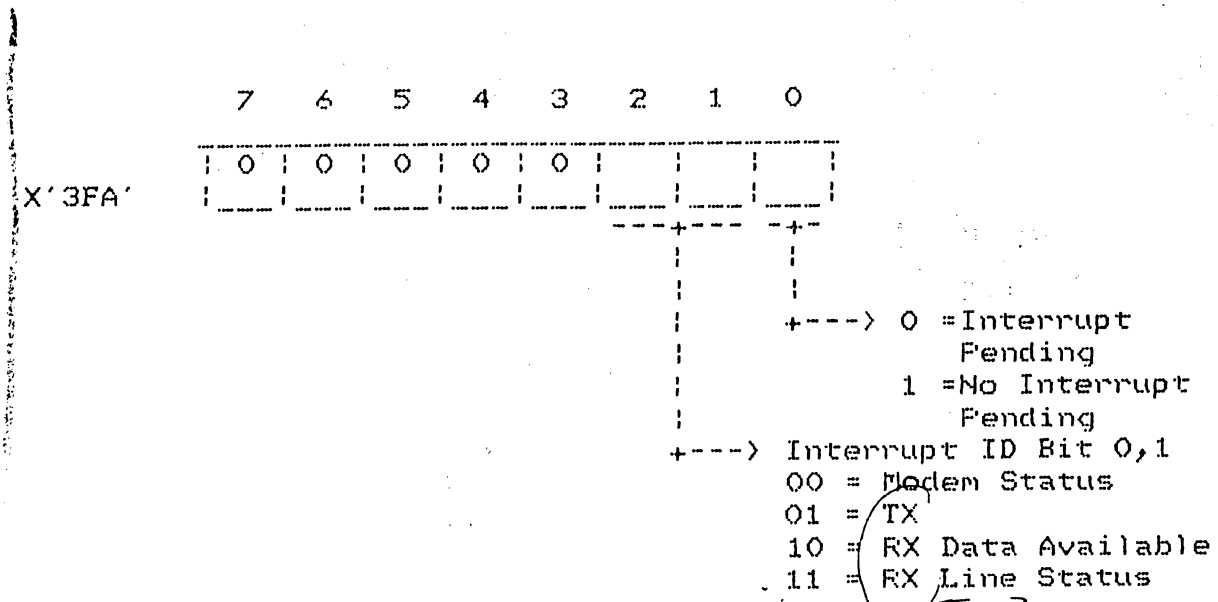
Interrupt Enable Register: This register is used for loading the most Significant Byte of the divisor value when DLAB=1, and as an interrupt enable register when DLAB=0. As an interrupt enable register, bits 0-3 are used to set/reset the individual interrupt enable bits for the four types of interrupts (Modem Status, RX Line, TX Hold, and RX Data) required for 8250 operation. Each bit can be separately set to "0" or "1" which enables or disables the corresponding interrupt. All four interrupts can be enabled or disabled without affecting the rest of the system. When all four interrupts have the enable bit set to "0", the interrupt identification register is not loaded with any interrupt information.



Interrupt Identification Register: To minimize the software overhead during data transfer operations, the 8250 provides the logic facility for prioritizing the interrupts into four levels, as shown below:

INTERRUPT TYPE	PRIORITY LEVEL
Receiver Line Status	1 (Highest Priority)
Receive Data Ready	2
Transmitter Holding Reg. Empty	3
Modem Status	4 (Lowest Priority)

The content of the Interrupt Identification Register indicates that a prioritized interrupt is pending. The type of the pending interrupt is determined by bits 0, 1, and 2 of this register. The bit description of the Interrupt ID register and the interrupt controls are given in Table 2-7.



P1-233

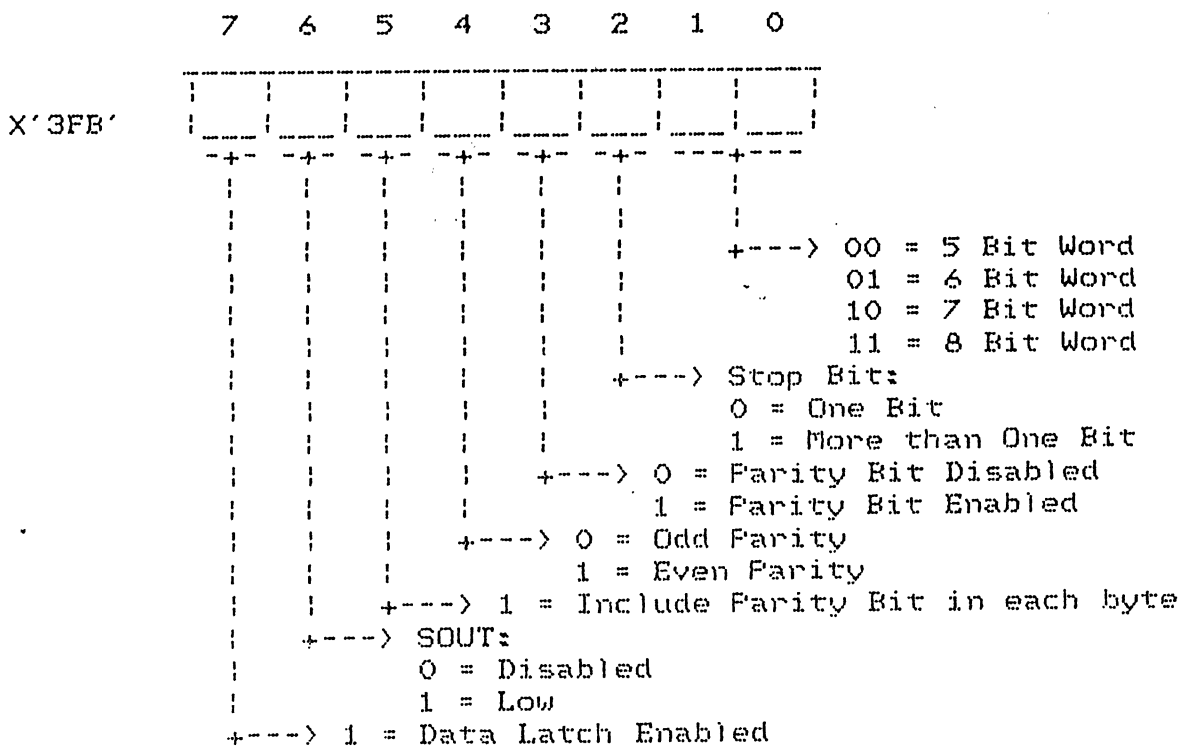
Tx ?
Rx ?

Table 2-7: Interrupt Controls

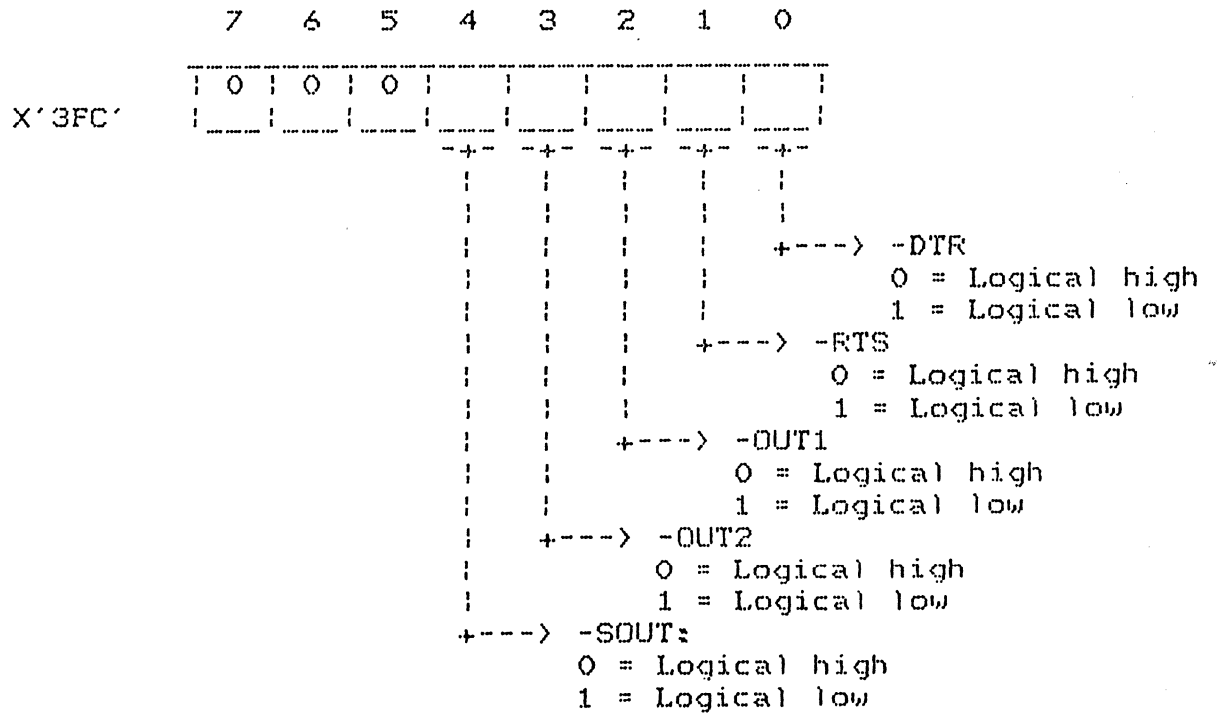
INTERRUPT ID BIT 2	1	0	LEVEL	INTERRUPT TYPE	INTERRUPT Source & Reset Control
0	0	1	-	None	Source: None
1	1	0	1	Receiver Line Status.	Source: Overrun, Parity, Framing, or Break Error. Reset : Read the Line Status Register.
1	0	0	2	Received Data Available.	Source: Data Available on Receiver. Reset : Read the Receiver Buffer Register.
0	1	0	3	Transmitter Holding Register Empty.	Source: Transmitter Hold Register Empty. Reset : Read Interrupt ID Register. Or Write Transmitter Hold Register.
0	0	0	4	Modem Status	Source: CTS, DSR, RI, or Received Line Signal Direct.

P1-234

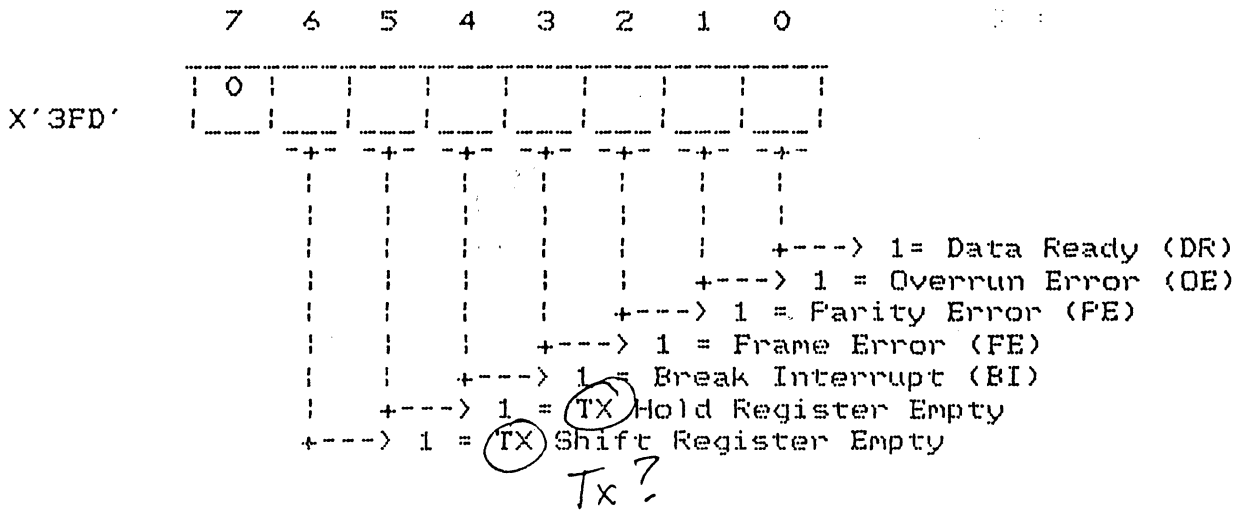
Line Control Register: This register is used by the system programmer to specify the format of the asynchronous data communication. The specified data format is stored in this register at I/O address X'3FB'. This register can be read by the system programmer to check its content for use by the program. The format and the bit definition of this register are shown below:



Modem Control Register: This register is used by the system programmer to control the operation of modems, or devices emulating modems. The content of this register, depending on its setting in I/O address X'3FC', will force the modem signals to a specified state (as shown in the diagram below). Bits 2 and 3 are auxiliary user-designated output. Bit 4 is used to enable the loopback feature for testing the 8250 controller chip. When set to "0", bit 4 forces the transmitter serial output signal -SOUT (Active Low) to a logical "1" state and causes the receiver signal input, -SIN, to be disconnected. The output of the transmitter shift register is looped back into the receiver shift register input. By activating the -SOUT bit, the modem input control signals -CTS, -DRS, -RLSD, and -RI are disconnected from external lines and are internally connected to the modem output control signals -DTR, -RTS, -OUT1, and -OUT2. These internal connections cause the transmitted data to be received immediately. This feature is used to verify the transmitter and receiver paths. During the loopback diagnostic test, both receiver and transmitter interrupts are fully operational, and the lower four bits of the modem control register are used as an interrupt source under control of the interrupt enable register.



Line Status Register: This register is used by the system programmer to retrieve status information on the 8250 serial communication controller that concerns data transmission. Line status is stored in I/O address X'3FD' and contains the information as shown in the following diagram:



Tx ?

Bit 0 of line status register, when set to "1", indicates that the input data is received and has been transferred into the receiver buffer register. This bit is reset to "0" either by writing a "0" into this bit position, or by the processor reading the data into the receiver buffer register, which in effect indicates buffer empty.

Bit 1 of line status register, when set to "1", indicates that data in the receiver buffer was not read by the processor before the next character was stored in the receiver buffer, thus destroying the previously received data. This bit will be reset to "0" when the processor reads the contents of the line status register.

Bit 2 of line status register, when set to "1", indicates that the receiver data did not have a correct parity bit. This bit will remain set until the processor reads the contents of the line status register.

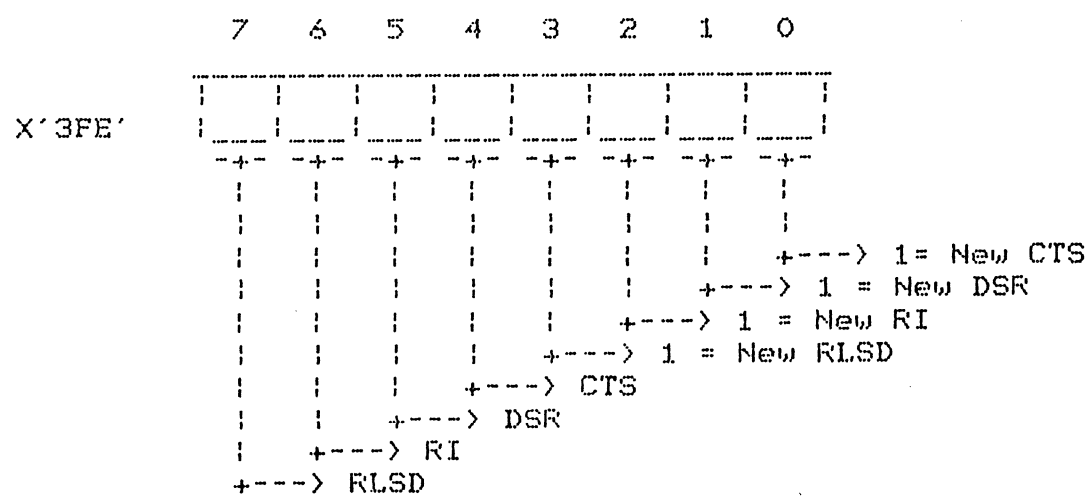
Bit 3 of line status register, when set to "1", indicates that the receiver data did not have a valid stop bit. This bit will remain set until the processor reads the content of the line status register.

Bit 4 of line status register, when set to "1", indicates that the input data signal was held in 'spacing' state longer than a full word transmission time, which includes start bit, data bit (8 bit Max.), parity bit, and stop bit(s). This bit will remain set until the processor reads the content of the line status register.

Bit 5 of line status register, when set to "1", indicates that the data from the transmitter holding register is transferred into the transmitter shift register, and the serial communication controller (8250) is ready to accept a new character for transmission. It also causes the 8250 to issue an interrupt to the processor, signaling that the transmit holding register is empty (providing the interrupt is enabled). This bit will be reset to "0" when the processor loads the transmitter holding register with data.

Bit 6 of line status register, when set to "1", indicates that the transmitter shift register is empty. This bit will reset to "0" when data from transmitter holding register is loaded into the transmitter shift register.

Modem Status Register: This register is used to provide the current status of the line connecting the modem, or devices emulating modems, to the processor. This register is accessed by reading I/O address X'3FE'. The high order four bits (bits 4-7) contain the state of Clear To Send (CTS), Data Set Ready (DSR), Ring Indictor (RI), and Received Line Signal Detect (RLSD). The low order four bits (0-3), when set to "1", indicate a change in the state of the corresponding signals stored in bits 4-7, and are designated by prefix New.



2.9.3 Secondary Serial Communication, UART

The MAD-1 Personal Workstation supports the facility for an optional secondary asynchronous serial port. This option consists of an IBM compatible serial asynchronous expansion board, or any IBM compatible, that plugs into the slot located in the computing module above the CPU board. The opening for the secondary port external interface connector is in the back of the computing module and is level with the serial expansion board (when installed).

2.9.3.1 Secondary Port, Functional Description

The functions of the secondary serial port are identical to those of the primary serial port described earlier in this Section. The differences in usage are more from a programming point of view. The program now addresses all the data, control, and status registers in I/O address spaces X'2F8' through X'2FF' instead of address spaces X'3F8 through X'3FF'.

Figure 2-12 shows the layout of the IBM serial communication expansion board that is used for the secondary asynchronous serial port.

No!

Layout of IBM serial communication expansion board

We do not want to show this!

Figure 2-12: IBM Serial Communication Expansion Board

The operation of the secondary serial port is also defined by the contents of the registers selected by the decode of bits A0, A1, and A3 of I/O addresses X'2F8' through X'2FF' for the secondary port, and X'3F8'- X'3FF' for the primary port.

Table 2-8: I/O Address Assignment For Primary & Secondary Port

I/O Address (Hex)		Corresponding Register	
Primary	Secondary		
3F8	2F8	TX Buffer	DLAB=0 (Write)
3F8	2F8	RX Buffer	DLAB=0 (Read)
3F8	2F8	Divisor Latch LSB	DLAB=1
3F9	2F9	Divisor Latch MSB	DLAB=1
3F9	2F9	Interrupt Enable Register	
3FA	2FA	Interrupt Identification Register	
3FB	2FB	Line Control Register	
3FC	2FC	Modem Control Register	
3FD	2FD	Line Status Register	
3FE	2FE	Modem Status Register	

Table 2-9: I/O Address Decode

I/O Address Bits	State Of DLAB	Function of the Selected Register
9.8.7.6.5.4.3.2.1.0		
1 * 1 1 1 1 1 x x x	-	
0 0 0	0	Receive Buf (Read)/Holding (Write)
0 0 1	0	Interrupt Enable
0 1 0	x	Interrupt Identification
0 1 1	x	Line Control Register
1 0 0	x	Modem Control
1 0 1	x	Line Status
1 1 0	x	Modem Status
1 1 1	x	Not Used
0 0 0	1	Divisor Latch LSB
0 0 1	1	Divisor Latch MSB

*: Bit 8 is always "1" for the primary interface
Bit 8 is always "0" for the secondary interface

2.9.3.2 Secondary Serial Port Interrupt Operation

Interrupt Request line 3 (IRQ3) is normally used for secondary communication operations. This line requires that the serial communication be enabled for interrupt, which is accomplished by setting bit 3 of the modem control register (I/O address 'X'2FC') to a value of "1".

2.9.3.3 Secondary Serial port Registers and Programming

There are several data, control, and status registers that are used for programming the operation of the Intel 8250 UART. These registers are addressable by the program using the assigned I/O address of each register, as listed in the following table:

REGISTER	I/O ADDRESS
TX Buffer (DLAB=0)	X'2F8'
RX Buffer (DLAB=1)	X'2F8'
Divisor Latch, LSB (DLAB=1)	X'2F8'
Divisor Latch, MSB (DLAB=1)	X'2F9'
Interrupt Enable Register	X'2F9'
Interrupt Identification Register	X'2FA'
Line Control Register	X'2FB'
Modem Control Register	X'2FC'
Line Status Register	X'2FD'
Modem Status Register	X'2FE'

2.9.3.4 Secondary Port Interface Description

The secondary serial port supports the same interface protocols that are used on the primary serial port. Connector J8, located on the back of the computing module (see Figure 2-13), is used as the secondary serial port external interface. It is a 25-Pin "D" shell connector that is used to interface to the IBM serial communication expansion board (optional) when it is installed in the computing module as the secondary serial port. The interface signal lines are shown in Figure 2-14.

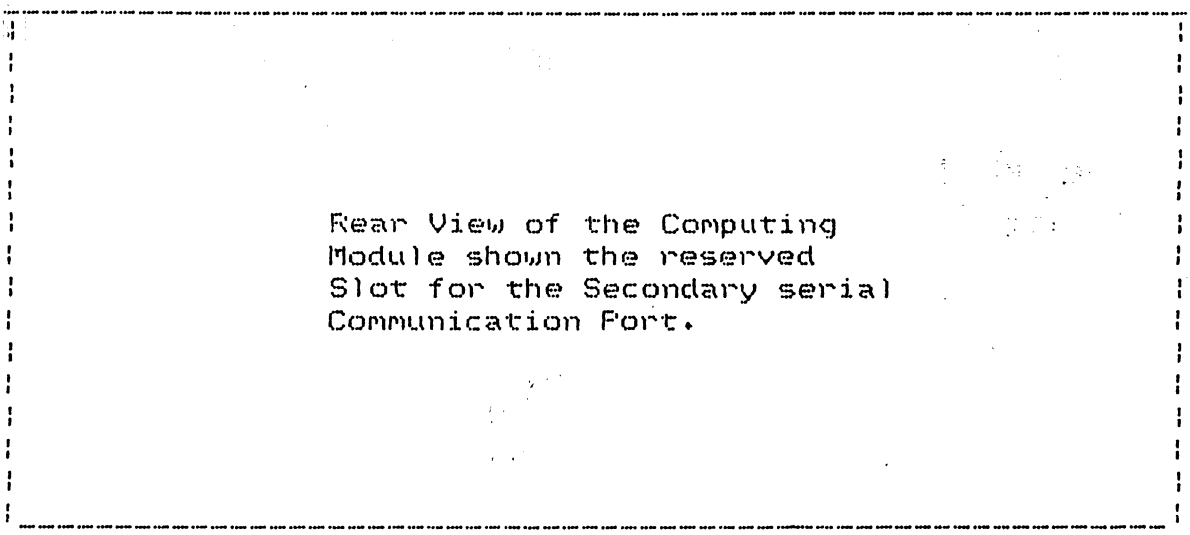


Figure 2-13: Back of Computing Module

(Standard RS-232C Levels)

	01	(GROUND)	01	
	02	< (DATA OUT)	02	
	03	(DATA IN) >	03	
	04	< (RTS)	04	
	05	(CTS) >	05	
	06	(DSR) >	06	
	07	(Signal Ground)	07	
SERIAL EXTERNAL DEVICE	08	(CARRIER DETECT) >	08	ASYNCHRONOUS COMMUNICATION INTERFACE RS-232C
	09	(Not Connected)	09	
	10	(Not Connected)	10	
	11	(Not Connected)	11	
	12	(Not Connected)	12	
	13	(Not Connected)	13	
	14	(Not Connected)	14	
	15	(Not Connected)	15	
	16	(Not Connected)	16	
	17	(Not Connected)	17	
	18	(Not Connected)	18	
	19	(Not Connected)	19	
	20	< (DTR)	20	
	21	(Not Connected)	21	
	22	(RING INDICATOR) >	22	
	23	(Not Connected)	23	
	24	(Not Connected)	24	
	25	(Not Connected)	25	

Figure 2-14: Secondary Serial Interface (UART) Connector J14

2.9.4 Tertiary Serial Communication, USART

The MAD-1 computer provides a smart serial communication port, refered to as Tertiary Serial Communication. This communication interface supports Asynchronous, IBM Bisync (BSC), and SDLC/HDLC protocols and utilizes the Intel 8274 multi-protocol serial controller chip to provide a variety of serial communication functions. The multi-protocol serial controller is capable of interfacing high-speed communication lines with the MAD-1 computer. The functional block diagram is shown in Figure 2-15.

The operation of the tertiary serial port is not compatible with IBM. It uses I/O address spaces X'2E8' through X'2EF' for referencing data, control, and status registers. These addresses are not used by the IBM PC/XT and therefore do not interfere with other IBM compatible operations.

The tertiary serial communication port provides two independent serial channels (Channel A and B). Each channel contains eight internal write, and three internal read registers. Both sets of registers may be accessed by either channel.

For normal operation, Channel A is jumpered to support RS-232C or RS-422 interface protocol and Channel B is designated to support the optional internal modem.

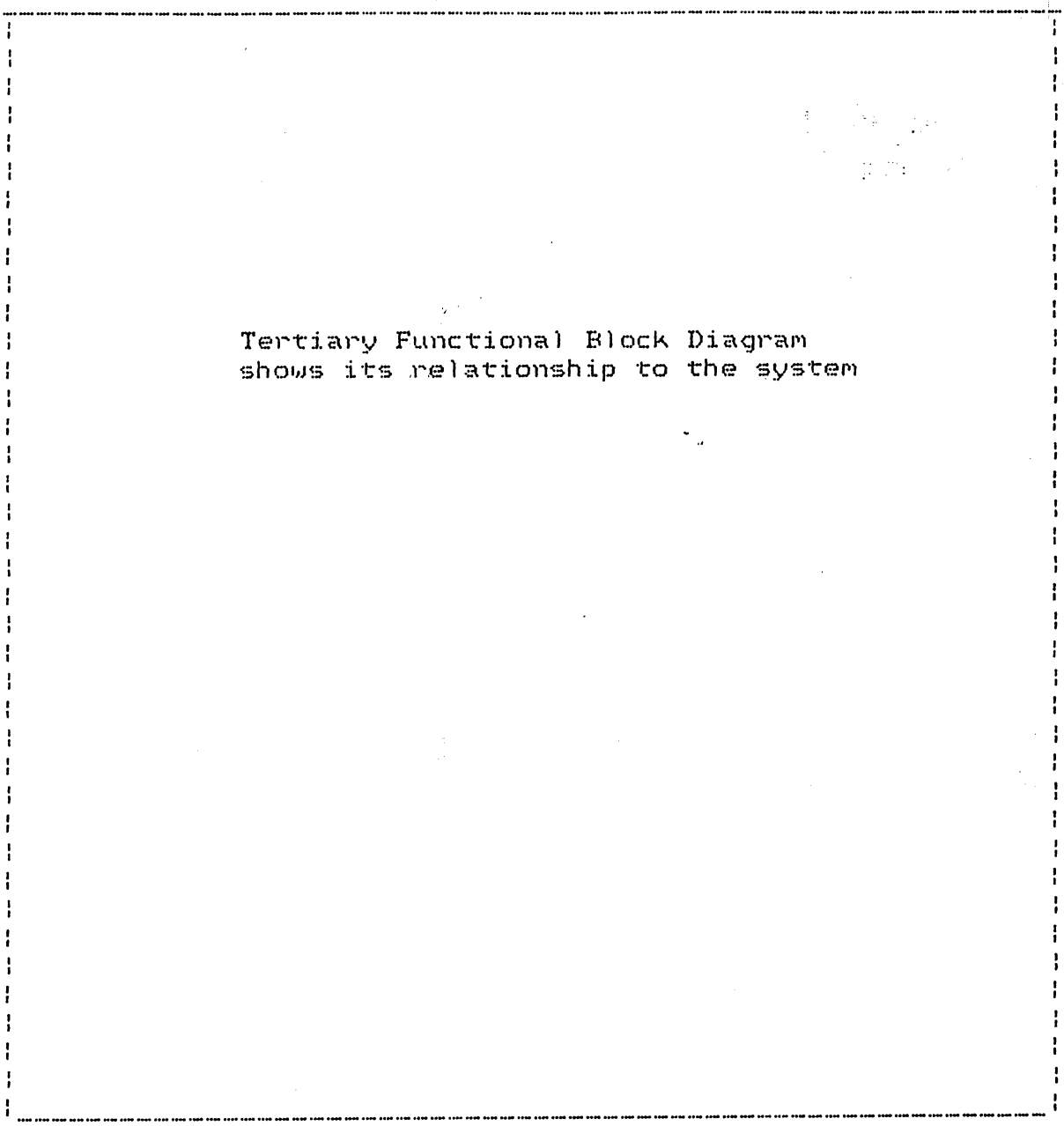
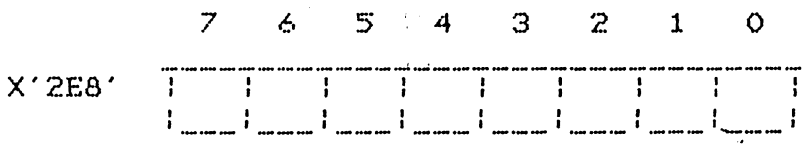


Figure 2-15: Tertiary Block Diagram

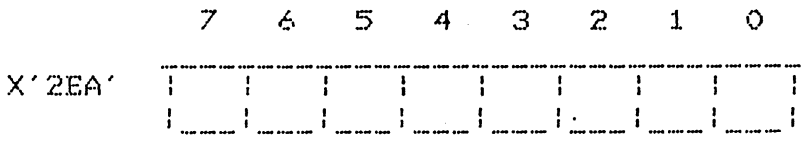
2.9.4.1 Tertiary Port Programming

I/O addresses X'2E8' through X'2EF' have been assigned to operate the tertiary serial communication port. As mentioned earlier, these addresses are not used in the IBM PC/XT systems and therefore do not interfere with other compatible operations. The descriptions of the registers used by the tertiary port are listed below:

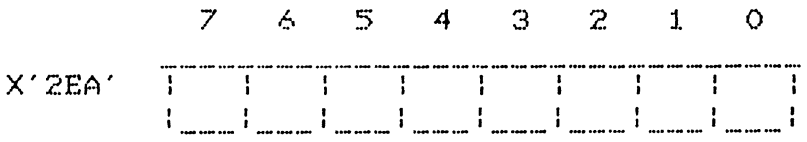
Tertiary Channel A Data:



Tertiary Channel A Status: This register is used to read the contents of any one of the three internal read registers pointed to by the register pointer value set in the command register.

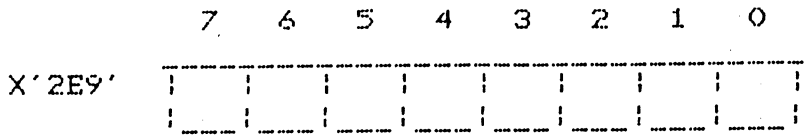


Tertiary Channel A Command:

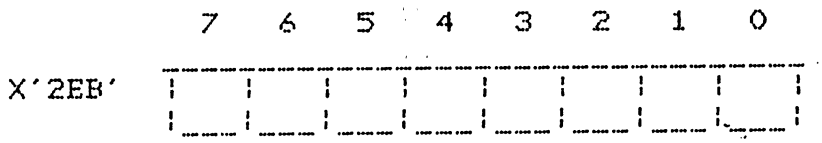


+-> Internal Register Pointer:
- 000 = Register 0
- 001 = Register 1
- 010 = Register 2
- 011 = Register 3
- 100 = Register 4
- 101 = Register 5
- 110 = Register 6
- 111 = Register 7

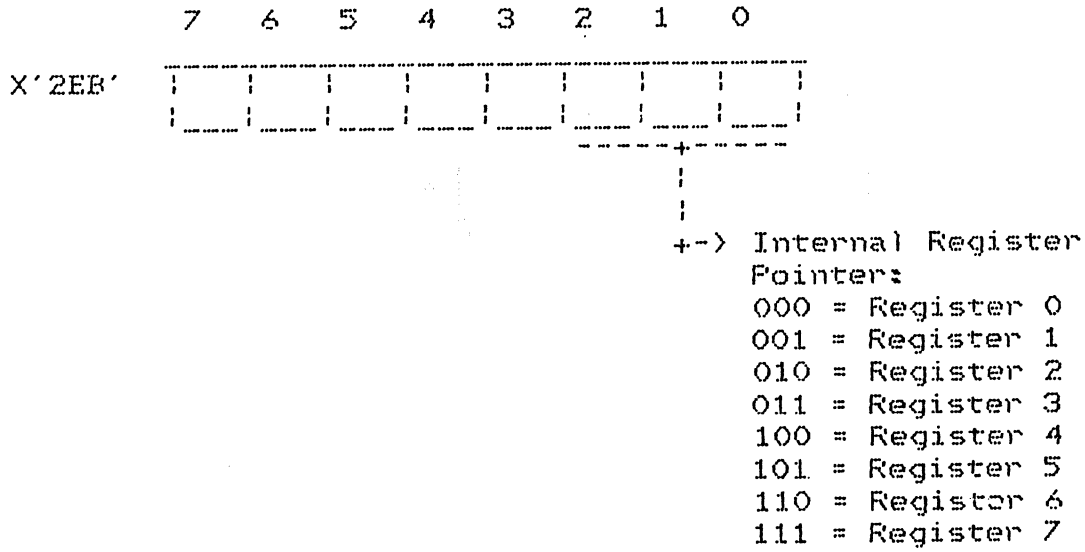
Tertiary Channel B Data:



Tertiary Channel B Status: This register is used to read the contents of any one of the three internal read registers pointed at by the register pointer value set in the command register.



Tertiary Channel B Command:



2.9.4.2 Tertiary Interface Connector

Connector J14 is a 25-pin "D" shell connector in the back of the computing module and is connected to the tertiary port interface logic. The location of the connector and its pin assignment are shown in the Figure 2-16 and the interface signals are shown in Figure 2-17.

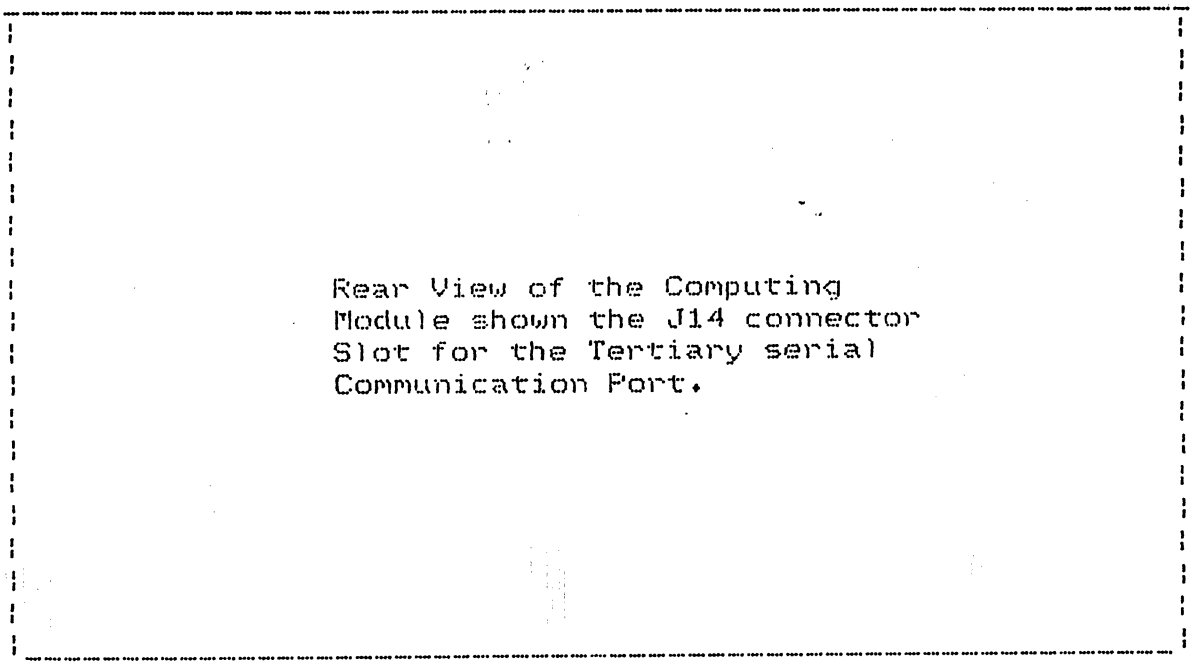


Figure 2-16: Back of Computing Module Showing J14

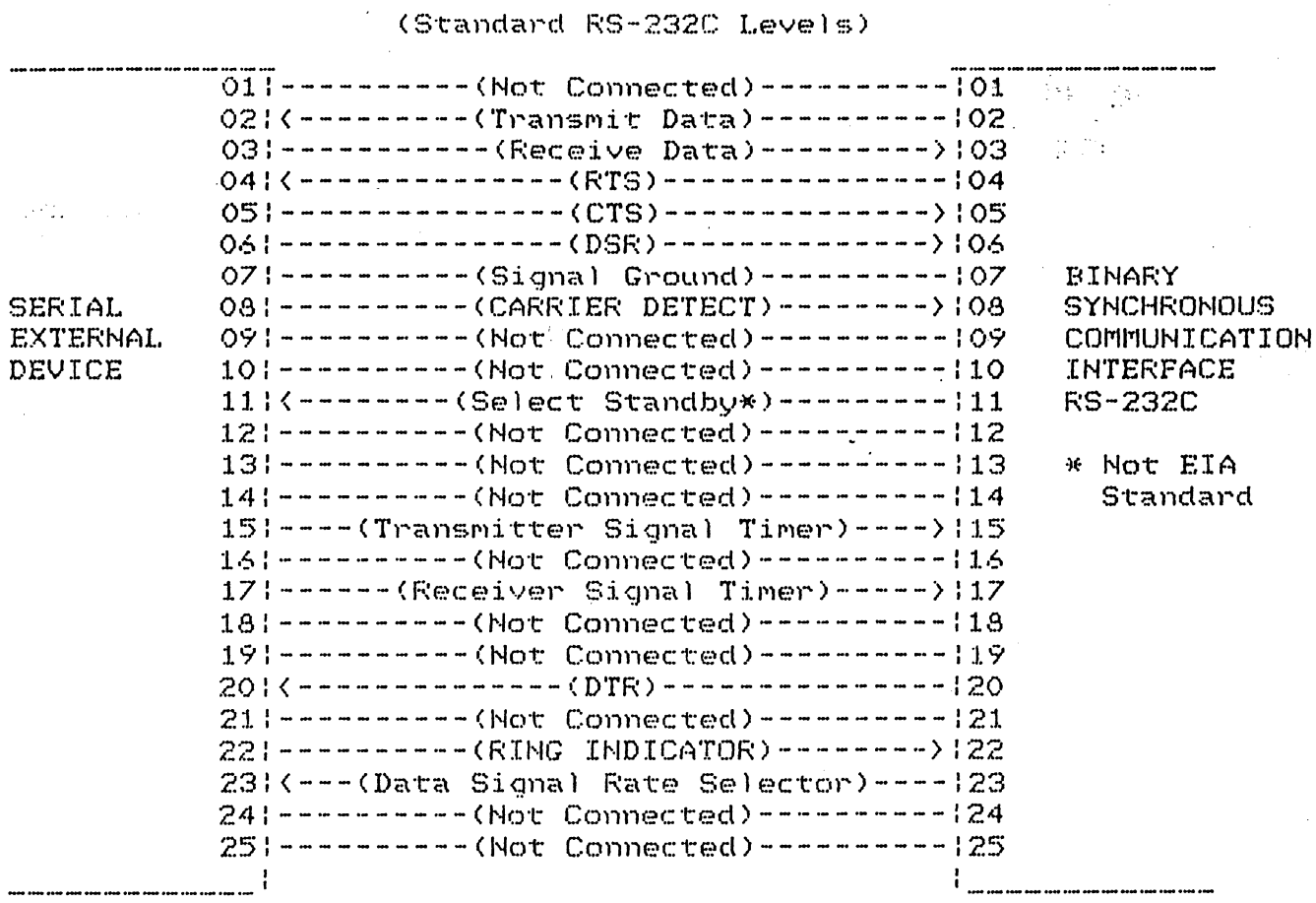


Figure 2-17: Tertiary Serial Interface (USART) Connector J14

2.9.5 Serial Interface Line Voltage Specification

This section describes the signal voltage levels for data exchange over the interface cable between the serial port and the external device. Depending on the type of serial interface and protocol, signal voltage levels may be different for the receiver and transmitter logic.

As shown in Figure 2-18, data transmission consists of two states: 'Marking', which denotes binary "1"; and 'Spacing', which denotes binary "0". Depending on the protocol, each end of the cable may have different voltage levels assigned. Figure 2-19 describes both the valid and invalid voltage levels and the logical state of the line in representing "0" or "1".

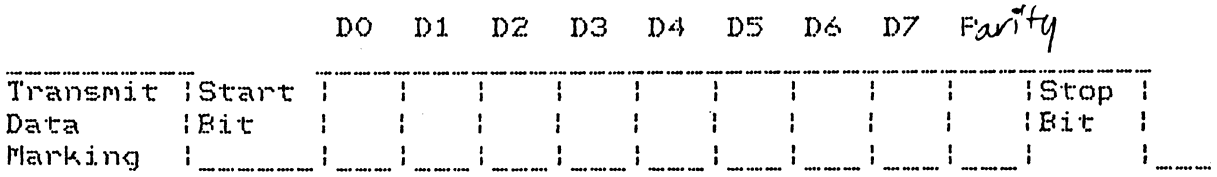


Figure 2-18: Data Transfer Format Diagram

2.9.5.1 Interface Signal Level For Primary Serial Port

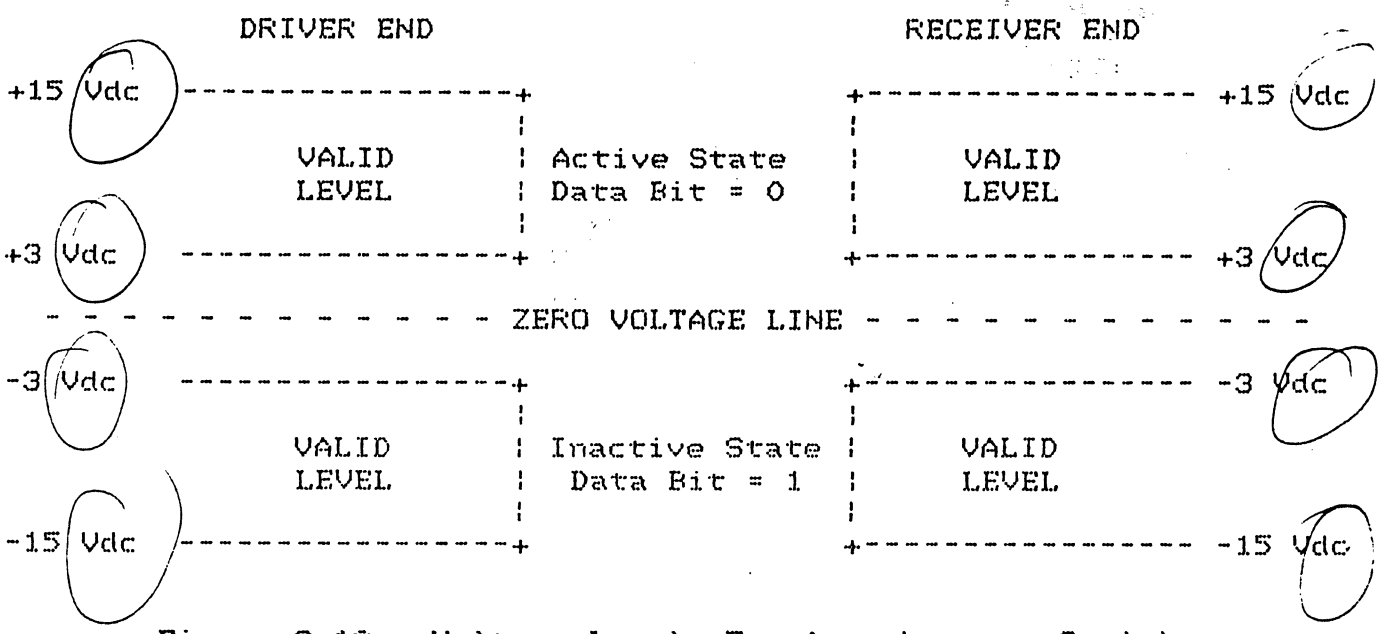


Figure 2-19: Voltage Levels For Asynchronous Serial Communication Interface Signals

2.9.5.2 Interface Signal Level For Tertiary Serial Port

The Tertiary Interface conforms to EIA RS-232C/CCITT V.24 interface signal levels, as shown in the following figure:

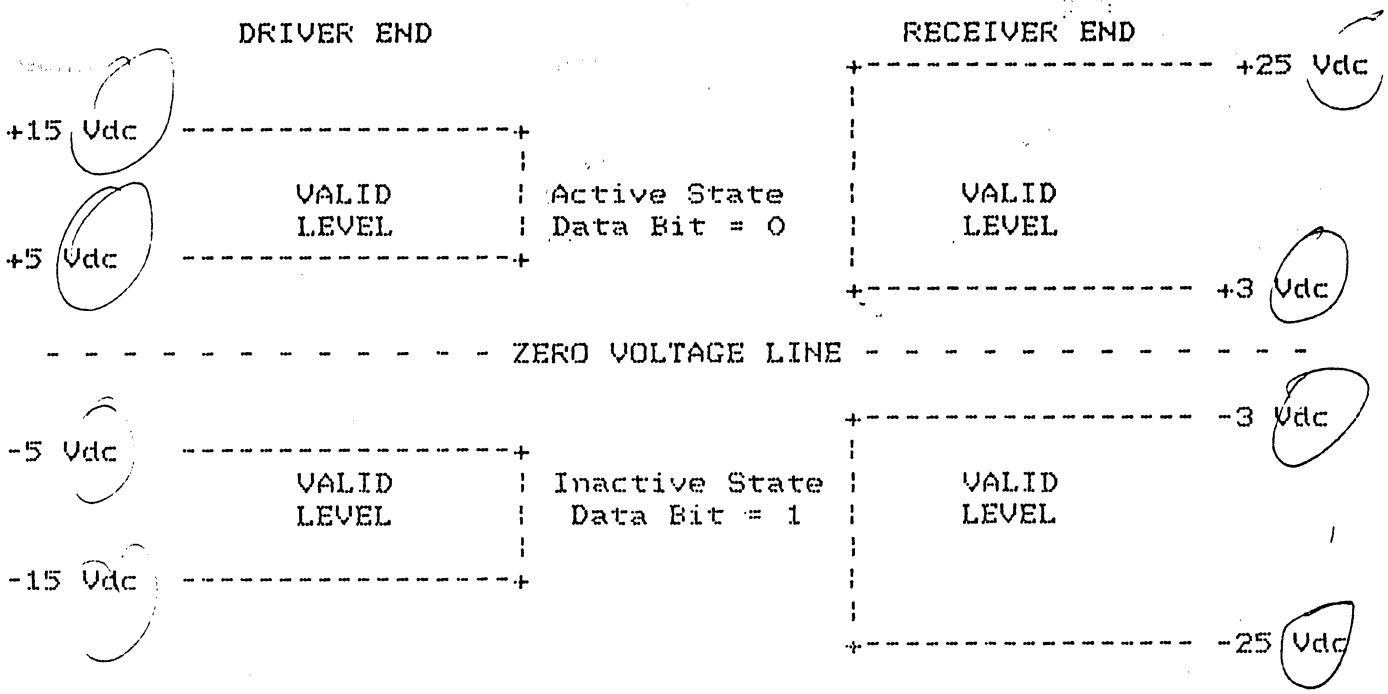


Figure 2-20: Voltage Levels For Synchronous Serial Communication Interface Signals

2.10 PARALLEL PRINTER INTERFACE

The MAD-1 Workstation supports a Parallel (centronics compatible) Printer Interface that is specifically designed to be attached to printers with parallel port interface. However, this port may be used as a general Input/Output port for any device or application that supports its protocol. The Interface consists of 12 TTL-buffer output points, which can be written or read under under program control utilizing the processor IN/OUT instructions.

Interrupt Request line 7 (IRQ7) is used by this port to interrupt the processor when the ACKNOWLEDGE signal is asserted. IRQ7 is jumpered to the Programmable Interrupt Controller (Intel 8259A-2) via jumper W-25, and can be enabled or disabled under program control. The Reset line from the Power-On circuitry is ORed with the program output point which allows the device attached to this port to receive a Power-On reset when the processor is reset.

2.10.1 Parallel Interface Operation

This port, when operating with an attached printer, loads the data or the printer command into its 8-bit output latches and then writes the latched data onto the printer with the strobe line generated by the processor. At this time, the program may read the input port for printer status to determine when the next character is to be strobed onto the printer, or it may interrupt to inform the program that the printer is "NOT BUSY". Since the print data are latched onto the output latches prior to actual print, the output may be looped and read back for diagnostic purposes, which allows the fault to be isolated between the interface and the attached device. The printer interface block diagram is shown in Figure 2-21.

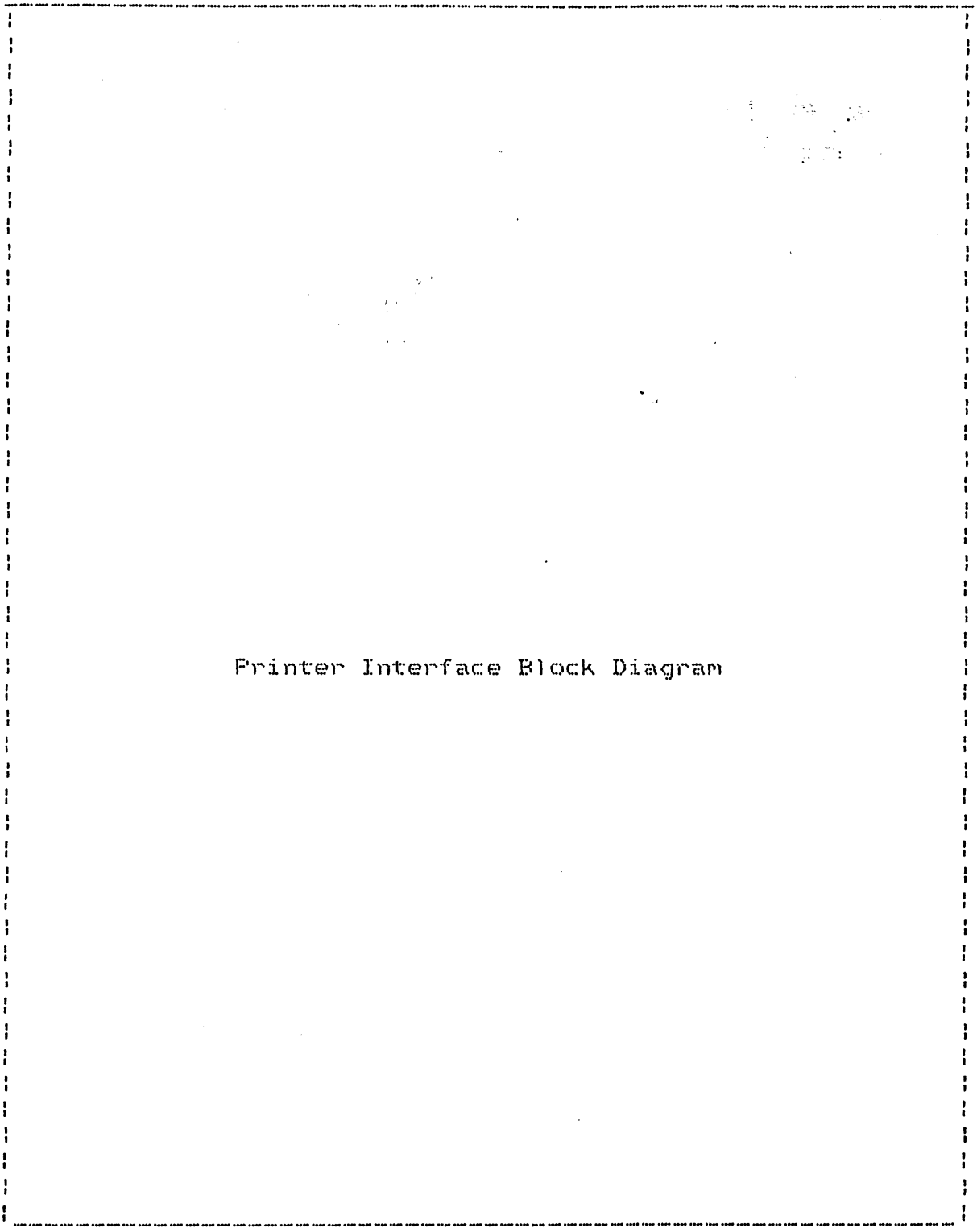


Figure 2-21: Printer Interface Block Diagram

2.10.2 Parallel Interface Connector

The Input/Output signals are made available at the 25-pin "D" shell connector J13 located on the back of the computing module. The signals are standard TTL capable of sourcing 2.6 mA and sinking 24 mA. The location of J13 is shown in Figure 2-22 and the interface signals are shown in Figure 2-23.

****** C A U T I O N ******

Care must be taken to ensure that no external device pulls any of these lines low to ground.

****

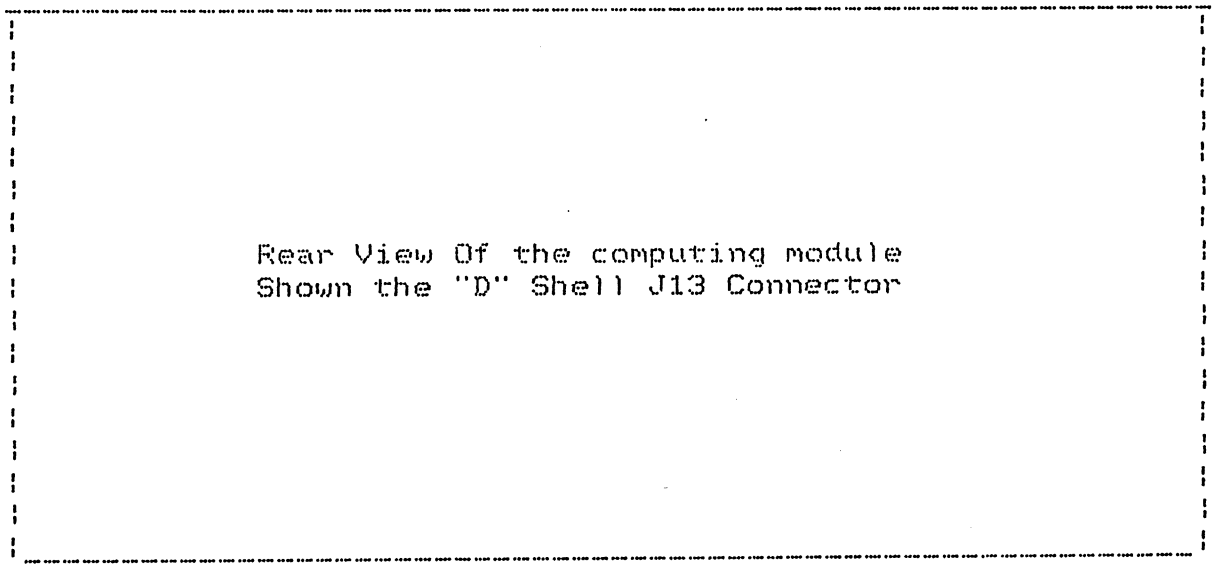


Figure 2-22: Back of Computing Module Showing J13

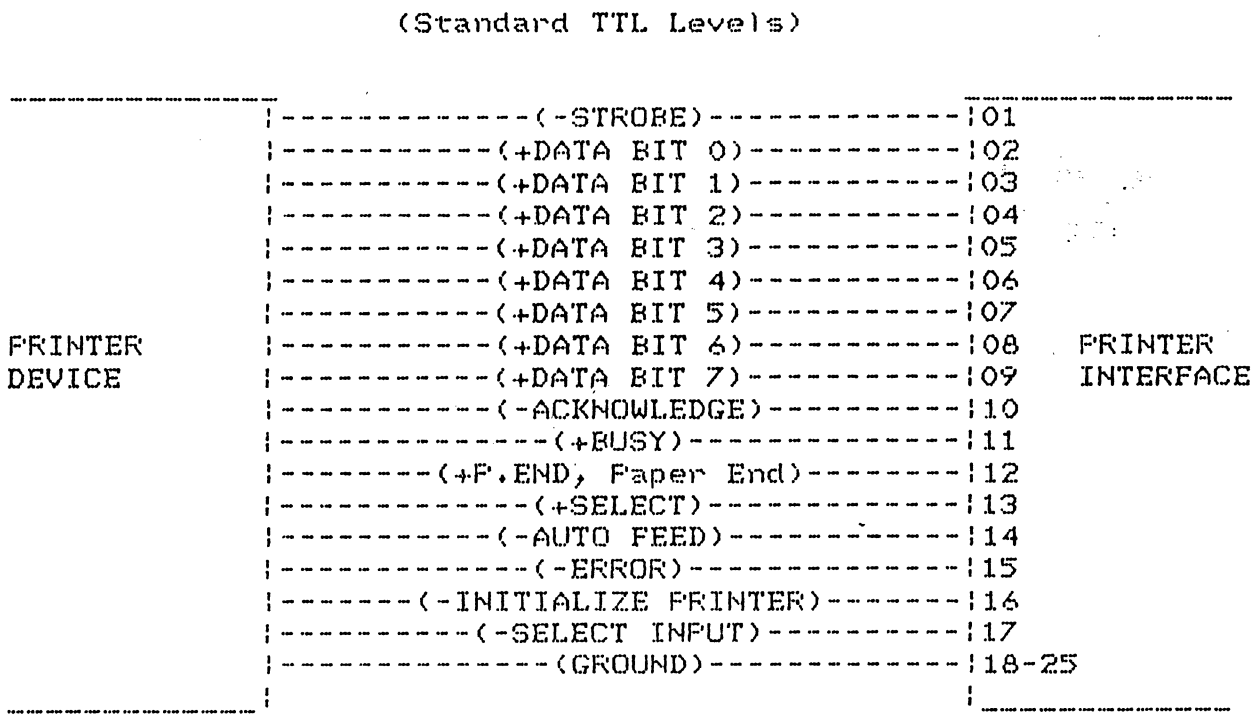
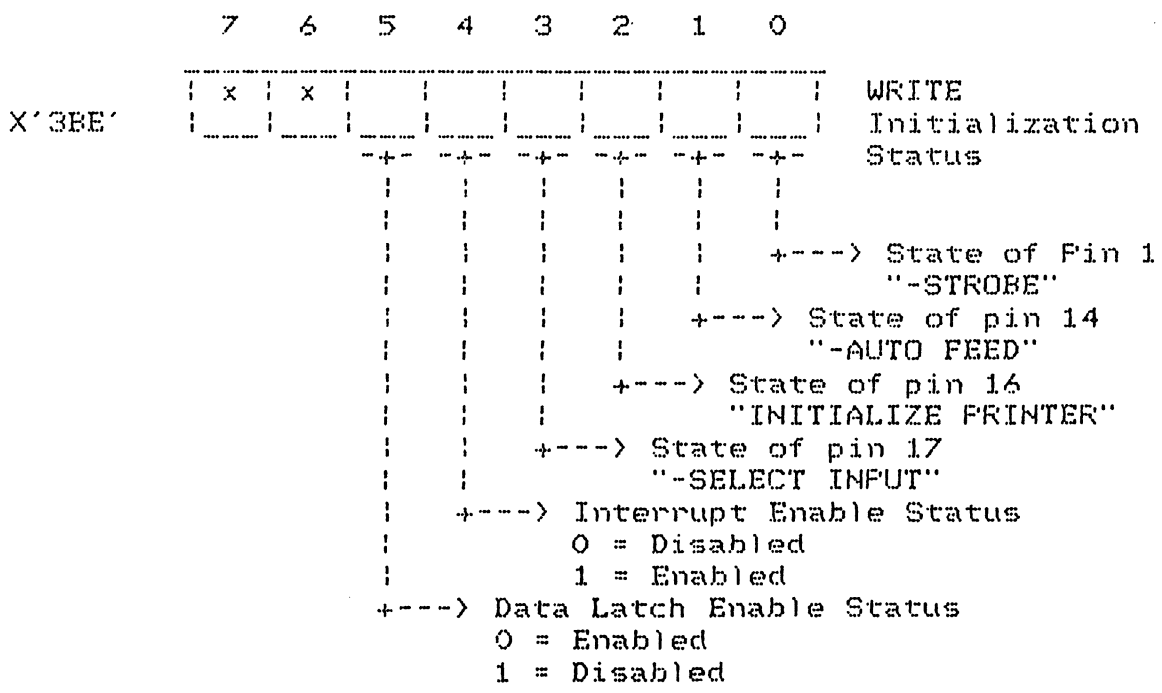


Figure 2-23: Printer & Printer Interface

2.10.3 Programming Considerations

There are five Input/Output instructions which the parallel interface responds to: two of the five I/O instructions are used for output operations and the remaining three are used for input operations. The output instructions are used for transferring data into the bus buffer and data latches, whose outputs are present on pins 18-25 of the parallel interface connector (J13). Two of the three input instructions are used by the processor to read the contents of the bus buffer and the data latches. The third input instruction is used by the processor to read the real time state of the signals on the parallel printer interface connector. For programming this port, the MAD-1 supports I/O addresses X'3BC', X'3BD', and X'3BE'. I/O addresses X'378 - X'37F' used by IBM PC/XT are not supported.

Status Register: This register is used to read status from, and write initialization status to the printer interface.



2.11 CLOCK/CALENDAR, MSM 58321 chip

The MAD-1 provides a real-time and date calendar facility using the MSM 58321 chip with back-up battery. This chip continues to operate when the system is powered off using the battery back-up system to maintain DC power. DC power will be supplied to the chip for up to five years with no other power supplied.

An 8-bit control and an 8-bit data register are used for handling the communication between the MSM 58321 and rest of the system. Since the clock/calendar facility shares the same I/O address space (X'3BC, 3BD') assigned to the parallel printer, the data latches in the Parallel Printer Interface logic must be enabled WITHOUT strobing data to the printer using the Initialization Register at I/O address X'3BE'

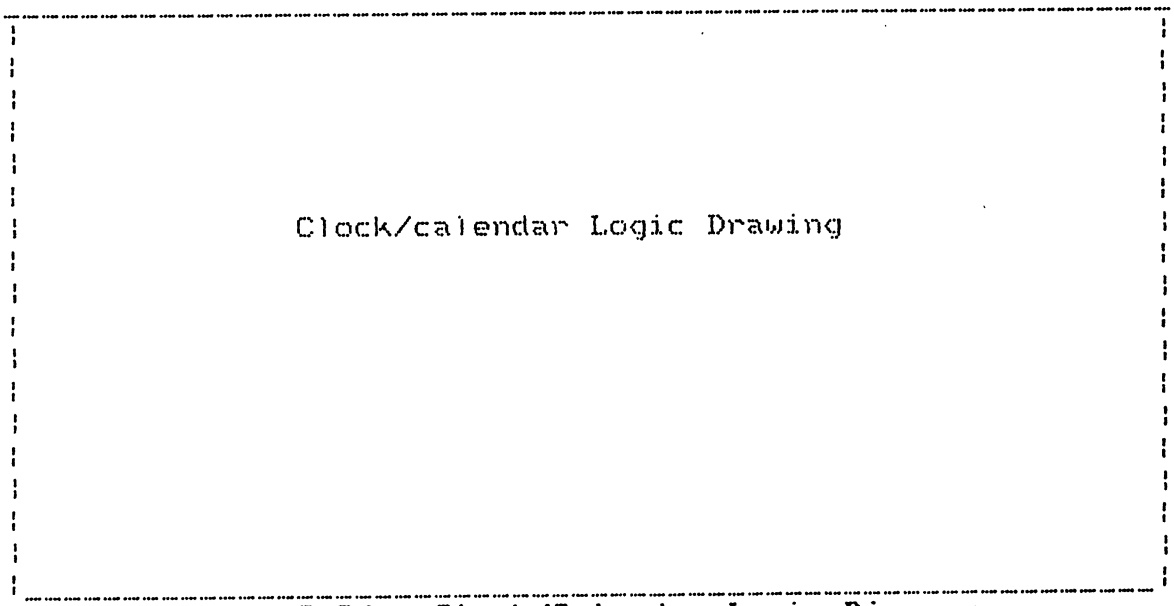
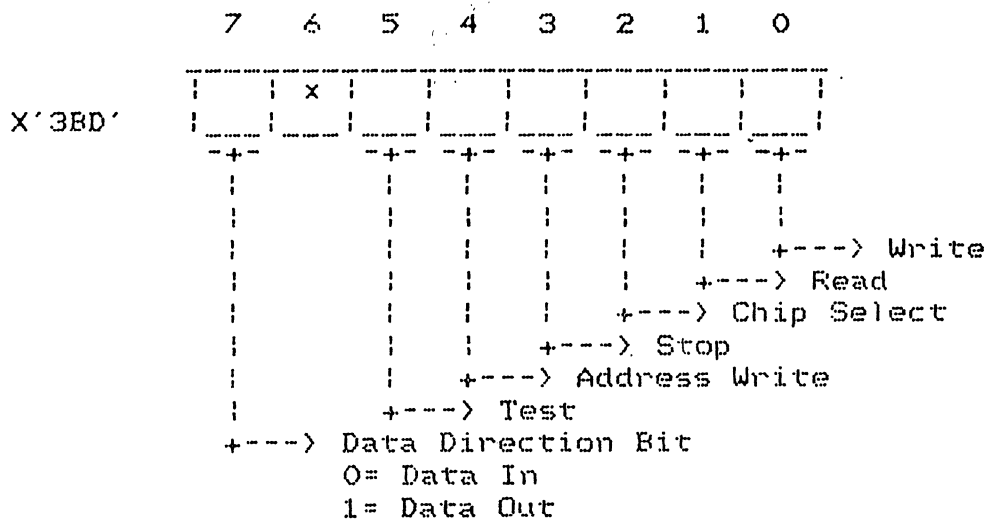


Figure 2-24: Clock/Calendar Logic Diagram

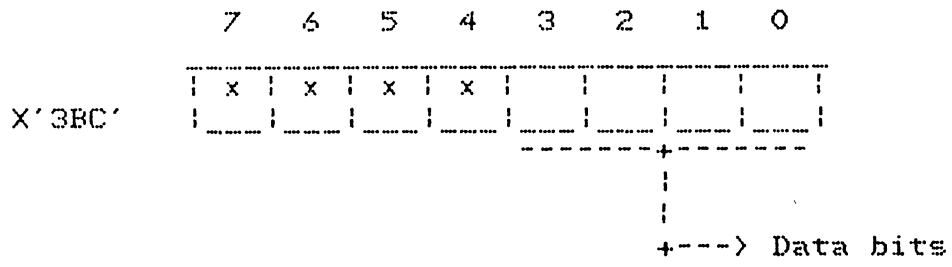
2.11.1 Clock/Calendar Registers

The clock/calendar MSM 58321 chip provides an 8-bit control register and an 8-bit data register to allow the user to set the internal counter of the chip under program control.

Clock/Calendar Control Register: This register is used by the system to write six bits of control information to I/O address area X'3BD' as shown below:



Clock/Calendar Data Register:



2.11.2 Clock/Calendar Programming Considerations

The following Table provides the translation for the values written into the data register and the internal counter, when bit 0 (Write) and bit 4 (Address Write) of the control register are set to "1".

VALUE IN DATA REG.	INTERNAL COUNTER
X'00'	Second 1's
X'01'	Second 10's
X'02'	Minute 1's
X'03'	Minute 10's
X'04'	Hour 1's
X'05'	Hours 10's
X'06'	Day of Week
X'07'	Day 1's
X'08'	Day 10's
X'09'	Month 1's
X'0A'	Month 10's
X'0B'	Year 1's
X'0C'	Year 10's

2.12 SYSTEM CONFIGURATION SWITCH

The configuration switch is an 8-bit dip switch located on the CPU board in the computing module. This switch combines the functions of the IBM PC system configuration switches as shown in the following table:

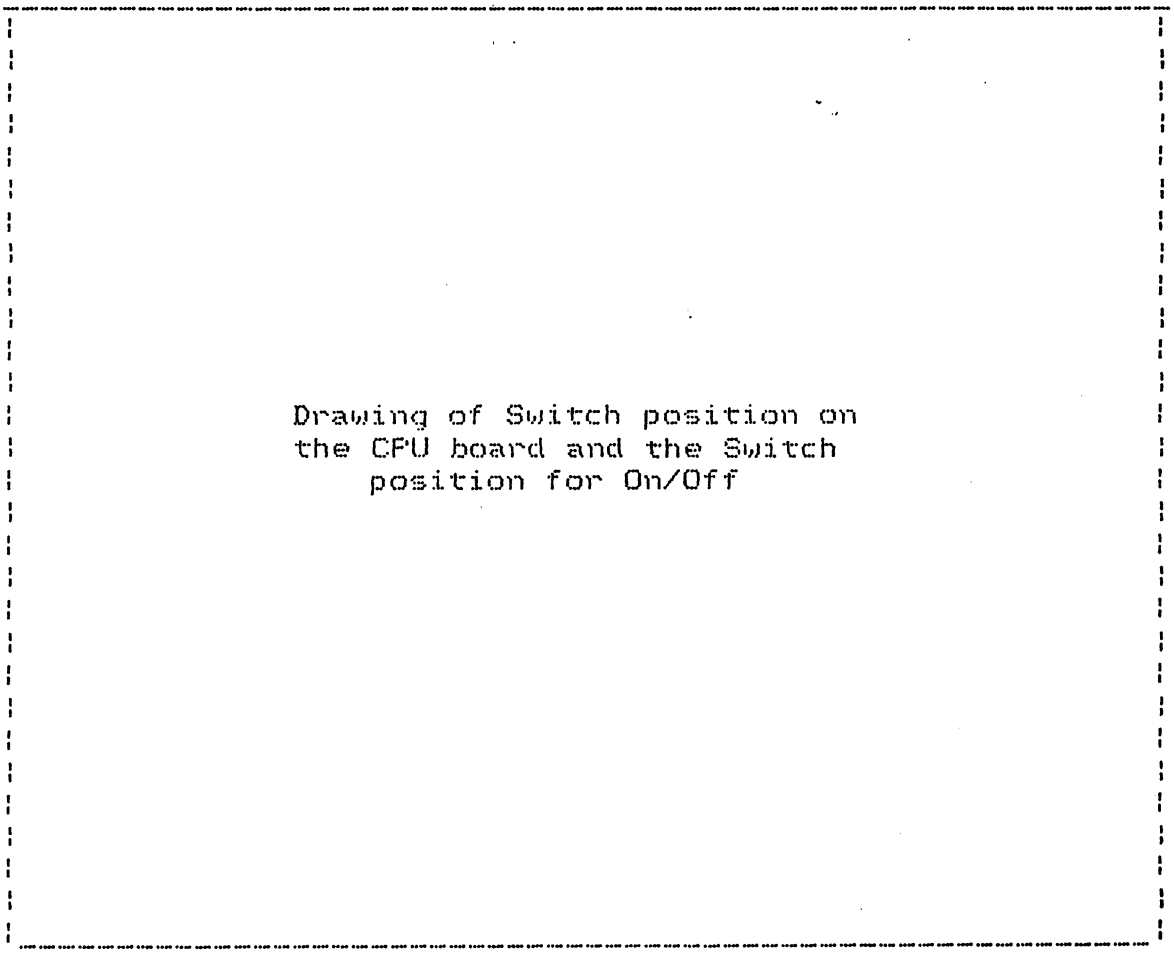


Figure 2-25: Switch Positions

SW 1:

MAD-1 - Off Position = Boot from Floppy Disk Drive
On Position = Boot from Hard Disk (if installed)
IBM PC- Off Position = Floppy Disk not installed.
On Position = Floppy Disk installed.

SW 2:

MAD-1 - Not Used (Set to On Position)
IBM PC- Off Position = Co-Processor 8087 installed.
On Position = Co-Processor 8087 not installed.

SW 3 and 4:

MAD-1 - SW 3 Off, 4 Off = Memory size 128K
SW 3 On, 4 Off = Memory size 256K
SW 3 Off, 4 On = Memory size 384K
SW 3 On, 4 On = Memory size 512K

IBM PC- SW 3 Off, 4 On = Memory size 128K
SW 3 On, 4 Off = Memory size 192K
SW 3 Off, 4 Off = Memory size 256K

SW 5 and 6:

MAD-1 - SW 5 Off, 6 Off = Monochrome Display, more than 1
SW 5 Off, 6 On = Color Display, 40 x 25 Color Mode
SW 5 On, 6 Off = Color Display, 80 x 25 Color Mode
SW 5 On, 6 On = Use COM 1 device as console

IBM PC- SW 5 Off, 6 Off = Monochrome Display, more than 1
SW 5 Off, 6 On = Color Display, 40 x 25 Color Mode
SW 5 On, 6 Off = Color Display, 80 x 25 Color Mode
SW 5 On, 6 On = No monitor installed

SW 7 and 8:

MAD-1 - SW 7 Off, 8 Off = One Floppy Drive installed.
SW 7 Off, 8 On = Two Floppy Drives installed.
SW 7 On, 8 Off = Three Floppy Drives installed.
SW 7 On, 8 On = Four Floppy Drives installed.

IBM PC- SW 7 Off, 8 Off = One Floppy Drive installed.
SW 7 Off, 8 On = Two Floppy Drives installed.
SW 7 On, 8 Off = Three Floppy Drives installed.
SW 7 On, 8 On = Four Floppy Drives installed.

Shouldn't this be in the IBM delta section? (only give MAD switch settings here)

Index

what about secondary?

Table of Contents

Chapter 3

VIDEO CONTROL AND DISPLAY

This chapter contains the physical, functional, and operational descriptions for the video control and video display used in the MAD-1.

3.1 PHYSICAL DESCRIPTION

The video control board is used in conjunction with the CPU board to provide video control signals and data for the monochrome and color/graphics display module.

It is a 5 1/4" by 14" four layer printed circuit board (see Figure 3-1) which mounts on a short bracket above the CPU board in the computing module. Power supply voltages and control signals are supplied through two connectors: the main bus connector and an auxiliary connector used for expanding the I/O bus data to 16-bit data bus.

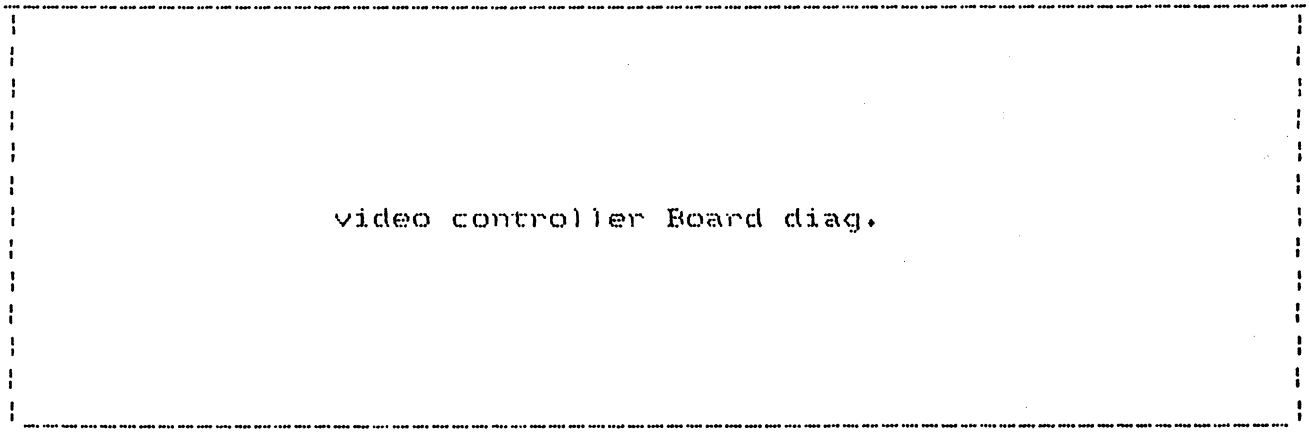


Figure 3-1: Video Controller Board

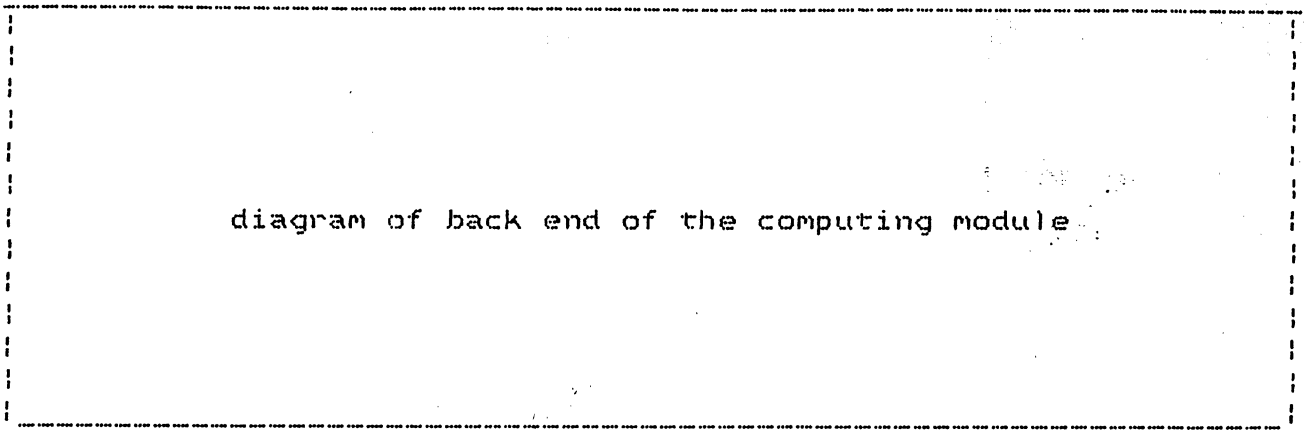


Figure 3-2: Back of Computing Module

Output video control signals generated on this board are carried to the video board unit via the 9-pin "D" shape connector (J10). Figure 3-2 shows the connectors on the back of the computing module and Table 3-1 provides the pin list:

Table 3-1: Pin List and Signal Name

Video Signal Connector (J10)	
Pin #	Signal Name
1	GND
* 2	Vertical Sync
3	Red
4	Green
5	Blue
6	Intensity
7	Monochrome Signal
8	Horizontal
9	Vertical Sync

*: Switch selectable:
a) Composite Sync via selecting jumper W-9
b) Ground via selecting jumper W-10

Note: The signals are driven with low-power-schottkey, and support one load at the output. Certain address lines may have up to a maximum of two loads.

3.2 FUNCTIONAL DESCRIPTION

The video display controller combines the functions of both the monochrome and color/graphics display adapters, except that it does not provide composite color video.

Note: Simultaneous monochrome and color/graphics are not supported.

Five modes of operation are supported by the video board. They include the monochrome alphanumeric supporting an 80 column by 25 line display screen, two color alphanumeric modes, one at 80 x25 and the other at 40 x 25, a medium resolution graphic screen at 320 x 200 , and a high resolution screen at 640 x 200. The monochrome and color/graphics modes are selected via different I/O address spaces (monochrome by X'3B4' thru X'3BF', color/graphics by X'3D4' thru X'3DF'). Both address spaces are supported on the bus and decoded by the video display board. For a quick reference, the summary of the video display modes is listed below:

MODE	CHARACTER CELL	COLUMNS X LINES
Monochrome Alphanumeric	9 x 14	80 x 25
Color Alphanumeric	8 x 8	40 x 25
Color Alphanumeric	8 x 8	80 x 25
Medium Resolution Graphics		320 x 200
High Resolution Graphics		640 x 200

Figure 3-3 shows the functional block diagram for the video display board. A complete description of the registers and memory layout are shown in the following figure.

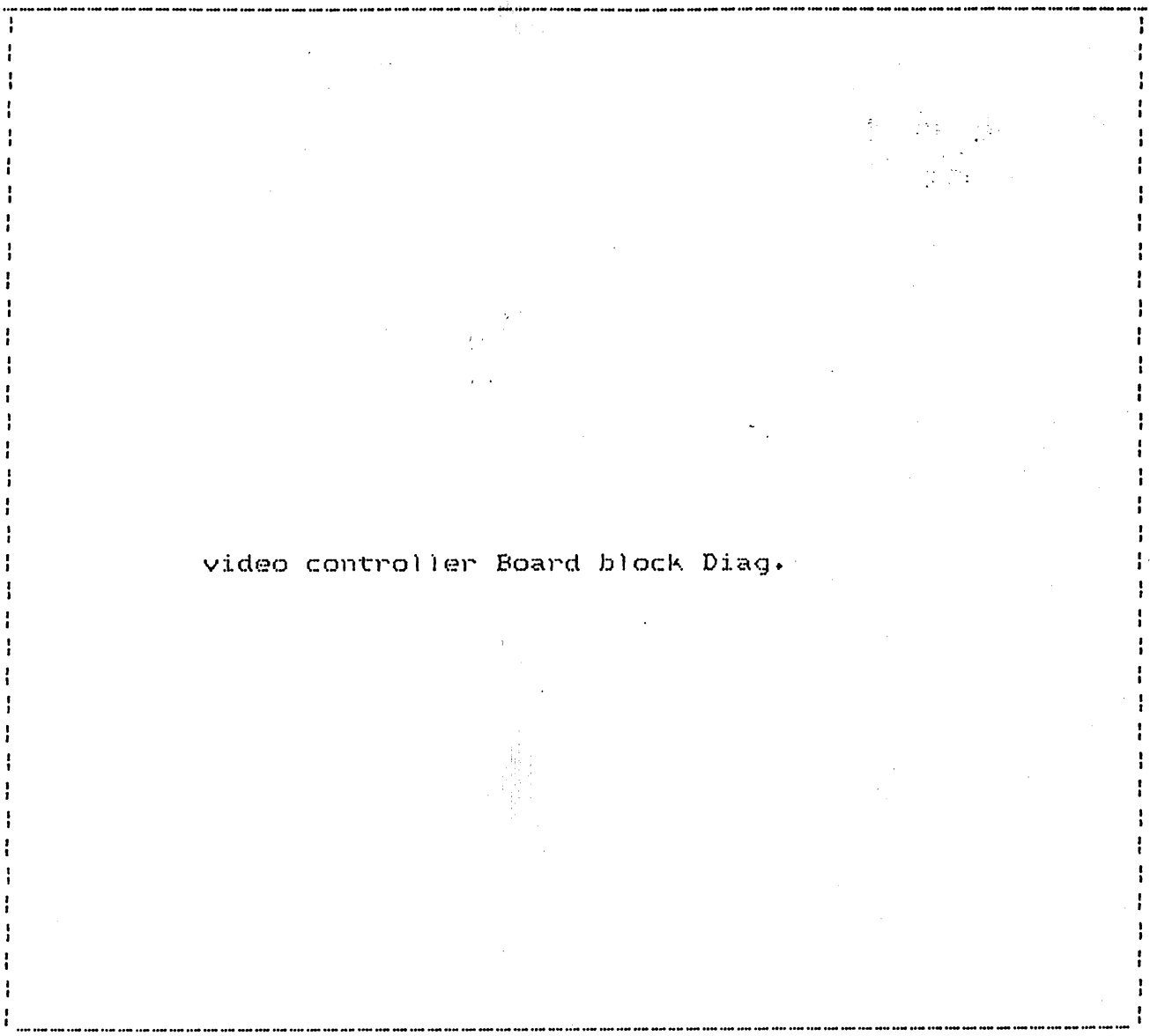


Figure 3-3: Functional Block Diagram

3.2.1 Video Memory Map

The video controller board is designed around the Motorola 6845 CRT controller with 16K bytes of static RAM (no parity bit) used for buffering alphanumeric data and as a bit-map for graphics data. Two consecutive bytes, character and its attribute can be written to the display buffer in 835 nsec, providing a data rate of 1.2 mega bytes/second. Figure 3-4 shows the memory map of the 16 Kbyte static RAM.

Note: The memory map used for monochrome display is located in different address than the memory map used for the color display.

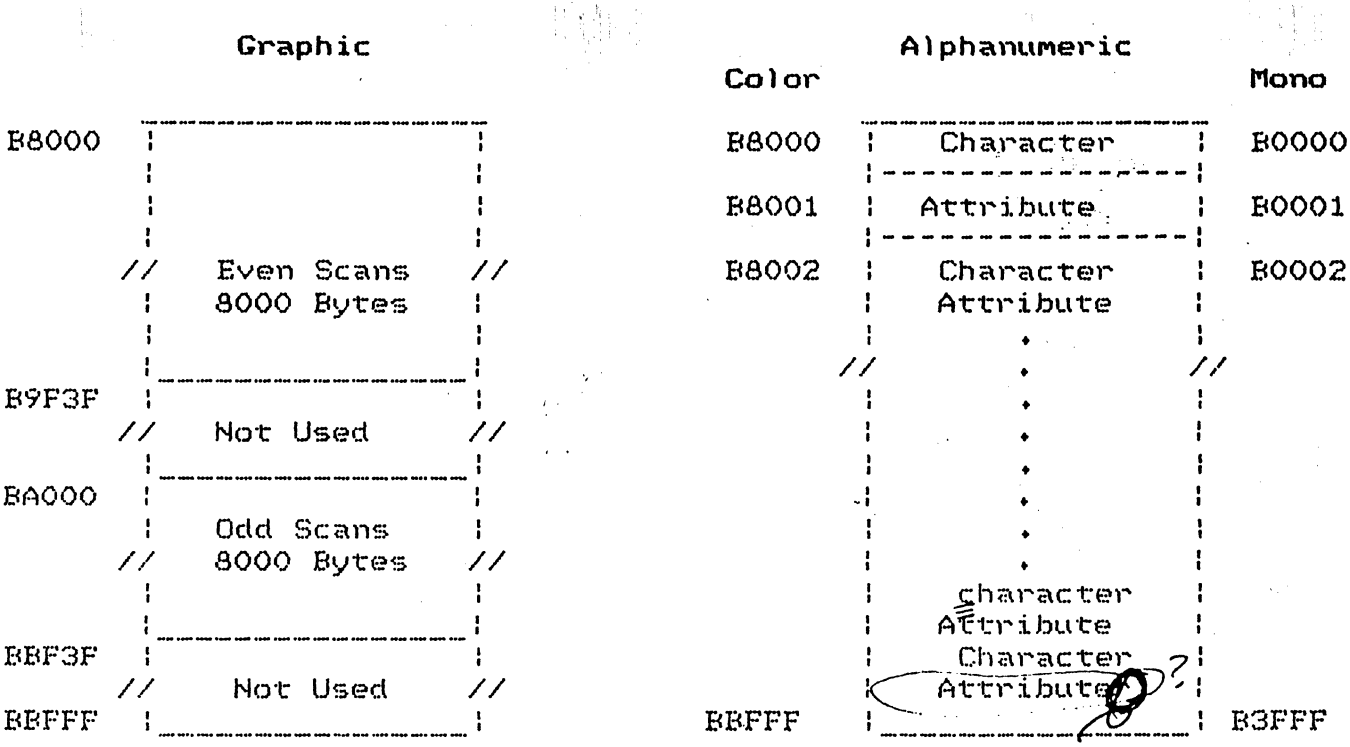


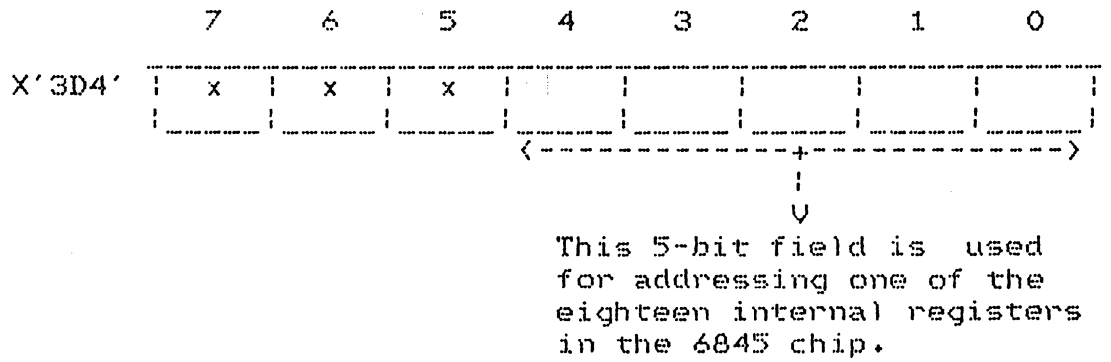
Figure 3-4: Memory Map

3.2.2 Registers

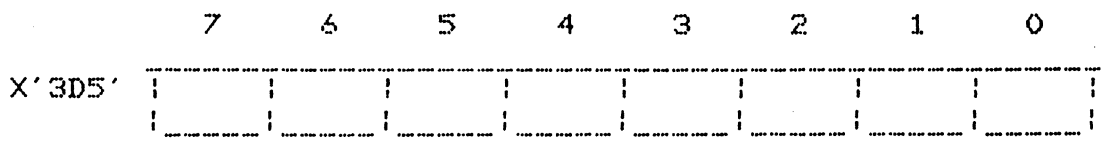
The Motorola 6845 CRT controller provides two 8-bit registers which are used for external interface logic (external to the chip itself). One of the registers, the index register, is used to select one of the eighteen internal registers in the 6845 controller chip. The index register is also addressable by the program, address X'3D4', for compatibility with programs which address the IBM PC color/graphic display. The second register is used as a data register. The data register is also addressable by program with an address X'3D5' (for compatibility with software).

In addition to the two registers provided by the CRT controller chip, the video display controller provides three more registers; the mode control register, the color select register, and the status register. These three registers are addressable with addresses X'3D8', X'3D9', X'3DA' (for compatibility with programs addressing the IBM PC monochrome display).

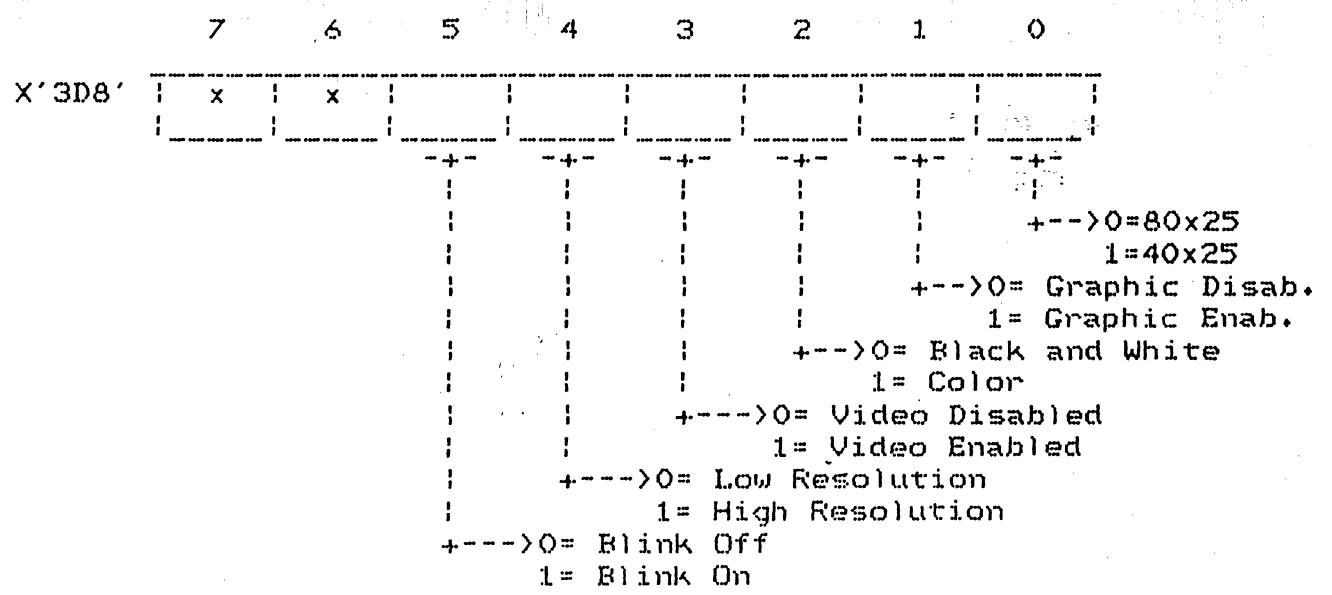
6845 Index Register: This address is used for monochrome display.



6845 Data Register: This address is used for monochrome display.

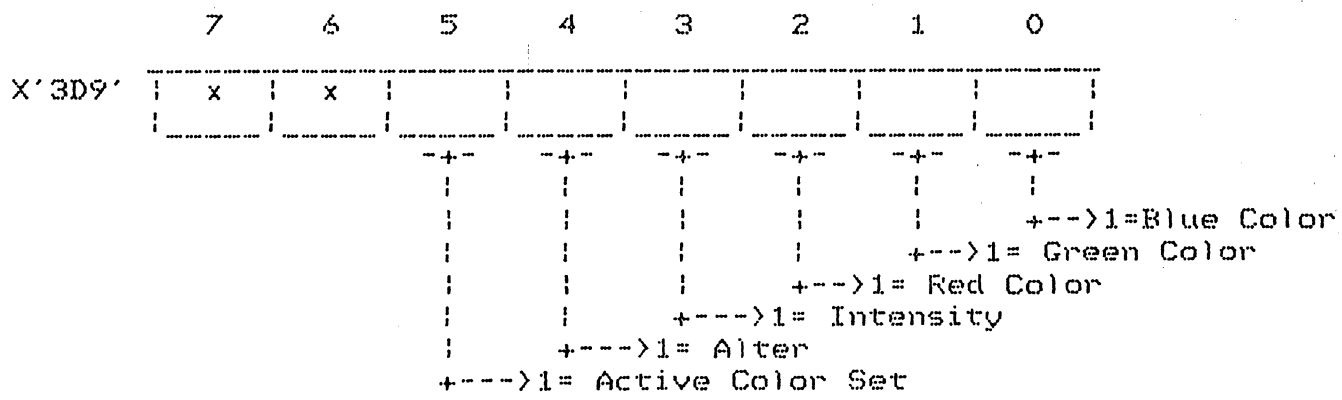


Video Mode Register Control:



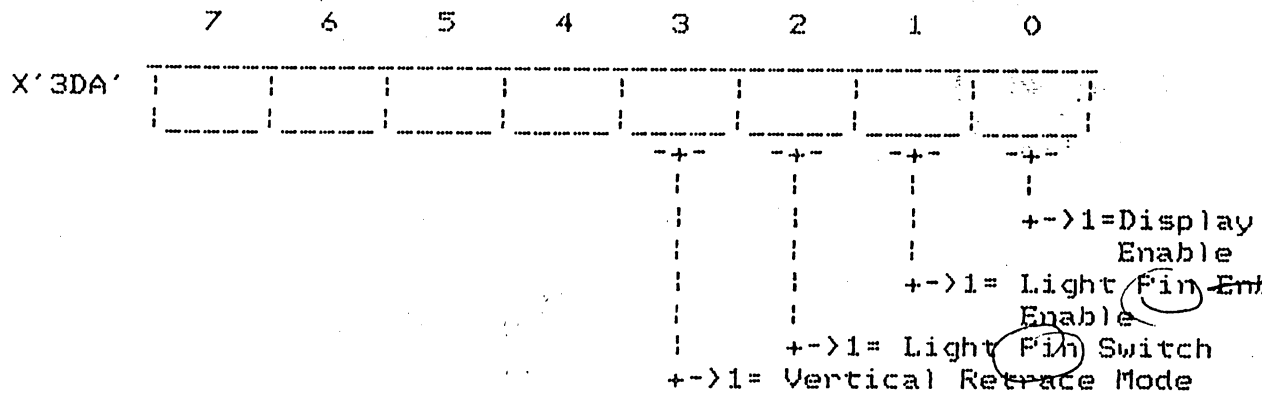
Address X'3B8' for Monochrome Display

Color Select Register:



Address X'3B9' for Monochrome Display

Status Register: This address used for monochrome display.



Note: The Light Pen Trigger Flip-Flop will be cleared by writing any data to location X'3DA'.

No light pen!

3.2.3 Programming Consideration

The parameters shown in the following table are for the internal registers of the Motorola 6845 CRT controller chip when used to operate the monochrome display. When the 6845 internal registers are used to operate the monochrome display, certain parameters must be followed. Table 3-2 lists the monochrome parameters:

Table 3-2: Monochrome Programming Parameters

Register	Function	Program Unit	Display Addr.
R0	Horizontal Total	characters	X'61'
R1	Horizontal Display	characters	X'50'
R2	Horizontal Sync Position	characters	X'52'
R3	Horizontal Sync Width	characters	X'0F'
R4	Vertical Total	characters	X'19'
R5	Vertical Total Adjust	Scan Line	X'06'
R6	Vertical Displayed	character Row	X'19'
R7	Vertical Sync Position	character Row	X'19'
R8	Interlace Mode	- - - - - -	X'02'
R9	Max. Scan Line Addr.	Scan Line	X'0D'
R10	Cursor Start	Scan Line	X'0B'
R11	Cursor End	Scan Line	X'0C'
R12	Start Address (H)	- - - - - -	X'00'
R13	Start Address (L)	- - - - - -	X'00'
R14	Cursor (H)	- - - - - -	X'00'
R15	Cursor (L)	- - - - - -	X'00'
R16	Reserved	- - - - - -	- -
R17	Reserved	- - - - - -	- -

To properly initialize the computer, the first command must set bit 4 of the mode control register (address X'3D8') to a value of '1'. This value selects the high resolution mode, and if not set, causes the processor not to operate, resulting in the processor not accessing the monochrome mode.

character Rom

The video display controller board ~~also~~ supports 256 characters, ~~and their associated attributes.~~ The memory bytes ~~containing~~ the characters are located in the even addresses of the display character ~~buffer~~ and the attribute bytes in the odd address, as shown in Figure 3-4. The attribute code is shown in Figure 3-5 and Table 3-3 contains the monochrome attribute map.

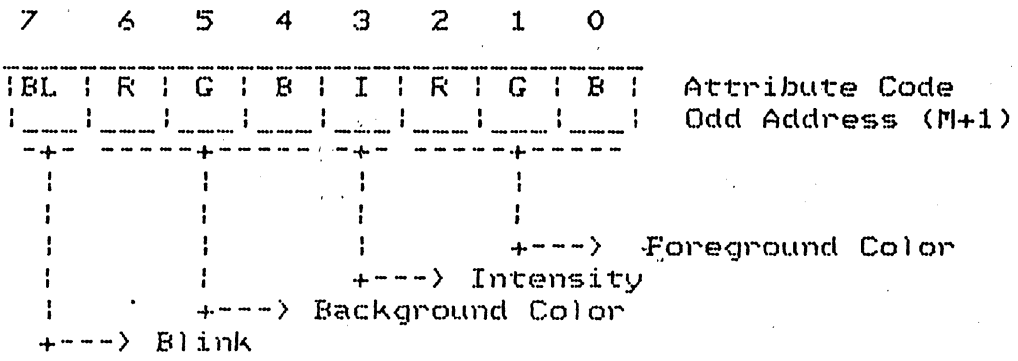


Figure 3-5: Attribute Code

Table 3-3: Monochrome Attribute Map

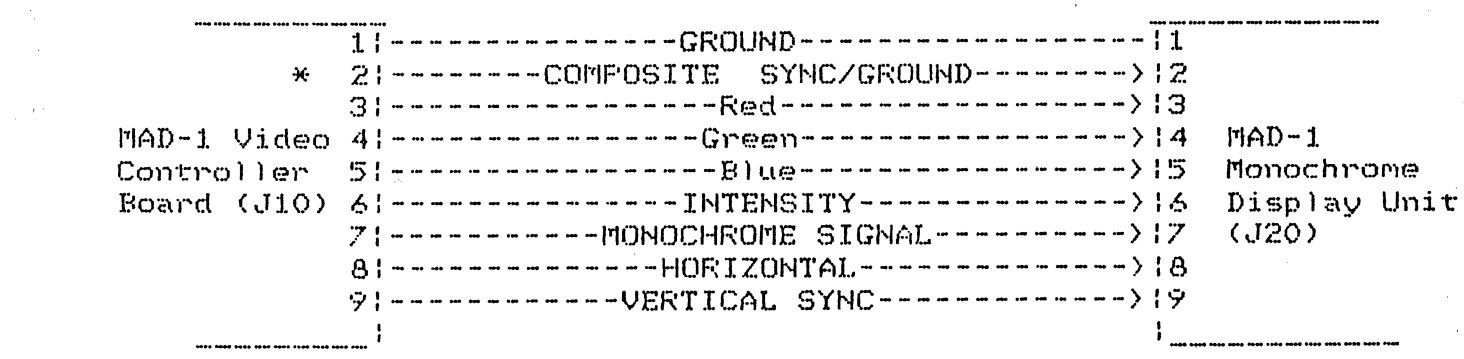
Background R G B	Foreground R G B	Function
0 0 0	0 0 0	None-Display
0 0 0	0 0 1	Underline
0 0 0	1 1 1	White Char/Black Bkgnd
1 1 1	0 0 0	Reverse Video

3.3 MONOCHROME DISPLAY

The MAD-1 monochrome display terminal is a high resolution CRT supporting green or an optional amber screen. The display screen is capable of displaying 25 lines of information with each line containing up to 80 characters. The electronics of the terminal are packaged in a low profile, compact enclosure that allows the monochrome terminal to be stacked on top of the data and/or computing module, or to sit separately. The angle of the display screen can be adjusted via a sliding lever attached to the back of the CRT enclosure.

3.3.1 Physical Description

The MAD-1 monochrome display is a low profile, lightweight, ergonomically designed CRT. Its control logic is received via a 9-pin 'D' type connector (J10) from the video controller board in the computing module. Power and ground signals are sent from the data module, connector J4, and received at the J21 connector on the display module (located on the back end of the display unit). Figure 3-6 shows the interface control signals from the computing module:



*: Used as a composite sync, when selecting jumper W-9
Used as a Ground signal, when selecting jumper W-10

Figure 3-6: Video Control Interface Signals

3.3.2 Functional and Operational Description

The actual character code and its attribute are generated by the video board located in the computing module and are driven over a cable to the CRT terminal for display. Characters on the screen are displayed by the proper formation of picture elements (dots) in a character box measuring 14 dots high by 9 dots wide. The screen is refreshed with the frequency of 50 Hz at the rate of 350 lines of vertical resolution and 720 lines horizontal resolution. The display intensity can be adjusted by a thumb switch located at the back of the CRT, next to connectors J20 and J21.

The 120 AC and 60 Hz power for the monochrome CRT, and the analog electronics are supplied by the data module through connector J21. The monochrome display is selected by software when I/O addresses X'3BE' - X'3BF' are used in addressing the display memory map.

Functional and operational characteristics of the monochrome display are given in the following list:

SCREEN:

- High-Persistence green phosphor.
- Etched surface to reduce glare.
- Screen size of 80 by 25 characters.
- Character box of 14 by 9 dots.
- Character six of 9 by 7 dots.

VIDEO SIGNAL:

- Maximum Bandwidth of 16.257 MHz.

VERTICAL DRIVE:

- Screen refresh at 50 Hz with 350 lines of vertical resolution and 720 lines of horizontal resolution.

HORIZONTAL RESOLUTION:

- Positive level, TTL compatibility at a frequency of 18.432 KHz.

3.4 COLOR DISPLAY

In addition to monochrome display support, the MAD-1 Workstation also supports the attachment of color display/graphic terminals. Since the memory map addresses used for the color display/graphics are identical to those used by IBM, all color terminals supported by the IBM PC/XT are also supported by the MAD-1 Workstation (See Appendix C for the system memory map).

The color display option on the MAD-1 is selected via software, using I/O addresses X'3DE' and X'3DF. Connection for the color CRT is made through the same ports used for the monochrome display.

The operational characteristics of the color display/graphics terminals supported by the MAD-1 are given in the following list:

SCREEN:

- o High contrast black screen.
- o Displays up to 16 colors.
- o Characters defined in an 8 by 8 matrix.

VIDEO SIGNAL:

- o Maximum Video Bandwidth of 14 MHz.
- o Red, Green, and Blue video signals and intensity are independent.

VERTICAL DRIVE:

- o Screen refresh at 60 Hz with 200 lines of vertical resolution.

HORIZONTAL DRIVE:

- o Positive level, TTL compatible at a frequency of 15.75 KHz.

delete underline

Chapter 4

KEYBOARD MODULE

4.1 PHYSICAL DESCRIPTION

Both the MAD-1 display and keyboard modules are designed to meet European ergonomic and DIN standards. The keyboard itself is a lightweight design built with approximately a 15 degree angle palm rest for comfort and convenience. Figure 4-1 provides a graphic layout of the 85-key keyboard:

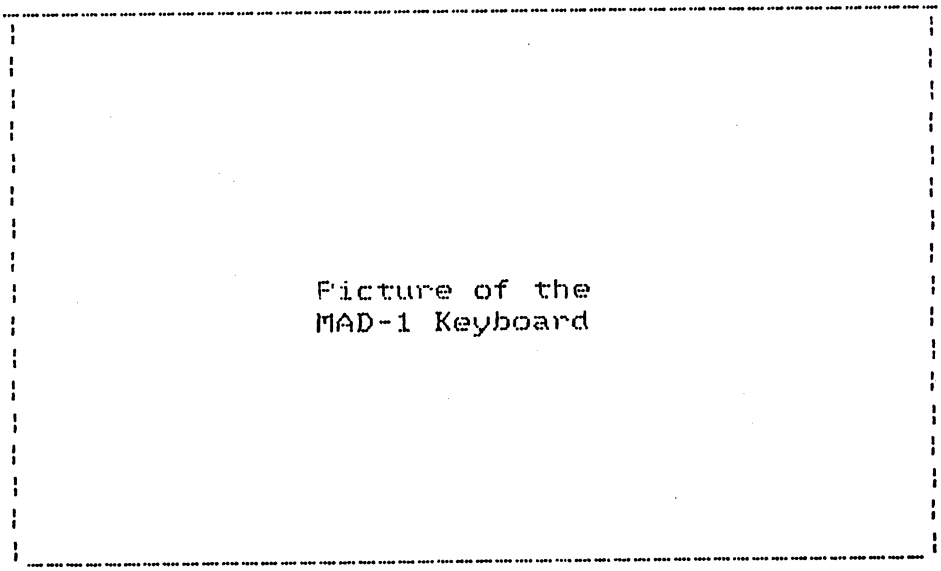


Figure 4-1: MAD-1 Keyboard

4.1.1 Physical Key Location

The MAD-1 keyboard contains 85 keys as compared to the 83 keys supported on the IBM PC/XT. The two additional keys are locations 31, [BREAK] key and 84, [,]. Each key is coded with a location number to provide an easy reference point and is also used in referencing the scan codes. Figure 4-2 shows the keyboard with the assigned location numbers:

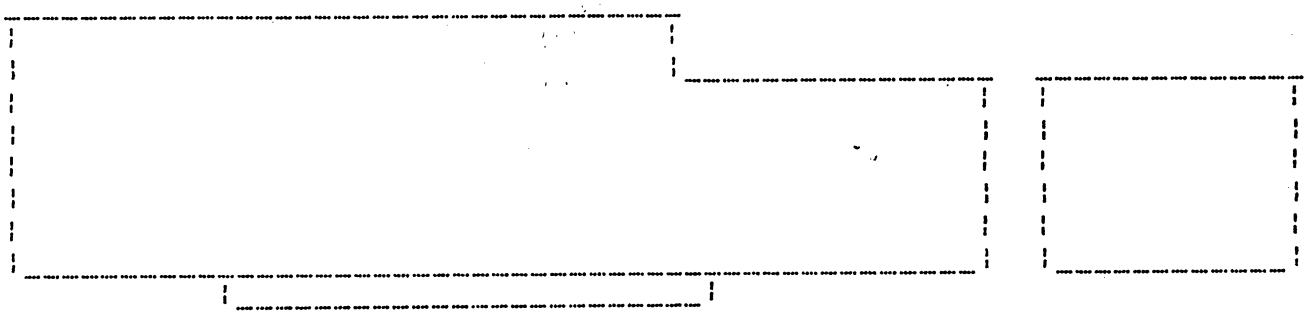


Figure 4-2: Keyboard Diagram Showing Location Numbers

4.1.2 Keyboard Connector Interface

The keyboard interface logic is located on the CPU board in the computing module. Signals are received over a six foot coiled flexible cable from connector J7 on the computing module to a telephone type connector on the back of the keyboard. Figure 4-3 shows the J7 connection on the computing module and Figure 4-4 provides the pin assignments of the coiled cable:

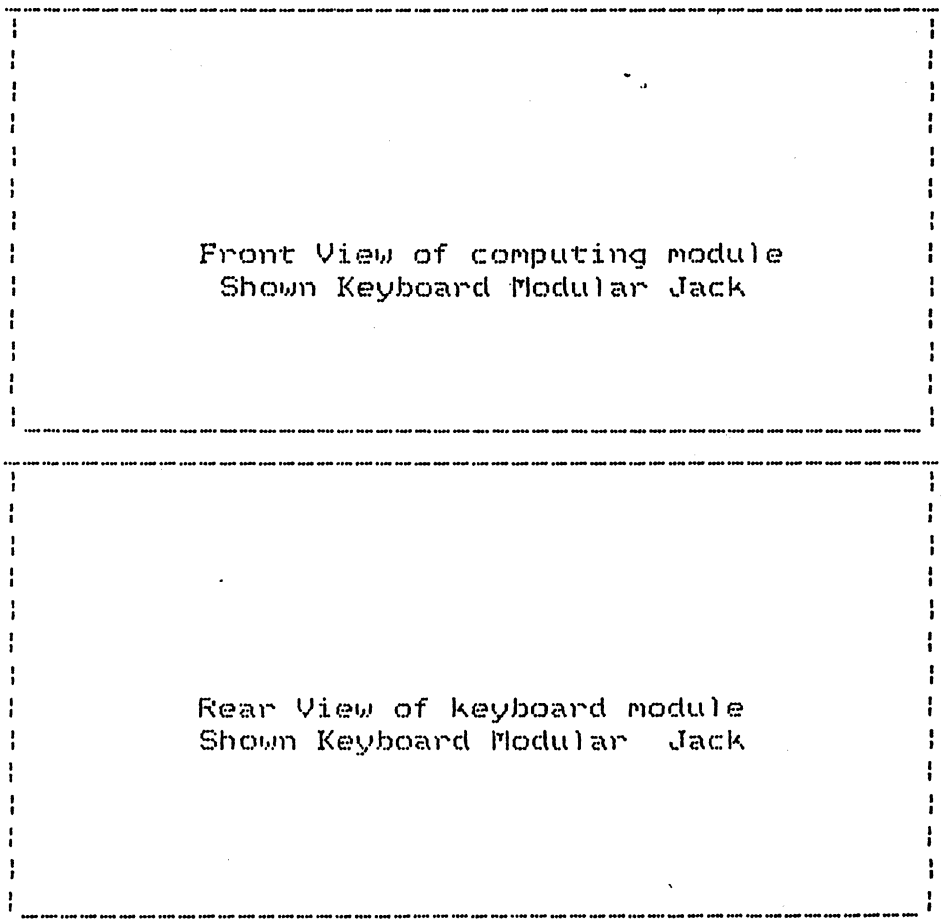


Figure 4-3: Interface Connectors

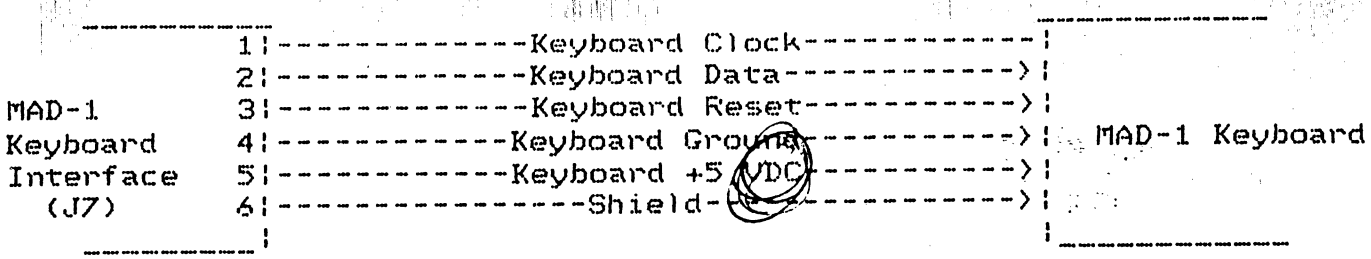


Figure 4-4: Pin Assignments

4.2 FUNCTIONAL DESCRIPTION

The 85 keys on the MAD-1 keyboard can be functionally divided into the following four groups:

1) Standard typewriter keys.
2) Numeric key pad arranged in standard calculator fashion.
3) Fixed function keys.
4) Programmable function keys.

The design of the keyboard interface provides for the return of scan codes rather than ASCII codes. The ability to receive scan codes rather than ASCII codes provides greater flexibility in defining keyboard operations. When a scan code is received, an IRQ1 interrupt is generated and the keyboard circuitry converts the serial data to parallel data. The parallel data is then sent onto port 'A' of the Intel 8255 programmable peripheral interface chip located on the CPU board. The keyboard interface diagram is shown in Figure 4-5.

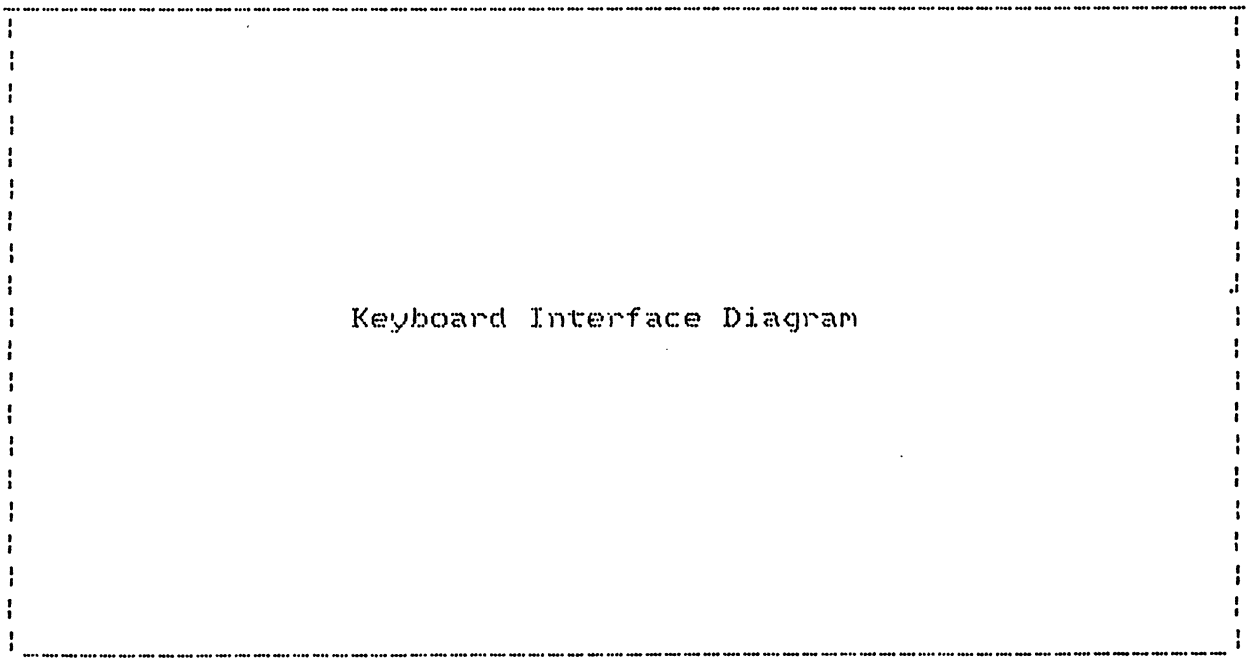


Figure 4-5: Keyboard Interface Diagram

The design of the keyboard is based on the Intel 8048 microprocessor. Supported functions include:

- Keyboard scanning.
- Buffering up to 16 scan-codes.
- Maintaining bi-directional serial communication with Central Processing Unit.
- Executing Hand-Shake protocol on each scan-code transfer.
- Power-on self test, checks keyboard ROM

The logic diagram of the keyboard module is shown in Figure 4-6.

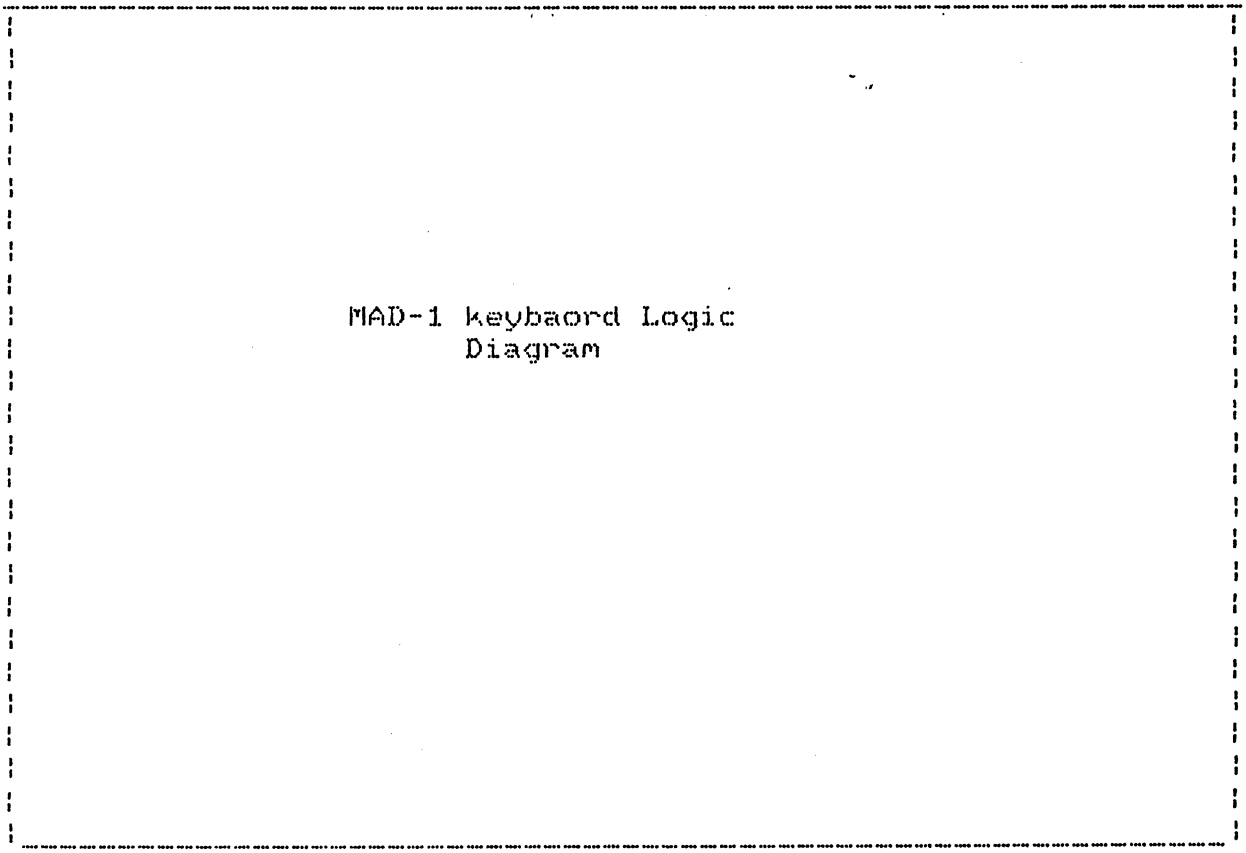


Figure 4-6: Keyboard Logic Diagram

4.2.1 Keyboard Buffer

The keyboard module has a 64-byte type-ahead buffer that is filled when the operator is entering data and the main processor is interrupted to attend to another task. Once the processor has finished the other task, it will return to process the characters stored in the type-ahead buffer.

4.2.2 Keyboard Scan Code

The design of the MAD-1 keyboard is based on the concept of scan codes rather than ASCII codes. This provides the user with the maximum flexibility for defining the functional operation of certain keys. All keys on the keyboard generate a unique pair of scan codes rather than conventional ASCII codes. These codes are returned to the keyboard interface logic located on the CPU board in the computing module.

Codes generated by each key are defined as "MAKE" or "BREAK" codes. For example; when key number 64 (RETURN Key) is pressed, it is considered a MAKE and generates a X'1C' code. When released, it is considered a BREAK and generates a X'9C' code. The hex value of the BREAK code is X'80' plus the hex value generated by the MAKE code of the same key.

The following figure shows the key location numbers followed by the scan code of each key in Table 4-1.

Figure 4-7: Keyboard Diagram Showing Key Location Numbers

Table 4-1: Keyboard Scan Codes

KEY LOCATION	SCAN CODE (Hex) BREAK	MAKE	KEY FUNCTION(S)
1	3B	BB	Function Key F1
2	3C	BC	Function Key F2
3	3D	BD	Function Key F3
4	3E	BE	Function Key F4
5	3F	BF	Function Key F5
6	40	C0	Function Key F6
7	41	C1	Function Key F7
8	42	C2	Function Key F8
9	43	C3	Function Key F9
10	44	C4	Function Key F10
11	01	81	"ESC" Escape Key
12	2B	AB	"\" Lower Case and "|" Upper Case
13	02	82	"1" Lower Case and "!" Upper Case
14	03	83	"2" Lower Case and "@" Upper Case
15	04	84	"3" Lower Case and "#" Upper Case
16	05	85	"4" Lower Case and "$" Upper Case
17	06	86	"5" Lower Case and "%" Upper Case
18	07	87	"6" Lower Case and "^" Upper Case
19	08	88	"7" Lower Case and "&" Upper Case
20	09	89	"8" Lower Case and "*" Upper Case
21	0A	8A	"9" Lower Case and "(" Upper Case
22	0B	8B	"0" Lower Case and ")" Upper Case
23	0C	8C	"-" Lower Case and "_" Upper Case
24	0D	8D	"=" Lower Case and "+" Upper Case
25	29	A9	"`" Lower Case and "~" Upper Case
26	0E	8E	"BACK SPACE" Key
27	47	C7	"HOME" When "NUM LOCK" key Pressed On "7" When "NUM LOCK" key Pressed Off
28	48	C8	Up Arrow, When "NUM LOCK" Pressed On "8" When "NUM LOCK" key Pressed Off
29	49	C9	"PGUP" When "NUM LOCK" Pressed On "PGUP" When "NUM LOCK" Pressed Off
30	4A	CA	"-" With or without "NUM LOCK" Key

(Continued)

Table 4-1 continued:

KEY LOCATION	SCAN CODE (Hex) BREAK	MAKE	KEY FUNCTION(S)
31	55	D5	"BRK" Break Key
32	0F	8F	"TAB" Key
33	10	90	"q" Lower Case and "Q" Upper Case
34	11	91	"w" Lower Case and "W" Upper Case
35	12	92	"e" Lower Case and "E" Upper Case
36	13	93	"r" Lower Case and "R" Upper Case
37	14	94	"t" Lower Case and "T" Upper Case
38	15	95	"y" Lower Case and "Y" Upper Case
39	16	96	"u" Lower Case and "U" Upper Case
40	17	97	"i" Lower Case and "I" Upper Case
41	18	98	"o" Lower Case and "O" Upper Case
42	19	99	"p" Lower Case and "P" Upper Case
43	1A	9A	"[" Lower Case and "{" Upper Case
44	1B	9B	"]" Lower Case and "}" Upper Case
45	46	C6	"SCROL/LOCK" Key
46	4B	CB	Left Arrow, When "NUM LOCK" Pressed On
			"4" When "NUM LOCK" Pressed Off
47	4C	CC	"SRCH" When "NUM LOCK" Pressed On
			"5" When "NUM LOCK" Pressed Off
48	4D	CD	Right Arrow, When "NUM LOCK" Pressed On
			"6" When "NUM LOCK" Pressed Off
49	45	C5	"NUM LOCK" Key
50	4E	CE	"+" With or Without "NUM LOCK" Pressed
51	3A	BA	"CAPS LOCK" Key
52	1D	9D	"CTRL" Control Key
53	1E	9E	"a" Lower Case and "A" Upper Case
54	1F	9F	"s" Lower Case and "S" Upper Case
55	20	A0	"d" Lower Case and "D" Upper Case
56	21	A1	"f" Lower Case and "F" Upper Case
57	22	A2	"g" Lower Case and "G" Upper Case
58	23	A3	"h" Lower Case and "H" Upper Case
59	24	A4	"j" Lower Case and "J" Upper Case
60	25	A5	"k" Lower Case and "K" Upper Case
61	26	A6	"l" Lower Case and "L" Upper Case
62	27	A7	";" Lower Case and ":" Upper Case
63	28	A8	"'" Lower Case and (") Upper Case

(Continued)

Table 4-1 continued:

KEY LOCATION	SCAN CODE (Hex) BREAK	MAKE	KEY FUNCTION(S)
64	1C	9C	"RETURN" Key
65	4F	CF	"END" When "NUM LOCK" Pressed On "1" When "NUM LOCK" Pressed Off
66	50	D0	Down Arrow, When "NUM LOCK" Pressed On "2" When "NUM LOCK" Pressed Off
67	51	D1	"PGDN" When "NUM LOCK" Pressed On "3" When "NUM LOCK" Pressed Off
68	38	B8	"ALT" Key
69	2A	AA	"SHIFT" Key
70	2C	AC	"z" Lower Case and "Z" Upper Case
71	2D	AD	"x" Lower Case and "X" Upper Case
72	2E	AE	"c" Lower Case and "C" Upper Case
73	2F	AF	"v" Lower Case and "V" Upper Case
74	30	B0	"b" Lower Case and "B" Upper Case
75	31	B1	"n" Lower Case and "N" Upper Case
76	32	B2	"m" Lower Case and "M" Upper Case
77	33	B3	"," Lower Case and "<" Upper Case
78	34	B4	"." Lower Case and ">" Upper Case
79	35	B5	"/" Lower Case and "?" Upper Case
80	36	B6	"SHIFT" Key
81	37	B7	"*" Lower Case and "PRINT" Upper Case
82	52	D2	"INS" When "NUM LOCK" Pressed On "0" When "NUM LOCK" Pressed Off
83	53	D3	"DEL" When "NUM LOCK" Pressed On "." When "NUM LOCK" Pressed Off
84	54	D4	"," With or Without "NUM LOCK" Pressed
85	39	B9	Space Bar Key

4.3 KEYBOARD OPERATIONAL DESCRIPTION

4.3.1 Standard Keys

The Standard keys consists of upper and lower case alphanumeric, numbers, punctuation marks and symbols, and standard control character such as, "TAB", "SHIFT", "CAPS LOCK", "BACKSPACE", and "RETURN". Key arrangement is similar to a standard typewriter keyboard, however, certain control keys will operate differently depending on the software. The following description of the standard function keys may differ depending on the software being used:

RETURN KEY: This key is also refered to as "ENTER" or "Carriage Return" (CR). When pressed, all data entered since the last RETURN will be sent to the system memory and will open a new line.

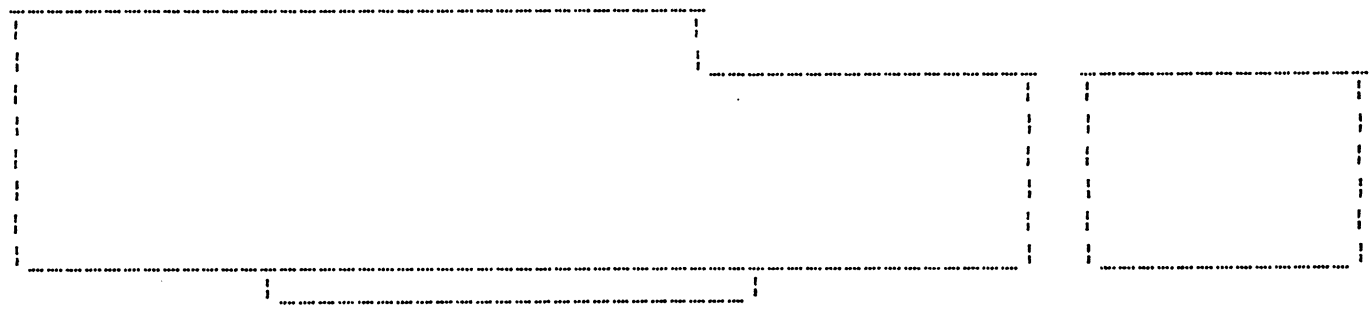
BACK SPACE: Backspaces the cursor one character at a time, erasing each character.

CAPS LOCK: Locks the alpha keys only into the uppercase mode. Pressing the CAPS LOCK key again will release this mode. Note that when in the LOCK mode, any alpha key pressed while the SHIFT key is pressed will result in a lowercase letter being typed.

4.3.2 Numeric Keypad

The numeric keypad is located on the right side of the keyboard and consists of 11 double function keys and three symbol keys. The numeric keys, 0 through 9, are arranged in standard calculator fashion and are activated when the NUM LOCK key is pressed. To disable the NUM LOCK function, simply press the NUM LOCK key again.

The numeric keypad also contains punctuation marks and symbols, cursor control keys, and function keys. The punctuation and symbol keys include the plus (+) and minus (-) signs, and the comma (,) and period (.). The function keys and the cursor control keys are invoked when NOT in the numeric lock function. An example of the use of each function key in a typical program follows:



HOME: Moves the cursor to begining of line, file, or document.

END: Moves the cursor to the end of line, file, or document.

PGUP: Scrolls the display up one screen.

PGDN: Scrolls the display down one screen.

INS: Switches between insert mode and overtype mode.

SRCH: Initiates a search for a specified character, word, sentence, or pattern.

DEL: Deletes data to the right of the cursor in a line.

<--: Moves the cursor one character to the left without erasing any data or adding any spaces.

-->: Moves the cursor one character to the right without erasing any data or adding any spaces.

/\ : Moves the cursor up one line. When the top of the screen is reached it will cause the screen to scroll up.

\/ : Moves the cursor down one line. When the bottom of the screen is reached, it will cause the to screen scroll down.

4.3.3 Fixed Function Keys

Fixed function keys are those keys that are non-programmable.

ESC: Causes the operation to cancel or stop.

BRK: Pressed in conjunction with the CTRL key (simultaneously), it will cause the execution of the current program to stop.

CTRL: Used to invoke the functions of other keys (alone it has no function).

ALT: Used to invoke an alternate function of other keys.

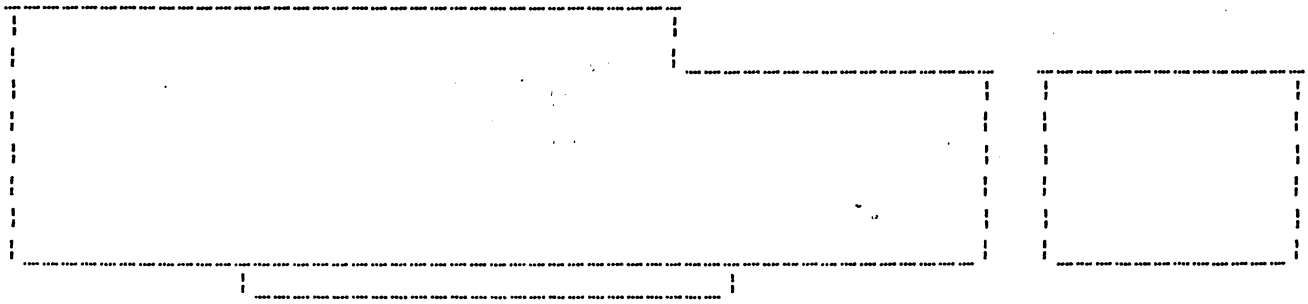
PRINT: Causes data on the display screen to be printed on the printer assigned to the console.

NUM LOCK: Causes the numeric keypad to enter the numeric mode and allow only the numbers, 0 through 9, to be typed. To release the numeric mode and use the cursor controls, press the NUM LOCK key again.

SCROL LOCK: Locks the screen in scroll mode.

4.3.4 Programmable Function Keys

The programmable function keys, F1 through F10, are capable of being programmed, via software, for any desired functions. This allows simple, as well as complex, functions to be invoked with a single keystroke.



4.3.5 Special Key combination

There are certain functions of the MAD-1 that require a special key combination to be performed. These function are:

CLEAR SCREEN: Pressing HOME while holding down the CTRL key clears the screen and moves the cursor to the upper most right of the screen.

in BASIC

left

HALT EXECUTION: Pressing BRK while holding down the ~~CNTL~~ CTRL key stops the current command execution.

SYSTEM RESET: Pressing CTRL, ALT, DEL keys simultaneously will causes a system reset.

insert hyphen instead of slash
CTRL-ALT-DEL

Chapter 5

FLOPPY DISK DRIVE

5.1 GENERAL DESCRIPTION

The MAD-1 data module contains enhanced double-headed, low-profile 5-1/4 inch Shugart SA455 MiniFloppy Disk Drives. These drives are capable of performing Read/Write operations in single and double density formats on both sides of a standard 5-1/4 inch diskette. Some of the highlights and features provided by the SA455 include:

- 500Kb (unformatted) storage capacity.
- Low power (12.5 watts)
- 125/250 kbits/second transfer rate.
- DC drive motor with precision servo speed control and integral tachometer.
- Band positioner
- Glass bounded ferrite/ceramic read/write head.
- Internal write protect circuitry.
- Activity light
- Solid die cast chassis.

The standard configuration of the MAD-1 Workstation contains two SA455 FDDs mounted side-by-side in the data module. Each unit is 1.62" H X 5.75" W X 7.96" D in size, weighs 3.3 pounds, and has a heat dissipation of approximately 9.6 watts.

5.2 FDD FUNCTIONAL DESCRIPTION

The SA455 half-height compact floppy disk drive contains all the necessary mechanical and electronic circuitry to interface with the disk drive controller logic and perform Seek, Write, and Read operations.

5.2.1 Read/Write and Control Logic

The single microprocessor controlled circuit card located in the disk drives provide Read/Write, head positioning, stepper motor drive, interface control, index detection, track zero detect, spin speed control, and dynamic braking functions. Logic for head selection between Head 1 and Head 2, read pre-amplification, and write drive are mounted within the sealed enclosure in proximity to read/write heads.

Two read/write heads are supported by a carriage mechanism coupled to the stepper motor through a rack-and-pinion motion translator. This translator allows for an increased number of data tracks while retaining the characteristics of the stepper motor. Data is recorded on one 130 mm diameter disk through two low force, low mass Winchester type ferrite heads. The Track 0 detector resides on the stepper motor and consists of a light source and a reciever. When this optical sensor is blocked by an interrupter on the motor shaft, it indicates one of several track zero positions. ~~indicates one of several logical track zero position.~~ The microprocessor determines the physical location of track 0 from redundant logical track 0.

5.3 FDD OPERATIONAL DESCRIPTION

This section describes the FDD drive operation starting with power sequencing, drive selection, motor on, track accessing, step in/out, side selection, and read/write operations.

5.3.1 FDD Power Sequencing

After the system is powered up, +5 and +12 DC supply voltages are applied (in any order) to the disk drive unit. During this time, the -WRITE GATE (Active Low Signal) line must be held inactive to prevent possible glitching of the media. The +5 Vdc is used for logic and +12 Vdc to power the spindle drive motor. After power is applied, there is a 100 msec delay before any operation is performed.

After powering on, the initial position of the heads with respect to the data tracks on the media is indeterminate. It is necessary that the heads are positioned by performing the STEP OUT operation until the Track 00 line is activated.

5.3.2 FDD Drive Selection

Drive selection occurs when one of the -DRIVE SELECT signals is true. Only the selected drive will respond to control input signals and only control output signal from that drive will be gated to the interface.

5.3.3 FDD Motor On

The FDD motor is idle when there is no seek/read/write operation. To perform any of these function the motor must first be turned on. This is accomplished by signal -MOTOR ON which is tied to bit 3 of the port B register in the 8255 programmable peripheral interface chip located on the CPU board. 500 ms must be introduced after the -MOTOR ON line is activated to allow the motor to reach its proper speed before any operation. The motor will stay on as long as the -MOTOR ON signal is active. It is the responsibility of the host system to deactivate the -MOTOR ON line to stop the motor, which will continue to rotate for three (3) seconds after the -MOTOR ON signal has been deactivated.

5.3.4 FDD Track Accessing

Read/Write head positioning is accomplished by the following:

- Setting -WRITE gate false
- Setting the appropriate -DRIVE SELECT true.
- Selected drive having -READY and -SEEK COMPLETE true.
- Setting the appropriate state of -DIRECTION IN
- Pulsing the -STEP

Each -STEP pulse will cause the R/W heads to move either one track in, or one track out depending on the state of -DIRECTION IN. When true it causes the R/W head to move inward, toward track 355, and when false it causes the head to move outward toward track 0.

5.3.5 FDD Step Out

While the -DIRECTION SELECT is inactive, a pulse on the STEP line will cause the read/write heads to move one track away from the center of the disk. For detailed timing, refer to the Shugart service manual.

5.3.6 FDD Step In

While the -DIRECTION SELECT is active, a pulse on the STEP line will cause the read/write heads to move one track closer to the center of the disk. For detailed timing, refer to the Shugart service manual.

5.3.7 FDD Side Selection

The side selection function is required to perform an operation with a double sided diskette. This is controlled by the I/O signal SIDE SELECTION which selects the read/write head on the side 0 surface of the diskette when -SIDE SELECTION is false, and selects the read/write head on the side 1 surface when the -SIDE SELECTION is true. After change of state in -SIDE SELECTION signal, a minimum of 100 micro-second time delay is required before any read or write operation to that diskette.

5.3.8 FDD Read Operation

The sequence of signal timing for reading data from the floppy disk drive is listed below:

- o Setting -WRITE gate false
- o Setting the appropriate -DRIVE SELECT true.
- o Selecting the appropriate -HEAD SELECT

5.3.9 FDD Write Operation

Following is the sequence of signal timing for writing data to the floppy disk drive:

- o Assuring -WRITE FAULT is false
- o Setting the appropriate -DRIVE SELECT true.
- o Selecting the appropriate -HEAD SELECT binary address.
- o Setting -WRITE GATE true and placing the data to be written on the MFM WRITE DATA lines.

5.3.10 Sequence of Events

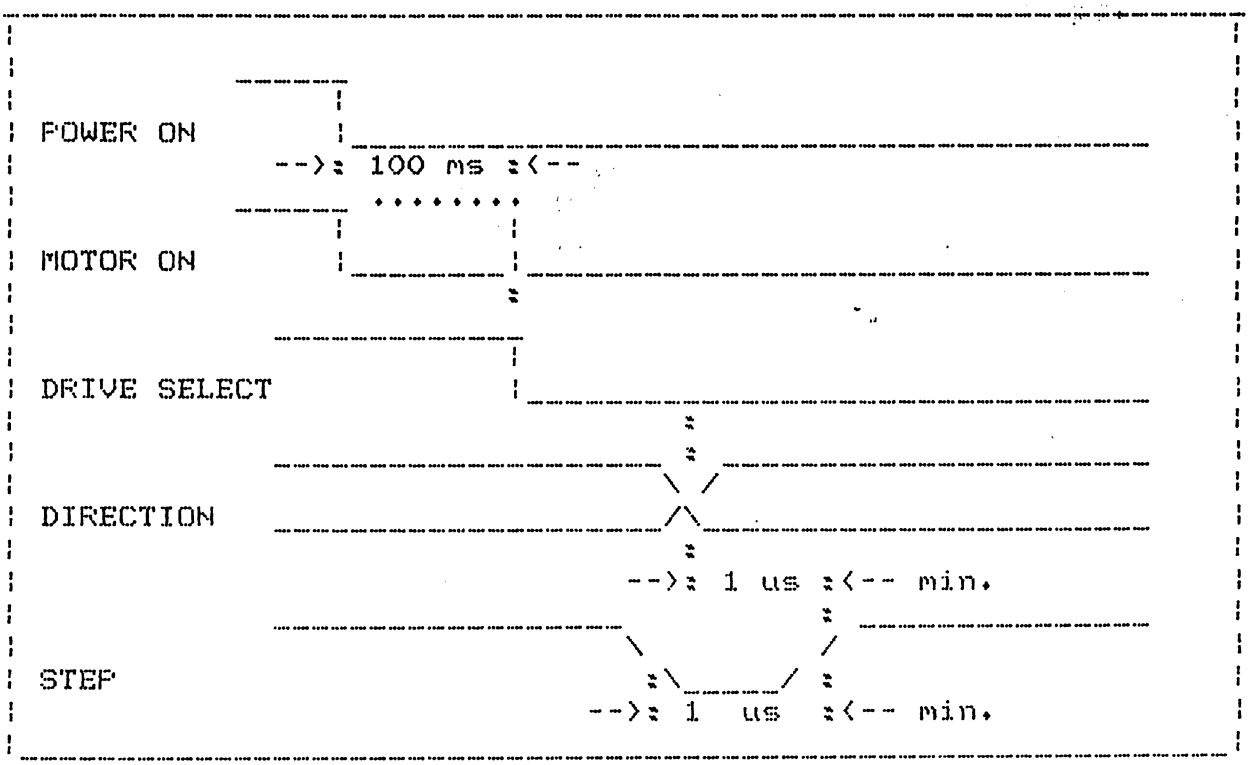
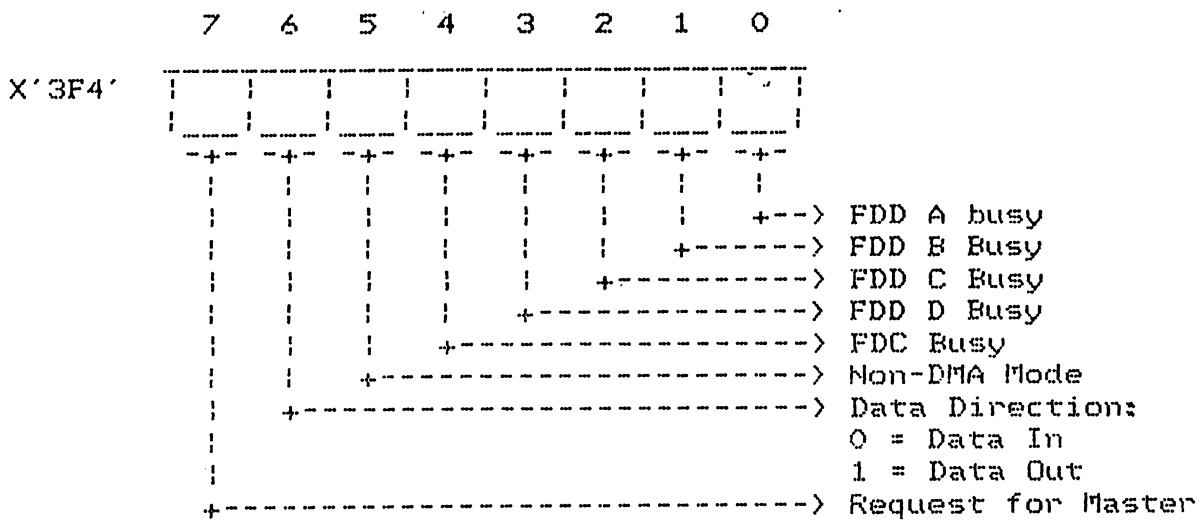


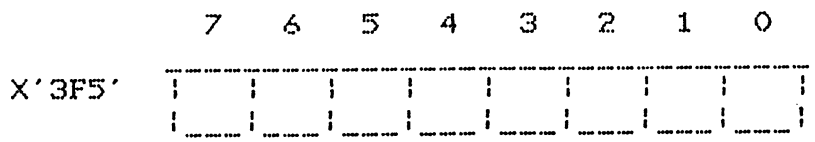
Figure 5-1: Sequence of Events Timing

5.4 FDD Programming Consideration

The NEC 765 floppy disk controller located on the CPU board in the computing module provides two registers in I/O locations X'3F4' and X'3F5'. These registers are used by the programmer for performing read, write, and status check operations using the SA455 floppy disk drive. **FDC Status Register:**



FDC Data/Command Register:



5.5 FDD INTERFACE DESCRIPTION

The interface signals between the SA455 MiniFloppy disk drive and the floppy interface logic may be divided into three categories: control lines, data lines, and power lines. The signal names and the line assignments are shown in Figure 5-2.

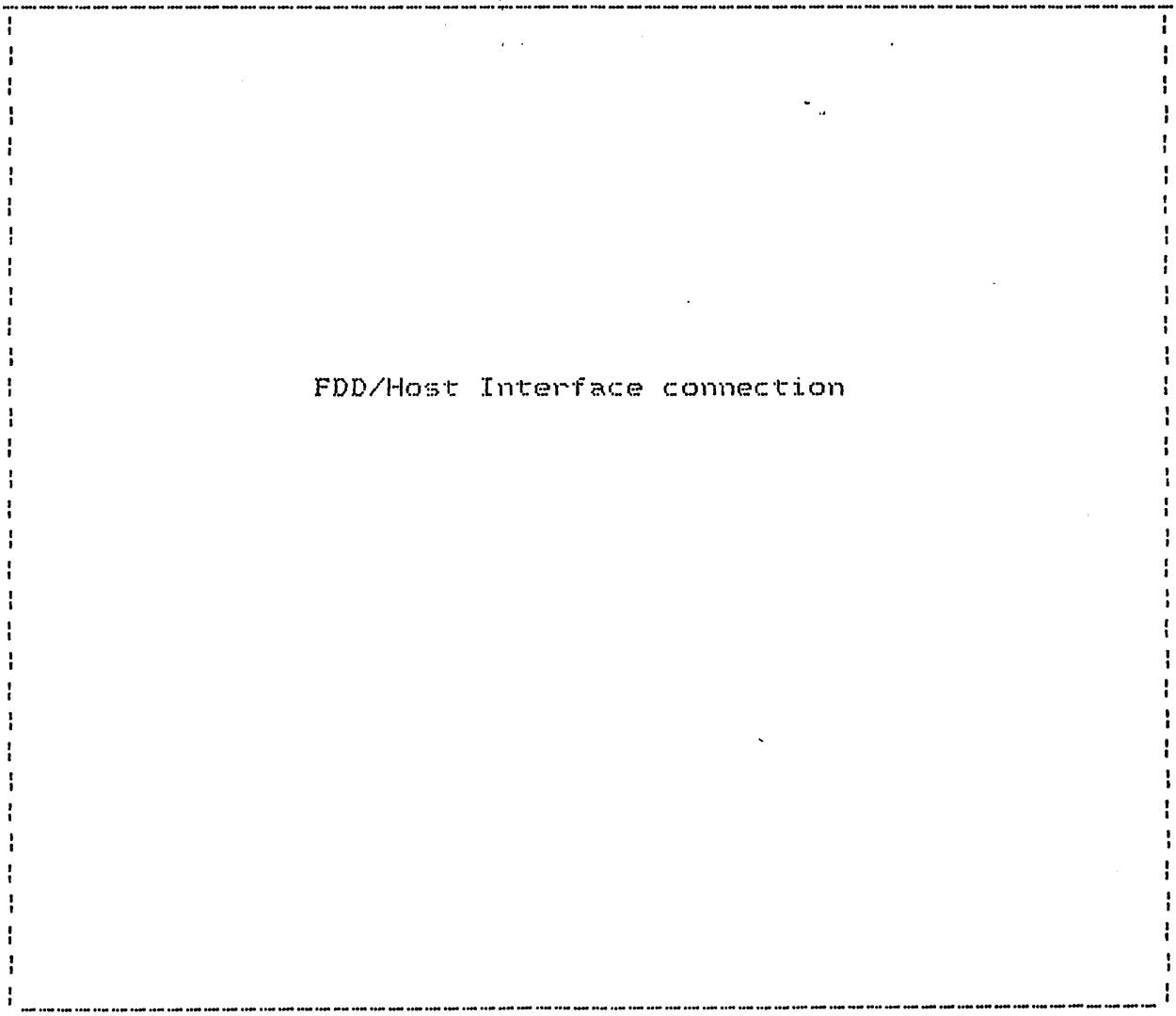


Figure 5-2: FDD Interface

5.6 FDD SPECIFICATION

PERFORMANCE SPECIFICATIONS

	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)
Byte Capacity (40 Track):		
Per Disk(unformatted)	250,000	500,000
Per Surface(unformatted)	125,000	250,000
Per Track(unformatted)	3,125	6,250
Per Disk(formatted 16R/T)	163,840	327,680
Per Track(formatted 16R/T)	2,048	4,096
Per Sector(formatted 16R/T)	128	256
Per Disk(formatted 10R/T)	204,800	409,600
Per Track(formatted 10R/T)	2,560	5,120
Per Sector(formatted 10R/T)	256	512
Transfer Rate	125 Kbits/sec	250 Kbits/sec
Latency (avg.)	100 ms	100 ms
Access Time:		
Track to Track	6 ms	6 ms
Average	93 ms	93 ms
Setting Time	15 ms	15 ms

FUNCTIONAL SPECIFICATIONS

	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)
Motor Start Time	500 ms	500 ms
Rotational Speed	300 rpm	300 rpm
Recording Density	2938 bpi	5876 bpi
Track Density	48 tpi	48 tpi

ELECTRICAL SPECIFICATION

+12 Vdc +/- 10% at 1.2 A (Max.)
+ 5 Vdc +/- 5% at 0.9 A (max.)

ENVIRONMENTAL SPECIFICATION

Temperature:

Operating	50'F (10.0'C)	to	115'F (46.1'C)
Shipping	-40'F (-40'C)	to	144'F (62.2'C)
Storage	- 8'F (-22.2C)	to	117'F (47.2'C)

Relative Humidity:

Operating	20% to 80%
Shipping	1% to 95%
Storage	1% to 95%

PHYSICAL SPECIFICATION

Dimensions:

Height	1.62 inches (41.1 mm)
Width	5.75 inches (146.1 mm)
Depth	7.96 inches (202.0 mm)

Weight 3.3 lbs (1.5 kg.)

5.7 RECORDING MEDIA, FLOPPY DISKETTE

The FDD uses standard 5-1/4" (133.4-millimeter) double-sided, double-density diskettes. For programming considerations, the recording medium is a flexible magnetic disk enclosed in a permanent protective jacket that allows the disk to freely rotate. The protective jacket has several openings and slots for Read/Write Operation (see Figure 5-3). During operation (read/write), the surface of the diskettes are constantly being cleaned by a soft fabric located inside the protective jacket.

Floppy Diskette Diagram

Figure 5-3: Diskette Diagram

5.8 MAINTENANCE

Refer to Shugart Service Manual (P/N 39239-0) for SA455 Minifloppy Drive.

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Chapter 6

HARD DISK INTERFACE AND DISK DRIVE

6.1 GENERAL DESCRIPTION

The MAD-1 optional hard disk drive is a 5-1/4" half-height rigid media employing Winchester technology. This compact disk drive is 1.69" H X 5.50" W X 8.00" D in size and occupies the same space as a single unit mini-disk floppy drive in the data module. It provides the user with reliable high performance data transfer at the rate of 5.0 Mbits/second with an unformatted capacity of 12,749,184 bytes. Some of the key features on the MAD-1 optional hard disk are given in the following list:

- Microprocessor control
- Open loop stepper head positioning.
- Head shipping zone
- Buffered seek
- Power up diagnostic
- 12,749,184 unformatted capacity
- 5.0 Mega-bits/second transfer rate
- Physical space requirement same as a mini floppy disk drive.

6.2 HARD DISK FUNCTIONAL DESCRIPTION

The MAD-1 half-height compact hard disk drive contains all the necessary mechanical and electronic circuitry for interfacing with the disk drive controller logic and performing Seek, Write, and Read operation.

6.2.1 Read/Write and Control Logic

The single microprocessor controlled circuit card located in the disk drive provides Read/Write, head positioning, stepper motor drive, interface control, index detection, track zero detect, spin speed control, and dynamic braking functions. Logic for head selection between Head 1 and Head 2, read preamplification, and write drive are mounted within the sealed enclosure in proximity to read/write heads.

Two read/write heads are supported by a carriage mechanism coupled to the stepper motor trough a rack-and-pinion motion translator. This allows for an increased number of data tracks while retaining the characteristics of the stepper motor. Data is recorded on one 130 mm diameter disk through two low force, low mass Winchester type ferrite heads. The track 0 detector resides on the stepper motor and consists of a light source and a receiver. This optical sensor, when blocked by an interrupter on the motor shaft, indicates one of several logical track zero positions. The microprocessor determines the physical location of track 0 from redundant logical track 0.

6.3 HARD DISK OPERATIONAL DESCRIPTION

This section describes the hard disk drive operation starting with power sequencing, drive selection, track accessing, head selection, and Read/Write operations.

6.3.1 Hard Disk Power Sequencing

After the system is powered up, +5 and +12 Vdc supply voltages are applied (in any order) to the disk drive unit. The +5 Vdc is used for logic and the +12 Vdc is used to power the spindle drive motor. The microprocessor verifies the spindle rotation for 3600 rpm, then activates the automatic track 0 positioning. Upon completion of Track 0 Positioning, signals -TRACK ZERO, -SEEK COMPLETE, and -READY becomes true.

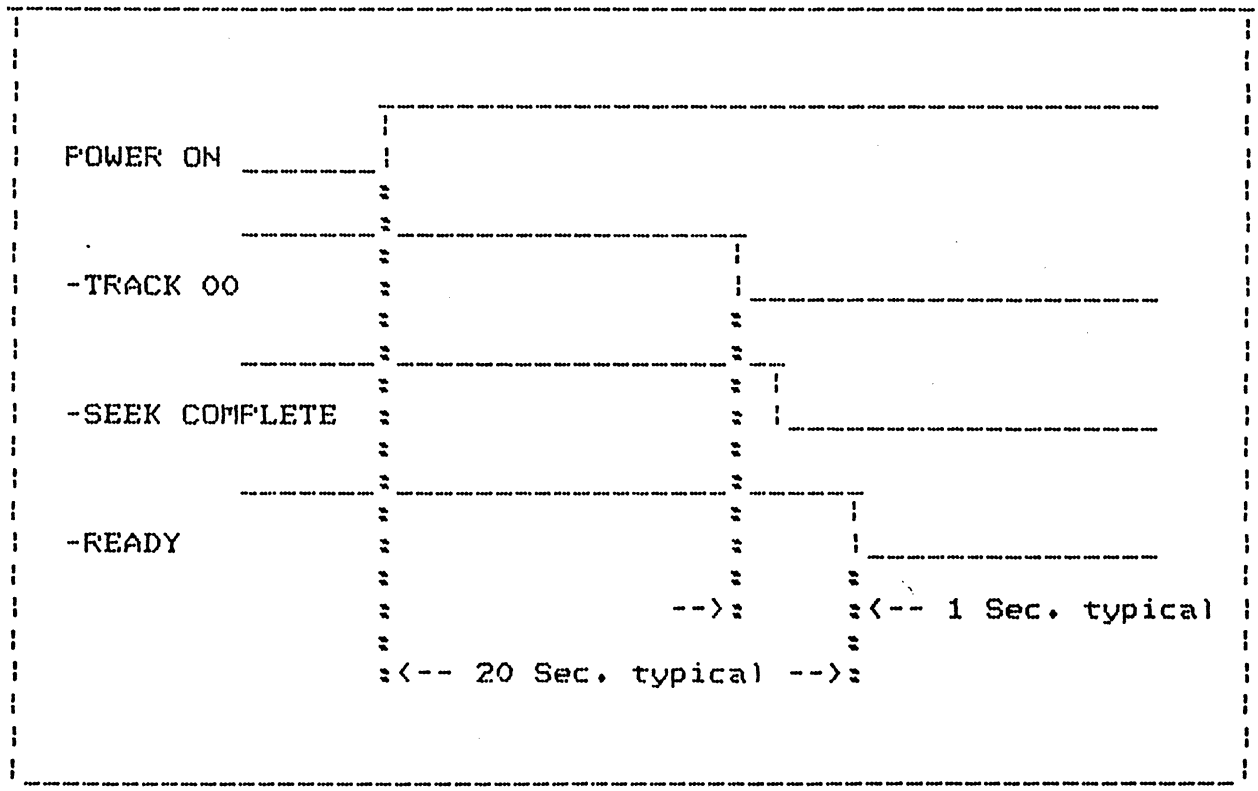

Figure 6-1: Hard Disk Power-On Timing Diagram

6.3 HARD DISK OPERATIONAL DESCRIPTION

This section describes the hard disk drive operation starting with power sequencing, drive selection, track accessing, head selection, and Read/Write operations.

6.3.1 Hard Disk Power Sequencing

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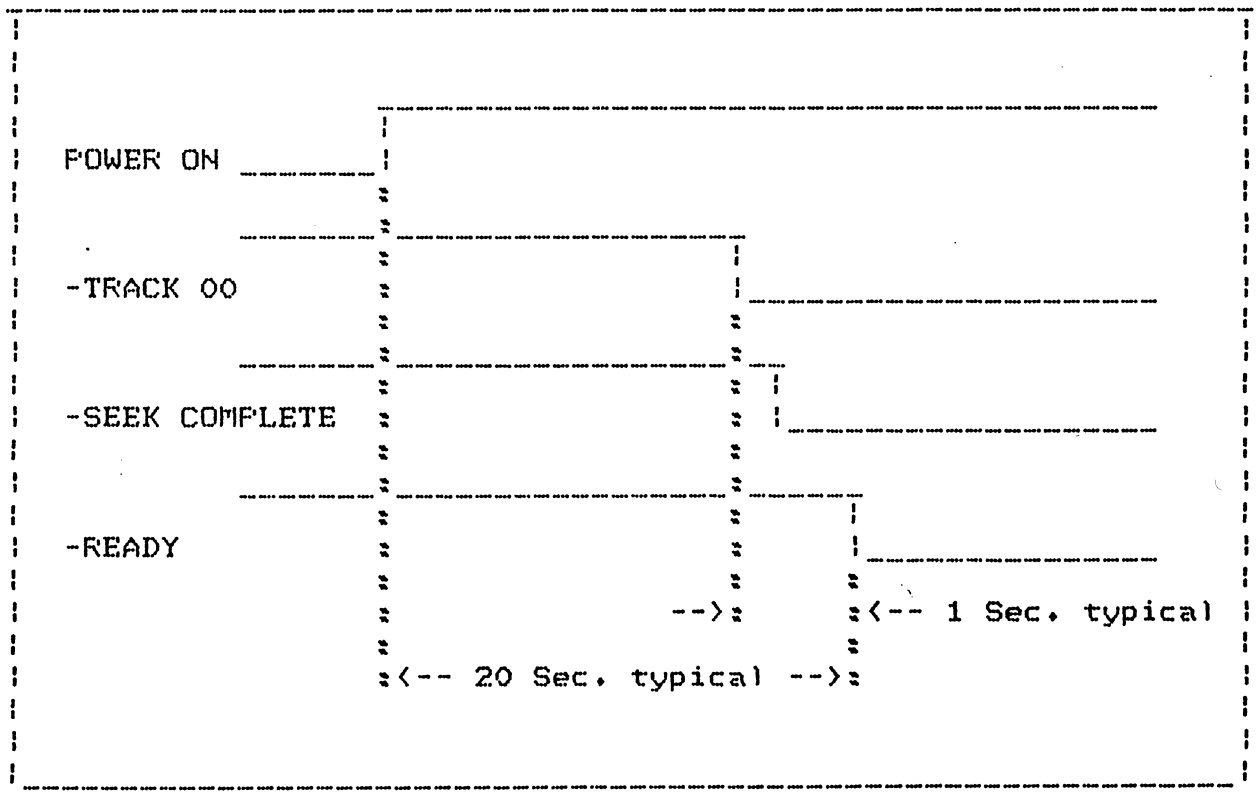


Figure 6-1: Hard Disk Power-On Timing Diagram

6.3.2 Hard Disk Drive Selection

Drive selection occurs when one of the -DRIVE SELECT signals is true. Only the selected drive will respond to control input signals and only control output signals from that drive will be gated to the interface.

6.3.3 Hard Disk Track Accessing

Read/Write head positioning is accomplished by:

- Setting -WRITE gate false
- Setting the appropriate -DRIVE SELECT true.
- Selected drive having -READY and -SEEK COMPLETE true.
- Setting the appropriate state of -DIRECTION IN
- Pulsing the -STEP

spell out

Each -STEP pulse will cause the R/W heads to move either on track in or one track out, depending on the state of -DIRECTION IN, when true it causes the R/W head to move inward, toward track 355, and when it is false it causes head to move outward toward track 0.

spell out

6.3.4 Hard Disk Head Selection

Either of the two heads may be selected by placing the heads binary address on the -HEAD SELECT 2 to the power of 0 (2e0) input line.

6.3.5 Hard Disk Read Operation

The sequence of signal timing for reading data from the hard disk drive is as follows:

- Setting -WRITE gate false
- Setting the appropriate -DRIVE SELECT true.
- Selecting drive having -READY and -SEEK COMPLETE true.
- Selecting the appropriate -HEAD SELECT

6.3.6 Hard Disk Write Operation

The following is the sequence of signal timing for writing data to the hard disk drive:

- Assuring -WRITE FAULT is false
- Setting the appropriate -DRIVE SELECT true.
- Selecting drive having -READY and -SEEK COMPLETE true.
- Selecting the appropriate -HEAD SELECT binary address.
- Setting -WRITE GATE true and placing the data to be written on the MFM WRITE DATA lines.

6.4 HARD DISK INTERFACE DESCRIPTION

The interface to the hard disk may be divided into three categories: control signals, data signals, and DC power signals. All control signals are digital and are driven by an open collector source. They are terminated by a 220/330 ohm resistor network in the driver. The control signals are gated into the drive by activating the appropriate -DRIVE SELECT line. The physical connection between the hard disk and the system involves four connectors (pin listing is given in Table 6-1): J1/P1 connection carrying control lines, J2/P2 connection handling the data lines, J3/P3 connection for the DC power lines (+5Vdc and +12 VDC), and the J4/P4 connection which provides frame ground.

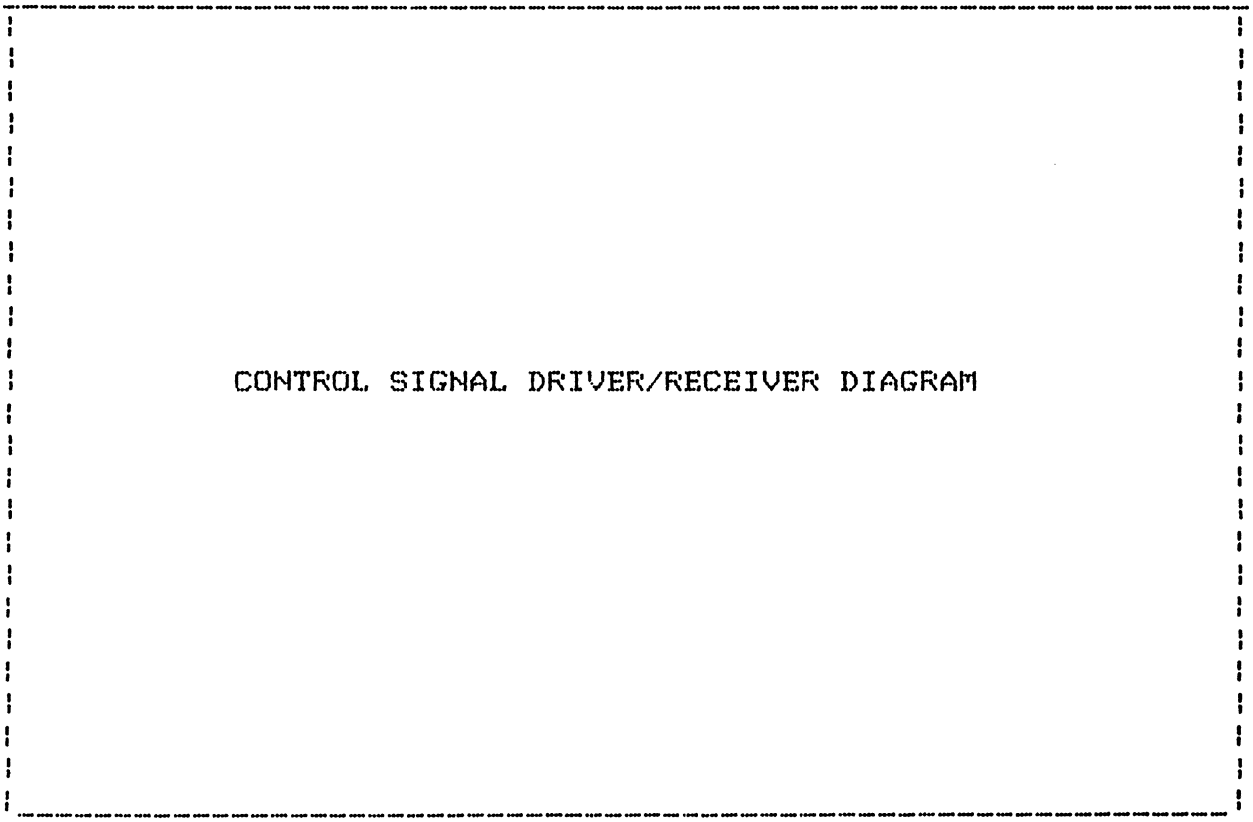


Figure 6-2: Control Signal Driver/Receiver Diagram

Table 6-1: Hard Disk Drive Interface Pin Assignment

CONNECTOR PIN NUMBER Ground	Signal	SIGNAL NAME
P1-01	P1-02	Reserved
P1-03	P1-04	Reserved
P1-05	P1-06	- Write Gate
P1-07	P1-08	- Seek Complete
P1-09	P1-10	- Track Zero
P1-11	P1-12	- Write Fault
P1-13	P1-14	- Head Select 2'
P1-15	P1-16	Reserved
P1-17	P1-18	Reserved
P1-19	P1-20	-Index
P1-21	P1-22	-Ready
P1-23	P1-24	-Step
P1-25	P1-26	-Drive Select 1
P1-27	P1-28	-Drive Select 2
P1-29	P1-20	-Drive Select 3
P1-31	P1-32	-Drive Select 4
P1-33	P1-34	-Direction In
P2-01	P2-02	-Selected
P2-03	P2-04	Reserved
P2-05	P2-06	+Spare
P2-07	P2-08	Reserved
P2-09	-	+Spare
P2-10	-	+Spare
P2-11	P2-12	Ground
P2-13	-	+MFM Write Data
P2-14	-	-MFM Write Data
P2-15	P2-16	Ground
P2-17	-	+MFM Read Data
P2-18	-	+MFM Read Data
P2-19	P2-20	Ground
P3-01	-	+12 Volts DC
P3-02	-	+12 Volts DC Return
P3-03	-	+ 5 Volts DC Return
P3-04	-	+ 5 Volts DC
P4		Frame Ground

VDC ?
Vdc ?

6.5 HARD DISK SPECIFICATION

PERFORMANCE SPECIFICATION

Storage Capacity: (Unformatted)	
Per Drive	12,749,184 Bytes
Per Track	10,416 Bytes
Storage Capacity: (Formatted)	
Per Drive	10.0 Megabytes
Per Track	8,192 Bytes
Per Sector	256 Bytes
Sectors per Track	32
Recording Heads	2 Heads
Cylinders	306
Data Tracks	612
Recording Density:	
Areal	4.87 X 10e6 bits/Sq. inch
Linear(MFM)	8290 bpi
Radial	588 tpi
Reliability:	
MTBF	8,000 hours, continuous operation
MTTR	30 minutes
Rotational Rate	3600 rpm +/- 1%
Data Transfer Rate	5.0 Mbits/second
Access Time:	
Average Latency	8.33 ms
Settling Time	15.0 ms
Seek Time	3.0 ms Track to Track
	* 85.0 ms Average
	* 205 ms Maximum
Start Time	20 seconds from Power On to Ready
Stop Time	15 seconds from Power Off time

*: Buffered including settling time.

ELECTRICAL SPECIFICATION

DC Voltage Input	+12 Vdc +/- 5%, 1.1 amps Max. + 5 Vdc +/- 5%, 1.5 amps Max.
AC Voltage Input	Not Required
Power Consumption	17 Watts typical

ENVIRONMENTAL SPECIFICATION

Temperature:	
Operating	40'F (4.4'C) to 115'F (46'C)
Storage	-40'F(-40'C) to 135'F (57'C)
Relative Humidity:	
Operating	8% to 80% non-condensing
Storage	8% to 80% non-condensing
Max. Wet Bulb	78'F (26'C)

PHYSICAL SPECIFICATION

Dimensions:	
Height	1.69 inches +/- 0.01%
Width	5.76 inches +/- 0.02%
Depth	8.00 inches +/- 0.02%
Weight	3.5 pounds

Chapter 7

BASIC INPUT/OUTPUT SYSTEM

7.1 INTRODUCTION

Appendix A

Glossary Of Terms

TERMS	DEFINITION
A/N	Alphanumeric
AND	Logical Operator
APA	All Points Addressable
ASCII	American Standard Code for Information Interchange
BAUD	Unit of Transmission, In asynchronous transmission, the unit of modulation rate corresponding to one unit of interval per second; that is , if the duration of unit interval is 20 milliseconds, the modulation rate equals 50 Baud.
BCC	Block-Check Character.
BIOS	Basic Input/Output System
BIT	Smallest Unit of Information
Byte	8 bit
BPS	Bit Per Second
BSC	Binary Synchronous Communication
CAS	Column Address Strobe
CCITT	Comite Consultatif International Telegraphique et Telephonique (European Standard Committe)
CPS	Character Per Second
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CRT	Cathode Ray Tube
CTS	Clear To Send
DLAB	Divisor Latch Address Bit
DIN	Deutsche Industrie Norm (German Industrial Standards)
DIP	Dual In-line Package
DMA	Direct Memory Access
DSR	Data Set Ready
DTR	Data Terminal Ready

TERMS	DEFINITION
EBCDIC	Extended Binary-Coded Decimal Interchange Code
ECC	Error Checking and Correction
EIA	Electronic Industries Association
EOT	End-of-Transmission character
EPROM	Erasable Programmable Read Only Memory
ETX	End-of-Text character
Hz	Hertz, unit of frequency
KB byte	Kilobytes; 1000 Bytes
KHz	Kilohertz, 1000 hertz
LED	Light Emitting Diode
m	One thousandth part
M	Mega (1,000,000)
MB byte	Megabyte; 1 million bytes
MFM	Modified Frequency Modulation
Modem	Modulator/Demodulator define, explain
nsec	Nanosecond (one billionth of second)
NRZI	None-Return-to-Zero Inverted
OR	Logical operation of what kind, for what?
PEL	Picture Element
PIXEL	Picture Element
PROM	Programmable Read Only Memory
RAS	Row Address Strobe
RGBI	Red-Green-Blue-Intensity
ROM	Read Only Memory
RTS	Request To Send
RS-232C	The standard set of EIA signals for communication with external equipment
RS-422	The standard set of EIA signals for communication with external equipment
RLSD	Receiver Line Signal Detect.
Rx Data	Receive Data
SDLC	Synchronous Data Link Control
serdes	Serializer/Deserializer
SS	Start-Stop transmission
TTL	Transistor-Transistor-Logic
TX Data	Transmit Data

Appendix B

I/O ADDRESS MAP

ADDRESS (Hex)	FUNCTION ASSIGNMENT
000-00F	Used for DMA control (Intel 8237A-5)
020-021	Used for interrupt control (Intel 8259A)
040-043	Used for timer control (Intel 8254)
060-063	Used for programmable peripheral chip (Intel 8255A-5)
080-083	Used as DMA page register
0Ax *	Used as NMI mask register
0Cx	Reserved
0Ex	Reserved
200-24F	Reserved
278-27F	Reserved
2E8-2EF	Asynchronous communication (Tertiary)
2F8-2FF	Asynchronous communication (Secondary)
300-31F	Used as a prototype card
320-31F	Used for fixed disk
378-37F	Used for printer
380-38C**	Used for the SDLC communications
380-389**	Binary synchronous communication (Secondary)
3A0-3A9	Binary synchronous communication (Secondary)
3B0-3BF	Used for monochrome display
3C0-3CF	Reserved
3D0-3DF	Used for color graphics
3E0-3E7	Reserved
3F0-3F7	Used for floppy disk~~ette~~
3F8-3FF	Asynchronous communications (Primary)

*: At power-on, NMI to the 80186 is masked off and the mask is controlled as follows:
ENABLE NMI = Write x'80' to I/O Address x'A0'
DISABLE NMI= Write x'00' to I/O address x'A0'

**: Since the addresses of these two functions overlap, they cannot be used together.

Appendix C

SYSTEM MEMORY MAP

STARTING ADDRESS Dec.	STARTING ADDRESS Hex.	FUNCTION
0	00000	512 K BYTES MAIN MEMORY ON CPU BOARD
16K	04000	
32K	08000	
48K	0C000	
64K	10000	
80K	14000	
96K	18000	
112K	1C000	
128K	20000	
144K	24000	
160K	28000	
176K	2C000	
192K	30000	
208K	34000	
224K	38000	
240K	3C000	
256K	40000	
272K	44000	
288K	48000	
304K	4C000	
320K	50000	
336K	54000	
352K	58000	
368K	5C000	
384K	60000	
400K	64000	
416K	68000	
432K	6C000	

STARTING ADDRESS Dec.	STARTING ADDRESS Hex.	FUNCTION
448K	70000	
464K	74000	
480K	78000	
496K	7C000	
512K	80000	128 K BYTES EXPANSION ON MEMORY EXPANSION BOARD
528K	84000	
544K	88000	
560K	8C000	
576K	90000	
592K	94000	
608K	98000	
624K	9C000	
640K	A0000	RESERVED ADDRESS SPACE
656K	A4000	
672K	A8000	
688K	AC000	
704K	B0000	<-- ADDRESS SPACE ASSIGNED TO MONOCHROME -->
720K	B4000	<---------- RESERVED ---------->
736K	B8000	<-ADDRESS SPACE ASSIGNED TO COLOR/GRAPHICS->
752K	BC000	<---------- RESERVED ---------->
768K	C0000	192 K BYTES MEMORY ADDRESS SPACE RESERVED
784K	C4000	
800K	C8000	
816K	CC000	
832K	D0000	
848K	D4000	
864K	D8000	
880K	DC000	
896K	E0000	
912K	E4000	
928K	E8000	
944K	EC000	
960K	F0000	32K ADDRESSING SPACE ASSIGNED TO BIOS
976K	F4000	
992K	F8000	RESERVED
1008K	FC000	

~~this differs from System memory map in User's Guide~~

Appendix D

JUMPER SELECT OPTION

MAD-1 provides 25 jumpers on the CPU board which allow the user to select various system configurations. These jumper connections are shown in Table C-1:

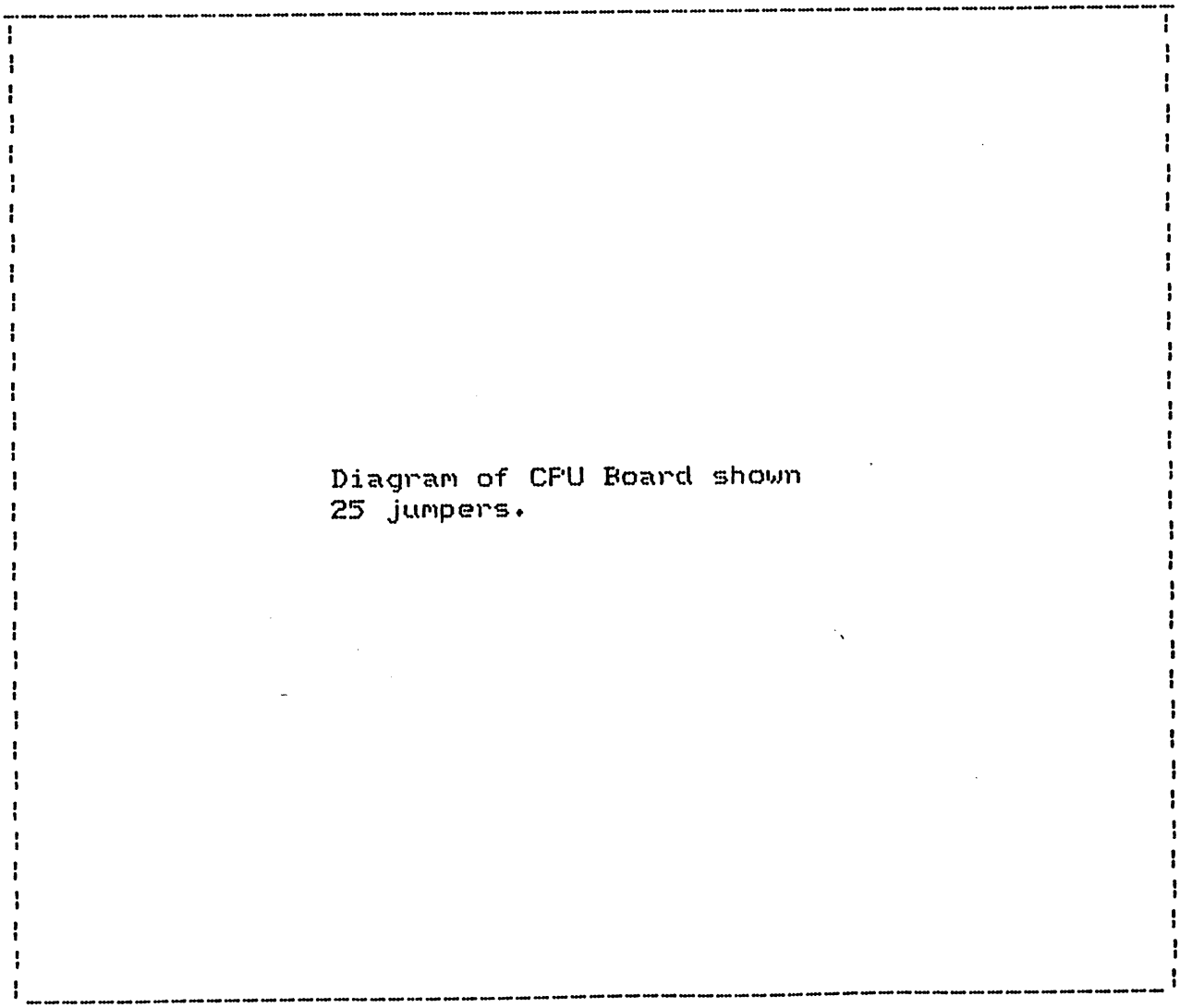


Table C-1: Jumper Select on CPU Board

JUMPER #	JUMPER CONNECTION & FUNCTION
W-01	Not Used
W-02	Tertiary Serial Port Configuration
W-03	Tertiary Serial Port Configuration
W-04	Tertiary Serial Port Configuration
W-05	Selects Transmit and Receiver Clock into 8274
W-06	Connects 80186 NMI input to Ground or to Parity circuitry.
W-07	Not Used
W-08	Not Used
W-09	Parity Circuit Test Jumper
W-10	Not Used
W-11	A to B connects 8274 Channel A's transmitter Data Ready to 80186 Channel 0's DMA request Line. C to D connects 8274 Channel A's receiver Data Ready to 80186 Channel 1's DMA request Line.
W-12	Floppy Write Precompensation
W-13	Floppy Write Precompensation
W-14	Tertiary Serial Port Configuration
W-15	Tertiary Serial Port Configuration
W-16	Tertiary Serial Port Configuration
W-17	Tertiary Serial Port Configuration
W-18	Tertiary Serial Port Configuration
W-19	Floppy Write Precompensation
W-20	Front Panel LED
W-21	A to C connects speaker clock to 8255 pin (P) C5 B to C connects Data Set Ready from Tertiary Serial Port (8274) to pin (P) C5 of 8255.
W-22	Interrupt Control AEN from 8237 or pin 5 of J-11.
W-23	Connects I/O CH RDY to 8237 RDY
W-24	Selects 4 MHz clock to 8237 and DMA clock from pin 3 of J-11.
W-25	A to C connects INT7 of 8259 to the parallel (Centronics) port circuitry. A to B connects INT7 of 8259 to the 8274 USART.

*: Jumper W-2 --> W-4 and W-14 --> W-18 to configure the Tertiary Serial Port as either an RS-422 or RS-232C port.

**: Jumper W-12 ,W-13, and W19 for different values to select the floppy's write pre-compensation on 9229 chip. See Floppy Write Pre-compensation table next page.

Table C-2: Floppy Write Pre-Compensation Table

JUMPER CONNECTION (0 = Short, 1 = Open) W-19	W-13	W-12	FLOPPY WRITE PRE-COMPENSATION TIME Nanoseconds
0	0	0	625 ns.
0	0	1	625 ns.
0	1	0	500 ns.
0	1	1	500 ns.
1	0	0	375 ns.
1	0	1	250 ns.
1	1	0	125 ns.
1	1	1	000 ns.

nsec? consistency!

MAD-1 provides 12 jumpers on the video board which allow the user the flexiblity of configuring the video for monochrome or color/graphics clock and color composition. The jumper connections are given in Table C-3:

Diagram of Video Board showing 12 jumpers.

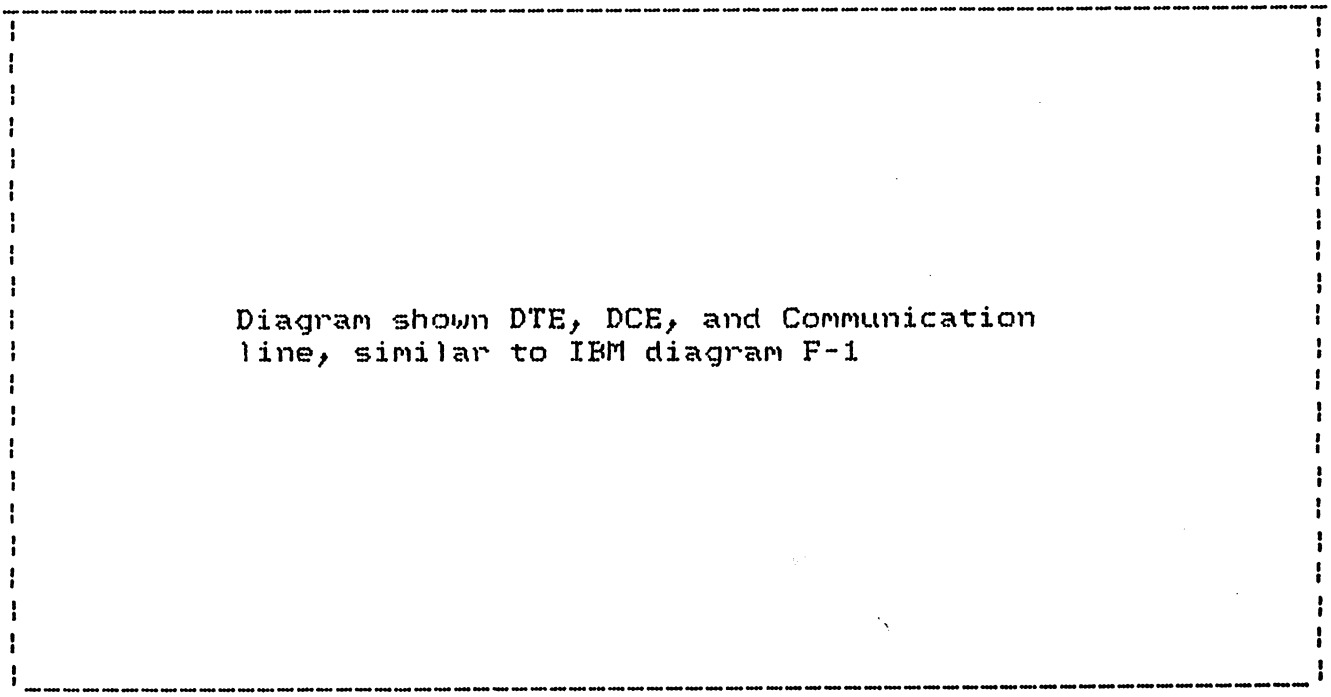
Table C-3: Jumper Select on Video Board

JUMPER #	JUMPER CONNECTION & FUNCTION
W-1	Not Used
W-2	When connected to ground, selects monochrome clocks.
W-3	When connected to ground, selects S/W of color or monochrome.
W-4	When connected to ground, selects clock for the color terminal.
W-5	When connected to ground, forces RGB off.
W-6	When connected to ground, forces RGB on.
W-7	When connected to ground, allows S/W control of intensity.
W-8	When connected to ground, forces intensity high.
W-9	When connected to ground, enables composite sync.
W-10	When connected to ground, shorts pin 2 of video display jack (composit sync signal).
W-11	When connected to ground, enables normal vertical sync signal.
W-12	When connected to ground, inverts vertical sync.

Appendix F

REMOTE COMMUNICATION

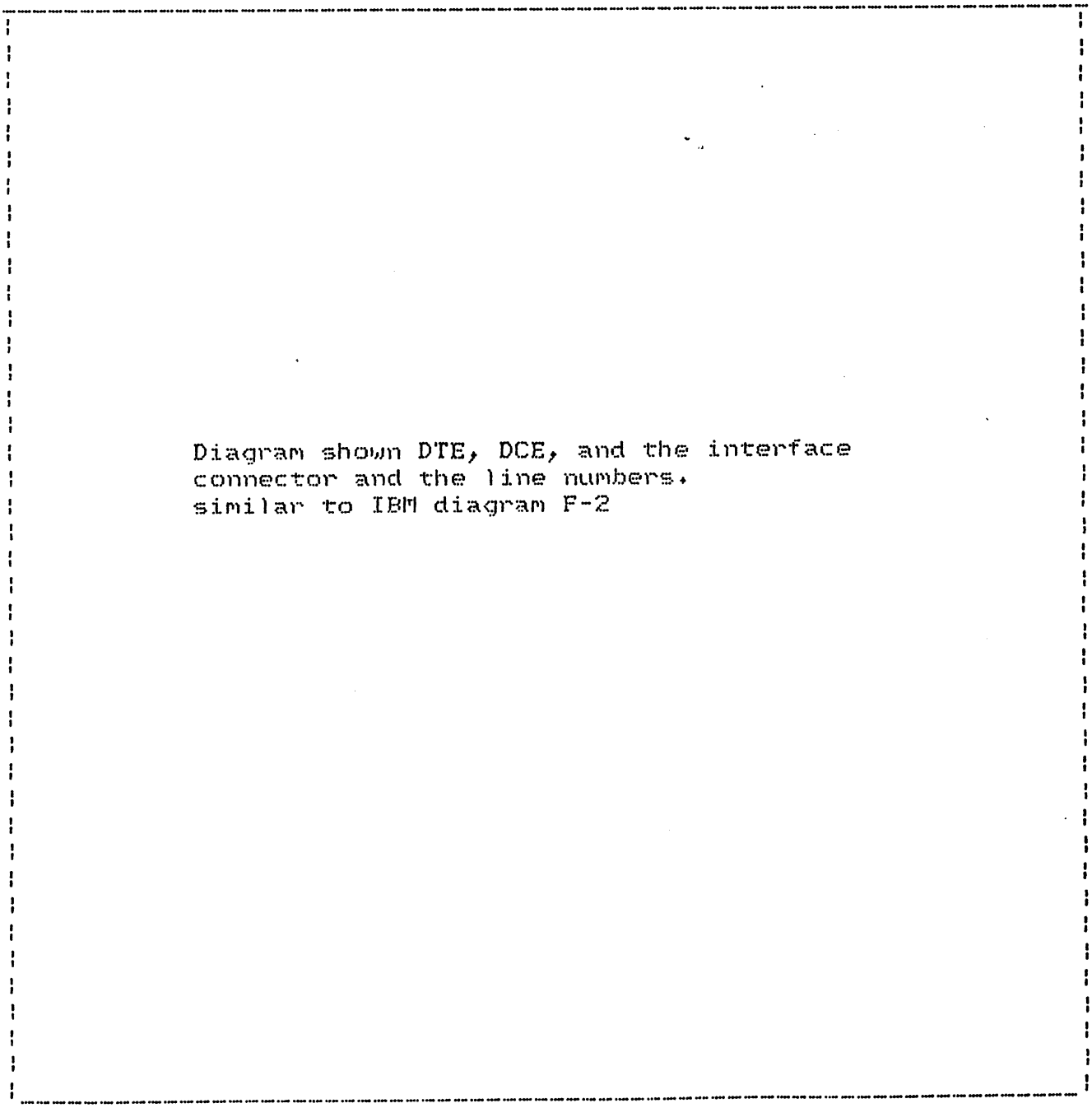
Remote communication between Data Terminal Equipment (DTE) and a host processor can be established using voice quality communication lines (standard telephone line) and Data Communication Equipment (DCE), as shown in the following figure:



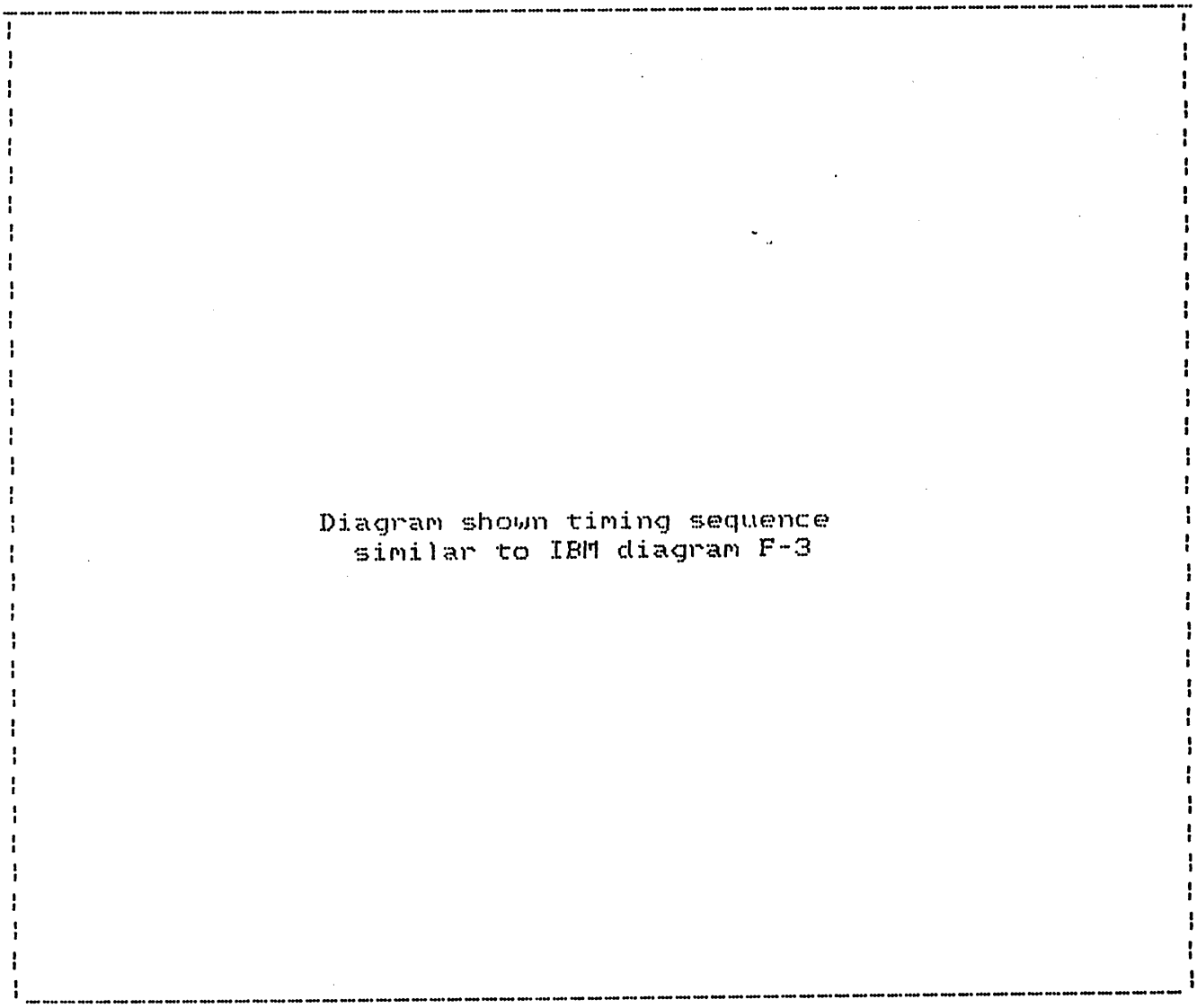
Connection between the data terminal equipment and data communication equipment is made through a cable conforming to the EIA or CCITT standard, using EIA/CCITT adapter which interfaces to the data terminal equipment.

Note: All EIA standards are labled with RS-nnn-r notation, and CCITT standards are labled with V.nn or X.nn.

The standardized interface defines the connector type, signal name, signal levels, and the pin assignments which are used to connect many different types of data terminal equipment to many types of data communication equipment. One of the most commonly used EIA interface is the RS-232C, which is equivalent to the CCITT V.24 interface. The connector used for this interface is a 25-pin "D" shell, as shown below:



The relative timing of each signal is shown in the following timing diagram. It describes the sequence of operation for establishing communication between the data terminal equipment and a data communication equipment using EIA RS-232C or CCITT V.24 interface.



Appendix G

SYSTEM COMPATIBILITY DELTA

G.1 Central Processing Unit Delta with IBM-PC

Table G-1: System Compatibility Delta Summary

FEATURES/FUNCTION	MAD-1	IBM-PC/XT
Processor	Intel 80186	Intel 8088
Co-Processor	Not provided	Intel 8087
Clock Frequency	6.0 MHz	4.77 MHz
CPU Cycle	167 nsec	210 nsec
Data Bus Width	16-bit Internal/External	8-bit External
Memory Cycle Time	667 nsec	840 nsec
Interrupt Request	IRQ2,3,5 are provided on the I/O Bus, IRQ4 is assigned to primary serial port, IRQ6 is assigned to the on board(CPU) floppy controller, and IRQ7 may be connected to the 8274 USART interrupt on the parallel printer port.	
DMA Channel	DMA Channel 0, 1, and 3 are carried on the bus, and CH2 is assigned to the on board floppy controller.	
Card Select	Not available	Provided
Clock/Calander	MSM-58321	Not provided

G.2 Serial Communiation Delta with IBM-PC

- Intel 8274 Multi-Protocol Serial Communication
  - * Synchronous Serial Communication
  - * IBM Bisync Serial Communication
  - * HDLC/SDLC

G.3 Input/Output Channel Delta with IBM-PC

The Mad-1 I/O channel consists of 86 lines which are a superset of the I/O channel set used by most of the PC compatible computers. These 86 lines include 62 signal lines (IBM I/O bus), with the exception of interrupt request lines IRQ4, IRQ6, and IRQ7, which are not used on the MAD-1 bus. The additional 24 lines are part of the MAD-1 bus expansion which is used for the addition of eight data bits (D8 - D15), power/ground lines, and six lines that are reserved for future use.

The I/O channel delta between the MAD-1 and the IBM-PC/XT is given in Table G-2.

Table G-2: I/O Channel Delta

I/O Channel	Signal Assignment		Comments
Pin #	MAD-1	IBM-PC	
B21	Reserved	IRQ7	Used for printer or auxiliary serial port.
B22	Reserved	IRQ6	Used for floppy disk controller.
B24	Reserved	IRQ4	Used for primary serial port.
A32 & B32	J9-3&J9-1	N/A	Reserved
A33 & A34	Reserved	N/A	
B33 & B34	Reserved	N/A	
A35 - A42	D8 - D15	N/A	Additional 8 data bits
B35	LBHE	N/A	Latched Byte High Enable
B36 - B38	+5 VDC	N/A	Additional voltage lines
B39 - B42	GND	N/A	Additional ground lines

G.4 Floppy Disk Drive Adapter Delta with IBM-PC

- Digital Output Register

G.5 Video Display Delta with IBM-PC

Integrated Monochrome, and Color/Graphics

G.6 Keyboard Delta with IBM-PC

The keyboard lay-out, and two addition Keys "BRK" and " , ".

To: From Users RA 10-24
From: Ryan Augustin
Subj: Power On Diagnostics (POD)
Date: Oct. 24, 1984

PRELIMINARY PRELIMINARY PRELIMINARY

POWER ON DIAGNOSTICS (POD)

This document describes the POD sequence for the MAD - 1 in release 841010 of the PROM. The task to be accomplished is to test various hardware and make sure the hardware is properly initialized. Once this is done, the MAD - 1 will beep once, then a Boot is attempted (using INT 19h). If the boot fails, the PROM moniter is invoked.

PHILOSOPHY:

The testing philosophy is to depend on as little untested hardware as possible. For this reason, no RAM is used until the first 64KB has been tested. This means that some of the early errors cannot be reported on the video monitor. If an error is detected in the first two tests, the CPU register and flag tests, the system will halt. Errors in subsequent tests will beep an error code on the speaker. Testing will continue after any error. The ID number (same as the number of beeps) of the first failing test will be printed to the monitor (provided the system isn't too sick) with a warning message. This means that some systems may boot and appear to work flawlessly even though an error was detected. If your MAD - 1 detects a fault in the POD sequence, contact your MAD - 1 service representative.

FIRST STAGE: No RAM is required for these tests to run

*h Test CPU registers with 0AAAAh and 05555h pattern, halt if mismatch.
*h Test CPU flag registers with set and reset, halt if error.
Initialize on board 8254 TIMER for timer functions and tone generator.
Initialize on board 8255 parallel I/O chip and dependent circuits:
floppy disk controller
keyboard circuit
I/O check circuit (held disabled)
parity circuit (held disabled)
Read and write PC compatible soft reset flag in RAM to set its parity.
Enable the RAM parity and I/O check circuits.
*t Perform a checksum test on each PROM.
*t Test the 8237A-5 DMA's registers.
*t Startup and test refresh circuitry and refresh DMA.
*t Test the first 64KB of RAM.
*t Test the parity error flag.
Initialize stack segment (SS) and stack pointer (SP) to use tested RAM

SECOND STAGE: Working RAM is required for these tests to run.

Setup a dummy interrupt table in RAM to test the interrupt controller.
*t Initialize and test the interrupt controller internal registers.
Setup the interrupt table for hardware, software and unused interrupts.
Read the dipswitch and set equipment flags.
*t Test video RAM (!!not implemented!!).
Initialize 6645 video controller. (INT 10)
Determine memory size: Switches:

3	4	size
on	on	128KB
off	on	256KB
on	off	384KB
off	off	Auto sizing *

Print message indicating memory size.
Clear the parity check circuits again.
*t Test memory above the first 64KB up to the top of memory.
*t Test the parity error flag again.
Initialize the floppy disk controller chip and floppy parameters.
Initialize the (Centronics compatable) parallel printer port. (INT 17H)
Initialize hard disk and controller (if present).
Print the 'LOADER' message and date code.
Test switch 2 of dipswitch;
If 'OFF':
Print message indicating manufacturing loop mode.
Jump back to first test of first stage.
Otherwise:
Continue.
Beep once.
Transfer control to boot interrupt (INT 19H).

LEGEND:

* Auto sizing writes and checks for a AA55H pattern on 16KB boundries above the first 64KB. The first failing test determines memory size.

*h System will halt if an error is detected.

*t Tests that will generate a beep sequence and error number, described below.

DETAIL OF TESTS:

6 beeps: PROM CHECKSUM
The value in each PROM address is added to the next. The resulting sum for each PROM must be zero.

9 beeps: DMA Test
The 8237A-5 DMA's 8 address and count registers are written and checked with 0AAAAh and 05555h patterns.

7 beeps: Refresh Initialization Test
Channel 0 of the 8237A-5 DMA is programmed for continuous mode. The address register must change within approximatley 50 microsec.

4 beeps: Memory test of first 64KB
The POD RAM tests use the REP LODSW and REP SCASB instructions to rapidly write and read test values in blocks of 16KB using the patterns 0AAh, 055h, 080h and 00h. The 080h pattern is used to change the value in the parity RAM, and the 00 pattern leaves memory clear.

5 beeps: Parity Test.
The parity status bit is read using the [illegible] peripheral chip. The bit will be set if a parity error occured.

8 beeps: Interrupt Controller Test.
055h and 0AAh patterns are written and checked in the interrupt controller chip. The data must read back as it was written

2 beeps: Memory test above the first 64KB.

This test functions the same as the memory tests for the first 64KB of RAM. If an error is detected in this test, an encrypted numeric message is printed to the monitor. The 16 bit message contains the failing bits, bank and even/odd address status.

Even/odd address status:

The first and leftmost nibble will be either a 1 or 0. If it's a 1 the failure was detected on an odd address, otherwise the error address is even.

Bank:

The second nibble is the bank number, with values 0 through 3. This translates to the rows of RAM chips for both even and odd. Using the bank number coupled with the even/odd address status will show the row of RAM causing the problem.

Bits:

The last two nibbles should be taken as 8 bits. Any bit set in this byte indicates the bit position of the error. Note that it is possible for more than one bit to be set (for example, if the memory size switch setting is greater than the available memory, this byte would most likely be '55').

All three pieces of information combined will point to one chip or more that are causing a problem. In some circumstances the last two nibbles will be zero. This indicates the error is unrepeatable and the bit location within the row is unknown.

The memory layout guides below show the information needed to locate any RAM chip that the memory test above the first 64KB indicates as being faulty.

SAMPLE ERROR:

After a 2 beep sequence, '1204' is printed to the monitor.

```
        2       0       4
        |       |       |
        |       |       Bits, both nibbles taken as 8 bits
        |       |
        |       Bank
        |
Even/Odd address status
```

SAMPLE ANALYSIS:

Even/Odd address status is set to 1, this means the error occured on an odd bank. The bank number is 2, indicating the error occured on bank 2. The bits value is 04, breaking this down to bits would be the same as 0000000100(binary). The bit in error is bit 2. Combining all three pieces shows that:

Bit 2, bank 2, odd bank is failing.

Using the memory layout guide below for a CPU fab# 310002, the location of the failing chip is determined to be 4J.

6 Mhz

		BITS [0-7]							
		=0=	=1=	=2=	=3=	=4=	=5=	=6=	=7=	PARITY
	(REF. DESIG)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
BANK [0-3] ODD	0000-1FFF(L) BANK 0 ODD									
	2000-3FFF(K) BANK 1 ODD									
	4000-5FFF(J) BANK 2 ODD			XXX						
	6000-7FFF(H) BANK 3 ODD									
BANK [0-3] EVEN	0000-1FFF(G) BANK 0 EVEN									
	2000-3FFF(F) BANK 1 EVEN									
	4000-5FFF(E) BANK 2 EVEN									
*	6000-7FFF(D) BANK 3 EVEN									

RAM layout guide, CPU Fab# 310002

Silkscreened reference designations are shown in parentheses().

the X's mark the failing RAM chip for the sample error given above.

8 Mhz

		BITS [0-7]								
	(REF. DESIG)	=0= (1)	=1= (2)	=2= (3)	=3= (4)	=4= (5)	=5= (6)	=6= (7)	=7= (8)	PARITY (9)
BANK [0-3] ODD	0000-1FFF(L) BANK 0 ODD									
	2000-3FFF(K) BANK 1 ODD									
	4000-5FFF(J) BANK 2 ODD									
	6000-7FFF(H) BANK 3 ODD									
BANK [0-3] EVEN	0000-1FFF(G) BANK 0 EVEN									
	2000-3FFF(F) BANK 1 EVEN									
	4000-5FFF(E) BANK 2 EVEN									
	6000-7FFF(D) BANK 3 EVEN									

RAM layout guide, CPU Fab# 310016

Silkscreened reference designations are shown in parentheses().

10 beeps: Video RAM test

The video memory test is identical to the tests for the memory above the first 64KB. The first nibble of the 16 bit word will be a 1 if the error is on an odd address (attribute) or 0 if the error is on an even address (data). The second nibble will always be 5 and the last two nibbles can be ignored. Use the following table to determine locations of RAM elements.

Video Board	Even/Odd	Location
Fab# 260005	Even	6B
	Odd	6D
Fab# 170001	Even	U9
	Odd	U7

Ryan Augustin

Ryan Augustin,
Software Lab