RCA 301

ELECTRONIC DATA PROCESSING SERVICE TRAINING

CONTROL LOGIC

TRAINING MANUAL

VOLUME II

Company Private

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F O R E W O R D

The four sections included in this text comprise the second volume of a series of logic descriptions, intended for use as a supplement to classroom instruction in the control logic segment of the RCA 301 Computer System training program. A description of the equipment logic has been incorporated in certain sections to maintain continuity and to clarify specific areas of the control logic, which are dependent upon peripheral equipment operations and controls.

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ANELEX LINE PRINTER CONTROL

The On-Line Printer Control, Model 316-1, enables the Processor to operate the On-Line Printer, Model 333, in accordance with the computer program. This module controls the printing and paper advance on command from the program control. Characters are read from the memory to the printer control module and the module determines the columns of a given line in which particular characters are to be printed. When an additional Model 333 Printer is used with the Processor, a second On-Line Printer Control, Model 316-2, is required.

The On-Line Printer, Model 333, is a high-speed mechanical printer. It uses a revolving drum which rotates at a speed of 1000 rpm or 660 rpm, depending upon the state of a switch on the Printer itself. There are 120 columns of 64 characters on the drum, enabling the Printer to print 120 characters per line (see Figure 7-1).

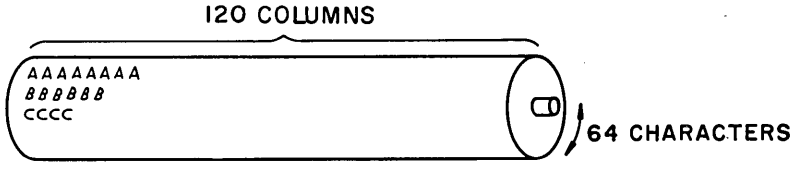


Figure 7-1. Print Drum.

Besides printing, the Model 333 Printer can advance paper at a maximum rate of 150 lines per second. Paper can be advanced a single line, a single page, or a portion of a page (vertical tab). Single line advancing is controlled by the Model 316 Control Logic, while the latter two types are controlled by a punched mylar tape in the Printer.

PRINT AND PAPER ADVANCE INSTRUCTION FORMAT (PAN/PAS)

In the 301 system, two Print and Paper Advance instructions exist - one normal and one simultaneous. The operation code for the Normal Mode instruction is the letter B, and the operation code for the Simultaneous Mode instruction is the letter C. The rest of the format for the two instructions is identical.

In a PAN or PAS instruction, the N character 2^5 bit being a one indicates synchronous operation, whereas a zero bit in that position indicates a non-synchronous operation of the Printer. Both will be discussed in detail at a later point. Also, the N character 2^4 bit selects the unit (2^4=0 selects Unit 1, 2^4=1 selects Unit 2). If the B3 character of the instruction is a one, the N character will indicate the number of lines to advance the paper (0-14) by the line count as well. The A Address of the instruction is ignored and the B Address has three separate functions. The first function of the B Address is to specify the most significant digits of a 120-location print area. The B1 character, as a second function, will determine if a line is to be printed or if only paper advancing is to be done. The B1 character must be even to print; if it is odd, no printing will occur and only paper advancing, if any, will take place. The B2 character must be zero and the B3 character provides the third function of the B Address by acting as an indicator to designate the type of paper advance. If the B3 character is a one, the paper will be advanced using N as a count. A two in the B3 position denotes a vertical tab using a mylar tape loop and a three represents a page change by the same tape loop.

STATUS FLOW FOR PRINTING

Both the normal and simultaneous Print and Paper Advance instructions select an SIO status level after staticizing. This SIO (Sense Input Output) status level has three basic functions. Two functions of SIO are to sense the Printer to see if it is busy and/or the Simultaneous Mode (for PAS instruction) to determine if the mode is free. Both of these functions are covered in detail in Volume 1, Section 2, of this manual.

Note.-SET HO (P) is produced on Print No. 3506016, area A-3, when the Line Printer is busy [LPB(1)] and either printing or paper advancing, or both, is about to be attempted.

The third function of SIO is preparing the control logic for printing and advancing paper.

Besides the SIO status level, the Print and Paper Advance instruction uses X1 and A1 status levels for Normal Mode operation, and Y1 and S1 status levels for Simultaneous Mode operation. Both pairs of status levels serve the same functions for their respective modes. Only the Normal Mode status flow, however, will be covered in this text.

Figure 7-2 is a simplified diagram of the printing portion of the instruction. As the print drum revolves, a soft iron disc will produce a character pulse for each notch on the disc by disrupting a magnetic field, There are 64 notches to correspond to the 64 characters on the drum. An index pulse is similarly produced each time the character, minus sign, comes up on the drum. The index pulse resets the Character Counter, which is a six-stage octal up-counter, and each character pulse triggers the counter up one. At TP01 time of an X1 status level, the contents of the counter are gated onto Bus 2 and Bus 3 of the Processor. At the same time, I9 or 99 is generated onto Bus 0 and Bus 1 from the Address Generator. In memory, from 9900 to

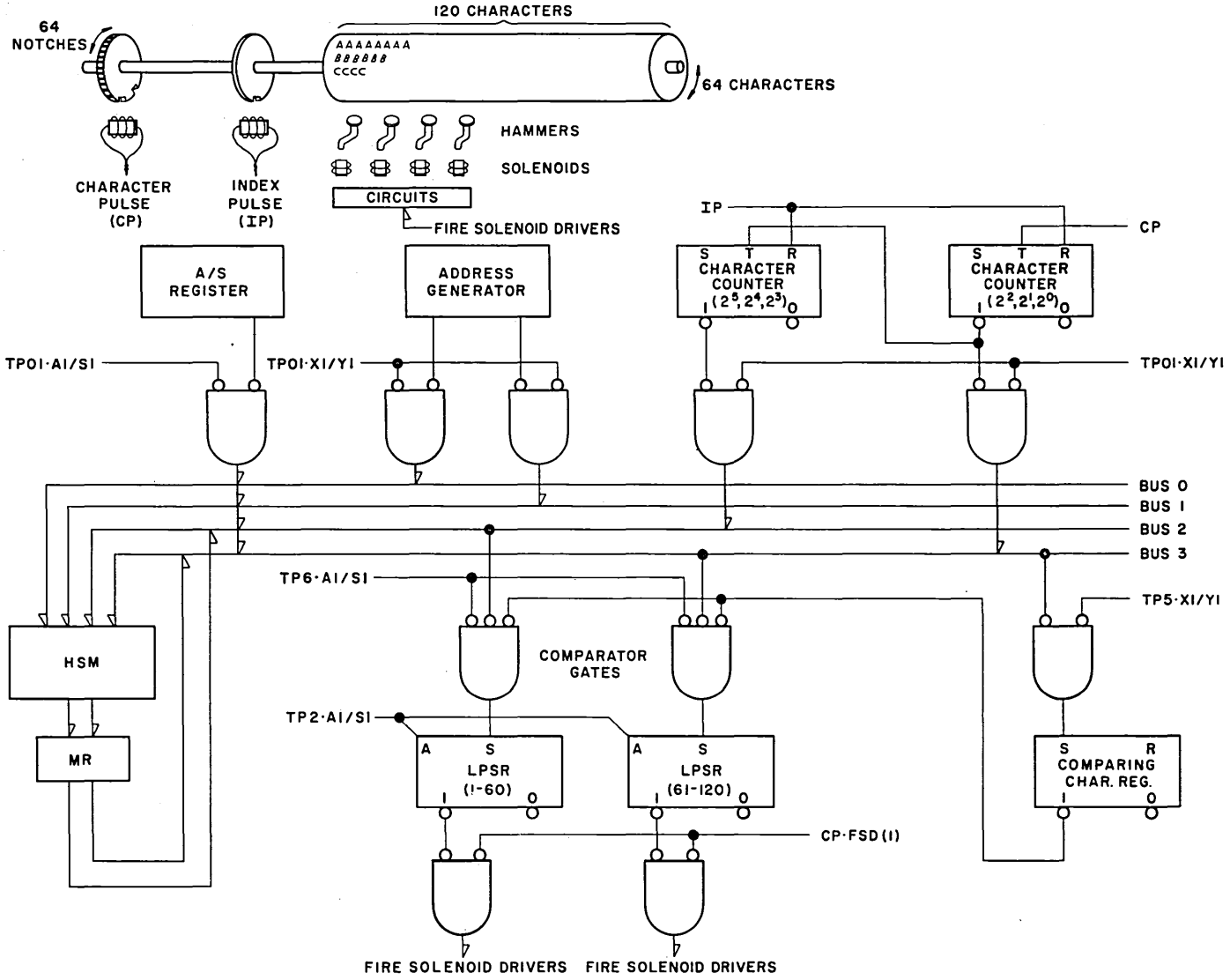


Figure 7-2. Simplified Print Logic.

9977 or from I900 to I977 (for 10K or 20K memory), a prestored table must exist like the one shown in Figure 7-3. The generated address locates the character in the table which corresponds to the character

MEMORY LOCATION	0	1	2	3	4	5	6	7	8 | 9
I90 OR 990	- MINUS	+ PLUS	SPACE	0	1	2	3	4	THESE
I91 OR 991	5	6	7	8	9	, COMMA	. PERIOD	@ AT	LOCATIONS
I92 OR 992	% PERCENT	: COLON	# NUMBER	$ DOLLAR SIGN	) CLOSE PAREN-THESIS	" QUOTE	10 SUB-SCRIPT	(OPEN PAREN-THESIS	CAN
I93 OR 993	] CLOSE BRACKET	; SEMI-COLON	> GREATER THAN	÷ DIVIDE	↑ ARROW UP	[OPEN BRACKET	< LESS THAN	= EQUAL SIGN	BE
I94 OR 994	A	B	C	D	E	F	G	H	USED
I95 OR 995	I	J	K	L	M	N	O	P	FOR
I96 OR 996	Q	R	S	T	U	V	W	X	WORK
I97 OR 997	Y	Z	CR CREDIT SYMBOL	' APOSTR-OPHE	* ASTER-ISK	& AMPER-SAND	/ SLASH	⌑ LOZENGE	AREA

Figure 7-3. Model 316 Line Printer Translation Table (10K and 20K Memory)

on the drum. This character is then read from memory and placed in the Comparing Character Register. The Computer will then execute 60 A1 status levels, bringing out a diad at a time, to be compared against the one character in the comparing register. For every match found, a one bit is inserted in a 120 stage shift register. After the 120 memory locations have been scanned and the shift register has been set up, the next character pulse triggers the firing of the hammers which correspond to the one bits in the shift register, thereby printing the character wherever it occurs in the line. Thus, one X1 and 60 A1 status levels are needed for every character printed. This requires 7 x 61 or 427 microseconds of Computer time per character on the drum.

The time between characters on the drum depends upon the speed of the drum. A speed of 1000 rpm means that 938 microseconds exist between characters, while a speed of 660 rpm provides 1420 microseconds between characters on the drum.

$$\frac{60 \text{ sec/min}}{1000 \text{ rev/min}} = 60 \text{ ms/rev} \qquad \frac{60 \text{ ms/rev}}{64 \text{ char/rev}} = 0.938 \text{ ms/char or } 938 \ \mu\text{s/char}$$

$$\frac{60 \text{ sec/min}}{660 \text{ rev/min}} = 90.9 \text{ ms/rev} \qquad \frac{90.9 \text{ ms/rev}}{64 \text{ char/rev}} = 1.420 \text{ ms/char or } 1420 \ \mu\text{s/char}$$

Therefore, the Computer has ample time to scan memory for one character, set up the shift register, and print before a new character comes up.

The N Register is initially set up to a count of either 64 or 47 during SIO, depending upon whether the Synchronous or Non-synchronous Mode is being used. Every X1 status level, N is counted down by one and upon reaching zero, the Computer will stop printing and perform the paper advance, if any (see Figure 7-4).

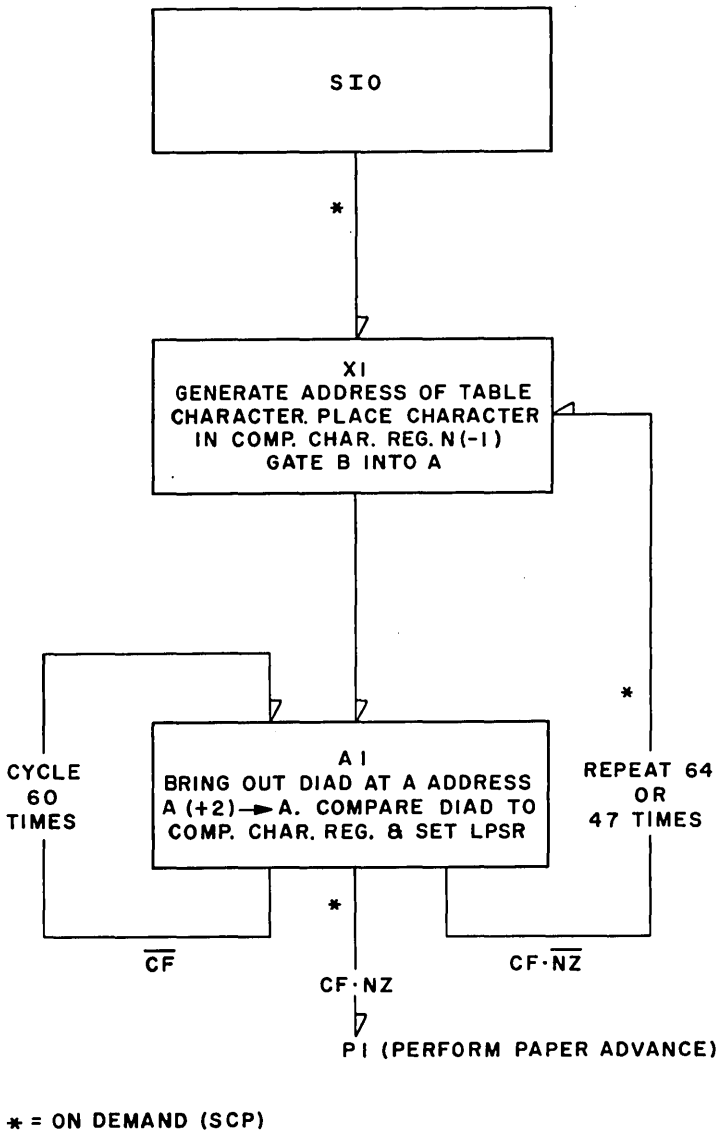


Figure 7-4. Status Flow for Normal Mode Print.

SYNCHRONOUS AND NON-SYNCHRONOUS OPERATION

A programmer has the choice of using one of two modes on the 301 Line Printer. The Non-synchronous Mode provides the advantage of printing all 64 characters on the drum, but in doing so must reduce the actual speed of printing. The Synchronous Mode prints at the speed of the drum, but must reduce the number of printable characters to 47.

Since one revolution of the drum takes 60 milliseconds (at the speed of 1000 rpm), all 64 characters could be printed in one line during that time. However, one line of paper advance will take 16 additional milliseconds including start and stop time, therefore, the Computer cannot print at the drum speed and the rate of printing is reduced from 1000 lines per minute to 790 lines per minute. This is the printing rate for non-synchronous operation at the high drum speed. Non-synchronous operation at the low drum speed (660 rpm) reduces the printing rate to 590 lines per minute.

To enable the Printer to print at the true drum speed of 1000 lines per minute or 660 lines per minute, the number of printable characters must be reduced from 64 to 47. The time it takes the drum to revolve over the 17 non-printable characters enables the Printer to advance paper one line and be ready to print a new line starting at the original point on the drum (see Figure 7-5). Synchronous operation then, is the mode of printing one line and advancing one line of paper within one drum revolution.

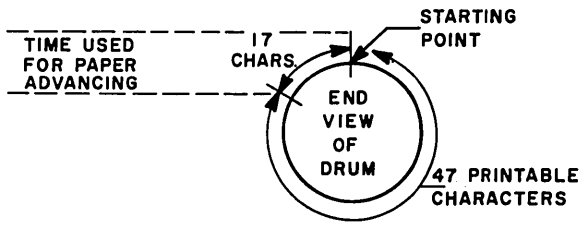


Figure 7-5. Synchronous Operation.

Since the Computer uses the same 47 printable characters every time, the control logic is wired to wait for the letter A before it starts the scan of memory. In the pre-stored table (Figure 7-3), the characters between 9940 and 9977 (I940 and I977) and between 9900 and 9916 (I900 and I916) comprise the 47 printable characters for synchronous operation. The characters, @ through = (9917 to 9937), are non-printable for the Synchronous Mode.

In synchronous operation, since the Computer waits for the character A to come up on the drum, it is obvious that unless several lines are to be printed, very little time would be saved, for in many cases almost one complete drum revolution might be wasted before the letter A comes up.

STATUS LEVEL SELECTION

Having discussed the functions of the various status levels for a PAN instruction, their actual selection and generation should be explained.

From end staticizing, the Computer automatically selects an SIO status level and executes it. During SIO, if Hold-Off does not become set and the level HON is produced, the Computer will reset P-NRQ on Print No. 3506024, area D-8, at TP3. The SIO and HON levels also have selected X1, and the STL-PT Flip-flops will contain an X1 status level at TP6, but since P-NRQ is reset, the X1 status level cannot come into existence at TPO time. When the control logic develops N-REQ, the P-NRQ Flip-flop becomes set and an X1 status level occurs. N-REQ is generated on Print No.3506016, area A-5, mainly from the Start Compute Pulse (SCP) which is produced through a one shot in area D-4 by the Character Pulse. Therefore, the first X1 status level doesn't occur immediately after an SIO, but instead must wait until the next Character Pulse from the drum. This is to insure the Computer of the full amount of time between characters for its first scanning operation. The X1 status level is thus said to occur upon a demand from the control logic. This demand is the SCP.

The X1 status level automatically selects an A1 status level. P-NRQ remains set during the X1 and 60 successive A1's, while the Computer scans 120 locations for the one character on the drum. Upon producing Count or Characher Finished (CF - Print No. 8617005, area B-6), the Computer senses that the 120 locations have been scanned and another X1 status level is selected. At the same time, on Print No. 3506024, area C-7, CF and A1•PAN resets P-NRQ at TP3. Once again the Computer must wait for the next character pulse from the drum. The next character pulse or SCP produces N-REQ, which in turn sets P-NRQ and a new series of one X1 and 60 A1 status levels occur. The same character pulse also triggers the printing of the character just scanned by firing the solenoid drivers.

For every X1 status level, the N Register is decremented by one. Upon reaching zero, the level NZ is produced and when coupled with CF, signifies the end of printing for that particular line and a P1 status level is selected. However, CF and the last A1 status level reset P-NRQ once again, and the Computer cannot continue until another character pulse is received. The last character pulse triggers the printing of the final character just scanned and again generates N-REQ to set P-NRQ and permit the Processor to staticize a new instruction, while the control logic begins the paper advance independently.

DETAILED LOGIC FOR PRINTING

During SIO, at TP123, the B Address is placed on the Bus and at TP1, if the N 2^5 Flip-flop is set, the Print Synchronous (PRT SYNCH) Flip-flop becomes set (Print No. 3506016, area C-6). This flip-flop informs the control logic of the mode of operation that is being requested by the instruction. If PRT SYNCH is set, this signifies synchronous operation and if PRT SYNCH remains reset, the non-synchronous operation is performed.

On Print No. 3506018 (AND Gate 187D1), if SIO of a PAN/PAS is present and Line Printer Busy (LPB) is reset, the level STI will be

produced at TP2. STI is an abbreviation for start instruction or start initiate and is responsible for setting up a large portion of the control logic for printing and paper advancing during SIO.

With STI, the B3 character which is on Bus 3 will set the proper flip-flop for paper advancing: Line Shift (LS) becomes set if the character on Bus 3 is a one, Vertical Tab (VT) becomes set if the B3 character is a two, and Page Change (PC) becomes set if the B3 character is a three.

STI is also involved with selecting the module that is addressed by the N character 2^4 bit. On Print No. 3506018, area C-3, STI primes AND Gate 183C3; and if the N 2^4 Flip-flop is reset, a high output is produced which sets the Select (SEL) Flip-flop. With SEL set, a high from the zero output primes OR Gate 183B1 to produce MOD SEL (N) for 316-1, which conditions the control logic used with the first unit Printer. At STI time, if SEL doesn't become set due to the N 2^4 being present, the MOD SEL (N) for 316-2 is generated and the second unit Printer control module is used. These MOD SEL levels do most of their selection by way of AND Gate 166B2 on Print No. 3506016 and the (SIO·PAN/PAS) output level.

If STI is present on AND Gate 162C1 and the B1 character 2^0 bit is absent, the Print (PRT) Flip-flop becomes set. In other words, an even B1 character which indicates printing is needed before PRT will become set. PRT will be set for the entire printing of a line and only becomes reset just prior to paper advancing by the termination level, CF·NZ. The main function of PRT is to help generate N-REQ.

In area D-3,4 of Print No. 3506018, STI also gates the N character into the Line Count Register (LCR). The LCR will hold the count of the number of lines to advance paper by line shift, thereby freeing the N Register for another function, namely, holding the count of the number of times to scan 120 locations of print area.

At TP2 of SIO, the paper advance code (B3 character) was gated from Bus 3 to set its respective flip-flop (LS, VT or PC). At TP3 then, the B3 Flip-flops will be reset and the B Register will contain the address of the first character in the 120-location print area. If a transfer to the Simultaneous Mode is effected, the address of the first character is transferred to the T Register by inhibiting the B3 character and inserting a parity bit so that T3 will contain a zero.

Also, at TP3 of SIO, the N Register (Print No. 3506027) is set to all ones and a count of either 64 or 47 is inserted, depending upon the original N 2^5 bit which indicated non-synchronous or synchronous operation. If the operation is to be non-synchronous, a count of 64 will be set up by resetting all stages except the 2^6 and if synchronous operation has been selected, a count of 47 is created by resetting only the 2^6 and 2^4 Flip-flops.

Note.-OR Gates 276D1 and 276D2 actually form a flip-flop which will become set at TP1·SIO if N 2^5 is set, indicating Synchronous Mode. Otherwise, the flip-flop remains reset to signify non-synchronous operation. This flip-flop is used to set up a count of 64 or 47.

An X1 status level of a PAN primes OR Gate 273C5 to trigger N down one and the Nine Count Adjust logic is not used during the PAN, since the Computer requires 64 or 47 triggers to obtain NZ. (See N Register Logic description in the 301 Processor Training Manual for Nine Count Adjust logic).

At TP4 time of SIO, the Line Printer Busy (LPB) Flip-flop will be set, except when printing is to be done (B1 - 2^0 (P)) during a simultaneous operation (LPNS (1N)) while the Simultaneous Mode is busy (SB (1N)). These conditions will inhibit pin 16 of AND Gate 163C1.

When set, LPB indicates the Printer and its corresponding control logic are in use and will inhibit another PAN/PAS instruction from being initiated by setting the Hold-Off Flip-flop. Hold-Off, being set, will keep the Computer cycling in SIO until the Printer is free. To reset LPB, the Print (PRT) and Fire Solenoid Drivers (FSD) Flip-flops must be reset (both flip-flops are set during printing) and the combination level, $\overline{LS(1)/VT(1)/PC(1)}$ (P), must be absent at TP6 time. This combination level will exist during the paper advance.

It should be emphasized that paper advancing is an independent operation regardless of the mode. Thus, if only paper advancing is to occur, B1 2^0 (P) will exist and will inhibit AND Gate 163D1 permitting the LPB Flip-flop to become set. The B1 2^0 bit also generates a level known as Simultaneous Paper Advance Inhibit (SPI) on Print No. 3506024, area B-2, and will inhibit setting Hold-Off for that special combination (see Volume 1, Section 2, of this Manual).

At TP6 of SIO, the Computer will select one of four status levels. If Hold-Off is set, SIO is again selected. If the level HON exists, the PAN instruction can be executed in the Normal Mode and an X1 status level is selected. If HOS exists, a simultaneous Y1 status level is selected. (HON and HOS are defined in Volume 1, Section 2.) A P1 status level will be selected if only paper advancing has been initiated (B1 2^0(1)), or if a PAS instruction has been transferred to the Simultaneous Mode (NOR 2^0 (1)), thereby freeing the Processor's Normal Mode in both cases.

As was discussed earlier, the X1 status level must wait for the Start Compute Pulse (SCP) before beginning the scan of memory. Once an X1 is begun, three basic functions will occur. The first of these functions is generating a table address at TP01. This is accomplished by gating the contents of the Character Counter onto Bus 2 and Bus 3, while the Address Generator generates I9 or 99 onto Bus 0 and Bus 1.

Print No. 3506023 contains the Character Counter (area C-2 through C-6) which consists of eight triggerable flip-flops designed to count up. The 2^0, 2^1, and 2^2 with parity give one octal number, while the 2^3, 2^4, and 2^5 and parity form the second octal number. Parity is needed in both digits to form an address.

From the logic, it can be seen that the Index pulse (present when a minus sign occurs on the drum) will reset the Character Counter and that the character pulse (present for any character coming up on the drum) will trigger the counter's 2^0 stage. Therefore, when the drum is revolving, this counter will always be triggered in synch with each character on the drum.

To gate the contents of the Character Counter onto the bus lines 2 and 3, an output from OR Gate 237B2 is needed. AND Gates 237B1 and 238B3 feed OR Gate 237B2 to handle both Normal and Simultaneous Mode operation. AND Gate 237B1 requires that Flip-flop 238B1 be set, meaning an X1 status level is selected and LPNS reset, signifying Normal Mode operation. A high from AND Gate 237C3 is also required to prime 7B1 and this level will exist if LPB is set and Paper Shift (PS) is reset. Such a combination exists for printing and not paper advancing.

The Address Generators for a 20K and 10K system are shown on Print Nos. 3506013 and 3506029 respectively. The I9 or 99 generated by X1·PAN, combined with the output from the Character Counter, forms an address which is sent to the MAR to address the prestored table at TP1. Meanwhile, the Comparing Character Register (Print No. 3506023) is reset in preparation for receiving the character from the table at TP5 time. Once the character from the table reaches the Comparing Character Register, the flip-flop outputs will be sent to the Comparator gates on Print No. 3506020, area D-2 through D-8, in the form of CC levels.

A second function of the X1 status level is to gate the B Address into the A Register at TP23 time. The B Register will always hold the initial starting address of 120-location print area while the A Register will be used to address the individual diads during the process of scanning. The third function of X1 is to count N down by one at TP3 (Print No. 3506027, area C-3).

To obtain N-REQ and thereby produce the first X1 status level after SIO, the START SCAN Flip-flop must be set (Print No. 3506016, area C-2). START SCAN could have been set by the level STI during SIO for non-synchronous operation. If this were the case, then the next character to appear on the drum would initiate an X1. However, if PRT SYNCH became set during SIO (indicating synchronous operation), START SCAN could not become set with the level STI. The printer logic must then wait for the letter A on the drum before START SCAN can be set and the first X1 status level can be generated. This is accomplished by the CC 2^5 (ON) level on OR Gate 165C1. Once the Character Counter reaches an octal count of 40, the CC 2^5 Flip-flop will become set and the letter A will be appearing under the hammers on the drum. If CC 2^5 is set, the (ON) level will go high and trigger START SCAN to the set state. The Computer will now initiate an X1 and 60 A1 status levels to scan for the letter A. It should be pointed out that once START SCAN is set, the zero output inhibits the triggering by CC 2^5 since a constant high is applied to the flip-flop and a low to high going edge is needed to trigger. Thus, START SCAN will remain set until paper advancing is begun, at which time the PS Flip-flop will reset START SCAN.

The A1 status level has one basic function, namely, to bring out two characters from the print area in memory and compare them to the one character in the Comparing Character Register. For each match found, a one bit is inserted in the Line Printer Shift Register (LPSR) and the bits are advanced during the next A1.

At TP01 of A1, the A Address is sent to the MAR and to the Bus Adder to be modified by +2. Also, at TP1 of A1, the FSD Flip-flop is set (Print No. 3506016, area B-2). This flip-flop is a necessary prime along with the Character Pulse to drive the solenoid drivers corresponding to the one bits in the LPSR. Since the first CP is needed to initiate the scan of memory for the first character on the drum, the hammers should not be energized for the first CP and FSD will do the inhibiting. The first A1 status level sets FSD, and when the next CP occurs, the hammers will be fired to print the character just scanned. Each succeeding CP will fire the hammers as well since FSD will not become reset until PRT does, which is at the end of printing.

The LPSR never becomes reset but is always being primed for zeros. At TP2 of A1, an advance pulse is generated on Print No. 3506020, area C-6, and two zeros are advanced into the LPSR. At TP6 time, if a compare exists between the character on Bus 2 and the character in the Comparing Character Register, the first stage of LPSR is set. The second stage is also set if a compare exists with the character on Bus 3. (Note that the characters on Bus 2 and Bus 3 came from the print area in memory at the A Address.) The next A1 status level will bring out two new characters while the result of the first comparison as well as two more zeros are advanced into the LPSR. Hence, if no comparison occurs, only zeros are advanced into the shift register and when a comparison does occur, a one bit is inserted.

Note.- Assuming that the stages being primed for zeros are stages 60 and 120, then stage 1 connects to column 1 and stage 61 connects to column 2 on the Printer. Furthermore, stage 60 connects to column 119 and stage 120 connects to column 120. All odd numbered columns connect to stages 1 through 60 while all even numbered columns connect to stages 61 through 120. See the chart in area B2 on Print No. 3506020.

It should be pointed out that if an octal 17 is placed anywhere in the table instead of the character that normally occupies that location, the Print Inhibit (PRT INH) Flip-flop on Print No. 3506023,

area B-2, will become set when that location is addressed. This flip-flop inhibits setting LPSR; thus, only zeros are inserted and that particular character will not be printed.

From the A1 status level, the Computer will select another A1, provided the CF level doesn't exist. CF will occur when the A Register reaches B initial plus 120. Since A counts up by 2 for each A1, it will take 60 A1 status levels to scan 120 locations and generate CF. With CF generated, the Computer will reset P-NRQ and select an X1 status level, provided NZ is not present. When the next character pulse occurs, X1 is generated, the character just scanned is printed and a new character is set up in the Character Counter, thereby starting a new scanning process all over again.

When NZ and CF are produced, a P1 status level is selected and printing will terminate. The combination level, NZ·CF, will reset the PRT Flip-flop on Print No. 3506016, area D-2, upon the final SCP pulse. When PRT becomes reset, FSD does as well. At TP4 with PRT reset, AND Gate 162B2 produces a high output which resets PRT SYNCH (area C-5). Since FSD is reset, the hammers cannot be energized; thus, no printing will occur and the paper advance is initiated.

PAPER ADVANCE LOGIC

Paper advancing is begun by generating the level SET PAD on Print No. 3506016, area A-6. This is accomplished by AND Gate 167B4 which requires FSD and PRT reset, LPB set, and PS reset, all of which denotes printing has finished and the paper advance hasn't begun yet. SET PAD is used on Print No. 3506018, AND Gate 186C2. If one of the three flip-flops (LS, VT or PC) is set, OR Gate 186C1 will produce a low output which, when coupled with SET PAD, will set the Paper Advance (PAD) Flip-flop. Once this flip-flop becomes set, the Printer will begin to move paper and will stop the paper only when PAD becomes reset.

When PAD becomes set, Paper Shift (PS) is set upon the following TP6. PS indicates paper is currently in the process of being advanced, and doesn't become reset until the module is freed.

If the paper is advanced by Line Shift, the Computer will count the number of lines in the LCR. In area D-2 of Print No. 3506018, PAPER FEED STROBE occurs with every line advanced by the Printer and triggers LCR down one. When the LCR reaches zero (all stages reset), the level LCRO is generated. LCRO, with the set output from the LS Flip-flop, primes AND Gate 186C2 which resets PAD and stops the paper.

If paper is advanced by the mylar tape loop, the levels VERTICAL TAB (N) and PAGE CHANGE (N) will be generated when a hole is sensed in the proper column (2^0 channel for VT and 2^1 channel for PC). Each level is coupled respectively with its corresponding flip-flop (VT or PC) set output on AND Gates 185C1 and 185C2. The outputs of these gates reset the PAD Flip-flop.

The output from OR Gate 185B1 is labeled PAD RESET (P). This level is used on Print No. 3506019 to set Flip-flop 195C1. Once 195C1 is set, each SCP pulse will trigger a binary counter up one. When the counter reaches a count of seven, a combination level called (RESET LS, VT, PC) is generated in area B-6. The purpose of this logic is to let the paper stop completely before the Printer frees the control module. Seven SCP pulses amount to at least seven milliseconds at the fast drum speed. The level (RESET LS, VT, PC) resets the three flip-flops on Print No. 3506018, which in turn produce a low output from Inverter 186B2. With $\overline{\text{LS(1)/VT(1)/PC(1)}}$ (P) now low, the LPB Flip-flop becomes reset on Print No. 3506016, area D-3 and C-3. Line Printer Housekeeping (LP HSK) is then produced from AND Gate 164C3 at TP1 to clear the module for a new instruction.

Besides paper advancing by instruction, the Printer has a button labeled TOF (Top of Form). Essentially, pushing this button causes a Page Change. On Print No. 3506019, when TOF is depressed, Flip-

flop 194C2 becomes set, thereby generating TOF (IN). TOF (IN) will set the PC Flip-flop on Print No. 3506018 by way of AND Gate 185D2, providing FSD is reset. This means TOF will not work during printing. At the same time PC becomes set, AND Gate 187C3 sets PAD, initiating paper advance by Page Change. Paper is stopped in the same manner as before with Flip-flop 194C2 becoming reset with PAD RESET (P).

ACCURACY CONTROL AND IOS INSTRUCTION

There are three flip-flops involved with accuracy control on Print No. 3506016, area B-7. If bad parity exists on Bus 2 or Bus 3 at TP5 of an A1 status level, the Write Error (WE) Flip-flop will become set. If bad parity exists in the Comparing Character Register, the Read Error Flip-flop will be set at TP5 of an A1 status level. The Device Does Not Follow (DDF) Flip-flop is set when LOW PAPER is sensed during SIO of a Page Change or when the Operable level is lost while the Printer is busy. Any one of these alarms produces Printer Alarm (PRA) in area A-8, which in turn resets FSD to stop printing. Each of the three alarms feeds the stop logic to stop the Computer as well.

AND Gate 184B5 will be primed if an Input-output Sense instruction is testing the Printer (7 or G for N Character -- see 301 Programmers' Reference Manual). If the Printer is printing, FSD or PRT will be set and OR Gate 183A1 will generate the level MOTION (P). This level is used on Print No. 8617005 to indicate the Printer is printing. If the Printer is advancing paper, PS is set and the level REVERSE is sent back to the Processor. These two levels are used in the Tape Station tests with the same A0 character bits. If the Printer is inoperable, the level, Inoperable, is generated from low paper or loss of the Operable level.

The On-Line Printer Control, Model 396-1, permits a 160 column printer (Model 335) to be connected to the 301 Processor. An additional control module (396-2) allows the use of a second 160 column printer. The only differences in the logic of the 396-1 control, as compared

to that of the 316-1 control, are the shift register and the CF recognition gate. The shift register must contain 160 stages and Gate 6B1 on Print No. 8617005 must recognize A initial plus 160. (A1 - 2^0 (1), A2 - 2^2 (1) and A2 - 2^1 (1))

The highest speed of the 335 drum is 1070 rpm, and there are 66 character positions on the drum, three of which are blank. The space character is represented by an underline. At this high drum speed, the time between characters is approximately 850 microseconds, and since the Simultaneous Mode requires 1134 microseconds to scan memory (81 status levels at 7 microseconds each X 2 = 1134 microseconds), the Simultaneous Mode cannot be used.

The low drum speed of the 335 Printer is 715 rpm. Thus, 1270 microseconds exist between characters at this speed, and since the Simultaneous Mode requires 1134 microseconds to scan memory, there is sufficient time between characters to execute a Simultaneous Print and Paper Advance instruction at the lower drum speed.

301 DATA RECORD FILE CONTROL

GENERAL INFORMATION

The Data Record File, Model 361, is a high capacity, random access, input-output storage device. Data is recorded magnetically on discs 6-7/8 inches in diameter. The outer half of each disc contains a band of magnetic-oxide coated mylar, upon which information is recorded. The inner half of the disc consists of 23 spiral grooves, used to provide head-tracking accuracy.

Data is recorded as blocks of information on two interwoven bands on each side of the disc at a rate of 2.5 KC. Each block is recorded in a cell and each band contains ten cells.

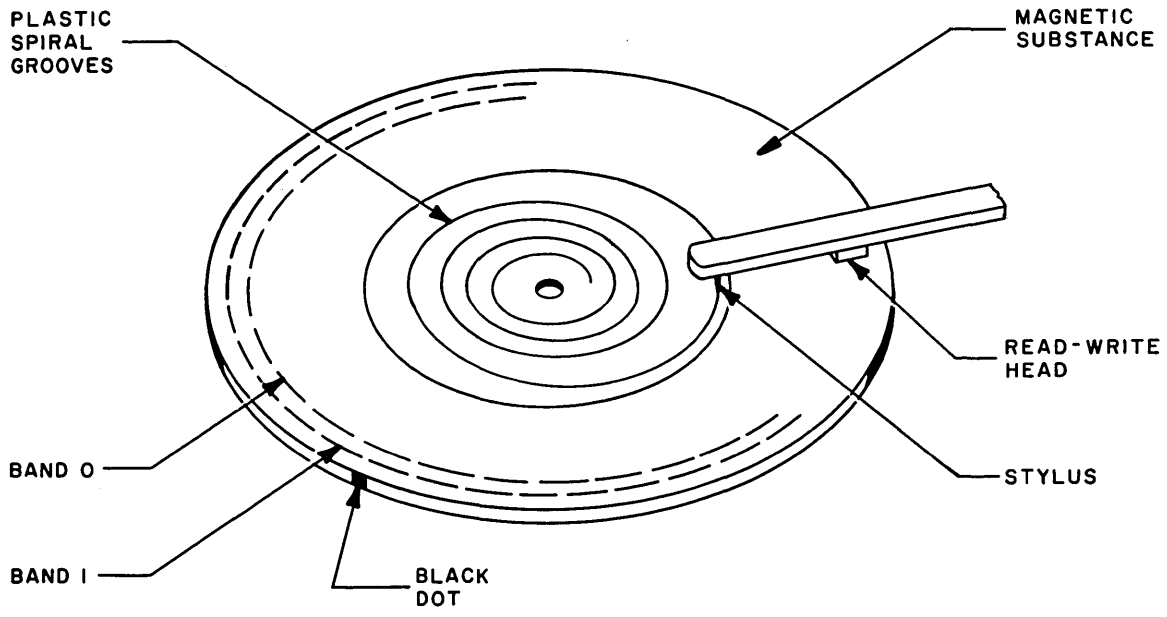


Figure 8-1. Disc Tracking, Simplified Diagram.

A cell is a fixed time length rather than a physical length due to the fact that recording is done spirally. Each cell is 400 milliseconds long (two revolutions of the disc) and starts and finishes always at the same points on the disc. The start and finish of a cell is indicated by a control signal called a Block Pulse. This Block Pulse will also signify the start of the next cell in sequence. A cell will always contain one block of information.

A block may be defined as consisting of from one to nine hundred characters of information. It must end with an EB control symbol, if the block consists of less than 900 characters. All information transfers involving the Record File must be accomplished by means of blocks of information.

Each Record File unit has a complement of 128 records stored in a cage or basket. This basket is round and carries the records in individual slots separated by wire spacers. The basket is mounted vertically on a horizontal shaft and is able to rotate in either direction to ensure maximum efficiency for record selection. When the discs are in the upper portion of the basket, they are held in by gravity, and when in the lower half of the basket, they are held in by two rubber belts. All information is recorded in serial fashion, using a modified NRZ type of recording. Not only the characters, but also the bits of the characters are recorded serially. The 2^0 bit is recorded first and 2^6 bit last, maintaining good odd parity. There is no timing track recorded on the disc.

Since 900 characters maximum are recorded per block with one block per cell, ten cells per band, and 512 bands per Record File unit, there are a total of 36,000 characters recorded on each disc, or a total of 4.6 million characters recorded in one Record File unit. Each of the 512 bands are individually addressable with one Band Select instruction, while each of the ten cells within a band are individually addressable during a Block Read or Block Write instruction. This gives a total of 5,120 individually accessable cells, each of which can contain an item of information in block format.

Access time to a selected band varies from one to 3.5 seconds, depending upon where, in the basket, the record containing the band is located. After the band is selected, access time to a cell on the band will vary from 1.5 to 5.1 seconds, according to which cell on the band is addressed.

Two Record File units can be utilized with one Processor along with their respective control modules, 317-1 or 317-2.

PROGRAMMING

In order to understand how the Record File is programmed, it is necessary to understand how the device works mechanically.

Before information can be read or written, the block on a disc which contains this information must be chosen. Before this can be done, the band which contains this block must be chosen from the 512 that are in the basket. Thus, before information transfer can take place, a Band Select Normal instruction must be performed.

Band Select Instruction (BSN) (D)

This instruction will cause the Control Module to send to the Record File unit the address of the selected band. The Record File unit will then receive the address, and if the parity of the address is good, the unit will then search through the basket to find the record that contains the selected band.

When the band is found, the record will be taken from the basket by a transfer arm and placed on a turntable. The turntable is located on top of the unit and is belt driven by an AC motor at 300 rpm. The disc is placed on the turntable so that it may be used.

Mounted adjacent to the turntable is the read-write head transport arm. It is used to support and move the head and stylus, so that the head and stylus may be placed on the disc on the turntable when infor-

mation transfer is to take place. It moves out of the way when the disc is being rejected or a new disc is being selected.

The R-W transport arm has three fixed positions it may attain; namely, Reject, Ready and Play. Reject position is reached when a disc is rejected. The arm is then at an angle of approximately 45 degrees above the horizontal. Ready is reached when a Band Select instruction has just been performed or a Read or Write, where the disc is not rejected. It is reached at approximately 15 degrees above the horizontal. This is the position the arm must be at before a Read or Write instruction can be executed. The Play position is reached when the transport arm has placed the head and stylus on the disc so that information transfer may occur.

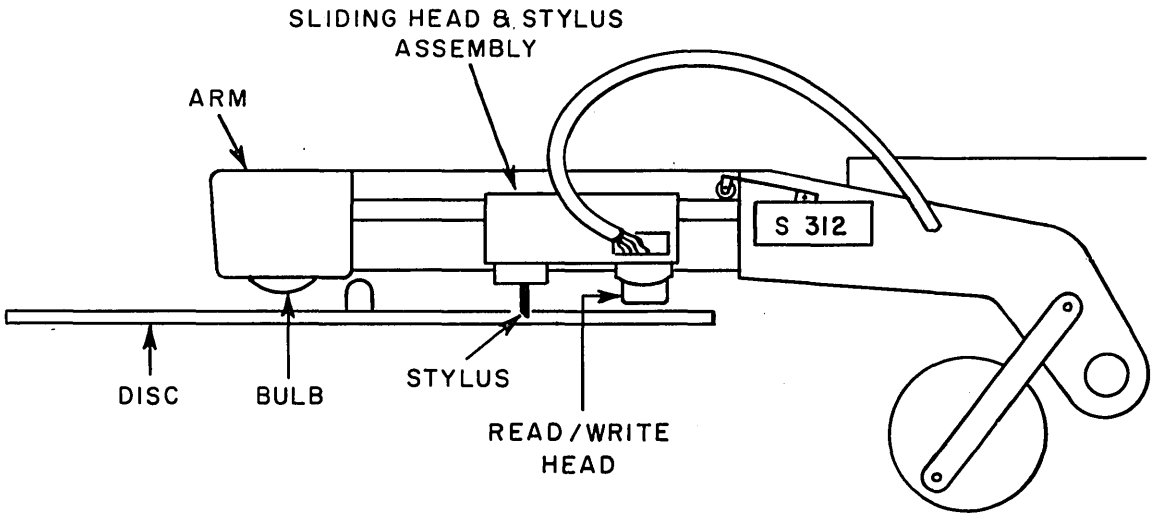


Figure 8-2. Record File Head Assembly (Play Position).

When the record has been placed on the turntable by the transfer arm, the R-W transport arm will then move to the Ready position. Then, the correct band on the "up" side of this disc is chosen.

The Read-Write head has two channels with two windings per channel. One winding is for reading or writing; the other winding of the channel is for erase. One channel of the head, the one nearest the center of the disc, is used for Band 0. The other, nearest the periphery of the disc, is used for Band 1.

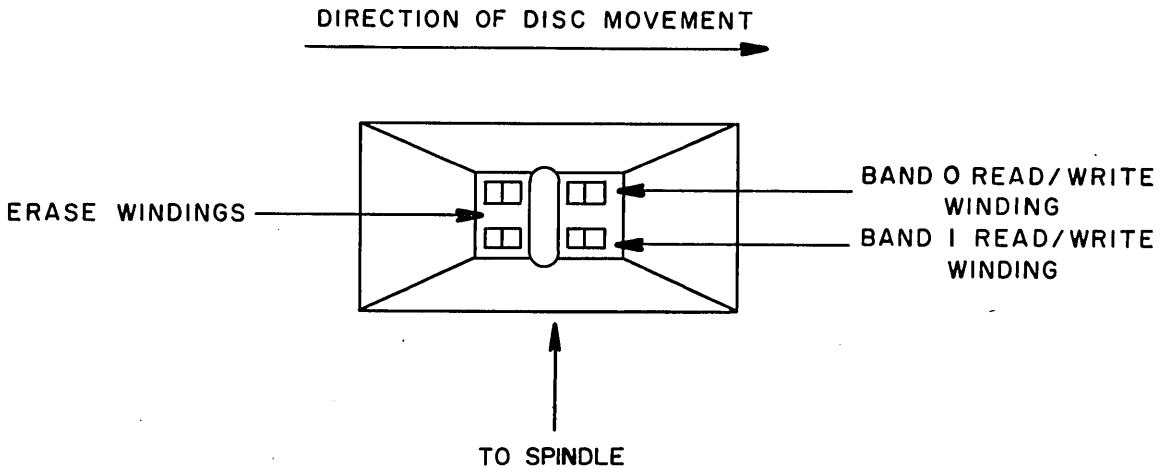


Figure 8-3. Read/Write/Erase Head (Bottom View).

One channel of the head or the other will be chosen to make the final selection as to what band on the disc is to be used. Any one of the bands in the basket, numbered from 000 to 511 may be selected in this manner.

The Band Select Normal instruction need only be performed once if the selected band is to be used more than one time. Another BSN need be performed only if a different band is required.

The N 2^0 bit of the BSN instruction indicates a special case, if present. It indicates that the programmer knows that the new band that is desired is on the up side of the disc already on the turntable. It should be the band that has not been previously selected. This N 2^0

bit will not allow the mechanics of the unit to reject the disc on the turntable but will cause the R-W head merely to switch from one channel to the other. Thus, it has selected the other band on the up side of the disc. No time is wasted for any mechanical operation.

The following formula may be used to determine which record and on what side of the record a particular band is on:

$$\frac{\text{Band No.}}{4} = \text{Record No.}$$

A remainder of 0 indicates band 0, side 0
A remainder of 1 indicates band 1, side 0
A remainder of 2 indicates band 0, side 1
A remainder of 3 indicates band 1, side 1

The zero side of the disc is the one marked with a serial number. The record positions are numbered on the hub of the basket just below the record slot from 000 to 127. The small arrow between each number indicates the direction the zero side of the record should face.

Read/Write Instruction [BRN/S(F/G)·BWN/S(H/I)]

The purpose of a Read or Write instruction is to transfer a specified number of blocks of information to or from the Record File and Memory. This instruction will first find the selected cell, allow transfer of information between it and memory and any other sequential blocks specified by the instruction.

The instruction works by causing the R-W transport arm to lower the head and stylus onto the disc. The arm will be in the Play position. The stylus will then engage in the first groove of the disc and pull the R-W head radially across it. The stylus must move three grooves into the disc before the head is positioned over the start of the first cell of either band. These three grooves of travel allow the head time to stop any bouncing that may have occurred when it was forced onto the moving disc.

It is then determined whether the first cell is the starting cell. If it is, the information transfer will begin. If the first cell is not the starting cell, then the head will travel over cells until the starting cell is found. The transfer of information will begin using the specified number of blocks. The instruction will then terminate, causing the R-W transport arm to go to either the rollback (Ready) position or to reject the record.

The maximum number of blocks of information that can be transferred is ten. This number will decrease in inverse proportion to the number of the starting cell. At all times, the maximum number of blocks available for information transfer will be equivalent to the tens complement of the starting cell number.

Example:

10 minus starting cell No. = Number of available blocks
10 minus No. 4 cell = 6 blocks

CONTROL LOGIC

Band Selection

The Band Select Normal instruction will cause the Record File unit to search through the basket, pick out the record which contains the addressed band, place it on the turntable, and position the R-W transport arm at the Ready position. All the mechanical operation will be carried on off-line from the Processor. The control module needs only an SIO status level to initiate the instruction, and time pulses from the Processor to perform it.

The Record File uses relay logic and since a relay is a binary device, the Record File must be binarily addressed in order to perform a Band Select. The B_1, B_2 and B_3 characters of the Band Select instruction contain a binary coded address using decimal positional notation. Because this is true, the Band Select instruction must perform a trans-

lation from decimal to binary in order to properly address the Record File.

Band Address Translation (Decimal to Binary) - The Record File, during a BSN, is addressed by a nine bit binary address, 2^0 - 2^8, including three parity bits. The address takes this format:

$$P3\ 2^8 \quad P2\ 2^7\ 2^6\ 2^5\ 2^4 \quad P1\ 2^3\ 2^2\ 2^1\ 2^0$$

P stands for Parity. Good odd parity is maintained in each of the three segments of the address, giving overall odd parity. Any address from 000 to 511 can thus be represented.

In order to understand the operation of the translation, it is necessary to remember that a decimal number is written using positional notation. A three-digit number (such as the Band Address) will thus represent $10^2 + 10^1 + 10^0$. It can also be stated that the 10^0 character represents the units digit of the address, the 10^1 the tens digit, and the 10^2 character the hundreds digit.

The number 258, then, actually indicates 8 + 50 + 200 = 258. The control module takes advantage of this fact to perform the translation using a process of binary addition.

This addition is performed in a triggerable up-counter consisting of 2^0 - 2^8 bits, including P1, P2 and P3 in the format of the binary band address. This register is the Record File Address Buffer (RFAB). In conjunction with this are the One Digit Counter (ODC) used to store the B_2 character (tens character), and the Address Translation Register (ATR) used to store the B_1 character (hundreds character). The B_3 character of the Band Address is stored in the RFAB in the 2^0 - 2^3 and P1 flip-flops. The transfer of these characters to their respective buffers takes place during SIO. The actual translation will take place after SIO, using only TP's from the Processor.

Since, in 301 code, a decimal number is its actual binary equivalent, the RFAB will initially contain the units character (in binary form).

To this number it will add the tens and hundreds characters in their binary form. After SIO, the control module will then proceed to add to the number initially in RFAB ($8 = 1000_{(2)}$) as many binary tens ($2^1 + 2^3$) as are indicated by the B_2 character in the ODC.

Since the character in ODC is a 5, binary ten will be added to the 8 in RFAB five times. $5 \times 1010_{(2)} = 110010_{(2)} = 50_{(10)}$. This procedure is accomplished by first triggering the highest order bit (2^3) and then lower order bit (2^1) of the RFAB five times. The sequence in which the bits are triggered is determined by the Sequencing Counter (SC).

When the addition of binary 10, five times, has been completed, RFAB will then hold binary 58. Now the addition of binary 100 must be performed. The 2 from ATR is then gated into ODC to control the number of times that binary 100 is being added.

Again, as the addition takes place, the Sequencing Counter (SC) will control the sequence in triggering of bits. Since binary 100 is 1100100, the 2^6 bit is first, then 2^5, then 2^2. Thus, the triggering is still from the highest order bit to the lowest. Binary hundred is then added twice, effectively adding binary 200 to the binary 58 in RFAB, giving binary 258 as the result. This address will be sent to the Record File unit and will initiate the Band Selection mechanics.

The approximate time to perform this translation may be determined by the following formula:

$$(3 \times 7 \times B_2) + (4 \times 7 \times B_1) = T \text{ in microseconds}$$

The formula is derived from the fact that it takes three periods of seven microseconds each to perform a single addition of binary 10, and this is multiplied by the B_2 (tens) character. It takes four periods of seven microseconds to add binary 100 and this is multiplied by the B_1 (hundreds) character. The B_3 character is initially in correct binary form. The preceding formula does not apply when translation of the address, 000, is performed. This translation would require seven microseconds.

Band Selection Logic

The majority of the logic for BSN is found on Print Nos. 8617638, 639 and 641. During TP3 of SIO, the B_3 character is gated into the 2^0 - 2^3 flip-flops of RFAB, to form the base of the binary address. The B_2 character, the tens character of the address, is gated into the ODC, a triggerable down counter. The B_3 character, the hundreds character of the address, is gated into the ATR. In the control logic on Print No. 8617641, RFB and SEL will be set, indicating that a Band Selection will be taking place.

The actual translation is performed by adding binary ten (1010) to the RFAB successively according to the tens character in ODC, then adding binary one hundred (1100100) to RFAB, according to the hundreds character which was transferred to ODC from ATR. This is done by sensing for a zero in ODC before triggering, then triggering until the ODC character is equal to zero. When the translation is complete, as signified by the Decoding Complete (DCC) Flip-flop becoming set, a 35 millisecond one-shot gates the address over to the Record File unit and allows Band Selection to occur. From the sequence involved, the maximum translation time is approximately 301 microseconds, the average being 150 microseconds.

The RN 2^0 Flip-flop, when set, will indicate that the desired band is on the up side of the disc already on the turntable. The setting of this flip-flop will save time mechanically, because the disc will not be rejected and then selected again by the transfer arm. Translation of the address will be accomplished even though the RFABA 2^0 Flip-flop will indicate which band on the disc will be selected.

Band Selection Sequencing Example - The B Register holds 0111, therefore, band 111 will be selected. The binary configuration of $111_{(10)}$, minus parity, is $1101111_{(2)}$.

At SIO·TP3, BB level on Print No. 8617638, area C-2, gates the B_3 character from Bus 3 into RFAB 2^0 - 2^3, therefore, RFAB 2^0 and RFABA 2^0

will be set. PAR 1 (6384B2) will be triggered set. B_2 is gated to the ODC and B_1 is gated to ATR. SIO will then be lost and the translation would now be dependent on Processor TP's only.

TP1 -- AND Gate 6385D2 is enabled and, in turn, primes AND Gates 6385C3, 5C4, 3C3, 3C4 and 2C2. SC 2^0 and SC 2^1 (6382D1 and 6384D1) being set will inhibit triggering at this time, thus RFAB holds $000000001_{(2)}$.

TP3 -- The output from AND Gate 6385D1 triggers SC 2^0 and SC 2^1 reset (OO). AND Gate 6383D1 is now permissive, and primes AND Gate 6383C3.

TP1 -- The inverted output from AND Gate 6385D2 permits AND Gate 6383C3 (ATH is reset at this time) to trigger RFAB 2^3 set. RFAB now holds $000001001_{(2)}$.

TP3 -- The output from AND Gate 6385D1 triggers SC. AND Gate 6382D2 is enabled, and primes AND Gate 6382C2.

TP1 -- The inverted output from AND Gate 6385D2 permits AND Gate 6382C2, which in turn triggers RFAB 2^1 set. Also, the output from AND Gate 6382C2 sets the Trigger One Digit Counter (TODC1) via OR Gate 6384C6. RFAB now holds $000001011_{(2)}$. A binary ten has been added to the character which was gated from B_3 to RFAB.

TP3 -- Since one addition has been completed, the ODC on Print No. 8617639 will be triggered down once to zero via AND Gate 6392C5. Also, AND Gate 6385D1 is enabled and triggers SC.

TP4 -- The output from AND Gate 6394B2 sets the Counter equals Zero (CZ) Flip-flop and triggers ATH set. This indicates that the addition of tens is now complete, and that the addition of hundreds will now be accomplished.

TP5 -- On Print No. 8617638, AND Gate 6385C4 is enabled, and sets SC. Also, CK PAR(N) is generated via Inverter 6384C2.

TP0 -- TDOC1 is reset.

TP1 -- AND Gate 6385D2 is enabled, but since AND Gates 6383D1, 3D2 and 2D2 are inhibited, RFAB cannot be triggered. ODC is reset via AND Gate 6397C4.

TP2 -- On Print No. 8617639, since CZ is set, AND Gate 6397C2 is permissive and generates a gating level to gate the ATR into the ODC.

TP3 -- AND Gate 6394B3 resets CZ. SC on Print No. 8617638 is triggered reset by AND Gate 6385D1, thus permitting AND Gate 6383D1.

TP1 -- The inverted output from AND Gate 6385D2, since ATH is set, will enable AND Gate 6385C3 to trigger RFAB 2^6 set. RFAB now holds $001001011_{(2)}$.

TP3 -- AND Gate 6385D1 triggers SC to 01. AND Gate 6382D2 is now permitted, and primes AND Gate 6385C4.

TP1 -- AND Gate 6385D2 permits AND Gate 6385C4, which triggers RFAB 2^5 set. RFAB now holds $001101011_{(2)}$.

TP3 -- AND Gate 6385D1 triggers SC to 10. AND Gate 6383D2 is now permitted and primes AND Gate 6383C4.

TP1 -- The inverted output from AND Gate 6385D2 permits AND Gate 6383C4, which triggers RFAB 2^2 set. Also, AND Gate 6383C4 permits OR Gate 6384C6 to set TODC1. RFAB now holds $001101111_{(2)}$, which is equal to decimal 111. The decimal to binary translation is now complete.

TP3 -- On Print No. 8617639, TODC1 (ON) is used through OR Gate 6392C4 to trigger ODC to zero.

TP4 -- AND Gate 6394B2 sets CZ and triggers ATH reset.

TP5 -- On Print No. 8617638, AND Gate 6385D4 resets SC, and generates CK PAR(N) via Inverter 6384C2.

TP6 -- On Print No. 8617639, AND Gate 6394A2 sets DCC. On Print No. 8617638, since DCC is set, which indicates decoding completed, a 35 millisecond One-Shot (6388B1) is fired via AND Gate 6388C4. This produces a gating level to send the binary address to the Record File unit via the Record File Address lines.

The pin 5 output from One-Shot 6388B1 is used on Print No. 8617641 to set Flip-flop 6418D1. When the Ready pulse is finally received, AND Gate 6418D2 is permitted, and at TP6, will reset the Record File Busy (RFB) and Select (SEL) Flip-flops. The control module is now free.

Pin 5 of 6388B1 is used to set Flip-flop 6418D1. When the Ready pulse is finally received, 6418D2 is permitted, and at TP6, will reset RFB 6417B2) and SEL (6416B1). The control module is now free.

At TP3 of SIO, P-NRQ was reset. The Processor cannot begin staticizing another instruction until P-NRQ is set at TP5, when SEL is set, CZ is set, and ATH is reset. This will occur just before DCC is set, and the decimal to binary translation is complete. NOR REQ is generated by AND Gate 6404B7, to allow the Processor to staticize the next instruction in sequence.

Reading and Writing

All information transfer in the Record File is by means of blocks of information; a block consisting of from 1 to 900 characters, ending with an EB symbol, if less than 900 characters are recorded. Because there are ten cells per band and only one band may be selected at a time, a maximum of ten blocks of information may be read from or written to with one instruction. The maximum is variable, depending upon the starting block addressed by the B_3 character of the Block Read or Block Write instruction.

One block of information is contained within one cell in the Record File, a cell being defined as a fixed time length of 400 milliseconds. One cell is equal to two revolutions of the disc. A control signal, called a Block Pulse, is generated in the Record File unit to designate the starting point of each cell.

This Block Pulse is produced by a black marker placed on the edge of the disc, and is sensed for by photo-transistor circuitry. This pulse will only be produced when the head is resting on the disc. The Block Pulse is used extensively throughout the logic.

When reading or writing, the control module is used primarily to gate only the specified information from the Record File to Memory, or vice-versa. It has no buffer of its own for storing information, since each Record File unit has its own read and write buffer.

Basic Unit Writing - Writing in the Record File unit is accomplished by a modified Non-Return to Zero (NRZ) type of recording. Each character is recorded serially, and since only one channel is being recorded, each bit of a character is written serially. The 2^0 bit is recorded first, 2^6 bit last, maintaining good odd parity.

Since the transfer rate of the Record File is 2.5 KC, each character will occupy a 400 microsecond space on the disc. Seven bits of the character are recorded and there is a gap generated between each character. The 400 microsecond space is divided into eight 50-microsecond spaces. The first seven spaces each contain a bit of the character, 2^0 - 2^6, while the eighth space is the inter-character gap.

If a character is to be written, a Demand pulse is produced to place a character in the "Write Buffer", a shift register. The timing of the unit, controlled by a 40 KC oscillator, indicates the beginning of each bit space by generating a flux change on the disc. This is produced by a pulse called CP1.

If a one bit is to be written, as indicated by a one bit being present in the output of the shift register, a CP2 pulse will generate a

second flux change on the disc. This second flux change, if present, will be recorded 25 microseconds after CP1. The next CP1 is produced 25 microseconds later. This procedure continues for the entire seven bits of the character, since CP1 is the advance pulse for the shift register.

Before writing to a selected cell can start, the control module must send a Write Command level to the Record File unit. This will cause a 15 millisecond gap to be generated in the beginning of the cell and start the timing of the unit.

The timing will then produce a Demand pulse to request an A1/S1 status level. The status level will be used to take a character from memory so that the control module can gate it from the MR onto Bus 3 and into the "write buffer" of the unit. The Demand pulses will be received by the control module once every 400 microseconds, as long as the Write Command level is gated to the unit.

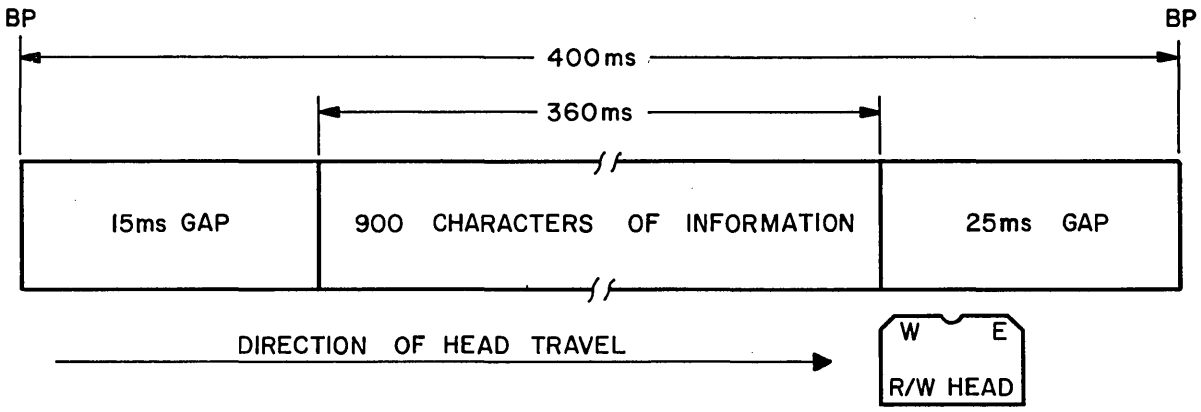


Figure 8-4. Cell Format of 900 Character Block.

After all information within a block is written to a cell, the Write Command level is lost and the rest of the cell is erased until the next Block Pulse is received.

Simplified Reading - It will be assumed that during a previous BSN, a specific band had been selected and the record containing that band was placed on the turntable. The transport arm will then be at Ready.

A Read instruction (BRN) could then be performed. This instruction would cause the transport arm to place the stylus and head in contact with the disc. This is done by a Run level produced during SIO. Since the disc is continuously rotating, the stylus would begin to pull the head across the disc.

Eventually, the first Block Pulse would be produced. This would occur about 1500 milliseconds after SIO, assuming time for the motion of the transport arm from Ready to Play.

During SIO, the B_3 character of the BRN instruction was gated into the ODC, a triggerable down counter. The character will be sensed for zero to determine when the transfer of information can take place from the selected starting cell.

If ODC is not zero when the first Block Pulse is received, this indicates that the first cell is not the starting cell, therefore, any information in this cell, even though each character will produce a Demand pulse, will be ignored. The next Block Pulse would be used to generate a trigger for ODC and the logic again senses for zero.

This procedure would continue until the character in ODC was equal to zero. Upon receiving the next Block Pulse, the control module would realize that this was the beginning of the starting cell and information transfer could begin. At this time, the Block Pulse is then used to develop a trigger for the N Register since it indicates the number of blocks of information to transfer. The instruction will terminate when N is equal to a decimal zero (2^0 - 2^3 bits are reset).

In the Record File unit, each character that is read from the disc is placed in a buffer which has direct parallel output onto Information Read-Out Lines (INFRO). These lines come into the control module.

Each character read from the disc will generate a Demand pulse, which will request an A1 or S1 status level in order to place this character into memory.

When the control module receives this Demand pulse, it decides whether it came from a block within a selected cell (by looking at ODC). If it has come from a selected cell, the Demand will be allowed to generate a Normal or Simultaneous Request. When the A1/S1 reaches the control module, the character is gated from the INFRO lines and placed on Bus 3 where it will eventually be placed into memory via the MR.

All other characters within this block will be allowed to generate N-REQ's or S-REQ's. When an EB symbol or 900 characters are sensed in this block, any other Demand pulses will be ignored. The EB or 900th character will be placed into memory.

At this time, the N Register is sensed for zero. If Decimal "N" Zero (DNZ) exists, the instruction will terminate. If it is not equal to zero, the next block in sequence will be read until DNZ exists.

If the instruction is terminated, the Run level is lost and this will cause the transport arm to either Rollback or Reject, according to the B_1 character of the instruction. The control module will then be free to perform a new instruction.

Read Logic

A BRN instruction uses only two types of status levels: SIO and A1/S1. The SIO will be used to set up the control module, while the A1/S1 will occupy only a minor position in the control module since it only allows the control module to gate the character from the "read buffer" in the Record File unit into memory.

During SIO of BRN on Print No. 8617641, AND Gate 6417D1 will produce an output indicating that the Model 317-1 Control Module is being selected. This is indicated by the $N\text{-}2^4$ bit of the instruction being reset. $N\text{-}2^4(1)$ indicates Model 317-2.

At TP1, AND Gate 6416B2 had been generating HK(P). At TP2 of SIO, AND Gate 6417C5 will attempt to set the Record File Write or Read Flip-flop, but since a BRN is going to be executed, RFWR will not be set. AND Gate 6415C4 attempts to set Record File Normal or Simultaneous (RFNS), but since SOP is not present, this indicates a Normal Mode instruction will take place and RFNS will not be set.

The level RI(N) (6417C2) is produced to indicate that a Record instruction is to take place.

At TP3, AND Gate 6414C4 will attempt to set the Reject (REJ) Flip-flop (6414C5), to indicate whether a Reject is to be performed at the termination of this instruction. If this flip-flop cannot be set as indicated by Bus1 2^{0}(N) applied to 6414C4, a Rollback will be performed instead.

On Print No. 8617640, AND Gate 6404D2 attempts to set End Block Inhibit (EBI), if the Bus2 2^{0}(N) indicates only a count of 900 is to be sensed for to terminate transfer of information for a block.

Print No. 8617639 shows that AND Gate 6397C1 will provide a gating level to gate Bus 3 into the ODC. This is the B_3 character of BRN which indicates the starting cell.

On Print No. 8617641, AND Gate 6417C4 will set RFB at TP4. This will inhibit Housekeeping and prime AND Gate 6415C3, and at TP5 of SIO, RUN (6415C5) will be set. RUN primes 6415B2 and, if Start Run (ST RUN) (6415C6) is set by Ready from the Record File unit, the RUN(P) level is sent to the unit. Ready(P) indicates that a band has been selected and the R-W head is at the Ready position.

The Run level causes the transport arm to place the head and stylus on the disc so that the band may now be used. Nothing will occur in the control module until the first Block Pulse is received. This arrives approximately 1500 milliseconds after RUN is set.

Block Pulse(P) sets the Initiate Block Pulse (IBP) Flip-flop (6415B3), which sets Block Pulse (BP) at TP5. BP produces a timed six microsecond Block Pulse in the control module. The output of BP primes AND Gates 6416B4 and 6415B4 which are sensing for CZ.

CZ (6394A1) senses for a zero in the ODC. If ODC is zero initially, this indicates that the first cell is the starting cell and information transfer may begin. If CZ is not set, then AND Gate 6416B4 produces TODC2. TODC2 is used on AND Gate 6392C5 to trigger down ODC by one, so that ODC will set CZ when the starting cell is reached. Each Block Pulse would arrive at 400 millisecond intervals to trigger ODC down until the starting cell was reached.

When CZ is set, the next Block Pulse will produce Trigger N or M (TN/TM) through AND Gate 6415B4. TN/TM is applied to AND Gate 6406A2 to set Read Write Start (RWS) at TP3. RWS being set will then allow the transfer of information. If does so by priming AND Gate 6404B2 so that when a Demand pulse is received from the information in this cell and DEMAND (6405C5) is set, a NOR-REQ will be produced by 6404B4. Also, with BP and CZ set, Gate 6418B2 will set the Block Pulse Delay (BPD) Flip-flop at TP6. BPD will be used to generate a trigger pulse for the N Register during the first A1 of each block that is read, in order to determine when the proper number of blocks have been read. DNZ will be generated by the N Register when this occurs.

This NOR-REQ will set P-NRQ in the Processor, allowing the generation of the A1 that was selected during SIO. The A1 is first received on AND Gate 6408D3 and since a Band Select is not being performed, and the unit is in the Normal Mode, AND Gate 6407D2 is primed. Since Busy is set, Inverter 6407C1 will produce G, a negative level. G is used as a prime in place of the A1.

G and TP1 will be used on AND Gate 6382C3 to trigger up the RFAB so that a count of 900 characters may be reached. This is the reason that RFAB has a 2^9 bit. Since a Read is being performed, AND Gate 6407C2 will prime 6407B2. At TP23 of the A1, the character on the INFRO lines will be gated onto Bus 3 via 6407B2 and then into memory.

The procedure will continue: receiving a Demand pulse, generating an A1, and gating the character into memory at a rate of once every 400 microseconds. Eventually, termination conditions for the block will come about, i.e., an EB symbol or 900 characters.

An EB symbol is sensed on Bus 3 by AND Gate 6406D1, which will prime AND Gate 6405C2 at TP23. As long as an EB is sensed for and an A1 status level is present, TP3 will clock 6405C2 and set End Block (EB). This will indicate that all information transfer for this block is complete.

EB being set, will inhibit AND Gates 6404B2 and 6405C4 so that any other Demand pulses will not generate NOR-REQ's and A1's. EB being set, will prime AND Gate 6405B3 so that during the A1 of the EB symbol at TP4, RWS will become reset, further inhibiting any status levels from being produced.

If no EB had been sensed, AND Gate 6405D1 would have been primed with a count of 899 in RFAB. At TP6 of the 899th status level, 899 Characters (899 CH) (6405C1) would have been set. This and the 900th A1 would prime AND Gate 6405C3 and EB would become set at TP3. Again at TP4, 6405B3 would reset RWS.

When RWS is reset through OR Gate 6405B6, AND Gate 6405A1 is primed. The other prime to this gate must come from DNZ being sensed on OR Gate 6404A1. Thus, 6405A1 will set Record File Terminate (RF TER), only when the specified number of blocks have been read. If DNZ does not exist at this time, the control module will wait until the next Block Pulse is received and read the next block in sequence.

When DNZ is finally received and RF TER is set, RUN (6415C5) is reset. One-Shot 6414C6 is then fired, and pin 23 will produce a three microsecond low, priming 6414B2 and 6414B1. Depending upon the setting of REJ then, 6414A2 produces REJECT or 6414B1 produces ROLLBACK. These signals will initiate their respective functions in the mechanics of the unit. One-Shot 6414C6 will then produce a three microsecond high pulse from pin 21, resetting REJ in preparation for the next instruction.

Also, when RF TER was set, AND Gate 6418D3 was primed so that at TP6, AND Gate 6418C2 reset RFB, thus allowing the control module to become free. The last A1 with NTER will then select STA1 and STA2 status levels, storing the A final address at locations 0212 -- 0215.

Write Logic

The Write Logic is initiated in a manner similar to Read logic, with the exception that RFWR (6417B1) is set at TP2 of SIO. The selected cell is found in the same manner as when reading.

The timing of the unit will produce Demand pulses when the Write Command level is sent by Gate 6417B4, so that the A1 generated will gate the character onto the Write INFO lines via 6407B3 and 6406B2 at TP56. The only difference between Write and Read is in termination.

When EB is set during a Write instruction, AND Gate 6405B4 is primed, and when the next Demand pulse is received, RWS is reset. The extra Demand pulse is ignored since EB is set, but it indicates that the last character sent to the Record File unit has been written.

The A1 which gated the last character to the unit did not know that termination conditions were present, so another A1 was selected. When AND Gate 6405B4 produces a high output then, and if DNZ is present, AND Gate 6404B5 will produce another NOR-REQ when RF TER is set. RF TER is set after another Demand pulse is received to ensure proper reception of Verify. Gate 6404A3 producing NTER, with the A1 just requested, will select P1 and cause the instruction to terminate. The last A1 does not use memory and does not store A final. AND Gate 6418D3 will then reset RFB and RFWR at TP6 of the "dummy" A1.

ACCURACY CONTROL LOGIC (Print No. 8617642) (654)

Record Address Error (RAE) - A Record Address Error may be generated in the Record File by Gate 6422C3, which checks the parity of the ODC every TP5 during a band select translation. 6423C3, 6424C3 and 6424C3 check the parity of the RFAB, just after an addition of binary tens or

hundreds has been performed. The gating signal, Check Parity (CK PAR (N)) is produced from Inverter 6384C2. AND Gate 6424C4 compares the state of the RFAB Flip-flops against their complementary DRFAB Flip-flops to ensure that proper triggering has taken place.

When the Record File unit receives the address, it will send the Address Parity Error (Address P.E.) signal to 6422C2 to indicate a record address error exists. The busy signal on 6422C2 is generated by the Record File unit to indicate when a disc has been selected and is on the turntable. It prevents a parity error from being generated when the other band on the up-side of the disc is selected. Gate 6423C2 is used during a Read or Write instruction to check for proper selection of the band on the selected disc, by comparing the select return signal to the setting of RFABA 2^0, when a block pulse is received.

Device Doesn't Follow (DDF) - A DDF alarm may be generated during any Read or Write instruction by Gates 6425C6, 6425C5, 6425C4 and 6425C3, by checking the parity in RFAB at TP5 of every A1/S1 status level. During a Read or a Write, the RFAB counts the number of characters transferred. Gate 6426C1 checks the parity of the ODC, which contains the count of the number of blocks to bypass at TP5 as long as Run is present.

Gate 6426C2 checks for the presence of the Operable signal when the BEGIN (N) pulse is generated from 6417B7 (a one ms pulse).

6427C5 checks the configuration of the block pulse counter to detect a count greater than 10. If more than 10 BP's have been received, the unit has been improperly programmed, or an excess number of BP's have been generated, during reading or writing.

Write Error (WE) - The Write Follow (WF) Up-Counter (6426B1) allows 42 microseconds between the Demand pulse and the reception of Write Verify, before generating a RF WE during writing. Write Parity Check (WPC) should be reset before WF equals a count of $110_{(2)}$.

Read Error (RFRE) - The Read Error Flip-flop (6426A2) will be set if the Verify level is absent at termination of the instruction. The Verify

level will be lost if a bad character (short or with bad parity) is read from a cell. An octal 57 will be found in the memory location(s) corresponding to that character(s) placement on the disc.

Character in Gap (RFCIG) - CIG (6421A1) will be set during a Read or Write instruction, if the information transferred has improper format, i.e., a block is not terminated by an E_B symbol or 900 characters. 6422A2 ensures that a Read or Write instruction was being performed before allowing 6422A3 to halt the Processor.

Simultaneous Alarm (SAL) - If any of the applied errors occur when the Record File is operating in the Simultaneous Mode, 6424B4 will generate SAL to indicate the Simultaneous Mode error to the operator.

CARD READER AND CONTROL

The Card Reader, Model 323, in conjunction with the Card Reader Control, Model 314-1R/2R, can be used as a card input device which will link the 301 system with other card-input systems.

The control module allows cards punched in RCA 301 Machine code to be read directly (six-bit characters, two characters to a column) into High Speed Memory. Each card punched in RCA 301 Machine code can contain 160 characters (two from each column of an 80 column card), which may be read into memory, operated upon by the Processor, arranged in desired format, and sent out to any one of a number of output devices (paper tape, magnetic tape, record file, punched card, or printed "hard copy").

The control module also allows cards punched in Electronic Accounting Machine (EAM or Card) code to be read and automatically translated to 301 Machine code as reading is taking place. The 301 Card code (twelve bits to a character, one character to a column) is read in and translated to 80, six-bit Machine code characters.

The 301 Processor itself, if the card uses a six-bit, two character per column code or a twelve-bit, one character per column code, can perform a programmed translation of the card, should the card contain information in a code other than RCA 301 Machine or RCA 301 Card code.

CARD READER MECHANISM AND LOGIC

In order to explain the function of the 314 control module, a basic understanding of the mechanics and electronics involved in obtaining information from holes punched in a card is necessary. The discussion is not intended for mechanical or electrical setup, but rather to give a good understanding of what the Card Reader does and how it does it.

The function of the Card Reader is to take a number of cards, one by one, and send them across a read station, where the information (in the form of punched holes) contained by the card may be sensed and changed to a form more adaptable to the use of a computing system (binary bits represented by the presence or absence of electronic signals).

The function of the Reader logic is to control the mechanical portion of the Reader and correlate the timing of card motion and position to the reading station. It also must, by using this timing, inform the control module when the punched-hole information has been changed to a form adaptable to the uses of the control module.

Card Timing

The first thing which must be accomplished in timing a card is to name a basic division of time. This basic division of time is to be called a card cycle. A card cycle is the time which elapses between the time the leading edge of one card passes a point until the leading edge of the next card passes that point. The card cycle will be timed by means of a disc which will take exactly one card cycle to make one revolution. This disc will produce a Card Index (CI) pulse each time it makes one revolution. The transport is designed to move a card one card cycle each time this disc makes one revolution. Therefore, the card moves at the same rate as the disc, and the disc may be used as the timing standard.

The CI pulse determines only the general position of the card, i.e., it tells the logic nothing of the row position of the card. In order to sense this card properly, it must be known not only where the card is, but exactly what row of the card is there. Reading must be attempted only when a row is in a position to be read.

A card contains twelve rows, so it would be desirable to sub-divide a card cycle into twelve parts, one part for each row. However, it is necessary, when passing cards through the transport, to leave space between them. In order that space be left between cards, the cycle must be divided into a number of parts greater than the number of rows in the card.

The card cycle for the 323 Reader is divided into 16 parts. Twelve of these parts will correspond to the twelve rows of the card, and four will represent the space between cards. The 16 evenly spaced pulses produced by the timing standard disc are called Row Index (RI) pulses. The disc, now, for each revolution will produce one CI pulse and sixteen RI pulses.

In order to obtain the desired pulses from the code disc, photo-sensing stations are placed around the disc in a position such that Card Index sensing will see one hole per card cycle, and Row Index will see 16 holes per card cycle (see Figure 9-1).

In addition to a pulse which tells when a row is starting to pass over the read station (RI), a second set of 16 pulses is produced by a photo-sensing station situated to see the same 16 holes seen by the Row Index sensing station. This sensing station is located a distance from the Row Index station so it will produce a Transfer Index (TI) pulse, 2.25 milliseconds after the leading edge of any RI pulse. The TI pulse will occur after the brush has progressed into the hole. It indicates that information is ready to be transferred from the staticizer to the control module (provided a card is actually at the read station when it is produced).

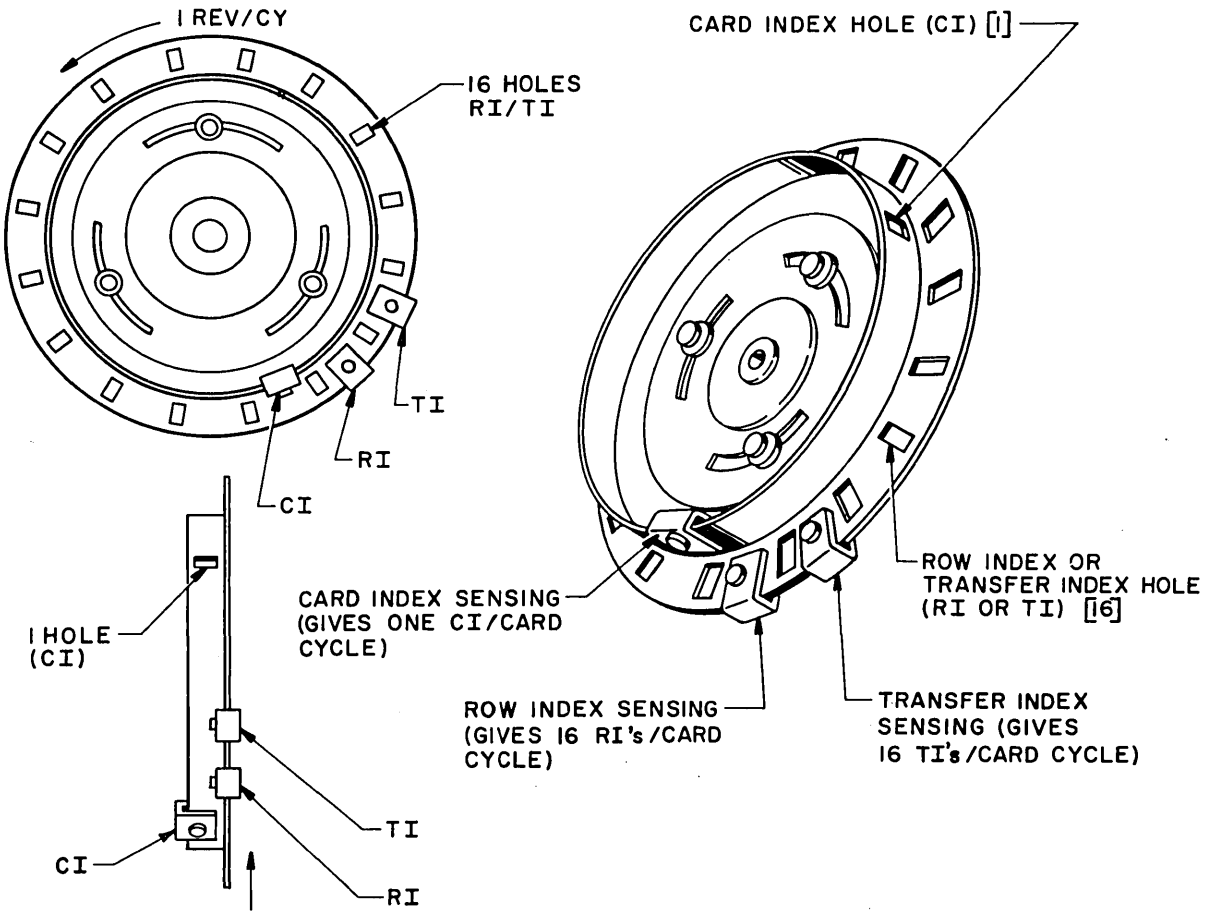


Figure 9-1. Timing Disc.

The three basic timing pulses and their functions are:

Card Index (CI) - This pulse marks the beginning of each card cycle, and occurs once per card cycle.

Row Index (RI) - This pulse divides the card cycle into 16 parts, one for each of twelve card rows and four for the distance between cards. It occurs 16 times per card cycle.

Transfer Index (TI) - This pulse occurs with the same frequency as RI and is delayed mechanically, 2.25 milliseconds from RI, to provide a signal which indicates that information is ready to be transferred from staticizer to control module.

These three pulses are produced by the code disc which is used to time all card motion and to locate the physical position of the card at any time. These pulses, however, do not look at the card itself. Therefore, to insure that disc timing has produced physical card motion, the card itself will be used to produce a signal which will be used in conjunction with the output of the code disc. This is accomplished by a photo-sensing station located in the transport itself. When a card enters the transport, the photo-sensing station will produce a signal to inform the logic that a card has actually entered the transport. This signal is called Card Presence (CP).

All necessary signals are now being generated to properly read a card (CI -- one per cycle; RI and TI -- 16 per cycle; and CP -- one for each card entering the transport). When the motors are running at full speed, the code disc turns at the rate of 600 rpm, allowing 600 cards to be read each minute. This gives a CI pulse once every 100 milliseconds, and RI and TI pulses each 6.25 milliseconds.

Machine Logic

The Run level shown on Print No. 8619091, area D-8, is a command from the control module which is responsible for starting the motors in the Card Reader. The Running (N) level from the output of OR Gate 305 is inverted to Running (P) which is used to pull relay K401. In area A-7, the contacts of K401 will be closed, and with the Jam relay (K402) de-energized and the Operable relay (K403) energized, the selenium controlled rectifiers (SCR402 and SCR401) will be gated to start the motors. The motors will then turn the code disc which will produce the three basic timing signals (RI, TI and CI) on Print No. 8619093, area 7.

The 16 stage Row Level Shift Register on Print No. 8619093, area D-4, will produce 16 Row Level pulses (RL1 through RL16), which are used to inform the control logic that a specific row is present at the read station. The RI, which arrives while the register is being primed by a CI pulse, will advance a single one bit into stage one of the register, producing RL1. The 15 remaining RI pulses will produce RL's 2 through 16 by advancing this one bit through the register. Since there are 6.25 milliseconds between advance (RI) pulses, the one bit will remain in each stage of the shift register for 6.25 milliseconds allowing each RL to last 6.25 milliseconds.

How soon the first RL1 is generated after the motors are started depends upon how far the Card Index hole in the code disc is situated from the CI sensing station. Once a CI pulse is received, the first series of RL pulses may be produced. When RL5 is generated, a special timing sequence will be followed to determine the picking (moving from the input hopper to the transport) of cards. Refer to Figure 9-2 and the Master Timing Diagram on page 9-47. Figure 9-2 shows a series of Row Levels generated during one card cycle (RL1 through RL16). RL5 has been expanded to show the feed-timing sequence.

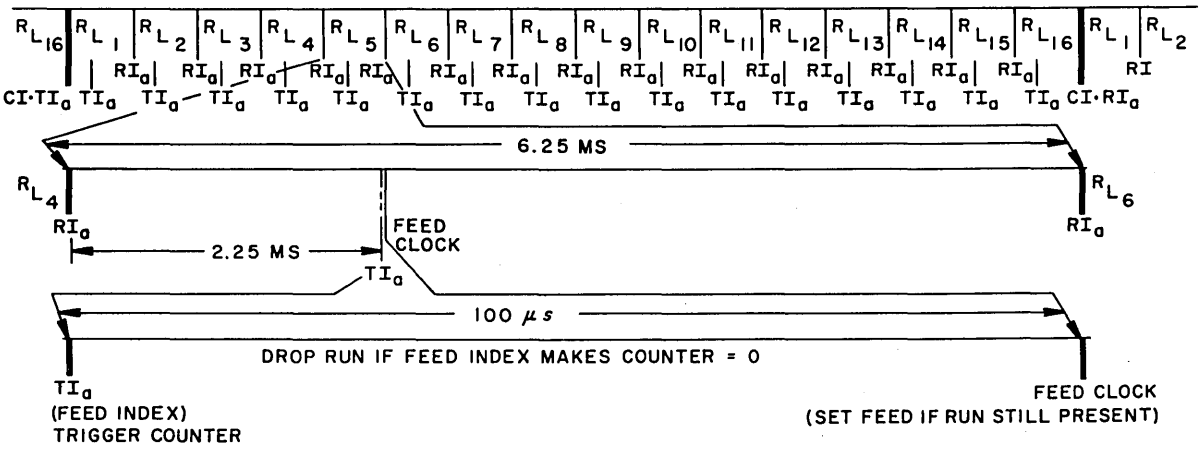


Figure 9-2A. Timing Sequence-Feed Control.

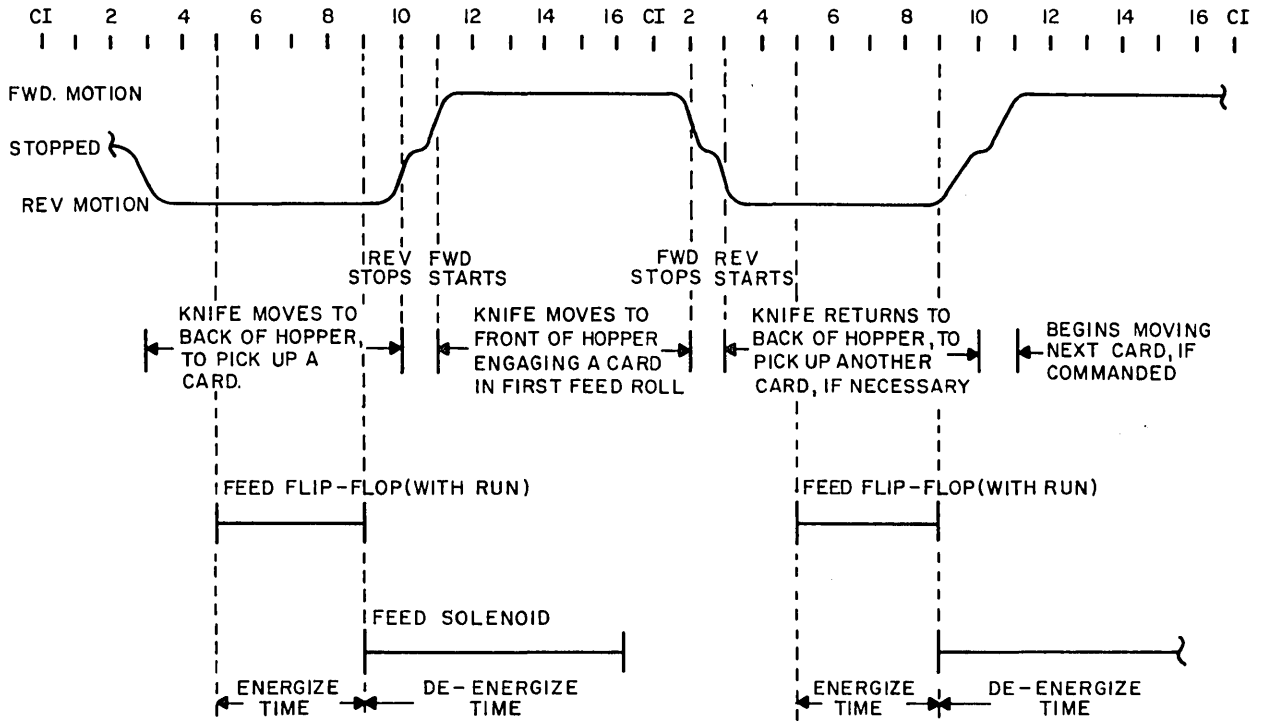
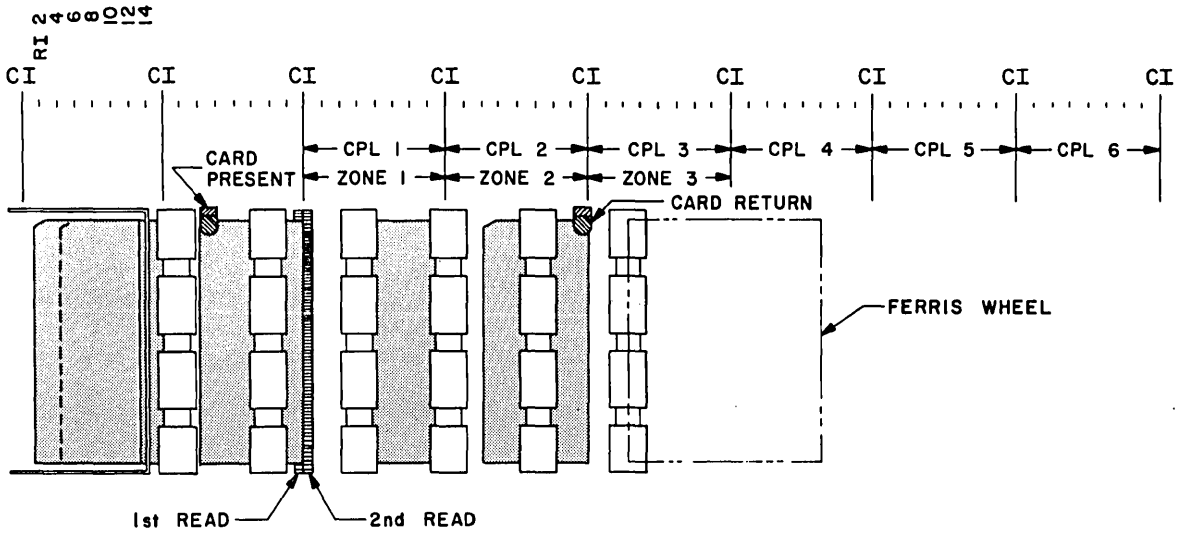


Figure 9-2B. Picker Knife Motion Timing.

Once RL5 (the first one in this case) is generated (Print No. 8619093), AND Gate 244 (area B-4) is primed. When TIa (TI occurs 2.25 milliseconds after RI, which determines the leading edge of a row) occurs, AND Gate 244 is fully primed. If ALT FEED (high from 268) is not present, Gate 266 allows a Feed Index pulse to be generated through Transmitter 240 (the use of ALT FEED will be discussed later). Feed Index is sent to the control module where it is called Index. The effect that Index has upon the logic will be discussed later; however, it will be used to trigger a counter which will deterime whether the Run level should be held.

The Run level, after the motors have been started and a card has been fed, has the sole function of controlling the feeding of cards. Therefore, when a card has entered the transport, the Run level becomes a Feed level and will no longer be needed to keep the motors running.



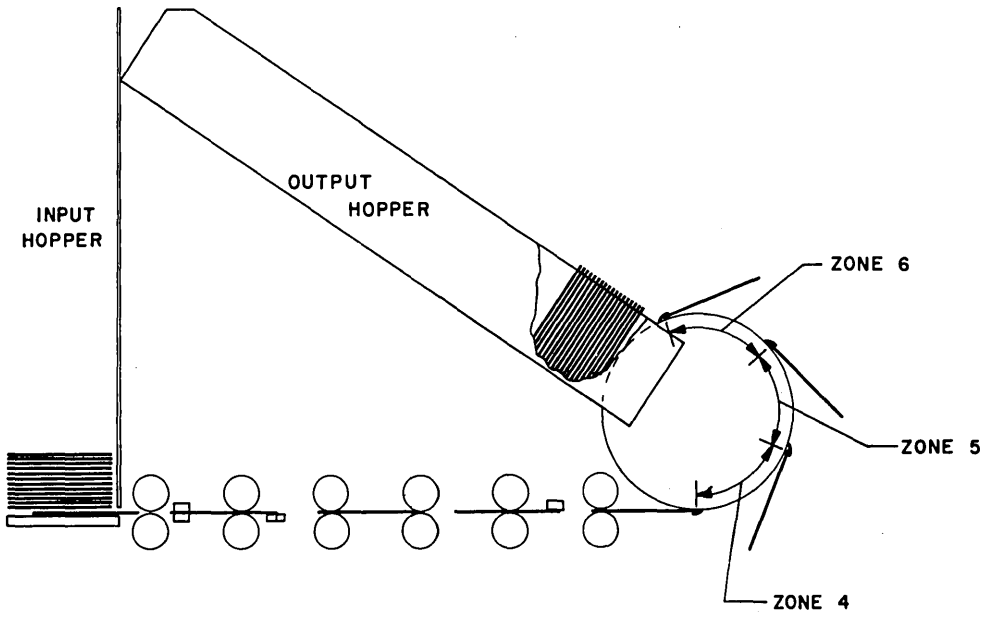


Figure 9-3. Card Position vs. Code Disc.

The Run level, at this time, also is causing the motors to run. If at least one card is not picked at this time (first instruction), the motors will stop and nothing will happen.

The inverted output of AND Gate 266 which gave Feed Index also triggers a 100 microsecond one-shot. After 100 microseconds, a three microsecond pulse called Feed Clock is generated.

Feed Clock goes to Print No. 8619091, area D-6, AND Gate 309. Provided Feed Index (produced 100 microseconds before) did not cause the Run level to disappear, AND Gate 309 will produce the signal Feed Com. Feed Com will get through AND Gate 311, provided the output hopper and reject hoppers each have room and an error (Feed Error) hasn't been generated. AND Gate 311 will set the Feed Flip-flop which, in turn, will energize the Feed solenoid (area C-2) and initiate a picker-knife cycle.

During RL4 of the next card cycle, the card will have become engaged in the first set of feed rollers and advanced to the Card Presence photo-sensing station (see Figure 9-3). When the card has reached the Card Presence photo-sensing station (see Print No. 8619093, area C-7), Amplifier 237 produces a low output (as the beam of light is broken by the opaque edge of the card). The low is inverted to a high which will set the Card Present Flip-flop. The Card Present Flip-flop primes the first stage of a six stage shift register for a one bit, which will be advanced into stage 1 when the next CI arrives. This shift register is the Card Presence Level Shift Register and will produce Card Presence Levels 1 through 6 (CPL1, CPL2, CPL3, etc.).

To understand the use of a Card Presence level, the transport must be examined. Remember that the code disc is producing pulses at the same rate that the card is physically moving through the transport (see Figure 9-3). Starting at the first read station, the transport can be defined as containing three zones. From the first read station to the end of the transport, there exists a distance of three card cycles. Therefore, it will take a card three cycles' time to travel from the first read station to the end of the transport.

It is important to know when a card is in each zone. Therefore, a signal in the logic is generated to inform the electronics when the leading edge of a card is in each zone. The signal is the Card Presence Level. During the time the leading edge of a card is traveling through Zone 1, the CPL1 signal will be present. During the time the leading edge of a card is traveling through Zone 2, CPL2 will be present, and so on. Since, by definition, Zone 1 begins at the first read, it can be said that the leading edge (row 9) of the card is on the first read station when the leading edge of CPL1 is developed. Therefore, actual reading should begin when CPL1 is generated.

On Print No. 8619093, area C-5, is the CPL Shift Register. Note that each Card Index will advance the CPL Shift Register. If the Card Index arrives at a time when the Card Present Flip-flop is set, then a one bit will be advanced into the CPL Shift Register. This one bit says the leading edge of a card has entered Zone 1. If a card was sensed by the Card Presence photo-sensing station (RL4 time), at CI time, it will have moved to the first read station. This is true because, physically, the first read station is one card width (12 rows) from the Card Presence photo-sensing station. Twelve rows after RL4, a Card Index is generated (giving another RL1 after RL16), so the CI after Card Presence says the card has advanced to the first read station and is ready to be read. In order to inform the logic that the card is ready to be read, a control flip-flop (Data Ready, area B-5) will be set.

When CPL1 is first generated, row 9 is under the brushes and ready to be read, so Data Ready will be set by the output from AND Gate 249. The set output from Data Ready will prime AND Gate 261, which in turn will trigger a 500 microsecond one shot when RIa is produced. This one shot, when fired, will prime AND Gates 264 and 265.

The output from AND Gate 264 is called Strobe Input One (SI1), which is generated twelve times, once for each row on the card. It can only be generated while Data Ready is set (RL1 through RL13). However, since AND Gate 264 is inhibited during RL13, SI1 is developed at RL1 through RL12 only.

The second gate, 265, will produce Strobe Input Two (SI2), which is developed 12 times per cycle, once for each row on the card. SI2 is developed for each Row Index during which Data Ready is set, except during RL1.

SI1 is developed 12 times (RL1 through RL12) and SI2 is developed 12 times (RL2 through RL13). SI1 will allow the first read station to obtain information from the card. SI2 will allow the second read station to obtain information from the card to check for accuracy. Physically, the second read is identical to the first, but is located one row further down the transport than the first. This means, while row 9 is being read on the first station, there is nothing on the second; and while row Y is being read on the second station, nothing is on the first. Therefore, RL1 which indicates that row 9 is on the first read station inhibits reading by the second station, while RL13 (indicating row Y is on the second read station) inhibits reading by the first station.

The SI signals allow the appropriate set of brushes to be energized (SI1 -- first read brushes; SI2 -- second read brushes). See Print No. 8619092. SI1 will cause the 3A141, area D-6, number 101, to apply -48V to the first read brushes. Any here one of the 80 brushes is touching the segmented block (by falling through a hole in the card), a prime on a corresponding brush level changer will allow that level changer to set a stage of an 80 stage shift register. Each segment of the block is connected to its own level changer, and each level changer is connected to its own stage of the 80 stage shift register. Each read station has its own segmented block, set of brush level changers, and shift register.

When a brush falls through a hole, it primes its brush level changer (represented on Print No. 8619092, area D-4, by logical element 103) and the level changer, in turn, sets a stage of the 80 stage shift register. After the strobe, each column that had a punch in it will have caused a corresponding stage of the shift register to become set. The row strobed, therefore, is "duplicated" in the shift register (a one bit representing a hole and a zero bit representing no hole).

Once the shift register has been loaded, a Ready signal will be sent to the control module. When the control module "sees" this signal, it will examine the contents of the shift register stage by stage or essentially, it will examine the card column by column.

It does this by examining the first stage, which contains information according to the contents of column 1 on the card. When it has determined whether or not column 1 had a punch (indicated by DATA 1, area B-2), an Advance signal (area B-8) will be sent to the shift register by the control module. The control module is still looking at DATA 1 which is still coming from stage 1. However, because the shift register has been advanced, it contains information according to what was in the second stage or in the second column. After a second Advance pulse, the first stage will contain information according to the third stage or third column, etc.

Note that the last stage of the shift register is constantly primed for zero bits, so that when the control module has sent 80 Advance pulses, or examined all 80 columns, the shift register will contain all zero bits ready for the next row to be read.

How the control module handles the information from each shift register will be discussed later. Remember that for each row on the card, the control module will send 80 Advance pulses, examining stage 1 each time.

In order that the control module may know when the shift register contains the information, a signal must be sent to it. This signal is developed on Print No. 8619093, area B-1, and is called Ready.

Ready is a three microsecond pulse developed at TI time (TI occurs 2.25 milliseconds after RI, which allowed the read station to be strobed). Each TIa (TI delayed 250 microseconds and chopped to three microseconds) applied to AND Gate 256, area B-4, gives Ready as long as the Data Ready Flip-flop is set. Data Ready is set during 13 row levels; therefore, 13 Ready pulses will be developed, one for each card row, and an extra one to allow checking of the last row.

CONTROL LOGIC

The function of the Card Reader Control, Model 314-1R/2R, is two-fold:

1. It must cause the reader mechanism to feed cards and control this feeding according to the programmed instructions. It does this by means of the Run Command, which may be modified by the ALT FEED signal.
2. The control logic must service the shift register once the information on the card has been strobed to it. Servicing the shift register consists of representing the information on the card in a machine oriented code (six-bit binary) and placing this information in memory.

Feeding of Cards

The control that the control module has over card motion is centered upon the Run Command. It has already been seen that to start the motors, a Run Command is necessary. It was also seen that in order for a card to be moved into the transport and advanced to the read station, a routine which occurs during RL5 was executed. The part the control module plays in this routine will now be discussed.

Referring to Figure 9-4, note that RL5 with TIa (a three microsecond pulse) will produce the signal Feed Index. This signal is sent to the control module where it does several things.

During the SIO status level, a flip-flop called Start was set. This flip-flop will give a Run Command immediately, causing the motors to begin running. When the first CI pulse is received, the first set of row levels is initiated. At RL5, the Index pulse is developed, and if a row 9 of a card has not reached the read station before RL5 time (the motors were not running at the time the instruction was staticized), the First Card Flip-flop will be set, indicating the first card in a series of cards is to be read by this instruction. At the same time, Index will trigger a three stage binary up-counter. This counter is the Card Start Register (CS Register).

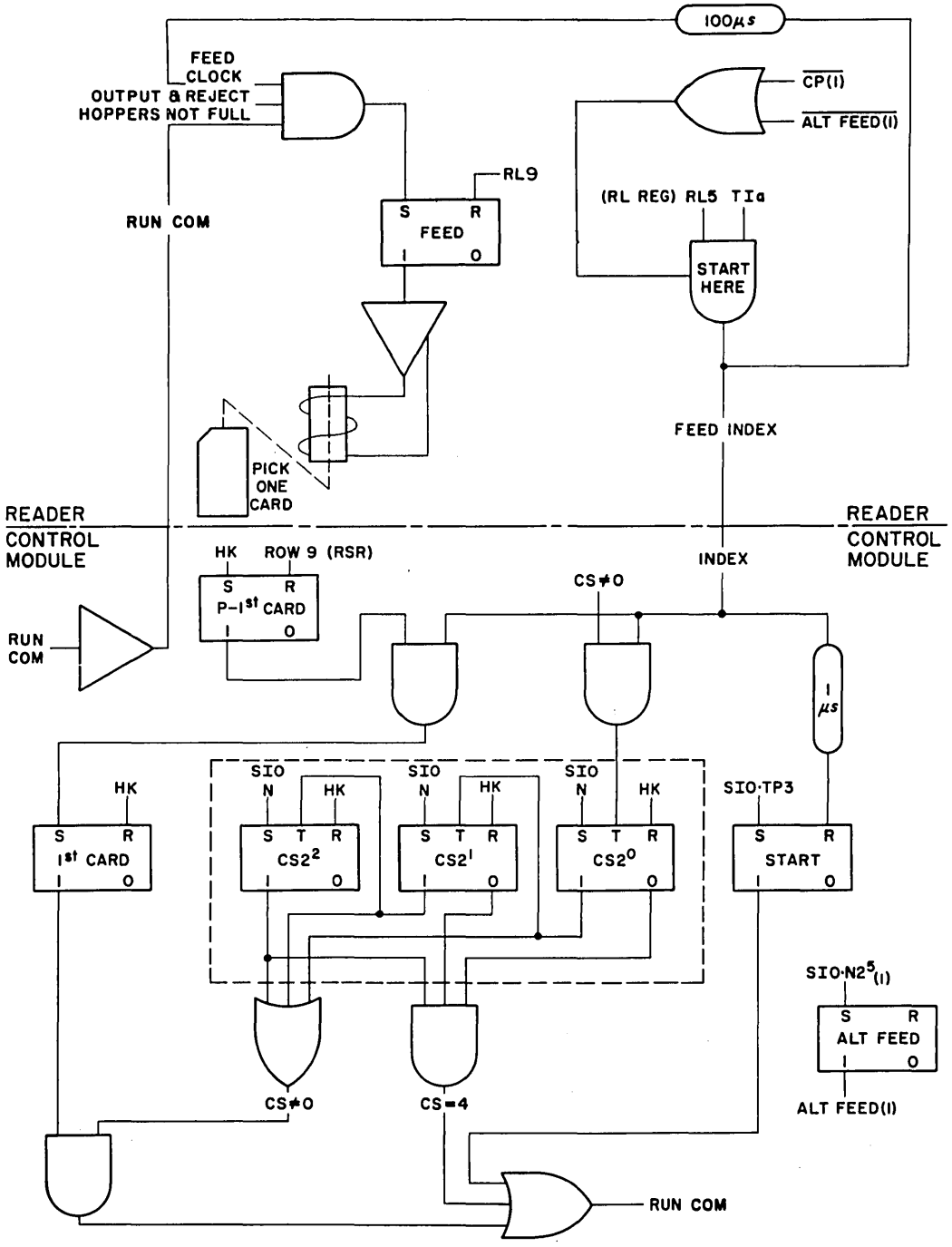


Figure 9-4. Card Feed Logic 314-1R/2R, 1/2 Control Module.

The CS Register is used to keep track of the number of cards fed by the first instruction in a series, and to control the feeding of cards by ensuing instructions. Assume continuous reading of four cards. Relate the Master Timing Diagram on page 9-47 to Figure 9-4.

The first Index pulse will set First Card and trigger the CS Register plus one. The program for reading four cards continuously will have a four in the first N character. The complement (a three) of the character will be placed in the CS Register. The Index pulse will trigger the three to a four. Since First Card is set and the CS Register contains something other than zero, a prime to hold the Run level will be developed. The Index pulse, delayed one microsecond, will reset the Start Flip-flop so that the signal CS≠0 will hold the Run Command.

After 100 microseconds, the signal Feed Clock will be developed. Feed Clock, because CS≠0 is holding the Run Command, will set the Feed Flip-flop and allow a card to be picked from the input hopper. Two RL's will be developed before the card reaches the first read station. During the second RL5, a second Index pulse will be developed. This second Index pulse will trigger the CS Register to five (CS≠0), so the Run Command can still be held, Feed will again be set, and a second card will be fed.

The third CI pulse to arrive after the motors were started will initiate reading of the first card picked, since the first card will have reached the first read station by the time the third CI pulse is developed (see Master Timing Diagram on page 9-47 and Figure 9-4).

During the time that row 5 of this card is being read, a third Index pulse will be developed, the CS Register will be triggered to six, the Run Command will be held, and Feed will be set for the third time, allowing a third card to be picked.

While the first card is being read, a series of Ready pulses will be developed. The thirteenth, and last, Ready pulse will allow the control module to check row Y (the check read station is one row farther

down the transport than the first read). Once row Y has been checked (RL13), the instruction will terminate and the Run Command will be dropped. The leading edge of the Run Command is always determined by the Start Flip-flop which is set at TP3 of SIO.

Note that CP is developed shortly before the arrival of the second Feed Index pulse. On Print No. 8619091, it can be seen that the signal CP, when present, will hold the Running signal to keep the motors running (area D-4, OR Gate 302). CP is derived from the physical presence of the card and is responsible for the Card Presence levels. Therefore, once a card has reached the card presence photo-sensing station, it is the presence of any cards in the transport which keeps the motors running. The Run Command, thereafter, has an effect only upon the cards fed.

As was seen, three cards were picked by the first instruction and one was read. The trailing edge of the Run Command was determined by termination of the instruction, and the instruction will always terminate when one full card has been read. The ensuing instructions, when staticized, will find the motors still running since the first instruction has picked two more cards than it read and will not have to wait for a card to travel the entire distance from the input hopper to the read station. The card was traveling this distance while the first card was being read.

Due to this difference in timing between the first instruction and each instruction following sequentially, conditions for holding the Run Command will change. The difference in timing stems from the fact that the first instruction finds the motors at rest, no pulses being produced, and the card that is to be read more than a cycle away from the read station in the input hopper. Every instruction after the first (with continuous feeding) will find the motors already in motion, timing pulses already being produced, and the card to be read less than four row levels from the read station. Logic to make the distinction between these two conditions is incorporated in the First Card Flip-flop.

The first instruction will start the motors running, and the first timing signal sent back to the control module will be the Feed Index pulse. Index will find Pre-First Card set, and will set First Card. Every instruction thereafter in that sequence will find timing pulses already produced and provided they are staticized before the card approaching the read station arrives at the read station, will first see the Ready pulses produced by RL1 through RL5; and then will see the Index pulse. Ready, produced during RL1, will generate row 9 in the control module and cause Pre-First Card to become reset. The Index pulse developed will not be able to set First Card since it will occur after row 9.

Because First Card cannot be set, CS≠0 is no longer the condition which will allow the Run Command to be held. The Run Command now must be held by CS=4. To obtain a four in the CS Register after receiving the Index pulse, a three must have been gated in. Since the complement of the N Register is placed in the CS Register, the instruction must be written with a four as its N character. Therefore, in order for instructions after the first instruction in a sequence to pick a card, the N character in these instructions must contain a four. If the instruction contains anything other than four, the Run Command, which is now acting as a feed level, cannot be held beyond Index and no card will be picked. The fact that no cards will be picked with anything other than a four in the N Register, is used to determine the terminating sequence for continuous feeding.

In a continuous feed, the first instruction will pick three cards and read only one. This leaves two extra cards in motion in the transport. The second instruction and each instruction after which has a 4 as the N character, will pick one card. This means that the number of cards to be read by a given continuous sequence will be in motion in the transport at a time when two less than the number of cards in the sequence have actually been read.

To terminate this sequence, two instructions which will read the two extra cards, but will not pick any additional cards, are necessary.

These instructions will be instructions first with N=2, then N=1. Neither of these instructions will feed any cards (the complement of a two is five and Index will trigger it to a six). Six is not four, so the Run Command will be absent when Feed Clock is developed and no card will be picked. The complemented "one" will be triggered to a seven, and again it will not be possible to pick any cards. Each of these instructions will read a card so the extra two cards of the continuous sequence will be read.

The important factors in feeding cards are:

1. Start is used to generate the leading edge of the Run Commands. During the first instruction, its function is to start the motors.

2. The first instruction in a series of instructions is treated differently from the other instructions in the sequence. The first instruction will pick the number of cards specified by N to a maximum of three. In a continuous feed program or sequence, the first instruction will contain an N character of 4, will place three cards in motion, and will read one of the three. The first instruction will pick cards to be read by the second and third instructions of the sequence. Each instruction will terminate upon reading one card.

3. The other instructions in a sequence will pick a card only if the N character is equal to four. Any other number will not allow any cards to be picked.

4. The two extra cards picked by the first instruction must be taken care of by the last two instructions of the sequence. These last two instructions will read the two cards, but will not pick any cards.

5. The leading edte of the Run Command is always determined by Start. If a card is to be picked, Run Command will remain until termination. If no card is to be picked, Run Command

will be dropped at RL5. The trailing edge, therefore, can be either at termination (RL13 as in Master Timing Diagram; N=4) or at Feed Index (RL5 as in Master Timing Diagram; N=2, N=1).

Alternate Feed - In the continuous feed program, a period of approximately 20 milliseconds (during part of RL13, after the check routine has been executed and all of RL's 14, 15 and 16) is available as free processing time to the Computer (assuming Normal Mode operation). During this 20 milliseconds time, the program may be required to operate on the card data just read in.

Within the specified 20 milliseconds, the program is required to provide the next Card Read instruction or the Processor will miss one or more rows of information from the card approaching the read station, and eventually generate an error.

Should the portion of the program which is operating on the card data require more time than 20 milliseconds, a feature called Alternate Feed can be used to provide extra time.

Print No. 3506039 contains the Alternate Feed (ALT FEED) Flip-flop in area A-5. If the program requires more time than 20 milliseconds, a 2^5 bit may be placed in the N character of each Card Read instruction (note the CS Register gets its value only from bits 2^0 to 2^2 and that bits 2^3 to 2^5 have no effect on this counter). The 2^5 bit will allow AND Gate 395A1 to set ALT FEED during SIO (Set CS is generated on Print No. 3506038 by AND Gate 382D1 through Inverter 382D3).

With ALT FEED set, Transmitter 397A1 will generate the signal ALT FEED (P). ALT FEED (P) is then applied to OR Gate 269 (Print No. 8619093, area B-2) through Receiver 268. With ALT FEED set, pin 7 of OR Gate 269 will be low. Each time the Card Present Flip-flop is set, pin 8 will also be low causing the OR Gate to produce a high to inhibit generation of Feed Clock and Feed Index by AND Gate 266. Because Feed Clock cannot be generated, Feed cannot be set (Print No. 8619091, area C-4) and a card cannot be picked.

The effect of this is to cause the Reader to pick a card, miss a card, pick a card, miss a card, etc. There then will exist a distance of 20 row index points from the trailing edge of one card to the leading edge of the following card instead of 4 row index points as in continuous, non-alternate feed. This allows the program to provide a Card Read instruction each 120 milliseconds (instead of 20 milliseconds) providing an extra 100 milliseconds for processing card data between cards. The Reader can then read cards at the rate of 300 cards per minute while processing the card data as it is read.

The alternate feed instruction differs from the regular continuous feed instructions only in the 2^5 bit in the N character. The sequence itself will differ only in termination. The first instruction will pick only one extra card, therefore, the required number of cards will be in motion in the transport when one less than the required number has been read. It is, therefore, necessary to program only one instruction which will pick no cards. This instruction will have an N character of 8.

Transfer of Information

The second function of the control module is to service the Data One Shift Register Print No. 8619092 as each card row is strobed into it. Servicing the shift register consists of representing the contents of the shift register (according to the row read) in machine orientated, six-bit code.

Organization of Card Data vs. HSM Data

Information may be recorded on a card in one of two ways. The control logic is designed to read a card according to the manner in which the information is represented on the card.

The first method of representing information on a card is in the 301 Card code. 301 Card code is a twelve-bit, decimally orientated code. Ten rows (rows zero to nine) represent the ten decimal digits. Three rows (rows zero, X and Y) are used to represent zones. The zone

punches, in conjunction with the ten decimal punches, may be used to represent four groups of characters:

Group 1 - no zone punch
Group 2 - Y zone punch
Group 3 - X zone punch
Group 4 - zero zone punch

The 301 Machine code, which is a six-bit binary code, is designed in a way to make it compatible with the twelve-bit Card code. Four bits (2^0 through 2^3) may be arranged in 16 different configurations. 301 code uses 15 of these possible combinations or, decimally, it uses the numbers zero to fourteen.

Two bits (2^4 and 2^5) may be arranged in four possible combinations. These two bits can be called zone bits. The four combinations of zone bits in conjunction with the 15 combinations of information bits may be used to represent four groups of characters:

Group 1 - $2^4(0)$, $2^5(0)$
Group 2 - $2^4(1)$, $2^5(0)$
Group 3 - $2^4(0)$, $2^5(1)$
Group 4 - $2^4(1)$, $2^5(1)$

The Card code then is set up in a way very similar to the Machine, or six-bit code. As an example, the decimal number nine is, in six-bit Macine code, a nine in Group 1. The "nine" is represented in the information bits $2^0(1)$, $2^1(0)$, $2^2(0)$, $2^3(1)$. It is in Group 1 because the zone bits are $2^4(0)$ and $2^5(0)$. Similarly, on a card, the "nine" is represented by an information punch in row 9. It is in Group 1 because it has no zone punch.

The letter I is a nine in Group 2. To represent an I in six-bit code, the information bit configuration will be the same as with the nine, but it must be placed in Group 2. To place it in Group 2, a zone bit configuration $2^4(1)$ and $2^5(0)$ is necessary. Similarly, an I in twelve-bit Card code is a nine in Group 2. The nine again is represented as an information punch in row 9. To make it an I, it must be placed in Group 2. Therefore, a zone punch in row Y is necessary.

The Card code can be related to the Machine code in this way in the majority of cases. Should the information configuration of the Machine code character exceed a value of nine (the highest value information punch on the card), more than one information punch is necessary. To represent this value, a punch is placed first in row 8. Then, to give it a value equal to the Machine code character, a punch will be placed in a row which will add to the value of eight.

For example, an asterisk (*) is a twelve in Group 3. Twelve exceeds the value of nine, so a punch will be placed in row 8. The difference between eight and twelve is four, so a second punch will be placed in row 4. The character is in Group 3, so a third punch will be placed in row X. This pattern is violated in three instances. The row 0 punch must be used in two ways: to represent a decimal zero when it stands alone, and to represent Group 4 when it stands with other punches. This generates a case which causes the rules to be violated. A quotation mark (") is, according to the code, a Group 4 zone configuration by itself.

On the card, theoretically, it would be a Group 4 zone punch by itself. However, characters in Group 4 are represented by a punch in row 0. A punch in row 0 by itself must represent decimal zero. To distinguish decimal zero from quotation mark, zone punch X and zone punch zero are put on the card.

A second violation of the pattern is seen in the character, underline. Underline is the character which is used to represent a space. A space on a card is represented by no punches in any row, whereas, following the pattern, it would be a punch in row 8 and a punch in row 2. The quotation marks and the space are the only exceptions to the pattern.

The third violation of the pattern is found in a special character, the "plus zero" (+0). "+0" is $37_{(8)}$ in six-bit machine code. This makes it a $15_{(10)}$ in Group 2. In theory, this would be the combination 8-7 (to give $15_{(10)}$) and Y (to place it in Group 2). However, a problem arises with the combination 8-7. When 8-7 is read in, it

will generate $15_{(10)}$, which is $17_{(8)}$. $17_{(8)}$ (as will be discussed later) has a special function in the translation logic. If an 8-7 combination is allowed to generate an octal 17, the translation logic will not function correctly; therefore, the 8-7 combination is never allowed to exist. The character "+0" is represented, instead, as a "Zero-Y" combination.

The second way that information may be recorded on a card is directly in six-bit code, that is, in Machine code. If the card is punched in Machine code, each row becomes equivalent to a binary bit. Row 9 is no longer equivalent to a nine, but merely a 2^5 bit. Row 8 represents a 2^4 bit, etc. Since each column has a possibility of twelve punches, two characters may be placed in each column when the six-bit Machine code is used. The six rows, 9 through 4, represent the six binary bits of the first character in a given column, and characters represented in rows 9 through 4 are referred to as the A characters. The six rows, 3 through Y, represent the six binary bits of the second character in a given column, and characters represented in rows 3 through Y are referred to as the B characters. Parity is not recorded on the card, but is generated by the control module.

The card may be recorded in the standard 301 Card code and a true translation from the twelve-bit Card code to six-bit Machine code must take place. The card could also be recorded in six-bit Machine code, in which case the control module need place only the proper bit in memory according to the presence of information and row position of the information.

To inform the control module of the way in which the card is recorded, the console button, BCT (Bypass Card Translator), is used. The control module, if it finds the BCT button has <u>not</u> been depressed, assumes the card to be recorded in the standard twelve-bit Card code, and will treat the information according to the rules mentioned for Card code related to Machine code. If, however, the BCT button <u>is</u> depressed, the control module assumes that the card contains 160 characters, already in six-bit code form, and will proceed to place bits into

memory through 160 locations, according to row and column position. Figure 9-5 shows two cards: one recorded in EAM, or 301 Card code (twelve-bit code); another recorded in 301 Machine code (six-bit code).

The first card, recorded in six-bit Machine code, will be read into 80 memory locations since there is one character represented in each column and there are 80 columns on a card. These 80 characters are read in according to the instruction from A initial to A initial plus 79.

The second card, recorded in six-bit Machine code, will be read into 160 memory locations since there are two characters in each column. The A characters (row 9 to 4) will be read in according to the instruction from A initial to A initial plus 79. Starting with row 3, the B characters (rows 3 to Y) will be read in according to the instruction from A initial plus 80 to A initial plus 159.

The card then can be recorded in one of two ways: Card code (twelve bits) or Machine code (six bits). To inform the control module how to treat the information, the BCT console button is used. With BCT off, the card is read, according to the pattern relating Card to Machine code, into 80 HSM locations. With BCT on, assigned to each row is an individual bit value (to rows 9 to 4 of each column an individual memory location, and to rows 3 to Y of each column another individual memory location). The card, with BCT on, will then be read into 160 memory locations.

Transfer of Data

As was discussed earlier, the information will be strobed from the card into an 80 stage shift register (the DATA 1 Shift Register) one row at a time. Timing of the strobes is accomplished within the logic of the Reader itself. The control module's part in reading consists of servicing the shift register, and it is informed when to service it by the timing signal, Ready, generated in the Reader.

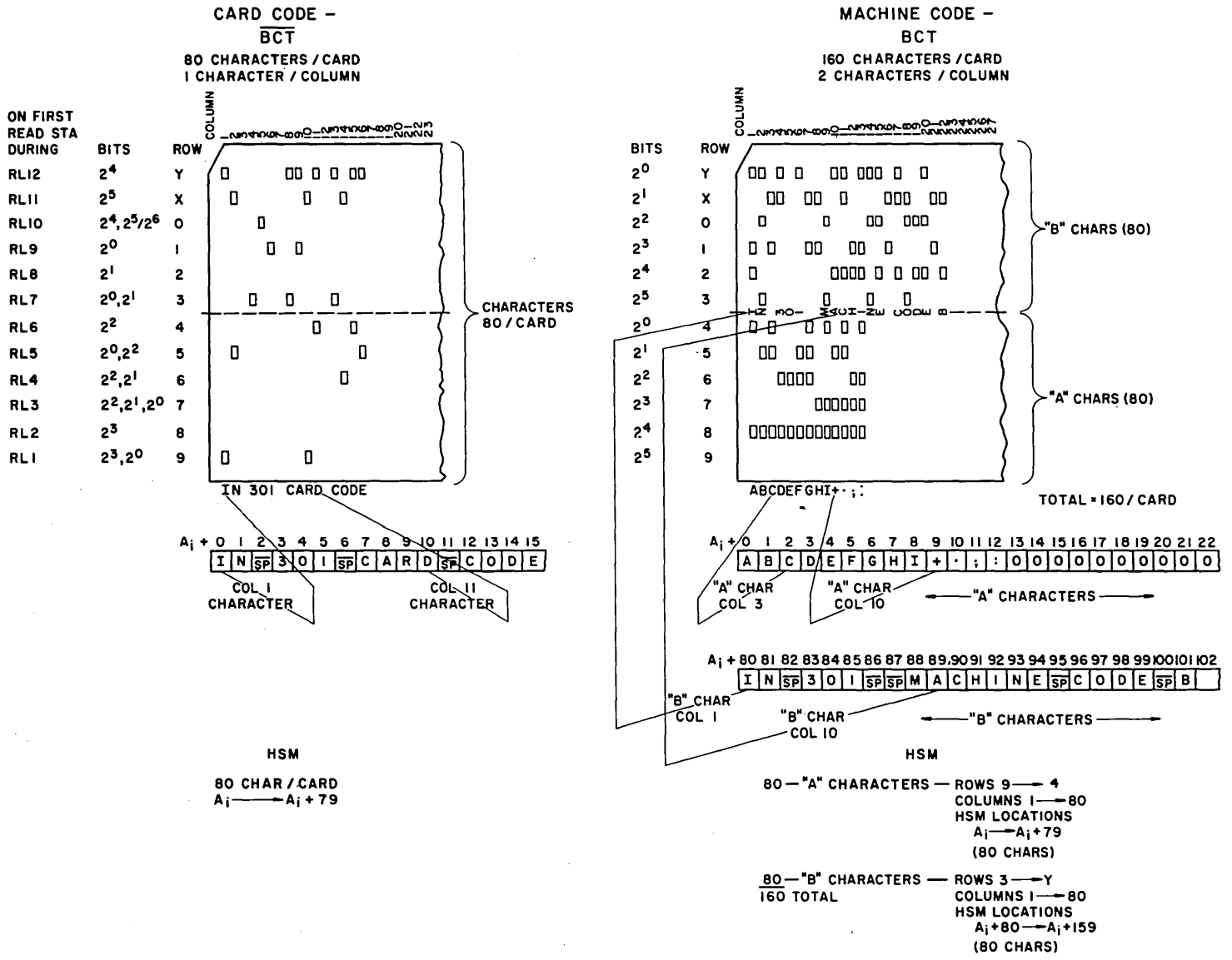


Figure 9-5. Function of Translator (314-1R/2R Control Module).

Figure 9-6 shows, in a simplified manner, how the reader generates strobe timing and service request timing. Any time CPL1 is generated, the leading or row 9 edge of the card can be said to be entering Zone 1 of the transport. By definition, the beginning of Zone 1 is the first read station. The Data Ready Flip-flop is responsible for "remembering" and informing the logic of the time when a usable portion of the card is passing over the read station.

Data Ready, when set, will allow the first read station to be strobed twelve times during a cycle (during RL's 1 to 12). At the same time, Data Ready will allow the Reader to transmit a service request signal (Ready) to the control module as each TI pulse is generated.

Note here, that when reading a card, two separate shift registers will be used to keep track of the card rows. One register in the Reader itself generates 16 equal levels for the sole purpose of timing the card motion, read strobing, and accuracy logic. These levels have been, and will be, referred to as Row Levels (RL's).

It shall now be seen that the control module contains a second shift register to keep track of card rows. This shift register differs from that in the Reader in that its sole purpose is to allow the control module to know the row position of the information being examined, so that translation may take place accordingly. This register (see Print No. 3506036, area D-2 through D-5) produces twelve levels, one to correspond to each card row (levels 9 through Y). A distinction in reference to these two level generators is drawn.

Levels generated by the Reader are Row Levels (RL's). Those generated by the control module are simply Rows. Note now that RL1 refers to the first row to enter the transport. The first row to enter the transport is row 9; therefore, RL1 in the Reader will correspond to Row 9 in the control module, RL2 to Row 8, RL3 to Row 7, etc.

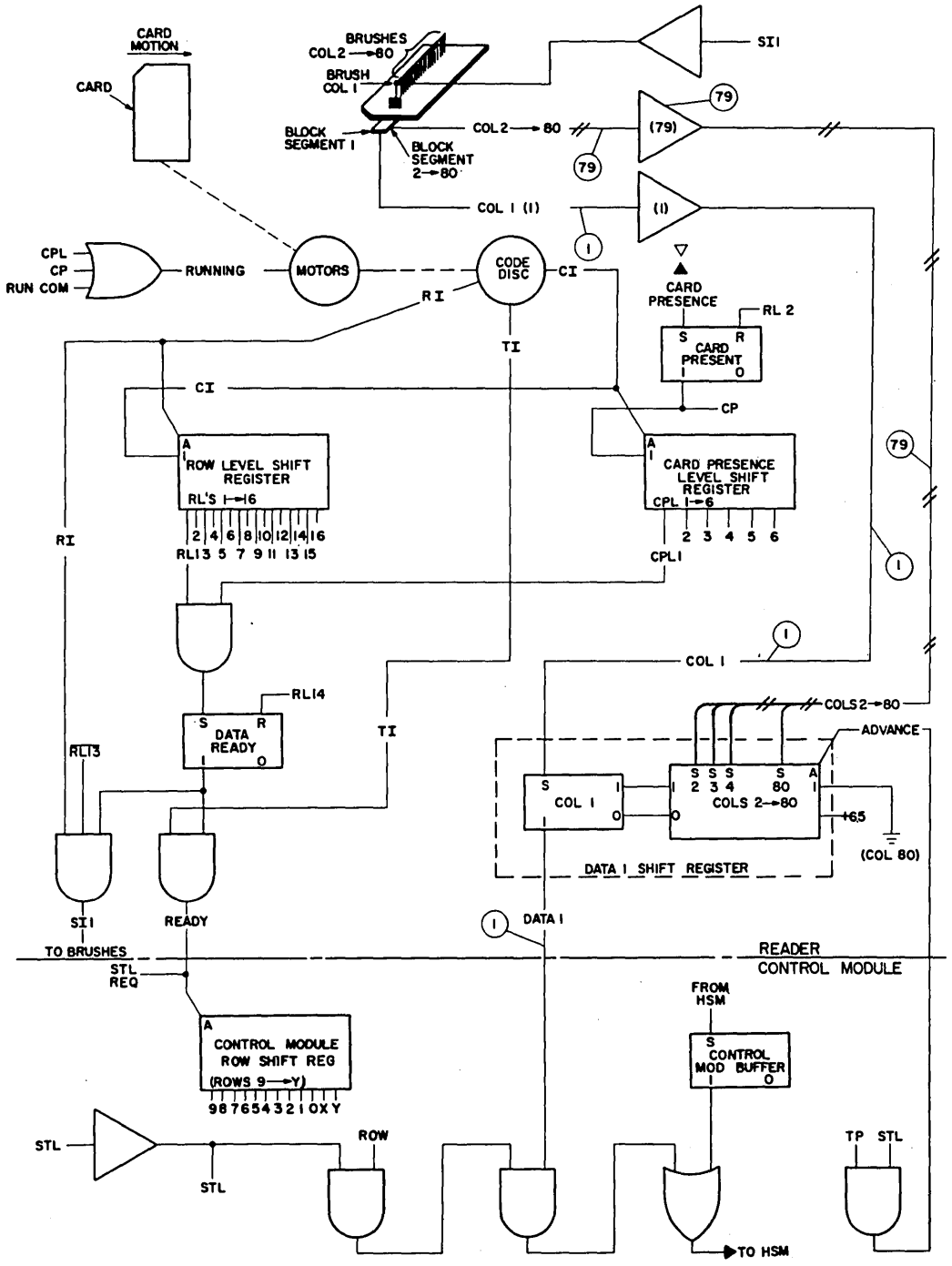


Figure 9-6. Read Logic (323 Reader)

The control module now must take the information supplied by the Reader and treat it according to the state of the BCT button. It first determines if column 1 of the row presently being read did not contain information by checking the first stage of the 80 stage shift register. At the same time, it will bring out of memory, information which represents punches in any previous row and put it into a buffer. The control module then examines the shift register to determine which row is presently being read, and according to the BCT button, will generate a bit or bits to correspond to the row. These generated bits are then combined with the accumulated information in the Card Buffer and a new character is written into HSM. Then the control module will advance the Data 1 Shift Register causing the contents of stage 2 (column 2 information) to move to the first stage of the 80 stage shift register, and the operation again begins with the control module checking the first stage of the 80 stage shift register.

Read Timing (Control Module)

The two most important signals to the control module are the Row Ready signal generated by Ready, and the Data 1 signal generated by a bit in stage 1 of the 80 stage shift register.

Ready - Row Ready - On Figure 9-7, each Row Index, while Data Ready is set, allows a card row to be strobed into the shift register. After 2.25 milliseconds, TI causes a Ready pulse, when Data Ready is set, to initiate the control module routine which will service the shift register.

The Ready pulse is used to inform the control module that a row is ready to be read into HSM. The Ready pulse first sets a flip-flop called Pre-Row Ready. At TP0, with Pre-Row Ready set, Row Ready will be set. Pre-Row Ready is used in conjunction with TP0 to synchronize the arrival of Ready with the Processor's standard time pulse generator (Print No. 3506038, area B-6, from Print No. 3506039, AND Gate 397C3). At TP0, Row Ready is set. It will remain set for six micro-

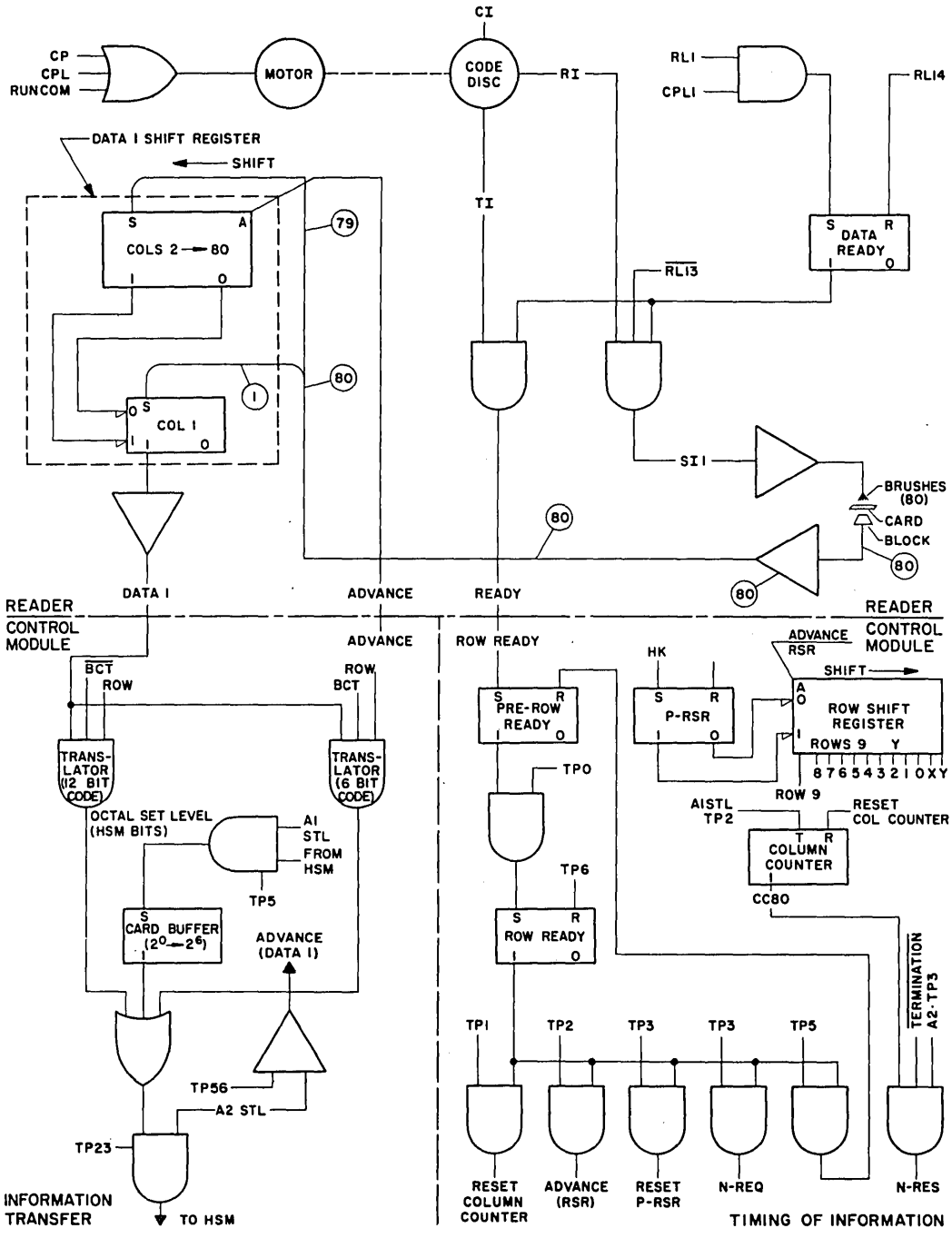


Figure 9-7. Control Module 314-1R/2R Timing of Info. Transfer

seconds until TP6. During these six microseconds, it will initiate the routine for reading the card row into memory.

At TP1, Row Ready allows the Column Counter to be reset. The Column Counter is used to keep track of the number of columns read into memory and at Row Ready time, no column of this row has yet been read (OR Gate 384D1).

At TP2, Row Ready allows the row shift register in the control module to be advanced. This is necessary to the proper organization of data in memory as related to the card. The control module, in order to know what bits to generate, must know what row the card information is coming from (Print No. 3506036, area D-5 through D-2).

At TP3, the Prime Row Shift Register (P-RSR) Flip-flop (365D2) is reset. This is important only during the first Row Ready of each card. It allows TP2 to advance a one bit into the first, or row 9, stage of the shift register. Then it causes the next Row Ready to advance a zero into stage 1, and the one bit into stage 2, or row 8. This ensures that only one Row Level will be generated at a time.

At TP3, a status level request is generated. The control module needs status levels, first to examine memory for information previously read; and second, to place any new information from the card into HSM. Status Level Request is generated on Print No. 3506038, from either 5A1 or 4A1, by Gate 4C1.

At TP5, Pre-Row Ready is reset to insure that the Row Ready routine is executed only once for each row by preventing Row Ready from again becoming set at TP0 (AND Gate 386C3).

Data 1 and Translation - The control module now must take the card information and put it in a form adaptable to HSM. To do this, the BCT button, the row present, data in stage 1 of the 80 stage shift register, and information from any previous row must be considered.

Figure 9-8 shows, in flow chart form, how the control module will handle information punches in a row, for any given memory location, if the card is in 301 Card code (twelve-bit code or $\overline{\text{BCT}}$). Assume a card

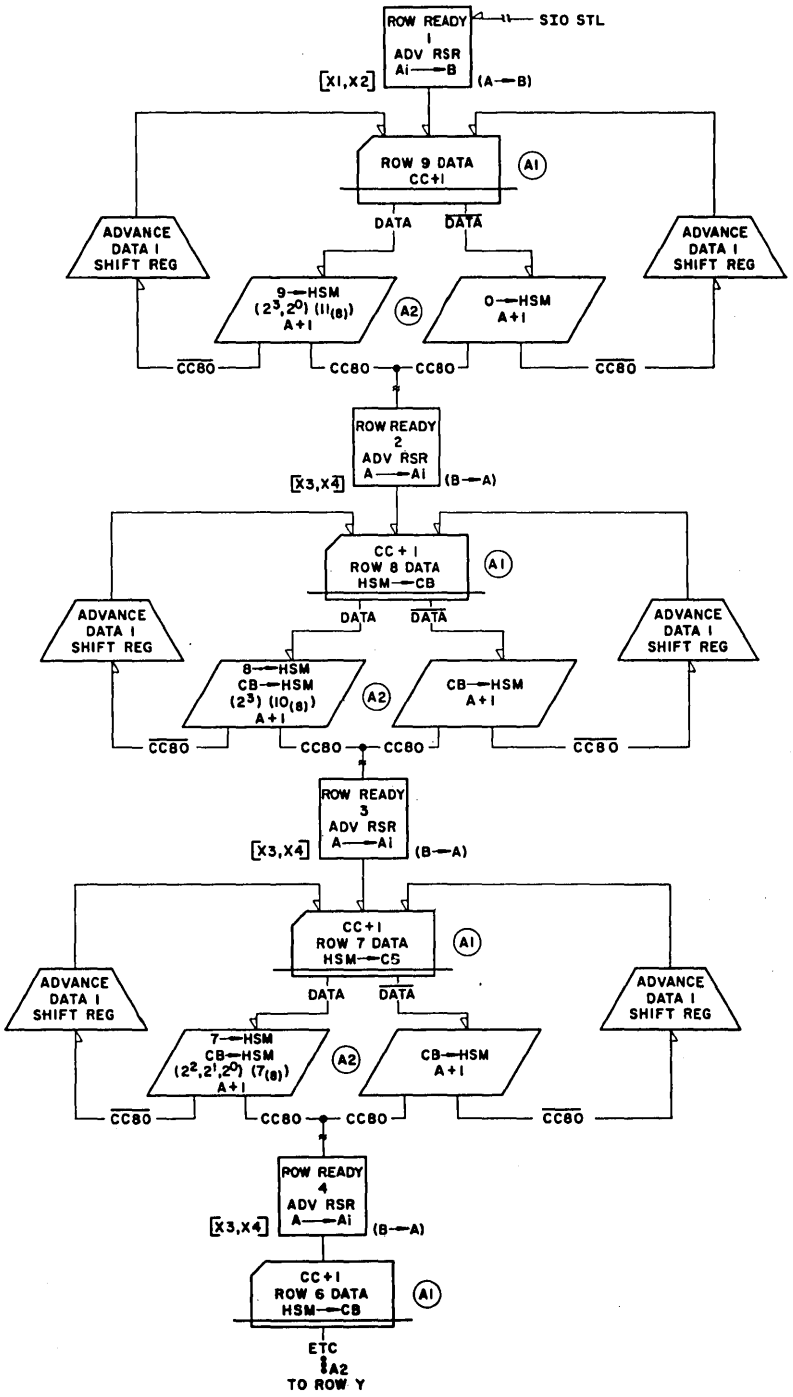


Figure 9-8. Flow Chart 314 Translating Control Module (Without BCT).

is just starting to be read. The first Row Ready pulse will generate the routine just discussed. The status level request will cause execution of an X1 status level. During the X1 status level, the contents of the A Register are gated to B in order that A initial may be remembered for the scan of each row. Next, a dummy X2 status level is executed, and from it an A1 is selected.

The normal function of the A1 status level is to access the memory location assigned to the information contained in a given column and place it in the Card Buffer (Print No. 3506035). The purpose of this is to combine information that may have been read from a previous row with the information from the row being scanned. However, because row 9 is the first row to be read, there could be no previous information. A zero (parity bit only) will be used during the time a card is being read to indicate that no punch was found in the card. During the A1 status level at row 9, instead of gating the information from memory into the Card Buffer, the Parity Flip-flop is set on the assumption that no punch exists.

Then the A2 status level will look at the first read data (stage 1 of the 80 stage shift register). If it finds that there actually was data, the information bit configuration for a 9 will be generated by developing Set 11 through AND Gate 361B1 of the translator. This octal Set level will be applied to the OR gates on Print No. 3506035, area B-3 through B-7. An octal 11 is represented by 2^3 and 2^0 bits; therefore, Set 11 is applied to OR Gates 353B1 and 355B2 to generate 2^3 and 2^0 bits when the A2 status level gates the zero out of the Card Buffer. The parity bit on the Card Buffer, in combination with the bits developed by the octal Set level, will cause A2 to gate a true Machine code nine to the bus.

Every row after row 9, when BCT is not used, will follow the same pattern as indicated on the flow chart on Figure 9-8. However, the A1 status level will bring from memory the information in the location assigned the column and will be allowed to gate this information into the Card Buffer when reading rows following row 9.

If no punch were found in row 9 or 8, but row 7 did contain a punch, the lack of data in row 9 would have allowed the zero generated in the Card Buffer to be placed, as a zero, back into HSM.

During the A1 which was executed for row 8 in this column, the zero generated by row 9 would be brought back out of the HSM location and placed into the Card Buffer. The A2, because it found that again there was no data, would allow the contents of the Card Buffer to be gated, unchanged, back to HSM. When the location was accessed for the third time, or for row 7, the zero again would be gated into the Card Buffer during A1. However, because data was found in row 7, the octal level, Set 07, will be generated and a seven will be gated back and written into HSM at the memory location.

Note that the zero generated by the lack of a punch in row 9 will constantly be written back into HSM until data is found. During the time the card is in the process of being read, a zero in a card read in HSM location means that, as yet, no punch has been found in the column which corresponds to that location.

Special consideration must be given the way in which the zone rows 0, X, and Y are treated. Because of the exceptions to the relationship of Machine to Card code (zero vs quote marks, the space, and " + Ø) a special procedure is followed in treating the information concerned in these rows (see Figure 9-9). Several sample characters will be taken and traced through the logic and flow charts, Figures 9-8 and 9-9.

The character "@" is an ordinary character in Group 1. The value of the information bits is twelve. The zone configuration for Group 1 is $2^5(0)$ and $2^4(0)$. On the card, the information value will be represented by a punch in row 8 and row 4. Group 1 on a card is represented by the absence of any zone punch.

When row 9 is read, no data is found and a zero is written to HSM (see Figure 9-8). When row 8 is read, the zero is placed in the Card

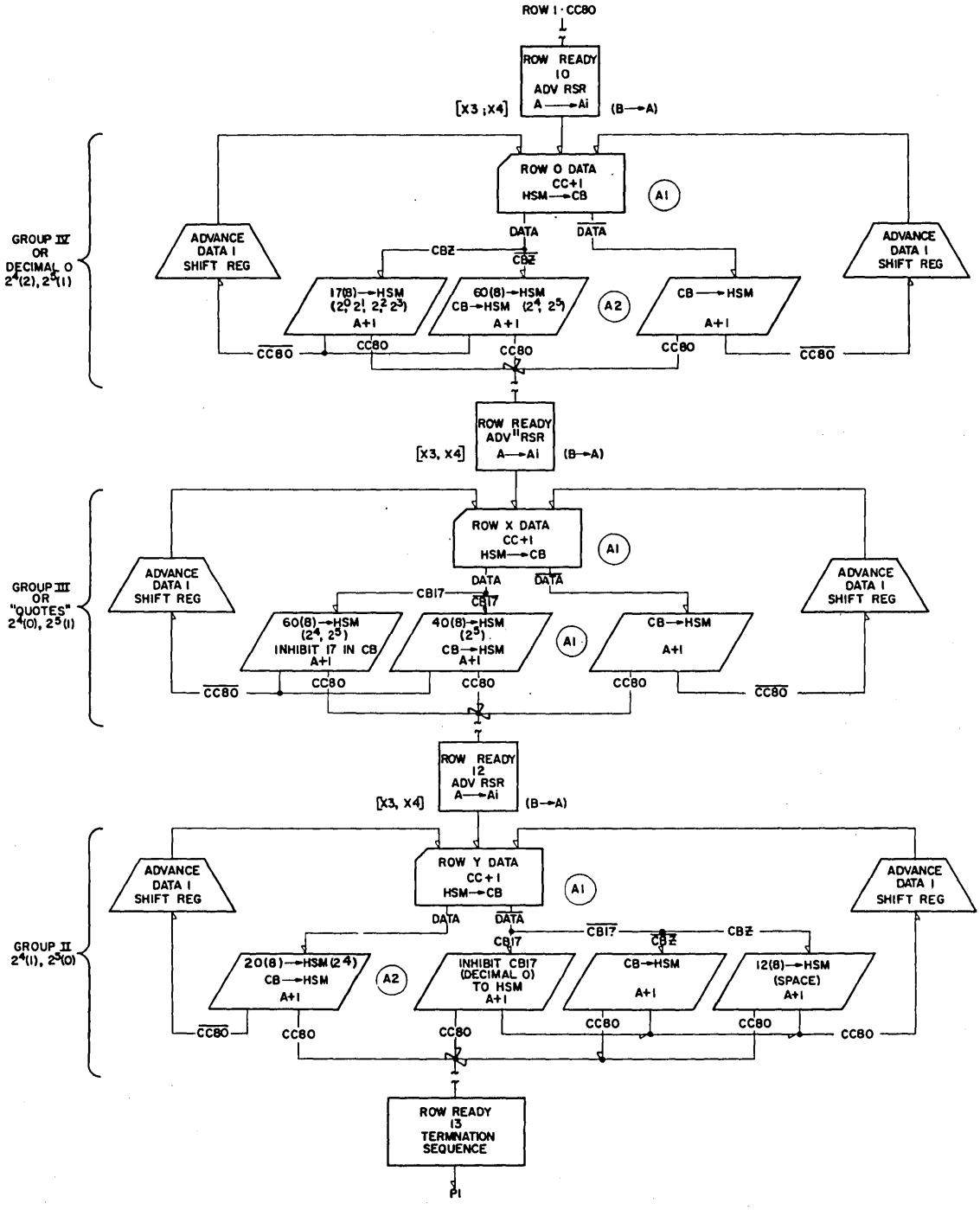


Figure 9-9. Flow Chart Translating Control Module (Zone Punch).

Buffer. Because a punch exists in row 8, the octal level, Set 10, is developed and a 2^3 bit is written to HSM. No data will be found in rows 7 through 5, and during reading each of these rows, the 2^3 bit will be brought from HSM, then written back to HSM, unchanged due to the lack of data from the card.

Row 4, when read, will have data. The 2^3 bit will again be brought from memory but now, because data is present, the octal level, Set 04, will be developed. This will cause a 2^2 bit as well as the 2^3 generated by the punch in row 8 to be written to HSM. Memory now contains an @ symbol. This character will be unchanged by rows 3 to Y because they contain no data.

Another example is the character "N" which has an information bit value of five and is in Group 3 $\left[2^4(0),\ 2^5(1)\right]$. The Card code information value is row 5 and the zone value (Group 3) is row X. Reading row 9 and finding no data will cause a zero to be placed in memory. Lack of data in rows 8 through 6 will allow the zero to remain unchanged. Data in row 5 will develop the octal level, Set 05, and 2^2 and 2^0 bits will be placed in HSM. Rows 4 through 0 contain no data so the five will remain unchanged. Row X will cause the octal level, Set 40. A 2^5 bit will be combined with the five in the Card Buffer, changing the five to an N. No data is contained in row Y so the N will remain unchanged, and final HSM contents at that location will be the character N.

The exceptions to the rule cause row 0 to be treated differently from the other rows. Because a zero is used to indicate that no punches have yet been found on the card during reading, a special configuration will be generated by data in row 0 (see Figure 9-9). If row 0 is reached, and no data is found in row 0, the contents of the Card Buffer are written to memory unchanged. If, however, row 0 is reached and data is present, two possibilities must be considered.

This punch in row 0 may be used simply as the zone punch for Group 4. In this case, an octal 60 should be combined with the previous information and the new character written to HSM. The row 0 punch could

also represent a zero. In this case, a zero should be seen in this location after the card is read.

If row 0 is reached and data in some other row was found, the zero generated at row 9 will have been changed. This means that the A1 status level will find some character other than zero in memory. If there was an information punch, the row zero punch must be the zone punch for Group 4, and an octal 60 will be combined with this information. This is true when the Card Buffer does not contain zero ($\overline{CBZ}$).

If, however, row 0 contains data and no previous row contained data, more possibilities are present. This punch in row 0 may stand alone to represent the character zero, it may stand with an X punch to represent quotation marks, or it may stand with a "Y" punch to represent "+0".

To determine exactly what the zero punch means in the case when no previous information was read, or the Card Buffer does contain zero (CBZ), the control module must first determine what lies in rows X and Y. If data is found in rows X or Y, then it is known to represent quotation marks or "+0." If no data is found in row X, the zero punch must represent the character zero.

However, at row 0 time, rows X and Y cannot yet be seen. Row Y time must be awaited and memory must store the fact that the card had a zero punch. To store this fact, a unique character will be written into HSM. The unique character is an octal 17 (all information bits). When row X is read, the Card Buffer is examined to see if it contains an octal 17. If it does, this indicates that rows 9 through 1 contained no information and row 0 did. If row X does contain data, with CB17 (Card Buffer = 17_8) the character must be quotation marks, and an octal 60 will be generated while the information bits will all be inhibited. This is done on the logic by Set 60B. The B distinguishes it from the level, Set 60A, which is generated with a zero punch and $\overline{CBZ}$.

Set 60A and Set 60B are generated on Print No. 3506036 (Set 60A from AND Gate 364B5, Set 60B from AND Gate 365B6). Both are applied to the Card Buffer (Print No. 3506035) to generate 2^4 and 2^5 bits. The difference lies in the fact that the A level is applied only here, while the B level is applied also to OR Gate 353B5 and prevents the information bits from being gated to HSM (inhibiting the octal 17).

Should no information be found in row X, the contents of the Card Buffer (octal 17 in the case discussed) will be gated, unchanged, back to HSM.

When row Y is reached, several possibilities must be cleared up. First, if there was a zero punch by itself (up until row Y), memory, at the beginning of row Y, would contain an octal 17. Lack of data in row Y, in conjunction with CB17, informs the control module that the character must be zero. The information bits are inhibited from going back to HSM by Inhibit CB17, and memory then contains a true zero. Presence of data in Row Y, with CB17 (which is $\overline{CBZ}$) indicates the character must be "+0", and "set 20" is generated to give $37_{(8)}$.

If a zero is found at the beginning of row Y, it indicates that no data was found in the column up to row Y. CBZ then, if no data is found in row Y either, will cause the control module to generate the signal Set 12 which will generate an underline character into HSM.

If no data is found in row Y but some other row (with the exception CB17 - row 0 alone) contained data, the standard procedure of gating the contents of the Card Buffer to HSM unchanged will be followed. If data <u>is</u> found in row Y, it must be a zone punch for Group 2 and Set 20 will be developed. This will cause a 2^4 bit to be combined with any previous data, thus putting the previous data into Group 2.

Data Organization with BCT

When a card has been punched in six-bit Machine code (refer back to Figure 9-5), two characters are contained in each column, 160 charac-

ters on a card. The A characters must be assembled into 80 locations from the contents of rows 9 through 4, assigning bit values to each row. The B characters must be assembled into another set of 80 locations from the contents of rows 3 through Y.

This is accomplished very simply. The first Row Ready after SIO will cause execution of an X1 and an X2 status level. This will place the contents of the A Register into the B Register to remember the starting point of each row. They, 80 pairs of A1-A2 status levels, operate in the same way they would without BCT, except data in row 9 will merely generate a 2^5 bit into HSM, row 8 data a 2^4 bit, row 7 a 2^3 bit, and so on to row 4 data which will generate a 2^0 bit.

Just before each scan, an X3 and an X4 status level will be executed to return the B Register to the A or the A Address to A initial for the scan of that row. This, of course, is not true at the beginning of row 9. X1 and X2 are executed at the beginning of row 9 to place A initial in the B Register.

Without BCT, the beginning of each row from row 8 to row X will allow execution of X3 and X4 status levels. This will cause the control module to assemble all the information contained on the card into the same 80 locations.

However, with BCT, the characters on the card number 160 and cannot be placed in 80 locations. When the end of row 4 (2^0 bit) has been reached, all bit positions in the first set of 80 locations have been used. Therefore, the end of row 4 should cause the control module to generate some status level other than the X3 and X4 and prevent the A Register from returning to A initial, to scan the same 80 locations for row 3.

This is accomplished by executing an X1 and an X2 after row 4. With X1 and X2, the A Register contents will be gated to the B Register. The A Register will be addressing one location to the right of the location which received column 80 data from rows 9 to 4. Therefore,

the X1 and X2 will change the starting point of the scan by changing the B Register contents from A initial to A initial plus 80.

Then, row 3 data will be allowed to place 2^5 bits (where data exists) into a second set of 80 locations, from A initial plus 80 to A initial plus 159. The beginning of row 2 will again execute X3 and X4. Now, the B Register will contain not A initial, but A initial plus 80 and row 2 also will place its bits (2^4 bits) into locations A initial plus 80 to A initial plus 159, etc.

The logic recognizes the need for using the second set of 80 locations on Print No. 3506038. In area D-3, AND Gate 383D1 recognizes the conditions. When BCT is depressed (it must be, otherwise the entire card should go into 80 locations) during row 4 and when the A2 status level has gated the information from column 80 (CC80) back to HSM (TP4), the first half of the card can be said to have been read. These conditions cause the ACC Flip-flop to become set, informing the PCU that the A characters are complete and the next status level should be X1 instead of X3. Note ACC will be reset as soon as the A2 is completed, so that the Row Ready for the beginning of row 2 will execute an X3.

Parity Generation (Print No. 3506035)

During the discussion of the translator, no mention was made of how good parity is ensured. The parity generation logic is straight forward in that it takes into consideration three simple truths:

1. It is known that the A1 status level will place good parity into the Card Buffer (parity would have been checked by the Memory Register).
2. It is known that any legitimate data from the card, whether BCT or $\overline{\text{BCT}}$, will add at least one bit to the character, and will add this bit where one did not previously exist.

3. A basic fact exists that adding one to a number will change it from even to odd, or if already odd, from odd to even. Adding any odd number to any odd number will generate an even number. Adding an odd number of bits to an odd number of bits will generate an even number of bits.

Therefore, because it is known that the Card Buffer will always contain good parity or an odd number of bits, all that need be done is complement the parity bit each time card data will add an odd number of bits to the previous data. On Print No. 3506035, OR Gate 357C3 takes care of this.

First, with BCT, any time data is present on the card, one bit (which is an odd number) will be added to the number of bits in the character. AND Gate 358C2 then will cause the parity information to be complemented when gating out.

Second, without BCT, Set levels will be produced (see Print No. 3506036, AND Gates 365B1, 365B2). All that need be done is apply each Set level that will produce an odd number of bits to OR Gate 357C3. Any set level, such as 07, which generates an odd number of bits will complement the parity information.

Accuracy Control - MPE

When a card is punched in 301 Card code, the maximum number of punches which may be necessary to generate any character in a given column is three. When three punches are used, one of the three must occur in row 8. When no punches are found in a column, an underline character will be written into memory. Therefore, no combination of punches which will generate an octal 12 (row 8, row 2) is legal. The Multi-Punch Error (MPE) logic (Print No. 3506036) will ensure that these illegal combinations of punches will be detected.

Any of the combinations of row and card data (the OR gates with Set levels applied) with previous card data (AND gates with CB conditions applied) listed in this logic is a violation of one or more MPE rules and will allow a Multi-Punch Error alarm.

Remember that MPE is generated due to the information as punched on the card. No amount of reading and re-reading will change the fact that one column on the card contains an MPE. Therefore, the alarm logic will not stop the Computer until the entire card has been read in. Then appropriate action may be taken.

One problem exists in the case of an MPE. The parity generation logic assumes three things, one of which is that when card data is present, it will generate one or more bits where no bits previously existed. Note here that in many cases of MPE, this assumption will be violated. As an example, a punch in row 7 and row 2 is an MPE. It will be detected by AND Gate 367C1 or 367C2 when data is found in row 2, generating Set 02 on OR Gates 368D3 and 368C1. However, row 7 data will have previously generated 2^0, 2^1 and 2^2 bits. Set 02 will again try to generate a 2^1 bit. The parity generator is incapable of coping with this situation. Although 02 is trying to add one (an odd number) bit, the total number of bits in the character remains unchanged while parity is complemented. In this case, complementing generates bad parity. In order that the Computer does not stop on a MRPE, good parity must be gated out.

This is solved by "blanking out" the character which caused MPE. Print No. 3506036 shows this. The A1 status level will place the previous information into the CB at TP5, and it will then be known that MPE exists. The next TP0 (which brings an A2 status level) will prime AND Gate 365C4 and Pre-MPE will be set (provided an A2 status level is actually present to put a low on the reset input). P-MPE generates the signal, Set 57, which will cause a $57_{(8)}$ to be gated to HSM, assuring good parity.

At TP5, when the 57 has reached memory, the MPE Flip-flop will be set. The error, however, cannot be gated out to stop the Computer until the entire card has been read (End set).

Note that with BCT, any number of punches in any combination is legal. MPE cannot be generated because no Set level can ever be produced when BCT is depressed.

Accuracy - Termination

Little mention, to this point, has been made of the second read station. Logically, this read station is identical to the first read station. It will be loaded with the contents of each row (strobed during RL2 through RL13) one Row Level after that row has been read by the first read station.

The Computer uses the data contained in the Data 2 Shift Register in a simple way -- it "counts" the number of times data has been seen in the second read station.

Two four-stage binary up-counters are seen on Print No. 3506037. The first is the Hole Count Register (HCR). Each time a hole is found by the first read station, this counter is triggered plus one. The second is the Check Card (CKC) Counter. Each time data is found in the second read, or check station, it also is triggered plus one.

When the entire card has been read, if no punches were lost or gained by the first and second read, the CKC will have been triggered exactly the same number of times the HCR was triggered and they should each contain the same bit configuration. A compare will be made to determine that they actually do contain the same configuration. If a non-comparison occurs, a Card Compare Error (CCE) alarm will be generated and the Computer will stop, indicating a punch was either lost or gained.

The greatest problem created here is that stemming from the fact that when row Y has been read into HSM, it has not yet been strobed into the second read station. Memory time need no longer be used, but the last row must be advanced out of the second shift register in order to trigger the CKC equal to the HCR.

The termination routine begins with the thirteenth Row Ready pulse. The first twelve Row Ready pulses were used to read the card and the thirteenth will indicate that row Y has been loaded into the second read shift register and the number of holes in the card must be counted. However, status levels must no longer be executed (memory contains all the card information after the twelfth Row Ready). Therefore, the logic will generate "artificial" timing to simulate pairs of A1 or A2 status levels. This is accomplished by the Off-Line Check (OLCK) Flip-flop. This flip-flop, while set, will allow the Column Counter to be triggered up, the Check Counter (CKC) to be triggered according to read data from the second shift register and the second read shift register to be advanced so that each bit may be examined.

To begin the row Y check sequence, the logic must first be prepared. When CC80 for row Y is reached, the End Flip-flop on Print No. 3506037, area C-3, is set. This indicates that the last row of the card has been read into memory and the need for memory is ended. The End Flip-flop primes AND Gate 384C2, which will produce the output, Instruction Terminate, when the card has been read and checked.

Each time the Computer reaches CC80, N-RES will be developed to cause the Computer to wait for the next Row Ready. During reading, the status level waiting to be executed will be an X status level. However, at the end of row Y, the control module no longer needs memory time, so a P1 will be selected (R12 is used to cause P1 to be selected). When the Instruction Terminate signal is developed, P1 will be executed and the next instruction staticized.

To develop Instruction Terminate, row Y must first be checked. At the end of row Y, AND Gate 384C2 will have all primes except Miscellaneous (MSC). The MSC Flip-flop is found on Print No. 3506036, area B-2.

At the end of row Y, the Computer will await the thirteenth Row Ready pulse. When it arrives, the Row Ready routine will be followed (see Print No. 3605038, area B-6, and Figure 9-7). At TP1, with Row Ready, MSC will be set (row Y is still present in the shift register at TP1 since the shift register will not be advanced until TP2).

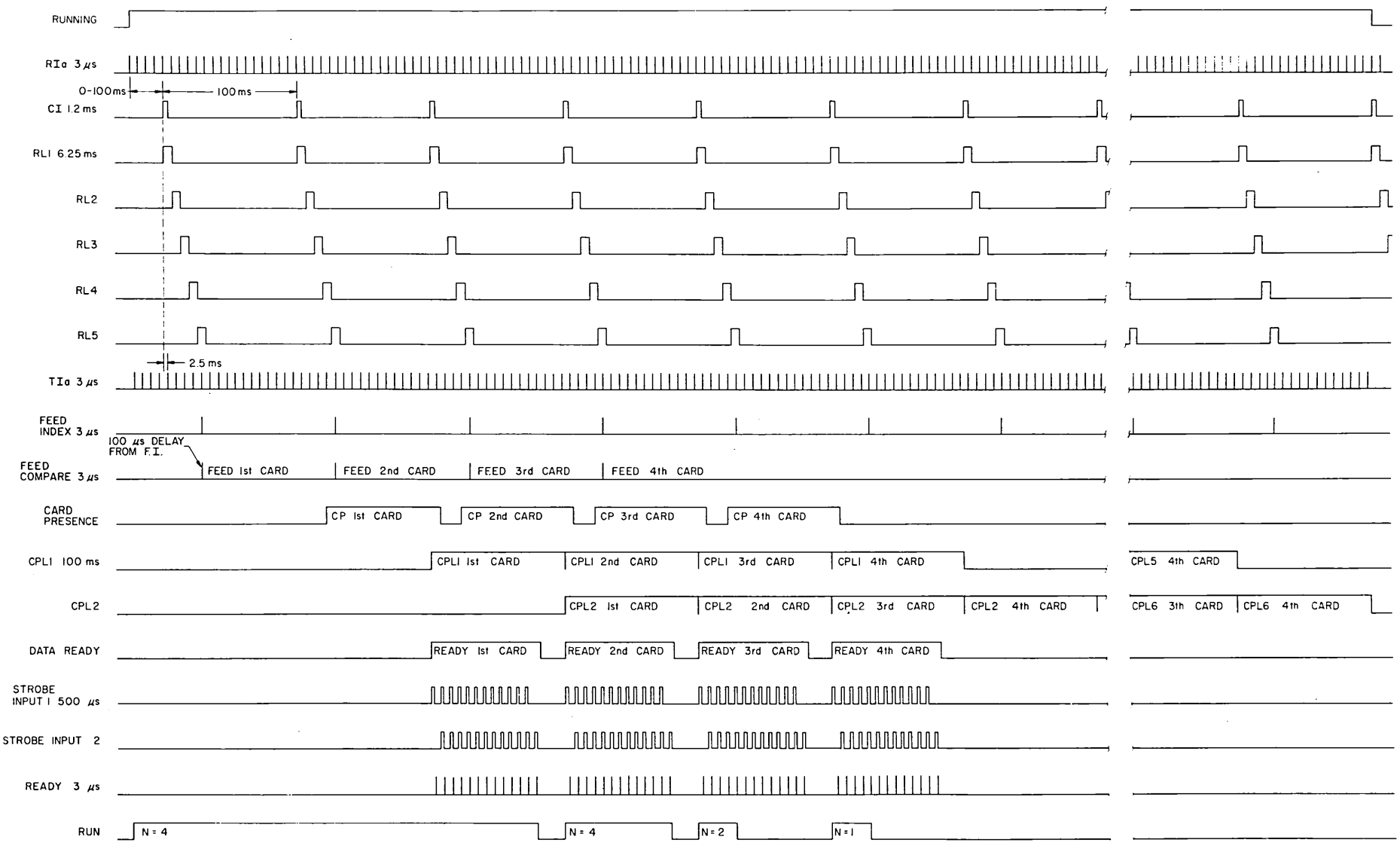
On Print No. 3506038, setting MSC would appear to provide the last condition for developing Instruction Terminate. Note, however, (on Print No. 3506036) that the signal TP1 Row Ready (from AND Gate 364C1) allowed MSC to be set. This same signal is taken to Print No. 3506038, OR Gate 386D1, and resets the Column Counter. At Row Ready TP1 time then, the MSC prime will be applied to AND Gate 384C2, but the same signal that gives MSC will cause the other prime, CC80, to be lost.

It is now necessary to obtain CC80 to terminate. To get CC80, the Column Counter must be triggered up. No more A1 status levels will be generated by this instruction (the card is already in memory), so OLCK must be used to trigger the Column Counter.

To cause OLCK to become set, a trigger pulse must be applied to it. To trigger OLCK, P-OLCK must be set. P-OLCK will be set by the fact tha t MSC is set at Row Ready TP3 time. Every TP1 thereafter, as long as P-OLCK remains set, OLCK will be triggered. When it goes to the set state, it will allow the Column Counter to be triggered up at TP2 while AND Gate 375D1 will allow the CKC to be triggered up according to the data in read station 2. At TP56, it will cause AND Gate 394B8 to produce Shift which will advance the Data 2 Shift Register. It also advances Data 1, but the Data 1 information (all zeroes) is being ignored (see Print No. 8619092).

At TP1, the P-OLCK Flip-flop will allow OLCK to be triggered reset. While OLCK is in the reset state, nothing happens. The triggering of OLCK set and reset simulates the timing generated by A1 and A2 status levels during reading to ensure proper recovery time for the shift registers. The cycle continues until a TP2, during which OLCK is set and the Column Counter is triggered to 80.

Once CC80 is reached, Instruction Terminate is developed through AND Gate 384C2. At TP4, Instruction Terminate primes AND Gate 378C2 to allow CCE to be set if CKC does not compare to HCR. At TP5, Instruction Terminate (on OR Gate 384B3) generates N-REQ, allowing the Computer to execute the P1 which was selected by the A2 status level which wrote column 80, row Y data to memory. TP5 also allows P-Busy (387C2) to be reset and TP0 will reset Busy. TP1 will generate Housekeeping (HK) and the control module will be freed.



MASTER TIMING DIAGRAM MODEL 323 CARD READER

ICT CARD PUNCH AND CONTROL

The Card Punch, Model 334, in conjunction with the Card Punch Control, Model 315, is used to punch 80 column Electronic Accounting Machine (EAM) cards in 301 Card code, by row, at the rate of 100 cards per minute. The cards are placed face down, 9 edge first, into the input (feed) hopper, which has a capacity of 800 cards. The cards will pass through the machine when being punched, and will be deposited in the output (stacker) pocket. Any rejected cards will also be placed in the output pocket, but these cards will have their edge offset 3/8 inch in the pocket if Error Detection is used in the future. The output hopper will also hold 800 cards.

The machine can operate in two modes. One mode exists when it is under control of the Processor; the other mode is called the Gang Punch Mode. The Gang Punch Mode is used primarily for adjustment of the timing of the unit, and makes servicing the unit itself a very simple procedure. Since the unit has its own power supply, the test mode (Gang Punch Mode) allows the unit to punch as many duplicates of an initially punched card as the technician wishes, without using valuable Processor time.

PROGRAMMING

Due to the type of mechanical operation of the unit, programming is a very simple procedure. The Operation Code is a 2 or 3 indicating a normal or simultaneous punch operation. The N character must be a zero (0) to indicate a CPN/CPS. Anything other than zero would indicate BCPN/BCPS. The A Address indicates the HSM address of the first character to be punched and the B Address indicates the HSM address of the last character to be punched.

Thus, with one instruction, punching will continue until A-B Equality (ABE) is reached, and as many cards as are necessary to contain the information being punched will be fed by the unit. If it is wished, all of memory can be punched with one instruction. A typical example of a Card Punch Normal instruction would be:

2 0 0000 0199

The above instruction would then proceed to punch the arithmetic tables (which contain 200 characters) on to three cards, with 40 unpunched columns left on the last card. When ABE is reached, the instruction would terminate. It would require about 1800 milliseconds to punch the three cards.

Upon termination of this instruction, because of the mechanical arrangement of the unit, the last card punched would remain in the transport mechanism, just ahead of the read-check station. This card must be checked and placed in the output hopper. In order to do this, two "dummy" instructions are necessary; one to check the card, and one to place the card in the output hopper.

These dummy instructions will feed two cards (one each). Therefore, each instruction must have the A Address initially equal to the B Address with a non-punchable character in that location.

These cards that are fed will remain in the transport mechanism, but this has no effect, since one of these cards must be under the punch

die to give an Operable level in order to punch any more cards. One card will be just before the punch station, the other will be just before the read-check station. A third card, which also is unpunched, is sitting just before the output hopper. This card was fed by the instruction which punched the last card.

CARD PUNCH MECHANICS

Because its operation is restricted by its mechanical functioning, the Model 334 Punch requires a minimum of control signals from the control module, thus allowing logical simplicity. Once the unit has started on a card cycle, it must unconditionally finish that card cycle. The Punch only requires punch information from the Processor to punch the card, and a card under the read brushes to send punch data to the Processor.

The transport mechanism (Figure 10-1) is fed by an input hopper which will hold 600 to 800 cards maximum. The first set of feed rollers is used to grasp the card from the picker knife. (The lower roller will move downward to allow the card to come between it and the upper roller, so that the card may be tightly gripped when the lower roller again moves against the upper roller.) The first feed rollers push the card between the punch station die and the punch guide assembly. The second set of feed rollers is used to take the card from the punch station and feed it into the check station. The check station consists of segmented brush blocks (a row of brushes, electrically separate, for each column). The brushes rest on a contact roller which has a copper shell and is used as the common return for the brushes. The third set of feed rollers is used to pull the card all the way through the check station, and place the card in position to be placed in the output hopper. The stacker rollers are used to take the card and force it into the output hopper.

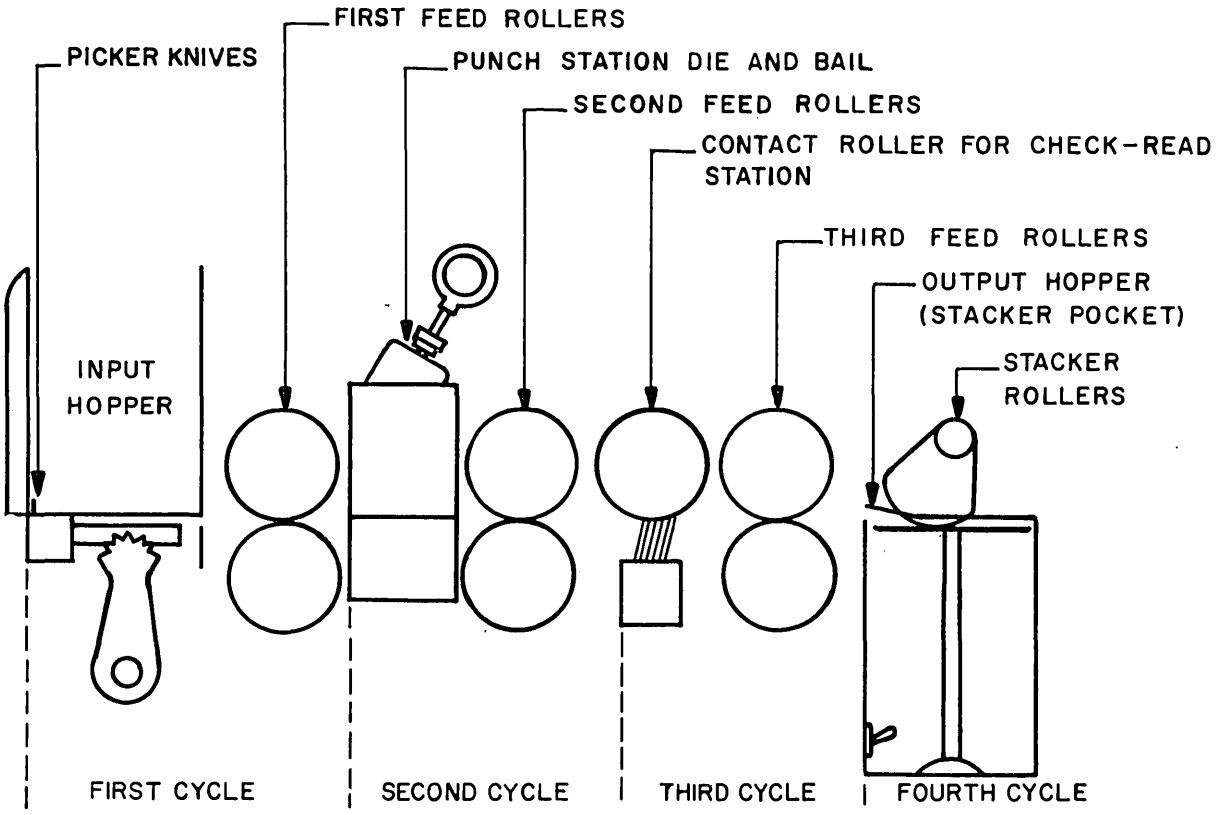


Figure 10-1. Simplified Transport Mechanism (Side View)

There are four card cycles associated with the transport mechanism. The respective card cycles will occur in the following sequence:

1. When the card is fed into position just before the punch station die.

2. When the card is punched and placed before the read-check station.

3. When the card is checked and fed into position just before the stacker rollers.

4. When the card is placed into the output hopper by the stacker rollers.

Once one of these cycles has been initiated by the Processor, the mechanics of the unit will finish the remaining cycles. Card movement in the Punch is an eccentric (Start-Stop) movement since all rollers are driven by a Geneva mechanism. The card punch must have an eccentric movement so that the card will not be in motion when it is being punched. Thus, for simplicity in timing, all mechanisms except the punch bail are driven by the Geneva mechanism. The picker knives however, have a smooth motion since they are driven by cams.

The Geneva mechanism consists of a gear with seven slots machined into it so that it transforms uniform rotary motion into start-stop eccentric motion. Since a card cycle in the Punch consists of 14 rows (a movement of ¼ inch per row), the Geneva will turn two revolutions per card cycle.

The cam which turns the Geneva is driven by a pulley which is belt-drived from the motor. When the machine has been turned on, the motor can run if a command is sent from the Processor. As long as the motor is running, the Geneva is turning. The feed rollers do not need to turn at this time, so there is a seven-point ratchet clutch which connects the feed rollers to the Geneva output drive for motion, only when it is necessary to perform a card cycle. The punch bail however, is continuously moving, since it is driven by a vernier gear, which is driven by the eccentric shaft drive gear.

Card Feed

When a Run Command is sent from the Processor to the Punch mechanism, it energizes a magnet (Feed solenoid) which will then release a ratchet arm. This ratchet arm is actually part of a clutch assembly which is used to connect the output motion of the Geneva mechanism to the feed rollers.

The clutch assembly consists of a 14-point clutch which is driven by a shaft (belt driven from the motor). On this shaft exists a Constant Running Cam (CRC) which also has 14 points. A set of switch

breaker points are driven by the CRC, and are used to energize the magnet (Feed solenoid) at the proper time, when a Run Command is received from the Processor.

When the ratchet arm is released, it will engage the 14-point clutch at the nearest point, and the clutch will then turn on the shaft. The clutch will turn a cam which drives another ratchet arm. This second ratchet arm will then act to engage the drive from the Geneva mechanism to the feed rollers and a card cycle will be initiated.

During a card cycle, a card will always be fed, and will move through 14 start-stop motions, unless it is being fed by the picker knives. Since the card has 12 rows, and the cards are spaced two rows apart, one card cycle equals 14 rows. One start-stop motion is equivalent to one row of the card. Thus, each row will be motionless when it is being punched, or read-checked.

When the first ratchet arm (which initially engaged the 14-point clutch) comes around through a complete circle, if the run level has dropped out, the magnet will then re-latch the ratchet arm, thus removing the drive from the 14-point clutch. This would cause the end of the card cycle, and no further movement of the cards in the transport mechanism would exist.

If a Run level existed at the time that the ratchet arm came before the Feed solenoid, the Feed solenoid would not re-latch the ratchet arm, and the machine would go through another card cycle. The machine would continue to go through card cycles until the Run level finally dropped out.

Thus, the number of cards fed and punched would depend upon how long the Run level existed in the unit. Since the instruction will only terminate on ABE, the Run level is held up until ABE is reached in the Processor. When ABE is reached, the Run level drops out, and the correct number of cards necessary to contain all the punched information have been fed.

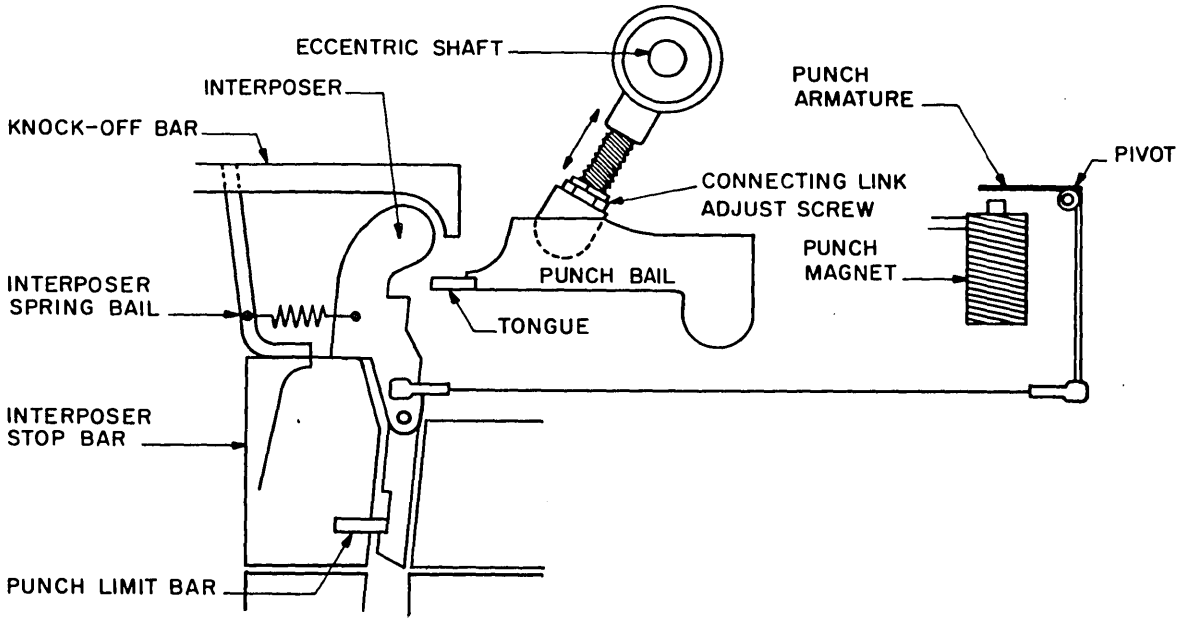


Figure 10-2. Punch Mechanism

Figure 10-2 shows the Punch mechanism. As previously stated, the eccentric shaft is being driven continuously by a vernier gear from the cam which drives the Geneva. Therefore, the punch bail is constantly moving up and down. It is synchronized with the Geneva so that when the punch bail is in its lowest position, a row of a card will be directly beneath the punch knives and held without motion.

Punching will occur when a specific row of a card is coming under the punch die. The Processor will search memory and fill an 80 stage shift register with one bits, in accordance with the information in memory. The registers which contain one bits will then energize the punch magnets corresponding to their column location. When the punch magnets are energized, the armature will pull the interposer forward. When the punch bail begins its downward stroke, the punch bail tongue will engage the slot in the interposer, and will then drive the punch

knives through the card. If a magnet is not energized, the interposer will be held against the stop bar by the interposer spring. Since the interposer is not pulled forward, the tongue cannot catch the slot of the interposer, and a hole will not be punched in that column.

Read - Checking

During the next card cycle after punching, the card is checked for accuracy by reading it. The read-check station consists of 80 wire brushes and a contact roller. The contact roller has an outer shell made of copper, which is electrically insulated from the frame of the unit. A common brush is used to complete the circuit for the contact roller. Each of the 80 brushes is electrically separate, and they are used to drive transmitters which send the read-check information over to the Processor.

A negative 48 volt level is applied to the contact roller through the common brush. Then, when a row comes under the contact roller, the brushes will fall through the holes in that row and make contact with the roller. The negative 48 volts will go through these brushes and cause the corresponding transmitter to give a high output. This information is placed into a register in the control module, and eventually checked against what should have been punched. If there is no equal comparison, a Card Compare Error (CCE) alarm will be generated. On the last card cycle, the card will be forced into the output hopper by the stacker rollers.

UNIT CONTROL SIGNALS

Certain control signals are used in the Card Punch to insure accuracy in punching and reading, and to tell where a card or a row of a card is in relation to the transport mechanism. Two control signals are used to indicate where a card is in relation to the punch station and in relation to the brush read-check station.

A short lever is mounted in the transport mechanism just before the punch die. This lever is used to actuate the Die Card Lever switch. When a card is in position before the punch die, the lever will be pushed upward, activating the Die CL switch, thus giving indication that there is a card ready to be punched, and that punching can occur. This could be termed a Card Presence level.

Another lever and switch unit is for the read-check station. When the card is in front of or under the brushes, the Brush Card Lever switch will be activated, thus giving a Brush Card Presence level. This level will be used in the Processor to control the comparison of the punch information and the read-check information.

There are three types of cam and switch assemblies within the unit (see Figure 10-3). Type one is used to keep a switch actuated for most of a card cycle, or a small portion of a card cycle. Examples of this are P2 (Start Hold), P3 (Error Reset), P4 (Operable Hold), and P5 (Stacker Roll Contact).

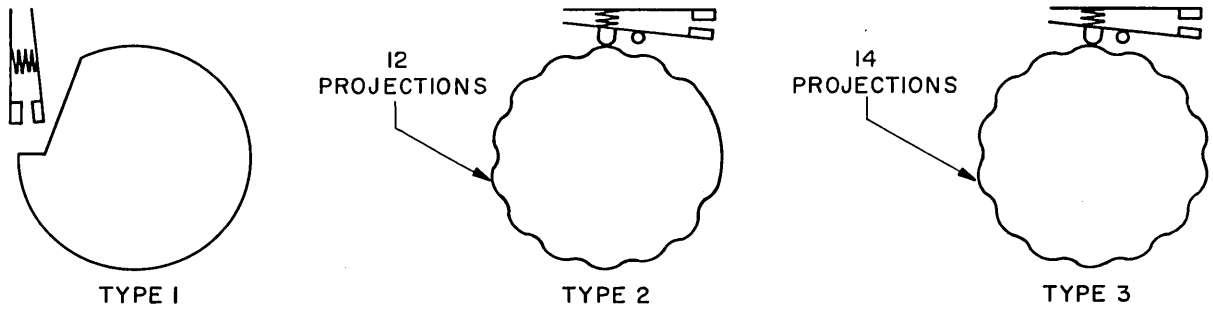


Figure 10-3. Cam and Switch Assemblies

Type 2 cam and switch consists of a cam with 12 out of 14 possible projections spaced around the periphery of the cam. A switch is actuated by the cam movement so that the switch will make contact 12 times during one revolution. These pulses from the switches will generally be used to indicate when a row is ready to be punched or read.

Examples of this type of cam are called circuit breakers (CB), i.e., CB1, 2 (make CB punch); 4 (break CB punch); CB5 (make CB check); CB6 (break CB check).

Type 3 cam and switch consists of a 14 point cam with a set of breaker points. This forms the Constant Running Cam (CRC), which is the index cam. This switch is used in relation to the 14 point clutch. There is only one of this type in the mechanism. This type of cam and switch will give 14 pulses per revolution, with one revolution corresponding to one card cycle. This pulse is used to determine the correct time to energize the clutch actuation solenoid.

Three other pulses are produced by the ICT punch mechanism, strictly for Processor use. These are Card Index, Punch Index, and Row Index. Card Index is produced by a photo-diode sensing unit, which looks at the edge of a revolving disc. The revolving disc has a notch cut into its edge. When the notch rotates between the photo-diode and light unit, it allows the light to activate the photo-diode, and inhibits producing a Card Index pulse. The CI pulse is produced at all other times of the revolution of the disc. A Card Index pulse will then exist for 518 milliseconds of a 600 millisecond card cycle.

Row index is produced by a photo-diode sensing unit which looks at the edge of a disc with 14 notches on its outer perimeter. When the photo-diode sees the light through a notch in the rotating disc, a Row Index pulse is produced. Fourteen Row Index pulses are produced every card cycle, with a time duration of 43 milliseconds from leading edge to leading edge.

Card Index is used in conjunction with Row Index in order to produce Punch Index. This will be discussed under Machine Logic.

DISCUSSION OF TIMING CHART (Print No. 8616545)

As discussed previously, most control signals for use in the ICT Punch are generated by contact timings of switches actuated by card movement

and cams. Print No. 8616545 shows the relationship that should exist between these signals and the card and punch bail stroke motion during a card cycle.

Looking at the top of the chart, the index points referred to can also be seen on the index timing gear on the Punch Unit. This timing gear has indices cut into it and labeled from 1 to 14 inclusive. It should be noted that each labeled index corresponds to each increment of ten teeth on the timing gear. The gear contains 140 teeth around its periphery. Point 13.5 (point 13 plus 5 teeth) is labeled with a D to indicate the starting point of the card cycle. The letter D refers to datum point, or the point of reference of all pulse data.

The Timing Chart then, covers one card cycle, or 600 milliseconds. There is a time of 42.86 milliseconds per row and 4.286 milliseconds per tooth, since the timing gear turns through one revolution per card cycle. The timing chart is used primarily for maintenance, and to show when, during the card cycle, the various contacts should be generating a control signal, or at what point in its movement the card or mechanical assemblies should be.

If the 14 point clutch is engaged by hand at point D and the mechanism is moved by manual force applied to the hand crank, the timing of the contacts can be checked against the chart to ensure that the proper tooth of the timing gear is being indicated by the arrow, when the contacts are opening or closing. As an example, when point 9 is adjacent to the indicating arrow, CB1, 2 should just be making contact at that point.

MACHINE LOGIC

Due to mechanical timing, the Punch does not require a great deal of logic in order to perform its functions. Thus the unit has only a small amount of logic within it, the greater portion being relay logic.

In order to operate the Punch, certain conditions must exist on Print No. 8616544. The Safety relay (K103) and the Operable relay (K102) must be energized.

The coil for K103 is in area B-3, and two conditions must exist before it can be energized. The Die Contact switch (contacts DC-1 and DC-2) in area C-3 must be closed. This condition will exist when the die block is locked in. The second condition is that the Knockoff Contact switch (contacts PB1-A and PB1-B) must be closed. This condition will exist when the knockoff bar for the interposer knives is locked on. Then when the Power On switch (SDS 202) is depressed, K103 will have -19.5 volts applied through it, and will become energized. When K103 is energized, contacts 4 and 5 in area B-3 will be a prime for energizing K102 (Operable).

Starting in area C-3, four conditions are then necessary to energize K102. The Interlock switch (S501) must be closed, which indicates the cover is on the punch mechanism, the Punch Stacker switch (contacts 1 and 2) must be closed indicating that the output hopper is not full, and the Die CL switch (contacts, DL-1 and DL-2) must be closed. When these contacts are closed, this acts as a Card Presence level, effectively saying that a card is just before the punch station, and is ready to be punched.

This first card must be placed in the transport mechanism before the Processor can use the Punch. This is done by depressing the Start button (SDS 204) in area A-5. Contacts 5 and 6 will cause K104 (Run) to be energized. Contacts 4 and 5 of K104 in area B-8 will energize K109 (Start) because K103 has been previously energized. Contacts 2 and 3 of K109 in area D-2 will cause SCR 101 and SCR 102 to conduct, thus starting the punch motor.

The motor will start to drive all engaged gear mechanisms and the Constant Running Cam (CRC). CRC contacts 1 and 2 in area C-3 will then energize K108, which will then hold itself energized by contacts 4 and 5, area B-3. K108, contacts 17 and 18 in area B-6, will then

energize the Feed Coil since P1 is closed. P1 will cause the feed clutch latch to engage the feed clutch, coupling eccentric (Start-Stop) output motion from the Geneva mechanism to the rollers, while the feed knives are operated by the feed cam, thus feeding a card. The unit will continue to go through the card cycle until K102 is energized. K104 will then be de-energized by contacts 1 and 2 of K102, area A-6, and remove primes for holding K109 and K108 energized.

K109 however, has a self-holding contact in series with contacts of P2 (Start Hold), which will hold K109 energized until one tooth before the end of the card cycle. P2 will release, and release K109 so that the punch motor can eventually stop. K108 will immediately release when K104 releases, so that the feed coil will not be energized again, and no more cards will be fed.

Thus, when Start is initially depressed, and even though it may be held depressed, only one card will be fed, so that the Die CL will prime for energizing K102, in order to have Operable. Contacts of the Mag Card Lever, when closed, simply mean that the input hopper (magazine) is not empty.

When K102 is energized, contacts 4 and 5 in area C-4 will give Operable (P). Contacts 2 and 3 in area B-6 will permit a Run level from the Processor to energize K104 in order to feed cards, when punching occurs. It can be concluded that the punch motor will not be running between runs of the Unit (see Figure 10-4).

When the 14 point clutch is engaged, and the machine is running through the card cycle, all the P and CB cams and timing discs are rotating and generating their respective outputs. The timing discs which produce CI and RI are rotating to produce these levels. These levels can be seen in area D-4 through D-7.

PA 2 (area D-6) is used to produce CI, and will have a high output from pin 24, only when the photocell sees the light through the notch in the disc. CI will therefore always be negative when present to

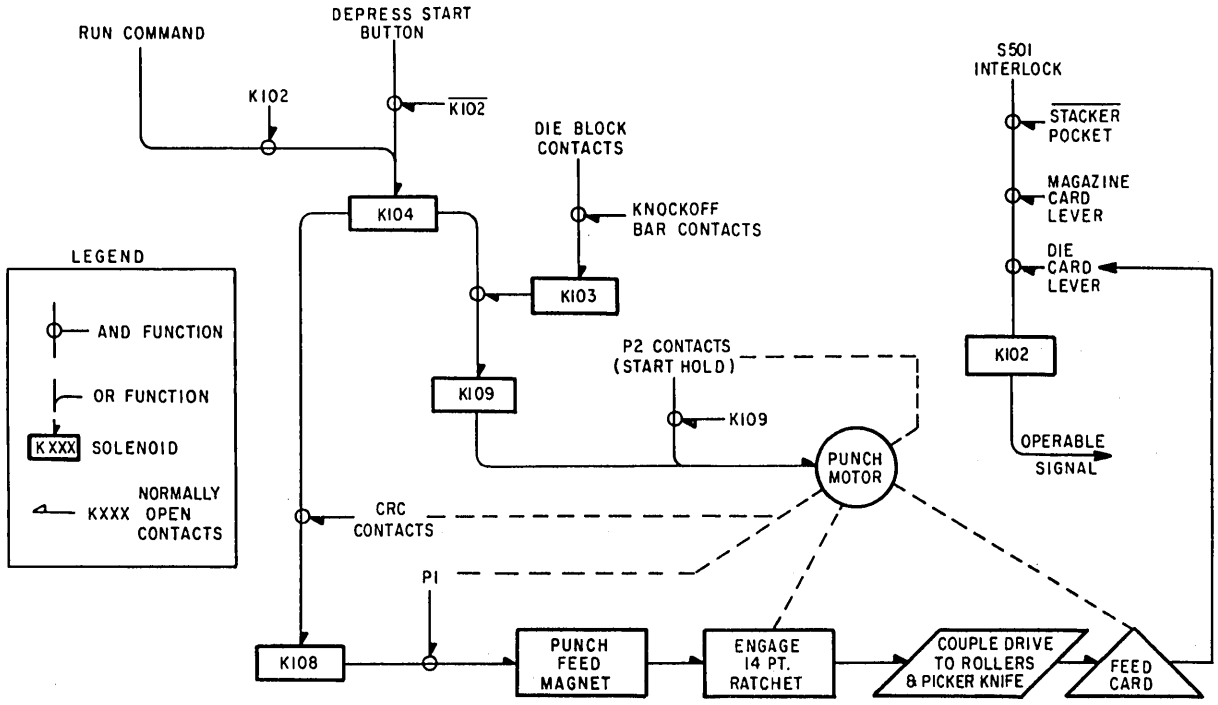


Figure 10-4. Relay Sequencing for 334 Card Punch (Starting or Run).

prime AG1 (area D-5). From IV1 (area D-4) Card Index is positive when present. This will be a 518 millisecond level. CI will prime AG1 from the time that Row 9 to Row 12 of the card is under the punch station. CI is a prime for producing Punch Index.

Row index is produced from PA1 (area D-6), when the photocell unit detects the light through the notches in the timing disc. It will exist as a high on pin 23 for 21.5 milliseconds, 42.86 milliseconds from leading edge to leading edge. This pulse, through IV2 (area D-5) becomes a negative pulse, producing Row Index (N) and priming AG1 pin 9 to produce Punch Index (P) when CI is present.

Therefore, Punch Index will occur simultaneously with RI. Only 12 PI's will be produced due to CI, compared to 14 RI's. Only CI (P) and PI (P) are sent to the Processor.

CB 1, 2 and 3, 4 are used when punching to determine when the punch magnets should be energized. Since the CB contacts are driven from 12 point cams, one point on the cam is equivalent to a row. CB 3, 4 are closed one tooth before CB 1, 2 and will open in the reverse manner. This method of using a set of contacts to make a circuit, and another to break the circuit allows easy adjustment as to timing. The timing for these CB's can be seen on the Timing Chart (Print No. 8616545). CB contacts are shown on Print No. 8616544, in area C-4. They are used to apply -19.5 volts to one side of the punch magnets so that they may be energized if their corresponding solenoid driver CD 80 (area C-6) is primed. The CD 80 solenoid drivers will be energized by punch information which comes from an 80 stage shift register in the control module. One bits in the shift register will prime the corresponding solenoid drivers, and when the entire circuit is closed by CB1, 2, the corresponding magnets will be energized.

The CB's will cause the magnets to be energized just before the punch bail starts on its downward travel, so that the interposes will be pulled. CB 3, 4 will then release the magnets when the punch bail is on its downward movement so that the shift register can be set up for the next row. This will occur for each of the 12 rows punched.

CB5 and CB6 are used to determine when read-check strobing of the card should occur. These CB contacts are in series when used by the Processor and their timing is staggered to allow convenience in make and break timing adjustment.

Contacts of CB5 and CB6 can be seen on Print No. 8616544, area C-7. They are used to apply -48 volts to the contact roller at the correct time. The correct strobing time is shown on the Timing Chart, (Print No. 8616545). As each row of the card comes between the brushes and the contact roller, CB5 will permit the -48 volts to be applied to the contact roller. The brushes will have fallen through the corresponding holes in the card and will make contact with the Roller. The -48 volts applied to the brushes will then be applied to the corres-

ponding LS transmitter (area D-6), which will send the levels to the Processor in order to place one bits in an 80 stage shift register. This information will then be checked against what should have been punched.

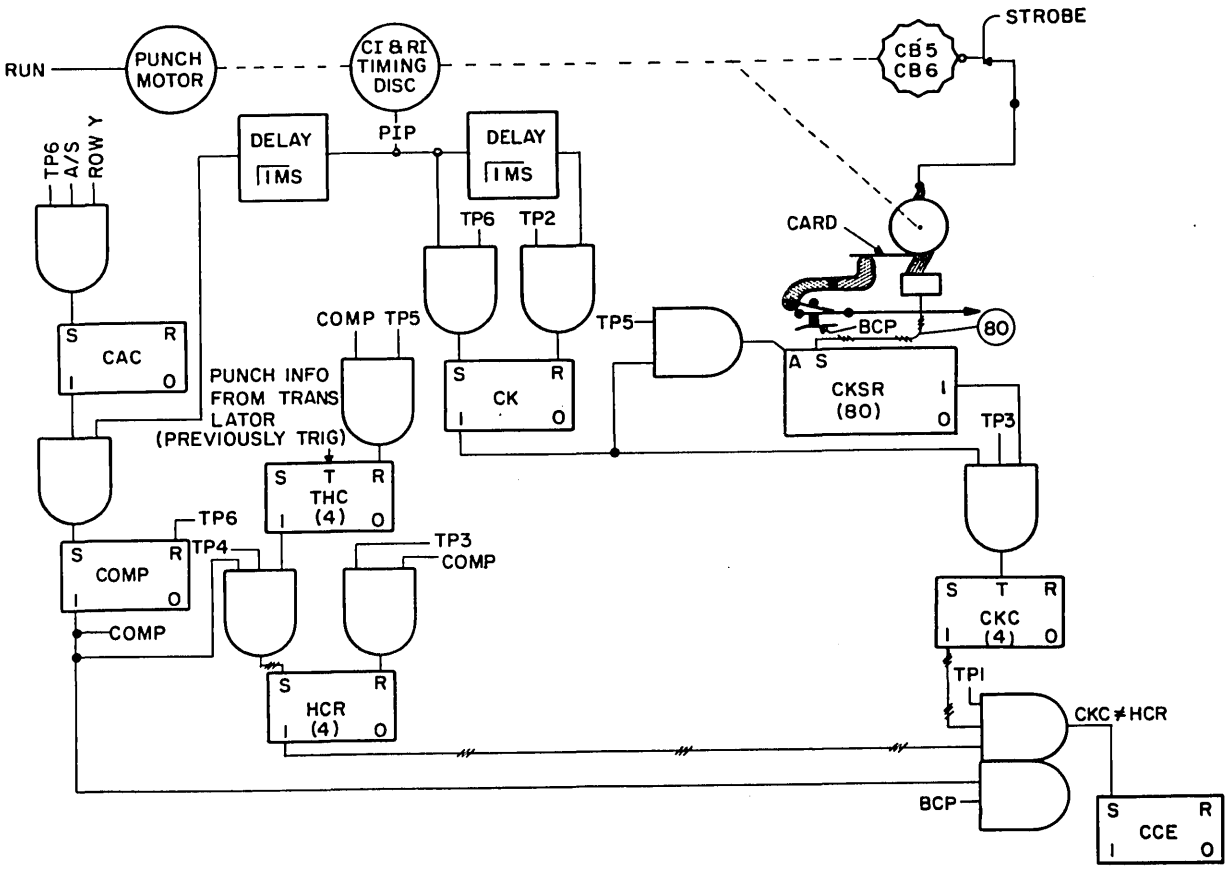


Figure 10-5. Card Check Circuitry

In order to check this information however, some level is needed to tell the Processor when a card is under the read-check station. This is the Brush Card Presence level (area C-3), produced by the Brush Card Lever when a card activates the switch contacts BL-1 and BL-2 (area C-4).

The last portion of logic is that of the reject function. This is not now used in the Processor. When a card is rejected, it is simply offset in the output hopper (stacker) 3/8 of an inch. This is done by setting FF1 (area C-7) with an error indication. This will then energize K105 through CD-81. Contacts of K105 (Offset) are shown in area B-7. Contacts 4 and 5 will make and will energize L2 (Offset Stacker coil) when P5 makes contact during the card cycle that the checked card is being placed in the output hopper. This coil will cause the stacker rollers to offset the card 3/8 inch. Then, when P3 makes contact nine milliseconds later, FF1 is reset. The Punch will then continue normally and all preceding cards will be placed in the output hopper normally.

CONTROL LOGIC

The ICT Punch Control, Model 315, consists of five rows of 301 logic within the Processor. It is used to allow the ICT Card Punch, Model 334, to punch 80 column EAM cards in 301 Card code, according to information in memory. Due to the instruction format, one instruction will punch information on the cards, feeding as many cards as are necessary, until ABE is reached. Those cards will be checked for accuracy one card cycle behind punching.

The Card Punch Control module is addressed by a zero (0) in the N character of a Card Punch instruction. This zero will be the only indication that the Punch instruction is a CPN rather than a BCPN. The logic for this is seen on Print No. 8617037, Op Dec Matrix 1. AND Gate 377D1 will have a high out if an instruction with a two (2) in the NOR Register is staticized. Through OR Gate 377C3, two gates are primed, 377C1 and 377C2. Depending upon a decimal zero in the N Register, CPN or BCPN will be generated. Model 315 is addressed by CPN.

Simplified Operation

Due to the mechanical operation format of the ICT Punch, the Card Punch Control does not require a great amount of control logic. All that is

necessary to feed a card is the Run level from the control module, and all that is necessary to punch a card is information in the Card Punch Shift Register (CPSR). To read-check a card, it is necessary to have a card under the read brushes, and this information is sent, row by row, to the Check Count register (CKC).

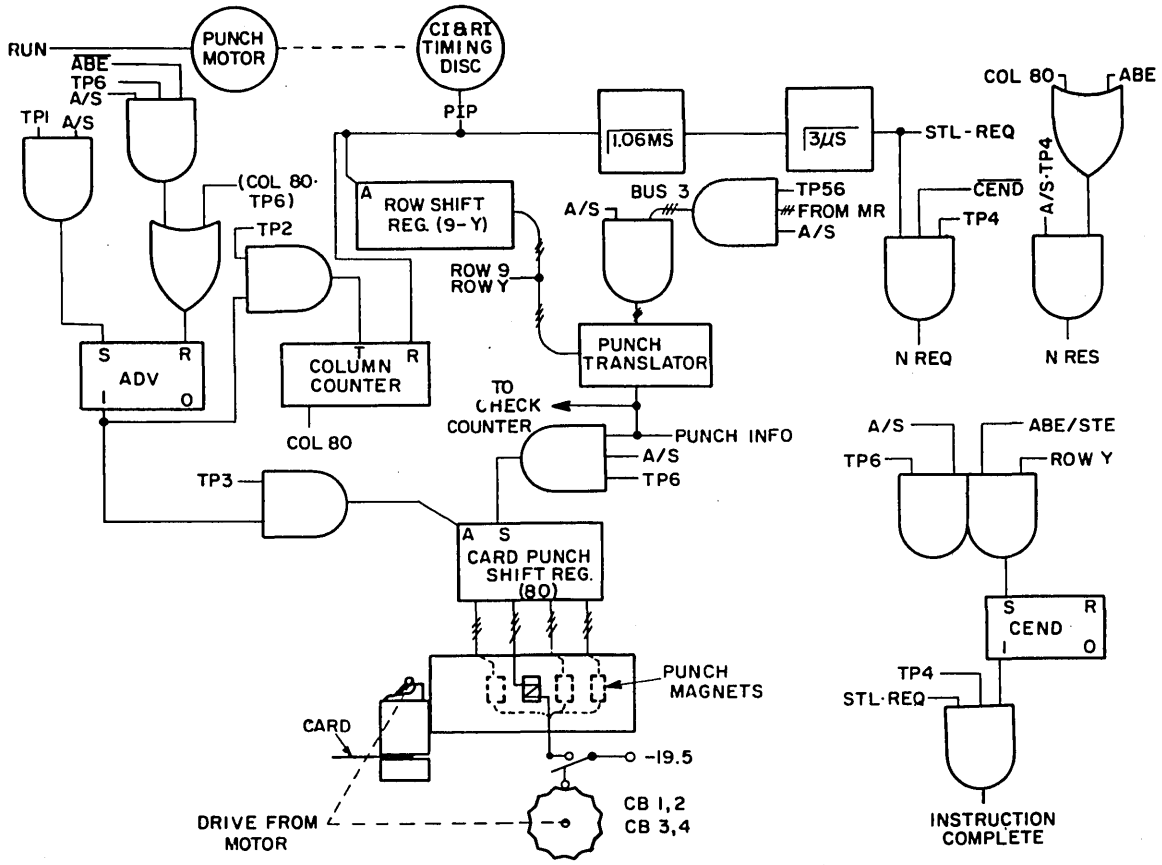


Figure 10-6. 315 Card Punch Control Module

While punching, Punch Index is used to tell the control module what row is going to be punched next, so that the Processor may then prepare the CPSR with information from memory. The CPSR is used to

energize the punch magnets (solenoids) within the unit, to actuate their corresponding interposers. Then, on the downward stroke of the punch bail, holes will be punched in that row.

The Computer prepares the CPSR with one bits by searching the designated area of memory consisting of 80 locations; using a series of A1 status levels. It will first go through an X1 and an X2 status level to store A initial so that it can return to the correct starting point at the beginning of each row on the card. The X2 selects an A1, and depending upon the setting of ABE, 80 A1 status levels may be performed.

These A1 status levels each take a character from memory, in sequential order, and send it through the card punch translator. This translator looks at the row that is going to be punched and compares this to the character. According to the 301 Card code, it will give an output, attempting to set the first stage of the CPSR. An advance pulse will be produced and shift this information over one column. This process will continue for 80 status levels if ABE is not set during the series of status levels. At the end of the 80th A1, a level called Column Count of 80 (CC80) is produced, and causes the Computer to select an X3 status level. The X3 status level will be executed and will select an X4.

The X3 and X4 status levels will take the A initial address, previously stored by X1 and X2, and place it back in the A Register, to again initiate searching memory to prepare the CPSR for punching the next row. This would continue until row Y, the last row on the card, was searched. At the end of the 80 A1 status levels for row Y, no X3 or X4 status levels will be selected. If ABE is set at this time, a P1 status level will be selected, and the instruction is terminated.

If ABE is not set, the Run level will be held up to the Punch so that another card cycle might be accomplished, and another card fed to be punched. An X1 and X2 will be selected and executed, storing A <u>final</u> of the previous card, so that the next 80 locations of memory can be

searched to prepare CPSR to punch information to the rows of the card. This cycle will continue until ABE is reached, as before, upon reaching the 80th A1 during each row.

ABE may be set however, during the series of A1's at row 9, indicating that a full card of information is not to be punched. Then, instead of going through 80 A1's per row, only that number of A1's will be produced which will allow the necessary number of characters (less than 80) to be punched. Then, when ABE is set during Row Y, the instruction can terminate.

When the second card is being punched, the first to be punched will be read-checked. This is accomplished by comparing the number of holes that should have been punched, to the number of holes that has been punched. While the CPSR is being filled, the number of one bits that are produced are counted in a four stage up-counter called Temporary Hole Count (THC) register.

It can be a four stage register, since, even though more holes than 15 are punched, there will be a certain count in the register when the counting for a card is finished. This count will then be placed in a Hold Count Register (HCR) and stored, until a check can be made against the number of holes that have been read-checked.

While the card is being read-checked, the information coming from each row is placed in parallel fashion in an 80 stage shift register. This information is then advanced out, the one bits being counted in a four stage register. This register is called the Check Counter (CKC).

When the entire card has been read, the information in the CKC is compared to the HCR. If they are not equal, Card Compare Error (CCE) is generated, and the Processor and Punch unit are stopped. The card that caused the error will be just beyond the read-check station in the transport mechanism.

Due to the fact that the Card Punch unit will move a card only one card cycle at a time, two dummy instructions are necessary to move

the last card of an instruction (which was just punched) to the read-check station to be checked, and then placed in the output hopper.

Since cards will be fed during these dummy instructions, A should be equal to B initially, and A must be addressing a non-punchable character. A space symbol or underline is a non-punchable character. The punch unit will then be prepared for the next punch instruction.

Detailed Logic for Punching

The Card Punch Busy (CPB) Flip-flop (6305B4) and Card Punch Normal to Simultaneous (CPNS) Flip-flop (6305B3) are shown on Print No. 8617630. During the SIO status level, with a CPN instruction staticized, AND Gate 6305C4 is permissive, and primes AND Gates 6305B2 and 6305B1. Since SOP (N) is not present at TP2, AND Gate 6305B1 will not set CPNS. At TP4, since AND Gate 6305C5 has a low output, the CPB Flip-flop will be set. Setting CPB will then inhibit HK from being produced.

Also, at TP2 of the SIO, AND Gate 6302B3 set Card Advance (CAD) and produced a pulse called Set Row 9 (P). This level is applied to OR Gate 6308D2 to set the Row 9 Flip-flop of the Row Shift Register (6308C2). This register consists of 12 shift flip-flops primed for zeros, and produces Row Levels 9 through Y to tell the control module what row of the card is being punched.

At TP3 after CAD is set, AND Gate 6302A3 sets the Run flip-flop; then, at TP4 of SIO, with CPB set, a Run level is sent to the Card Punch unit to energize K104 and start the mechanism in motion.

Also after SIO, AND Gate 6302D1 checks for the Card Punch unit being operable at TP1. If not, Device Doesn't Follow (DDF) becomes set, and resets CAD at TP6.

The SIO status level selects an X1 status level. P-NRQ was not reset, therefore an X1, an X2 and 80 A1 status levels are performed. (On the first card punched, it will be assumed that ABE is not set, indicating that more than one card must be punched).

X1 and X2 store the contents of the A Register in location 0202-0205, so that this initial A Address might be returned to search memory for the next row.

The A1 status level will then prime AND Gate 6315A1. At TP1, Advance (ADV) will become set. This flip-flop is used to develop an Advance pulse to trigger up the Column Counter (COL 2^0-2^6) (6306C1), and to produce an Advance pulse for the CPSR.

The COL register is an up-counter which is used to count up to 80 A1 status levels, since 80 A1's are necessary to completely fill a row of a card with 80 characters. When COL 80 is produced by setting the COL 80 Flip-flop in area C-3, Print No. 8617630, this will indicate that the CPSR is filled with 80 bits of information so that a row may then be punched. This causes an X3 status level to be selected. The COL is triggered up by AND Gate 6306D2 when ADV is set at TP2.

The CPSR (6314D2) is an 80 stage shift register used to store the information to be punched in a given row. When the register is full, the stages of the register send their outputs over lines (80) so that the punch solenoids may be energized if there is a one bit in a corresponding stage of CPSR. CPSR is primed for zeros. CPSR is advanced every TP3 when ADV is set. When the first Advance pulse is produced, there will be no information in CPSR, but this has no detrimental effect.

AND Gate 6316D3 is used to set the first stage of CPSR and to trigger up THC if Punch Info (N) comes from the translator on Print No. 8617632.

The translator consists simply of a series of AND gates fed from Bus 3, with a Row level as the second prime input. The translator works simply by checking the bits of the character placed on Bus 3 by the A1 status level, and depending upon what row is going to be punched next, developing an output from AND Gate 6325A1 called Punch Info (N). AND Gate 6326B3 will inhibit an underline from producing Punch Info (N), since it is an un-punchable character. In that case, a blank column will be left on the card.

As an example, assume that at TP456, the A1 places an I (0011001) on Bus 3. If row 9 is going to be punched, AND Gate 6327B1 will have a high output. Since AND Gate 6326B3 is not fully primed, AND Gate 6325A1 will produce Punch Info (N) to set the stage of CPSR and to trigger up THC. When row Y is just ready to be punched, because the I has a 2^4 bit, a punch will be placed in Row Y in the corresponding column.

Parity of the character being translated is checked at TP5 of A1 by AND Gate 6322B2. If bad parity exists, a Write Error (WE) will be generated.

ADV (6315A3) is reset every TP6 of A1 by AND Gate 6315A2 if ABE is not set, so that no Advance pulses will be produced after the 80th A1, and during a Normal Mode status level when operating the card punch simultaneously. ABE is used to inhibit resetting ADV through AND Gate 6315A2, so that advance pulses may be produced to shift the bits in the shift register into their correct columns, since when ABE is set, 80 A1's are not produced. Under these conditions when COL 80 is produced, AND Gate 6314A1 will reset ADV at TP6. This will allow 80 Advance pulses to be produced at all times.

When COL 80 is produced at the end of searching memory to fill CPSR, because of primes from AND Gate 6307C3, the last A1 will come through AND Gate 6308B2 and prime AND Gate 6308B5. Then, since COL 80 is set, N-RES will be produced to reset P-NRQ at TP4. This will halt normal status levels until P-NRQ becomes set by N-REQ. Punching of the first row can now occur, since CPSR is filled with bits, and is energizing corresponding magnets in the Punch unit.

Then, at index point 9.4, when the punch bail is on it's downward movement, a Punch Index Pulse (PIP) will be received by the control module (AND Gate 6318C6). PIP (P) must go low before AND Gate 6318C6 will give a high out. When PIP (P) disappears, the low that will then exist fires One Shot 6318C2, 8C5. A three microsecond pulse delayed one millisecond from the disappearance of PIP (P) is generated by

6318C5. AND Gate 6318C6 will then produce a three microsecond high called ADV-Row (N) through Inverter 6318C7. This level sets the Pre-Check (P-CK) (6318B1) Flip-flop, and is used on Print No. 8617630 to advance the Row Shift Register and to reset the Column Counter through Inverters 6308C3 and 6307C1. When the Row Shift Register is advanced, row 8 will then be produced. With P-CK set, Check (CK) is set at TP6 through AND Gate 6318B2.

AND Gate 6318C6 fires One Shot 6317C1, 7C2 which resets P-CK one millisecond after it was set, so that AND Gate 6318B3 can reset CK at TP2. During the one millisecond delay, CK primes AND Gates 6313D1 and 6313C3. AND Gate 6313D1 produces an advance pulse at TP5 for CKSR, so that information will be shifted out to AND Gate 6313C3. At the next TP3, AND Gate 6313C3 will produce a trigger pulse to trigger up CKC. In this manner the holes that have been read in row 9 of the previously punched card are counted. The CKSR will require 79 advance pulses (80 minus 1), since the first stage initially has an output to trigger up CKC through AND Gate 6313C3. More advance pulses will be produced than are necessary during the one millisecond that CK is set, but this has no effect since CKSR is primed for zeros.

When the output on pin 24 of 6317C2 goes high again, it will fire 6316C1, which is a 60 microsecond delay to firing 6316C2. This One Shot produces a three microsecond output called STL-REQ (N). This level is applied to AND Gate 6306B1 to produce a N-REQ through 6307A3 as long as Card End (CEND) (6316B3) is not set. This will be set only when the instruction has been completed.

N-REQ will set P-NRQ, allowing the execution of the X3 and X4 and 80 A1 status levels. The X3 and X4 status levels will be used to read the initial A Address from memory, and place it in the A Register. The A1 status levels would perform the same function for row 8 that they did for row 9, i.e., taking a character from memory, comparing it to the row, and determining whether Punch Info should be generated for the character.

This cycle will then continue for all rows of the card, until row Y is being punched. When row Y is present in the control module, AND Gate 6317B1 will generate a pulse output every TP6 of an A1. The first A1 of row Y will set Card Almost Complete (CAC) (6317B3), and prime AND Gate 6316B1 through Inverter 6317C4. AND Gate 6316B1 is used only when actually terminating the instruction, whereas CAC is used when terminating punching to a card.

When the PIP (P) of row Y disappears, P-CK is again set, to go through the routine of triggering up CKC. One millisecond later, 6317C2 resets P-CK and will be used to set Pre-Compare (P-COMP) (6317B6) through AND Gate 6317B4 since CAC is set. Since P-COMP is now set, Compare (COMP) (6317A3) will be set through AND Gate 6317A1 at TP0.

COMP being set is used to compare the information in the HCR from the previous card, with CKC information. This is done by AND Gate 6312B3. With COMP set at TP1, and with Brush Card Presence (BCP), if any of the gates feeding Inverter 6313B3 has a high out, AND Gate 6312B3 will set Card Compare Error (CCE) (6312B4). This error will halt the Processor and stop the Punch unit so that no more cards are fed or punched.

TP2·COMP is used to reset the Column Counter via AND Gate 6307D2 (the search of memory using 80 A1's has been completed for row Y), and the Row Shift Register. Gate 6314C7 is used to reset the HCR and CKC at TP3. TP4 is used to gate the count in THC into the HCR and to set the Row 9 Flip-flop of the Row Shift Register through AND Gate 6314D1.

TP2 had reset CAC through AND Gate 6317B2. TP3 had then reset P-COMP through AND Gate 6317B5, and TP6 will reset COMP.

At this time the control module is now ready to punch the second card, since COMP was used to set things up. The Run level will continue to hold up, allowing the feed solenoid to be energized for the second card cycle, feeding a second card and allowing a second card cycle to be performed. The card just punched will now be beneath the read-check station ready to be checked while the second card is being punched.

Sixty microseconds after P-COMP is set, STL-REQ is generated by 6316C2. STL-REQ will generate N-REQ to set P-NRQ, and since the last A1 produced for row Y of the first card selected X1, an X1 and X2 are executed. These status levels will store A initial plus 80 of the first card, since a new portion of memory is to be searched for the second card. The incremented A Address of the previous instruction is left in the A Register for use of row 9 of the second card.

It will be assumed that ABE will be set during punching of the second card, and the second card will be the last card punched. The instruction will be terminated on punching the second card and checking the first.

The X2 status level selected an A1, and then a series of A1's are performed. Assume that a total of 100 characters were to be punched, 80 to the first card, and 20 to the second. Because of this, only 20 A1 status levels will be needed to fill CPSR for each row.

Each A1 for row 9 will set ADV, therefore, COL will count up, and advance pulses will be produced for CPSR. ABE will be set during the 20th A1 of each row, and this will cause that status level to select an X3. N-RES will be produced at TP4, since OR Gate 6308B3 has ABE applied to it, as well as COL 80. ABE will then take the place of COL 80 in selecting and requesting status levels.

ABE is used on AND Gate 6315A2 so that ADV will remain set after the last A1 is produced for each row, since enough advance pulses must be produced to shift the information bits in CPSR into the correct columns. ABE inhibits AND Gate 6315A2 from resetting ADV on the last A1, and ADV will remain set until COL 80 is produced (ADV is still triggering COL). AND Gate 6314A1 is then used to reset ADV. Thus, the required 80 advance pulses are produced for CPSR.

Punching for the second card will perform in the same manner as for the first card. The only difference being that only 20 A1's will be produced for each row. At Row 8, however, when ABE becomes set again

(ABE becomes set at TP1 of A1, and reset at TP6 of X4) Gate 6302B3 will reset CAD so that, with Card Index, AND Gate 6302A4 will reset RUN, removing the Run level from the Punch unit. The Punch unit will continue to run for a full card cycle, however, since P2 (Start Hold) will keep the punch motor running. Since the Run level has dropped out, no more card cycles can be performed.

The unit will continue punching and read-checking simultaneously until row Y is reached. The 20th A1 status level will prime AND Gate 6316B1 through AND Gate 6317B1. When ABE is set at TP1, CEND will be set, indicating that the instruction is about to terminate.

When COMP is set, read-checking will take place and the count in HCR is again compared to the count in CKC, thus the first card punched will be checked. The Brush Card Presence signal on 6312B3 will indicate that the card is under the Read-Check station and thus, may be checked.

Finally, when the last STL-REQ is generated, Pre-Instruction Complete (POIC) (6316A1) will be set by AND Gate 6316B4. Then, at the next TP3, AND Gate 6316A2 will set Instruction Complete (IC). At TP4, AND Gate 6316A4 will produce Instruction Complete.

INST-COMP (P) is used to produce N-REQ through OR Gate 6307A1 and CPB is reset at the next TP0 by AND Gate 6304B1. The instruction has then terminated and 100 characters have been punched on two cards with one instruction.

In order to read-check the second card punched, a "dummy instruction" must be performed. This will place the first card in the stacker pocket and allow the second card to pass beneath the read-check station. A second "dummy instruction" will then be used to place the second card in the output hopper.

GANG PUNCH MODE

The Gang Punch Mode in the 334 Card Punch is a special mode of operation which enables the service technician to test all the logic and mechanics of the Card Punch for any malfunction.

Basically, this mode of operation allows the Card Punch Unit to punch any number of duplicates of an initially punched card, without requireing any processor control. The initially punched card will usually have a special test pattern punched into it, to enable quick detection of poor registration, and picking up or dropping of holes in a card. Unit timing, as well as punch and read-check station operation, is checked.

The duplicate cards are punched by the information from the read-check station brushes being sent to the punch magnets as punch information. Any card under the read-check station will cause a duplicate of itself to be punched, one card-cycle behind the reading of the card. The technician may then observe the duplicate cards to determine what error, if any, has occurred.

OPERATIONAL SET-UP

In order to allow the machine to operate in this mode, a few simple cable changes must be performed.

Referring to unit Print No. 8616544 (503), the cabling from J106, J107, J108 and J109 must be disconnected from the Processor at the Punch Unit. Two special jumper cables should then be connected from J106 to J108 and J107 to J109. On Print 8616544, Area D-3, the Brush Info signals will then be used as Punch Info signals in Area C-6.

Area B-5 shows that the jumper from J107 to J109 will also serve to ground pin 21 of relay K106, the service relay, to enable the relay to become energized when power is applied. K106 will have the function of providing a simulated run command for the unit, allowing the Brush Read station to be strobed only when there is a card under the station

and causing CB5 and CB6 contacts to be connected in parallel in order to provide a longer read strobing pulse.

K106 contacts 3, 4, 5 (Area B-7) remove the possibility of a Run Command from the Processor from having any effect and allow a Run Command to be developed only when K102 contacts 4-5 (C-4) are closed. K102 will become energized when an initially punched card is placed at the bottom of the input hopper, unpunched cards are placed on top of it, and the Start Button is depressed by the technician. As soon as the first card is fed into position before the punch station, the Die Card Lever will be actuated, thus energizing K102, which will provide a continuous run command.

No Punch Information must be developed by the read-check station until a card is actually under the station. K106 contacts 11-12 (D-8) remove the normal strobe voltage from CB5 and CB6 and K106 contacts 13-14-15 (C-5) cause -48 volts to be sent through Brush Card Lever contacts (C-4) and K106, 7-8 (C-3) to be used as a strobe voltage only when a card is actually under the read-check station. This prevents the initially punched card from being punched when it is under the punch station.

K106 contacts 16-17-18, 19-20 (C-8) cause CB5 and CB6 to be placed in parallel to provide a longer strobe pulse to allow enough time to energize the punch magnets.

After start is depressed, the machine will continue to run through card cycles until the technician wishes to stop the machine. This may be done by depressing the Operable Button, SDS204, Area A-5. This will cause relay K107 to operate and its contacts 1-2 (Area B-7) will cause the Run Level to be dropped, thus stopping the machine at the end of that card cycle. The machine may be re-started by depressing the Start Button.

The value of using the Gang Punch Mode is that the entire Punch Unit may be checked, without using Processor time, to determine whether a fault exists in the control module or Card Punch itself.

LOGIC PRINT REFERENCES

Section 7 - Anelex Printer

Control Logic	
3506016	3506020
3506018	3506023
3506019	

Section 8 - Record File

Control Logic	Machine Logic
8617638	8619000
8617639	8619001
8617640	8619002
8617641	8619003
8617642	8619004
	8619005
	8619006
	8619007
	8619008

Section 9 - Card Reader

Control Logic	Machine Logic
3506035	8619091
3506036	8619092
3506037	8619093
3506038	
3506039	

Section 10 - Card Punch

Control Logic	Machine Logic
8617630	8616544
8617631	8616545
8617632	