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Graphic 7™

COMPUTER GRAPHICS DISPLAY SYSTEM

MODEL 5743 RAMP/CONIC GENERATOR TECHNICAL MANUAL

Information Products Division
Federal Systems Group
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SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

This maual describes the Mode 5743 Ramp/Conic Generator circuit card assembly, an optional device used to draw on-axis ellipses (from straight lines to circles) and to reposition the CRT beam as desired in the Sanders Associates, Inc. GRAPHIC 7 Computer Graphic Display System. The manual provides descriptive information installation, operation description, and maintenance information to aid in using and maintaing this card assembly.

1.2 EQUIPMENT DESCRIPTION

1.2.1 PHYSICAL DESCRIPTION

The ramp/conic generator circuit card is a 7.75-inch high by 12-inch long assembly, outfitted iwth a 98-pin plug that matches the 98-pin XA1A13 connector in the GRAPHIC 7 terminal controller. The card contains integrated-circuit microelectronic devices and discrete components connected as an operation circuit that interacts with other cards in the terminal controller to control the timing, pattern, and intensity of line vectors distributed to the connected displays.

1.2.2 FUNCTION DESCRIPTION

The ramp/conic generator card is an optional replacement for the ramp generator card supplied as the nominal XA1A13 card for the system. It operates with the two D/A converter cards, also located in the terminal controller unit, to sonstitute the vector position generator circuit. The ramp/conic generator card performs all functions of the original ramp generator and provides additional capabilities with respect to the generation of curved line vectors, representing ellipses or 90-degree segments thereof.

The ramp/conic generator responds to vector displacement values provided by the associated D/A converter cards, together with programmed selection signals from the graphic controller card, to produce X-axis and Y-axis ramp drive signals to the D/A converter cards and a Z-axis intensity signal to the otuptu channel card. In response to the various control inptus, the circuit can produce blanked or unblanked Z-axis outputs, drawing line vectors in one of four selectable patterns (solid, dotted, dashed, or centerline) at either of two speeds. The nominal ramp drive

outputs to the associated D/A converter cards are identical linear-ramp signals alternating from zero volts to +5V or the reverse in a displacement-associated time interval that determines the length of the line vector to the drawn. Short-vector ramp-drive signals (for vectors involving less than 1/32 display screen displacement) are produced as constant length ramps, however, with the Z-axis output being attenuated correspondingly to maintain a uniform display intensity.

Upon program command, in either case, the two ramp-drive outputs are generated as conic functions, with the Z-axis output being developed as the consine value of the true linear ramp signal and the Y-axis output being developed as the sine value. The resultant ellipsis pattern may be centered at any addressable location on or off the CRT screen and is oriented so that its major axis are parallel to the X and Y axes of the display indicator. The lengths of these axis are determined by instructions that specify semimajor and semiminor axis lengths for each ellipse, with each axis length being independently programmable from zero to half-screen values.

Part Number 1086939G1 is the standard ramp/conic generator. The G2 condition is a variant that operates at slower speed, intended for use in installations that have a Kratos display indicator.

SECTION 2

OPERATION

2.1 GENERAL

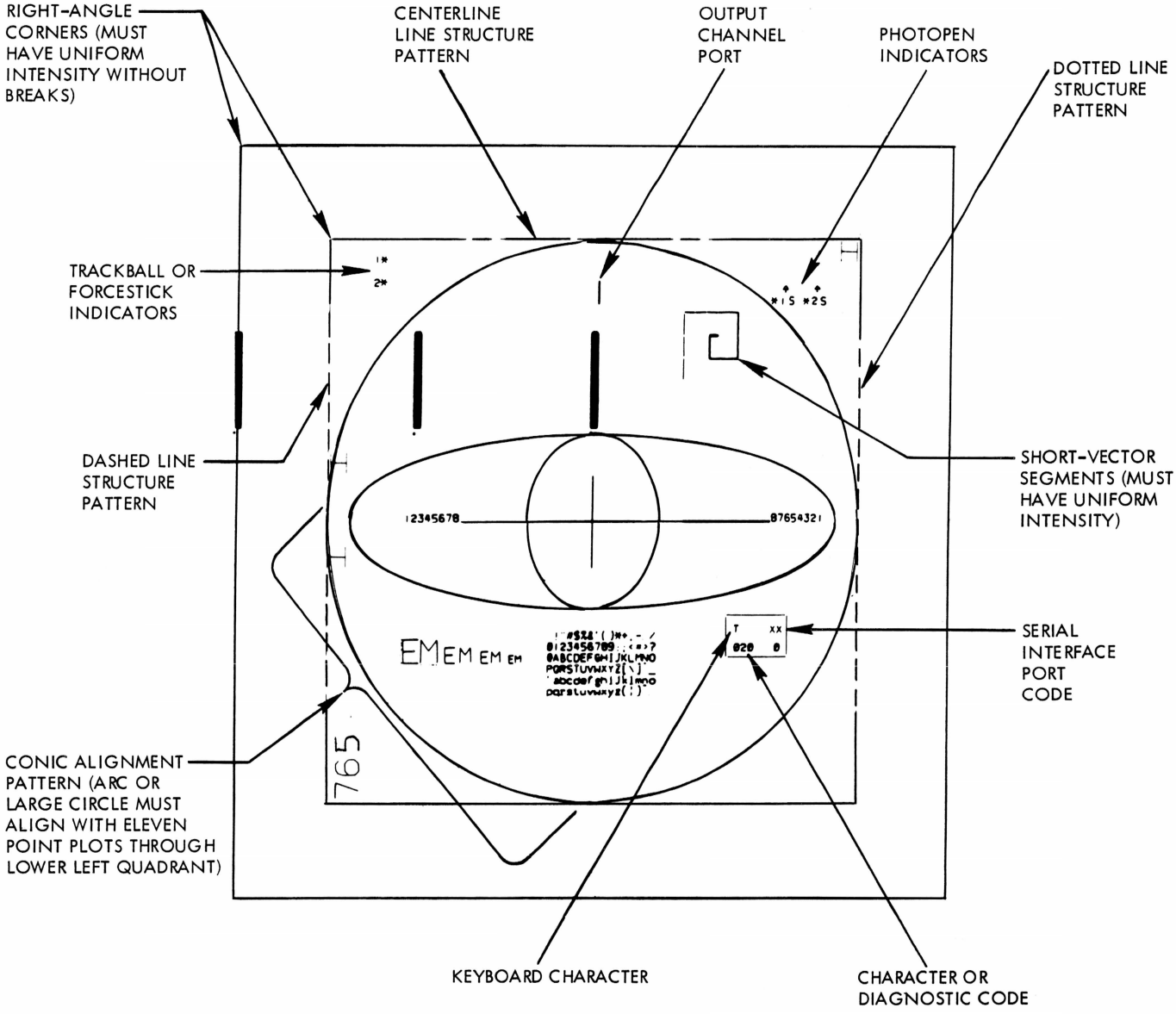
The ramp/conic generator circuit card assembly, in conjunction with the X-axis and Y-axis D/A converter cards and the graphic controller card, generates blanked move-displacement and unblanked line vector display axis position/drive commands to the D/A converter cards. No operator control or manipulation of these signals is provided. The circuit card is controlled by vector-displacement calculation results (the differential values between the existing display-axis positions and the new-position coordinates to which the display axes have been assigned) and software-generated mode/pattern control signals from the graphic controller card.

Operating mode is established by a 2-bit code made up of the VPS1+G and VPS2+G outputs from the graphic controller card in conjunction with an active VPST-G signal. Additional control inputs include the STKX-G signal, which switches the card from ramp mode to conic mode, a program-specified speed selection code established by data bits DB09-G and DB10-G, a program-specified line-structure selection established by data bits DB03-G and DB04-G, and the OFLW-A output from the D/A converter cards, which blanks any vectors proceding beyond the limits of the display area. In general, the designated selection signals are produced as applicable outputs from the graphic controller card in response to different kinds of program move and draw instructions. For details pertaining to the development and significance of these signals, refer to the GRAPHIC 7 Programmer's Reference Manual, GA-77-419, published by Sanders Associates, Inc.

2.2 OPERATOR CHECKOUT PROCEDURE

To determine proper operation of the ramp/conic generator card, ensure that the card is correctly mounted in the XA1A13 card slot in the terminal controller assembly, with the GRAPHIC 7 system fully energized. Press the LOCAL pushbutton switch on the terminal controller to display the verification test pattern. Confirm that the displayed pattern corresponds with the preprogrammed pattern configuration shown in figure 2-1, particularly with respect to the following relationships:

a. The corners of the displayed squares should be clearly defined right angles, with a uniform intensity through the points of congruence in all four corners.



NOTE

This figure illustrates the verification test pattern that is generated when the conic generator option is installed in the terminal controller. If a conic generator card is not installed, each circle and ellipse will be displayed as four straight lines.

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Figure 2-1. Verification Test Pattern

b. The central portions of the sides of the inner square should represent different line-structure patterns--respectively solid (bottom), dotted (right), dashed (left), and centerline (top).

c. The large outer circle should be a symmetric circle, with the arc of the lower left-hand quadrant aligned with the ten point plots marking off 10^{o} increments from 180^{o} (center left-hand edge) to 270^{o} (center bottom edge) and the intermediate 225^{o} point.

d. The short-vector segments making up the broken pattern in the middle of the upper right-hand quadrant must present a uniform intensity.

If the verification test pattern fails to comply with any one or more of these requirements, perform the alignment procedure of Section 5 to establish correct operating conditions.

SECTION 3

THEORY OF OPERATION

3.1 GENERAL

This section describes the functional operation of the Model 5743 Ramp/Conic Generator circuit card assembly. Figure 3-1 is a simplified block diagram for the circuit; paragraph 3.2 provides a basic functional operation discussion, keyed to that figure. Figure 3-3 is a detailed functional block diagram; paragraph 3.3 provides a detailed functional operation describing the interrelationships between the various circuit components defined in that figure.

3.2 BASIC FUNCTIONAL OPERATION

Figure 3-1, located at the end of this paragraph discussion, shows the basic functional blocks of the ramp/conic generator circuit card and indicates the relationship of these blocks with each other and with associated circuits in the system. These blocks and their basic functions are as follows:

a. Toggle Flip-flop. The toggle flip-flop is a complementary flip-flop that is cleared by an active VPIZ-G (Vector Position Initialize) pulse and subsequently alternates between set and reset states in response to successive VPST-G (Vector Position Start) pulses from the graphic controller card. The state of this flip-flop at any given time determines the incremental polarity of a ramp timing signal to be developed by the ramp generation logic.

b. Ramp Generation Logic. The ramp generation logic responds to each change in state of the toggle flip-flop output signal by generating a linearly incremented/decremented RAMP timing signal that either rises from zero volts to +5V (if TOGGLE signal is high) or declines from +5V to zero volts (if TOGGLE signal is low). The speed at which this RAMP voltage changes from one limit to the other is determined by three factors:

1. A normal/fast command ($\overline{\text{FAST}}$) generated by the mode control logic in response to the vector function selection code given by the concurrent VPS1+G and VPS2+G inputs (fast for blanked position moves and point plots, normal for unblanked vectors).

2. A move/vector command ($\overline{\text{VROM}}$), also generated by the mode control logic in response to the VPS1+G and VPS2+G signals (faster for move instructions, slower for vector instructions).

3. Length of vector to be drawn (constant 1.25-microsecond rate for vectors of less than 1/32 full-screen deflection; proportionally scaled at approximately 3.3 microseconds per inch of vector displacement for all longer unblanked vectors).

The ramp generation logic circuit also produces a ramp-inprocess timing code: one of two outputs (ACLP-or BCLP-) is active when the alternate-state RAMP signal is at one of its two limits; both are inactive when the RAMP signal is moving from one limit to the other. This condition code is used by other circuits on the card to enable or inhibit related timing functions. In addition, these two signals also produce an active OVCK-E (Overflow Interrupt Clock) signal during the same inprocess ramp-development period. This output is used to clock the status of the OVFW-A (Overflow) output from the D/A converters into a program interrupt register circuit on the ROM and status card, thereby informing the program whenever either D/A converter card reports that the latest-loaded instruction calls for a vector displacement to some point outside the programmable area of the display.

c. X/Y Ramps Control Logic. The W/Y ramps control logic develops independent X-axis (RMPX+E) and Y-axis (RMPY+E) ramp voltages, respectively sent to the X-axis and Y-axis D/A converter cards. The receipt of an active VPS2+G signal sets this circuit to its ramp-mode function, meaning that both ramp-voltage outputs are derived from the common RAMP output from the ramp generation logic. In the case of a DRKY (Draw Conic) instruction, however, a subsequent STKX-G (Start Conic) pulse sets the ramps control logic to its conic-mode function before the associated VPST-G pulse triggers the toggle flip-flop to initiate a new ramp-development period. In this case, the RAMP output from the ramp generation logic is first split through respective cosine-function and sine-function networks that develop appropriate amplitude relationships for production of curved display vectors.

d. Z-axis Control Logic. The Z-axis control logic produces the VECZ+E drive voltage, which controls the presence and intensity of the display vector defined by the associated X-axis and Y-axis drive voltages. This circuit decodes mode select bits from the graphic controller card to determine whether a display vector is to be drawn and decodes the ramp-limit signals from the ramp control logic to determine when the display vector, if so, is being drawn. When the result is a short vector (less than 1/32 full screen), a common wire-ORed output from the ramp timing logic attenuates the VECZ+E output to ensure a consistent display intensity. When the display vector is to be other than a solid line, the associated line structure control logic blanks and unblanks the VECZ+G output as necessary to produce the requested line structure pattern (dotted, dashed, or centerline), as explained below.

f. Mode Control Logic. The mode control logic decode two mode select signals from the graphic controller circuit to generate appropriate enabling conditions for other circuits on the card. The decoding also monitors the common OFLW-A overflow signal from either D/A converter card, together with the six most-significant Y-axis position bits. The resultant outputs determine whether the ramp generation logic produces a vector-draw ramp or a position-move ramp, whether that ramp is calculated

at fast speed or at normal speed, whether the ramp timing logic can activate the function-busy signal, and whether the Z-axis control logic can unblank for a vector output.

g. Line Structure Control Logic. The line structure control logic completes the unblank-enable condition for the Z-axis control logic when line vectors are being drawn. This circuit becomes enabled whenever an active BUSY output from the operation timing logic indicates that a valid ramp timing signal is in process. The line structure control logic decodes data bit signals passed on the DB03-G and DB04-G lines during an active STDZ-G pulse interval to determine whether the vector line should be solid, dotted, dashed, or centerline (alternate long and short dashes). The resultant output is an unblank-enable signal that causes the Z-axis control logic to activate the VECZ+E display drive signal when active. The active duration of this unblank-enable signal is established by the decoding circuitry such that the resultant pattern produces the desired line structure.

h. Line Vector Speed Control Logic. The line vector speed control logic selects one of two clock rates for the just described line structure control logic when the Z-axis control logic activates a clock-enable gating signal. The faster speed is established by a self-triggering oscillator. This speed is used for displaying graphic presentations on a display screen or high-speed printers. The slower speed, obtained by dividing the oscillator output by 16, normally is used for driving a connected hard-copy device with limited speed capability. The speed selections are determined by a data-bit selection code passed on the DB09-G and DB10-G lines at the time of a low-going STDP-G pulse from the graphic controller circuit.

3.3 DETAILED FUNCTIONAL OPERATION

Figure 3-3, located at the end of this paragraph discussion, is a detailed block diagram of the ramp/conic generator circuit card assembly, showing the functional components of the various logic circuits on that card. The following discussion is keyed to that diagram, following the same order of presentation used in the preceding basic operation discussion. For full circuit details, refer to the engineering logic diagram, 1086941, located in Section 6.

3.3.1 TOGGLE FLIP-FLOP CIRCUIT

Toggle flip-flop U17B acts as a circuit turn-on switch. The flip-flop initially is cleared by activation of the programmable VPIZ-G display-initialization output from the graphic controller card. The trailing edge of each subsequent occurrence of a VPST-G pulse clocks this complementary flip-flop, causing it to alternate from one logic state to the other. When the toggle flip-flop is reset, it presents a low-level TOGGLE signal to the constant-current generator subcircuit in the ramp generation logic as the output from inverter U39B. This low-level initialization condition causes that constant-current generator to operate such that capacitor C9 becomes completely discharged (or remains discharged, if initially in that state), producing a nominal 0V output from the following buffer driver as the low-limit RAMP signal to the X/Y ramps control logic.

The next-following VPST-G signal, registering the start of a programmed display operation, clocks the toggle flip-flop to its set state. This condition causes the constant current generator to switch polarity, charging capacitor C9 until the RAMP buffer driver produces a nominal +5V output, clamped by an associated limiter circuit. Similarly, the next-following VPST-G signal returns these conditions to the initial state. The RAMP signal thus is produced as a continuing linear alternation between 0V and +5V, with each such excursion beginning with each successive alternation of the toggle flip-flop as the result of a new display instruction from the operating program. Since the charging current is constant in either case, the integrated charging slope of the RAMP output signal is linear.

The toggle flip-flop also produces the TOGL-E card output as the output from inverter U24B. This TOGL-E output is low while the flip-flop is set (charging ramp), high while the flip-flop is reset (discharging ramp). The TOGL-E signal connects as a conditioning input to the graphic controller card and to both of the X-axis and Y-axis D/A converter cards. On the latter cards, this initially inactive signal (in conjunction with the inactive VPBY+E output from the operation timing logic circuit on this same card) sets up the A-position storage multiplexers on each D/A converter card to accept new position data inputs upon receipt of an active STDX-G/STDY-G timing pulse. (The program presents the new position data inputs and then activates the STDX-G/STDY-G pulse, as applicable, prior to starting the first RAMP-signal cycle.)

When the program activates a VPST-G pulse to start a ramp-generation cycle, the toggle flip-flop becomes set, activating the TOGL-E output. This condition sets up the B-position storage register on both D/A converter cards to become clocked by an active VPNL+E pulse, that signal is produced as an output from the ramp timing logic circuit at the end of the ramp generation period, as described later in the discussion of that circuit.

The two state-value outputs from the toggle flip-flop also connect as conditioning inputs to the operation timing logic. These signals let that circuit establish timing (start of move and end of move) for blanked position-move ramp cycles, passing these timing conditions to the D/A converters, as will be described.

3.3.2 RAMP GENERATION LOGIC

The ramp generation logic includes a vector length calculator, a charge rate calculator, and a ramp generator. The following paragraphs discuss each of these subcircuits in detail.

3.3.2.1 Vector Length Calculator. The vector length calculator computes the displacement distance between the beginning of the vector operation about to be performed and its end location. The actual vector length is the hypotenuse of a triangle having the X-axis displacement as one side and the Y-axis displacement as the other side. The circuit approximates this value by computing the sum of the larger displacement and half of the smaller displacement.

The inputs to this circuit are the binary bits representing the displacement distances between the end of the last vector, as defined by the old position data stored in the X-axis and Y-axis D/A converters, and the end of the new vector, as defined by the new position data just loaded into those cards by the last load

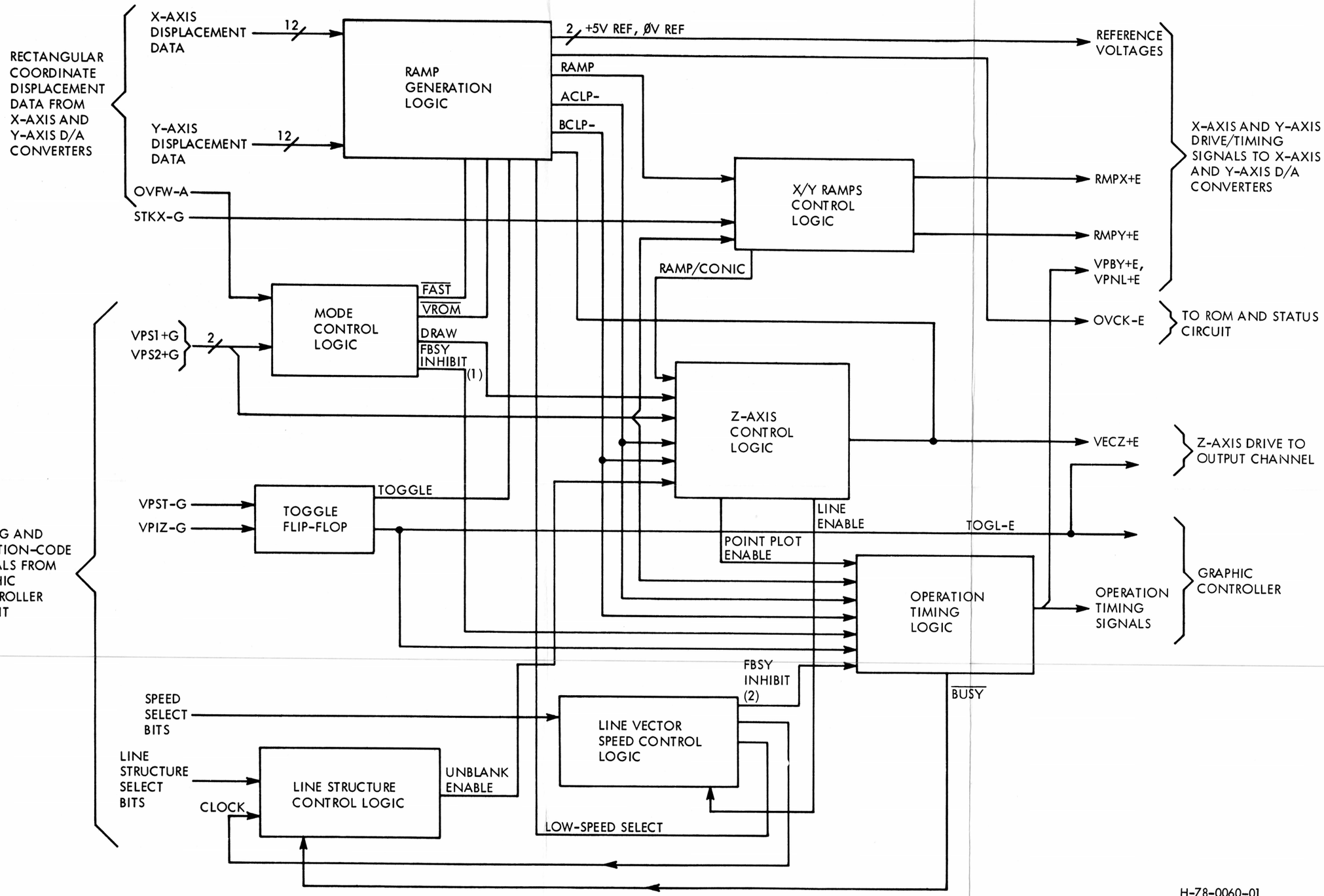

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Figure 3-1. Simplified Block Diagram of Ramp/Conic Generator Circuit Card Assembly (A1A13)

instruction. The X-axis displacement is given by bits LX00+A through LX10+A from X-axis D/A converter card A1A14; the Y-axis displacement is given by bits LY00+A through LY10+A from Y-axis D/A converter A1A15.

These inputs are applied to one of two adders, in combination with the CARX+A carry value from the position storage register on the X-axis D/A converter. This combination makes the adder produce the sum of the full X-axis displacement and half of the Y-axis displacement as a 12-bit binary range value, RX00+ through RX11+. The same inputs also are applied to the other adder, in combination with the CARY+A carry value from the storage register on the Y-axis D/A converter card. This combination makes that adder produce the sum of the full Y-axis displacement and half the X-axis displacement as a different 12-bit binary range value, RY00+ through R11+.

Finally, the same displacement inputs also are applied to a comparator to obtain an output that is high when the X-axis displacement is the larger value. This signal is the steering control for a multiplexer that receives the outputs from both adders. The multiplexer output, RV00- through RV11-, thus represents the correct vector range length approximation, R, for the given displacement combination in accordance with the algorithm:

R = larger deviation + 1/2 smaller deviation

The 12-bit code of this result is larger than actually required in order to provide for full-range diagonal deflections. Bits RV00- through RV09- provide for full-screen on-axis displacement in either horizontal or vertical dimensions through the 1024-by-1024-increment area of the viewing field on the GRAPHIC 7 display screen. Bit RV10- provides the additional length needed to provide for full-scale on-axis vector displacement through a 2048-by-2048-increment area surrounding the actual viewing field. Finally, bit RV11- provides the additional length needed to provide for diagonal displacement through that same full-range distance. The extended range capability also provides for more accurate angular resolution for long-radius arcs.

Note that the programmable area is twice as large as the displayable area. Vectors can be plotted into and in the programmable area but cannot be displayed outside of the displayable area. In an attempt to resolve the inherent confusion, this manual uses the phrase "full-screen" to designate displacement across the displayable viewing area and uses the phrase "full-scale" to designate displacement across the actual programmable area.

3.3.2.2 Charge Rate Calculator. The charge rate calculator establishes the charge rate for the ramp generator circuit, selecting the rate as a function of the vector length range value established by the vector length calculator. This circuit incorporates a short vector detector, a long vector length switch, a vector charge rate read-only memory (ROM), a position-move charge rate ROM, and a short vector intensity control circuit, consisting of buffer gates and a resistor ladder network. This calculator circuit has three different modes of operation, depending on whether the calculated vector length is (1) less than 1/32 of a full-screen deflection, (2) 1/32 full-screen length or longer, or (3) a move-only displacement (with the Z-axis drive signal blanked by related circuitry).

3.3.2.2.1 Constant Time Mode. When any of the 31 display vector lengths of less than 1/32 full-screen deflection is to be drawn, all medium/long-vector inputs RV05- through RV11- are inactive. Under these conditions, the short vector detector passes a high-level attenuation enable signal to the buffer inverter gates in the short vector intensity control circuit. This input enables those gates to decode the vector length value carried by vector length calculator outputs RV02- through RV05-. The most-significant value, RV05-, has a length value of 1/32 full-screen length and thus must be inactive at this time. Therefore, the output from the buffer inverter gates circuit represents one of eight coding possibilities, as determined by the three most significant bits of the short-length vector value. These outputs control the resistor ladder network to attenuate the VECZ+E output from the Z-axis control logic circuit as appropriate for the length of the short vector. The control operates such that the Z-axis drive voltage decrease proportionally with short-vector length. This change then proportionally attenuates display intensity for the shorter vectors in order to maintain a consistent level of brightness to the human eye.

The vector charge rate ROM produces a 12-bit output, IØ- through I11-. This 12-bit word is a control selection applied to a constant current generator in the ramp generator circuit. For any of the 32 incremental lengths covered by the short-vector intensity control circuit, all 12 bits are low, causing the constant current generator to produce a fairly rapid ramp excursion, taking approximately 1.25 microseconds. This common charge rate constitutes a constant-time mode of operation, used for all short vectors regardless of actual length.

3.3.2.2.2 Vector Constant Velocity Mode. When any of the other vector possibilities (1/32 full-screen deflection or longer) is to be drawn, the enabling output from the short vector detector to the short vector intensity control circuit is inactive. This condition disables the buffer inverter gates in that latter circuit, producing a resistor ladder network output that maintains a maximum steady-state Z-axis drive intensity when that signal is active. A different output from the short vector detector serves as a high/low select signal for the long vector length switch and the vector charge rate ROM. This signal goes high when the short vector detector receives a vector value in which any one or more of RV08- through RV11- are active (i.e., calling for a vector displacement of one quarter or more of the display viewing area).

When the select signal is low, signifying a medium vector length of less than one quarter of the viewing area, the long vector length switch passes inverted replicas of the four least-significant bits of the 12-bit vector displacement code, RV00- through RV03-. These bits and the next four bits from that same 12-bit code, RV04- through RV07-, then are applied to the vector charge rate ROM. These conditions cause that ROM to produce a corresponding charge rate output word as bits I0- through I11-, covering vector lengths from one displacement increment through 255 displacement increments (including the previously discussed short-length vectors).

When the select signal is high, signifying a vector length of one quarter or more of the displayable viewing area, the long vector length switch passes inverted replicas of the four most-significant bits of the displacement value, RV08- through RV11-. These bits and the same mid-value bits, together with the switch select

values, make the vector charge rate ROM produce a correspondingly different charge rate output word. This long-vector output covers vector lengths from 256 increments through the full-scale diagonal displacement of 4095 increments.

Recall that short vectors representing a displacement of less than 1/32 of the breadth of the viewing area are drawn while the ramp generator circuit is set for minimum constant-time operation, with each such short vector requiring approximately 1.25 microseconds as the limit-to-limit ramp excursion period. For 1/32 viewing area displacement and all longer vectors, however, the ramp generator circuit operates in constant-velocity mode. This change is a result of the differential charge-rate value of the output word from the vector charge rate ROM. For all short vectors (less than 1/32 displacement), this output is a 12-bit all-bits-low value (000 hexidecimal). For the case of the borderline 1/32 full-screen displacement (one display increment longer than a "short" vector), this same output is produced, but with the VECZ+E output from the Z-axis control logic now produced at full intensity.

For the case of the next longer increment, however, the control word output from the vector charge rate ROM is a definite positive value (07C, hexidecimal, 124 decimal). This condition turns on specific gates in a current-inhibiting ladder network in the constant current generator. The resultant reduction in current flow through the constant current generator means that capacitor C9 takes slightly longer to charge (or discharge). Consequently, the RAMP output from the ramp generator circuit exhibits a slower rate of change and takes a longer period of time to reach the applicable end-of-ramp limit.

Similarly, the next longer display vector request will produce an even larger output-word value, thereby decreasing the available amount of current flow even further. This condition produces a RAMP signal that takes proportionally longer to reach the applicable end-of-ramp voltage level. The total of 4096 different charge rates--hence ramp durations--that can be established by the 12-bit value carried by lines I0- through I11- thus allow the selection of an equal number of different time periods, each representing the time required by the RAMP signal to change from one voltage limit value to the other.

The vector charge-rate ROM input/output relationships operate such that the ROM functions as an I/R calculator, selecting a C9 current-flow charge rate that is inversely proportional to the range of the vector length. This relationship in turn means that the charging time is proportional to the vector length and hence constitutes a measurement of the time required to draw the corresponding line vector for the given displacement distance. The ROM-program setup is arranged, for example, so that the full-screen vector deflection is accomplished in approximately 40 microseconds. A display line of half that length has double the charge rate, however, meaning that capacitor C9 becomes charged in half that time. Similarly, a line of one fourth full length has four times the charge rate, so that capacitor C9 is charged in one fourth of the full-screen time, etc. The short-length vectors, representing less than 1/32 full-screen deflection, all are accomplished in the constant-rate interval of approximately 1.25 microseconds. Intermediate vectors vary in proportion to their length, calculated at a scale rate of approximately 3.3 microseconds per inch of display vector length.

3.3.2.2.3 Position-move Constant Velocity Mode. When the vector request is a move instruction, not requiring any display, the displacement can be made at a higher speed. Shorter jumps, such as point-plot moves and character-position moves, can be performed in fast mode, as will be explained in the discussion of the ramp generator circuit. Longer blanked vectors must approximate the time required by the D/A-driven deflection amplifiers to realign the blanked CRT beam with the new address, which will be the beginning point for the next-following display instruction.

In this latter case, quite different operation of the charge-rate calculator circuit is established by the $\overline{\text{VROM}}$ input from the mode select decoder. The VPS1+G input is low for this instruction, making the mode select decoder deactivate the $\overline{\text{VROM}}$ signal. Its resultant high-level value now disables the vector charge-rate ROM. At the same time, the low-level complement of that signal from gate U24F now enables the position move charge-rate ROM and simultaneously inhibits the short vector detector from enabling the short vector intensity control circuit.

The position move charge-rate ROM now responds to the 8-bit code carried by output lines RV04- through RV11- from the vector length calculator circuit. The resultant 8-bit output from that ROM is wire-ORed with the eight most-significant bits of the vector charge-rate control word output to the ramp generator circuit. This output thus follows a different charge-rate pattern, which produces much faster (hence shorter) ramp alternations. A full-screen move deflection is accomplished in approximately 25 microseconds, while a short-length move is accomplished in approximately 0.8 microseconds.

3.3.2.3 Ramp Generator. The ramp generator circuit responds to each change in state of the TOGGLE flip-flop signal by switching from one side of a constant-current generation loop to another. The amount of current flow through the loop is controlled by the 12-bit charge-rate control word output from the just-described charge rate calculator and by the $\overline{\text{FAST}}$ output from the mode select decoder, which essentially serves as a very-high-significance bit for the charge rate control word.

3.3.2.3.1 Normal Operation. Each half of the constant current generator is designed to pass current through a loop that includes capacitor C9 in common. When the TOGGLE input goes low (initial state condition), one half of the circuit passes current such that capacitor C9 becomes completely discharged, with the RAMP output from amplifier U43 consisting of a steady-state low-limit value, as established by a two-stage 0V limiter. The limiter circuit consists of Q32, which limits all negative excursions below -0.7V, and second-stage diode CR70, which limits all negative excursions below -0.3V. When the TOGGLE input goes high, the other half of the circuit conducts current through an opposite path to a high-limit value established by a +5V two-stage limiter. This latter subcircuit consists of first stage Q31, which limits all positive excursions above +5.7V, and second stage diode CR69, which limits all positive excursions above +5.3V. The RAMP output thus alternates from just below 0V to just over +5V* when the TOGGLE input goes high, and then alternates back to just below 0V again when the TOGGLE input next goes low.

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*The limit values of the RAMP signal are given elsewhere as nominal values of 0V (lower limit) and +5V (upper limit). The discussion in this paragraph gives more accurate values for explanatory purposes. Bear in mind, however, that the actual values of a RAMP output are determined by manual alignment adjustments based on visual observation of the resultant display conditions.

The ramp generator circuit also includes two limit detectors that monitor the RAMP signal at all times. Low limit detector U40 produces a low BCLP-signal when capacitor C9 is fully discharged--i.e., when the RAMP signal is at its nominal 0V lower limit. Similarly, high-limit detector U42 produces a low ACLP- signal when capacitor C9 is fully charged--i.e., when the RAMP signal is at its nominal +5V upper limit. Whenever the ramp voltage output from the constant current generator is in transit from one limit to the other, of course, both of these two detector outputs must be high simultaneously. These two signals thus constitute a 2-bit timing code for ramp generator circuit operation, used for controlling other card circuits, as follows:

ACLP-	BCLP-	Meaning of Code Condition
Low	Low	Logically impossible.
Low	High	RAMP signal is at (or approaching) nominal 0V lower limit.
High	Low	RAMP signal is at (or approaching) nominal +5V upper limit.
High	High	RAMP signal is in transit from one limit value to the other.

These same two signals also are applied to NAND gate U26B, producing an OVCK-E (Overflow Clock) output that goes low during each ramp-generation period. This output connects to ROM and status card A1A9 as the clock signal to an interrupt-register cell that receives the common OVFL-A (Overflow) output from the D/A converters as its data input. Either D/A converter activates the OVFL-A signal to announce that the last requested instruction would move the CRT beam position out of the programmable area. In that event, as explained in the discussion of the mode control logic circuit on this card, the active OVFL-A signal will ensure blanking of the Z-axis output. In addition, that same active OVFL-A input to the ROM and status card will let that circuit produce an interrupt signal to interrupt the program.

The ramp generator circuit also includes a reference voltage regulator, which establishes a +5V reference level used by this circuit card and the two associated D/A converters. The +5V-potential REFP+E output from that circuit is the positive reference used as the bias for one of two D/A converter circuits on each of the two D/A converter cards. Similarly, the ground-potential REFN+E output is the negative reference used as the bias for the other D/A converter circuit on both of those cards. These reference voltages are compared against the respective ramp-drive signal (RMPX+E on X-axis D/A converter A1A15, RMPY+E on Y-axis D/A converter A1A14) and associated position registers to determine whether that D/A converter should produce an output at any given time. The D/A circuits thus use these reference voltages to activate deflection amplifier drive signals that move the CRT beam in the direction established by the latest-stored position data, with the duration of that deflection signal being controlled by the duration of the associated ramp-drive signal.

The rate of change at which this ramp-timing alternation is allowed to occur is determined by 13 pairs of transistor gates, one gate from each pair being located in each of the two halves of the constant current generator. The charge-rate control

inputs to this circuit normally maintain these current-diverting transistor switches in each circuit-half in their "off" condition. This situation means that a maximum amount of current flows through the constant current generator, producing a very fast charge time for capacitor C9. This rate is the one used for very short vectors, producing a constant-time ramp duration if 1.25 microseconds. As longer vector displacements are requested, however, the vector-length calculator circuit makes the charge-rate calculator circuit raise the value of the charge-rate output word carried on lines I0- through I11-. These changes then turn on corresponding combinations of current-diverter gates to tap off some of the applicable current, thereby reducing the current flow through C9 proportionally. The maximum full-length display deflection thus is indicated by an all-bits-high charge-rate control word, which reduces current flow through the constant current generator to the minimum value required to ensure reliable circuit operation. This condition provides a capacitor charging time of approximately 40 microseconds for full-screen deflections.

3.3.2.3.2 Fast-Speed Mode. The preceding discussion has pertained to the normal condition, when the $\overline{\text{FAST}}$ signal from the mode select decoder is an inactive high level. This high-level state means that the $\overline{\text{FAST}}$-controlled current diverting gating path normally diverts nearly 80% of the full current nominally available to the constant current generator. Consequently, the preceding discussion of normal-speed operation actually pertains to the applicable division of the remaining 20% of the total current flow. When the VPS1+G/VPS2+G code specifies a fast-mode instruction (used only for blanked character-position displacements and point plots), the $\overline{\text{FAST}}$ input becomes an active low level. This input condition turns off the normally active gates in the $\overline{\text{FAST}}$-controlled diverting path, thereby adding the associated 80% of total current flow to the C9 charging path. This change means that capacitor C9 becomes charged or discharged almost immediately under these instruction conditions, regardless of any control inputs applied by the ramp control logic to the less-significant current-diverter gates controlled by the charge-rate output word from the ramp generator logic.

3.3.2.3.3 Low-Speed Mode. The ramp generator circuit also includes a low-speed integrator switch, that is controlled by the line vector speed control logic. This switch normally is an open circuit, having no effect on the RAMP signal. When the program requires slow speed operation (as for driving a slow-speed hard-copy device), the line speed control logic produces a high-level SPED-signal, causing the low-speed integrator switch to close a circuit path between the ramp-signal output from the constant current generator and a capacitor C16 connection to ground. This condition effectively adds C16 to C9, meaning that the RAMP signal takes longer to reach its applicable charge/discharge limits.

3.3.3 X/Y RAMPS CONTROL LOGIC

The function of the S/Y ramps control logic is to convert the RAMP output from the previously described ramp generation logic into separate X-axis and Y-axis timing signals, respectively identified as RMPX+E and RMPY+E. This circuit is controlled by ramp/conic selection flip-flop U17A, which is cleared by each active occurrence of the VPS2+G mode control signal.

3.3.3.1 Ramp-Mode Operation. This cleared state represents the normal-use ramp-mode function. This condition closes U48 switching paths such that the RAMP signal output from the ramp generation logic divides into two output paths that produce separate drive signals for the associated D/A converter cards. Each of these output paths is identical, consisting of a third-stage limiter circuit and a following unity gain amplifier. The third-stage limiter circuit completes the refinement of the RAMP input by establishing precise 0V and +5V limits and maintaining linear ramp slope within ±20 mV accuracy. In this case, both ramp-drive outputs are identical, and the resultant CRT beam deflection follows a straight line.

3.3.3.2 Conic-Mode Operation. When the ramp cycle is to be a conic operation, activation of the VPS2+G code input is followed by an active STKX-G (Start Conic) pulse from the graphic controller. The high-going trailing edge of that pulse then sets flip-flop U17A, representing a conic-mode function. This condition changes the U48 switching paths such that the inputs to the two ramp-output circuits now consist of the respective outputs from two separate ladder networks, both of which receive the original RAMP signal in common. One of these networks produces an output that represents a cosine value of the concurrent RAMP signal at any time; this output connects to the output circuit that produces the RMPX+E drive signal applied to X-axis D/A converter card A1A15. The other ladder network produces an output that represents the sine value of the concurrent RAMP signal; this output connects to the output circuit that produces the RMPY+E drive signal applied to Y-axis D/A converter card A1A14. The combination of these trigometric functions thus replaces the rectangular-coordinate technique of the ramp mode, which produces straight line vectors, with a polar-coordinate technique, which produces elliptic lines.

So long as ramp/conic selection flip-flop U17A is in its normal reset state, then, the two D/A converter cards receive identical drive signals, producing a linear displacement of the displayed line from an old screen position address to a new screen position address. When this selection flip-flop is set, however, the respective outputs are trigonometric timing functions that cause the eventual display point to move faster with respect to one rectangular axis than to the other, thereby producing a curved line that represents a conic-section displacement.

3.3.4 Z-AXIS CONTROL LOGIC

The Z-axis control logic determines whether the vector displacements currently being driven by the RMPX+E and RMPY+E outputs are to be displayed or not--and, if so, how bright the display line is to be. This circuit contains a line vector unblanking logic subcircuit and a point-plot unblanking logic subcircuit, together with output gating driven by these two special-application decoding subcircuits. The output gating normally produces an inactive low-level VECZ+E output, which blanks the CRT trace. When the last-received instruction calls for a line vector or a point-plot operation, however, the appropriate decoding subcircuit causes the output gating to activate a high-level VECZ+E output to drive the CRT Z-axis control signal.

3.3.4.1 Line Vector Unblanking Logic Operation. The line vector unblanking logic receives as inputs the VPS1+G line draw command, an associated line-draw enabling output from the mode select decoder, the ACLP- and BCLP- ramp limit signals from the ramp generator logic, and the ramp/conic status signal from the ramp/conic selection flip-flop. Whenever these signals confirm that the ramp generator logic is generating a ramp signal (ACLP- and BCLP- both are high) for a line vector

instruction (VPS1+G and the draw command from the mode select decoder both are high), this decoding logic applies a high line-enable signal to NAND gate U15C.

If the X/Y ramps control logic is set for ramp-mode operation, the high-level status input from the ramp/conic selection flip-flop causes this high-level enabling signal to be concurrent with the generation time of the ramp signal, terminating as soon as the ramp reaches its applicable end-limit potential (i.e., when either ACLP- or BCLP- go low). If the X/Y ramps control logic is set for conic-mode operation, however, the low-level status input from that flip-flop introduces a 20-nanosecond delay to accommodate the additional timing requirements of the sine-function and cosine-function subcircuits in the X/Y ramps control logic.

The other input to AND gate U15C is the unblank-enable output from the line structure control logic. The nature of that signal during the concurrent line vector enabling period depends on the associated line structure selection instructions applied to that circuit by the program. This output will be either a steady-state high logic level (solid line request) or an alternating signal with high-level periods representing the CRT-on time of a dotted, dashed, or centerlined line structure, as applicable.

The resultant low-level activation(s) from NAND gate U15C pass through a 40-nanosecond delay that matches the Z-axis output with the timing of the slower X-axis and Y-axis drive outputs from the X/Y ramps control logic. This UNBLANK signal then drives a high-level VECZ+E signal from inverting-OR gate U39D for the duration(s) of the unblanking-enable output from the line structure control logic during the active duration of the line-enable output from the line-vector unblanking logic. Recall that the actual voltage potential of the VECZ+E signal also is a function of the concurrent bias output from the short vector intensity control circuit in the ramp generation logic. For short vectors of less than 1/32 full-screen deflection, this output is a length-associated value that attenuates the concurrent Z-axis drive output to maintain an even brightness across the display.

3.3.4.2 Point-Plot Unblanking Logic Operation. The point-plot unblanking logic receives the ACLP- and BCLP- ramp-limit timing signals from the ramp generation logic, the VPS1+G and VPS2+G instruction-code signals, and the SPED- status output from speed selection flip-flop U6C. When the instruction code specifies a point-plot operation (both VPS1+G and VPS2+G are high), the point-plot unblanking logic responds to the end of a ramp-generation interval (either ACLP- or BCLP- goes low) by triggering a one-shot timing circuit that activates a low-level PPUB (point-plot unblank) output pulse. When the ramp generator logic is in low-speed mode (SPED- output from flip-flop U6C is high), this PPUB pulse is extended proportionally. Either way, the active PPUB signal drives a high VECZ+E output from inverting-OR gate U39D for its momentary duration.

3.3.5 OPERATION TIMING LOGIC

The operation timing logic monitors associated circuits to determine the in-process and completion times of the response to the last-received instruction and notifies the D/A converter cards of such events. This notification steers new position data inputs to the inactive position registers on the D/A converter cards and clears old data from the register at the end of the ramp-generation period. The circuit also sends an active FBSY-X output to the graphic controller card during most inprocess operation periods.

The inputs to this circuit include timing signals from the point-plot unblanking logic and line-vector unblanking logic, the ACLP- and BCLP- ramp limit signals from the ramp generation logic, and the status signals from toggle flip-flop U17B. An operation time decoder in this circuit monitors these inputs to produce a $\overline{\text{BUSY}}$ signal that is low during any of the following four operating conditions:

a. The ramp generator circuit is generating a charging ramp (applicable for line vector, move, or point-plot operations).

b. The ramp generator circuit is generating a discharging ramp (applicable for line vector, move, or point-plot operations).

c. The ramp generation time associated with one of the first two possibilities refers to a conic line vector, and the associated 20-nanosecond delay following completion of that ramp has not yet timed out.

d. The ramp generation time associated with one of the first two possibilities refers to a point plot, and the point-plot pulse that follows completion of that ramp has not yet timed out.

The low-level $\overline{\text{BUSY}}$ signal unlocks the line structure control logic, allowing that circuit to perform as directed by the program. At the same time, this signal is applied to an inprocess/done detector circuit that produces three resultant outputs, as follows:

a. VPBY+E (Vector Position Busy) - This normally low output goes high as soon as the operation time decoder confirms a ramp-generation sequence has started and stays high for a brief delay interval following completion of ramp generation and any associated timing functions (i.e., point-plot timing or additional conic-mode delay). This high signal state sets up the A and B position registers on the two associated D/A converter cards to monitor each other's outputs.

b. VPNL+E (Vector Position Null) - This normally low output pulse goes high during the post-operation delay interval of the VPBY+E signal. This high signal state, in conjunction with the concurrent logic state of the TOGL-E output signal, activates a loading pulse for those parallel-input position registers in the D/A converter cards which currently contain the oldest address data. The concurrently high VPBY+E signal causes those registers to be monitoring the outputs of the other registers, which contain the newest-loaded address (i.e., the current position at the end of the just-concluded operation). These conditions cause the no longer needed old address values in the first registers to be replaced by the current-position address values in the second.

c. FBSY-X (Function Busy) - This normally high output signal goes low during the active period of the $\overline{\text{BUSY}}$ output from the operation time decoder, provided that certain enabling conditions are valid. This signal, which also can be activated by the common wire-ORed outputs from certain other circuit cards in the terminal controller, connects to the graphic controller card as one of three external signals that can inhibit the master clock signal on that card, thereby inhibiting completion of concurrent processing functions. The active FBSY-X signal thus prevents the program from continuing to the next instruction until the current vector-displacement action has been completed.

The FBSY-X output from the ramp/conic generator card can be inhibited by a unique operation condition. This condition occurs when the card is operating in normal-speed mode (i.e., the hardcopy-associated low speed mode has not been requested) and the mode select decoder confirms that the current instruction calls for a point-plot or character-position operation. Under these circumstances, the mode decoder produces a high-level FBSY INHIBIT output that, in conjunction with the normal-speed output from speed flip-flop U6C, drives a low FBSY INHIBIT output from NAND gate U26D. This latter low-level signal then inhibits the FBSY gating circuit in the inprocess/done detector logic, maintaining the FBSY-X output line at a high logic level without affecting the operation of the VPBY+E and VPNL+E gating circuits.

The reason for this development is that the activation of FBSY-X to inhibit the graphic controller means that the graphic controller then must remain in its inhibited state until an internal clock signal on that card determines that the FBSY-X signal has again gone inactive. That very interrogation technique thus adds excessive delay in the case of point plots, which thus would require approximately 2.25 microseconds each. The inhibition of FBSY-X thus reduces the point-plot interval to approximately 1.95 microseconds, which easily allows the point-plot function to be completed before the graphic controller circuit can change setup conditions of the ramp/conic generator input signals.

The address-updating function of the VPBY+E and VPNL+E signals simplifies system programming for on-axis vector displacements. Updating the oldest address to the current-position address at the end of each operation means that the next new-position address, to be loaded into the same position registers on both D/A converter cards, only needs to be specified when actually changed. If the next displacement only travels along one axis, therefore, the other axis can remain at its already updated current-position address.

3.3.6 MODE CONTROL LOGIC

The mode control logic establishes appropriate enabling/disabling signals for various circuit functions on the ramp/conic generator as a response to corresponding inputs. The inputs to this circuit include the VPS1_G and VPS2+G instruction-code signals from the graphic controller card, the OFLW-A overflow status output from the D/A converters, and the six most-significant vector-length bits supplied by the Y-axis D/A converter card. Table 3-1 illustrates the relationship between the various input condition possibilities of these signals and the resultant control condition applied to other logic circuits on this card.

The basic control inputs are the VPS1+G and VPS2+G mode-selection inputs, as follows:

a. Both VPS1+G and VPS2+G are low during processing of all move instructions (MVXA, MVYA, MVXR, MVYR, and MVSR) and of the load-conic instruction (LDKY). This condition causes the mode control logic to inhibit the line-vector unblanking circuit in the Z-axis control logic to prevent unblanking of the Z-axis drive signal.

b. VPS1+G is high with a low VPS2+G signal during the processing of all draw instructions (DRXA, DRYA, DRXR, DRYR, DRSR, and DRKY). Under these conditions, the mode control logic produces a low VROM signal to enable the vector charge-rate ROM in the ramp generator logic and also enables the line vector unblanking circuit in

register is a steady-state high logic level. This signal completes the enabling condition for the Z-axis control logic output circuit, unblanking the VECZ+E Z-axis drive output during active ramp-development periods--hence producing a steady-state, solid line vector on the CRT.

For the other three patterns, the shift register output is a function of the loading conditions supplied by the decoding network when the operation timing logic activates the shift command by initiating a low-level BUSY signal. The 16-bit register loading conditions are as follows:

a. Bits 0 and 4 always grounded (output high).

b. Bits 1, 2, 5, 6, 9, 10, 13, and 14 follow DB04-G (output low for dotted line, high for dashed or centerline operations).

c. Bits 3, 7, 11, and 15 are exclusive-OR of selection code (output low for dotted or dashed lines, high for centerline operation).

d. Bits 8 and 12 are complement of negative-AND of selection code (output high for centerline operation, low for all other operations).

The results, as shown in figure 3-2, produce the desired VECZ+E enabling conditions. Since the "solid" selection activates the LOAD input to the register, its subsequent output is the steady-state complement of the bit 15 input, as previously described. For the other selection conditions, however, actuation of a SHIFT command by the operation timing logic causes the shift register to continually sequence through the applicable bit pattern. These patterns, as shown in figure 3-2, produce a "dot" condition during one out of every four clocking periods, a "dash" condition during three out of every four clocking periods, or a "centerline" condition as sequences of two and eleven clock periods, respectively, each separated by a single clock-pulse period.

3.3.8 LINE VECTOR SPEED CONTROL LOGIC

The line vector speed control logic decodes the program-requested speed selection and controls associated circuits accordingly. The heart of this speed control logic is speed-selection flip-flop U6C, which becomes reset when the graphic controller card produces an active low-going STDP-G signal while DB09-G and DB10-G data bus lines both are low (slow speed selection). If DB10-G is low and DB09-G is high (regular speed selection) at that time, however, flip-flop U6C becomes set.

The regular-speed set state of flip-flop U6C primes the FBSY-X inhibit circuit (gate U26D). The high set-state output also enables a clock-select gating path in the line vector speed control logic that routes the output of a tank-circuit oscillator as the clocking signal for the 16-bit shift register in the associated line structure control logic. This oscillator is enabled as a free-running circuit only during the ramp-development period of a line vector drawing instruction, while the LINE ENABLE output from the line vector unblanking circuit in the Z-axis control logic is high. The oscillator is designed to match the speed requirements of line structure patterns with the vector charge rate of the ramp generator circuit.

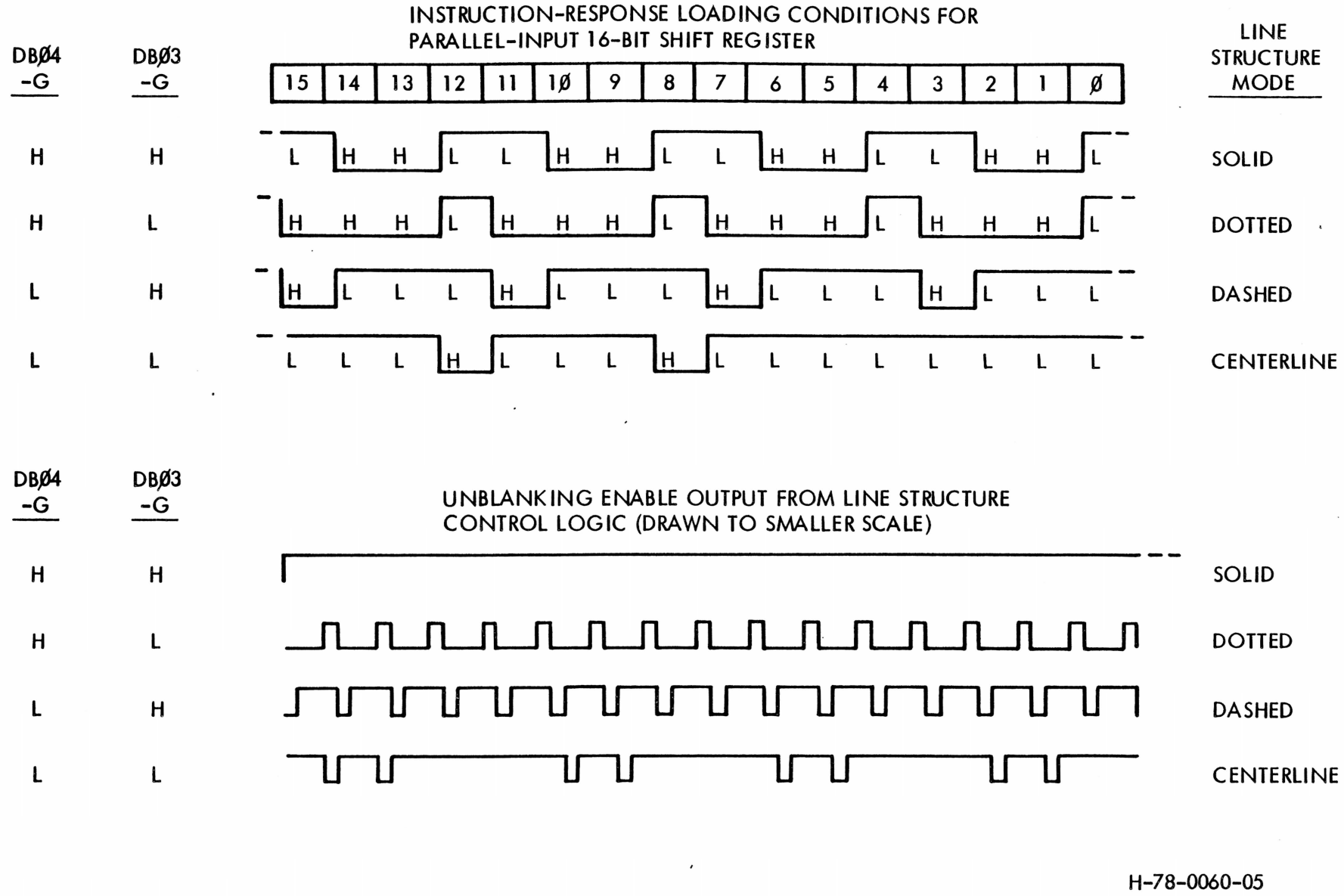

Figure 3-2. Timing Diagram for Development of Line Structure Output Patterns

When speed-selection flip-flop U6C is reset, the FBSY-X inhibit circuit and the normal-speed clock select gating path both become disabled. At the same time, the high-level reset-state SPED- output from that flip-flop closes the low-speed integrator switch in the ramp generator circuit to retard the development of the RAMP signal by the additional charging time of capacitor C16. The high-level SPED- signal also extends the point-plot pulse-delay period of the point-plot unblanking logic in the Z-axis control logic circuit.

Finally, the same high-level SPED- signal also enables a different clock-select gating path in the line vector speed control logic, this one passing the output of a divide-by-16 counter as the clocking input to the line structure control logic output register. This divide-by-16 counter, which is clocked by the output of the ramp-enabled oscillator, thus passes to the line structure control logic a signal that has only 1/16 of the normal-speed oscillator frequency, meaning that the resultant vector line structure patterns applied to the Z-axis control logic output circuit will take sixteen times as long to produce. This slowdown thus matches the vector output to the limited speed capabilities of a hardcopy printer when applicable.

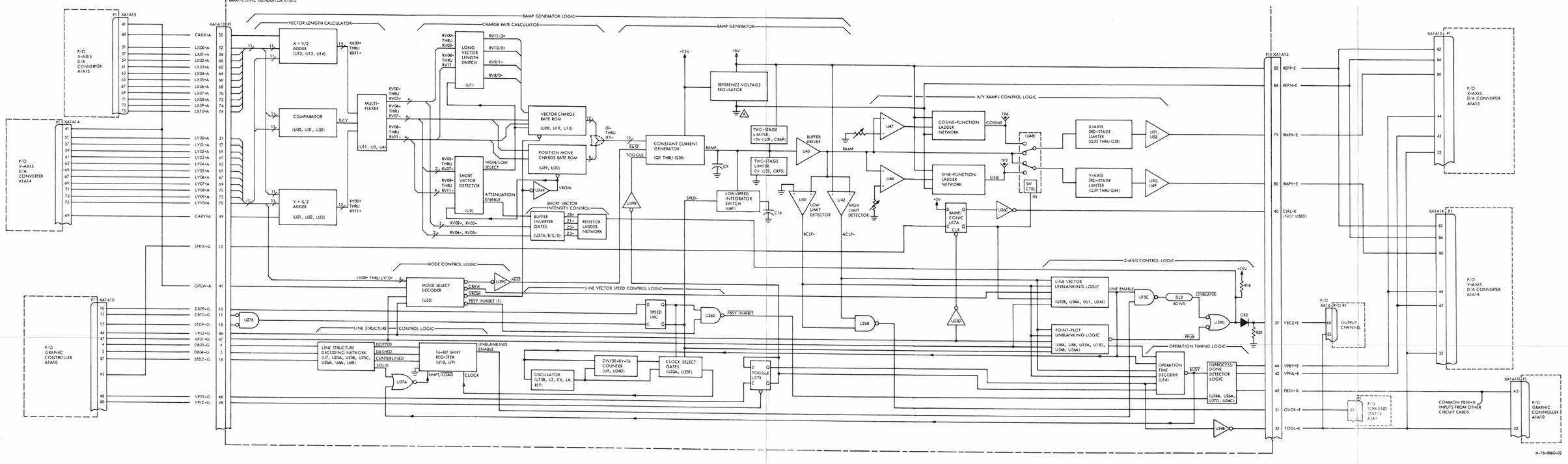

Figure 3-3. Detailed Functional Block

SECTION 4

INSTALLATION

4.1 GENERAL

This section provides information pertaining to unpacking of the Model 5743 Ramp/Conic Generator card and installing it in the GRAPHIC 7 system.

4.2 UNPACKING AND VISUAL INSPECTION

Inspect the shipping container carefully. If the container shows any evidence of rough handling or is sufficiently damaged to have affected the contained assembly, notify the carrier immediately.

After removing the ramp/conic generator card from the container, inspect the card assembly for any damage. If the unit seems damaged in any way, notify Sanders Associates, Inc., immediately.

4.3 INSTALLATION

Install the ramp/conic generator circuit card assembly as follows:

a. Turn off ac power at the terminal controller unit.

b. Obtain access to terminal controller card cage and remove ramp generator circuit card assembly A1A13 (or previously installed ramp/conic generator circuit card assembly A1A13, if applicable).

c. Install replacement ramp/conic generator circuit card assembly in the XA1A13 card slot of the terminal controller card cage.

d. Turn on ac power for the terminal controller unit and perform the operator's checkout procedure of paragraph 2.2, preceding.

SECTION 5

MAINTENANCE

5.1 MAINTENANCE PHILOSOPHY

The overall maintenance approach is based on using the ramp/conic generator checkout procedure presented in paragraph 2.2, preceding. The Model 5743 ramp/conic generator circuit card assembly is an off-the-shelf item and is not field repairable; maintenance is limited to alignment and fault isolation to the circuit card level.

5.2 TROUBLESHOOTING

The optional ramp/conic generator card is a direct replacmeent for the nominal ramp generator circuit card assembly with full pin-to-pin compatibility. Consequently, system troubleshooting remains unchanged and should be performed in full accordance with the procedure given in the Terminal Controller Maintenance Manual for the GRAPHIC 7 Computer Graphics Display System. When performance of that troubleshooting procedure isolates a problem to the ramp-conic generator card, perform the alignment procedure in the following paragraph to determine whether the fault is a true failure or merely a case of circuit degradation/misalignment.

5.3 ALIGNMENT PROCEDURE

The following instructions represent the alignment procedure for the Model 5743 ramp/conic generator circuit card assembly. The procedure requires a DVM for voltage measurements within an accuracy of three decimal places (true value plus or minus one millivolt). Perform this procedure whenever the display presentation fails to pass any one or more of the opeator checkout examinations of paragraph 2.2 or exhibits patently incorrect operation on the part of the ramp/conic generator circuit (i.e., horizontal and vertical corner-angle presentations either do not meet at a common point or are visably brighter than the lines themselves, required line-structure patterns are not displayed, conic presentations are clearly unsymmetric, or short-vector presentations are either too bright or too dim). In the event that any one or more of these failure conditions cannot be corrected by performance of the full alignment procedure, replace the defective ramp/conic generator card. For location of referenced test points, adjustments, and jumper connections, see drawing 1086939, located in Section 6.

a. With system power off, mount ramp/conic generator card on terminal controller card extender to gain ready access to test points and potentiometer adjustments.

b. Reactivate system power and place system in LOCAL mode to obtain graphic display presentation of program-generated test pattern (see figure 2-1).

c. Monitoring TP1 (REFP+E) with DVM, adjust R90 to obtain reference voltage value within limits of +5.00 ± 0.01V.

NOTE

The following two adjustments are temporary setups that deliberately misadjust the ACLP/BCLP "window" to cover a wider voltage range than the RAMP signal actually allows. This condition is identified by vector-end "blooming" on the display when the additional pre-knee and post-knee RAMP-display time produces brighter spots on the display that the vector itself. Once these bright spots are obtained, reduce general display intensity to desired personal-comfort level so as to minimize bloom-point glare and dispersion, with line vectors just showing.

d. Monitoring displayed test pattern, adjust R166 fully clockwise to temporarily lower operating limit of BCLP- low-limit detector below actual ramp-end value, as indicated by blooming of associated vector-end points on display screen.

e. Monitoring displayed test pattern, adjust R160 fully clockwise to temporarily raise operating limit of ACLP- high-limit detector above actual ramp-end value, as indicated by blooming of assicated vector end points on display screen.

NOTE

Steps f and g, following, pertain to alignment of ramp control logic to establish proper ramp window settings.

f. Align X-axis ramp control logic as follows:

1. Connect a temporary jumper between test points TP7 (X-axis PRERAMP) and TP8 (REFN-E ground) to nullify effect of input signal.

2. Monitoring TP9 (RMPX+E) with DVM, adjust R92 to obtain RMPX+E baseline value of 0.000 ± 0.001V.

3. Remove temporary jumper installed in step 1.

4. Monitoring displayed test pattern, adjust R187 (X-axis -RAMP LIMIT) for maximum coincidence of lower superimposed H-character symbols at left-hand side of display screen.

5. Monitoring displayed test pattern, adjust R180 (X-axis +RAMP LIMIT) for maximum coincidence of upper superimposed H-character symbols at left-hand side of display screen.

g. Align Y-axis ramp control logic as follows:

1. Connect a temporary jumper between test points TP10 (Y-axis PRERAMP) and TP11 (REFN-E ground) to nullify effect of input signal.

2. Monitoring TP12 (RMPY+E) with DVM, adjust R213 to obtain RMPY+E baseline value of 0.000 ± 0.001V.

3. Remove temporary jumper installed in step 1.

4. Monitoring displayed test pattern, adjust R205 for maximum coincidence of bright dots marking vector-end and vector-beginning limits in either lower left-hand corner or upper right-hand corner of display are.

5. Monitoring displayed test pattern, adjust R201 for maximum coincidence of bright dots marking vector-end and vector-beginning limits in either upper left-hand corner or lower right-hand corner.

NOTE

Steps h through r, following, pertain to alignment of conic-generation adjustment potentiometers. Although final close-tolerance values are given where applicable, bear in mind that the interactive nature of these adjustments means that this sequence may have to be repeated several times in order to achieve final settings for all adjustments. If you find it impossible to achieve any one or more of these adjustments successfully even after repeated cycles, replace the defective circuit card assembly.

h. Using DVM, confirm that cathode of VR5 measures +5.1V ± 0.51V.

i. Monitoring junction of C18 and R125 with DVM, adjust R124 (±5V REFERENCE) to obtain value as close as possible to +5.100V (must be within 1% limits from +5.049V through +5.151V).

j. Monitoring junction of C21 and R128 (GROUND REFERENCE) with DVM, adjust R127 to obtain value as close as possible to 0.000V (must be within tolerance limits from -0.051V through +0.051V).

k. Monitoring displayed test pattern, adjust R122 to move conic traces outward on Y-axis just until large outer circular trace begins to flatten at junctions with top and bottom sides of inner square (90^{o} and 270^{o} points).

l. Monitoring displayed test pattern, adjust R158 to move conic traces outward on X-axis just until large outer circular trace begins to flatten at junctions with left and right sides of inner square (180^{o} and 0^{o}).

m. Monitoring displayed test pattern, adjust R99 (250^{o} Y-axis pull) for maximum-possible coincidence of large circular trace with 250^{o} and 260^{o} points plots (2nd and 3rd from bottom; see figure 5-1).

n. Monitoring displayed test pattern, adjust R135 (195^{o} X-axis pull) for maximum-possible coincidence of large circular trace with 190^{o} and 200^{o} point plots (2nd and 3rd from top; see figure 5-1).

o. Monitoring displayed test pattern, adjust R134 (225^{o} X-axis offset) for maximum-possible coincidence of large circular trace with 220^{o} and 230^{o} point plots (5th and 6th from top; see figure 5-1).

p. Monitoring displayed test pattern, adjust R95 (240^{o} Y-axis gain) for maximum-possible coincidence of large circular trace with 240^{o} point plot (4th from bottom; see figure 5-1).

q. Monitoring displayed test pattern, adjust R131 (210^{o} X-axis gain) for maximum-possible coincidence of large circular trace with 210^{o} point plot (4th from top; see figure 5-1).

r. Repeat steps i through q as necessary to ensure best-possible settings of these interactive adjustments. Bear the following relationships in mind to determine further-adjustment requirements:

1. Sine-function roundness depends on settings of R124, R122, and R95.

2. Cosine-function roundness depends on settings of R127, R158, and R131.

3. General combined-function roundness depends on settings of R99, R134, and R135.

s. Once optimum roundness is obtained, close ramp-end limit detector windows to correct settings as follows:

1. Monitoring displayed test pattern, adjust R160 counterclockwise just until bright spots marking high-end knee of RAMP vectors disappear.

2. Monitoring displayed test pattern, adjust R166 counterclockwise just until bright spots marking low-end knee of RAMP vectors disappear.

t. Adjust overall display-screen intensity to desired personal-comfort level, and then adjust R19 as necessary to obtain uniform-intensity level for all short-vector segments in upper right-hand quadrant of test pattern.

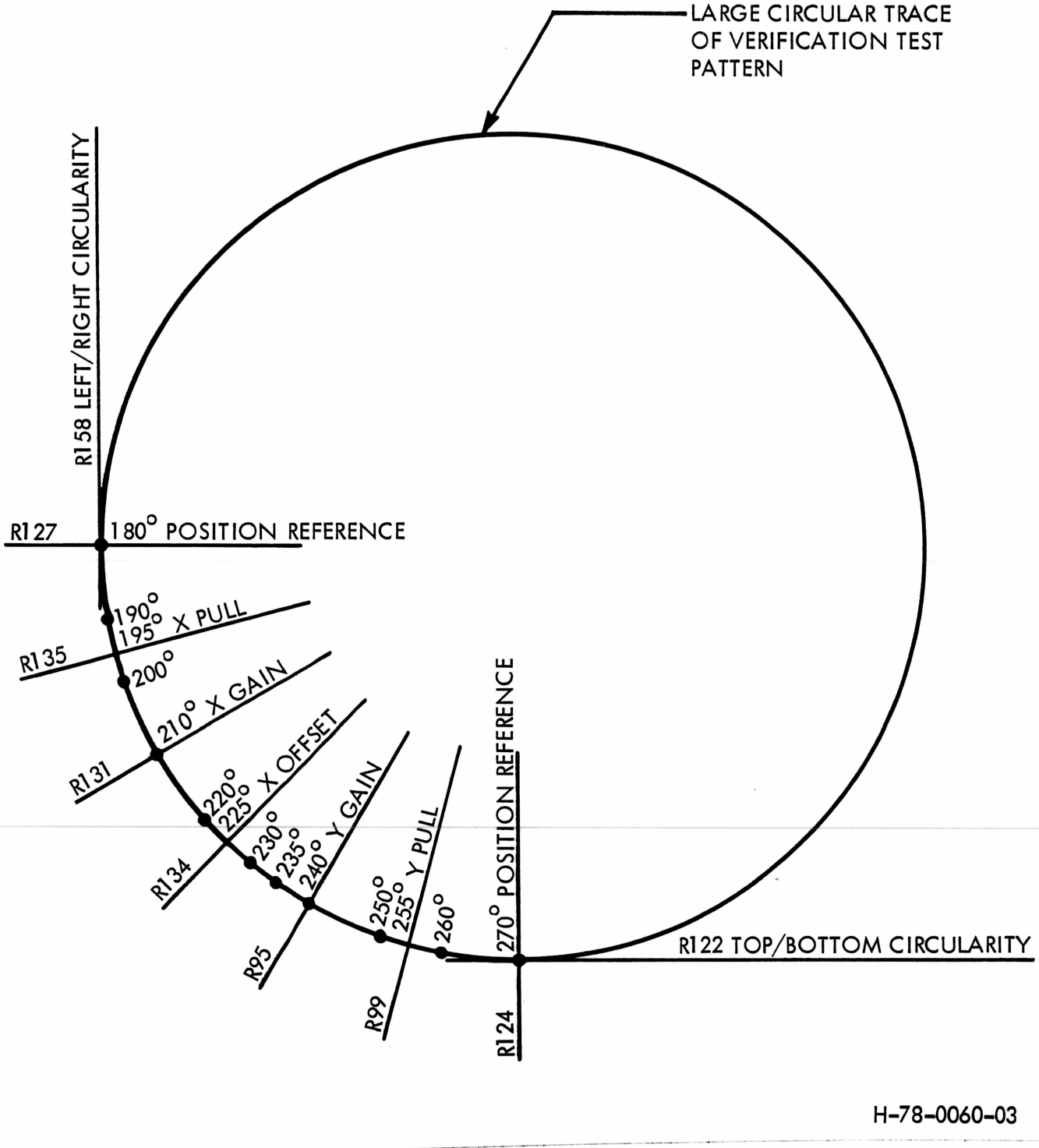

Figure 5-1. Effect of Conic Adjustment Potentiometer Settings

SECTION 6

DIAGRAMS AND PARTS LIST

6.1 GENERAL

This section contains the parts-layout assembly drawing, the full parts list, and the schematic logic diagram for the Model 5743 Ramp/Conic Generator circuit card assembly. The drawings are arranged in numerical order, as follows:

1086939	Circuit Card Assembly, Ramp/Conic Generator
PL1086939	Parts List, Ramp/Conic Generator CCA (Sheets 2 thru 10)
1086941	Logic Diagram, Ramp/Conic Generator (Sheets 1 thru 5)

REVISION STATUS

PARTS LIST	SH	1	2	3	4	5	6	7	8	9	10	11	12
	REV	J	D	B	B	B	B	B	B	B	E		
	SH	13	14	15	16	17	18	19	20	21	22	23	24
	REV												

DWG REV	D
WL REV	N/A

2. PARTS LIST SHEET ONE IS THE CONTROLLING REVISION FOR THE COMBINED PARTS LIST, DRAWING AND WIRE LIST.

1. SHOP PRACTICE TOLERANCES AND DRAWING INTERPRETATION WITHIN 815002 SUPPLEMENT THIS DRAWING.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
—	REL FOR PREPROD	18 AUG 77	WG/REQ
A	REV PER ECO 76110	30 NOV 77	AS/RLB
B	REV PER ECO 76163	10 MAY 78	RP/RLB
C	REV PER ECO 76237	27 OCT 78	WG/RLB
D	REV PER ECO 76268		
E	REV PER ECO 76311	1 FEB 79	SG/WL
F	REV PER ECO 76387	7 JUN 79	WG/WL
G	REV PER ECO 76411	3 JUL 79	WG/WL
H	REV PER ECO 96236	18 DEC 79	RDM/WL
J	REV PER ECO 96383	9 APR 80	WG/WL

PREPROD
CHANGE BY ECO ONLY

MFG K Bunk 9/6/77

1086851	GRAPHIC-7
NEXT ASSY	USED ON
APPLICATION	

CONT NO.

DRFTG	DR W. Guzowski 8 JUL 77	DATE
	APPD	
	CHK	
ENGRG	DEV R. Grant 9-1-77	
	E/M	
	PROJ J. E. Keller 9-6-77	

SANDERS ASSOCIATES, INC — NASHUA, NEW HAMPSHIRE

CIRCUIT CARD ASSY, RAMP/CONIC GEN.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

SHEET 1 OF 10

OP—1039 REV B

DWG SIZE E

PARTS LIST

ITEM NO.	QTY PER ASSY G1	QTY PER ASSY G2	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
1	1	1		E		1086940G2	CIRCUIT CARD SUBASSY	
2								
3	1	1		A		0310092P001	MED (SN7400N) U15	
4	1	1		A		0310225P001	MED (SN74H00N) U26	
5	1	1		A		0310226P001	MED (SN74H01N) U39	
6	1	1		A		0310200P001	MED (SN7402N) U27	
7	1	1		A		7013070P085	MED (SN74S03N) U36	
8	1	1		A		0310319P001	MED (SN74S04N) U24	
9	1	1		A		0310202P001	MED (SN7404N) U25	
10	1	1		A		0310320P001	MED (SN74S20N) U34	
11	1	1		A		0310205P001	MED (SN7437N) U38	
12	1	1		A		7013070P036	MED (SN74S51N) U33	
13	1	1		A		0310270P001	MED (SN74H53N) U16	
14	1	1		A		7013070P026	MED (SN74S74N) U17	
15	1	1		A		0310208P001	MED (SN7475N) U6	
16	3	3		A		0313024P001	MED (SN7485N) U30,31,32	
17	1	1		A		0310098P001	MED (SN7493AN) U5	
18	1	1		A		0313026P001	MED (SN74148N) U2	
19	4	4		A		7013070P022	MED (SN74S158N) U1, 3, 4, 11	
20	2	2			01295	SN74165N	MED U9,18 (TI)	
21	6	6		A		7014130P002	MED (74283N) U12,13,14,21,22,23 (TI)	
22	1	1		A		0310213P001	MED (F9321PC) U7	
23	1	1		A		0310328P001	MED (F9602PC) U8	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV D | SHEET 2

PARTS LIST

ITEM NO.	QTY PER ASSY G1	QTY PER ASSY G2	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
24	1	1			17856	DG187BA	MED U41 (SILICONIX)	
25	1	1			17856	DG190AP	MED U48 (SILICONIX)	
26	5	5		A		7013128P001	MED (HA2-2525-5) U43,46,47,50,51	
27								
28								
29	1	1			02714	LM-220H-5.0	MED U45 (NAT)	
30	2	2			02714	LM-261H	MED U40,42 (NAT)	
31	1	1		A		0310244P001	MED (LM-305-A) U53 (NAT)	
32	1	1			02714	LM-317H	MED U44 (NAT)	
33								
34	2	2		A		7534002P008	MED (LH-0002CH) U49,52	
35	1	1		A		0228041P032	MED (899-1-R1K) U37	
36	1	1				1086947P32	PROGRAMMED PROM (6306-1J) U35	
37	1	1		A		1086962P6	PROGRAMMED PROM (6300-1J) U20	
38	1	1		A		1086962P7	PROGRAMMED PROM (6300-1J) U29	
39	1	1				1086963P5	PROGRAMMED PROM (6305-1J) U10	
40	1	1				1086963P6	PROGRAMMED PROM (6305-1J) U19	
41	1	1				1086963P7	PROGRAMMED PROM (6305-1J) U28	
42	-	1				CK06BX152K	CAP, 1500PF, ±10%, 200V C16	
43	13	13		A		7506001P027	CAP, 100PF, ±5%, 500V, C1,29,31,51,53 65,67,70,73,80,81,85,88	
44	2	2		A		7506001P020	CAP, 51PF, ±5%, 500V, C2,3	
45	1	1		A		7506001P022	CAP, 62PF, ±5%, 500V, C6	

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SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV B SHEET 3

PARTS LIST

ITEM NO.	QTY PER ASSY G1	QTY PER ASSY G2	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
46	68	68		A		7502023P055	CAP, .01UF, ±10%, 100V, C7,10,11,12,13 25,27,28,30,33,35-43,45,47-50,54 55,57,59-64,68,71,72,74-79,83,86 87,89-111	
47	1	1		A		7506001P055	CAP, 1500PF, ±5%, 500V, C9	
48	1	1		A		7506001P019	CAP, 47PF, ±5%, 500V, C14	
49	1	—		A		7502023P063	CAP, .027UF, ±10%, 50V, C16	
50	2	2		A		7011451P117	CAP, 1UF, ±20%, 50V, C19,20	
51	5	5		A		7506001P001	CAP, 1PF, ±.5PF, 500V, C22,23,44,52,56	
52	2	2		A		7011451P067	CAP, 22UF ±20%, 35V, C24,26	
53	4	4		A		7011451P019	CAP, 39UF, ±10%, 10V, C8,15,32,34	
54	6	6		A		7506001P006	CAP, 10PF. ±5%, 500V, C46,58,66,69,82,84	
55	2	2		A		7502023P073	CAP, .1UF, ±10%, 50V, C17,18	
56	1	1				C330C105Z5UICA	CAP, 1UF, +80-20%, 50V, C21 (KEMET)	
57								
58	8	8		A		7550001P073	RES, 1K OHMS, ±5%, .25W, R1,3,6,15,25 172,182,203	
59	9	9		A		7550001P066	RES, 510 OHMS, ±5%, .25W, R2,4,7,9 12,174,190,195,211	
60	2	2		A		7550001P080	RES, 2K OHMS, ±5%, .25W, R5,14	
61	2	2		A		7550001P068	RES, 620 OHMS, ±5%, .25W, R8,13	
62	19	19		A		7550001P097	RES, 10K OHMS, ±5%, .25W, R10,26-34 62-70	

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SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV B SHEET 4

OP—277 REV C

PARTS LIST

ITEM NO.	QTY PER ASSY G1	G2	G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
63	1	—		A		7550001P123	RES, 120K OHMS, ±5%, .25W, R11	
64	3	—		A		7550001P094	RES, 7.5K OHMS, ±5%, .25W, R16, 183, 204	
65	11	11		A		7550001P084	RES, 3K OHMS, ±5%, .25W, R17, 38, 41 48, 71, 177, 185, 186, 198, 208, 209	
66	1	1				RLR20C8250FM	RES, 825 OHMS, ±1%, .50W, R18	
67	3	3		A		7558001P007	RES, VAR, 1K OHMS, ±20%, .50W, R134, 180 201	
68	1	1		A		7558001P026	RES, VAR, 1K OHMS, ±20%, .50W, R19	
69	1	1		A		7550001P058	RES, 240 OHMS, ±5%, .25W, R20	
70	1	1				RLR07C4990FM	RES, 499 OHMS, ±1%, .25W, R22	
71	1	1				RLR07C1001FM	RES, 1K OHMS, ±1%, .25W, R23	
72	3	3				RLR07C2001FM	RES, 2K OHMS, ±1%, .25W, R24, 50, 73	
73	3	3				RLR07C4021FM	RES, 4.02K OHMS, ±1%, .25W, R21, 51, 74	
74	2	2		A		7550001P041	RES, 47 OHMS, ±5%, .25W, R35, 171	
75	1	1		A		7550001P070	RES, 750 OHMS, ±5%, .25W, R36	
76	3	3		A		7550001P077	RES, 1.5K OHMS, ±5%, .25W, R37, 86, 87	
77	1	1		A		7550001P081	RES, 2.2K OHMS, ±5%, .25W, R39	
78	3	3		A		7550001P083	RES, 2.7K OHMS, ±5%, .25W, R40, 175, 196	
79	6	6		A		7550001P085	RES, 3.3K OHMS, ±5%, .25W, R42-47	
80	2	2				RL20S301G	RES, 300 OHMS, ±2%, .50W, R49, 72	
81	2	2				RLR07C8061FM	RES, 8.06K OHMS, ±1%, .25W, R52, 75	
82	2	2				RLR07C1622FM	RES, 16.2K OHMS, ±1%, .25W, R53, 76	
83	2	2				RLR07C3162FM	RES, 31.6K OHMS, ±1%, .25W, R54, 77	

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SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV B SHEET 5

PARTS LIST

ITEM NO.	QTY PER ASSY G1	QTY PER ASSY G2	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
84	2	2				RLR07C6342FM	RES, 63.4K OHMS, ±1%, .25W, R55, 78	
85	2	2				RLR07C1273FM	RES, 127K OHMS, ±1%, .25W, R56, 79	
86	2	2				RLR07C2553FM	RES, 255K OHMS, ±1%, .25W, R57, 80	
87	2	2		A		7550001P138	RES, 510K OHMS, ±5%, .25W, R58, 81	
88	6	6		A		7550001P145	RES, 1MEG OHMS, ±5%, .25W, R59, 82 176, 184, 197, 207	
89	2	2		A		7550001P152	RES, 2MEG OHMS, ±5%, .25W, R60, 83	
90	2	2		A		7550001P159	RES, 3.9MEG OHMS, ±5%, .25W, R61, 84	
91	1	1		A		7550001P046	RES, 75 OHMS, ±5%, .25W, R85	
92	6	6		A		7550001P025	RES, 10 OHMS, ±5%, .25W, R88, 173, 181 191, 202, 212	
93	5	5				RLR07C5621FM	RES, 5.62K OHMS, ±1%, .25W, R89, 97, 114, 132, 150	
94	3	3		A		7558001P006	RES, VAR, 500 OHMS, ±20%, .50W, R90, 95, 131	
95	1	1				RLR07C2871FM	RES, 2.87K OHMS, ±1%, .25W, R91	
96	1	1		A		7550001P063	RES, 390 OHMS, ±5%, .25W, R92	
97	4	4				RLR07C1961FM	RES, 1.96K OHMS, ±1%, .25W, R93, 98 129, 136	
98	1	1				RLR07C3571FM	RES, 3.57K OHMS, ±1%, .25W, R94	
99	2	2				RLR07C3921FM	RES, 3.92K OHMS, ±1%, .25W, R96, 133	
100	4	4		A		7558001P011	RES, VAR, 20K OHMS, ±20%, .50W, R99, 135 192, 213	
101	2	2				RLR07C3242FM	RES, 32.4K OHMS, ±1%, .25W, R101, 139	
102	2	2				RLR07C2803FM	RES, 280K OHMS, ±1%, .25W, R102, 138	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.		
A	94117	PL	1086939

REV B | SHEET 6

PARTS LIST

ITEM NO.	QTY PER ASSY G1	QTY PER ASSY G2	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
103	2	2				RLR07C3652FM	RES, 36.5K OHMS, ±1%, .25W, R103, 141	
104	2	2				RLR07C1213FM	RES, 121K OHMS, ±1%, .25W, R104, 140	
105	2	2				RLR07C3012FM	RES, 30.1K OHMS, ±1%, .25W, R105, 143	
106	2	2				RLR07C5492FM	RES, 54.9K OHMS, ±1%, .25W, R106, 142	
107	2	2				RLR07C2612FM	RES, 26.1K OHMS, ±1%, .25W, R107, 145	
108	2	2				RLR07C2942FM	RES, 29.4K OHMS, ±1%, .25W, R108, 144	
109	2	2				RLR07C2262FM	RES, 22.6K OHMS, ±1%, .25W, R109, 147	
110	2	2				RLR07C1692FM	RES, 16.9K OHMS, ±1%, .25W, R110, 146	
111	4	4				RLR07C1962FM	RES, 19.6K OHMS, ±1%, .25W, R100, 111, 137, 149	
112	2	2				RLR07C1002FM	RES, 10K OHMS, ±1%, .25W, R112, 148	
113	2	2				RLR07C1652FM	RES, 16.5K OHMS, ±1%, .25W, R113, 151	
114	2	2				RLR07C1272FM	RES, 12.7K OHMS, ±1%, .25W, R115, 153	
115	2	2				RLR07C2941FM	RES, 2.94K OHMS, ±1%, .25W, R116, 152	
116	2	2				RLR07C8251FM	RES, 8.25K OHMS, ±1%, .25W, R117, 155	
117	2	2				RLR07C1271FM	RES, 1.27K OHMS, ±1%, .25W, R118, 154	
118	2	2				RLR07C3091FM	RES, 3.09K OHMS, ±1%, .25W, R119, 157	
119	2	2				RLR07C3320FM	RES, 332 OHMS, ±1%, .25W, R120, 156	
120	2	2				RLR07C2320FM	RES, 232 OHMS, ±1%, .25W, R121, 159	
121	2	2		A		7558001P004	RES, VAR, 100 OHMS, ±20%, .50W, R122, 158	
122	1	1				RLR07C7150FM	RES, 715 OHMS, ±1%, .25W, R123	
123	1	1		A		7558001P003	RES, VAR, 50 OHMS, ±20%, .50W, R124	
124	1	1				RC20GF391J	RES, 390 OHMS, ±5%, .50W, R126	
125	1	1		A		7558001P002	RES, VAR, 20 OHMS, ±20%, .50W, R127	

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SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV B | SHEET 7

PARTS LIST

ITEM NO.	QTY PER ASSY G1	G2	G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
126	1	1				RLR07C3010FM	RES, 301 OHMS, ±1%, .25W, R128	
127	1	1				RLR07C5111FM	RES, 5.11K OHMS, ±1%, .25W, R130	
128								
129	1	1				RLR07C1212FM	RES, 12.1K OHMS, ±1%, .25W, R216	
130	2	2		A		7558001P010	RES, VAR, 10K OHMS, ±20%, .50W, R160, 166	
131	1	1				RLR07C3092FM	RES, 30.9K OHMS, ±1%, .25W, R161	
132	2	2				RLR07C1502FM	RES, 15K OHMS, ±1%, .25W, R162, 169	
133	5	5				RLR07C2430FM	RES, 243 OHMS, ±1%, .25W, R125, 163 164, 167, 168	
134	2	2		A		7550001P113	RES, 47K OHMS, ±5%, .25W, R165, 170	
135	2	2		A		7550001P088	RES, 4.3K OHMS, ±5%, .25W, R178, 199	
136	2	2				RLR07C1471FM	RES, 1.47K OHMS, ±1%, .25W, R179, 200	
137	2	2		A		7558001P009	RES, VAR, 5K OHMS, ±20%, .50W, R187, 205	
138	2	2				RLR07C4641FM	RES, 4.64K OHMS, ±1%, .25W, R188, 206	
139	2	2		A		7550001P096	RES, 9.1K OHMS, ±5%, .25W, R189, 210	
140	4	4		A		7550004P057	RES, 220 OHMS, ±5%, .50W, R193, 194, 214, 215	
141	—	2				RC07GF153J	RES, 15K OHMS, ±5%, .25W, R11, 16	
142								
143	54	54		A		7538002P017	DIODE, IN4148, CR1-46, 73-76, 79-82	
144	22	22				IN5712	DIODE, CR47-68	
145	6	6		A		7012776P001	DIODE, HPA-5082-2800, CR69-72, 77, 78	
146								
147								

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV B | SHEET 3

PARTS LIST

ITEM NO.	QTY PER ASSY G1	G2	G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
148	2	2		A		7538002P102	DIODE, IN751-A, 5.1V, VR6,8	
149	1	1		A		7538002P011	DIODE, IN752-A, 5.6V, VR1	
150	2	2		A		7538002P036	DIODE, IN754-A, 6.8V, VR3,4	
151	1	1		A		7538002P013	DIODE, IN756-A, 8.2V, VR2	
152	2	2		A		7538002P057	DIODE, IN758-A, 10V, VR7,9	
153	1	1				SES-157	DIODE, 5.1V, ±1%, VR5 (SEMTEX)	
154								
155	5	5		A		7610001P084	TRANSISTOR, 2N2222-A, NPN, Q28,30,32,38,44	
156	15	15		A		7610001P057	TRANSISTOR, 2N2369-A, NPN, Q1,3,5,7,9,11 13,15,17,19,21,23,25,33,39	
157	5	5		A		7610001P046	TRANSISTOR, 2N2907-A, PNP, Q27,29,31,34,41	
158	15	15		A		7610001P038	TRANSISTOR, 2N4209, PNP, Q2,4,6,8,10,12 14,16,18,20,22,24,26,36,42	
159	2	2		A		7610011P003	TRANSISTOR, MD-918, DUAL PNP, Q35,40	
160	2	2		A		7610011P004	TRANSISTOR, MD-5000, DUAL PNP, Q37,43	
161								
162	1	1		A		7518001P078	COIL, 22 µH, ±10%, L1	
163	5	5		A		7518001P086	COIL, 100 µH, ±10%, L2-6	
164								
165								
167	1	1		A	00222	HM40	DELAY LINE, 40NS (HM-40) DL2 (ESC)	
168	1	1		A		7518003P002	DELAY LINE, 20NS (HM-20) DL1	
169								

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
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SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV B | SHEET 9

PARTS LIST

ITEM NO.	QTY PER ASSY G1	QTY PER ASSY G2	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
170	40	40		A		640048P1	WAFER, THERMAL CONDUCTING	
171	2	2		A		640049P1	WAFER, THERMAL CONDUCTING	
172	3	3		A		640085P1	WAFER, THERMAL CONDUCTING	
173	12	12		A		640085P2	WAFER THERMAL CONDUCTING	
174	12	12		A		165046P1	TEST POINT, TP1-12	
175	2	2			53894	#175	HEATSINK (AHAM)	
176	6"	6"		A		278000P13	WIRE, ELEC, 22 AWG	
177	6"	6"		A		270006P5	TUBING, INSUL, TEFLON	
178	AR	AR		A		93002P1	SOLDER	
179								
180								
181	REF	REF		A		815003	PWB, REQ FOR	
182	REF	REF		E		1086941	LOGIC DIAGRAM	
183	REF	REF		A		778000	APPL OF EPOXY MARKING CMPD	
184	1	1		A		7506001P033	CAP, 180PF ±5%, 500V, C4	
185	1	1		A		7506001P037	CAP, 270PF ±5%, 500V, C5	
186	1	1		D		1086608P18	CONNECTOR, ELEC.	
187	2	2			07707	6010	EYELET	
188	2	2		A		600107P1	CARD EJECTOR	
189	2	2		A		630003P14	EYELET	
190	—	2		A		7550001P094	RES, 7.5K, ± 5%, .25W, R183, 204	

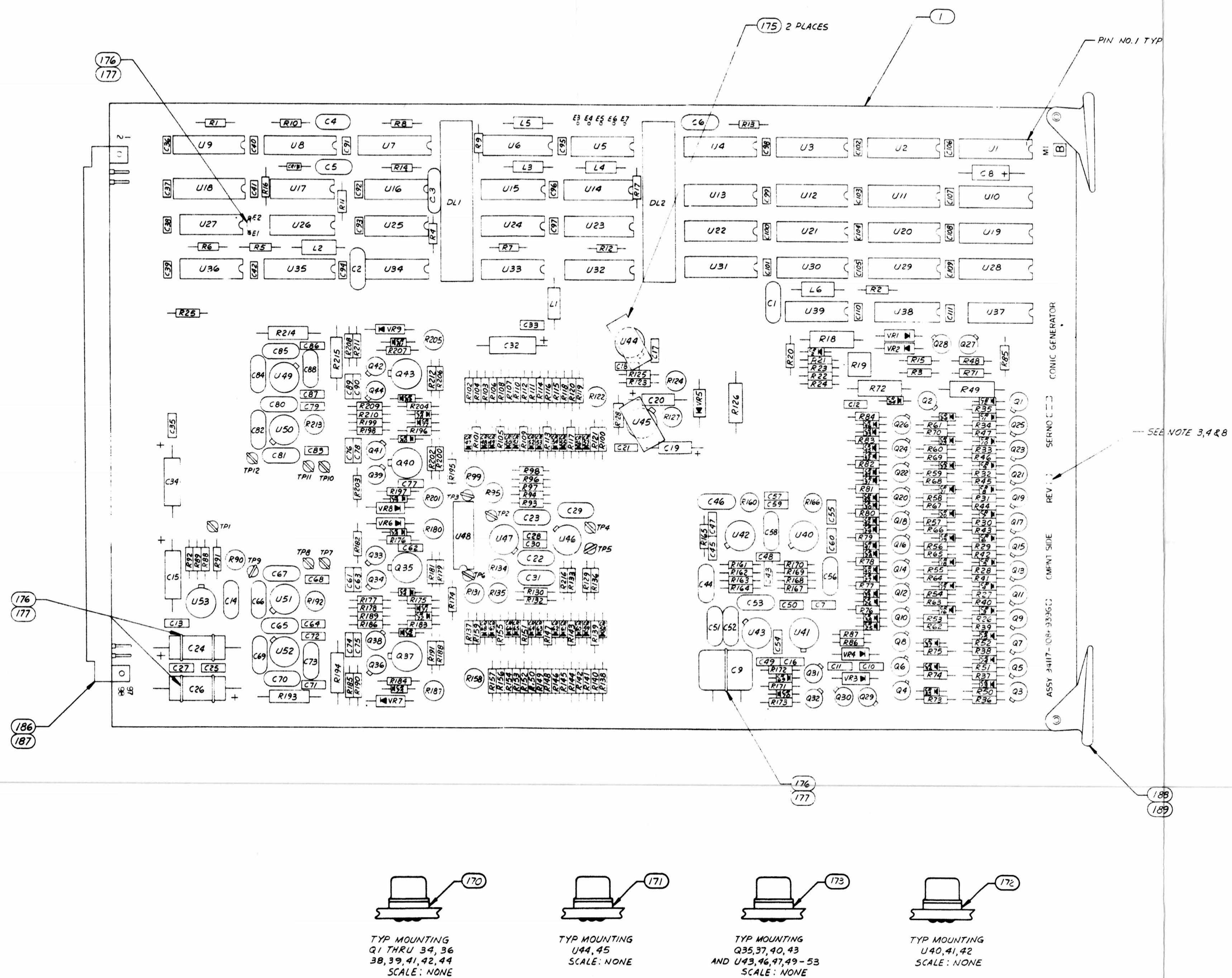
SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1086939

REV E | SHEET 10

OP—277 REV C

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	—	REL FOR PREPROD	18 AUG 77	WG/REG
	A	REV PER ECO 76163	10 MAY 78	RD/RWB
	B	REV PER ECO 76237	27 OCT 78	WG/RLB
	C	REV PER ECO 76387	7 JUN 79	WG/WL
	D	REV PER ECO 76411	3 JUL 79	WG/WL



JUMPER TABLE	
1086939G2 ONLY	
CUT	ADD
E5 TO E6	E5 TO E7

(G1) **FOR PARTS LIST** SEE PL 1086939

(G2) SEE JUMPER TABLE

8. MARK SER NO., G CONDITION AND REV AT FINAL ASSEMBLY.
7. SOLDER TIPS OR WIRE TO BE .09 MAX FROM BOARD
6. MAX COMPONENT HEIGHT TO BE .44
5. OTHER THAN SPECIFICALLY NOTED, CHARACTERS ARE REFERENCE AND NOT TO BE MARKED.
4. MARK CHARACTERS .04-.16 HIGH, IN ACCORDANCE WITH MIL-STD-130.
3. PARTS LIST SHEET ONE IS THE CONTROLLING REVISION FOR THE COMBINED PARTS LIST AND DRAWING.
2. THIS ASSY SHALL MEET THE REQUIREMENTS OF ITEM 181.
1. SHOP TOLERANCES AND DRAWING INTERPRETATION WITHIN S15002 SUPPLEMENT THIS DRAWING.

NOTES UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON
1086851	GRA-7
APPLICATION	

QTY PER ASSY (G6 G5 G4 G3 G2 G1) | ITEM | SIZE | PART OR IDENTIFYING NO. | DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .XX DECIMAL ± — .XXX DECIMAL ± — ANGLES ± —

PREPROD CHANGE BY ECO ONLY

MFG K Smith 9/6/77

CONT NO.

DRFTG DR W. Gurowski 8 JUL 77 · APPD · CHK

ENGRG DEV R. Grant 9-1-77 · E&M · PROJ J. E. Kelley 9-6-77

SANDERS ASSOCIATES, INC NASHUA, NEW HAMPSHIRE

CIRCUIT CARD ASSY, RAMP/CONIC GEN

SIZE E | CODE IDENT NO. 94117 | DWG NO. 1086939

SCALE 2/1 | SHEET 1 OF 1

DO NOT SCALE PRINT

1086939

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	—	REL FOR PREPROD	18AUG77	NG/REQ
	A	REV PER ECO 76110	22 SEP 77	NG/RJB
	B	REV PER ECO 76237	27 OCT 78	NG/RJB
	C	REV PER ECO 76268	3 JUL 79	NG/WL
	D			

REVISION STATUS OF SHEETS						
SHEET	1	2	3	4	5	X
REVISION	D	C	D	D	A	X

A CLAMP COMPARATOR

+15V, R161 30.9K ±1%, R165 4.7K, C46 10, +15V
A CLAMP ADJ: R160 10K ±20% 1/2W CW, C43 .01UF ±10% 100V, -15V
R162 15K ±1%, C45 .01UF ±10% 100V, +5A, C47 .01UF ±10% 100V
R163 243 ±1%, C44 1±.5, U42 LM2611H, ACLP- SH 4
R164 243 ±1%, C48 .01UF ±10% 100V, -15V

SH 3 AB +5 REF

LIMITER STAGES, 1 & 2

+5A, +15V, U48 DG190: VL, Vcc, VR, VEE, D1–D4, S1–S4, IN1, IN2
AC SH 2 SINE — 1% U17-6
AF SH 4
AD SH 2 COSINE
SH 3 AA RAMP
AE SH 2

Q31 2N2907A, R171 47, C49 .01UF ±10% 100V, CR69 HPA5082-2800
R172 1K, CR70 HPA5082-2800, R173 10, Q32 2N2222
+15V, C50 .01UF ±10% 100V, C51 100, U43 HA2525-5, C52 1±.5, C53 100, C54 .01UF ±10% 100V, -15V

R170 47K, C58 10, +15V, +5A, C57 .01UF ±10% 100V, C59 .01UF ±10% 100V
R167 243 ±1%, C56 1±.5, R168 243 ±1%, C55 .01UF ±10%, 100V, R169 15K ±1%
U40 LM2611H, C60 .01UF ±10% 100V, -15V
R166 10K ±20% 1/2W CW, +15V, -15V
BCLP- SH 4

THIRD STAGE LIMITER

+15V, Q33 2N2369A, C61 .01UF ±10% 100V, R177 3K, R178 4.5K, Q34 2N2907A, C63 .01UF ±10% 100V, VR6 IN751A 5.1V
R176 1MEG, CR73, CR74, Q35 MD918, R182 1K
CR71 HPA5082-2800, R175 2.7K, C62 .01UF ±10% 100V, R181 10, +RAMP LIMIT
R179 1.47K ±1%, R180 1K ±20% 1/2W CW, TP7, TP8
CR72 HP5082-2800, R174 510, PRE RAMP R191 10
+15V, R187 5K ±20% 1/2W CW, -RAMP LIMIT, R188 4.64K ±1%, R183 7.5K
Q36 2N4209, R184 1MEG, CR75, CR76, Q37 MD5000, Q38 2N2222A
R185 3K, R186 3K, -15V, R189 9.1K, VR7 IN753A 6.2V, C75 .01UF ±10% 100V, R190 510

X AXIS DRIVER

+15V, C64 .01UF ±10% 100V, C65 100, R192 20K ±20% 1/2W CW, U51 HA2525-5, C66 10, C67 100, C68 .01UF ±10% 100V, -15V
C69 10, C72 .01UF ±10% 100V, U52, C73 100, R194 220 1/2W, -15V
+15V, R193 220 1/2W, C70 100, C71 .01UF ±10% 100V, LH0002, TP9
P/O J1, 79 RMPX+E

THIRD STAGE LIMITER

+15V, Q39 2N2369A, C76 .01UF ±10% 100V, R198 3K, R199 4.3K, Q41 2N2907A, C78 .01UF ±10% 100V, VR8 IN751A 5.1V
R197 1MEG, CR79, CR80, Q40 MD918, R203 1K
CR77 HPA5082-2800, R196 2.7K, C77 .01UF ±10% 100V, R202 10
R200 1.47K ±1%, R201 1K ±20% 1/2W CW, TP10, TP11
CR78 HP5082-2800, R195 510, PRE RAMP R212 10
+15V, R205 5K ±20% 1/2W CW, R206 4.64K ±1%, R204 7.5K
Q42 2N4209, R207 1MEG, CR81, CR82, Q43 MD5000, Q44 2N2222A
R208 3K, R209 3K, -15V, R210 9.1K, VR9 IN753A 6.2V, C90 .01UF ±10% 100V, R211 510

Y AXIS DRIVER

+15V, C79 .01UF ±10% 100V, C80 100, R213 20K ±20% 1/2W CW, U50 HA2525-5, C81 100, C82 10, C83 .01UF ±10% 100V, -15V
C84 10, C87 .01UF ±10% 100V, U49, C88 100, R215 220 1/2W, -15V
+15V, R214 220 1/2W, C85 100, C86 .01UF ±10% 100V, LH0002, TP12
80 RMPY+E

7. FOR 1086939G2 CUT E6 TO E5
JUMPER E5 TO E7.
FOR 1086939G1 USE AS IS.
6. FOR 1086939G1: C16 = .027UF, ±10%, 50V
R11 = 120K
R16 = 7.5K
FOR 1086939G2: C16 = 1500 PF, ±10%, 200V
R11 = 15K
R16 = 15K
5. ANALOG GND DESIGNATED BY SYMBOL ⏚△.
DIGITAL GND DESIGNATED BY SYMBOL ⏚△.
4. UNLESS OTHERWISE SPECIFIED
DIODES ARE 1N4148.
3. PREFIX PARTIAL REFERENCE DESIGNATIONS WITH
2. UNLESS OTHERWISE SPECIFIED
RESISTANCE VALUES ARE IN OHMS
RESISTORS ARE ± 5 %, 1/4 W
K=1,000
MEG=1,000,000
CAPACITANCE VALUES ARE IN PICOFARADS
CAPACITORS ARE ± 5 %, 500V
UF=MICROFARADS
INDUCTANCE VALUES ARE IN MICROHENRIES
1. INTERPRET DRAWING PER 815002

NOTES

REFERENCE DATA		
DESCRIPTION	LAST NO.	DELETED NO.
RESISTOR	216	
CAPACITOR	C111	
DIODE	CR83/VR3	
TRANSISTOR	Q44	
INDUCTOR		
MICROELEMENT	U53	
WIRING DIAGRAM		

PREPROD — CHANGE TO ECO ONLY
DRN 9/6/77
1086939 — NEXT ASSY
1086851 — USED ON
APPLICATION

CONT NO.
DESIGN R. Logan JUNE 77
CHK
DEV R. Grant 9-1-77
ENG Roy Talley 9.6.77

SANDERS ASSOCIATES, INC. NASHUA, NEW HAMPSHIRE

LOGIC DIAGRAM
RAMP/CONIC GEN.

SIZE E | CODE IDENT NO. 94117 | DWG NO. 1086941
SCALE | SHEET 1 OF 5
DO NOT SCALE PRINT

1086941

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	—	REL FOR PREPROD	18AUG77	MG/RLB
	A	REV PER ECO 76110	7th NOV 77	MG/RLB
	B	REV PER ECO 76237	27 OCT 78	MG/PMD
	C	REV PER ECO 76268		

C28 .01UF ±10% 100V
C29 100
+15V
HA 2525-5
U47
R93 1.96K ±1%
R96 3.92K ±1%
R97 5.62K ±1%
R98 1.96K ±1%
TP2
TP3
R94 3.57K ±1%
R99 20K ±20% 1/2W 3 CW
C22 1±.5
R95 500 ±20% 1/2W 3 CW
C30 .01UF ±10% 100V
C31 100
-15V
+V REF
GND REF
C17 .1UF ±10% 50V
U44 LM317-H
R123 715 ±1%
R124 50 ±20% 1/2W 3 CW
R125 243 ±1%
C18 .1UF ±10% 50V
R100 19.6K ±1%
R101 32.4K ±1%
R102 280K ±1%
R103 36.5K ±1%
R104 121K ±1%
R105 30.1K ±1%
R106 54.9K ±1%
R107 26.1K ±1%
R108 29.4K ±1%
R109 22.6K ±1%
R110 16.9K ±1%
R111 19.6K ±1%
R112 10K ±1%
R113 16.5K ±1%
R114 5.62K ±1%
R115 12.7K ±1%
R116 2.94K ±1%
R117 8.25K ±1%
R118 1.27K ±1%
R119 3.09K ±1%
R120 332 ±1%
R121 2.32 ±1%
R122 100 ±20% 1/2W 3 CW
CR47 IN5712
CR48 IN5712
CR49 IN5712
CR50 IN5712
CR51 IN5712
CR52 IN5712
CR53 IN5712
CR54 IN5712
CR55 IN5712
CR56 IN5712
CR57 IN5712
R138 280K ±1%
R139 32.4K ±1%
R140 121K ±1%
R141 36.5K ±1%
R142 54.9K ±1%
R143 30.1K ±1%
R144 29.4K ±1%
R145 26.1K ±1%
R146 16.9K ±1%
R147 22.6K ±1%
R148 10K ±1%
R149 19.6K ±1%
R150 5.62K ±1%
R151 16.5K ±1%
R152 2.94K ±1%
R153 12.7K ±1%
R154 1.27K ±1%
R155 8.25K ±1%
R156 332 ±1%
R157 3.09K ±1%
R158 100 ±20% 1/2W 2 CW
R159 2.32 ±1%
CR58 IN5712
CR59 IN5712
CR60 IN5712
CR61 IN5712
CR62 IN5712
CR63 IN5712
CR64 IN5712
CR65 IN5712
CR66 IN5712
CR67 IN5712
CR68 IN5712
TP6
SINE AC SH 1
COSINE AD SH 1
+15V
R126 390 ±5% 1/2W VR5 SES-157 5.1V
R127 20 2 CW
C20 1UF ±20%, 50V
R128 301 ±1%
TP4
U45 LM220H-5.0
C21 1UF +80% -20% 50V
C19 1UF ±20% 50V
-15V
AE SH 1
R129 1.96K ±1%
+15V
HA2525-5
U46
TP5
R136 1.96K ±1%
C23 1±.5
R134 1K ±20% 1/2W CW 1
R216 12.1K ±1%
R132 5.62K ±1%
R133 3.92K ±1%
R130 5.11K ±1%
R131 500 ±20% 1/2W 3 CW
R135 20K ±20%, 1/2W 2 CW
R137 19.6K ±1%
-15V
L1 22
C32 39UF ±10% 10V
C33 .01UF ±10% 100V
C110 .01UF ±10% 100V
C111 .01UF ±10% 100V
PIN 14 → U37,38,39
+5A
PIN 7 → U38,39
P/O U1
P15V+ 95 96
N15V- 93 94
P05V+ 55 56 77 78
A RET SEE NOTE 5 97 98
D RET SEE NOTE 5 29 30 53 54
C24 22UF ±20% 35V
C25 .01UF ±10% 100V
C26 22UF ±20% 35V
C27 .01UF ±10%, 100V
+15V
-15V
C34 39UF ±10% 10V
C8 39UF ±10% 10V
PIN 5 → U5,6
C35 THRU C42, C91 THRU C109 .01UF ±10%, 100V
PIN 16 → U1,2,3,4,7 THRU U14, U18 THRU U23, U28 THRU 32, 35
PIN 14 → U15,16,17,24,25 26,27,33,34,36
+5D
PIN 8 → U1,2,3,4,7 THRU 14, 18 THRU 23, 28 THRU 32, 35
PIN 7 → U15,16,17, 24,25,26,27, 33,34,36
PIN 12 → U6,8,21
PIN 10 → U5

SPARES
S04 U24A
04 U25E
S03 U36D
HO1 U39A
02 U27C
UGD 75

PREPROD
SIZE E | CODE IDENT NO. 94117 | DWG NO. 1086941
SCALE NONE | SHEET 2 OF
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1086941

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	–	REL FOR PREPROD	18AUG77	JMG/REC
	D	REV PER ECO 76411	3JUL79	WG/WLP

899-1-1K

CURRENT DIVERTER SWITCHES

CONSTANT CURRENT GENERATOR

REFERENCE VOLTAGE REGULATOR

RAMP

PREPROD

SIZE	CODE IDENT NO.	DWG NO.
E	94117	1086941

SCALE

SHEET 3 OF

DO NOT SCALE PRINT

1086941

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	—	REL FOR PREPROD	18AUG77	NG/RLB
	A	REV PER ECO 76110	30NOV77	NG/RLB
	B	REV PER ECO 76237	27 OCT 78	NG/
	C	REV PER ECO 76268		KLB
	D	REV PER ECO 76411	3JUL79	NG/WL

P/O J1

VPST-G 48
VPIZ-G 38
VPS1+G 47
VPS2+G 46
OFLW-A 41
DBØ9-G 10
DBØ8-G 11
STOP-G 15
DBØ4-G 5
STDZ-G 14
DBØ3-G 4
STKX-G 13

+5A R2 510 L6 100 C1 100 TOGGLE SH3
+5A R3 1K
+5D R1 1K
U17B S74 PR CLR
U39B H01
U26B H00
U16 H53 R4 510
ACLP- SH1
BCLP- SH1
U24E S04
U33B S51
U39A S20 R7 510 DL1 GND R8 620
U34B S20 R9 510
U8A U8B 9602 C4 180 R10 10K C5 270 R11 SEE NOTE 6 CR1
L5 100 C3 51 R14 2K U15D 00
+5A R15 1K U39C H01 SH3 FAST
U35 6306-1J LYØ5+ LYØ6+ LYØ7+ LYØ8+ LYØ9+ LY10+ VROM SH 3
+5D R16 SEE NOTE 6 U36A S03 SPED- SH3
U15B 00 L3 100 C6 62 L4 100 R17 3K
U27B 02 U6C 75
U25B 04 U6B 75 U6A 75 U7 9321 Y15 U26A H00 U25C 04
U24A S04 U24B S04 U24C S04 U24D S04
U5 7493A R1 R2 CA CB QA QB QC QD E7 E4 E3 E6
U15C 00 DL2 GND R12 510 R13 620 UNBLANK
U27A 02 U15A 00 APDB
U26D H00 E1 E2
U39D H01
U18 U9 165 SIN SHLD CK CLK INH A B C D E F G H QH
U25E 04 SEE NOTE 7 U33A S51
U15 +5V R18 825 ±1% 1/2W CR2 R20 240 R19 1K ±20% 1/2W CW R21 4.02K ±1% R22 499Ω ±1% R23 1.0K ±1% R24 2.0K ±1% B C D E SHT 5
U17A S74 IP5 U39C 03 R25 1K AF SH 1
U25D 04

P/O J1
31 OVCK-E
32 TOGL-E
43 FBSY-X
44 VPBY+E
42 VPNL+E
33 VECZ+E
40 CIRL-K

LINE STRUCTURE LATCH / DECODE

PREPROD
CHANGE BY ECO ONLY

SIZE	CODE IDENT NO.	DWG NO.
E	94117	1086941

SCALE — SHEET 4 OF

DO NOT SCALE PRINT

1086941

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	–	REL FOR PREPROD	18AUG77	MK
	A	REV PER ECO 76237	27OCT78	MK

R CALCULATION

CONSTANT TIME DETECTION

SHORT VECTOR INTENSITY CONTROL

P/O J1

LXIØ+A 76
LXØ9+A 74
LXØ8+A 72
LXØ7+A 70
LXØ6+A 68
LXØ5+A 66
LXØ4+A 64
LXØ3+A 62
LXØ2+A 60
LXØ1+A 58
LXØØ+A 52
LY10+A 75
LYØ9+A 73
LYØ8+A 71
LYØ7+A 69
LYØ6+A 67
LYØ5+A 65
LYØ4+A 63
LYØ3+A 61
LYØ2+A 59
LYØ1+A 57
LYØØ+A 51
CARX+A 50
CARY+A 49

U12 283 · U13 283 · U14 283 · U21 283 · U22 283 · U23 283 · C4 · Co

U30 · U31 · U32 7485

U11 · U3 · U4 S158

U2 148

U28 · U19 · U10 · U20 G305-1

U38 37

U1 S158

RX11+ RX10+ RX09+ RX08+ RX07+ RX06+ RX05+ RX04+ RX03+ RX02+ RX01+ RX00+

RY11+ RY10+ RY09+ RY08+ RY07+ RY06+ RY05+ RY04+ RY03+ RY02+ RY01+ RY00+

YSEL+

RV11- RVIØ- RV09- RV08- RV07- RV06- RV05- RV04- RV03- RV02- RV01- RVØØ-

RV11/3+ RV10/2+ RV9/1+ RV8/Ø+ RV07- RV06- RV05- RV04-

I11- I1Ø- I9- I8- I7- I6- I5- I4- I3- I2- I1- IØ-

F G H J K L M N P R S T

SH3

Z3+ Z2+ Z1+ ZØ+

B C D E

SH4

VROM SH4 U24F S04

1086941

PREPROD	SIZE E	CODE IDENT NO. 94117	DWG NO. 1086941
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Model 5752 2-D Coordinate Converter Technical Manual (H-78-0061)

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