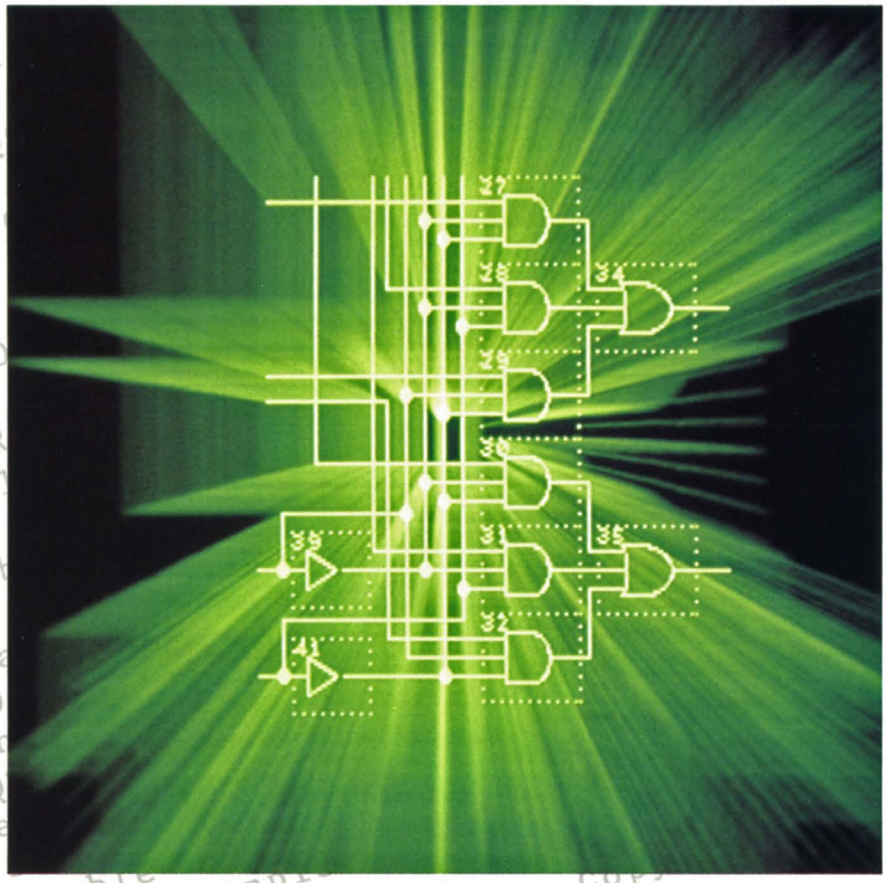
DASH-ABEL INTERFACE



LINKING SCHEMATIC CAPTURE AND PROGRAMMABLE LOGIC DESIGN.

DATA I/O

DASH-ABEL: CREATE PLD DESIGNS USING SCHEMATIC CAPTURE.

DASH-ABEL™ Interface links two powerful software tools, FutureNet's DASH™ PC Schematic Capture System and Data I/O®'s ABEL™ programmable logic design tool. These software programs allow you to describe logic functions by graphically arranging discrete or generic logic elements on a PC and automatically translating your design into programmable logic using ABEL. In ABEL, it is optimized and translated into a logic programmer-readable syntax. While DASH and ABEL can function as standalone design tools, the DASH-ABEL Interface assimilates the power of each for even greater design flexibility.

Because DASH-ABEL takes full advantage of ABEL's natural design language, it allows you to express your designs in any combination of schematics, Boolean equations, truth tables or state diagrams. You can design one segment of a logic circuit as a schematic and another in the ABEL language.

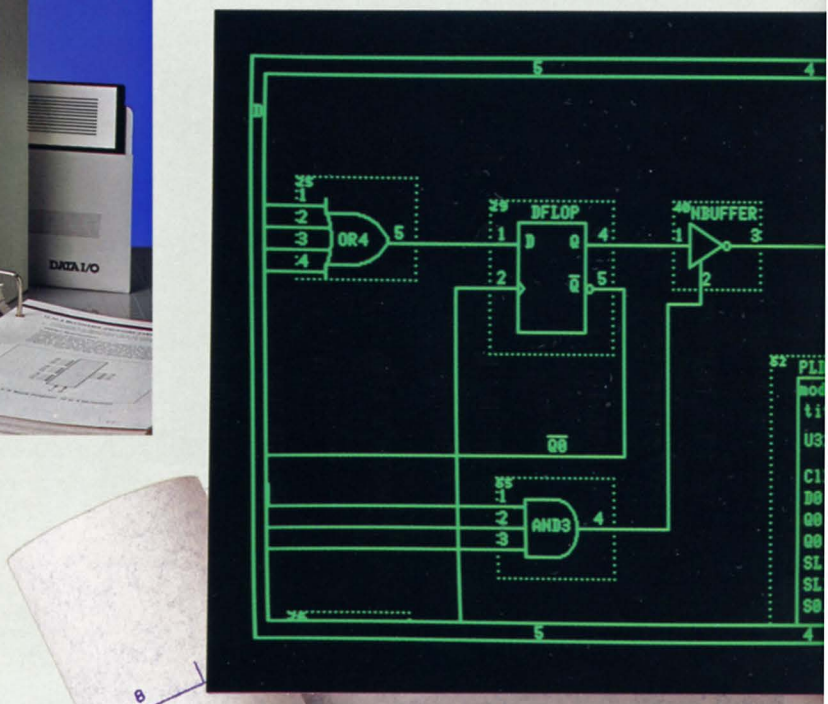
SCHEMATIC ENTRY: A NEW WAY TO CAPTURE PLD DESIGNS. Developed by FutureNet, DASH-1™ and enhanced DASH-2™ schematic entry packages integrate the personal computer with graphics processing to create the first personal computer workstation for board-level and chip-level system design. They virtually eliminate manual drafting by allowing the design engineer to create new schematics or change existing drawings directly on an IBM® PC, XT or AT.

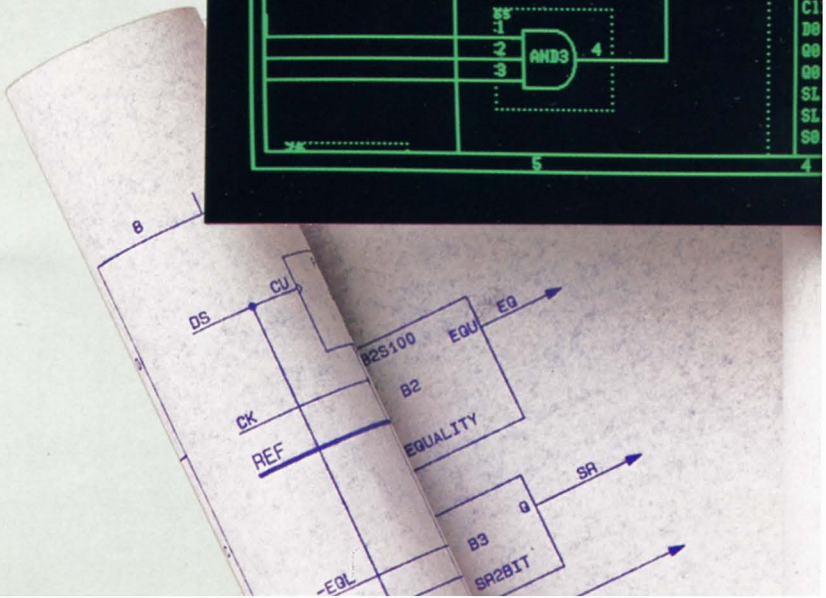
ABEL: THE POWERFUL HIGH-LEVEL LOGIC DESIGN TOOL. Data I/O's Advanced Boolean Expression Language (ABEL) compiles logic designs for virtually any programmable logic device (PLD), including PAL®s, PROMs, FPLAs, FPLSs and PLEs. It lets you express your design in any combination of truth tables, state diagrams or Boolean equations—whatever works best for you.

In ABEL, simulation is an integral aspect of the design process. You can write functional test vectors to verify your design in the same source file and syntax as the design itself. With the interactive simulation loop, you can create segments of a design, write test vectors and debug the design.

ABEL minimizes design effort and maximizes design flexibility. For example, set nota-

DASH-ABEL links DASH Schematic Entry Series with ABEL, a high-level logic design tool, to provide a comprehensive logic development workstation for implementing schematics in programmable logic.





tion lets you group signals together and treat each set as a unit in your design description. ABEL's powerful logic-reduction algorithm reduces the number of product terms for a given logic function. And ABEL produces files in standard formats, which can be downloaded directly into any logic programmer.

THE AUTOMATED DESIGN PROCESS.

THE CREATION OF THE CIRCUIT. Conceptualize your circuit design using schematic capture by selecting standard TTL devices from the DASH parts library or generic logic symbols from DASH-ABEL. By entering a few simple commands, you can move or delete components and modify or replicate the circuit.

Using ABEL's high-level syntax, you can create design test vectors for design verification during this stage.

THE CONVERSION TO BOOLEAN EQUATIONS. When you have finalized your circuit, identify the inputs and outputs of the schematic portions to be converted into programmable logic and create an ABEL "text box" for those segments. The text box includes your PLD selection and pin declarations.

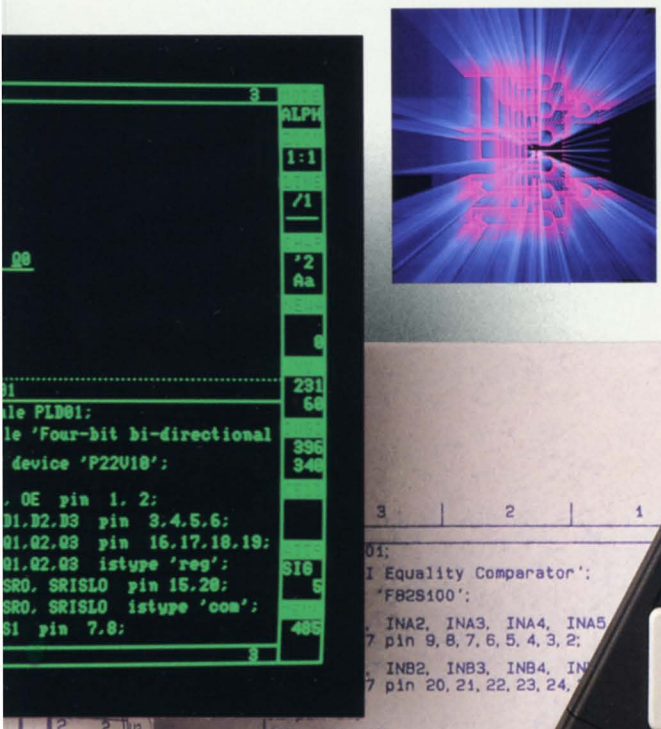
DASH-ABEL then automatically extracts the selected segments and translates them into an ABEL source file directly from the DASH output file. Target PLDs and schematic sections can be easily changed.

PROCESSING THE DESIGN. You can now use ABEL to translate the source file into a fusemap. After all circuit functions entered with DASH have been converted to Boolean equations, ABEL's language processor quickly performs the tedious logic reduction and error checking chores.

By using the test vectors you have created during design, ABEL can simulate operation and verify that the device will function properly before actual programming takes place. As a final step, it automatically creates documentation describing your design. This includes a full list of the reduced equations, a record of test vectors, a fusemap and a chip diagram showing the names of the input and output pins. You are now ready to download the fusemaps and test vectors into your logic programmer.

THE COMPLETE LOGIC DEVELOPMENT ENVIRONMENT.

Data I/O offers a comprehensive logic development environment which allows you to capture the power of even the most complex PLDs. Tailored to your individual requirements, a complete programmable logic workstation could include an IBM XT, ABEL, DASH-2, DASH-ABEL Interface, PROMlink™ (optional programmer and file handler software) and a model 60 Logic Programmer. To discover how our logic development environment replaces the need for expensive and cumbersome computer-aided engineering systems, contact your local sales engineer for ordering information.



DASH-ABEL allows design engineers to express the design of PLDs in the same schematic form as the entire circuit.

SOFTWARE UPDATE SERVICE. Joining Data I/O's Software Update Services assures you of prompt software updates for new devices and enhancements.

Data I/O has sales and sales representative offices worldwide to answer your questions or problems.

GENERAL SPECIFICATIONS

COMPATIBLE COMPUTERS: Personal computer (distributed on double-sided, double-density 5-1/4" floppies).
MS™-DOS or PC-DOS operating systems.
256k or larger memory.
Requires FutureNet's DASH Schematic Capture Package and Data I/O's ABEL for operation.

DEVICES SUPPORTED: Most 20- and 24-pin PALs, 40- and 84-pin PALs.
All IFLs: FPLS and FPGA.
Most popular logic PROMs.

DASH: DASH Schematic Capture eliminates manual drafting by allowing the design engineer to create new schematics or change existing drawings directly on an IBM PC, XT or AT.

ABEL: ABEL compiles logic designs for virtually all PLDs, including PALs, PROMs, FPLAs, FPLSs and PLEs. It also lets you express your design in any combination of truth tables, state diagrams or Boolean equations. ABEL is also available for VAX™ and VALID™ systems.

PLDtest: Data I/O's PLDtest dramatically reduces test vector generation time from days to just minutes, and assures faithful reproduction of your PLD design. It also provides fault grading to help engineers build testability into their PLD designs.

PROMlink: With Data I/O's PROMlink software driver, you can operate Data I/O's programmers from an IBM PC. This software package delivers the simplicity of a menu-driven operation and data file management.
Call your nearest Data I/O sales office or representative for more information about any of our logic development software tools.

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