DOLCH
LOGIC INSTRUMENTS

OPERATOR'S MANUAL FOR

300 MHz HIGH SPEED
(BURST) MEMORY OPTION

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CHANGES TO THIS MANUAL

This manual will be changed periodically to keep it current with improvements as we make them. Changes start with Service Notes that alert field service technicians to critical problem areas and changes in maintenance procedures. After a series of these notes are issued or a critical one is issued, we will publish change pages. which are the remove-the-old and insert-the-new type. When the company prepares a change package. It sends announcements to its users. The change packages are available upon request and without charge.

Record of Changes

The record of Changed Pages lists all the pages in this book. that are deleted. changed pages, added pages, and foldout pages.

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

Dolch Logic Analyzers are designed around 16 channel recording blocks called Data Acquisition Blocks (DABs). In some earlier documentation, these are called Single Board Logic Analyzers (SBLAs). Various interfaces and control configurations are built-in, and optional functions such as this one, are also available as firmware plug-ins.

Please refer to the Operator's manual of the host Logic Analyzer in which the 300 MHz option is installed for details of the Analyzer operation.

1.2 300 MHz HSM OPTION DESCRIPTION

The 300 MHz HSM is a 16 channel Logic Analyzer module providing high resolution timing data that is collected two different ways, depending on model and configuration. In the LAM 4850A and LAM 3250A it is "overlayed" on input groups A&B. However in the 64300 model series these inputs are assigned to a separate group, "a & b" (to differentiate them from the standard "A&B" TIMING DIAGRAM).

The 300 MHz HSM operates with an independent 300 MHz timebase clock and 512 word memory. Using its own cursor and set marker, timing measurements to 3.3 ns resolution are made. The 300 MHz HSM also features its own separate word search capability which can locate and identify any user defined, 16 bit word, and display the total number of times the word occurs in memory. As with the standard TIMING DIAGRAM, the resulting diagram can be expanded by a factor of 5 or 10. Channels can also be deleted or their display order can be changed on the keyboard.

1.3 REFERENCE DATA

Table 1-1 lists specifications for the 300 MHz HSM option.

Table 1-1. 300 MHz High Speed Memory Specifications		
SIGNAL INPUTS:	NUMBER	16
	IMPEDANCE	1 M Ohm/10pF at probe tip. (ALP 44H)
	THRESHOLD	Set by channel group A & B program
	MAXIMUM VOLTAGE	+/- 50 volts continuous; +/- 250 volts transient.
SAMPLING FUNCTIONS:	INTERNAL CLOCK	User programmable from 3.3 ns (300 MHZ) to 10 ms (100 Hz).
	EXTERNAL CLOCK	Not available with this option.
	TRIGGERING	Same as for host Analyzer, except that the recording window is centered on the final trigger occurrence.
	SKEW	+/- 1 bit channel-to-channel.
SOURCE MEMORY:	SIZE	16 bits by 512 words.
SEARCH FUNCTION:	WORD SEARCH	User definable 16 bit word that the Analyzer will search for and then locate in the 300 MHz memory. Search Word locations are identified by the cursor, and the total number of times the word occurs is displayed.

SECTION 2

INSTALLATION

2.1 GENERAL

The 300 MHz HSM option consists of hardware and software that are to be installed and tested at the factory.

2.2 INITIAL TURN-ON/CHECK-OUT

After power-up, the software directory should display:

9.4851 - 05 XX BURST MEMORY OPTION

("XX" is the software revision number.)

This message indicates that the option is operational.

SECTION 3

THEORY OF OPERATION

3.1 GENERAL

The 300 MHz HSM (also known as BURST MEMORY) provides the user with a higher speed sampling capability than is available with the normal recording mode. The independent timebase clock and 512 word memory of the 300 HSM is "overlayed" on the A & B memory block of the host Analyzer. On the 64300 model series, the memory is not overlayed, and is available for independent use.

3.2 OVERALL BLOCK DIAGRAM

Refer to Section 3, Functional Description/ Theory Of Operation of the host Analyzer's Operator's Manual for a description of the hardware interactions. Imagine the 300 MHz HSM as being inserted into the host Analyzer's overall block diagram. Figure 3-1 shows the configuration. Figure 3-2 shows a diagram of the connections between the LAM 4850A and the 300 MHz HSM, and the 64300 and the 300 MHz HSM. An external bridge adaptor is supplied with the 300 MHz HSM when it is installed in the 64300. This allows the 64300 to function in the same way as the LAM 4850A, tieing the 300 MHz HSM inputs to the selected pod group. Both, the 64300 and LAM 4850A use the DAB memory of pod groups E & F.

Triggering of the 300 MHz HSM is accomplished by the TRIG OUT B signal (indicating the final trigger event), which is also available at the rear panel of the Analyzer. After the TRIG OUT B signal goes active, the 300 MHz HSM is stopped with a delay so that the trigger word can be located between memory locations 0 and 256 of the display.

The delay, which follows after the TRIG OUT B signal, is dependent upon the number of trigger sequences. This delay is automatically compensated for in the Analyzer. Therefore, the trigger is always at the last ADVANCE trigger word. See Figure 3-3.

A dotted line showing the center of the 300 MHz HSM display is always shown when it is called. Because the TRIG OUT B point is near the center of the 300 MHz Memory, the actual trigger word is located somewhere to the left of the dotted line. The actual location depends on the ratio of the 300 MHz HSM clock interval to the internal sample clock interval. This ratio is automatically determined and limited by the software. When external clocks are used, the programmed internal range will also be limited. Note that the trigger word location can also be affected by which level in a sequence the last ADVANCE condition was programmed.

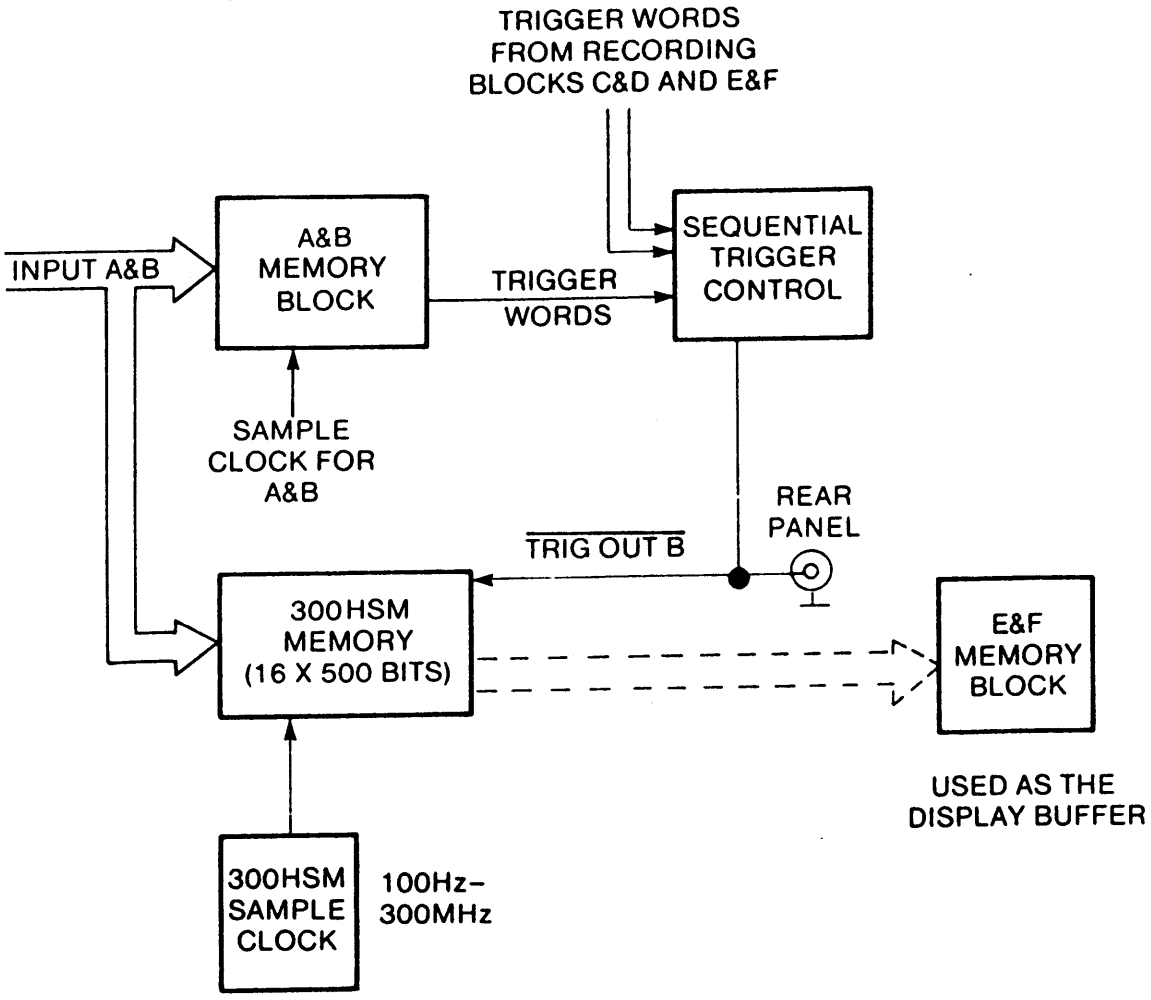

Figure 3-1. 300 MHz HSM/Analyzer Block Diagram

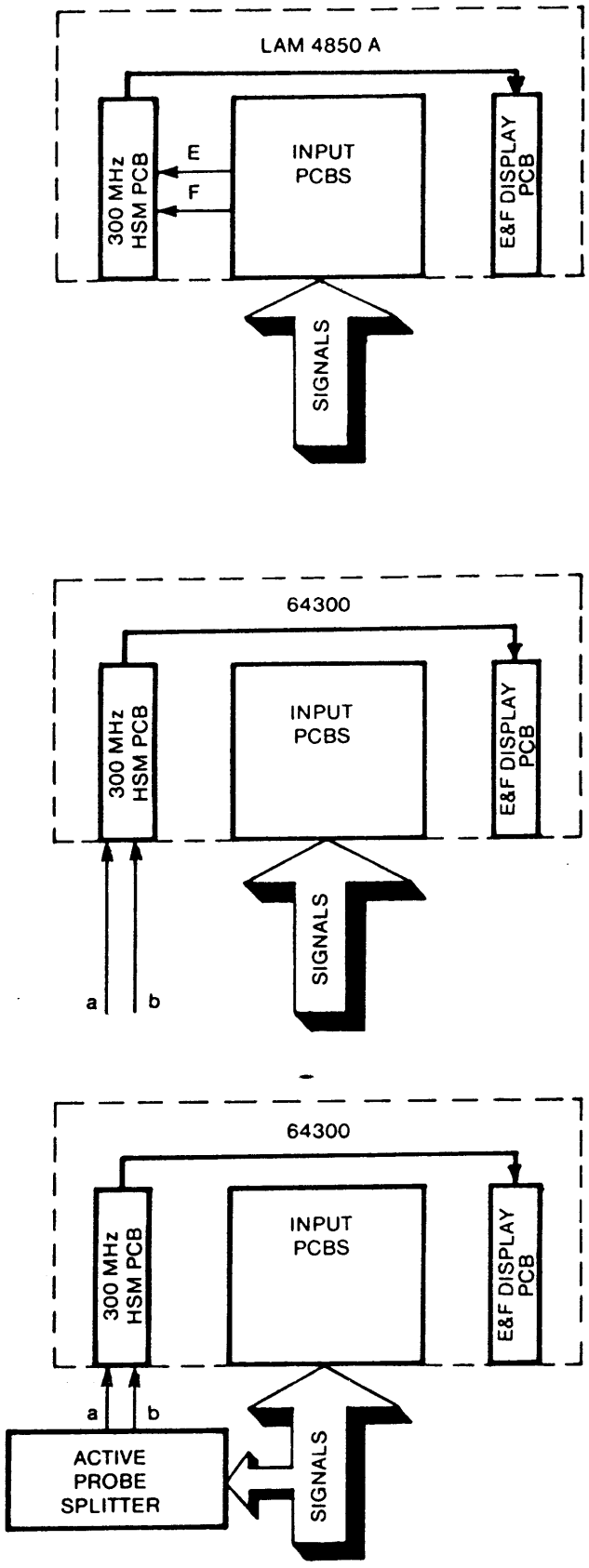

Figure 3-2. Analyzer Configurations

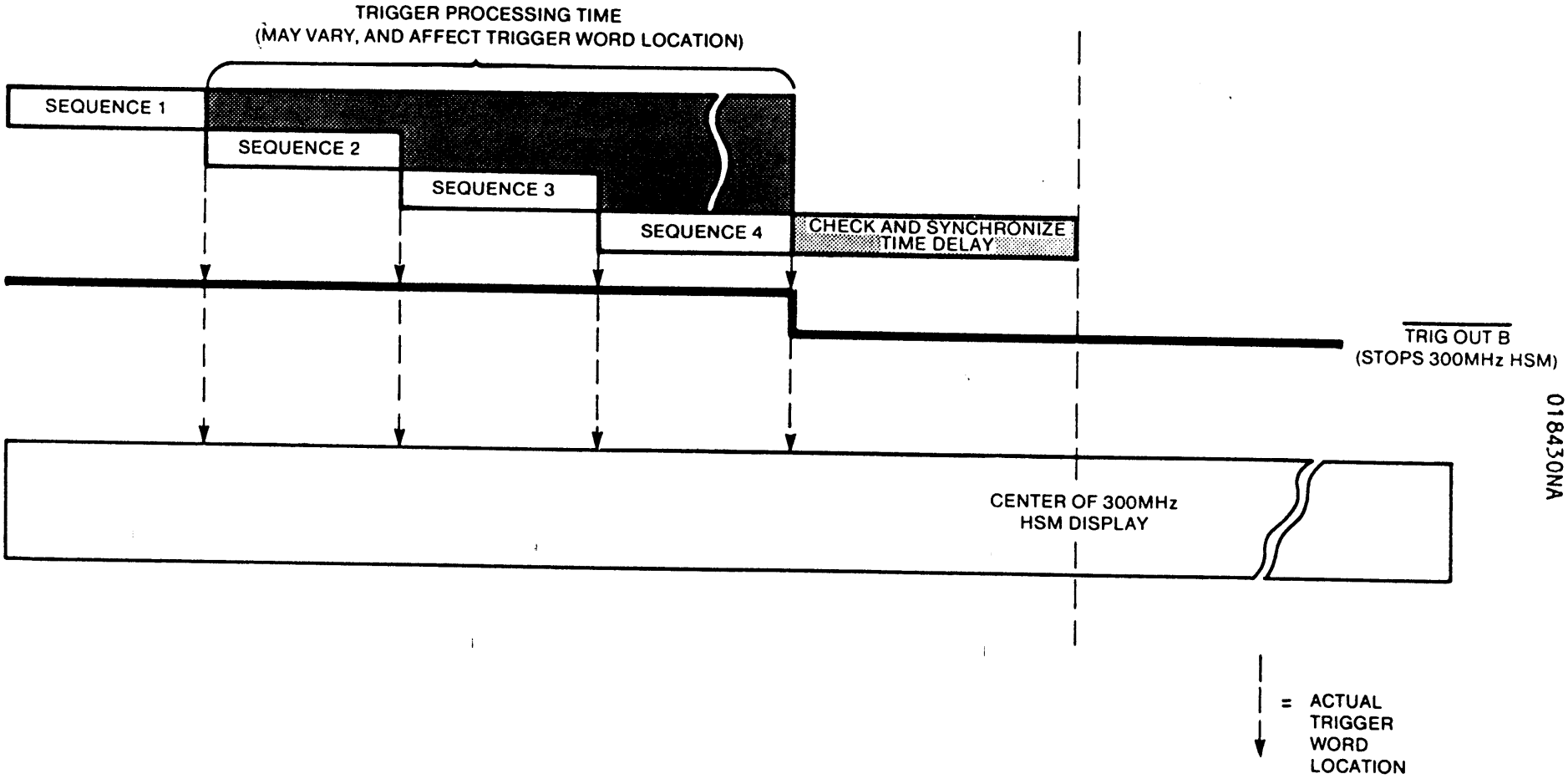

Figure 3-3. 300 MHz HSM Display/Trigger Relationship

SECTION 4

OPERATING PROCEDURES

4.1 INTRODUCTION

The means of accessing, operating, and analyzing the 300 MHz HSM are presented in this section. Refer to the host Analyzer Operator's Manual for details on controls and displays used to operate the Analyzer.

4.2 OPERATING CONTROLS

The 300 MHz HSM is accessed in the following manner:

1) Set the Power Switch to ON. Verify that the "POWER UP SELF TEST COMPLETE!" message shows the 300 MHz Burst Memory as an identified software package.

2) Press the "MENU" pushbutton until the OPTION TABLE is displayed.

3) Move the cursor to the 300 MHz BURST MEMORY option field, using the "EDIT" group pushbuttons.

4) Press the "OPTION" pushbutton. The 300 MHz HSM DISPLAY will be shown on the CRT.

4.2.1 300 MHz HSM DISPLAY

Figure 4-1 shows the display as it appears on the CRT. Table 4-1 identifies the major elements of the display. Refer to the host Analyzer TIMING DIAGRAM figure and table in Section 4, Controls and Displays of the Operator's Manual for additional details on the diagram.

4.3 MODES OF OPERATION

Modes of operation for the 300 MHz HSM are similar to those for the standard TIMING DIAGRAM:

- Selecting magnification
- Moving the magnified display
- Making time measurements
- Arranging channels
- Reprogramming Burst Clock
- Displaying Memories
- Search (Word) function

Some methods of controlling these options are slightly different. These differences will be discussed as applicable.

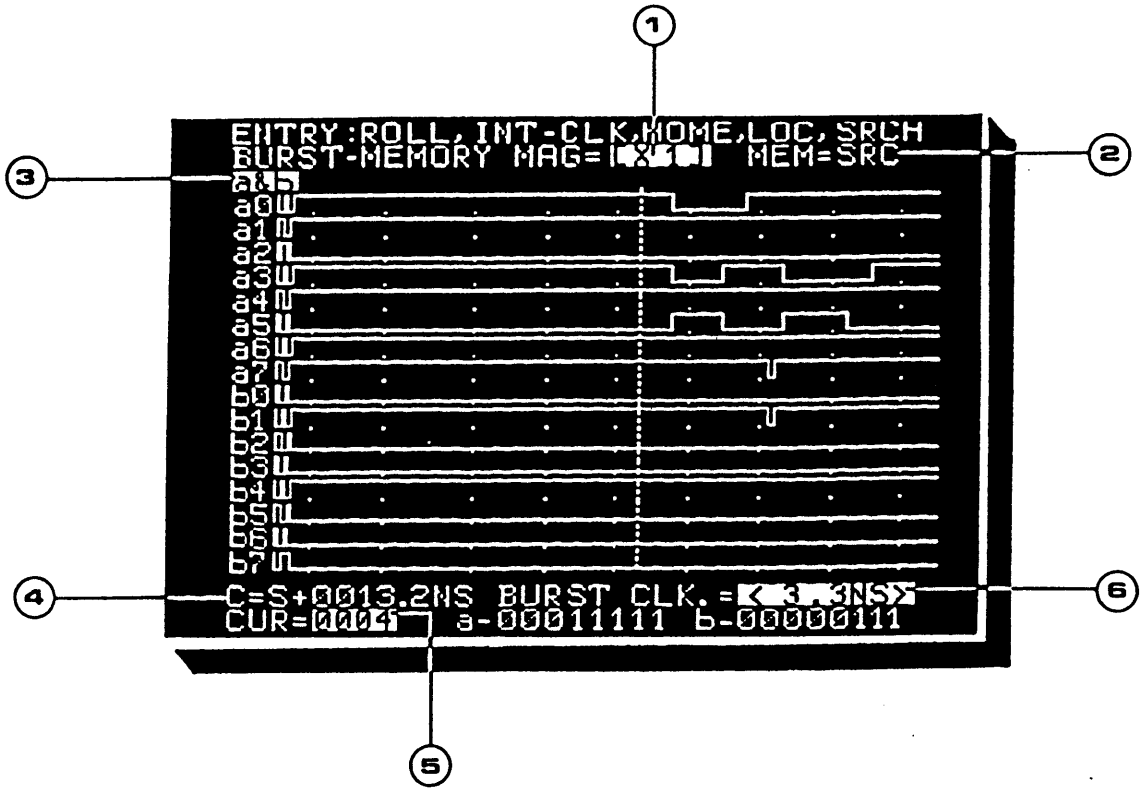

Figure 4-1. 300 MHz HSM Display

TABLE 4-1. 300 MHz HSM DIAGRAM ELEMENTS

LOC COR	FIELD ELEMENTS	DESCRIPTION
1	MAGNIFI-CATION	Indicates magnification selected. (X1,X5,X10)
2	MEMORY	Only SOURCE is available (standard). S+R and S->R are options.
	SRCH = WORD	Only Word search is available.
3	a&b	Channel arrangement within Burst Memory.
4	C=S+/-XXXXns	Time Measurement depending on Dual Time Base.
5	CURSOR	Indicates the cursor position for all channels (Pod Groups) displayed.
6	BURST CLK.	3.3 ns...10 ms. Preset at 3.3 ns (300 MHz) at power-up. Not preset with DataPak.

NOTE

Once the 300 MHz HSM option is called after a recording is made, information on the TIMING DIAGRAM for channel groups E&F is lost. Channel Group E&F information is, however, still available in the LIST DIAGRAM. Therefore, it is advisable to view (and possibly store) the TIMING DIAGRAM of channel group E&F before calling the 300 MHz HSM display.

The 300 MHz HSM is always sampling data during a recording (independent of whether the option is displayed), whenever the "START" pushbutton is pressed. Pre-record programming must be done correctly before the 300 MHz HSM (as well as standard) recording can take place.

With the 64300, the 300 MHz HSM may be set up to sample independently of the other pod groups. By using the Active Probe Splitter, it is possible to link the 300 MHz HSM recording to the general area where the Trigger Word can be found.

4.3.1 Selecting Magnification

The 300 MHz HSM DISPLAY can be expanded (to the right of the cursor) by factors of 1, 5, or 10, as with the standard TIMING DIAGRAM. The difference is that magnification is selected with the "ROLL" pushbutton - not the "TMG/MAG" pushbutton.

4.3.2 Programming Burst Clock

The 300 MHz HSM recording clock is the only recording parameter that needs to be programmed in addition to the basic instrument set-up. At power-up, the clock is set automatically to 300 MHz (3.3ns) and may be changed by using the "INC/DEC" pushbuttons. When the DataPak is installed, the clock is not automatically set to 300 MHz. The range of the 300 MHz HSM clock speeds is determined by the speed of the host Analyzer's internal clock. Table 4-2 shows the relationship between the host analyzer's internal clock speed and the permissable range for the 300 MHz HSM clock.

If the host Analyzer is used with external clocks, the programmable internal rate will still limit the range of the external clock, as shown in Table 4-2. To ensure that the 300 MHz HSM clock ratio is valid, the user must program the host Analyzer's internal clock to match the external clock rate as close as possible.

4.3.3 Other Modes Of Operation

All other modes of operation, and means of controlling the 300 MHz HSM (channel arrangement, timing measurement, etc.) are the same as for the standard TIMING DIAGRAM of the host Analyzer. Refer to the host Analyzer section on TIMING DIAGRAM operation for analysis, operation, memory functions, and search functions details.

If the host Analyzer uses external clocks, the programmed internal rate will still limit the range as shown in Table 4-2. To ensure that the External Clock/300 MHz HSM clock ratio is valid, program the host Analyzer's internal clock rate to match as close as possible to the external clock rate.

TABLE 4-2. HOST ANALYZER/BURST CLOCK RELATIONSHIP

HOST ANALYZER INTERNAL CLOCK	BURST MEMORY RANGE
50 ns	3.3 ns, 6.6 ns, 13.3 ns, 20 ns
100 ns	3.3 ns, 6.6 ns, 13.3 ns, 20 ns, 50 ns
200 ns	3.3 ns, 6.6 ns, 13.3 ns, 20 ns, 50 ns, 100 ns
500 ns	6.6 ns, 13.3 ns, 20 ns, 50 ns, 100 ns, 200 ns
1 us	13.3 ns, 20 ns, 50 ns, 100 ns, 200 ns, 500 ns
2 us	20 ns, 50 ns, 100 ns, 200 ns, 500 ns, 1 us
5 us	50 ns, 100 ns, 200 ns, 500 ns, 1 us, 2 us
10 us	100 ns, 200 ns, 500 ns, 1 us, 2 us, 5 us
20 us	200 ns, 500 ns, 1 us, 2 us, 5 us, 10 us
50 us	500 ns, 1 us, 2 us, 5 us, 10 us, 20 us
100 us	1 us, 2 us, 5 us, 10 us, 20 us, 50 us
200 us	2 us, 5 us, 10 us, 20 us, 50 us, 100 us
500 us	5 us, 10 us, 20 us, 50 us, 100 us, 200 us
1 ms	10 us, 20 us, 50 us, 100 us, 200 us, 500 us
2 ms	20 us, 50 us, 100 us, 200 us, 500 us, 1 ms
5 ms	50 us, 100 us, 200 us, 500 us, 1 ms, 2 ms
10 ms	100 us, 200 us, 500 us, 1 ms, 2 ms, 5 ms
20 ms	200 us, 500 us, 1 ms, 2 ms, 5 ms, 10 ms
50 ms	500 us, 1 ms, 2 ms, 5 ms, 10 ms
100 ms	1 ms, 2 ms, 5 ms, 10 ms
200 ms	2 ms, 5 ms, 10 ms
500 ms	5 ms, 10 ms

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