800 Series
Logic Analyzer
Service Manual

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SECTION 1: INTRODUCTION

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1.1 MANUAL CONTENTS

Section 1: Introduction
Includes a general description of each of the 800 Series including principles of operation, block diagram description, and performance characteristics. A brief description of the performance checks, software update installation procedure and preventative maintenance recommendations are also given.

Section 2: Self-Tests
Description of automatic and keyboard self-tests. In addition, a step-by-step illustration of self-tests performed with the Logic Analyzer Test Card is provided.

Section 3: Chassis, Motherboard, Power Supply, Disk Drive
Mainframe, motherboard layout, power supply, PCB arrangement and information on disk drive service and replacement.

Section 4: Keyboard
Description of keyboard, operation and circuitry.

Section 5: Display Module
Maintenance details of the Display module contained in the 800 series.

Section 6: Processor/Video
Microprocessor, memory, video display circuitry, and IEEE-488 interface details including a block diagram.

Section 7: 800 A, B & C State Control Board (15/20 MHz)
Block diagram, schematic and theory of operation for the 800 A, B, C State Analyzer Control board.

Section 8: 800 A, B & C State Memory Boards (15/20 MHz)
Block diagram, schematic and theory of operation for the 800 A, B, C State Memory Boards.

Section 9: 800 D State Control Board (25 MHz)
Block diagram, schematic and theory of operation for the 800 D State Analyzer Control Board.

Section 10: 800 D State Memory Boards (25 MHz)
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Section 11: 800 A & B Timing Control Board (100 MHz)
Block diagram, schematic and theory of operation for the 800 A, B Timing Control Board.

Section 12: 800 A, B Timing Memory Boards (100 MHz)
Block diagram, schematic and theory of operation for the 800 A, B Timing Memory Board.

Section 13: 800 C, D & E Timing Control Board (200 MHz)
Block diagram, schematic and theory of operation for the 800 C, D & E Timing Control Board.

Section 14: 800 C, D & E Timing Memory Boards (200 MHz)
Block diagram, schematic and theory of operation for the 800 C, D & E Timing Memory Board.

Section 15: CT/SA (Counter Timer/Signature Analyzer) Board
Description of the optional Counter-Timer and Signature Analyzer Plug-in Board.

Section 16: Waveform Board
Schematic and theory of operation for the optional Waveform Recorder Plug-in Board.

Section 17: Disk Controller, Computer Dynamic RAM
Description, operation and circuitry of the Disk Drive Controller and Dynamic RAM.

Section 18: Input Probes
Describes the three probes used with the 800 Series. The Model 80 or 81A Probe is used to apply input signals to the timing analyzer. The Model 51A Probe is used to apply signals to the state section. The Model 90 probe is used for CT/SA readings of external signals and to apply input signals to the CT/SA Board or Waveform Board.

Section 19: Motherboard Connections
Contains complete wiring and pin assignments for the 800 series in tabular form.

Section 20: Glossary
A glossary of terms used in this manual and logic analysis in general.

Section 21: Alignment
Alignment procedure for the Model 800 Logic Analyzer.

Section 22: Parts List
Parts list for the 800 Series Logic Analyzer.

Section 23: Circuit Boards
Component placement diagrams of the 800 Series Logic Analyzer printed circuit boards.

Section 24: Diagrams
Schematic diagrams of the 800 Series Logic Analyzer.

1.2 800 SERIES OPERATION

Instrument operation is covered in detail in the 800 Series Operator's Manual shipped with each unit. Additional copies are available from Nicolet.

The Operator's Manual contains several sections that may be useful from a maintenance point of view. These sections should be reviewed for a greater understanding of the product operation. The sections concerning keyboard, menus and displays, and reference should be particularly helpful. The reference section contains solutions to many common operating problems.

1.3 BLOCK DIAGRAM DESCRIPTION

Refer to Figure 1-1. The 800 Series is interconnected by a custom 60-wire system bus (called the S2 bus) that forms an I/O path for all the functional modules.

The CPU incorporates an Intel 8085 microprocessor that utilizes up to 48K bytes of ROM, and 48K bytes of RAM. The processor controls system operation, including data collection, keyboard scanning, display and interfacing.

The State Input circuitry consists of Model 51A probes connected to State Memories A, B and C. (The 800A uses no B Memory Board). Data is latched into these memories at rates up to 25 MHz. The data is continuously examined by the state control trigger detectors. When the data meets user-selected trigger conditions, it causes a Main Memory data collection.

Timing input data from two Model 80 or 81A probes (depending on the model) is fed to data comparators on Timing Memory boards A and B. The data is sent from the probes in 16-bit parallel data streams. Data is continuously examined by these comparators. The data is sent from the comparators to the Main Memory, at user-selected clock rates up to 200 MHz. The comparators continuously compare the incoming data with arm and trigger words entered from the keyboard at setup time.

When arm and trigger conditions are met, a snapshot of 1000 words of current data is locked into the Main Memory. This snapshot subsequently may be displayed and examined. The 1000-word snapshot also can be divided between pre-trigger and post-trigger words as selected from the keyboard at setup time.

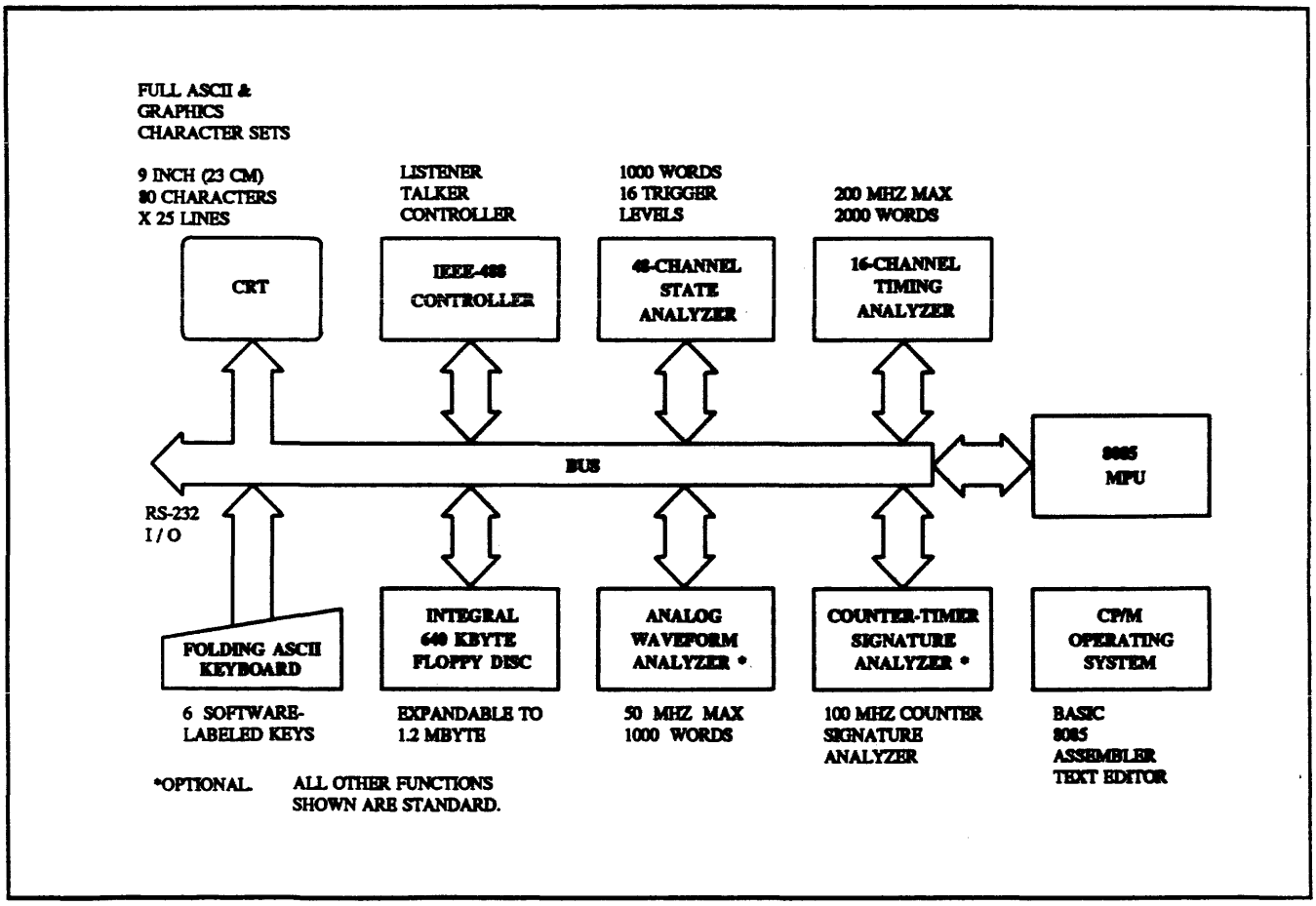

Figure 1-1 - 800 Series Simplified Block Diagram

The Main Memory retains the last data entered until a new set of data is loaded. The new set of data is loaded using the COLLECT (soft) key. Also, the contents of the Main Memory can be transferred to the Auxiliary Memory where it may be retained for comparison with subsequent Main Memory data collection. The contents of either the Main or Auxiliary Memory can be displayed under keyboard control.

The CRT Display is a raster scan unit with a 9-inch (23 cm) diagonal screen. The driving circuitry resides on the CPU board. A composite video output on the rear panel of the 800 Series allows use the of a large-screen monitor if desired.

The keyboard provides user access to the 800 Series parameter/measurement set (on the menus), display formats, trigger modes and interfaces. The keys are used for direct entry, menu selection and software-defined "soft" keys.

An RS-232 Interface is provided on models equipped with disk drives. This interface permits output of display-formatted data to a printer or other peripheral. The 800 Series also is provided as standard with an instrument-bus IEEE-488 Interface, allowing the 800 Series to be talker, listener (or controller if so equipped).

Optional measurement features are added to the 800 Series by adding the CT/SA (Counter-Timer/Signature Analyzer) PCB to the unit.

The Waveform Analyzer board can optionally be included in the 800 Series to obtain added analog measurement capabilities.

Mnemonic Disassembly accessories are available for a variety of microprocessors. Disassembly operates by loading programs from disk and collecting data using dedicated probes.

1.4 BASIC OPERATION

The 800 Series analyzer collects data under specified conditions and stores the data in memory for detailed examination.

To start data collection, the user presses COLLECT (soft key) on the keyboard. When the trigger conditions are met, data collection is automatically stopped by the analyzer. Alternately, selection may be made for data collection to continue after the trigger event. The user must specify the amount of post-trigger data to be collected. Once data collection has stopped, the data can be displayed in various formats for convenient analysis.

1.5 SOFTWARE UPDATE INSTALLATION

The parts, procedure and tools required to update the revision level of the operational software (resident in firmware) in the 800 Series Logic Analysis Systems to the most current one is given below. These parts are to be installed on the first PC board in the card cage closest to the CRT module assembly.

CIRCUIT BOARD SLOTS	
Front	
A	Processor (CPU card) <<---
B	RAM Disk
C	State Control
D	State Memory - C (LSB)
E	State Memory - A (MSB)
F	State Memory - B
G	Timing Control
H	Timing Memory - A
I	Timing Memory - B
J	Waveform
K	Counter-Timer/SA

Tools Required

1. Flat blade 1/4" screwdriver
2. 5/16" open end or box wrench
3 Small Phillips screwdriver
4. I.C. removal tool
5. Factory supplied replacement firmware

1.5.1 Procedure

Warning: Remove all power from the instrument before continuing.

Remove the line cord and probe cables, moving the unit to a suitable working environment.

To gain access to the CPU card, the top cover of the unit must first be removed using the flat blade screwdriver to loosen the "quarter turn" fasteners at the rear. Turn them counterclockwise to loosen.

Use the 5/16" wrench to remove the two hex nuts at the rear of the hold down bar, being careful not to drop them onto the motherboard surface.

Use the Phillips head screwdriver to remove the two screws retaining the hold down bar at the front of the card cage assembly. Remove the hold down bar for access to the front PCB, the CPU card.

Prior to lifting the CPU card, the floppy disk drive cable should be released from its hold down clamp on the rear of the CRT module enclosure. The card-edge connector should be pulled gently upward and set aside. If a Waveform Recorder card is installed in Slot J then remove the flat ribbon cable connected on the CPU card in Slot A. Release of the DIP Plug Assembly from the socket on the CPU board can be accomplished by carefully prying with the flat blade screwdriver under the edge of the plug. The CPU board's video connector also should be removed. Remove the 800 Series CPU card by prying on the LEFT HAND card edge removal hole and pulling straight upwards.

Examine the Replacement Firmware, factory supplied as a set of EPROMs. The label on the top of each EPROM contains the following information:

EPROM part number: Part number.

Revision/Version: Firmware revision or version.

Socket location: IC socket location on the CPU card where the EPROM is to be installed.

Model number: Logic Analyzer system.

EPROM Check Sum: Check sum of EPROM using either Data I/O programmer or format.

The label format is:

	Version/Revision	
EPROM P/N	61XX-X XX UX	Socket Location
Model #	M800X XXXX	EPROM Check Sum

The EPROMs are installed as follows:

With the video connector over the edge, place the CPU board with its component side up on a soft magazine cover. Be careful not to flex the card. Using the label format described previously to select the appropriate EPROM, remove and replace only one IC at a time to avoid confusion. Replace all of the EPROMs residing in IC locations U1, U2, U3, U4, U15, U16 and U17.

Reinstalling the CPU card and top cover is the reverse of the removal procedure.

Data/test "save" files are compatible from revision to revision. Remember to return all old EPROMs to the factory for full credit.

1.6 PREVENTATIVE MAINTENANCE

As in all electronic equipment, excessive dirt and heat build-up can lead to premature failure. The 800 Series Logic Analysis System operates normally over a range of temperatures. If, however, the fan filter on the rear panel becomes clogged or is obstructed, then the cooling ability is markedly diminished.

It is recommended that the fan filter be cleaned at regular intervals. A three to four inch clearance should be left behind the unit for free air flow at all times during operation. More frequent cleaning or physical repositioning may become necessary if excessive dirt buildup is detected or the unit feels abnormally warm during operation.

The floppy disk drive has been designed to be free from periodic maintenance (such as replacement of parts, grease-up, etc.) when it is operated under normal duty. The drives rarely need attention if the following precautions are followed:

* Avoid smoke filled environments

* Do not employ the "flippy" floppy diskettes where the rotational direction is reversed by inverting the diskette. The drives employ two-sided read/write mechanisms, inverting the diskettes can loosen trapped particles from the liners inside of the sheath.

* Do not operate the drive in a high humidity or excessively cold environment. If the analyzer is stored in a cold environment, allow adequate time for the chassis to reach normal room operating temperature before mounting and running a floppy diskette.

* Always follow all floppy disk handling precautions regarding creasing, heat, dirt, magnetic contamination, etc.

If disk subsystem problems (such as suspected media quality) are encountered that cannot be rectified by switching to another brand, then cleaning the heads is recommended as discussed in Section 3, Chassis, Motherboard, Power Supply and Disk Drive. If problems have been narrowed to the drive itself, then refer to Section 3 for the removal procedure. The drive contains no user serviceable components; repair dictates an exchange.

SECTION 2: SELF TESTS

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- 2.2.1 Processor Test ——— 2-2
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2.1 INTRODUCTION

The 800 Series provides three types of self-tests that can be useful in assessing the condition of the instrument.

#1. An automatic self-test is performed every time power is turned on.

#2. Self-tests that can be performed with the Logic Analyzer Test Card, part number 615-004602.

#3. Self-tests that can be performed using a system disk.

2.2 AUTOMATIC SELF TEST

The automatic self-test is performed during the first two seconds each time power is applied to the analyzer. This test goes through a set of performance checks of the 800 Series memories and other subsystems. The test reads the setting of the power-line frequency selector switch, S1-1, on the Processor board. The CRT vertical SYNC frequency is set to a matching 50 Hz or 60 Hz. Although this self-test does not provide a 100% check, it offers a high confidence level that the analyzer is operating properly.

Successful completion of the test is announced by a short beep followed by a display of the Configuration Menu. If the test is not successful, there will be no beep. This may indicate a switching power supply problem. Check the illumination of the green POWER LED on the keyboard. If the LED is not lighted, simply reset the POWER switch to off for a few seconds, then back on.

2.2.1 Processor Test

The 800 Series system software contains a test that automatically checks the processor board.

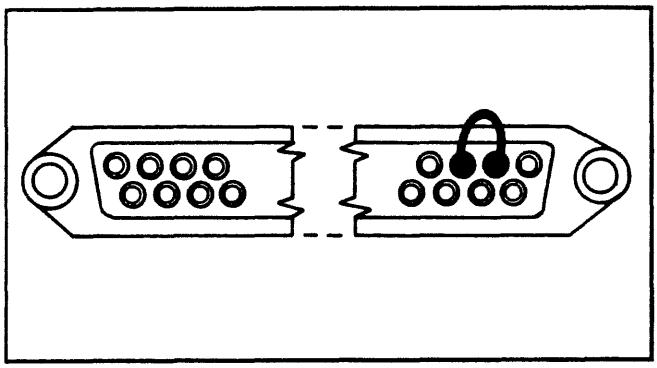


Figure 2-1: Connector Jumper

To run this test:

a. Turn the 800 **OFF**.

b. If a test of the RS-232 interface is desired, short pins 2 and 3 of the RS-232 connector, located on the rear panel of the unit. (See Figure 2-1).

c. Turn the 800 ON.

d. Press the BREAK key.

e. Verify that the display appears as shown in Figure 2-2. To abort the test, hold down the RESET key for three seconds.

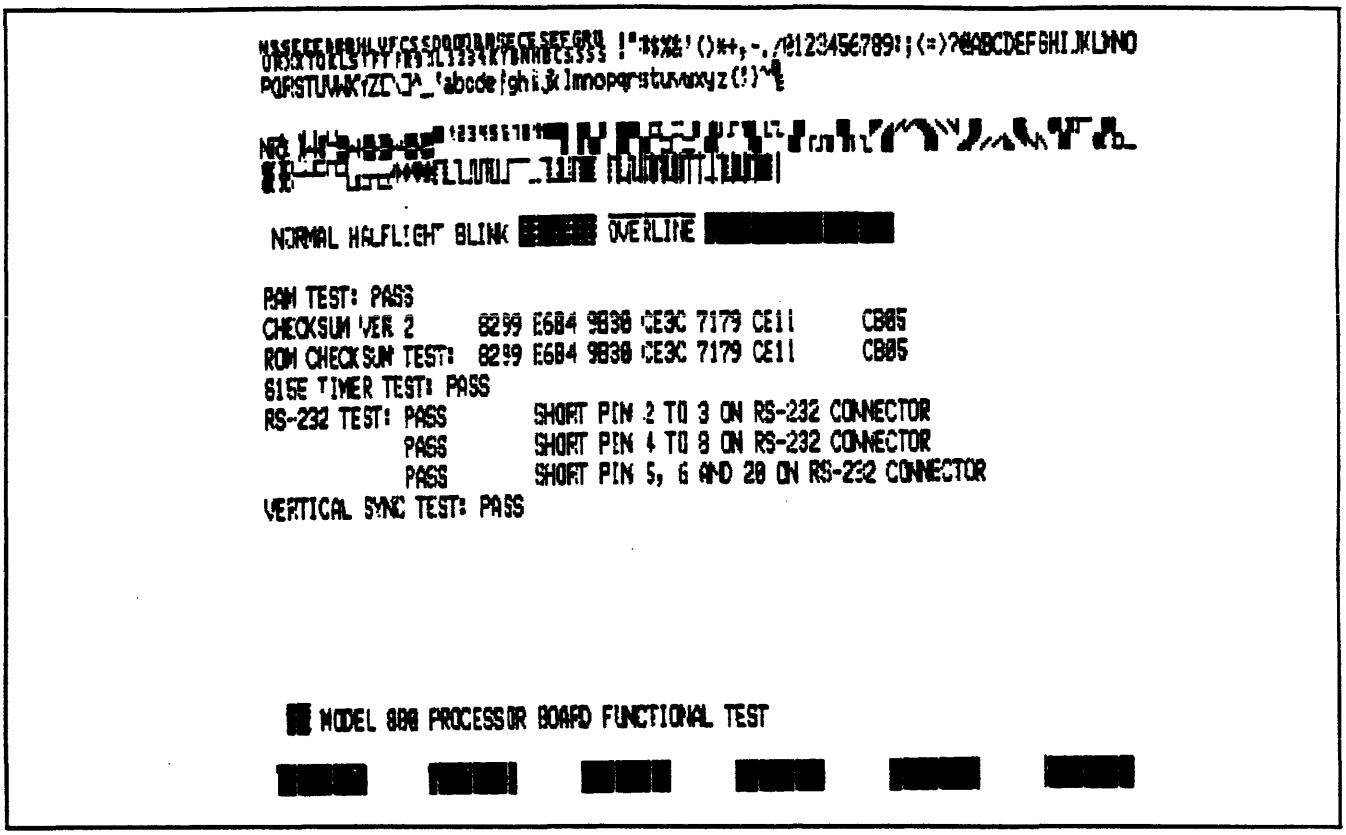


Figure 2-2: Self Test Screen

2.2.2 System Disk Self-Tests

Each CP/M equipped system contains two tests on the system diskette: the RAM test and the Keyboard test. To run these tests, insert a system disk into drive A with the write protect notch facing downwards, power the system on, and close the drive door. Then press the ESCape key. The CRT display will then look like Figure 2-3.

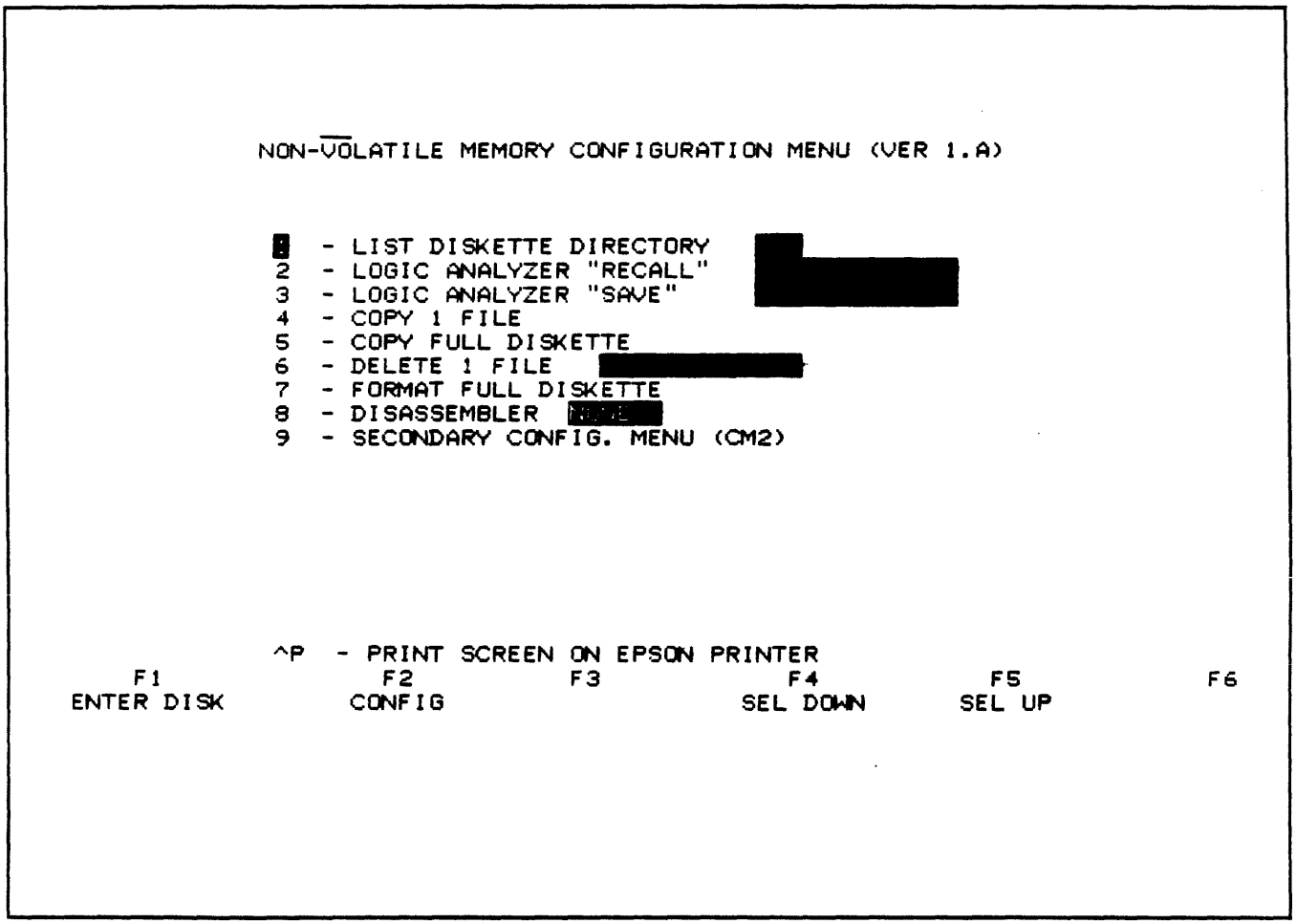


Figure 2-3: Screen

To run the RAM test, type RAMTEST <return>. This test writes a walking 1's pattern into the dynamic RAM, reads the data back and indicates any errors. The test runs continuously, taking about 20 minutes for each pass. The total number of errors and the number of test runs is indicated on the screen (Figure 2-4). To abort the test, press the RESET key.

```
48K DYNAMIC RAM TEST PROGRAM
WALKING I'S TEST:     1'S ADDR: 8896

TESTING ADDRESS:      ----
LAST FAILED ADDRESS:---- EXPECTED:--- READ:--
TOTAL FAILURES:
PASSES COMPLETED:
```

Figure 2-4: RAMTEST Screen

To run the keyboard test, type KYBDTEST <return>. Observe the keyboard display on the CRT. To test the keyboard, unlock the CAPS LOCK key. Strike each key displayed on the screen only once. As each key is struck, it will disappear from the screen. See Figure 2-5. Follow the remaining prompts carefully to complete the test.

```
        F1 F2 F3 F4 F5 F6 LABELS

     ESC 1 2 3 4 5 6 7 8 9 Ø - = ~ BS BK
       TAB q w e r t y u i o p [ | LF DEL
         a s d f g h j k l ; ' { RETURN
   S1        z x c v b n m , . /        S2
                  SPACE

  UNLOCK CAPS LOCK KEY

  PRESS EACH KEY ON KEYBOARD.
  ALL KEY LABELS SHOULD DISAPPEAR.
```

Figure 2-5: Keyboard Test Screen

To abort the test without finishing the sequence, press the RESET key for 2 seconds.

2.3 BASIC TESTS WITH THE LOGIC ANALYZER TEST CARD

The Logic Analyzer Test Card, part number 615-004602, provides a comprehensive functional test of the 800 Series Logic Analysis system hardware. A suitable procedure follows for the appropriate model. All steps necessary for a comprehensive evaluation are presented, thereby affording the user fault isolation. This procedure assumes the user has some familiarity with the operation of the 800 Series. If necessary, refer to the Operator's Manual.

2.3.1 Preliminary Tests

Perform the following tests to confirm operation at the most primitive level.

a. Disconnect the power cord from the analyzer. The power fuse and voltage cord must be visually inspected to verify correct installation for the current application. Refer to the discussion of the Mains Module in the Chassis section for more information. Reconnect the power cord.

b. Check the setting of SW1-1 on the Processor Board. The video vertical sync frequency is set to match the power mains frequency. ON = 60 Hz, OFF = 50 Hz.

2.3.2 Test Card Description

The Logic Analyzer Test Card consists of two 8-bit CMOS counters (A and B), a clock, and simple decoding logic. Refer to Figure 2-6 and schematic **166-004601** at the end of this manual. Each CMOS counter normally counts from (00) HEX to (FF) HEX. When the A counter reaches (40) HEX, the decode logic resets the B counter to (00) HEX.

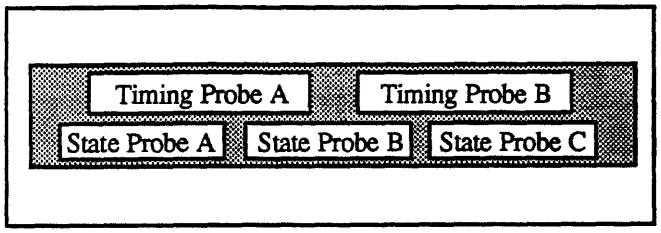


Figure 2-6: Logic Analyzer Test Card

The A channel connector is wired with the eight least significant bits corresponding directly to the output of the A counter. The eight most significant bits are tied to ground. Thus, the A channel provides a 16-bit word to the analyzer that sequences from (0000) HEX to (00FF) HEX.

The B channel connector is wired so that the 16 output bits toggle nonsequentially. A typical binary count sequence at the B channel connector is illustrated in Figure 2-7.

Count	Binary Pattern*	Hex Pattern
0	00000000 00000000	00 00
1	10000000 00000001	80 01
2	01000000 00000010	40 02
3	11000000 00000011	C0 03
.	. . .	
.	. . .	
.	. . .	
15	11110000 00001111	F0 0F

Figure 2-7

Note the difference in pin-outs between the 16-channel state probes and the 8-channel timing probes. Due to the difference, this exact pattern will be displayed on the 800 Series only when using the state probe. Use of an external clock for the timing analyzer and display of data in the state format can also yield similar results.

Power to the test card is supplied by the +5 V output at either probe connector.

The A counter is generally used as a signal source for the A state or timing probe. The B counter output feeds the B state or timing probe. The third 16-channel state probe (C) is not normally connected to the test card.

2.3.3 Setup

Before using the test card, proceed as follows:

a. Connect the A and B Model 51A State Probe cables to the 800 Series mainframe. LEAVE THE C PROBE UNCONNECTED. In the case of the Model-800 A system use the A and C connectors only.

b. Connect the A probe to the left-hand connector of the test card and the B probe to the right-hand connector. Set both probes for TRUE and TTL operation.

c. Turn the 800 Series power switch ON and wait for the self-test beep and Configuration Menu. Refer to Figure 2-8.

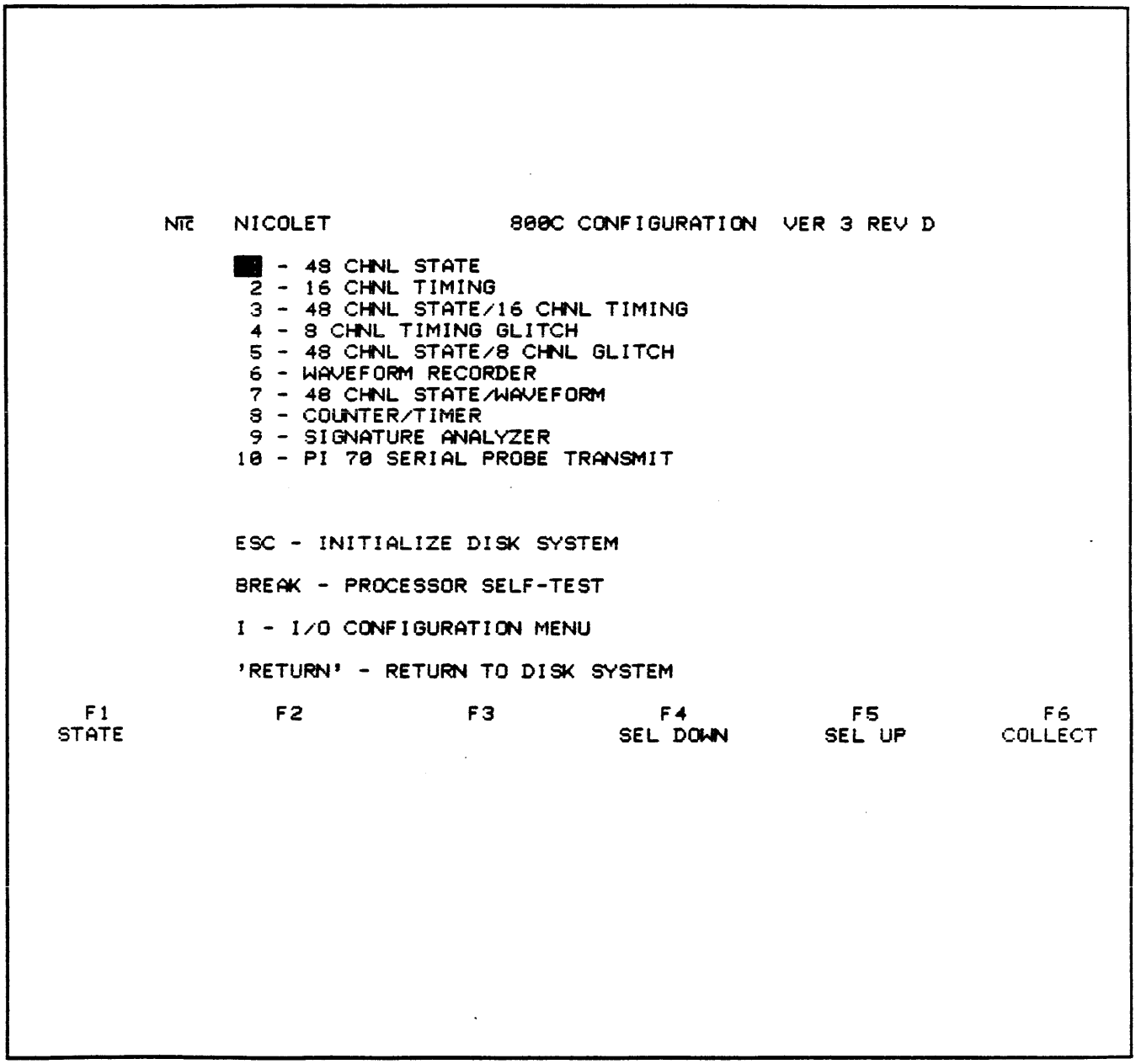


Figure 2-8: Configuration Menu

2.3.4 Basic State Tests

The six soft function keys are labeled F1 to F6 from left to right. They are identified by labels on the bottom line of the CRT. These labels differ from menu to menu, as selected with the SEL DOWN or SEL UP keys.

Examples using these keys follow.

a. To select the 48-CHANNEL STATE menu, press the STATE (F1) key to call the state menu (Figure 2-9A for Models 800 A, B, and C; Figure 2-9B for Model 800 D).

b. The Model 800 A, B, or C 32/48-channel state menu should be setup with default values in all fields except the trigger word field. Advance the blinking cursor to the trigger stack field, level 0, with the NEXT (F2) key. Position overshoot can be ignored since the menus wrap-around in all fields. Press the H key to format this field for a hexadecimal trigger word. Now enter the following trigger word: 0040.

   Observe the field at the lower right of the CRT. Other formats can be selected from this field using the indicated keys.

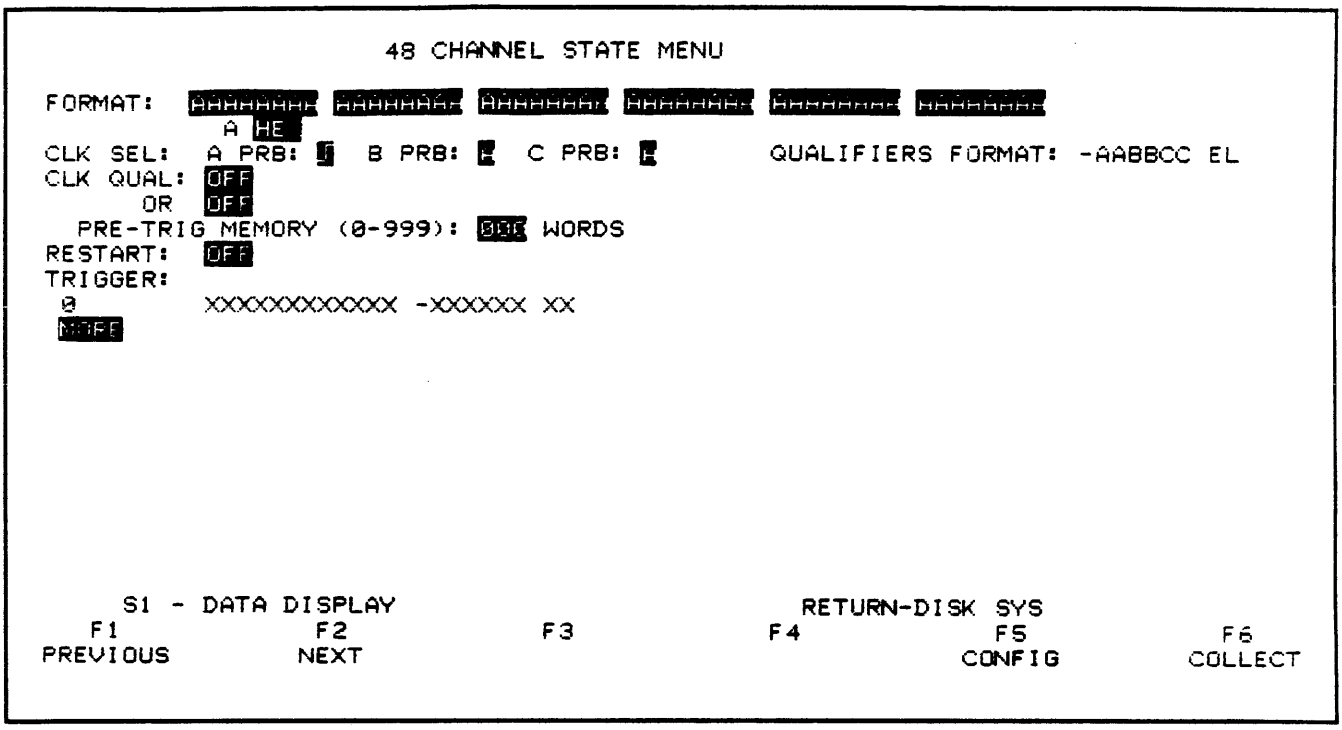


Figure 2-9A: Model 800 A, B, C State Menu

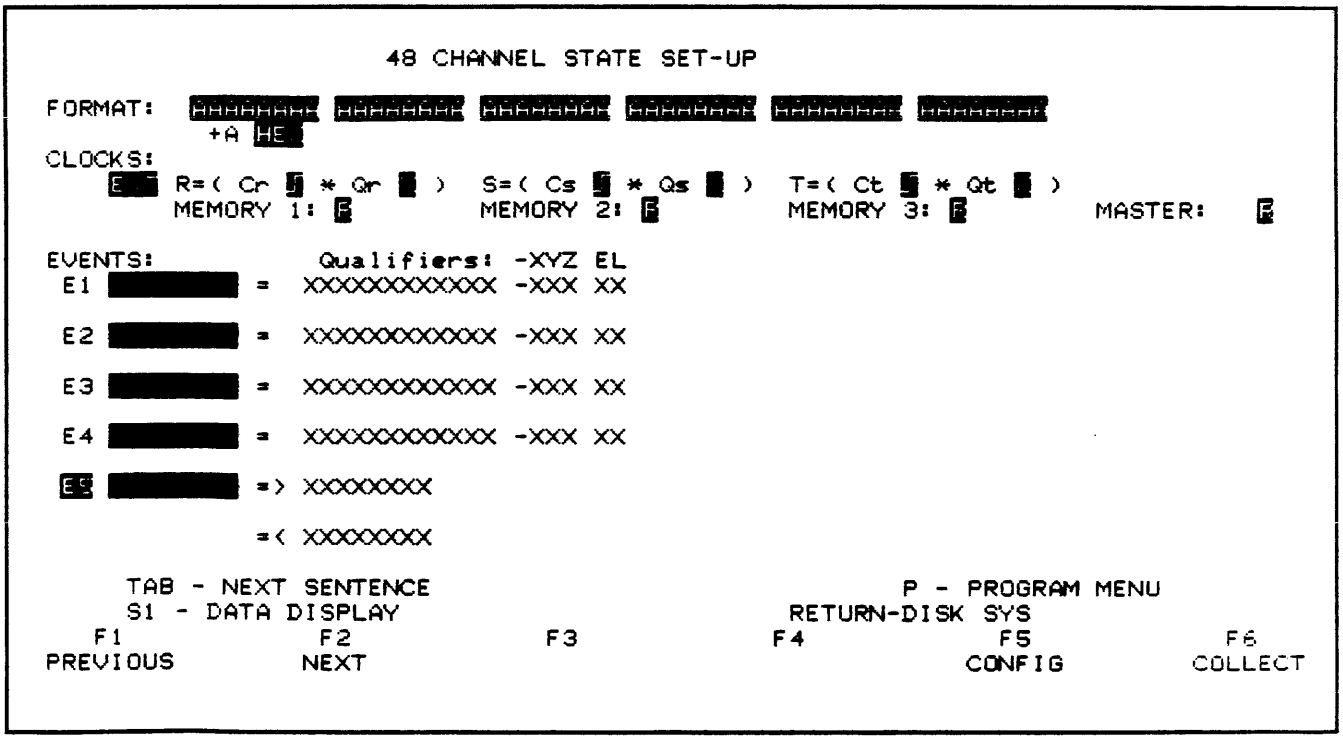


Figure 2-9B: Model 800 D State Menu

NOTE: Steps c and d are skipped when using the Model 800 A, B, or C systems.

c. The Model 800 D Setup Menu should be left with all default values except for EVENT E1. In the field provided for symbolic labels, enter FORTY. Place the cursor on that field using the PREVIOUS (F1) key. Enter the word and press NEXT (F2). Enter the bit pattern 0040 in hexadecimal.

d. On the Model 800 D, press P to enter the PROGRAM menu; setup conditions on STEP 1 such that the analyzer will STORE NONE. IF 0001 of E1 then GO TO (Step) 2 NO Link. STEP 2 should read STORE ALL. IF 1000 of ANY then DONE NO LINK. Leave the remaining fields at the default setting. See Figure 2-10.

e. Press COLLECT (F6) to take a data collection beginning at 0040. The Model 800 D will begin at 0041. Then press the LABELS key. Reformat the display in octal, decimal, binary and ASCII by pressing the O, Z, N, and Y keys in turn. Press the H key for the hexadecimal format. See Figure 2-11.

f. Scroll the display up and down by holding down the SCRL UP (F2) key SCRL DOWN (F1) key. Locate the end of the data collection (word +999) by pressing the LOCATE (F3) key followed by the E key. Next, locate word +101 by pressing LOCATE (F3) followed by +101. Omit the plus + sign on the Model 800 D. Finish with the trigger word at the top of the CRT by pressing the LOCATE (F3) and T keys. On the Model 800 D press the LOCATE (F3) and B keys.

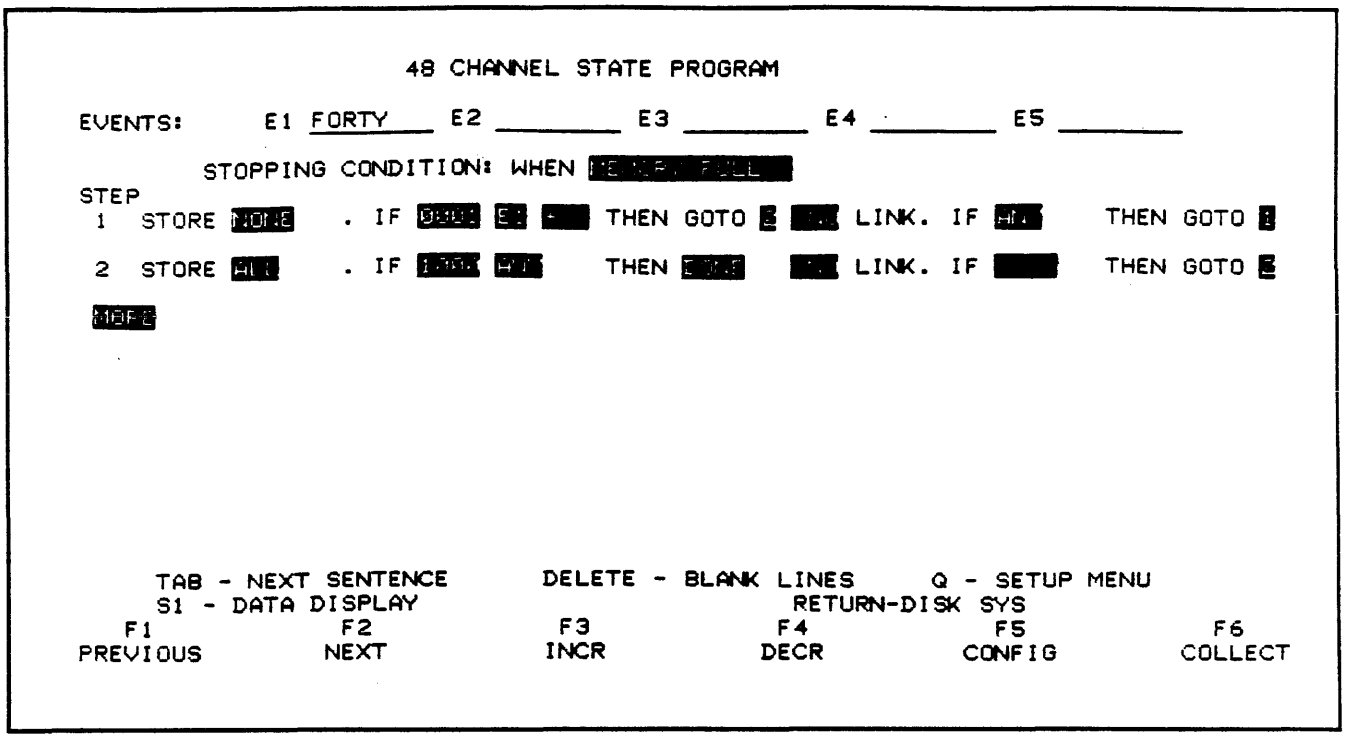


Figure 2-10: Model 800 D Program Menu

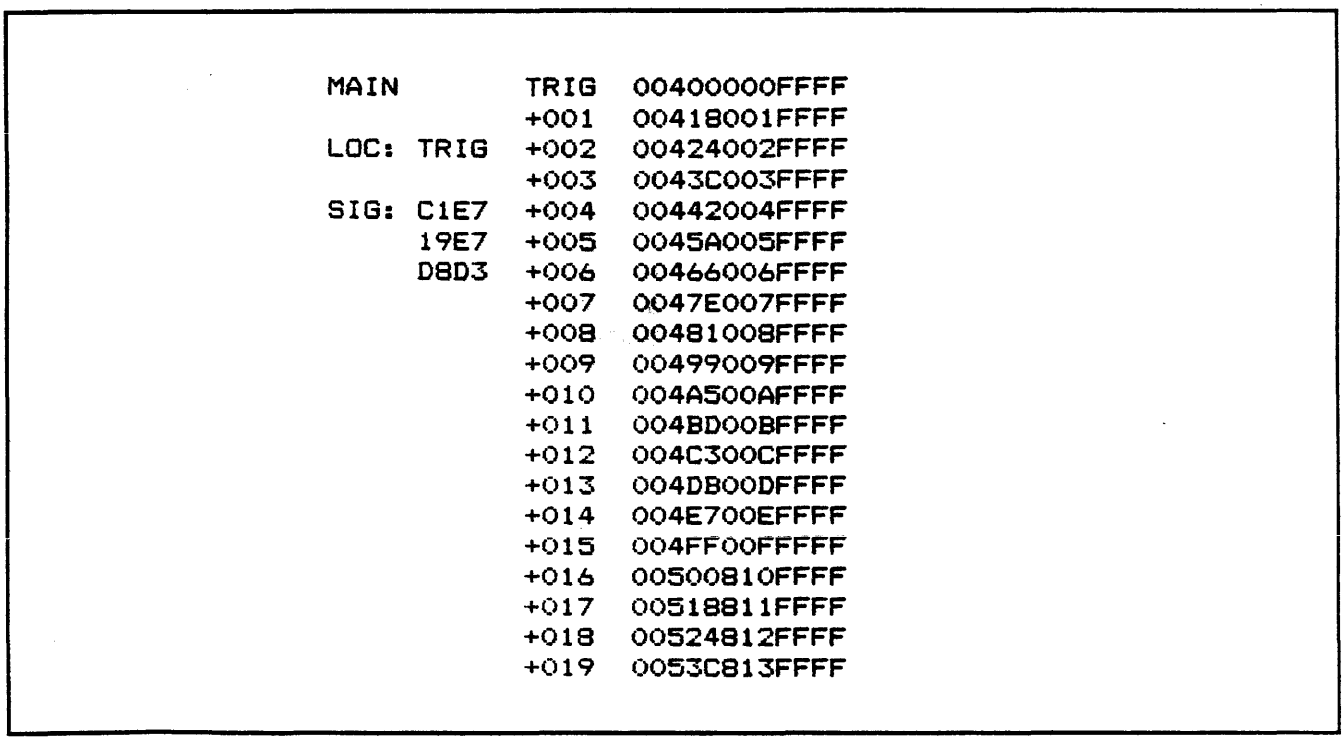


Figure 2-11: Hexadecimal Screen

2.3.4.1 Saving Data/Comparisons

To test the SAVE mode, press the LABELS (F6) key in the top row. Perform the SAVE function by pressing the S key. This action causes the entire data collection, the test codes (SIG), and the menu parameters to be stored in the 800 Series auxiliary RAM memory. Press the MEMSEL(M) key to display the auxiliary memory. Press M again to redisplay the main memory.

2.3.4.2 HOLD IF Mode

The HOLD IF mode is used to detect and isolate intermittent faults. The Model 800 A, B and C will halt the comparison process if the MAIN and the AUXILIARY memories are NOT EQUAL.

The halt conditions for the Model-800 D are when the MAIN and the AUXILIARY memories are EQUAL or are UNEQUAL; the choices are set as TRUE and FALSE on the SEARCH/COMPARE menu. Press SRCH/CMP (F4) while viewing the data to access the SEARCH/COMPARE menu. The default conditions allow all of the 48 incoming channels in the entire 1000 words of memory to be compared. See Figure 2-12.

On any of the 800 Series State Analyzers, activate this acquisition mode by simply pressing the # key (SHIFT and 3 together). Note that the flashing status messages indicate the analyzer is automatically collecting and comparing main and auxiliary data.

Hold the short grounding wire on pad 5 on the right-hand side (B side) of the test card to create a fault. Note that the flashing status message now reads HOLDING, and data is displayed. Remove the wire from pad 5.

Press the M key to compare the main and auxiliary data compression test codes. Notice that one of the three main memory test codes differs from the corresponding auxiliary memory test code. They are listed in order for the A, B and C Probes. This indicates that somewhere in the new data collection, one or more bits differ between the main and auxiliary memories. Now return to the main memory.

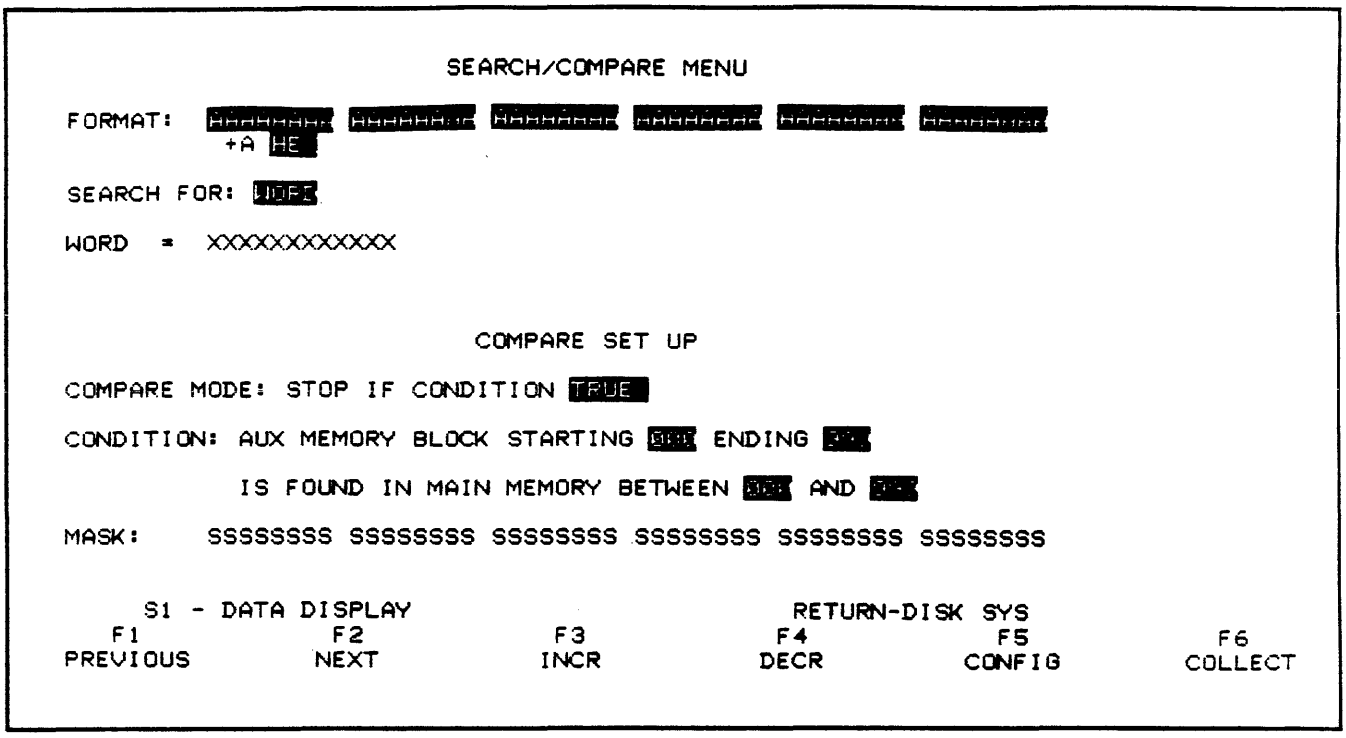


Figure 2-12: Model 800 D Search/Compare Menu

2.3.4.3 Difference Mode

The DIFFERENCE mode is used for rapid identification of differences between any previously-saved auxiliary memory data and main memory.

Press the / key to activate the DIFFERENCE mode. This key toggles the DIFFERENCE mode so that repeated keystrokes turn it on and off. In this mode, only clocked states (data words) that differ between the main and auxiliary memories are displayed at full-intensity. Data words that match are displayed at half-intensity. Press the SCRL UP (F2) key to find the first difference word. Refer to Figure 2-13.

Press the N key to view the difference in binary. Then press and hold the M key to locate the specific bits responsible for the differences. Note that the shorted bit appears on two input channels.

```
MAIN          TRIG  *0007E3C7FFFF
                    +001  *000813C8FFFF
LOC:  TRIG          +002  *000993C9FFFF
                    +003  *000A53CAFFFF
SIG:  C03F          +004  *000BD3CBFFFF
      C43F          +005  *000C33CCFFFF
      D8D3          +006  *000DB3CDFFFF
                    +007  *000E73CEFFFF
                    +008  *000FF3CFFFFF
                    +009  *00100BD0FFFF
                    +010  *00118BD1FFFF
DIFFERENCE          +011  *00124BD2FFFF
                    +012  *0013CBD3FFFF
                    +013  *00142BD4FFFF
                    +014  *0015ABD5FFFF
                    +015  *00166BD6FFFF
                    +016  *0017EBD7FFFF
                    +017  *00181BD8FFFF
                    +018  *00199BD9FFFF
                    +019  *001A5BDAFFFF
```

Figure 2-13: Difference Menu Screen

Return to the main memory and press the H key. Press LOCATE (F3) followed by D to place the first difference word at the top of the screen. This is an alternative and faster way of locating the first difference word. Now press LOCATE followed by S to find the next group of half-intensified words that are the same. Press the SCRL DWN key once to verify this. Refer to Figure 2-14.

Press LOCATE followed by T to place the trigger word at the top of the CRT. Then press the / key to disable the DIFFERENCE mode.

2.3.4.4 Search Word Mode

The SEARCH WORD mode allows you to locate any particular bit pattern within a data collection. You specify the word to search for and then the direction of search.

On the Model-800 A, B or C press the SRCH WRD (F4) key to obtain the menu shown in Figure 2-15. The Model-800 D menu is called the Search / Compare Menu. See Figure 2-12.

In the example, 009E is used as the word to be found in the data collection. (**NOTE:** This word occurs only once in the data memory). Key in 0-0-9-E (the rest of the field are X's - DON'T CARE). Press S2 to display the data again, then press K to search the data for 009E. Refer to Figure 2-16.

```
MAIN          +980   00 FE 7D BE FF FF
              +981   00 FF FD BF FF FF
LOC: +980     +982   00 00 03 C0 FF FF
              +983   00 01 83 C1 FF FF
SIG: C0F7     +984   00 02 43 C2 FF FF
     C3F7     +985   00 03 C3 C3 FF FF
     D8D3     +986   00 04 23 C4 FF FF
              +987   00 05 A3 C5 FF FF
              +988   00 06 63 C6 FF FF
              +989   00 07 E3 C7 FF FF
              +990   00 08 13 C8 FF FF
DIFFERENCE    +991   00 09 93 C9 FF FF
              +992   00 0A 53 CA FF FF
              +993   00 0B D3 CB FF FF
              +994   00 0C 33 CC FF FF
              +995   00 0D B3 CD FF FF
              +996   00 0E 73 CE FF FF
              +997   00 0F F3 CF FF FF
              +998   00 10 0B D0 FF FF
              +999   00 11 8B D1 FF FF
```

Figure 2-14: First Difference Screen

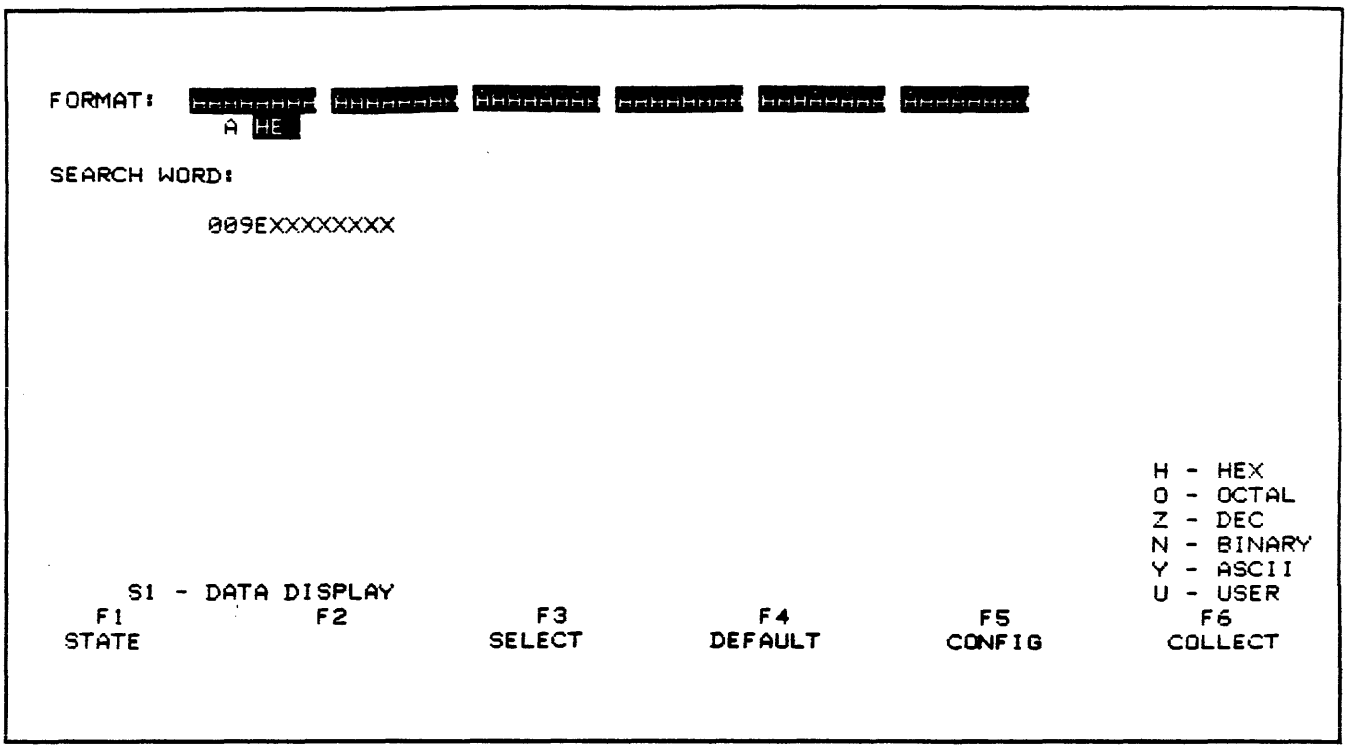


Figure 2-15: Model 800 A, B, and C Search Word Menu

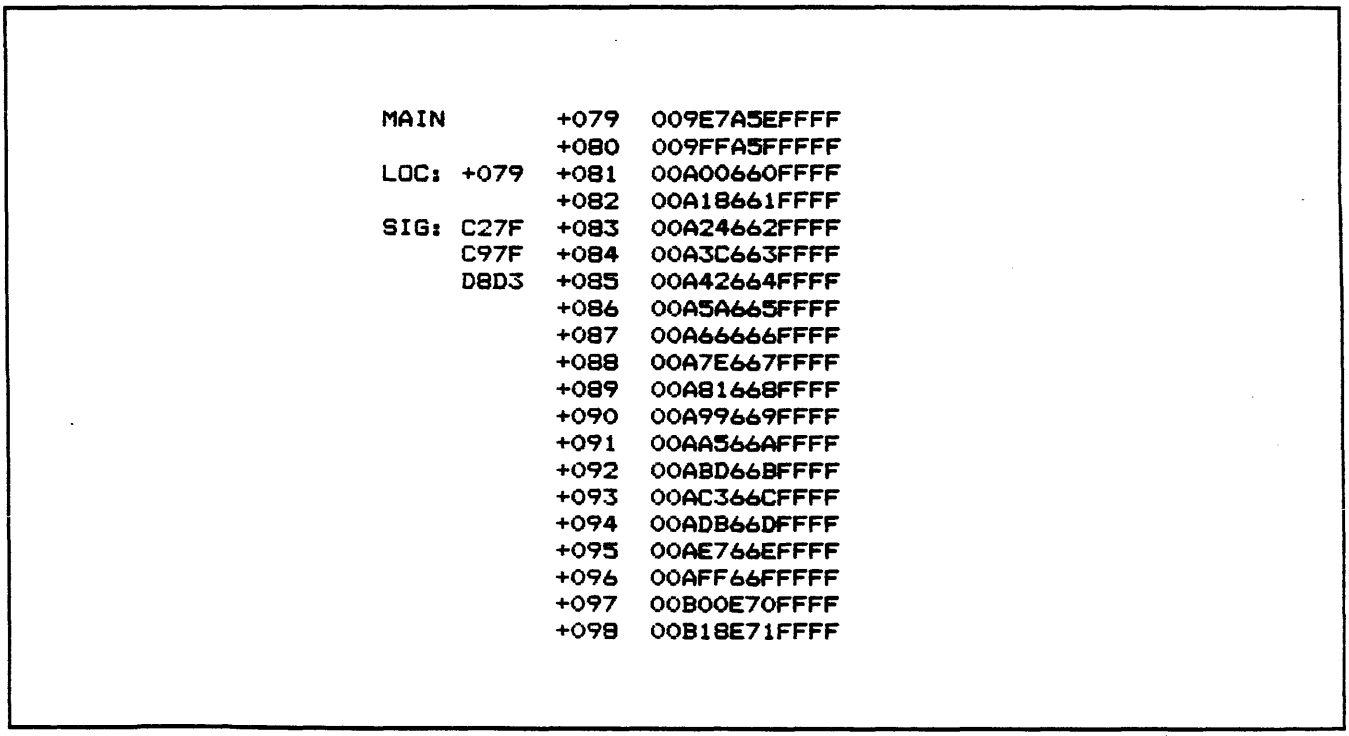


Figure 2-16: Result of Search on top Line of Display

2.3.5 Basic Timing Tests

Before starting this test, disconnect the M51A state probes from the test card.

Connect the two Model 80 Timing Probes to the 800 A, B Series mainframe. Use the Model 81A probes in the case of the Model 800 C, D, & E machines. Then connect these probes to the test card A and B outputs, respectively. The state probes may be left connected to the 800 Series mainframe.

Proceed as follows:

a. Press the F5 key to return to the Configuration List.

b. To select the 16-CHANNEL TIMING mode, press the SEL DOWN (F4) key. Call the menu with the TIMING (F1) key.

c. Select an external clock with a rising edge by pressing P. Use the NEXT (F2) key to step to the TRIGGER field. Specify a trigger word of 0-0-0-0-0-0-0-0 1-0-0-1-1-0-0-0.

   Use the NEXT key to step down to the PRE-TRIGGER field. Set this field to 00% using the appropriate keys. Leave all other menu entries set at the default value as shown in Figure 2-17. Models 800A and 800B menus differ slightly from this illustration.

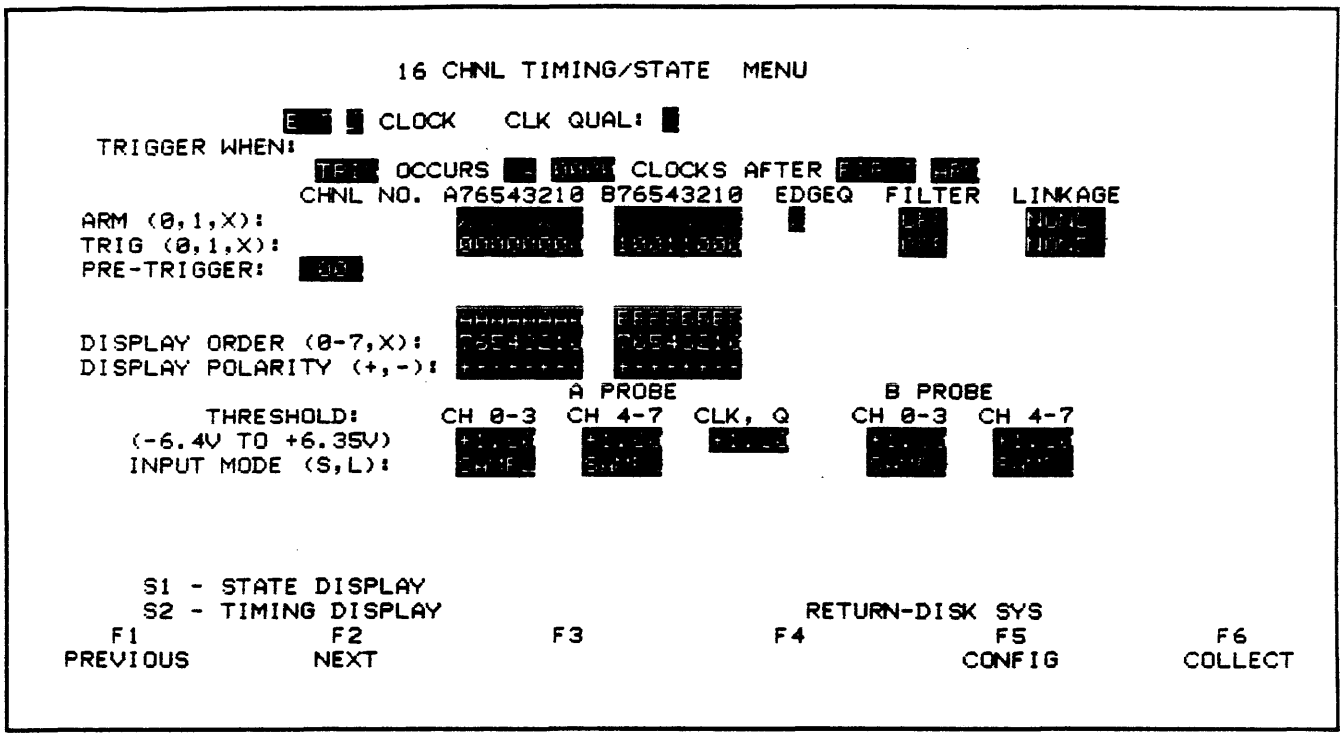


Figure 2-17: Model 800 C, D, & E Timing Menu

d. Press COLLECT (F6) key. When a data capture is complete, the screen fills with the timing diagram display. Refer to Figure 2-18.

e. The inverse video graticule represents the entire 1000 samples in the memory. Observe the small "00" indicator at the left end of the graticule is intensified. This indicates the 00% pre-trigger value set in previously. With 00% pre-trigger, the first word in the data collection (word 000) is the trigger word. The cursor reads the binary and hexadecimal values of each location in the data memory where the cursor is placed. Thus, the trigger word at cursor location 000 should be (0098) HEX . In Figure 2-18. this trigger word appears at the upper right-hand corner of the CRT.

f. Figure 2-18 also shows the 16 timing channels and the corresponding binary values at cursor location 000. The four most significant A channels (A7-A4) are at ground as described previously. The cross-hatched areas on certain channels indicate that data in the memory are occurring too close together. The current X1 magnification factor is unable to resolve this visually.

g. Sweep the expansion symbol, E, towards the middle of the CRT by pressing and holding F2. Stop the symbol at location 100 as indicated by the EXPAND FROM: readout in the lower right-hand portion of the CRT.

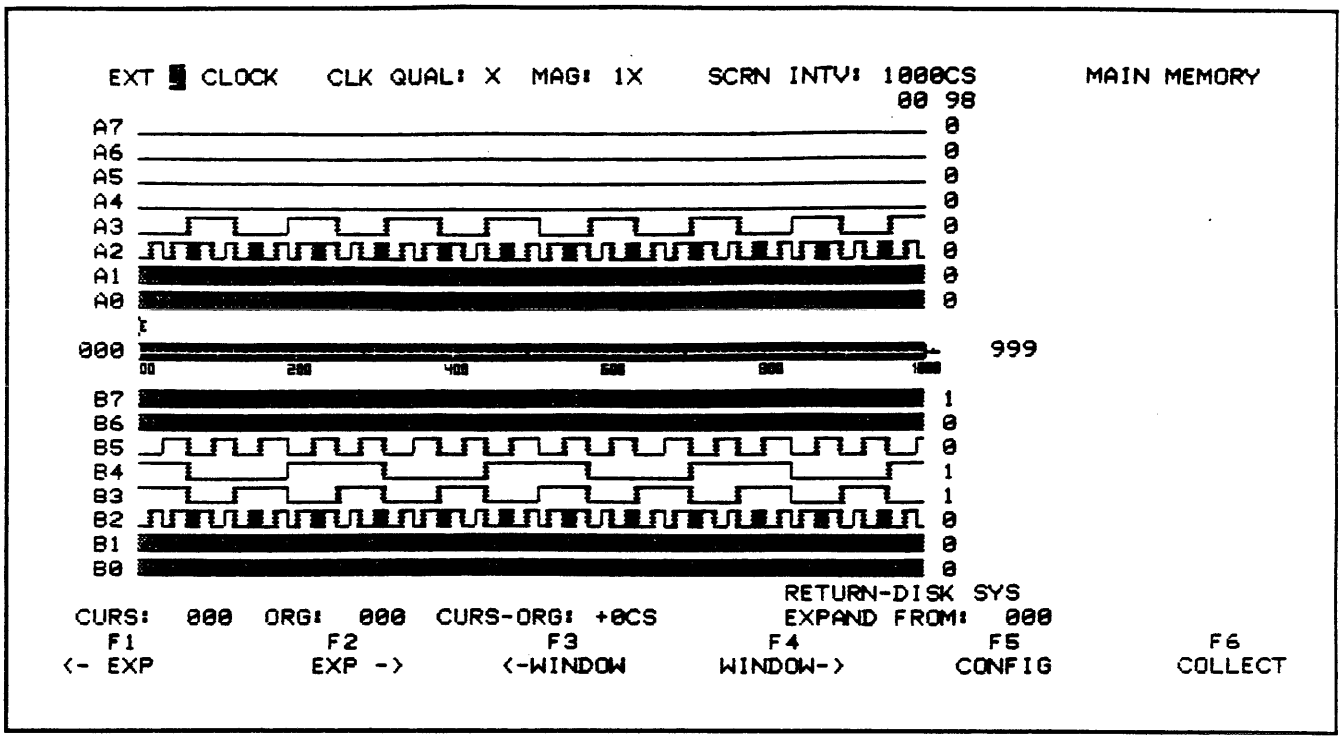


Figure 2-18: Timing Diagram Display

h. Next press the LABELS key. Try magnification factors between 2X to 20X using the 2 to 5 numeric keys as indicated in the LABEL MENU. After higher magnification keys are pressed, the inverse video indicator at the bottom of the screen reduces proportionately in size. This indicator shows the location and amount of timing data currently being displayed relative to the entire 1000-word data collection. At 20X magnification, note that the inverse video indicator is only 5% of the original (1X) size. The screen now displays timing data between memory locations 100 and 150. Refer to Figure 2-19. Finish by setting the magnification at 10X.

i. View other segments of the memory by pressing the <-WINDOW (F3) or the WINDOW -> (F4) keys and the REPEAT key simultaneously.

j. To quickly move the cursor from 000 to the left side of the screen interval at any magnification, press the L (LOCATE CURSOR) key. This is indicated in the LABELS menu. Bring the cursor to the center of the CRT by pressing the SPACE BAR. Overshoot can be remedied by pressing the BACKSPACE key.

k. This step is used to measure the relative time between the edges in two channels. Visually select an edge (rising or falling) in channel A2 and another edge (later in time) in channel B6. Step the cursor so that it aligns with the selected edge in Channel A2. Note the value of the cursor position indicator at the lower left of the screen. Now press the letter O to reset the origin from 000 to the current cursor location. The CURS-ORG indicator should now read +0CS, where CS stands for clock samples. (When an internal clock is being used, the indicator reads in units of time.) Next, step the cursor to the selected edge on channel B6. The CURS-ORG indicator will now directly read the time (in clock samples) between these two edges.

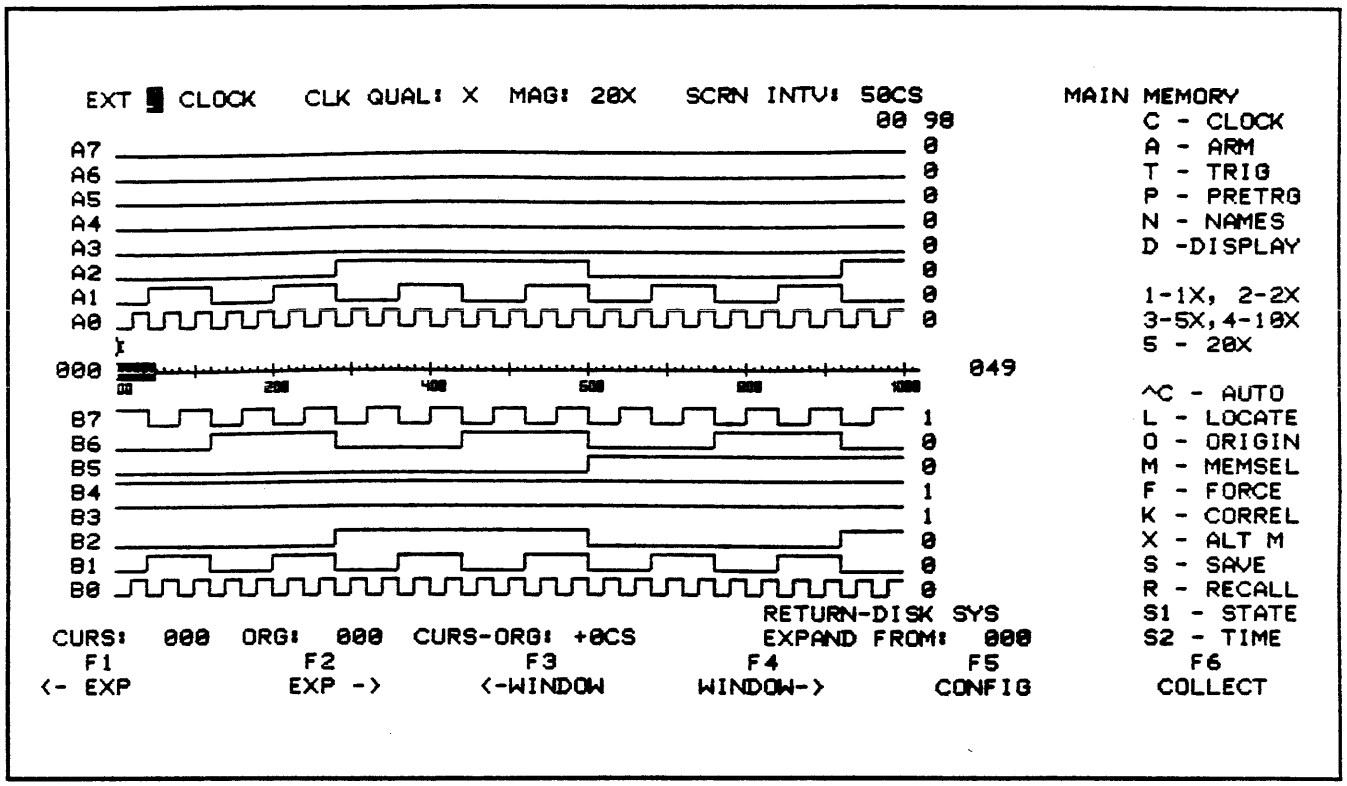


Figure 2-19: Timing Diagram with 20X Expansion

2.3.5.1 Saving Data/Correlation

To make a quantitative comparison of the 1000 bits sampled on each of the 16 channels between two separately made collections, NICOLET has built-in a correlation factor calculation.

a. Press the COLLECT key to take a new data collection. Then press the SAVE(S) key and observe the flashing SAVED message. To compare main and auxiliary data press K(CORREL) key. Note that a correlation factor of 1.000 is displayed at the right of each channel. This factor indicates that the 1000 bits in each main memory channel compares 100% with the 1000 bits in the corresponding auxiliary memory channel. Comparisons are done on a bit-for-bit basis. Refer to Figure 2-20. Thus, if a correlation factor of .995 were displayed, it would indicate that 5 bits out of 1000 were different, or 99.5% correlation.

b. Now short out the pad labeled 5 on the B side of the test card. While holding the short in place, press COLLECT. Now remove the short. To see which channel was affected by the short, press K again. Note that the correlation factor for channel B5 is significantly lower than 1.000. The other channels still have correlation factors of 1.000. This results from the use in this example of an external, synchronous clock from the test card. If the internal, asynchronous clock were used, the correlation factors of the other channels would probably never be exactly 1.000. This is due to normal sampling uncertainties.

c. In order to view the actual effect of the short on channel B5, press the M(ALT MEMORY) key. As shown in Figure 2-20, channel B5 should cycle between a 1 and a 0. Return to the main memory by pressing M. Also return to a 1X magnification by pressing the 1 key.

To view the timing data in a state format, press S1. The state data can be displayed in HEX, OCTAL, DECIMAL, BINARY or ASCII. Refer to Figure 2-21. Press the LABELS key to display the menu of formats available in this mode. Return to the timing diagram display by pressing S1 again.

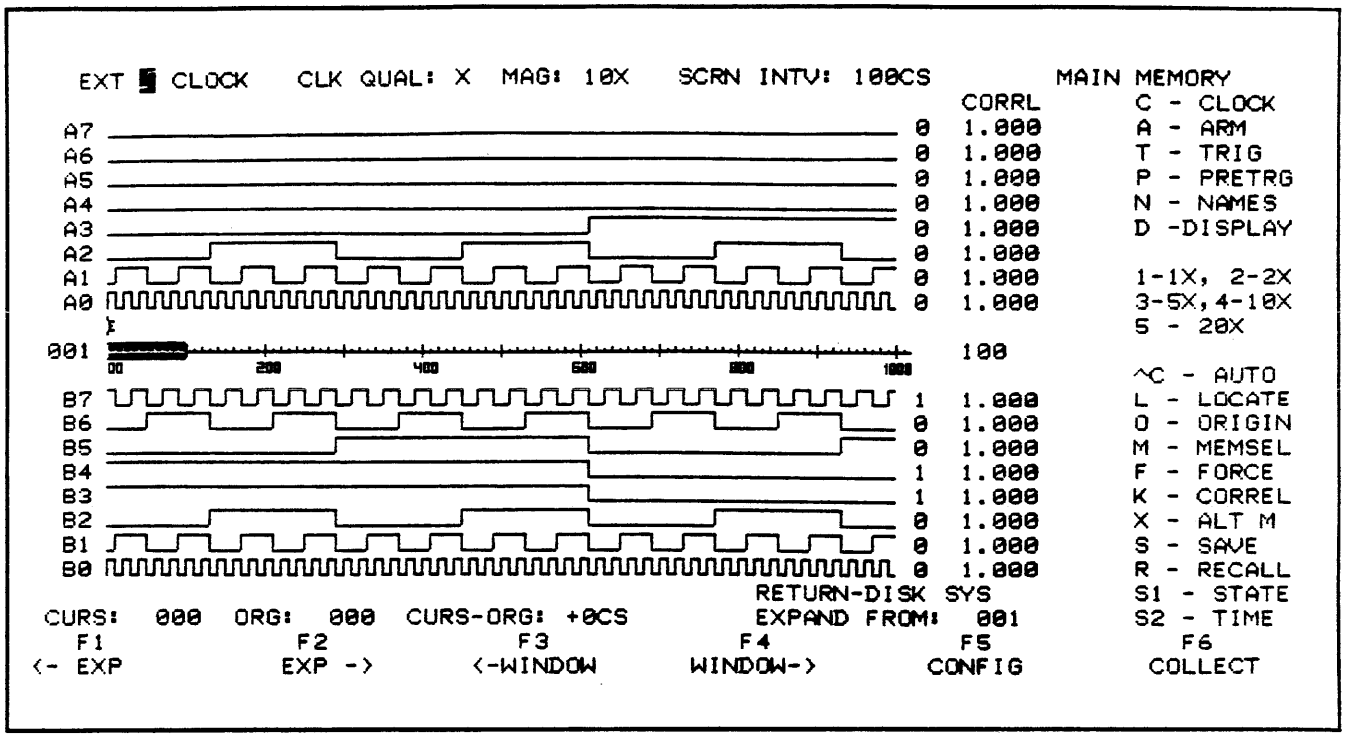


Figure 2-20: Correlation Display

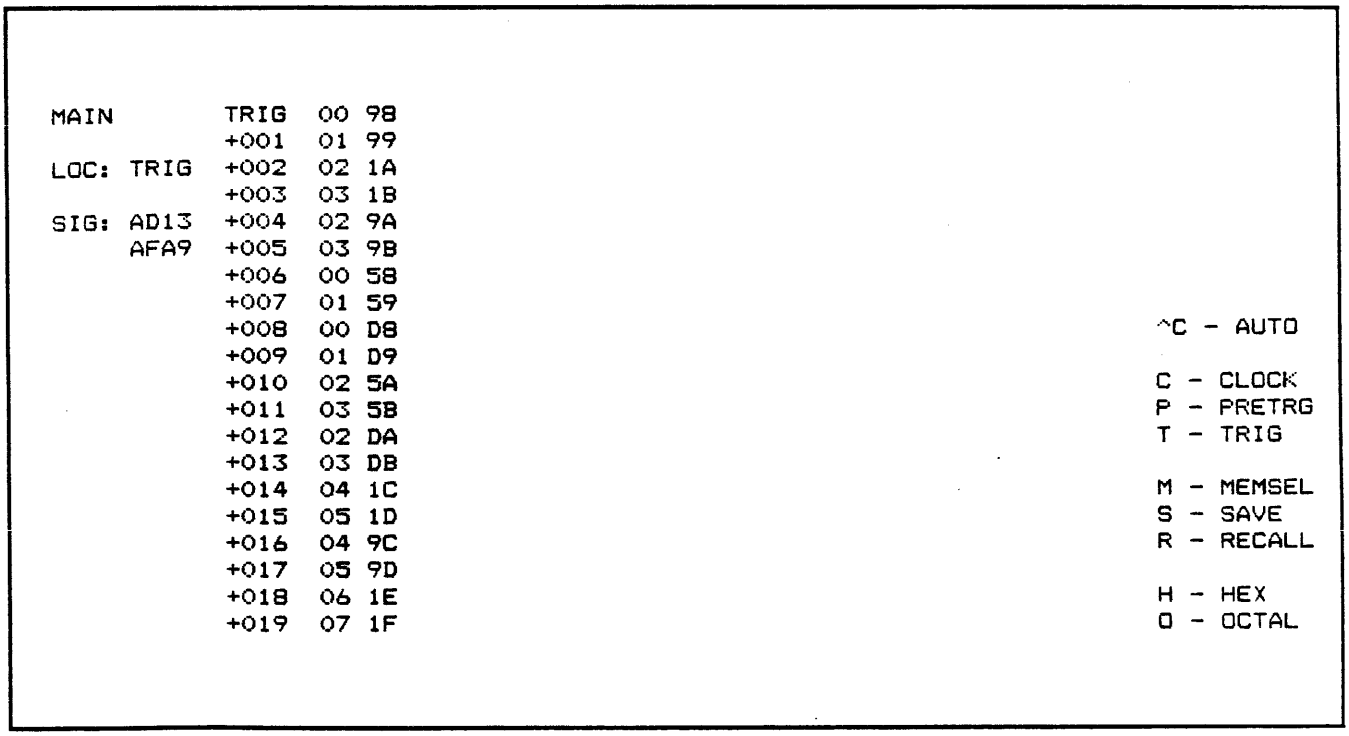


Figure 2-21: State Equivalent Display of Timing Samples

SECTION 3: CHASSIS, MOTHERBOARD, POWER SUPPLY, DISK DRIVE

3.1 Introduction ——— 3-1

3.2 Chassis Description ——— 3-1

3.3 Motherboard Description ——— 3-4

3.4 Power Supply Description ——— 3-6
- 3.4.1 Test Setup ——— 3-6
- 3.4.2 High Voltage Section ——— 3-8
- 3.4.3 Control Section ——— 3-9
- 3.4.4 Output Section ——— 3-11

3.5 Disk Drive Service ——— 3-12
- 3.5.1 Cleaning the Heads ——— 3-12
- 3.5.2 Removing the Disk Drives ——— 3-12

3.1 INTRODUCTION

Refer to the schematic diagrams, board layouts, interconnection diagram, and parts lists located at the end of this manual. Tables of connector pins versus signal names for all motherboard connectors are provided in the **Motherboard Connection** section. An alphabetical list of all interboard signals is included. The **Glossary** offers explanations for terms that may be unfamiliar.

3.2 CHASSIS DESCRIPTION

The chassis provides the supporting structure for the Front Bezel, Display Module, Card Cage Assembly, Rear Panel, and Power Supply. The top cover, a part of the chassis, provides protection to the internal components and adds structural strength to the complete assembly.

The units that will be discussed as part of the chassis group are; the chassis, cover, carrying handle, Mains Module, auxiliary power transformer, cooling fan, and the interconnecting wiring.

The Chassis consists of an aluminum bottom pan used to mount the front casting, rear panel, and extrusion rails. The front casting is joined to the rear panel by the longitudinal extrusion rails. The rails accept the side edges of the cover and bottom pan.

The shielded Display Module is mounted to the bottom pan by three threaded studs set into the bottom pan. The Card Cage Assembly is mounted to the bottom pan by three screws passing through the bottom pan. The cooling fan fastens to the rear panel by three screws through the rear panel. The auxiliary power transformer fastens to the rear panel by nuts on two threaded studs set into the rear panel. The Mains Module mounts into a rectangular hole in the rear panel with snap-in fasteners. The BNC connectors, Serial and GPIB connectors, mount onto the card cage and project through openings in the rear panel.

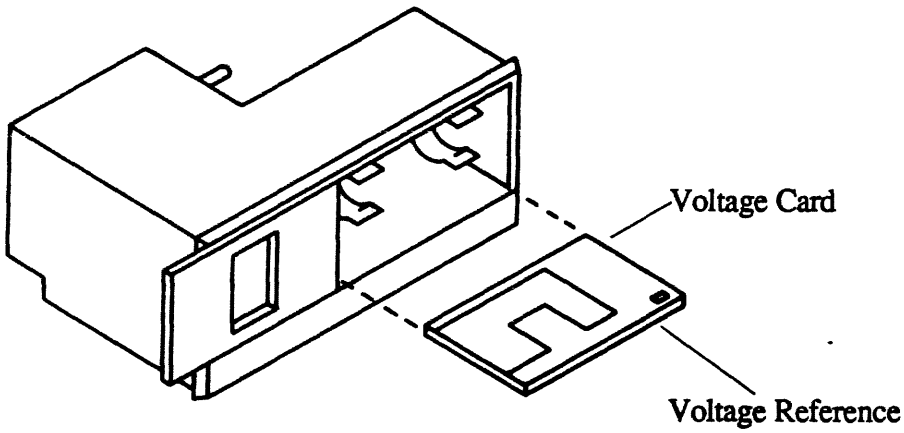
WARNING: Disconnect the AC power cord at the back of the chassis before removing the cover. The display module contains a very high voltage of 9 KV that can be lethal. Extreme caution must be used whenever power is applied to the Model 800 with the cover removed.

The cover folds around the top and halfway down the sides of the instrument. It fits into grooves in the extrusion rails. Clips that fit under the front casting secure the front of the cover. The cover is held in place at the rear by two quarter-turn fasteners that mate into fittings in a flange on the rear panel.

The carrying handle attaches to the extrusion rails. When the analyzer is in use, the handle can be folded underneath to prop the keyboard at a convenient working height.

The Mains Module is mounted in a rectangular cutout in the rear panel. It is held in place by snap-in fasteners attached to the sides of the module. Refer to the chassis wiring diagram.

A Voltage PCB in the Mains Module allows selection of the power mains voltage for the instrument. The sliding cover for this Voltage PCB can be opened only when the power cord is unplugged from the module. Voltage designators are etched in copper near the edges of the Voltage PCB. The voltage designator programmed by the PCB is visible on the upper rear edge when the board is in place. Refer to Figure 3-1.



Select as Appropriate: 100 V Nominal
115 V Nominal
230 V Nominal

NOTE: The card must be oriented so that the selected voltage can be read with the card installed.

Figure 3-1: Rear Panel & Voltage Select Card

CAUTION: Before applying power to the Model 800, make certain that the programmed Mains Voltage corresponds to the voltage being used, or serious damage to the internal power supply may result.

To change the voltage programmed - remove the PCB, change the orientation, and reinsert it. See Table 3-1 for the voltages available.

The power-mains fuse is located on the Mains Module just above the Voltage PCB. The rating of the fuse depends on the voltage programmed. See Table 3-1 for the required fuse ratings.

Selector Card	Operable Range	Fuse Required
100 V	90-110V	5A, 250V Slow Blow
115 V	105-125V	5A, 250V Slow Blow
230 V	210-250V	2.5A, 250V Slow Blow

Table 3-1: Power Source Requirements

The auxiliary transformer is mounted on two threaded studs set into the rear panel just above the Mains Module. The primary of this transformer acts as an autotransformer; supplying a nominal 115 VAC to the fan motor regardless of the programmed mains voltage. The secondary supplies 17 VAC to the Power Supply for an auxiliary supply circuit which is also independent of the mains voltage.

The cooling fan is mounted in a 4-inch round, air-intake hole in the rear panel. This hole is covered by a replaceable air filter. The fan motor is supplied with 115 VAC power from the auxiliary transformer. The fan draws air in through the rear panel air filter and exhausts it from the cover vents. This air flow lowers operating temperatures within the cabinet to safe levels. The air filter can be removed by loosening the thumbwheel screw. The filter should be cleaned by washing it in soapy water.

CAUTION: If the fan is not functioning, or if the air filter is dirty or otherwise obstructed, do not operate the Model 800. Doing so may result in serious damage to components through the instrument.

The interconnecting wiring is shown in the wiring diagram at the end of this section. All interconnections to the Display Module, Card Cage assembly, Front Panel, and Power Supply are made through connectors. Any of these units can be removed without unsoldering wires.

3.3 MOTHERBOARD DESCRIPTION

A Motherboard contains sockets, card guides and supporting structure for up to 11 individual PC boards.

Refer to Motherboard schematic **#166-0123-01** and board layout drawing **#615-0123-01.** The PCB slot assignments are fixed and the boards are keyed to fit into the correct slots. The location and part numbers of the boards are listed in Figure 3-2. The Model will determine which boards are inserted into the slots. The Model-800 E has empty slots C-F, and Model-800 A has an empty slot F. All models not equipped with options may have empty slots J-K .

CAUTION: Do not attempt to force a PCB into an incorrect slot or damage to the connector or PCB may result.

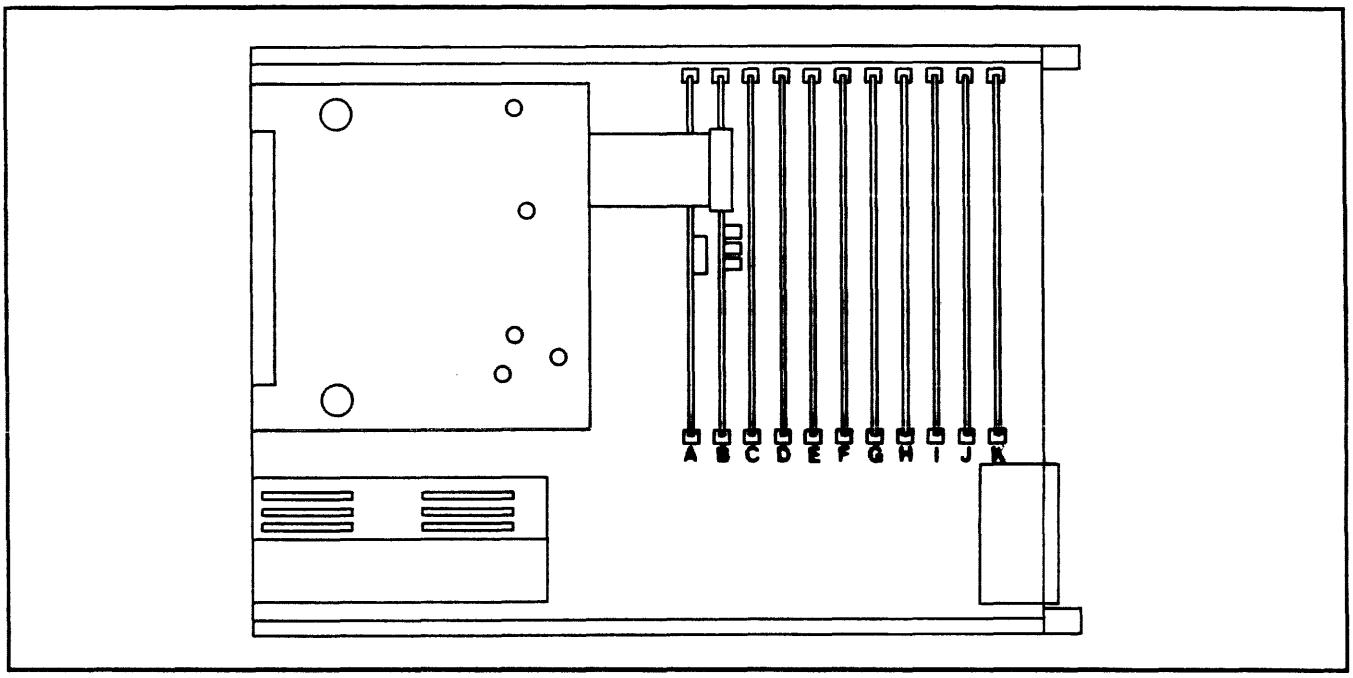


Figure 3-2: Circuit board locations

SLOT	CIRCUIT BOARD	PART NUMBER / MODEL		PART NUMBER / MODEL	
A	Processor	615-013001	A,B	143-0130-001	C,D,E
B	RAM DISK	615-011201	A,B *	143-0112-001	C,D,E *
C	State Control	615-036901	A,B,C	143-0361-001	D
D	State Memory-C (LSB)	615-036801	A,B,C	143-0360-001	D
E	State Memory-A (MSB)	615-036801	A,B,C	143-0360-001	D
F	State Memory-B	615-036801	B,C	143-0360-001	D
G	Timing Control	615-007101	A,B	143-0313-001	C,D,E
H	Timing Memory-A	615-006503	A,B	143-0312-001	C,D,E
I	Timing Memory-B	615-006504	A,B	143-0312-001	C,D,E
J	Waveform	615-007201	*	143-0072-001	*
K	Counter-Timer/SA	615-009901	*	143-0099-001	*

*** - Optional, may be equipped.**

NOTE: Any of the three State Memory boards are identical and may be interchanged. The two 100 MHz Timing Memory boards contain different decoder PROMs U52. The 200 MHz Timing Memory Boards have different PROMs in U46. (See appropriate section of this manual).

The PROM marked 4035-14 is required for the 100 MHz Timing Memory Board A in slot H.

The PROM marked 4035-15 is required for the 100 MHz Timing Memory Board B in slot I.

The PROM marked 4069-1C is required for the 200 MHz Timing Memory Board A in slot H.

The PROM marked 4069-2C is required for the 200 MHz Timing Memory Board B in slot I.

The Clock Qualifier Gate (U6) and the Clock Multiplexer (U2), both part of State Control, are contained on the Motherboard. These circuits are described in the **State Control Board** section.

Additional circuitry (U1, U3, U5) interfaces the link control signals and provides additional clock selection control. Components U4, U7, and U11 are shown on the board layout drawing and on the Motherboard schematic. The signals that must be sent to the Keyboard are fed to connector J1. This connector mates with a flat ribbon cable connected to the Keyboard.

The PC Board sockets are interconnected as described in the Motherboard Connections section. Some inversion of address lines to S1 is done so that electrically identical boards (State Memory) can occupy unique address spaces.

3.4 POWER SUPPLY DESCRIPTION

The Power Supply, mounted to the bottom pan of the instrument, is enclosed in a protective housing. The Power Supply is a pulse-width modulated, half-bridge, 25 KHz switching circuit operating directly off the AC power line. It supplies ±5 V and ±15 V to the Keyboard and Card Cage, +12 V to the Display Module, and +5 V or +12 V to the disk drive. It also provides very effective overvoltage and overcurrent protection for both the Power Supply itself and the circuits that it supplies.

Refer to schematic **#127-0122-001**. The major functional units of the Power Supply circuit are the High Voltage Section, Control Section and Output Section. These units are discussed further in the following subsections. Refer to assembly drawing **#143-0122-001** for major component location, disassembly and assembly information. Assembly drawing **#126-0122-201** depicts the PC Board component locations.

WARNING: This power supply circuit is connected directly to the AC mains with no intervening isolation transformer. When power is applied, lethal voltages are present. Only qualified service personnel familiar with line operated switching power supplies should undertake service of this supply, and then only with the following isolating test setup description Failure to observe these precautions may result in serious injury or death.

3.4.1 Test Setup

The AC input power is fed directly from the mains to rectifier circuit DB1 without an intervening isolation transformer. Therefore, it is essential that an isolation transformer be incorporated in the test setup as shown in Figure 3-3.

WARNING: Measurements or tests undertaken without the use of an isolation transformer may result in serious injury or death.

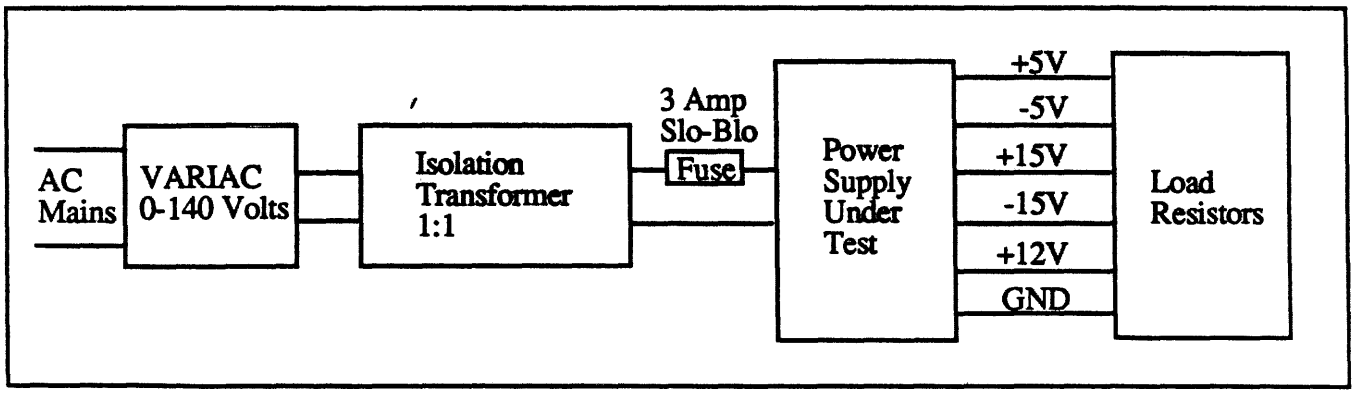


Figure 3-3: Power Supply Test Setup

To access the Power Supply:

NOTE: Read the entire procedure once before starting.

a. Disconnect the power cord and wait three minutes after the power is turned off to allow the capacitors to fully discharge.

b. Remove the top cover by loosening the two quarter-turn fasteners at the rear of the cover and sliding cover back.

c. Remove the two nuts holding the power supply cover. These are located between the power supply cover and disk drive bracket. Be careful not to damage the ground straps connected to the grounding stud.

d. Turn the unit over to expose the bottom cover and remove the two screws near the rear that hold down the power supply cover. The cover may now be removed, exposing the supply.

To remove the supply:

a. Unplug the power cords connecting the power supply to the Disk Drive, CRT and main Motherboard.

b. Remove the six screws mounting the power supply heatsink to the bottom pan. These may be accessed from the bottom.

c. The supply is now free and may be lifted up. Complete the removal by unplugging the six-conductor AC plug.

CAUTION: Do not risk damage to valuable circuit boards by using the analyzer as a test load for the sake of convenience. Use resistors as described n the following paragraph. Note that no load is needed on the +12V supplies unless they are specifically under investigation.

To load the power supply outputs:

a. Obtain a mating connector for P12 (see parts list). Make an adapter to connect the load resistors between the outputs and ground returns. Load resistance values are shown below:

MINIMUM LOADING			
OUTPUT	CURRENT	RESISTANCE	RATING
+5 V	5 A	1 ohm	25 W
-5 V	5 A	1 ohm	25 W
+12 V	----	(no load required)	
+15 V	200 mA	75 ohms	5 W
-15 V	200 mA	75 ohms	5 W

b. Bring power to the Power Supply by connecting the Mains Module **through an isolation transformer** to the power mains.

3.4.2 High Voltage Section

The High Voltage Section consists of the following: DB1, a VH 648 bridge rectifier; Q1 and Q2, Motorola MJE13007 power switching transistors; CR1,2, 1N3600 diodes; CR3,4, 1N4637 diodes; transformers T1 and T2; thermistor R1; and various resistors and capacitors.

This circuitry converts a nominal 100, 110 or 220 VAC, 50-60 Hz mains voltage to a center-tapped, nominal ±162 DC voltage. This DC voltage is converted to a fixed-frequency, pulse-width modulated, AC voltage across T1. The conversion is performed by the action of Q1, Q2, T2 and the control section. The output voltages of T1 are nominally 5 and 15 VAC RMS at a nominal frequency of 25 KHz.

Input from the power mains is sent directly to the rectifier DB1 with no intervening isolation transformer. Consequently, all components within the High Voltage Section are at mains potential! **Please see preceding Warnings and Cautions!** A Mains Module contains a Voltage PCB that is used to select the AC mains voltage that will be used to power the analyzer. This was described previously under **Chassis**. The three selection options are 100, 110 and 230 VAC.

If a mains voltage of 230 VAC is selected, it is applied across input pins P1-2 and P1-6. DB1 acts as a full-wave bridge rectifier and produces a nominal 325 V. This DC voltage is filtered by filter capacitors C3 and C4 connected in series. The junction of C3 and C4 is a center tap of the 325 V. This provides ±162 V for the switching circuit and transformer T1. R3 and R4 stabilize the center tap and act as bleeders. C5 and C6 are for EMI reduction. Fuse F1, a 3 amp Fast-Blow type, provides circuit board protection in case Q1 or Q2 shorts out. Any failure of Q1 or Q2 will happen faster than the fuse can blow.

If a mains voltage of 100 or 110 VAC is selected, it is applied across input pins P1-2 and P1-3. With this connection, DB1 acts as a full-wave doubler rectifier. DB1 produces a nominal 325 V across series-connected C3 and C4.

By means of transformer T2, the Control Section turns transistor Q1 ON and OFF in alternation with Q2. The cycle time is a nominal 40 microseconds. Note that Q1 and Q2 are never ON at the same time. This alternately applies +162 and -162 V across the primary of transformer T1. The resulting AC voltages across the secondaries of T1 are rectified and averaged in the Output Section. The longer Q1 and Q2 are ON during each cycle, the higher the DC output voltages from the Output Section. The width of the ON-pulse thus provides a means of voltage control. This is used by the Control Section for voltage regulation.

Capacitor C8 blocks any DC bias that might otherwise result from a mismatch between Q1 and Q2. Components R8 and C9 reduce ringing and transient spikes. CR1, R4, C10 and CR2, R6, C11 speed up the turn off times for Q1 and Q2.

3.4.3 Control Section

The Control Section consists of U1, a National DS3632 dual peripheral driver; U2, a Silicon General SG3524 regulating pulse-width modulator; Q4, a 2N3904 transistor; Q3, a 2N3905 transistor; Q5, a Motorola MCR101 SCR; CR5-7,9,10,17, all 1N3600 diodes; CR8, a 1N588 Zener diode; and DB2, an MDA100 bridge rectifier.

This circuit provides drive pulses through transformer T2 that switch Q1 and Q2 ON and OFF. It controls the width of these drive pulses in response to voltage feedback from the Output Section. The circuit provides good voltage regulation of the output voltages. It also detects any overcurrent condition, and reacts by shutting down the Power Supply.

The nucleus of the Control Section is the circuit U2. It is powered by a nominal +20 V from the bridge rectifier DB2. DB2 is fed, via P1-1 and P1-4, with a nominal 17 VAC at 50-60 Hz from a small transformer, T3. T3 is mounted on the rear panel, refer to Chassis Wiring diagram. Circuit U2 produces drive pulses at outputs CA and CB (pins 12 and 13). These are used, via U1 and transformer T2, to turn Q1 and Q2 ON and OFF. The repetition rate of the pulses is established by an oscillator in U2. The frequency is set by the values of R18 and C16 at pins 6 and 7 to a nominal 50 KHz. There are two U2 drive pulses for one cycle of the Q1-Q2 switching circuit. This sets the switching frequency of the power supply to a nominal 25 KHz.

The drive pulses from U2 act as follows. When CA is low and CB is high, U1 output 5 is turned OFF and output 3 is turned ON. The +20 V applied through R9 drives a current through winding 2-3 of T2. The current is driven in the direction making the dot end of the winding positive. This current in 2-3 induces voltages in windings 7-4 and 6-1, making their respective dot ends positive. The connections to these windings are such that Q2 is turned ON and Q1 remains OFF. The base of Q1 is driven even further negative.

The -162 V applied to Q2 drives current through T1 7-5 and T2 8-5 in the direction making the dot end of 8-5 positive. This regenerative action reinforces the base drive to Q2. Transformer T2 acts as a current transformer. Thus, the base drive current to Q2 is proportional to the T1 primary current through T2 8-5. The current ratio is such that Q2 is assured of being fully ON and out of the linear region.

Q2 is turned OFF again by the blanking pulse within U2 that brings CA high with CB. This turns U1 outputs 3, 5 ON, short circuiting T2 2-3 and turning OFF Q2 drive current at T2 6-1. This short circuit condition lasts for the duration of the blanking pulse, a nominal three microseconds. During this time Q2 and Q1 are both forced to remain OFF. This ensures that Q1 cannot be turned ON until Q2 is OFF. The turn-on time of these transistors is shorter than the turn-off time. Without a long enough blanking pulse, it would be possible for Q1 to turn ON while Q2 was still ON. For example, under conditions of low mains voltage and a compensating maximum pulse width for the switching circuit. This would put a short circuit across the +162 V supply and cause component damage.

The next half of the 20 KHz switching cycle starts with the leading edge of the blanking pulse. Any drive pulse that would turn Q1 ON is inhibited within U2 for the duration of the blanking pulse. At the end of the blanking pulse, the voltage regulation circuitry in U2 is again in control. That circuitry determines when to start the Q1 drive pulse, and CB is brought low. This turns U1 output 3 OFF and drives current through 2-3 of T2. The current is driven in the direction to turn Q1 ON and hold Q2 OFF. The rest of the action is analogous to that of the first half cycle.

Inputs to the U2 voltage regulation circuit are V+, pin 2, and V-, pin 1. The V+ input is supplied with a nominal +2.5 V reference voltage. The reference voltage is obtained, via R15, R17 and potentiometer R16, from regulated +5 V of U2, pin 16. Pin 16 output is also used as a source of +5 V power for other parts of the circuit. The V- input is supplied with a nominal +2.5 V of negative feedback via R32, R27 and R25. This is derived from the regulated +5 V output of the power supply. R28, R29 and C19 provide gain control and phase lag to the feedback amplifier. Lead compensation for the +5 V feedback signal is provided by C28. If the feedback voltage at V- exceeds the reference voltage at V+, U2 acts to reduce the drive pulse width. This reduces the output voltages of the power supply. If the feedback voltage at V- falls below the reference at V+, the action is the opposite. This regulating action does not appreciably affect the 25 KHz switching frequency, only the ON times of Q1 and Q2.

The variable resistor R16 is adjusted so that the Power Supply output voltage at the +5 V test point is +5.1 V ± 0.05 V. This adjustment should be made with both Power Supply output plugs connected to the analyzer, all circuit boards in place, and after the analyzer has had power applied for a period of 10 minutes.

As mentioned previously, the U2 clock frequency is set to a nominal 50 KHz by R18 and C16. The clock signal is a short-duty-cycle pulse that is also used as the blanking pulse. The pulse width is approximately 0.5 microseconds, which is not enough for the blanking pulse in this application. The output of the clock oscillator circuit is made available at pin 3. The Q3-Q4 circuit connected to this pin is used to stretch the clock/blanking pulse to a nominal three microseconds. This provides blanking protection for Q1 and Q2.

The SCR Q5, Zener diode CR8, and diodes CR6 and CR7 constitute an overcurrent shutdown circuit that functions as follows. A component of the voltage across winding 2-3 of T2 is proportional to the current in winding 8-5. Normally the voltage across winding 2-3 results in less than 7.5 V at the cathode of CR8 via CR6 or CR7. If the rated current in winding 8-5 is exceeded, the voltage at CR8 cathode will exceed 7.5 V and CR8 will conduct.

When CR8 conducts, SCR Q5 is triggered and shorts both sides of winding 2-3 to ground through CR6 and CR7. This holds both Q1 and Q2 OFF, shutting down the power supply indefinitely until the power is turned OFF. When power is turned ON, the supply will function normally if the cause of the shutdown has been removed.

Diodes CR17 and CR5 serve to clip any ringing voltages that appear at winding 2-3 of T2.

3.4.4 Output Section

The Output Section consists of VR1, an LM340T-12 +12 V series regulator; VR2, an LM350K +12 V regulator; DB3, a Varo VJ248X bridge rectifier, CR13 through CR16, all Schottky rectifiers; CR12, a 1N957B 6.8V Zener diode; and CR11, a 1N721A 20 V Zener diode.

This section contains rectifier and filter circuits for the four major output voltages of +5, -5, +15 and -15 volts. These circuits are fed with 25 KHz pulse-width modulated power from secondary windings on switching transformer T1. This section also contains a low-power series regulator, VR1, that provides +12 V for the Display Module. A second regulator, VR2, provides +12 V for the disk drive circuitry. Both low-power regulators are fed from the +15 V supply. The current ratings for these supply voltages are as follows:

VOLTAGE	MAXIMUM CURRENT
+5V	20.0 A
-5V	12.0 A
+15V	1.0 A
-15V	1.0 A
+12V CRT	1.5 A
+12V DISK	3.0 A
+5V DISK	1.0 A

DB3 acts as a full-wave bridge rectifier for both the +15 and -15 V supplies. It is fed from secondary windings, 11-1 and 10-2, on the switching transformer T1. L1-C23 and L2-C24 act as pulse-averaging and ripple filters for the +15 V and -15 V supplies, respectively. R31 is a bleeder for the -15 V supply. R30 and C20 suppress transient ringing in the secondary.

Series regulator VR1 drops part of the +15 V output to +12 V for the Display Module. C22 provides additional filtering and decoupling for the +12 V.

The two diodes CR13 and CR14 are rectifiers for the +5 V supply. They are each fed from the center tapped secondary windings of switching transformer T1. The cathodes of the diodes are connected to the L3-C25-C26 pulse-averaging and ripple filter. R33 and C29 suppress transient ringing in the 5 V secondaries.

The -5 V output circuit is the same as the +5 V, except for the differences to accommodate opposite polarity.

Zener diodes CR12 and CR11 form a shutdown circuit for over-voltage protection. If the +5 V output voltage rises above +6.8 V, Zener diode CR12 conducts. This causes SCR Q5 to trigger and shutting down the supply. CR11 provides similar overvoltage protection for the +15 V output. The minus voltages are not protected explicitly, but have protection due to the cross regulation with the positive voltages.

The feedback voltage for the Control Section is applied from the +5 V output through R32. The +5 V output is therefore tightly regulated. The other output voltages are regulated, but to a lesser degree than the +5 V output. The +12 V outputs benefit from the additional regulation afforded by the series regulators VR1, VR2.

L5 and C27 provide a second L-C filtering stage for the +5 V supply to the Disk Drive. This reduces noise to the drive via power supply coupling.

3.5 DISK DRIVE SERVICE

When the drives are used repeatedly in an excessively dirty environment, it is recommended that cleaning of the magnetic head surface be done periodically with a commercially available cleaning disk. Under normal circumstances this is not necessary. Since it is difficult to properly clean double-sided drives by a direct cleaning method (isopropyl alcohol and cotton gauze) without damaging the internal gimballed mechanism, use a high quality **Double-Sided** Cleaning Disk. Use of a single-sided disk can damage a head.

3.5.1 Cleaning the Heads

1. Start the spindle motor by applying power to the unit and pressing the ESCape key. Install the **Double-Sided** cleaning disk so that side 0 (the bottom side) and side 1 (the upper side) are both cleaned simultaneously. The head is loaded and cleaned when the drive door is closed. Engage for 10 to 30 seconds.

2. Open the drive door and remove the cleaning disk. The most appropriate cleaning time is different for each type of cleaning disk used. Follow the manufacturers recommendations.

3. To avoid concentration on a specific track (the system track read at cold boot), it is now recommended that the RESET button be depressed and held for three seconds. This effectively performs a" power-on reset".

4. Insert a normal operational disc and boot the DOS by pressing the ESCape key. Select a file (utility or data/test save file) and access those tracks by calling it up. Open the drive door in the midst of the read operation, remove the disk and reinsert the cleaning disc. This is to ease repeated wear-and-tear of a single "track" on the cleaning disc.

5. Eject and remove the cleaning disk and store carefully. Never use a damaged cleaning disk.

3.5.2 Removing the Disk Drives

The disk drives are removed by disconnecting the plug-in cables and ground strap, then removing the four mounting screws. Replacement is made in the reverse order from removal. The step-by-step removal procedure is as follows:

1. Remove the power cord and top cover as previously described.

2. Disconnect the two plug-in cables at the rear of the drive. Note the orientation of the cable connectors.

3. Disconnect the ground strap.

4. Tilt the 800 Series on its rear panel feet. The disk drive is held in place with four screws, two on top and two on the bottom. The bottom screws are reached through access holes in the bottom cover. Remove the two bottom screws.

5. Tilt the 800 Series back into its normal bench position. Remove the two top screws. Carefully remove the drive from the chassis.

SECTION 4: KEYBOARD

4.1 Keyboard ——— 4-1

4.2 Removal and Disassembly ——— 4-2

4.1 KEYBOARD

Refer to schematic drawing **166-012101.** Keystrokes from the matrix type keyboard are encoded by the MSM3914 (U7). The encoder clock is generated by a timer IC (U8) configured for a 30 KHz frequency. The X0-X3 signals output from encoder U7 are applied to two decoders (U5,U6). These decoders produce the scan signals in a 16x8 matrix. Lines Y0-Y7 are the matrix common input signals to the encoder. Each line is pulled up by a 4.7K ohm SIP (RP2). When a key is pressed, the input line common to that key in the matrix is encoded by U7. Signal **SAMPLE** is generated and stays true until the key is released.

A Schmitt-triggered NAND gate (U10) generates a 10 Hz clock rate. When a key is pressed, one-shot U9 fires for approximately one second. This prevents the 10 Hz clock from passing through U10. The signal is then ANDed at U10 with **SAMPLE-**, indicating the key is still depressed. The signal is inverted by U3 and then clocks U2. The Q- is output low and then inverted by U3 before going to the Motherboard. The coded data at PROM U4 is strobed off the board to the 8155 on the processor PCB. If a key is depressed longer than one second, U2 is clocked again causing a repeated strobe. When the 8155 receives the strobe and data, signal **DATA ACCEPTED** is sent back to the keyboard. This clears U2, setting Q high and **SAMPLE ACC** true. This sequence of operations confirms the reading of the pressed key. Output data lines and strobe are pulled up by a 1K x 9 SIP (RP1). Under normal key operations, pin 1 of U3 is held high, thereby doubling the repeat key function.

The repeat function uses the REPEAT key, that grounds U3 (pin 3), thus causing a clock to U1. As long as the REPEAT key is depressed, one-shot U1 will fire a 12 ms pulse. The 12 ms pulse is decoded by U5 and U6. The MSM3914 will cause the reading to be repeated while the key is depressed.

The SHIFT, CTRL and CAPS LOCK keys are read by PROM U4. A processor reset also is configured on the keyboard. Pressing the RESET key (RED) causes one-shot U1 to output a one second pulse. The key must be depressed for two seconds, holding off **CLEAR** until the one-shot fires. This sets Q of U2 high and pin 10 of U3 low, thus resetting the processor. When the key is released, **CLEAR** at U2 goes low, clearing U2, resetting Q low and pin 10 of U3 high.

4.2 REMOVAL AND DISASSEMBLY

The keyboard may be removed from the main chassis by the following steps:

a. Remove the retaining clips of the two hinges.

b. Unplug the 20 conductor connector.

c. Slide the keyboard off the hinge pins.

The keyboard may be extended by a remote ten foot cable (consult factory) for remote operation.

To disassemble the keyboard, remove the screws mounting the hinges and the rubber mounting feet. Remove the clasp retainers on the front lip of the keyboard housing. This will permit the entire keyboard assembly, including the top keyboard bezel, to be removed from the backing.

To remove the bezel, it is necessary to remove the screws that secure the extrusions to the PCB. Reassembly is accomplished in the reverse manner.

SECTION 5: CRT DISPLAY MODULE

5.1 Introduction ——— 5-1

5.2 AC Line Frequency ——— 5-1

5.3 CRT Adjustment Procedure ——— 5-2

5.1 INTRODUCTION

The display module is a nine-inch CRT monitor. It accepts a composite video signal sent from the Video Display board and produces a raster-scan video display. The BRIGHTNESS and CONTRAST controls are located on the front panel, and internal controls are provided for maintenance adjustments. The input power required by the module is provided by the 800 Series power supply.

WARNING: High voltage is used in the display module. Observe extreme caution when power is applied and the cover is removed.

5.2 AC LINE FREQUENCY

The Display Module does not use any line power directly. Primary line power is brought into the 800 Series to operate the power supply. As a consequence, there are line-frequency fields within the instrument that may produce minor interaction with the CRT display. To minimize interaction, the frequency of the vertical sync signal is adjusted as closely as possible to the line frequency. The vertical sync signal is produced on the Video Display board. It is contained in the composite video signal sent to the Display Module from the Video Display board.

The adjustment of the vertical sync frequency is automatically made by the Control Program at power-on time. For details, refer to the Sync Generator discussion in the Video Display section.

5.3 CRT ADJUSTMENT PROCEDURE

The Display Module, and in particular the CRT, is subject to component aging and may require occasional adjustment. Any adjustments that are found necessary should be made in accordance with the following instructions.

WARNING: The display module contains a very high voltage of 9 KV that can be lethal. The following procedures should be undertaken only by experienced technical personnel familiar with television or CRT monitor adjustment procedures.

WARNING: Remove all power from the instrument before continuing.

a. Unplug the power cord.

b. Loosen both quarter-turn screws at the rear of the top cover.

c. Remove the cover by sliding it to the rear of the instrument and upwards.

d. Remove the display module securing screws and cover to gain access to the adjustments. Refer to Figure 5-1.

Note: Early production units necessitate removing the module from the chassis. Refer to step e for these units.

e. Early production units require that the display module be removed from the chassis. This allows access to the screws holding the module cover. To remove the display module, use a long 8" socket extension to reach the three nuts as shown in Figure 5-1. Carefully remove the display module from the chassis sufficiently to loosen the module cover screws and cover. If necessary, temporarily disconnect the wires to obtain slack required for removal.

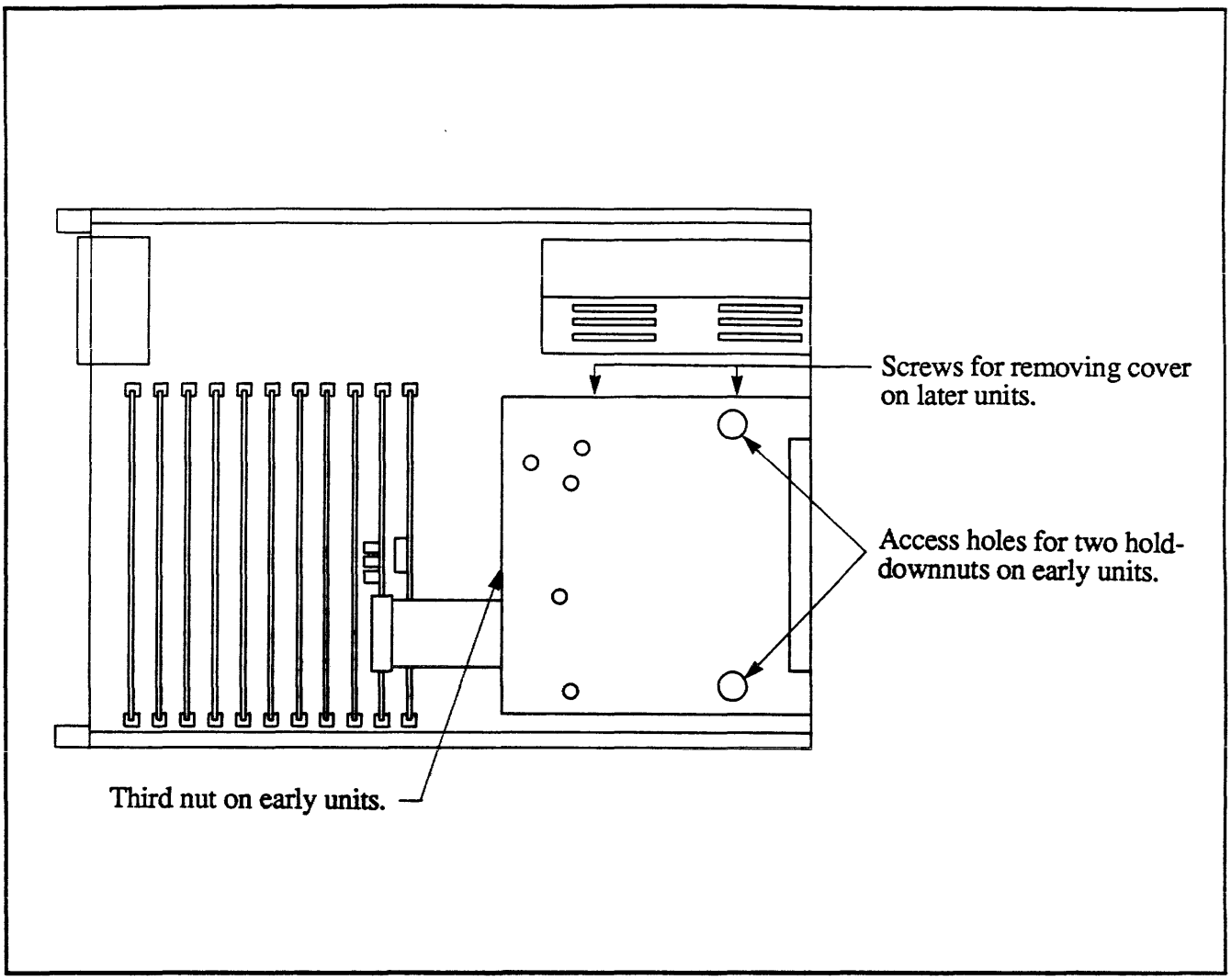


Figure 5-1: CRT Module Cover Removal

WARNING: Make all adjustments with plastic adjusting wands designed for this purpose. Do not use metal screwdrivers or any metal tool. Lethal voltages are present which can cause injury or death.

Replacement monitors are supplied by Nicolet with adjustments already made. Only minor touch-up of horizontal and vertical hold may be necessary after installation.

Before installing a replacement monitor, ALWAYS check for 12 volts at the heavy red and black leads on monitor PCB. Voltages lower than 11.5 V or more than 12.5 V will distort the display.

Touch-up adjustments are made as follows (Refer to Figure 5-2):

a. Verify that the three disconnects are properly connected. (Power, external video and processor.)

b. Turn power on, wait a few seconds for the beep, then depress the BREAK key for the processor test.

c. Turn the EXTERNAL BRIGHTNESS (on bracket) control fully on (clockwise). Then turn the EXTERNAL CONTRAST adjust to about one-half rotation or midpoint. At this point a display of some sort will appear on the screen.

d. Coarse adjustment of the HORIZONTAL HOLD must be made with a **plastic screwdriver**. Turn the HORIZONTAL HOLD adjust in either direction. The display screen will display diagonal lines. Turn the control in the opposite direction, diagonal lines will appear in the other direction. The coarse adjustment is between these two points. The display will appear to be running straight up and down.

e. The display may be stable, or appear to be rolling vertically. Using the **plastic screwdriver**, adjust the VERTICAL HOLD control until the display is rolling slowly downward. Turn the VERTICAL HOLD slightly counterclockwise until the display appears to snap into a locked position. The display should be locked and stable at this time, showing "Processor Test".

f. Note REVERSE on the display, located about one third down the screen. Adjust the front panel CONTRAST control until this block is brightest, just before edges of block start to distort. Any distortion of this block means the contrast is set too high. The brightness now may be reduced slightly for HALF LIGHT adjustment.

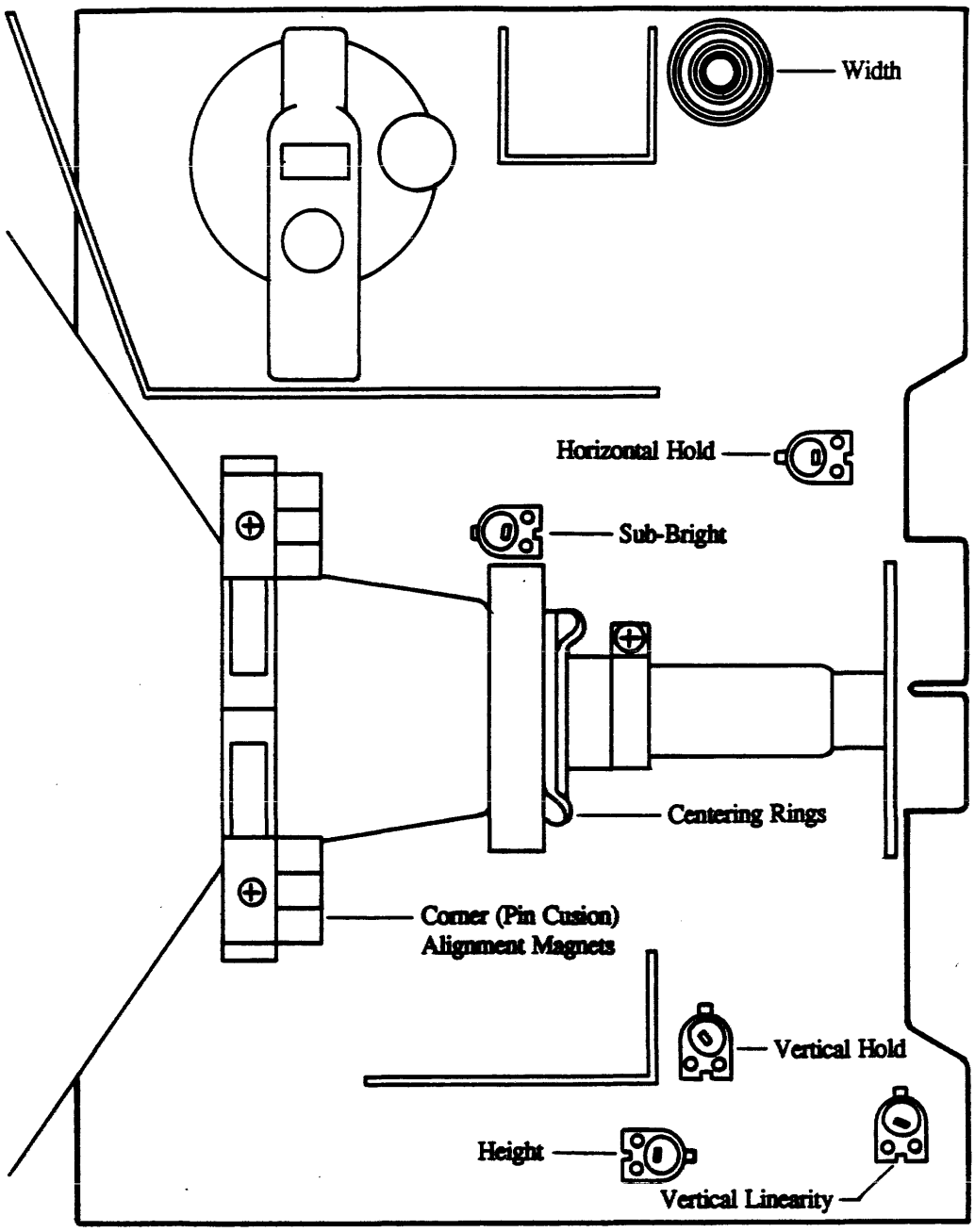
g. Note the alphabet in the upper right corner of display. VERY SLIGHTLY, move the HORIZONTAL HOLD control back and forth, until the "0" appears distorted. This is a sensitive adjustment, excessive movement will cause the display to drop out diagonally.

h. Turn power off, wait five seconds, turn power on. The display should show a locked, completely stable display of the Configuration Menu. Try this test several times. Any tendency to pull sideways or roll should be cured by very small adjustments of the HORIZONTAL or VERTICAL controls.

i. Press the Processor Test key. The display should be completely stable.

This completes the adjustment procedure.

Turn the **power off**, disconnect the power cord, and reassemble in the reverse order from disassembly.



NOTE: The BRIGHTNESS and CONTRAST controls are on the front panel external bracket.

Figure 5-2: CRT Adjustments

SECTION 6: PROCESSOR/VIDEO

6.1 Introduction ——— 6-1

6.2 Functional Description ——— 6-2
6.2.1 Microprocessor ——— 6-2
6.2.2 IEEE-488 Parallel Interface ——— 6-3
6.2.3 Video Generator ——— 6-5

6.1 INTRODUCTION

The Processor Board contains the microcomputer system. The system controls all analyzer hardware functions and performs other operations, including keyboard interface and video display.

The major components on the board include the 8085 microprocessor, 64K of EPROM, 4K of RAM, video generator, a RAM/IO/Timer IC, an IEEE-488 interface and related circuitry. All the schematics, board layout, and parts list, are included at the end of this manual.

6.2 FUNCTIONAL DESCRIPTION

Refer to schematic drawing **166-013001**. The functions described include microprocessor, video generator, and parallel interface. Each processor function will be discussed separately in the following paragraphs.

6.2.1 Microprocessor

Refer to sheet 1. The program execution is performed by U36, the 8085 microprocessor. The system clock (**CPUCLK**) is derived by U42 from the DOT Clock generator output at U6-8 on sheet 4. The 8085 is interfaced to the bus by U35, U48, U49 and U50. These circuits also perform the necessary demultiplexing functions for the 8085 data bus. U14 and U47 are buffers for CPU signals leaving the board.

On-board device address decoding is performed by U37, U38 and U51. Addresses are decoded by PROM U51, which, in turn, controls U37 and U38 to provide the appropriate device select signal. U51 also provides the appropriate signals for pins 18 and 21 of the EPROMs. The functions of these pins may vary according to the type of EPROM used.

U51 also controls data bus buffer U52. Note that if the **TEST** signal is high; U51 is disabled, selecting U38 (Pin 7); and the processor reads from switch S1. The outputs received from U38 are deglitched by enabling them only when **ALE** is low.

Refer to sheet 2. The program is stored in 2764 EPROMs U1-U4, U15-1b, and 2532 EPROM U17. The EPROM type and number installed will vary according to program requirements (i.e., some sockets might not be used). The 4K RAM is provided by U18-U21 and U27-U30.

Each RAM (a 2141 device) is 4K x 1 bit.. The RAM data outputs are buffered by U52 (sheet 1), the inputs are buffered by U39.

U40 is an 8155 that contains 256 bytes of RAM, three I/O ports, and a timer. It provides many Processor Board I/O and control functions and is connected to the data bus via U35 and U14 on page 1, and U39. Signal CCLK1 is the clock used for the timer function. CCLK1 is derived by U43, pin 2, from the DOT Clock oscillator output at U6, pin 8 (sheet 4). Port A provides a number of control functions, primarily for the video display.

Refer to sheet 3. Switches SW1-1 through SW1-8 are read by the processor via U5. When an SW1 switch is ON, the input to U5 is low (logic 0). Conversely, OFF is high (logic 1). These switches allow the user to specify certain parameters to the Control Program. SW1-1 selects the line frequency for the Video Generator. SW1-2 through SW1-8 change parameters of the RS-232C and IEEE-488 interfaces. The parameters specified by the switches are different for the two interfaces. Details are provided in this section for the IEEE-488 interface. The detailed information on the RS-232C interface is contained in Section 17, DISK CONTROLLER, COMPUTER, DYNAMIC RAM.

6.2.2 IEEE-488 Parallel Interface

The 800 Series analyzers are equipped with an IEEE-488-1978 parallel interface. The IEEE-488 interface is implemented primarily by U58, a TMS 9914 GPIB Interface Controller (see schematic sheet 3). The U58 data lines are buffered by U57, a 75160 transceiver. The U58 control lines are buffered by U59, a 75161 tranceiver.

Bus driver U57 can be configured in either the open collector or three-state mode. This is determined by the logic level at pin 11. A low level produces open collector operation and a high level produces three-state operation. The Processor Board is supplied with a jumper that produces open collector operation. This jumper can be removed if three-state operation is desired (see sheet 3 and board layout drawing).

The IEEE-488 connector on the rear panel is wired to J3, a 26-pin connector on the motherboard. The motherboard connects these lines to the Processor Board socket S2A.

SW1-2 through SW1-8. The meaning and values of these switches for the IEEE-488 interface are shown in Table 6-1 (page 6-4). The location and orientation are shown in Figure 6-1. Note that these DIP switches also affect the RS-232C interface parameters described in Section 17.

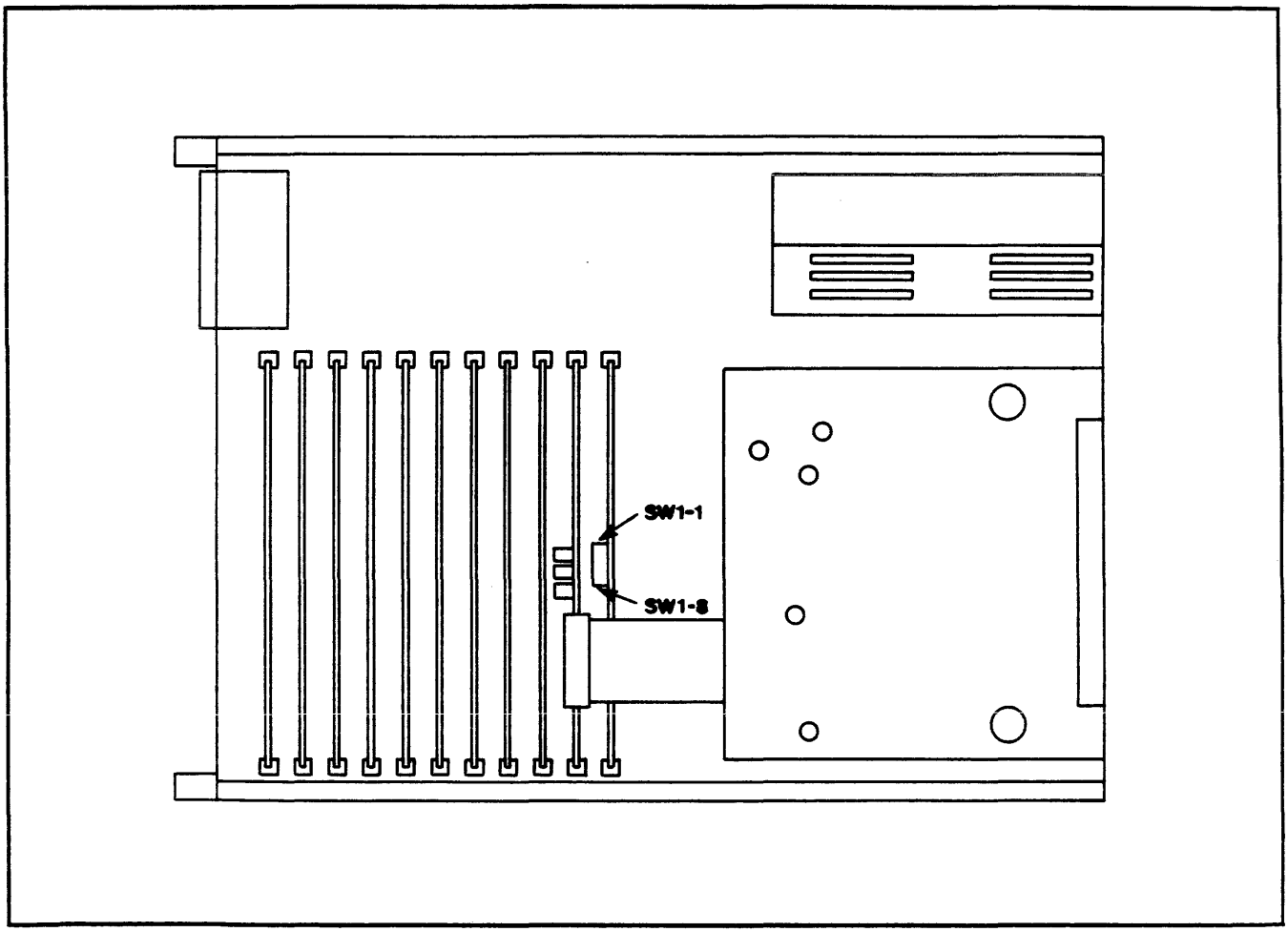


Figure 6-1: DIP Switch Location

SWITCH	DESCRIPTION	CONTROL
SW1-2	Keyboard State	DISABLED = ON ACTIVE = OFF
SW1-3	Interface State (IEEE-488 I/F)	DISABLED = ON ACTIVE = OFF
SW1-4	Termination Character Type	CR -> LF = ON CR = OFF
SW1-5	Address BIT 1	LOW = ON HIGH = OFF
SW1-6	Address BIT 2	LOW = ON HIGH = OFF
SW1-7	Address BIT 3	LOW = ON HIGH = OFF
SW1-8	Address BIT 4	LOW = ON HIGH = OFF

Table 6-1 DIP Switch 1 Selections

NOTE: Address bit 0, handled entirely by the Control Program, is 0 (low) for the Model 800 as LISTENERS, or 1 (high) for the 800 Series as TALKERS.

6.2.3 Video Generator

Refer to sheet 4. The Video Generator circuitry utilizes the Intel 8275 CRT controller, U33. U31 provides 2K bytes of video RAM accessed by both the CRT controller and the processor.

U53 and U7 buffer the Video Data Bus connection with the system data bus. U22, U23 and U24 select either the processor address bus or the output of the display character counter, U8. The selection is determined by the device that is currently accessing the video RAMs. U10, U11 and U41 generate **DACK-** that determines which device is accessing the RAM by controlling MUXs U22, U23, U24.

U6, Y1, U42 and U43 pin 2 generate the timing signals **CCLK, CPUCLK,** and **DOTCLK.** These signals are used to produce the video signal. In addition, U43 synchronizes the **CURCT** and **EXTVID** signals. The count output from U42 represents the horizontal dot position within a character. The **CURCT** signal is high when the count from U42 matches the position from the 8155 (U40) outputs, compared by U54, and latched by U43.

Video data is produced by U33, U25, U26, U34, U45, U12, U43, U44 and U13. U33 outputs a character code and line count to character ROM U25. The ROM produces the 8-bit pattern for that line of that character. This is loaded into U26, a shift register. Simultaneously, U34 latches the appropriate display attribute signals (reverse video, half light, etc.). These signals are sent to the DOT Logic PROM, U45 with the serial bit pattern from U26. Thus, signals **DOT** and **HALFLIGHT (VIDEO- + HALF)** are produced. These are resynchronized by U43 at pins 10, 12, buffered by U13, and sent to the base of Q1. Emitter follower Q1, produces a composite video output. Three pin connector J2 goes to the display module via a coaxial cable.

The LS165 shift registers U12 and U44 produce horizontal and vertical sync pulses with the horizontal and vertical retrace periods (**HRTC, VRTC**). These are buffered by U13, and mixed with the video signals in Q1. The **VRTC** signal is buffered by U9 and sent as a processor interrupt, **BV**, for software synchronization.

The value of the vertical retrace period is set at power-on initialization. At this time, the Control Program reads the setting of switch SW-1. The Control Program then loads a vertical retrace period, based on the switch setting, into the 8275 CRT Controller. Switch SW1-1 should be set by the user to match the power mains frequency as follows:

SW1-1	Mains Frequency
ON	60 Hz
OFF	50 Hz

Table 6-2

A slight adjustment of the CRT monitor may be required when switching from the 50 Hz to 60 Hz refresh rate.

Signals **HRTC, VRTC** and **DOTCLK** are fed to the optional Waveform Board via U9, a 16-pin DIP socket. The ready-for-display waveform signal is sent from the Waveform Board via J1-4 as **EXTVID-**. Signal **EXTVID-** is resynchronized by U43 and sent to the DOT Logic PROM U45.

SECTION 7: MODEL 800 A, B & C STATE CONTROL BOARD (15/20 MHZ)

7.1 Introduction ——— 7-1

7.2 Description ——— 7-2
- 7.2.1 Processor Interface ——— 7-2
- 7.2.2 Stack Management ——— 7-4
- 7.2.3 Clock Control ——— 7-5
- 7.2.4 Collection Address Counter ——— 7-6
- 7.2.5 Post Trigger Counter ——— 7-6
- 7.2.6 Restart Generator ——— 7-7
- 7.2.7 Trigger Delay Control ——— 7-8

7.1 INTRODUCTION

The State Control board directs the acceptance of data for storage by the Sate Memory boards for later analysis and display. The 800 Series each contain one State Control board except for the Model 800E which contains none.

Hardware registers, counters and RAMs on the State Control board are loaded by the Control Program. The loading information is entered from the keyboard under the guidance of the STATE menu. Using the parameters and modes specified, the State Control board implements the various State analysis operations.

As new technology becomes available, NICOLET reserves the right to enhance the performance specifications of its products. The **166-012801** State Control board allowed the State Memory boards to collect at a maximum data rate of 15 MHz. However, adding 20 MHz capability dictated a new design and board layout. Though the higher speed **166-036901** circuits contain numerous different parts, the block diagram and circuit description still apply. The two schematics, board layouts and associated parts lists are provided in the rear of this manual.

7.2 DESCRIPTION

A block diagram of the State Control board is shown in Figure 7-1, page 7-3. Also refer to the schematic diagram, board layout and parts list included at the end of this manual. Tables of connector pins versus signal names for all motherboard connectors are provided in MOTHERBOARD CONNECTIONS. An alphabetical list of all interboard signals is included. The GLOSSARY section offers explanations for terms that may be unfamiliar.

The functional units of the State Control board are the Processor Interface, Stack Management, Clock Control, Collection Address Counter, Post-trigger Counter, Restart Generator, and Trigger Delay Control. These units are discussed in the following subsections.

7.2.1 Processor Interface

Refer to schematic **166-012801**. The Processor Interface (sheet 1) is comprised of the Address Decoder, Status Ports, Interface Output Ports, and Interface Shift Register. This circuit allows the processor, under the direction of the Control Program, to load user-supplied information from the keyboard with the aid of menus. To prepare the analyzer for the intended application, the information is entered into registers, RAMs, and counters. The interface allows the processor to interrogate status and signal lines and to send various control signals when appropriate.

The Address Decoder consists of the following: U33, a 74LS10 triple 3-input NAND gate; U1, sections of a 74LS00 quad NAND gate; and U44 and U45, 74LS138 3-to-8 decoders. This circuit allows the processor to read and write to the Interface Satus and Output Ports, respectively. I/O read and write commands are used to perform these functions. Also, one port output signal, **RDALMEM-** (U44-14), is sent to the Collection Address Counter.

The Interface Output Ports, U46 and U47, are both 74LS374 octal-D flip-flops. Both flip-flops store software-generated control signals. U46 stores signals for the State Control board, U47 for the A, B probes and the A, B State Memory boards.

The Status Ports, U48 and U49, are both 74LS244 octal line receivers. The processor reads status signals from the State Control board. These are read via U49, U48-11 and U48-17. Data collection addresses are read by the processor from the State Control board through U49 and U48.

The Interface Shift Register has a part shown on each sheet of the schematic. The register consists of the following components:

a. U38, a 74LS164 8-bit shift register, sheet 1.
b. U32B, one-half of a CMOS 4015 dual 4-bit shift register, sheet 2.
c. U12, U25, 4015s, sheet 3.
d. U27, U28 and U32A, all 4015s, sheet 4.

These six 4015 devices have parallel readout, and allow the processor to store five sets of eight control bits. Only one daisy-chained data line is received instead of running the 8-bit Processor Data Bus to each of the five devices. The data line **SRDATA** is sent from the Interface Output Port U46-19. This 48-bit shift register stores control bits (U38, U32A) and preset counts (U32B, U12, U27, U28). The last bit in the last shift register, U25-2, is sent back to the Status Port at U48-6. This allows the Control Program to monitor the Shift Register load status.

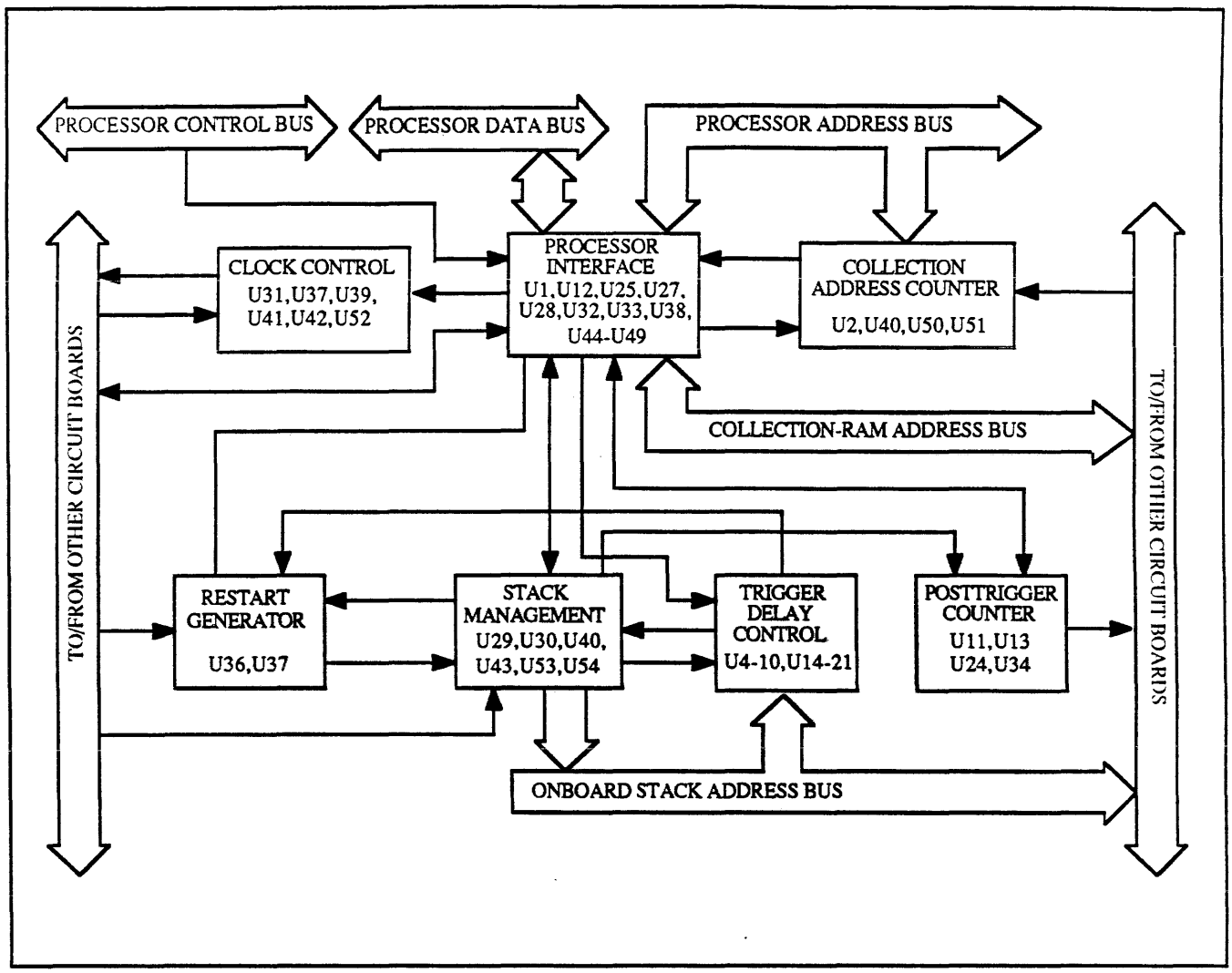


Figure 7-1: State Control Board Block Diagram

7.2.2. Stack Management

Stack Management (sheet 2) is comprised of the Stack Address Counter, Stack Address Latches, and Stack Control circuits. This circuit maintains the stack pointer by means of the Stack Address Counter. It also evaluates a number of input signals to determine when to POP (advance) or reset the stack pointer.

The Stack Address Counter, U43, a 74S169 synchronous 4-bit binary counter, generates signals NSA0 (Next Stack Address). This signal is sent to the address inputs of the Delay Count RAM (sheet 4). It is also sent, via stack address latches U53 and U54 (U55 on 20 MHz boards), to the Trigger Stack RAM on each State Memory board. The trigger stack address on the circuit board is the equivalent of the trigger level on the menu.

The stack RAMs have terminal addresses of 0F hex (15 dec). The Stack Address Counter is preset by the Control Program (through U32B) and always operates in the POP direction (always counts up). For example, if the menu specified trigger levels 0 through 8, the Stack Address Counter would be preset with 0F - 8 = 07. This RAM location, address 07, would contain the word for the first trigger level on the menu, level 0. The ending counter address, 0F, would contain the word for the last trigger level entered on the menu, level 8. At count 0F, the ripple-carry counter output at U43, pin 15 produces the stack-empty signal, **STKE-**. This is used by the Stack Control circuitry.

The Stack Address Latches, U53 and U54, are both 74S74 dual D flip-flops. They latch the address produced by the Stack Address Counter. This allows it to be stabilized for the Trigger-word and Qualifier-Word RAMs on the State Memory boards.

The Stack Control circuits consist of the following logic:

a. U52A, B, D, sections of a 74S86 quad exclusive-OR gate.

b. U37C, D, Sections of a 74F02 quad NOR gate used as inverters.

c. U31, a 74S02 quad NOR gate. Sections A and B are used as negative-input AND gates.

d. U40B, one-half of a 74F74 dual flip-flop.

e. Multiplexer U29, a 74S64 4-2-3-2 AND-NOR gate.

f. U32, a 74S74 dual D flip-flop.

g. U23B, a section of a 74S32 quad OR gate.

This circuit produces signals used by Stack Management and a number of signals used elsewhere on the board. The signals include the following:

a. **POPEN-** (POP Enable-). Advances the level in the trigger-word and qualifier-word stacks on the State Memory boards.

b. **POPSTK+** (POP Stack+, a clock derived from **POPEN-**). Advances the level in the delay-mode stack.

c. **PTENB+** (Post-trigger Enable+). Derived from the Stack Address Counter ripple-carry signal, **STKE-**. **PTENB+** is sent to the Post-trigger Counter, causing the count to start for collection of the specified number post-trigger data words.

7.2.3 Clock Control

Clock Control is comprised of the Clock Multiplexer (sheet 2) and the Clock Qualifier Gate (sheet 3). This circuit implements the keyboard entered selection of clock source and provides the final logic in the process of clock qualification.

The Clock Multiplexer consists of U39, a 74S64 4-2-3-2 AND-NOR gate; U41A, one-half of a 74S51 dual AND-NOR gate; and U42, one-fourth of a 10125 quad ECL-to-TTL translator. Signals **CLKSEL0** allows the Clock Multiplexer to implement menu selection of clocks for probe data latches on the Memory boards. **CKLSEL** is received from the Interface Shift Register. The A-board clock, **ALATCHCLK**, may be menu selected from either the positive-going or negative-going edge of **APROBCLK** (the A-probe incoming clock). The B-board clock, **BLATCHCLK**, may be menu-selected from **APROBCLK** or the +/- going edge of **BPROBCLK**. **BPROBCLK** is the B-probe incoming clock. The **CLATCHLK** selections are performed on the 800 Series Motherboard.

The Clock Qualifer Gate, U41 (sheet 3), is not used. The signal **CLKQUALI-** is generated on the Motherboard by U6, and is true (low) in the following cases.

a.If the incoming clock qualifier signals **ACQ1**, **BCQ1** and **CCQ1** are active, or

b.If **ACQ2** and **BCQ2** and **CCQ2** are active.

The signals **ACQ1,2**, **BCQ1,2** and **CCQ1,2** are received from pre-collection comparator RAMs on the State Memory Boards. **ACQ1** is active (high) if the following statement is true regarding the first clock-qualifier word specified in the menu: The two A-probe qualifier bits are matched by the bits received from the A-probe lines.

In a similar manner, BCQ1 is high if the first clock-qualifier word specified in the menu meets the folliwing statement: The second two qualifier bits are matched by the bits received from the B-probe lines. **CCQ1** operates similarly.

If all six qualifier bits are matched, **ACQ1**, **BCQ1**, and **CCQ1** are high and **CCLKQUALIN-** goes active low. Similarly, **ACQ2**, **BCQ2** and **CCQ2** represent the second clock-qualifier word on the menu.

Note the distinction between qualifier **words**, used with the menu, and qualifier **bits**, used with the probe leads. The A, B and C probes each have two qualifier leads, separate from the data input channels.

Either or both of the two bits on each of the probes can be used for trigger or clock qualification. The selection is made on the STTE menu. On the STTE menu, the qualifier bits appear in the clock-qualifier word or trigger word as -XXXXXX. The Xs mark the positions, left to right, of ACQ, AQ2, BQ1, BQ2, CQ1, and CQ2. If a value is given to the first X in the clock-qualifier word, such as -0XXXXX, then AQ1 is used as a clock qualifier. If the first X is also given a value in a trigger word, then AQ1 is also used as a trigger qualifier.

Clock qualifications by a data **word** appearing on the input channels is accomplished on the State Memory boards in a similar fashion, and is discussed in Section 8 (subsection 8.2.6) of this manual.

7.2.4 Collection Address Counter

The Collection Address Counter (sheet 3) consists of U50, U51 and U2 (U54 on 20 MHz board), 74F191 synchronous 4-bit binary counters; and U40A, one-half of a 74F74 dual D flip-flop. This circuit supplies 1024 sequential storage addresses for the Data Collection RAMs on the State Memory Boards. During display and analysis, the same circuitry allows the processor to address those RAMs when reading the collected data.

The three 4-bit counters are connected in cascade to form a 12-bit counter. This provides a capacity of 4096 counts, but is limited to 1024. Outputs RA0 through RA9 are sent as address bits to the Data Collection RAMs on the State Memory boards. In the load mode, the counters send the input levels through without change. This allows the processor to directly address the RAMs. The load mode is initiated by **RDALMEM-** (Read All Memory -), a Control Program Signal received from the Processor Interface. Before the Control Program releases **RDALMEM-**, it places zeroes on the counter input lines. Thus, when **RDALMEM-** is released, the counter is preset to 000.

With the **RDALMEM-** load signal inactive (high), the counters are ready to generate sequential addresses for the Data Collection RAMs. The count is advanced with each **BWE2+** clock pulse. **BWE2+** (B Write Enable +) is the qualified data collection clock. It is received from the State Memory board and is selected by the processor.

As the counters sequence 000 through 400 hex, the QC at U2-6 (occurring at count 400) is sent to flip-flop U40. This circuitry generates signal **ROLLOVER1+** the first time address 400 is reached. This signal is sent to Interface Status Port U48 for use by the Control Program.

The counter sequences through the RAM address range until the trigger conditions are met. The **BWE+** clock is subsequently stopped by signal **BCKLINH+** and is discussed in 7.2.5. In some instances, this clock interruption may occur before the first rollover. In other instances, the interruption may not occur until manual intervention, such as a FORCE DISPLAY or a menu call.

7.2.5 Post-Trigger Counter

The Post-trigger Counter (sheet 3) is comprised of the Counter and the Clock Inhibit circuits. This circuitry causes data collection to continue for the menu-specified number of data words after the trigger. The menu expresses this parameter as pre-trigger count, but the Control Program converts the number to post-trigger count. This allows more efficient circuit implementation.

The menu allows a pretrigger count range of 0 to 999 words.

The Post-trigger Counter consists of U11, U13 and U24, 74LS161 synchronous 4-bit binary counters. They are combined to form a 12-bit counter with a maximum count of 400h. This counyer serves to count the post-trigger count. The program limits the counter load so that the maximum count is 999.

At setup time, the Control Program presets the counter to the proper calculated value via serial data to U12 and U25A. The value loaded is 400-c, where c is the post-trigger count. The actual loaded value may vary by one or two counts from 400-c This allows for compensation of pipeline delays in associated circuitry.

When the trigger conditions have been met, signal **PTENB+** (Post-Trigger Enable) goes high. This disables the load inputs and enables the count function. The counter advances at each pulse of **BWE2+**, the qualified data-collection clock. The count completion is signaled by the ripple-carry output at U24-15.

The Clock Inhibit circuit consists of U35B,C,D, each one-fourth of a 74S00 quad NAND gate (B and C are used as negative-input OR gates); U23C, one-fourth of a 74S32 quad OR gate; and U34, a 74S74 dual D flip-flop. When the post-trigger count has been reached, this circuitry generates clock-inhibit signals which are described on page 7-7.

When the Counter reaches terminal count, the ripple-carry output at U24-15 goes high, producing signal **ACTDN+** (A Countdown +). This signal is sent, via U23, to set both halves of flip-flop U34. The Q- output of U34B is sent to U35 to produce **ACLKINH+** (A Clock Inhibit +). This signal is sent to all Memory Boards and inhibits further clocking of collected data. The Q output of U34B is returned via U23. This latches the set condition of U34 past the duration of the ripple-carry pulse.

The Q- output of flip-flop U34A produces the signal **PTCTDN+** (Post-trigger Countdown +). This signal is sent to Interface Status Port U48 to inform the Control Program that the post-trigger countdown is complete.

If the post-trigger count is 0, signals **PSTTG0+** (Post-trigger 0+) and **PTENB+** are high at NAND gate U35D inputs. The resulting low output from U35D then presets flip-flops U34A and U34B. This produces the signals **BCLKINH+** and **PTCTDN+** without any counting having occurred.

The Control Program can also produce signals **BCLKINH+**. This is done by sending signal **SWCLKINH-** (Software Clock Inhibit) to the inputs of negative OR gates U35B and U35C.

7.2.6 Restart Generator

The Restart Generator (sheet 3) consists of U37A,B, two sections of a 74F02 quad NOR gate (used as negative input AND gates); and U36, a 74S64 4-2-3-2 AND-NOR gate. This circuit generates the **RST-** (Restart) signal. This is used by Stack Management to reload the trigger Stack Address Counter with the address for level 0. This address is still latched in the Interface Shift Register section U32B. The system is then restarted, testing for a match of trigger conditions. Signal **RST-** is produced under any of the following conditions:

a. The NNNNth clock is reached when the ON-NNNNth-CLOCK delay mode is in effect.

b. The NNNNth clock is reached when the BEFORE-NNNNth-CLOCK delay mode is in effect.

c. The menu-specified RESTART word is recognized.

d. The Control Program outputs the signal **LDSTKAD+** (Load Stack Address) from Interface Output Port U46-2.

7.2.7 Trigger Delay Control

Trigger Delay Control (sheet 4) is comprised of the Delay Count RAM, Delay Counter, Delay-Mode RAM, and Delay-Mode Control. These circuits implement the menu-selectable trigger-delay functions. The circuits produce signals that allow the search for trigger words to proceed to the next level. The specified delay conditions are met on a level-by-level basis. Note that the trigger word at level 0 has no delay function.

The Delay Count RAM consists of U16, U17, U18 and U19, all 74S189 16-word x 4-bit static RAMs. They are connected in cascade to form a 16-word x four 4-bit digit RAM. This RAM is loaded by the processor at set-up time with the menu-selected delay count (the count range is 0-9999d). This is done for each of the 15 delayable trigger-word levels. The stored delay counts are used to preset the Delay Counter as each trigger-word level is reached during processing.

The four address lines of each RAM are applied in parallel with signals **NSA0-3** (Next Stack Address). Signal **NSA** is generated by the Stack Address Counter. The four address bits decode into 16 stack addresses that correspond to the 16 trigger-word levels on the menu. When loading the RAM at set-up time, the Control Program addresses it through the transparent Stack Address Counter (U43, sheet 2). Delay-count data for the RAM is loaded using U27 and U28, shift registers. After loading is completed, the Control Program presets the Stack Address Counter with the address count. This number corresponds to the number of trigger levels specified on the menu.

After RESET, the addresses are sent from the counting Stack Address Counter and start with trigger-word level 0. Although there can be no delay specified for trigger-word level 0, the level is stepped through for simplicity of logic. Note that trigger-word level 0 does not correspond to stack address 0 unless all trigger-word levels are specified. As each trigger stack level is entered, the stored 4-digit delay count for that level is determined. This data is sent from the Delay Count RAM to the Delay Counter as four 4-bit sections in parallel.

The Delay Counter consists of U3B,C,D sections of a 74S08 quad AND gate; U20, a 74F08; U5 through U8, all 74S162 synchronous 4-bit decade counters; and U26A, one-fourth of a 74S00 quad NAND gate. At the start of processing for each stack level, signal **POPEN-** (from Stack Control) is brought low. This loads the Delay Counter with the count stored in the Delay Count RAM for that stack level. The count value stored and loaded is 9999d-c, where c is the menu-specified count. This conversion is done so the ripple-carry out of U8-15 can be used to indicate terminal count. The actual loaded value may vary a few counts from 9999d-c. This allows for compensation of propagation delays in the associated circuitry. When **POPEN-** returns high, the counter begins to count.

The count is advanced by **DBCLK+** (Delayed B Clock +, derived from **BWE+**, the qualified data collection clock). This occurs when the count-enable inputs P (pin 7 on U5 through U8) are high. U3B,C,D and U20A,B provide carry look-ahead to speed up the counter. The P inputs receive **TRIGCTEN+** (Trigger Count Enable +) from Delay Mode Control. This signal is sent via U3B-5, U3C-10 and U20B-5. If the menu-entered delay mode specifies counting clocks, delay Mode Control holds the P inputs continually high. If the delay mode specifies count trigger-word recognitions, then each recognition is counted. This is accomplished by Delay Mode Control holding the P inputs high so that one clock pulse is counted.

When the terminal count is reached, the resulting ripple-cary out of U8-15 is sent to U20D,C and U26A. This produces signals **DLYCTDN+** and **DLYCTDN-** (Delay Countdown + and -).

The Delay-Mode RAM, U21, is a 74S189 16-word x 4-bit static RAM. As with the Delay Count RAM, the 16 word-addresses represent the 16 levels of the trigger stack. This RAM is loaded by the processor at set-up time using sections U32A and U32B of the Interface Shift Register. The RAM is loaded with the menu-selected delay mode for each of the 15 delayable trigger-word levels. The four data bits output to the Delay Mode Control flip-flops U9, U10 encode the mode information as follows:

a. D2, D3 and D4 constitute a 3-bit code for the five available delay modes.
b. D1 is high if triggering is to occur on or after the trigger word.
c. D1 is low if no trigger is to occur on or after the trigger word.

The mode encoded by D1 is not, strictly speaking, a delay mode. It applies to both delayed and undelayed trigger recognition. For reference, the available trigger-word delay modes and stored codes are shown below:

MENU DELAY MODE	D4	D3	D2
After NNNNth Clock	0	0	0
Before NNNNth Clock	1	0	0
On NNNNth Clock	0	1	0
Not On NNNNth Clock	1	1	0
Occurs NNN times	0	0	1

Delay-Mode Control consists of U9 and U10, two 74S74 dual D flip-flops; U4, a 74S64 4-2-3-2 AND-NOR gate; U15A, one-half of a 74S74; and U14A, one-half of a 74S51 dual AND-NOR gate.

Flip-flops U9 and U10 latch the delay-mode code bits, read out of the Delay-Mode RAM at NSA time. This data is for use during the processing of the current stack level. The U15A flip-flops generate a one-clock interval pulse on the NNNNth clock for use by the U4 multiplexer.

Signal **TRIGCTSEL+** (Trigger Count Select +), is the latched D2 mode-code bit at U9, pin 9. AND-NOR gate U14 uses **TRIGCTSEL+** to determine the nature of output signal **TRIGCTEN+** (Trigger Count Enable +) at pin 6. Signal TRIGCTEN+ is sent to the P enable inputs of the Delay Counter. If **TRIGCTSEL+** is high, then **TRIGCTEN+** usually is held low. The exception to this is when **TRIG-** (Trigger-word recognized -) pulses it high at each trigger-word recognition. It is held high long enough for the Delay Counter to count one clock. In this mode (D2=1), the Delay Counter counts trigger-word occurrences. In the mode (D2=0), the Delay Count counts clock pulses.

The U4 multiplexer combines the Delay Counter terminal-count signals, **DLYCTDN-** and **DLYCTDN+**, with the current delay mode information. This produces signal **DLYTC+** (Delay Terminal Count +). This signal is sent to Stack Control multiplexer U29 (sheet 2). This enables the next trigger-word recognition (signal **TRIG+**) to generate **POPEN-**. If other conditions are favorable, **POPEN-** advances the stack level. In some delay modes, **DLYCTDN+** or **DLYCTN-** will cause the Restart Generator to produce signal **RST-**. This signal overrides **DLYTC+** and starts the trigger-word search process over again.

SECTION 8: MODEL 800 A, B & C STATE MEMORY BOARDS (15/20 MHz)

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15 MHz Board

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8.1 INTRODUCTION

The State Memory board accepts data from 16 incoming data lines of the Model 51A Probes. If directed by State Control, the data is stored for later analysis and display. The Model 800 B and C each contain three State Memory boards while the Model 800 A contains only two. Each board receives 16 data lines from the interchangable Probe Pod A, B, or C. The boards are designated State Memory board A, B and C, respectively. The three boards are identical and interchangeable. However, certain connections to the Function Motherboard sockets plugged into each allocated socket operate differently. The following discussion will apply to all the State Memory Boards, except as noted.

As new technology becomes available NICOLET reserves the right to enhance the performance specifications of its products. The 166-012701 State Memory Board maximum data rate was increased from 12.5 MHz to 15 MHz simply by substituting new integrated circuits. However, the step to 20 MHz capability dictated a new board layout be done. Although the higher speed 166-036801 circuits contain numerous different parts, the block diagram and circuit description are very similar. The circuit description for the faster board is found beginning on page 8-13. The two schematics, board layouts and associated parts lists are provided in the rear of this manual.

8.2 FUNCTIONAL DESCRIPTION

A block diagram of the State Memory Board is shown in Figure 8-1. When appropriate, also refer to the schematic diagram, board layout and parts list at the end of this manual. Tables of connector pins versus signal names for the motherboard connectors are provided in MOTHER-BOARD CONNECTIONS. An alphabetical list of all signals is included. The GLOSSARY section offers explanations for terms that may be unfamiliar.

Major units of the State Memory Board circuitry include the following: Qualifier-Word RAM, Trigger-Word RAM, Data-Collection RAM, AUX RAM, Address Decoder, Clock Generator, and I/O buffers.

The qualifier-word memory and trigger-word memory can be considered as comparison devices. The data-collection and auxiliary RAM memory are typical storage devices. An operational description of these memories follows.

The Control Program stores the two menu-specified clock-qualifier words in the RAM. It also stores all the specified trigger words, level by level, in the Trigger-Word RAM. At run-time, an incoming data word is clocked into the Probe Input Buffer by the primary external clock. A data word consists of 18 parallel bits. These are comprised of 16 data bits and two qualifier bits. From the buffer, the data is sent to the Qualifier-Word RAM and the Trigger-Word RAM. The data is sent later to the Data Collection RAM.

The Qualifier-Word RAM compares the data word received with the two clock-qualifier words. The Trigger-Word RAM compares the incoming data word with the trigger word at the current trigger stack level. If the data word matches either of the clock-qualifier words, the current clock period is considered qualified for data. The data in the Probe Input Buffer is then stored in the Data Collection RAM.

If the qualifier-word comparison does not qualify the current clock period, the data word is not stored in the Data Collection RAM. Note that the menu may be specified with all bits as "don't care" X's. In that case, all clock periods will qualify.

This operation is described further in the following subsections.

8.2.1 Input/Output Buffers

Refer to schematic **#166-012701.**
The Input/Output Buffers are comprised of the following buffers: Probe Input Buffer, Probe Output Buffer, Setup Data Buffer, Read-TSA (Trigger Stack Address) Buffer, Collection Address Buffer, Collection Input Buffer, and Collection Output Buffer.

The **Probe Input Buffer** consists of U20 and U23, both 74S374 octal D flip-flops; and U36A, one-half of a 74S374. The 16-bits of data at the probe pod are applied to U20 and U23 via S2. The 16 data outputs are sent to three locations; the Collection Input Buffer, and the address inputs on both the Qualifier-Word RAM and the Trigger-Word RAM. The reason for sending this data to the address lines of the two RAMs will be discussed later.

Two qualifier bits, Q1 and Q2, are sent from the probe via S2 to two of the four inputs of U36A. The trigger output, FT, of the timing analyzer section is applied via S2 to the third input of U36A. The external input EXT, at the BNC connector on the rear panel, provides the fourth input via S2. The four outputs of U36A are sent to address inputs on both the Qualifier-Word RAM and the Trigger-Word RAM.

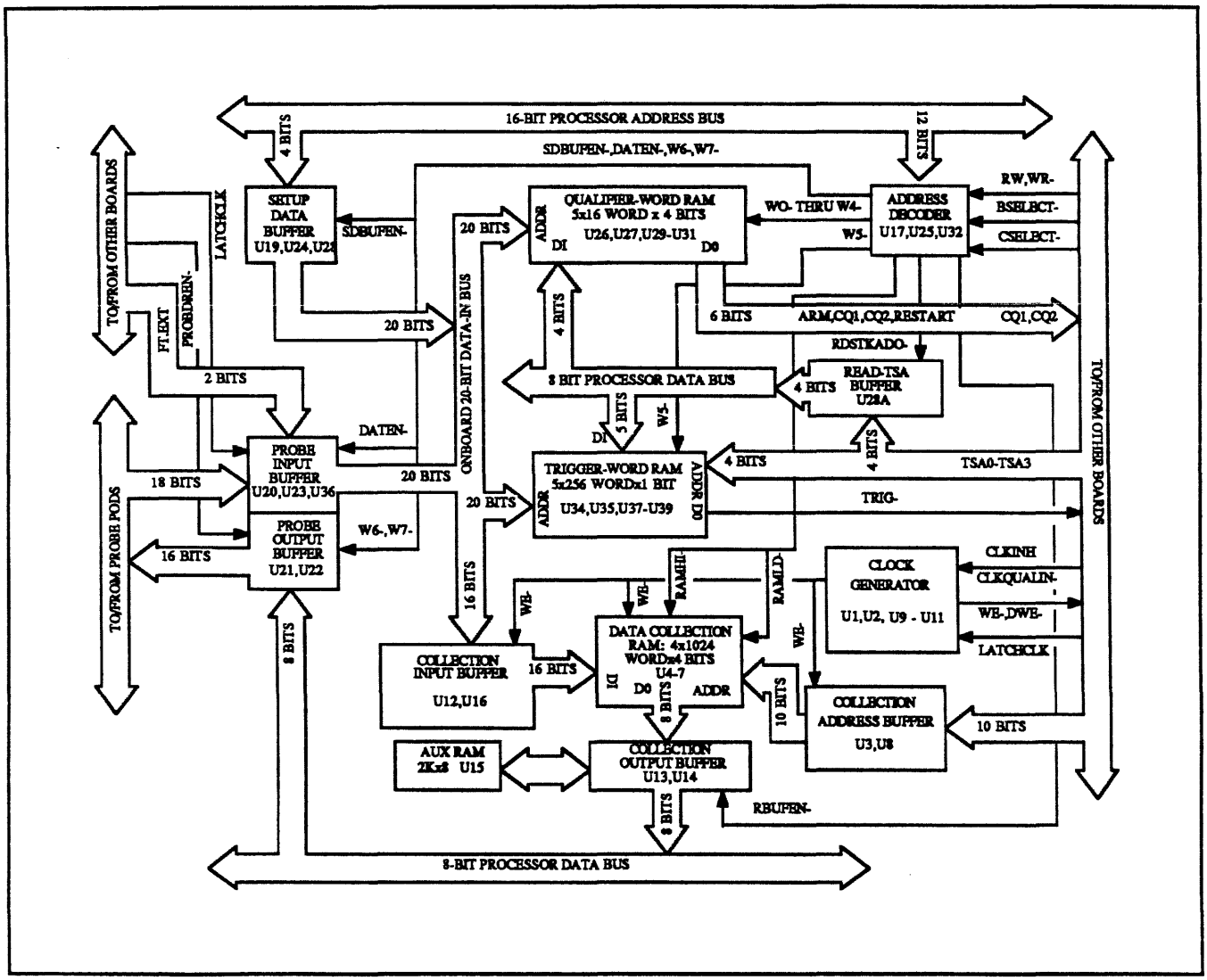

Figure 8-1: State Memory Board Block Diagram

U20, U23 and U36A are clocked by the menu-selected primary external clock, **LATCHCLK**. The signal **LATCHCLK** is received from the State Control board via S2. The outputs of all three devices are enabled at pin 1 by signal **DATEN-** (Data Enable Minus). This signal is received from U9 (pin 10), and is the inverse of STBUFEN- (Setup Data Buffer Enable-).

The **Probe Output Buffer** consists of U21 and U22, both 74S374 octal D flip-flops. This buffer is used to send data from the processor to either optional or custom probes designed to accomodate data output.

The eight inputs of U21 (DB0-DB7) are connected in parallel with those of U22 on the Processor Data Bus. The outputs of U21 and U22 are sent in cascade via S2 to the 16 probe data lines. The 8-bit input is demultiplexed to the 16-bit output using two strobe signals, **PROBEDREN 0-7** and **PROBEDREN 8-15**. The three-state outputs are enabled by **PROBEDREN** (Probe Data Remote Enable) that is generated at the State Control Board.

The **Setup Data Buffer** consists of U19 and U24, both 74LS244 octal buffers and U28B, one-half of a 74LS244. This buffer is used to load set-up data into the Qualifier-Word and Trigger-Word RAMs shown on sheet 2. This is described later in the Qualifier-Word RAM and Trigger Word RAM descriptions.

The 20 buffer outputs are sent in cascade via the On-board Data-In Bus to the Qualifier-Word and Trigger-Word RAMs. The four Qualifier-Word RAM input lines are demultiplexed to 20 output lines using the five write signals, **W0-** through **W4-**. In the case of the Trigger-Word RAM, demultiplexing is accomplished with the aid of the RAM. The Buffer three-state outputs are enabled by **STBUFEN-** (Setup Data Buffer Enable -). This signal is sent from the Address Decoder.

The **Read-TSA Buffer** consists of U28A, one-half of a 74LS244 octal buffer. It is used by the processor to read the trigger stack address supplied to the Trigger-Word RAM by State Control. The four input signals (**TSA0-TSA3**) are received from the State Control Board via S2. The four output lines of U28A are loaded onto the Processor Data Bus. The outputs are enabled by signal **RDSTK-** (Read Stack -) received from the Address Decoder.

The **Collection Address Buffer** consists of U3 and U8, both 74LS373 octal D latches. The 10 input signals (**RA0-RA9**) are received by U3 and U8 via S2 from the State Control board. They are sent to the 10 address inputs of the Data Collection RAM U4-U7. If the current clock period is qualified for data collection, the **RA** signal is latched into the buffer. The latching is caused by the negative-going **WE-** (WriteEnable-) pulse received from the Clock Generator (Q- output at flip-flop U10). This data collection address is held by the Collection Address Buffer for the duration of the **WE-** pulse. Signal **WE-** is also the write pulse for the Data Collection RAM.

The **Collection Input Buffer** consists of U12 and U16, both 74S374 octal D flip-flops. The 16 outputs of the Probe Input Buffer are applied to the 16 inputs of the Collection Input Buffer, then loaded by a delayed LATCHCLK. The 16 outputs of the Collection Input Buffer are applied in cascade to the Data Collection RAM and Collection Output Buffer. If the current clock period is qualified for data collection, signal **ACLKINH+** from the State Control Board is low. This allows the contents of the Collection Input Buffer to be written into the Data Collection RAM.

The two holding buffers (Collection Address & Input Buffers) are provided to compensate for propagation delays. The propagation delay is caused by the Clock Generator and qualification comparison. At high clock rates these delays may result in the next address and data word arriving before the current write has been completed. In this way the holding buffers allow sufficient time to complete the write to the Data Collection RAM.

The Collection Output Buffer consists of U13, a 74LS244 octal buffer; and U14, an 8304 bidirectional buffer. The processor uses the Collection Output Buffer to read collected data from the Data Collection RAM and AUX RAM. This is done for purposes of data analysis and display. The eight outputs of each RAM provide the 16 data inputs. The eight output lines are loaded onto the 8-bit Processor Data Bus. Signals **Ø-7EN** and **8-15EN** and **TRAN/REC** received from the Address Decoder enable the buffer outputs to the bus.

8.2.2 Clock Generator

Refer to the schematic, sheet 1. The Clock Generator consists of the following components: U1 and U2, both 50 ns delay lines with selectable delay outputs; U9 and U40, 74S04 hex inverters; U11, a 74S02 quad NOR gate (section B is used as a negative input AND gate); and U10A, one-half of a 74S74 dual D flip-flop. A low **CLKQUALIN-** signal signifies that the current input data word is approved for data collection. When a low **CLKQUALIN** signal is received at U11 pin 6, the delayed data collection clock **WE-** (Write Enable -) is generated at U10A pin 6. The Clock Generator also provides **WE+** (an inverted WE-) and **DLYWE-** (DeLaYed WE- clock). These signals are present at U11, pin 10 and U9, pin 2, respectively, for use by the State Control board.

The menu-selected primary external clock, **LATCHCLK** is received from the State Control board to clock the Probe Input Buffer. **LATCHCLK** also is sent via U9F to the delay line U1. After a nominal delay of 40 ns, U1 sends the clock pulse to the clock input of flip-flop U10A via U9D. If the output of U11B, pin 4, is high (by a low **CLKQUALIN** at the input), the flip-flop is set by the delayed clock. After a nominal 40 ns delay, the clock is reset by the feedback chain via delay line U2. The resulting 40 ns pulses are sent from the Q and Q- outputs of the flip-flop to inverters U11C and U11D. They also are sent as clock signals **WE+** and **(WE+RDALLMEM)-**. The Q output is delayed further by U2 and provided via inverter U9A as clock signal **DLYWE-** (Delayed Write Enable-).

Generation of all three clock outputs is terminated when **CLKINH+** goes high. The **CLKINH+** signal is sent to the input of U11A, holding flip-flop U10A reset. This condition occurs when data collection has been completed, or the FORCE DISPLAY keyboard key is depressed.

8.2.3 Address Decoder

The Address Decoder (sheet 1) consists of the following components: U25, a 74LS138 3-to-8 decoder; U32A, one-half of a 74LS138 3-to-8 decoder; U17, a 6308-1 256-word x 8-bit PROM; and U9E, one section of a 74S04 hex inverter. The processor has access to the State Memory board via the common Address and Data bus. U32A decodes the upper three bits of the address, enabling the PROM to generate eight control signals. The specific functions of the signals depend on the eight input controls. These controls and their functions are as follows:

a. **A12 and A11** determine which of the three memory boards (A, B, or C) is being accessed by the processor.

b. **A10** determines whether the upper byte (8-15) or lower byte (0-7) is being accessed by the processor.

c. **CSEL and BSEL** identify, by ground or voltage, in which of the three slots (A, B or C) the memory board is inserted. If the A memory is accessed by the processor, no control signals will be generated in the B and C memory slots. The A memory BSEL, CSEL levels combined with the A Memory Address on A15, A14, A13, A12 and A11, control these signals.

d. **S1** distinguishes between processor read and write commands.

e. **I/O/Mem** distinguishes between I/O and Memory addresses.

f. **Main/Aux** determines whether the collection (main) memory or the Aux memory is being accessed. They both have identical addresses. The Main/Aux signal is received from a State Control Board I/O bit.

The control signals that are generated by the Address Decoder are as follows:

a. **8-15EN** (8-15 Enable) enables the upper data byte (main memory only) onto the Processor Data Bus via buffer U13.

b. **0-7EN** (0-7 Enable) enables the lower main memory byte or the Aux Memory byte onto the Processor Data Bus via bi-directional buffer U14. The lower byte can be a read or write.

c. **AUX OE** enables the Aux Memory for a read operation.

d. **RDALLMEM-** (Read All Memory) enables all main memories on all Memory Boards for a read. The proper Memory is selected by the 8-15 and 0-7 enables.

e. **AUX CS-** selects the Aux Memory for read or write operation.

f. **AUX WE/T/R-** selects the Aux Memory for a write operation. Also places the U14 processor interface buffer in the write (receive) direction.

g. **STBUFEN-** (Setup Data Buffer Enable) enables decoder U25 to write the Qualifier-Word RAM, the Trigger-Word RAM, or probe outputs U21 and U22.

h. **RD STK-** (Read Stack Address) enables the Trigger Stack Address (trigger level) onto the Processor Data Bus.

8.2.4 Data Collection RAM

The Data Collection RAM (sheet 1) consists of U6, U7, U4 and U5, all 2149H 1K-word x 4-bit static RAMs.

The 10 outputs of the Collection Address Buffer are applied to the 10 address lines of the four 1Kx4 RAMs. The 16 output lines of the Collection Input Buffer are cascaded to the four sets of four data-in lines of the RAMs. U5 is at the high order end.

In the collection or write mode, pin 10 (write enable) of the RAMs is held low. The **WE+RDALLMEM** signal sent from the Clock Generator is applied in parallel to the chip select inputs of the RAMs. Therefore, in the write mode, the RAMs act as a single 1024-word x 16-bit RAM. 16-bit data words, sent from the Collection Input Buffer, are written to RAM by the write pulses from the Clock Generator. The Collection Address Counter on the State Control Board provides sequential addresses via the Collection Address Buffer. **ACLKINH+** places the RAMs in the write mode.

In the read mode, **ACLKINH** is high (no write enable). The **RDALLMEM** signal received from address decoder U17 is applied to chip select. Then data is transferred to the Processor bus via buffer U13 or U14, depending on the address selection.

8.2.5 Auxiliary RAM

The Auxiliary RAM consists of U15, an HM6116 2048 x 8-bit RAM. The AUX RAM is used to save a data collection from the Main Memory (1024 x 16-bit RAM). The data is saved by reading it out of the main memory and storing each byte in the AUX memory. The address for a given byte is identical for main memory or Aux memory. The processor makes the Main/Aux selection by setting an I/O bit on the State Control Board. The save routine might consist of the following partial sequence:

Output Main memory select
Read D2CF
Output Aux memory select
Write D2CF
Output Main memory select
Read D2D0
etc.

The data is read from the AUX RAM in the following manner: The 11 address lines **(A0-A10)** of RAM U15 are received from the Processor Address Bus. Buffer U14 is enabled in the transmit direction when a byte is read out.

Address Decoder outputs **AUXWE, AUXCS-** and **AUXOE-** are used as the write-enable, chip-select, and output-enable inputs of RAM U15.

8.2.6 Qualifier Word RAM

The Qualifier-Word RAM (sheet 2) consists of U26, U27, U30, U31 and U29, all 74S289 16-word x 4-bit static RAMs. The RAMs are connected as follows: The 16 data lines from the output of the Probe Input Buffer are divided into four sets of four lines. Four address inputs are sent to each of the four RAMs, U26, U27, U30 and U31. The four most significant bits are applied to the four address inputs of U26. Four qualifier signals **Q1, Q2, FT,** and **EXT** are sent from the Probe Input Buffer to the address lines of RAM U29.

Each RAM has 16 possible combinations of four bits on the address lines. These bits address the 16 word locations in the RAM. Thus, any given combination of values of the four probe input bits will be unique. This combination will address a unique word location in the specified RAM. Each word location contains four storage bits. These four bits are assigned as follows: Bit 0 to the **ARM** word; bit 1 to the **CQ1** clock-qualifier word; bit 2 to the **CQ2** clock-qualifier word; bit 3 to the **RESTART** word.

NOTE: The ARM word is used only in the Counter Timer/Signature Board. It is the first of the two trigger words shown on the respective menus. The Arm Comparator output is buffered and sent to a rear panel BNC.

As an example, assume that a menu has specified, in binary format, the following first clock-qualifier word:

0110 001X XXXX XXXX ..... -1XXXXX XX

The Control Program places the four most significant bits, 0110, on the address inputs of RAM U26. This is accomplished via the Setup Data Buffer. A 1 is written into the CQ1-word bit position (the second bit position). This is done via the DI1 input of the RAM using write enable **W3-** sent from the Address Decoder. The Control Program also writes into the other three bit positions for the **ARM, CQ2,** and **RESTART** words.

The 1 that is written into the 0110, bit-1 location means match. The Control Program writes a 0 (no match) into bit 1 of the other 15 words in RAM U26. Thus, when the four MSBs of the incoming data are 0110, RAM U26 will output a 1 from D01. For all other bit combinations, a 0 will be output from D01.

The next set of four bits, 001X, are used to address RAM U27. The Control Program writes a 1 into bit 1 of the words at addresses 0010 and 0011. This is done because the LSB of this set is a "don't care" X. A 0 is written into bit 1 of the remaining 14 words. For RAMs U30 and U31, the Control Program writes a 1 into bit 1 of all 16 words. This is done because all four address bits are Xs. RAM U29 is addressed by the qualifier-bit group, 1XXX. A 0 is written into bit 1 of the eight word locations addressed by 0000 through 0111. A 1 is written into bit 1 of the eight word locations addressed by 1000 through 1111.

Assume that at run-time, the data word shown below is clocked into the Probe Input Buffer. The data is clocked by **LATCHCLK** and placed on the address inputs of the five RAMs in the Qualifier-Word RAM. Refer to Figure 8-1.

	U26	U27	U30	U31	U29
Data Word	0110	0011	1010	0001	0000
Qual. Word	0110	001x	xxxx	xxxx	xxxx

The Control Program loads a 1 in bit 1 at address 0110, for RAM U26. This provides a match, making **D01** a 1. Similarly, output D01 is a 1 for U27, U30, U31, and U29. The 74S289 RAMs have open collector outputs. All four D01 outputs are tied together and applied to S2-3 as CQ1. This provides a wired AND for the four D01 outputs. For the input data word in the example, signal **CQ1** is high (logic 1).

RAM outputs CQ1, CQ2 of U26, U27, U30, U31 (data clock qualifiers) differ from CQ1 and CQ2 of U29 (probe clock qualifiers). A data clock qualifier will inhibit collection of an unqualified data word. It will not inhibit the generation of a data trigger signal. A probe clock qualifier will inhibit both data collection and trigger generation.

Now assume that the following data word is received.

	U26	U27	U30	U31	U29
Data Word	0111	0010	0001	1110	0000
Qual. Word	0110	001x	xxxx	xxxx	xxxx

This word produces a 0 at the D01 output U26, and signal **CQ1** goes low.

The Qualifier-Word RAM provides six output signals, **ARM**, data **CQ1, CQ2, RESTART.** and probe **CQ1, CQ2.** They are sent to connector pins S2-20, 3, 33, 17,19, and 18, respectively. Signals data **CQ1** and **CQ2** are used by the Clock Control on the State Control Board. This is shown on sheet 3 of that schematic DQ2 at U23.. Signal **RESTART** is used by the RESTART Generator on the State Control board. The **ARM** signal is a linkage from the timing analyzer. Probe CQ1 and CQ2 from U29 go to the Motherboard's U6 to generate CCLKQUALIN-.

8.2.7 Trigger Word RAM

The Trigger-Word RAM (sheet 2) consists of U34, U35, U38, U39 and U37. These are all Signetics 82S117 256-word x 1-bit static RAMs. The 256 1-bit word locations in each RAM are addressed by eight address inputs, **A7-A0.**

The Trigger-Word RAM inputs are configured in a similar manner as the Qualifier-Word RAM inputs. The 16 data lines output from the Probe Input Buffer are divided into four sets of four lines. One set is sent to address inputs A3-A0 of each of the four RAMs, U34, U35, U38 and U39. The four qualifier lines output from the Probe Input Buffer (**Q1, Q2, FT, EXT**) are sent to address inputs A3-A0 of U37. Trigger Stack Address lines **TSA3-TSA0** are received from the State Control Board. These signals are applied as address inputs A7-A4 of the five RAMs. These four address bits **(TSA3-TSA0)** are decoded into 16 blocks of 16 locations each. Each block represents one of the 16 trigger stack levels on the menu.

The Trigger-Word RAM performs the comparison function in much the same way as the Qualifier-Word RAM. The bit organization differs between the two. For example, start at level 0 of the trigger stack. As before, the incoming 20-bit data word is divided into five 4-bit groups. Each group feeds four address inputs of one of the five RAMs. These four bits address 16 locations. As in the Qualifier-Word RAM, each location represents one of 16 possible combinations of 1s and 0s for the four bits.

As with the Qualifier-Word RAM, each location is loaded at set-up time with a 1 or a 0. This provides a "match" or "no match" according to the bit configuration of the trigger word at stack level 0. As before, the five RAM outputs are connected in a wired AND configuration. Thus, there must be a match for all five 4-bit groups of the incoming data word. This will produce a TRUE output from the Trigger-Word RAM.

The four search words in the Qualifier-Word RAM are the **ARM, CQ1, CQ2** and **RESTART** words selected from the menu . All must be compared with the incoming data word simultaneously. Each search word is assigned a bit in the RAM output word. In the Trigger-Word RAM, the 16 trigger words are not compared simultaneously. Only the trigger word at the current trigger stack level is compared. Each of the 16 search words is assigned a block of 1-bit RAM words. The proper block is selected by the 4-bit Trigger Stack Address received by the A7-A4 inputs of each RAM.

A comparison is made as the Trigger Stack Address at the A7-A4 inputs of each RAM advances to the next higher stack level. At each advance, the four bits at the A3-A0 inputs are shifted to the next block of 16 stored bits. One bit is required for each of the 16 possible combinations of the four input data bits. At any given stack level, the five RAMs appear as a Qualifier-Word RAM having only one qualifier word.

The 82S117 RAMs have open collector outputs. All five single-bit outputs are wire ANDed to produce the output signal **TRIG+** (Trigger +) at connector pin S2- 16. The **TRIG+** signal is used by Stack Management on the State Control board. The pull-up resistor for the wired AND is on the State Control board. The RAM output is sent to U33B, translated to ECL level, inverted, and applied to S2-10 as signal **ST-** (State Trigger -).

8.3 BOARDS A, B, and C

The function differences between boards plugged into the A slot, B slot and C slot are discussed in the following paragraphs.

8.3.1 Qualifier BITS

There are two qualifier lines received from each of the three probe pods. Those coming from Pod A connect to Board A, Pod B to Board B, and Pod C to Board C. The EXT qualifier and LINK from the timing analyzer are applied to Boards A, B and C. These four signals are sent to each board at the inputs to U36A in the Probe Input Buffer. The term names of these signals are **Q1, Q2, EXT** and **FT.**

On the menu, the probe qualifier bits are displayed as follows:

-XXXXXX XX

The formatting is shown on the menu Clock Select line as follows:

QUALIFIERS: -AABBCCEL

With additional identification of signal names, the menu format is as follows:

QUALIFIERS: -AQ1,AQ2,BQ1,BQ2,CQ1,CQ2,
EXT,LINK

The signals at the Probe Input Buffer, Qualifier-Word RAMs and Trigger-Word RAMs are as shown below:

EXT,LINK,AQ1,AQ2 (for Board A)
EXT,LINK,BQ1,BQ2 (for Board B)
EXT,LINK,CQ1,CQ2 (for Board C)

The input qualifier lines, Q1 and Q2, are distinct from the outputs of the Qualifier-Word RAM, -CQ1 and -CQ2. For either the A or B Board, the -CQ1 output represents the result of the comparison of the following two words: An entire input data word and the entire menu-specified first clock-qualifier word, including both the Q1 and Q2 bits. Similarly, the -CQ2 output represents the result of the comparison of the following two words: An entire input data word and the entire menu-selected second clock-qualifier word, including both the Q1 and Q2 bits.

8.3.2 Signal CLKQUALIN

CLKQUALIN- (Clock Qualifier In -) is the signal that enables the Clock Generator. This is done by enabling U10 to produce Write Enable signal **WE-** at pin 6 (State Memory board), and **WE+** and **DLYWE-** clock pulses (State Control board). Signal **WE-** is the pulse that causes the current 16-bit data word to be stored in the Data Collection RAM. The **CLKQUALIN-** signal to State Memory Boards A and B are wired to a constant low (true) level. Refer to the Clk Qual Gate at the top of sheet 3, State Control Board schematic. Thus the State Memory Boards at the A or B sockets will collect a 16-bit data word at every occurrence of **LATCHCLK**. This is true regardless of the outcome of the clock-qualifier comparison. Board C provides a qualified master clock function. The clock signals (C)WE+ (S2, pin 5), and (C)DLYWE- (S2, pin 6) from board C drive the State Control Board address counter, where they are called BWE+ (S2-35) and BTAPCLK (S2-37), respectively.

The data words collected by Boards A and B are written one on top of the other into the same address. This continues until the clock qualification requirements set up in the Qualifier-Word RAM on Boards A, B and C are met. Then the C data word is collected as well as the A and B data words. Signals (C)WE+ and (C)DLYWE- are also generated so that the data collection address is advanced. The next A data word (qualified or not) is sent to the new address. This preserves the qualified A data word in the previous address.

8.3.3 Signal CLKINH

The Clock Generator on the State Memory Board can be inhibited from producing the **WE** family of clocks. This is done using signal **CLKINH+** (Clock Inhibit +) received from State Control.

State Control generates three such signals described as follows:
Signals **ACLKINH+** for Board A, **BCLKINH+** for Board B, and **CCLKINH+** for Board C.

Boards A, B and C finish the collection at the same time. The collection is stopped by concurrent signals **ACLKINH+**, **BCLKINH+** and **CCLKINH+** received from State Control. When processing the collected data, the Control Program reads 16-bit words from equivalent addresses in Boards A, B and C. The Control Program then places them side-by-side in main memory as one 48-bit word.

8.3.4 Signal BSELECT-

The Control Program can read from only one State Memory board at a time. It must write setup data into the Qualifier-Word RAM and Trigger-Word RAM one board at a time. This ability is provided by signal **BSELECT-**. This is sent via connector pin S2-15 to Address Decoder pin U17-5 with a pull-up resistor. Connector pin S2-15 is hard-wired low at the A and B sockets, but left open at the C socket. This causes **BSELECT-** to be high at the C Board. The A and B boards are differentiated by inverting the address line A11 that is sent to the A board. The Address Decoder responds to Board A and B addresses when the signal is low, and to Board C addresses when the signal is high.

8.4 FUNCTIONAL DESCRIPTION

A block diagram of the State Memory Board is shown in Figure 8-2. When appropriate, also refer to the schematic diagram, board layout and parts list at the end of this manual. Tables of connector pins versus signal names for the motherboard connectors are provided in MOTHER-BOARD CONNECTIONS. An alphabetical list of all signals is included. The GLOSSARY section offers explanations for terms that may be unfamiliar.

Major units of the State Memory Board circuitry include the following: Qualifier-Word RAM, Trigger-Word RAM, Data-Collection RAM, AUX RAM, Address Decoder, Clock Generator, and I/O buffers.

The qualifier-word memory and trigger-word memory can be considered as comparison devices. The data-collection and auxiliary RAM memory are typical storage devices. An operational description of these memories follows.

The Control Program stores the two menu-specified clock-qualifier words in the RAM. It also stores all the specified trigger words, level by level, in the Trigger-Word RAM. At run-time, an incoming data word is clocked into the Probe Input Buffer by the primary external clock. A data word consists of 18 parallel bits. These are comprised of 16 data bits and two qualifier bits. From the buffer, the data is sent to the Qualifier-Word RAM and the Trigger-Word RAM. The data is sent later to the Data Collection RAM.

The Qualifier-Word RAM compares the data word received with the two clock-qualifier words. The Trigger-Word RAM compares the incoming data word with the trigger word at the current trigger stack level. If the data word matches either of the clock-qualifier words, the current clock period is considered qualified for data. The data in the Probe Input Buffer is then stored in the Data Collection RAM.

If the qualifier-word comparison does not qualify the current clock period, the data word is not stored in the Data Collection RAM. Note that the menu may be specified with all bits as "don't care" X's. In that case, all clock periods will qualify.

This operation is described further in the following subsections.

8.4.1 Input/Output Buffers

Refer to schematic **#166-036801.**
The Input/Output Buffers are comprised of the following buffers: Probe Input Buffer, Probe Output Buffer, Setup Data Buffer, Read-TSA (Trigger Stack Address) Buffer, Collection Address Buffer, Collection Input Buffer, and Collection Output Buffer.

The **Probe Input Buffer** consists of U27 and U30, both 74F374 octal D flip-flops; and U26, one-half of a 74F374. The 16-bits of data at the probe pod are applied to U27 and U30 via S2. The 16 data outputs are sent to three locations; the Collection Input Buffer, and the address inputs on both the Qualifier-Word RAM and the Trigger-Word RAM. The reason for sending this data to the address lines of the two RAMs will be discussed later.

Two qualifier bits, Q1 and Q2, are sent from the probe via S2 to two of the four inputs of U26. The trigger output, FT, of the timing analyzer section is applied via S2 to the third input of U26. The external input EXT, at the BNC connector on the rear panel, provides the fourth input via S2. The four outputs of U26 are sent to address inputs on both the Qualifier-Word RAM and the Trigger-Word RAM.

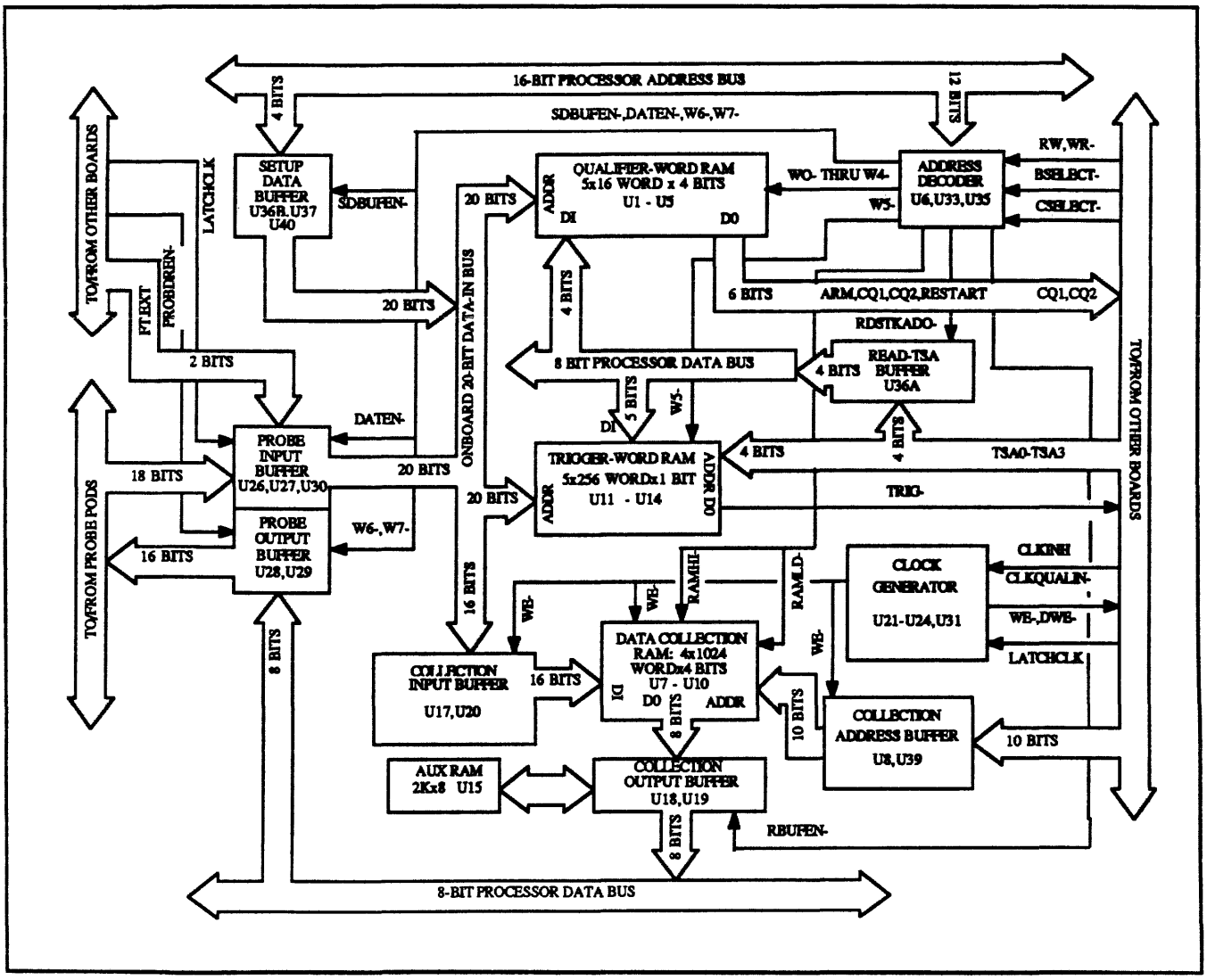

Figure 8-2: State Memory Board Block Diagram

U26, U27 and U30 are clocked by the menu-selected primary external clock, **LATCHCLK**. The signal **LATCHCLK** is received from the State Control board via S2. The outputs of all three devices are enabled at pin 1 when signal **STBUFEN** is low. This signal is received from U35 (pin 13), and is the inverse of STBUFEN- (Setup Data Buffer Enable-).

The **Probe Output Buffer** consists of U28 and U29, both 74F374 octal D flip-flops. This buffer is used to send data from the processor to either optional or custom probes designed to accomodate data output.

The eight inputs of U28 (DB0-DB7) are connected in parallel with those of U29 on the Processor Data Bus. The outputs of U28 and U29 are sent in cascade via S2 to the 16 probe data lines. The 8-bit input is demultiplexed to the 16-bit output using two strobe signals, **PROBEDREN 0-7** and **PROBEDREN 8-15**. The three-state outputs are enabled by **PROBEDREN** (Probe Data Remote Enable) that is generated at the State Control Board.

The **Setup Data Buffer** consists of U37 and U40, both 74F244 octal buffers and U36B, one-half of a 74F244. This buffer is used to load set-up data into the Qualifier-Word and Trigger-Word RAMs shown on sheet 3. This is described later in the Qualifier-Word RAM and Trigger Word RAM descriptions.

The 20 buffer outputs are sent in cascade via the On-board Data-In Bus to the Qualifier-Word and Trigger-Word RAMs on sheet 3, discussed later. The Buffer three-state outputs are enabled by **STBUFEN-** (Setup Data Buffer Enable -). This signal is sent from the Address Decoder.

The **Read-TSA Buffer** consists of U36A, one-half of a 74F244 octal buffer. It is used by the processor to read the trigger stack address supplied to the Trigger-Word RAM by State Control. The four input signals (**TSA0-TSA3**) are received from the State Control Board via S2. The four output lines of U36A are loaded onto the Processor Data Bus. The outputs are enabled by signal **RDSTK-** (Read Stack -) received from the Address Decoder.

The **Collection Address Buffer** consists of U38 and U39, both 74F373 octal D latches. The 10 input signals (**RA0-RA9**) are received by U38 and U39 via S2 from the State Control board. They are sent to the 10 address inputs of the Data Collection RAM U7-U10. If the current clock period is qualified for data collection, the **RA** signal is latched into the buffer. The latching is caused by the **RAMADEN** (RAM Address Enable) pulse received from the Clock Generator (Q- output at flip-flop U24). This data collection address is held by the Collection Address Buffer for the duration of the RAMADEN pulse.

The **Collection Input Buffer** consists of U17 and U20, both 74F374 octal D flip-flops. The 16 outputs of the Probe Input Buffer are applied to the 16 inputs of the Collection Input Buffer, then loaded by a delayed LATCHCLK. The 16 outputs of the Collection Input Buffer are applied in cascade to the Data Collection RAM and Collection Output Buffer. If the current clock period is qualified for data collection, signal **WE + RD ALL MEM** (Write Enable or Read All Memory) from the State Control Board is low. This allows the contents of the Collection Input Buffer to be written into the Data Collection RAM.

The two holding buffers (Collection Address & Input Buffers) are provided to compensate for propagation delays. The propagation delay is caused by the Clock Generator and qualification comparison. At high clock rates these delays may result in the next address and data word arriving before the current write has been completed. In this way the holding buffers allow sufficient time to complete the write to the Data Collection RAM.

The Collection Output Buffer consists of U1, a 74F244 octal buffer; and U18, a 74F245 bidirectional buffer. The processor uses the Collection Output Buffer to read collected data from the Data Collection RAM and AUX RAM. This is done for purposes of data analysis and display. The eight outputs of each RAM provide the 16 data inputs. The eight output lines are loaded onto the 8-bit Processor Data Bus. Signals **Ø-7EN** and **8-15EN** and **AUXWE,T/R-** received from the Address Decoder enable the buffer outputs to the bus.

8.4.2 Clock Generator

Refer to the schematic, sheet 2. The Clock Generator consists of the following components: U21 and U31, both 50 ns delay lines with selectable delay outputs; U22 and U32, 74F04 hex inverters; U23, a 74F02 quad NOR gate (section B is used as a negative input AND gate); and U24A, one-half of a 74F74 dual D flip-flop. A low **CLKQUALIN-** signal signifies that the current input data word is approved for data collection. When a low **CLKQUALIN** signal is received at U23 pin 6, the delayed data collection clock **WE+** (Write Enable -) is generated at U24A pin 6. The Clock Generator also provides **WE+** (an inverted WE-) and **C TAB CLOCK**, which becomes **DLYWE-** on the State Control Board. These signals are present at U23, pin 10 and U32, pin 2, respectively, for use by the State Control board.

The menu-selected primary external clock, **LATCHCLK** is received from the State Control board to clock the Probe Input Buffer. **LATCHCLK** also is sent via U22D to the delay line U31. After a nominal delay of 40 ns, U31 sends the clock pulse to the clock input of flip-flop U24A via U22F. If the output of U23B, pin 4, is high (by a low **CLKQUALIN** at the input), the flip-flop is set by the delayed clock. After a nominal 40 ns delay, the clock is reset by the feedback chain via delay line U21. The resulting 40 ns pulses are sent from the Q and Q- outputs of the flip-flop to inverters U23C and U23D. They also are sent as clock signals **WE+** and **(WE+RDALLMEM)-**. The Q output is delayed further by U21 and provided via inverter U22A as clock signal **C TAB CLK**.

Generation of all three clock outputs is terminated when **CLKINH+** goes high. The **CLKINH+** signal is sent to the input of U23A, holding flip-flop U24A reset. This condition occurs when data collection has been completed, or the FORCE DISPLAY keyboard key is depressed.

8.4.3 Address Decoder

The Address Decoder (sheet 2) consists of the following components: U25, a 74F138 3-to-8 decoder; U33A, one-half of a 74F138 3-to-8 decoder; U35, a 6308-1 256-word x 8-bit PROM; and U22C, one section of a 74F04 hex inverter. The processor has access to the State Memory board via the common Address and Data bus. U33A decodes the upper three bits of the address, enabling the PROM to generate eight control signals. The specific functions of the signals depend on the eight input controls. These controls and their functions are as follows:

a. **A12 and A11** determine which of the three memory boards (A, B, or C) is being accessed by the processor.

b. **A10** determines whether the upper byte (8-15) or lower byte (0-7) is being accessed by the processor.

c. **CSEL and BSEL** identify, by ground or voltage, in which of the three slots (A, B or C) the memory board is inserted. If the A memory is accessed by the processor, no control signals will be generated in the B and C memory slots. The A memory BSEL, CSEL levels combined with the A Memory Address on A15, A14, A13, A12 and A11, control these signals.

d. **S1** distinguishes between processor read and write commands.

e. **IO/Mem** distinguishes between I/O and Memory addresses.

f. **Main/Aux** determines whether the collection (main) memory or the Aux memory is being accessed. They both have identical addresses. The Main/Aux signal is received from a State Control Board I/O bit.

The control signals that are generated by the Address Decoder are as follows:

a. **8-15EN** (8-15 Enable) enables the upper data byte (main memory only) onto the Processor Data Bus via buffer U19.

b. **0-7EN, AUXEN** (0-7 Enable Aux. Enable) enables the lower main memory byte or the Aux Memory byte onto the Processor Data Bus via bi-directional buffer U18. The lower byte can be a read or write.

c. **AUX OE** enables the Aux Memory for a read operation.

d. **RDALLMEM-** (Read All Memory) enables all main memories on all Memory Boards for a read. The proper Memory is selected by the 8-15 and 0-7 enables.

e. **AUX CS-** selects the Aux Memory for read or write operation.

f. **AUX WE/T/R-** selects the Aux Memory for a write operation. Also places the U18 processor interface buffer in the write (receive) direction.

g. **STBUFEN-** (Setup Data Buffer Enable) enables decoder U6 to write the Qualifier- Word RAM, the Trigger-Word RAM, or probe outputs U28 and U29.

h. **RD STK-** (Read Stack Address) enables the Trigger Stack Address (trigger level) onto the Processor Data Bus.

8.4.4 Data Collection RAM

The Data Collection RAM (sheet 3) consists of U7, U8, U9, and U10, all 2149D-2 1K-word x 4-bit static RAMs.

The 10 outputs of the Collection Address Buffer are applied to the 10 address lines of the four 1Kx4 RAMs. The 16 output lines of the Collection Input Buffer are cascaded to the four sets of four data-in lines of the RAMs. U10 is at the high order end.

In the collection or write mode, pin 10 (write enable) of the RAMs is held low. The **WE+RDALLMEM** signal sent from the Clock Generator is applied in parallel to the chip select inputs of the RAMs. Therefore, in the write mode, the RAMs act as a single 1024-word x 16-bit RAM. 16-bit data words, sent from the Collection Input Buffer, are written to RAM by the write pulses from the Clock Generator. The Collection Address Counter on the State Control Board provides sequential addresses via the Collection Address Buffer. **ACLKINH+** places the RAMs in the write mode.

In the read mode, **ACLKINH** is high (no write enable). The **RDALLMEM** signal received from address decoder U35 is applied to chip select. Then data is transferred to the Processor bus via buffer U18 or U19, depending on the address selection.

8.4.5 Auxiliary RAM

The Auxiliary RAM consists of U34, an HM6116 2048 x 8-bit RAM. The AUX RAM is used to save a data collection from the Main Memory (1024 x 16-bit RAM). The data is saved by reading it out of the main memory and storing each byte in the AUX memory. The address for a given byte is identical for main memory or Aux memory. The processor makes the Main/Aux selection by setting an I/O bit on the State Control Board. The save routine might consist of the following partial sequence:

Output Main memory select
Read D2CF
Output Aux memory select
Write D2CF
Output Main memory select
Read D2D0
etc.

The data is read from the AUX RAM in the following manner: The 11 address lines **(A0-A10)** of RAM U34 are received from the Processor Address Bus. Buffer U18 is enabled in the transmit direction when a byte is read out.

Address Decoder outputs **AUXWE, AUXCS-** and **AUXOE-** are used as the write-enable, chip-select, and output-enable inputs of RAM U34.

8.4.6 Qualifier Word RAM

The Qualifier-Word RAM (sheet 3) consists of U1-U5, all 74S189 16-word x 4-bit static RAMs. The RAMs are connected as follows: The 16 data lines from the output of the Probe Input Buffer are divided into four sets of four lines. Four address inputs are sent to each of the four RAMs, U1-U4. The four most significant bits are applied to the four address inputs of U26. Four qualifier signals **Q1, Q2, FT,** and **EXT** are sent from the Probe Input Buffer to the address lines of RAM U5.

Each RAM has 16 possible combinations of four bits on the address lines. These bits address the 16 word locations in the RAM. Thus, any given combination of values of the four probe input bits will be unique. This combination will address a unique word location in the specified RAM. Each word location contains four storage bits. These four bits are assigned as follows: Bit 0 to the **ARM** word; bit 1 to the **CQ1** clock-qualifier word; bit 2 to the **CQ2** clock-qualifier word; bit 3 to the **RESTART** word.

NOTE: The ARM word is used only in the Counter Timer/Signature Board. It is the first of the two trigger words shown on the respective menus. The Arm Comparator output is buffered and sent to a rear panel BNC.

As an example, assume that a menu has specified, in binary format, the following first clock-qualifier word:

0110 001X XXXX XXXX ..... -1XXXXX XX

The Control Program places the four most significant bits, 0110, on the address inputs of RAM U1. This is accomplished via the Setup Data Buffer. A 1 is written into the CQ1-word bit position (the second bit position). This is done via the DI1 input of the RAM using write enable **W3-** sent from the Address Decoder. The Control Program also writes into the other three bit positions for the **ARM, CQ2,** and **RESTART** words.

The 1 that is written into the 0110, bit-1 location means match. The Control Program writes a 0 (no match) into bit 1 of the other 15 words in RAM U1. Thus, when the four MSBs of the incoming data are 0110, RAM U1 will output a 1 from D01. For all other bit combinations, a 0 will be output from D01.

The next set of four bits, 001X, are used to address RAM U2. The Control Program writes a 1 into bit 1 of the words at addresses 0010 and 0011. This is done because the LSB of this set is a "don't care" X. A 0 is written into bit 1 of the remaining 14 words. For RAMs U3 and U4, the Control Program writes a 1 into bit 1 of all 16 words. This is done because all four address bits are Xs. RAM U5 is addressed by the qualifier-bit group, 1XXX. A 0 is written into bit 1 of the eight word locations addressed by 0000 through 0111. A 1 is written into bit 1 of the eight word locations addressed by 1000 through 1111.

Assume that at run-time, the data word shown below is clocked into the Probe Input Buffer. The data is clocked by **LATCHCLK** and placed on the address inputs of the five RAMs in the Qualifier-Word RAM. Refer to Figure 8-1.

	U1	U2	U3	U4	U5
Data Word	0110	0011	1010	0001	0000
Qual. Word	0110	001x	xxxx	xxxx	xxxx

The Control Program loads a 1 in bit 1 at address 0110, for RAM U1. This provides a match, making **D01** a 1. Similarly, output D01 is a 1 for U2-U5. The 74S189 RAMs have open collector outputs. All four D01 outputs are tied together and applied to S2-3 as CQ1. This provides a wired AND for the four D01 outputs. For the input data word in the example, signal **CQ1** is high (logic 1).

RAM outputs CQ1, CQ2 of U1-U4 (data clock qualifiers) differ from CQ1 and CQ2 of U5 (probe clock qualifiers). A data clock qualifier will inhibit collection of an unqualified data word. It will not inhibit the generation of a data trigger signal. A probe clock qualifier will inhibit both data collection and trigger generation.

Now assume that the following data word is received.

	U1	U2	U3	U4	U5
Data Word	0111	0010	0001	1110	0000
Qual. Word	0110	001x	xxxx	xxxx	xxxx

This word produces a 0 at the D01 output U1, and signal **CQ1** goes low.

The Qualifier-Word RAM provides six output signals, **ARM**, data **CQ1, CQ2, RESTART.** and probe **CQ1, CQ2.** They are sent to connector pins S2-20, 3, 33, 17, 19, and 18, respectively. Signals data **CQ1** and **CQ2** are used by the Clock Control on the State Control Board. This is shown on sheet 2 of that schematic (DQ1, DQ2 at U23). Signal **RESTART** is used by the RESTART Generator on the State Control board. The **ARM** signal is a linkage from the timing analyzer. Probe CQ1 and CQ2 from U5 go to the Motherboard's U6 to generate CCLKQUALIN-.

8.4.7 Trigger Word RAM

The Trigger-Word RAM (sheet 3) consists of U11-U15. These are all 27L501 256-word x 1-bit static RAMs. The 256 1-bit word locations in each RAM are addressed by eight address inputs, **AD7-AD0.**

The Trigger-Word RAM inputs are configured in a similar manner as the Qualifier-Word RAM inputs. The 16 data lines output from the Probe Input Buffer are divided into four sets of four lines. One set is sent to address inputs AD3-AD0 of each of the four RAMs. The four qualifier lines output from the Probe Input Buffer (**Q1, Q2, FT, EXT**) are sent to address inputs A3-A0 of U15. Trigger Stack Address lines **TSA3-TSA0** are received from the State Control Board. These signals are applied as address inputs A7-A4 of the five RAMs. These four address bits (**TSA3-TSA0**) are decoded into 16 blocks of 16 locations each. Each block represents one of the 16 trigger stack levels on the menu.

The Trigger-Word RAM performs the comparison function in much the same way as the Qualifier-Word RAM. The bit organization differs between the two. For example, start at level 0 of the trigger stack. As before, the incoming 20-bit data word is divided into five 4-bit groups. Each group feeds four address inputs of one of the five RAMs. These four bits address 16 locations. As in the Qualifier-Word RAM, each location represents one of 16 possible combinations of 1s and 0s for the four bits.

As with the Qualifier-Word RAM, each location is loaded at set-up time with a 1 or a 0. This provides a "match" or "no match" according to the bit configuration of the trigger word at stack level 0. As before, the five RAM outputs are connected in a wired AND configuration. Thus, there must be a match for all five 4-bit groups of the incoming data word. This will produce a TRUE output from the Trigger-Word RAM.

The four search words in the Qualifier-Word RAM are the **ARM, CQ1, CQ2** and **RESTART** words selected from the menu . All must be compared with the incoming data word simultaneously. Each search word is assigned a bit in the RAM output word. In the Trigger-Word RAM, the 16 trigger words are not compared simultaneously. Only the trigger word at the current trigger stack level is compared. Each of the 16 search words is assigned a block of 1-bit RAM words. The proper block is selected by the 4-bit Trigger Stack Address received by the A7-A4 inputs of each RAM.

A comparison is made as the Trigger Stack Address at the A7-A4 inputs of each RAM advances to the next higher stack level. At each advance, the four bits at the A3-A0 inputs are shifted to the next block of 16 stored bits. One bit is required for each of the 16 possible combinations of the four input data bits. At any given stack level, the five RAMs appear as a Qualifier-Word RAM having only one qualifier word.

The 27LS01 RAMs have open collector outputs. All five single-bit outputs are wire ANDed to produce the output signal **TRIG+** (Trigger +) at connector pin S2- 16. The **TRIG+** signal is used by Stack Management on the State Control board. The pull-up resistor for the wired AND is on the State Control board. The RAM output is sent to U25B, translated to ECL level, inverted, and applied to S2-10 as signal **ST-** (State Trigger -).

8.5 BOARDS A, B, and C

The function differences between boards plugged into the A slot, B slot and C slot are discussed in the following paragraphs.

8.5.1 Qualifier BITS

There are two qualifier lines received from each of the three probe pods. Those coming from Pod A connect to Board A, Pod B to Board B, and Pod C to Board C. The EXT qualifier and LINK from the timing analyzer are applied to Boards A, B and C. These four signals are sent to each board at the inputs to U26A in the Probe Input Buffer. The term names of these signals are **Q1, Q2, EXT** and **FT.**

On the menu, the probe qualifier bits are displayed as follows:

-XXXXXX XX

The formatting is shown on the menu Clock Select line as follows:

QUALIFIERS: -AABBCCEL

With additional identification of signal names, the menu format is as follows:

QUALIFIERS: -AQ1,AQ2,BQ1,BQ2,CQ1,CQ2,
EXT,LINK

The signals at the Probe Input Buffer, Qualifier-Word RAMs and Trigger-Word RAMs are as shown below:

EXT,LINK,AQ1,AQ2 (for Board A)
EXT,LINK,BQ1,BQ2 (for Board B)
EXT,LINK,CQ1,CQ2 (for Board C)

The input qualifier lines, Q1 and Q2, are distinct from the outputs of the Qualifier-Word RAM, -CQ1 and -CQ2. For either the A or B Board, the -CQ1 output represents the result of the comparison of the following two words: An entire input data word and the entire menu-specified first clock-qualifier word, including both the Q1 and Q2 bits. Similarly, the -CQ2 output represents the result of the comparison of the following two words: An entire input data word and the entire menu-selected second clock-qualifier word, including both the Q1 and Q2 bits.

8.5.2 Signal CLKQUALIN

CLKQUALIN- (Clock Qualifier In -) is the signal that enables the Clock Generator. This is done by enabling U24 to produce Write Enable signal **WE-** at pin 6 (State Memory board), and **WE+** and **C TAB CLK** clock pulses (State Control board). Signal **WE+RDALLMEM** is the pulse that causes the current 16-bit data word to be stored in the Data Collection RAM. The **CLKQUALIN-** signal to State Memory Boards A and B are wired to a constant low (true) level. Refer to the Clk Qual Gate at the top of sheet 3, State Control Board schematic. Thus the State Memory Boards at the A or B sockets will collect a 16-bit data word at every occurrence of **LATCHCLK**. This is true regardless of the outcome of the clock-qualifier comparison. Board C provides a qualified master clock function. The clock signals **(C)WE+** (S2, pin 5), and **(C)CTABCLK** (S2, pin 6) from board C drive the State Control Board address counter, where they are called **BWE+** (S2-35) and **BTAPCLK** (S2-37), respectively.

The data words collected by Boards A and B are written one on top of the other into the same address. This continues until the clock qualification requirements set up in the Qualifier-Word RAM on Boards A, B and C are met. Then the C data word is collected as well as the A and B data words. Signals **(C)WE+** and **(C)CTABCLK** are also generated so that the data collection address is advanced. The next A data word (qualified or not) is sent to the new address. This preserves the qualified A data word in the previous address.

8.5.3 Signal CLKINH

The Clock Generator on the State Memory Board can be inhibited from producing the **WE** family of clocks. This is done using signal **CLKINH+** (Clock Inhibit +) received from State Control.

State Control generates three such signals described as follows:
Signals **ACLKINH+** for Board A, **BCLKINH+** for Board B, and **CCLKINH+** for Board C.

Boards A, B and C finish the collection at the same time. The collection is stopped by concurrent signals **ACLKINH+**, **BCLKINH+** and **CCLKINH+** received from State Control. When processing the collected data, the Control Program reads 16-bit words from equivalent addresses in Boards A, B and C. The Control Program then places them side-by-side in main memory as one 48-bit word.

8.5.4 Signal BSELECT-

The Control Program can read from only one State Memory board at a time. It must write setup data into the Qualifier-Word RAM and Trigger-Word RAM one board at a time. This ability is provided by signal **BSELECT-**. This is sent via connector pin S2-15 to Address Decoder U35, pin 5 with a pull-up resistor. Connector pin S2-15 is hard-wired low at the A and B sockets, but left open at the C socket. This causes **BSELECT-** to be high at the C Board. The A and B boards are differentiated by inverting the address line A11 that is sent to the A board. The Address Decoder responds to Board A and B addresses when the signal is low, and to Board C addresses when the signal is high.

SECTION 9: MODEL 800 D STATE CONTROL BOARD

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9.1 INTRODUCTION

The Model 800 D contains one State Control board. It directs the acceptance of data for storage by the State Memory boards for later analysis and display. Hardware registers, counters and RAMs on the State Control board are loaded by the Firmware Resident Control Program. The loading information is entered from the keyboard under the guidance of the SETUP and PROGRAM menus. Using the parameters and modes specified, the State Control board implements the various state analysis operations.

9.2 DESCRIPTION

A block diagram of the 25 MHz State Analyzer is shown in Figure 9-1. Also refer to the schematic **#166-036101**, board layout and parts list included at the end of this manual. Tables of connector pins versus signal names for all motherboard connectors are provided in MOTHERBOARD CONNECTIONS. An alphabetical list of all interboard signals is included. The GLOSSARY section offers explanations for terms that may be unfamiliar.

The functional units of the State Control board are the Processor Interface, Sequencer, Clock Control, Collection Address Counter and Delay Counter. These units are discussed in the following subsections starting on page 9-3.

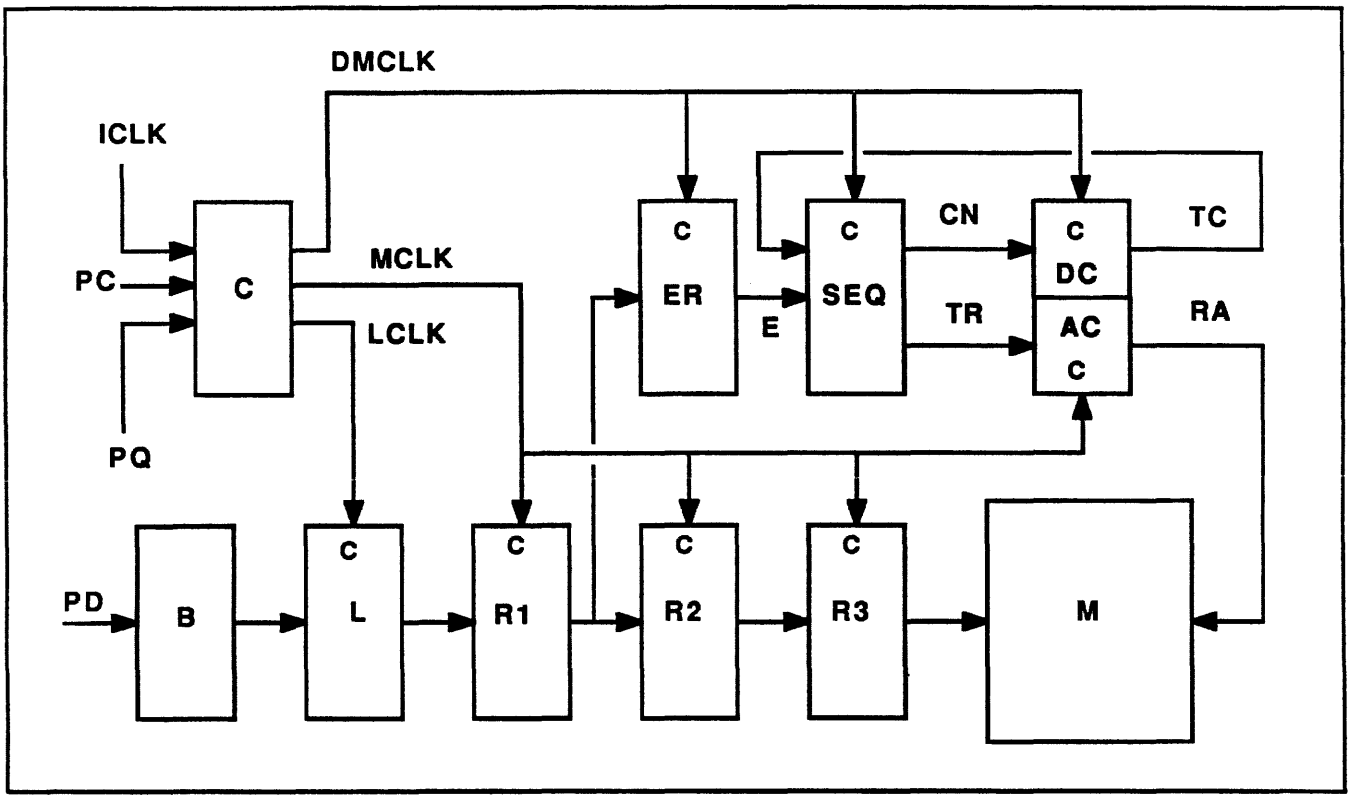

Figure 9-1: 25 MHz State Analyzer Block Diagram

Legend					
a	address input	C	clock select	ICLK	internal clock
c	clock input	L	local latch	LCLK	local clock
d	data input	M	collection memory	MCLK	master clock
E	event output	R1	1st stage register	DMCLK	delayed master
RA	memory address	R2	2nd stage register clock	PC	probe clock
TC	terminal count	R3	3rd stage register	PQ	clock qualifier
TR,CN	count enable	ER	event recognizer	PD	Probe data
B	buffer				

9.2.1 Processor Interface

Refer to sheet 4. The Processor Interface is comprised of the Address Decoder, Status Ports, Interface Output Ports, and Interface Shift Register. This circuitry allows the processor, under the direction of the Control Program, to load user-supplied information. This information is entered from the keyboard with the aid of menus. To prepare the analyzer for the intended application, the information is entered into registers, RAMs, and counters. The interface allows the processor to interrogate status and signal lines, and send various control signals when appropriate.

The 74LS138 address decoder (U35) decodes information to generate the following outputs: the clock signal for the sequencer, the enable signal for the status reads, and the enable signal for the memory address readouts. The clock inhibit circuit (sheet 2 Section C2) takes **SEL** and **ROLLOVER** as inputs, and uses one of them as the clock inhibit signal **-HALT**. This signal is used to stop the delayed master clock and also sent to the processor status port. The signal SEL from the shift register is used to select MEMORY FULL or the SEQUENCE DONE condition as the clock inhibit signal.

Every time the processor accesses the state analyzer hardware for loading test parameters, collection display, or saves into the auxiliary memory, it activates the LOAD ADDRESS (**LDA-**) signal (sheet 4). Generated via decoder U51, the signal is applied to the counters U62, U63, U64 which then function as latches. The addresses on the S1 bus from the processor will address the memories directly.

During the collection, the processor reads via U61 (the 74S157), U48 (the 74LS244) and U13 (the 74LS74) in Section B5, the addresses of the memories in order to determine how many clocks have been received from the probes, and when the collection finished. The processor reads these counters (U62-U64) to find the last memory address.

U52 is a 74LS374 latch, loaded by the processor to control memory selection, clock selection, and probe control lines.

On sheet 2, U50 is another 74LS374 control latch, and U49 is a 74LS244 buffer for reading the State Control status. **SRDATA-** from U50 (pin 5) is used as a serial data line to load several 4015 shift registers with control signals (U29, U32 on sheet 3, U2, U41, U42 on sheet 5.) SRCLK from U50 (pin 2) clocks the serial loading of the shift registers.

9.2.2 Sequencer Operation

Refer to sheet 2. The sequencer, a state machine, is comprised of 2149-21 RAMs (U30 and U31) and a latch (74F374) U46. It has 16 states, two for every program line on the menu. Each program line consists of three sentences: the STORE condition, the first IF condition (containing the counter and link outputs), and the ELSE condition (the second IF condition). The first sequencer state is used to load the delay counters and the second state is used for the counting. Both sequencer states control all the subsequent functions such as TRACE, LINK, etc. The states used for loading the counters are the even numbered states. The sequencer remains at that state only for one clock. The initial state the sequencer starts from after loading is state 0 and the last state is state 15. Depending on how the user has setup the PROGRAM MENU, the sequencer can jump from any state to another.

The signal that inhibits the clocks at termination of the collection is called **HALT-** . It is decoded from the sequencer by U7 and U60. This signal also informs the processor that the state analyzer is done collecting. Among other status signals, **S0-S4** are used to report the status of the sequencer to the CPU via U49 (normally displayed in the lower left corner of the display screen). This readout is translated to the step number on the PROGRAM MENU. Two other signals go to U49: **AQ** and **BQ** which are the qualifier bits from the probes. These signals, in addition to being used as qualifier bits, are also used as control lines in "handshaking" for dedicated probes.

The word recognizer outputs (**WR1-WR5**) from the State Memory board arrive at the State Control board via the custom 60 wire S2 bus. There they are latched in by U44 (74F374) with the master clock and address the sequencer RAM to determine the next state.

These RAM's are loaded according to the events (the user's defined bit pattern) from the STATE PROGRAM menu. This is done by the processor after the COLLECT function has been entered. During the loading of the RAM's, addresses from the CPU for the S0-S3 inputs (via U45) are latched in U46. For the lines **WR1-WR4, RG** and **TC-**, inputs are latched in U47. The data to the RAM's are latched in U45. While loading the RAM's, the outputs of the latch for the word recognizers, U44, are put in tri-state mode.

When the analyzer sequencer has been loaded and it's ready for collection, the output of U45 and U47 will go to tri-state mode and U44 will be active. U46 is used in either the loading or the collecting mode; in the collecting mode it latches the sequencer output. It should also be noted that the fifth word recognizer (which can also be used as a 32 bit wide range recognizer) **WR5/RNG** output from the State Memory board goes through more logic (U8, U10, U23) located on the State Control board before being latched.

9.2.3 Clock Control

Clock control is comprised of the Clock Multiplexer and the Clock Qualifier Gate (sheet 5). This circuitry implements the keyboard entered selection of clock source and provides the final logic in the process of clock qualification.

Unlike the Model 800 A, B, or C system, all the clocks from the probes come in to the State Control board. In order to have a flexible clock selection from the menu, the clocks go through a multiplexer circuit. The clocks are implemented in ECL logic to reduce the accumulated clock delay with respect to the data. The clocks and the qualifiers are translated to ECL levels in U69 and U71 (10124) in Section B/C7. The 4015B CMOS shift registers (U12, U41, U42) in Section D4-7 get loaded by the processor to control which clock (or combination of clocks) is selected from which Probe pod, and for which memory board. Also selected is the Master Clock source(s) Since the clock circuit functions on all ECL levels, U41 and U42 are translated to 0V for high level and to -5V for low level by two 2N3905 transistors (Q1 and Q2) in Section D6. Gates U56 and U70C,D enable the clock qualifiers, if selected. Qualifier latches U57A and U55 are wire-OR'ed with the probe clocks to product qualified clocks.

There are three such circuits: one for the intermediate clocks (Cr, Cs, Ct) from each of the three probes. After propagating through these circuits, the three intermediate clocks drive four MUX circuits in U24, U39, U40, U70. Here they are ORed with each other per the menu specification. For example, the user may need either a read or write signal to clock the analyzer and therefore specify the Boolean combination Cr+Cs from the A and B Probes. The output of the clock circuits has been translated to TTL level by the 10125, U68 in Section C2.

The master clock circuit functions differently than the intermediate latch clock circuit since it uses a delay pipeline U54 (10197). This pipeline circuit is adjusted at final test with jumpers E19-E23 connected to E24. See Section B2. This is done so that when the master clock and the intermediate latch clocks have the same source (i.e., they happen at the same time) the master clock is delayed several nanoseconds. This allows for the propagation of the first set of latches on the State Memory board. These latches (U14 and U27) on the State Memory board (sheet 1) are clocked by the latch clocks (LCLK) before latching the data into the first memory pipeline registers (U13, U28).

If the internal clock is used to asynchronously clock the data from the Model 51A State Probes, then that signal comes into the clock circuitry on sheet 5 (Section C1) via the S2 bus, Pin 36. This signal's source is the Timing Analyzer 200 MHz Oscillator and Divider Chain. The highest Timing Analyzer clock sample frequency useable on this board is 50 nanoseconds; all such inputs are enabled only when the CMOS shift register (U12) in Section D7 and the level translator U69 drive a low level to U53 Pins 7 and 10.

Also provided is an initialization circuit (U20, U21, U66, U67) on sheet 5 so that the very first clock will not be a glitch. This is possible since the processor which enables the clock circuit for collection and the incoming clocks are asynchronous.

9.2.4 Collection Address Counters

The State Memory board high speed RAM addresses come from the State Control board. These collection memory addresses **RA0-9** are generated by 74F191 counters U62, U63, U64 (sheet 4) which are decade counters in an increment mode. U64 is the LSB stage. Prior to collection, these counters get preset to 23. After 1000 counts (the memory capacity) the rollover bit will be set (U65, Section A3) if the collection hasn't already halted due to a Program Menu condition.

This address is applied to the memory board's address port and the 74LS244 buffer (U48). It is sent to custom 60 wire S2 bus. The start address of the collection memory is loaded to the counter by the memory read signal **-LDA** and processor address **A0-9**. The signal -LDA is produced from the Control Program so the address counter becomes the buffer of the processor address A0-9 when -LDA is true. Then the processor can read the collection memory content on each State Memory board. The signal ROLLOVER on U65-5 (74S74) will go high if the address RA0-9 is more than 1024. This signal is sent to the boards status port and the clock inhibit circuit.

9.2.5 Delay Counter

There are 8 steps on the PROGRAM MENU. Each step has a universal counter available for clock or event (pass) delay counting. Therefore, the hardware must have either 8 sets of counters, or a set of programmable counters. The single set consists of high speed 74F190 decade counters (U2, U3, U4, U5) on sheet 3 to count from 0000-9999. These counters get loaded from high speed RAM's (U14-U17) which are addressed by the sequencer. The RAM addresses are altered every time the sequencer changes state. Therefore, during collection when the sequencer changes state, it addresses a different location in the RAM's which send a different data to be loaded into the counters.

The data in the RAM's are from the user defined count on the State Program Menu. It is loaded into the RAM's through the serial shift registers (4015 U29 and U32) by the processor just before the collection starts. The counter's output signals are decoded through U1, U6 and U18. This decode is called **TC-**, and occurs when all counters have reached their terminal count. It should be noted that U2 is in the increment mode and U3, U4, U5 are in he decrement mode.

While U3, U4 and U5 count down, U2 counts up because the AND gate U18 (74S134) needs high active signals to generate the terminal count -TC. The 16x4 RAMs (27S03A) U14, U15, U16, U17 store the BCD counts of 8 sequencer steps. When -PL (Section D7) goes low, the new count is loaded to the counter. The S1-S3 and RI1-RI16 buses and **-WRC** (write strobe) are used to program the RAMs. The delay counter is enabled by **CNT/HLD-** when high, and its output, the terminal count -TC, is feedback to the sequencer.

9.3 STATE CONTROL SIGNAL LIST

The signal list is on pages 9-8 and 9-9.

9.4 STATE CONTROL BOARD S2 PINS

The State Control Board S2 pin assignments are on page 9-10.

MODEL 800 D 25 MHz STATE CONTROL SIGNAL LIST

SIGNAL	DESCRIPTION
A CLK SEL	Selects edge of external clock A.
A CNTL	Control bit used with microprocessor dedicated probes.
A PROB DREN-	Enables analyzer to output data to probe A.
A0-A15	CPU board processor address bus.
A PROB CLK	Clock coming from probe A, same as Cr on the menu.
AQ	Qualifier bit from probe A.
AQ CLK SEL	Selects the polarity of the A probe clock qualifier.
B CLK SEL	Selects edge of the external clock B.
B PROB DREN-	Enables the analyzer to output data to probe B.
BPROB CLK	Clock coming from probe B, same as Cs on the menu.
BQ	Qualifier bit from the B probe.
BQ CLK SEL	Selects polarity of the B probe clock qualifier.
CLK2	Clocks the data into registers for loading.

SIGNAL	DESCRIPTION
CLKINH1-	Inhibits clocks when rollover occurs.
CLKINH2-	Inhibits clocks at the ECL translators when either rollover occurs or when the processor sets the SCLKINH-.
SCKLINH-	Software clock inhibit issued by the processor.
CNT/HLD-	When high, it allows delay counters to count.
CPROB CLK	Clock coming from probe C, same as Ct on the menu.
CQ	Qualifier bit from the C probe.
CT	Internal clock source from timing analyzer, ECL.
DB0-DB7	CPU board based processor data bus.
HALT-	When low, inhibits clocks from making further collections; also lets the processor know state analyzer is done.
INIT-	Initializes clock circuit at beginning of each collect.
IO/M-	Low when memory locations are addressed versus I/O.
IOEN-	Low when input/output ports are addressed versus memory.
LCLK1	Intermediate latch clock for State Memory Board 1.

SIGNAL	DESCRIPTION
LCLK2	Intermediate latch clock for State Memory Board 2.
LCLK3	Intermediate latch clock for State Memory Board 3.
LDA-	When low, loads address counter with processor address.
LINK	Signal connected to the link bus.
MAIN/AUX-	When low, selects Aux Memory for read/write operation.
CLK1	Clocks the menu data into registers during loading.
MCLK	Master clock, generated on board latching all intermediate clocks.
MCLK1	Master clock, buffered.
MCLK2	Master clock, buffered.
PL-	When low loads data from RAMS into delay counters.
PROBEN	Control bit for enabling probe A & B DREN-.
RA0-RA9	Output of address counters from SCB to SMB.
RD RAM ADD	When low enables processor to read address counter output.
RD STATUS-	When low, enables processor to read status port.
ROLLOVER	Status bit indicating 1000 address counts. When set high, indicates 1000 samples collected in memory.
RW	When low, processor is doing a read operation.
S BUS	S0-S3 bits.
SEL	When set high, allows either rollover or sequencer to initiate the HALT-; when set low, rollover has no control.
SR CLK	Shift register clock.
SR DATA	Shift register data.
TC-	Output of the delay counter circuit; when low, indicates end of count.
TRACE	When high, allows data to be recorded in the memory.
TS-	When high, sets output of several registers and TC- signal to TRI- state.
WE-	Write signal for high speed memories.
WR SEQ-	Used during load; when low, writes to sequencer rams.
WR1-WR4	Word recognizer inputs from the SMB.
WRC-	Writes signal for delay counter rams.
WR STATE CNTL-	Writes the control bits into U50.

Model 800 D State Control Board S2 Pin Assignment

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	31	GND
2	MAIN/AUX-	32	
3	WE-	33	
4	ALCLK	34	BLCLK
5		35	CCLK
6	CLCLK	36	CT
7		37	WR5
8		38	MCLK
9	RA7	39	
10	RA6	40	CQ
11	RA5	41	CPROBCLK
12	RA4	42	LINK
13	RA3	43	APROBDREN-
14	RA2	44	BPROBDREN-
15	RA1	45	
16	RA0	46	
17	WR4	47	
18	WR3	48	
19	WR2	49	
20	WR1	50	
21		51	
22		52	
23	APROBCLK	53	
24	ACLKSEL	54	BQCLKSEL
25	AQ	55	BQ
26	AQCLKSEL	56	BCLKSEL
27	ACTL	57	BPROBCLK
28	RA8	58	
29	RA9	59	
30	GND	60	GND

SECTION 10: MODEL D STATE MEMORY BOARD (25 MHz)

10.1 Introduction — 10-1

10.2 Description — 10-2
- 10.2.1 Pipeline Registers — 10-3
- 10.2.2 Word Recognizer RAM — 10-3
- 10.2.3 Processor Interface — 10-4
- 10.2.4 Input/Output Buffers — 10-4
- 10.2.5 Address Decoder — 10-5
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10.3 Boards A, B and C — 10-7
- 10.3.1 Qualifier BITS — 10-7
- 10.3.2 Signals BSEL and CSEL — 10-8
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10.5 Pin Assignments — 10-8

10.1 INTRODUCTION

The Model 800 D is a 25 MHz, 48 channel Logic State Analyzer. Some differences between other models in the 800 Series exist on the Motherboard for this analyzer. Each of the State Memory boards accept data from 16 incoming data lines. If directed by the State Control, the data is stored for later analysis and display. The Model 800 D contains three State Memory boards. Each board receives 16 data lines from the associated and interchangeable Model 51A Probe Pod A, B, or C. The boards are designated State Memory board A, B and C, respectively. On the Setup Menu, they are referred to as Memory 1, 2, and 3, respectively. The three boards are identical and interchangeable. However, certain connections to the Motherboard allow each allocated socket to operate differently. The following discussion will apply to all the State Memory boards, except as noted.

10.2 FUNCTIONAL DESCRIPTION

A block diagram of the State Analyzer is shown in Figure 10-1. When appropriate, also refer to the schematic diagram, board layout and parts list at the end of this section. Tables of connector pins versus signal names for motherboard connectors are provided in MOTHERBOARD CONNECTIONS. An alphabetical list of all signals is included. The GLOSSARY section offers explanations for terms that may be unfamiliar.

Major functional units of the State Memory board circuit include the: Word-Recognizer RAM, High Speed Data-Collection RAM, Low Speed Auxiliary (AUX) RAM, Address Decoder, Pipeline Registers, and I/O buffers.

The **Word-Recognizer Memory** can be considered a comparison device. The data collection and auxiliary RAM memory are typical storage devices.

The Control Program stores the five menu-specified EVENT bit patterns in the RAM, program step by program step. At run-time, an incoming data word is clocked into the Probe Input Buffer by the primary external clock. A data word consists of 18 parallel bits. These are comprised of 16 data bits and two qualifier bits from each probe. From the buffer, the data is sent to the intermediate latch. The data is sent later to the Data Collection RAM.

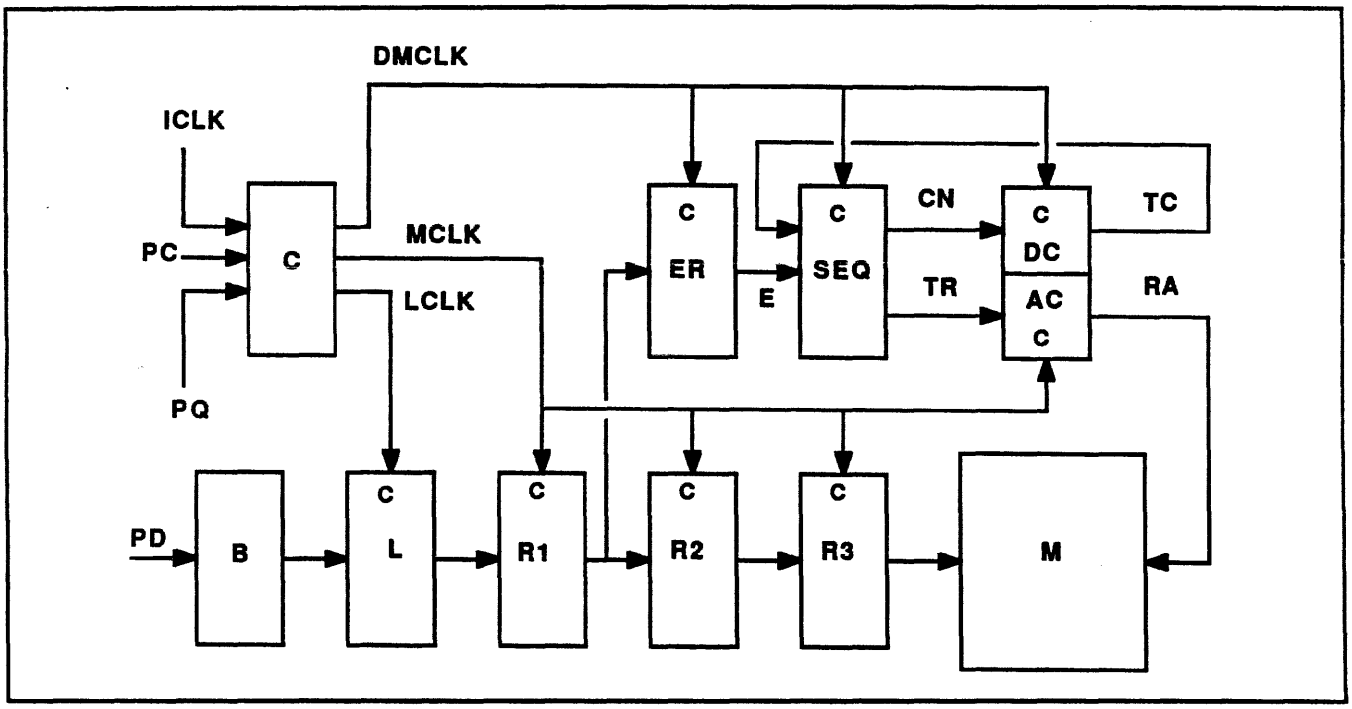

Figure 10-1: Block Diagram

Legend					
a	address input	C	clock select	ICLK	internal clock
c	clock input	L	local latch	LCLK	local clock
d	data input	M	collection memory	MCLK	master clock
E	event output	R1	1st stage register	DMCLK	delayed master
RA	memory address	R2	2nd stage register clock	PC	probe clock
TC	terminal count	R3	3rd stage register	PQ	clock qualifier
TR,CN	count enable	ER	event recognizer	PD	Probe data
B	buffer				

10.2.1 Pipeline Registers

Refer to sheet 1 of diagram **166-036001.**

The data from the system under test arrives from the probes via the daughter board, to the motherboard, and on to the octal buffers on the memory board (74LS244) U39 and U54. The data then is latched in two octal D type flip-flops (74F374) U14, U27 by a latch clock. The latch clock on each memory board can be different. The latch clocks come from the Control board and are defined by the user on the menu. The data is then latched in the first pipeline (74F374) U13, U28 by the master clock, and then goes to the word recognizer RAMs and the pipelines via local data bus LD0-19.

The purpose of the pipeline is as follows. There is a feature in this analyzer that allows the user to be selective about the data collected by storing only the data that match the user's defined pattern (s). These data stores can be discontinuous. In order to do this, the user has to program those desired patterns and ranges in the menu EVENT/RNG fields. When the analyzer is collecting, before actually storing the data, it compares the data against the programmed patterns. If the data doesn't match the programmed pattern, it will be discarded. To discard data, the trace signal (one of the sequencer outputs) has to go false, causing the main acquisition memory address counter to stop incrementing. When new data arrives at the memory, it will be recorded over old unwanted data at that same address. For this trace signal to be true, the data has to be recognized in the word recognizer. This output of the word recognizer drives the sequencer and causes the trace. This takes three clocks to occur. Therefore, the data arriving at the memory has to be delayed for three clocks. This is done by the pipeline registers U5, U6, U19, U20, U31, and U33.

10.2.2 Word Recognizer RAM

The Word Recognizer RAM is comprised of U8, U9, U22, and U23 on sheet 2. They compare incoming data on LD0-19 with the patterns stored from the menu, and can recognize four events and a range simultaneously. Its outputs are latched by U10 and U37.

With three memory boards, the output of the word recognizer on each board must be true before the word recognizer output to the sequencer is considered valid. Therefore, the word recognizer outputs are ANDed. This is done by converting the outputs to an open collector type output stage (74S09) by U51 and wire ANDing them on the common bus. The output of the fifth word recognizer (WR5) from U10, has additional circuitry (U25, U26) to be functional as either an EVENT or as a RANGE. Other outputs of the word recognizer circuits are **A (ECL)** which is the ECL level of WR1 and **T (ECL)** which is the ECL level of WR2. These two signals are used by the plug-in board Counter Timer/Signature Analyzer for the start and the stop conditions. The outputs are picked up from the open collector end of the word recognizers so that they are only valid when word recognizer output of all three boards are true. The last output of the word recognizer is the ARM which is the same as WR1, but it only represents patterns matching the State Memory board 1. ARM from U55 goes to the rear panel for linking to other devices. This operation is described further in the following subsections.

10.2.3 Processor Interface

In order to load the State Memory board word recognizers with the user's defined pattern, the Program will take the information from the menu and preset the registers and the RAMs in the analyzer. This action is transparent to the users and is performed once the COLLECT key is pressed. The logic for interfacing this board to the processor are buffer U17, and registers (U7, U21, U34, U35,U36) on sheet 2. When the analyzer is in the loading process, the outputs of the pipeline registers (U13, U24, U28 page 1) are put in the tri-state mode. Conversely, when the analyzer is in the collect mode the output of the interface registers (U34, U7, U21 U35, U36) are put in the tri-state mode.

To display the data from the high speed memories on the screen, the processor reads the data through U18 and U44 on page 3. It should be noted that addresses to the high speed memories come from the control board through the S2 bus via buffers U49 and U50. These address lines are driven by a high speed counter on the State Control board while the analyzer is in the collect mode, and they are driven by the processor when data is being displayed or saved.

U30 on sheet 2, U42 and U43 on sheet 3 are address decoders that select the appropriate chips for a CPU command.

10.2.4 Input/Output Buffers

The Input/Output Buffers are comprised of the following buffers: Probe Input Buffer, Probe Output Buffer, Setup Data Buffer, Collection Address Buffer, and Collection Output Buffer.

The Probe Input Buffer consists of U39 and U54, both 74S244. The 16-bits of data at the probe pod output are applied to U39 and U54 via the custom 60 wire S2 bus. See Section C7 on sheet 1.

A qualifier bit, Q is sent from each probe via the S2 bus to the input of U53. The trigger output, FT, of the timing analyzer sequencer is applied via S2 to another input of U53. The external input EXT at the BNC connector on the rear panel provides still another input via S2. The outputs of U53 and the 16 data bits are sent to address inputs on Word-Recognizer RAM by way of an internal bus LD0-LD19. This is already after the first level of pipeline latches. See Section C4.

The signal **LCLK**, which latches the probe data, is the intermediate clock selected from the Setup Menu as the clock for Memory Card 1, 2, 3, or a combination thereof. LCLK is received from the State Control Board via S2.

The Probe Output Buffer (sheet 2) consists of U38 and U52, both 74LS374 octal D flip-flops. This buffer is used to send data from the processor to optional or custom probes designed to accommodate data output.

The eight inputs of U38 (DB0-DB7) are connected in parallel with those of U52 and are buffered by U17 (74LS244) from the Processor Data Bus. The outputs of U38 and U52 are sent via S2 to the 16 probe data lines. The 8-bit input is demultiplexed to the 16-bit output using two strobe signals, **PROBEDREN 0-7** and **PROBEDREN 8-15**. The three state outputs are enabled by **PROBDREN** (Probe Data Remote Enable) that is generated at the State Control board.

The Setup Data Buffer consists of U7, U21, and U34-36. They are used to load setup data into the word-recognizer RAMs U8, U9, U22 and U23. The 20 address outputs (LD0-19) and 16 data inputs (D1-D16) are sent in cascade via the CPU bus. The 8 bus lines are demultiplexed to 36 output lines using the write signals W0-W4. The buffer three-state outputs are enabled by **STBUFEN-** (Setup Buffer Enable -) from decoder U42.

The Collection Address Buffer (sheet 3) consists of U49 and U50, both 74LS244s. The 10 input signals (RA0-RA9) are received via the S2 bus from the State Control board. They are sent to the 10 address inputs of the Data Collection RAM (U45-U48). If the current clock period is qualified for data collection, the collection address is held by the Collection Address Buffer for the duration of the WE- pulse. Signal **WE-** is the write pulse for the Data Collection RAM.

The Collection Output Buffer consists of U44, a 74LS244 octal buffer; and U18, a 74F245 bidirectional buffer. The processor uses the Collection Output Buffer to read collected data from the Data Collection RAM and AUX RAM. The eight outputs of each RAM provide the 16 data inputs. The four output lines are loaded onto the 8-bit Processor Data Bus. Signals 0-7EN- and 8-15EN- and AUX WE;T/R- received from the Address Decoder U42 (6308) enable the buffer outputs to the bus.

10.2.5 Address Decoder

The Address Decoder consists of the following components: U30, a 74LS138 3-to-8 decoder (sheet 2); U43, one-half of a 74LS138 3-to-8 decoder; and U42, a 63081 256-word x 8-bit PROM (sheet 3). The processor has access to the State Memory board via the common S1 Address and Data bus. U43 decodes the upper three bits of the address, enabling the PROM to generate eight control signals. The specific functions of the signals depend on the eight input controls. These controls and their functions are as follows:

a. **A12** and **A11** determine which of the three memory boards (A, B, or C) is being accessed by the processor.

b. **A10** determines whether the upper byte (8-15) or lower byte (0-7) is being accessed by the processor.

c. **CSEL** and **BSEL** identify by ground or voltage in which of the three slots (A, B or C) the memory board is inserted. If the A memory is accessed by the processor, no control signals will be generated in the B and C memory slots. The A memory BSEL, CSEL levels combined with the A Memory Address on A15, A14, A13, A12, and A11 control these signals.

d. **S1** distinguishes between processor read and write commands.

e. **IO/Mem-** distinguishes between I/O and Memory addresses.

f. **Main/Aux-** determines whether the collection (main) memory or the Aux memory is being accessed. They both have identical addresses. The Main/Aux signal is received from a State Control Board I/O bit.

The control signals that are generated by the Address Decoder are as follows:

a. **8-15EN-** (8-15 Enable) enables the upper data byte (main memory only) onto the Processor Data Bus via buffer U44.

b. **0-7EN-** (0-7 Enable) enables the lower main memory byte or the Aux Memory byte onto the Processor Data Bus via bidirectional buffer U18.

The lower byte can be a read or write.

c. **AUX OE-** enables the Aux Memory for a read operation.

d. **RDALLMEM-** (Read All Memory) enables all main memories on all Memory boards for a read. The proper Memory bank is selected by the 8-15 and 0-7 enables.

e. **AUX CS-** selects the Aux Memory for read or write operation.

f. **AUX WE;T/R-** selects the Aux Memory for a write operation. Also places the U18 processor interface buffer in the write (receive) direction.

g. **STBUFEN-** (Setup Data Buffer Enable) enables either the Setup Data Buffer (during setup), or data input latches U24, U13, U28 (during collection).

10.2.6 Data Collection RAM

The Data Collection RAM (sheet 3) consists of U45, U46, U47, and U48, all 2149H 1K-word x 4-bit static RAMs.

The 10 outputs of the Collection Address Buffer (U49 and U50) are applied to the 10 address lines of the four 1K x 4 RAMs. The 16 output lines of the Collection Input Buffer are applied to the four sets of four data-in lines of the RAMs. U46 is at the high order end.

In the collection or write mode, the **WE-** (write enable) sent to the RAMs is held low. The (RD ALL MEM + WE) signal (sheet 1 Section B6) is sent in parallel to the chip select inputs of the RAMs. Therefore, in the write mode, the RAMs act as a single 1024-word x 16-bit RAM. 16-bit data words, are written to RAM by the WE- write pulses. The Collection Address Counter on the State Control board provides sequential addresses via the Collection Address Buffer.

In the read mode, WE- is high (no write enable). The RDALLMEM signal received from address decoder U42 is applied to the RAM. The data is then transferred to the Processor bus via buffer U18 or U44, depending on the address selection.

10.2.7 Auxiliary RAM

There is also an Auxiliary Memory on each memory board so that the data can be saved for reference or for later transport to the floppy. When user requests a data save, the processor reads the the data from the high speed RAM memories and stores it in the Auxiliary Memory.

The Auxiliary RAM consists of (U32) an HM6116 2048 x 8-bit RAM. The AUX RAM is used to save a data collection from the Main Memory (1024 x 16-bit RAM). The data is saved by reading it out of the main memory (U47, U48, U45, U46) and storing each byte in the AUX memory. The address for a given byte is identical for the main memory or the AUX memory. The processor makes the Main/Aux selection by setting an I/O bit on the State Control board.

The data is read from the AUX RAM in the following manner: The 11 address lines (A0-A10) of the RAM U32 are received from the processor address bus. Buffer U18 and U44 are enabled in the transmit direction when a byte is read out.

10.3 BOARDS A, B and C

The differences in function between boards plugged into the A slot, B slot and C slot are discussed in the following paragraphs.

10.3.1 Qualifier Bits

There is a qualifier line received from each of the three Model 51A Probe pods. That coming from Pod A connects (via the S2 bus) to the board in the slot for Board A, Pod B to Board B, and Pod C to Board C. The EXT qualifier from the rear panel and FT from the Timing Analyzer Sequencer TRIGger output are applied to Boards A, B and C. These three signals are sent to each board at the inputs to U53 in Section D6 of page 1.

On the Setup Menu, the qualifier bits are displayed as follows:

-XXX XX

The formatting is shown on the menu legend line as follows:

QUALIFIERS: -XYZ EL

With additional identification of signal names, the menu format is as follows:

QUALIFIERS: -AX, BY, CZ, EXTernal, LINK input

The signals at the Probe Input Buffer U53-are as shown below:

AX,EXT,LINK (for Board A) BY,EXT,LINK (for Board B) CZ,EXT,LINK (for Board C)

10.3.2 Signals BSEL and CSEL

The Control Program can read from only one State Memory board at a time. It must, therefore, write setup data into the Word-Recognizer RAM one board at a time. This ability is provided by signal BSEL and CSEL. This is sent via connector pins S2-15 and S2-2 to Address Decoder U42 pin 5 and 4, with a pull-up resistor RP1. The B and C boards are differentiated by altering the addresses A10-A12. The Address Decoder responds to Board A addresses with one set of signals, and to Board C addresses with others.

10.3.3 Local Clock

Signal LCLK (local clock) on each board originates at the State Control Board. LCLK on Boards A, B, and C are driven by ALCLK, BLCLK, and CLCLK, respectively, from the Control Board.

10.4 SIGNAL LIST

The signal list is on page 10-9.

10.5 PIN ASSIGNMENTS

The Model 800 D State Memory board S2 pin assignments list is on page 10-10.

25 MHz STATE MEMORY LIST

0-7 EN-	Enables the processor to read the low byte of the memory.
8-15 EN-	Enables the processor to read the high byte of the memory.
A (ECL)	E1 output translated to ECL levels for use by counter/timer.
A0-A10	CPU Board based Processor address bus.
ARM1	Output of the word recognizer (E1) to the back panel BNC output.
AUX CS-	Chip select for aux memory.
DB0-DB7	CPU Board based Processor data bus.
EXT	External link input from the back panel.
FT	Link input to the state analyzer from TCB or back panel.
I/O 0-15	Input to high speed memory from output of last pipeline; also the output from collection memory to processor bus when reading data.
LCLK	One of the three local (intermediate) clock from the control board.
LD0-19	While running this bus is data from the first pipeline; while being loaded it is the output of latches that interface to processor.
MCLK1	Buffered master clock.
MCLK2	Buffered master clock.
PD0-PD15	Probe output to memory.
Q	Qualifier bit. Comes from Model 51A Probe.
RA0-RA9	Address bus from SCB to SMB providing memory address for collection and display.
RD ALL RAM-	Low when reading memories. When active causes pipeline output to tri-state.
ST BUFEN	Disables output of first pipeline when processor loads board.
T (ECL)	E1 output translated to ECL levels for use by counter/timer.
W1-W4	Write signals decoded by different addresses to program word recognizer RAMs through latches.
WE-	Write enable; comes from SCB and should be adjusted to 25 ns on the SCB.
WR1-WR4	Output of word recognizers E1 to E4; goes to S2 bus; wire AND'ed with same outputs from other memory boards in the system.

Model 800 D State Memory Board S2 Pin Assignment

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	31	GND
2	CSEL	32	RA9
3	WE-	33	
4	LCLK	34	GND
5		35	GND
6	WR5	36	GND
7	MCLK	37	
8	MAIN/AUX-	38	GND
9	A(ECL)	39	RA7
10	T(ECL)	40	RA6
11	FT	41	RA5
12	EXT	42	RA4
13	RA8	43	RA3
14	PROBDREN-	44	RA2
15	BSEL	45	RA1
16		46	RA0
17		47	WR4
18		48	WR3
19		49	WR2
20	ARM	50	WR1
21		51	PD7
22	DQ	52	PD6
23	PD13	53	PD4
24	PD14	54	PD1
25	PD15	55	PD2
26	PD12	56	PD0
27	PD11	57	PD5
28	PD10	58	PD8
29	PD3	59	PD9
30	GND	60	GND

SECTION 11: MODEL 800 A & B TIMING CONTROL BOARD (100 MHz)

11.1 Introduction ——— 11-1

11.2 Description ——— 11-1
- 11.2.1 Processor Interface ——— 11-2
- 11.2.2 Clock Generator ——— 11-3
- 11.2.3 Clock Control ——— 11-4
- 11.2.4 Trigger Control ——— 11-7
- 11.2.5 Arm Control ——— 11-8
- 11.2.6 Sequencer ——— 11-8
- 11.2.7 Post Trigger and Delay Counters ——— 11-10

11.1 INTRODUCTION

Hardware registers, counters, and RAMs on the Timing Control board are loaded by the Control Program. The loading is done using information entered at the keyboard with the aid of the TIMING menu. The Timing Control board directs the collection of timing data in the Timing Memories.

11.2 FUNCTIONAL DESCRIPTION

A block diagram of the Timing Control board is shown in Figure 11-1. Also refer to the schematic diagram, board layout and parts list included at the end of this manual. Tables of connector pins versus signals for all mother board connectors are provided in SIGNAL AND INTER-CONNECTION TABLES. An alphabetical list of all interboard signals is also provided. The GLOSSARY section offers explanations for terms that may be unfamiliar.

The functional units of the Timing Control Card are as follows: The Processor Interface, Clock Generator, Clock Control, Trigger Control, Sequencer, Post-trigger Counter and Delay Counters. These units are discussed in detail in the following subsections.

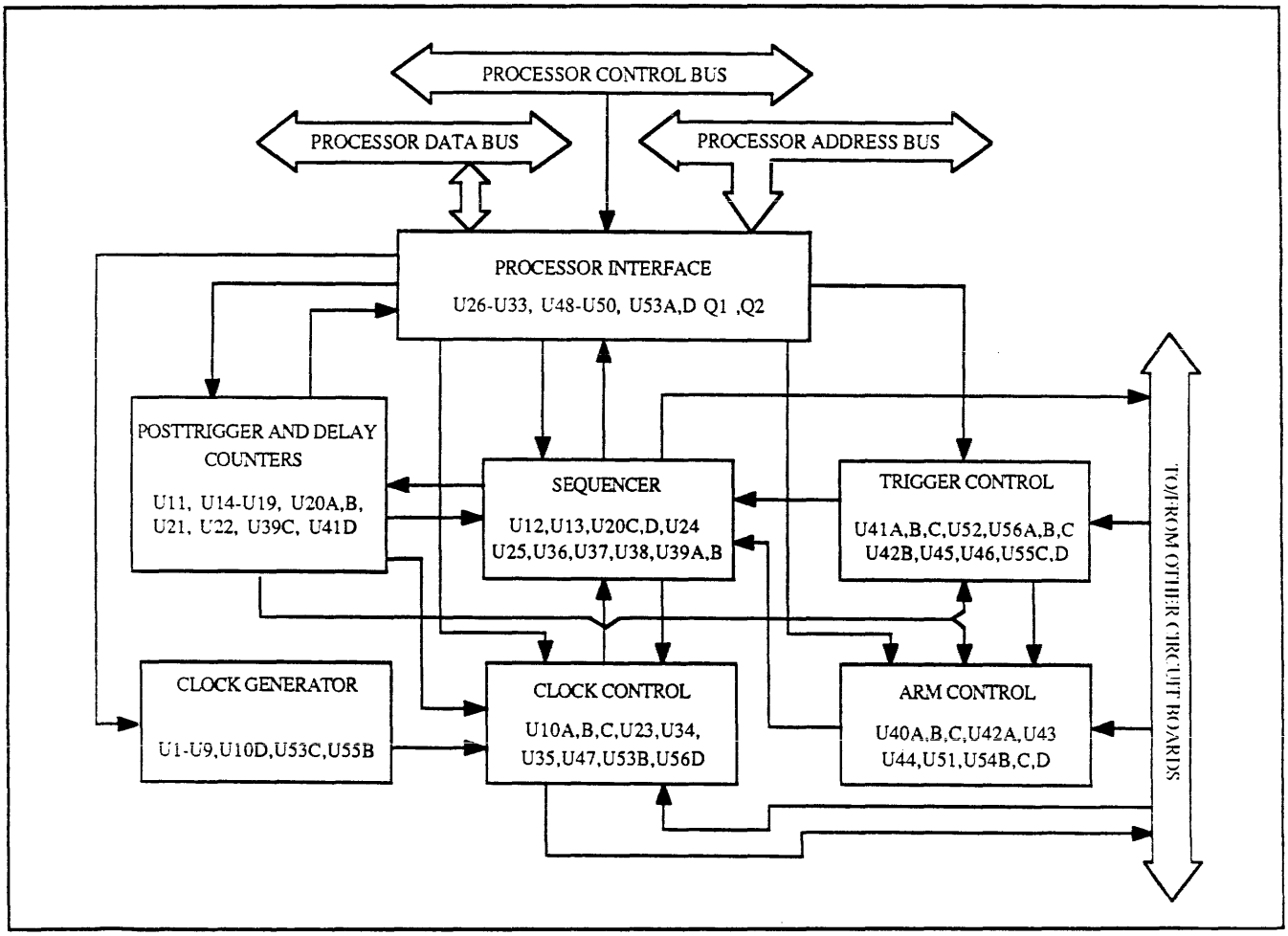

Figure 11-1: Timing Control Board Block Diagram

11.2.1 Processor Interface

Refer to schematic **166-007101,** sheet 4. The Processor Interface is comprised of the following: The Address Decoder, Master Control Register, Control Shift Register, and Status Port. This circuitry allows the processor to load the register, counters and RAMs on the Timing Control board with user-supplied information. This prepares the analyzer to execute the intended application. The processor can interrogate various status and signal lines and send control signals.

The Address Decoder consists of U50, a 74LS138 3-to-8 decoder. This circuit allows the processor to perform the following operations:

a. Clock the Master Control Register (with **MCRCLK**).

b. Address the Status Port with **RDSTAT-.**

c. Send write enable signal **WRRAM-** to the Sequencer RAM.

d. Send reset signal **RESET-** to the Sequencer Latch.

The Master Control Register consists of U49, a 74LS374 octal D flip-flop, and Q1 and Q2, both 2N3905 transistors. U49 latches control signals sent from the Processor Data Bus when clocked by MCRCLK from the Address Decoder. These signals include the following:

a. **SRCLK,** the clock for the Control Shift Register.

b. **SRDATA,** serial data for the Control Shift Register.

c. **SWCLKINH,** a clock-inhibit signal that allows the Control Program to stop all clocks from Clock Control when appropriate.

The remaining signals sent from the Master Control Register are high-speed control signals. These high-speed signals are too fast for the Control Shift Register to handle and are sent to the Clock Generator. The shift register data line, U49-5, doubles as a clock-select signal line when the register is not being loaded. Transistors Q1, Q2, shift signal levels from TTL to CMOS on the two signals that feed the Control Shift Register.

The Control Shift Register consists of eight CMOS 4015 dual 4-bit static shift registers, U26 through U33. These registers supply 63 software-generated control signals to other circuits on the Timing Control board. The registers are loaded in series through the SRDATA line from the Master Control Register. The 63 parallel outputs are supplied at ECL-compatible levels. This method saves considerable circuit board space. Otherwise, space would have been required for 62 parallel input signals and 62 level-shifting transistor circuits.

The Status Port consists of U48, a 74LS373 octal D latch, and U53A,D, sections of a quad ECL-to-TTL translator. Latch U48 acts as an input port that allows the processor to read the status of certain signals. U53A and D translate the levels of two ECL signals feeding the TTL latch.

11.2.2 Clock Generator

The Clock Generator (sheet 6) is comprised of the following: The Clock Oscillator, First Stage Divider, First Stage Selector, Second Stage Divider, and Second Stage Selector. This circuitry generates internal clock pulses in discrete clock periods from 20 nS through 10 mS. The 10 nS clock period is obtained by a multiplexing scheme to be described later. These clock periods also provide the means for the Control Program to select the keyboard-specified clock period.

The Clock Oscillator consists of U10D, a section of a 10102 quad NOR gate; Y1, L1,C1, R2, RP1-7, RP11-4; U9, an 10138 biquinary counter; and U53C, a section of a 10125 ECL-to-TTL translator. U10D and the associated components form an oscillator with a 100 MHz output. This 100 MHz signal is fed to both clock inputs of counter U9. U9 produces a 50 MHz signal at pin 15 and a 20 MHz signal at pin 4. The 50 MHz (20 ns) signal is the fastest clock in the complement. This 50 MHz signal is applied directly to Clock Control (sheet 8) as signal INT50 (Internal 50 MHz). The 20 MHz (50 nS) signal is translated to TTL level by U53C and sent to the First Stage Divider. It is also sent directly to the Second Stage Selector for possible selection by the Control Program.

Capacitor C1 is adjusted for reliable lock to the crystal frequency of 50 MHz ±0.1%, measured at pin U9-15. The First Stage Divider consists of U1, a 74LS74 dual D flip-flop; and U8, a 74LS90 biquinary counter. By successively dividing the 50 nS input signal, this circuitry produces four clock signals. The four signals have periods of 100 nS (at U1-5), 200nS (at U1-9), 500 nS (at U8-8), and 1000 nS (at U8-12). These signals are sent to the First Stage Selector.

The First Stage Selector consists of U2, a 74LS151 1-of-8 data selector. This circuit uses two software-generated clock-select signals **CLKSELD** and **CLKSELE**. These two signals are sent from the Processor Interface. They are used to select the pin 6 output from one of the four inputs received from the First Stage Divider. The selected output is sent to the Second Stage Divider for further processing. It is also sent directly to the Second Stage Selector for possible selection by the Control Program.

The Second State Divider consists of four 74LS90 biquinary counters, U4 through U7. Each of these counters is connected to divide-by-10 logic. The four-divider chain provides four output clock signals.

The four signals have periods equal to the input period multiplied by 10 (at U4-12), 100 (at U5-12), 1000 (at U6-12) and 10,000 (at U7-12). For example, with 100 nS selected as the input, the output signals would have periods of 1 uS, 10 uS, 100 uS and 1 mS. The four output signals are sent to the Second Stage Selector. The Second Stage Selector consists of U3, a 74LS151 1-of-8 data selector, and U55B, a section of a 10124 quad TTL-to-ECL translator. A 50 ns clock is received on input pin 14. The output of the First Stage Selector is received on pin 15. The outputs of the Second Stage Divider are received on pins 1,2,3 and 4. The Processor Interface feeds selector U3 inputs (pins 9, 10 and 11) with the clock-select signals CLKSELA, CLKSELB, and CLKSELC.

The Control Program can select either the pseudo clock or any one of 17 internal clocks. This is achieved by manipulating three select signals and the two signals CLKSELD and CLKSELE. The clock periods range from 50 nS through 10 mS in cascading 1-2-5 ratios. The 20 nS selected clock output at pin 6 is sent via U55B to Clock Control as ECL- level signal INT<50 (Internal Less Than 50 MHz).

11.2.3 Clock Control

Clock Control (sheet 8) is made up of Qualifier Control, the Final Clock Selector, and A/B Multiplexer (Motherboard). This circuitry and the Control Program implement the clock selection. The following selections may be entered via the keyboard:

a. The choice of internal or external clock.

b. If internal, the choice of a 50 MHz or <50 MHz clock;. the specified value of the <50 MHz clock having been pre-selected in the Clock Generator.

c. If external, the choice of the positive or negative-going edge.

d. If external, the choice of 0, 1 or X for clock-qualifier polarity.

Internal to the analyzer, data is always clocked with a positive-going clock edge. Therefore, any keyboard entered negative-going edge must be converted to a positive-going edge for the working clock used within the analyzer. This conversion, if required, is performed by Clock Control. Also, Clock Control shuts off all analyzer working clocks at post-trigger terminal count. This is accomplished by using the clock inhibit signals from the Post-trigger Counter.

Qualifier Control consists of U10A,B,C, sections of a 10102 quad NOR gate and U47, a 10130 dual latch. Section C of U10 has an OR output, and sections A and B are used as negative-input gates. The clock qualifier signal, **QCLK+** is received from the A-channel Model 80 Probe. It is connected to one input of gate U10A. The inverted clock qualifier signal, **QCLK-** is received from the A-channel Model 80 Probe. It is connected to one input of gate U10B. The clock qualifier from the B-channel Model 80 Probe is not used. Gates U10A and U10B are enabled by the software-generated control signals **SWQCLK0-** (Software Clock Qualifier 0 -) and **SWQCLK1-**, respectively.

The keyboard-entered selections of 0, 1 or X for clock qualifier polarity determines how these two signals are used. The selections are implemented as described below:

a. If the choice was 0, the Control Program brings SWQCLK0- low. A low level of QCLK+ will produce a high (true) qualifier signal, QUAL, at U10C-14.

b. If the choice was 1, the Control Program brings SWQCLK1- low. A low level of QCLK- will produce a high QUAL signal at U10C-14.

c. If the choice was X, the Control Program brings both SWQCLK0- and SWQCLK1- low. Signal QCLK+ will produce a high QUAL at either high or low level.

Signal QUAL is sent to the D inputs of latches U47A and U47B. The common clock input (pin 9) is left unconnected so that it is pulled low internally. This allows the latches to be clocked separately. The two polarities of the external clock signal, CLK+ and CLK- are sent from the Model 80 Probe. CLK+ is sent to pin 6 and CLK- to pin 11. The latches are transparent while these clock inputs are low, and latch on the positive-going clock transition. The Q- output of U47A, is clocked by the leading edge of CLK+. This Q- output is used to enable gate U35A. This is the control gate for the working clock that represents an external positive-going clock edge. The Q- output of U47B is clocked by the trailing edge of CLK-. This Q- output is used to enable gate U35B. This is the control gate for the working clock that represents the external negative-going clock edge.

If signal QUAL is high during the positive-going clock edge, a low level is sent from the Q- output of the set latch(s) to the corresponding U35 gate. The level is held low for the duration of the clock period. These enabling levels establish that the corresponding clock edge meets the qualifier conditions and may be further selected by the Final Clock Selector.

The Final Clock Selector consists of U34 and U35, both 10211 dual 3-input, 3-output NOR gates. They are used as negative-input AND gates. By means of enabling signals, the Control Program uses these gates to select the data clock for the analyzer in accordance with keyboard entries. The following choices are available:

a. The choice of external or internal clock. The external clock is handled by gates U35A (for CLK-) and U35B (for CLK+). The internal clock is handled by gates U34A (for INT50) and U34B (for INT<50).

b. The choice of the positive-going or negative-going edge if the clock is external. This choice is implemented by signals **SWPE-** (Software Positive Edge -) and **SWNE-** at gates U35A and U35B, respectively.

c. The choice of a 50 MHz or <50 Mhz clock frequency if the clock is internal. The specified value of the <50 MHz clock has been pre-selected in the Clock Generator. This choice is implemented by software generated signals **SW50-** (Software 50 MHz -) and **SW<50-** at gates U34A and U34B, respectively.

Note that the analyzer always uses the positive-going edge of the working clock. A negative-going edge entered from the keyboard must be converted to an equivalent positive-going edge. This conversion is made in gate U35B. These 10211 AND gates require negative inputs. Gate U35B is enabled by SWNE- and fed by CLK+, which has a negative-going trailing edge. This produces a working clock with a positive-going trailing edge. Similarly, the U35A gate is enabled by SWPE- and fed by CLK- which has a negative-going leading edge. This produces a working clock with the desired positive-going leading edge.

Gates U34 and U35 implement clock shutoff at the end of post-trigger data collection. This is done using clock-inhibit signals **CLKINHA+**, **CLKINHB+**, and **CLKINHC+** received from the Post-trigger Counter. Signals CLKINHA+ at U35A and CLKINHB+ at U35B are wired ORed with respective clock qualifier signals. Signal CLKINHC+ is applied to both U34A and U34B. At the time of post-trigger terminal count, all three clock inhibit signals go high simultaneously. Thus the working clock is shut off no matter which of the four gates is active.

A wired OR consisting of one output from each of the four gates in the Final Clock Selector produces the final working clock. This signal is fed to the Clock Delay circuit. Within the logic of the Control Program, the four selecting signals are mutually exclusive. Therefore, only one of the four gates is enabled at any given time. If either SW50- or SW<50- is low, both SWPE- and SWNE- are held high. Or, if either SWPE- or SWNE- is low, both SW50- and SW<50- are held high. An identical clock from a separate wired-OR set of the gate outputs is sent to pin S2-6 as signal CT (Clock, Timing). This signal is one of the two clocks sent to the Timing Memory boards. Signal CLKTTL, to be discussed later, is the other. Signal CT is also the clock for the Waveform Control Board. CT is sent to the Clock Conditioning circuit shown on sheet 5 of the Waveform Control board schematic.

The Clock Delay circuit consists of U23, a delay line; U53B, a section of a 10125 quad ECL-to-TTL translator; and U56D, a section of a 10101 quad OR/NOR gate. The 10101 is used as a buffer/driver. This circuitry produces the following two working clocks:

a. **CLKECL**, an ECL-level clock that is identical to the CT clock except that it is delayed by about 2.5 nS.

b. **CLKTTL**, a TTL-level clock that is identical to the CT clock except that it is delayed by about 15 nS.

CLKECL is used throughout the Timing Control Board. CLKTTL is used by the Timing Memory Boards. CLKTTL is sent to the Clock Generator shown on sheet 1 of the Timing Memory Board schematic.

The A/B Multiplexer circuitry is located on the Motherboard, but is described in this section. Please refer to the Motherboard schematic during the discussion.

The A/B Multiplexer consists of the following:

a. U1-U3, all 10116 ECL triple differential amplifiers (Daughter Board).

b. Section A of U11, a 10125 ECL-to-TTL translator.

c. Sections A and C of U7, a 7406 hex open- collec tor inverter.

d. U9, a multi-tapped 20 nS delay line.

e. Relays U8 and U4 (Daughter Board), and various resistors and diodes.

Differential amplifiers U1-U3, when active, connect the Probe outputs of A Probe in parallel with that of B Probe. These amplifiers are made active when their Vcc Supply voltage is switched on by relay U4. This is caused in response to signal BPBSNS received from the Processor Board. Signal **BPBSNS** is enabled by the Control Program when the 2000-word data collection mode is selected from the keyboard. The enabling signal is bit 5 of port C in U40, the 8155 on the Processor Board..

In the 2000-word mode, amplifiers U1-U3 are active. Note that in this mode, all data is collected from the A Probe. The B Probe should not be connected to the analyzer. An error message will appear on the CRT if the B Probe is connected.

A B-Clock Delay circuit is comprised of Amplifier U10C, the delay line U9, and translator U11. This is identical to the Clock Delay Circuit on the Timing Control board. Using clock **BCT** as input, this B Clock Delay circuit generates clock **BCLKTTL** for the B Memory board. Via Motherboard connections, **CLKTTL** from Timing Control (S2-G43) is sent to the A Memory board as **ACLKTTL** (S2-H43). Also, clock **CT** from Timing Control board (S2-G6) is sent to the A Memory board as **ACT** (S2-H6).

In the 16-bit, 1000-word data collection mode, clock **BCT** (the ECL-level clock) is sent via the contacts of relay U8 to become **BCT**. A relay is used to avoid the propagation delay of a solid state device. BCLKTTL is essentially identical to ACLKTTL. The A Memory and B Memory collect data in unison as 16- bit words. The A Memory receives data from the A Probe and the B Memory from the B Probe.

Signal **100MHz** (S2A-35) causes relay U9 to select an inverted CT clock from U10A as clock BCT. This occurs in the 8-bit 2000-word data collection mode. Clocks BCT and BCLKTTL are 180° out of phase with clocks ACT and ACLKTTL. Together, the A Memory and B Memory receive 2000 interlaced 8-bit words from the A Probe. Because of the 2-phase clock, the collection interval is half the normal clock interval of CT. The 20 nS CT clock, for example, produces a 10 nS collection interval. The Control Program takes this into account when responding to keyboard entry of the clock interval for the 2000-word mode.

11.2.4 Trigger Control

Trigger Control (sheet 3) is comprised of the Trigger Linker and the Trigger Filter. This circuitry allows the Control Program to set up specified trigger linkages with other Model 800 Series analyzers, or external trigger signals. It also implements the keyboard-selected degree of trigger filtering. Trigger filtering provides that the trigger signal be true longer than a specified number of clock periods to be considered valid.

The Trigger Linker consists of the following components: U56A,B,C, sections of a 10101 quad OR/NOR gate, used as buffer-inverters; U55C,D, sections of a 10124 quad TTL-to-ECL translator; and U42B, U45 and U46, all 10117 dual 2-wide OR- NAND gates.

The upper OR gates in U45A,B and U46A are not used. The software-generated enabling levels applied to these OR gates are **SWTT0-**, **SWSTA0-**, and **SWSTB0-**. These signals are always held high so the outputs of the three NAND gates are controlled by the lower OR gates.

U56A,B and C are used to provide both true and inverted signals to the OR-NAND gates U45A,B and U46A. However, as noted above, only the inverted outputs are used. U55C,D convert TTL level signals to ECL level. The ECL signals are sent to gates U46B and U42B and to Sheet 2 for gates in the ARM Linker.

The outputs of the five 2-wide OR-NAND gates are connected in a wired AND. All outputs must be low to produce the active-low trigger signal. This signal is sent to the Trigger Filter. The enabling signal **SWTT1-** is always held low by the Control Program. This insures that the Timing trigger **TT-** will control the output of the U45A.

Signals STA- and STB- are not used in the Model 800 A or B. The Control Program holds signals SWSTA1- and SWSTB1- high. Thus, the outputs of U45B and U46A are held low. These signals then do not interfere with the wired AND of the remaining three OR-NAND gates.

Gates U46B and U42B implement the trigger linkage function. The keyboard input may specify a trigger link to the External signal. This causes the Control Program to bring SWEXT- low so that EXT controls the output of U46B. Otherwise, SWEXT- is held high and EXT has no effect. Similarly, if a trigger link to another analyzer has been specified, SWFST- is brought low. This allows signal FS to effect the output of U46B. Signal FS is produced from LINK by circuitry on the Motherboard. If a link to the Waveform trigger has been specified, SWWT- is brought low. This allows signal WTRIG+ to control the output of U42B.

All enabled linkages must be true simultaneously with TT- to produce a true (low) trigger output. This is caused because of the wired AND connection of the OR-NAND gate outputs. The true (low) trigger output signal is sent to U41A-4 and U41B-6 as TRIG-.

The Trigger Filter consists of U41A,B,C, sections of a 10102 quad NOR gate and U52, a 10137 decade counter. Section A of the 10102 is used as a negative-input AND gate, sections B and C are used as inverters.

U41B inverts TRIG- and feeds it to the U52 decade counter at pin 9. At setup time, the S1 and S2 inputs to the decade counter are both low. This causes the counter to be in the load mode. The Control Program presets the counter to the keyboard-specified filter value. Signals **TF0-TF3** (Trigger Filter 0-3) received from the Processor Interface, are used for this function. This value may range from the default value of 0 to a maximum of 9.

When the trigger signal goes true, S1 goes high, putting the counter in the count down mode. Clocked by CLKECL from Clock Control, the counter counts down from the preset filter value. The counter outputs are connected in wired AND. When the count reaches 0, the pin 5 input to AND gate U41A is brought low. The 0-count low level is inverted by U41C. This signal is sent back to the counter Carry-In input, U52-10, to stop the count. If TRIG- at U41A-4 is still true at 0 count, signal TRIG+ goes true at the output of U41A. TRIG+ is sent to the Sequencer Latch (sheet 5).

11.2.5 Arm Control

Arm Control (sheet 2) is comprised of the Arm Linker and the Arm Filter. This circuitry allows the Control Program to set up keyboard-specified linkages with External, other Model 800 A and B analyzers, or Waveform arm signals. The circuitry also implements the keyboard-selected degree of arm filtering. Arm filtering provides that the arm signal be true for a specified number of clock periods to be considered valid.

The Arm Linker consists of the following components: U54B,C,D sections of a 10101 quad OR/NOR gate, used as buffer-inverters; and U42A, U43 and U44, all 10117 dual 2-wide OR-NAND gates. The operation of this circuitry is analogous in every respect to the operation of the Trigger Linker. Note that ECL-level EXT and FS signals are taken from the U55 translators in the Trigger Linker.

The Arm Filter consists of U40A,B,C, sections of a 10102 quad NOR gate and U51, a 10137 decade counter. Section A of the 10102 is used as a negative-input AND gate, sections B and C are used as inverters. The operation of this circuitry is analogous in every respect to the operation of the Trigger Filter.

11.2.6 Sequencer

The Sequencer (sheet 5) is comprised of Load Control, the Sequencer Latch, the Sequencer RAM, Sequencer Output, and LINK Control. This circuitry allows the Control Program to set up sequences in accordance with the keyboard-entered instructions. The sequence operations pertain to the Delay Counter and Post-trigger Counter in relation to the arm and trigger events.

Load Control consists of U39A,B, sections of a quad TTL-to-ECL translator; and U20C,D, U38, quad AND gates. Circuits U39A and B provide level translation for the RESET- signal. RESET- is sent to the Sequencer Latch. Level translation is also provided for **WRRAM-** (Write RAM) write-enable signal sent to the Sequencer RAM. Both of these signals are received from the Address Decoder in the Processor Interface. Gates U20C,D and U38 are enabled by the **LDSEQ+** (Load Sequencer +) signal. This signal is received from the Control Shift Register in the Processor Interface. When enabled, these gates feed setup address signals, **PTCTR03** (Post-trigger Counter 03) through PTCTR08, to the Sequencer RAM.

The Sequencer Latch consists of U12, a 10186 hex D flip-flop. Inputs to the latch are the ARM+ and TRIG+ signals from Arm Control and Trigger Control, the **DLYTC-** (Delay Terminal Count -) signal from the Delay Counter, and the three state output lines from the Sequencer RAM. The six outputs of the latch are sent to the six address inputs of the Sequencer RAM. Output Q0 also feeds the **ARML+** (Arm Latch +) signal to the Count Mode Selector (sheet 7). The outputs Q3,4 and 5 also feed signals S0 (Sequence 0), S1, and S2 to Sequencer Output.

The Sequencer RAM consists of U13, U25 and U37, all 10148 64-word x 1-bit static RAMs. The RAM data inputs are sent from the Processor Interface with signals **PTCTR00** (Post-trigger Counter 00), PTCTR01 and PTCTR02. The RAM address inputs are wired OR connected. The input signals are sent from either the Sequencer Latch or the Load Control gates.

At setup time, the processor brings the RAM WE- inputs low with signal WRRAM-. The processor resets the Sequencer Latch so that all latch outputs are low. The RAM address inputs are therefore under processor control through the Load Control gates. This allows the Control Program to load the RAMs with sequencing data in accordance with the keyboard-entered delay mode information. Sequencer Latch output signals S0,S1 and S2 are all low. These signals are applied to the decoder, producing output signals, **DLYCNT+/LD-** and **PTCNT+/LD-** that are in the load state (low). This allows the Control Program to preset the Delay Counter and Post-trigger Counter to appropriate values.

At run time, the Control Program brings the Load Control gate outputs low with a low LDSEQ+. This leaves the RAM address inputs under control of the Sequencer Latch. The Sequencer Latch is clocked by CLKECL. Starting with address 00, the Sequencer Latch steps through the control sequence stored in the RAM. The high-order three bits of each successive RAM address are determined by the three RAM outputs from the previous address. The low-order three address bits change when an arm-word or trigger-word match occurs. The bits also change when the delay terminal count is reached. At the proper point in the delay control sequence, S0, S1 and S2 decode to bring DLYCNT+/LD- high. This starts the delay count. Similarly, at the proper time, PTCNT+/LD- is brought high, thus starting the post-trigger count.

Sequencer Output consists of U36, a 10125 quad ECL-to-TTL translator; and U24, a 10162 1-of-8 decoder. Translators U36B,C and D translate the Sequencer Latch outputs S0, S1 and S2 to TTL level and sent to the Status Port in the Processor Interface. Sequencer Latch outputs S0, S1, and S2 also are sent to the three decoder inputs.

The decoder produces two output signals, **DLYCNT+/LD-** (DelayCount + / Load -) and **PTCNT+/LD-** (Post-trigger Count + / Load -). These signals are sent to the Delay Counter and Post-trigger Counter, respectively. Signal PTCNT+/LD- is also sent through translator U36A as signal **FT** (Function of Timing). This signal is sent to the Status Port in the Processor Interface. Signal FT is also sent, via connector pin S2E-11, to LINK Control on the Motherboard for possible linking to another Model 800. Both signals, PTCNT+/LD- and FT, go high when the Model 800 A or B arm and trigger conditions have been met.

The LINK Control circuitry is located on the Motherboard, but will be discussed here (see Motherboard schematic). The circuit consists of sections B, C, and E, sections of U5, a 7406 hex open-collector inverter.

When no link is set in the timing menu, the Model 800 A or B, as timing analyzer, is specified as the master in a linking. Then the LINK Control circuit allows the Control Program to enable signal FT as the outgoing LINK signal via U5C.

When the link is set in the timing menu, the Model 800 A or B, as timing analyzer, is the slave in the linking. Then the LINK Control circuit allows the Control Program to enable an incoming LINK signal as signal **LINK-**. Signal LINK- is sent via U5D to the Arm Linker and Trigger Linker circuits on the Timing Control board, where it is labelled **FS**.

11.2.7 Post-trigger and Delay Counters

Refer to sheet 7 of the schematic diagram. The Post-trigger and Delay Counters are comprised of the Count Mode Selector, the Delay Counter, and the Post-trigger Counter. These circuits allow the Control Program to implement the selected delay function and specified pre-trigger and post-trigger division of collected data.

The Count Mode Selector consists of the following components: U20A,B, sections of a 10104 quad AND gate, and U41D, a section of a 10102 quad NOR gate (used as an inverter). The wired OR outputs of U20A and B produce signal **DLYCLK** (Delay Clock). This signal occurs either at every ARML+ occurrence or at every CLKECL clock. The controlling signal depends on the polarity of software-generated signal DLYARM+/CLK-. This signal is dependent on a keyboard entry. DLYCLK is used to clock the Delay Counter.

The Delay Counter consists of U17, U18, U19 and U21, all 10137 decade counters; and U22A,B,D, sections of a 10103 quad OR gate. The 10103 gates are used as negative-logic AND gates. The counters are operated in the countdown mode. Using the U22 AND gates, the four counters are connected in cascade. A terminal count of 0000 produces a low signal, **DLYTC-** (Delay Terminal Count -). This signal is wired AND at the junction of U21 and U22D outputs. The maximum preset count value is 9999.

The Post-trigger Counter consists of the following components: U14, U15 and U16, all 10137 decade counters, U22C, a section of a 10103 quad OR gate (used as a negative-logic AND gate); U11, a 10211 dual 3-input, 3-output NOR gate; and U39C, a section of a 10124 quad TTL-to-ECL translator. The counters are operated in the countdown mode. Using AND gate U22C, these counters, on a terminal count of 000, will produce low levels at pins 5, 7 of AND gate U11A. The maximum preset count value is 999.

At setup time, the counters are placed in the load mode by a low level on signal PTCNT+/LD-. This signal is sent from the Sequencer to the counter S1 mode-select inputs. This allows the Control Program to load the counters with the post-trigger count. To accomplish this, signals **PTCTR00** (Post-trigger Counter 00) through PTCTR11 are used. The Post-trigger counter signals are received from the Control Shift Register in the Processor Interface. The Control Program derives the post-trigger count from 1000 minus the specified pre-trigger count.

At run time, if the specified arm, delay and trigger conditions are met, the Sequencer brings **PTCNT+/LD-** high. This puts the Post-trigger Counter in the countdown mode. Then, the preset count is decremented by **CLKECL** which is received from Clock Control. A terminal count of 000 produces high outputs sent from AND gate U11A if signal **ENCLKINH-** (Enable Clock Inhibit-) is low. Signal **ENCLKINH-** is received from the Control Shift Register in the Processor Interface. It is normally brought low by the Control Program at run time. The three outputs of U11A are connected in wired-OR with those of U11B. This produces three identical signals, **CLKINHA+** (Clock Inhibit A+), **CLKINHB+**, and **CLKINHC+**. All are produced either by the post-trigger termial count at U11A or by **SWCLKINH-** (Software Clock Inhibit-) at U11B. Signal SWCLKINH- is received from the Master Control Register in the Processor Interface. It is used by the Control Program during setup. When the post-trigger terminal count has been reached, the working clocks are turned off. This is done by the three clock inhibit signals that are sent to Clock Control and turn off **CT**, **CLKECL**, and **CLKTTL**. Three identical clock inhibit signals are needed because two are separately wired-ORed with the two Qualifier Control latch outputs. These are shown on sheet 8.

SECTION 12: MODEL 800 A & B TIMING MEMORY BOARD (100 MHz)

12.1 Introduction ——— 12-1

12.2 Description ——— 12-2
- 12.2.1 Processor Interface ——— 12-2
- 12.2.2 Clock Generator ——— 12-2
- 12.2.3 Timing RAM ——— 12-4
- 12.2.4 Data Comparators ——— 12-9

12-1 INTRODUCTION

There are two identical Timing Memory boards in the Model 800 A and B. These boards store high-speed incoming data in a multiplexed static RAM as directed by the Timing Control board. Also, using logic-gate comparators, they detect matches of incoming data with keyboard-specified arm and trigger words. When specified from the keyboard, they detect and pulse-stretch data glitches for storage and display.

12.2 DESCRIPTION

A block diagram of the Timing Memory board is shown in Figure 12-1. Also refer to the schematic diagram, board layout and parts list included at the end of this manual. Tables of connector pins versus signal names for all motherboard connectors are provided in MOTHERBOARD CONNECTIONS. An alphabetical list of all interboard signals is also provided. The GLOSSARY section offers explanations for terms that may be unfamiliar.

The functional units of the Timing Memory board are the Processor Interface, Clock Generator, Timing RAM, and Data Comparators. These units are discussed in detail in the following subsection.

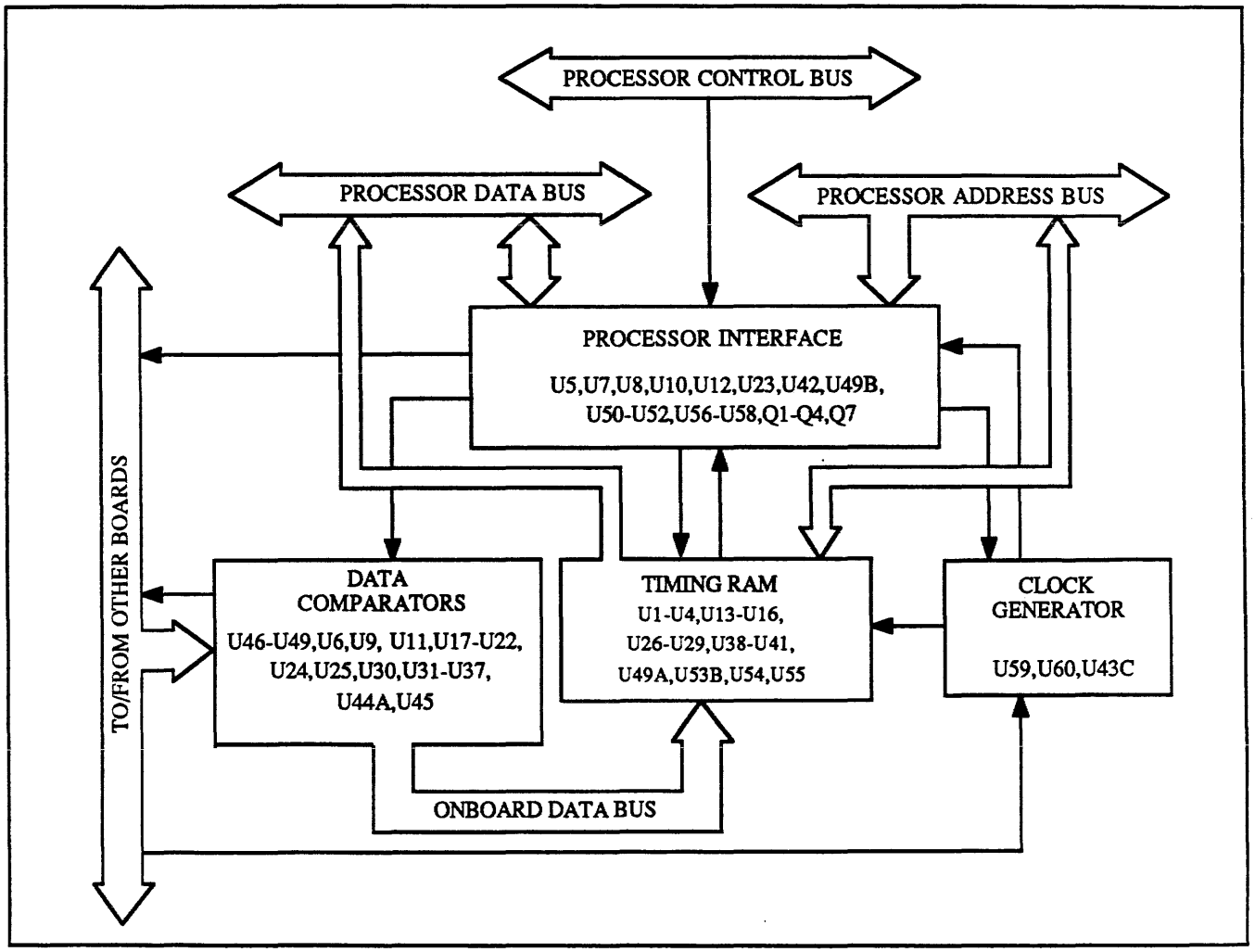

Figure 12-1: Timing Memory Board Block Diagram

12.2.1 Processor Interface

Refer to schematic **166-0065-01**. The Processor Interface is comprised of the following components: Address Decoder, A/B Decoder, Probe Threshold Control, Control Port, Status Port, Last-Word Address Port (sheet 2), and Control Shift Register (partly on sheet 3, partly on sheet 4). This circuitry allows the Control Program to setup certain Probe parameters according to keyboard-entered instructions. It also causes certain control signals to be sent, and to interrogate various status lines as needed.

The Address Decoder (sheet 1) consists of U52, an MMI 6301-1 246 word x 4-bit PROM; U43B, a section of a 74S10 triple 3-input NAND gate (used as an inverter); and U51, a 74LS138 3-to-8 decoder. PROM U52 is enabled by processor control signal **RW-** (Read OR Write). The PROM accepts Address Bus signals A10-A15 and control signals **S1** (Read) and **IO+/M-** (I/O + Memory-). These inputs are decoded to produce the following control signals.

a. **RDLAST-** (Read Last -) enables the Last-Word Address Port, U5 on sheet 2.

b. **RDRAM-** (Read RAM-) places the RAM Address Counter (U54 and U55 on sheet 2) in the load mode. This enables the processor to preset the counter or address the RAM.

c. **EN51-** (Enable U51-) enables the second state address decoder, U51. Decoder U51 is enabled by EN51-.

U51 then accepts Processor Address Bus signals **A0** and **A1** and processor controls signals **IO+/M-** and **RW**. It decodes them to produce the following control signals:

d. **EORAM0** through **EORAM3** (Enable Output, RAM 0 - 3), enable the outputs of RAM sections 0, 1, 2, and 3, respectively.

e. **LDTHRESHA-** (Load Threshold A-) and **LDTHRESHB-** enable the CS- inputs of D/A converters U56, U57 in Threshold Control.

f. **ENSTAT-** (Enable Status-) enables the Status Port, U50.

g. **ENCTRL-** (Enable Control -) enables the Control Port, U42.

The A/B Decoder is located on the Motherboard, but will be discussed in this section (see Motherboard schematic **166-012301**). The circuit consists of sections D, E and F of U7, a 7406 hex open-collector inverter.

This circuit inverts some of the address bits sent to the B Memory board S2 socket. This allows the Control Program to separately address the Timing Memory boards. They must be plugged into the A and B Memory board S2 sockets on the Motherboard.

The Probe Threshold Control consists of the following components: U56 and U57, AM 6080 8-bit D/A converters; and U58, an LM747 dual operational amplifier. U57 is enabled by **LDTHRESHA-**, received from the Address Decoder, and **WR-**, received from the processor. D/A converter U57 converts a digital value to an analog voltage. THe keyboard-entered digital value is sent from the Processor Data Bus by the Control Program. The analog voltage is applied to operational amplifier U58A that produces **THRESHA**. This signal is sent to the Model 80 Probe. **THRESHA** is a threshold reference voltage for the external clock, the qualifier, and data channels 0, 1,2, and 3. Similarly, U56 and U58B supply **THRESHB** to the Model 80 Probe for data channels 4, 5, 6 and 7.

Potentiometer R19 is used to set the reference voltage applied to pin 14 of D/A converters U56 and U57. This voltage, as measured at test point TP1, should be 10.0V, ±0.05V.

The Control Port consists of U42, a 74LS174 hex D flip-flop; Q3, a 2N3905 transistor; and A7, a 2N3904 transistor. When flip-flop U42 is enabled by signal **ENCTRL-**, the following signals are clocked into the flip-flops from the Processor Data Bus:

a. **PRSCLKG-** (Preset Clock Generator) presets the four flip-flops in the Clock Generator.

b. **CLRCLKG-** (Clear Clock Generator) clears the four flip-flops in the Clock Generator.

c. **SRDATA** (Shift Register Data) serial data to be loaded into the Control Shift Register.

d. **CLKSR** (Clock, Shift Register) the clock that loads the Control Shift Register.

e. **HYSTCTRL** (Hysteresis Control), when high, adds hysteresis to the comparators in the Model 80 probe. Transistors Q3 and Q7 supply signal **HYST** as a voltage level, measured with the probe connected. When hysteresis is ON, it is +1.7V, and when hysteresis is OFF, it is -5.1V.

f. **DSELT+/W-** (Data Select Timing+/Waveform-) is sent to the Data Comparator circuits. It is used to select either Timing data from the Model 80 probe or waveform data from the Waveform Control board.

The Status Port consists of U50, a 74LS367 hex bus driver with 3-state outputs; and Q4, a 2N3904 transistor. When the U50 outputs are enabled by **ENSTAT-**, this circuitry allows the processor to read the following signals:

a. **CLKPH0-** through **CLKPH3-** (Clock, Phase 0-3) when read at clock shutoff time, determines which of the four RAM sections contains the last data word collected.

b. **ROLLOVER** indicates that the memory has been filled (at least once), and has started over-writting prior collected data with new data.

c. **ENDSRD** (End Shift Register Data) is the last bit in the Control Shift Register chain. This permits the Control Program to determine the status of **SRDATA** as shifted through the registers. Transistor Q4 converts the level from CMOS to TTL.

The Last-Word Address Port (sheet 2) consists of U5, a 74LS244 octal buffer with 3-state outputs. The inputs at U5 are received from the Address Counter. The outputs are sent to the Processor Data Bus. The outputs are enabled by **RDLAST-**, received from the Address Decoder after clock shutoff. When enabled, this port allows the Control Program to read the contents of the Address Counter. This counter still contains the last memory address that stored collected data. This address and the status of the 4-phase clock provide the orientation point for processing the collected data. For example, counting back from this point by the post-trigger count establishes the location of the stored trigger word.

The Control Shift Register consists of U7, U8, and U23 (sheet 4), and U10 and U12 (sheet 3), all CMOS 4015 dual 4-bit static shift registers; and Q1 and Q2 (sheet 3), both 2N3905 transistors. Q1 and Q2 translate Control Port signals **CLKSR** and **SRDATA** from TTL level to CMOS level. Shift Register sections U7, U8, U10, and U12 transmit sofware-generated control signals to the Arm-Bit and Trigger-Bit Comparators. The comparators detect data matches with keyboard-specified arm and trigger words. Shift Register section U23 transmits the software-generated control signals to the Data Selectors. These select either Timing data or Waveform data for storage in the Timing RAM.

12.2.2 Clock Generator

The Clock Generator (sheet 1) consists of U59 and U60, both 74S74 dual flip-flops; and U43C, a section of a 74S10 triple 3-input NAND gate. This circuitry provides a 4-phase clock to the timing RAM.

The four flip-flops are connected in cascade. All preset inputs are received in parallel by **PRSCLKG-**. All clear inputs are received in parallel by **CLRCLKG-**. The preset and clear signals both are received from the Control Port. The flip-flops are all clocked by **CLKTTL** from the Timing Control board. The 4-phase clock outputs are sent from the Q-side of the flip-flops.

The Clock Generator is started in the preset condition. The D input of the first flip-flop is held low by the output of gate U43C. Feedback around the first flip-flop, U59A, would normally produce a divide-by-two. In this case, the feedback is held-off for three **CLKTTL** clock periods. The holdoff is accomplished by the 3-input NAND gate, U43C. The delay allows the Q-low pulse to ripple down to the third flip-flop, U60A. Refer to Figure 12-2, page 12-5. The result is an asymmetrical divide-by-four operation for each flip-flop. This produces the set of output clock signals shown in the figure. The clock pulse at the Q- output of each successive flip-flop is delayed from the preceding flip-flop by one **CLKTTL** period.

The 4-phase clock is sent to the Timnig RAM section as **CLKPH0-**, **CLKPH1-**, **CLKPH2-**, and **CLKPH3-**. One clock phase is applied to each of the four sections. An additional clock, **CLKPH0+**, is produced at the Q output of U59A and sent to the Address Counter. The application of these clocks will be discussed in the next subsection.

12.2.3 Timing RAM

The Timing RAM (sheet 2) is comprised of the Address Counter, Rollover Detector, and Timing RAM Sections 0, 1, 2, and 3. Each of the four RAM sections stores 256 8-bit words, thus the total storage capacity is 1024 8-bit words. The memory is arranged so that the 45 ns RAMs can store data that is clocked at intervals as short as 20 ns.

The two Timing RAMs (one from each board) are used to store 2000 8-bit words or 1000 16-bit words sent from the Data Comparators. Although the full memory capacity is 2048 words, the post-trigger count is adjusted so that only 2000 or 1000 words are collected. The data received from the Comparators may have been generated by either the Model 80 probe (as timing data) or the Waveform Control board (as waveform data). After collection, data stored in the Timing RAMs may be read by the Control Program for analysis and display.

The Address Counter consists of U54 and U55, both 74LS191 4-bit binary counters; and U44A, a section of a 74S10 triple 3-input NAND gate (used as an inverter). The two counters are wired to count up and are connected in cascade (through U43). This will produce an 8-bit output. The 8-bit output is sent to the input of Address Latch U4 (Timing RAM Section 0) and to the Last Word Address Port, U5.

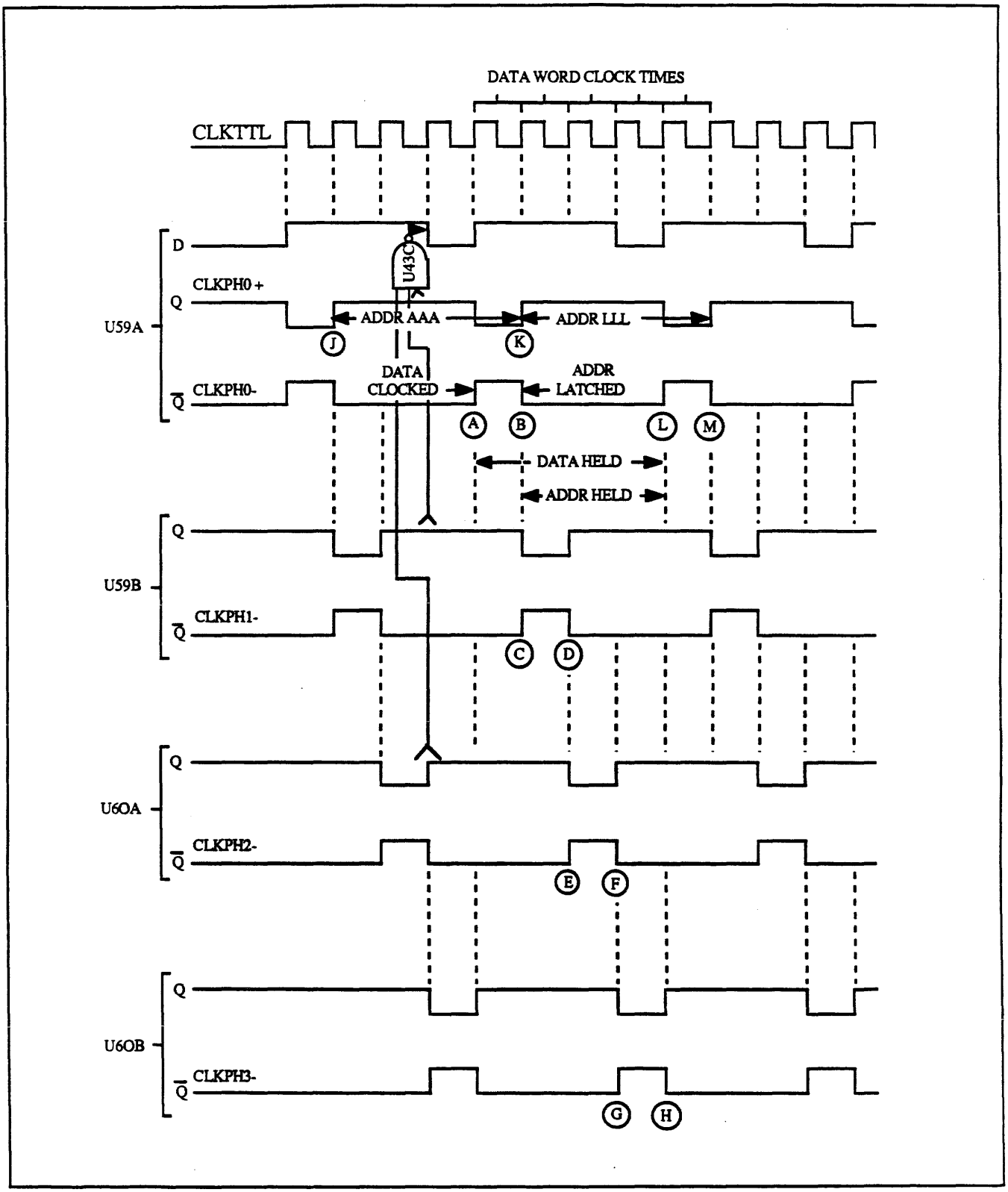

Figure 12-2: Clock Generator Timing Diagram

The counter load-control inputs are controlled by **RDRAM-**, generated by the Address Decoder. When **RDRAM-** is low, the counter outputs follow the inputs. This mode is used by the Control Program to preset the counter to 000 before data collection starts. This mode is also used to address the Timing RAM when reading data after collection stops. The counter is clocked by **CLKPH0+** sent from the Clock Generator. Clocking occurs on the positive-going edge of this signal.

When data collection begins, the Address Counter starts from 000 and advances the address one count with each **CLKPH0+** clock. The maximum count is 256 (000-255), the memory capacity of one section of the Timing RAM. If clocking continues beyound thiis point, the counter overflows and starts over again from 000. Counting stops when the **CLKTTL** input clock to the Clock Generator is stopped by the Timing Control board.

The Rollover Detector consists of U53B, one-half of a 74LS73 dual J-K flip-flop. This circuit detects the first occurrence of overflow of the Address Counter. The J input of the flip-flop is wired high, and the K input is wired low. Once set, the flip-flop will not change state again until reset by a low clear signal at pin 6. The flip-flop is clocked by the MSB and RA7 of the Address Counter. Clocking occurs on the negative-going edge of this signal. As the maximum address count is approached, the MSB goes low again. This transition clocks the flip-flop. The signal used to clear the flip-flop, **PRSCLKG-**, is sent from the Control Port. The same signal is used to preset the Clock Generator. Thus, before the start of data collection, the Rollover Detector is cleared at the same time the Clock Generator is initialized.

The flip-flop outputs ROLLOVER, twhich is sent to the Status Port on sheet 1. There it can be accessed by the Control Program. After data collection has stopped, the Rollover Detector state is used to determine the location of the trigger word in the Timing RAM.

Timing RAM Section 0 consists of the following components: U16 and U29, both Fairchild 93422 256-word x 4-bit static RAMs with 3-state outputs; Address Latch U4, a 74S373 octal D latch; and Data Latch U41, a 74S374 octal D flip-flop. This circuitry stores 256 8-bit words of collected data.

The address inputs of the two RAMs are received in parallel from Address Latch U4. The inputs of the Address Latch are sent from the Address Counter, signals **RA0** (RAM Address bit 0) through **RA7**. The 4-bit data inputs of the two RAMs are connected in cascade to the 8-bit output of Data Latch U41. The inputs of the Data Latch are received via the onboard Timing Data Bus. These input signals are **TDB0** (Timing Data Bus bit 0) through **TDB7**. The 4-bit data outputs are sent in cascade to the 8-bit Processor Data Bus. These signals are **DB0** (Data Bus bit 0) through **DB7**.

The output-enable inputs of the two RAMs are controlled in parallel by signal **EORAMO-** sent from the Address Decoder. The phase-0 clock signal, **CLKPH0-**, is received from the Clock Generator and sent to the following points: two RAM write-enable inputs, U16-U20 and U29-20; the Address Latch enable, U4-11; and the Data Flip-Flop clock input, U41-11.

Timing RAM Section 1 consists of RAMs U15 and U28, Address Latch U3, and Data Latch U40. The IC types are the same for all four RAM sections. The address inputs of the two RAMs are received in parallel from Address Latch U3. The inputs of the Address Latch are received from Address Latch U4 in Section 0. The other operations of this section are similar to those of Section 0. The exceptions are that enable signal **EORAM1-** is sent from the Address Decoder and clock signal **CLKPH1-** is sent from the Clock Generator.

Timing RAM section 2 consists of RAMs U14 and U27, Address Latch U2, and Data Latch U39. The operations of this section are similar to those of Section 1. The differences are as follows: The inputs of Address Latch U2 are received from Address Latch U3 in Section 1; the enable signal is **EORAM2-**, and the clock signal is **CLKPH2-**.

Timing RAM Section 3 consists of RAMs U13 and U26, Address Latch U1, and Data Latch U38. The operations of this section are similar to those of Section 2. The differences are as follows: The inputs of Address Latch U12 are received from Address Latch U2 in Section 2; the enable signal is **EORAM3-**, and the clock signal is **CLKPH3-**.

As described, the address inputs to the RAM sections are configured in an open loop. They are sent as follows: From the Address Counter to the Section 0 Address Latch, from the Section 0 Address Latch to the Section 1 Address Latch, from the Section 1 Address Latch to the Section 2 Address Latch, and from the Section 2 Address Latch to the Section 3 Address Latch. The reason for using this design will become apparent.

A typical data collectin cycle is described below. Refer to Figure 12-2, page 12-5, the Clock Generator Timing Diagram.

Data word AA on the Timing Data Bus is clocked into U41 Section 0 Data Latch by the positive-going edge of **CLKPH0-**. Refer to point A on the timing diagram. This data is held in U41 until the next positive-going clock edge at point L. Address AAA, the current address count, was set in the Address Counter by **CLKPH0+** at point J. This address is latched in the U4 Section 0 Address Latch. The address is latched by the low level at the negative-going transition of **CLKPH0-**. Refer to point B on the diagram. The address is held latched for the duration of the low level.

The Address Counter is advanced one count by the positive-going edge of **CLKPH0+** (point K on the diagram). This point coincides with the address latch point B. However, note that propagation time delays the arrival of the new address at Section 0 until after the current address has been latched. The new address at Section 0 is LLL, the current address is AAA. The write enable inputs of the Section 0 RAMs are also brought low at point B. This write enable pulse is held true until the positive-going transition of **CLKPH0-** at point L. The data and address inputs are both held stable for the duration of the pulse.

The 93422 RAMs are described in the following paragraphs. The minimum write-pulse length, specified as 30 ns, is always exceeded. Even using the minimum **CLKTTL** period of 20 ns, the write-pulse width is 3 x 20 ns = 60 ns. The data is clocked into the Data Flip-Flop one **CLKTTL** period ahead of the write pulse. This provides a data setup time of at least 20 ns, four times the specified 5 ns minimum. The address is latched in the Address Latch on the same clock transition that starts the write pulse. However, the address has been stable for much longer than the required 10 ns. The total time is approximately 70 ns as follows: the time is 50 ns minimum in the Address Counter for the Section 0 RAMs. In addition, it has been stable for 20 ns minimum in the preceding Address Latch for the RAMs in Sections 1, 2 and 3.

At point C the postive-going edge of **CLKPH1-** clocks data word CC into the Section 1 Data Latch U40. Data has changed since point A because the data is being sent to the Data Flip-Flops at the **CLKTTL** rate. The latches are connected in parallel to the onboard Timing Data Bus.

At point D, the AAA address being held in the Section 0 Address Latch is latched into the Section 1 Address Latch by the low level of **CLKPH1-**. Note that although a count increment has been started in the Address Counter, address AAA can still be used by Sections 1, 2, and 3. This is because of the series loop connection of the Address Latches. The write-enable inputs of the Section 1 RAMs are also brought low at point D, thus storing word CC.

Data word AA is now written into the Section 0 RAMs at address AAA. Data word CC is written into the Section 1 RAMs at address AAA. Data is clocked at point E and addresses latched at pin F. This operates so that data word EE is written into the Section 2 RAMs at address AAA. Similarly, data word GG is written into the Section 3 RAMs at address AAA.

Each address stores four consecutive data words, one in each RAM section. Each RAM section stores every fourth data word in consecutive addresses. When the Address Counter has reached maximum count, each RAM section conains 256 data words. This makes a total of 1024 data words interlaced in the four RAM sections.

At the next **CLKPH0+**, the Address Counter overflows and starts over at address 000. Data collection may end at any address count, and on any one of the 4-phase clock pulses.

At the end of data collection (post-trigger terminal count), **CLKTTL** stops. This stops the Clock Generator which, in turn, stops the Address Counter. This leaves all Timing RAM Address Latches and Data Flip-Flops in the same state as at the last memory write. The Control Program reads the Last-Word Address Port to find the address of the last word stored. It also reads, from the Status Port, the state of the four flip-flops in the Clock Generator. This defines which RAM section stored the last word at that last address. The Control Program can then locate the address and RAM section for any desired stored data word.

After the **CLKTTL** has stopped, the Control Program can read data words from the Timing RAM. This is done by bringing the Address Counter load control lines low with signal **RDRAM-** received from the Address Decoder. The Address Counter receives addresses from the Processor Address Bus. In this load mode, the incoming addresses are sent straight through the Section 0 Address Latch, U4. The Control Program also clears the Clock Generator flip-flops with **CLRLKG-** received from the Control Port. This brings all clock outputs to the RAM address latches high. This holds all four Address Latches in the transparent mode.

The sequence of operations is described as follows. The Control Program places an address on the Processor Address Bus. That address is sent by the Address Counter to all four Address Latches in the loop. Note that all four RAM sections are addressed simultaneously. The Control Program can select the RAM section that contains the word to be read. That RAM section is selected by activating the proper RAM output-enable line. This signal is one of **EORAM0-** through **EORAM3-**, and is sent via the Address Decoder.

12.2.4 Data Comparators

There are eight Data Comparators, one for each of the eight parallel incoming data lines. The incoming data may be sent from the Waveform Control board, or from the Model 80 probe. If sent from the Waveform Control board, the data is applied only to the Data Selector and the ECL-to-TTL translator. The Data Selector selects either the Waveform or Timing data. If sent from the Model 80 probe, the data is acted upon by two comparator functions. The first of these detects any glitch in the data. The second detects any match with a corresponding arm or trigger-word bit.

The 800 Series Logic Analyzer operation defines a glitch as follows: A pulse on a data line that exceeds the selected voltage threshold and is shorter than the selected analyzer clock period.

A user definition of a glitch may be as follows: A pulse shorter than the normal data period or target-system clock period. Since the analyzer clock period is usually shorter than the incoming data period, many such user-defined glitches are processed as data. They are, therefore, displayed to the user without requiring the use of the glitch capture mode.

Selection of glitch-capture or sample mode of input data is made on a line-by-line basis by menu-prompted keyboard entries. The Data Comparators allow the Control Program to turn glitch capturing on or off for each incoming data line.

Data Comparator 0, shown on sheet 4, consists of the following components:

a. U48B,C, sections of a 10102 quad NOR gate.

b. U47A, one-half of a 10130 dual latch.

c. U36B, one-half of a 10131 dual master-slave, positive-edge clocked, type D flip-flop.

d. U19, a 10117 dual 2-3-input OR-AND/OR-NOR gate.

e. U31B, one-fourth of a 10158 quad 2-input multiplexer.

f. U30A, one-fourth of a 10125 quad ECL-to-TTL translator.

This circuitry performs the data comparator and data selection functions for data bit 0.

Data Comparators 1 through 7 (sheets 3 and 4) operate identically to Data Comparator 0. The IC numbers and signal term names differ.

The following description Data Comparator 3 can be applied to the other seven Comparators. Refer to Figures 12-3 and 12-4.

Timing data sent from the Model 80 Probe is input to the Comparator in differential form. That is, as two signals of opposite polarity, labelled **D3+** and **D3-**. **D3+** is sent to the D input of Data Latch U37B. The common clock input for the U37 dual latch (C-) is left unconnected and is pulled low internally. The two latches in U37 are therefore controlled independently by their individual CE- inputs. The CE- input of U37B is received with signal **D3G+/S-** (Data Bit 3, Glitch + / Sample -). Signal D3G+/S- is sent from the U23 section of the Control Shift Register (sheet 4).

If the sample mode has been selected for Data Bit 3, the CE- input of latch U37B is held low with D3G+/S-.

When the CE- input is low, the set and reset inputs of U37B are inhibited. This causes the Q output to follow the D input. Thus, in the sample mode, Data Latch U37B has essentially no effect. Timing data is sent straight through to the D input of Data Flip-Flop U32A. U32A is a master-slave, type D flip-flop that is clocked by the positive-going edge of the clock signal. The U32A clock input is received with signal **CT** (Clock, Timing). CT is received, via U44A, from the Clock Control on the Timing Control board.

The CT clock is keyboard-selected as either external or internal. If the clock is internal, the clock period is also keyboard-selected. For timing analysis, the clock is usually selected as internal. The clock period is usually selected to be shorter than the data period by a factor of at least 10. This ensures that resolution will be adequate.

When the glitch-capture mode has been selected for Data Bit 3, the **CE-** input to U37B is held high with signal **D3G+/S-**. The latched mode is defined as when the CE- input is high. In this mode, the D input has no effect and U37B responds only to the set and reset inputs. The outputs of Comparator Gates U49C and U49D are sent to U37B set and reset inputs, respectively. D3- and the U32A Q output are applied to the inputs of gate U49C. The D3+ and the U32A Q- output are applied to the inputs of gate U49D.

Comparator Gate U49C detects positive-going transitions in **D3+** by detecting the negative-going transitions in **D3-**. Comparator Gate U49D detects any negative-going transitions in **DE+**. Any positive-going transition in **DE+** (whether by data or glitch) sets latch U37B. Any negative-going transition in **D3+** resets latch U37B. The U37B's Q output is clocked into flip-flop U32A as in the sample mode.

Note that the ECL devices used in the Comparator circuits are fast enough so that any glitch pulses ≥5 nS will be detected.

Operation of the Arm-Bit and Trigger-Bit Comparator Gates is described as follows.

The upper OR gate of Arm-Bit Comparator Gate U9B receives the Q output of U32A and software-generated signal **AW3B1-**. This is the Arm Word 3-Bit selected as 1 -. The lower OR gate of U9B receives the Q- output of U32A and signal **AW3B0-**. These AW3B signals are software-generated in accordance with keyboard selection. They are generated by U8 of the Control Shift Register in the Processor Interface. The output of the NAND gate in U9B is ANDed with the outputs of the other seven Arm-Bit Comparator Gates. All seven Comparator Gate outputs must be low in order to produce a low **TA-** output signal.

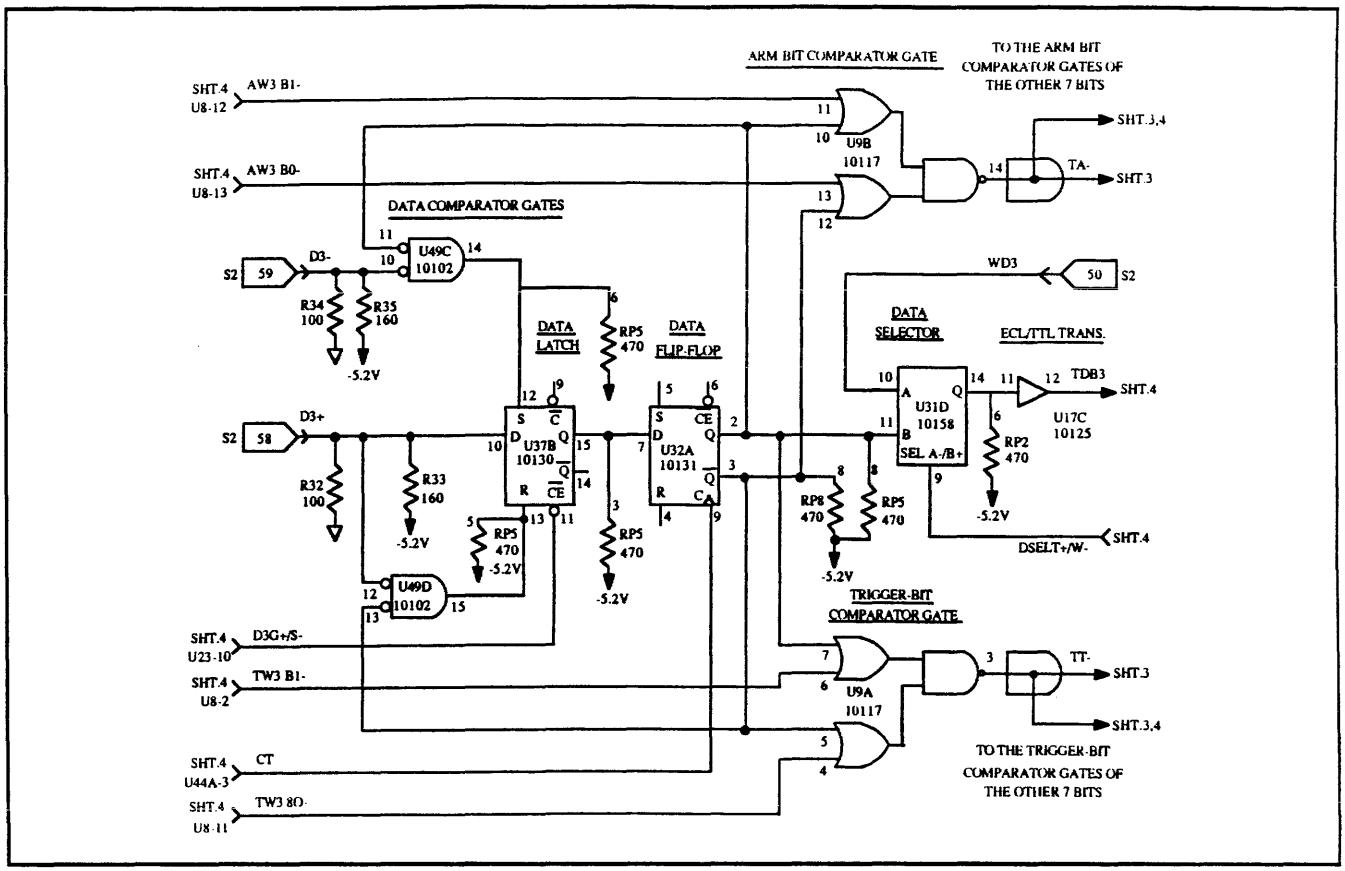

Figure 12-3: Data Comparator Expanded Schematic

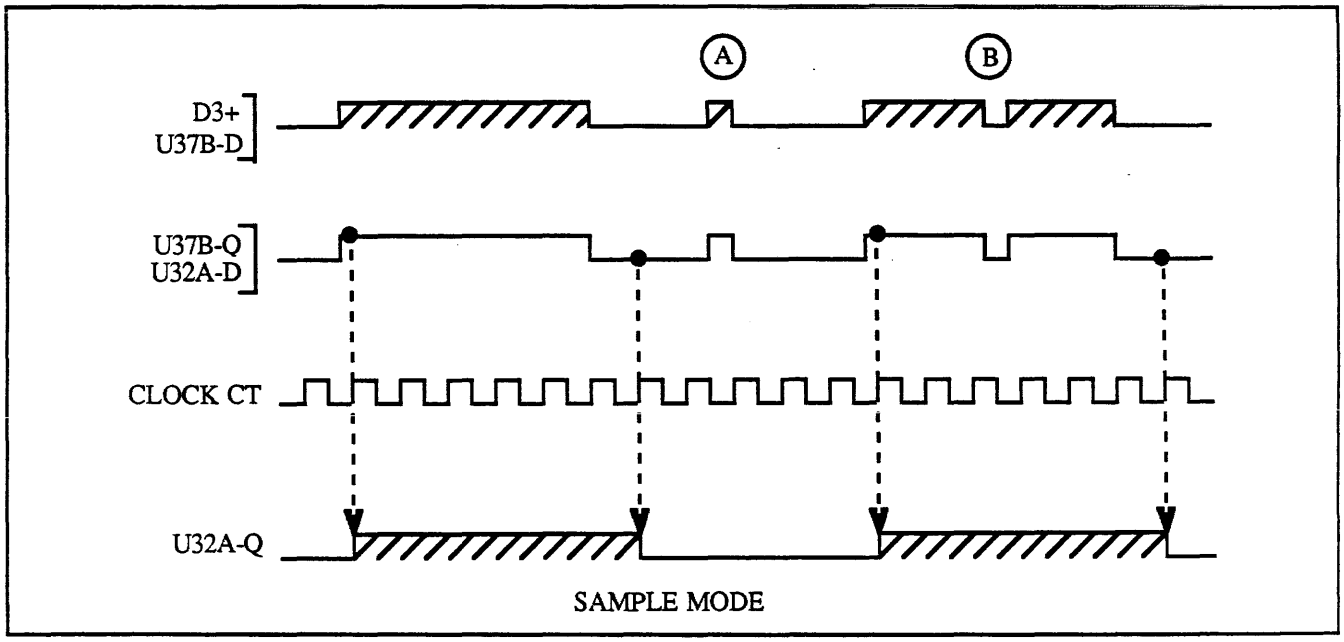

Figure 12-4: Data Comparator Timing Diagram

If Arm-Word Bit 3 was keyboard-specified as a 1 (high), then signal **AW3B1-** is held low (true) and signal **AW3B0-** high. If arm bit 3 was specified as a 0, the Control Program holds **AW3B1-** high and **AW3B0-** low. If arm bit 3 was specified as X (don't care)., the Control Program holds both **AW3B1-** and **AW3B0-** high.

Assume that arm bit 3 was specified as a 1. Signal **AW3B0-** will be high, and the lower OR gate of U9B will always have a high output. This will be true regardless of the data input. This leaves the upper OR gate in Control of the U9B NAND gate output. Signal **AW3B1-** will be low, and as long as U32A-Q (that reflects D+) is low, the output of the upper OR gate will be low and U9B-14 will contribute a low to the wired AND output **TA-**. If the outputs of the other seven Arm-Bit Comparator Gates are also low, **TA-** will be low. This indicates that an arm-word match has occurred.

If arm bit 3 was specified as a 0, U32A-Q- goes high (indicating that D3+ is low). Signal U39B-14 will contribute a low to the wired AND output **TA-**.

If arm bit 3 was specified as an X, the output of both OR gates will always be high (because both **AW3B1-** and **AW3B0-** are high). Signal U9B-14 will constantly contribute a low to **TA-**.

In the glitch-capture mode, the captured glitches will have the same effect as data on the operation of the Arm-Bit Comparator Gate. Spurious bit matches can be prevented by a keyboard-specified arm-word filter setting of 2. This designates that the arm-word match must be present at least two clock periods inorder to be acted upon. However, filter setitngs greater than 2 must be used with caution when the signal period is less than 10 times the clock period.

Note that the filtering action affects only the arm-word and triggering-word match function. It does not affect the storage and display of collected data. Refer to the Trigger Filter circuit shown on the Timing Control schematic, sheet 3.

The Trigger-Bit Comparator Gate operates in exactly the same way as the Arm-Bit Comparator Gate. The output of U9A, **TT-**, is connected in a wired AND with the outputs of the other seven Trigger-Bit Comparator Gates.

Data Selector U31D is used by the Control Program to select either Timing data or Waveform data. The selected data will be stored in the Timing RAM. Bit 3 Timing data is sent from U32A-Q to input B of U31D. Bit 3 Waveform data, **WE3**, is sent from the Waveform board via pin S2-50 to input A of U31D. Signal **DSELT+/W-** is the Data Select Timing+/Waveform- signal.

DSELT+/W- is used to select one input or the other as output to the level translator U17C. The output of U17C, **TDB3** (Timing Data Bus bit 3), is placed on the onboard Timing Data Bus. This signal is applied to the inputs of the Data Latches in the Timing RAM sections.

SECTION 13: MODEL C, D & E TIMING CONTROL BOARD (200 MHz)

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13.3 Timing Control Signal List ——— 13-7

13.1 INTRODUCTION

The Model 800 200 MHz Timing Analyzer consists of one Timing Control board (description follows) and two Timing Memory boards (described in Section 14), each handles 8 channels of data from the two M81A Probes. The analyzer samples incoming data at 200 MHz on all channels using an internal clock, and at 75 MHz using an external clock. Hardware registers and counters on the Timing Control Board (**TCB**) are loaded by the Control Program. The loading is done using information entered at the keyboard with the aid of the TIMING menu. The Timing Control board serving as a peripheral to the microprocessor on the CPU board directs the collection of timing data on the Timing Memory Boards (**TMB**).

13.2 DESCRIPTION

A block diagram of the Timing Control board is shown in Figure 13-1. Also refer to the schematic diagram **166-031301**, board layout and parts list that are included at the end of this manual. Tables of connector pins versus signal names for all motherboard connectors are provided in MOTHERBOARD CONNECTIONS. An alphabetical list of all interboard signals is also provided. The GLOSSARY section offers explanations for terms that may be unfamiliar.

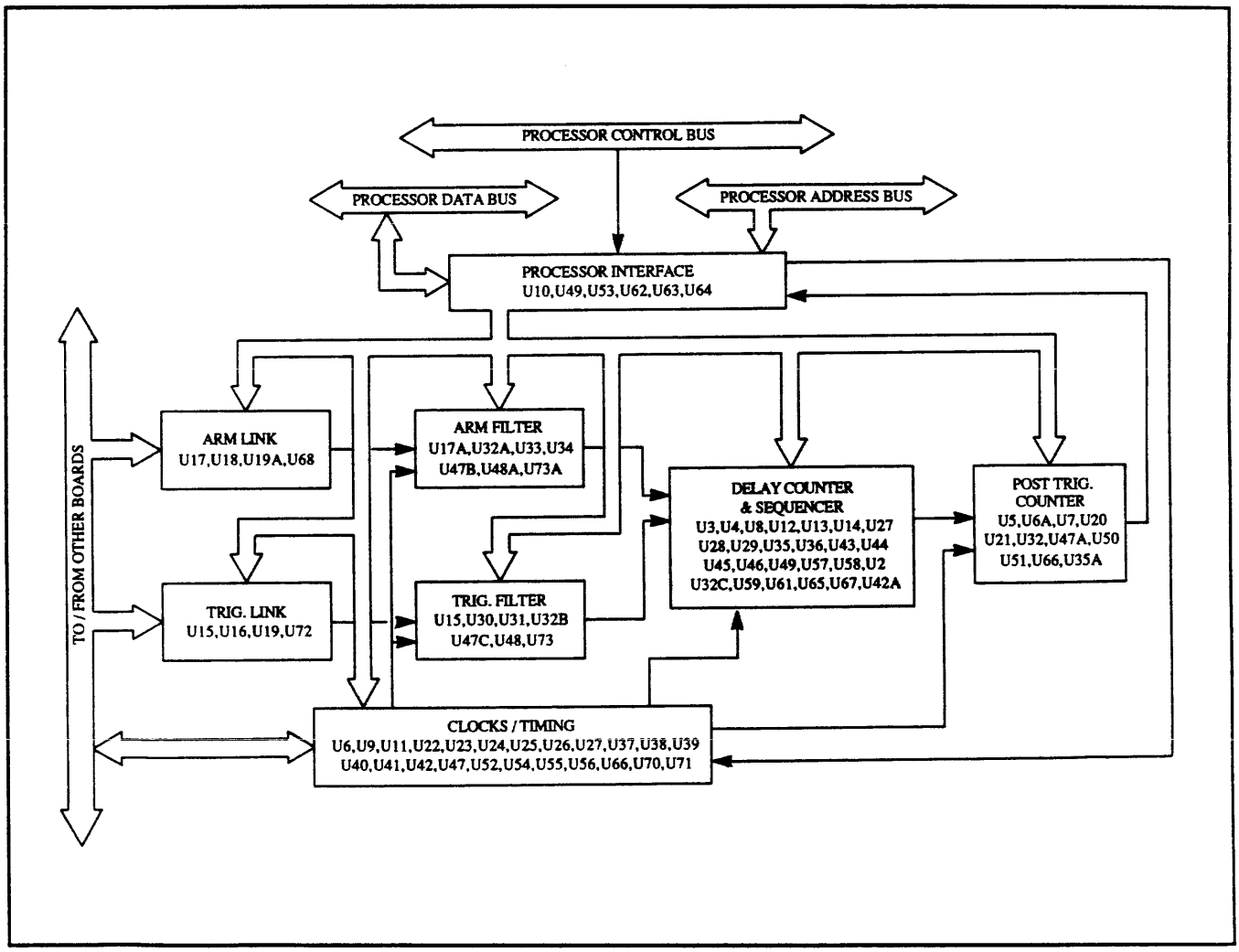

Figure 13-1: Timing Control Board Block Diagram

The functional units of the Timing Control board are as follows: The Processor Interface, ARM/TRIG link, ARM/TRIG filter, Clocks & Timing Control, Delay and Post-trigger Counters & Sequencer. These units are discussed in detail in the following subsections.

All the functions of the control boards are loaded through the shift register using the processor data bus. The ARM/TRIG link circuit is provided to link the ARM or TRIG to any combination of State, Waveform and/or the rear panel external inputs. Use of these linking functions is menu programmable. The output of the link circuit drives the filter circuit and enables the filter counter when ARM (or TRIG) occurs. If the ARM is still active when the filter counter counts to 0, then the filter output will go active. The filter can be programmed from 2 to 15.

The output of both filters drive the Sequencer. The ARM output starts the delay counter. When the filter output for TRIG occurs (if the programmed conditions are met such as trigger before count, or trigger after count) then the output of the sequencer will go high. This signal is called **PTENB**. It is the rear panel **BNC LINK** signal from the timing analyzer, and also activates the post-trigger counter. Post-trigger counter starts counting a preset value (which is 1000 minus the menu value) and then generates the HALT signal. HALT inhibits all clocks and sets a flag to let the processor know that the collection is complete. When reading the memory data, it again uses the processor data bus.

The timing analyzer has two sources for the clock, internal and external. The internal clock runs from 5 nS to 50 mS. A 200 MHz oscillator produces the fast clock and dividers generate the rest from this source. The external clock comes from the probe. Its rate can be from DC to 75 MHz and has a selectable active edge.

13.2.1 Processor Interface

The processor interface controls loading of the Timing Control board with data and addresses received from the processor via the S1 data/address bus.

Refer to sheet 6. This sheet depicts the processor and status interfaces. Two data bits are received from the processor data bus: DB0 serially loads ten shift registers: U12, U13, and U67 (sheet 2)
U19, U72, and U73 (sheet 3)
U66 and U21 (sheet 4)
U10 and U53 (sheet 5)

It is this data that provides most of the information used on the Timing Control board. The other bit, DB1, sets the HALT via latch U49.

The address decoder consists of 1-of-8 decoder U63. It receives the six bits of address information allowing selection of the processor clock, **PROCCLK**, the shift register clock, **SRCLK**, which loads the shift register, and **RESET** to clear any of the controls that have already been set at power-on or from previous operations. A fourth signal, **RdSTAT** is sent from U63 as the enable input to Status Buffer U62. U62 is used as ECL/TTL interface to the bus. U64 is used to translate levels (TTL / CMOS & ECL) from the bus to the rest of the circuits.

The circuitry associated with U62 comprises the status interface. This interface reads the status of the sequencer. For example, status may be read when the sequencer has detected the arm pattern and is ARMed, or when the sequencer is waiting for the counter to finish counting, or when waiting to detect the trigger bit pattern. When the trigger occurs and the collection has been completed, the system is in a halt position and the status interface outputs indicate it has finished.

13.2.2 Clock Generator

The circuitry at the top of sheet 4 is the internal clock and counter/select logic. Clocking is generated by this logic for both internal or external clocks. Internal clock uses a crystal controlled oscillator running at 200 MHz. This is comprised of crystal Y1, NOR gates U9, L1, R4, and the associated capacitors.

To select 200 MHz, the signals INTCLK1, INTCLK2 are output in section C3 at U6, pins 2 and 3. The 200 MHz also is applied to divide-by-two flip-flop U22, which produces 100 MHz. The 100 MHz is sent to a series of four decade counters U23, U24, U39, U54. U39 and U54 are CMOS dual counters producing two decades of output.

13.2.3 Clock Control

The 100 MHz (10 nanosecond) signal and all outputs of the counters are sent to multiplexer U38. The output provided is from 10 nanoseconds to 10 milliseconds in decade steps, selected by **SELA**, **SELB**, and **SELC**. The selected multiplexer output is sent to the biquinary ECL divider U52, from which a divide-by-two or divide-by-five may be selected, by enabling the appropriate NOR gate of U37. This allows the selected frequency to be further divided-by-one, two or five by select signals **DIV1, DIV2,** or **DIV5**, respectively. The selected frequency is determined by the loading of the shift registers U10, U53 shown in section D of sheet 5.

The external clock is received from the probe at receivers U71 shown in section C6 on sheet 5. The qualifier bit, **QCLK** also is received at U71. The user can menu select the clock qualifier as a one, a zero or a don't care. If this qualifier input line is not used as a clock qualifier, it can be applied to the circuit as an edge qualifier via flip-flops U55, U40 and NOR gates U25 in section B5. The external clock and qualifier are sent to transparent latch U56 in section C4. Then the clock is applied to buffer NOR gate U41 and sent out as CLKA1, CLKA, CLKB.

If the internal clock were selected, then the external clock will be disabled. This is done on the menu by not selecting either the positive or negative edges of the external clock. If neither edge is selected, then no external clock has been selected, but instead the internal clock. The internal and external clock outputs are tied together at NOR gates U26. These signals are used within the control board as CLKA1, and are sent to each of the Timing Memory Boards as CLKA and CLKB via coaxial cables. In this way, the clock sent from the control board is exactly the same throughout the entire system. The two that are sent to the memory boards are not carried through edge connectors because the frequency is up to 200 MHz. The biphase logic NOR gates in U11 are not presently used.

13.2.4 Arm/Trigger Control

Refer to sheet 3 of the schematic. Two ARM signals are received by U18, one for each of the two Timing Memory boards. Likewise, two TRIGger signals are received by U16. The external signals received by U68/U17 are external link (**EXT**), a waveform link (**WTRG**), and a signal called **LINK** from the state analyzer or rear panel BNC. These inputs can be used for either an ARM or TRIG condition.

Shift registers U19 and U72 control which signals are used as ARM and TRIG conditions, in response to the menu setup.

One additional timing qualifier is available. It is called **TRIGQ** and is derived from the probe A QUALifier input, via circuitry on sheet 5 discussed earlier. It may be menu programmed either as a zero or one level qualifier, a don't care, or as a rising or falling edge qualifier. It is called the ARM edge qualifier on the menu. When all of the qualifiers are satisfied, the outputs of U17 and U18 will go low. These ECL outputs are tied together as shown in a wired-OR arrangement.

The ARM filter circuit shown in section D3 of sheet 3 is comprised of ARM filter hex counter U33, latches U34 control, shift register U73 and the associated gates. In a similar TRIGger filter circuit, U30, U31, U73 are used, shown at section B3 of the sheet. As these two filters are similar, only the ARM filter will be discussed. Since the counter cannot set up in less than 5 nanoseconds, it's clock is delayed one clock period by U34A/U32A before a countdown is started. For example, when all the arm and linkage occurrences have been satisfied, it is time to start the filter's countdown. U33 pin 9, the **COUNT/LOAD-** input is pulled high by U17A. With a 200 MHz asynchronous clock frequency, the next clock will occur in less than five nanoseconds. Instead of starting the count on the next clock, it waits one additional clock.

This allows over 5 nanoseconds, typically 7-8 nanoseconds, which will satisfy the setup time for counter U33. If this counter is loaded with a zero, it signifies that the filter is OFF. In this case, the signal will pass directly through latch U34 and the next clock will cause the ARM output. Otherwise, the counter decrements to zero, and U48A-15 enables U34.

The output ARM and TRIGger signals are sent to the delay counter circuits shown on sheet 2.

13.2.5 Delay Circuits

Once the user defines the ARM and TRIGger events, as described earlier, he can also choose to program a delay between the two. The delay count may require the TRIG event to occur BEFORE, AFTER, or ON nnnn CLOCKS, or BEFORE or AFTER nnnn ARMS.

Refer to sheet two of the schematics. A 14-bit presettable counter is formed by U28, U27, U42, all 10136 counters, and U14, a 10H131 dual flip-flop, with associated gating. It is loaded with a delay value by the control program via shift registers U12 and U13. It begins counting down when ARM occurs, and when zero is reached, it outputs **TC+** (Terminal Count) and **TC-** at U45 pins 15 and 9. U45-14 also goes high, which inhibits further counting.

TC- (U45-9) is high until the count expires, which blocks a low-going trigger signal from passing through flip-flop U46B. This is acccomplished by pulling high the wire-OR connection with the -TRIG signal at U44-15 (section B-3); a low state would be required to allow a trigger. If menu-selected (by a low SET2 signal at U46-12), this allows a trigger to pass only AFTER the delay period. Similarly, TC+ goes high only after the count expires, and thus allows triggers to pass through U46A only BEFORE the delay is over. That mode is enabled by a low SET1 signal at at U46-5. In either case, the U46 output **PTENB** (Post Trigger Enable) goes high only when the menu-selected sequence is met. PTENB is also latched by U45A,B, and sent to the mother board as **FT+** (Fast Trigger), which is a LINK signal to trigger the state analyzer or other slave.

Clocking for the delay counter, **CLKC**, comes from U4-4 (section C-6). Two sources are possible for this clock: CLKA1 (U36-13), the main timing analyzer clock, is selected by CLKEN (U36-12); or occurences of the +ARM event (U32-7) are selected by ARM ENB (U32-6). The enable signals are set by the control program to allow a choice of delay-by-clocks or delay-by-ARM-events. In the latter mode, the delay counter decrements each time the ARM condition appears and disappears (goes true, then false).

The -ARM signal, indicating the ARM condition is now true, is received by U35-4 (section B-6). This exclusive-OR gate normally inverts the -ARM signal to its positive-true sense, but can also pass it unaltered if MODE SELect from the control program is high. When an ARM occurs, U35-3 goes high. An R-S latch U59A,B is then set, and continues to hold the line high even after the ARM event has passed, due to the wire-OR connection. U29 then buffers this latched ARM signal at pins 2, 3, and 4.

U29 pin 2 goes to four inputs of U2, and disables the control signals that preset U14 and prevent counting. U14, the top two bits of the delay counter, is thus allowed to begin counting. Pin 2 also goes to U3-7, which creates a two-clock delay before releasing U14's reset line. This allows sufficient setup time in the counters at the highest speeds.

U29 pin 3, when the first ARM occurs, sets dual flip-flop U57, whose outputs enable U44 to pass the -TRIG signal. U58 can also be used to enable the trigger signal under certain menu conditions. It is set by the inverse of the ARM signal.

U29 pin 4 controls the COUNT/LOAD- input (pin 9) of the delay counters U28, U27, and U42. When ARM occurs, the line goes high and they are allowed to begin counting. Prior to ARM, the counters are still in the LOAD state.

13.2.6 Post-Trigger Counters

The post-trigger counters are found on the lower part of sheet 4. A ten-bit presettable counter is formed by U20 and U7, 10136 four-bit counters, and U50, a 10H131 dual flip-flop. The counter is loaded by the control program with the the number of samples to be taken after trigger. Shift register U21 loads U7 and U20, while U50 is loaded by manipulating its set and clear lines via U66A and U51.

Signal PTENB, Post-Trigger Enable, starts the count down. Clock signal CLKF at U50 pin 6 is a buffered CLKA1, the main timing analyzer clock. When the count reaches zero, the output of NOR gate U6A goes high. U5A,B form an R-S latch that continues to hold the line high. U32 passes the signal +HALT, which stops the internal clock via U22 and informs the processor that collection is finished. Two gate delays later, U60 sends +HALT to the two Timing Memory Boards.

13.3 TIMING CONTROL SIGNAL LIST

The Model 800 C, D & E Timing Control Signal List is located on page 13-7.

MODEL 800 C, D & E TIMING CONTROL SIGNAL LIST

SIGNAL	DESCRIPTION
200 MHZ SEL	When low, selects the 200 MHz clock
ARM ENB	When high, causes delay counter to count arm occurrences.
ARM+	Output of the arm word recognizer, high active.
ARM-	Output of the arm word recognizer, low active.
BI PHASE+	Always low, not used.
BI PHASE-	Always high, not used.
CLK A	Clock to memory board.
CLK B	Clock to memory board.
CLK EN	When high, causes delay counter to count clocks.
CT	Clock for Counter/Timer board.
EXT CLK	External Clock Inputs
EXT (TTL)	External Link Inputs
FT+	TTL level of PTENB used as link output.
HALT+	When high, inhibits all clocks.
INT SEL	When low, selects internal clock.
LARM	Goes low when the first arm occurs.
LINK (TTL)	Link bit between the instrument, high active.
PROC.CLK	To initialize delay CNTR. For counting arm occurrences.
PTENB	Goes high when ARM, COUNT, TRIG events have occurred.
Q0-	When low, qualifies 0 for QCLK.
Q1-	When low, qualifies 1 for QCLK.
QCLK	Clock qualifier inputs.
RESET	Initializes all Flip Flops.
SEL A,B,C	Selects the internal clock rate.
DIV 5,2,1	Selects the internal clock rate.
SET1	Set high when trigger is expected after N counts.
SET2	Set high when trigger is expected before N counts.
SWNE-	When low, selects EXT CLK negative edge.
SWPE-	When low, selects EXT CLK positive edge.
T1-T4	Selects edge qualifier operation.
WTRG+	Link input from waveform.

SECTION 14: MODEL 800 C, D & E TIMING MEMORY BOARD

14.1 Introduction ——— 14-1

14.2 Description ——— 14-2
- 14.2.1 Processor Interface ——— 14-3
- 14.2.2 Clock Generation ——— 14-3
- 14.2.3 Timing RAM ——— 14-4
- 14.2.4 Threshold Level DAC's ——— 14-8

14.3 Signal List ——— 14-10

14.1 INTRODUCTION

The Series 800, 200 MHz Timing Analyzer consist of one Timing Control board (described in Section 13) and two functionally identical Timing Memory boards (described below), each handles 8 channels of data from the two M81A Probes. The analyzer samples incoming data at up to 200 MHz on all channels using an internal clock, and at up to 75 MHz using an external clock. The operation of only the A Memory Board will be described. The only difference between the boards is the address decoder chips (U46), thereby enabling easy subassembly fault isolation by swapping after the decoder chip is interchanged. These Timing Memory Boards (**TMB**) store high-speed incoming data in a multiplexed high-speed RAM as directed by the Timing Control Board (**TCB**). Also, using logic-gate comparators, matches of incoming data with keyboard-specified arm and trigger words are detected. When specified from the keyboard, data glitches are detected and pulse-stretched for storage and display.

Each board contains analog circuits (on sheet 4) to allow setting of the voltages for the threshold from the menu control. The M81A Probes are connected via the motherboard, the daughter board, and the probe cables. Differential ECL level Probe data is received by receivers U53, U54, U55, shown on sheet 2 and applied directly to the two Gate Arrays, U41 and U42. These proprietary ECL monolithic integrated circuits are housed in a 68 pin leadless chip carrier (LCC) package and are available only through NICOLET.

The Gate Arrays each contain sample and latch circuits and data comparator (word recognizer) circuits. They receive data patterns from the probes, sampling and latching them. The comparator circuits will recognize a matching pattern that the user has defined for TRIGgering or for the ARMing, sending a TRIGger or ARM match signal to the Timing Control board to advance the sequencer state. Note that the ECL circuits in the Gate Arrays are fast enough so that any glitch pulses >3 ns (in ECL logic only) will be detected. These are stretched so that they can be sent, along with received data, to the memory. The Timing Memory board circuits are operating at very high speed, 200 MHz, yet the memory chip technology is limited to 50 MHz. An implementation with four-phase operation between the Gate Array and memory is used. Thus, there are four sets of memory U28-U29, U30-U31, U6-U7, U8-U9. While data is received at each set of memory, every 20 nanoseconds, the Gate Array is sending data every 5 nanoseconds to one of the four sets of memory.

This data sampling continues until specific data is recognized and the ARM signal is sent out. The ARM/TRIGger signals are sent via ribbon cable to the Timing Control board for processing.

14.2 DESCRIPTION

Refer to the schematic **166-031201** and the block diagram of the Timing Memory board shown in Figure 14-1. Also refer to the signal list, board layout and parts list included at the end of this manual. Tables of connector pins versus signal names for all motherboard connectors are provided in MOTHERBOARD CONNECTIONS. An alphabetical list of all interboard signals is also provided. The GLOSSARY section offers explanations for terms that may be unfamiliar.

The functional units of the Timing Memory Board are the Processor Interface, Timing Generator, High-Speed RAMs, Data Receivers and Digital to Analog Converters (DACs). These units are discussed in detail in this section.

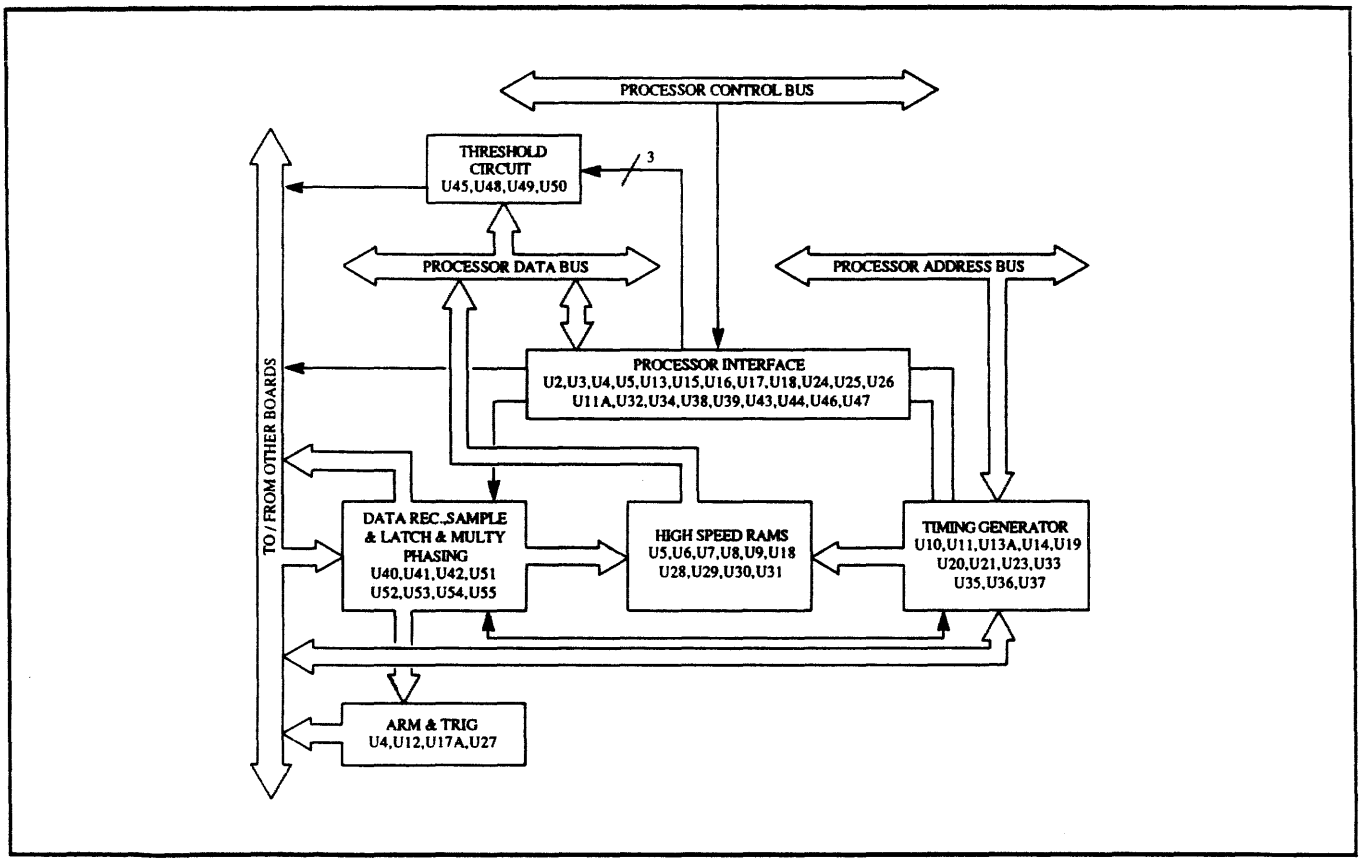

Figure 14-1: Timing Memory Board Block Diagram

14.2.1. Processor Interface

Refer to sheet 3. U47 is the bidirectional bus transceiver that will receive the word recognizer data and also the data for clock phasing (memory chip interweaving). The address decoder logic, U46, U34, U44, receives the addresses which are used in several ways. The logic generates the shift register clock signal (**SRCLKIN**). The Gate Array is loaded with SRCLKIN and the DAC address load signals (**-LD1** to **-LD3**) come from U44 based on these clocks. The software clock (**SWCLK**) in section B1 used to clock RAM addresses after collection is complete.

The serial shift register (U26 and U39) is loaded by the clock (**SRCLKIN**) generated by the address decoder logic and shifted in level by comparator, U43. The clock signal SRCLKIN is also sent to the Gate Arrays, U41 and U42, on sheet 2 in section C8. This signal controls the word recognizer pattern loading in the Gate Array and some of the timing circuit control lines to the shift register. This shift register is loaded serially only through data bit zero (DB0). The data comes from the data bus and loaded one bit at a time. The data is clocked into the shift registers by SRCLKIN. The operation is repeated about forty times to load the shift registers. The shift register output (ED0-ED7 + SELECT and control lines) is sent to the multiplexers U51, U52 shown on sheet 2.

14.2.2 Clock Generation

The 200 MHz clock for this system is generated and initiated on the Timing Control board. It is sent to the Memory board through the coaxil cable shown on sheet 5, CLKA. Several different timing signals are generated. A set of four timing signals is generated, one for each set of the RAM memory spaced at 5 nanosecond intervals. This technique is discussed in the next section on Timing RAM. Another timing signal generated will control the loading of addresses received from the processor. The loading always will start from a known address which is referenced as 0. It will write data into this one location, then the next, but the addresses must be set before the data to be recorded is present. Addresses are set for one block while the data is being loaded into a previously addressed block, i.e., addresses are being "set" multiplexed ahead of the data.

The timing relationship for writing the data and sending the addresses is not feasible at all frequencies. It works for frequencies less than 50 MHz. Over 50 MHz, a different timing method is used. The timing generator circuit generates the address timing and also generates a different set of timing relationships dependant on the clock frequency.

14.2.3 Timing RAM

The Timing RAM is comprised of the address counter, rollover detector and the Timing RAM sections 1, 2, 3, and 4. On sheet 2, these sections are in chips U30 and U31, U29 and U28, U9 and U8, and U7 and U6 respectively. Each of the four sections stores 256 8-bit words, thus the total storage capacity is 1024 8-bit words. The memory is arranged so that the 10 nS RAMs can store data that is clocked at intervals as short as 5 nanoseconds. The chips are ECL logic parts, Fairchild or AMD 93422 256-word x 4-bit static RAMs with 3-state outputs.

The data received from the Gate Arrays may be generated by either the Model 81A Probe (as timing data), or the Waveform Recorder Board (as Waveform data). After collection, data stored in the Timing RAMs may be read by the Control Program for analysis and display.

Refer to sheet 2. The data comes from the probes through the daughter board and the Motherboard P2. Once on the Timing Memory boards, the data is received by 10H116's U53, 54 and 55. It is then sent to the Gate Arrays, U41 and U42. U51 and U52 are used to receive data from the Waveform board since it uses the A Timing board described herein to store the flash-converted data. Since U51 and U52 are multiplexers, ED0-ED7 or the Waveform data could be sent to the Gate Arrays. ED0-ED7 data are written into shift register U39 by the processor for the purposes of test. Presently all factory tests are performed using external patterns applied through the probes. It should be noted that Gate Arrays are programmable to accept either the probe data or the Waveform data at MUXin. See Figure 14-2. Once the data is input to the Gate Array it goes through a sample and latch circuit and then gets clocked into latches.

The output of this flip-flop goes to the word recognizer circuit as well as a 4-phasing circuit to stretch the data. The outputs of the word recognizer are called ARM and TRIG and the data outputs are called D11- D44. The data output from the Gate Array goes directly into the memories. Shown as inductor symbols on the schematic L1-L4 are ferrite beads for isolating VCC1 from the ground. These function to prevent the Gate Array outputs from oscillating.

The timing diagram in Figure 14-3 (page 14-5) explains how the data get written into the memories. The data stream (labelled DATA A, B, C, etc.) is the data fed directly from the probes into the Gate Array. The clock trace is labelled CLOCK and is the system clock rate at which the data is sampled. This is menu selected. CLK1-CLK4 are the four-phase clocks derived from the CLOCK, but at one-fourth the frequency.

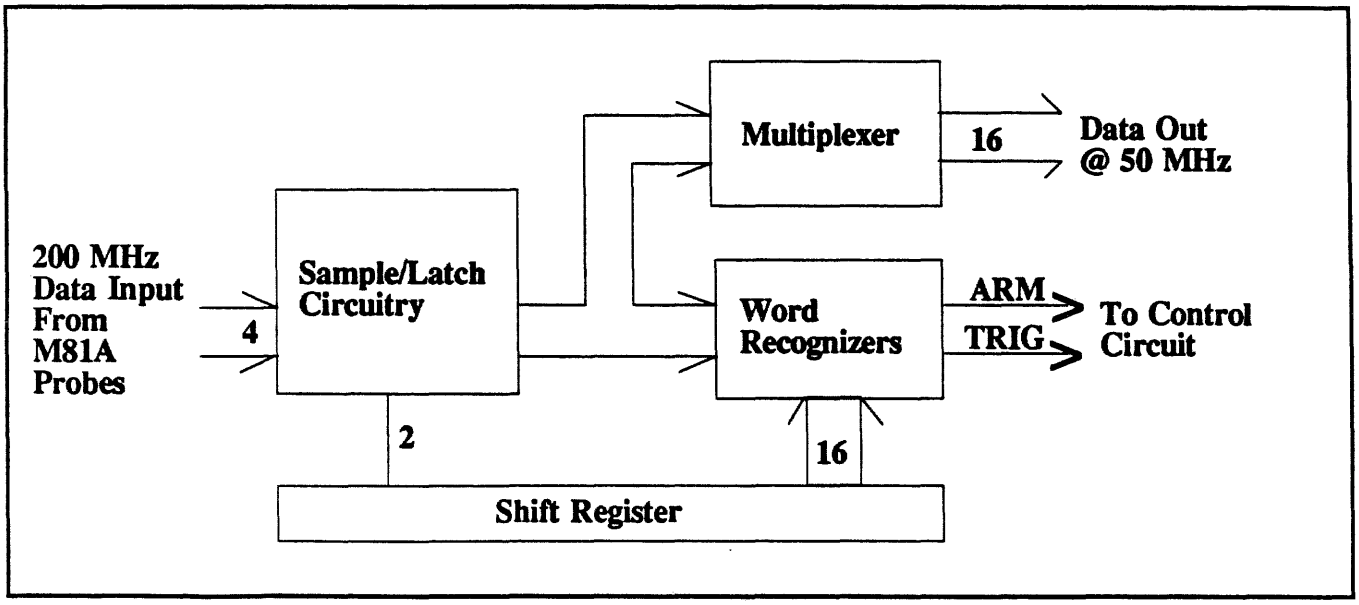

Figure 14-2: Gate Array Block Diagram

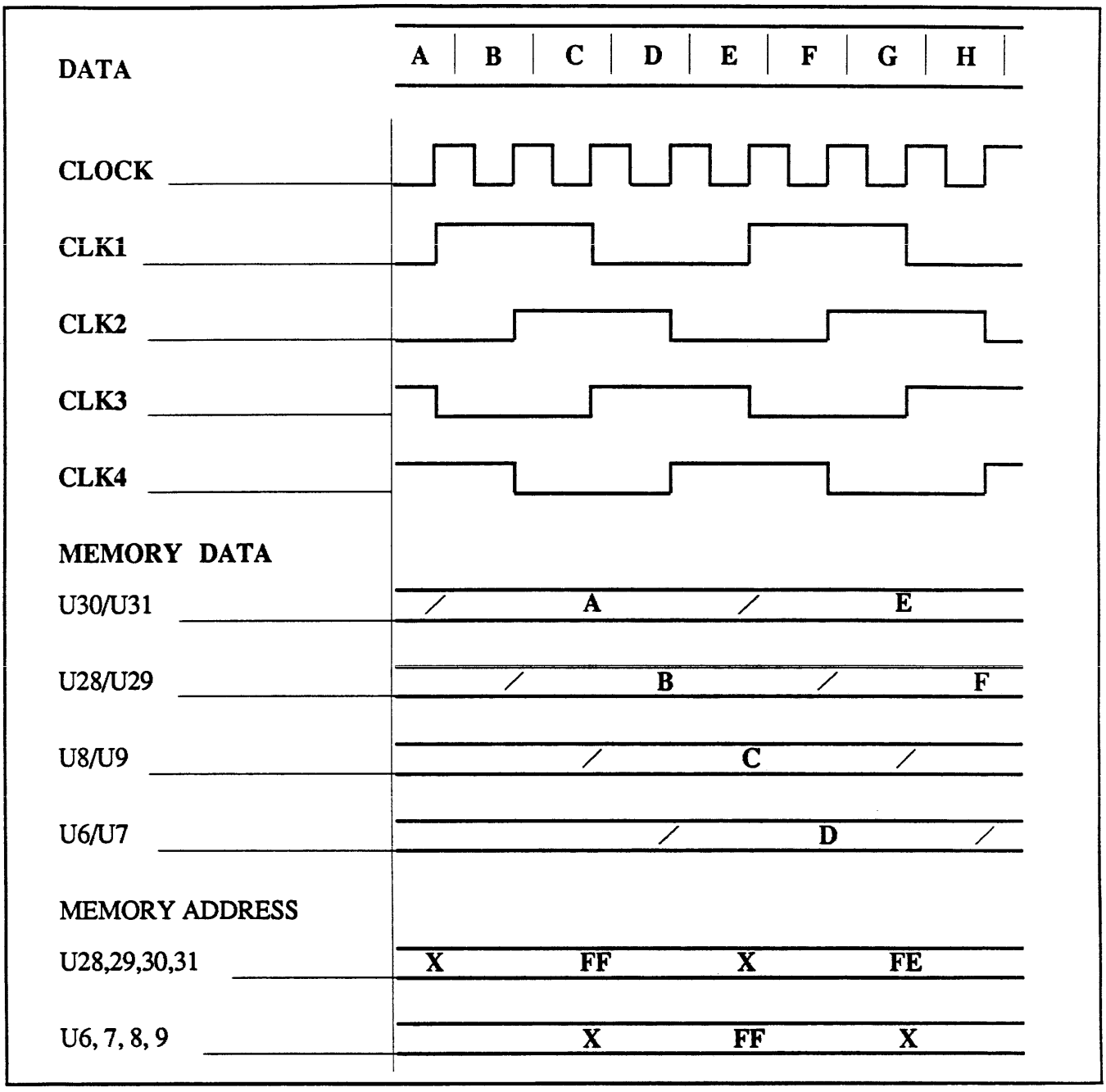

Figure 14-3: Timing Diagram

As is indicated in the timing diagram, the four-phasing allows the data to be present four times longer than the sample rate. This makes possible the memory writing when data is sampled at the maximum 5 nS interval. This timing relationship remains in effect regardless of sampling speed. When the collection is made, all of the high speed RAM's (U6, 7, 8, 9, 28, 29, 30, 31) are chip enabled, but the write signal to each byte happens at different times. However, when the data is read by the processor for display purposes, only two RAM's at a time are enabled and their output is read through U5 and U18 (3430). These chips are in effect ECL/TTL translators with tri-state outputs.

While the analyzer is collecting, the addresses to the RAM's are provided by the address counters U15 and U16 (10136, sheet 4). As indicated in the timing diagram, addresses to the memories associated with phase 1 and 2 is one half phase offset from phase 3 and 4. This is done by latching the addresses for phases 3 and 4 into U2 and U3 (10153) one half phase later. It should also be noted that the address counter starts from FF and counts down to 00. If the data collection rolls over in the memory while looking for a trigger, the OVER FLOW bit gets set by U17 (10131) to indicate this fact to the processor.

After collection is done and while the collected data is being read by the processor for display, the address for the memories is determined by the processor. These incoming addresses are translated from TTL to ECL by U24 and U25 (10124). In this case, the counters function as latches, latching the address that the processor is sending. Write signals to the memories are generated by U20 and U21 (10H131, sheet 5). When the analyzer is done collecting, the hardware, status gets latched in U33 (10186) and read by te processor through U37 (3430). This is done for calculating the last address of the memory with valid data. Prior to the processor addressing the memories for read, it sets WR1-WR4 high so that nothing will be written.

When the Timing Memory board has triggered and collected all of the data, the status is read by the processor, then the software clock SWCLK will clock the RAM addresses. The SWCLK is sent to the address counter via a wire-OR connection at U15-13 (sheet 4, section D5.) This logic is now no longer using 200 MHz analyzer clock from the Timing Control board, but is using the clock received from the processor.

On sheet 4 in section D6, the address data (A2-A9) for presetting the Address counters U15 and U16 is received directly by TTL to ECL translators (U24, U25) from the processor via the mother-board. The translator outputs are inverted since the counters U15, U16 are used as decrementing counters. In the 700 Series hardware, incrementing counters were used and thus those address lines were not inverted. The inverted address data are sent to hex counters U15, U16 which are wired in cascade to produce an 8 bit output. The 8-bit output is sent to the input of address latch U2 and U3. The description of their interaction follows.

The address counter starts at 000 and decrements the address one count. When the timing analyzer is being loaded, it will start with this known address sent by the processor as a preset. The software will always load address 0 which will be translated into timing memory as address FF. The high speed recording RAM counters U15 and U16 must be in the preset or load mode and require a clock signal. When -PRESET is low, the counters will be in the preset mode (pin 9 low). When -PRESET is high, the counters are in a countdown mode (pin 9 high). The -PRESET signal is software controlled as is the software clock signal SWCLK. The sequence then is as follows:

a. The software holds the addresses on the address lines. The data is received, translated and inverted by U24, U25. The counters are held in the preset mode by -PRESET being low.

b. When the software instructs the logic to latch the address, the software clock is pulsed. The address data is loaded by the two counters and latched.

Each time the software clock goes high, it causes the counter to be decremented by one if in the countdown mode; or if in the preset mode, it will cause new address data to be latched. The software clock also is sent to negative D-latches U2, U3. The negative D-latch outputs only follow the input if the clock input (pin 13) is low. When the clock goes high, it latches the contents and will not change, regardless of the input signal. Thus, when the clock goes high, the negative D-latches latch the current address data and the counter decrements by one. On the next half-cycle, the clock goes low, and the latched values will be sent from U2, U3. On the rising edge of the clock signal, the data for U2, U3 become stable and U15, U16 data are changed. On the falling edge of the clock signal, the counters remain stable in preset mode, but the outputs of U2, U3 change. The output of the counters U15, U16 are used for the A side of memory, phase 1 and 2. The outputs of the negative D-latches U2, U3 are used for the B side of memory, phase 3 and 4.

When the function is complete, the software reads the status. This information includes the "last address used" location, which phase was written last, and whether the overflow bit (U15 pin 4) was true. This information is used to determine the location of the trigger word in the Timing RAM.

To determine the last address written, the carry out (pin 4 of U15) is monitored by ECL-to-TTL tri-state translator, U38. When strobe 2 (signal -ST2) becomes active ECL data is translated to TTL data and sent to the data bus. The software monitors the processor data bus bit D5 output of U38, if it is not 0, then counter U15 has not reached terminal count and another software clock signal is sent. When bit D5 sent from U38 is 0, then the software uses the number of clock signals sent to determine the last memory location used.

Translator U38 also is used to keep track of the overflow bit. The most significant bit of the counter U15, AA7, is high during the countdown. This is changed when the counter completes decrementing from FF to 00, then AA7 goes low. This bit is the clock input to flip-flop U17. When U17 is clocked, the inverted (Q-) output goes high indicating OVERFLOW to be true. This condition means that the memory has rolled over and is read by the software via U38.

14.2.4 Threshold Level DAC's

A difference between the Model 800 A and B Systems and the Model 800 C, D, & E Systems is that in the latter systems, up to three different thresholds are used for various inputs in each probe. Probe A uses different hardware for channels 0-3, channels 4-7, and the clock/clock qualifier inputs. Probe B's channel grouping for thresholds are the same, but the clock/clock qualifier group is not used. On the menu there are five threshold groups, three for the A board and two for the B board. Each time the operator writes into one of these fields to alter the factory default settings, he then executes COLLECT, and the data is written into the selected DAC. The thresholds may be set from +6.35 volts to -6.4 volts. All three groups are provided for with necessary DACs in both the A and B Timing Memory boards.

The processor data bus received at U47 is sent in parallel to the three DACs (U48, U49, U50) in the threshold circuits, as shown on sheet 4 section A/B/C6. The three sets of DAC808 DACs and LF347 op-amps all operate in an identical manner. These DACs each have a self-contained latch. This simplifies the operation to sending the binary data to the DAC input and enabling a load signal (LD1, LD2, LD3). The data is received in parallel by all three DACs, but each DAC has a different load address. The proper DAC load address line goes low (-LD1, -LD2 or -LD3) and the data is latched into the proper DAC. The DACs output a current, so a current-to-voltage converter op-amp (U45) provides the function of converting the output into an analog voltage. The current output of the DACs may be from 0-2 milliamperes.

The reference voltage for all DAC's should be set to -10.0 V at TP1 by R38. If 00H (the lowest limit) is written into the DAC from the bus, then there will be no current flowing from the DAC. With no current flowing through the 6.49 K Ohm resistor (R28, R29, or R30), there will be no voltage drop across the resistor, therefore the circuit output will be -6.40 volts. However,if FFH (the upper limit) is written into the DAC from the bus there will be 2 ma current flowing out (this 2 ma current should be adjusted by the 1K Ohm resistor provided at the input of each DAC while monitoring the output voltage). This current flows into the 6.49K resistor and causes approximately +13 volts of voltage drop. Since one end of the resistor is at -6.40 the other end will be at +6.35. The voltage +6.35 is achieved by adjusting the 1K pot R40-R42. For every increment between 00H and FFH (256 steps), the output voltage ranges from -6.40 to +6.35 in 50 millivolts increments.

The data for the DAC's go through a transceiver U47 (74F245) from the data bus and write signals, -LD1 to -LD3, are from the address decoder circuit, U46 (6349) and U44 (74LS139). These -LD signals are low active and should go low no sooner than 50 nS after the data setup. This is the purpose for the delay through U43 (LM 339, pins 9 and 14).

The DAC current may vary up to 2% between DACs, so an adjustable calibration voltage is used to set each DAC. This adjustment is made using R40, R41, R42 for U48, U49 and U50, respectively. The reference voltage is generated by Zener diode CR1 (7.5 V) plus diode CR2 (0.5 V) providing an 8 V reference. This voltage is divided by the resistor network R36, and R39, R34, R33, and applied to pin 10 of the appropriate DAC. The potentiometers are used to adjust the output current of each DAC as measured at the op-amp outputs.

The op-amps (U45) are supplied with a reference voltage of -6.40 volts by the voltage regulator VR1 and the associated resistor network. Potentiometer R38 is used to set this voltage to -6.40 volts. These op-amps are configured with a negative feedback loop. This means that a voltage on one input is equal to the voltage on the other input. For troubleshooting, if -6.40 V is applied to the positive input (pins 10, 3, 12), then the same voltage must appear on the negative input (pins 9, 2, 13). The voltage should vary only by the offset voltage of the op-amp (a few millivolts). If the voltage is different by more than this amount, a faulty component is indicated, either a resistor, capacitor or the op-amp.

To adjust the reference with R38, a value of 00 HEX is applied to the DACs from the menu. Then the potentiometer is adjusted so that -6.40 volts is the level at the DAC output. This makes zero current flow through the 6.49K ohm resistors R28, R30, R29. For this adjustment, program +6.35 volts into the menu for threshold and setup the analyzer to run that value to the DAC by pressing COLLECT. This should provide a 2 ma output from the DAC and a voltage drop of approximately 13 volts across the 6.49K resistor R28, R29 or R30. Potentiometer R40 should be adjusted so the op-amp output at THRESHOLD A (P2- 14) is +6.35 volts. Check several intermediate values of threshold voltage to verify correct operation. All threshold voltages also should be checked at the probe to completely verify proper system operation. The voltage readings should be accurate within 50 millivolts.

MODEL 800 C, D, & E TIMING MEMORY SIGNAL LIST

SIGNAL	DESCRIPTION
DO-D7	Data from the Timing Probe.
WD0-WD7	Data from the Waveform Board.
ED0-ED7	Data from the Shift Register.
SR CLK	Shift register clock.
SR D IN	Shift register data in.
CLK1-CLK4	4-phase clock.
SELECT MUX	Selects either WD0-WD7 or ED0-ED7
CLK A1	System clock for gate arrays.
ARM * -	Word recognizer OUTPUT,ARM
TRIG * -	Word recognizer OUTPUT,TRIG
AA0-7	Memory address for phases 1 and 2.
AB0-7	Memory address for phases 3 and 4.
BS1-	When low, selects phase 1 memory.
WRT1-	When low, writes to phases 1 memory.
D0-D7	Data bus to and from the processor.
Vbb	Equal to -1.30 volts, reference for ECL.
LD1-	Writes on falling edge data bus value into DAC.
ST1-	When low, processor is reading PORT 1.
HS-/LS+	Not used, always low.
PRESET+	Initializes latches.
PRESET-	Sets memory address counters to be latches.
SW CLK	Software clock; clocks the memory address into U15/U16
HALT-	Inhibits all clocks.

SECTION 15: CT/SA (COUNTER TIMER/SIGNATURE ANALYZER) BOARD

15.1 Introduction ——— 15-1

15.2 Microprocessor Interface ——— 15-1

15.3 Input Circuit ——— 15-2

15.4 Counter-Timer Description ——— 15-2

15.5 Signature Analyzer ——— 15-3

15.1 INTRODUCTION

The Counter-Timer/Signature Analyzer (C-T/SA) board contains two independent functions that share input circuitry and microprocessor interfacing. The Counter-Timer section is a full function frequency counter and interval timer based on the Intersil ICM7226B LSI device. The Signature Analyzer is based on a 16-stage tapped shift register with feedback. This generates a calculated number based on a serial bit stream received via the input probe. It emulates the Hewlett-Packard algorithm for signature analysis. Nicolet is under license from Hewlett-Packard to produce the H-P compatible signature analyzer.

15.2 MICROPROCESSOR INTERFACE

Refer to the block diagram, Figure 15-1 and schematic **166-009901** (sheet 3). The C-T/SA Board occupies I/O space from 70 HEX to 73 HEX . The six most significant bits are decoded by U5 (74LS32) and U6 (74LS10). These output signals are used to gate U16, a 74LS138. The most significant select bit is connected to the S1 (pin 47) signal of the processor. This determines if the cycle is a read or write. Consequently, outputs **Y4-Y7** are I/O read select lines, and **Y0-Y2** are write select lines for addresses 70-73, respectively. These signals are used for the functions described by their names on the schematic.

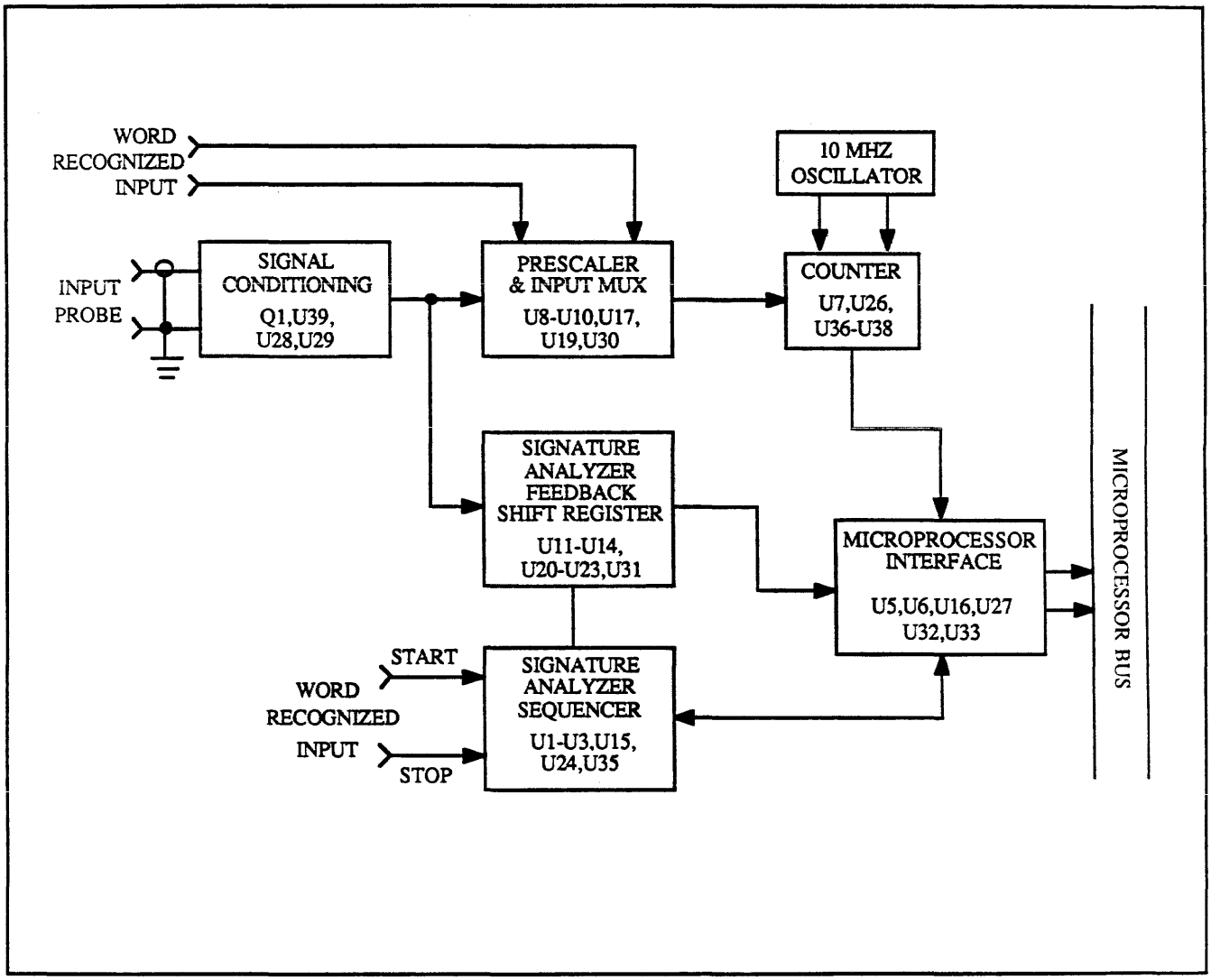

Figure 15-1: CTSA Block Diagram

15.3 INPUT CIRCUIT

Refer to sheet 2. The DATA IN signal is applied to Q1A via the input r-c circuitry. The input impedance of this circuit is approximately 1 megohm shunted by 30 pF. Capacitor C36 provides high frequency compensation. Diodes CR1 and CR2 clip the input signal at ±2.5V. This protects FET Q1 and U39, the AM687 high speed comparator. Transistor Q1 is set up as a zero-offset source follower to provide DC coupled current gain. R26 is adjusted for zero volts at U39-8, with input probed grounded. U39 compares the input signal with a threshold voltage generated by the D/A converter U28 and buffer U29.

The ECL level outputs of U39 drive a delay line. The delay line output is used by the Signature Analyzer, and a pre-scaled and input MUX that is used by the Counter-Timer. The delay line is necessary to adjust the timing of the input data with the clock. The clock must go through additional circuitry within the rest of the Logic Analyzer.

Other inputs to the board are the Arm and Trigger signals, S2 pins 9 and 10. These are generated by the state analyzer and become start/stop signals. The start/stop signals are used by the Signature Analyzer and the Counter-Timer in interval mode. These are buffered by U10, an MC10116, and synchronized by part of U30, an MC10176.

The clock signals CT and CWE+ are buffered by U10 and U39 respectively. The selection between these two signals is made by half of U19. This is done by grounding of one of two S2 connector pins (28 or 29). The pin grounded indicates that it is being used in a state or timing analyzer. In all 800 models, pin 29 is grounded and SIG CLK+ comes from CWE+, the state analyzer's collection clock.

15.4 COUNTER-TIMER DESCRIPTION

Refer to sheet 2. The Counter-Timer device receives the DATA A input via four-to-one multiplexer U9 and ECL-to-TTL converter U17. The MUX enables the processor to select either the rear panel probe input, the probe frequency divided-by-10 via U8, the start (ARM) signal, or the system clock. In addition, the stop (TRIG) signal is buffered by U17 for use in the interval mode.

Refer to sheet 3. The range and function inputs of U7 (ICM7226B) are driven by U27 and U38, both 8-to-1 multiplexers. These select which of the digit strobe signals are sent to the range and function inputs. The select lines of both multiplexers are driven by U37. U37 is an octal latch that is setup as output port 70 HEX .

The Intersil ICM7226B provides an eight digit output with the following characteristics: Frequency of input A to 10 MHz; period of A from 400 nanoseconds to 10 seconds; frequency ratio of A to B inputs; and interval from A input to B input.

The results of the measurement are presented at the BCD outputs sequentially. That is, one digit at a time, as indicated by the digit strobe outputs. These digit strobes are sent to a priority encoder, U26, that encodes these eight inputs into a 3-bit binary word. The four BCD outputs, the encoded strobe, and a valid strobe signal are buffered onto the processor bus by U36. This is initiated by an I/O read from address 72 HEX .

Half of U25 is used to detect an overflow status. This signal, and measurement-in-progress, are buffered by U34. This is the status port and responds to an I/O read from address 73 HEX. The Signature Analyzer status is also read from this port.

15.5 SIGNATURE ANALYZER

Refer to sheet 1. The Signature Analyzer is based on shift registers U11 through U14 and XOR gate U31. A delay is generated by U30 to compensate for delay in the start and stop signal paths. Input signal SIGDATA from the probe amplifier is summed with a feedback signal from the 16-stage shift register. The feedback signal is generated by summing the 7th, 9th, 12th and 16th stage outputs in U31. This yields a signature identical to that of the Hewlett-Packard Signature Analyzer when used under the same conditions.

The outputs of the shift registers are converted from ECL to TTL levels by U20 through U23. The TTL level signals are then multiplexed onto the Processor Data Bus by U32 and U33. The signature is read by I/O reads from addresses 70 HEX and 71 HEX

The operation of the shift register is controlled by the S1 and S2 inputs. These signals are the outputs of flip-flops U15B and U1A, respectively. These flip-flops, with flip-flop C (U15) and U2 and U3, form a sequencer that operates as shown in Figure 15-2. The state of the sequencer is converted to TTL by U35 and to tri-state by U34. U34 responds to an I/O read from address 73 HEX. The sequencer is reset by an I/O write to address 73 HEX .

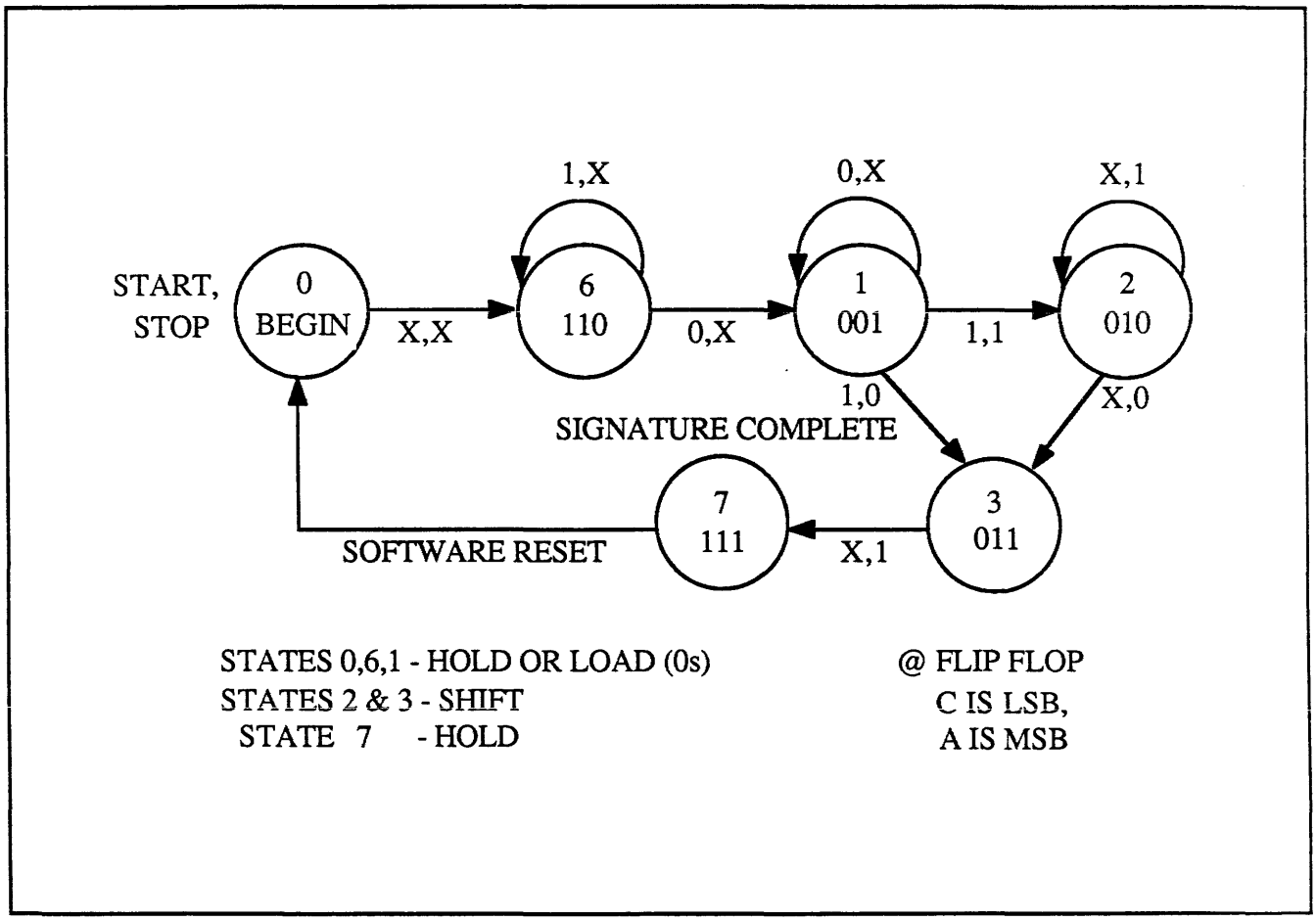

Figure 15-2: Signature Analyzer Sequencer State Diagram

SECTION 16: WAVEFORM BOARD

16.1 Introduction ——— 16-1

16.2 Functional Description ——— 16-2

16.1 INTRODUCTION

The Waveform board provides a high speed analog interface and special display hardware used to display the collected analog signal.

16.2 FUNCTIONAL DESCRIPTION

Refer to schematic **166-007201**, the board layout and parts list at the end of this manual. Tables of connector pins versus signal names for all Motherboard connectors are provided in MOTHERBOARD CONNECTIONS. An alphabetical list of all interboard signals is provided. The GLOSSARY section offers explanations for terms that may be unfamiliar.

The input signal is received via edge connector pin S2-29 that is connected to the rear panel BNC connector. Relay K1 selects DC (closed) or AC input coupling. Relays K2-K5 and the associated components form a precision attenuator network with division ratios of 1, 10, 100 and 1000. Relay K6 provides a ground reference when closed.

FET Q1 is configured as a zero-offset source follower and is used for buffering and impedance transformation. This signal is applied to a low-pass filter consisting of C16, C17 and L1. This filter limits the bandwidth of the signal to be presented to the A/D converter. U13, an SG592 video amplifier, in conjunction with relays K7 and K8, forms a programmable gain amplifier.

Refer to sheet 2. U9, an LH0024 operational amplifier (op-amp), and transistor Q2 provide high speed, low output impedance buffering. This is used to drive the A/D converters and the triggering circuit. The offset, or vertical position voltage is added at the input of U9. The offset voltage is generated under software by D/A converter U11 and the associated buffer.

The triggering circuit consists of an AM687 high speed comparator, U8. This circuit compares the input signal to a reference generated by D/A U10 under software control. The true or complement outputs of the AM687 are selected by U7 to determine the slope of the triggering signal. This output is sent to trigger latch U20, an MC10131 dual D flip-flop. The other half of the MC10131 is used to hold the trigger latch reset until the clock starts.

U6 is wired as output port D5 HEX. This allows control of the circuit via relays K1-K8 and the trigger polarity select line.

Refer to sheet 5. The A/D converter is two multiplexed TRW TDC1014Js. The A/D converter output is sent to the Timing Memory board for storage.

After collection in the Timing Memory, the data is processed by the CPU before being sent to a 256-word x 8-bit display memory in the display section of the Waveform board (sheet 4). The display memory occupies address locations 2E00H through 2EFFH. No provision is made for reading this memory. Operation of the display section follows.

The CRT screen is mapped into the display memory as 256 vertical columns corresponding to 256 X values. Each X value is assigned a memory location. The 8-bit data value in each memory location determines the Y value of the video dot for that X value. The resulting string of 256 dots constitutes the waveform and is sent to the Video Display board for display on the CRT.

It is possible that a dot in the string will be displaced up or down from the preceding dot more than one raster scan line. If this occurs, the circuit will fill in the gap. This is done by adding a string of vertical dots to the scan line in the new column above or below the preceding dot. The number of dots added may range from one to many, as required. This preserves the visual continuity of the display. The circuitry on sheet 3 accomplishes this function.

Note that the line must be allowed to begin and end inside the screen boundaries. Thus, a scale and annotation may be included in the display. The gap-fill feature is inhibited for Y values of FF HEX. The Control Program places an FF-value dot at the beginning and end of the data string. No vertical line is drawn to or from the FF-value dot, and the dot itself is not displayed.

The display may be inhibited by writing a 00 or enabled by writing a 01 to port D4 HEX. The display must be inhibited while the memory is being altered.

SECTION 17: DISK CONTROLLER, COMPUTER, and DYNAMIC RAM

17.1 Disk Controller Circuit ——— 17-1

17.2 RAM Description ——— 17-2

17.3 RS-232C Serial Interface ——— 17-2

17.1 DISK CONTROLLER CIRCUIT

Refer to schematic **166-011201** (sheet 1). The controller utilizes the Western Digital floppy disk controller chip set. These are U34, U18, and U19 (WD1793, WD1691, and WD2143). Signals received from the drive are buffered by U24 and U21 (7414). Signals sent to the drive are buffered by U22, U23 and U38 (7438). This floppy disk controller is programmed for operation with any industry standard 5-1/4" floppy disk drive at double density. The 1 MHz clock which U34 requires is generated from Y2, a 2 MHz crystal. The bi-directional data bus of U34 is buffered by U46 (DP8304). Circuitry for an RS-232C interface also is contained on this board.

Three potentiometers, R1, R2, R3, are shown in Figure 17-1. They are provided for aligning floppy disk R/W operations as follows:

a. R1 (50K ohm) adjusts the output of VCO U17 (74LS629) to free run at 2 MHz. Resistor network R9, R5, R7 ensures quiescence at approximately 1.5 volts at pins PU, PD of U18.

b. R2 (10K ohm) adjusts the amount of data write pre-compensation for tracks > = 44. It is nominally set at 400 nS. The amount of write precompensation can be observed at pin 4 of U18. This is done by putting the disk controller into a continuous write operation.

c. R3 (10K ohm) adjusts the width of RAW DATA-, nominally set at 750 ns.

U34 is selected by address decoder U56 and U35. U44 generates the clock required by latch U45 (LS374) and signal +RDBB. This signal puts the processor into a wait state by pulling RDY low when both INTRQ and DRQ are inactive.

U36 and U37 comprise a time-out circuit. This circuit is used to control the motor ON signal sent to the drive. The time-out circuit causes the motor ON signal to go inactive approximately three seconds after last access. This is done when there is no disk read/write operation, or when U34 has not been selected for more than three seconds. This is accomplished by keeping pin 1 of U36 and U37 high so as to allow the counter U36 to count INDEX pulses. The ripple carry output will then cycle to U37 and U37, pin 6 will go low. On all model 800's, pins 6 and 34 are crossed by jumpers at the disk drive connector to accomodate the particular disk drive used.

17.2 RAM DESCRIPTION

Refer to sheet 2 of the schematic. The system contains 48K bytes of memory (24 chips of 16K x 1 dynamic RAM, U1-U16 and U25-U32). Signals ROW- and COL- respectively strobe in row and column addresses into the RAMs during a read/write operation. U54 and U55 (LS244) buffer the address lines before being strobed into the respective RAM addresses.

Signals RAS, CAS- are generated by the following chips: U39, U49, U50, U40, U41. RAS- has two major constituents: RASA+ provides read or write access and RASR+ increments the refresh address counter U33, whose outputs will be strobed. Note the refresh address inputs when ROW- and COL- have both gone inactive. The refresh counter outputs are buffered by U43 (LS244). U52 (LS374) latches the RAM data-out contents during a read operation. This allows the processor to read the RAM data at an appropriate time. U53 is the input data buffer to the RAMs.

17.3 RS-232C SERIAL INTERFACE

An RS-232C Serial Interface is also provided. The interface is bi-directional, and the Control Program can be commanded to transmit what is being displayed on the CRT. A printer with suitable serial input can thus produce hard-copy duplicates of the menu set-ups and data displays.

Timing, control and serialization of data for the interface are accomplished by the Control Program. Refer to sheet 3 of the schematic. The I/O circuitry consists of USART U47 (6551), line driver U57 (1488) and line receiver U56 (1489).

Signals are routed from the RS-232C connector on the rear panel via a 16-pin DIP socket (J2) on the motherboard to the DISK-RAM PCB socket S2B. Signal flow is shown in Table 17-1.

Some parameters required by the Control Program to operate the interface are obtained from the settings of a DIP switch located on the Processor PCB. The function of these switches for the RS-232C interface are shown in Table 17-2. Figure 17-1 depicts location.

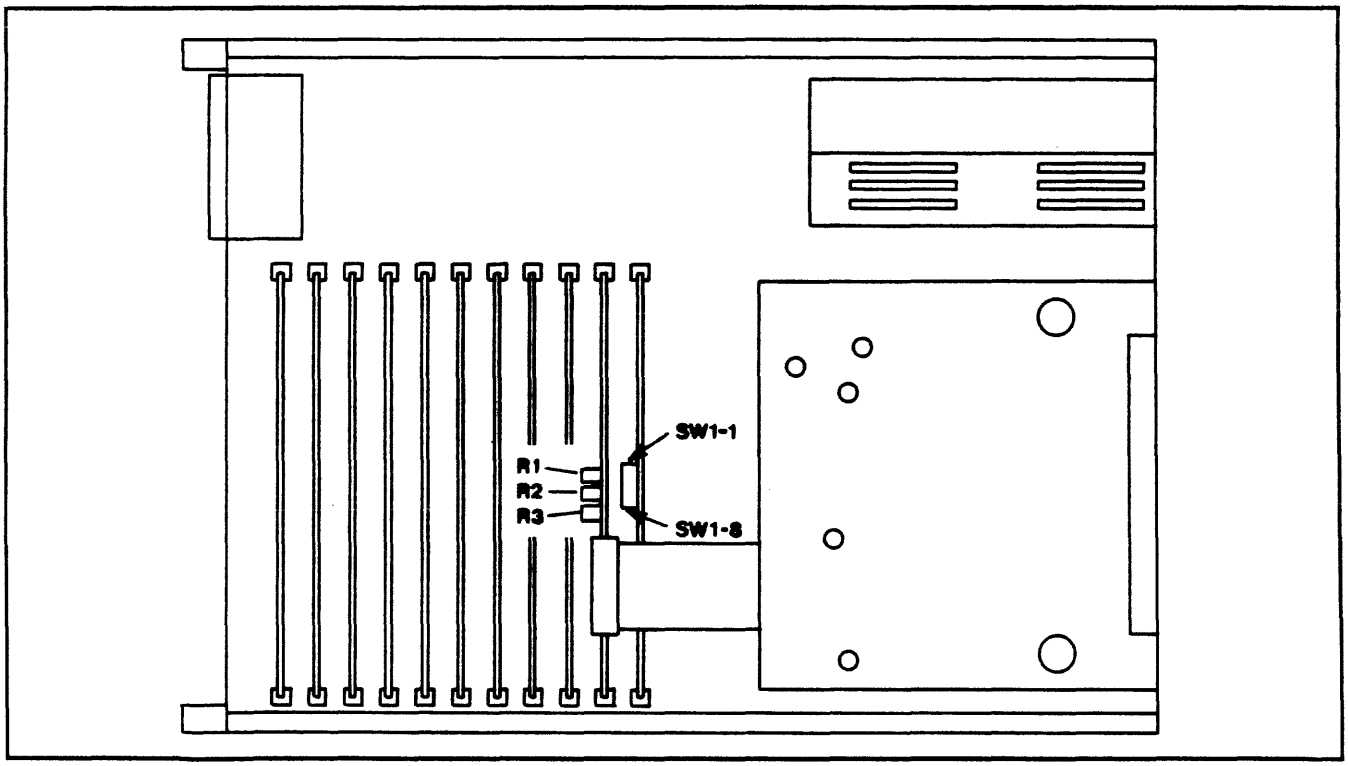

Figure 17-1: Potentiometer and Dip Switch Locations

Signal Outputs	U47 Pin	U57		S2B Pin	Rear Panel DB-25 Pin
		IN	OUT		
TXD	10	2	3	5	3 *
RT	8	13	11	6	4
DTR	11	10	8	35	20
Signal Inputs	**U47 Pin**	**U58**		**S2B Pin**	**Rear Panel DB-25 Pin**
		OUT	IN		
DSR	17	6	4	7	6
CTS	9	3	1	37	5
DCD	16	11	13	36	8
RXD	12	8	10	38	2 *

Table 17-1: RS-232C Signal Flow

* A jumper area is provided on the board for exchanging pins 2 and 3.

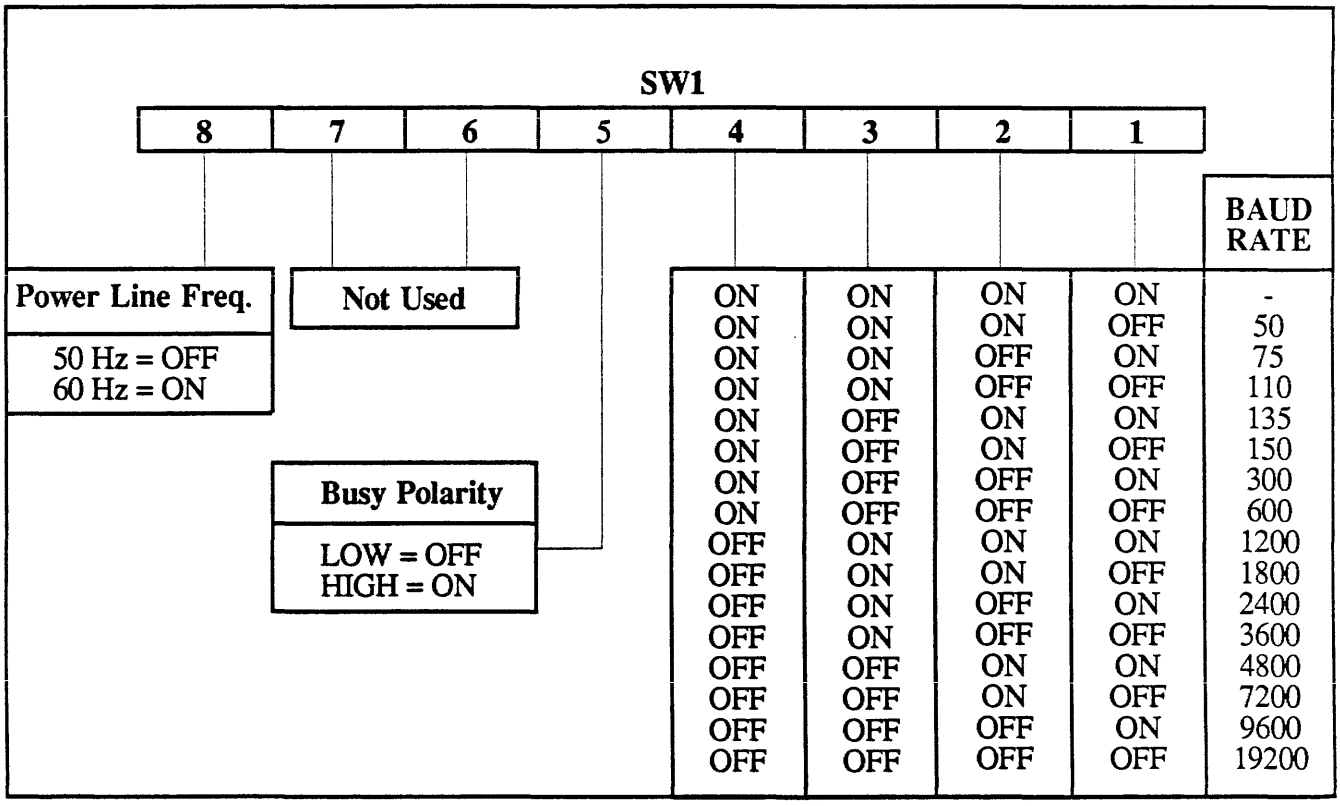

Table 17-2: RS-232C DIP Switch Settings

NOTE: DIP switch is located on Processor Board.

SECTION 18: INPUT PROBES

18.1 Introduction ——— 18-1

18.2 Model 51A Probe ——— 18-2

18.3 Model 80 Probe ——— 18-2
- 18.3.1 Input Buffers ——— 18-2
- 18.3.2 Comparators ——— 18-3
- 18.3.3 Application ——— 18-4

18.4 Model 81A Probe ——— 18-4
- 18.4.1 Hybrid Integrated Circuits ——— 18-4
- 18.4.2 Application ——— 18-6

18.5 Model 90 Probe ——— 18-6

18.1 INTRODUCTION

There are four types of input probes used with the Model 800 Series Logic Analyzers. They are as follows: The Model 51A Probe (for State sections of all models), the Model 80 (for the Timing section of the Model 800 A and B), the Model 81A (for the Timing section of the Model 800 C, D, & E), and the Model 90 probe (for the Counter-Timer/Signature Analyzer and Waveform Recorder sections). These probes provide high impedance signal inputs that can be placed close to the target signals. The probes then can convert the acquired signals to a form suitable for transmission to the Model 800 Series for recording and analysis. A general description follows. The detailed descriptions begin on page 18-2.

The **Model 51A** Probe is used for input to the State analyzer section. The 51A provides inputs for 16 data signals, one clock input signal, and two qualifier signals. Two Model 51A Probes are normally used with the Model 800 A analyzer, whereas three Model 51A's are normally used on the remaining state analyzers in the series. For analysis of microprocessor-based systems, these general purpose (i.e., for TTL, ECL, CMOS etc.) probes are replaced by "quick-connect" microprocessor specific personality probes. Such dedicated probes are not covered herein.

The Model 51A qualifier signals may be applied (by keyboard instructions) to the clock signal internal to the analyzer. At the same time, these same signals may be applied to any or all of the 16 levels of the trigger words in the trigger stack on the Model 800 A, B, or C. In the case of the Model 800 D, these signals can be used on any of the Setup Menu's five events, or be used to qualify the three clocks. The nominal impedance of all inputs is 100K ohms shunted by 10 pF.

The probe contains a manual adjustment for setting the logic threshold of all incoming signals. It also contains a switch for pre-setting this threshold to TTL level. The probe also contains a switch for inverting the incoming qualifier and data signals if desired. The active edge clock polarity is keyboard-selected.

The **Model 80** Probe is used for input to the Model 800 A and B Timing analyzer section. It WILL NOT function properly on an Model 800 C, D, or E analyzer. It provides inputs for eight data signals, a clock signal, and a clock qualifier signal. The nominal impedance of all inputs is 1 Megohm shunted by 6 pF. The logic threshold voltage for these inputs is variable and is set by keyboard entry. Also, the inputs have a keyboard switchable hysteresis function (200 millivolts).

The **Model 81A** Probe is used exclusively for input to the Model 800 C, D or E analyzer Timing section. This probe is NOT functionally interchangeable with the Model 80. It also provides inputs for eight data signals, a clock signal, and a clock qualifier signal. The nominal impedance of all inputs is 1 Megohm shunted by 6 pF. The logic threshold voltage for these inputs is also variable and is set by keyboard entry. No provision for hysteresis has been made.

The **Model 90** Probe is used for input to the Counter-Timer/Signature Analyzer and to the Waveform Recorder sections. It is a standard oscilloscope-type probe.

These probes are described in greater detail in the following subsections.

18.2 MODEL 51A PROBE

The Model 51A Probe interfaces the State analyzer to the system under test.

This probe incorporates comparators for high input impedance and variable threshold selection. Each probe interfaces 16 data bits, 2 qualifier bits and a clock input. A switch on the probe is provided to present a fixed threshold of 1.6 V for convenience. A monitoring point permits measuring the threshold voltage that can be adjusted over the range of approximately ±6.2 V. The voltage at this monitoring point with respect to the probe ground is one-half, or 50%, of the actual threshold voltage. The Model 51A also incorporates a data complement (invert) switch for active-low bus conventions. The impedance for all inputs is 100 K ohms shunted by 10 pF. Earlier versions had 44 K ohms shunted by 15 pF.

Refer to schematic **166-001521**, the board layout and the parts list at the end of this manual.

Resistors RN1-RN4 form voltage dividers that apply one-half of the input voltage to U1-U5. U1-U5 are high-speed quad voltage comparators, either Motorola MC3430 or National DS3651. The input capacitance of the comparators is compensated by capacitors C1-C19. Resistors R4, R5 and R7 provide approximately 200 millivolts of hysteresis to the clock input. Comparators U1-U5 accept a threshold reference from the voltage divider formed by R10-R12 or R8, R9. These high-speed comparators convert the variable input voltages to TTL levels acceptable by the State Memory Board. Switch S1 controls whether buffers U6-U10 operate in a true or complement mode. U10 also selects clock polarity and provides buffering for clock and qualifier signals. The probe receives ±5V power from the analyzer through the ribbon cable.

The Model 51A Probe receives a functional check when used in the analyzer self-test with the Logic Analyzer test card.

Although the input resistor divider provides some input protection, voltages higher than ±25 V may damage the circuits and should be avoided.

18.3 MODEL 80 PROBE

The Model 80 Probe is used for input to the Timing analyzer section of the Model 800 A and B models. Refer to schematic **166-005201**, board layout and parts list at the end of this manual. For each of the 10 input channels, the Model 80 Probe contains an input buffer and a comparator. The circuits of all channels are identical. The schematic diagram shows the first two channels in detail and the remaining channels in an abbreviated form.

18.3.1 Input Buffers

There are 10 input buffers: one for each of the eight data inputs, one for the clock input and one for the clock qualifier input. Because all the buffers are identical, only one will be described. That description can be applied to all the others.

The channel-0 input buffer consists of transistor Q1, a Siliconix E420 dual J-FET; CR1 and CR2, both 1N3600 diodes; and various capacitors and resistors.

The major functions of the buffer are to provide signal isolation and high input impedance.

The impedance presented to the incoming signal is essentially determined by the 3:1 passive divider made up of R1, R2, C1 and stray capacitance. The high input impedance of Q1A has little effect on the overall circuit impedance. This input impedance is nominally 1 Megohm shunted by 6 pF. CR1 and CR2 are clamping diodes that provided overvoltage protection for Q1A against input voltage peaks as high as ±100V. The useable input voltage switch (before clipping by these diodes begins) is ±9V. Q1A is a zero-offset source follower circuit. The output of this circuit is fed to the Channel 0 voltage comparator.

Variable resistor R5 is used to compensate for any mismatch that may exist between Q1A and Q1B. R5 is adjusted so that, with the signal input grounded, the voltage at pin 9 of the comparator U1B is 0.0V ±0.005V.

18.3.2 Comparators

As with the input buffers, there are 10 identical comparators and only one will be described.

The Channel-0 comparator consists solely of U1B, one-half of an AMD AM687 high-speed dual comparator with complementary ECL outputs. The comparator converts a variety of logic-signal inputs into outputs with pre-established ECL levels and fast transition times.

The comparator positive input, U1B-9, is fed with the low impedance signal from the Channel-0 buffer. The negative input, U1B-10, is fed with threshold voltage **THRESHA** (threshold A) that is compared to the incoming signal. As the input signal crosses this threshold from below, the output of the comparator switches from low to high. As the input signal crosses this threshold from above, the output of the comparator switches from high to low. THRESHA is received, via connector pin J6-5, from a D/A converter on the Timing Memory Board (sheet 1, TMB schematic). It is keyboard-specified over a range of -6.4V to +6.35 V in 0.05V steps. The default value is set by the software at +1.60V, suitable for TTL logic. Threshold voltage accuracy is ±0.05V.

The comparator **LE** (Latch Enable) input, U1B-13, is grounded. Under this condition, if LE-, U1B-12, is held negative (below -100 mV), the comparator outputs would be latched in their existing logic states. The latched mode is not used in this application. In the transition region between latched and unlatched modes, there is a small hysteresis range for LE-. This feature is used and is described below.

When the input hysteresis has been keyboard-specified as ON, a nominal voltage of +1.7V is sent to the probe. This signal (**HYST**) appears at connector pin J6-34. This voltage is divided down by R6 and R8 to a nominal +45 mV at the LE- input, U1B-12. There it produces a hysteresis of 67 mV at the probe input (because of the 3:1 input divider, R1-R2). When the input hysteresis function has been keyboard-specified as OFF, signal HYST becomes -5.1V. This divides down to -134 mV at LE- and puts the comparator in the non-hysteresis non-latch mode. The signal HYST is received from the Control Port on the Timing Memory Board via connector S2-15 (sheet 1, TMB).

Comparators will oscillate if threshold input signals have longer rise or fall times than the propagation time of the comparators (8 nanoseconds in this case). However, in this circuit such oscillations are prevented if the hysteresis function is in effect. It is recommended that hysteresis be used normally. The exception would be an application requiring an investigation of the transition region. Accordingly, the default hysteresis condition is ON.

The comparator provides a differential output at ECL levels. The output signals, D0+ and D0-, are fed through pins J6-33, 32 to the Timing Memory Board at pins S2-52, 53 (sheet 3, TMB). The outputs of U1B are open emitters. The necessary pull-down resistors on the Timing Memory Board provide a 60 ohm termination for each of the signal lines. Both polarities of the data signals are needed by the glitch detecting circuitry on the Timing Memory Board. But the positive signal alone is used when the sample mode, rather than the glitch capture mode, has been keyboard-selected.

The clock channel output signals, CLK+ and CLK-, are fed via J6-3, 2 to Clock Control on the Timing Control Board at S2-56, 55. They may be keyboard-selected as the operating clock (refer to the TCB schematic sheet 8). The clock qualifier output signals, **QCLK+** and **QCLK-** , are fed via J6-9, 8 to Clock Control on the Timing Control Board at S2-58, 57. These signals may be used as a clock qualifier if the probe-based clock has been selected as an operating clock. Both polarities of the clock and the clock-qualifier signals are needed by the logic in the Clock Control circuits.

18.3.3 Application

The following comments pertain to the internal operation of the Probe-Analyzer system. They are not intended as a discussion of the extensive uses of the instrument in analyzing a target system. Refer to the Operator's Manual for more information on uses of the Model 800 Series.

The Model 80 probe is designed for use in both synchronous and asynchronous (state and timing) analysis. The discussion will cover both types of analysis.

Essentially, the only difference is in the use of the clock and the clock qualifier inputs.

In the timing analysis mode, the clock will probably be selected as internal source. The probe clock and the clock-qualifier will not be connected to the system under test. Any signal at the clock-qualifier input has no effect when an internal clock is being used.

In the mode where an external synchronous clock is used (high speed 16-bit "state" analysis), the probe clock input will be connected to the external source (either synchronous or not synchronous) to the target system. The clock-qualifier input may be connected if qualification of the clock signal is desired.

18.4 MODEL 81A PROBE

The Model 81A Probe is used for input to the Model 800 C, D & E Timing analyzer section. Refer to schematic **166-031501**, board layout and parts list at the end of this manual. For each pair of the 10 input channels, the Model 81A Probe contains a custom hybrid integrated circuit (U1-U5). The schematic pairs the channels as 0-1, 2-3, 4-5, 6-7, and QClk-Ext.Clk. The circuits of all channels are identical. Hybrid replacement should be done only in an environment where necessary precautions against static electricity have been taken: grounded wrist straps, conductive floor mats etc.

18.4.1 Hybrid Integrated Circuits

There are 10 channels to the Model 81A probe with two inputs for each channel. The non-inverting signal input is the incoming voltages while the inverting signal input is the reference from the Timing Memory Board D/A converters. There is a circuit for each of the eight data inputs, one for the clock input and one for the clock-qualifier input. Because all are identical, only channel 0 will be described. That description can be applied to all others.

The hybrid consists of FET-input buffers, transient protection and voltage stabilization circuitry, and ECL line drivers. External to the chip are various capacitors and resistors. The major functions of the hybrid are to provide signal isolation, high input impedance and line driving capability for signal transmission to the Timing Memory Board.

The impedance presented to the incoming signal is essentially determined by that of the matched pair of J-FET's and associated stray capacitance inside of the hybrid. The high input impedance of FET's dictates that the probe ground be connected before the signal inputs as static charges can easily rupture the gate structures. This input impedance is nominally 1 Megohm shunted by 6 pF.

There are internal spark-gaps to provide limited static protection against input transients.

The hybrid converts a variety of logic-signal inputs into outputs with pre-established ECL levels and fast transition times to provide the analyzer with complementary ECL levels.

The positive input, U5-14, comes directly from the system under test. The negative input, U5-12, combines DC feedback from the outputs yet is AC\coupled from the inputs by C19. Resistors R33 and R34 provide ground fault protection for the probe-analyzer combination. The voltage Vth1 and Vth2 (threshold) is compared to the incoming signal. Thresholds are received, via connector pin P1-5, from a D/A converter on the Timing Memory Board (sheet 4, Model 800 C, D & E TMB schematic). They are keyboard-specified (in groups of four data channels and separately for the clock/qualifier inputs) over a range of -6.4V to +6.35 V in 0.05V steps. The default value is set by the software at +1.60 V, suitable for TTL logic. There are two fixed presets: for TTL and for ECL logic. Threshold voltage accuracy is ±0.05V.

The hybrid is provided with hysteresis that is not defeatable. The outputs of hybrid are open emitters and the necessary termination resistors are on the Timing Memory Board. Both polarities of the data signals are needed by the glitch detecting circuitry located on the Timing Memory Board. As on the 100 MHz systems, the positive signal alone is used when the sample mode, rather than the glitch capture mode, has been keyboard-selected.

The clock channel output signals, EXTCLK+ and EXTCLK-, are fed via P1-3, 2 to Clock Control on the Timing Control Board (sheet 5) at S2-56, 55. They may be keyboard-selected as the operating clock (refer to the TCB schematic). The clock qualifier output signals, QCLK+ and QCLK-, are fed via P1-9, P1-8 to Clock Control on the Timing Control Board at S2-58, 57. These signals may be used as a clock qualifier if the probe clock has been selected as an operating clock.

They may also be applied to the ARM word recognizer. They then function as an ARM edge qualifier (level or edge selectable). This input is used in place of the clock qualifier, as it is the same physical input channel. Both polarities of the clock and the clock-qualifier signals are needed by the logic in the Clock Control circuits.

18.4.2 Application

The following comments pertain to the internal operation of the Probe-Analyzer system. They are not intended as a discussion of the extensive uses of the instrument in analyzing a target system. Refer to the Operator's Manual for more information on the many uses of the Model 800 Series. The Model 81A probe is designed for use in both high performance synchronous and asynchronous (state and timing) analysis. The discussion will cover both types of analysis. Essentially, the only difference is in the use of the clock and the clock qualifier inputs.

In the timing analysis mode, the clock will probably be selected as internal source. The probe clock and the clock-qualifier will not be connected to the system under test. Any signal at the clock-qualifier input has no effect when an internal clock is being used.

In the mode where an external synchronous clock is used (high speed 16-bit "state" analysis), the probe clock input will be connected to the external source (either synchronous or not synchronous) to the target system. The clock-qualifier input may be connected if qualification of the clock signal is desired. On the Model 800 C, D & E Timing analyzers the qualifier signal can be applied to the ARM word recognizer. It is then called an edge qualifier and is used in place of the the clock qualifier, as it is the same physical input channel.

18.5 MODEL 90 PROBE

The Model 90 Probe interfaces the Counter-Timer / Signature Analyzer or the Waveform Recorder to the system under test. It is a high-quality oscilloscope probe selected for suitability to this application.

The following accessories are supplied as standard equipment:
a. Insulating Tip
b. Spring Hook
c. IC Adapter
d. BNC Adapter

Model 90 Probe Specifications

Bandwidth:	DC to 10 MHz
Input Capacity:	70 pF
Working Voltage:	600 Vdc, Peak
Input Resistance:	1 Megohm

SECTION 19: SERIES 800 MOTHERBOARD CONNECTIONS

19.1 Introduction ——— 19-1

A. Series 800 Motherboard Connections ——— 19-2
- Interboard Signals. S1 Connections ——— 19-2
- S2 and Power Connections ——— 19-4
- Circuit Connections ——— 19-13

B. Model 800 D 25 MHz State S2 Bus Connections ——— 19-15

19.1 INTRODUCTION

This section contains the motherboard connector allocations. Different cards are differently keyed and cannot be fully inserted into incorrect slots.

The connectors on the motherboard are denoted from the front to rear as A through K. The plug-in PC boards associated with these connectors are as follows.

A.	Processor		
B.	RAM/Disk		
C.	State Control Board	(SCB)	
D.	State Memory Board	(SMB)	Least significant (Probe C)
E.	State Memory Board	(SMB)	Most significant (Probe A)
F.	State Memory Board	(SMB)	(Probe B)
G.	Timing Control Board	(TCB)	
H.	Timing Memory Board	(TMB)	
I.	Timing Memory Board	(TMB)	
J.	Waveform Recorder		
K.	Counter-Timer/Signature Analyzer	(CTSA)	

NOTE: Connector J12 is the Daughter Board bearing the probe connectors.

NOTE: The signal lists on pages 19-2 through 19-13 apply to all Series 800 Logic Analyzers. Additional signals for the Model 800 D Logic Analyzer are on pages 19-14 and 19-15.

INTERBOARD SIGNALS. S1 CONNECTIONS (Less Power & Ground)		
Signal Name	**Pin**	**Board**
ALE	50	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A00	55	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A01	24	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A02	58	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A03	28	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A04	23	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A05	25	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A06	56	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A07	57	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A08	52	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A09	53	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A10	54	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
A11	27	S1A, S1B, S1C, S1D, S1E, S1G, S1H, S1J, S1K, U7-9
A12	26	S1A, S1B, S1G, S1H, S1I, S1J, S1K
A13	44	S1A, S1B, S1G, S1J, S1K, U7-11
A14	14	S1A, S1B, S1G, S1H, S1I, S1J, S1K
A15	45	S1A, S1B, S1G, S1K U7-11
A13-	44	S1C, S1D, S1E, S1F, S1H, S1I, U7-10, RP3-6
A11-	27	S1F, S1I, U7-8, RP3-8
A15-	45	S1C, S1D, S1E, S1F, S1H, S1I, S1J, S1K
A14-	14	S1C, S1D, S1E, S1F,
A12-	26	S1C, S1D, S1E, S1F,
CLK	11	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
DB0	48	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-3
DB1	49	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-18
DB2	19	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-14
DB3	17	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-13
DB4	18	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-8
DB5	20	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-7
DB6	51	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-4
DB7	21	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U1-17
DBEN+	22	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
HLDA	7	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
HOLD	39	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K

INTERBOARD SIGNALS. S1 CONNECTIONS (Less Power and Ground)		
Signal Name	**Pin**	**Board**
INTA-	37	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
INTR	13	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
IOEN-	8	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
IO/M-	15	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
RDY	38	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
RD-	59	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
RST	10	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
RST5.5	43	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
RST6.5	12	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
RST7.5	42	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
RW	9	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
SID	40	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, C6, RP3-2, U7-1, J12-49
SOD	16	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
S0	46	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
S1	47	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
TRAP-	41	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, J1-3
WR-	29	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K, U4-5
SPARE	34	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K
SPARE	4	S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H, S1I, S1J, S1K

S2 and POWER CONNECTIONS	
Signal Name	**Board and Pin Connections**
ARM-	S2F-9, S2G-38, R7, S2K-9, S2D-9
ARM+	S2D-20, S2E-20, S2F-20, U3-5,6
ARMOUT-	U3-4, J10-5, RP1-4
CLKINH+	S2C-38, S2D-7, S2E-7, S2F-7
CLKSEL2+	U1-2, U4-1, U2-3
CLKSEL2-	U4-2, U2-11, U2-4
CLKSEL3-	U4-4, U2-13
CLKSEL3+	U1-19, U4-3, U2-6
DQ1+	S2C-3, S2D-3, S2E-3, S2F-3
DQ2	S2C-33, S2D-33, S2E-33, S2F-33
EXT	S2D-12, S2E-12, S2F-12, S2G-12, J10-11
EXT1+	U4-10, U3-9
EXT1-	S2A-49, U4-11
FS	S2C-42, U3-3
GND	J2-(4,10) J3-(12,14,16,18,20,22,23,24) J10-(2,4,6,8,) J1-(1,2) J10(10,12,14,16) S1A-(1,30,31,60), S1C-(1,30,31,60), S1D-(1,30,31,60) S1E-(1,30,31,60), S1F-(1,30,31,60), S1K-1,30,31,50) S2A-(1,19,30,31,60) S2C-(1,30,31,60), S2D-(1,30,31,34,35,36,38,60) S2E-(1,15,30,31,34,35,36,37,38,60) S2F-(1,15,30,31,34,35,36,37,38,60) S1B-(1,30,31,60) S1G-(1,30,31,60) S1H-(1,30,31,60) S1I-(1,30,31,60) S1J-(1,30,31,60) S2G-(1,30,31,60) S2B-(1,30,31,60) S2H-(1,30,31,35,36,60) S2I-(1,30,31,35,36,60) S2J-(1,28,30,31,58,59,60) S2K-(1,30,31,36,40,60) S2K-29 SPK

S2 and POWER CONNECTIONS	
Signal Name	**Board and Pin Connections**
GND	U1-(1,10) U10-(1,16), U11,16 U7-7, U9-(7,14) U6-(2,3,7,9,10) U2-(7,9,10), U3-7, U4-7, U5-7 R3, R5 J4-(1,7) J12-(1,2,36,72,35,107,108) C2,C3, C4, C5, C6, C7, C8, C9
LINK	S2D-11, S1E-11, S2F-11, J10-3, RP1-2, U3-1, U5-(4,11,12,10)
RA0	S2C-16, S2D-46, S2E-46, S2F-46
RA1	S2C-15, S2D-45, S2E-45, S2F-45
RA2	S2C-14, S2D-44, S2E-44, S2F-44
RA3	S2C-13, S2D-43, S2E-43, S2F-43
RA4	S2C-12, S2D-42, S2E-42, S2F-42
RA5	S2C-11, S2D-41, S2E-41, S2F-41
RA6	S2C-10, S2D-40, S2E-40, S2F-40
RA7	S2C-9, S2D-39, S2E-39, S2F-39
RA8	S2D-13, S2E-13, S2F-13, S2C-28
RA9	S2D-32, S2E-32, S2F-32, S2C-29
MAIN/AUX-	S2D-8, S2E-8, S2F-8, S2C-2
LINK-	RP1-8, S2G-42, S2A-5, U5-13
RDYOUT-	S2A-7 U5-(5,6)
RESTART	S2F-17 S2E-17, S2D-17, S2C-47
SADATAIN	S2K-41, J10-7
TRIG+	S2C-45, S2D-16, S2E-16, S2F-16
TRIGE-	S2F-10 S2G-10, S2K-10, R8, S2D-10
TRIGOUT-	U11-5, J10-1
TSA0	S2C-20, S2D-50, S2E-50, S2F-50
TSA1	S2C-19, S2D-49, S2E-49, S2F-49
TSA2	S2C-18, S2D-48, S2E-48, S2F-48
TSA3	S2C-17, S2D-47, S2E-47, S2F-47
WR+	U4-6, U3-8
WR1-	U3-10 U1-11, RP1-5

S2 and POWER CONNECTIONS	
Signal Name	**Board and Pin Connections**
+15	S2A-(2,32), S2B-(2,32), S2K-(2,32), J2-4 S2H-2, S2H-32 S2I-2, S2I-32, S2J-2, S2J-32 R1 S1G-2, S2G-32, (optional)
+5	C2, C3 C4, C5, C7, C9 J2-(1,2) S1B-(5,6,35,36), S1C-(5,6,35,36), S1D-(5,6,35,36) S1E-(5,6,35,36), S1F-(5,6,35,36), S1K-(5,6,35,36) RP1-1, RP2-1, RP3-1 U1-20, U2-(1,14), U3-14, U4-14, U5-14, U6-(1,14), U7-14 U11-8, J12-(141,142) S1G-(5,6,35,36) S1H-(5,6,35,36) S1I-(5,6,35,36) S1J-(5,6,35,36) S1A-(5,6,35,36) CR1-
+12	S2H-44, S2I-44, J12-24, J12-48
-12	S2I-13, S2H-13, J12,26, J12-4
-15	S2B-(3,33), S2A-(3,33), J2-9 S2H-3, S2H-33, S2I-3, S2I-33 S2J-3, S2J-33, S2K-3, S2K-33 (S2G-3, S2G-33 optional)
-5.2	J2-(5,6), C8 S1A-(2,3,32,33) S1B-(2,3,32,33), S1C-(2,3,32,33), S1D-(2,3,32,33) S1E-(2,3,32,33), S1F-(2,3,32,33), S1K-(2,3,32,33) S1J-2, S1J-3, S1J-32, S1J-33 S1I-2, S1I-3, S1I-32, S1I-33 S1G-2, S1G-3, S1G-32, S1G-33 S1H-2, S1H-3, S1H-32, S1H-33 U10-8, U11-8 R6, R7, R8, R4 R2 J12-(143,144)

S2 and POWER CONNECTIONS			
Signal Name	**Board and Pin Connections**		
232TXD	S2B-5,	J4-3	
232DCD	J4-8,	S2B-36	
232DSR	S2B-6,	J4-4	
232DTR	J4-20,	S2B-35	
232DSR	J4-6,	S2B-7	
232RXD	J4-2,	S2B-38	
232CTS	J4-5,	S2B-37	
488ATN	J3-21,	S2A-29	
488DAV	J3-11,	S2A-28	
488D1	J3-1,	S2A-42	
488D2	J3-3,	S2A-11	
488D3	J3-5,	S2A-41	
488D4	J3-7,	S2A-10	
488D5	J3-2,	S2A-40	
488D6	J3-4,	S2A-9	
488D7	J3-6,	S2A-39	
488D8	J3-8,	S2A-38	
488EOI	J3-9,	S2A-58	
488IFC	S2A-(5,6),	J3-17	
488NDAC	J3-15,	S2A-27	
488NRFD	J3-13,	S2A-57	
488REN	S2A-26	J3-10	
488SRQ	J3-19	S2A-59	
ACLKSEL	S2C-24,	J12-121	
ACQ1	S2E-19,	U6-12,	RP2-6
ACQ2	S2E-18,	U6-5,	RP2-5
ACTL	S2C-27,	J12-119	
AD0	S2E-56,	J12-89	
AD1	S2E-54,	J12-91	
AD2	S2E-55,	J12-90	
AD3	S2E-29,	J12-84	
AD4	S2E-53,	J12-92	
AD5	S2E-57,	J12-88	
AD6	S2E-52,	J12-93	
AD7	S2E-51,	J12-94	
AD8	S2E-58,	J12-87	
AD9	S2E-59,	J12-86	
AD10	S2E-28,	J12-85	
AD11	S2E-27,	J12-83	
AD12	S2E-26,	J12-82	
AD13	S2E-23,	J12-79	
AD14	S2E-24,	J12-80	
AD15	S2E-25,	J12-81	

S2 and POWER CONNECTIONS	
Signal Name	**Board and Pin Connections**
ALATCHCLK	S2C-4, S2E-4
APROBCLK	S2C-23, J12-122, U2-12
APROBDREN-	S2C-43, S2E-14
AQCLKSEL	S2C-26, J12-120
AQ1 (C)	S2C-25, S2E-21, J12-77
AQ2 (T)	S2E-22, J12-78
BPBSNS+	J12-127, U7-2
BCLKSEL	S2C-56, J12-124
BCQ1	S2F-19, U6-11, RP2-8
BCQ2	S2F-18, U6-6, RP2-7
BCTL	S2C-53, J12-126
BD0	S2F-56, J12-69
BD1	S2F-54, J12-74
BD2	S2F-55, J12-70
BD3	S2F-29, J12-62
BD4	S2F-53, J12-65
BD5	S2F-57, J12-68
BD6	S2F-52, J12-64
BD7	S2F-51, J12-63
BD8	S2F-58, J12-67
BD9	S2F-59, J12-66
BD10	S2F-28, J12-61
BD11	S2F-27, J12-60
BD12	S2F-26, J12-59
BD13	S2F-23, J12-56
BD14	S2F-24, J12-57
BD15	S2F-25, J12-58
BLATCHCLK	S2C-34, S2F-4
BPROBCLK	S2C-57, U2-5, J12-123
BPROBDREN-	S2C-44, S2F-14
BQCLKSEL	S2C-54, J12-125
BQ1 (C)	S2C-55, S2F-21, J12-54
BQ2 (T)	S2F-22, J12-55

S2 and POWER CONNECTIONS	
Signal Name	**Board and Pin Connections**
CCLKQUALIN-	S2D-37, U6-8
CCLKSEL	J12-117, U1-5
CCQ1	S2D-19, U6-13, RP2-4
CCQ2	S2D-18, U6-4, RP2-3
CCTL	J12-116, U1-15
CD0	S2D-56, J12-109
CD1	S2D-54, J12-111
CD2	S2D-55, J12-110
CD3	S2D-29, J12-100
CD4	S2D-53, J12-112
CD5	S2D-57, J12-106
CD6	S2D-52, J12-113
CD7	S2D-51, J12-114
CD8	S2D-58, J12-105
CD9	S2D-59, J12-104
CD10	S2D-28, J12-101
CD11	S2D-27, J12-102
CD12	S2D-26, J12-103
CD13	S2D-23, J12-97
CD14	S2D-24, J12-98
CD15	S2D-25, J12-99
CLATCHCLK	U2-8, S2D-4
CPROBCLK	J12-118, U2-2
CPROBDREN-	S2D-14, U1-16
CQCLKSEL	J12-115, U1-9
CQ1 (C)	S2D-21, J12-95, U3-(11,12)
CQ1-	RP1-3, U3-13 (optional)
CQ2 (T)	S2D-22, J12-96
CTAPCLK-	S2D-6, S2C-37
CWE+	S2D-5, S2C-35, S2K-35

S2 and POWER CONNECTIONS	
Signal Name	**Board and Pin Connections**
AT-	S2H-7, S2G-7 S2I-7
ACH0+	S2H-52, J12-44
ACH0-	S2H-53, J12-43
ACH1+	S2H-54, J12-42
ACH1-	S2H-55, J12-41
ACH2+	S2H-56, J12-40
ACH2-	S2H-57, J12-39
ACH3+	S2H-58, J12-38
ACH3-	S2H-59, J12-37
ACH4+	S2H-29, J12-34
ACH4-	S2H-28, J12-33
ACH5+	S2H-27, J12-32
ACH5-	S2H-26, J12-31
ACH6+	S2H-25, J12-30
ACH6-	S2H-24, J12-29
ACH7+	S2H-23, J12-28
ACH7-	S2H-22, J12-27
ACLK+	S2G-56, J12-51
ACLK-	S2G-55, J12-50
ACT	S2H-6, S2G-6, S2J-6, S2K-6, S2C-36, U8-1, U10-5, R6, R5
ACLKTTL	S2H-43, J12-43
HYSTERYSIS A	S2H-15, J12-46
A THRESHOLD A	S2H-14, J12-45
A THRESHOLD B	S2H-45, J12-47
AQCLK+	S2G-58, J12-53
AQCLK-	S2G-57, J12-52

S2 and POWER CONNECTIONS				
Signal Name	**Board and Pin Connections**			
BCH0+	S2I-52,	J12-23		
BCH0-	S2I-53,	J12-22		
BCH1+	S2I-54,	J12-21		
BCH1-	S2I-55,	J12-20		
BCH2+	S2I-56,	J12-16		
BCH2-	S2I-57,	J12-17		
BCH3+	S2I-58,	J12-18		
BCH3-	S2I-59,	J12-19		
BCH4+	S2I-29,	J12-15		
BCH4-	S2I-28,	J12-14		
BCH5+	S2I-27,	J12-13		
BCH5-	S2I-26,	J12-12		
BCH6+	S2I-25,	J12-11		
BCH6-	S2I-24,	J12-10		
BCH7+	S2I-23,	J12-9		
BCH7-	S2I-22,	J12-8		
100 MHz	S2A-35,	U7-5		
FT+	S2G-11,	U5-8		
BCT	S2I-6,	U7-13,	U8-14,	U10-13
BCLKTTL	S2I-43,	U11-4		
HYSTERYSIS A	S2I-15,	J12-7		
B THRESHOLD A	S2I-14,	J12-5		
B THRESHOLD B	S2I-45,	J12-6		

S2 and POWER CONNECTIONS	
Signal Name	**Board and Pin Connections**
TT-	S2H-8, S2G-8, S2I-8, U11-7
WD0	S2H-21, S2J-21
WD1	S2H-51, S2J-51
WD2	S2H-20, S2J-20
WD3	S2H-50, S2J-50
WD4	S2H-19, S2J-19
WD5	S2H-49, S2J-49
WD6	S2H-18, S2J-18
WD7	S2H-48, S2J-48
WFIN	S2J-29, J10-13
WTRIG	S2G-40, S2J-40
-T/S	No Connection on S2K-28
KD6	S2A-17, J1-6
KD6	S2A-47, J1-7
KD4	S2A-16, J1-8
KD3	S2A-46, J1-9
KD2	S2A-15, J1-10
KD1	S2A-45, J1-11
KD0	S2A-14, J1-12
DAAP	S2A-44, J1-4
STRB	S2A-48, J1-13
BEEP+	S2A-6, U7-3
REBOOT	S2A-51, J1-3

CIRCUIT CONNECTIONS				
1.	U2-11,	U2-4		
2.	U4-10,	U3-9		
3.	U4-6,	U3-8		
4.	U3-10,	U1-11,	RP1-5	
5.	U9-1,	U10-15		
6.	U1-2,	U4-1		
7.	U1-19,	U4-3		
8.	U11-1,	U11-6		
9.	U9-6,	U4-3		
10.	U1-6,	U3-2		
11.	U1-12,	U5-9		
12.	C1+,	R1-2		
13.	U7-4,	R1-1		
14.	U11-2,	U11-1		
15.	U10-2,	U8-8		
16.	U10-12,	U10-9,	U10-11,	U10-4
17.	U10-5,	R6,	R5	
18.	U7-2,	J12-127		

Signal Name	Board and Pin Connections
ACLKSEL	S2C-24, J12-121
ACTL	S2C-27, J12-119
ADQ	S2E-22, J12-78
A(ECL)	S2D-9, S2F-9, S2G-38, S2K-9, R7
ALCLK	S2C-4, S2E-4
APD15	S2E-25, J12-81
APD14	S2E-24, J12-80
APD13	S2E-23, J12-79
APD12	S2E-26, J12-82
APD11	S2E-27, J12-83
APD10	S2E-28, J12-85
APD9	S2E-59, J12-86
APD8	S2E-58, J12-87
APD7	S2E-51, J12-94
APD6	S2E-52, J12-93
APD5	S2E-57, J12-88
APD4	S2E-53, J12-92
APD3	S2E-29, J12-84
APD2	S2E-55, J12-90
APD1	S2E-54, J12-91
APD0	S2E-56, J12-89
APROBCLK	S2E-23, J12-122
APROBDREN-	S2C-43, S2E-14
AQ	S2C-25, J12-77
AQCLKSEL	S2C-26, J12-120
ARM	S2D-20, S2E-20, S2F-20, U3-(5,6)
BCLKSEL	S2C-34, J12-124
BDQ	S2F-22, J12-55
BLCLK	S2C-34, S2F-4
BPD15	S2F-25, J12-58
BPD14	S2F-24, J12-57
BPD13	S2F-23, J12-56
BPD12	S2F-26, J12-59
BPD11	S2F-27, J12-60
BPD10	S2F-28, J12-61
BPD9	S2F-59, J12-66
BPD8	S2F-58, J12-67
BPD7	S2F-51, J12-63
BPD6	S2F-52, J12-64
BPD5	S2F-57, J12-68
BPD4	S2F-53, J12-65
BPD3	S2F-29, J12-62
BPD2	S2F-55, J12-70
BPD1	S2F-54, J12-74
BPD0	S2F-56, J12-69
BPROBCLK	S2C-57, J12-123
BPROBDREN-	S2C-44, S2F-14
BQ	S2C-55, J12-54
BQCLKSEL	S2C-54, J12-125
CCLK	S2C-35, S2K-35

Signal Name	Board and Pin Connections
CCLKSEL	U1-5, J12-117
CCTL	U1-15, J12-116
CDQ	S2D-22, J12-96
CLCLK	S2C-6, S2D-4 (jumper on Motherboard, remove U2)
CPD15	S2D-25, J12-99
CPD14	S2D-24, J12-98
CPD13	S2D-23, J12-97
CPD12	S2D-26, J12-103
CPD11	S2D-27, J12-102
CPD10	S2D-28, J12-101
CPD9	S2D-59, J12-104
CPD8	S2D-58, J12-105
CPD7	S2D-51, J12-114
CPD6	S2D-52, J12-113
CPD5	S2D-57, J12-106
CPD4	S2D-53, J12-112
CPD3	S2D-29, J12-100
CPD2	S2D-55, J12-110
CPD1	S2D-54, J12-111
CPD0	S2D-56, J12-109
CPROBCLK	S2C-41, U2-2, J12-118 (jumper on Motherboard)
CPROBDREN-CT	S2D-14, U1-16 S2C-36, S2G-6, S2H-6, S2J-6, S2K-6, U8-1, U10-15, R5, R6
CQ	S2C-40, S2D-21, J12-95, U3-(11,12) (jumper on Motherboard)
CQCLKSEL	U1-9, J12-115
EXT	S2D-12, S2E-12, S2F-12, S2G-12, J10-11
FT	S2D-11, S2E-11, S2F-11, J10-3, RP1-2, U3-1, U5-(4,10,11,12)
LINK	S2C-42, U3-3
MAIN/AUX-	S2C-2, S2D-8, S2E-8, S2F-8
MCLK	S2C-38, S2D-7, S2E-7, S2F-7
RA9	S2C-29, S2D-32, S2E-32, S2F-32
RA8	S2C-28, S2D-13, S2E-13, S2F-13
RA7	S2C-9, S2D-39, S2E-39, S2F-39
RA6	S2C-10, S2D-40, S2E-40, S2F-40
RA5	S2C-11, S2D-41, S2E-41, S2F-41
RA4	S2C-12, S2D-42, S2E-42, S2F-42
RA3	S2C-13, S2D-43, S2E-43, S2F-43
RA2	S2C-14, S2D-44, S2E-44, S2F-44
RA1	S2C-15, S2D-45, S2E-45, S2F-45
RA0	S2C-16, S2D-46, S2E-46, S2F-46
T(ECL)	S2D-10, S2F-10, S2G-10, S2K-10, R8
WR5	S2C-37, S2D-6
WR4	S2C-17, S2D-47, S2C-47, S2F-47
WR3	S2C-18, S2D-48, S2E-48, S2F-48
WR2	S2C-19, S2D-49, S2E-49, S2F-49
WR1	S2C-20, S2D-50, S2E-50, S2F-50
WE-	S2C-3, S2D-3, S2E-3, S2F-3
GND	S2C-(1,30,32,60) and S2D-(1,30,31,34,35,36,38,60) and S2E-(1,15,30,31,34,35,36,37,38,60) and S2F-(1,15,30,31,34,35,36,37,38,60)

SECTION 20: GOSSARY

20.1 Introduction ——— 20-1

20.1 INTRODUCTION

Certain words within the body text of an explanation are emphasized. These words are explained elsewhere in the glossary.

A/D	Analog-to-Digital (converter)
ASCII	American Standard Code for Information Interchange.
BNC	A designation for a type of coaxial connector. Used by many manufacturers.
Boolean	A type of binary algebra used in logic design.
CMOS	Complementary Metal Oxide Silicon; a family of ICs named after the manufacturing technology.
CRT	Cathode Ray Tube.
CRTC	CRT Controller; a special purpose LSI circuit.
D/A	Digital-to-Analog (converter).
DMA	Direct Memory Access; memory access that is not under supervisioon of the controlling microprocessor.
ECL	Emitter-Coupled Logic; a family of high-speed, digital logic ICs.
EPROM	Erasable Programmable ROM can be erased with ultraviolet light and reprogrammed.
FET	Field-Effect Transistor.
Glitch	A transient logic level transition of shorter duration thatn a sampling clock.
GPIB	General Purpose Interface Bus. A bus that meets specification IEEE-488.
HEX or H	Hexadecimal; when placed after a number (that may include alpha characters A-F), indicates that the number is in base-16 notation.
IEEE-488	An institute of Electrical and Electronics Engineers standard digital parallel interface for programmable instrumentation (the full name of the standard is ANSI/IEEE Std 488-1975).
K	A unit mulitplier meaning x 1000 (x 1024 actually).
LED	Light Emitting Diode.
LSI	Large Scale Integrated circuit.

Mains	The public utility AC power lines.
MMI	Monolithic Memories, Inc. A manufacturer of IC devices.
OC	Open Collector, a type of IC circuit design.
Op-Amp	Operational Amplifier; usually a linear IC.
PC	Printed Circuit.
PCB	Printed Circuit Board.
Pin-out	A list of device pins (connector, IC, relay, etc.).
PROM	Programmable ROM.
RAM	Random Access Memory; implies both read and write capabilites.
ROM	Read-Only-Memory. Type of memory that can be read from but not written into; programmed during manufacturing.
RS-232C	An Electronic Industries Association standard for a data communication interface.
SIP	Single In-Line Package; the term is related to DIP (Dual In-Line Package).
TTL	Transistor-Transistor Logic; a family of general purpose, digital ICs.
USART	Universal Synchronous/Asynchronous Receiver-Transitter; an LSI communications device.

22.1 PARTS LIST INDEX

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M51A PROBE

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-001502	PCB/M51A	1.000/+0
1	134-824500	IC/3430/3651 QUAD COMPARATORS	5.000/+0
1	134-707503	IC/7486N 2-XOR	4.000/+0
1	134-716009	IC/74S86	1.000/+0
1	015-/22900	PIN/SOLDER TERMINAL 120-1032-	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	12.000/+0
1	023-740200	CAP 100PF 1KV 10% TANT	1.000/+0
1	023-745700	CAP 8.2PF 1KV 10%	19.000/+0
1	024-820700	CON 40F HDR/SOL D/RA	1.000/+0
1	026-/19200	POT 200 PCB .5W	1.000/+0
1	100-711200	RES NET/DIP 22K 16PIN 8RES	2.000/+0
1	100-711300	RES NET/SIP 22K 10PIN 9RES	2.000/+0
1	201-121000	RES 121 01% 1/8W	1.000/+0
1	201-200100	RES 2K 01% 1/8W PRE	1.000/+0
1	201-200200	RES 20K 01% 1/8W PRE	1.000/+0
1	201-221200	RES 22.1K 01% 1/8W	3.000/+0
1	201-332200	RES 33.2K 01% 1/8W	1.000/+0
1	201-475000	RES 475 01% 1/8W	1.000/+0
1	201-681000	RES 681 01% 1/8W PRE	1.000/+0
1	201-681900	RES 68.1 01% 1/8W PRE	2.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	4.000/+0
1	025-756000	SW/SL 2P2T GF-126-0211 CW	2.000/+0
1	085-000101	CBL/MODEL 50/51 PROBE	1.000/+0

BASIC WAVEFORM BOARD

LEVEL	PART NUMBER	DESCRIPTION					QUANTITY
1	134-738403	IC/10125F ECL TRANSLATOR					1.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR					3.000/+0
1	134-740003	IC/74S08 2-NAND					1.000/+0
1	134-740200	IC/TL084 QUAD OP AMP					1.000/+0
1	134-743403	IC/74LS85 COMPARATOR					4.000/+0
1	134-745409	IC/74S64					1.000/+0
1	134-747103	IC/74LS161 4 BIT COUNTER					2.000/+0
1	134-773400	IC/10102L ECL GATE					1.000/+0
1	134-821600	IC/74S11 3-AND					1.000/+0
1	134-822300	IC/74S139 2TO4 DECODER					1.000/+0
1	134-830300	IC/LH0024C OP-AMP HIGH SLEW					1.000/+0
1	134-830500	IC/6080 8BIT DAC					2.000/+0
1	134-831000	IC/687 VOLTAGE COMPARATOR					1.000/+0
1	134-831700	IC/592A VIDEO AMPLIFIER					1.000/+0
1	134-836500	IC/93L422/93422 4 BIT TTL MEM					2.000/+0
1	176-401001	FIRM/6301-1 WAVEFORM U38					1.000/+0
1	201-100000	RES 100	01%	1/8W		PRE	2.000/+0
1	201-100100	RES 1K	01%	1/8W		PRE	4.000/+0
1	201-100200	RES 10K	01%	1/8W		PRE	7.000/+0
1	201-100300	RES 100K	01%	1/8W		PRE	2.000/+0
1	201-100400	RES 1M	01%	1/8W		PRE	2.000/+0
1	201-130100	RES 1.3K	01%	1/8W		PRE	2.000/+0
1	201-150100	RES 1.5K	01%	1/8W		PRE	4.000/+0
1	201-196400	RES 1.96M	01%	1/8W		PRE	1.000/+0
1	201-200200	RES 20K	01%	1/8W		PRE	1.000/+0
1	201-274000	RES 274	01%	1/8W		PRE	2.000/+0
1	201-332000	RES 332	01%	1/8W		PRE	2.000/+0
1	201-432900	RES 43.2	01%	1/8W		PRE	1.000/+0
1	201-475100	RES 4.75K	01%	1/8W		PRE	1.000/+0
1	201-475300	RES 475K	01%	1/8W		PRE	1.000/+0
1	201-475900	RES 47.5	01%	1/8W		PRE	1.000/+0
1	201-562900	RES 56.2	01%	1/8W		PRE	1.000/+0
1	201-649000	RES 649	01%	1/8W		PRE	4.000/+0
1	201-681000	RES 681	01%	1/8W		PRE	3.000/+0
1	201-681900	RES 68.1	01%	1/8W		PRE	1.000/+0
1	201-825900	RES 82.5	01%	1/8W		PRE	2.000/+0
1	201-909000	RES 909	01%	1/8W		PRE	2.000/+0
1	201-909300	RES 909K	01%	1/8W		PRE	1.000/+0
1	615-929400	WAVEFORM BD MOD BD(PAL=5)					1.000/+0
*2	000-929400	PCB/WAVEFORM MOD BD (PAL=5)				Y	1.000/+0
*2	023-707500	CAP 6.8MF 35V 10% TANT G					2.000/+0
*2	023-722300	CAP .047MF 50V CERM G					3.000/+0
*2	024-714700	CON 1M HDR/SOL					19.000/+0
*2	100-703500	RES NET/SIP 680 10PN 9RE					1.000/+0
*2	134-738203	IC/F10176F ECL					2.000/+0
*2	134-820100	IC/SDA6020 6BIT ADC 50MHZ SI					1.000/+0
*2	134-830700	IC/21185 DELAY LINE 50NSEC					1.000/+0
*2	134-831500	IC/10116 LINE RECEIVER					1.000/+0
*2	201-137000	RES 137	01%	1/8W		PRE	2.000/+0
*2	201-162000	RES 162	01%	1/8W			2.000/+0
*2	201-274000	RES 274	01%	1/8W		PRE	2.000/+0
*2	201-825900	RES 82.5	01%	1/8W		PRE	2.000/+0

BASIC WAVEFORM BOARD continued

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	134-738403	IC/10125F ECL TRANSLATOR	1.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	4.000/+0
1	134-740003	IC/74S08 2-NAND	1.000/+0
1	134-740200	IC/TL084 QUAD OP AMP	1.000/+0
1	134-743403	IC/74LS85 COMPARATOR	4.000/+0
1	134-745409	IC/74S64	1.000/+0
1	134-747103	IC/74LS161 4 BIT COUNTER	2.000/+0
1	134-773400	IC/10102L ECL GATE	1.000/+0
1	134-821600	IC/74S11 3-AND	1.000/+0
1	134-822300	IC/74S139 2TO4 DECODER	1.000/+0
1	134-830300	IC/LH0024C OP-AMP HIGH SLEW	1.000/+0
1	134-830500	IC/6080 8BIT DAC	2.000/+0
1	134-831000	IC/687 VOLTAGE COMPARATOR	1.000/+0
1	134-831500	IC/10116 LINE RECEIVER	1.000/+0
1	134-831700	IC/592A VIDEO AMPLIFIER	1.000/+0
1	134-835000	IC/TDC1014J 6BIT FLASH ADC	2.000/+0
1	134-836500	IC/93L422/93422 4 BIT TTL MEM	2.000/+0
1	176-401001	FIRM/6301-1 WAVEFORM U38	1.000/+0
1	201-100000	RES 100 01% 1/8W PRE	2.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	4.000/+0
1	201-100200	RES 10K 01% 1/8W PRE	7.000/+0
1	201-100300	RES 100K 01% 1/8W PRE	2.000/+0
1	201-100400	RES 1M 01% 1/8W PRE	2.000/+0
1	201-130100	RES 1.3K 01% 1/8W PRE	2.000/+0
1	201-150100	RES 1.5K 01% 1/8W PRE	4.000/+0
1	201-196400	RES 1.96M 01% 1/8W PRE	1.000/+0
1	201-200200	RES 20K 01% 1/8W PRE	1.000/+0
1	201-274000	RES 274 01% 1/8W PRE	2.000/+0
1	201-332000	RES 332 01% 1/8W PRE	2.000/+0
1	201-432900	RES 43.2 01% 1/8W PRE	1.000/+0
1	201-475100	RES 4.75K 01% 1/8W PRE	1.000/+0
1	201-475300	RES 475K 01% 1/8W PRE	1.000/+0
1	201-475900	RES 47.5 01% 1/8W PRE	1.000/+0
1	201-562900	RES 56.2 01% 1/8W PRE	1.000/+0
1	201-649000	RES 649 01% 1/8W PRE	4.000/+0
1	201-681000	RES 681 01% 1/8W PRE	3.000/+0
1	201-681900	RES 68.1 01% 1/8W PRE	1.000/+0
1	201-825900	RES 82.5 01% 1/8W PRE	2.000/+0
1	201-909000	RES 909 01% 1/8W PRE	2.000/+0
1	201-909300	RES 909K 01% 1/8W PRE	1.000/+0

CT/SA TIMING BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	022-727000	DIO LEDR 5V 555-2003 VERT DLT	1.000/+0
1	023-740600	CAP 15PF 1KV 10% TANT	1.000/+0
1	134-712803	IC/74LS00N 2-NAND	1.000/+0
1	134-719403	IC/74LS151N MULTIPLEXER	2.000/+0
1	134-720803	IC/74LS10N 3-NAND	1.000/+0
1	134-723909	IC/74LS257	2.000/+0
1	134-730903	IC/74LS367N HEX DRIVER	1.000/+0
1	134-731009	IC/74LS138	1.000/+0
1	134-732903	IC/74LS32N 2-OR	1.000/+0
1	134-732909	IC/74LS32	1.000/+0
1	134-736803	IC/74LS374N REGISTER	1.000/+0
1	134-736809	IC/74LS374	1.000/+0
1	134-738203	IC/F10176F ECL	1.000/+0
1	134-738403	IC/10125F ECL TRANSLATOR	6.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	1.000/+0
1	134-739109	IC/74LS244	1.000/+0
1	134-739803	IC/74LS148 OCTAL ENCODER	1.000/+0
1	134-749803	IC/10103F ECL-4-2 INPUT MOT	1.000/+0
1	134-792800	IC/10104F ECL 2 INPUT AND	1.000/+0
1	134-793200	IC/10141F ECL 4BIT SHIFT REG	4.000/+0
1	134-827500	IC/10135 J-K M/S FLIP-FLOP	2.000/+0
1	134-827700	IC/10138 BI-QUINARY COUNTER	1.000/+0
1	134-828100	IC/10161 1TO8 DECODER	1.000/+0
1	134-828300	IC/10164 8 LINE MULTIPLEXER	1.000/+0
1	134-830500	IC/6080 8BIT DAC	1.000/+0
1	134-830800	IC/21182 DELAY LINE 20NSEC	1.000/+0
1	134-831000	IC/687 VOLTAGE COMPARATOR	1.000/+0
1	134-831400	IC/10117 OR-AND/OR-AND INVERT	1.000/+0
1	134-831500	IC/10116 LINE RECEIVER	1.000/+0
1	134-831600	IC/10113 2-XOR	1.000/+0
1	134-834600	IC/7226B 10MHZ COUNTER SYSTEM	1.000/+0
1	201-825900	RES 82.5 01% 1/8W PRE	1.000/+0

M800 RAM/DISK BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-011201	PCB/RAM DISK	1.000/+0
1	134-711209	IC/74S74	1.000/+0
1	134-712803	IC/74LS00N 2-NAND	1.000/+0
1	134-712903	IC/74LS04N HEX INVERTER	1.000/+0
1	134-713203	IC/74LS74N FLIP-FLOP	3.000/+0
1	134-713209	IC/74LS74	3.000/+0
1	134-715303	IC/7438N O/C 2-NAND	4.000/+0
1	134-720403	IC/74LS02N 2-NOR	2.000/+0
1	134-724703	IC/7414 HEX INVERTER	2.000/+0
1	134-731009	IC/74LS138	2.000/+0
1	134-732903	IC/74LS32N 2-OR	1.000/+0
1	134-736803	IC/74LS374N REGISTER	2.000/+0
1	134-745704	IC/4116(5290-M)16K DYN RAM	24.000/+0
1	134-741803	IC/1489 QUAD LINE RECEIVER	1.000/+0
1	134-747103	IC/74LS161 4 BIT COUNTER	1.000/+0
1	134-751603	IC/74LS393 DUAL 4BIT B COUNTE	1.000/+0
1	134-762900	IC/74LS629 OSCILLATOR	1.000/+0
1	134-776503	IC/74LS01N 2-NAND OC	1.000/+0
1	134-783600	IC/74F244 OCTAL BUFFER	4.000/+0
1	134-822300	IC/74S139 2T04 DECODER	1.000/+0
1	134-824400	IC/8304 8BIT TRANSCEIVER	1.000/+0
1	134-834100	IC/2143 4PHASE CLOCK GENERATO	1.000/+0
1	134-834500	IC/9602 MONOSTABLE MULTIVIBRA	1.000/+0
1	023-700100	CAP 100PF 500V 05% MICA R	1.000/+0
1	023-706800	CAP 150PF 500V 05% MICA R	1.000/+0
1	023-711000	CAP 22MF 35V 10% TANT G	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	61.000/+0
1	023-726600	CAP 6.8MF 35V 10% TANT R	3.000/+0
1	023-728400	CAP 330PF 1KV 20% CERM R	1.000/+0
1	023-740200	CAP 100PF 1KV 10% TANT	2.000/+0
1	023-740800	CAP .01MF 25V 20% CERM	2.000/+0
1	023-743900	CAP .68MF 35V TANT A	1.000/+0
1	023-747100	CAP 22MF 16V 20% TANT DROP	6.000/+0
1	024-714700	CON 1M HDR/SOL	2.000/+0
1	024-724800	CON 40F DIP/SOL AMP	1.000/+0
1	024-730900	CON 28F DIP/SOL 641267-3 AM	1.000/+0
1	026-708600	POT 50K PCB .5W	1.000/+0
1	026-719500	POT 10K PCB .5W 68XR10K BE	2.000/+0
1	100-705800	RES NET/SIP 4.7K 8PIN 7RES	2.000/+0
1	100-710000	RES NET/SIP 220 8PIN 7RES	1.000/+0
1	100-710100	RES NET/DIP 22 14PIN 7RES	2.000/+0
1	100-710500	RES NET/SIP 10K 8PIN 7RES	1.000/+0
1	121-704800	REG -5V .1A 79L05 B	1.000/+0
1	121-706100	REG 12V 3A 78L12C	2.000/+0
1	121-706400	REG 12V 1.5A LM340T-12/7812CT	1.000/+0
1	121-706600	REG -12V .1A MC79L12CP MO	1.000/+0
1	121-706700	REG 5V .1A MC78L05AC	1.000/+0
1	134-834200	IC/1793 FLOPPY DISK CONTROLLE	1.000/+0
1	134-834300	IC/6551A WART	1.000/+0
1	134-834700	IC/1488 MDTL LINE DRIVER	1.000/+0
1	134-835400	IC/WD1691 LINE DRIVER	1.000/+0
1	191-712900	CRYS/2MHZ HC-33 .001%	1.000/+0
1	191-713000	CRYS/1.8432MHZ HC33 .005%	1.000/+0
1	201-100000	RES 100 01% 1/8W PRE	1.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	3.000/+0
1	201-100200	RES 10K 01% 1/8W PRE	3.000/+0
1	201-150200	RES 15K 01% 1/8W PRE	1.000/+0
1	201-200100	RES 2K 01% 1/8W PRE	3.000/+0
1	201-475200	RES 47.5K 01% 1/8W	1.000/+0
1	201-681900	RES 68.1 01% 1/8W PRE	1.000/+0
1	201-100200	RES 10K 01% 1/8W PRE	1.000/+0
1	201-200200	RES 20K 01% 1/8W PRE	1.000/+0
1	201-487200	RES 48.7K 01% 1/8W PRE	1.000/+0

M700 KEYBOARD BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-012101	PCB/M764 KEYBOARD	1.000/+0
1	134-713209	IC/74LS74	1.000/+0
1	134-722903	IC/74LS132 2-NAND S.T.	1.000/+0
1	134-711500	IC/555V TIMER	1.000/+0
1	134-728803	IC/28S42 PROM (74S472)	1.000/+0
1	134-731009	IC/74LS138	2.000/+0
1	134-743903	IC/74LS33 QUAD NOR	1.000/+0
1	134-834500	IC/9602 MONOSTABLE MULTIVIBRA	2.000/+0
1	022-719800	DIO TRRF 1N4152 30V .5W G FC	3.000/+0
1	023-726500	CAP 1MF 35V 10% TANT R	1.000/+0
1	023-728400	CAP 330PF 1KV 20% CERM R	1.000/+0
1	023-740800	CAP .01MF 25V 20% CERM	12.000/+0
1	023-743800	CAP 33MF 6.3V TANT	2.000/+0
1	024-822200	CON 2M HDR/SOL RA	1.000/+0
1	100-700700	RES NET/4.7K 10P9RES	1.000/+0
1	100-702700	RES NET/SIP 1K 10PN 9RE	1.000/+0
1	134-834400	IC/3914A KEYBOARD ENCORDER	1.000/+0
1	201-100300	RES 100K 01% 1/8W PRE	1.000/+0
1	201-150100	RES 1.5K 01% 1/8W PRE	1.000/+0
1	201-221300	RES 221K 01% 1/8W PRE	1.000/+0
1	201-332000	RES 332 01% 1/8W PRE	1.000/+0
1	201-475000	RES 475 01% 1/8W	1.000/+0
1	201-475100	RES 4.75K 01% 1/8W PRE	4.000/+0
1	201-475200	RES 47.5K 01% 1/8W	1.000/+0
1	201-475900	RES 47.5 01% 1/8W PRE	1.000/+0
1	201-681000	RES 681 01% 1/8W PRE	1.000/+0
1	201-681200	RES 68.1K 01% 1/8W	1.000/+0
1	201-825000	RES 825 01% 1/8W PRE	1.000/+0
1	023-739600	CAP 10MF 25V 20% ALUM	1.000/+0
1	023-744100	CAP 100MF 6.3V ALUM	1.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	1.000/+0

M700/M800 POWER SUPPLY

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	004-710500	BUSH/NYLON SHOULDER 3052 KE	2.000/+0
1	004-710800	BUSH/ID .190 OD .276 TEFLON	4.000/+0
1	006-006401	WASH/FIBER	2.000/+0
1	019-003401	INDUCT/21MH	2.000/+0
1	019-731900	INDUCT/560UH	2.000/+0
1	021-719500	TRN NPN MJE13007 400V 80W	2.000/+0
1	022-727800	DIO BRID VH648 600V 6A	1.000/+0
1	022-727900	DIO BRID VJ148X 100V 10A	1.000/+0
1	022-728100	DIO RECT 1N5812 50V 20A	2.000/+0
1	022-729900	DIO SCHT IN6096 40V 25A	2.000/+0
1	023-744700	CAP 820MF 200V ALUM	2.000/+0
1	023-746100	CAP .01MF 1KV 10% TANT	1.000/+0
1	032-700800	INSUL/DIODE	1.000/+0
1	040-726900	CLAMP/CAPACITOR MOUNTING VR3A	2.000/+0
1	098-007901	HT SINK/M764 POWER SUPPLY	1.000/+0
1	103-047000	RES 47 5% 1W	1.000/+0
1	105-018100	RES 180 5% 2W	1.000/+0
1	106-709200	RES 10 5W WW	1.000/+0
1	121-706300	REG 1.2 TO 33V 3A LM350K	1.000/+0
1	121-706400	REG 12V 1.5A LM340T-12/7812CT	1.000/+0
1	238-040000	WSH BEL .128X.318X.015 S	3.000/+0
1	258-10400021	SPCR NT #4 1/8" .187 NYLON	2.000/+0
1	405-003104	M764 AC POWER PLUG ASSY	1.000/+0
*2	015-722600	PIN M 18-24G 02-06-2103	6.000/+0
*2	024-819600	CON 6M REC/CRP	1.000/+0
1	405-003203	M764 12V POWER CABLE ASSY	1.000/+0
*2	015-722600	PIN M 18-24G 02-06-2103	2.000/+0
*2	024-819700	CON 2M REC/CRP	1.000/+0
1	405-003303	M764 DC POWER PLUG ASSY	1.000/+0
*2	015-714100	PIN F 14-20GA 02-09-1104	7.000/+0
*2	015-714200	PIN M 14-20GA 02-09-2103	1.000/+0
*2	024-819400	CON 12F REC/CRP 03-09-1122 MO	1.000/+0
1	405-005301	M700/800 DISK POWER PLUG	1.000/+0
*2	015-723100	PIN F 60662-1	8.000/+0
*2	024-703600	CON 4F REC/CRP 1-480424-0 AM	2.000/+0
1	615-012290	M700/800 PWR SUP BASIC PCB	1.000/+0
*2	000-012201	PCB/M700 POWER SUPPLY	1.000/+0
*2	015-722900	PIN/SOLDER TERMINAL 120-1032-	3.000/+0
*2	022-719800	DIO TRRF 1N4152 30V .5W G FC	8.000/+0
*2	022-725900	DIO TRRF IN4937 600V 1A MO	1.000/+0
*2	022-729200	DIO ZENR IN960B 9.1V .5W	1.000/+0
*2	022-729400	DIO ZENR IN721A 20V .4W	1.000/+0
*2	022-729500	DIO ZENR IN957B 6.8V .4W	1.000/+0
*2	022-730000	DIO BRID MDA100A 50V 1A MO	1.000/+0
*2	023-721100	CAP 10MF 6V 20% TANT R	2.000/+0
*2	023-740100	CAP 180PF 1KV 10% TANT	1.000/+0
*2	023-743400	CAP 10MF 200V 5% MYLAR	1.000/+0

M700/M800 POWER SUPPLY BOARD continued

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
*2	023-744300	CAP .01MF 50V MYLAR CAP	2.000/+0
*2	023-745100	CAP .001MF 1KV 10% TANT	1.000/+0
*2	023-745200	CAP .0047MF 1KV 10% TANT	1.000/+0
*2	023-745800	CAP 1000PF 500V MICA	1.000/+0
*2	023-746100	CAP .01MF 1KV 10% TANT	2.000/+0
*2	023-746500	CAP .1MF 50V 15% CERM	3.000/+0
*2	024-824000	CON 1F JCK/SOL RED 402-102	2.000/+0
*2	024-824100	CON 1F JCK/SOL BLK 402-103	1.000/+0
*2	024-824200	CON 1F JCK/SOL BLUE 402-105	2.000/+0
*2	026-719300	POT 200 PCB .5W	1.000/+0
*2	070-710500	FUSE/3A 250V FAST 3AG	1.000/+0
*2	071-711500	HOLDER/FUSE 3529	2.000/+0
*2	079-701100	THERMISTER 150 C 2D754	1.000/+0
*2	102-700200	MOVISTOR/V130LA10A	1.000/+0
*2	102-700700	MOVISTER/V275LA15A	1.000/+0
*2	103-047100	RES 470 5% 1W	2.000/+0
*2	105-056000	RES 56 5% 2W	1.000/+0
*2	134-772600	IC/LM3524N	1.000/+0
*2	134-772609	IC/SG3524	1.000/+0
*2	134-831200	IC/3632 PERIPHERAL DRIVER	1.000/+0
*2	201-100000	RES 100 01% 1/8W PRE	3.000/+0
*2	201-100100	RES 1K 01% 1/8W PRE	2.000/+0
*2	201-100200	RES 10K 01% 1/8W PRE	3.000/+0
*2	201-100300	RES 100K 01% 1/8W PRE	1.000/+0
*2	201-150200	RES 15K 01% 1/8W PRE	2.000/+0
*2	201-200100	RES 2K 01% 1/8W PRE	4.000/+0
*2	201-221000	RES 221 01% 1/8W PRE	2.000/+0
*2	201-221200	RES 22.1K 01% 1/8W	1.000/+0
*2	201-243000	RES 243 01% 1/8W	1.000/+0
*2	201-475100	RES 4.75K 01% 1/8W PRE	2.000/+0
*2	201-681200	RES 68.1K 01% 1/8W	1.000/+0
*2	201-909100	RES 9.09K 01% 1/8W PRE	1.000/+0
*2	208-047900	RES 4.7 1% 1/2W	2.000/+0
*2	208-221300	RES 221K 1% 1/2W	2.000/+0
*2	208-475900	RES 47 1% 1/2W	1.000/+0
*2	021-701800	TRN PNP 2N3905 40V .35W B	1.000/+0
*2	021-712600	TRN 2N3904	1.000/+0
*2	021-720100	TRN SCR MCR101 15V .8A	1.000/+0
*2	019-001001	XFORMER/DRIVE	1.000/+0
*2	019-003001	XFORMER/M764 MAIN	1.000/+0
*2	019-731800	INDUCT/68UH	1.000/+0
*2	023-739800	CAP 1000MF 10V	5.000/+0
*2	023-744800	CAP 470MF 50V 20% ALUM	4.000/+0
*2	023-746600	CAP 22MF 16V 20% ALUM	2.000/+0

M700/M800 POWER SUPPLY BASIC BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-012201	PCB/M700 POWER SUPPLY	1.000/+0
1	015-722900	PIN/SOLDER TERMINAL 120-1032-	3.000/+0
1	022-719800	DIO TRRF 1N4152 30V .5W G FC	8.000/+0
1	022-725900	DIO TRRF IN4937 600V 1A MO	1.000/+0
1	022-729200	DIO ZENR IN960B 9.1V .5W	1.000/+0
1	022-729400	DIO ZENR IN721A 20V .4W	1.000/+0
1	022-729500	DIO ZENR IN957B 6.8V .4W	1.000/+0
1	022-730000	DIO BRID MDA100A 50V 1A MO	1.000/+0
1	023-721100	CAP 10MF 6V 20% TANT R	2.000/+0
1	023-740100	CAP 180PF 1KV 10% TANT	1.000/+0
1	023-743400	CAP 10MF 200V 5% MYLAR	1.000/+0
1	023-744300	CAP .01MF 50V MYLAR CAP	2.000/+0
1	023-745100	CAP .001MF 1KV 10% TANT	1.000/+0
1	023-745200	CAP .0047MF 1KV 10% TANT	1.000/+0
1	023-745800	CAP 1000PF 500V MICA	1.000/+0
1	023-746100	CAP .01MF 1KV 10% TANT	2.000/+0
1	023-746500	CAP .1MF 50V 15% CERM	3.000/+0
1	024-824000	CON 1F JCK/SOL RED 402-102	2.000/+0
1	024-824100	CON 1F JCK/SOL BLK 402-103	1.000/+0
1	024-824200	CON 1F JCK/SOL BLUE 402-105	2.000/+0
1	026-719300	POT 200 PCB .5W	1.000/+0
1	070-710500	FUSE/3A 250V FAST 3AG	1.000/+0
1	071-711500	HOLDER/FUSE 3529	2.000/+0
1	079-701100	THERMISTER 150 C 2D754	1.000/+0
1	102-700200	MOVISTOR/V130LA10A	1.000/+0
1	102-700700	MOVISTER/V275LA15A	1.000/+0
1	103-047100	RES 470 5% 1W	2.000/+0
1	105-056000	RES 56 5% 2W	1.000/+0
1	134-772600	IC/LM3524N	1.000/+0
1	134-772609	IC/SG3524	1.000/+0
1	134-831200	IC/3632 PERIPHERAL DRIVER	1.000/+0
1	201-100000	RES 100 01% 1/8W PRE	3.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	2.000/+0
1	201-100200	RES 10K 01% 1/8W PRE	3.000/+0
1	201-100300	RES 100K 01% 1/8W PRE	1.000/+0
1	201-150200	RES 15K 01% 1/8W PRE	2.000/+0
1	201-200100	RES 2K 01% 1/8W PRE	4.000/+0
1	201-221000	RES 221 01% 1/8W PRE	2.000/+0
1	201-221200	RES 22.1K 01% 1/8W	1.000/+0
1	201-243000	RES 243 01% 1/8W	1.000/+0
1	201-475100	RES 4.75K 01% 1/8W PRE	2.000/+0
1	201-681200	RES 68.1K 01% 1/8W	1.000/+0
1	201-909100	RES 9.09K 01% 1/8W PRE	1.000/+0
1	208-047900	RES 4.7 1% 1/2W	2.000/+0
1	208-221300	RES 221K 1% 1/2W	2.000/+0
1	208-475900	RES 47 1% 1/2W	1.000/+0
1	021-701800	TRN PNP 2N3905 40V .35W B	1.000/+0
1	021-712600	TRN 2N3904	1.000/+0
1	021-720100	TRN SCR MCR101 15V .8A	1.000/+0
1	019-001001	XFORMER/DRIVE	1.000/+0
1	019-003001	XFORMER/M764 MAIN	1.000/+0
1	019-731800	INDUCT/68UH	1.000/+0
1	023-739800	CAP 1000MF 10V	5.000/+0
1	023-744800	CAP 470MF 50V 20% ALUM	4.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	2.000/+0

M764 MOTHER BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	134-736803	IC/74LS374N REGISTER	1.000/+0
1	134-736809	IC/74LS374	1.000/+0
1	134-791603	IC/74F64 AND OR INVERT	2.000/+0
1	615-012300	M800 MOTHER BD BASIC ASSY	1.000/+0
*2	000-012301	PCB/M764 MOTHER BOARD	1.000/+0
*2	023-717400	CAP .1MF 50V 20% CERM R ER	8.000/+0
*2	023-726500	CAP 1MF 35V 10% TANT R	1.000/+0
*2	024-733100	CON 14 PIN DIP 641261-3	2.000/+0
*2	024-741800	CON 25F REC/SOL 206584-1 AM	1.000/+0
*2	024-819300	CON 20M HDR/SOL	1.000/+0
*2	024-820600	CON 60 EDG/SOL DUAL	22.000/+0
*2	024-825600	CON 12M REC/SOL 09-18-5121 MO	1.000/+0
*2	026-702300	POT 5K PCB .5W	1.000/+0
*2	029-708200	RELAY/REED SPDT DIP	1.000/+0
*2	100-705800	RES NET/SIP 4.7K 8PIN 7RES	1.000/+0
*2	100-709900	RES NET/SIP 2.2K 8PIN 7RES	1.000/+0
*2	100-711100	RES NET/SIP 470 8PIN 7RES	1.000/+0
*2	134-725303	IC/7406N O/C HEX INVERTER	1.000/+0
*2	134-736809	IC/74LS374	1.000/+0
*2	134-738403	IC/10125F ECL TRANSLATOR	1.000/+0
*2	134-776503	IC/74LS01N 2-NAND OC	2.000/+0
*2	134-782303	IC/74F04 HEX INVERTER	1.000/+0
*2	134-830800	IC/21182 DELAY LINE 20NSEC	1.000/+0
*2	134-831500	IC/10116 LINE RECEIVER	1.000/+0
*2	201-121000	RES 121 01% 1/8W	1.000/+0
*2	201-182000	RES 182 01% 1/8W	1.000/+0
*2	201-274000	RES 274 01% 1/8W PRE	1.000/+0
*2	201-475000	RES 475 01% 1/8W	3.000/+0
*2	201-825900	RES 82.5 01% 1/8W PRE	1.000/+0
*2	022-719800	DIO TRRF 1N4152 30V .5W G FC	1.000/+0

M764 DAUGHTER BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-012401	PCB/M764 DAUGHTER BOARD	1.000/+0
1	022-719800	DIO TRRF 1N4152 30V .5W G FC	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	3.000/+0
1	024-819100	CON 26M HDR/SOL ST	3.000/+0
1	024-823600	CON/34M HDR/SOL 609-3437 TB	2.000/+0
1	029-708300	RELAY/REED DPST DIP	1.000/+0
1	134-831500	IC/10116 LINE RECEIVER	3.000/+0
1	103-047000	RES 47 5% 1W	1.000/+0

M800 PROCESSOR BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	023-715100	CAP .05MF 50V CERM R	1.000/+0
1	134-715709	IC/74S04	1.000/+0
1	000-013001	PCB/M700 PROCESSOR	1.000/+0
1	134-718303	IC/74S02N 2-NOR	1.000/+0
1	134-720509	IC/74LS174	2.000/+0
1	134-720803	IC/74LS10N 3-NAND	1.000/+0
1	134-722009	IC/4040B	1.000/+0
1	134-722703	IC/74LS08N 2-AND	1.000/+0
1	134-731009	IC/74LS138	2.000/+0
1	134-739109	IC/74LS244	1.000/+0
1	134-740003	IC/74S08 2-NAND	1.000/+0
1	134-742300	IC/2141-5/9244 4KX1 RAM	8.000/+0
1	134-743803	IC/74LS157	3.000/+0
1	134-747103	IC/74LS161 4 BIT COUNTER	1.000/+0
1	134-751700	IC/75160 488 BUFFER	1.000/+0
1	134-751800	IC/75161 488 BUFFER T	1.000/+0
1	134-776503	IC/74LS01N 2-NAND OC	1.000/+0
1	134-783200	IC/74F373 OCTAL LATCH	1.000/+0
1	134-783600	IC/74F244 OCTAL BUFFER	3.000/+0
1	134-783903	IC/74LS166 SHIFT REGISTER	1.000/+0
1	134-812403	IC/74LS165 8-BIT SHIFT REG	2.000/+0
1	134-821900	IC/74S38 2-NAND BUF O/C	1.000/+0
1	134-826000	IC/74F245 TRANSCEIVER	4.000/+0
1	134-837000	IC/DM8160	1.000/+0
1	021-712600	TRN 2N3904	1.000/+0
1	022-719800	DIO TRRF 1N4152 30V .5W G FC	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	26.000/+0
1	023-740600	CAP 15PF 1KV 10% TANT	1.000/+0
1	023-743800	CAP 33MF 6.3V TANT	2.000/+0
1	023-745100	CAP .001MF 1KV 10% TANT	1.000/+0
1	024-715900	CON 16F DIP/SOL 641262-3 AM	1.000/+0
1	024-721300	CON 24F DIP/SOL 641266-3 AM	2.000/+0
1	024-730900	CON 28F DIP/SOL 641267-3 AM	6.000/+0
1	024-733100	CON 14 PIN DIP 641261-3	1.000/+0
1	024-740700	CON 20F DIP/SOL 641264-3 AM	1.000/+0
1	024-825300	CON 16F DIP/SOL 516-AG11D	1.000/+0
1	100-700700	RES NET/4.7K 10P9RES	3.000/+0
1	100-701500	RES NST/SIP 10K 10PIN 9RES	1.000/+0
1	100-702700	RES NET/SIP 1K 10PN 9RE	1.000/+0
1	100-705800	RES NET/SIP 4.7K 8PIN 7RES	2.000/+0
1	134-712803	IC/74LS00N 2-NAND	1.000/+0
1	134-713203	IC/74LS74N FLIP-FLOP	1.000/+0
1	134-713209	IC/74LS74	1.000/+0
1	134-736400	IC/8085A-2 8BIT MICROPROCESSO	1.000/+0
1	134-752100	IC/9914 488 CONTROLLER T	1.000/+0
1	134-759800	IC/MK4802/HM6116-3 2K/8 150N	1.000/+0
1	134-824700	IC/8275 CRT CONTROLLER	1.000/+0

M800 PROCESSOR BOARD continued

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	134-834800	IC/8155-2 RAM 2K W/I/O TIMER	1.000/+0
1	191-713300	CRYS/13.219 MHZ 60HZ	1.000/+0
1	201-332000	RES 332 01% 1/8W PRE	2.000/+0
1	201-475000	RES 475 01% 1/8W	8.000/+0
1	201-475100	RES 4.75K 01% 1/8W PRE	2.000/+0
1	201-475900	RES 47.5 01% 1/8W PRE	1.000/+0
1	201-681000	RES 681 01% 1/8W PRE	1.000/+0
1	201-681200	RES 68.1K 01% 1/8W	1.000/+0
1	208-047900	RES 4.7 1% 1/2W	2.000/+0
1	208-075000	RES 75 1% 1/2W	1.000/+0
1	023-721000	CAP 100MF 16V 20% TANT R	1.000/+0
1	023-726300	CAP 22MF 35V TANT R	1.000/+0
1	023-726600	CAP 6.8MF 35V 10% TANT R	1.000/+0
1	024-820000	CON 3M HDR/SOL	1.000/+0
1	025-757000	SW/SL 8POS DIP	1.000/+0
1	134-717403	IC/14S10 PROM (74S287/6301-1)	1.000/+0
1	134-728803	IC/28S42 PROM (74S472)	1.000/+0
1	134-758700	IC/2532JL 32K EPROM T	2.000/+0
1	134-806000	IC/2764 8KX8 EPROM 450NSEC	6.000/+0
1	176-403511	FIRM/ U45 6301-1 M700 PROC	1.000/+0
*2	134-717403	IC/14S10 PROM (74S287/6301-1)	1.000/+0
*2	134-717409	IC/14S10 74S287 6301-1	1.000/+0
1	176-406205	FIRM/ U51 6348-1 PROC W/IO	1.000/+0
*2	134-728803	IC/28S42 PROM (74S472)	1.000/+0

BASIC TIMING MEMORY BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-006501	PCB/TIMING MEMORY	1.000/+0
1	015-722900	PIN/SOLDER TERMINAL 120-1032-	3.000/+0
1	021-701800	TRN PNP 2N3905 40V .35W B	3.000/+0
1	021-712600	TRN 2N3904	2.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	50.000/+0
1	023-728400	CAP 330PF 1KV 20% CERM R	1.000/+0
1	023-739600	CAP 10MF 25V 20% ALUM	4.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	2.000/+0
1	026-719900	POT 50 PCB .5W 3329H-500 BR	1.000/+0
1	100-705800	RES NET/SIP 4.7K 8PIN 7RES	1.000/+0
1	100-710900	RES NET/SIP 100 8PIN 7RES	2.000/+0
1	100-711000	RES NET/SIP 160 8PN7RES	2.000/+0
1	100-711100	RES NET/SIP 470 8PIN 7RES	9.000/+0
1	121-706100	REG 12V 3A 78L12C	1.000/+0
1	121-706600	REG -12V .1A MC79L12CP MO	1.000/+0
1	134-711209	IC/74S74	2.000/+0
1	134-715803	IC/74S10N 3-NAND	1.000/+0
1	134-718103	IC/74LS191N COUNTER	2.000/+0
1	134-720509	IC/74LS174	1.000/+0
1	134-730903	IC/74LS367N HEX DRIVER	1.000/+0
1	134-731009	IC/74LS138	1.000/+0
1	134-738403	IC/10125F ECL TRANSLATOR	2.000/+0
1	134-739003	IC/74S374N REGISTER	4.000/+0
1	134-739109	IC/74LS244	1.000/+0
1	134-740600	IC/4015 SHIFT REGISTER	5.000/+0
1	134-756400	IC/747 DUAL 741 OP AMP	1.000/+0
1	134-773400	IC/10102L ECL GATE	4.000/+0
1	134-773500	IC/10131 D FLIP FLOP M/S	4.000/+0
1	134-805603	IC/74S373 OCTAL LATCH	4.000/+0
1	134-824000	IC/74LS73 J-K FLIP-FLOP	1.000/+0
1	134-827400	IC/10130 D FLIP-FLOP	4.000/+0
1	134-828000	IC/10158 2 INPUT MULTIPLEXER	2.000/+0
1	134-830500	IC/6080 8BIT DAC	2.000/+0
1	134-831400	IC/10117 OR-AND/OR-AND INVERT	8.000/+0
1	134-831500	IC/10116 LINE RECEIVER	1.000/+0
1	134-836500	IC/93L422/93422 4 BIT TTL MEM	8.000/+0
1	201-100000	RES 100 01% 1/8W PRE	4.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	8.000/+0
1	201-150100	RES 1.5K 01% 1/8W PRE	2.000/+0
1	201-162000	RES 162 01% 1/8W	2.000/+0
1	201-200100	RES 2K 01% 1/8W PRE	2.000/+0
1	201-243200	RES 24.3K 01% 1/8W PRE	1.000/+0
1	201-332000	RES 332 01% 1/8W PRE	1.000/+0
1	201-332100	RES 3.32K 01% 1/8W PRE	5.000/+0
1	201-475000	RES 475 01% 1/8W	1.000/+0
1	201-681000	RES 681 01% 1/8W PRE	1.000/+0
1	201-825900	RES 82.5 01% 1/8W PRE	1.000/+0
1	214-107100	RES 1.07K .5% 1/8W	4.000/+0
1	214-200200	RES 20K .5% 1/8W	4.000/+0

TIMING CONTROL BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-007101	PCB/TIMING CONTROL	1.000/+0
1	134-713203	IC/74LS74N FLIP-FLOP	1.000/+0
1	134-713209	IC/74LS74	1.000/+0
1	134-719403	IC/74LS151N MULTIPLEXER	2.000/+0
1	134-722203	IC/74LS90 COUNTER	5.000/+0
1	134-731009	IC/74LS138	1.000/+0
1	134-736803	IC/74LS374N REGISTER	1.000/+0
1	134-736809	IC/74LS374	1.000/+0
1	134-738403	IC/10125F ECL TRANSLATOR	2.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	2.000/+0
1	134-740600	IC/4015 SHIFT REGISTER	8.000/+0
1	134-745803	IC/74LS373 OCTAL LATCH	1.000/+0
1	134-749803	IC/10103F ECL-4-2 INPUT MOT	1.000/+0
1	134-773400	IC/10102L ECL GATE	3.000/+0
1	134-792700	IC/10101F ECL 2 INPUT OR/NOR	2.000/+0
1	134-792800	IC/10104F ECL 2 INPUT AND	2.000/+0
1	134-827400	IC/10130 D FLIP-FLOP	1.000/+0
1	134-827600	IC/10137 DECADE COUNTER	9.000/+0
1	134-827700	IC/10138 BI-QUINARY COUNTER	1.000/+0
1	134-827800	IC/10148 64BIT RAM	3.000/+0
1	134-828200	IC/10162 1 TO 8 DECODER	1.000/+0
1	134-828700	IC/10186 D M/S FLIP-FLOP	1.000/+0
1	134-829000	IC/10211 3-IN 3-OUT NOR	2.000/+0
1	134-831400	IC/10117 OR-AND/OR-AND INVERT	5.000/+0
1	015-722900	PIN/SOLDER TERMINAL 120-1032-	1.000/+0
1	021-701800	TRN PNP 2N3905 40V .35W B	2.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	25.000/+0
1	023-740200	CAP 100PF 1KV 10% TANT	1.000/+0
1	023-740800	CAP .01MF 25V 20% CERM	1.000/+0
1	023-741000	CAP 3.5TO20PF 250V CERM	1.000/+0
1	024-715900	CON 16F DIP/SOL 641262-3 AM	1.000/+0
1	100-710900	RES NET/SIP 100 8PIN 7RES	1.000/+0
1	100-711000	RES NET/SIP 160 8PN7RES	1.000/+0
1	100-711100	RES NET/SIP 470 8PIN 7RES	10.000/+0
1	134-829000	IC/10211 3-IN 3-OUT NOR	1.000/+0
1	134-830800	IC/21182 DELAY LINE 20NSEC	1.000/+0
1	191-712800	CRYS/100MHZ HC18 .005%	1.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	6.000/+0
1	201-182000	RES 182 01% 1/8W	1.000/+0
1	201-221000	RES 221 01% 1/8W PRE	2.000/+0
1	201-274000	RES 274 01% 1/8W PRE	1.000/+0
1	201-332100	RES 3.32K 01% 1/8W PRE	2.000/+0
1	201-475000	RES 475 01% 1/8W	2.000/+0
1	019-003301	TOROID 100MHZ	1.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	2.000/+0

1K STATE MEMORY BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	023-717400	CAP .1MF 50V 20% CERM R ER	20.000/+0
1	023-740200	CAP 100PF 1KV 10% TANT	1.000/+0
1	023-743800	CAP 33MF 6.3V TANT	2.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	2.000/+0
1	100-700700	RES NET/4.7K 10P9RES	1.000/+0
1	100-710700	RES NET/DIP 2.2 16PIN	1.000/+0
1	134-711209	IC/74S74	1.000/+0
1	134-715709	IC/74S04	2.000/+0
1	134-718303	IC/74S02N 2-NOR	1.000/+0
1	134-731009	IC/74LS138	2.000/+0
1	134-736803	IC/74LS374N REGISTER	2.000/+0
1	134-736809	IC/74LS374	2.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	1.000/+0
1	134-739003	IC/74S374N REGISTER	5.000/+0
1	134-739109	IC/74LS244	4.000/+0
1	134-759800	IC/MK4802/HM6116-3 2K/8 150N	1.000/+0
1	134-789104	IC/2149H 45NS MEMORY	4.000/+0
1	134-805603	IC/74S373 OCTAL LATCH	2.000/+0
1	134-824400	IC/8304 8BIT TRANSCEIVER	1.000/+0
1	134-830600	IC/27LS01/93411 256 RAM 45NSE	5.000/+0
1	134-830700	IC/21185 DELAY LINE 50NSEC	2.000/+0
1	134-835100	IC/74S289	5.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	1.000/+0
1	201-221000	RES 221 01% 1/8W PRE	2.000/+0
1	201-332000	RES 332 01% 1/8W PRE	2.000/+0

M800 TIMING MEMORY BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-031201	PCB/M800 TIMING MEMORY	1.000/+0
1	015-722900	PIN/SOLDER TERMINAL 120-1032-	4.000/+0
1	019-731700	INDUCT/FERRITE BEAD	4.000/+0
1	021-701800	TRN PNP 2N3905 40V .35W B	1.000/+0
1	022-719800	DIO TRRF 1N4152 30V .5W G FC	1.000/+0
1	022-729600	DIO TRRF IN916 20V 10MA	1.000/+0
1	022-729800	DIO ZERN IN958B 7.5V .4W	1.000/+0
1	023-740400	CAP 47PF 1KV 10% TANT	1.000/+0
1	023-740800	CAP .01MF 25V 20% CERM	6.000/+0
1	023-743500	CAP .1MF 50V 10% CERM	42.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	5.000/+0
1	024-818400	CON 10M HDR/SOL RA	1.000/+0
1	024-824300	CON 1F CXL/SOL 26060-3 AM	1.000/+0
1	026-719400	POT 500 PCB .5W	1.000/+0
1	026-719600	POT 1K PCB .5W 62M1K BE	4.000/+0
1	098-708700	HT SNK/6073B TH	1.000/+0
1	098-708800	HT SNK/68 PIN CHIP CARRIER	2.000/+0
1	100-702700	RES NET/SIP 1K 10PN 9RE	1.000/+0
1	100-705700	RES NET/SIP 56 8 PN 7 RE	2.000/+0
1	100-709600	RES NET/SIP 162/260 8PIN	3.000/+0
1	100-710400	RES NET/SIP 470 10PIN 9RES	4.000/+0
1	100-710900	RES NET/SIP 100 8PIN 7RES	5.000/+0
1	100-711100	RES NET/SIP 470 8PIN 7RES	15.000/+0
1	121-702400	REG -1.2TO-37V 1.5A 337T E NA	1.000/+0
1	121-704800	REG -5V .1A 79L05 B	1.000/+0
1	133-014002	HYBRID GATE ARRAY	2.000/+0
1	134-712803	IC/74LS00N 2-NAND	1.000/+0
1	134-722403	IC/74LS139N MULTIPLEXER	1.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	3.000/+0
1	134-740600	IC/4015 SHIFT REGISTER	1.000/+0
1	134-749803	IC/10103F ECL-4-2 INPUT MOT	1.000/+0
1	134-753700	IC/LM339 DIFFERENTIAL COMP.	1.000/+0
1	134-792800	IC/10104F ECL 2 INPUT AND	1.000/+0
1	134-793100	IC/10136F ECL HEX COUNTER	2.000/+0
1	134-824500	IC/3430/3651 QUAD COMPARATORS	4.000/+0
1	134-826000	IC/74F245 TRANSCEIVER	1.000/+0
1	134-826800	IC/10H210 ECL 3-IN 3-OUT OR	1.000/+0
1	134-827000	IC/10H159 ECL 2INPUT MULTIPLE	2.000/+0
1	134-827100	IC/10H158 ECL 2INPUT MULTIPLE	1.000/+0
1	134-827300	IC/10H131 ECL D FLIP-FLOP	5.000/+0
1	134-827900	IC/10153 QUAD LATCH	2.000/+0
1	134-828000	IC/10158 2 INPUT MULTIPLEXER	1.000/+0
1	134-828700	IC/10186 D M/S FLIP-FLOP	1.000/+0
1	134-829100	IC/10422 1K RAM 7NSEC	8.000/+0
1	134-829500	IC/10H104	3.000/+0
1	134-829600	IC/10H105 2-3-2 OR/NOR	3.000/+0
1	134-832900	IC/4094B 8 STAGE SHIFT REG	1.000/+0
1	134-833800	IC/DAC808 8BIT DAC	3.000/+0
1	134-833900	IC/LF347 JFET OP-AMP	1.000/+0
1	134-838400	IC/10H116 LINE RECIEVER	3.000/+0
1	201-100000	RES 100 01% 1/8W PRE	19.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	4.000/+0
1	201-105100	RES 1.05K 01% 1/8W PRE	1.000/+0
1	201-200100	RES 2K 01% 1/8W PRE	1.000/+0
1	201-249100	RES 2.49K 01% 1/8W PRE	3.000/+0
1	201-274000	RES 274 01% 1/8W PRE	6.000/+0
1	201-332100	RES 3.32K 01% 1/8W PRE	1.000/+0
1	201-475000	RES 475 01% 1/8W	4.000/+0
1	201-590100	RES 5.9K 01% 1/8W	1.000/+0
1	215-649100	RES 6.49K .25% 1/8W	3.000/+0

M800 TIMING CONTROL BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-031301	PCB/M800 TIMING CONTROL	1.000/+0
1	013-700900	JUMPER 2F HDR 2-530153-2 AM	1.000/+0
1	015-722900	PIN/SOLDER TERMINAL 120-1032-	5.000/+0
1	019-005801	INDUCT/TOROID T12-0 200MHZ	1.000/+0
1	021-701800	TRN PNP 2N3905 40V .35W B	1.000/+0
1	021-712600	TRN 2N3904	1.000/+0
1	022-719800	DIO TRRF 1N4152 30V .5W G FC	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	1.000/+0
1	023-740500	CAP 33PF 1KV 10% TANT	1.000/+0
1	023-740600	CAP 15PF 1KV 10% TANT	1.000/+0
1	023-740800	CAP .01MF 25V 20% CERM	2.000/+0
1	023-741000	CAP 3.5TO20PF 250V CERM	1.000/+0
1	023-745500	CAP 2.2PF 1KV CERM	1.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	3.000/+0
1	024-823300	CON 1M HDR/SOL 75401-007	2.000/+0
1	024-824300	CON 1F CXL/SOL 26060-3 AM	2.000/+0
1	026-719600	POT 1K PCB .5W 62M1K BE	1.000/+0
1	098-708700	HT SNK/6073B TH	1.000/+0
1	100-709500	RES NET/SIP 100 10PIN 9RES	1.000/+0
1	100-709600	RES NET/SIP 162/260 8PIN	13.000/+0
1	100-710900	RES NET/SIP 100 8PIN 7RES	6.000/+0
1	100-711100	RES NET/SIP 470 8PIN 7RES	7.000/+0
1	121-702400	REG -1.2TO-37V 1.5A 337T E NA	1.000/+0
1	134-731009	IC/74LS138	1.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	1.000/+0
1	134-740600	IC/4015 SHIFT REGISTER	10.000/+0
1	134-749803	IC/10103F ECL-4-2 INPUT MOT	1.000/+0
1	134-753700	IC/LM339 DIFFERENTIAL COMP.	1.000/+0
1	134-773400	IC/10102L ECL GATE	2.000/+0
1	134-792800	IC/10104F ECL 2 INPUT AND	1.000/+0
1	134-793100	IC/10136F ECL HEX COUNTER	5.000/+0
1	134-824500	IC/3430/3651 QUAD COMPARATORS	1.000/+0
1	134-826700	IC/10H211 ECL 3-IN 3-OUT OR	2.000/+0
1	134-826800	IC/10H210 ECL 3-IN 3-OUT OR	3.000/+0
1	134-827200	IC/10H136 ECL HEX COUNTER	2.000/+0
1	134-827300	IC/10H131 ECL D FLIP-FLOP	13.000/+0
1	134-827400	IC/10130 D FLIP-FLOP	1.000/+0
1	134-827700	IC/10138 BI-QUINARY COUNTER	3.000/+0
1	134-828300	IC/10164 8 LINE MULTIPLEXER	1.000/+0
1	134-828900	IC/10197 HEX AND	1.000/+0
1	134-829400	IC/10H102 2-NOR	10.000/+0
1	134-829500	IC/10H104	2.000/+0
1	134-829600	IC/10H105 2-3-2 OR/NOR	3.000/+0
1	134-829700	IC/10H107 2-XOR/XNOR	1.000/+0
1	134-829800	IC/10H109 4/5-OR/NOR	1.000/+0
1	134-829900	IC/10H117 OR-AND/OR-AND-INV	2.000/+0
1	134-833700	IC/14518B CMOS BCD COUNTER	2.000/+0
1	134-838400	IC/10H116 LINE RECIEVER	1.000/+0
1	191-711400	CRYS/200 MHZ .0035% HC18 RH	1.000/+0
1	201-100000	RES 100 01% 1/8W PRE	1.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	4.000/+0
1	201-121100	RES 1.21K 1% 1/8W	1.000/+0
1	201-150100	RES 1.5K 01% 1/8W PRE	1.000/+0
1	201-200100	RES 2K 01% 1/8W PRE	1.000/+0
1	201-274000	RES 274 01% 1/8W PRE	1.000/+0
1	201-332100	RES 3.32K 01% 1/8W PRE	1.000/+0
1	201-475000	RES 475 01% 1/8W	9.000/+0
1	201-511900	RES 51.1 01% 1/8W	1.000/+0
1	201-681000	RES 681 01% 1/8W PRE	1.000/+0
1	201-162000	RES 162 01% 1/8W	2.000/+0

M800 STATE MEMORY BOARD

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-036001	PCB/M800 STATE MEMORY	1.000/+0
1	134-736803	IC/74LS374N REGISTER	7.000/+0
1	134-731009	IC/74LS138	2.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	1.000/+0
1	134-739003	IC/74S374N REGISTER	4.000/+0
1	134-739109	IC/74LS244	2.000/+0
1	134-739203	IC/74S32N 2-OR	1.000/+0
1	134-740003	IC/74S08 2-NAND	2.000/+0
1	134-740903	IC/74LS240N OCTAL BUFFER	1.000/+0
1	134-823200	IC/74S244 LINE DRIVERS	4.000/+0
1	134-766703	IC/74F374 OCTAL FLIP FLOP	10.000/+0
1	134-823400	IC/74LS09 2-NAND	1.000/+0
1	134-826000	IC/74F245 TRANSCEIVER	1.000/+0
1	134-832300	IC/2148 4K RAM 35NSEC	8.000/+0
1	134-821400	IC/74S09 2-AND O/C	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	53.000/+0
1	023-747100	CAP 22MF 16V 20% TANT DROP	2.000/+0
1	024-721300	CON 24F DIP/SOL 641266-3 AM	1.000/+0
1	024-740700	CON 20F DIP/SOL 641264-3 AM	1.000/+0
1	024-797700	CON 10M HDR-SOL D/RA AP	2.000/+0
1	100-709700	RES NET/SIP 1K 8PIN 7RES	2.000/+0
1	134-759800	IC/MK4802/HM6116-3 2K/8 150N	1.000/+0
1	201-200100	RES 2K 01% 1/8W PRE	1.000/+0
1	176-008802	FIRM/ 6308-1 1K ST. MEM	1.000/+0
*2	134-835500	IC/6308-1 PROM	1.000/+0

M800 STATE CONTROL BOARD (25 MHz)

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-036101	PCB/M800 STATE CONTROL	1.000/+0
1	134-710409	IC/74S00	2.000/+0
1	134-711209	IC/74S74	2.000/+0
1	134-712803	IC/74LS00N 2-NAND	1.000/+0
1	134-713203	IC/74LS74N FLIP-FLOP	1.000/+0
1	134-713209	IC/74LS74	1.000/+0
1	134-715803	IC/74S10N 3-NAND	2.000/+0
1	134-720703	IC/74S189N/27S03 BIPOLAR RAM	4.000/+0
1	134-720803	IC/74LS10N 3-NAND	1.000/+0
1	134-722703	IC/74LS08N 2-AND	1.000/+0
1	134-731009	IC/74LS138	2.000/+0
1	134-732903	IC/74LS32N 2-OR	1.000/+0
1	134-736803	IC/74LS374N REGISTER	4.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	2.000/+0
1	134-739109	IC/74LS244	2.000/+0
1	134-740600	IC/4015 SHIFT REGISTER	5.000/+0
1	134-766303	IC/74F191 COUNTER	3.000/+0
1	134-766403	IC/74F00 2-NAND	3.000/+0
1	134-766703	IC/74F374 OCTAL FLIP FLOP	2.000/+0
1	134-773400	IC/10102L ECL GATE	5.000/+0
1	134-821500	IC/74S20 4-NAND	1.000/+0
1	134-826100	IC/74F190 DECADE COUNTER	4.000/+0
1	134-827400	IC/10130 D FLIP-FLOP	2.000/+0
1	134-832200	IC/2149 CMOS 4K RAM 25NSEC	2.000/+0
1	021-701800	TRN PNP 2N3905 40V .35W B	2.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	52.000/+0
1	023-728400	CAP 330PF 1KV 20% CERM R	1.000/+0
1	024-822800	CON 5M HDR/SOL D/RA	2.000/+0
1	100-711100	RES NET/SIP 470 8PIN 7RES	10.000/+0
1	134-733403	IC/74LS30N 8-NAND	1.000/+0
1	134-738403	IC/10125F ECL TRANSLATOR	1.000/+0
1	134-740003	IC/74S08 2-NAND	1.000/+0
1	134-773500	IC/10131 D FLIP FLOP M/S	1.000/+0
1	134-788203	IC/74F10 NAND	1.000/+0
1	134-821700	IC/74S30 8-NAND	1.000/+0
1	134-822100	IC/74S134 12-NAND	1.000/+0
1	134-822900	IC/74S175 D FLIP-FLOP	1.000/+0
1	134-823200	IC/74S244 LINE DRIVERS	1.000/+0
1	134-828900	IC/10197 HEX AND	1.000/+0
1	134-829000	IC/10211 3-IN 3-OUT NOR	1.000/+0
1	134-830800	IC/21182 DELAY LINE 20NSEC	1.000/+0
1	201-100100	RES 1K 01% 1/8W PRE	6.000/+0
1	201-150100	RES 1.5K 01% 1/8W PRE	1.000/+0
1	201-221000	RES 221 01% 1/8W PRE	1.000/+0
1	201-221100	RES 2.21K 01% 1/8W PRE	1.000/+0
1	201-332000	RES 332 01% 1/8W PRE	1.000/+0
1	201-332100	RES 3.32K 01% 1/8W PRE	2.000/+0
1	201-475100	RES 4.75K 01% 1/8W PRE	3.000/+0
1	201-511900	RES 51.1 01% 1/8W	1.000/+0
1	201-681000	RES 681 01% 1/8W PRE	1.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	2.000/+0

1K STATE MEMORY BOARD (20 MHz)

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-036801	PCB/1K STATE MEMORY	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	38.000/+0
1	023-740200	CAP 100PF 1KV 10% TANT	1.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	1.000/+0
1	100-700700	RES NET/4.7K 10P9RES	1.000/+0
1	100-710600	RES NET/SIP 2.2K 10PIN 9RES	2.000/+0
1	134-738903	IC/10124F ECL TRANSLATOR	1.000/+0
1	134-766703	IC/74F374 OCTAL FLIP FLOP	7.000/+0
1	134-782203	IC/74F74 DUAL FLIP-FLOP	1.000/+0
1	134-782303	IC/74F04 HEX INVERTER	2.000/+0
1	134-783200	IC/74F373 OCTAL LATCH	2.000/+0
1	134-783600	IC/74F244 OCTAL BUFFER	4.000/+0
1	134-783700	IC/74F32 QUAD 2-INPUT OR GATE	1.000/+0
1	134-788903	IC/74F02 2-NOR	1.000/+0
1	134-789403	IC/74F138 MULTIPLEXER	2.000/+0
1	134-825900	IC/74F289 64BIT RAM	5.000/+0
1	134-826000	IC/74F245 TRANSCEIVER	1.000/+0
1	134-830600	IC/27LS01/93411 256 RAM 45NSE	5.000/+0
1	134-830700	IC/21185 DELAY LINE 50NSEC	2.000/+0
1	134-831900	IC/6116LP-2 16K RAM 120NSEC	1.000/+0
1	134-832300	IC/2148 4K RAM 35NSEC	4.000/+0
1	134-835500	IC/6308-1 PROM	2.000/+0
1	176-008802	FIRM/ 6308-1 1K ST. MEM	2.000/+0
*2	134-835500	IC/6308-1 PROM	1.000/+0
1	201-182000	RES 182 01% 1/8W	3.000/+0
1	201-221000	RES 221 01% 1/8W PRE	10.000/+0
1	201-332000	RES 332 01% 1/8W PRE	2.000/+0
1	201-475000	RES 475 01% 1/8W	1.000/+0

1K STATE CONTROL BOARD (20 MHz)

LEVEL	PART NUMBER	DESCRIPTION	QUANTITY
1	000-036901	PCB/1K STATE CONTROL	1.000/+0
1	134-711209	IC/74S74	1.000/+0
1	134-736803	IC/74LS374N REGISTER	1.000/+0
1	134-736809	IC/74LS374	2.000/+0
1	134-738403	IC/10125F ECL TRANSLATOR	1.000/+0
1	134-739109	IC/74LS244	2.000/+0
1	134-740600	IC/4015 SHIFT REGISTER	5.000/+0
1	134-745409	IC/74S64	1.000/+0
1	134-747103	IC/74LS161 4 BIT COUNTER	3.000/+0
1	134-751403	IC/74S51 AND-OR-INVERTER	2.000/+0
1	134-766303	IC/74F191 COUNTER	3.000/+0
1	134-766403	IC/74F00 2-NAND	3.000/+0
1	134-766503	IC/74F08 2-NAND	2.000/+0
1	134-782203	IC/74F74 DUAL FLIP-FLOP	8.000/+0
1	134-783700	IC/74F32 QUAD 2-INPUT OR GATE	1.000/+0
1	134-788203	IC/74F10 NAND	1.000/+0
1	134-788903	IC/74F02 2-NOR	2.000/+0
1	134-789403	IC/74F138 MULTIPLEXER	2.000/+0
1	134-791603	IC/74F64 AND OR INVERT	3.000/+0
1	134-822400	IC/74S162 4BIT DECADE COUNTER	4.000/+0
1	134-826200	IC/74F189 64BIT RAM	5.000/+0
1	134-826300	IC/74F169 UP/DOWN COUNTER	1.000/+0
1	134-826400	IC/74F164 SHIFT REGISTER	1.000/+0
1	134-826500	IC/74F86 2-XOR	1.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER	32.000/+0
1	023-740100	CAP 180PF 1KV 10% TANT	1.000/+0
1	023-740200	CAP 100PF 1KV 10% TANT	2.000/+0
1	100-710400	RES NET/SIP 470 10PIN 9RES	3.000/+0
1	100-711600	RES NET/SIP 220/330 8PIN 7RES	1.000/+0
1	201-221000	RES 221 01% 1/8W PRE	19.000/+0
1	201-221100	RES 2.21K 01% 1/8W PRE	1.000/+0
1	201-332000	RES 332 01% 1/8W PRE	5.000/+0
1	201-475900	RES 47.5 01% 1/8W PRE	1.000/+0
1	201-562900	RES 56.2 01% 1/8W PRE	6.000/+0
1	023-746600	CAP 22MF 16V 20% ALUM	2.000/+0

M81A PROBE

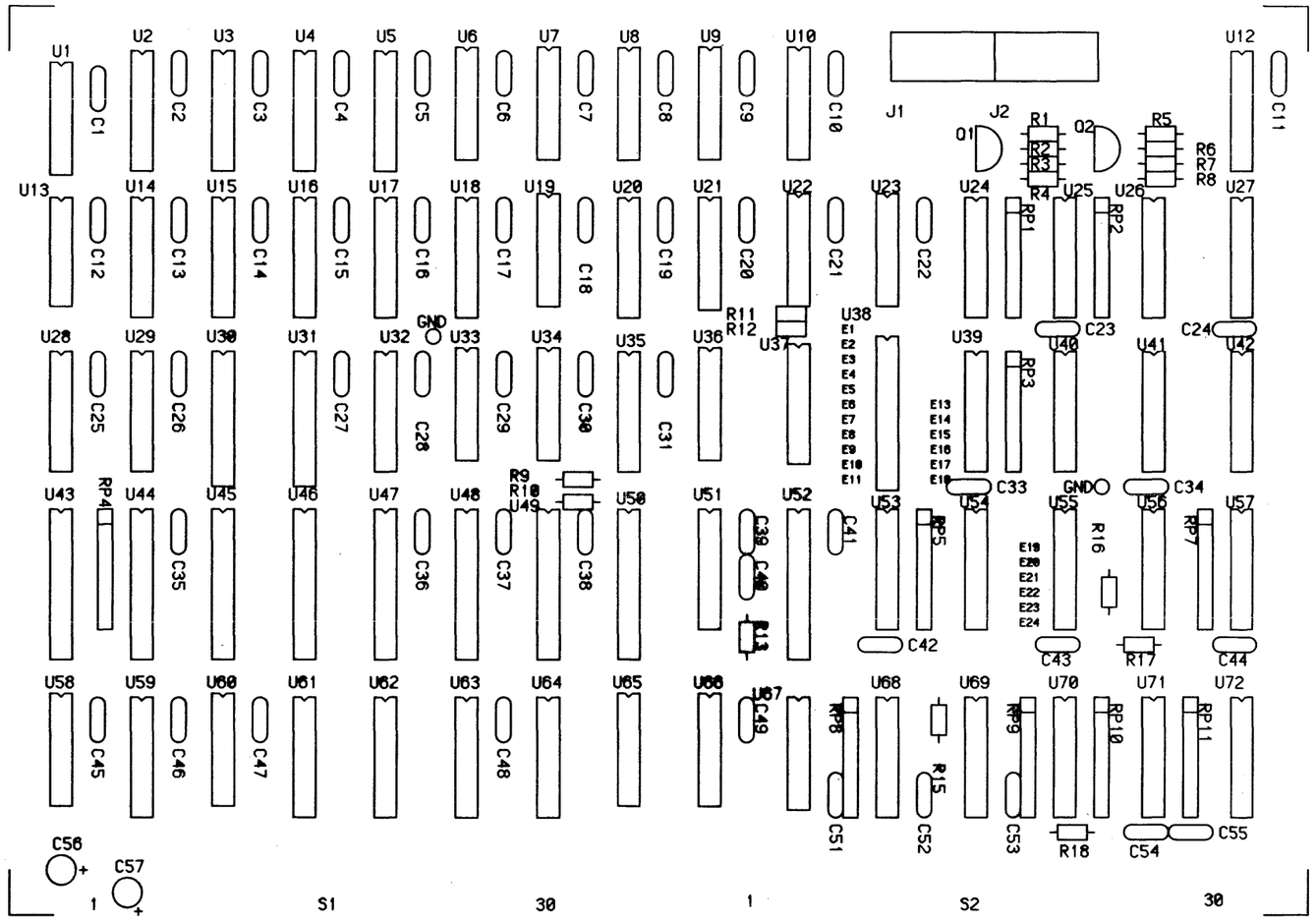
LEVEL	PART NUMBER	DESCRIPTION		QUANTITY
1	000-031501	PCB/M81A PROBE	Y	1.000/+0
1	013-700900	JUMPER 2F HDR 2-530153-2 AM		1.000/+0
1	015-722900	PIN/SOLDER TERMINAL 120-1032-		4.000/+0
1	022-719800	DIO TRRF 1N4152 30V .5W G FC		2.000/+0
1	023-717400	CAP .1MF 50V 20% CERM R ER		16.000/+0
1	023-739600	CAP 10MF 25V 20% ALUM		3.000/+0
1	024-820700	CON 40F HDR/SOL D/RA		1.000/+0
1	024-823300	CON 1M HDR/SOL 75401-007		7.000/+0
1	085-002901	CBL/MODEL 80		1.000/+0
1	133-013301	HYBRID 2 CHANNEL PROBE		5.000/+0
1	201-010000	RES 10 01% 1/8W	PRE	10.000/+0
1	201-020000	RES 20 01% 1/8W		10.000/+0
1	201-274900	RES 27.4 01% 1/8W		2.000/+0
1	201-475000	RES 475 01% 1/8W		1.000/+0
1	201-681000	RES 681 01% 1/8W	PRE	1.000/+0

TRICK CARD

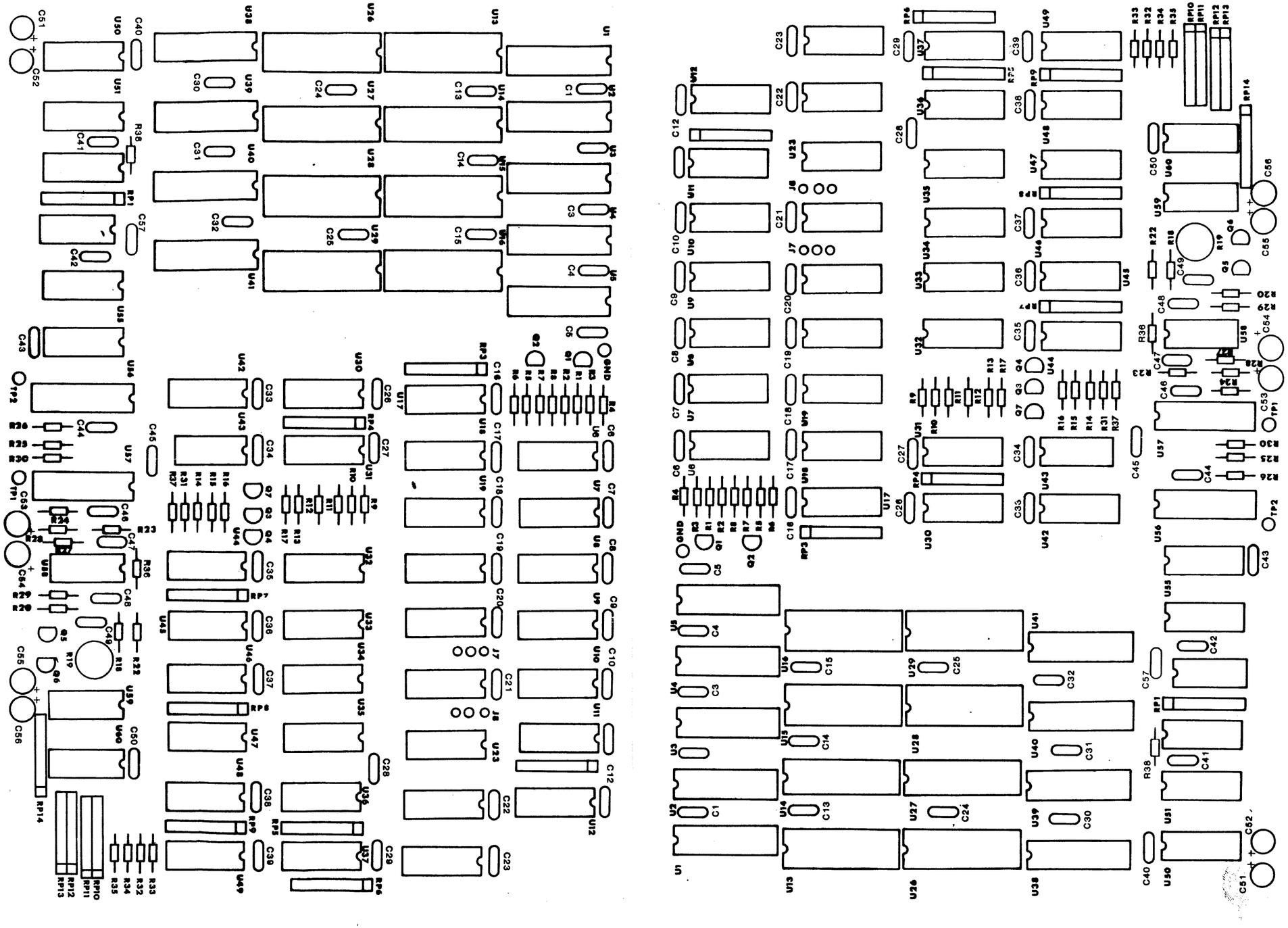
LEVEL	PART NUMBER	DESCRIPTION		QUANTITY
1	000-004601	PCB/DEMO CARD		1.000/10
1	134-824600	IC/4520 CMOS UP COUNTER		2.000/10
1	134-824800	IC/4011 CMOS 2-NAND		2.000/10
1	134-824900	IC/4002 CMOS 4-NOR		1.000/10
1	023-740800	CAP .01MF 25V 20% CERM		1.000/10
1	023-745300	CAP .001MF 50V		1.000/10
1	201-100200	RES 10K 01% 1/8W	PRE	1.000/10
1	201-475900	RES 47.5 01% 1/8W	PRE	2.000/10
1	051-704900	BUMPER END CAP 322-2		4.000/10
1	201-100000	RES 100 01% 1/8W	PRE	1.000/10

23.1 CIRCUIT BOARDS

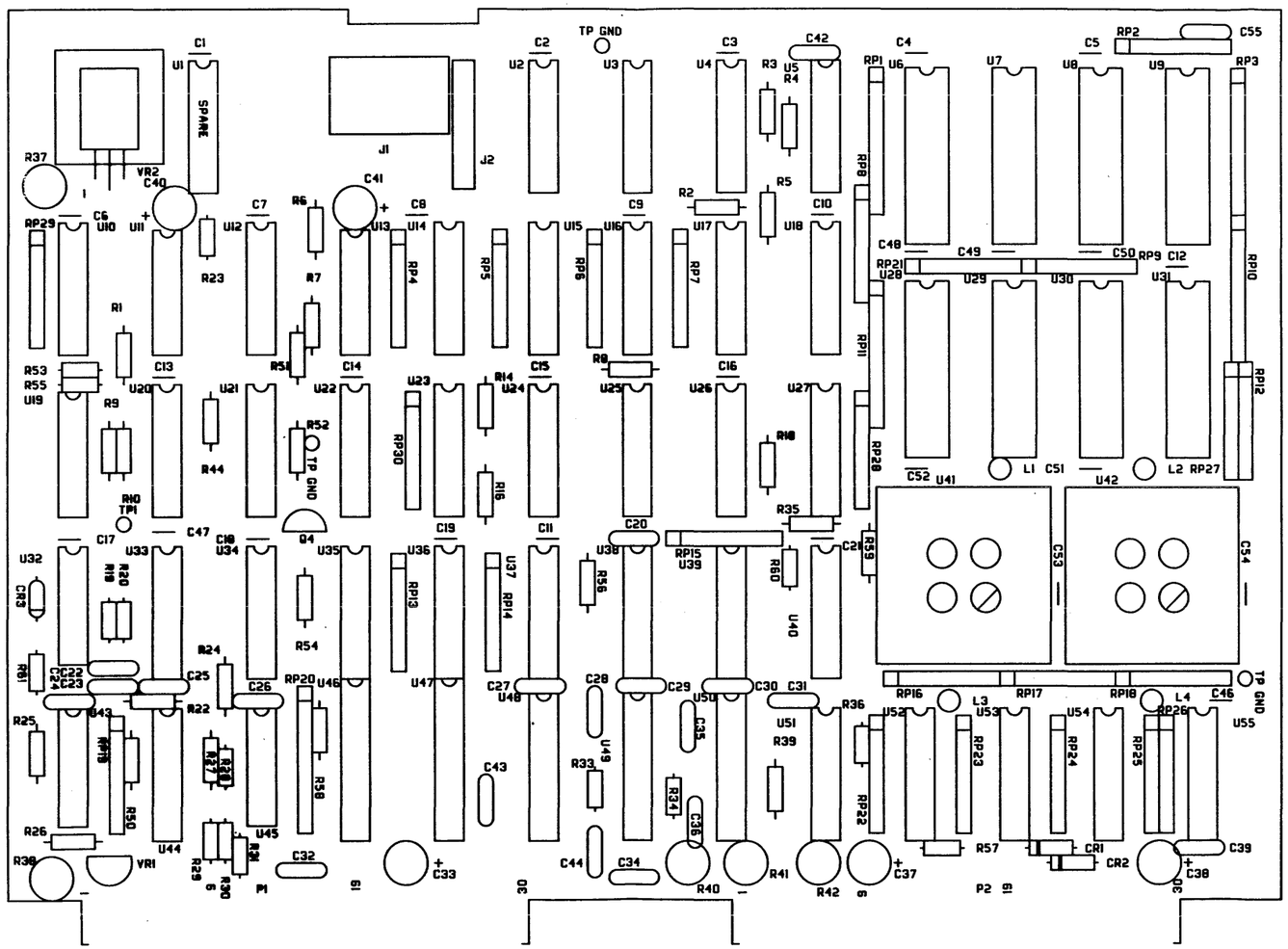
166-036101	M800 State Control (25 MHz) Board	23-3
166-006501	M800 Basic Timing Memory Board	23-4
166-031201	M800 Timing Memory Board	23-5
166-036001	M800 State Memory (25 MHz) Board	23-6
166-031301	M800 Timing Control Board	23-7
166-009901	CTSA Board	23-8
166-011202	M700 Disk RAM Controller	23-9
166-007201	Waveform Board	23-10
166-007101	M700/800 Power Supply	23-11
166-013020	M700/800 Processor Board	23-12
166-004602	M540/532 Trick Card	23-13
166-012401	M764 Daughter Board	23-13
166-012201	M700/800 Power Supply	23-13
166-012190	M764 Keyboard	23-14
166-012301	M764 Motherboard	23-15
166-012801	1K State Control (15 MHz) Board	23-16
166-036901	1K State Control(20 MHz) Board	23-17
166-036801	1K State Memory (20 MHz) Board	23-18
166-012701	1K State Memory Board	23-19
166-031501	M81A Probe	23-20
166-001502	M51A Probe	23-20
166-005201	M80 Probe	23-20



M800 State Control (25 MHz) Board
615-036101



M800 Basic Timing Memory Board
615-006501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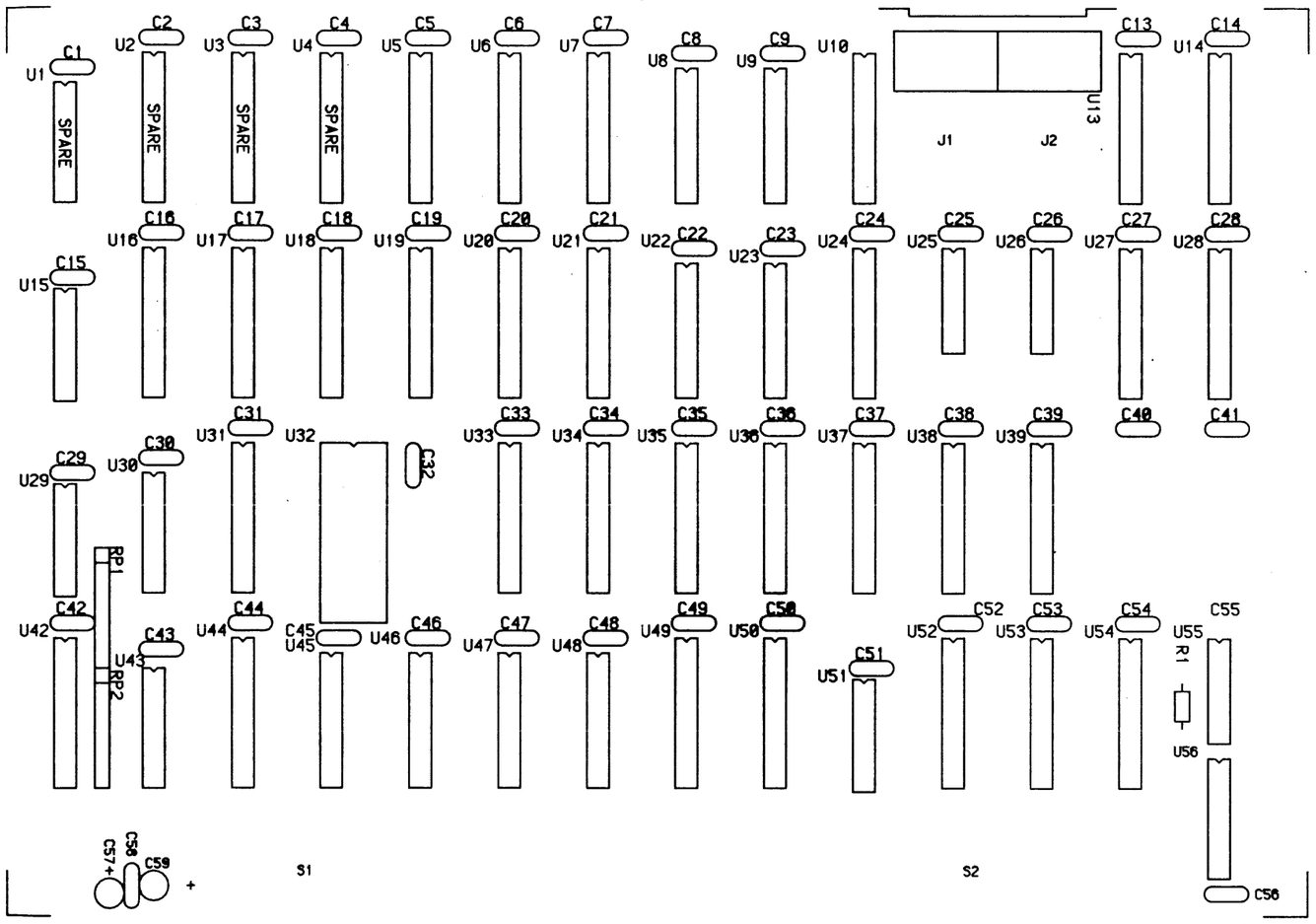
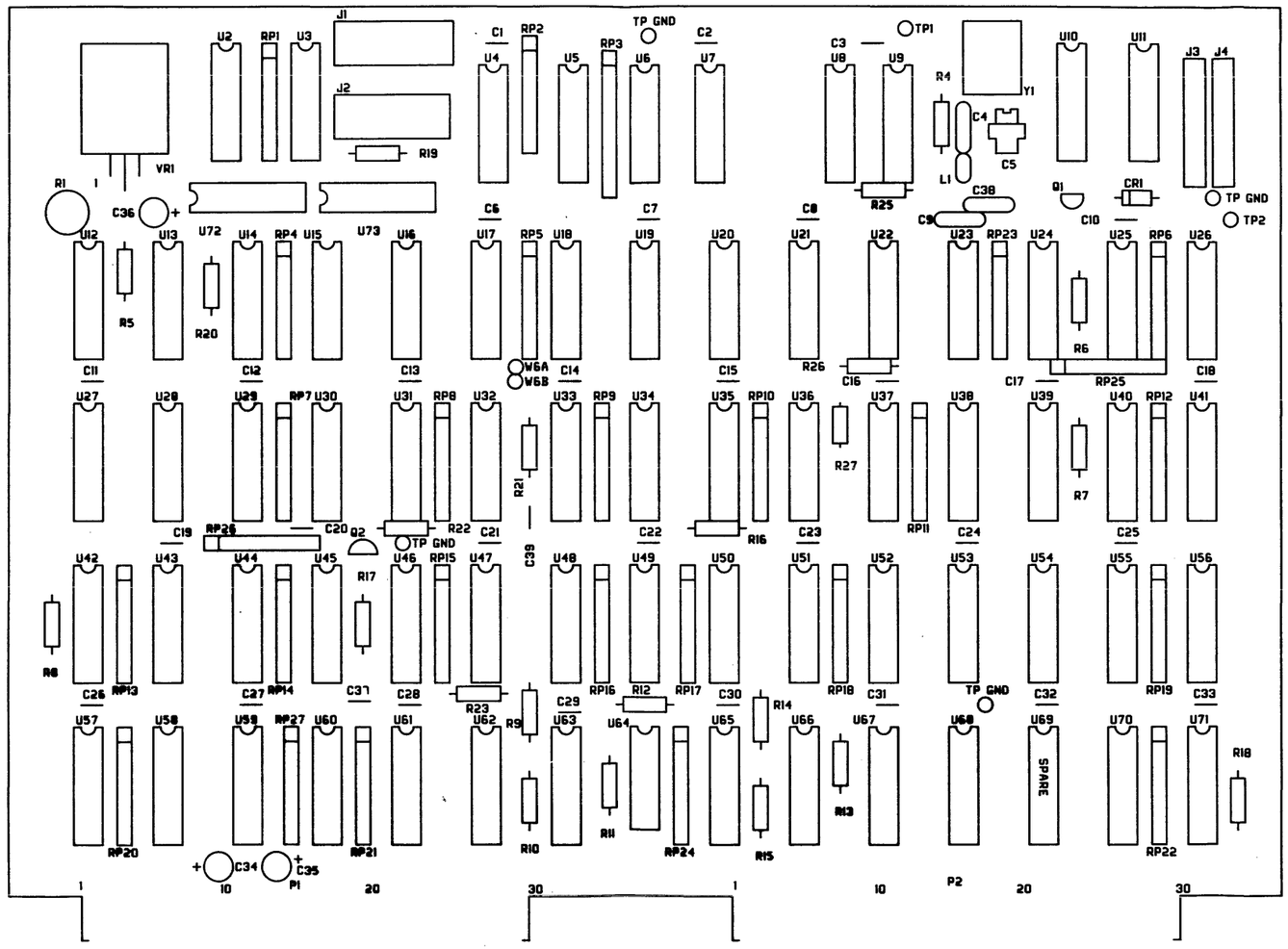
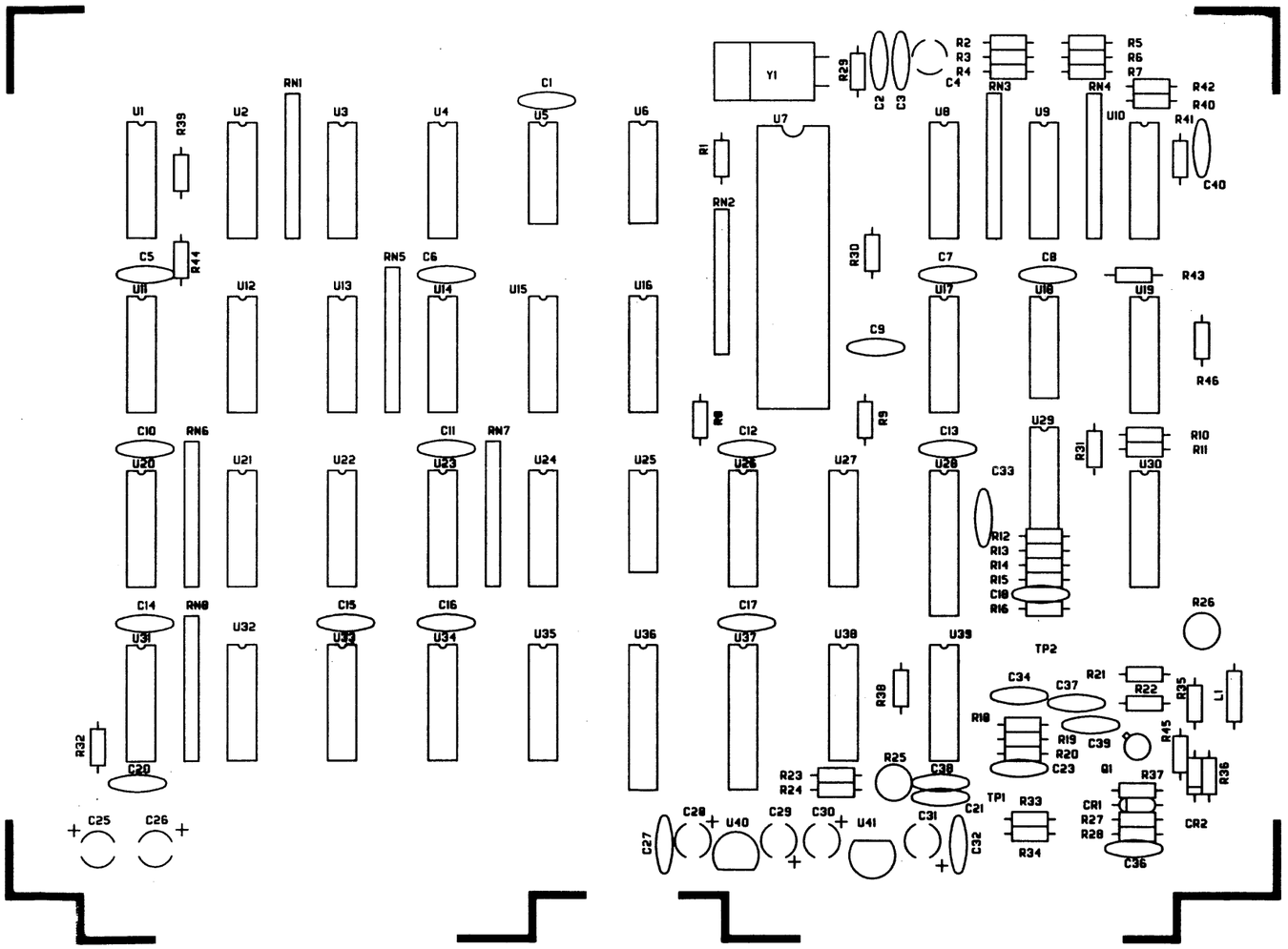


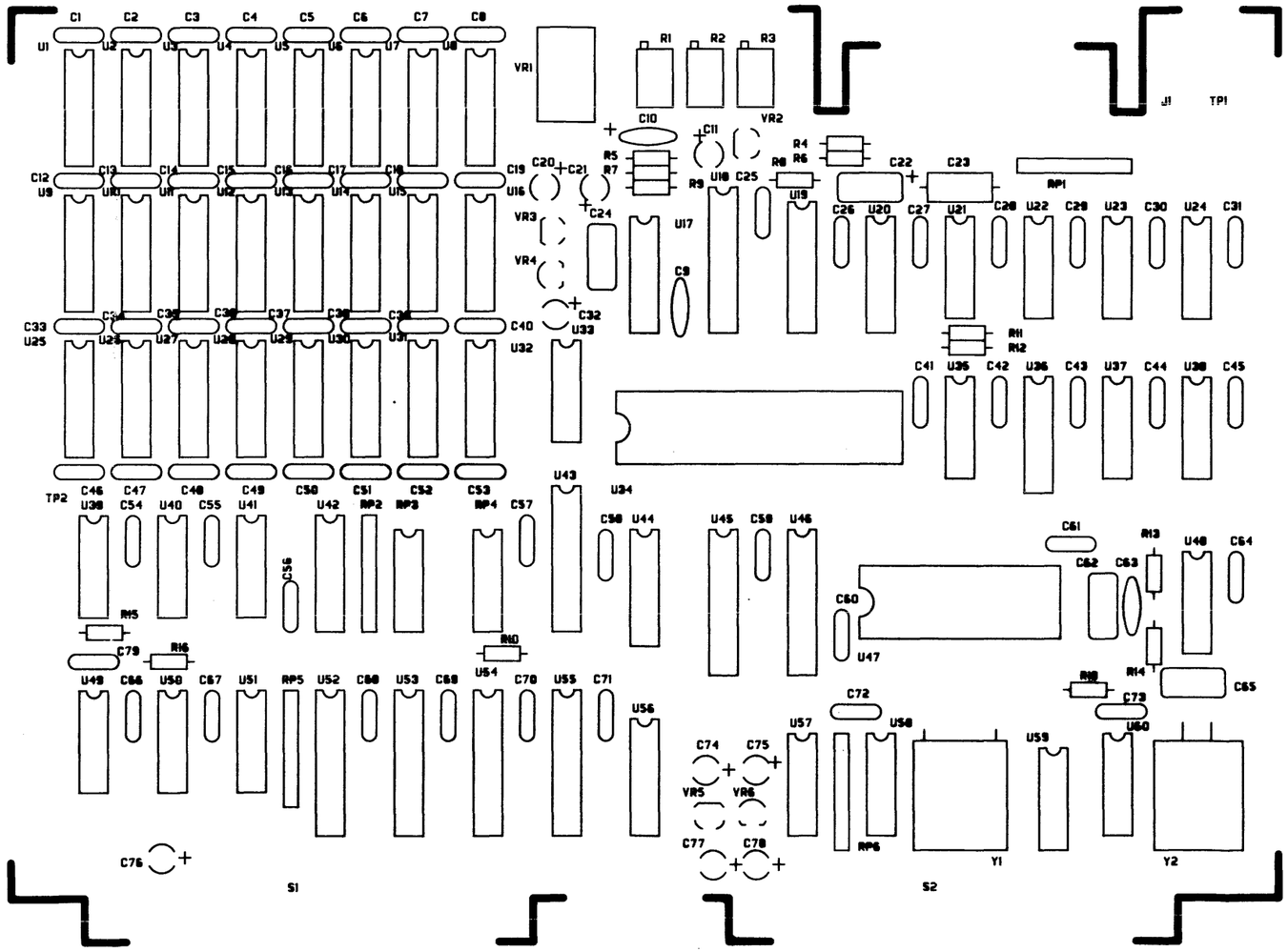
M800 State Memory (25 MHz) Board
615-036001

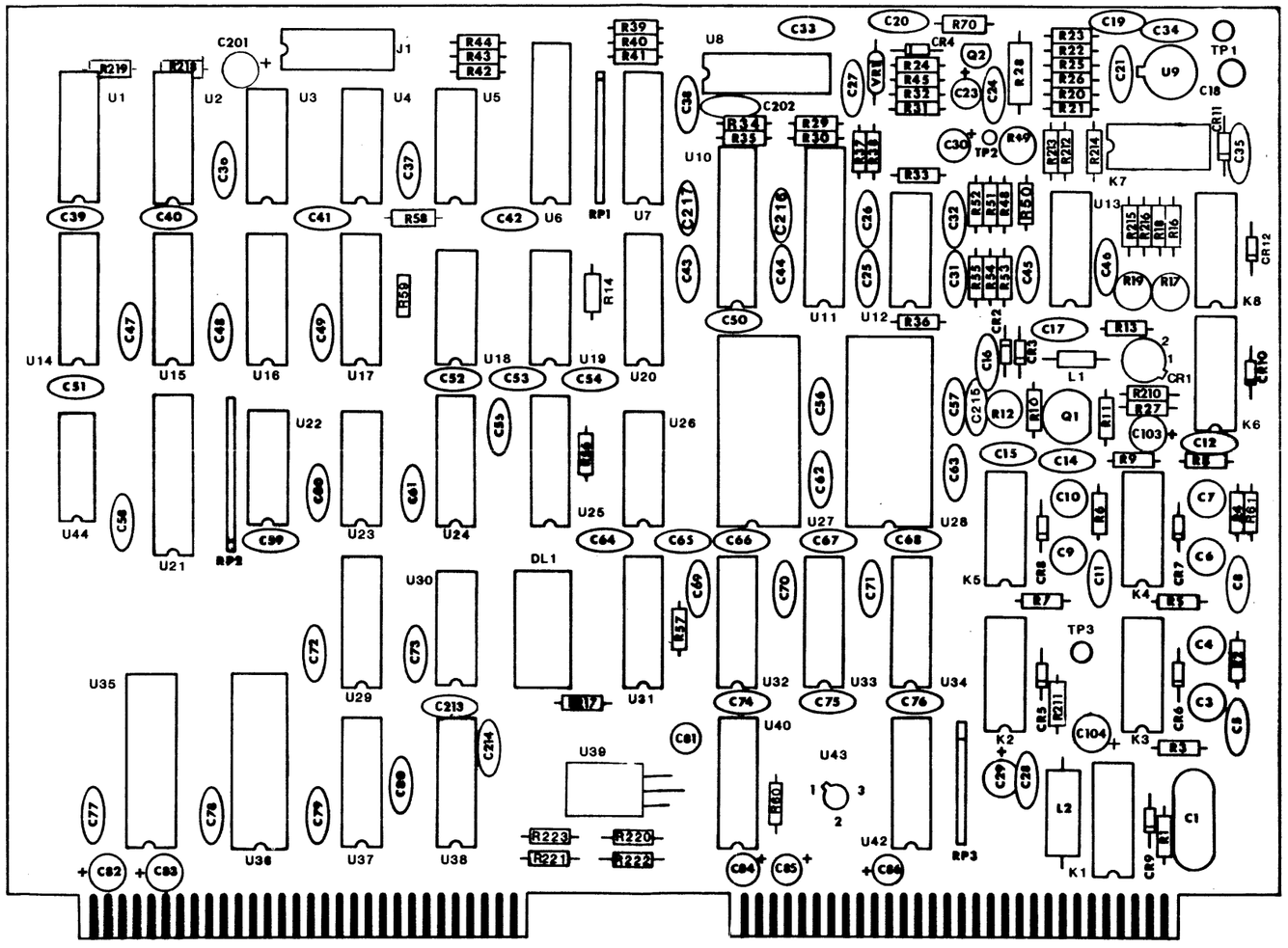


M800 Timing Control Board
615-031301

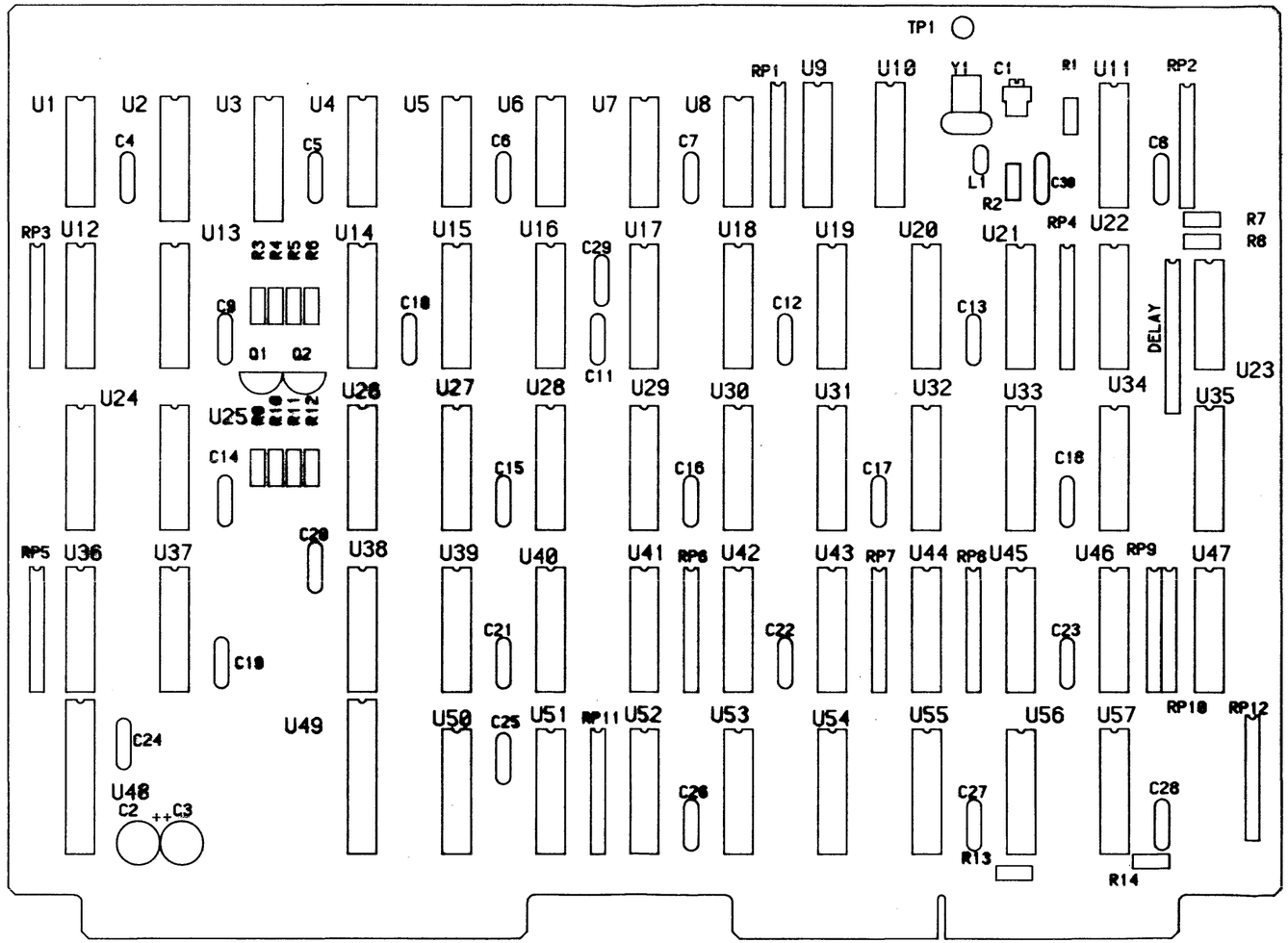


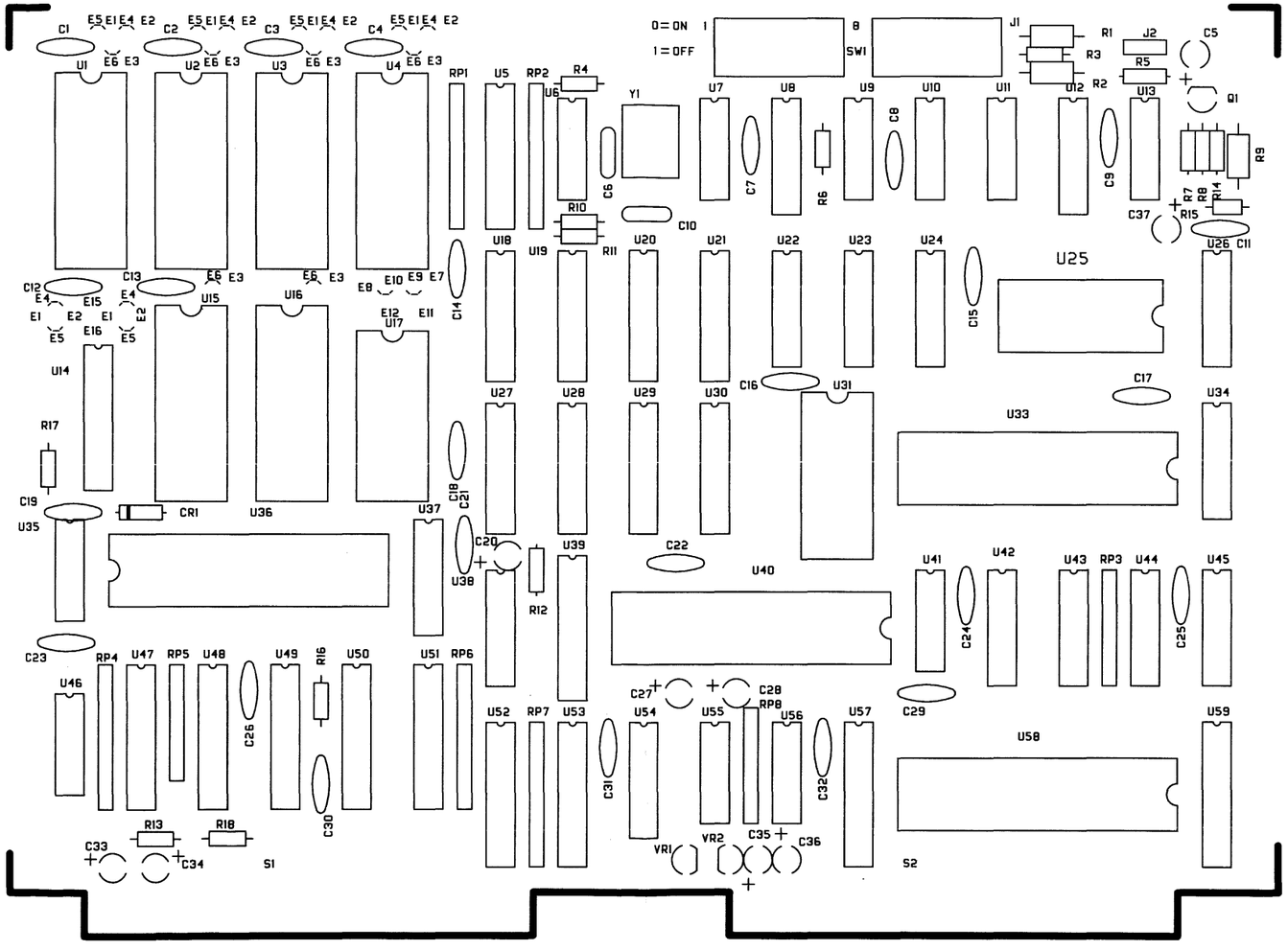
CTSA Board
615-009901

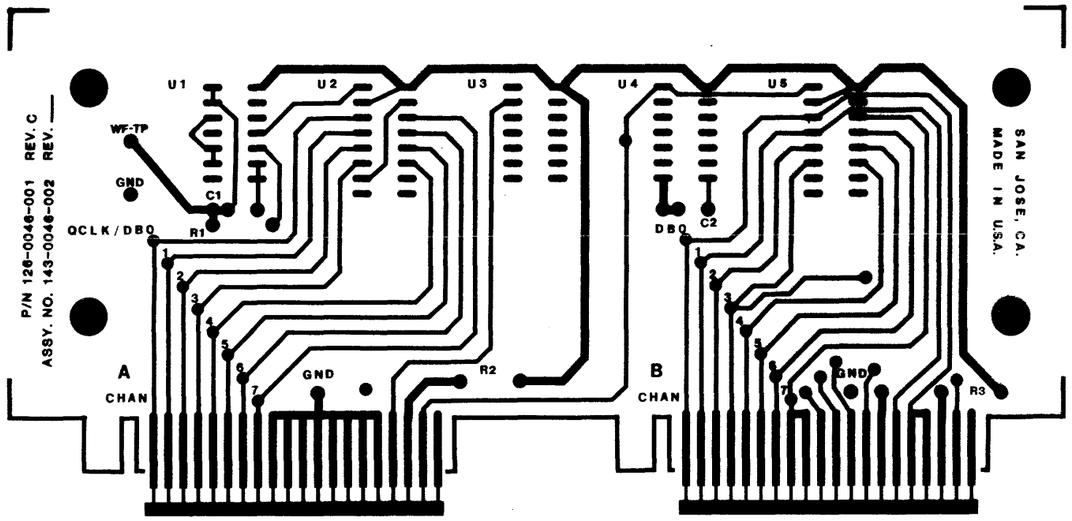

C1 C2 C3 C4 C5 C6 C7 C8
U1 U2 U3 U4 U5 U6 U7 U8
VR1
R1 R2 R3
VR2
J1
TP1
C10
C11
R4
R5
R6
R7
R8
R9
C22
C23
RP1
C12 C13 C14 C15 C16 C17 C18 C19
U9 U10 U11 U12 U13 U14 U15 U16
C20 C21
C24
U17
U18
C25
U19
C26 U20 C27 U21 C28 U22 C29 U23 C30 U24 C31
VR3
VR4
C9
C32
U33
C40
U32
RH1
RH2
C33 C34 C35 C36 C37 C38 C39
U25 U26 U27 U28 U29 U30 U31
C41 U35 C42 U36 C43 U37 C44 U38 C45
U43
U34
TP2
C46 C47 C48 C49 C50 C51 C52 C53 C57
U38 C54 U40 C55 U41 U42 RP2 RP3 RP4
C58 U44
U45 C58 U46
C61
C62 C63
R13
U48 C64
C60
U47
C56
RH5
C79
RH6
RH0
U54
R14
C65
R18
C73
U60
U49 C66 U50 C67 U51 RP5 U52 C68 U53 C69 C70 U55 C71
U56
C72
U57
U58
U59
C74 C75
VR5 VR6
C77 C78
RP6
C76
Y1
Y2
S1
S2



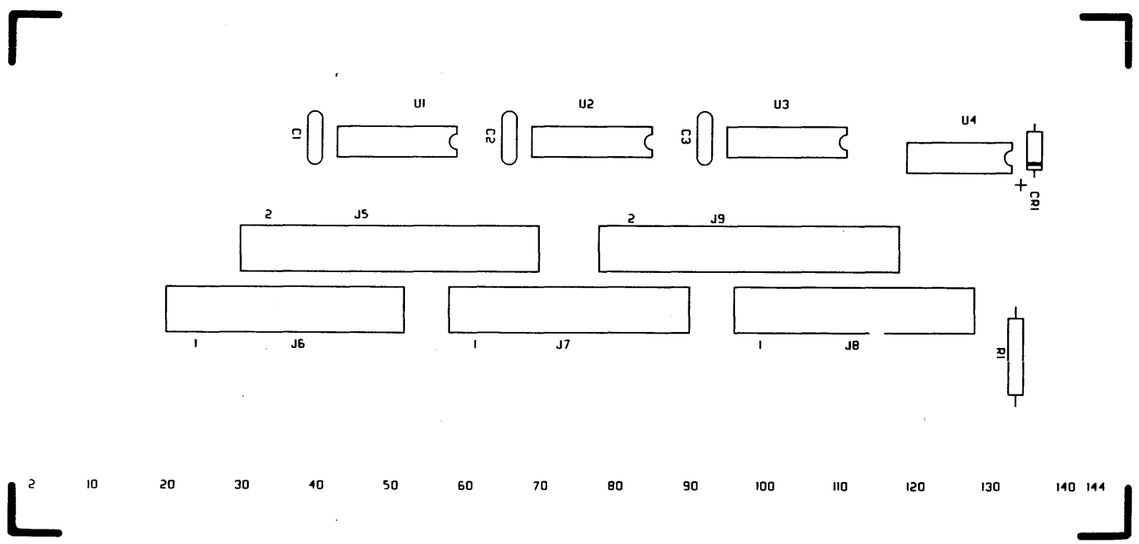
Waveform Board
615-007201


TP1
U1
U2
U3
U4
U5
U6
U7
U8
RP1
U9
U10
Y1
C1
R1
U11
RP2
C4
C5
C6
C7
L1
R2
C30
C8
RP3
U12
U13
U14
U15
U16
C29
U17
U18
U19
U20
U21
RP4
U22
R7
R8
C9
C10
C11
C12
C13
Q1
Q2
DELAY
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
C14
C15
C16
C17
C18
C20
RP5
U36
U37
U38
U39
U40
U41
RP6
U42
U43
RP7
U44
RP8
U45
U46
RP9
U47
C19
C21
C22
C23
U49
U50
C25
U51
RP11
U52
U53
U54
U55
U56
U57
RP10
RP12
C24
U48
C2
C3
C26
C27
C28
R13
R14

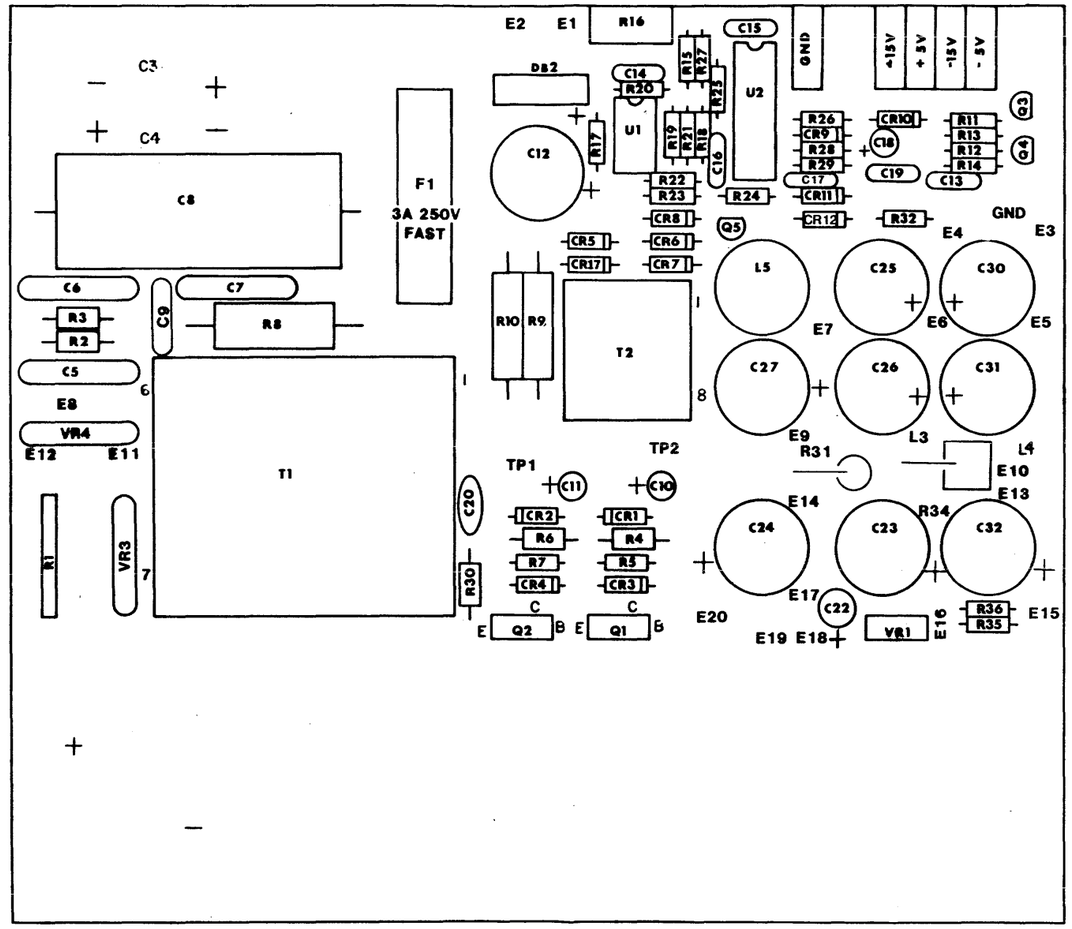

C1
C2
C3
C4
U1
U2
U3
U4
RP1
U5
RP2
U6
R4
Y1
U7
U8
U9
U10
U11
U12
U13
J1
R1
R3
R2
J2
R5
C5
Q1
R9
R7
R8
R14
R15
C37
C8
C9
C6
C7
R6
C10
R10
R11
U18
U19
U20
U21
U22
U23
U24
U25
U26
C11
C12
C13
C14
C15
U14
U15
U16
U17
C16
C17
U27
U28
U29
U30
U31
U33
U34
R17
C19
U35
CR1
U36
U37
C18
C21
U38
C20
U39
C22
U40
U41
U42
U43
RP3
U44
U45
C24
C25
C23
RP4
U47
RP5
U48
U49
R16
U50
U46
C26
C30
U51
RP6
U52
RP7
U53
C27
C28
RP8
U54
U55
U56
U57
U58
U59
C29
C31
C32
R13
R18
C33
C34
S1
VR1
VR2
C35
C36
S2
0=ON
1=OFF
SW1



Model 540/532 Trick Card
615-004602



M764 Daughter Board
615-012401

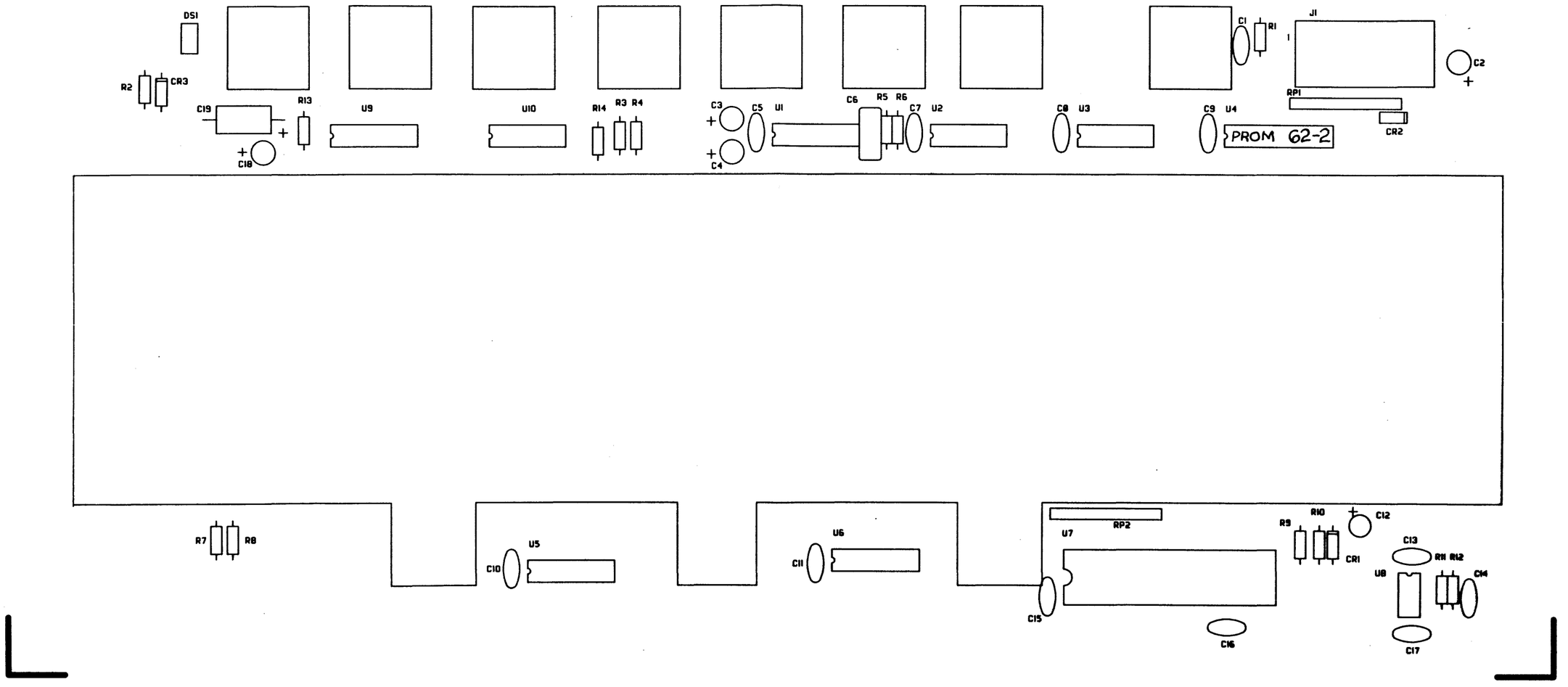


M700/800 Power Supply
615-012201

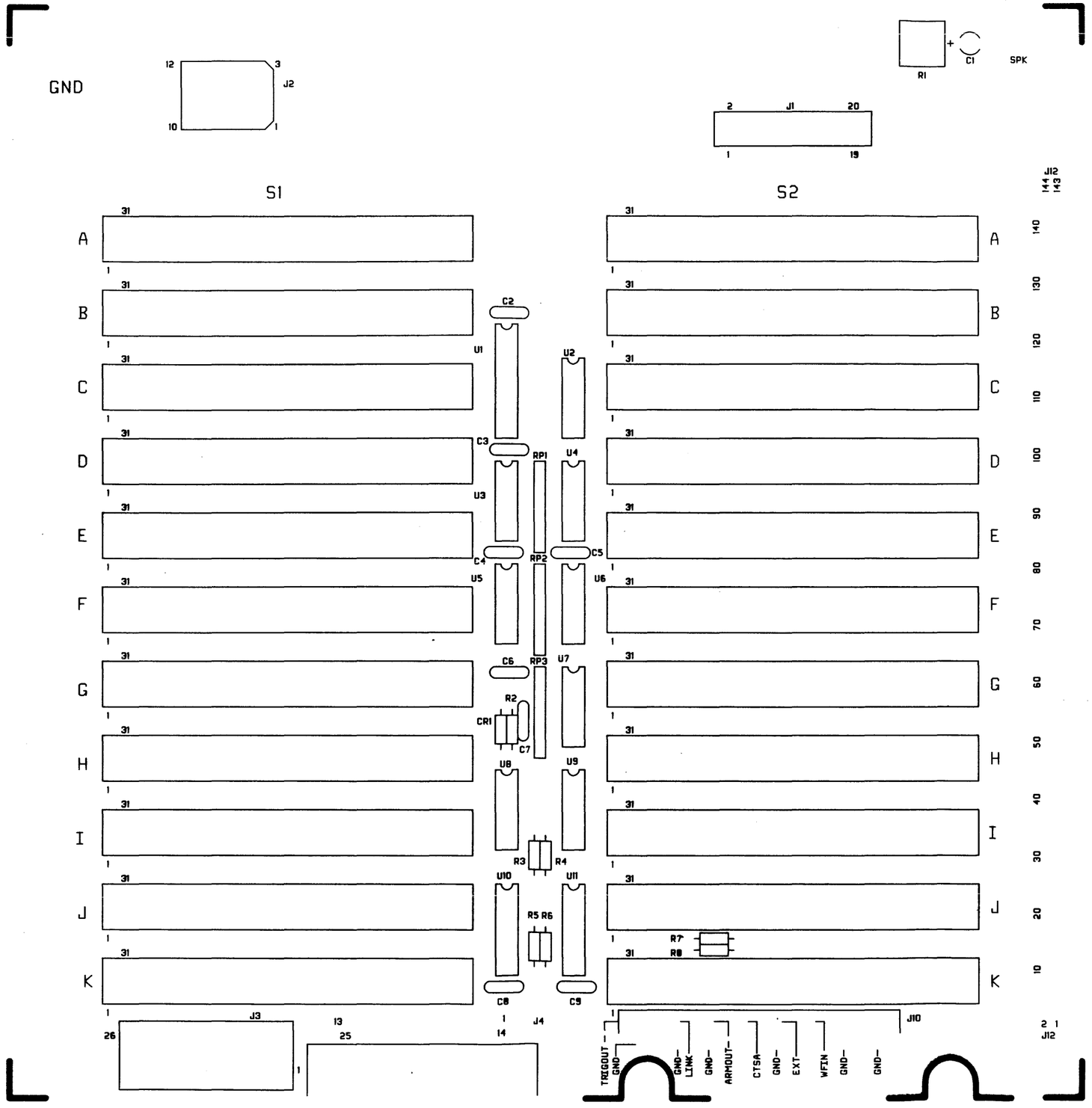
Model 540/532 Trick Card
615-004602

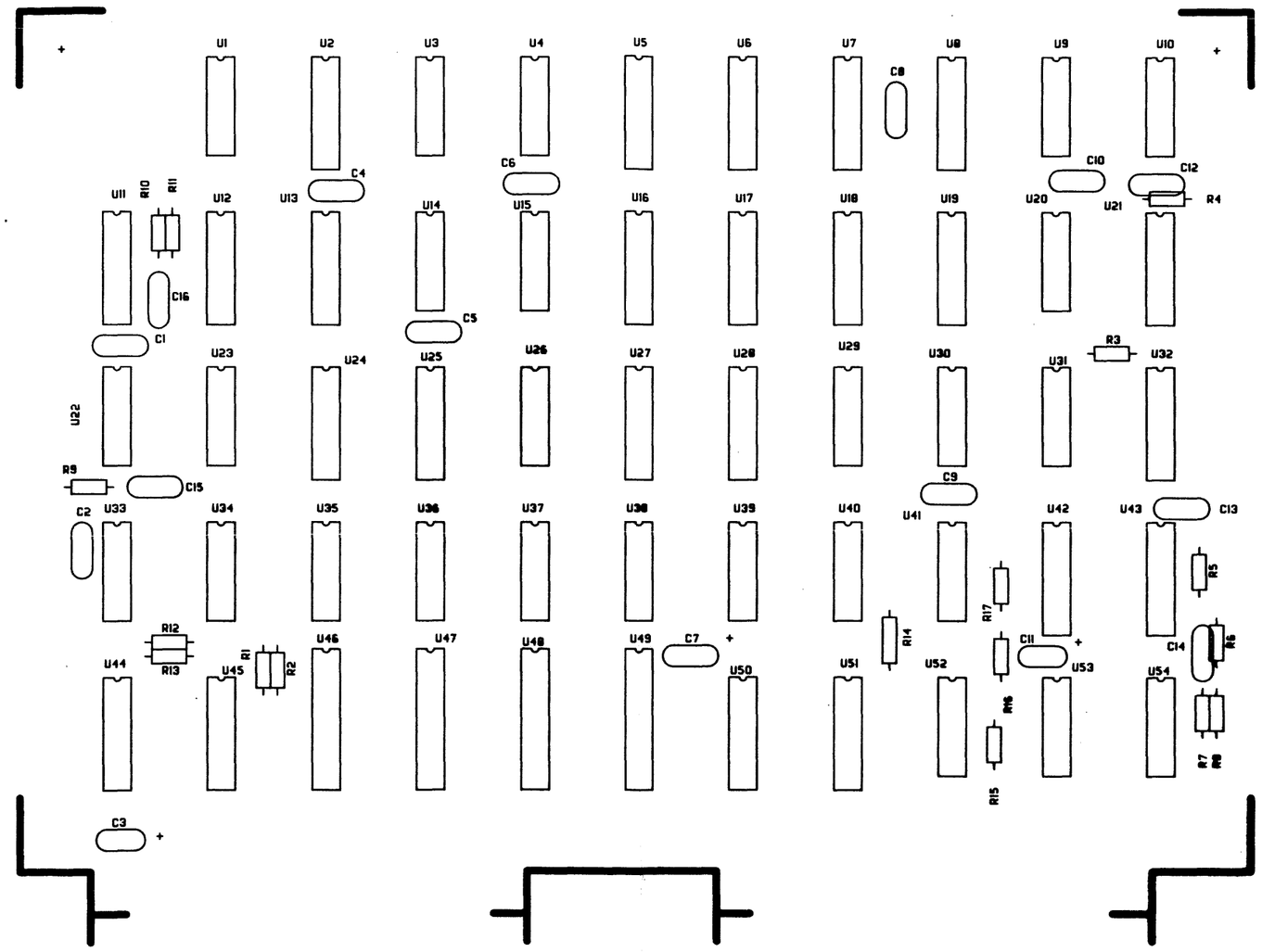
M764 Daughter Board
615-012401

M700/800 Power Supply
615-012201

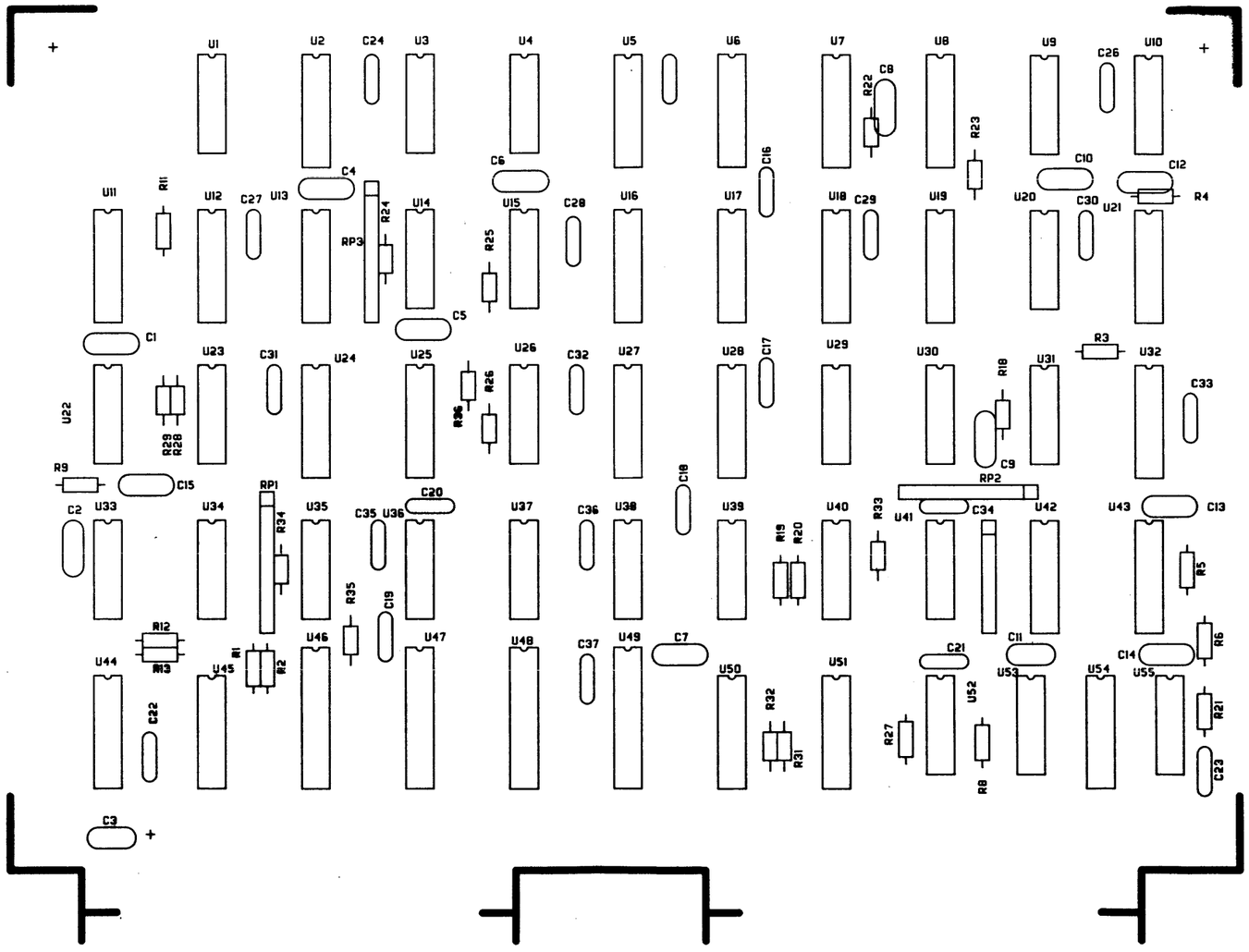


M764 Keyboard
615-012190

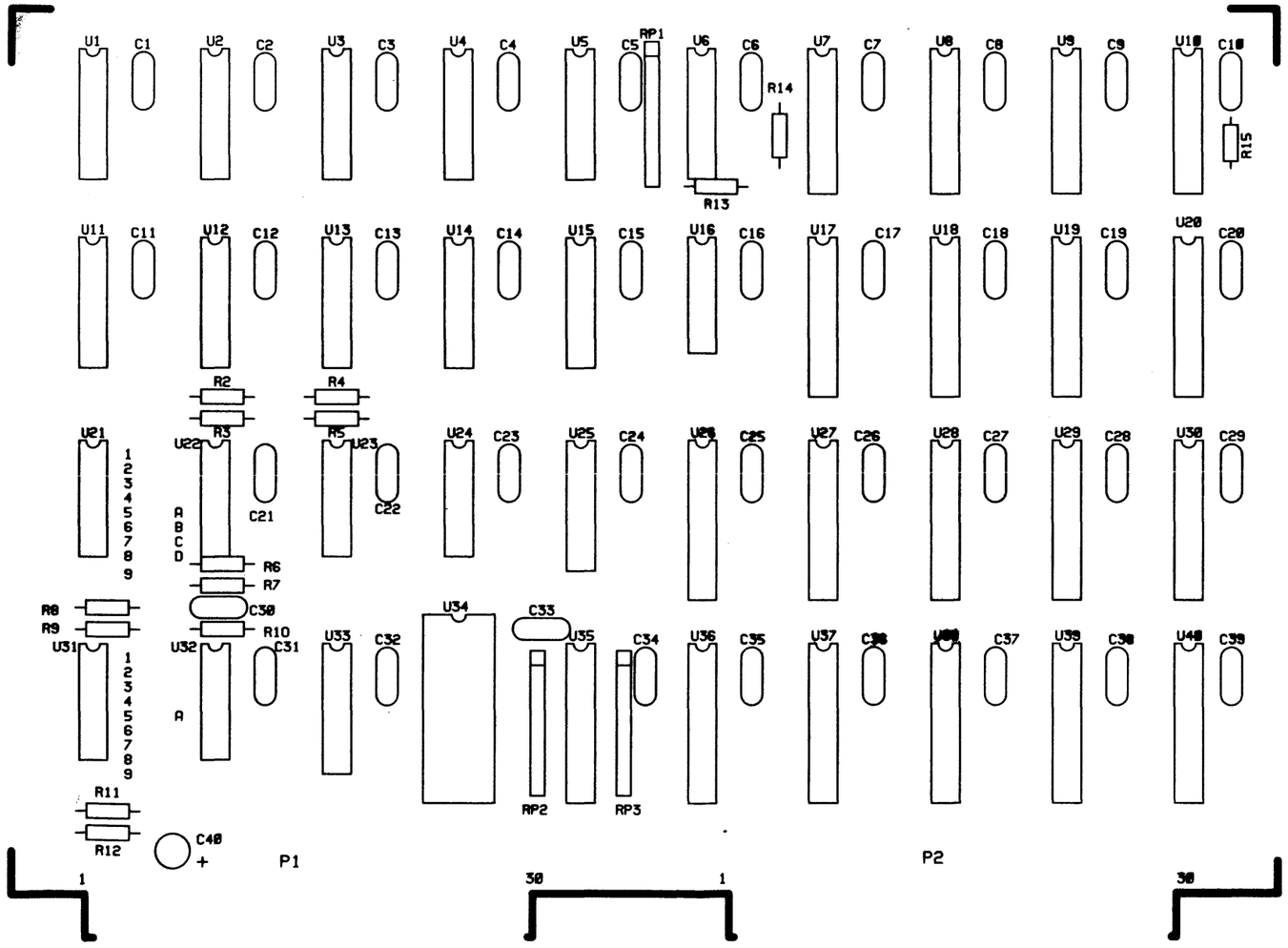

GND
12
3
J2
10
1
R1
C1
SPK
2
J1
20
1
19
S1
S2
J12
144
143
A
B
C
D
E
F
G
H
I
J
K
31
1
140
130
120
110
100
90
80
70
60
50
40
30
20
10
C2
U1
U2
C3
RP1
U4
U3
C4
RP2
C5
U5
U6
C6
RP3
U7
R2
CR1
C7
U8
U9
R3
R4
U10
U11
R5 R6
R7
R8
C8
C9
J3
26
13
25
14
J4
J10
2 1
J12
TRIGOUT
GND
GND
LINK
GND
ARMOUT
CTSA
GND
EXT
WFIN
GND
GND



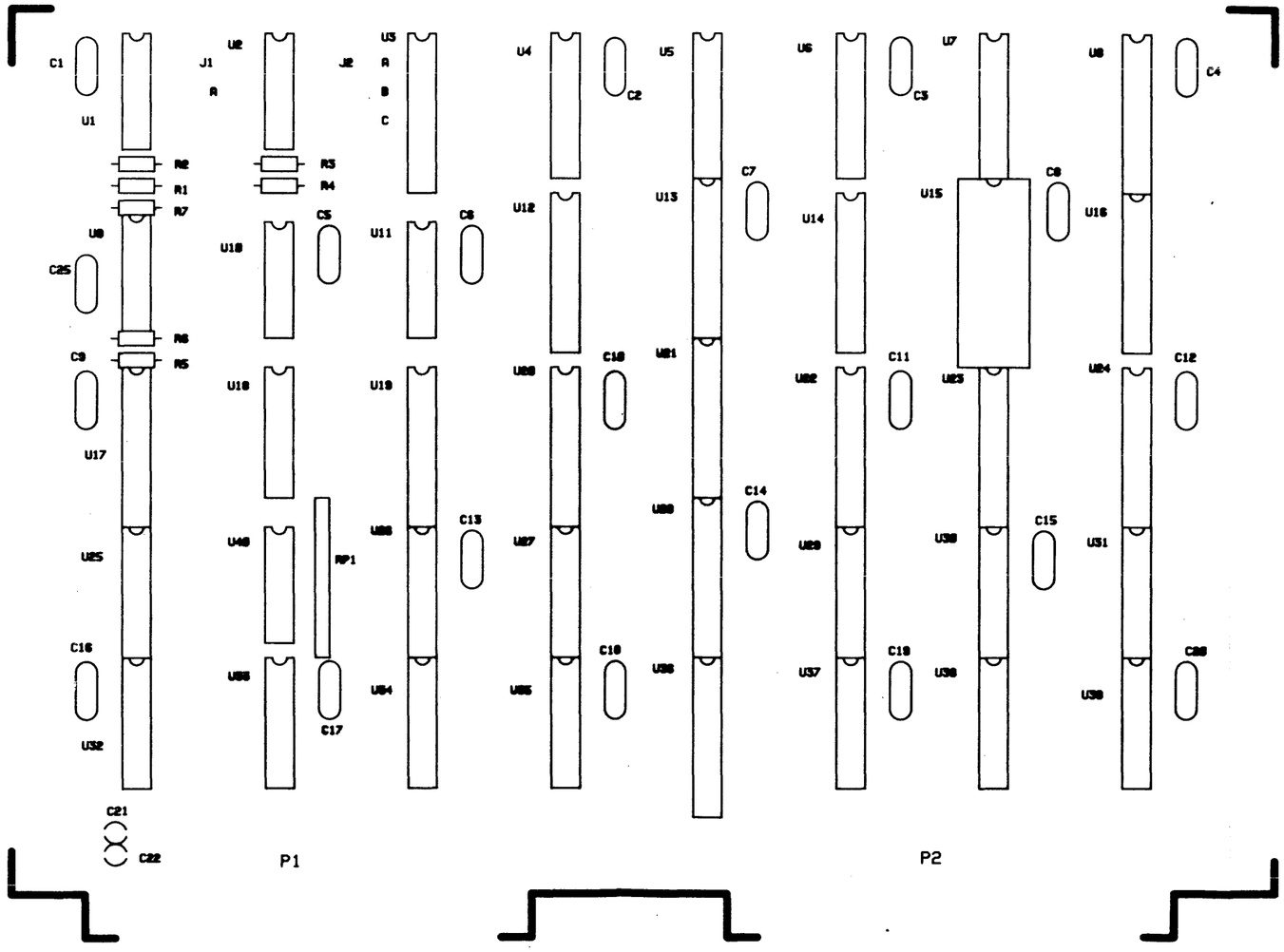
1K State Control (15 MHz) Board
615-012801



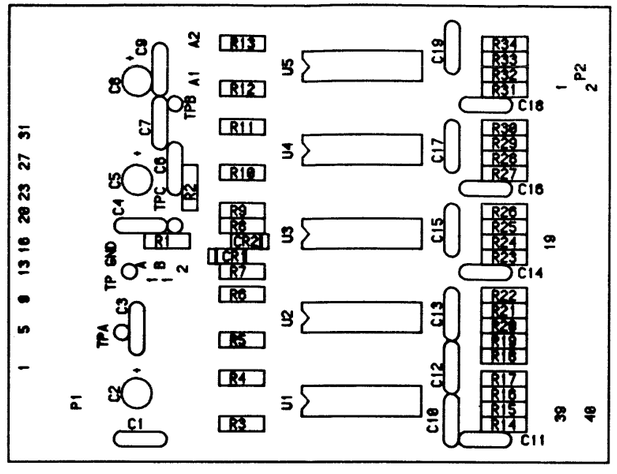
1K State Control (20 MHz) Board
615-036901



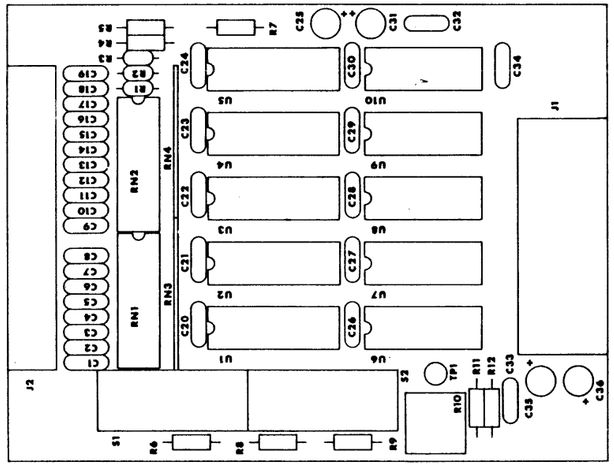
1K State Memory (20 MHz) Board
615-036801



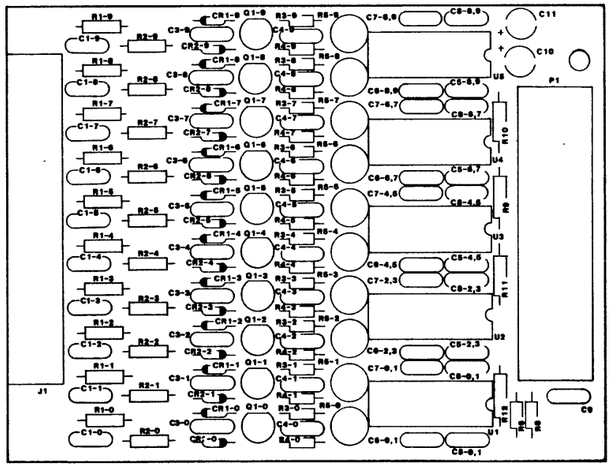
1K State Memory Board
615-012701



M81A Probe
615-031501



Model 51A Probe
616-001502



Model 80 Probe
615-005201

24.1 Diagrams

Diagram	Diagram Number	Page
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1K State Control	166-012801	24-12
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1K State Memory	166-012701	24-20
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M800 State Congtrol	166-036101	24-25
M800 State Memory (25 MHz)	166-036001	24-30
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Timing Memory	166-006501	24-41
800 Timing Control	166-031301	24-45
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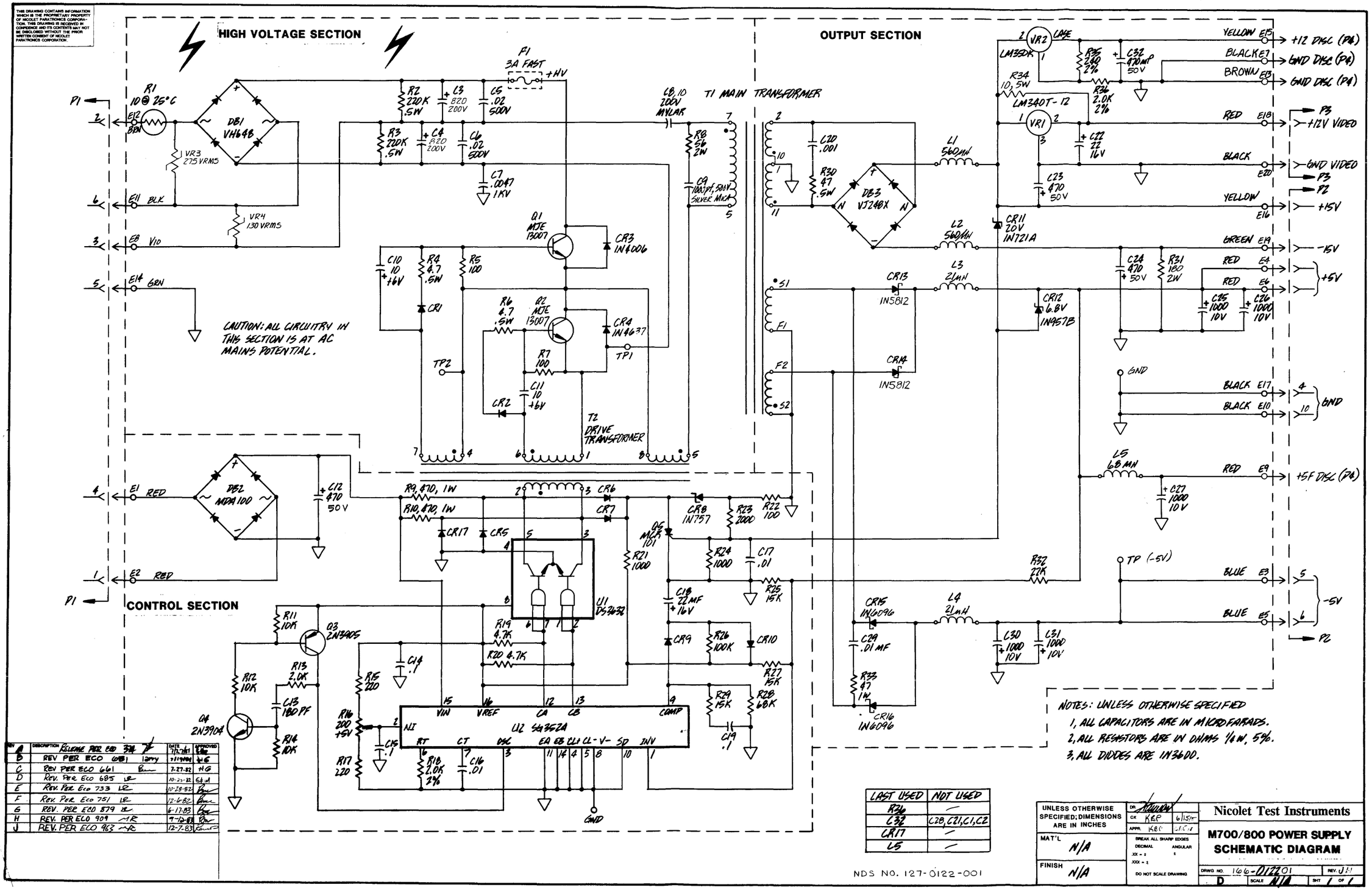
Waveform Board	166-007201	
Disk Ram Controller	166-011201	24-64
Model 540/532 Trick Card	166-004601	24-67
Model 80 Probe	166-005201	24-68
Model 51A Probe	166-001501	24-69
Model 81A Probe	166-031501	24-71



REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECO 324	7/27/81	
B	REV PER ECO 681	7/19/82	HG
C	REV PER ECO 661	7-27-82	HG
D	REV. PER ECO 685	10-25-82	
E	REV. PER ECO 733	10-28-82	
F	REV. PER ECO 751	12-6-82	
G	REV. PER ECO 879	6-17-83	
H	REV. PER ECO 909	9-12-83	
J	REV. PER ECO 963	12-7-83	

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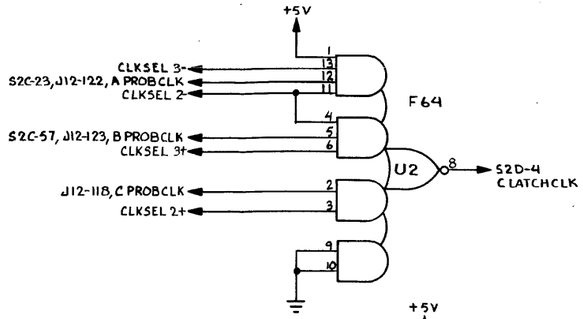
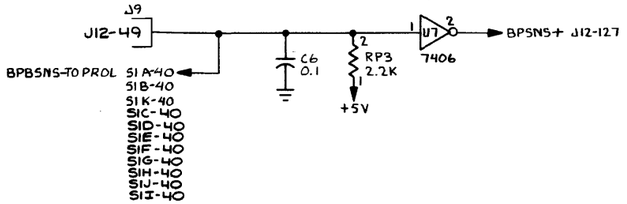
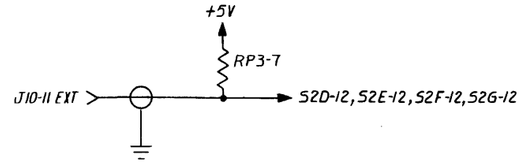
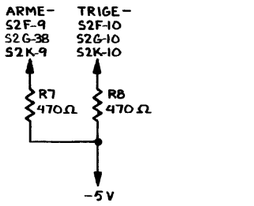
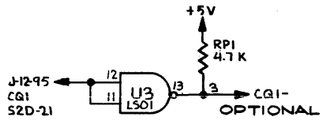
REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECO #38	7/24/81	RBH
B	REV. PER ECO 499	2/15/82	RBH
C	REV PER ECO 477	3-9-82	
D	REV. PER ECO 1084 MR	8-8-84	

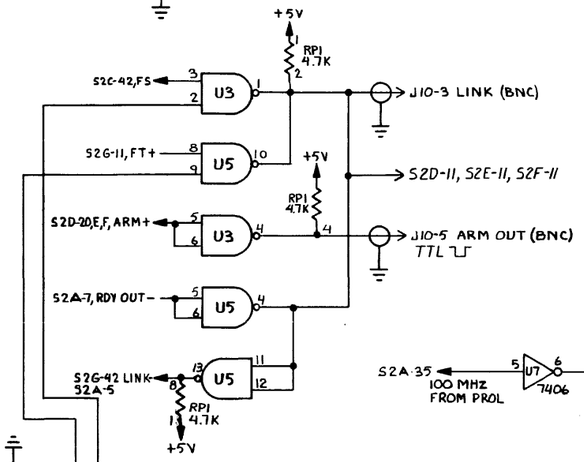


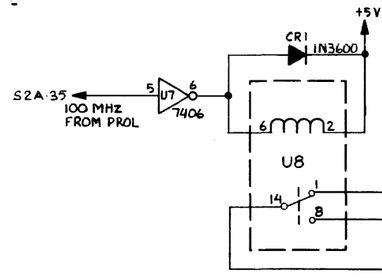


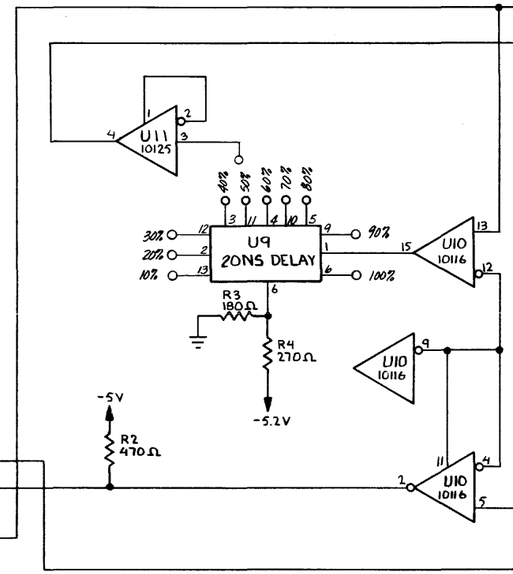


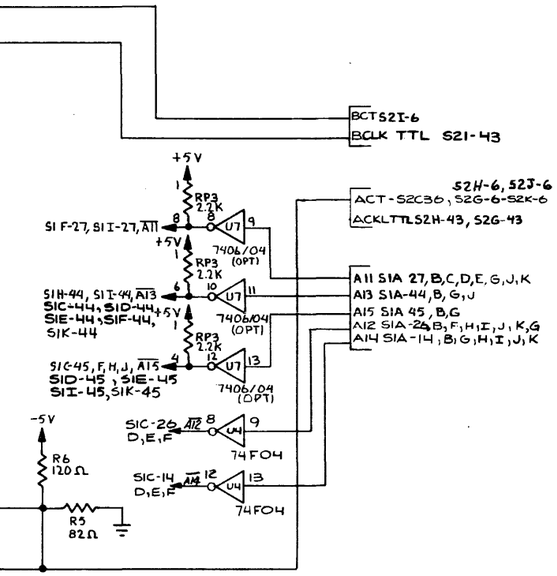


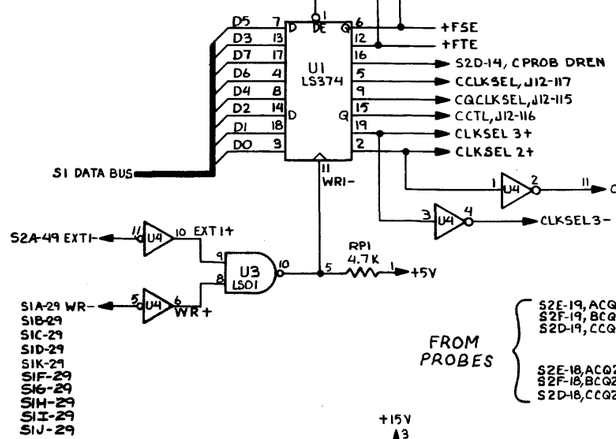


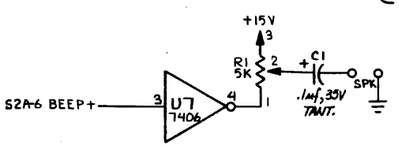


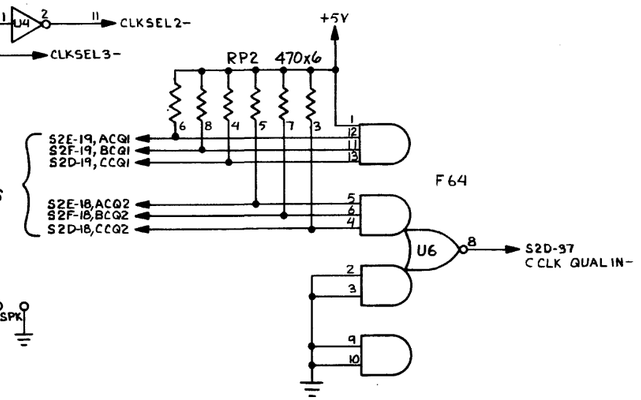


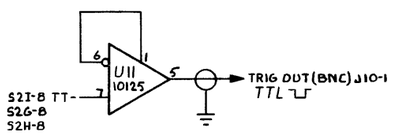












POWER AND GROUND LOCATER CHART					
REF. DES.	TYPE	GND	+5V	-5V	PINS
U1	74LS374	10	20	—	20
U2, U6	74S64	7	14	—	14
U5, U3	74LS01	7	14	—	14
U4	74LS04	7	14	—	14
U7	7406	7	14	—	14
U10	10116	1,16	—	8	16
U11	10125	16	9	8	16

NDS NO. 127-0123-001

10125	U11	2		
74LS01	U5	1		
74LS04	U4	2		
TYPE	REF DES	QTY.	LAST USED	NOT USED
SPARE GATES			REF. DES.	

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES

MAT'L N/A

FINISH N/A

BREAK ALL SHARP EDGES
DECIMAL ANGULAR
XX = ± °
XXX = ±
DO NOT SCALE DRAWING

DR RGH 9-22-81
CK 11-18-81
APPR. 11/25/81

Nicolet Test Instruments

M764 MOTHER BD. SCHEMATIC

DRWG NO. 1006-012301 REV D
D SCALE FULL SHT 1 OF 1

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REV	DESCRIPTION	DATE	APPROVED
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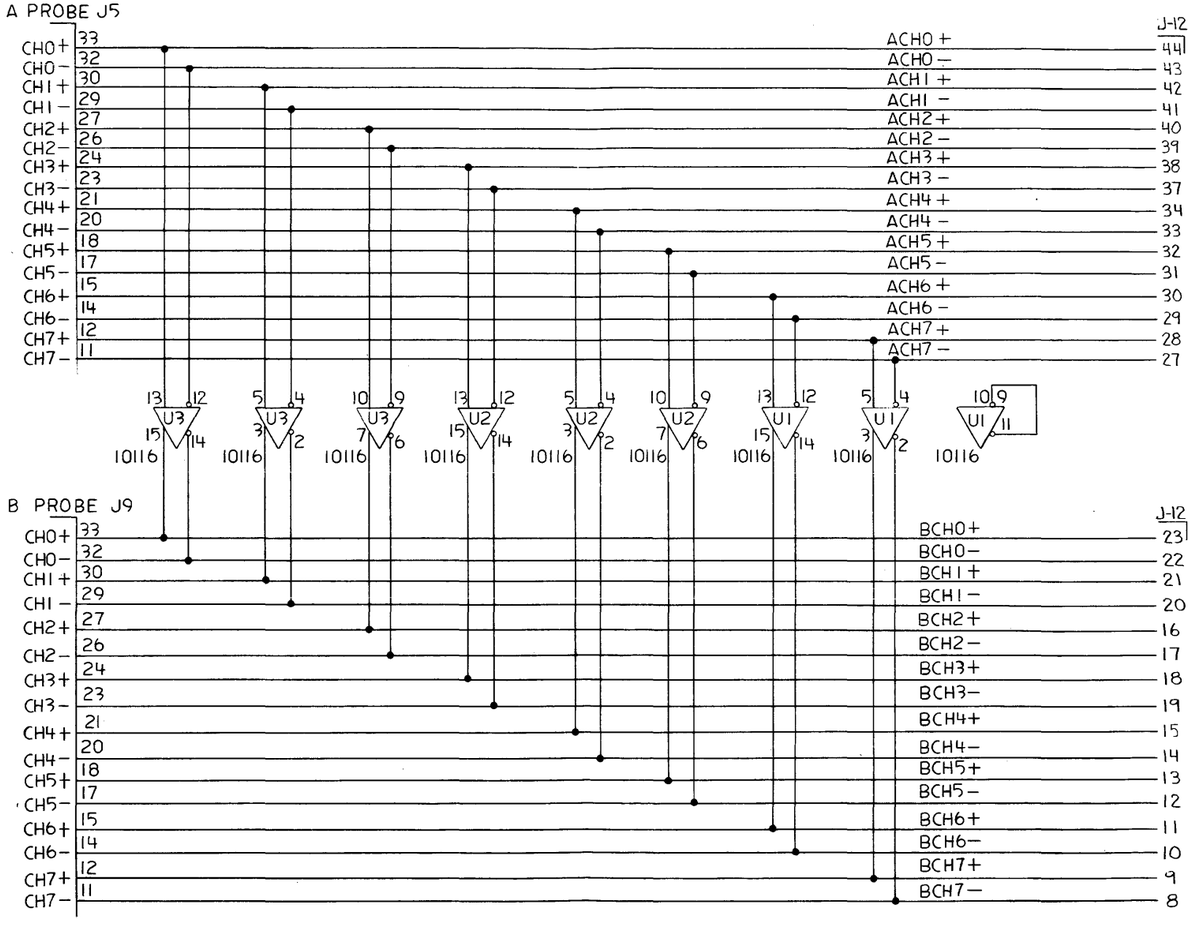
B	REV. PER ECO 635 [illegible]	8-31-82	AG

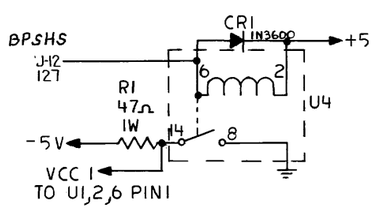


J9	J1, J2, J3, J4
CR1	
R1	
C3	
U4	
LAST USED	NOT USED
REF. DESIGNATORS	

POWER AND GROUND LOCATER CHART					
REF. DES.	TYPE	GND	+5V	−5V	PINS
U1, U2, U3	10116	1, 16	—	8	16

NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE WIRE LIST FOR J6, J7, J8 INTEL CONNECTIONS.
2. THIS SCHEMATIC TO BE USED WITH 126-0124-0001 REV.'s "A" & "B" PC FAB.



NDS NO. 127-0124-001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR RG.	9-29-81	Nicolet Test Instruments
	CK [illegible]	11-18-81	M764 DAUGHTER BD. SCHEMATIC
	APPR. GFM	11/30/81	
MAT'L N/A	BREAK ALL SHARP EDGES DECIMAL XX = ± XXX = ± ANGULAR ±		
FINISH N/A	DO NOT SCALE DRAWING		DRWG NO. 166-012401 REV. B
			D SCALE NONE SHT 1 OF 1

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REV	DESCRIPTION	DATE	APPROVED
A	RELEASE ECO 349	9/7/78	KKP
B	REV PER ECO 533	9/	
C	REV. PER ECO 5% LR	3-33 BA	
D	REV PER ECO 591 LR	4-26-83	
E	REV. PER ECO 1026 MTC	2-24-84	

DATA ACCEPTED 4 (J1) — 47Ω R6 — R5 4.7K — +5V — C6 330 PF, 1KV — U2 ½ 74LS74 (CLR, PR, D, CLK, Q) — RP1 1K SIP — U3 LS33 — J1-13 — U3 LS33 — 1K SIP RP1 — +5V

U8 555 — R11 1.5K — R12 680 — C17 .01 — C19 .01 — +5V

J1-3 — U3 LS33 — REBOOT — U2 ½ 74LS74 — R3 100K — C3 33 6V TANT — U1 ½ 9602 — C1 .01 — REBOOT — R1 470 — +5V

19, 20, 1, 2 — +5V SOURCE .01 C5, C7, C8, C9, C10, C11, C13, C15 25V DISC 1 PER I.C. PACKAGE — *C2 22 16V ALUM. — +5 — R2 330 — D1

C16 .01 25V — SHIFT — R8 4.7K — CAPS LOCK — R7 4.7K — CTRL — CR2 IN3600 — CR3 IN3600

U4 MMI 6348 512×8 PROM — J1 — 1K X 7 PLCS USE 10 PIN SIP — RP1 — R10 68K — C12 33 16V TANT — CR1 1N4148 — RESET

U7 OKI MSM3914A — SAMPLE CLK — SHIFT SET — SHIFT BIT — SAMPLE ACC — D0 D1 D2 D3 D4 D5 D6 D7 — SPD1 SPD2 SPD3 — RES CLR — CUT — A R — SHIFT CUT — LOAD 10 11 12 13 — Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

SEE DETAIL A

BREAK	1	2	3	4	5	6	7	8	9						LEFT BLANK	F1
	Q	W	E	R	T	Y	U	I	O						RIGHT BLANK	F2
	A	S	D	F	G	H	J	K	L						@	F3
	Z	X	C	V	B	N	M	,	.		–				]	F4
	ESC				Q			\	BACK SPACE		^				:	F5
				[	P											F6
				TAB	;			RET								F7
				DEL	/	SPACE		LF								

4.7K X 8* — * USE 10 PIN SIP. RP2

U5 74LS138 — Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 — C B A

U6 74LS138 — Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 — C B A

DETAIL A — TYP. 66 PLCS — KEYSWITCH

U10 LS132 — U13 LS33 — R13 820 — 1UF 10V TANT — R14 220K — 10.25V — C18 — U9 9602 — RP2 4.7K SIP — U13 LS33 — REBOOT — R9 4.7K — U1 ½ 9602 — CLKKEY — R4 47K — C4 1UF 35V TANT

3. THIS SCHEMATIC TO BE USED WITH REVISION('S) "C" P.C.B. FABRICATION.
2. ALL RESISTOR VALUES ARE IN OHMS.
1. ALL CAPACITOR VALUES ARE IN UF.
NOTES: UNLESS OTHERWISE SPECIFIED.

NDS NO. 1[illegible]-0121-001

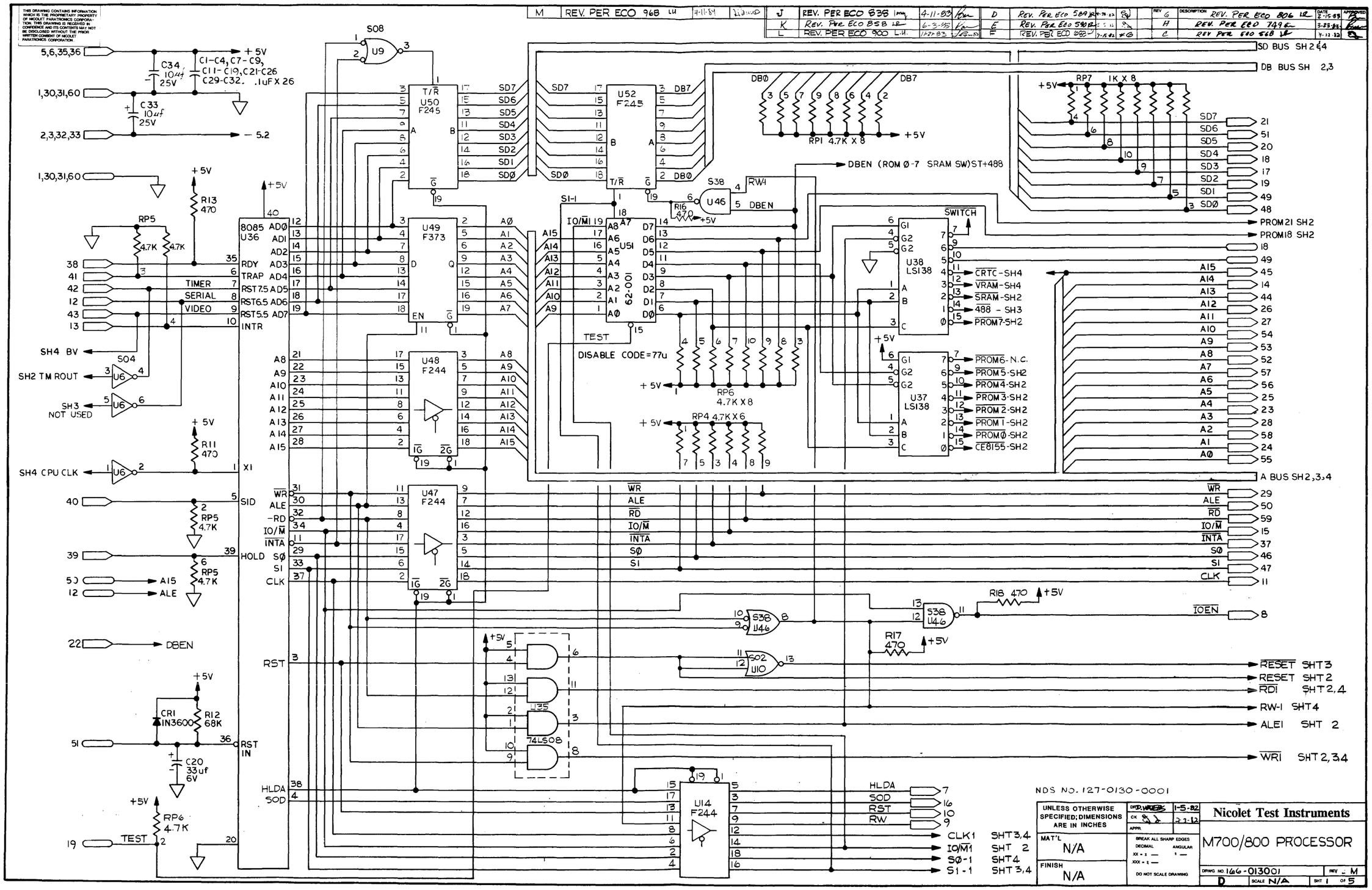
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES — MAT'L N/A — FINISH N/A — BREAK ALL SHARP EDGES — DO NOT SCALE DRAWING

DR [illegible] 9-25-8 — CK KKP 9-[illegible]-81 — APPR KKP 9-[illegible]-81

Nicolet Test Instruments

M764 KEYBOARD SCHEMATIC

DRWG NO 1660-021101 — REV E — D — SCALE NONE — SHT 1 OF 1



M REV. PER ECO 968 LH 4-11-84
J REV. PER ECO 838 4-11-83
K REV. PER ECO 858 6-3-83
L REV. PER ECO 900 L.H. 11-21-83
D REV. PER ECO 589
E REV. PER ECO 590
F REV. PER ECO 683
REV G DESCRIPTION REV. PER ECO 806 DATE 2-15-83
H REV. PER ECO 749 3-23-83
C REV. PER ECO 568 4-12-82
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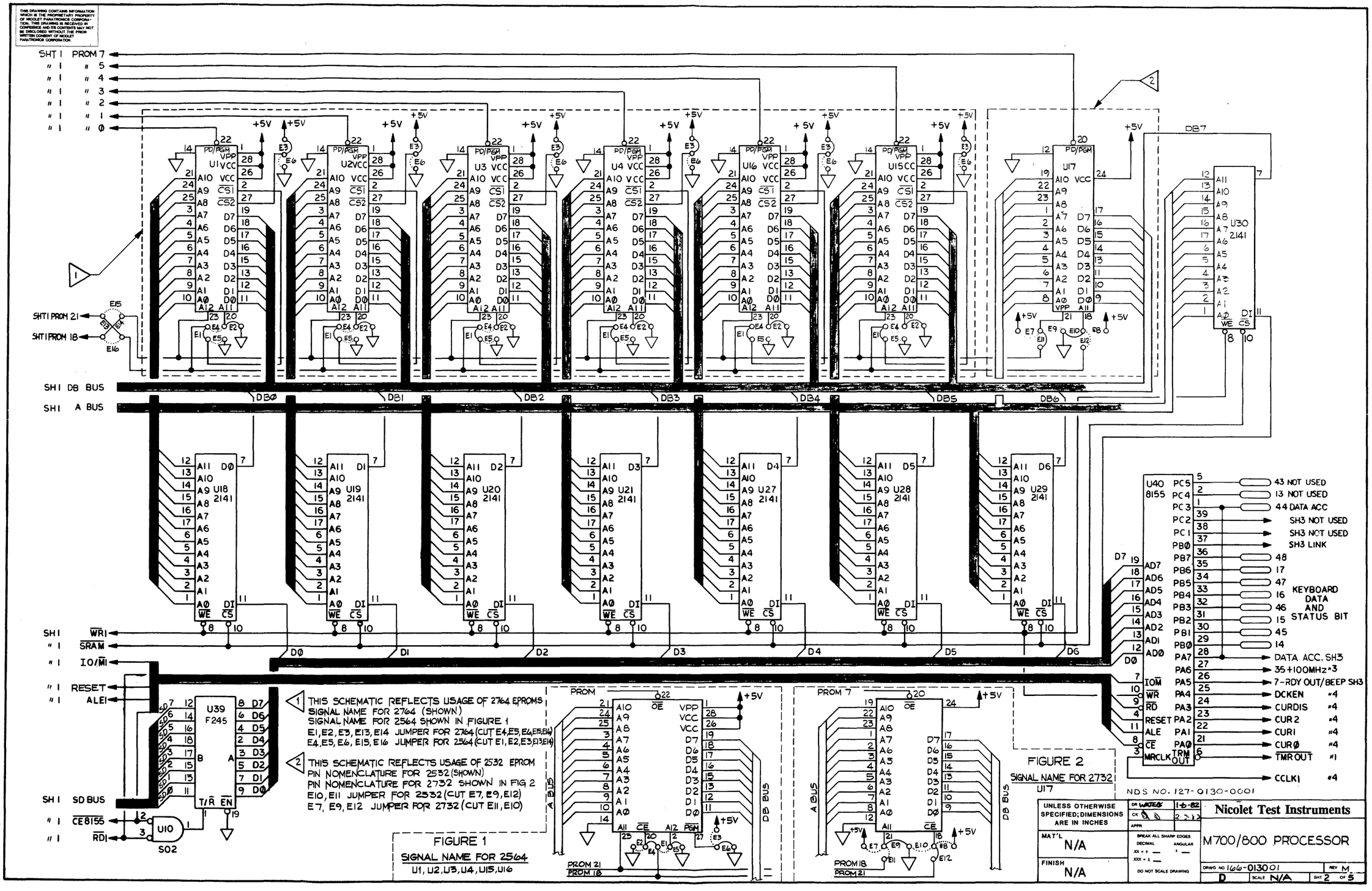
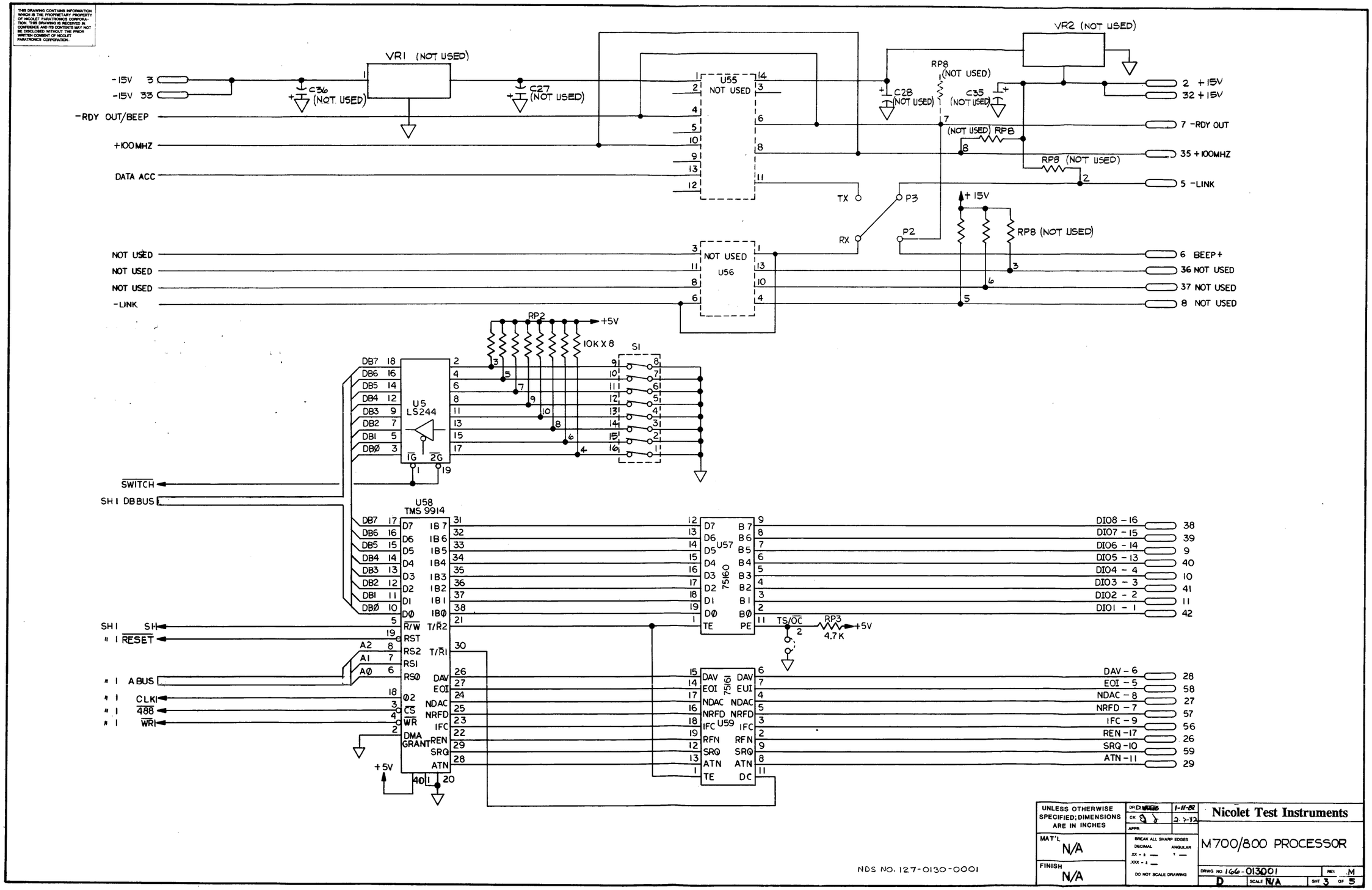
SD BUS SH 2 & 4
DB BUS SH 2,3
DBEN (ROM Ø-7 SRAM SW) ST+488
PROM21 SH2
PROM18 SH2
A BUS SH2,3,4
DISABLE CODE=77u
TIMER
SERIAL
VIDEO
SH4 BV
SH2 TM ROUT
SH3 NOT USED
SH4 CPU CLK
DBEN
RESET SHT3
RESET SHT2
RDI SHT2,4
RW-1 SHT4
ALE1 SHT 2
WRI SHT 2,3,4
CLK1 SHT3,4
IO/M1 SHT 2
SØ-1 SHT4
S1-1 SHT 3,4
NDS NO. 127-0130-0001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
Nicolet Test Instruments
M700/800 PROCESSOR
DRWG NO. 166-013001
REV M
SCALE N/A
SHT 1 OF 5

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF NICOLET PARATRONICS CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF NICOLET PARATRONICS CORPORATION.




THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF NICOLET PARATRONICS CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF NICOLET PARATRONICS CORPORATION.
VR1 (NOT USED)
VR2 (NOT USED)
-15V 3
-15V 33
C36 (NOT USED)
C27 (NOT USED)
U55 NOT USED
C28 (NOT USED)
C35 (NOT USED)
RP8 (NOT USED)
-RDY OUT/BEEP
+100MHZ
DATA ACC
2 +15V
32 +15V
7 -RDY OUT
35 +100MHZ
5 -LINK
TX
RX
P3
P2
+15V
RP8 (NOT USED)
NOT USED
NOT USED
NOT USED
-LINK
U56 NOT USED
6 BEEP+
36 NOT USED
37 NOT USED
8 NOT USED
RP2
+5V
10K X 8
S1
U5 LS244
SWITCH
SH1 DBBUS
U58 TMS 9914
U57 75160
U59 75161
TS/OC
RP3 4.7K
SH1 SH
" 1 RESET
" 1 ABUS
" 1 CLK1
" 1 488
" 1 WR1
DIO8 - 16
DIO7 - 15
DIO6 - 14
DIO5 - 13
DIO4 - 4
DIO3 - 3
DIO2 - 2
DIO1 - 1
DAV - 6
EOI - 5
NDAC - 8
NRFD - 7
IFC - 9
REN - 17
SRQ - 10
ATN - 11
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING
Nicolet Test Instruments
M700/800 PROCESSOR
DRWG NO 166-013001
REV M
SCALE N/A
SHT 3 OF 5
NDS NO. 127-0130-0001

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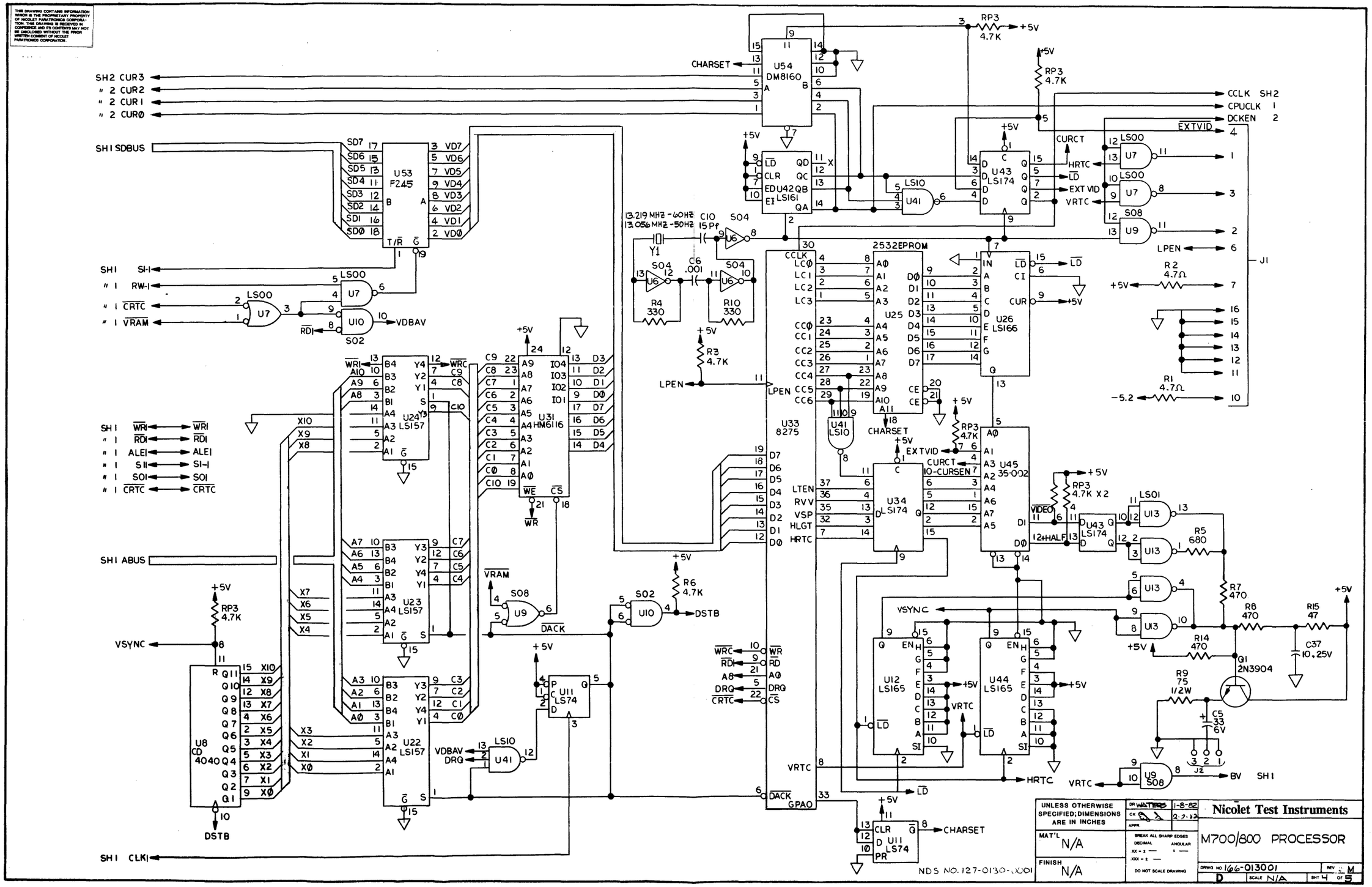

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF NICOLET PARATRONICS CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF NICOLET PARATRONICS CORPORATION.

REV	DESCRIPTION	DATE	APPROVED

SPARE GATES		
REF. DES.	TYPE	PIN NO.

REFERENCE DESIGNATOR	
LAST USED	NOT USED
RP7	RP8
CR1	
C37	C27, C28
R18	
U59	U32, U55, U56
Q1	

POWER & GROUND LOCATOR CHART						
REF. DES.	TYPE	GND	+5V	-5V		PIN NO.
U36	8085A-2	20	40			40
U10	S02	7	14			14
U6	S04	7	14			14
U9	S08	7	14			14
U46	S38	7	14			14
U7	LS00	7	14			14
U13	LS01	7	14			14
U41	LS10	7	14			14
U11	LS74	7	14			14
U37, U38	LS138	8	16			16
U22, U23, U24	LS157	8	16			16
U42	LS161	8	16			16
U12, U44	LS165	8	16			16
U26	LS166	8	16			16
U34, U43	LS174	8	16			16
U5	LS244	10	20			20
U47, U48, U14	F244	10	20			20
U39, U50, U52, U53	F245	10	20			20
U49	F373	10	20			20
U51	62-001	10	20			20
U45	35-002					16
U18, U19, U20, U21, U27, U28, U29, U30	2141					18
U8	4040					16
U40	8155					40
U33	P8275					40
U57	75160					20
U59	75161					20
U31	HM6116	12	24			24
U58	TMS 9914	20	40			40
U25, U17	2532/2732					24
U1, U2, U3, U4, U15, U16	2764/2564	14	28			28
U35	74LS08	7	14			14
U54	DM8160		16			16

S1 — CONNECTOR — S2

NDS NO. 127-0130-0001

ITEM / LTR	P/N	DESCRIPTION	QTY

MATERIAL: N/A — DRN BY UDAY — DATE 11-15-83 — CHK'D — DATE

FINISH: N/A — ENG — DATE — MFG — DATE

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; RESISTORS ARE IN OHMS; CAPACITORS ARE IN uf

THIS SCHEMATIC TO BE USED WITH REVISION(S) 'D' PCB FABRICATION

DECIMAL .XX ± .XXX ± — ANGULAR ±

BREAK ALL SHARP EDGES

DO NOT SCALE DRAWING

Nicolet Test Intruments

DESCRIPTION: M700/800 PROCESSOR

DRAWING NO 166-013001 — REV M

D — SCALE N/A — SHT 5 OF 5

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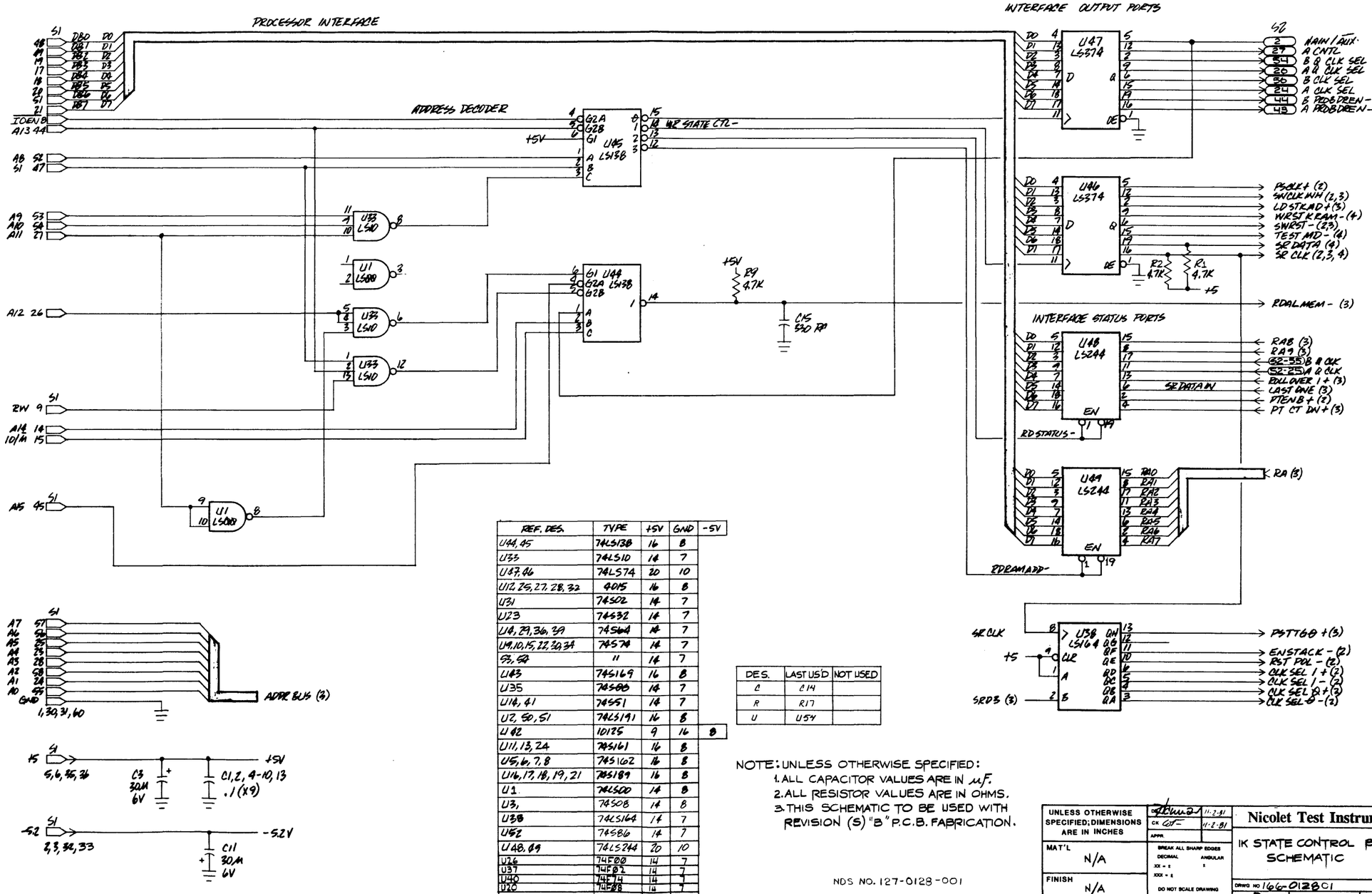
REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECO 501	2.17	
B	REV PER ECO 625 LR	6/2	
C	REV PER ECO 1078 MC	4-11-84	
D	REV PER ECO 1200 MC	5-29-84	



REF. DES.	TYPE	+5V	GND	-5V
U44, 45	74LS138	16	8	
U33	74LS10	14	7	
U47, 46	74LS74	20	10	
U12, 25, 27, 28, 32	4015	16	8	
U31	74S02	14	7	
U23	74S32	14	7	
U4, 29, 36, 39	74S64	14	7	
U9, 10, 15, 22, 30, 34	74S74	14	7	
S3, S2	11	14	7	
U43	74S169	16	8	
U35	74S00	14	7	
U16, 41	74S51	14	7	
U2, 50, 51	74LS191	16	8	
U 82	10125	9	16	8
U11, 13, 24	74S161	16	8	
U5, 6, 7, 8	74S162	16	8	
U16, 17, 18, 19, 21	74S189	16	8	
U1	74LS00	14	8	
U3,	74S08	14	8	
U38	74LS164	14	7	
U52	74S86	14	7	
U48, 49	74LS244	20	10	
U26	74F00	14	7	
U37	74F02	14	7	
U40	74F74	14	7	
U20	74F08	14	7	

DES.	LAST USED	NOT USED
C	C14	
R	R17	
U	U54	

NOTE: UNLESS OTHERWISE SPECIFIED:
1. ALL CAPACITOR VALUES ARE IN μF.
2. ALL RESISTOR VALUES ARE IN OHMS.
3. THIS SCHEMATIC TO BE USED WITH REVISION (S) "B" P.C.B. FABRICATION.

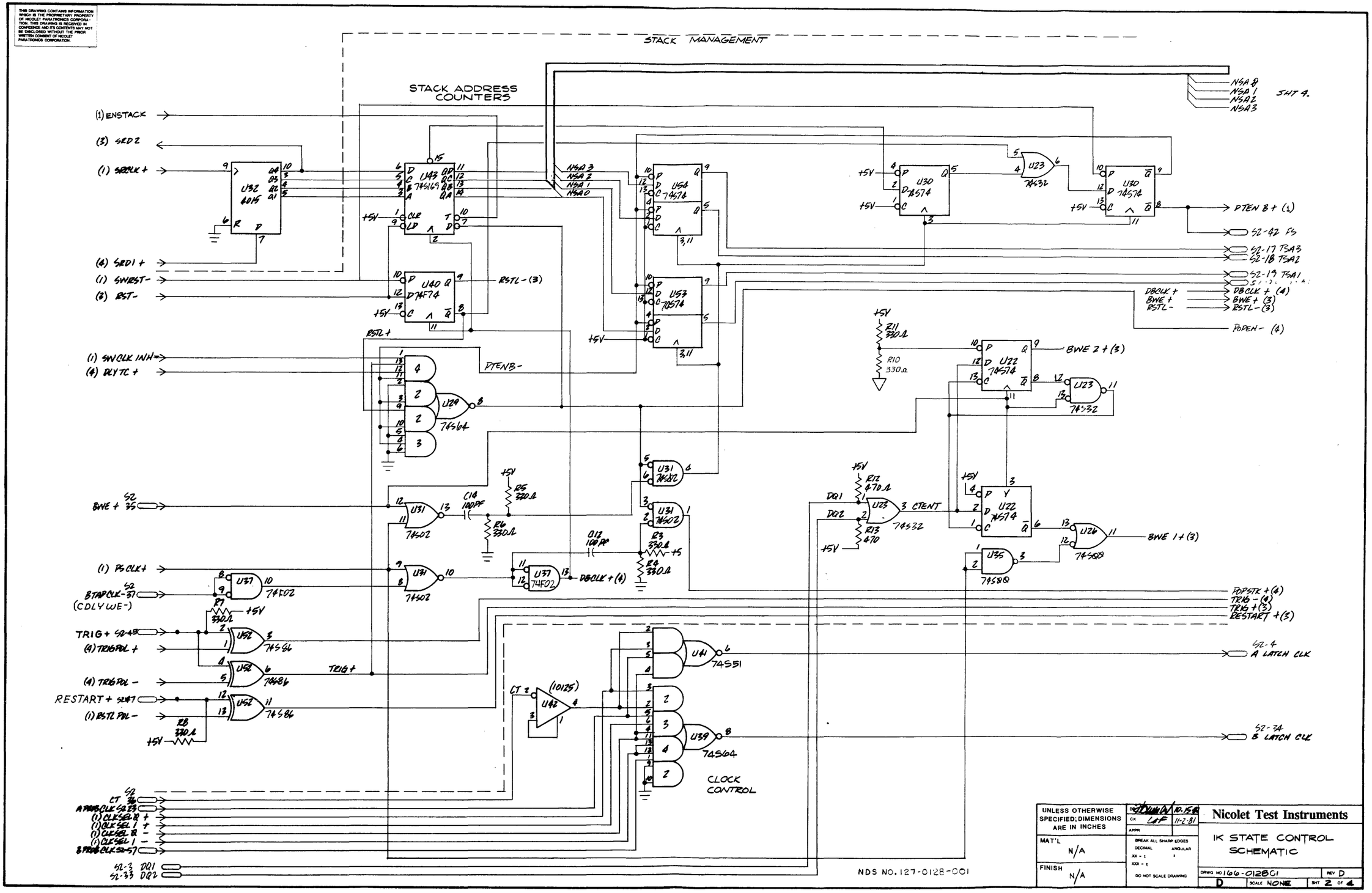
NDS NO. 127-0128-001

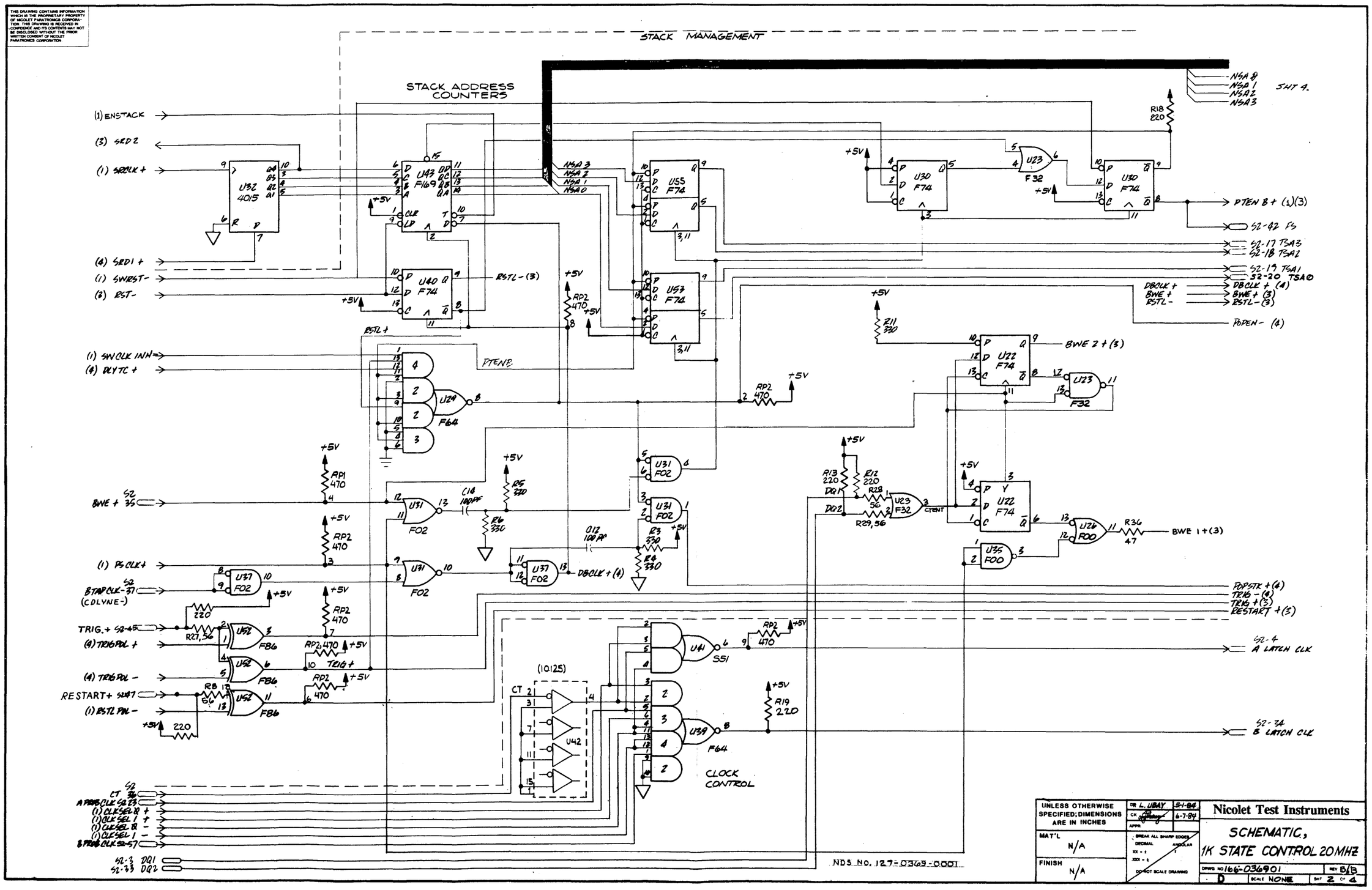
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
BREAK ALL SHARP EDGES
DECIMAL XX = ± XXX = ± ANGULAR ±
DO NOT SCALE DRAWING
DR 11-2-81
CK 11-2-81
APPR

Nicolet Test Instruments

IK STATE CONTROL BOARD SCHEMATIC

DRWG NO 166-0128-01 REV D
D SCALE NONE SHT 1 OF 4


STACK MANAGEMENT
STACK ADDRESS COUNTERS
(1) ENSTACK
(3) SRD2
(1) SRCLK +
(4) SRD1 +
(1) SWRST-
(3) RST-
(1) SWCLK INH
(4) DLYTC +
BWE + S2 35
(1) PSCLK +
BTAPCLK- S2 37
(CDLYWE-)
TRIG + S2-45
(4) TRIGPOL +
(4) TRIGPOL -
RESTART + S2-47
(1) RSTL POL -
CT S2 36
APROBCLK S2-23
(1) CLKSEL 0 +
(1) CLKSEL 1 +
(1) CLKSEL 0 -
(1) CLKSEL 1 -
BPROBCLK S2-57
S2-3 DQ1
S2-33 DQ2
NSA 0
NSA 1
NSA 2
NSA 3
SHT 4.
PTEN B + (1)
S2-42 FS
S2-17 TSA3
S2-18 TSA2
S2-19 TSA1
DBCLK +
BWE +
RSTL -
DBCLK + (4)
BWE + (3)
RSTL - (3)
POPEN - (4)
BWE 2 + (3)
BWE 1 + (3)
POPSTK + (4)
TRIG - (4)
TRIG + (3)
RESTART + (3)
S2-4 A LATCH CLK
S2-34 B LATCH CLK
RSTL - (3)
RSTL +
PTENB -
DBCLK + (4)
CTENT
CLOCK CONTROL
NDS NO. 127-0128-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING
Nicolet Test Instruments
IK STATE CONTROL SCHEMATIC
DRWG NO 166-0128C1
REV D
SCALE NONE
SHT 2 OF 4



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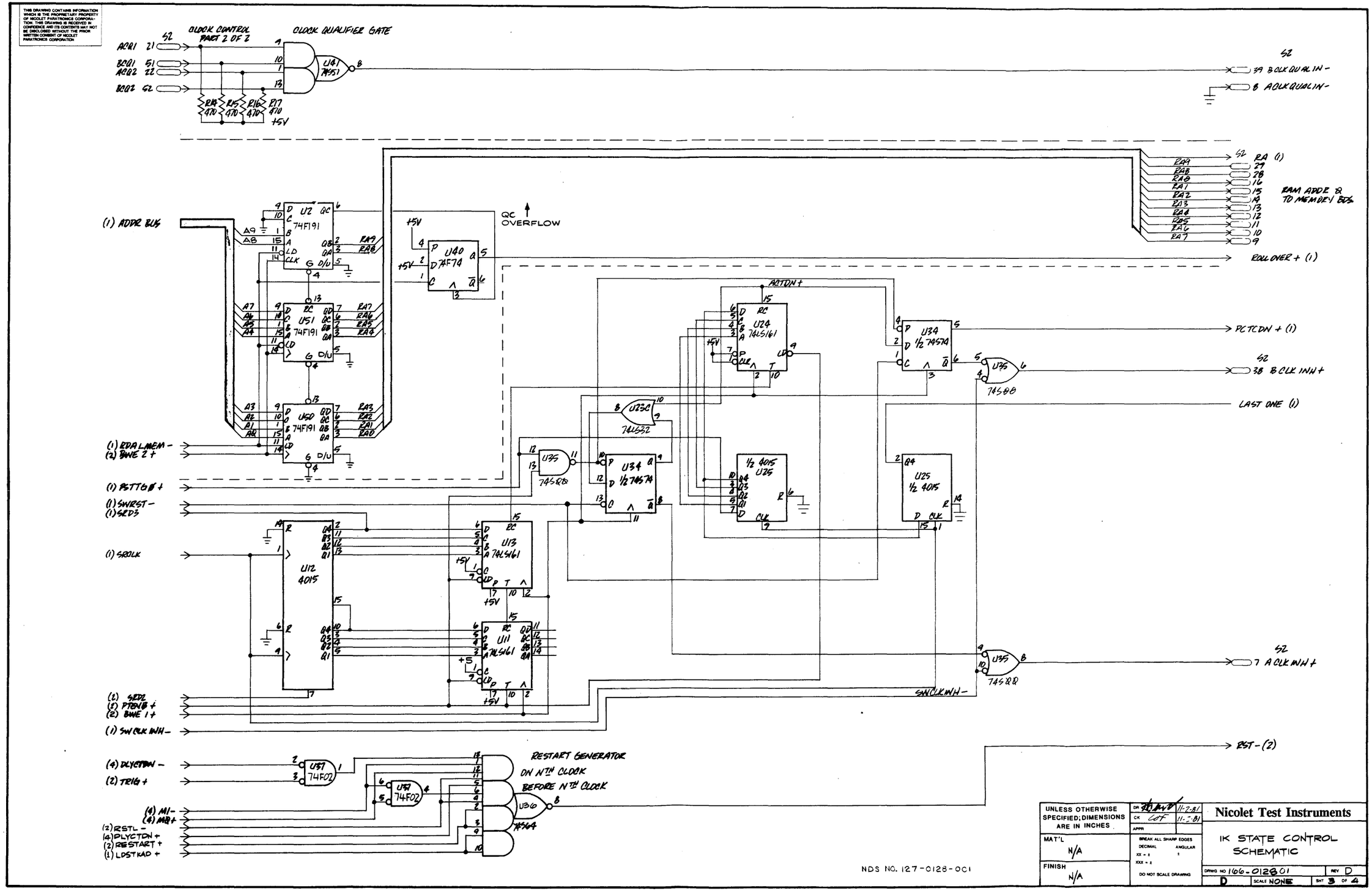

CLOCK CONTROL PART 2 OF 2
CLOCK QUALIFIER GATE
ACQ1 21
BCQ1 51
ACQ2 22
BCQ2 52
U41 74S51
R14 470
R15 470
R16 470
R17 470
+5V
39 BCLK QUAL IN -
8 ACLK QUAL IN -
RA (1)
RAM ADDR Q TO MEMORY BDS
ROLL OVER + (1)
(1) ADDR BUS
U2 74F191
U51 74F191
U50 74F191
U40 74F74
QC OVERFLOW
ACTDN +
U24 74LS161
U34 1/2 74S74
U35 74S00
PCTCDN + (1)
38 BCLK INH +
LAST ONE (1)
U23C 74LS32
U35 74S00
U34 1/2 74S74
1/2 4015 U25
U25 1/2 4015
(1) RDA LMEM -
(2) BWE 2 +
(1) PSTTGØ +
(1) SWRST -
(1) SRD3
(1) SRCLK
U12 4015
U13 74LS161
U11 74LS161
U35 74S00
7 ACLK INH +
SWCLK INH -
(2) SRD2
(2) PTENB +
(2) BWE 1 +
(1) SWCLK INH -
RST - (2)
(4) DLYCTDN -
(2) TRIG +
U37 74F02
U37 74F02
RESTART GENERATOR
ON NTH CLOCK
BEFORE NTH CLOCK
U36 74S64
(4) MI -
(4) MQ +
(2) RSTL -
(4) DLYCTDN +
(2) RESTART +
(1) LDSTKAD +
NDS NO. 127-0128-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
DR 11-2-81
CK 11-2-81
APPR
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
IK STATE CONTROL SCHEMATIC
DRWG NO 166-012801
REV D
D
SCALE NONE
SHT 3 OF 4

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DELAY MODE CONTROL PART 1

DELAY MODE RAM

INTERFACE SHIFT REGISTAR PART 1 OF 4

(1) TESTMD-

(2) SRDI+

(2) RDPSTK+

(1) SR CLK

(1) SR DATA

NSA3
(2) NSA2
(2) NSA1
NSA0
(1) WRSTKRAM+
(2) TRIG-
(2) POPEN-
(2) DBCLK+

M1- (2)
MB+ (3)
SRDI+ (2)

SRDH

DLYTC+ (2)

BEFORE NTH CLOCK
NOT ON NTH CLOCK

TRIG POL+ (2)
TRIG POL- (2)

DLYCTDN- (3)

DLYCTDN+ (3)

DELAY MODE CONTROL PART 2 OF 2

TRIG-

NDS NO. 127-0128-001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR		10-15-81
	CK		11-2-81
	APPR		
MAT'L N/A	BREAK ALL SHARP EDGES	DECIMAL	ANGULAR
		XX ±	±
FINISH N/A		XXX ±	
	DO NOT SCALE DRAWING		

Nicolet Test Instruments

IK STATE CONTROL SCHEMATIC

DRWG NO 1166-0128C1 REV D

D SCALE NONE SHT 4 OF 4

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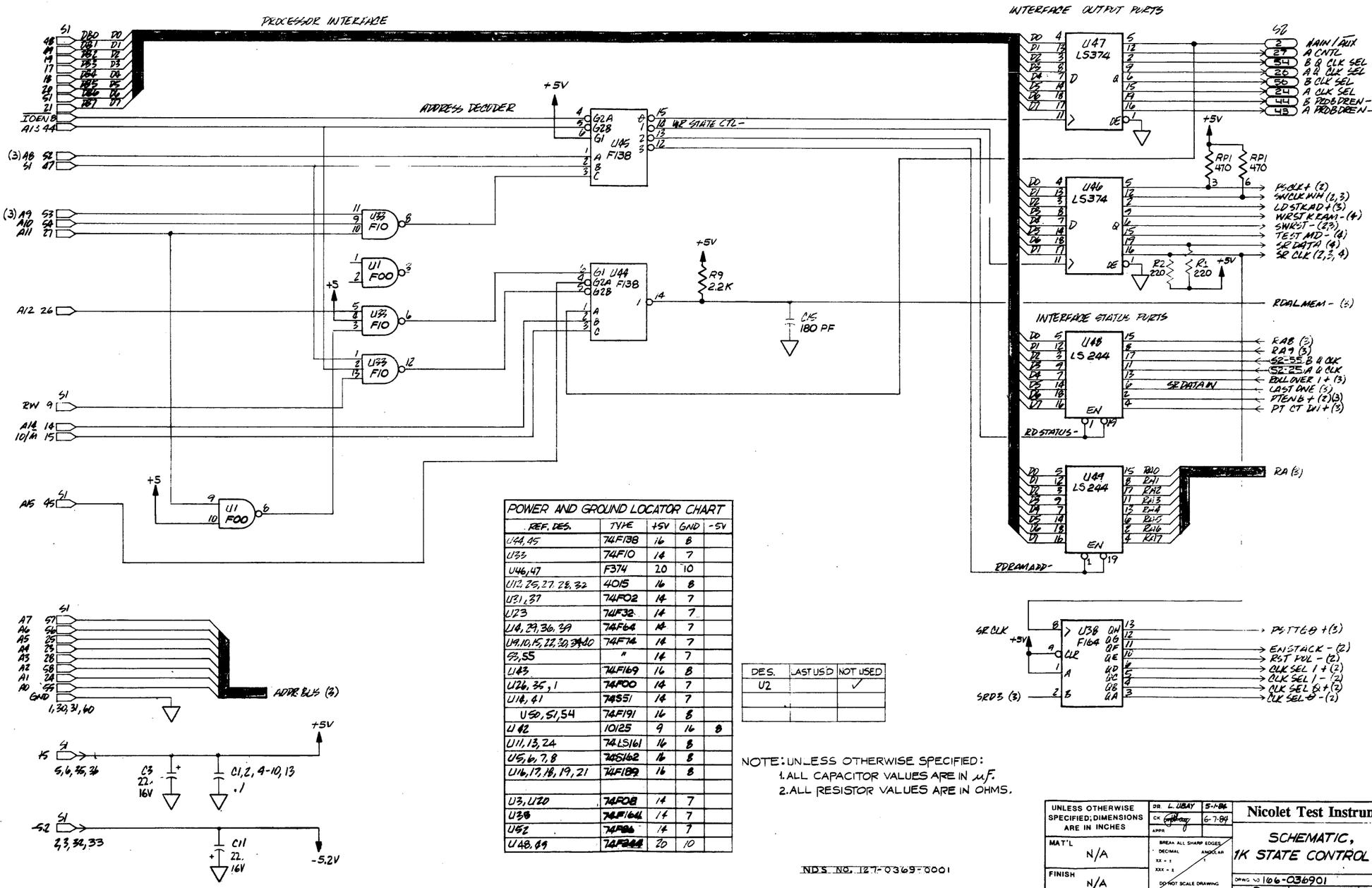
REV.	DESCRIPTION	DATE	APPROVED
-/C	PROTOTYPE		
A/A	RELEASE PER ECO 1260	11-12-84	
A/B	REV. PER ECO 339 MG	2-6-85	
B/A	REL. PER ECO 1346 MG	2-22-85	
B/B	REV. PER ECO 1476 VL	7-10-85	



REF. DES.	TYPE	+5V	GND	-5V
U44, 45	74LF138	16	8	
U33	74LF10	14	7	
U46, 47	F374	20	10	
U12, 26, 27, 28, 32	4015	16	8	
U31, 37	74LF02	14	7	
U23	74LF32	14	7	
U8, 29, 36, 39	74LF64	14	7	
U9, 10, 15, 22, 30, 34, 40	74LF74	14	7	
S3, S5	"	14	7	
U43	74LF169	16	8	
U26, 35, 1	74LF00	14	7	
U18, 41	74S51	14	7	
U50, 51, 54	74LF191	16	8	
U62	10125	9	16	8
U11, 13, 24	74LS161	16	8	
U5, 6, 7, 8	74S162	16	8	
U16, 17, 18, 19, 21	74LF189	16	8	
U3, U20	74F08	14	7	
U36	74LF164	14	7	
U52	74F86	14	7	
U48, 49	74F244	20	10	

DES.	LAST USED	NOT USED
U2		✓

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR. L. UBAY 5-4-84
MAT'L N/A	CK 6-7-84
FINISH N/A	APPR

BREAK ALL SHARP EDGES. DECIMAL XX ± .1 XXX ± .01 ANGULAR ± 1°. DO NOT SCALE DRAWING

Nicolet Test Instruments

SCHEMATIC, 1K STATE CONTROL 20MHZ

DRWG NO 166-036901 REV B/B

D SCALE NONE SHEET 1 OF 1

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CLOCK QUALIFIER GATE

RP4 220/330

(1) ADDR BUS

RAM ADDR TO MEMORY BDS

ROLLOVER + (1)

QC OVERFLOW

ACTION +

PCTCDN + (1)

LAST ONE (1)

(1) RDALMEM -
(2) BWE 2 +

(1) PSTTGØ +
(1) SWRST -
(1) SED3

(1) SROLK

(2) SED2
(2) PTDIØ +
(2) BWE 1 +
(1) SW CLK WH -

SWCLKWH -

(4) DLYCTDN -
(2) TRIG +

(4) MI -
(4) MØ +
(2) RSTL -
(4) DLYCTDN +
(2) RESTART +
(1) LDSTKAD +

RESTART GENERATOR
ON NTH CLOCK
BEFORE NTH CLOCK

RST - (2)

NDS NO. 127-0369-0001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR L. LIBAY 5-2-86	Nicolet Test Instruments	
	CK 6-7-86	SCHEMATIC, 1K STATE CONTROL 20 MHZ	
	APPR		
MAT'L N/A	BREAK ALL SHARP EDGES .DECIMAL ANGULAR XX = ± XXX = ±		
FINISH N/A	DO NOT SCALE DRAWING	DRWG NO 166-036901 REV B/B	
		D SCALE NONE SHT 3 OF 4	

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DELAY MODE CONTROL PART 1

DELAY MODE RAM

INTERFACE SHIFT REGISTAR PART 1 OF 4

(1) TEST MD-
(2) SRDI+
(2) RDPSTK+
(1) SR CLK
(1) SR DATA
NSA3
NSA2
(2) NSA1
NSA0
(1) WRSTKRAM+
(2) TRIG-
(2) POPEN-
(2) DBCLK+

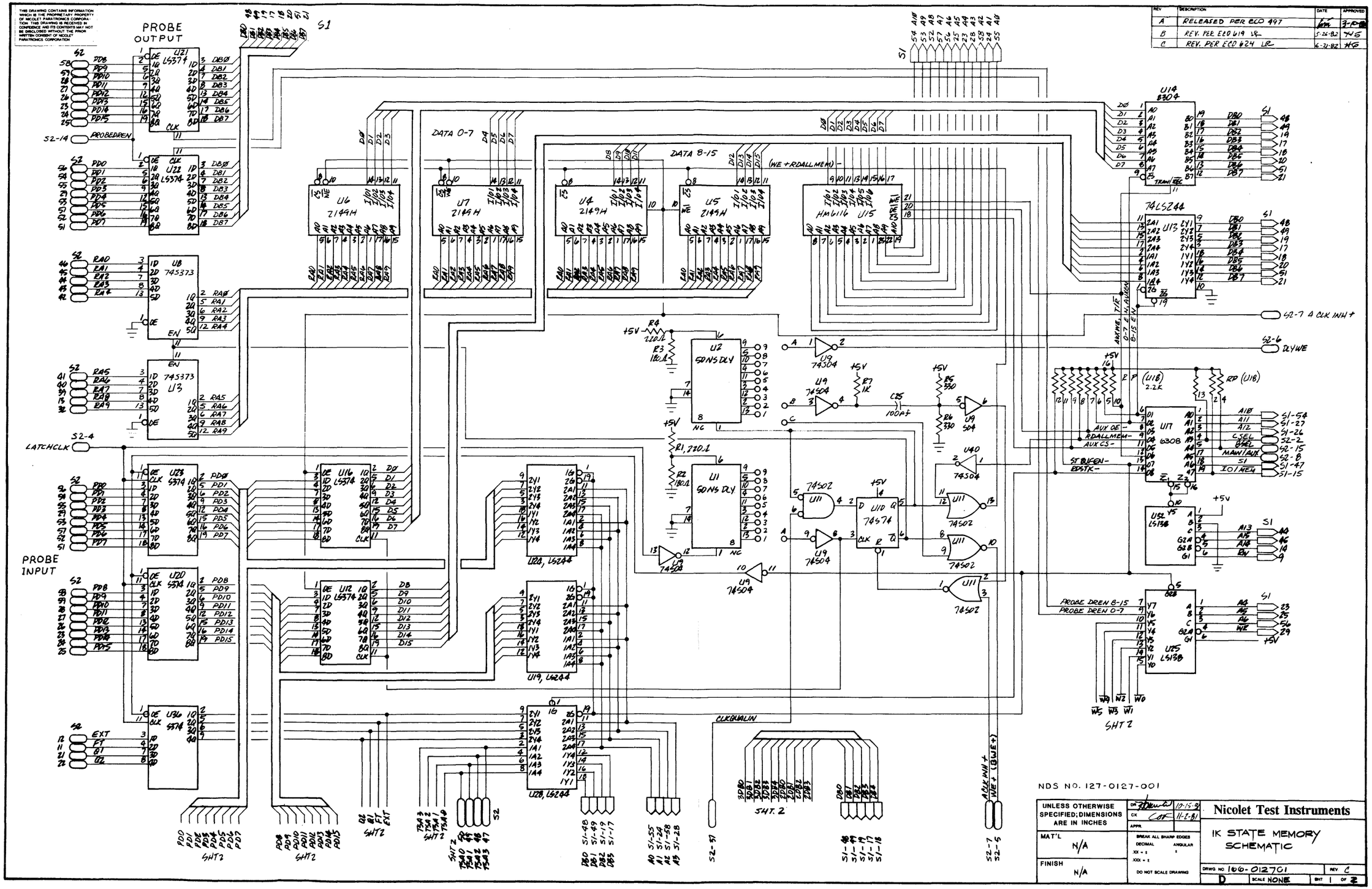
+5V
RP3 470
RP3, 470
R22 220
R23 220
R24 220
R25 220
R26 220
RP2 470

U110 S74
U9 F74
U115 1/2 F74
U4 S64
U14 S51
U8 S162
U7 S162
U6 S162
U5 S162
U32 4015
U28 4015
U27 4015
U21 F189
U19 F189
U18 F189
U17 F189
U16 F189
U20 F08
U26 F00
U3 F08

M1+
M1-
MB+
MB-
SRDH
BEFORE NTH CLOCK NOT ON NTH CLOCK
DLYTC+ (2)
TRIG PDL+ (2)
TRIG PDL- (2)
DLYCTDN- (3)
DLYCTDN+ (3)
M1- (3)
MB+ (3)
SRDI+ (2)
TRIG-
DELAY MODE CONTROL PART 2 OF 2

NDS No. 127-0369-0001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR L. UBAY 5-1-84	Nicolet Test Instruments	
MAT'L N/A	CK [illegible] 6-7-84	SCHEMATIC, 1K STATE CONTROL 20MHZ	
FINISH N/A	APPR	DRWG NO. 166-036901	REV B/B
BREAK ALL SHARP EDGES DECIMAL XX ± .1 XXX ± .1 ANGULAR ± 1° DO NOT SCALE DRAWING	D	SCALE NONE	SHT 4 OF 4



PROBE OUTPUT
PROBE INPUT
DATA 0-7
DATA 8-15
(WE + RDALLMEM)
U6 2149H
U7 2149H
U4 2149H
U5 2149H
HM6116 U15
U14 8304
74LS244 U13
U17 6308
U2 50NS DLY
U1 50NS DLY
U10 74S74
U9 74S04
U40 74S04
U11 74S02
U23 S374
U20 S374
U36 S374
U16 LS374
U12 LS374
U24, LS244
U19, LS244
U28, LS244
U25 LS138
U52 LS138
U21 LS374
U22 LS374
U8 74S373
U3 74S373
LATCHCLK
PROBEDREN
CLKQUALIN
SHT 2
NDS NO. 127-0127-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
Nicolet Test Instruments
IK STATE MEMORY SCHEMATIC
DRWG NO 166-012701
REV C
SCALE NONE
SHT 1 OF 2

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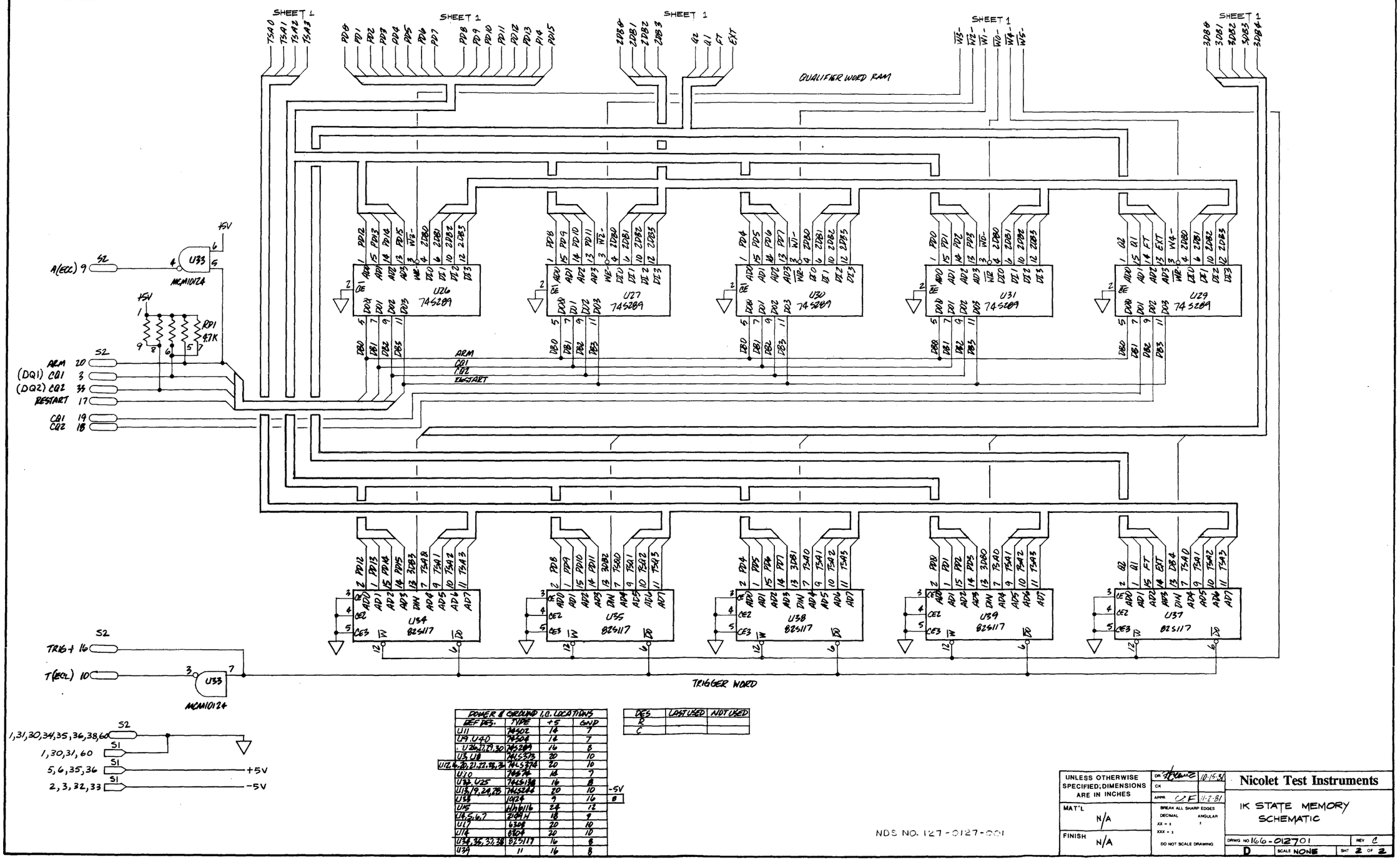


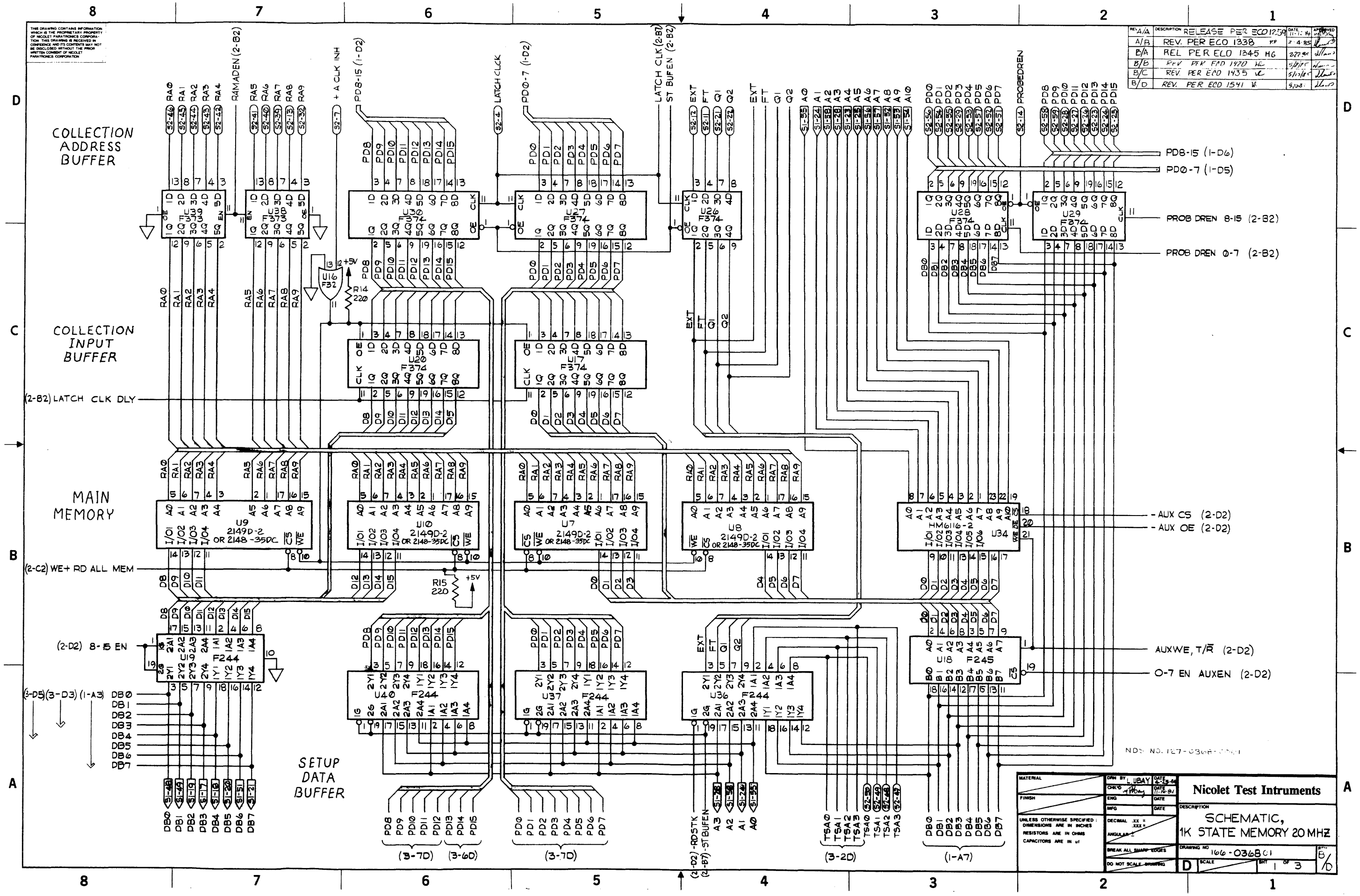
POWER & GROUND I.C. LOCATIONS			
REF DES.	TYPE	+5	GND
U11	74S02	14	7
U9, U40	74S04	14	7
U26,27,29,30	74S289	16	8
U3, U18	74LS273	20	10
U12,16,20,21,22,28,34	74LS374	20	10
U10	74S74	14	7
U32, U25	74LS138	16	8
U13,19,24,28	74LS244	20	10
U33	10124	9	16
U15	WD1016	24	12
U4,5,6,7	2149H	18	9
U17	6309	20	10
U14	6504	20	10
U34,36,37,38	82S117	16	8
U39	11	16	8

-5V
8

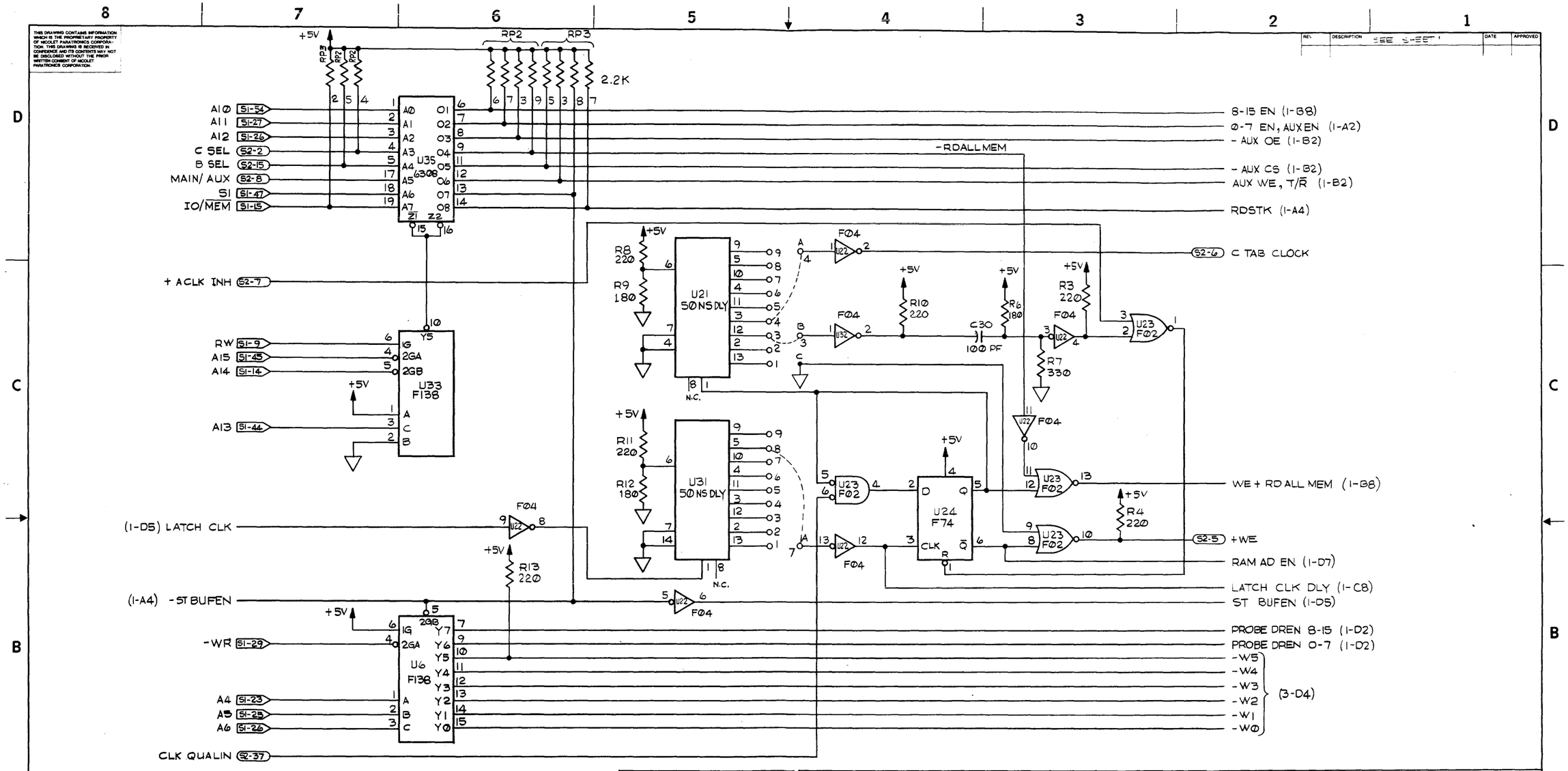
DES	LAST USED	NOT USED
R		
C		

NDS NO. 127-0127-001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR [illegible]	10-16-81	Nicolet Test Instruments
	CK		
	APPR C.F.	11-2-81	
MAT'L N/A	BREAK ALL SHARP EDGES DECIMAL ANGULAR XX = ± XXX = ±		1K STATE MEMORY SCHEMATIC
FINISH N/A	DO NOT SCALE DRAWING		DRWG NO 166-012701 REV C
	D	SCALE NONE	SHT 2 OF 2



COLLECTION ADDRESS BUFFER
COLLECTION INPUT BUFFER
MAIN MEMORY
SETUP DATA BUFFER
(2-B2) LATCH CLK DLY
(2-C2) WE+ RD ALL MEM
(2-D2) 8-15 EN
(3-D5)(3-D3)(1-A3)
PD8-15 (1-D6)
PD0-7 (1-D5)
PROB DREN 8-15 (2-B2)
PROB DREN 0-7 (2-B2)
- AUX CS (2-D2)
- AUX OE (2-D2)
AUXWE, T/R̄ (2-D2)
0-7 EN AUXEN (2-D2)
(3-7D)
(3-6D)
(3-2D)
(1-A7)
Nicolet Test Intruments
SCHEMATIC, 1K STATE MEMORY 20 MHZ
166-0368 01



REF DESIGNATOR	
LAST USED	NOT USED

SPARE GATES		
REF. DES	TYPE	PIN NO.

POWER AND GROUND LOCATOR CHART					
REF DES.	TYPE	GND	+5V	-5V	# PINS
U23	74F02	7	14		14
U22,32	74F04	7	14		14
U16	74F32	7	14		14
U24	74F74	7	14		14
U33	74F138	2,3,8	1,16		16
U6	"	8	6,16		16
U19,36,37,40	74F244	10	20		20
U18	74F245	10	20		20
U1,2,3,5,4	74S189A	2,8	16		16
U38,39	74F373	1,10	20		20
U17,20,26,27,28,29,30	74F374	10	20		20
U25	10124	16	6,9	8	16
U34	HM6116-2	12	24		24
U7,8,9,10	2149D-2	9	18		18
U35	6308	10	20		20
U11,12,13,14,15	82S117	3,4,5,8	16		16

REF. DES.	TYPE	GND	+5V	-5V	# PINS
U21,31	50 NS DLY	7,14			14

NDS NO. 127-0[illegible]8-0001

ITEM / LTR	P/N	DESCRIPTION	QTY

MATERIAL

FINISH

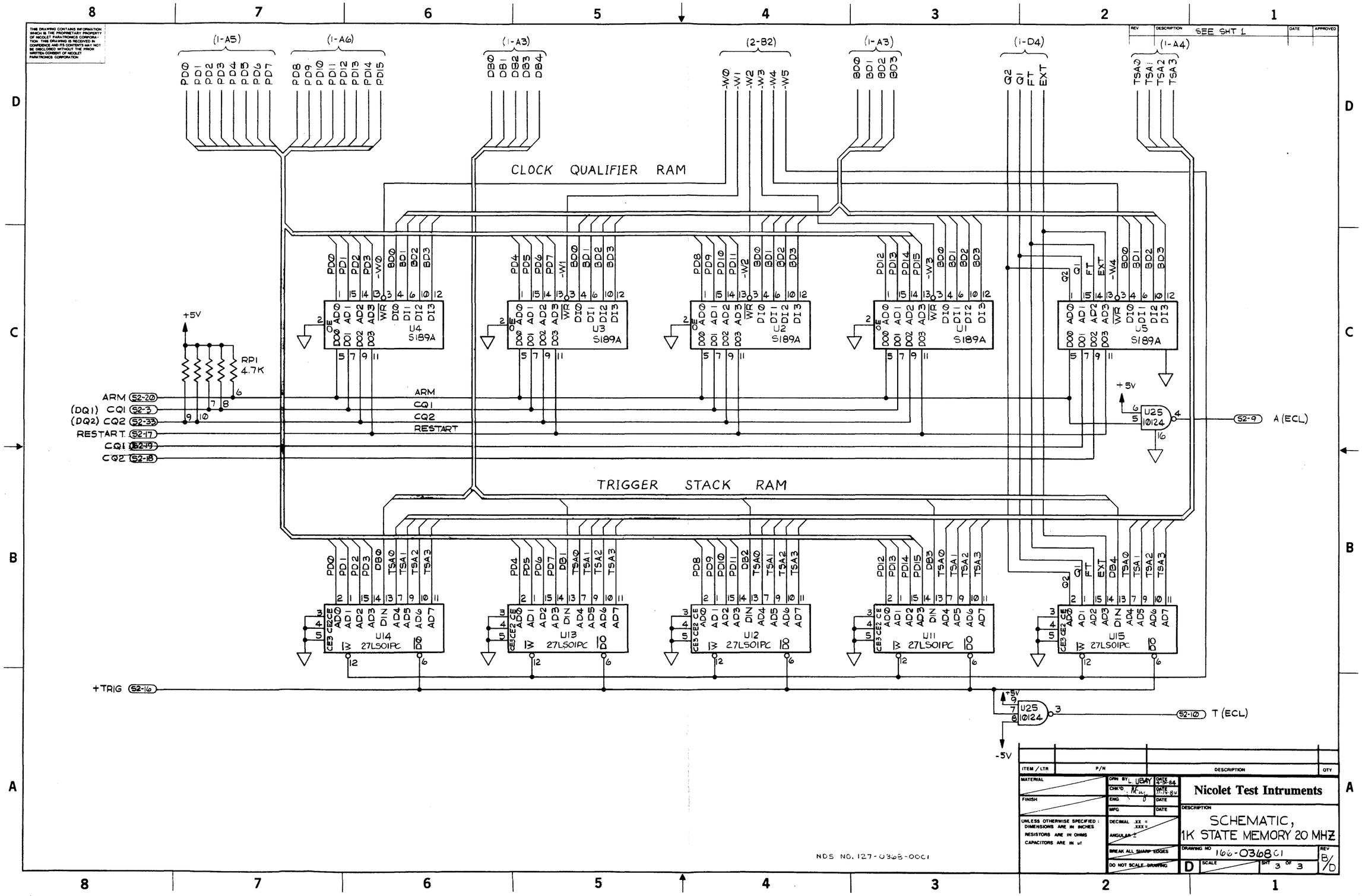
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES RESISTORS ARE IN OHMS CAPACITORS ARE IN uf

DRN BY L. UBAY DATE 5-1-84
CHK'D DATE 11-14-84
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

Nicolet Test Intruments

DESCRIPTION
SCHEMATIC,
1K STATE MEMORY 20 MHZ

DRAWING NO 166-036801
D SCALE SHT 2 OF 3 REV B/D



CLOCK QUALIFIER RAM
TRIGGER STACK RAM
U4 S189A
U3 S189A
U2 S189A
U1 S189A
U5 S189A
U14 27LS01PC
U13 27LS01PC
U12 27LS01PC
U11 27LS01PC
U15 27LS01PC
U25 10124
RP1 4.7K
+5V
-5V
ARM
CQ1
CQ2
RESTART
(DQ1) CQ1
(DQ2) CQ2
RESTART
+TRIG
A (ECL)
T (ECL)
SEE SHT 1
Nicolet Test Intruments
SCHEMATIC,
1K STATE MEMORY 20 MHZ
166-0368C1
NDS NO. 127-0368-00C1

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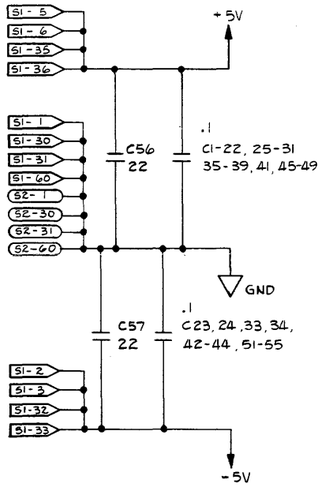
REV	DESCRIPTION	DATE	APPROVED
B/1	PROTOTYPE	8-3-81	
B/A	RELEASE PER ECO 1287	11-13-84	
B/B	REV. PER ECO 1295	11-27-84	
B/C	REV PER ECO 1305 PP	12-3-84	
B/D	REV. PER ECO 1315 PP	12-17-84	
C/A	REV PER ECO 1301 HG	3-7-85	
C/B	REV. PER ECO 1533 LL	8-22-85	

SPARE GATES		
REF DES	TYPE	PIN NO.

REF DESIGNATOR	
LAST USED	NOT USED
U72	U11
R14	
C58	C32,50
RP11	RP26
Q2	
J2	
E24	

POWER AND GROUND LOCATOR CHART							
REF DES.	TYPE	GND	+5V	-5V			# PINS
U8,21	74S10	7	14				14
U10	74S20	7	14				14
U9	74S30	7	14				14
U66	74S08	7	14				14
U22,65	74S74	7	14				14
U18	74S134	8	16				16
U61	74S157	8	16				16
U38	74S244	10	20				20
U19,	74LS00	7	14				14
U36	74LS10	7	14				14
U35, 51	74LS138	8	16				16
U20	74S175	8	16				16
U49,48	74LS244	10	20				20
U52 ,45. 47. 50	74LS374	10	20				20
U37	20NS DLY						14
U12,41,42	4015B	16		8			16
U30,31	2149	9	18				18
U14,15,16.17	AM27S03A	8	16				16
U24,39,40,56,70	10102	1,16		8			16
U69.71	10124	16	9	8			16
U68	10125	16	9	8			16
U55.57	10130	1,16		8			16
U54	10197	1,16		8			16
U1,33,58	74F00	7	14				14
U6	74F10	7	14				14
U2,3,4,5	74F190	8	16				16
U62,63,64	74F191	8	16				16
U46,44	74F374	10	20				20
U23,67	74S00	7	14				14
U13	74LS74	7	14				14
U60	74LS30	7	14				14
U7	74LS08	7	14				14
U25,59,43,26,27,28	SPARE						
U53	10211	1,15,16		8			16
U72	10131	1,16		8			16
U29,32	4015B	8	16				16
U34	74LS32	7	14				14
RP1,2,3.5,7.8,9.10.11	470Ω X 7			1			8
RP4	470Ω X 7		1				8



NOTES : UNLESS OTHERWISE SPECIFIED.

1. SYMBOL = S1 CONNECTOR
   SYMBOL = S2 CONNECTOR

NDS NO. 127-0361-0101

ITEM / LTR	P/N	DESCRIPTION	QTY

MATERIAL

FINISH

UNLESS OTHERWISE SPECIFIED : DIMENSIONS ARE IN INCHES RESISTORS ARE IN OHMS CAPACITORS ARE IN uf

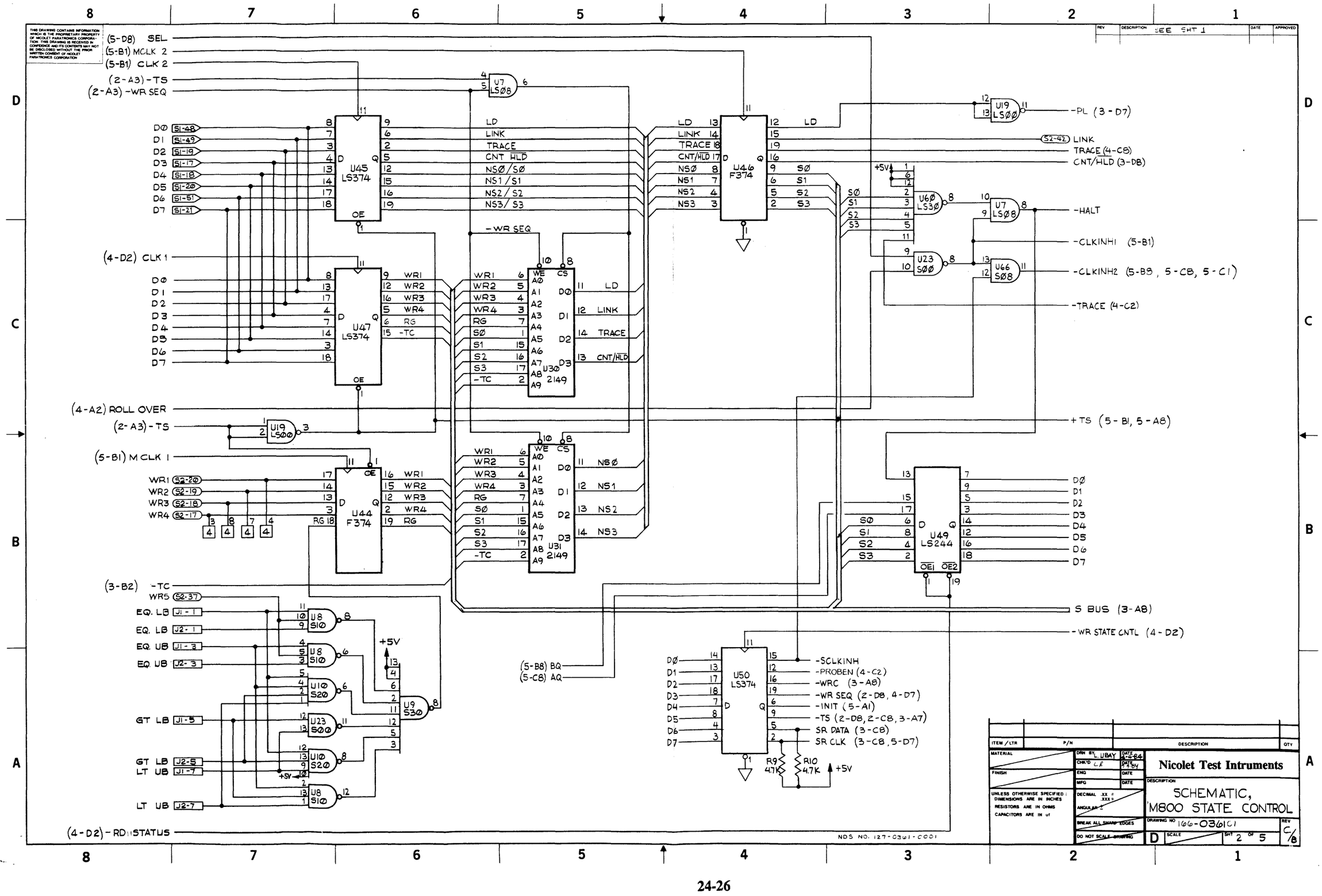
DRN BY L. LEBAY DATE 2-19-81
CHK'D L. Ramos DATE 2-19-81
ENG NS DATE 11-27-84
MFG DATE

DECIMAL XX = XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

Nicolet Test Intruments

DESCRIPTION
SCHEMATIC,
M800 STATE CONTROL

DRAWING NO 166-036101 REV C/B
D SCALE SHT 1 OF 5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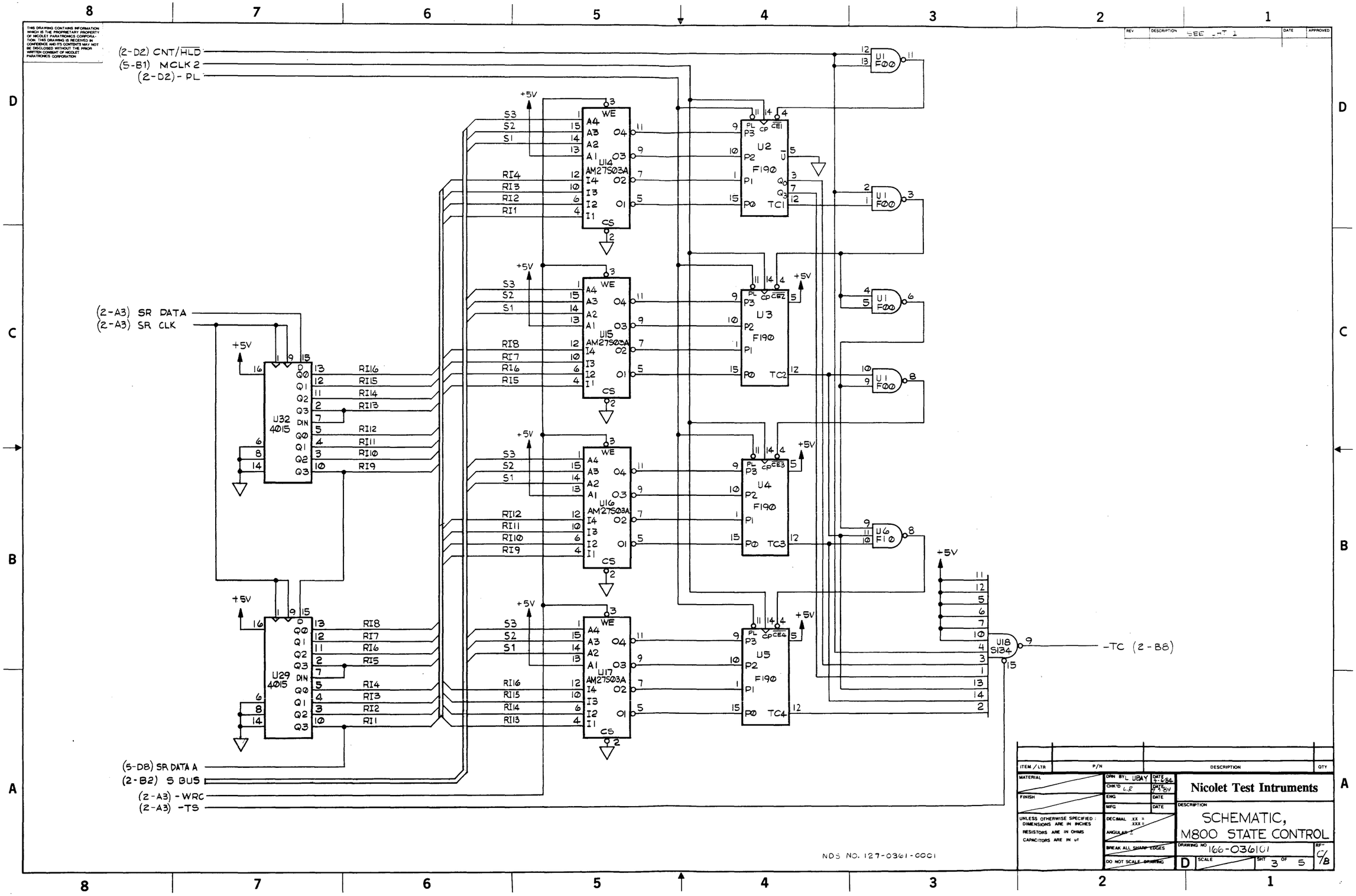
REV DESCRIPTION SEE SHT 1 DATE APPROVED
(5-D8) SEL
(5-B1) MCLK 2
(5-B1) CLK 2
(2-A3) -TS
(2-A3) -WR SEQ
U7 LSØ8
U45 LS374
U46 F374
U19 LSØØ
U6Ø LS3Ø
U23 SØØ
U66 SØ8
U47 LS374
U3Ø 2149
U44 F374
U31 2149
U8 S1Ø
U1Ø S2Ø
U9 S3Ø
U49 LS244
U50 LS374
D0 D1 D2 D3 D4 D5 D6 D7
LD LINK TRACE CNT HLD NSØ/SØ NS1/S1 NS2/S2 NS3/S3
-WR SEQ
(4-D2) CLK 1
WR1 WR2 WR3 WR4 RG -TC
(4-A2) ROLL OVER
(2-A3) -TS
(5-B1) M CLK 1
WR1 (S2-2Ø) WR2 (S2-19) WR3 (S2-18) WR4 (S2-17)
(3-B2) -TC
WR5 (S2-37)
EQ. LB J1-1
EQ. LB J2-1
EQ. UB J1-3
EQ. UB J2-3
GT LB J1-5
GT LB J2-5
LT UB J1-7
LT UB J2-7
(4-D2) -RD STATUS
(5-B8) BQ
(5-C8) AQ
+5V
R9 4.7K
R10 4.7K
-PL (3-D7)
(S2-42) LINK
TRACE (4-C8)
CNT/HLD (3-D8)
-HALT
-CLKINH1 (5-B1)
-CLKINH2 (5-B8, 5-C8, 5-C1)
-TRACE (4-C2)
+TS (5-B1, 5-A8)
S BUS (3-A8)
-WR STATE CNTL (4-D2)
-SCLKINH
-PROBEN (4-C2)
-WRC (3-A8)
-WR SEQ (2-D8, 4-D7)
-INIT (5-A1)
-TS (2-D8, 2-C8, 3-A7)
SR DATA (3-C8)
SR CLK (3-C8, 5-D7)
NDS NO. 127-0361-C001
ITEM / LTR P/N DESCRIPTION QTY
MATERIAL FINISH
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES RESISTORS ARE IN OHMS CAPACITORS ARE IN uf
DRN BY L. UBAY DATE 4-4-84
CHK'D L.B DATE 4-4-84
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING
Nicolet Test Intruments
DESCRIPTION
SCHEMATIC, M800 STATE CONTROL
DRAWING NO 166-0361C1
REV C/8
D SCALE SHT 2 OF 5



(2-D2) CNT/HLD
(5-B1) MCLK 2
(2-D2) - PL
(2-A3) SR DATA
(2-A3) SR CLK
(5-D8) SR DATA A
(2-B2) S BUS
(2-A3) - WRC
(2-A3) -TS
U14 AM27S03A
U15 AM27S03A
U16 AM27S03A
U17 AM27S03A
U2 F190
U3 F190
U4 F190
U5 F190
U32 4015
U29 4015
U1 F00
U6 F10
U18 S134
-TC (2-B8)
NDS NO. 127-0361-0001
Nicolet Test Intruments
SCHEMATIC, M800 STATE CONTROL
DRAWING NO 166-036101
SHT 3 OF 5

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REV	DESCRIPTION	DATE	APPROVED
	SEE SHT. 1		

(2-A3) -WR SEQ
(2-A3) -PROBEN

-IOEN S1-8
- A13 S1-44
A8 S1-52
S1 S1-47
A9 S1-53
A10 S1-54
A11 S1-27
- A12 S1-26
RW S1-9
- A15 S1-45
- A14 S1-14
IO/ M S1-15

U35 LS138 (G1, G2A, G2B, A, B, C)
U36 LS10
U34 LS32
U19 LS00
U51 LS138 (G1, G2B, G2A)
+5V
R13 4.7K
C40 330 PF
U65 S74 (S, Q, D, C)
U34 LS32

-WR STATE CNTL (2-A2)
-RD STATUS (2-A8)
-RDRAM ADD (4-B2)
CLK 2 (2-D8)
CLK 1 (2-C8)
-LDA (4-A7)

U52 LS374
D0 D1 D2 D3 D4 D5 D6 D7
S2-2 MAIN/ $\overline{\text{AUX}}$
S2-27 A CNTL
S2-54 BQ CLK SEL
S2-26 AQ CLK SEL
S2-56 B CLK SEL
S2-24 A CLK SEL
S2-44 - B PROB DREN
S2-43 - A PROBE DREN

(2-D2) TRACE
U33 F00
-TRACE (2-C2)

A0 S1-55
A1 S1-24
A2 S1-58
A3 S1-28
U64 F191 (P0 P1 P2 P3, Q0 Q1 Q2 Q3, LD, CLK, TC)
RA0 RA1 RA2 RA3
U58 F00

A4 S1-23
A5 S1-25
A6 S1-56
A7 S1-57
U63 F191
RA4 RA5 RA6 RA7
U58 F00

A8 S1-52
A9 S1-53
U62 F191
RA8 RA9 QC N.C.
U58 F00

(4-D2) - LDA
(5-B1) M CLK1

U61 LS157 (Ioa Iob Ioc Iod, I1a I1b I1c I1d, S, Za Zb Zc Zd)
RA0 RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8 RA9

U48 LS244
D0 (2-C2)
D1 (2-C2)
D2 (2-C2)
D3 (2-C2)
D4 (2-C2)
D5 (2-C2)
D6 (2-C2)
D7 (2-C2)

-RD RAM ADD (4-D2)
S2-16 RA0
S2-15 RA1
S2-14 RA2
S2-13 RA3
S2-12 RA4
S2-11 RA5
S2-10 RA6
S2-9 RA7
S2-28 RA8
S2-29 RA9

U13 LS74 (S, Q, D, C)
+5V
U65 S74 (PR, Q, D, CK, CLR)
ROLLOVER (2-C8)

NDS NO. 127-0361-0001

ITEM / LTR	P/N	DESCRIPTION	QTY

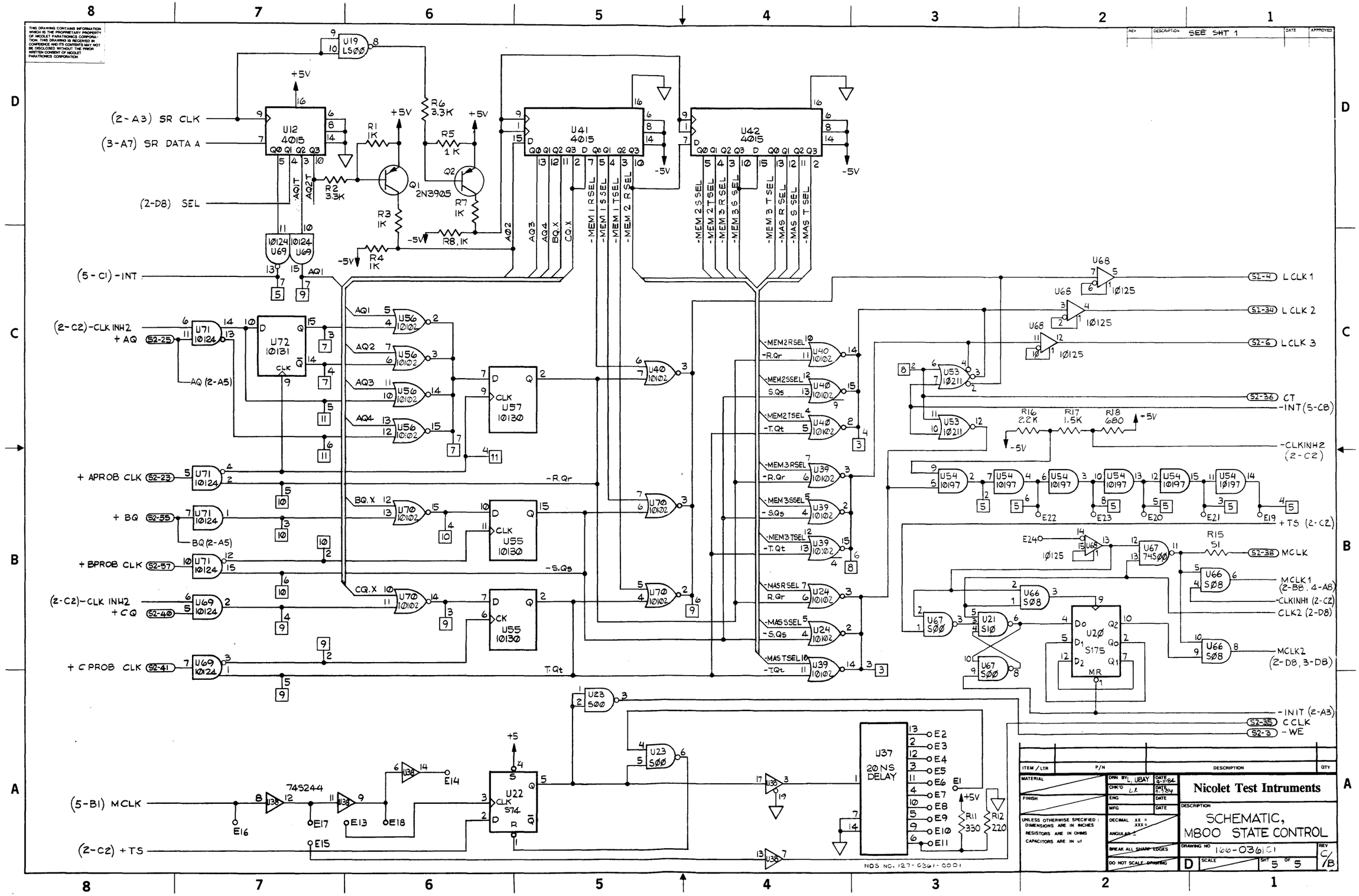
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, RESISTORS ARE IN OHMS, CAPACITORS ARE IN uf
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

DRN BY L. UBAY DATE 2-8-84
CHK'D L.R. DATE 2-8-84
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±

Nicolet Test Intruments

DESCRIPTION: SCHEMATIC, M800 STATE CONTROL

DRAWING NO 166-036101 REV C/8
SCALE D SHT 4 OF 5



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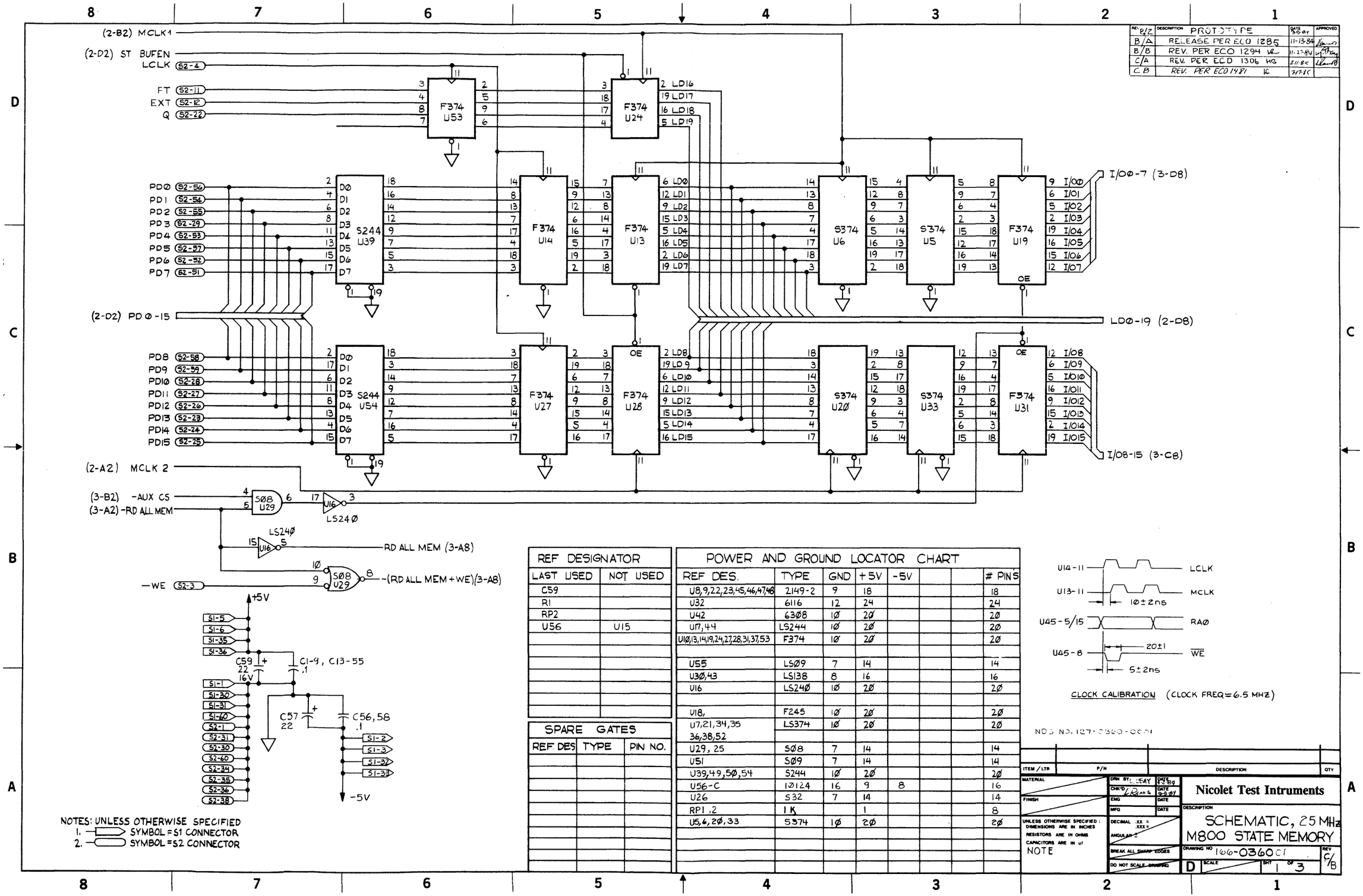
SEE SHT 1
(2-A3) SR CLK
(3-A7) SR DATA A
(2-D8) SEL
(5-C1) -INT
(2-C2)-CLK INH2 + AQ
+ APROB CLK
+ BQ
+ BPROB CLK
(2-C2)-CLK INH2 + CQ
+ C PROB CLK
(5-B1) MCLK
(2-C2) +TS
U12 4015
U41 4015
U42 4015
U19 LS00
U72 10131
U57 10130
U55 10130
U20 S175
U37 20NS DELAY
U22 S74
74S244
L CLK 1
L CLK 2
L CLK 3
CT
-INT (5-C8)
-CLKINH2 (2-C2)
+TS (2-C2)
MCLK
MCLK1 (2-B8, 4-A8)
-CLKINH1 (2-C2)
CLK2 (2-D8)
MCLK2 (2-D8, 3-D8)
-INIT (2-A3)
C CLK
-WE
NDS NO. 127-0361-0001
Nicolet Test Intruments
SCHEMATIC, M800 STATE CONTROL
DRAWING NO 166-0361C1
SHT 5 OF 5



REV	DESCRIPTION	DATE	APPROVED
B/2	PROTOTYPE	3-9-84	
B/A	RELEASE PER ECO 1285	11-13-84	
B/B	REV. PER ECO 1294	11-27-84	
C/A	REV. PER ECO 1306	2-11-85	
C/B	REV. PER ECO 1481	7-17-85	

REF DESIGNATOR	
LAST USED	NOT USED
C59	
R1	
RP2	
U56	U15

SPARE GATES		
REF DES	TYPE	PIN NO.

POWER AND GROUND LOCATOR CHART							
REF DES.	TYPE	GND	+5V	-5V			# PINS
U8,9,22,23,45,46,47,48	2149-2	9	18				18
U32	6116	12	24				24
U42	6308	10	20				20
U17,44	LS244	10	20				20
U10,13,14,19,24,27,28,31,37,53	F374	10	20				20
U55	LS09	7	14				14
U30,43	LS138	8	16				16
U16	LS240	10	20				20
U18,	F245	10	20				20
U7,21,34,35 36,38,52	LS374	10	20				20
U29, 25	S08	7	14				14
U51	S09	7	14				14
U39,49,50,54	S244	10	20				20
U56-C	10124	16	9	8			16
U26	S32	7	14				14
RP1,2	1K		1				8
U5,6,20,33	S374	10	20				20

ITEM / LTR	P/N	DESCRIPTION	QTY

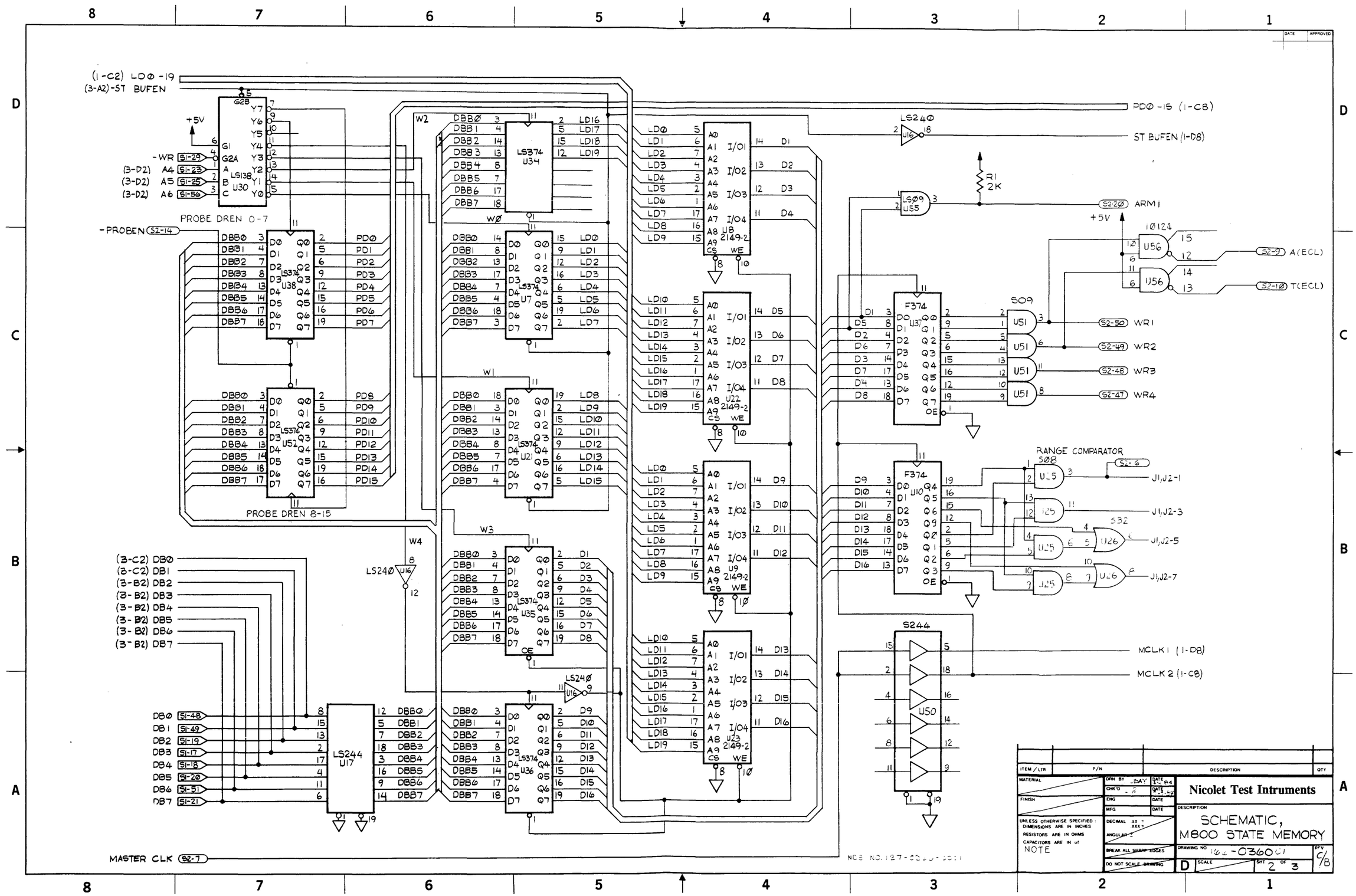
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES RESISTORS ARE IN OHMS CAPACITORS ARE IN uf
NOTE

DRN BY: L. LEAY DATE 4-2-84
CHK'D: L. Ramos DATE 9-5-84
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

Nicolet Test Intruments

DESCRIPTION
SCHEMATIC, 25 MHz
M800 STATE MEMORY

DRAWING NO 166-0360C1 REV C/B
D SCALE SHT 1 OF 3


(1-C2) LD0-19
(3-A2)-ST BUFEN
+5V
-WR S1-29
(3-D2) A4 S1-23
(3-D2) A5 S1-25
(3-D2) A6 S1-56
LS138 U30
PROBE DREN 0-7
-PROBEN S2-14
LS374 U38
LS374 U52
PROBE DREN 8-15
W2
W0
W1
W3
W4
LS374 U34
LS374 U7
LS374 U21
LS374 U35
LS374 U36
LS240 U16
(3-C2) DB0
(3-C2) DB1
(3-B2) DB2
(3-B2) DB3
(3-B2) DB4
(3-B2) DB5
(3-B2) DB6
(3-B2) DB7
DB0 S1-48
DB1 S1-49
DB2 S1-19
DB3 S1-17
DB4 S1-18
DB5 S1-20
DB6 S1-51
DB7 S1-21
LS244 U17
MASTER CLK S2-7
U8 2149-2
U22 2149-2
U9 2149-2
U23 2149-2
PD0-15 (1-C8)
ST BUFEN (1-D8)
LS240 U16
R1 2K
LS09 U55
S2-20 ARM1
+5V
10124 U56
S2-9 A(ECL)
S2-10 T(ECL)
S09 U51
F374 U37
S2-50 WR1
S2-49 WR2
S2-48 WR3
S2-47 WR4
RANGE COMPARATOR
S08 U25
S32 U26
S2-6
J1,J2-1
J1,J2-3
J1,J2-5
J1,J2-7
F374 U10
S244 U50
MCLK1 (1-D8)
MCLK2 (1-C8)
NOTE
Nicolet Test Intruments
SCHEMATIC, M800 STATE MEMORY
162-0360C1
SHT 2 OF 3
REV C/B

REV	DESCRIPTION	DATE	APPROVED
	SEE SHT. 1		

(1-D2) I/Ø-7

(1-C2) I/Ø8-15

RAØ (52-46)
RA1 (52-45)
RA2 (52-44)
RA3 (52-43)
RA4 (52-42)
RA5 (52-41)
RA6 (52-40)
RA7 (52-39)

U49 74S244

RA8 (52-13)
RA9 (52-32)

U5Ø 74S244

U47 2149-2
U48 2149-2
U45 2149-2
U46 2149-2

I/ØØ I/01 I/02 I/03 I/04 I/05 I/06 I/07
I/Ø8 I/09 I/Ø1Ø I/Ø11 I/Ø12 I/Ø13 I/Ø14 I/Ø15

U32 HM6116

I/ØØ I/01 I/02 I/03 I/04 I/05 I/06 I/07
CS OE WE
- AUX WE, T/R
- AUX OE
- AUX CS

A1-56 AØ
A1-24 A1
A1-58 A2
A1-28 A3
A1-23 A4 (3-D8)
A1-25 A5 (3-D8)
A1-26 A6 (3-D8)
A1-57 A7
A1-52 A8
A1-53 A9
A1-54 A1Ø

U18 F245

I/ØØ I/01 I/02 I/03 I/04 I/05 I/06 I/07
OE DR
Ø-7 EN

DBØ DB1 DB2 DB3 DB4 DB5 DB6 DB7

U44 LS244

I/Ø8 I/09 I/Ø1Ø I/Ø11 I/Ø12 I/Ø13 I/Ø14 I/Ø15
8-15 EN

DBØ (2-B8)
DB1 (2-B8)
DB2 (2-B8)
DB3 (2-B8)
DB4 (2-B8)
DB5 (2-B8)
DB6 (2-B8)
DB7 (2-B8)

- AUX CS (1-B8)
Ø-7 EN,
- RD A11 MEM (1-B8)
- ST BUFEN (2-D8)

+5V

U43 LS138
A B C G2A G2B G1
Y5

AI3 (51-44)
AI5 (51-45)
AI4 (51-14)
RW (51-9)

RP1 1K
RP2 1K
RP2 1K

U42 6308
AØ A1 A2 A3 A4 A5 A6 A7

AIØ (51-54)
AI1 (51-27)
AI2 (51-26)
C SEL (52-2)
B SEL (52-15)
MAIN/AUX (52-8)
SI (51-47)
IO/MEM (51-15)

8-15 EN
Ø-7 EN, -AUX EN
- AUX OE
- RD A11 MEM
- AUX CS
- AUX WE, T/R
- ST BUFEN

(1-B6) RD A11 MEM
(1-B6) -(RD A11 MEM+WE)

NDS NO. 127-0360-CCØ1

ITEM / LTR	P/N	DESCRIPTION	QTY

MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, RESISTORS ARE IN OHMS, CAPACITORS ARE IN uf
NOTE

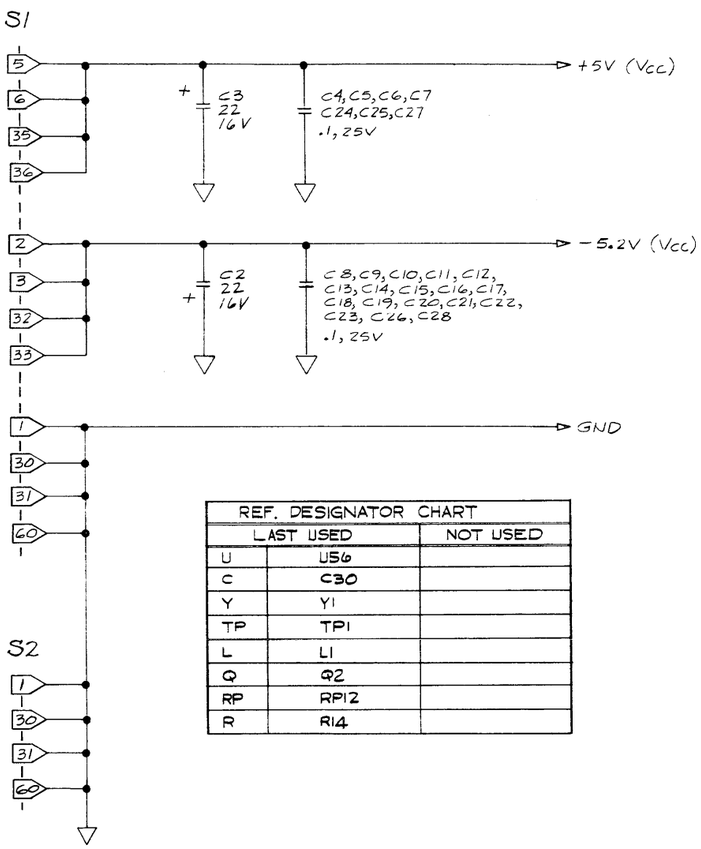
DRN BY LARRY U DATE 82-84
CHK'D C. R. DATE 8-84
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

Nicolet Test Intruments

DESCRIPTION
SCHEMATIC,
M800 STATE MEMORY

DRAWING NO 166-036001 REV C/B
D SCALE SHT 3 OF 3

REV	DESCRIPTION	DATE	APPROVED
C	[illegible]	3-[illegible]	WOS
D	REV PER ECO [illegible] 153A	[illegible]	[illegible]
E	REV PER ECO 185	[illegible]	[illegible]
F	REV PER ECO 227 [illegible]	11/6/80	KBP
G	REV PER ECO 420	10-26-81	[illegible]
H	REV PER ECO 558	[illegible]	[illegible]
J	REV. PER ECO [illegible]	[illegible]	[illegible]
K	REV. PER ECO 811 [illegible]	5-7-83	[illegible]
L	REV. PER ECO 830 [illegible]	4-14-83	[illegible]
M	REV. PER ECO 906 [illegible]	9-12-[illegible]	[illegible]



REF. DESIGNATOR CHART		
LAST USED		NOT USED
U	U56	
C	C30	
Y	Y1	
TP	TP1	
L	L1	
Q	Q2	
RP	RP12	
R	R14	

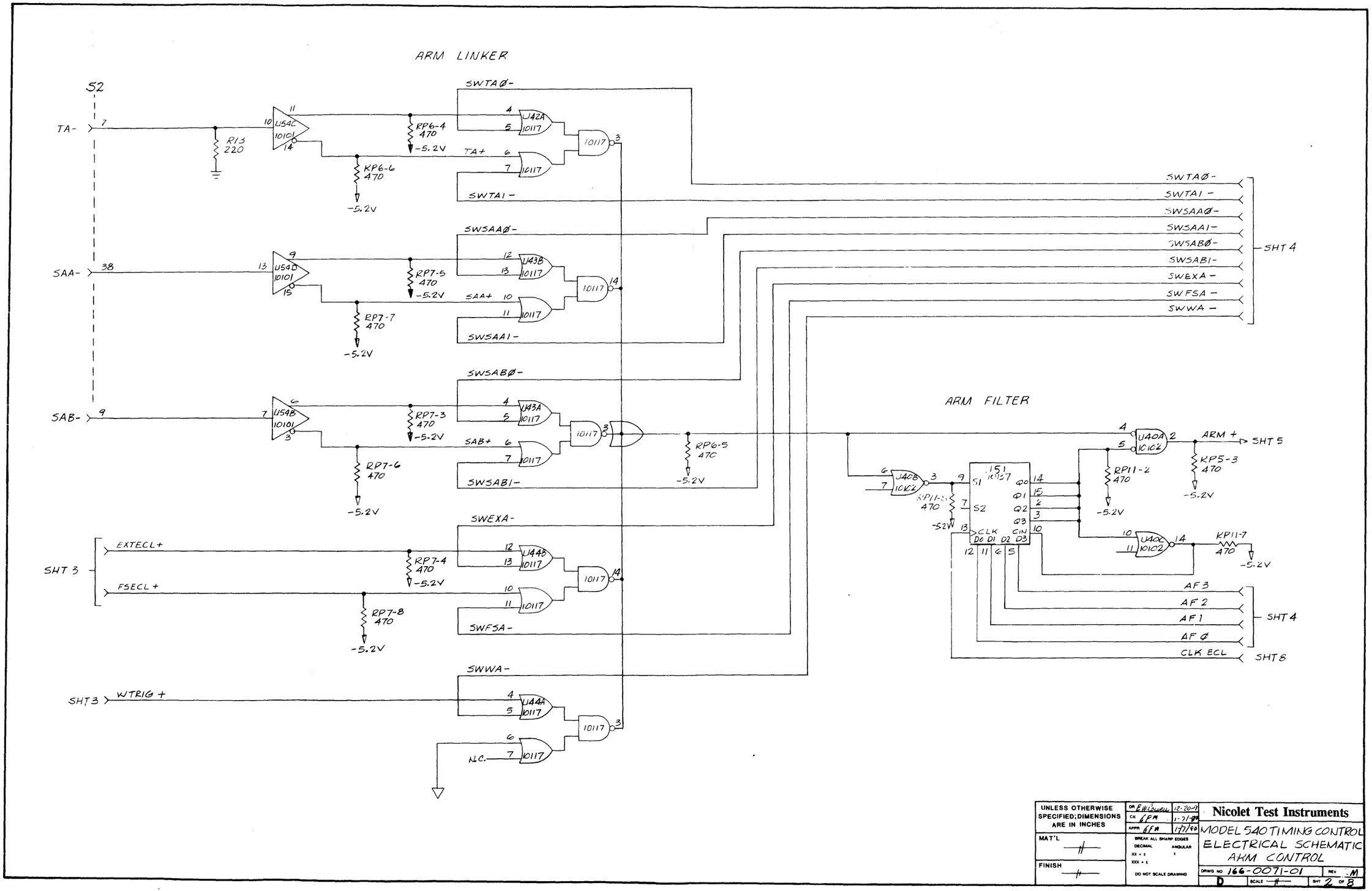
POWER DISTRIBUTION

"U" NUMBER'S	DEVICE	+5V (VCC)	-5.2V (VCC)	GND	PACKAGE
54,56,	10101	—	8	1,16	16 DIP
42,43,44,45,46	10117	—	8	1,16	↑
40,41,10	10102	—	8	1,16	
51,52,16,15,14,21,19,18,17	10137	—	8	1,16	
55,39	10124	9	8	16	↓
50	74LS138	16	—	8	16 DIP
49	74LS374	20	—	10	20 DIP
53,36	10125	9	8	16	16 DIP
48	74LS373	20	—	10	20 DIP
26,27,28,30,31,32,33,29	CD4015	—	8	16	16 DIP
20,38	10104	—	8	1,16	↑
12	10186		8	16	
37,25,13	10148		8	1,16	
24	10162		8	1,16	↓
2,3	74LS151	16	—	8	16 DIP
4,5,6,7,8	74LS90	5	—	10	14 DIP
1	74LS74	14	—	7	14 DIP
9	10138	—	8	1,16	16 DIP
22	10103	—	8	1,16	↑
11,35,34	10211	—	8	1,15,16	↓
47	10130	—	8	1,16	16 DIP

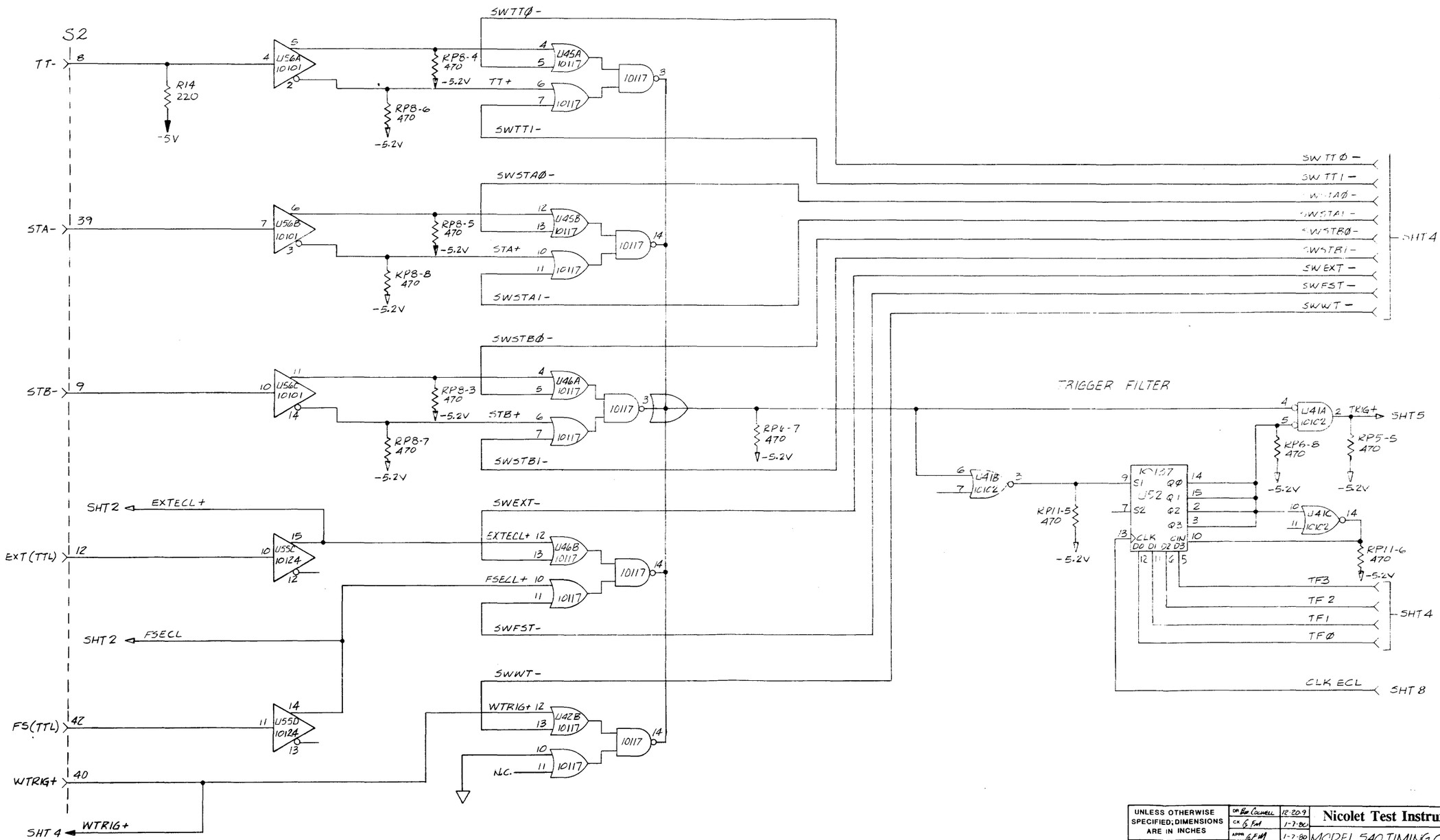
3. THIS SCHEMATIC TO BE USED WITH REV. "J&K" P.C.B. FABRICATION
2. ALL CAPACITORS ARE IN MICROFARADS, DISC CERAMIC
1. ALL DISCRETE RESISTORS ARE 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED:

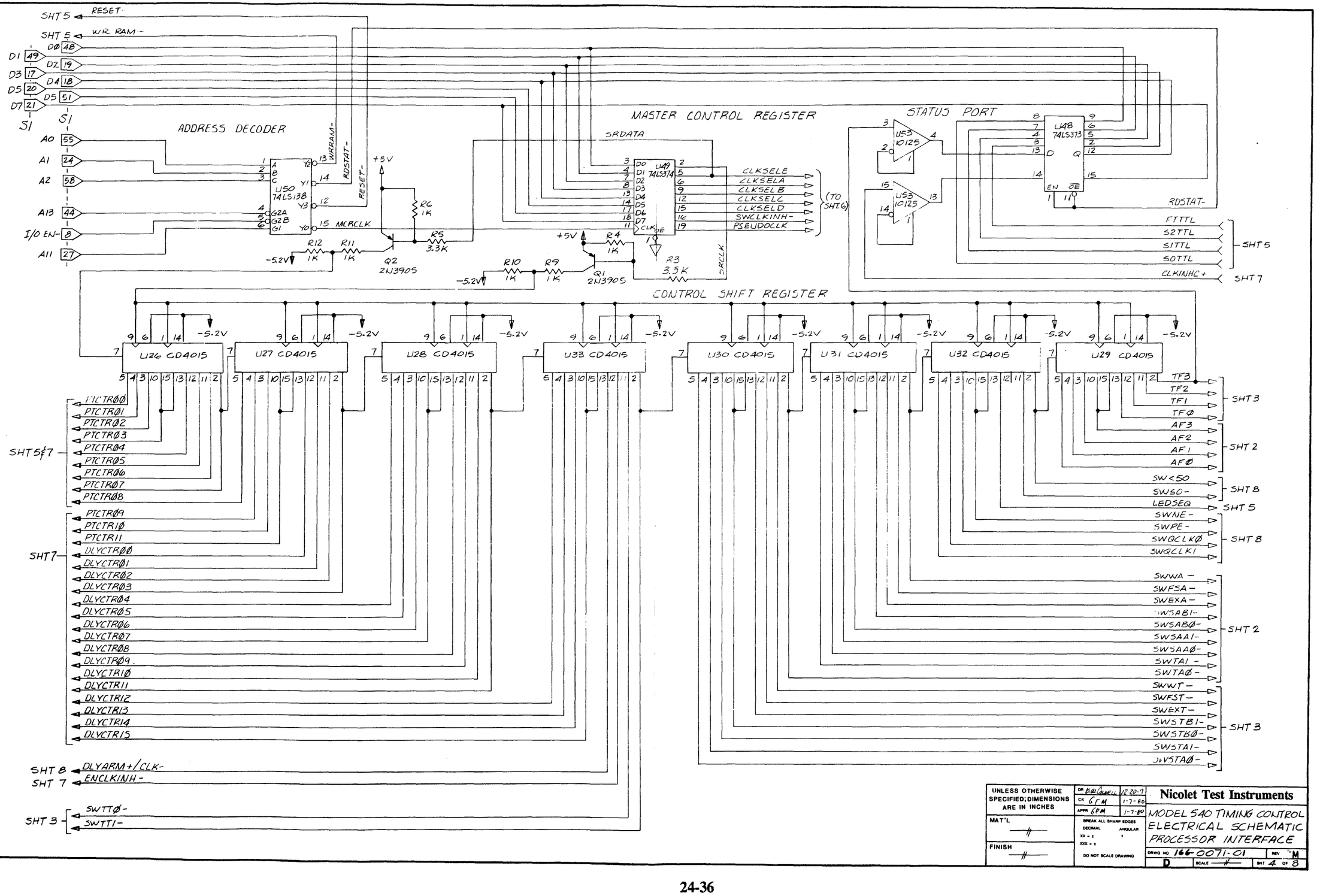
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR [illegible]	1-3-80	Nicolet Test Instruments
	CK [illegible]	[illegible]	MODEL 540 TIMING CONTROL ELECTRICAL SCHEMATIC PWR & GND DISTRIBUTION
MAT'L —	APPR [illegible]	1-7-80	
FINISH —	BREAK ALL SHARP EDGES DECIMAL XX = ± XXX = ± ANGULAR ± DO NOT SCALE DRAWING		DRWG NO 166-0071-01 REV M
			D SCALE SHT 1 OF 8


ARM LINKER
S2
TA-
SAA-
SAB-
SHT 3
EXTECL+
FSECL+
SHT3
WTRIG+
SWTAØ-
SWTA1-
SWSAAØ-
SWSAA1-
SWSABØ-
SWSAB1-
SWEXA-
SWFSA-
SWWA-
SHT 4
ARM FILTER
ARM +
SHT 5
AF 3
AF 2
AF 1
AF Ø
CLK ECL
SHT 8
N.C.
-5.2V
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
Nicolet Test Instruments
MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
ARM CONTROL
DRWG NO 166-0071-01
REV M
SHT 2 OF 8

TRIGGER LINKER



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR Ron Colwell 12-20-9	Nicolet Test Instruments	
	CK G. Fort 1-7-80		
	APPR G.F.M. 1-7-80	MODEL 540 TIMING CONTROL	
MAT'L —	BREAK ALL SHARP EDGES	ELECTRICAL SCHEMATIC	
	DECIMAL ANGULAR	TRIGGER CONTROL	
FINISH —	XX ± .1 ±	DRWG NO 166-0071-01	REV M
	XXX ± .1	D SCALE —	SHT 3 OF 8
	DO NOT SCALE DRAWING		


SHT 5 RESET
SHT 5 WR RAM -
D0 48
D1 49
D2 19
D3 17
D4 18
D5 20
D5 51
D7 21
S1
S1
ADDRESS DECODER
A0 55
A1 24
A2 58
A13 44
I/O EN- 8
A11 27
U50 74LS138
WRRAM-
RDSTAT-
RESET-
15 MCRCLK
+5V
R6 1K
R5 3.3K
R12 1K
R11 1K
-5.2V
Q2 2N3905
MASTER CONTROL REGISTER
SRDATA
U49 74LS374
CLKSELE
CLKSELA
CLKSELB
CLKSELC
CLKSELD
SWCLKINH-
PSEUDOCLK
(TO SHT 6)
SRCLK
R4 1K
R3 3.3K
R10 1K
R9 1K
Q1 2N3905
STATUS PORT
U53 10125
U48 74LS373
RDSTAT-
FTTTL
S2TTL
S1TTL
SOTTL
SHT 5
CLKINHC+
SHT 7
CONTROL SHIFT REGISTER
U26 CD4015
U27 CD4015
U28 CD4015
U33 CD4015
U30 CD4015
U31 CD4015
U32 CD4015
U29 CD4015
TF3
TF2
TF1
TF0
SHT 3
AF3
AF2
AF1
AF0
SHT 2
SW<50
SWSO-
SHT 8
LEDSEQ
SHT 5
SWNE-
SWPE-
SWQCLK0
SWQCLK1
SHT 8
SHT 5&7
PTCTR00
PTCTR01
PTCTR02
PTCTR03
PTCTR04
PTCTR05
PTCTR06
PTCTR07
PTCTR08
SHT 7
PTCTR09
PTCTR10
PTCTR11
DLYCTR00
DLYCTR01
DLYCTR02
DLYCTR03
DLYCTR04
DLYCTR05
DLYCTR06
DLYCTR07
DLYCTR08
DLYCTR09
DLYCTR10
DLYCTR11
DLYCTR12
DLYCTR13
DLYCTR14
DLYCTR15
SWWA-
SWFSA-
SWEXA-
SWSAB1-
SWSAB0-
SWSAA1-
SWSAA0-
SWTA1-
SWTA0-
SHT 2
SWWT-
SWFST-
SWEXT-
SWSTB1-
SWSTB0-
SWSTA1-
SWSTA0-
SHT 3
SHT 8 DLYARM+/CLK-
SHT 7 ENCLKINH-
SHT 3 SWTT0-
SWTT1-
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
XX = ±
XXX = ±
DO NOT SCALE DRAWING
DR 12-20-79
CK 1-7-80
APPR 1-7-80
Nicolet Test Instruments
MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
PROCESSOR INTERFACE
DRWG NO 166-0071-01
REV M
D
SCALE
SHT 4 OF 8

SHT 4 — PTCTRØØ, PTCTRØ1, PTCTRØ2
SHT 2 — ARM+
SHT 3 — TRIG+
SHT 7 — DLYTC−
SHT 8 — CLKECL

SEQUENCER LATCH

U12 10184

ARML+ → SHT 7

SØ
S1
S2

SEQUENCER OUTPUT

U24 10162

DLYCNT+/LD− → SHT 7
PTCNT+/LD− → SHT 7

RP4-8 470 −5.2V
RP6-2 470 −5.2V

LOAD CONTROL

+5V

RESET− — U39B 10124 — KP5-4 470 −5.2V

WRRAM− — U39A 10124 — RP3-5 470 −5.2V

PTCTRØ3 — U20C 10104 — RP3-2 470 −5.2V

PTCTRØ4 — U20D 10104 — RP3-3 470 −5.2V

PTCTRØ5 — U38C 10104 — RP3-4 470 −5.2V

PTCTRØ6 — U38B 10104 — RP5-2 470 −5.2V

PTCTRØ7 — U38D 10104 — RP5-6 470 −5.2V

PTCTRØ8 — LDSEQ+ — U38A 10104 — RP5-7 470 −5.2V

SEQUENCER RAM

U37 10148
U25 10148
U13 10148

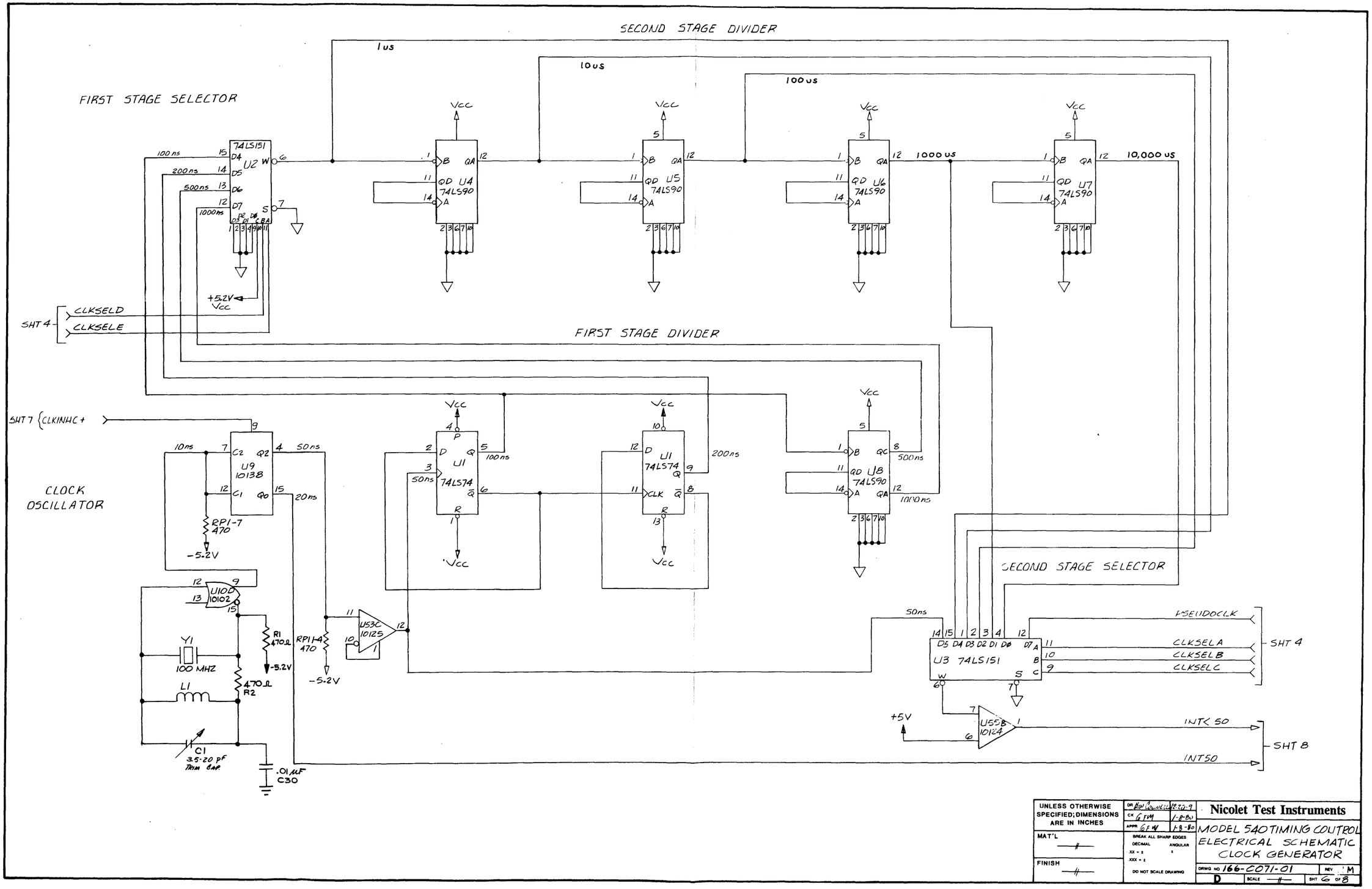
RP3-8 470 −5.2V
RP3-7 470 −5.2V
RP3-6 470 −5.2V

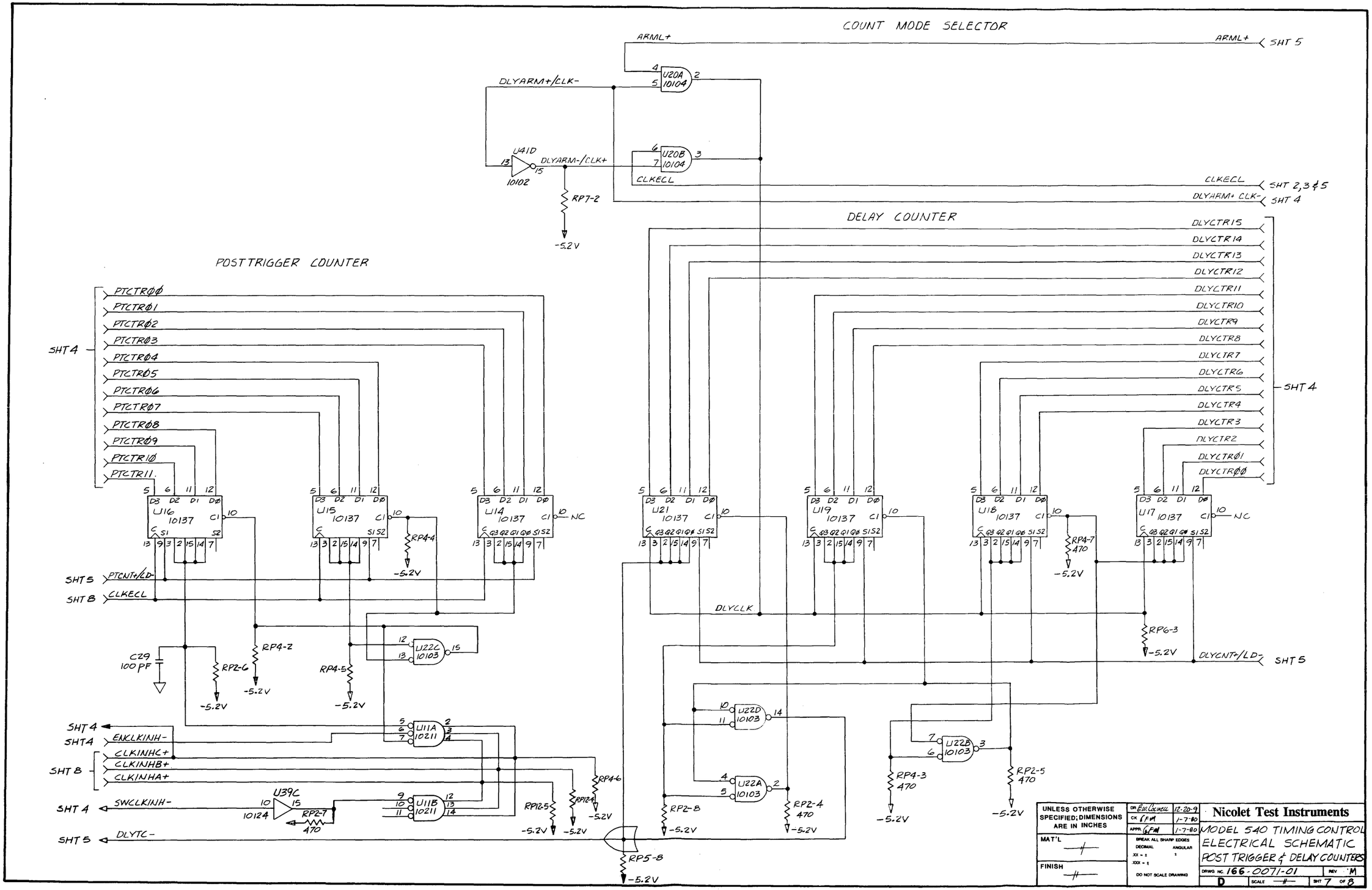
S2 — FT

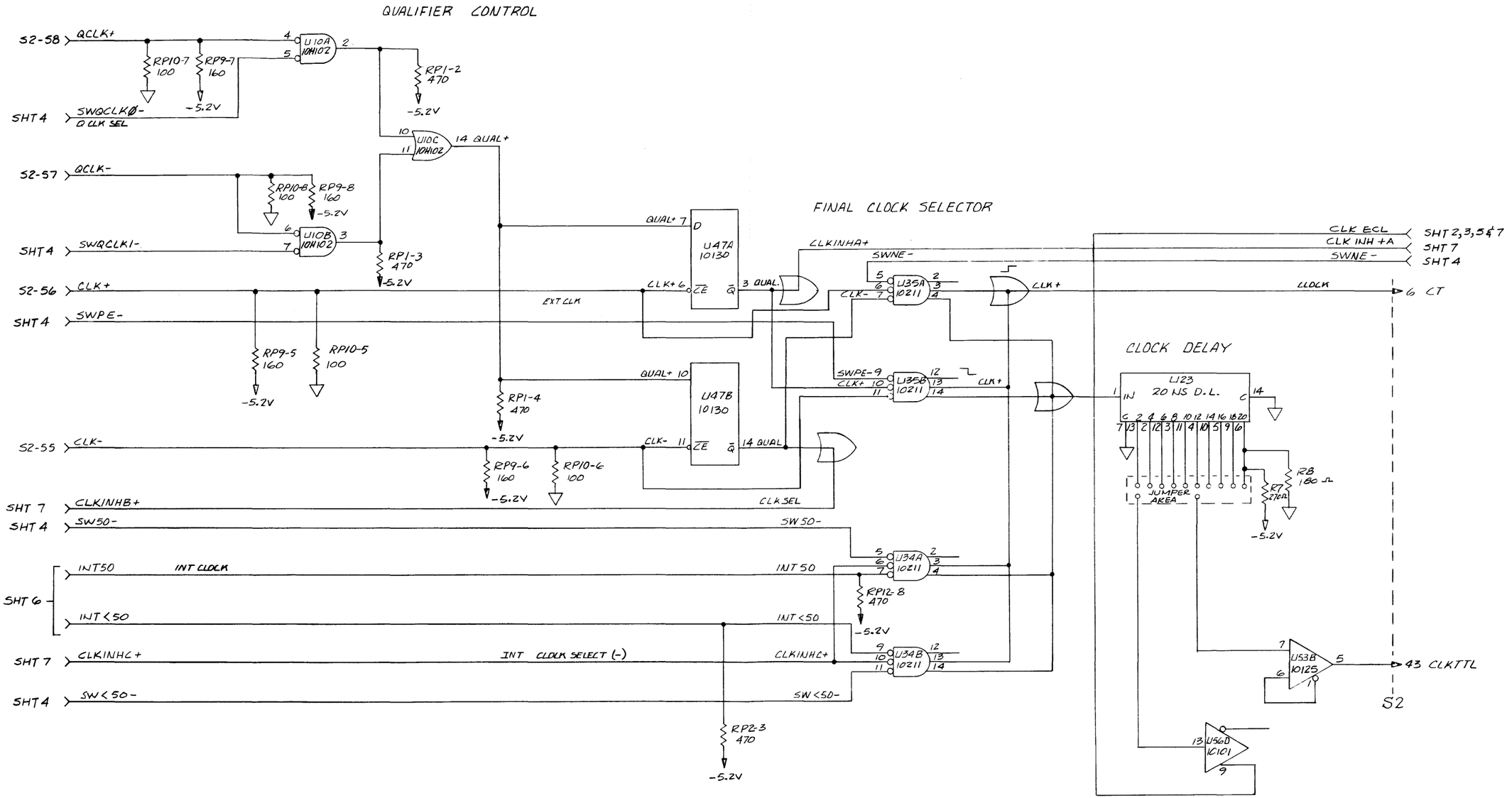
U36A 10125 — FTTTL
U36D 10125 — SØTTL
U36C 10125 — S1TTL
U36B 10125 — S2TTL

SHT 4

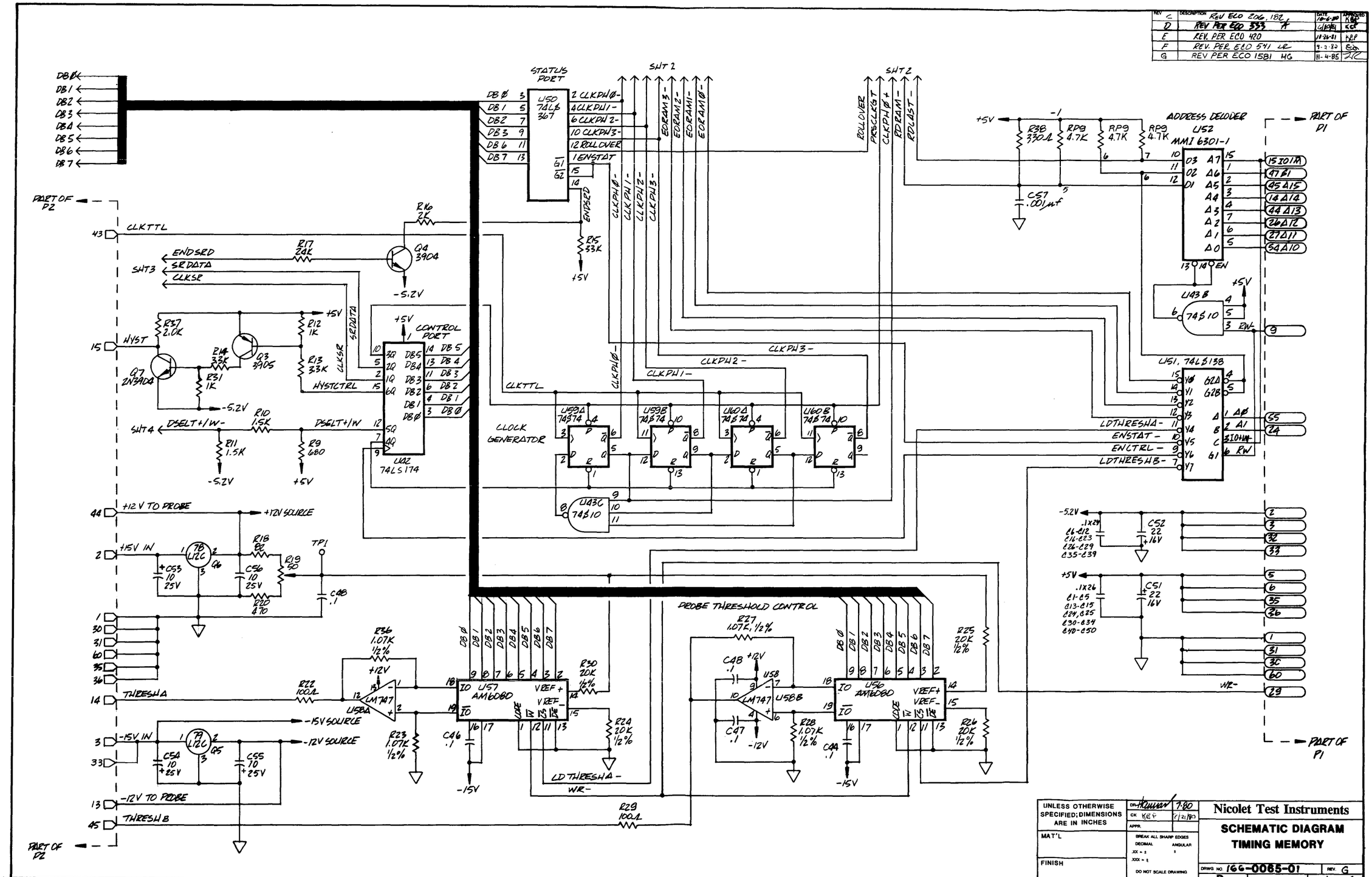
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR B.W.Conwell 12-20-79	Nicolet Test Instruments	
	CK G.F.M 1-7-80	MODEL 540 TIMING CONTROL	
MAT'L —	APPR G.F.M 1-8-80	ELECTRICAL SCHEMATIC	
FINISH —	BREAK ALL SHARP EDGES; DECIMAL ANGULAR ±; XX = ±; XXX = ±	SEQUENCER	
	DO NOT SCALE DRAWING	DRWG NO 166-0071-01 REV LM	
	D SCALE —	SHT 5 OF 8	


SECOND STAGE DIVIDER
FIRST STAGE SELECTOR
1us
10us
100us
1000us
10,000us
74LS151
U2
U4
74LS90
U5
74LS90
U6
74LS90
U7
74LS90
100ns
200ns
500ns
1000ns
+5.2V
Vcc
SHT 4
CLKSELD
CLKSELE
FIRST STAGE DIVIDER
SHT 7
CLKINHC+
CLOCK OSCILLATOR
U9
10138
10ns
50ns
20ns
RP1-7
470
-5.2V
U1
74LS74
100ns
50ns
U1
74LS74
200ns
U8
74LS90
500ns
1000ns
SECOND STAGE SELECTOR
U10D
10102
Y1
100 MHZ
L1
R1
470Ω
470Ω
R2
C1
3.5-20 pF
Trim Cap.
.01µF
C30
RP11-4
470
U53C
10125
50ns
U3
74LS151
PSEUDOCLK
CLKSELA
CLKSELB
CLKSELC
SHT 4
+5V
U55B
10124
INT< 50
INT50
SHT 8
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DECIMAL
ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
CLOCK GENERATOR
DRWG NO 166-C071-01
REV M
D
SCALE
SHT 6 OF 8

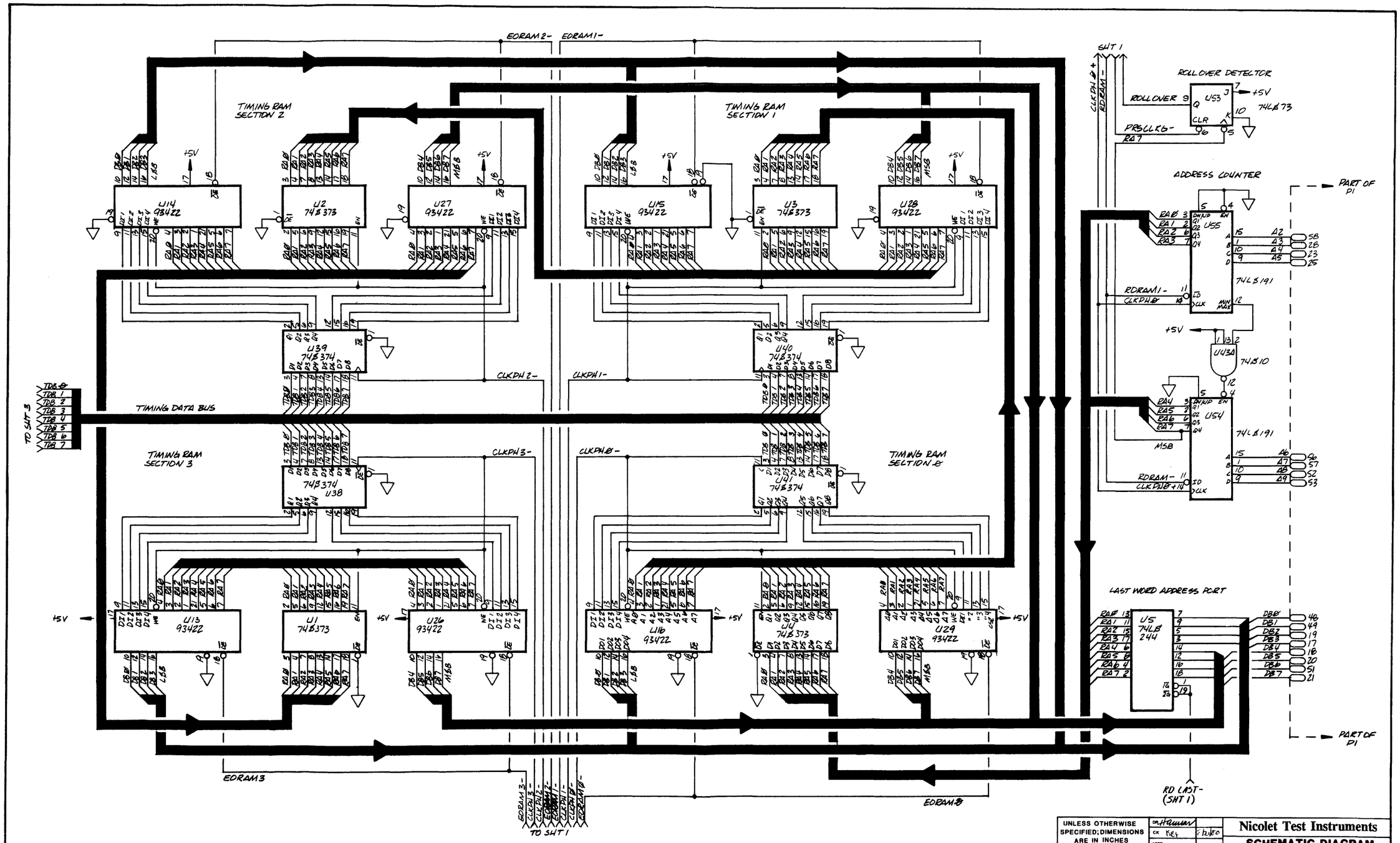

COUNT MODE SELECTOR
ARML+
SHT 5
DLYARM+/CLK-
U20A 10104
U20B 10104
U41D 10102
DLYARM-/CLK+
CLKECL
SHT 2,3 & 5
DLYARM+ CLK-
SHT 4
RP7-2
-5.2V
DELAY COUNTER
DLYCTR15
DLYCTR14
DLYCTR13
DLYCTR12
DLYCTR11
DLYCTR10
DLYCTR9
DLYCTR8
DLYCTR7
DLYCTR6
DLYCTR5
DLYCTR4
DLYCTR3
DLYCTR2
DLYCTRØ1
DLYCTRØØ
POSTTRIGGER COUNTER
PTCTRØØ
PTCTRØ1
PTCTRØ2
PTCTRØ3
PTCTRØ4
PTCTRØ5
PTCTRØ6
PTCTRØ7
PTCTRØ8
PTCTRØ9
PTCTR1Ø
PTCTR11
U16 10137
U15 10137
U14 10137
U21 10137
U19 10137
U18 10137
U17 10137
NC
RP4-4
RP4-7 470
RP6-3
SHT 5
PTCNT+/LD-
SHT 8
CLKECL
DLYCLK
DLYCNT+/LD-
C29 100 PF
RP2-6
RP4-2
RP4-5
U22C 10103
U22D 10103
U22A 10103
U22B 10103
U11A 10211
U11B 10211
U39C 10124
ENCLKINH-
CLKINHC+
CLKINHB+
CLKINHA+
SWCLKINH-
DLYTC-
RP2-7 470
RP12-5
RP12-4
RP4-6
RP2-8
RP2-4 470
RP4-3 470
RP2-5 470
RP5-8
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DR 12-20-9
CK 1-7-80
APPR 1-7-80
BREAK ALL SHARP EDGES
DECIMAL
ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
POST TRIGGER & DELAY COUNTERS
DRWG NO. 166-0071-01
REV M
D
SCALE
SHT 7 OF 8



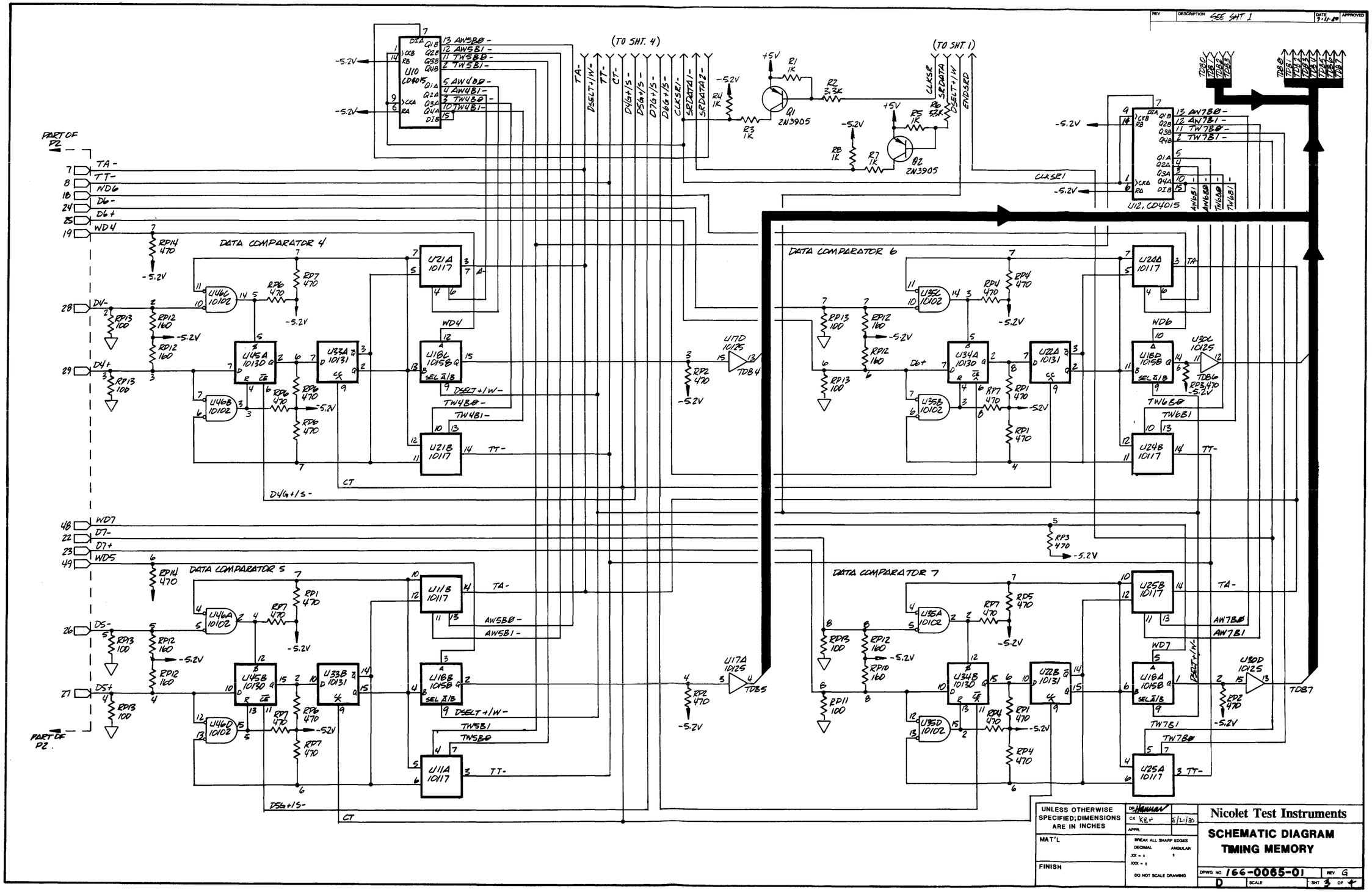
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR B.W. Colwell 12-20-79	Nicolet Test Instruments
MAT'L —	CK C.H. 12-21-79	MODEL 540 TIMING CONTROL
FINISH —	APPR.	ELECTRICAL SCHEMATIC
BREAK ALL SHARP EDGES DECIMAL ANGULAR .XX ± .1 ± .XXX ± .5	DO NOT SCALE DRAWING	CLOCK CONTROL
		DRWG NO 166-0071-01 REV M
		D SCALE — SHT 8 OF 8



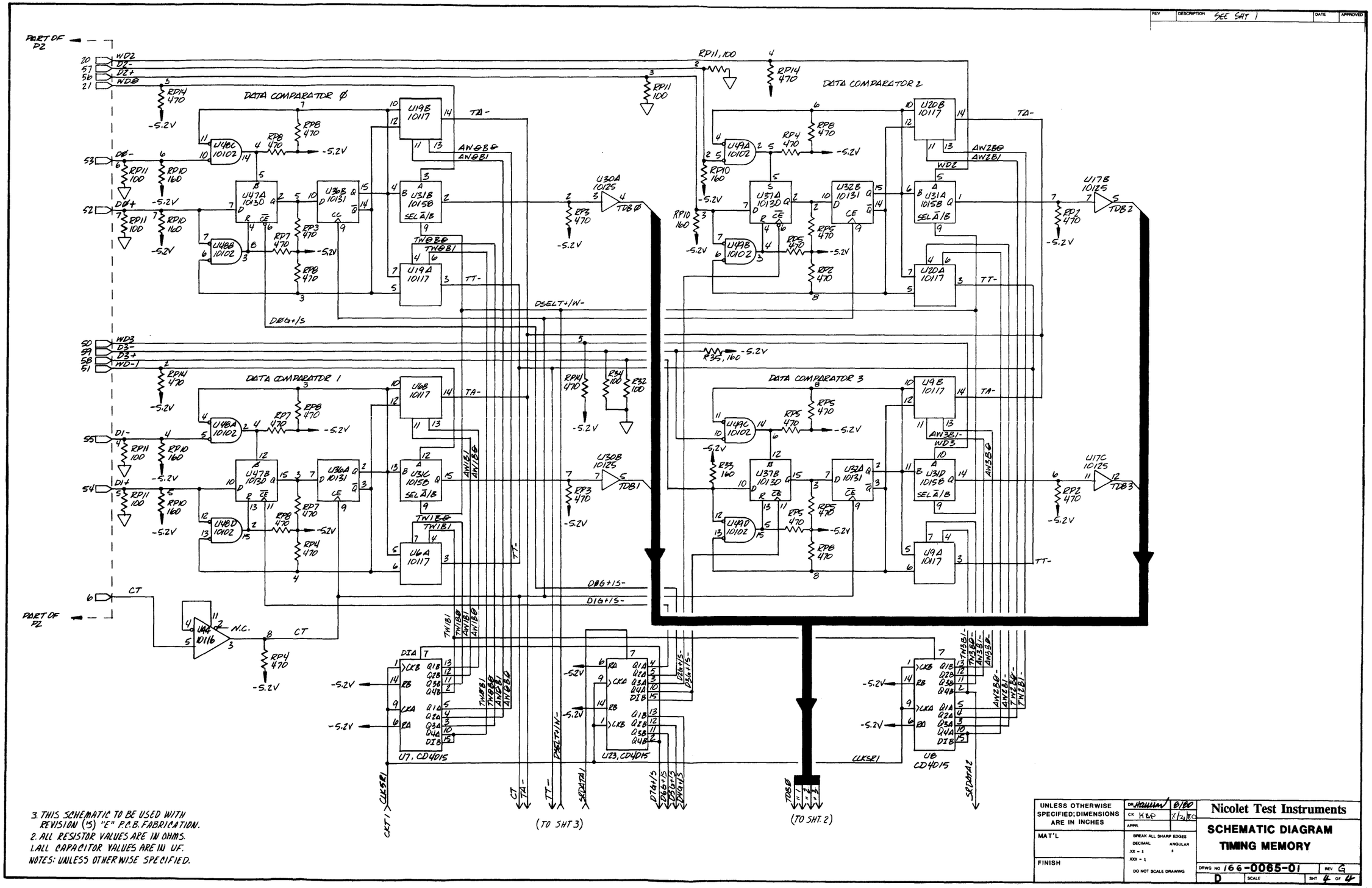
REV ECO 206, 182
REV PER ECO 333
REV. PER ECO 420
REV. PER ECO 541
REV PER ECO 1581 HG
STATUS PORT
U50 74LS 367
CONTROL PORT
U42 74LS174
CLOCK GENERATOR
U59A 74S74
U59B 74S74
U60A 74S74
U60B 74S74
U43C 74S10
U43B 74S10
U51, 74LS138
ADDRESS DECODER
U52 MMI 6301-1
PROBE THRESHOLD CONTROL
U57 AM6080
U56 AM6080
U58A LM747
U58B LM747
PART OF P1
PART OF P2
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
Nicolet Test Instruments
SCHEMATIC DIAGRAM
TIMING MEMORY
DRWG NO. 166-0065-01
REV. G
SHT 1 OF 4



EDRAM2-
EDRAM1-
TIMING RAM SECTION 2
TIMING RAM SECTION 1
TIMING RAM SECTION 3
TIMING RAM SECTION Ø
TIMING DATA BUS
TO SHT 3
CLKPH2-
CLKPH1-
CLKPH3-
CLKPHØ-
EDRAM3
EDRAMØ
TO SHT 1
SHT 1
ROLLOVER DETECTOR
ROLLOVER
PRSCLKG-
ADDRESS COUNTER
PART OF P1
RDRAM1-
CLKPHØ
MSB
RDRAM-
CLKPHØ+
LAST WORD ADDRESS PORT
RD LAST- (SHT 1)
U14 93422
U2 74S373
U27 93422
U15 93422
U3 74S373
U28 93422
U39 74S374
U40 74S374
U38 74S374
U41 74S374
U13 93422
U1 74S373
U26 93422
U16 93422
U4 74S373
U29 93422
U53 74LS73
U55 74LS191
U43A 74S10
U54 74LS191
U5 74LS244
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DECIMAL
ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
SCHEMATIC DIAGRAM
TIMING MEMORY
DRWG NO 166-0065-01
REV G
D
SCALE
SHT 2 OF 4



REV
DESCRIPTION SEE SHT 1
DATE 9-11-80
APPROVED
(TO SHT. 4)
(TO SHT. 1)
PART OF P2
DATA COMPARATOR 4
DATA COMPARATOR 5
DATA COMPARATOR 6
DATA COMPARATOR 7
U10 CD4015
U12, CD4015
Q1 2N3905
Q2 2N3905
U17D 10125
U17A 10125
U30C 10125
U30D 10125
TDB4
TDB5
TDB6
TDB7
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DECIMAL
ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
SCHEMATIC DIAGRAM
TIMING MEMORY
DRWG. NO. 166-0065-01
REV. G
D
SCALE
SHT 3 OF 4



REV
DESCRIPTION SEE SHT 1
DATE
APPROVED
PART OF P2
DATA COMPARATOR Ø
DATA COMPARATOR 1
DATA COMPARATOR 2
DATA COMPARATOR 3
U7, CD4015
U23, CD4015
U8 CD4015
(TO SHT 3)
(TO SHT. 2)
3. THIS SCHEMATIC TO BE USED WITH REVISION ('S) "E" P.C.B. FABRICATION.
2. ALL RESISTOR VALUES ARE IN OHMS.
1. ALL CAPACITOR VALUES ARE IN UF.
NOTES: UNLESS OTHERWISE SPECIFIED.
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DR Hauman 8/80
CK KBP 8/21/80
APPR
BREAK ALL SHARP EDGES
DECIMAL
ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
SCHEMATIC DIAGRAM
TIMING MEMORY
DRWG NO 166-0065-01
REV G
D
SCALE
SHT 4 OF 4

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF NICOLET PARATRONICS CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF NICOLET PARATRONICS CORPORATION

REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECO 953	11-29-83	
B	REV PER ECO 990 ME	1-1-84	
C	REV PER ECO 1016 ME	2-5-84	
D	REV. PER ECO 1037 LWM	2-15-84	
E	REV PER ECO 1059 ME	3-27-84	
B/A	REV PER ECO 1049 ME	5-1-84	
C/A	REV PER ECO 1151 MR	7-10-84	
C/B	REV PER ECO 1231 RP	9-24-84	
C/C	REV. PER ECO 1244 PP	10/11/84	
D/A	REV. PER ECO 1281 RP	11/8/84	
E/A	REV. PER ECO 1301 MG	12-8-	
E/B	REV. PER ECO 1409 LM	4-19-85	
E/C	REV. PER ECO 1462	6-18-85	

SPARE GATES

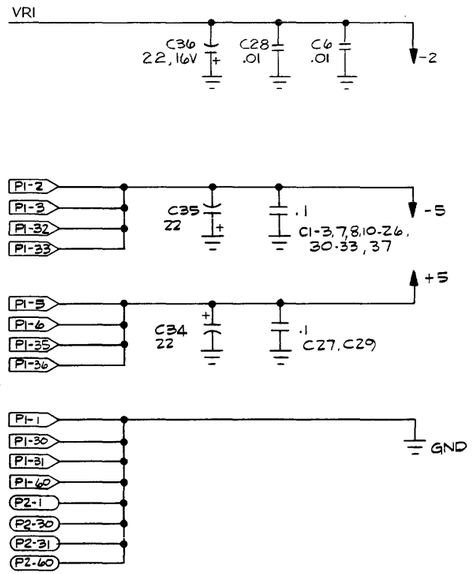
REF. DES.	TYPE	PIN NO.
U5	10102	10,11,14
U70	10102	2,4,5, 3,6,7
U68	10124	6,10,12,15
U11	10H102	9,12,13,15
U59	10H102	10,11,14
U36	10H104	10,11,14
U48	10H105	6,7,9,10,11
U35	10H107	12,14,15
U61	10H131	9,10,11,12,13
U72	40158	2,11,12,13,15
U49	10H131	2,3,4,5,6,7

REFERENCE DESIGNATOR

LAST USED	NOT USED
R27	R2 ,R3,R28,24
U73	U1
C39	
CR1	
Y1	
Q2	
RP27	
L1	L2

POWER & GROUND LOCATOR CHART

REF. DES.	TYPE	GND	+5	-5	-2	PIN NO.
U62	3430	8	16	12		16
U10,12,13,19,53,66,67,2:72 73	4015B	16		6,8,14		16
U39,54	4518	2,10,16		7,8,15		16
U5,70	10102	1,16		8		16
U47	10103	1,16		8		16
U68	10124	16	9	8		16
U56	10130	1,16		8		16
U7,20,27,28,42	10136	1,16		8		16
U23,24,52	10138	1,16		8		16
U38	10164	1,16		8		16
U3	10H103	1,16		8		16
U2,45,9,11,15,17,25 3731,59	10H102	1,16		8		16
U32,36	10H104	1,16		8		16
U43,44,48	10H105	1,16		8		16
U35	10H107	1,16		8		16
U6	10H109	1,16		8		16
U71	10H116	1,16		8		16
U16,18	10H117	1,16		8		16
U14,31,34,40,46,49,50	10H131	1,16		8		16
U55,57,58,61,22	10H131	1,16		8		16
U30,33	10H136	1,16		8		16
U4,8,29	10H210	1,16,15		8		16
U41,26	10H211	1,16,15		8		16
U63	74LS138	8	16			16
U64	LM339		3	12		14
U69	SPARE					
U65	10104	1,16		8		
RP1,6,7,9,10,12,13,14,16,19,20,22	270/162	8		1		8
RP25	270/162	8		1		8
RP2,11,17,21,23,24,26,27	470			1		8
RP3	100				1	10
RP4,5,8,15,18,	100				1	8
U60	101 7	1,16		8		16



ITEM / LTR	P/N	DESCRIPTION	QTY

MATERIAL

FINISH

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; RESISTORS ARE IN OHMS; CAPACITORS ARE IN uf

DRN BY JBAY DATE

CHK'D DATE

ENG DATE 11-7-84

MFG DATE

DECIMAL XX = XXX =

ANGULAR ±

BREAK ALL SHARP EDGES

DO NOT SCALE DRAWING

Nicolet Test Intruments

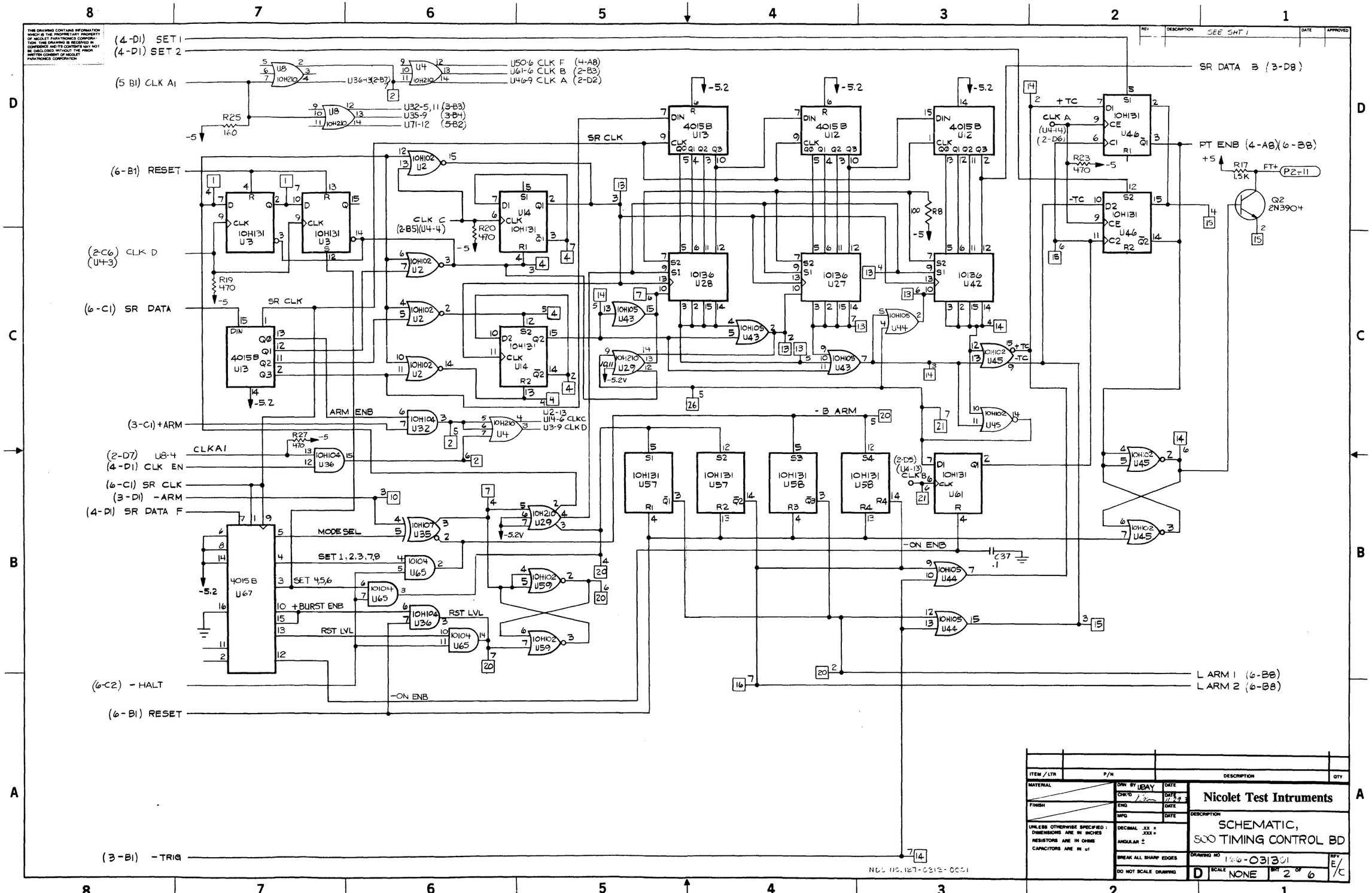
DESCRIPTION: SCHEMATIC, 800 TIMING CONTROL BD.

DRAWING NO 146-03180 1

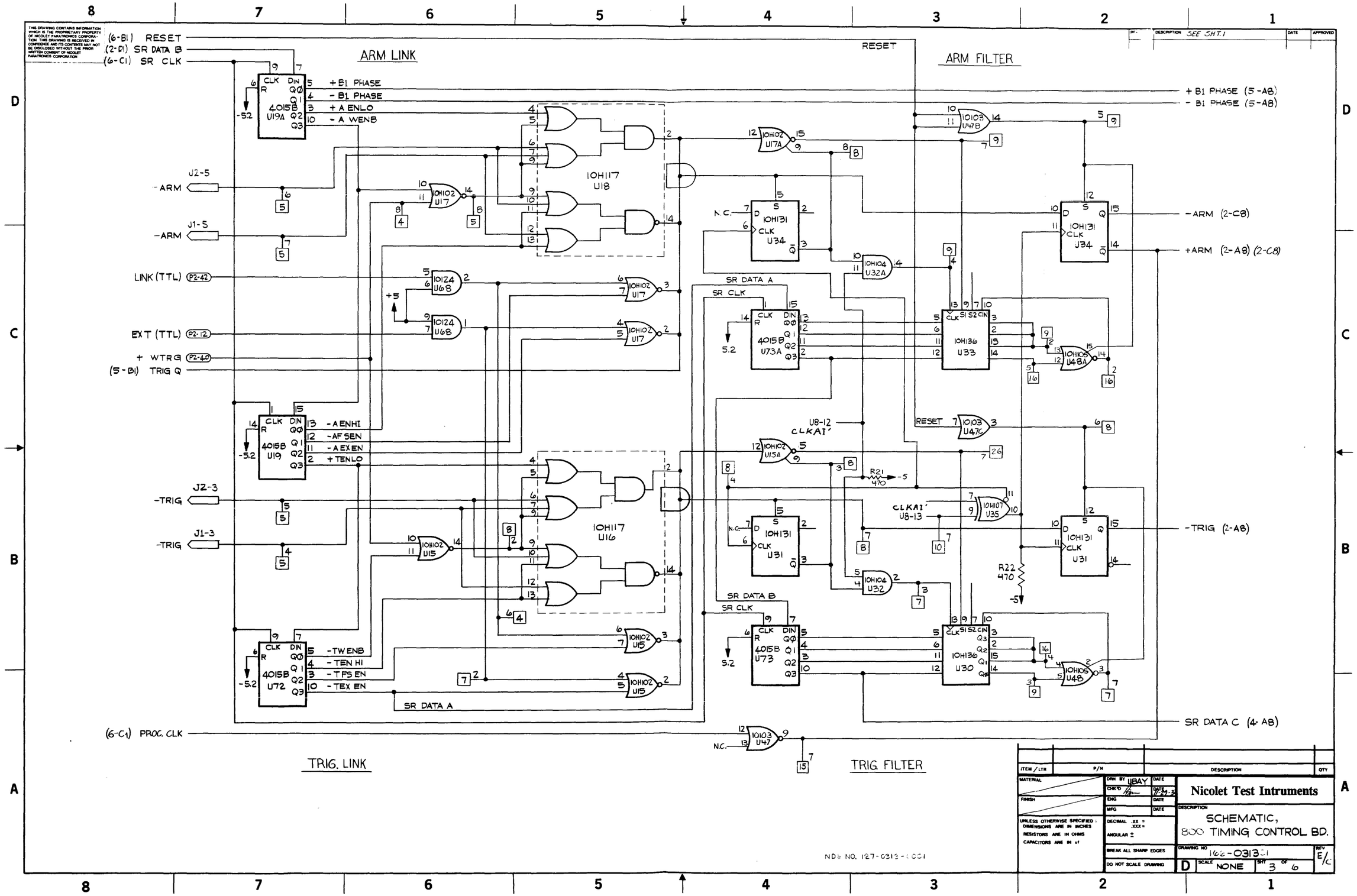
REV E/C

D SCALE NONE SHT 1 OF 6

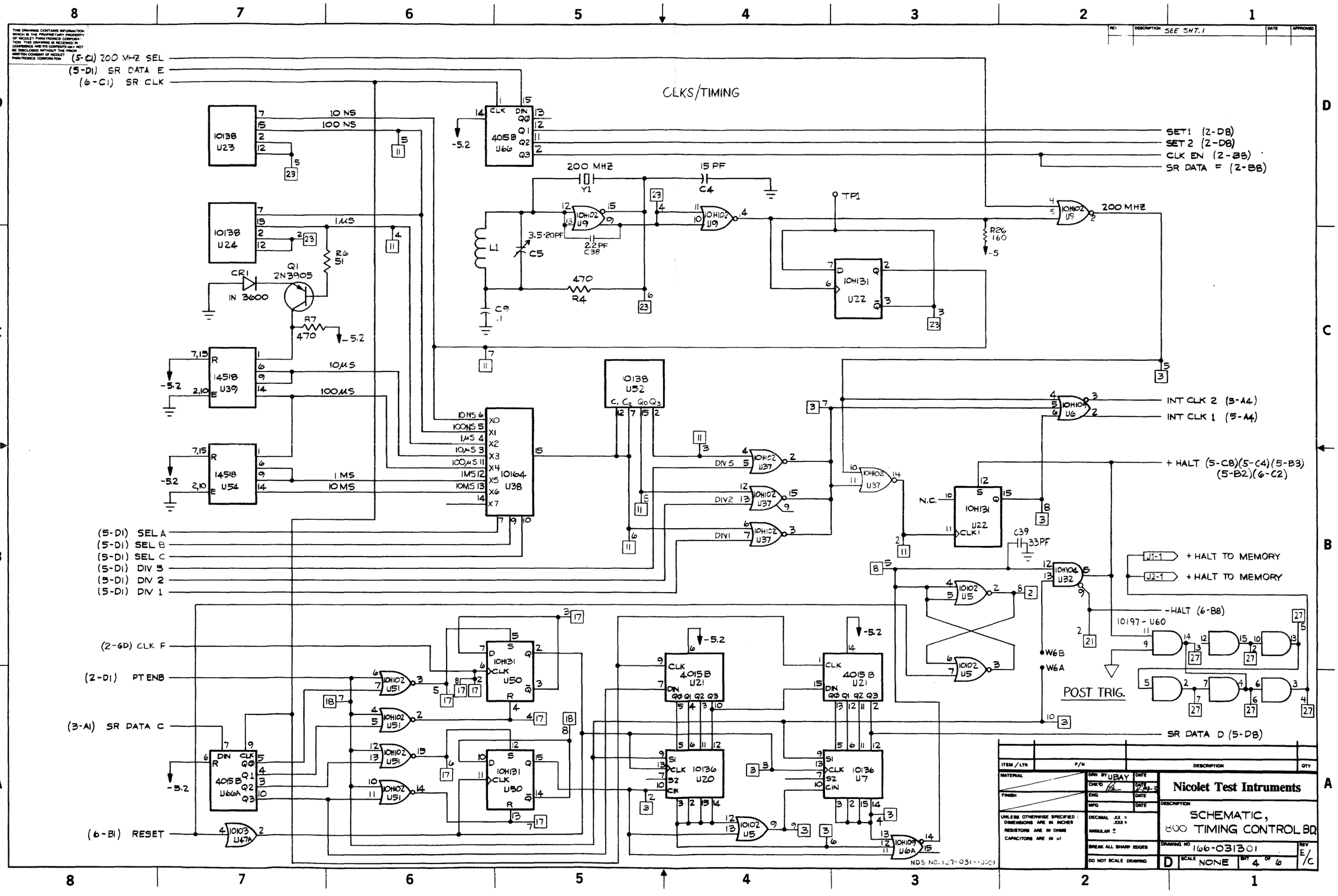
NDS NO. 127-0318[illegible]-001

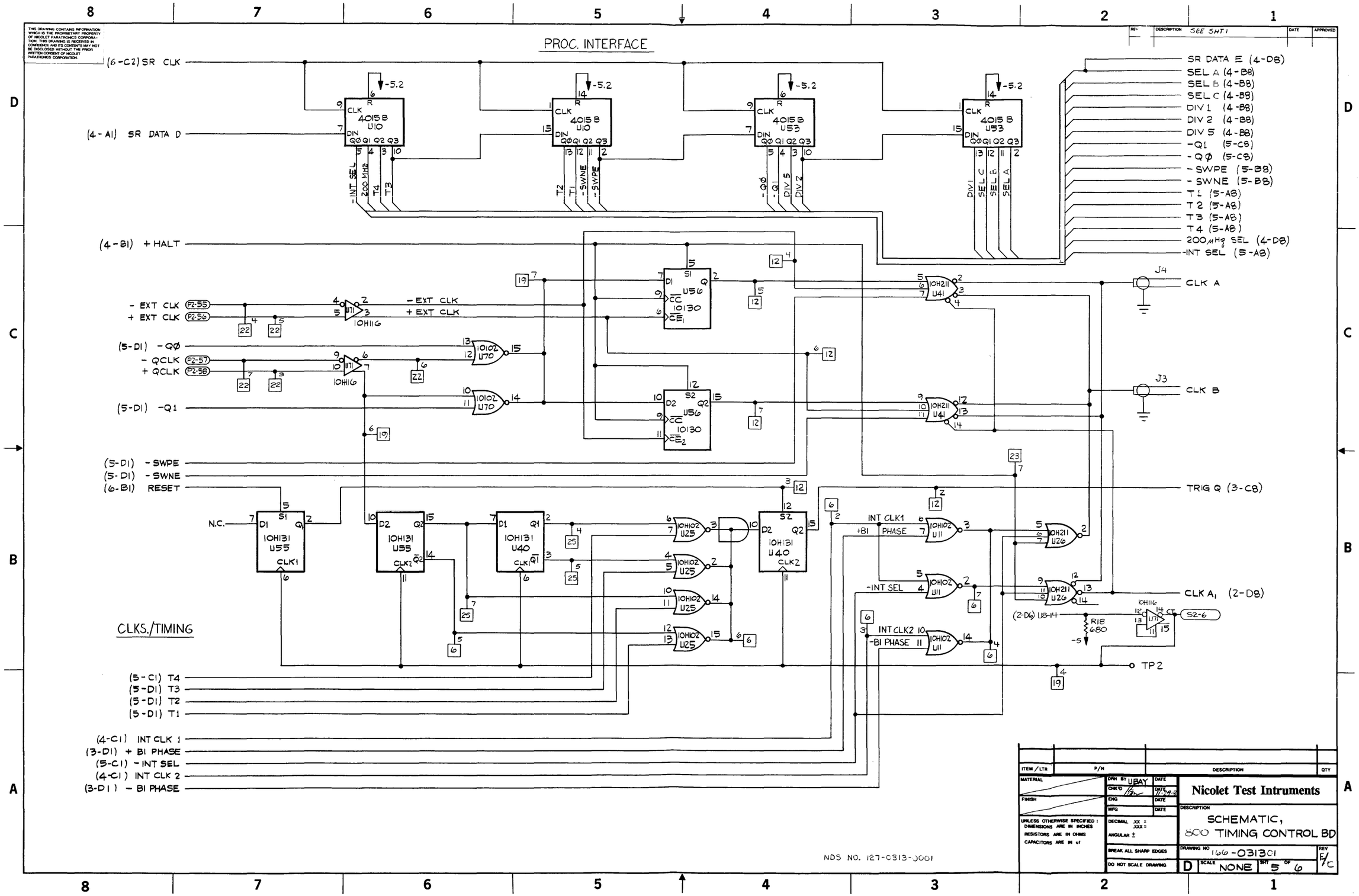


(4-D1) SET 1
(4-D1) SET 2
(5 B1) CLK A1
(6-B1) RESET
(2-C6) CLK D (U4-3)
(6-C1) SR DATA
(3-C1) +ARM
(2-D7) U8-4 CLKA1
(4-D1) CLK EN
(6-C1) SR CLK
(3-D1) -ARM
(4-D1) SR DATA F
(6-C2) -HALT
(6-B1) RESET
(3-B1) -TRIG
SR DATA B (3-D8)
PT ENB (4-A8)(6-B8)
L ARM 1 (6-B8)
L ARM 2 (6-B8)
SR CLK
ARM ENB
MODE SEL
SET 1,2,3,7,8
SET 4,5,6
+BURST ENB
RST LVL
-ON ENB
-B ARM
CLK A
CLK B
CLK C
CLK D
Q2 2N3904
FT+
P2-11
SEE SHT 1
Nicolet Test Intruments
SCHEMATIC, 500 TIMING CONTROL BD
DRAWING NO 166-031301
SCALE NONE
SHT 2 OF 6
REV E/C



ARM LINK
ARM FILTER
TRIG. LINK
TRIG. FILTER
(6-B1) RESET
(2-D1) SR DATA B
(6-C1) SR CLK
+B1 PHASE
-B1 PHASE
+A ENLO
-A WENB
-ARM
LINK (TTL)
EXT (TTL)
+ WTRG
(5-B1) TRIG Q
-A ENHI
-AF SEN
-A EX EN
+TENLO
-TRIG
-TW ENB
-TEN HI
-TFS EN
-TEX EN
SR DATA A
SR DATA B
SR CLK
(6-C1) PROC. CLK
+B1 PHASE (5-A8)
-B1 PHASE (5-A8)
-ARM (2-C8)
+ARM (2-A8) (2-C8)
-TRIG (2-A8)
SR DATA C (4-A8)
CLKA1'
U8-12
U8-13
R21 470
R22 470
10H117 U18
10H117 U16
4015B U19A
4015B U19
4015B U72
4015B U73A
4015B U73
10H131 U34
10H131 U31
10H136 U33
10H136 U30
10H102 U17
10H102 U15
10H102 U17A
10H104 U32A
10H104 U32
10H103 U47B
10H103 U47C
10H103 U47
10H105 U48A
10H105 U48
10H107 U35
10124 U68
NDS NO. 127-0313-0001
Nicolet Test Intruments
SCHEMATIC, 800 TIMING CONTROL BD.
DRAWING NO 166-0313-01
SCALE NONE
SHT 3 OF 6


CLKS/TIMING
(5-C1) 200 MHZ SEL
(5-D1) SR DATA E
(6-C1) SR CLK
SET1 (2-D8)
SET 2 (2-D8)
CLK EN (2-B8)
SR DATA F (2-B8)
200 MHZ
15 PF
TP1
INT CLK 2 (5-A4)
INT CLK 1 (5-A4)
+ HALT (5-C8)(5-C4)(5-B3)(5-B2)(6-C2)
+ HALT TO MEMORY
-HALT (6-B8)
POST TRIG.
SR DATA D (5-D8)
(5-D1) SEL A
(5-D1) SEL B
(5-D1) SEL C
(5-D1) DIV 5
(5-D1) DIV 2
(5-D1) DIV 1
(2-6D) CLK F
(2-D1) PT ENB
(3-A1) SR DATA C
(6-B1) RESET
Nicolet Test Intruments
SCHEMATIC, 800 TIMING CONTROL BD
166-031301
NONE
4 OF 6


PROC. INTERFACE
CLKS./TIMING
(6-C2) SR CLK
(4-A1) SR DATA D
(4-B1) + HALT
- EXT CLK
+ EXT CLK
(5-D1) -QØ
- QCLK
+ QCLK
(5-D1) -Q1
(5-D1) - SWPE
(5-D1) - SWNE
(6-B1) RESET
N.C.
(5-C1) T4
(5-D1) T3
(5-D1) T2
(5-D1) T1
(4-C1) INT CLK 1
(3-D1) + B1 PHASE
(5-C1) - INT SEL
(4-C1) INT CLK 2
(3-D1) - B1 PHASE
SR DATA E (4-D8)
SEL A (4-B8)
SEL B (4-B8)
SEL C (4-B8)
DIV 1 (4-B8)
DIV 2 (4-B8)
DIV 5 (4-B8)
-Q1 (5-C8)
-QØ (5-C8)
- SWPE (5-B8)
- SWNE (5-B8)
T1 (5-A8)
T2 (5-A8)
T3 (5-A8)
T4 (5-A8)
200 μHz SEL (4-D8)
-INT SEL (5-A8)
CLK A
CLK B
TRIG Q (3-C8)
CLK A1 (2-D8)
TP2
INT CLK1
+B1 PHASE
-INT SEL
INT CLK2
-B1 PHASE
4015B U10
4015B U53
10H131 U55
10H131 U40
10H130 U56
10H116
10H102 U70
10H102 U25
10H102 U11
10H211 U41
10H211 U26
R18 680
S2-6
NDS NO. 127-0313-0001
Nicolet Test Intruments
SCHEMATIC, 800 TIMING CONTROL BD
DRAWING NO 166-031301
SCALE NONE
SHT 5 OF 6
D

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RE	DESCRIPTION	DATE	APPROVED
	SEE SHT. 1		

PROC. INTERFACE

DB1 P1-49
DB0 P1-48
A0 P1-59
A1 P1-24
A2 P1-58
A13 P1-44
I/OEN P1-8
A11 P1-27
(4-B1) -HALT
(2-B1) L ARM 1
(2-A1) L ARM 2
(2-D1) PT ENB

+5V
LM339 U64
R11 1K
R16 1K
R13 1K
R12 470
74LS138 U63
10H131 U49
10124 U68
3430 U62
R15 2K
R14 1K
R10 3.3K
R9 1.2K
-5.2
R1 1K
R5 270 5%
LM337T VR1
C35 16V 22
C36 16V 22
C28 .01
C6 .01
-2.0V

SR DATA (2-C8)
+HALT (4-B2)
-HALT (2-AB)
-PROC. CLK (3-A8)
SR CLK (2-B8)(3-D8)(4-D8)(5-D8)
RESET (2-A8)(3-D9)(4-A8)(5-B8)
DB7 P1-21
DB6 P1-5
DB5 P1-20
DB4 P1-18
-Rd STAT

NDS NO. 127-0313-0001

ITEM / LTR	P/N	DESCRIPTION	QTY

MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
RESISTORS ARE IN OHMS
CAPACITORS ARE IN uf

DRN BY UBAY DATE
CHK'D DATE
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

Nicolet Test Intruments

DESCRIPTION
SCHEMATIC, 800 TIMING CONTROL BD

DRAWING NO 166-031301 REV E/C
D SCALE NONE SHT 6 OF 6

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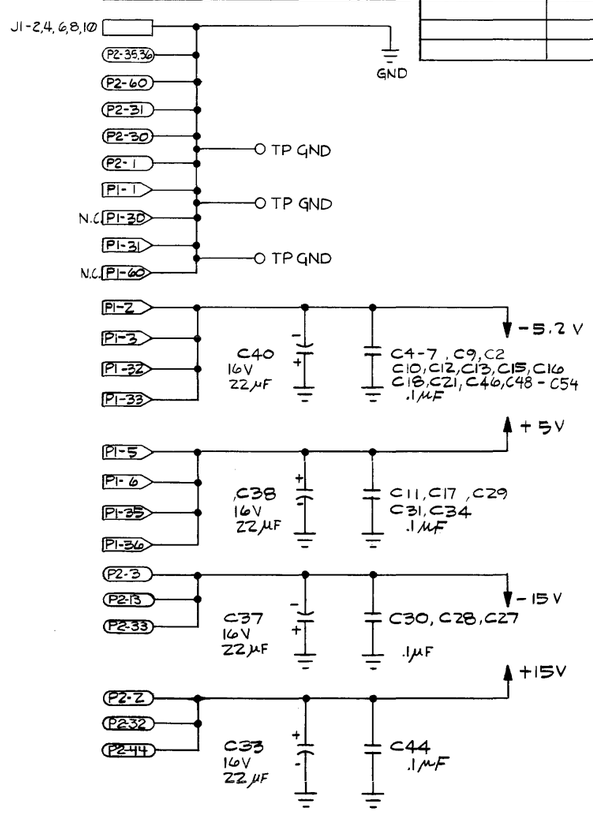
REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECO 905 LK	11-26-83	
B	REV. PER ECO 991 LW	1-5-84	
C	REV. PER ECO 999 ME	1-31-84	
D	REV. PER ECO 1038 ME	3-13-84	
E	REV. PER ECO 1058 MR	3-27-84	
B/A	REV. PER ECO 1097 ME	5-7-84	
C/A	REV. PER ECO 1151 MR	7-10-84	
C/B	REV. PER ECO 1230 RP	9-28-84	
C/C	REV. PER ECO 1246 RP	10/11/84	
D/A	REV. PER ECO 1265 RP	11/8/84	
E/A	REV. PER ECO 1300 MG	1-3-85	
E/B	REV. PER ECO 1357 LK	2-12-85	
E/C	REV. PER ECO 1425 LK	5-9-85	
E/D	REV. PER ECO 1469 LW	6-27-85	
E/E	REV PER ECO 1562 MG	1-7-86	

SPARE GATES

REF. DES.	TYPE	PIN NO.

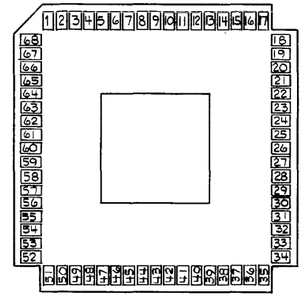
REFERENCE DESIGNATOR

LAST USED	NOT USED
U55	
RP30	
CR2	
C55	C45
R60	R15, R32, 11, 12, 13, 17
	21, 45, 49
TP1	
TPG3	
VR2	
Q4	

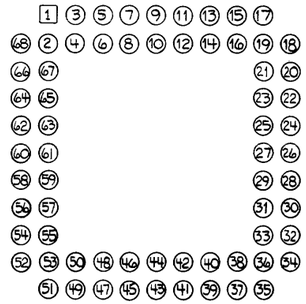


POWER & GROUND LOCATOR CHART

REF. DES.	TYPE	GND	+5	-5	-2	PIN NO.
U1	SPARE					
U2,3	10153	1,16		8		16
U4,20,21,35	10H131	1,16		8		16
U5,18,37,38	3430	8	16	12		16
U6,7,8,9,28,29,30,31	10422	1,24		12		24
U22	10104	1,16		8		16
U11, 27, 40	10H105	1,16		8		16
U12	10103	1,16		8		16
U10,13,23	10H104	1,16		8		16
U14	10H210	1,16,15		8		16
U15,16	10136	1,16		8		16
U17,	10H131	1,16		8		16
	SPARE					
U19	10H158	16		8		16
U51, 52	10H159	16		8		16
U24,25,34	10124	16	9	8		16
U39	4015	16		8		16
U26	4096	15,16		8		
U32	74LS00	7	14			14
U33	10186	16		8		16
U36	10158	16		8		16
U22	10104					
U43	LM339		3	12		
U44	74LS139	8	16			16
U45	LF347		+15: 4	-15:11		14
U46	6349	10	20			20
U47	74F245	10	20			20
U48,49,50	DAC 808	9,13,16	18	-15:15		18
U53, 54, 55	10H116	1,16		8		16
U41,42	GA	5,6,18,19,20,21,32,33,34,46,47,52,53,63,66,67,68		26,27,60,61		68
RP22,24,25,26	100Ω X7				1	8
RP1,3,10,11	470Ω X9			1		10
RP2,5-7,9,14-18,21,28-30	470Ω X7			1		8
RP19	470Ω X7	1				8
RP20	1K X9		1			10
RP4,8,13,23	162/260 X6	8		1		8
RP12 RP27	56Ω X7				1	8



GATE ARRAY PINOUT
TOP VIEW



GATE ARRAY SOCKET (PINS LOCATION)
CIRCUIT SIDE VIEW

NDS NO. 127-0312-0001

ITEM / LTR	P/N	DESCRIPTION	QTY

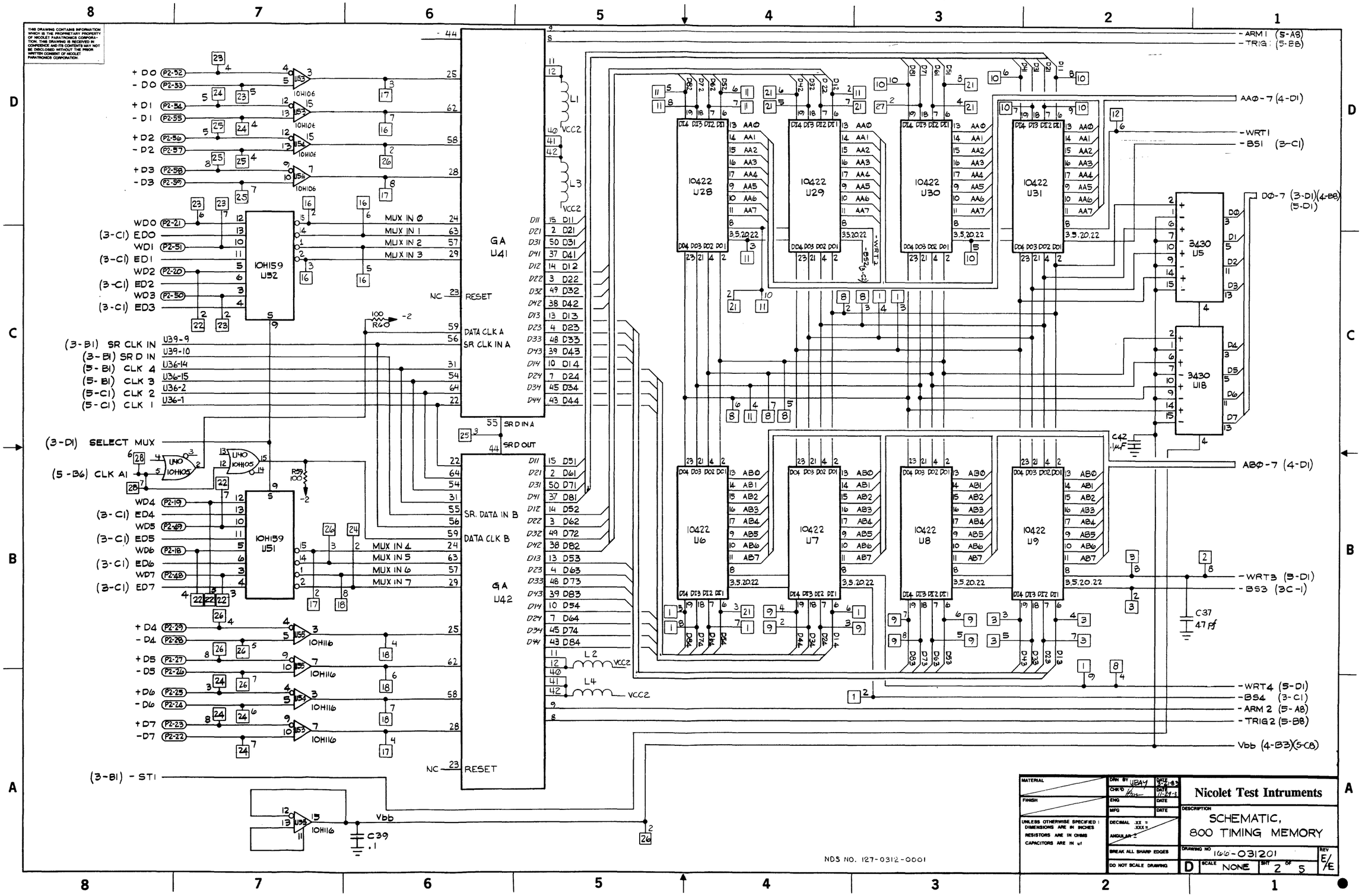
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED : DIMENSIONS ARE IN INCHES RESISTORS ARE IN OHMS CAPACITORS ARE IN uf

DRN BY LIBAY DATE 12-1-83
CHK'D DATE 12-4-83
ENG DATE
MFG DATE
DECIMAL .XX = XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

Nicolet Test Intruments

DESCRIPTION
SCHEMATIC,
800 TIMING MEMORY

DRAWING NO 166-031201 REV E/E
D SCALE NONE SHT 1 OF 5



THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF NICOLET PARATRONICS CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF NICOLET PARATRONICS CORPORATION.
GA U41
GA U42
10H159 U52
10H159 U51
10422 U28
10422 U29
10422 U30
10422 U31
10422 U6
10422 U7
10422 U8
10422 U9
3430 U5
3430 U18
MUX IN 0
MUX IN 1
MUX IN 2
MUX IN 3
MUX IN 4
MUX IN 5
MUX IN 6
MUX IN 7
RESET
DATA CLK A
SR CLK IN A
SR D IN A
SR D OUT
SR. DATA IN B
DATA CLK B
(3-B1) SR CLK IN
(3-B1) SR D IN
(5-B1) CLK 4
(5-B1) CLK 3
(5-C1) CLK 2
(5-C1) CLK 1
(3-D1) SELECT MUX
(5-B6) CLK A1
(3-B1) - ST1
- ARM 1 (5-A8)
- TRIG 1 (5-B8)
AA0-7 (4-D1)
- WRT1
- BS1 (3-C1)
D0-7 (3-D1)(4-B8) (5-D1)
AB0-7 (4-D1)
- WRT3 (5-D1)
- BS3 (3C-1)
- WRT4 (5-D1)
- BS4 (3-C1)
- ARM 2 (5-A8)
- TRIG 2 (5-B8)
Vbb (4-B3)(5-C8)
C37 47 pf
C42 .1µF
C39 .1
NDS NO. 127-0312-0001
Nicolet Test Intruments
SCHEMATIC, 800 TIMING MEMORY
166-031201
D
NONE
2 OF 5
E/E

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF NICOLET PARATRONICS CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF NICOLET PARATRONICS CORPORATION.

REV	DESCRIPTION	DATE	APPROVED
	SEE SHT 1		

PROC. INTERFACE

DB7 PI-21
DB6 PI-51
DB5 PI-20
DB4 PI-18
DB3 PI-17
DB2 PI-19
DB1 PI-49
DBØ PI-48
74LF245 U47
D7 D6 D5 D4 D3 D2 D1 DØ
DØ-7 (4-C8)(5-D1)(2-D1)
STROBE (5-C8)
74LS00 U32
-READ
-RW PI-9
A14 PI-14
A15 PI-45
A13 PI-44
A12 PI-26
A11 PI-27
A10 PI-54
-IO/M PI-15
S1 PI-47
A1 PI-24
AØ PI-55
6349 U46
RP20 1K
10124 U34
R50 3.3K
R52 1K
R58 1K
R51 1K
Q4 2N3905
-5.2
SR DATA
SR CLK IN
4094 U26
SELECT MUX (2-C8)
-HS/+LS (5-B8)
+PRESET (5-B8)(4-C3)
-PRESET (4-D8)
-BS1 (2-D1)
-BS2 (2-C3)
-BS3 (2-B1)
-BS4 (2-A1)
SR CLK
LM339 U43
470 RP19
DØ
4015B U39
-5.2V
ED7 (2-B8)
ED6 (2-B8)
ED5 (2-B8)
ED4 (2-B8)
ED3 (2-C8)
ED2 (2-C8)
ED1 (2-C8)
EDØ (2-C8)
10104 U22
SRDIN (2-C8)
SR CLK IN (2-C8)
74LS139A U44
STB
SR CLK
-ST1
U12 10103
SW CLK (4-D8)
U43 LM339
R61 470
CR3 IN3600
2K R25
1K R26
-ST1 (2-A8)
-ST2 (5-C2)(4-B3)
74LS139B U44
-LD1 (4-A8)
-LD2 (4-B8)
-LD3 (4-C8)
R37 1K
R1 270 5%
C40 16V 22
C41 16V 22µF
.1µF C1,C3,C14, C19,C8
LM337T VR2
-2

NDS NO. 127-0312-0001

ITEM / LTR	P/N	DESCRIPTION	QTY

MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES RESISTORS ARE IN OHMS CAPACITORS ARE IN uf
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

DRN BY UBAY DATE 5-21-83
CHK'D DATE
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±

Nicolet Test Intruments

DESCRIPTION
SCHEMATIC, 800 TIMING MEMORY

DRAWING NO 166-031201 REV E/E
D SCALE NONE SHT 3 OF 5

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF NICOLET PARATRONICS CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF NICOLET PARATRONICS CORPORATION.

REV	DESCRIPTION	DATE	APPROVED
	SEE SHT. 1		

(3-B1) SW CLK
-PRESET
(2-C3)(5-B1) - WRT2
(5-B1) - HALT

10H104 U13

A9 P1-53
A8 P1-52
A7 P1-51
A6 P1-50
A5 P1-25
A4 P1-23
A3 P1-20
A2 P1-58

10124 U24
10124 U25

-5.2 100

10136 U15
10136 U16

AA7 AA6 AA5 AA4 AA3 AA2 AA1 AAØ

AAØ-7 (2-D1)
ABØ-7 (2-B1)

10153 U2
10153 U3

AB7 AB6 AB5 AB4 AB3 AB2 AB1 ABØ

+5

IN916 CR2
IN958B CR1 7.5V
R57 270
+5

C30 .1
C36 .1
-15
C31 .1

R36 100
R39 2.49K 1%
1K R42

DAC 808 U50

R29 6.49K 1%
C32 .01
LF347 U45
R27 100
.01
C25

(3-A1) - LD3

D7 D6 D5 D4 D3 D2 D1 D0

(2-D1)(3-D1)(4-C8) DØ-7

C28 .1μF
C35 .1μF
-15
C34 .1
+5

R34 2.49K 1%
1K R41

DAC 808 U49

R30 6.49K 1%
C26 .01
LF347 U45
R22 100Ω
.01
C23

(3-A1) - LD2

THRESHOLD

C27 .1
C43 .1
-15
C29 .1
+5

R33 2.49K 1%
1K R40

DAC 808 U48

R28 6.49K 1%
C24 .01
LF347 U45
R24 100
C22 .01
+15

(3-A1) - LD1

-6.4 VOLTS

VR1 7905 VIN VOUT GND
-15
270 5%
R31
C47 .1
R38 500
TP1 40V
R20 5.9K 1%
R19 10.5K 1%

+ PRESET (5-B8) (3-D1)

10H131 U17 D CLK Q

OVERFLOW
C20

3430 U38

D4 D5 D6 D7

(2-A1) Vbb
(3-B5) -ST2 (5-C8)

PROC. INTERFACE

P2-45 THRESHOLD B
P2-15 THRESHOLD C
P2-14 THRESHOLD A

NDS NC. 127-0312-0001

ITEM / LTR	P/N	DESCRIPTION	QTY

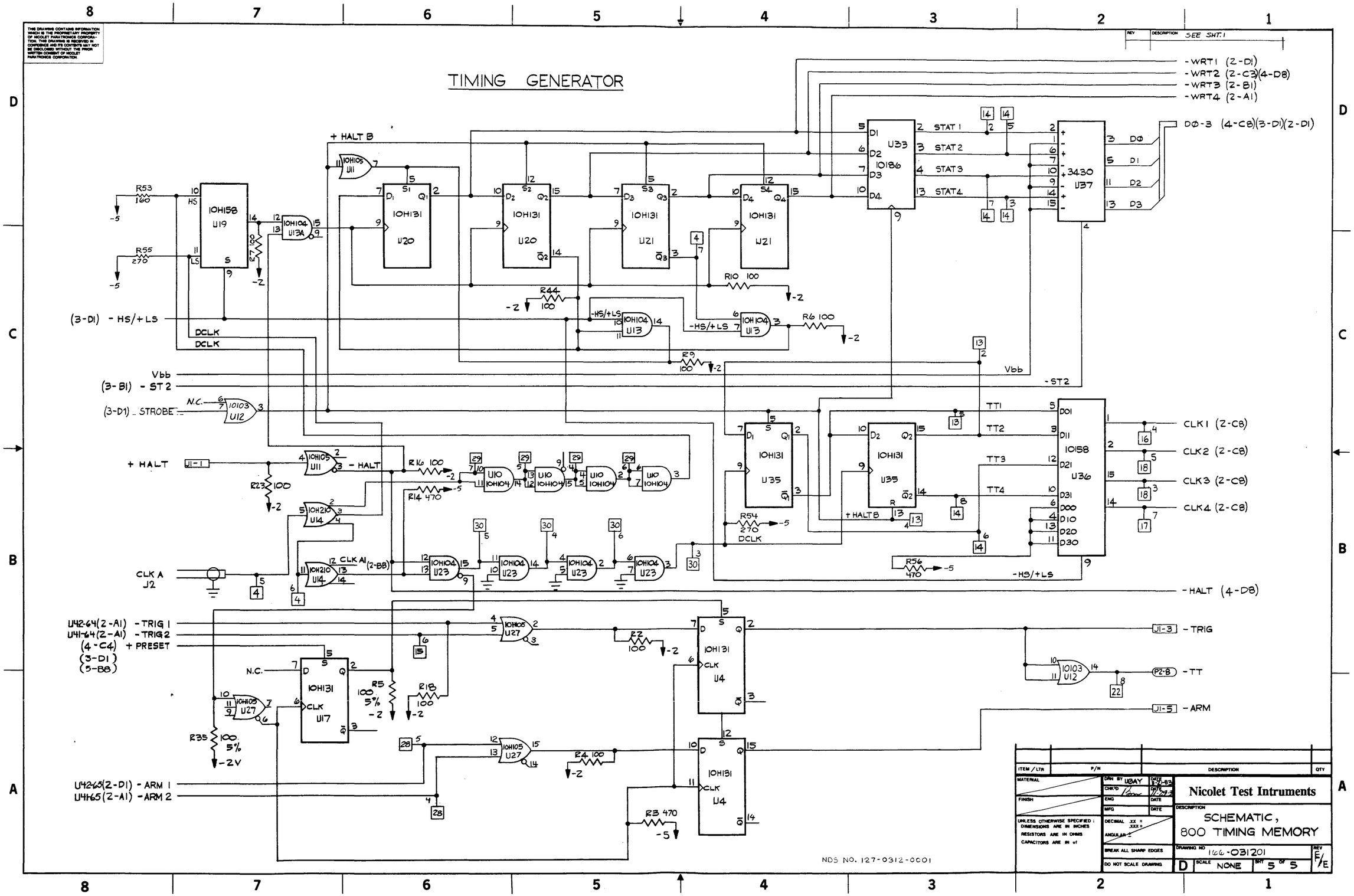
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; RESISTORS ARE IN OHMS; CAPACITORS ARE IN uf

DRN BY UBAY DATE 5-21-82
CHK'D DATE 11-29-83
ENG DATE
MFG DATE
DECIMAL .XX = .XXX =
ANGULAR ±
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

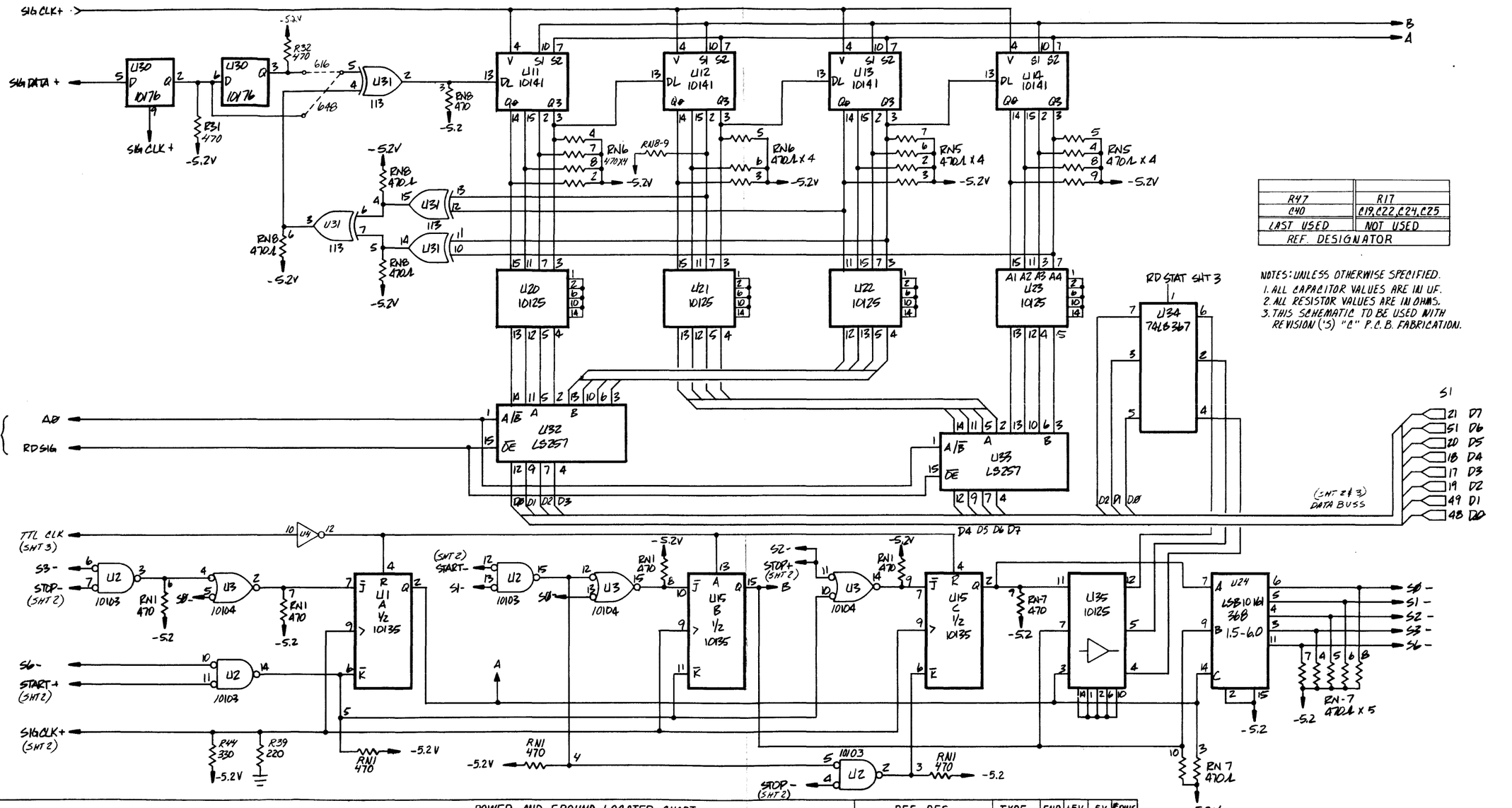
Nicolet Test Intruments

DESCRIPTION
SCHEMATIC,
800 TIMING MEMORY

DRAWING NO 1006-031201 REV E/
D SCALE NONE SHT 4 OF 5


TIMING GENERATOR
SEE SHT. 1
-WRT1 (2-D1)
-WRT2 (2-C3)(4-D8)
-WRT3 (2-B1)
-WRT4 (2-A1)
DØ-3 (4-C8)(3-D1)(2-D1)
+ HALT B
STAT 1
STAT 2
STAT 3
STAT 4
(3-D1) - HS/+LS
DCLK
Vbb
(3-B1) - ST2
(3-D1) - STROBE
+ HALT
- HALT
CLK A
J2
CLK A1 (2-B8)
CLK1 (2-C8)
CLK2 (2-C8)
CLK3 (2-C8)
CLK4 (2-C8)
- HALT (4-D8)
U42-64(2-A1) - TRIG 1
U41-64(2-A1) - TRIG 2
(4-C4) + PRESET
(3-D1)
(5-B8)
U42-65(2-D1) - ARM 1
U41-65(2-A1) - ARM 2
- TRIG
- TT
- ARM
NDS NO. 127-0312-0001
Nicolet Test Intruments
SCHEMATIC,
800 TIMING MEMORY
166-031201
NONE
5 OF 5

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 268	1/13/80	[illegible]
C	REV PER ECO 454	2/3/82	[illegible]
D	REV. PER ECO 539 LR	7-1-82	[illegible]
E	REV. PER ECO 631 LR	7-1-82	[illegible]
F	REV PER ECO 916 MR	10-18-82	[illegible]



R47	R17
C40	C19, C22, C24, C25
LAST USED	NOT USED
REF. DESIGNATOR	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL CAPACITOR VALUES ARE IN UF.
2. ALL RESISTOR VALUES ARE IN OHMS.
3. THIS SCHEMATIC TO BE USED WITH REVISION ('S) "C" P.C.B. FABRICATION.

POWER AND GROUND LOCATER CHART

REF. DES.	TYPE	GND	+5V	-5V	#PINS
U25	74LS00	7	14		14
U6	74LS10	7	14		14
U5	74LS32	7	14		14
U16	74LS138	8	16		16
U26	74LS148	8	16		16
U27, U38	74LS151	8	16		16
U9	10164	1,16		8	16

REF. DES.	TYPE	GND	+5V	-5V	#PINS
U36	74LS244	10	20		20
U32, U33	74LS257	8	16		16
U34	74LS367	8	16		16
U37	74LS374	10	20		20
U18	LC02021008	7,14	–	–	14
U28	AM6080	10	20	17	20
RP1, RP3, RP4, RP5, RP6, RP7, RP8	470Ω RP			1	10

REF. DES.	TYPE	GND	+5V	-5V	#PINS
U39	AM687	3,14	11	6	16
U7	7226B	12	25		40
U2	10103	1,16		8	16
U3	10104	1,16		8	16
U31	10113	1,16		8	16
U10	10116	1,16		8	16
U19	10117	1,16		8	16

REF. DES.	TYPE	GND	+5V	-5V	#PINS
RP2	1K RP		1		10
U29	LM747		9	4	14
U4	10124	16	9	8	16
U17, U20, U21, U22, U23, U35	10125	16	9	8	16
U1, U15	10135	1,16		8	16
U8	10138	1,16		8	16
U11, U12, U13, U14	10141	1,16		8	16
U24	10161	1,16		8	16
U30	10176	1,16		8	16

NDS NO. 127-0099-001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES

MAT'L N/A

FINISH N/A

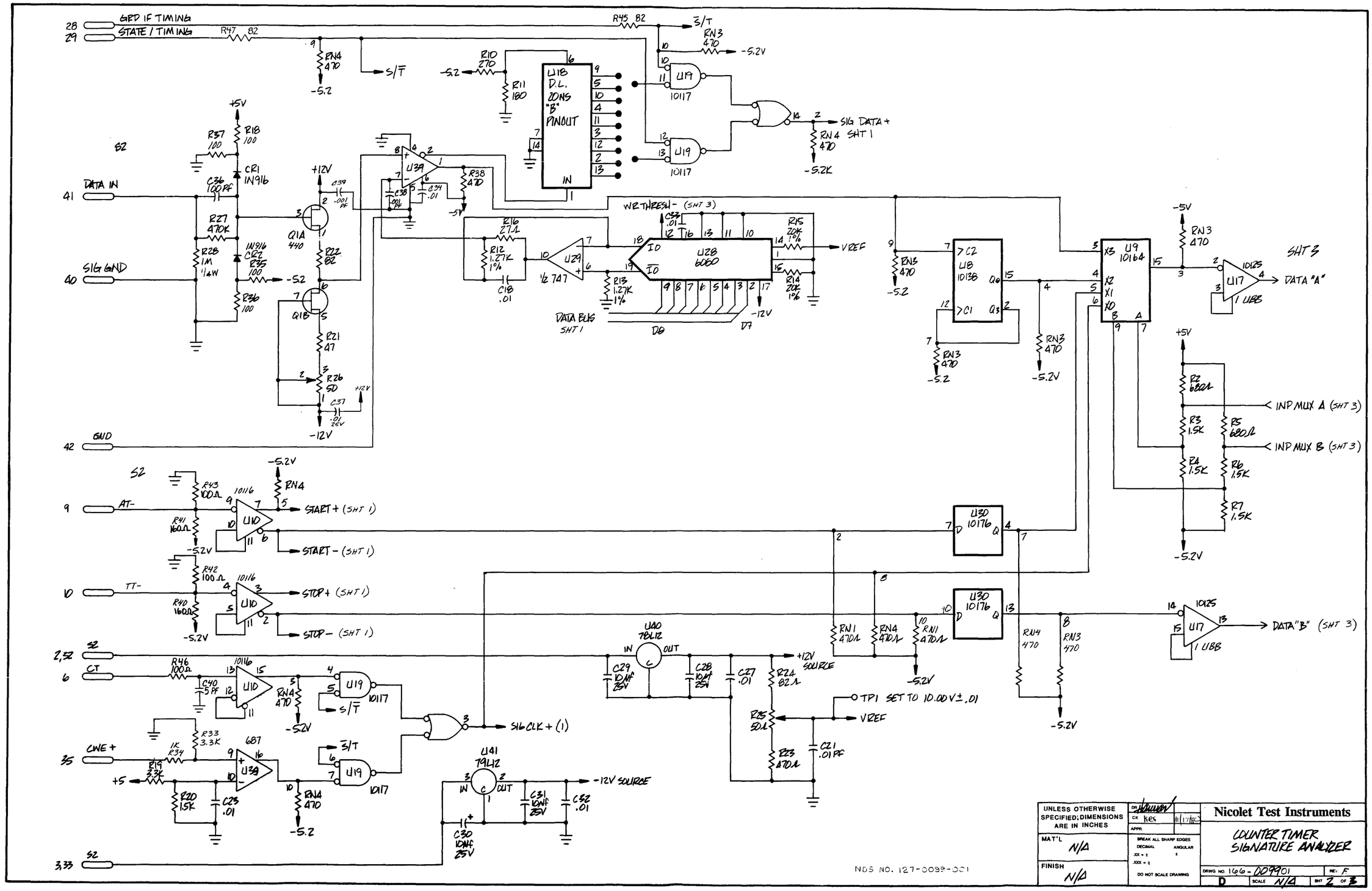
DR [illegible] 11-2-80
CK KRP 1/17/80
APPR.

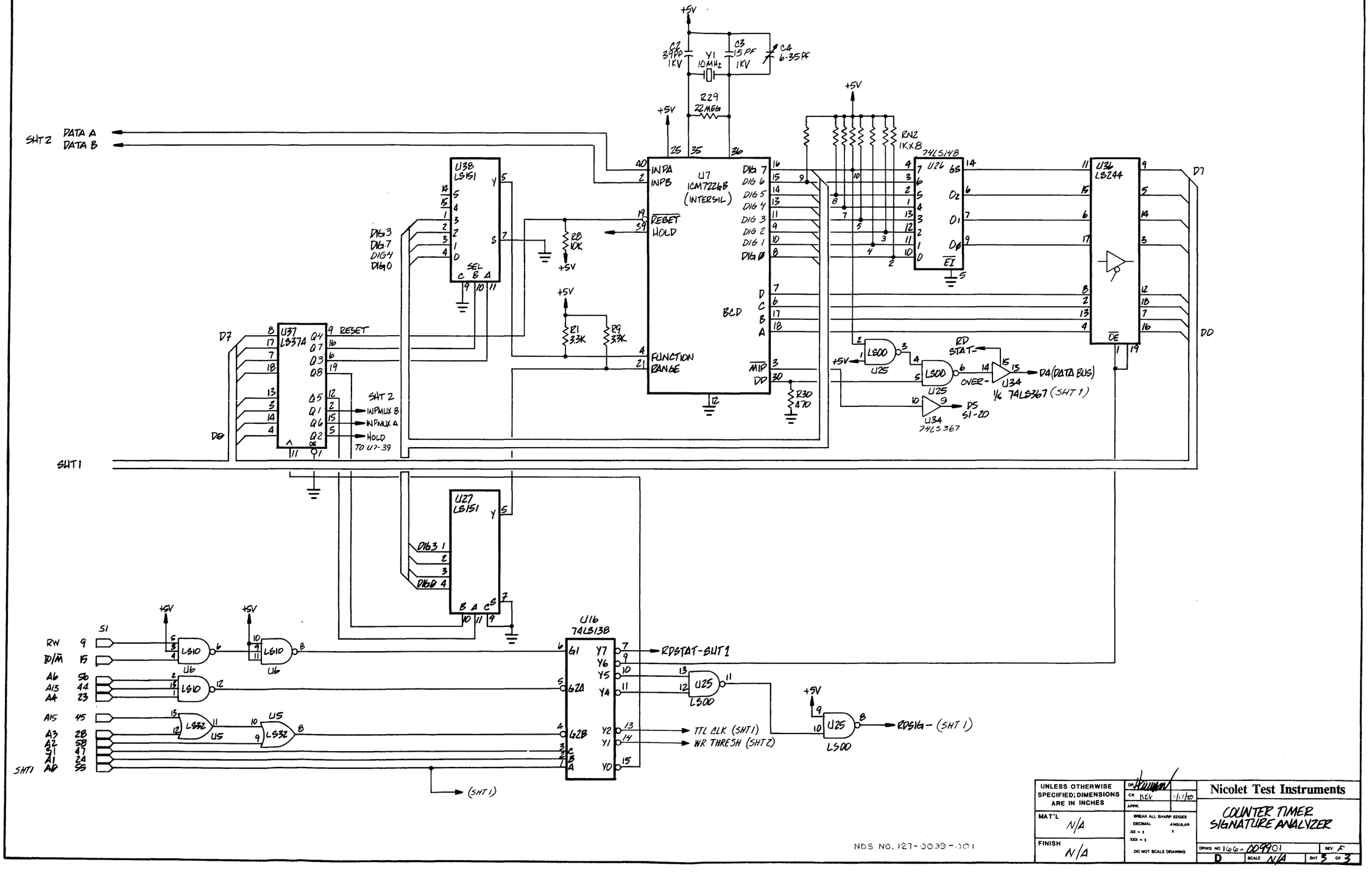
BREAK ALL SHARP EDGES
DECIMAL ±
ANGULAR ±
XX = ±
XXX = ±
DO NOT SCALE DRAWING

Nicolet Test Instruments

COUNTER TIMER SIGNATURE ANALYZER

DRWG NO 166-009901 REV F
D SCALE N/A SHT 1 OF 3

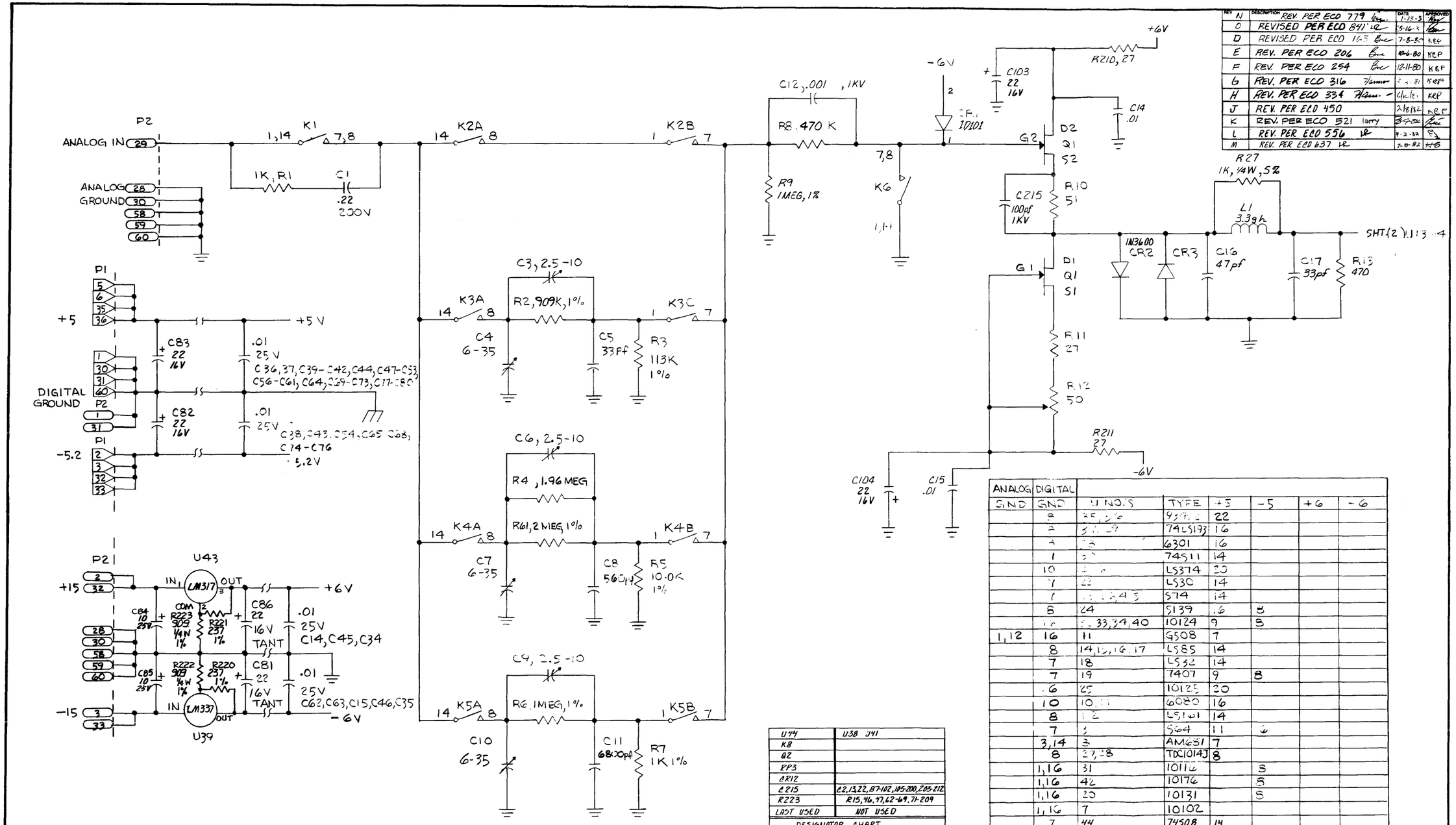

GRD IF TIMING
STATE / TIMING
DATA IN
SIG GND
GND
AT-
TT-
CT
CWE +
SIG DATA + SHT 1
WR THRESH - (SHT 3)
VREF
DATA BUS SHT 1
SHT 3
DATA "A"
INP MUX A (SHT 3)
INP MUX B (SHT 3)
START + (SHT 1)
START - (SHT 1)
STOP + (SHT 1)
STOP - (SHT 1)
DATA "B" (SHT 3)
+12V SOURCE
TP1 SET TO 10.00V ± .01
SIG CLK + (1)
-12V SOURCE
NDS NO. 127-0099-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
Nicolet Test Instruments
COUNTER TIMER SIGNATURE ANALYZER
DRWG NO. 166-009901
REV F
SCALE N/A
SHT 2 OF 3



NDS NO. 127-0039-001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR	Nicolet Test Instruments
	CK KEV 1/17/80	COUNTER TIMER SIGNATURE ANALYZER
	APPR.	
MAT'L N/A	BREAK ALL SHARP EDGES DECIMAL XX = ± XXX = ± ANGULAR ±	DRWG NO 1166-009901 REV F
FINISH N/A	DO NOT SCALE DRAWING	D SCALE N/A SHT 3 OF 3

REV	DESCRIPTION	DATE	APPROVED
N	REV. PER ECO 779	1-13-83	
O	REVISED PER ECO 841	5-16-83	
D	REVISED PER ECO 165	7-8-80	KRP
E	REV. PER ECO 206	10-6-80	KRP
F	REV. PER ECO 254	12-11-80	KRP
G	REV. PER ECO 316	3-4-81	KRP
H	REV. PER ECO 334	4-6-81	KRP
J	REV. PER ECO 450	2/8/82	KRP
K	REV. PER ECO 521	8-5-82	
L	REV. PER ECO 556	9-2-82	
M	REV. PER ECO 637	7-8-82	



U44	U38 J41
K8	
Q2	
EP3	
ARIZ	
C215	C2, 13, 22, 87-102, 185-200, 205-212
R223	R15, 46, 47, 62-69, 71-209
LAST USED	NOT USED
DESIGNATOR CHART	

ANALOG GND	DIGITAL GND	U NO.'S	TYPE	+5	-5	+6	-6
	9	25,26	9334	22			
	2	3,4,9	74LS193	16			
	4	5,6	6301	16			
	1	3	74S11	14			
	10	1	LS374	20			
	7	22	LS30	14			
	1	21,23,24,35	S74	14			
	8	24	S139	16	8		
	12	1,33,34,40	10124	9	8		
1,12	16	11	G508	7			
	8	14,15,16,17	LS85	14			
	7	18	LS32	14			
	7	19	7407	9	8		
	6	25	10125	20			
	10	10,11	6080	16			
	8	12	LS181	14			
	7	5	S64	11	6		
	3,14	3	AM651	7			
	8	27,28	TDC1014J	8			
	1,16	31	10116		8		
	1,16	42	10176		8		
	1,16	20	10131		8		
	1,16	7	10102				
	7	44	74S08	14			

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL CAPACITOR VALUES ARE IN UF.
2. ALL RESISTOR VALUES ARE IN OHMS.
3. THIS SCHEMATIC TO BE USED WITH REV.('S) H P.C. FAB.

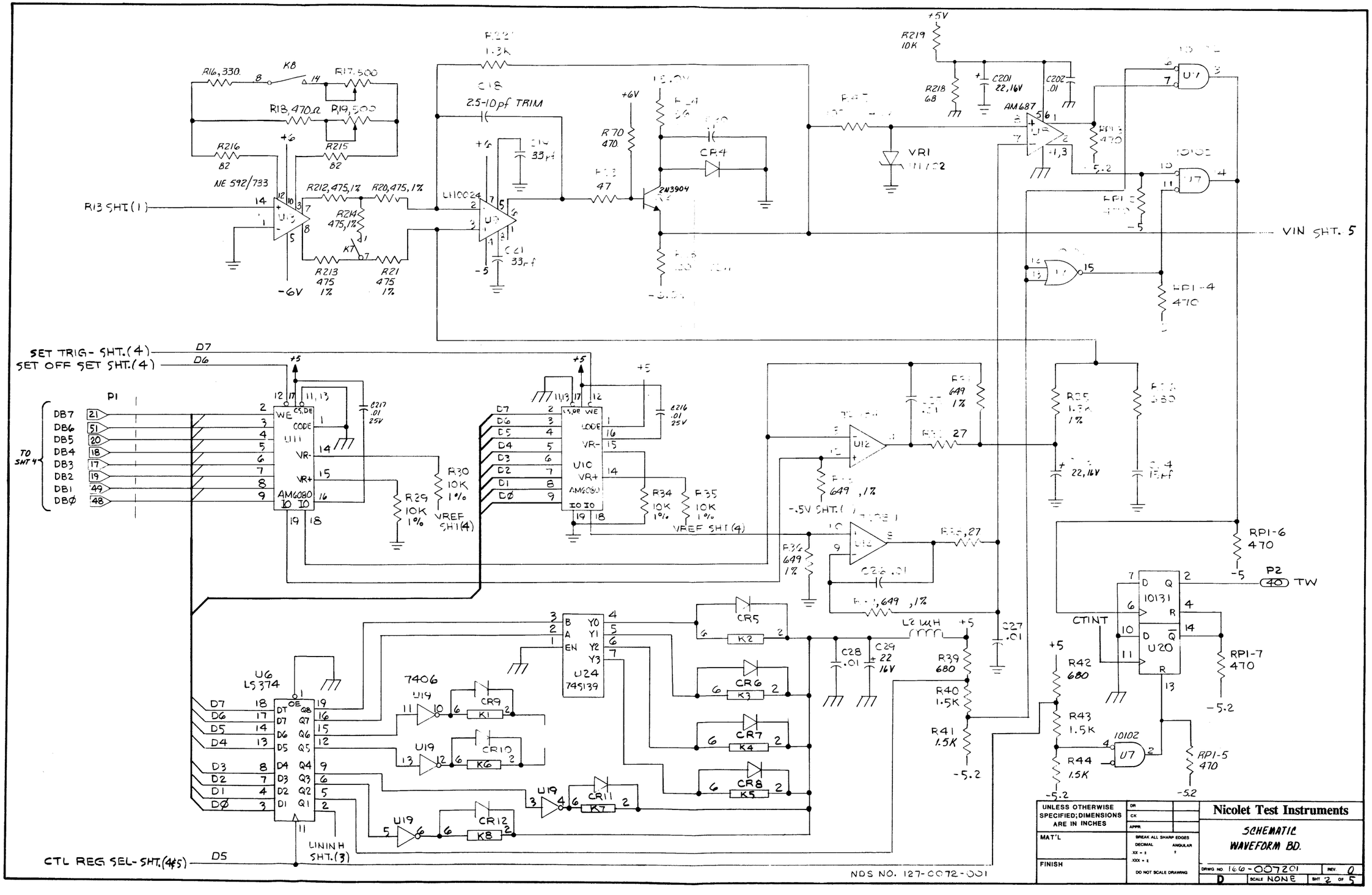
NDS NO. 127-0072-001

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DR G.S. 2-14-80
CK
APPR.
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
XX = ±
XXX = ±
DO NOT SCALE DRAWING

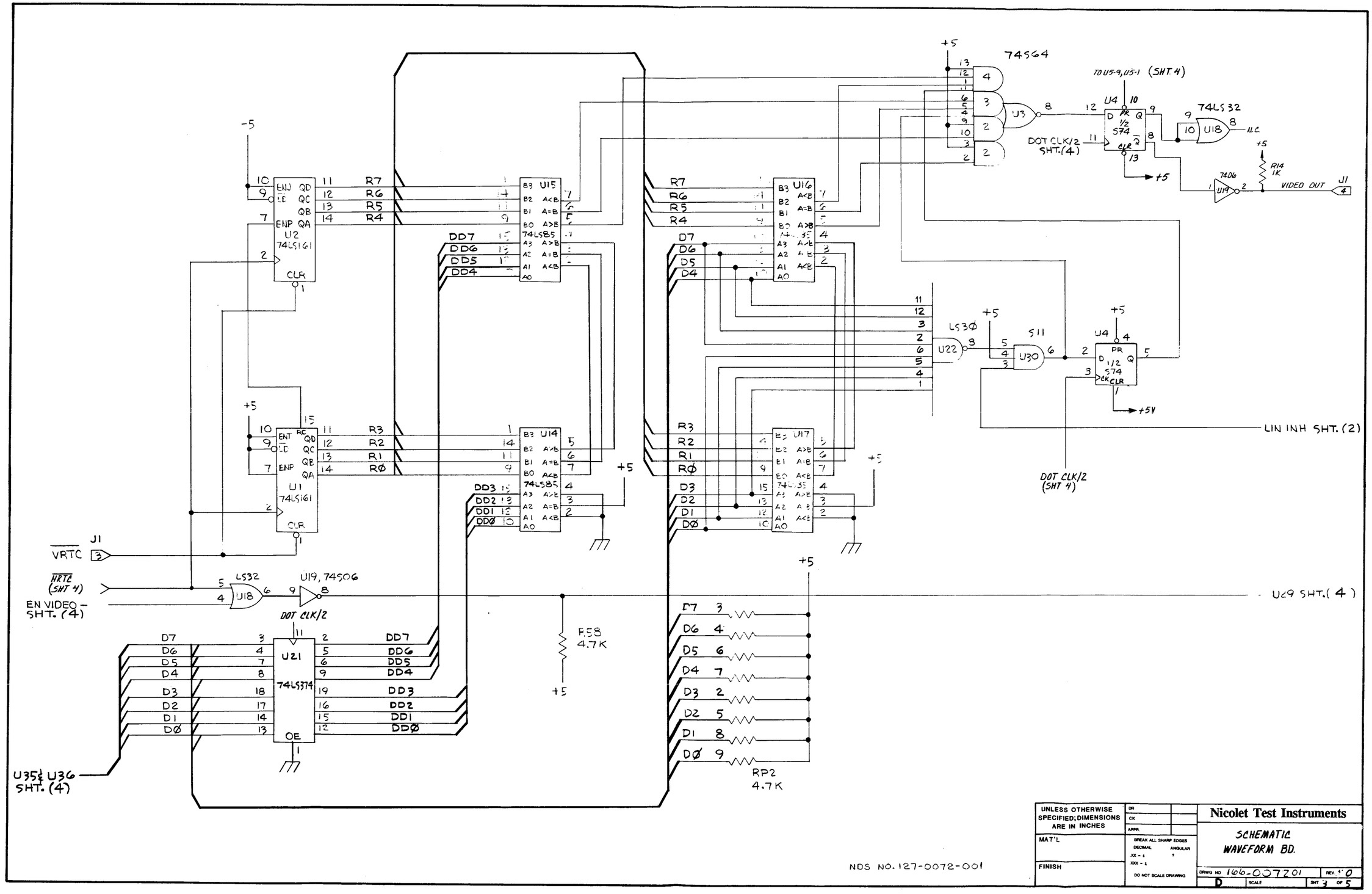
Nicolet Test Instruments

SCHEMATIC WAVEFORM BOARD

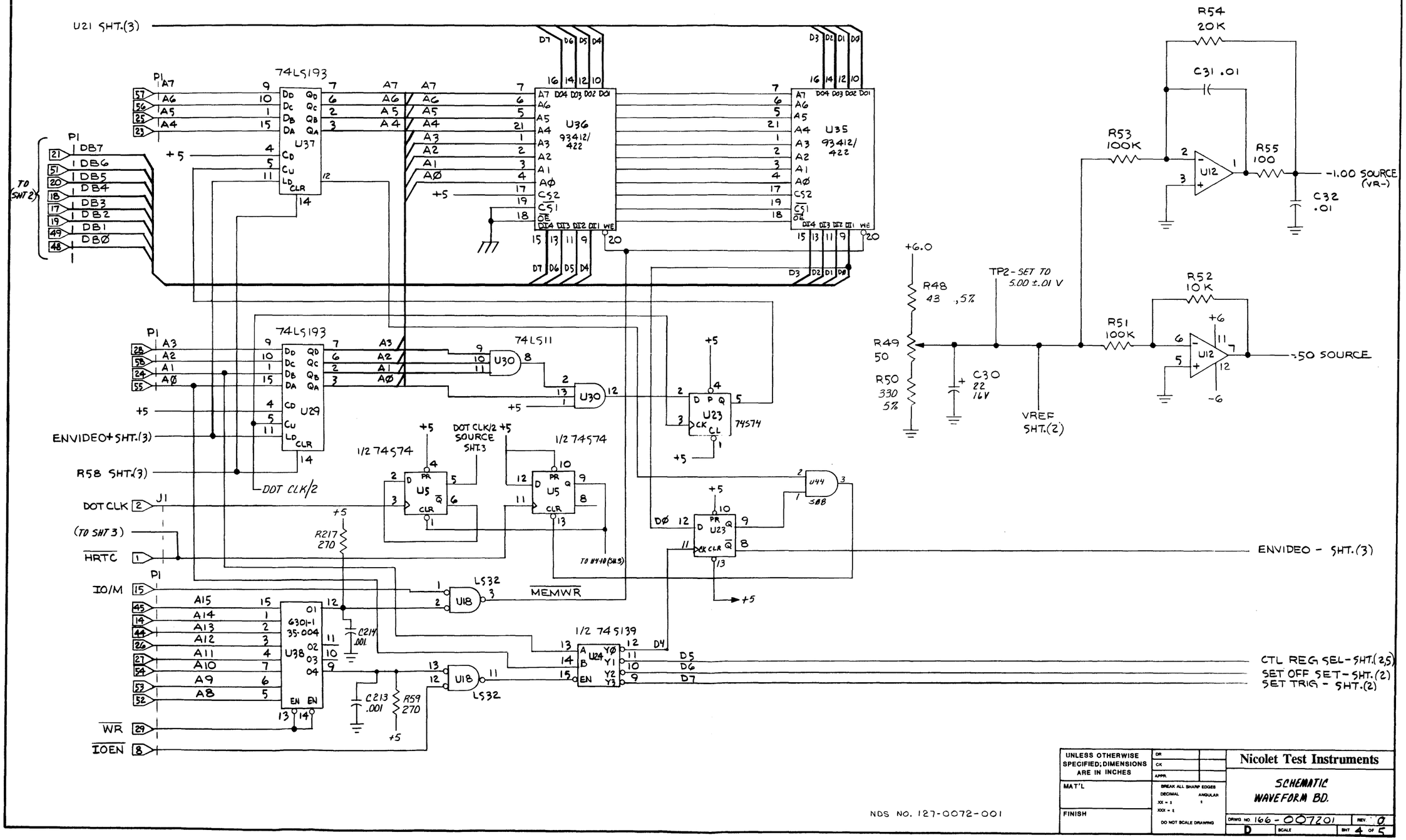
DRWG NO. 166-0072-01 REV. O
D SCALE SHT 1 OF 5

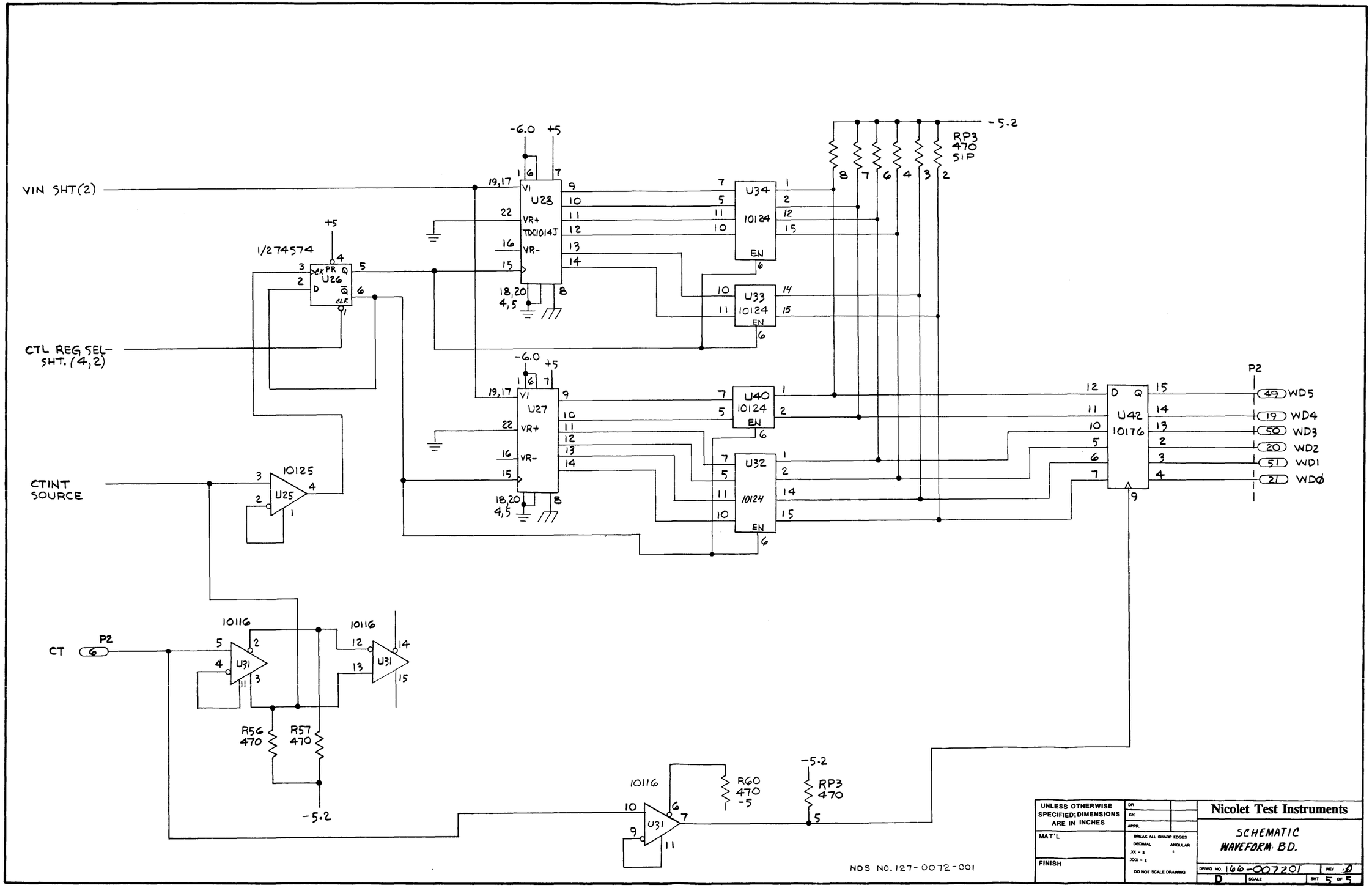


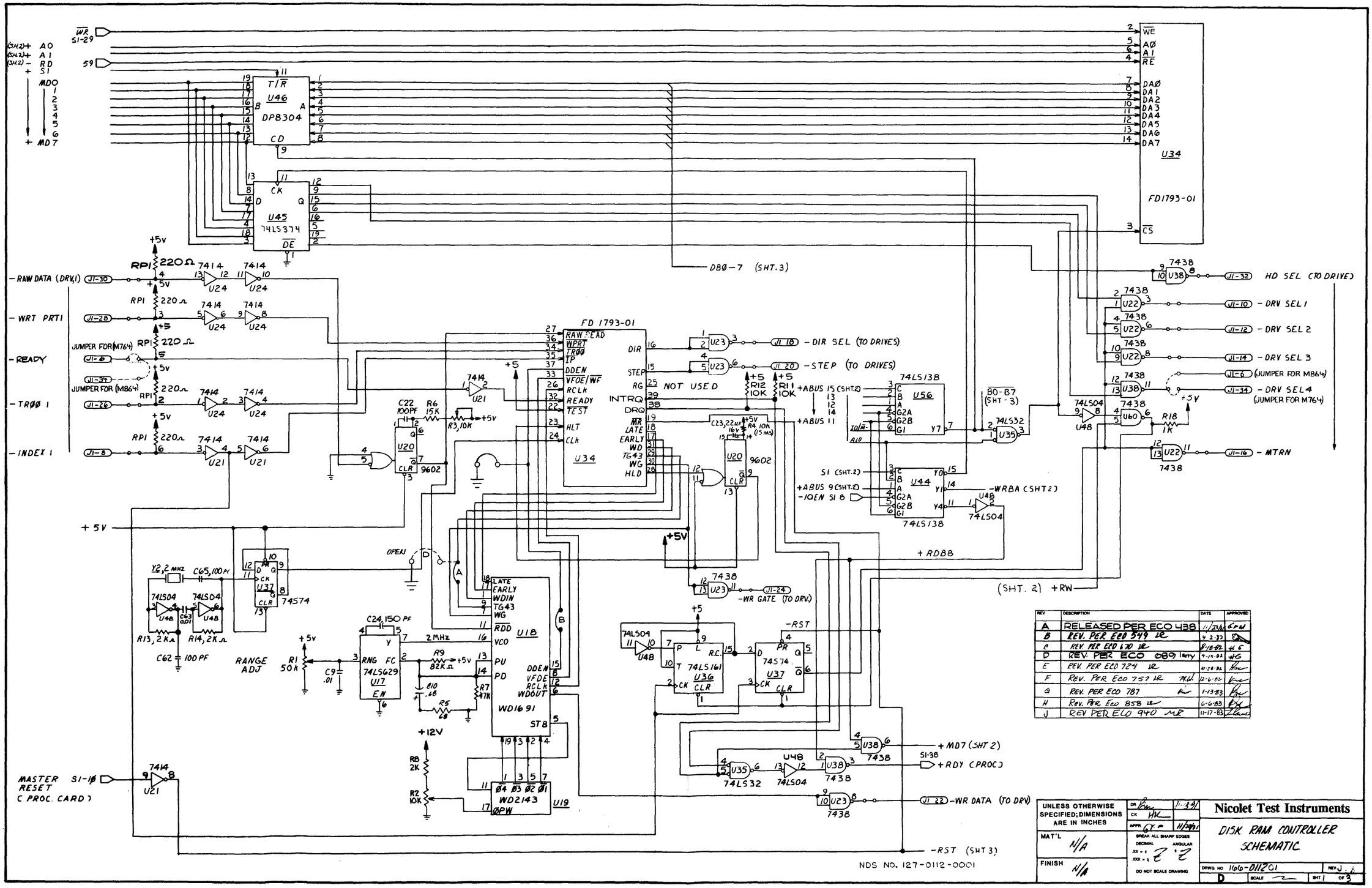
R13 SHT.(1)
VIN SHT. 5
SET TRIG- SHT.(4)
SET OFF SET SHT.(4)
CTL REG SEL- SHT.(4&5)
TO SHT 4
VREF SHT(4)
LININ H SHT.(3)
CTINT
TW
NE 592/733
LH0024
AM687
AM6080
LS374
74S139
7406
10131
10102
2N3904
NDS NO. 127-0072-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING
Nicolet Test Instruments
SCHEMATIC WAVEFORM BD.
DRWG NO 166-007201
REV 0
SCALE NONE
SHT 2 OF 5



74S64
TO U5-9, U5-1 (SHT. 4)
74LS32
DOT CLK/2 SHT. (4)
74LS161
74LS85
74LS374
LS30
S11
LS32
U19, 74S06
DOT CLK/2
VIDEO OUT
LIN INH SHT. (2)
DOT CLK/2 (SHT 4)
VRTC
HRTC (SHT 4)
EN VIDEO - SHT. (4)
U29 SHT. (4)
U35 & U36 SHT. (4)
R58 4.7K
RP2 4.7K
R14 1K
NDS NO. 127-0072-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
Nicolet Test Instruments
SCHEMATIC WAVEFORM BD.
DRWG NO 166-007201
REV. 0
SHT 3 OF 5


U21 SHT.(3)
74LS193
U37
U36
93412/422
U35
93412/422
TO (SHT 2)
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
74LS193
U29
74LS11
U30
U23
74S74
ENVIDEO+SHT.(3)
R58 SHT.(3)
DOT CLK/2
DOT CLK
(TO SHT 3)
HRTC
IO/M
WR
IOEN
1/2 74S74
U5
DOT CLK/2 SOURCE SHT.3
R217 270
TO H4-10 (SH.3)
U44
SBB
MEMWR
LS32
U18
6301-1 35-004
U38
C214 .001
C213 .001
R59 270
1/2 74S139
U24
ENVIDEO - SHT.(3)
CTL REG SEL-SHT.(2,5)
SET OFF SET-SHT.(2)
SET TRIG - SHT.(2)
R54 20K
C31 .01
R53 100K
R55 100
U12
-1.00 SOURCE (VR-)
C32 .01
+6.0
R48 43 ,5%
TP2-SET TO 5.00 ±.01 V
R49 50
R50 330 5%
C30 22 16V
VREF SHT.(2)
R52 10K
R51 100K
-.50 SOURCE
NDS NO. 127-0072-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING
Nicolet Test Instruments
SCHEMATIC WAVEFORM BD.
DRWG NO 166-007201
REV 0
D
SCALE
SHT 4 OF 5


VIN SHT(2)
CTL REG SEL-
SHT. (4,2)
CTINT
SOURCE
CT
P2
1/274574
U26
U28
TDC1014J
U27
U34
10124
U33
10124
U40
10124
U32
10124
U42
10176
U25
10125
U31
10116
RP3
470
51P
R56
470
R57
470
R60
470
-5
-6.0
+5
-5.2
WD5
WD4
WD3
WD2
WD1
WDØ
NDS NO. 127-0072-001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
DR
CK
APPR.
BREAK ALL SHARP EDGES
DECIMAL
ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
SCHEMATIC
WAVEFORM BD.
DRWG NO. 166-007201
REV D
D
SCALE
SHT 5 OF 5



REV	DESCRIPTION	DATE	APPROVED
A	RELEASED PER ECO 438	11/23/80	GPM
B	REV. PER ECO 549 LR	4-2-82	[illegible]
C	REV. PER ECO 670 LR	8-18-82	HG
D	REV. PER ECO 689 larry	9-15-82	HG
E	REV. PER ECO 724 LR	10-28-82	[illegible]
F	REV. PER ECO 757 MW	12-6-82	[illegible]
G	REV. PER ECO 787	1-13-83	[illegible]
H	REV. PER ECO 858 LR	6-6-83	[illegible]
J	REV PER ECO 940 MR	11-17-83	[illegible]

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES

MAT'L N/A

FINISH N/A

DR [illegible] 11-13-81

CK [illegible]

APPR [illegible] 11/20/81

BREAK ALL SHARP EDGES

DECIMAL XX ± ± XXX ± ±

ANGULAR ± ±

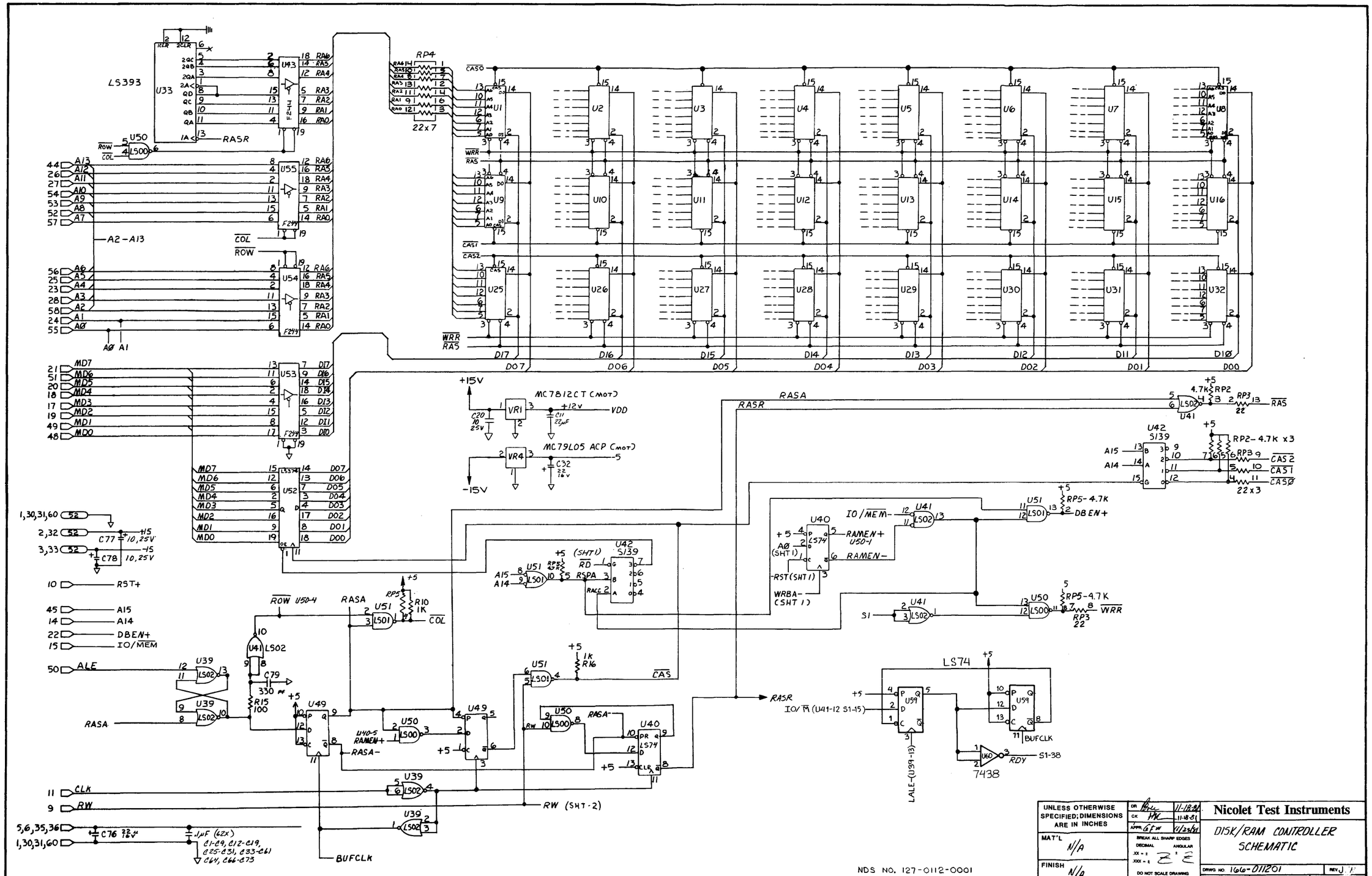
DO NOT SCALE DRAWING

Nicolet Test Instruments

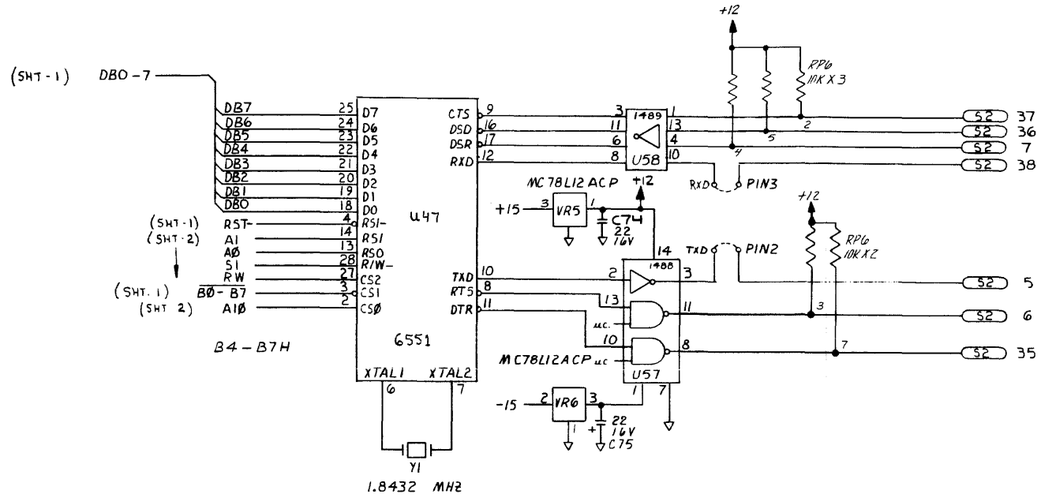
DISK RAM CONTROLLER SCHEMATIC

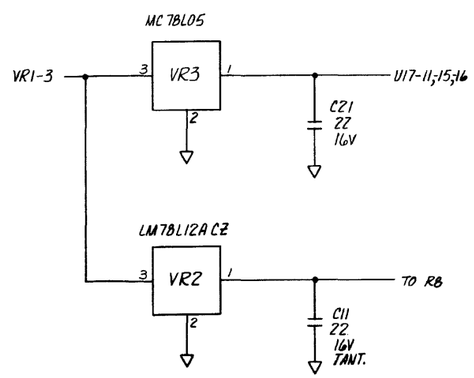
DRWG NO 166-011201 REV J

D SCALE — SHT 1 OF 3



LS393
U33
U43
F244
RASR
U50
LS00
ROW
COL
U55
U54
U53
U52
A2-A13
A0 A1
RP4
22x7
CAS0
WRR
RAS
CAS1
CAS2
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U25
U26
U27
U28
U29
U30
U31
U32
D17
D16
D15
D14
D13
D12
D11
D10
D07
D06
D05
D04
D03
D02
D01
D00
+15V
-15V
MC7812CT (MOT)
VR1
VDD
MC79L05 ACP (MOT)
VR4
RASA
RASR
U41
LS02
RP2
RP3
U42
S139
RP2-4.7K x3
CAS2
CAS1
CAS0
22x3
U51
LS01
RP5-4.7K
DBEN+
U40
LS74
RAMEN+
RAMEN-
U50-1
RST(SHT1)
WRBA-(SHT1)
U50
RP5-4.7K
WRR
RP3
22
RST+
A15
A14
DBEN+
IO/MEM
ALE
U39
U49
U40
LS74
RASA
RASA-
RAMEN+
U40-5
CAS
RASR
IO/M (U41-12 S1-15)
LALE-(U39-13)
U59
BUFCLK
U60
7438
RDY
S1-38
CLK
RW
RW (SHT-2)
BUFCLK
C76
.1µF (62X)
C1-C9, C12-C19, C25-C31, C33-C61, C64, C66-C73
NDS NO. 127-0112-0001
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
DR 11-18-81
CK 11-18-81
APPR 11/23/81
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
DISK/RAM CONTROLLER SCHEMATIC
DRWG NO. 166-011201
REV J
D
SCALE
SHT 2 OF 3





3. THIS SCHEMATIC TO BE USED WITH REVISION (S) "B" P.C.B. FABRICATION.
2. ALL RESISTOR VALUES ARE IN OHMS.
1. ALL CAPACITOR VALUES ARE IN UF.
NOTES: UNLESS OTHERWISE SPECIFIED.

TP2	
Y2	
U60	
VR6	
C79	
RP6	
R20	
LAST USED	NOT USED
REF. DESIGNATORS	

POWER AND GROUND LOCATOR CHART

REF. DESIGN.	TYPE	GND	+5V	-5V	+12V	-12V	PINS
U50	74LS00	7	14				14
U17	74LS629	8,9	15,16				16
U46	DP8304	10	20				20
U20	9602	8	16				16
U19	2143-03	9	18				18
U18	1691	10	20				20
U34	1793-1	20	21		40		40
U58	1489	7	14				14
U57	1488	7			14	1	14
U47	6551A	1	15				28
U1-U16, U25-U32	16K DRAM	16	9	1	8		16
U33	LS393	7	14				14
U53-U55, U43	F244	10	20				20
U45, U52	LS374	10	20				20
U21, U24	7414	7	14				14
U22, U23, U38, U60	7438	7	14				14
U51	74LS01	7	14				14
U39, U41	74LS02	7	14				14
U35	74LS32	7	14				14
U40, U49, U59	74LS74	7	14				14
U44, U56	74LS138	7	16				16
U42	74S139	7	16				16
U36	74LS161	7	16				16
U48	74LS04	7	14				14
U37	74S74	7	14				14

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L N/A
FINISH N/A
DR 11-18-81
CK HK
APPR [illegible] 11-23-81
BREAK ALL SHARP EDGES
DECIMAL XX = ± XXX = ± ANGULAR ±
DO NOT SCALE DRAWING

Nicolet Test Instruments
DISK RAM CONTROLLER SCHEMATIC
DRWG NO 166-011201 REV J
D SCALE SHT 3 OF 3

NDS NO. 127-0112-0001

REV	DESCRIPTION	DATE
A	ECO 124	3-4-80
B	ECO 201	9-16-80

A CHANNEL

B CHANNEL

U1 CD4011

U2 CD4520

U3 CD4002

U4 CD4011

U5 CD4520

C1 .01 μf

C2 .001 μf

R1 10KΩ

R2 47Ω

R3 47Ω

+5V

N.C.

D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 QCLK CLK

'U' NUMBERS	DEVICE	Vcc (+5V)	GND
U1, U4	CD4011	14	7
U2, U5	CD4520	16	8
U3	CD4002	14	7

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DESIGN BY		DATE 8-4-80
CHECKED BY		DATE 9-18-80
ENG		DATE 9-18-80
APPR. REL.		DATE 9-18-80
DECIMAL	XXX = ±.005 XX = ±.02	
FRACTIONAL	± 1/64	
ANGULAR	± 0°30'	
BREAK ALL SHARP EDGES		
DO NOT SCALE DRAWING		

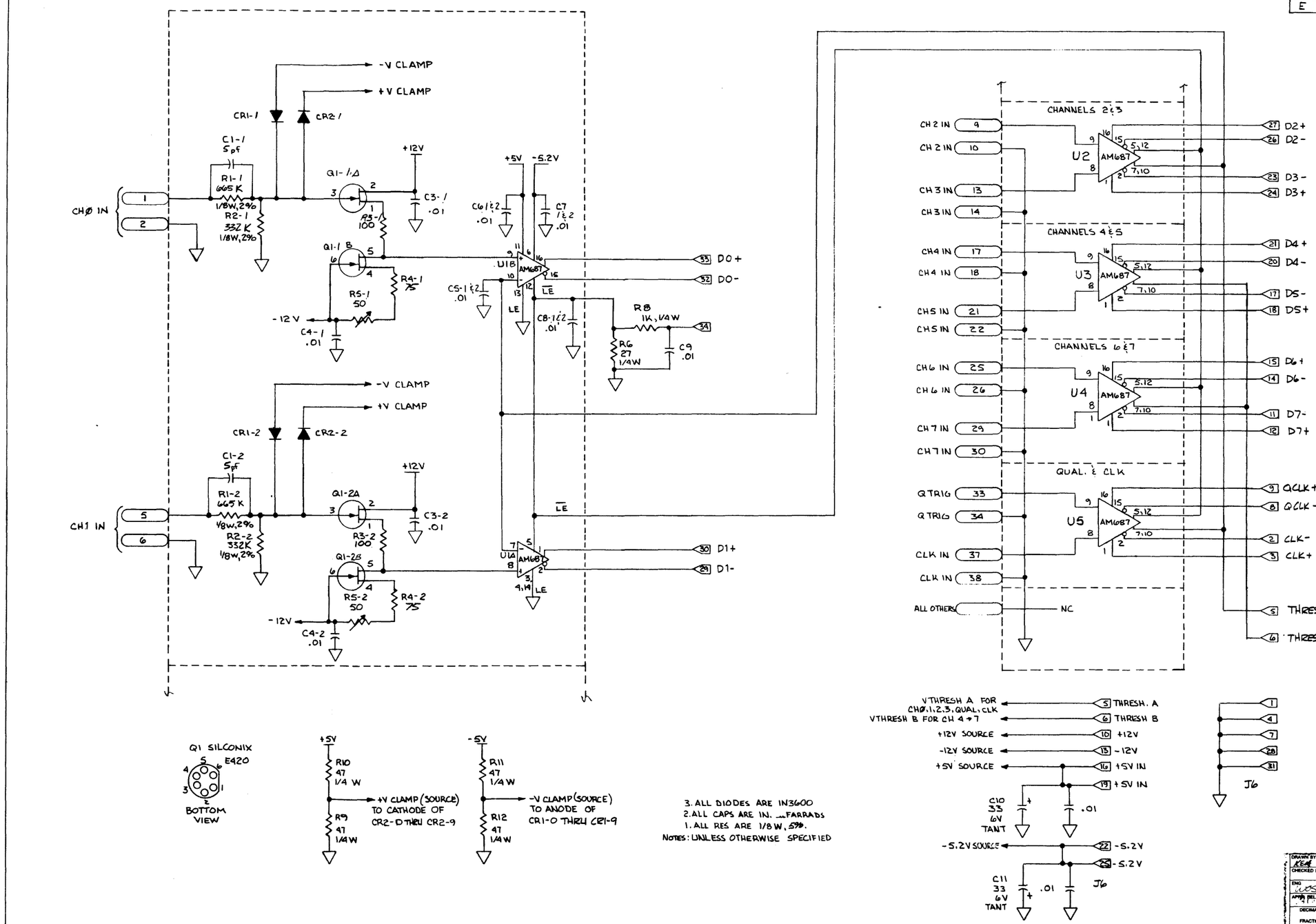
Nicolet Test Intruments

DESCRIPTION: SCHEMATIC, MODEL 540/532 TRICK CARD

DRAWING NO. 166-0046-01 B

SCALE NONE SHT 1 OF 1 REV.

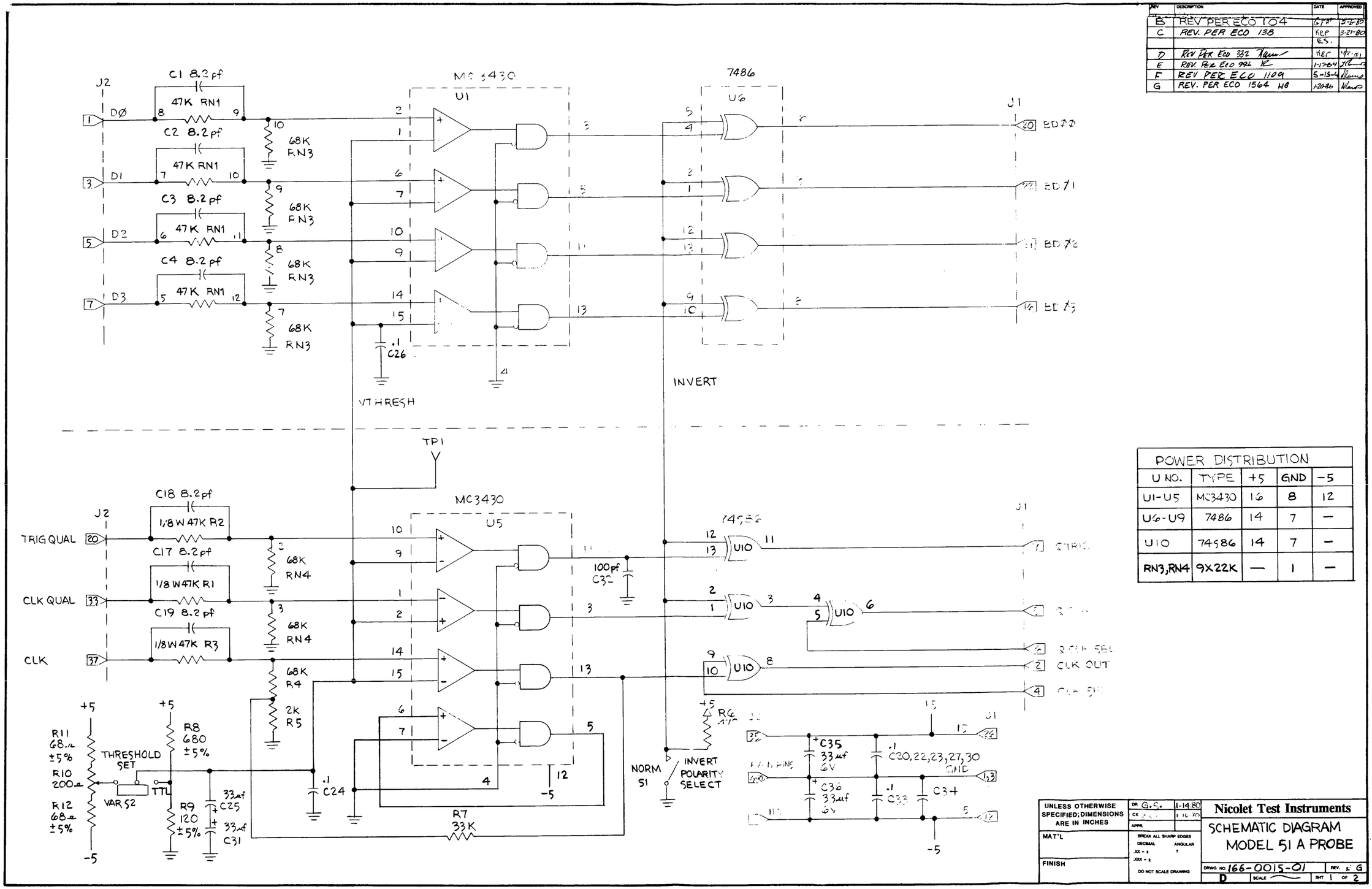
REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 179	[illegible]	[illegible]
C	REV PER ECO 197	[illegible]	[illegible]
D	REV PER ECO 318	3-19-81	KBP
E	REV PER ECO 1176 MR	7-26-81	[illegible]



3. ALL DIODES ARE IN3600
2. ALL CAPS ARE IN. μFARRADS
1. ALL RES ARE 1/8W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED

DRAWN BY KEA	DATE 8/23/79	Nicolet Test Instruments
CHECKED BY	DATE	DESCRIPTION: SCHEMATIC DIAGRAM Model 80 Probe
ENG WOS	DATE 11/15/79	
APPR. REL. [illegible]	DATE [illegible]	
DECIMAL .XXX = ±.005 .XX = ±.02 FRACTIONAL ± 1/64 ANGULAR ± 0°30'		DRAWING NO. 166-0052-01 E
BREAK ALL SHARP EDGES		SCALE SHT 1 OF 1 REV.
DO NOT SCALE DRAWING		

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 104	GFP	2-6-80
C	REV. PER ECO 138	KBP	3-21-80
		ES.	
D	REV PER ECO 332	KBP	4/2/81
E	REV. PER ECO 996	1-17-84	
F	REV PER ECO 1109	5-15-84	
G	REV. PER ECO 1564 HB	1-20-86	



POWER DISTRIBUTION				
U NO.	TYPE	+5	GND	-5
U1-U5	MC3430	16	8	12
U6-U9	7486	14	7	—
U10	74S86	14	7	—
RN3,RN4	9X22K	—	1	—

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES

MAT'L

FINISH

DR G.S. 1-14-80

CK 1-16-80

APPR.

BREAK ALL SHARP EDGES

DECIMAL .XX = ± .XXX = ±

ANGULAR ±

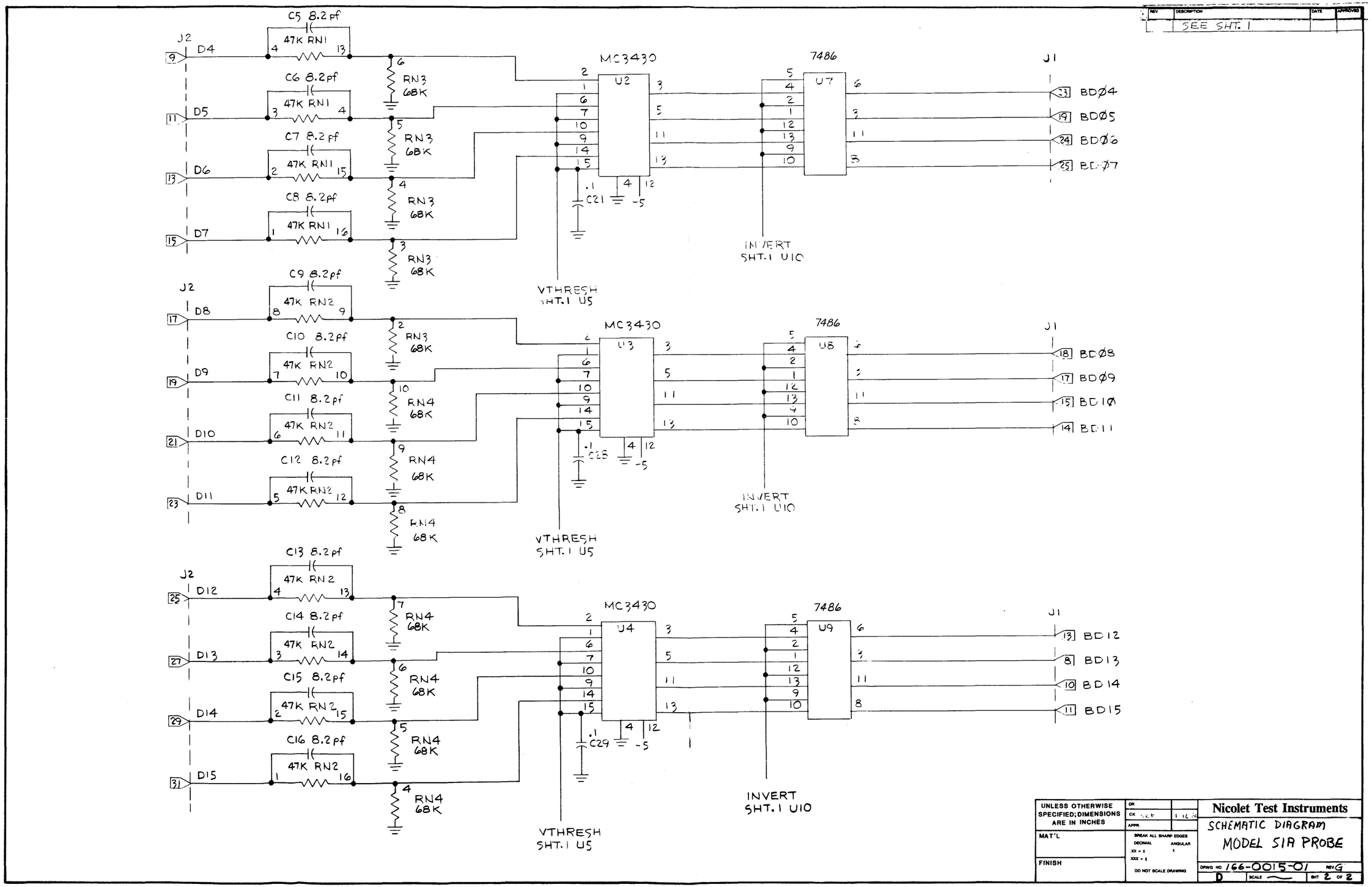
DO NOT SCALE DRAWING

Nicolet Test Instruments

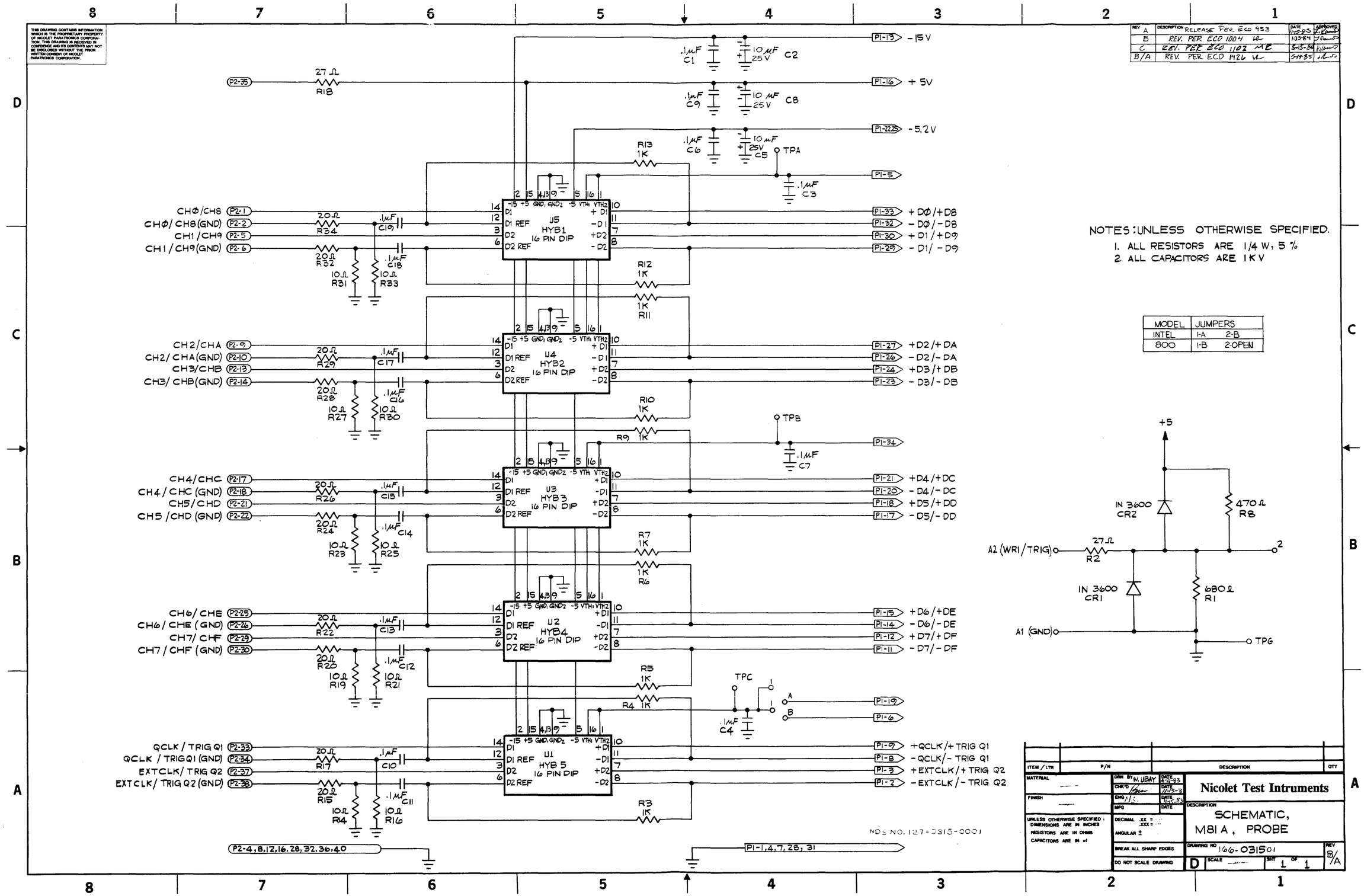
SCHEMATIC DIAGRAM
MODEL 51 A PROBE

DRWG NO. 166-0015-01 REV. G

D SCALE — SHT 1 OF 2



SEE SHT. 1
J2
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
C5 8.2pf
C6 8.2pf
C7 8.2pf
C8 8.2pf
C9 8.2pf
C10 8.2pf
C11 8.2pf
C12 8.2pf
C13 8.2pf
C14 8.2pf
C15 8.2pf
C16 8.2pf
47K RN1
47K RN2
RN3 68K
RN4 68K
MC3430
U2
U3
U4
7486
U7
U8
U9
C21
C28
C29
-5
VTHRESH SHT.1 U5
INVERT SHT.1 U10
J1
BDØ4
BDØ5
BDØ6
BDØ7
BDØ8
BDØ9
BD1Ø
BD11
BD12
BD13
BD14
BD15
UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DECIMAL
ANGULAR
DO NOT SCALE DRAWING
Nicolet Test Instruments
SCHEMATIC DIAGRAM
MODEL S1A PROBE
DRWG NO 166-0015-01
REV G
D
SCALE
SHT 2 OF 2



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REV A DESCRIPTION RELEASE PER ECO 953 DATE 1-15-83 APPROVED
B REV. PER ECO 1004 DATE 1-23-84
C REV. PER ECO 1102 DATE 5-15-84
B/A REV. PER ECO 1426 DATE 5-14-85
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1/4 W, 5 %
2. ALL CAPACITORS ARE 1 KV
MODEL JUMPERS
INTEL 1-A 2-B
800 1-B 2-OPEN
-15 V
+5V
-5.2V
TPA
TPB
TPC
TPG
U5 HYB1 16 PIN DIP
U4 HYB2 16 PIN DIP
U3 HYB3 16 PIN DIP
U2 HYB4 16 PIN DIP
U1 HYB 5 16 PIN DIP
CH0/CH8
CH0/CH8(GND)
CH1/CH9
CH1/CH9(GND)
CH2/CHA
CH2/CHA(GND)
CH3/CHB
CH3/CHB(GND)
CH4/CHC
CH4/CHC(GND)
CH5/CHD
CH5/CHD(GND)
CH6/CHE
CH6/CHE(GND)
CH7/CHF
CH7/CHF(GND)
QCLK/TRIG Q1
QCLK/TRIG Q1(GND)
EXTCLK/TRIG Q2
EXTCLK/TRIG Q2(GND)
+D0/+D8
-D0/-D8
+D1/+D9
-D1/-D9
+D2/+DA
-D2/-DA
+D3/+DB
-D3/-DB
+D4/+DC
-D4/-DC
+D5/+DD
-D5/-DD
+D6/+DE
-D6/-DE
+D7/+DF
-D7/-DF
+QCLK/+TRIG Q1
-QCLK/-TRIG Q1
+EXTCLK/+TRIG Q2
-EXTCLK/-TRIG Q2
A2 (WR1/TRIG)
A1 (GND)
IN 3600 CR2
IN 3600 CR1
470Ω R8
680Ω R1
27Ω R2
NDS NO. 127-0315-0001
P2-4,8,12,16,28,32,36,40
P1-1,4,7,28,31
Nicolet Test Intruments
SCHEMATIC, M81A, PROBE
DRAWING NO 166-031501
REV B/A
SHT 1 OF 1

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