AN ABSTRACT OF THE THESIS OF

FARHAD AGHDASI for the degree of MASTER OF SCIENCE

in Electrical and Computer Engineering presented on April 29, 1976

Title: The Design of an Interface Between IEEE Standard Bus and Unibus-CP1100/GPIB Interface

Abstract approved: Redacted for privacy

Donald L. Amort

CP1100/GPIB Interface is an interface between the "General Purpose Interface Bus", which is an implementation of the Universal Bus described in IEEE Standard 488-1975, and Unibus. This interface enables TEKTRONIX CP1100 series controlers to operate GPIB-compatible instruments connected to the General Purpose Interface Bus. The designer can now incorporate into a GPIB system the control and data processing capabilities of Tektronix controlers and software. The interface is also compatible with Digital Equipment Corporation (DEC) PDP-11 minicomputers.

The Design of an Interface between IEEE Standard Bus and Unibus-CP1100/GPIB Interface

by

Farhad Aghdasi

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

June 1976

APPROVED:

Redacted for privacy

Associate Professor of Electrical and Computer Engineering

Redacted for privacy

Head of Department of Electrical and Computer Engineering

Redacted for privacy

Dean of Graduate School

Date thesis is presented April 29, 1976

Typed by Brenda Johnson for Farhad Aghdasi

TABLE OF CONTENTS

	Page
INTRODUCTION	1
DEVICE REGISTERS	4
Listener Status Register	6
Listener Data Buffer	7
Talker Status Register	7
Talker Data Buffer	10
GPIB Status Register	11
Parallel Poll Register	12
GPIB Data Register	13
INTERRUPT VECTORS	14
CIRCUIT DESCRIPTION	16
Address Decoding	16
Registers	17
Multiplexers for Registers	19
Interrupt Circuitry	20
Handshake Circuitry	23
Error Messages	26
Driver/Receivers	28
CABLE AND EDGE CONNECTORS	29
GPIB Pin Assignment	29
CP1100 Pin Assignment	30
CP1100/GPIB INTERFACE ELECTRICAL SPECIFICATION	32
BIBLIOGRAPHY	34
APPENDIX	35
Schematic	35
Cross Reference Table	36

THE DESIGN OF AN INTERFACE BETWEEN IEEE STANDARD BUS AND UNIBUS- CP1100/GPIB INTERFACE

INTRODUCTION

The CP1100/GPIB Interface enables TEKTRONIX CP1100-Series Controllers to operate GPIB-compatible instruments connected to the General Purpose Interface Bus. The designer can now incorporate into a GPIB system the control and data processing capabilities of Tektronix controllers and software.

The interface is also compatible with Digital Equipment Corporation (DEC) PDP-11 minicomputers.

The GPIB. The General Purpose Interface Bus in an implementation of the universal bus described in IEEE Standard 488-1975. Its purpose is to provide an effective communications link over which messages can be carried between instruments in a clear and orderly manner. Instruments designed to operate according to the standard can be connected directly to the bus and operated by the controller using this interface.

The bus uses eight data and eight control lines. Information is transferred asynchronously bit-parallel, byte-serial. This allows instruments with different cycle times to operate together using the handshakes specified in the standard.

GPIB System. A GPIB system includes a controller, such as

a Tektronix CP1100-Series Controller, a talker, such as a counter or digital multimeter, and a listener, such as a line printer or signal generator. More than one function can be combined in a single instrument. For example, a Tektronix controller using this interface can function as a controller, listener, and talker.

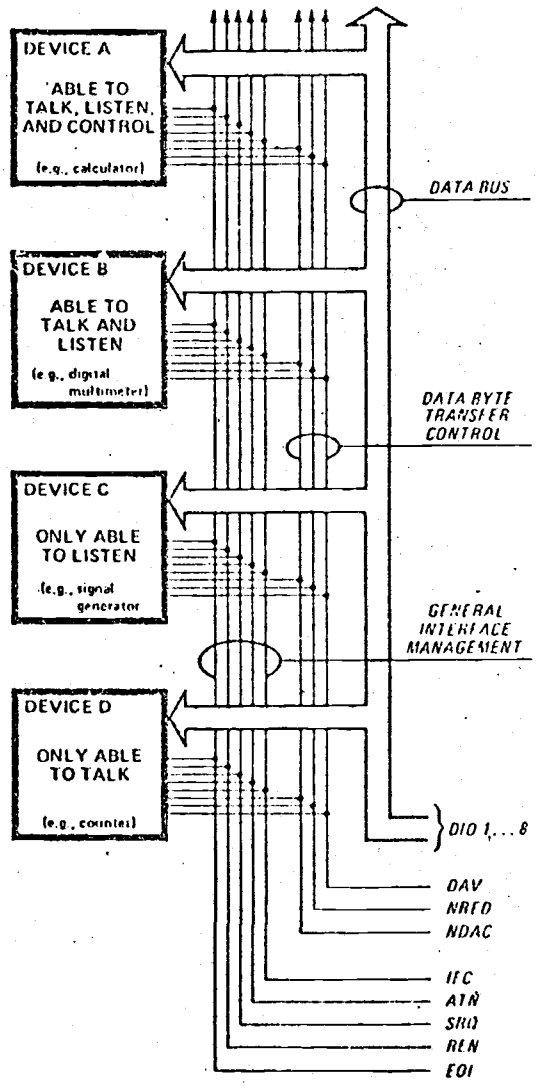


Figure 1. A typical GPIB System showing bus organization.

GPIB Messages. Messages on the bus are either interface messages or device dependent messages. Interface messages are used to manage the interface functions of the instruments. They designate talkers and listeners, for example. Device dependent messages, by contrast, are not used by the interfaces to change their state or configuration, but contain the data being transferred between device functions of the instruments.

Interface Capabilities. Using this interface, the CP1100 Controller is capable of the combined allowable subsets to the controller interface function specified in the IEEE Standard. The controller can send device addresses, universal and addressed commands, and conduct parallel polls. It can act as system controller, controller-in-charge, or relinquish control to another device. It has the full capabilities of the source and acceptor handshakes and can be a talker and listener.

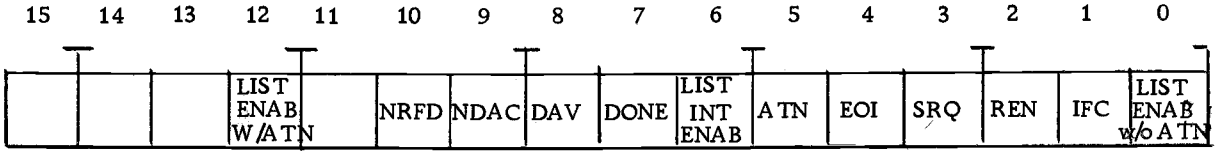
The interface uses a special one-byte register to increase through-put on the GPIB when it is acting as a listener. There are six other addressable registers and eight interrupt vectors for use in programming the controller's interaction with the other devices on the bus.

DEVICE REGISTERS

There are seven registers used in communicating with the CP1100/GPIB Interface. (See Figure 2.1.) The bottom four bits of the CP1100 address specify the register address. This address must be even. The only byte operations allowed are reads of the even byte. The high bits of the register addresses are strappable to the range 764000_8 to 767760_8. All bits are read/write unless otherwise indicated.

2.1 Listener Status Register

Listener Status Register (LSR) AAAAA0



Bit 12: Listener Enable w/ATN

Set: By writing a 1 into it.

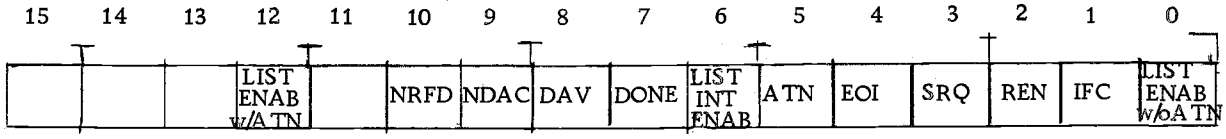
Cleared: By writing a 0 into it or CP1100 RESET.

Function: If this bit is a 1 and ATN is asserted on the GPIB, the interface will handshake for all data and latch it in the Listener Data Buffer. Setting this bit will clear Done if ATN is set.

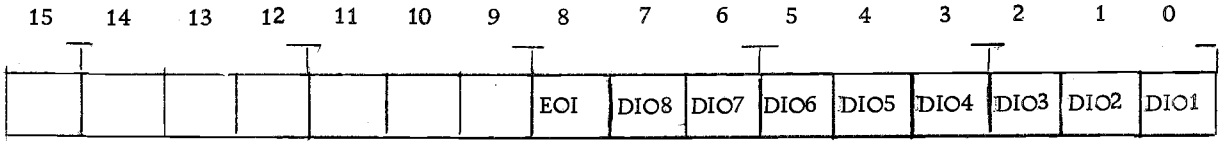
Bit 7: Done (Read only).

Set: When a character is available in the input data buffer.

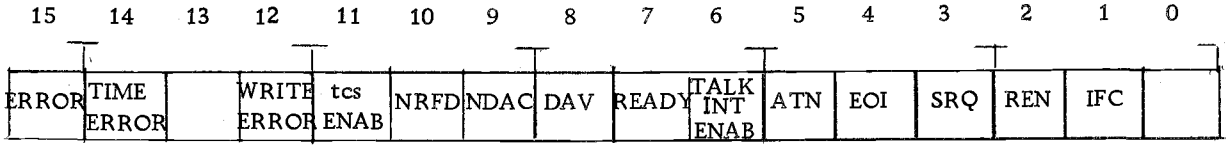
(2.1) Listener Status Register (LSR) AAAAA0



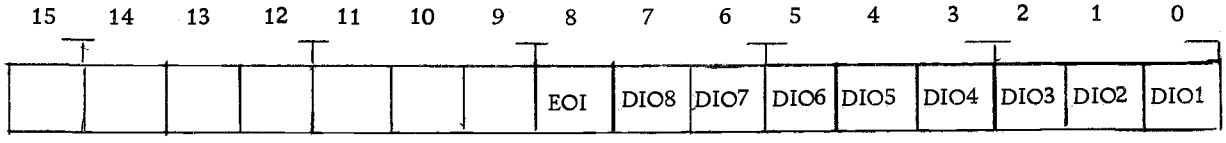
(2.2) Listener Data Buffer (LDB) AAAAA2



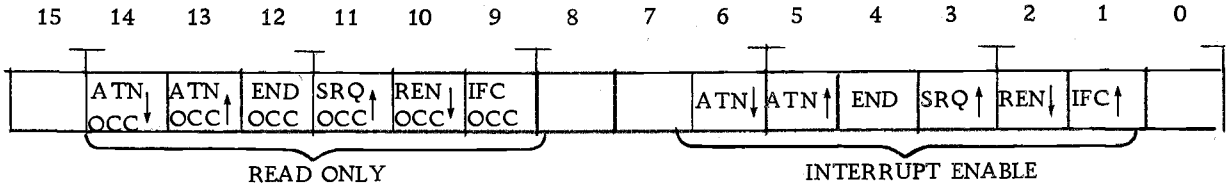
(2.3) Talker Status Register (TSR) AAAAA4



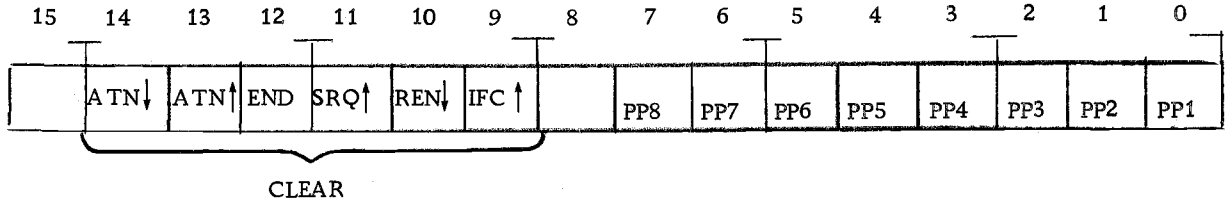
(2.4) Talker Data Buffer (TDB) AAAAA6



(2.5) GPIB Status Reigster (GSR) AAAA10



(2.6) Parallel Poll Register (PPR) AAAA12



(2.7) GPIB Data Register (GDR) AAAA14

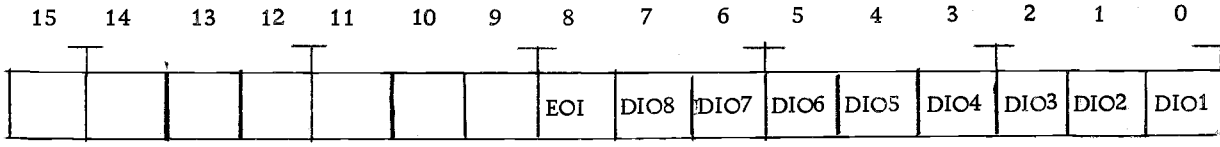


Figure 2-1. CP1100/GPIB Interface Registers.

Cleared: By any reference to the Listener Data Buffer, CP1100 RESET, or by setting LIST ENAB w/o ATN and ATN is not asserted, or by setting LIST ENAB w/ATN while ATN is asserted.

Function: Used to indicate data, which was read from the GPIB, is available in the LDB.

Bit 6: Listener interrupt enable.

Set: By writing a one into it.

Cleared: By writing a zero into it or CP1100 RESET.

Function: If set, then LSR_7 = 1 (Done) causes an interrupt.

Bit 0: Listener Enable w/o ATN

Set: By writing a one into it.

Cleared: By writing a zero into it or CP1100 RESET.

Function: When this bit is set, the interface performs the listener handshake and places each data byte received in the LDB. Setting this bit clears DONE (LSR_7) if ATN is not set.

Bit 10 NRFD

Bit 9 NDAC

Bit 8 DAV

Bit 5 ATN

Bit 4 EOI

Bit 3 SRQ

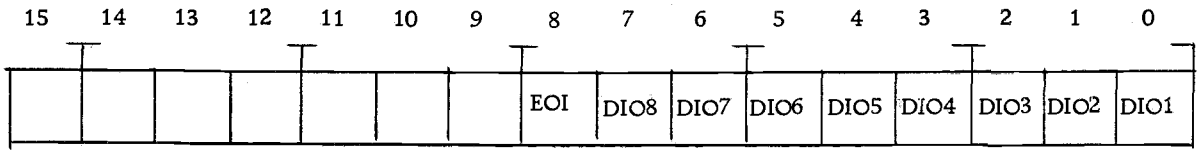
These bits are read only. They are current value of the corresponding lines on the GPIB. A 1 indicates the corresponding

Bit 2 REN line is asserted on the GPIB.

Bit 1 IFC

2.2 Listener Data Buffer

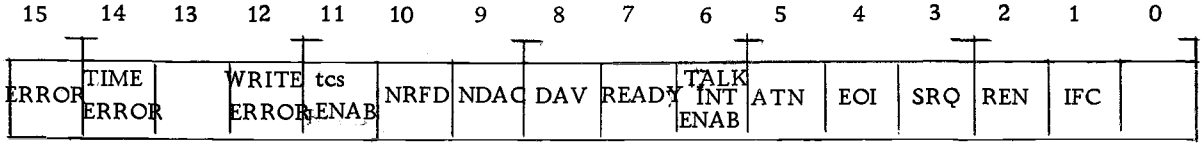
Listener Data Buffer (LDB) AAAAA2



The Listener Data Buffer is a read only register. Reading the LDB obtains the value of the corresponding lines of the GPIB for the last data byte read by the acceptor handshake in the interface from the GPIB. LSR_7 is set when a new byte has been latched in the LDB. LSR_7 is cleared by any reference to the LDB.

2.3 Talker Status Register

Talker Status Register (TSR) AAAAA4



Bit 15: Error (Read only).

Set: Whenever WRITE ERROR and TIME ERROR are set.

Cleared: Whenever WRITE ERROR and TIME ERROR

are zero or CP1100 RESET.

Bit 14: Timing Error (Read only).

Set: 1) By attempting to write into TDB when we are already busy outputting a byte on the GPIB, or when attempting to write to the TDB when ATN on GPIB is set and the ATN flip-flop (TSR_5) is not set. The output operation is not performed.

2) If ATN transitions from unasserted to asserted on the GPIB while a handshake operation is in progress. The output operation is terminated.

Cleared: By writing to TDB or RESET.

Function: If this bit is set, it indicates a timing problem in the output of a byte.

Bit 12: Write Error (Read only).

Set: IF NRFD and DNAC are sensed unasserted at the start of a transfer (write to TDB) or if TSR_{14} is set. The output operation is not performed.

Cleared: By a write to TDB (the set has precedence over the clear) or CP1100 RESET

Bit 11: tcs Enable

Set: By writing a one into it.

Cleared: By writing a 0 into it or CP1100 RESET or whenever TSR_5 (ATN) = 1.

Function: When this bit is set, TSR_5 (ATN) will be set when the acceptor handshake function of the interface is in the Acceptor Not Ready State (ANRS). This is determined by finding DAV unasserted, NRFD and NDAC asseted on the GPIB.

Bit 7: Read (Read only).

Set: When the interface does not contain a byte in the GPIB buffer.

Note: A RESET will put the source handshake in the idle state and ready will be set.

Cleared: When the GPIB output buffer is loaded with new data.

Bit 6: Talker interrupt enable.

Set: By writing a one into it.

Cleared: By writing a zero into it or RESET.

Function: When it is a one, it allows either Error = 1, or ready = 1 to cause an interrupt.

Bit 1: IFC

Set: Writing a one into it or by CP1100 RESET.

Cleared: CP1100 RESET or clears itself (one-shot).

Function: Causes IFC to be asserted on the GPIB for 150 us. This bit is read/write so while IFC is being asserted, the value read from the register in

this bit position will be a one.

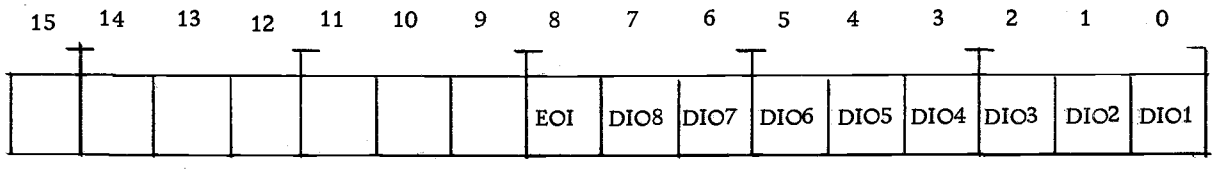
Bit 10 NRFD
Bit 9 NDAC
Bit 8 DAV
Bit 5 ATN
Bit 4 EOI
Bit 3 SRQ
Bit 2 REN
Bit 1 IFC

These are latches in the interface. They are set by writing a 1 into them. They are cleared by writing a 0 into them or by a RESET. Reading the TSR reads the status of these latches in the corresponding bit positions. The outputs of the latches drive the GPIB in a corresponding manner. (If the output of the latch is a one, the line is asserted.) The one exception is that Bit 5 (ATN) is also set if TSR_{11} (tcs) is set and the handshake is in the ANRS state.

Note: normally, the interface will not perform the acceptor handshake if ATN is asserted on the GPIB. However, if the ATN latch TSR is set, it is not an error condition to do so with attention set.

2.4 Talker Data Buffer

Talker Data Buffer (TDB) AAAAA6

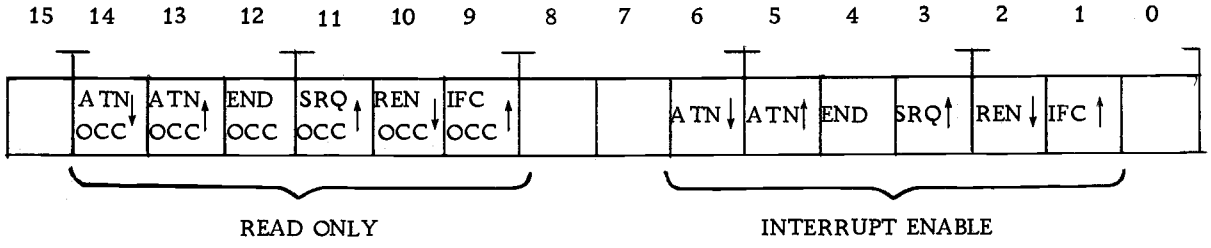


The bit layout of the TDB is the same as the LDB. The only difference is that the TDB is a write only register. (Reading it returns all

zeros.) A write to the TDB causes the data to be written to the GPIB bus.

2.5 GPIB Status Register

GPIB Status Register (GSR) AAAA10



The bits in the GSR come in pairs. There are interrupt enable bits which are set and cleared by writing into the register. They are also reset by a RESET on the CP1100 bus. The condition occurred bits are also cleared by writing into the PPR register and they are set when the specified condition occurs. Each of the bits controls an interrupt. The interrupt occurs if the enable bit is 1 and the condition occurred bit is 1. Once an interrupt has occurred for a given condition, another will not occur until one of the two related bits have been reset to zero and set to 1 again. The vector addresses for the interrupts are specified later. The conditions for setting of the occurred bits automatically are:

Bit 9: IFC↑ This bit is set whenever IFC goes from unasserted to asserted on the GPIB.

Bit 10: REN↓ This bit is set when REN goes from asserted to unasserted on the GPIB.

Bit 11: SRQ↑ This bit is set whenever SRQ transitions from unasserted to asserted on the GPIB.

Bit 12: END This bit is set when E01 is asserted and DAV goes from asserted to unasserted on the GPIB. This is essentially the end of message interrupt.

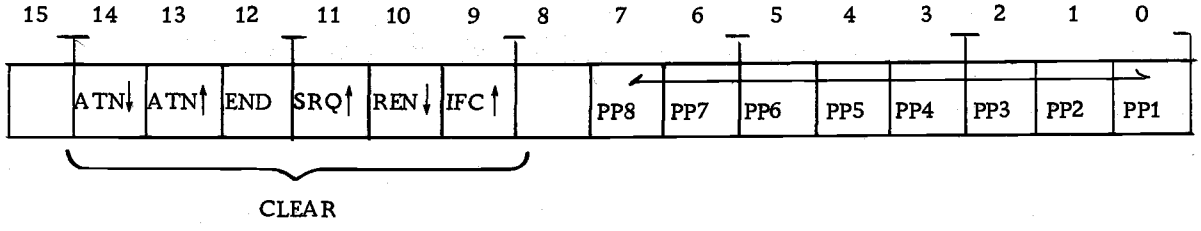
Bit 13: ATN↑ This bit is set when ATN is sensed unasserted to asserted on the GPIB.

Bit 14: ATN This bit is set when ATN on the GPIB goes from asserted to unasserted. This signals that an addressed talker can now talk.

Note: Whenever GSR_{14} = 1 (ATN) and LSR_{12} = 1 (LIS ENAB w/ATN), the interface will assert NRFD (no effect to TSR_{10}, just to GPIB line. This allows time for software to set Listener Enable (if necessary). To release NRFD, GSR_{14} (ATN OCC) must be cleared by writing a one into PPR_{14} (ATN CLEAR).

2.6 Parallel Poll Register

Parallel Poll Register (PPR) AAAA12

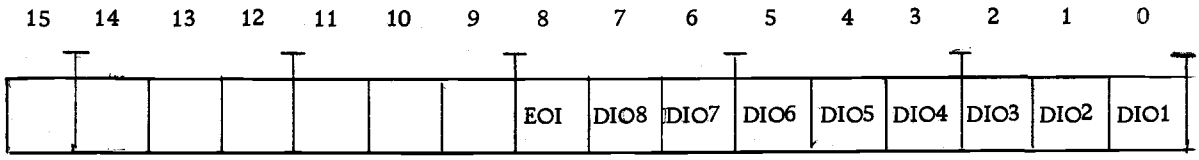


This register is used to respond to a parallel poll. If PP_i is a 1 then

the GPIB parallel poll response message PPR_i is sent on the GPIB. A RESET will set this register to all zeros. Otherwise bits are set and cleared by writing to the register. Writing a one in bits 9 through 14 does a clear of the corresponding bits in the GSR.

2.7 GPIB Data Register

GPIB Data Register (GDR) AAAA14



Reading this register obtains the current status of each of the corresponding lines on the GPIB. A 1 indicates the line is asserted on the GPIB.

INTERRUPT VECTORS

There are eight interrupt vectors. This leaves three bits which should be strappable to the range 000-340. If more than one interrupt condition is pending when the interrupt bus request is recognized, the interrupt with the highest corresponding interrupt request vector address will be on the interrupt recognized. The following is a list of interrupts and their corresponding addresses. An X in the address means the digit can be any value from 0 to 3.

Vector address		
X00 or X40	ATN↓	(Attention negative transition)
X04 or X44	ATN↑	(Attention)
X10 or X50	LISTEN	(data byte ready)
X14 or X54	TALK	(source handshake complete)
X20 or X60	END	(End of Message Interrupt)
X24 or X64	SRQ↑	(Service Request)
X30 or X70	REN↓	(Remote Enable Negative Transition)
X34 or X74	IFC↑	(Interface Clear)

The generation of interrupts other than TALK and LISTEN are controlled by bits in the GPIB Status Register (GSR). For each interrupt condition, there is an enable bit and a condition occurred bit. If both these bits are a 1, an interrupt is requested. If either

(or both) are 0, no interrupt is generated. Once an interrupt has been generated for a condition another one for the same condition will not be generated until either (or both) the enable bit or the condition occurred bit has been cleared to zero and then reset.

CIRCUIT DESCRIPTION

The circuitry of CP1100/GPIB interface can be divided into seven sections.

1. Address Decoding.
2. Registers
3. Multiplexers
4. Interrupt Circuitry
5. Handshake
6. Error Messages
7. Driver/Receivers

These sections have been described with reference to the schematic in the appendix. A cross reference has been provided following the schematic to facilitate locating the Integrated Circuit Components.

Address Decoding

There are seven strap options, A_4 through A_{10}, that give the interface the flexibility of responding to a range of addresses 164000-17776 octal. The sixteen address lines of the unibus are compared with the address of the interface, using a 6 bit unified bus comparators, U7, U8 and U9. When the interface is addressed by CP1100, pin 6 of U30 which is a 3 to 8 decoder, is enabled and 4 lower bits of the address are decoded to access one of the seven registers in the interface. Notice that the interface only responds to even bytes and

therefore, bit 0, for addressing purposes, is always unasserted.

Registers

The operation of the seven registers of this interface and their bit allocations have been described earlier. Here we show their location and briefly describe how they have been implemented.

1. Listener Status Register (LSR). Bits 0, 6 and 12 are latched in U44. On a write cycle into this register pin 12 of U66A goes high and clocks the information into U44. Bits 1, 2, 3, 4, 5, 8, 9 and 10 are the current values of the corresponding lines denoted as BUS1, BUS2, etc., and are read by CP1100 through the Multiplexers U24, U22, U43, U61, and U40. U107 is used for bit 7, the operation of which is described in the Handshake cycle.

2. Listener Data Buffer (LDB). U45 is used for this buffer. It latches the data coming in CP1100 through the interface. EOI is regarded as the 9th bit of data.

3. Talker Status Register (TSR). Bit 1, IFC, is implemented in a one shot, U130A. When a "1" is written in this location by CP1100, a pulse with duration 150μ sec appears at pin 13 of U130A which goes to pin 4 of U100 and after inversion appears on pin 2 of U100. Pin 13 of U130A also goes to pin 3 of U24 and CP1100 can read it through U3. U85 is used for bits 2, 3, and 6. U60 is used for bits 4, 8, 9, and 10. They are simply latches that CP1100 can write into

or read from. They also drive the bus lines through U100 and U102. U129B is the latch for bit 5. This latch is also set when the interface is in ANRS state, $\overline{DAV}$ is low, NRFD is low and NDAC is also low. Pin 12 of U127A goes high, if bit 11 is set. Then latch 11 is also high and pin 6 of U113B goes low and sets the flip-flop. U107 is used for Bit 7 and its operation is described in Handshake cycle. For bit 11 latch U73B is used. Bits 12, 14 and 15 are used for error messages and are described separately.

4. Talker Data Buffer (TDB). U5 is used to latch the data going from CP1100 to GPIB. Its operation is described in Handshake cycle.

5. GPIB Status Register (GSR). For bits 1, 2, 3, , 5, and 6, U65 is used. Bits 9, 10, 11, 12, 13 and 14 are the outputs of U47B, U49B, U68B, U69B, U87B and U88B. Their operation is described in "Interrupt Circuitry".

6. Parallel Poll Reigster (PPR). U64 and U63 are used for the first 8 bits of this Register (bits 0-7). When a Parallel poll is to be performed, ATN and EOI are high, pin 3 of U106A goes low, the outputs of two-line to one-line data selectors, U123 and U84 will all be high. Therefore all the inputs of U121 and U81 which are tri-state buffers are high. If any of these buffers is enabled, its output would go low and if any of these buffers is disabled its output will be held high by the pull-up resistors, unless another device on

the bus is holding it low. Therefore these buffers for Parallel poll look like open collectors, as required by IEEE STD. If a bit of PPR is high the corresponding buffer will be enabled through U124 or U83.

Bit 9 is not a latch. The process of writing a "1" in this bit takes pin 6 of U50B low which takes pin 3 of U70A low and clears U47B which clears bit 9 of GSR. Bits 10, 11, 12, 13 and 14 perform a similar function for U49B, U68B, U69B, U87B and U88B clearing bits 10, 11, 12, 13 and 14 of GSR.

7. GPIB Data Register (GDR). This Register only reads the status of each of the corresponding lines on the GPIB, DATABO-DATAB8, through the Multiplexers.

Multiplexers for Registers

To read the contents of the registers and the interrupt vector, the correct information should be put on the unibus at the right time. For this purpose data selectors/multiplexers U4, U24, U23, U22, U21, U43, U42, U41, U61, U40, U20 are used. The inputs to these chips come from the registers, but only the requested information chosen by the control lines A, B, and C appear at the outputs. These control lines are the outputs of U51 which is a 8 line to 3 line priority encoder. The inputs to this chip are the select lines of the registers and $\overline{\text{GIV}}$ line (Grant Interrupt Vector) which is the control line for the

interrupt vector. When a register is addressed or an interrupt has occurred, this information is encoded into the control lines which, in turn, select the appropriate line of the multiplexers and place them on the outputs D0-D12. For D13, D14, and D15 gates are used to perform the same function. D0-D15 go to the inputs of transceivers U3, U2, U1, U0 which are enabled on a read cycle or when an interrupt is granted.

Interrupt Circuitry

There are eight different sources of interrupt.

1. ATN↓ (Attention negative transition). When ATN occurs a "1" is clocked in the flip flop U88B. Pin 1 of U67A goes high and if GSR6 is also high (i.e., ATN interrupt is armed) a "1" is clocked in U88A and $\overline{Q0}$ goes low. This makes pin 15 of U52 which is an 8 to 3 priority encoder to go high and also encode $\overline{QO}$ on the 3 output lines pins 6, 7, and 9. When EO has gone high the interrupt cycle starts. The four states of the interrupt cycle IDLE, BUS REQ, SEL ACK, and MASTER are shown in a table on the schematic. By EO going high, pin 12 of U32D goes high and pin 11 goes low , and the flip flop U12B gets cleared. Therefore the interrupt circuitry goes from IDLE state to BUS REQ state. This request of the bus is granted by BG5IN going high which makes pin 6 of U10C go low and pin 2 of U91A go high and clocks a "0" in U12A and the transition from BUS REQ

state to SEL ACK state occurs. The interrupt is acknowledged by CP1100. Then BGIN5 goes low. It takes pin 6 of U10C high, pin 2 of U91 goes low. When pin 11 of U27D is low pin 13 of U27D goes high clocking a "1" into the flip flop U12B and the transition from SEL ACK state to MASTER state occurs. In this state, pins 4 and 5 of U32B are high and $\overline{\text{GIV}}$ becomes asserted. The interrupt vector INT2, INT3, INT4, INT5, INT6, and INT7 is placed on the bus indicating the source of interrupt. After the assertion of $\overline{\text{GIV}}$, both inputs of U93A are low and pin 1 of U39A goes high ($\overline{\text{SSYNC}}$ is still asserted), and pin 10 of U31C MIDLE goes low and flip flop U12A gets set and interrupt circuitry goes to IDLE state at the same time pins 4 and 5 of U72 go low and the 3 to 8 encoder U72 becomes enabled pin 15 SO goes low and flip flop U88A becomes cleared. EO goes low and the interrupt circuitry remains in the IDLE state until another interrupt occurs.

The ATN$\downarrow$ flip flop (U88B) is cleared by writing a "1" into PPR register bit 14. This gives a negative edge to pin 3 of U90A which in turn gives a negative edge to pin 13 of U88B. This flip flop is also cleared by a reset which gives $\overline{\text{INIT}}$ a negative edge which in turn gives a negative edge to pin 11 of U89D. The status of ATN flip flop U88B can be accessed by CP1100 by reading the GSR register bit 14.

2. <u>ATN$\uparrow$ (Attention)</u>. When a positive transition of ATN occurs a "1" is clocked into U87B. If this interrupt is armed (i.e., GSR5 is

high) a "1" is clocked into U87A and $\overline{Q1}$ goes low. The 8 line to 3 line priority encoder encodes the input to prepare the interrupt vector and EO goes high. The interrupt cycle starts in the same manner as described for ATN↓.

3. LISTEN (Data Byte Ready). When $\overline{DONE}$ is low which means data byte is ready and if LISTEN interrupt enable is asserted, i. e., bit 6 of LSR register is a "1", then pin 13 of U31D goes high and a "1" is clocked into U73A and $\overline{Q2}$ goes low. The rest of the interrupt operation is similar to previous interrupts.

4. TALK (Source Handshake Complete). When TALK INT ENAB which is bit 6 of TSR register is asserted LATCH 6 is low and a negative transition of READY clocks a "1" into U112B. This gives a negative transition to $\overline{Q3}$. The rest of the interrupt operation is similar to previous interrupts.

5. END (End of Message Interrupt) A negative transition of EOI or DAV clocks a "1" into U69B and if GSR4 is asserted a "1" is clocked into U69A and Q4 goes low and the interrupt cycle continues the same as before.

6. SRQ (Service Request). On a positive edge of SRQ a "1" is clocked into U68B. If GSR3 is asserted, a "1" is clocked into U68A and $\overline{Q5}$ goes low and the interrupt operation is started.

7. REN (Remote Enable Negative Transition). On a negative transition of REN, a "1" is clocked into U49B and if GSR2 is asserted

a "1" is clocked into U49A. $\overline{Q6}$ goes low and the interrupt operation continues as before.

8. IFC (Interface Clear). On a positive edge of IFC a "1" is clocked into U47B and if GSR1 is high a "1" is clocked into U47A. $\overline{Q7}$ goes low and the interrupt operation continues.

If more than one interrupt occurs at the same time, or if several interrupts have occurred without any of them being armed and suddenly all are armed by asserting all the bits in GSR register, then the priority encoder U52 allows the interrupts to follow each other according to their priority. IFC has the highest priority and ATN↓ the lowest. U72 clears the flip flop of the interrupt that has been serviced just after the relevant vector has been read by CP1100.

Handshake Circuitry

Handshake cycle is the process whereby digital signals effect the transfer of each data byte across the interface by means of an interlocked sequence of states and control signals. Interlocked denotes a fixed sequence of events in which one event in the sequence must occur before the next event may occur.

Handshake is divided into two parts, a) Acceptor Handshake and b) Source Handshake.

Acceptor Handshake Cycle. In this cycle the interface is the Listener and controls the lines $\overline{NRFD}$ and $\overline{NDAC}$. The device that

is the Talker on the bus controls $\overline{DAV}$.

At the start of this cycle, bit 0 of LSR Register is set to make the interface a Listener. Pin 8 of U105A is "0" and listen is high. Alternatively ATN is high and bit 12 of LSR is set. Pins 12 and 13 of U103D are high, pin 10 of U103C is low and pin 5 of U102 is high, pin 7 of U102 is low and $\overline{NDAC}$ on the bus is asserted. The interface is ready to accept data, Ready bit in the TSR is high and $\overline{NRFD}$ on the bus is also high. The device that is the Talker puts the data on the bus and asserts DAV. Pins 4 and 5 of U109B are high and pin 6 goes low. Pin 3 of U103A goes high, pins 10 and 11 of U127C are already high, pin 8 of U127C goes low which makes pin 9 of U102 go low NRFD gets asserted ($\overline{NRFD}$ on the bus goes low). On the rising edge of DAV pin 12 of U108A goes low and clocks the data in U45. Then pin 6 of U91C goes high which sets U107B, setting Done bit of LSR and clocks a "1" into U129A which takes pin 8 of U109C low (NDACIN goes low) which takes U103D pin 11 high. Pin 5 of U102 goes low and $\overline{NDAC}$ on the bus goes high indicating the data has been accepted. Here one cycle is completed. The Talker device puts a new byte of data on the bus and the Handshake cycle is repeated. Before a new byte of data is clocked into U45, the previous data should be read by GP1100 which generates a pulse at pin 13 of U93D which is transferred to pin 12 of U110F. This pulse clears flip flop U107B at the end of the read operation.

Source Handshake Cycle. In this cycle the interface is the Talker and controls $\overline{DAV}$ line. The device or devices that are Listener(s) on the bus control $\overline{NRFD}$ and $\overline{NDAC}$ lines.

When all Listener devices on the bus have indicated readiness to accept data, $\overline{NRFD}$ is high and $\overline{NDAC}$ is low. CP1100 latches a byte of data in U5 when $\overline{MSYNC}$ and $\overline{C1}$ and $\overline{sel6}$ go low giving a falling edge to STALK. The falling edge of STALK also clears Ready flip flop U107A and also fires the one shot U130B, after at least 2μ sec delay for data settling. It clocks a "0" in U111B which in turn clocks a "1" into U111A. $\overline{DAVIN}$ goes low, pin 8 of U101C goes high and $\overline{DAV}$ on the bus, pin 7 of U100, goes low. In response to this the Listener devices take $\overline{NRFD}$ line low and after all have accepted the data $\overline{NDAC}$ line goes high, pin 13 of U125D goes low, pin 11 of U125D goes low and clears U111B and U111A, $\overline{DAVIN}$ goes high which takes $\overline{DAV}$ high. This also clocks a "1" into the Ready flip flop U107A indicating the readiness for a new byte. The Listener devices make $\overline{NRFD}$ go high. This is the end of one Handshake cycle.

When the interface is not engaged in the Parallel poll, i.e., ATN and EOI are not both asserted, pin 3 of U106A is high and 2 line to 1 line data selectors, U123 and U84, put the data on the bus through Tri-state buffers, U121 and U81. These buffers are enabled by U124 and U83 when Ready is low.

For the purpose of transmitting data the buffers are Tri-state

to increase speed. however for Parallel poll they should look like open collectors.

Note: Since the outputs of bit 1 through bit 10 of TSR Register directly drive the bus, CP1100 has complete control over the interface and it is possible to check the operation of the interface by performing a false Handshake without any other device being connected on the GPIB. The Status of the GPIB control lines can be ready by CP1100 through LSR Register.

Error Messages

There are four conditions that cause an error to occur:

1. When $\overline{\text{NRFD}}$ and $\overline{\text{NDAC}}$ lines on the bus are both high and CP1100 tries to out put a data byte. In this case pin 3 and 4 of U108B are high and when CP1100 puts a byte of data in TDB pin 5 of U108B also goes high and pin 6 goes low and pin 10 of U126B goes low and sets the out put of this flip flop which is bit 12 of TSR register, i.e., write Error. $\overline{\text{LATCH 12}}$ is low which takes pin 8 of U113C high taking pin 11 of U113D low and D15 goes high when TSR is addressed, i.e. $\overline{\text{sel4}}$ goes low. Therefore bit 15 of TSR, which is the Error bit, is also set.
2. When the interface is already busy putting a byte out and CP1100 tries to put a second byte out. In this case $\overline{\text{READY}}$ is high when STALK goes high and pin 3 of U89A goes high taking pin 6 of

of U105B low. It sets U126A and U126B, both bit 12 and 14 of TSR Register are set. Also bit 15 (error bit) is set.

3. When CP1100 is putting a byte out while $\overline{\text{ATN}}$ line is asserted by another device on the GPIB. In this case ATN and $\overline{\text{LATCH5}}$ are both high. Pin 6 of U106B is low and pin 5 of U105B is high. When CP1100 tries to put a byte out pin 4 of U105B also goes high and pin 6 goes low asserting both error flip flops U126A and U126B. Bits 12 and 14 of TSR Register get set and also bit 15, Error bit, gets set through U113C.

4. When the interface is busy out putting a byte and $\overline{\text{ATN}}$ on the bus gets asserted. In this case pin 2 of U126A, $\overline{\text{READY}}$, is high when ATN goes high a "1" is clocked into the flip flop and bit 14 of TSR Register gets set as well as bit 15 (Error).

Therefore, if an error occurs, bit 15 of TSR is always set and bits 12 and 14 of TSR identify the type of error.

Error flip flops are cleared by a correct write into TDB Register, where STALK pin 10 of U125C goes low and clears U126A and when pin 12 of U86A goes high clocks a "0" in U126B. Error bits are also cleared by $\overline{\text{INIT}}$.

Driver/Receivers

For data lines on the Unibus U3, U2, U1 and U0 are used for drivers/receivers. They also invert the signals. The receivers are only enabled when data or an interrupt vector is to be read. U109A and U67C are the control logic. For address lines, U7, U8, U9, comparators are designed to act as drivers too.

For control lines of GPIB U100 and U102 are used for driver receivers. They also invert the signals. For data lines of GPIB, U121 and U81 are used for drivers. They are Tri-state for data transfer but look like open collectors for Parallel poll. For receivers U122 and U82 are used.

This concludes the circuit description of CP1100/GPIB Interface. It is possible to modify the address decoding and interrupt structure of this interface to design an interface between LSI-11 Computer and the General Purpose Interface BUS.

CABLE AND EDGE CONNECTORS

GPIB Pin Assignment

GPIB PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
1	DIO1 (LSB)	DIO1 (data input output 1)
2	DIO2	
3	DIO3	DIO8 (data input output 8)
4	DIO4	(Message bytes are carried
13	DIO5	on the DIO signal lines in
14	DIO6	a bit-parallel byte-serial
15	DIO7	form, asynchronously, and
16	DIO8 (MSB)	generally in a bidirectional manner.)
6	$\overline{\text{DAV}}$	DAV (data valid) is used to indicate the condition (availability and validity) of information on the DIO signal lines.
7	$\overline{\text{NRFD}}$	NRFD (not ready for data) is used to indicate the condition of readiness of device(s) to accept data.
8	$\overline{\text{NDAC}}$	NDAC (not data accepted) is used to indicate the condition of acceptance of data by device(s)
11	$\overline{\text{ATN}}$	ATN (attention) is used to specify how data on the DIO signal lines are to be interpreted and which devices must respond to the data.
9	$\overline{\text{IFC}}$	IFC (interface clear) is used to place the interface system, portions of which are contained in all interconnected devices, in a known quiescent state.

GPIB PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
10	$\overline{SRQ}$	SRQ (service request) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events.
17	$\overline{REN}$	REN (remote enable) is used (in conjunction with other messages) to select between two alternate sources of device programming data.
5	$\overline{EOI}$	EOI (end or identify) is used to indicate the end of a multiple byte transfer sequence or, in conjunction with ATN, to execute a polling sequence.
18	GND (6)	
19	GND (7)	
20	GND (8)	signal grounds. Gnd (n) refers to signal ground return of the referenced pin #.
21	GND (9)	
22	GND (10)	
23	GND (11)	
24	GND (LOGIC)	

CP1100 Pin Assignments

CP1100 PIN NAME	SIGNAL NAME	
EH2	$\overline{A0}$	
EH1	$\overline{A1}$	
EF1	$\overline{A2}$	
EV2	$\overline{A3}$	INTERFACE
EU2	$\overline{A4}$	ADDRESS LINES
EV1	$\overline{A5}$	
EU1	$\overline{A6}$	
EP2	$\overline{A7}$	
EN2	$\overline{A8}$	
ER1	$\overline{A9}$	
EP1	$\overline{A10}$	
EL1	$\overline{A11}$	
EC1	$\overline{A12}$	

EK2	$\overline{A13}$	
EK1	$\overline{A14}$	
ED2	$\overline{A15}$	
ED1	$\overline{A16}$	
CU2	$\overline{INT2}$	
CT2	$\overline{INT3}$	INTERRUPT
CN2	$\overline{INT4}$	
CP2	$\overline{INT5}$	VECTOR ADDRESS
CV2	$\overline{INT6}$	
CM2	$\overline{INT7}$	
CS2	$\overline{D0}$	
CR2	$\overline{D1}$	
CU2	$\overline{D2}$	
CT2	$\overline{D3}$	
CN2	$\overline{D4}$	
CP2	$\overline{D5}$	
CV2	$\overline{D6}$	
CM2	$\overline{D7}$	
CL2	$\overline{D8}$	
CK2	$\overline{D9}$	
CJ2	$\overline{D10}$	
CH1	$\overline{D11}$	
CH2	$\overline{D12}$	
CF2	$\overline{D13}$	
CE2	$\overline{D14}$	
CD2	$\overline{D15}$	
DP2	BG 5 IN	Bus Grant in
DR2	BG 5 OUT	Bus Grant out
EE1	$\overline{MSYN}$	Master sync
EJ1	$\overline{SSYN}$	Slave sync
DL1	$\overline{INIT}$	Initialize
EF2	$\overline{BCI}$	Clear interrupts
DF2	$\overline{BUS\ REQ}$	Bus request
FT2	$\overline{SACK}$	Sync acknowledge
FM1	$\overline{INTR}$	Interrupt (sends Vector address with INTR)
FD1	$\overline{BBZY}$	Bus Busy

CP1100/GPIB INTERFACE ELECTRICAL SPECIFICATION

GPIB DATA RATE

Standard Bus:

Bus distance -	20 meters
Bytes/sec-	250 K
Load Interval-	2 meters
Driver type -	open collector 48 ma

INTERCONNECTED DEVICES: 15 max

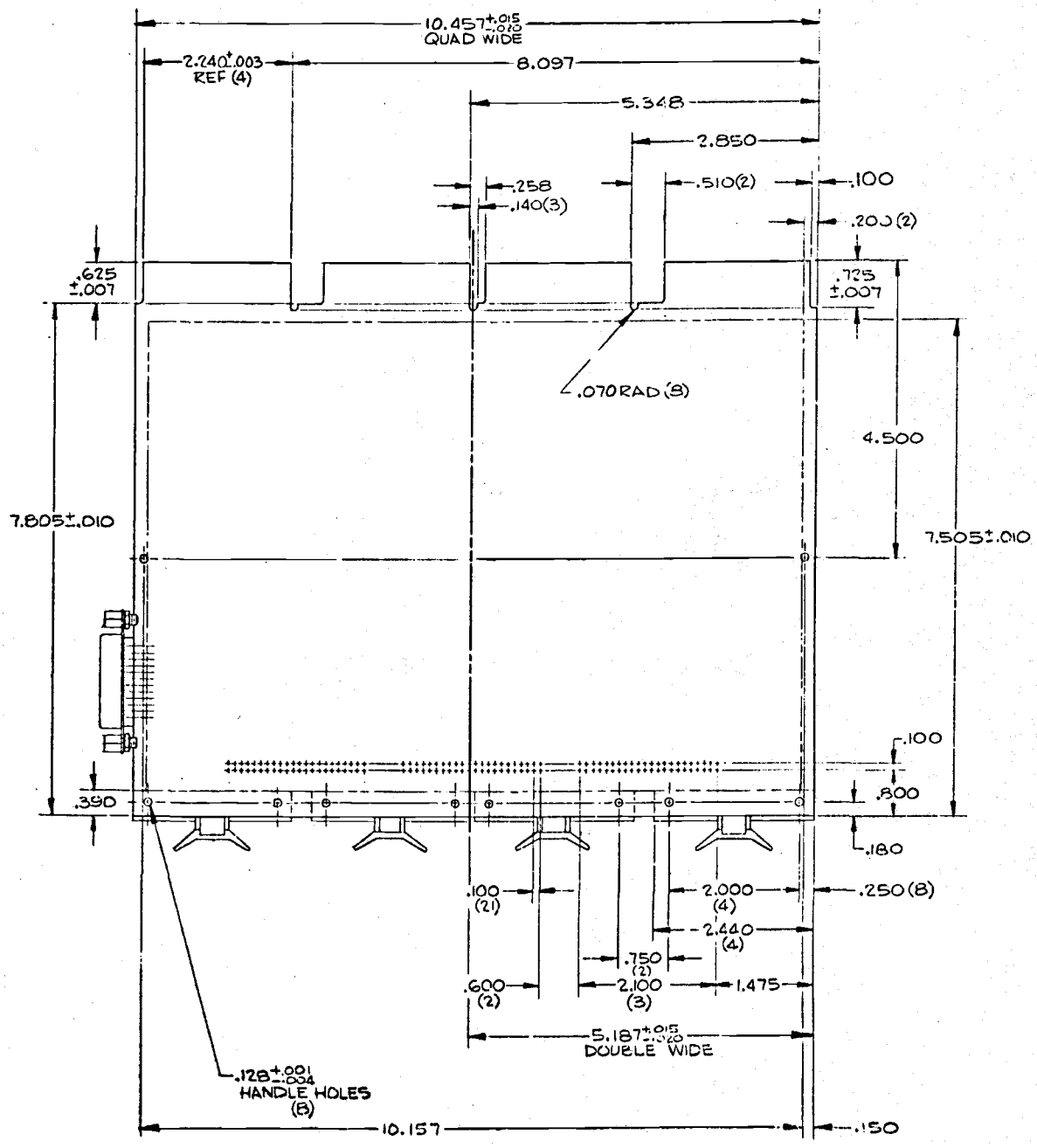
CABLE LENGTH: 20 meters max

SIGNAL LINES (GPIB): 16 active: 8 data 8 control

ELECTRICAL CIRCUITS

TTL	High = asserted - 2.4 v
	Low = unasserted - 0.8 v

Mechanical Specifications

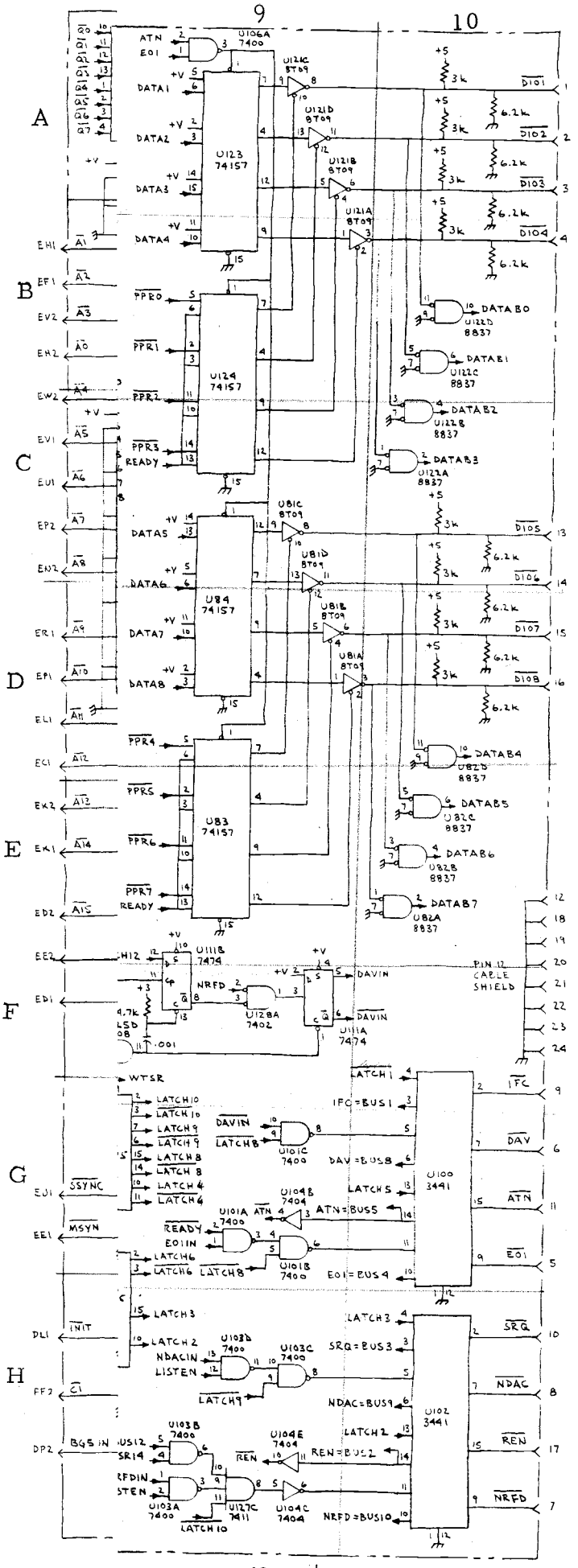


BIBLIOGRAPHY

1 IEEE Standard Digital Interface for Programmable Instrumentation, 488-1975.

2 PDP-11 Peripherals Handbook, 1975. Digital Equipment Corporation, (DEC).

APPENDIX



CP1100/GPIB INTERFACE

CROSS REFERENCE TABLE

U0	E7	U47B	F4
U1	D7	U48A	F4
U2	D7	U48B, D	E4
U3	C7	U48C	D4
U4	A6	U49A	E5
U5	C8	U49B	E4
U6	-	U50A, B	F3
U7	F1	U50C	E5
U8	D1	U50D	F5
U9	C1	U51	C2
U10A	H1	U52	A1
U10B, D, F	B1	U53A, B	G1
U10C	H2	U53C	G2
U10E	G2	U53D, E, F	A1
U11A	G5	U60	G9
U11B	G2	U61	C6
U11C	H1	U63	H8
U11D	H5	U64	G8
U12A	G3	U65	C3
U12B	G4	U66A	H8
U13A, D	G5	U66B	F9
U20	E6	U66C	F8
U21	E6	U67A	A4
U22	D6	U67B	B4
U23	C6	U67C	E7
U24	B6	U67D	G3
U27A, C	H5	U68A	E5
U27B	H1	U68B	E4
U27D	H4	U69A	D5
U30	B2	U69B	D4
U31A, B	C4	U70A, B	F3
U31D	B4	U70C	E3
U31C	G3	U70D	D3
U32B	G4	U71A	D5
U32C	B5	U71B	E5
U32D	H4	U71C	B5
U40	D6	U71D	A5
U41	B6	U72	A2
U42	A6	U73A	B5
U43	F6	U73B	H7
U44	H8	U81A, B	D9
U45	C9	U81C, D	C9
U47A	F5	U82A, B, C	E10

U82D	D10
U82E	H5
U82F	G1
U83	E9
U84	D9
U85	H9
U86A	A7
U86B	B3
U87A	A5
U87B	B4
U88A	A5
U88B	B7
U89A	B7
U89B	F7
U89C	B3
U89D	A3
U90A	A3
U90B	B3
U90C	D3
U90D	E3
U91A	H3
U91B	G6
U91C	D8
U91D, E, F	F6
U92A	C5
U92B	F6
U93A	G3
U93B	F7
U93C, D	E8
U100	G10
U101A, B, C	G9
U101D	D3
U102	H10
U103A, B, C, D	H9
U104A	H5
U104B	G9
U104C	B7
U104D, E	H9
U104F	E8
U105A	E8
U105B	B7
U106A	A9
U106B	A7
U106C	D8
U106D	A7
U107A	A8
U107B	D9
U108A	E9
U108B	A8
U108C	H4
U109A	C8
U109B	C9
U109C	D9
U109D	E7
U110A, D	A8
U110B	C8
U110C	H6
U110E	H1
U110F	E8
U111A	F9
U111B	E9
U112A, B	C5
U113A	D8
U113B	H7
U113C	G6
U113D	F6
U121A	B9
U121B, C, D	A9
U122A, B	C10
U122C, D	B10
U123	A9
U124	B9
U125A	A7
U125B	B8
U125C	B7
U125D	F9
U126A	B7
U126B	B8
U127A	H7
U127B	A8
U127C	H9
U128A	F9
U128B	B4
U128C	H8
U128D	D8
U129A	D8
U129B	H7
U130A	H6
U130B	E9