WILSON Laboratories, Inc.

TX-1200

MAINTENANCE MANUAL

REVISIONS
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Prepared by:

WILSON Laboratories, Inc.

2237 North Batavia Street
Orange, California 92665

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1.0 CRYSTAL OSCILLATORS

There are two crystal oscillators which run continuously. One supplies 2.88 MHZ and the other provides an optional frequency determined by the user's tape speed requirements. Both crystal frequencies may be divided to provide precise tape writing clocks, but the 2.88 MHZ is also a necessary reference for the speed display logic.

2.0 SPEED SELECT

The SPEED panel switch selects one of six standard speeds. If the last position, 75 IPS, is selected, four additional DIP switches located at B14 on the logic board are enabled. Each one of these four DIP switches can select a different speed. A total of 10 different speeds can thus be selected. Additionally, the "6250" configuration control may be used to modify each of the 10, so that a maximum of 20 different speeds can be realized.

The speed select does not control the tape speed; it only provides a clock whose frequency is matched to the bit rate of the speed selected. It does this by pulling down one (or more) of the

9 inputs of the priority encoder C14. The outputs of C14 drive four address inputs of C13 PROM; the fifth input is supplied by the "6250" switch signal. The C13 PROM has 32 locations, each containing 8 bits. Seven of the PROM outputs supply the parallel loading inputs of scaling counter C11+C12. The eighth PROM output controls which of the two crystal oscillators will be gated into the clock input of C11+C12.

The scaled "speed" output C5 is a square wave whose frequency is proportional to the tape speed. For example, the C5 frequency for 75 IPS is 0.48 MHZ. This is obtained by selecting the 2.88 MHZ oscillator and dividing its frequency by 6. Since the flip-flop output E6.5 must divide by 2 to create a square wave, the scaling action of C11+C12 must be to divide by 3.

The least ratio by which C11+C12 can divide is 2; the maximum ratio is 128. The ratio is determined by the C13 PROM output. The PROM output must be the two's complement of the divide ratio.

RATIO	PROM LOW OUTPUTS
2	C13.1
3	C13.2
4	C13.1+C13.2
5	C13.3

The combination of crystal frequency and the C11+C12 counter ratio determines the tape speed to which the C5 output is matched. Following are the ratios and crystal frequencies which match several standard tape speeds:

	CRYSTAL MHZ						
	2.304	2.88	3.20	3.84	4.80	5.12	6.40
SPEED							
12.5		18	20	24	30	32	40
25		9	10	12	15	16	20
37.5		6		8	10		
45	4	5					
60	3			5			
75		3		4	5		
125			2		3		4
150				2			
200						2	
250							2

3.0 TAPE CLOCKS

Additional scaling logic divides the C5 frequency. Two flip-flops located at D2 either divide by 2 for high density NRZI or divide

by 3 for low density NRZI. Multiplex gate E3.9 selects either this divided frequency for NRZI or the undivided C5 for PE to produce output 4XC. 4XC is further divided by a factor of 4 to produce WCØ, which is the frequency of the tape bit rate. Following are MHZ values of C5 and WCØ for different speeds and densities:

SPEED IPS	12.5	25	37.5	45	60	75
C5	0.080	0.160	0.240	0.288	0.384	0.480
WCØ PE	0.020	0.040	0.060	0.072	0.096	0.120
WCØ NRZI LO DEN	0.0067	0.0133	0.020	0.024	0.032	0.040
WCØ NRZI HI DEN	0.010	0.020	0.030	0.036	0.048	0.060

RD CLK is an 8 times multiple of WCØ. It is used in the PE missing edge detect logic to divide the bit cell time into 8 fractions.

4.0 MOTION CLOCKS

The C5 frequency is divided by counters B6 and B7 to produce clock outputs C8-C20. These clocks provide time intervals proportional to tape movement. When writing, data block lengths and record gaps are derived from these clocks.

5.0 TEST START

All test action is started by depressing the START STOP switch. The anti-chatter circuit E8.8/E8.11 clocks on the RUN flip-flop. A1.3 then goes high, allowing C17 to clock on the SM (synchronous motion) flip-flop. The SM output passes through B2.13 and A3.6 to become SXC. SXC through either A3.8 or D3.8 sends a motion control signal to the transport, causing either a forward or reverse motion to begin. The direction of motion is determined by the MOTION select switch.

6.0 TEST STOP

The RUN flip-flop may also be clocked off by depressing the START STOP switch. SM will then be clocked off by the next C17 fall and tape motion will stop. The RUN flip-flop will be reset by the $\overline{\text{RST RUN}}$ if an error is counted when STOP ON ERROR is selected. $\overline{\text{RST RUN}}$ also causes a stop if EOT is sensed when reading in FWD or FWD/FWD motion or if BOT is sensed when in REV or REV/REV motion.

Depressing the REWIND switch will also reset RUN. Any illegal command combination will force RUN off.

7.0 MOTION CONTROL

The MOTION switch selects one of six modes of test motion:

a. FWD is a steady forward tape movement which stops at EOT when reading only and rewinds to BOT if writing.

b. REV is a reverse read only steady tape movement which stops at BOT.

c. ALT is an endless cyclic motion which reads a single block, alternately forward and reverse. Flip-flop B3.6 toggles with each change of direction.

d. FWD/FWD is a cyclic forward-stop-forward motion. If the WRITE is down the test motion ends at EOT. If the WRITE switch is up, an automatic rewind occurs at EOT. Also, when writing, the BLOCK LENGTH control determines the length of the block written.

e. REV/REV is a read only cyclic reverse-stop-reverse motion which stops at BOT.

f. PROGRAM is an endless of sequenced forward and reverse motion which progresses forward along the tape. If the WRITE switch is up, automatic rewind will occur at EOT. If the WRITE switch is down, EOT will start a reverse cyclic progress of the tape.

8.0 CYCLIC MOTION

There are two types of cyclic motion, forced cycling and block following. Forced cycling motion is timed by a selected motion clock. Block following motion is started by the C17 clock but continues until the end of a block is sensed.

Cyclic writing is always forced; cyclic reading will be forced if the RAMP switch is up. If cyclic writing with a double gap head, then the duration of the write strobes will be timed by the selected motion clock, but the motion will not stop until the last character written has been read.

Tape motion begins when C17 fall at B5.9 clocks on SM. The tape ramps up to synchronous speed and will have moved about 0.5 inch when the next C17 fall at B5.12 clocks on WDT. WDT applied at B1.10 enables a motion clock selected by B8 to be counted at E2.1; after 8 counts the CF (cycle finished) output at E2.6 will rise. Now, if the

tester is ramp reading or writing with a single gap head, the CF signal will be inverted at B1.6 and will go through A1.6 to force SM off. SM going down resets WDT, and WDT low makes E2.2 high, which brings down CF to finish the cycle.

When SM went low, the tape speed ramped to a stop with a tape movement of about 0.1 inch. The next fall of C17 will again clock on SM to start a new cycle.

On block following and on cyclic writing with a double gap head, C3.12 will be low to switch SM resetting from CF to $\overline{\text{REND}}$.

$\overline{\text{RDSI}}$ applied to D11.6 are read strobes developed from data edges read from the tape. RDT will be clocked on by the first $\overline{\text{RDSI}}$ sensed after WDT goes high. Gate output C1.8 will go high, allowing D5 counter to count 4XC beginning with a starting count of 8. Each $\overline{\text{RDSI}}$ reloads D5 to the beginning count of 8. If no $\overline{\text{RDSI}}$ pulses are sensed for two bit cell times, $\overline{\text{REND}}$ will go low to signal the end of a block.

Thus, after motion is started, at least one read strobe must be sensed to signal the start of a block. Then there must follow an absence of read strobes for a tape length equal to two characters before motion will be stopped.

9.0 FORCED CYCLING BLOCK LENGTH

If the PROGRAM mode is selected, A8.1 will be high and the A8 counter will be incremented by the $\overline{\text{RSTSM}}$ signal at the end of each tape movement. A8 outputs drive B8 select inputs so that for each tape movement a different motion clock is selected. This makes successive tape movements differ in length.

If the PROGRAM mode is not selected, A8.1 load input will be low and A8 outputs will follow A8 inputs. The BLOCK LENGTH select switch makes one of six inputs to A9 priority encoder low. A9 outputs feed through A8 to input B8 multiplexer as the select address. B8 thus selects one of six clocks matching the BLOCK LENGTH switch position. The BLOCK LENGTH indicated on the panel corresponds to the number of characters in each block when writing NRZI at 800 BPI. The time period from the rise of WDT to the rise of CF is the time required to write this number of characters. Tabulated below is the tape length in inches of WDT·$\overline{\text{CF}}$ time.

PANEL LENGTH	NRZI LENGTH	PE LENGTH
8	0.01	0.04
64	0.08	0.08
128	0.16	0.16
256	0.32	0.32
512	0.64	0.64
1024	1.28	1.28

10.0 CONTINUOUS MOTION

The single C17 cycle time interval between the turn-on of SM which starts tape motion and the beginning of WDT applies equally to both cyclic and continuous motions. On continuous motions the low CYCLE input to B1.9 prevents CF output and the low CYCLE input to C3.2 blocks SM reset by $\overline{\text{REND}}$. The continuous motion direction is selected by placing the MOTION switch in either the FWD or REV position.

11.0 ALTERNATE MOTION

With the MOTION select switch in the ALT position, the $\overline{\text{ALT}}$ signal will be low, and when RUN is up the gate output B2.2 will be high, allowing SM input at B3.9 to clock a direction reversing flip-flop B3.6. Initially, B3.6 is high, producing forward motion on the first movement. When SM falls, B3.6 goes low so the next cycle is reverse motion. Each SM fall will clock B3.6 to the opposite state and reverse the motion.

If the RAMP switch is up, the motion will be forced cyclic with the magnitude of the movement selected by the BLOCK LENGTH control. If the RAMP switch is down, the motion will match the length of the recorded block.

12.0 PROGRAM MOTION

When the MOTION switch is set to PROGRAM and RUN is started, cyclic forward motion begins. After the tape moves off BOT, C4.2 counter reset input will go low, allowing the counter to be incremented by SM at the end of each cycle. Counter output 3PRO is alternately low and high each 4 cycles. Output $\overline{3PR2}$ is low only at the count of 7. Initially, $\overline{A}$ is high and $\overline{2PRO}$ is low and $\overline{FWT}$ follows the state of $\overline{3PRO}$. $\overline{FWT}$ input to A6.5 forces the first four cycles to be forward motion. $\overline{3PR2}$ input to A6.3 forces the seventh cycle also to be forward. Of each 8 cycles, 5 are forward and 3 are reverse, so the tape oscillates and progresses in the forward direction.

When EOT is sensed, ETOL input to C7.2 goes high and $\overline{A}$ is clocked low at the end of the next forward movement. $\overline{2PRO}$ is forced high and $\overline{FWT}$ no longer follows $\overline{3PRO}$ but remains high. Now only $\overline{3PR2}$ forces forward motion so the tape oscillates 7 cycles reverse and 1 forward, progressing backward until BOT forces $\overline{A}$ high again.

13.0 WRITING

Test writing requires that the WRITE switch must be up and the tape motion must be forward. In the PROGRAM mode, writing may

occur during the forward cycles forced by $\overline{FWT}$ low but not during the forward cycles caused by $\overline{3PR2}$ low.

Write current is on when the $\overline{WEN}$ signal to the transport is low. Input E8.5 controlled by the WRITE switch must be high and either $\overline{FWD}$ signal derived from the MOTION switch must be low or the combination $\overline{2PRO}$ and $\overline{3PRO}$ PROGRAM mode signals must both be low.

14.0 WRITE DATA STROBE

In order to write data on the tape, $\overline{WDS}$ (write data strobe) pulses must be sent to the transport each character time. The character time is defined in the tester by WCØ. For NRZI writing each WCØ fall triggers one-shot D9 which generates a 2-microsecond wide CLOCK pulse. For PE writing 2XC triggers D9 to generate two CLOCK pulses per character.

$\overline{WDS}$ pulses to the transport begin at WDT time after the tape has ramped up to speed. $\overline{WDS}$ pulses are terminated by the rise of CF when FWD/FWD or PROGRAM block writing is in process.

15.0 WRITE RESET STROBE

A single write reset strobe $\overline{\text{WARS}}$ is automatically generated at the end of each cyclic write block. $\overline{\text{WARS}}$ is sent to the transport for the purpose of resetting the write data flip-flop. This also records the LRCC test character.

E10.3 follows WDT·$\overline{\text{CF}}$ by one CLOCK period so C1.11 and C6.2 are high for one CLOCK period following the end of $\overline{\text{WDS}}$ time. This allows the single $\overline{\text{WARS}}$ pulse to be transmitted.

If the WRITE RESET switch is up when writing (not in program mode), then WARS TIME will be high and $\overline{\text{WARS}}$ will be held solidly low. This nullifies the effect of $\overline{\text{WDS}}$ strobes and the tape is erased.

16.0 WRITE DATA

Nine drivers, F3, F2, and F1.8, transmit inverted write data $\overline{\text{WDØ}}$-$\overline{\text{WDP}}$ to the transport. Nine exclusive OR gates, F7, F6, and F5.8, supply the drivers with true write data for NRZI recording and with WCØ modulated data for PE recording.

The RANDOM/ANSI/TRACK switch selects one of three data sources. RAN DATA is a sequenced data pattern generated by E4 from the continuously running clock. ANSI data is a sequenced set of 16 characters output by F12 ROM. TRACK data is supplied by the $\overline{SD\emptyset}$-$\overline{SDP}$ outputs of the nine track switches.

If RANDOM data is selected, the F8 and F9 shift registers are operated in the shift mode. RAN DATA at the serial input F8.1 is shifted each character time sequentially to the eight tracks Ø-7. Track P is supplied with parity data generated by F4.

When ANSI data is selected, the sequenced F12 ROM outputs are passed through F10 and F11 and parallel loaded into the shift registers F8 and F9 each character time. Track P data again comes from F4 parity generator. When TRACK data is selected, the $\overline{SD\emptyset}$-$\overline{SD7}$ track switch levels are parallel loaded into F8 and F9 each character time. Track P data comes from the $\overline{SDP}$ level through selector E5.9.

17.0 READ DATA ERROR NRZI

Selector E5.12 outputs a parity check high level from C25 if there is an error when reading RANDOM or ANSI data. On TRACK data reading the comparison gates F26, E26, and D26.4, compare read

data with track switch data on each track and a comparison error will also output at E5.12 as a high level. The ERR-NRZ output of E11 will be clocked high by $\overline{RDS}$ on each error character except that ERR-NRZ is inhibited for the first two $\overline{RDS}$ in each block. RDT-1 will rise on the first $\overline{RDS}$ and E11.5 will rise on the second $\overline{RDS}$. When blocks are read reverse, the first character is the LRCC character which validly generates parity and comparison error.

NRZI data is checked for LRCC error by C26. If C26.9 output remains high at the end of the block after the last character has been read, then there is an LRCC error.

18.0 READ DATA ERROR PE

PE data requires that the RD level in each track change at the center of each cell time. Ones and zeros are identified by whether the change is a rising change or a falling change. The tester does not identify ones and zeros but tests only that the interval between RD changes does not exceed a prescribed limit. The expected interval is 1/2 cell time and the interval test indicates error if the interval exceeds 3/4 cell.

There are nine identical RD edge detecting circuits, F25, E25, and D26.3. Negative pulses derived from each edge are used to reset nine shift registers, A13-A20. These shift registers are clocked and shifted by the RD CLK signal which is eight times faster than the character rate. An error output EØ-EP will rise if there are seven or more RD CLK pulses between two consecutive RD edges. ERP PE output from B19.8 is the sum of errors on all tracks.

The nine TRACK LEDs show which track is erroring. Error pulses $\overline{E\emptyset}$-$\overline{EP}$ directly set nine LED driving flip-flops C23-F23 and C22.9. Any LEDs lighted stay on until reset by RDT-1 going down at the end of the block.

On RANDOM and ANSI data full one bit intervals will occur between RD edges. Selector E9.4 supplies 4XC for missing edge detect counting. Errors will show on intervals exceeding 1-1/2 cells.

19.0 TRACK DATA INDICATORS

The same LEDs that show which track is failing in PE will show data "ones" when reading NRZI. The read strobe $\overline{RDS}$ clocks the driving flip-flops according to the RD level at the data input.

20.0 READ STROBE

The read strobe from the transport is labeled $\overline{\text{RDS IN}}$ which becomes $\overline{\text{RDSI}}$ at E3.7 for NRZI operation. The transport supplies no read strobe on PE operation. An $\overline{\text{RDSI}}$ signal is created by summing at F1.11, the edge detecting signals from tracks 2 and P. The two flip-flops D1 serve to block the use of at least the first four cell edges in each block because it is expected that PE beginning data will be bad.

The $\overline{\text{RDSI}}$ signal through D6.5 drives the RDS indicator. $\overline{\text{RDSI}}$ is also used to detect the beginning and end of data blocks.

For NRZI data strobing the $\overline{\text{RDS-IN}}$ signal becomes $\overline{\text{RDS}}$ at gate E12.3. Gates D11.10 and D11.13 perform a necessary clipping of the trailing edge of $\overline{\text{RDS-IN}}$ for the AMPEX transport.

21.0 ERROR COUNTING

PE and NRZI error signals are summed at E14.8 and pass through E12.6 if the tester is not writing with a single gap head. E10.6 is set high on each error pulse and clocked off by WCØ.

E10.6 is shifted through E9 to appear at E9.10 as ERROR PULSE four WCØ cycles after the error occurred. Gate A7.12 limits ERROR PULSE transmission to RDT time. RDT goes down two character times after the last $\overline{\text{RDS}}$ so the 4-character delay in ERROR PULSE provides for clipping parity errors from the LRCC character and PE missing edge errors which necessarily occur while sensing block end.

The LRC ERR is added through A7.6 and B11.8. The combined error signals are counted by B9 and B10 which also drive the LED ERROR display. LRCC errors latch on LRCC indicator. The FWD and WRITE indicators show what action was happening at the time of the error.

22.0 BOT DELAY

The $\overline{\text{BOT}}$ signal from the transport forces $\overline{\text{BOT DLY}}$ low. If RUN is up, $\overline{\text{BOT DLY}}$ forces forward motion through A2.3 and A3.6. After the tape has advanced off BOT, eight cycles of C17 are counted at C4.13. $\overline{\text{BOT DLY}}$ then rises, allowing SM cycles to begin. The tape moves about four inches forward during the $\overline{\text{BOT DLY}}$ time.

23.0 SPEED INDICATOR

Speed measurement can be made by reading either 800 BPI NRZI or 1600 BPI precision recorded tapes. The tape will read solid ones. $\overline{RD2}$ rising edges at D12.10 will pass through D16.7 and be counted by the display counter at L1.15. Counters F14-F17 count the 2.88 MHZ clock to develop load pulses which pass through D16.4, E12.11, and U2.6 to pin 5 on each display decode. The load pulse transfers the $\overline{RD2}$ count to a latch which drives the display. Immediately after the load pulse, a reset pulse from C17.6 is applied to the display counters at pin 12. This returns the display counters to zero value before counting the next interval.

Reset pulses are generated at precise intervals of 0.0125 second. B17 is a one-shot, triggered by the reset pulses, which limits load pulses to one per second so that the display will remain steady long enough to be read.

PE tapes have twice as many $\overline{RD2}$ edges per inch as NRZI tapes. D2 is a counter output which rises and falls each eight $\overline{RD2}$ counts. Gates D15.6 and D12.8 block half of the $\overline{RD2}$ pulses so that only 800 per inch are counted.

When the STATUS TEST switch is pressed, E18.8 gates WCØ clock onto the $\overline{RD2}$ line. The WCØ signal is counted to give indication of the speed selected by the SPEED control.

24.0 SKEW INDICATOR

Skew measurements are made when reading tapes recorded with solid ones on each track. Skew is the amount of tape travel between sensing a data edge on the leading track and sensing the corresponding edge on the most lagging track. NRZI skew is usually no greater than 200 microinches or about 1/6 of the character spacing at 800 BPI. PE skew may be several bits in magnitude with readings as high as 2000 microinches.

Nine skew counters, F21, E21, D21, C21, and B21.6, clock on $\overline{RDØ}$-$\overline{RDP}$ falling edges. After eight counts the outputs DØ-DP rise. On each track, the timing offset of the output rise matches the offset of the clocking input fall. The ANY signal rises when the first track output rises. The ALL signal rises when the last track output has risen. The time interval (skew period) between the rise of ANY and the rise of ALL is proportional to the skew measurement desired.

On NRZI skew measurement the skew counters are reset by the first $\overline{RDS}$ pulse after ANY rises. On PE skew measurement the counters are reset periodically by forced missing edge error signals. On PE skew writing the $\overline{BLINK\ OSC}$ signal clocks B24.9 about once per second. 2XC then clocks B25.8 low for 1/2 cell time, causing B24.3 to miss one toggle and the tape is written with a simultaneous missing edge on all tracks.

NRZI skew periods are spaced 8 x .00125 = 0.01 inch; PE skew periods are spaced 16 x .000625 = 0.01 inch. Because of this equal spacing, the same display counter reset interval derived from F14-F17 is applicable to both.

C17.5 gates D14 counter to count the CLK input during the skew period. D14.15 output scaled 16:1 is passed through D16.7 and counted by the display counter at L1.15.

The 16:1 scaling by D14 multiplied by the 10000-microinch interval between skew periods determines that the interval between reset pulses to the display counter must be 160000 CLK pulses. Counters F14-F17 provide a scaling factor of 20000 and the gating of F14 by E17.4 multiplies this by a factor of 8.

25.0 LEADING TRACK INDICATORS

The rise of the ANY signal clocks nine flip-flops, B18, C18, C19, D18, and C17.8. The data input to these flip-flops come from the skew counter outputs. Only the leading data input will be high when ANY rises, so only one LED will light and will indicate the leading track.

26.0 SKEW TRACK DISABLE

Any of the track switches may be switched down to remove these tracks from the skew measurement and from the leading track indication. This is accomplished by the SDØ-SDP inputs to the ANY, ALL, and leading track circuits.

27.0 STATIC SKEW

When the STATIC switch is depressed, A25 multivibrator chops the CLK supply and reduces its average rate by a factor of 10. This stretches the skew reading accumulation time by a factor of 10

to produce average readings of greater consistency. Gates U2 limit display loading to a single time after the STATIC switch is depressed. The display then remains steady as long as the switch is held.

28.0 TROUBLESHOOTING AIDS

1. Symptom: No panel lights, no action.

   Check that fan is blowing, if no fan check AC power cord and fuse. If fan is blowing disconnect cables to transport and measure voltage between READ DATA 7 and GND of panel. Voltage should be near 5 volts, if not, OV protect may have crowbared supply. Turn power off for a few seconds then back on. If then no power suspect +5 to ground shorts or power supply failure.

2. Symptom: No transport motion.

   Check that transport responds to its own controls. Check that transport is loaded and on line. Check that UNIT SELECT switch is up, READY and ON LINE

LEDs should be lighted. If not, check that cables are plugged correctly at transport.

If only one of the three transport motions, forward, reverse and rewind is failing suspect either a defective cable connection or a failure in the logic. The cable may be tested by grounding successively A3.8, D3.8 and D3.3 to cause each of these three motions. If motion response is O.K. then trace logic by referring to diagram and circuit description. To have forward or reverse motion both RUN and SM must toggle on and the MOTION test point on the panel should go high.

3. Symptom: Skew readings show unreasonable value.

Transports must be in continuous forward or reverse motion and must be reading solid ones on all tracks. Check that the data select switch is set to TRACK, select FWD motion, set WRITE RESET to normal, set WRITE switch up, set all TRACK switches up, then start motion. Note that if the WRITE switch is set after motion is started the transport will not be writing but will be reading old data.

If skew readings are still unreasonable check skew STAIRCASE test point with scope to measure analog skew and compare with digital reading. Check also with scope that bit rate timing is correct for the specified density and speed of the transport.

4. Symptom: Unsteady or wrong interval rate observed at CLOCK test point.

   Suspect bad crystal oscillator. Check with scope on logic board that crystal frequency is steady and correct. If crystal frequency is O.K. then trace through scaling logic to discover source of failure.

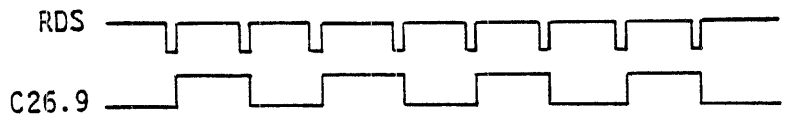
5. Symptom: Expected errors do not show on ERROR STATUS display.

   Test all LEDs by depressing STATUS TEST. Then set switches to UMT SELECT, RANDOM, FWD, WRITE, OVERRIDE and start motion. If head is dual gap the transport should be writing and reading. Force parity errors by grounding one of the READ DATA test points. Error counter should count, OVERFLOW, FWD, and WRITE LEDs should be on. If transport is NRZI the

The RDS LED should also be on. If not, look with scope at RDS test point. If no RDS strobes, be sure WRITE RESET switch is at NORMAL.

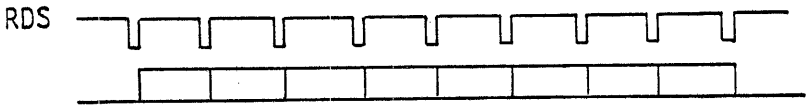
6. Symptom: Bad LRCC circuit suspected.

Set switches to NRZI, TRACK, FWD/FWD, BLOCK LENGTH 8, WRITE, DUAL GAP, OVERRIDE, and HIGH DENSITY. Set all DATA CONTROL track switches high to write all ones. Start RUN and sync scope on RDS test point. Eight RDS pulses should show on each motion cycle, set scope time to show all 8. Look with scope at pin C26.9, waveform should be as shown below:

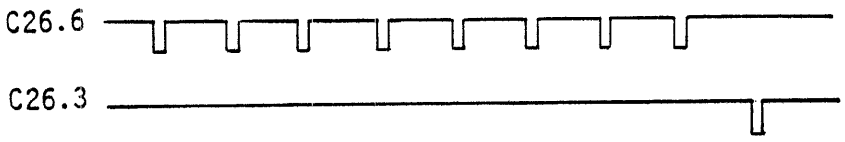


If transport is low density, approximately 6 RDS will show but C26.9 should remain low after the last RDS.

Next, set data select to RANDOM. Waveforms should be as shown below. The ninth RDS will be intermittent but C26.9 should always be low (assuming good data is being read) after the time of the ninth RDS.



If no ninth RDS shows check that $\overline{\text{WARS}}$ pulse is emitted after the write strobes. Sync on C26.6 and look at C26.3. The pattern for 800 BPI NRZI should be as shown.



ATTACHMENT A - DOCUMENT NO. 650033

UNITESTER OPERATION

Connect the TX-1200 cables to the Edge connectors

JC = Control (J16B)

JR = Read (J6B)

JW = Write (J1B)

Turn on power to the TX-1200 and set controls as follows on the TX-1200 Panel.

a. Unit Select
b. 9 Track
c. Normal (not Ampex)
d. All Track switches up position
e. Track switch data selected
f. Write switch up position
g. Speed to 12.5 IPS
h. Block length to 1024
i. Motion control set to forward

Dual Gap

The following control indicators on the unitester should be on

a. Select

b. Write Enable

NOTE

> The indicators will only work if Pin 8 is jumpered to +5V on the write connector.

The unitester switches will light the corresponding leds on the control panel as they are pushed up.

NOTE

> You must leave the following switches on for the unitester to work.
>
> 1. On line
> 2. Ready

Press start on the TX-1200 and the data channel leds should light and also RDS should be on. By turning on and off each data channel track switch, you should count up the error counter.

Press stop and set the motion control to FWD/FWD and press start. The data channel leds will flash on and off in step with what the block length is set to.

Checking Program Mode

In program mode and you press start, the following action will happen.

Write enable comes on, forward will count 4 times, then reverse will come on and stop counting. Press Start/Stop switch to repeat this sequence.

Checking the Alternate Mode

1. Place Ramp switch up.
2. Turn off Write switch.
3. Press Start/Stop switch.

The unitester forward and reverse should be cycling.

When you set EOT on and reset the switch, the EOT LED stays on. Use the Ready Switch to clear the EOT latch.

NOTE

This test module works in NRZI mode only.

ATTACHMENT B

TX-1200 Control Cable Signals

TX-1200 Pin Number	Signal Name	Function	Tape Unit Pin Number
J1 - 6	SPEEDIO	SPEED STATUS	A
J1 - 8	REWIND	REWIND STATUS	N
J1 - 10	EOT	END OF TAPE STATUS	U
J1 - 12	BOT	BEGINNING OF TAPE STATUS	R
J1 - 14	RWC	REWIND COMMAND	H
J1 - 16	SRC	STOP/REVERSE COMMAND	E
J1 - 18	SFC	STOP/FORWARD COMMAND	C
J1 - 22	UNLOAD	REWIND UNLOAD COMMAND	V
J1 - 24	NRZI	DENSITY SELECT (7 TRACK ONLY)	D
J1 - 26	UNIT SEL	SELECT UNIT 0	J
J1 - 28	OFFLINE	OFF LINE COMMAND	L
J1 - 30	DENS	DENSITY STATUS	F
J1 - 32	FLPRT	FILE PROTECT STATUS	P
J1 - 34	RD4	READY STATUS	T
J1 - 36	UNLINE	ON LINE STATUS	M
J1 - 40	WEN	WRITE ENABLE COMMAND	K
J1 - 11,13,21,23,25 27,29,31,33,35 37	GND	GROUND	1,2,3,4,5,6,10,11 12,13,14,16,18

TX-1200 Read Cable Signals

TX-1200 Pin Number	Signal Name	Function	Tape Unit Pin Number
J3 - 1	RDS IN	READ STROBE	2
J3 - 3	RDP	PARITY CHANNEL	1
J3 - 4	NRZI STAT	NRZI/PE STATUS	10
J3 - 5	RD7	CHANNEL SEVEN	18
J3 - 7	RD6	CHANNEL SIX	17
J3 - 9	RD5	CHANNEL FIVE	15
J3 - 11	RD4	CHANNEL FOUR	14
J3 - 13	RD3	CHANNEL THREE	9
J3 - 15	RD2	CHANNEL TWO	8

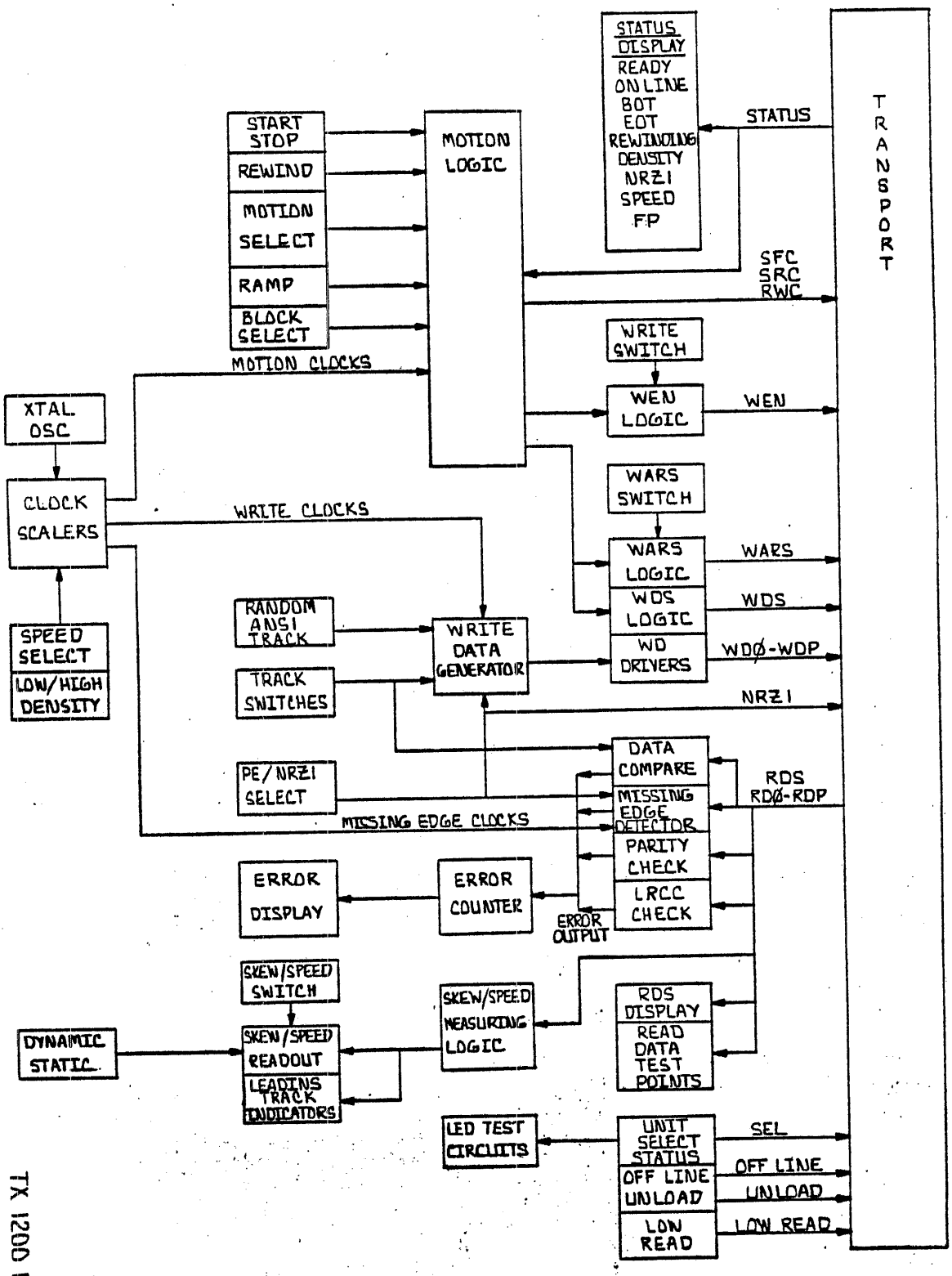
TX-1200 Read Cable Signals (continued)

TX-1200 Pin Number	Signal Name	Function	Tape Unit Pin Number
J3 - 17	RD1	CHANNEL ONE	4
J3 - 19	RD0	CHANNEL ZERO	3
J3 - 6,8,10,12,14 16,18,20	GND	GROUND	A,B,C,D,J,K,L,M, R,S,U,V

TX-1200 Write Cable Signals

TX-1200 Pin Number	Signal Name	Function	Tape Unit Pin Number
J2 - 1	WARS	WRITE RESET	C
J2 - 3	WEN	WRITE PERMIT	B
J2 - 5	WDS	WRITE DATA STROBE	A
J2 - 7	WD5	CHANNEL FIVE	T
J2 - 9	WD4	CHANNEL FOUR	S
J2 - 11	WD3	CHANNEL THREE	R
J2 - 13	WD2	CHANNEL TWO	P
J2 - 15	WD1	CHANNEL ONE	N
J2 - 17	WD0	CHANNEL ZERO	M
J2 - 19	LOW READ	LOW READ THRESHOLD	D
J2 - 21	WD6	CHANNEL SIX	U
J2 - 22	WD7	CHANNEL SEVEN	V
J2 - 2,4,6,8,10,12, 14	GND	GROUND	1,3,4,6.10,11,12,13,14, 15,16,17,18

On Pertec model tape units, the write cable connector is identified as J102, the control cable connector is J101, and the read cable connector is J103.
On Wangco model tape units, the write cable connector is identified as J1B, the control cable connector is J16B, and the read connector is J6B.



TX 1200 BLOCK DIAGRAM

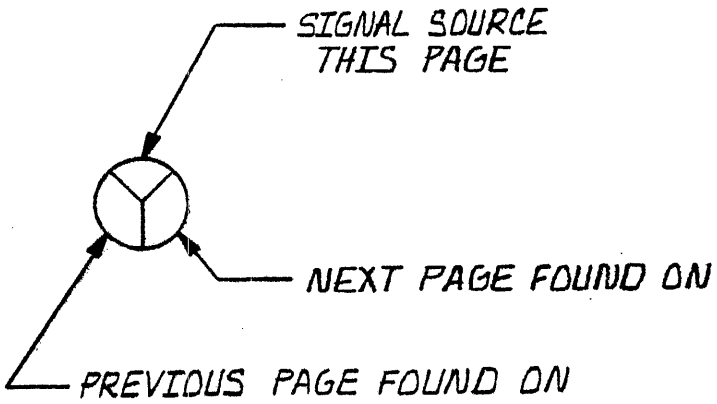
TX 1200 BLOCK DIAGRAM

TX-1200
CONNECTOR TERMS

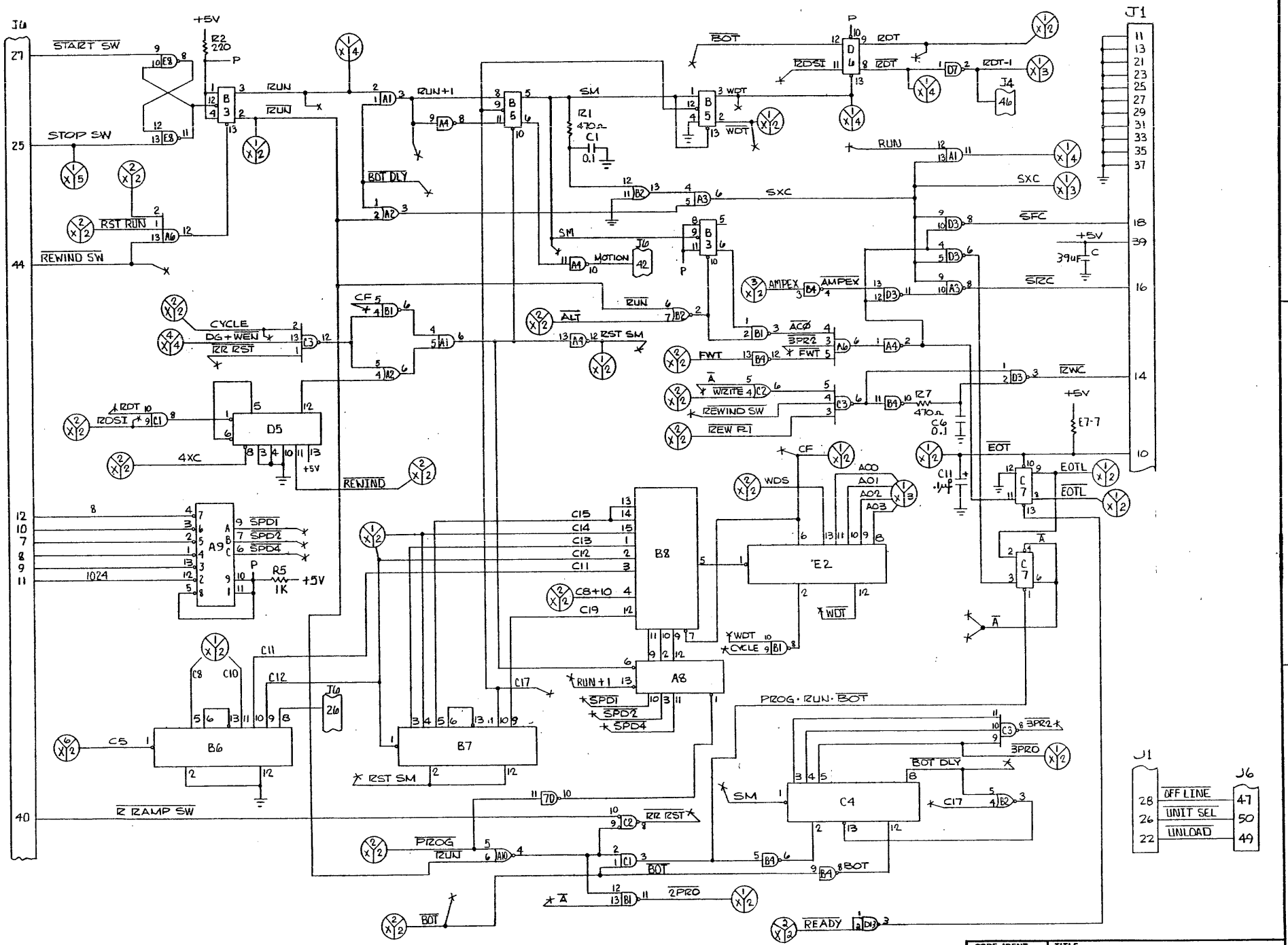
	J1	J2	J3	J4	J5	J6	
1		WARS	RDS IN	RD6	L.T.6	2 ER L	1
2		GND	+5V	GND	L.T.7	16 ER L	2
3		WEN	RDP	RD2	L.T.4	4 ER L	3
4		GND	NRZI STAT	GND	L.T.5	1 ER L	4
5		WDS	RD7	RD7	L.T.2	OV FL L	5
6	SPEED ID	GND	GND	GND	L.T.3	8 ER L	6
7		WD5	RD6	RD3	L.T.1	128 BL	7
8	REWIND	GND	GND	GND	L.T.Ø	256 BL	8
9		WD4	RD5	RDP	FWD E	512 BL	9
10	EOT	GND	GND	GND	WR E	64 BL	10
11	GND	WD3	RD4	RD4	CK 7	1024 BL	11
12	BOT	GND	GND	GND	R 7	8 BL	12
13	GND	WD2	RD3	RDØ	BL 7	STOP ON 8	13
14	RWC	GND	GND	GND	L.T.P		14
15		WD1	RD2	RD5	STATIC		15
16	SRC		GND	GND	SKEW	RCON	16
17		WDØ	RD1	RD1	SP 45	F/F	17
18	SEC		GND	GND	SP 60	F CON	18
19		LOW READ	RDØ	RDS IN	SP 25	ALT	19
20		+5V	GND	GND	SP 37.5		20
21	GND	WD6				R/R	21
22	UNLOAD	WD7			SP 12.5		22
23	GND	WDP				C8+10	23
24	NRZI	+5V			SP 75		24
25	GND				RST ERRS	STOP SW	25
26	UNIT SEL	+5V					26
27	GND			SDØ		START SW	27
28	OFF LINE			SKEW SYNC	L P 7		28
29	GND			SD5			29
30	DENS			TR5 L	AMPEX		30
31	GND			ERR P •	STATUS T	E10 • 6	31
32	FL PRT			TR3 L	OFF L L		32
33	GND			SD4			33
34	RD4			TR1 L	FP L		34
35	GND			SD6	6250	WRITE	35
36	UN LINE			TR7 L	DEN L	INH	36
37	GND			SD2		PROG	37
38				TRØ L	LRCC L	ILL C L	38
39	+5V			SD7	NRZI	HI DENS	39
40	WEN			TR2L	NRZ L	RRAMP	40
				SD3		WR RES S	41
				TR4 L	RDY L	MOTION •	42
				SDP		T TR	43
				TR6 L	BOT L	REW SW	44
				DG SW		CLOCK •	45
				TR P L	REW L		46
				LOW RSW		OFF L	47
				RANDAT	EOT L	RDS L	48
				TSD SW		UNLOAD	49
					SPEED L	UNIT SEL	50

		F	E	D	C	B	A	
J2	1	7437	7421	7474	7408	7437	7408	1
	2	7437	74393	74107	7432	380	7432	2
	3	7437	74157	7437	7410	74107	7437	3
	4	74180	74151	74393	74393	7404	7404	4
J1	5	7486	74157	74197	7432	74107	555	5
	6	7486	7474	7474	7437	74393	7411	6
	7	7486	34A4714	7404	7474	74393	7411	7
	8	7495	7437	7432	7432	74151	74197	8
J6	9	7495	7495	74121	7408	74193	74147	9
	10	74157	74107	7408	7406	74107	7402	10
	11	74157	7474	7402	74163	7432	———	11
	12	74S288	7437	7408	74163	7408	74164	12
	13	34A4714	7404	7400	74188	34A4714	74164	13
	14	74161	7432	74161	74147	SW	74164	14
	15	74161	7404	7432	XTAL	XTAL	74164	15
J5	16	74161	7408	74157	380	380	74164	16
	17	74161	7402	74175	7474	9602	74164	17
	18	7438	7438	7474	7474	7474	74164	18
	19	7438	7438	7438	7474	7430	74164	19
	20	7404	7404	7404	7404	7404	74164	20
J4	21	74393	74393	74393	74393	74393	470Ω +	21
	22	7432	7432	7432	7474	———	———	22
	23	7474	7474	7474	7474	7404	7474	23
	24	3484714	3484714	8242	7430	74107	7408	24
J3	25	8242	8242	7474	74180	7474	555	25
	26	8242	8242	7404	MC8502	26		

IC LOCATOR



EPLANATION OF SHEET TO SHEET
REFERENCE BUBBLE.



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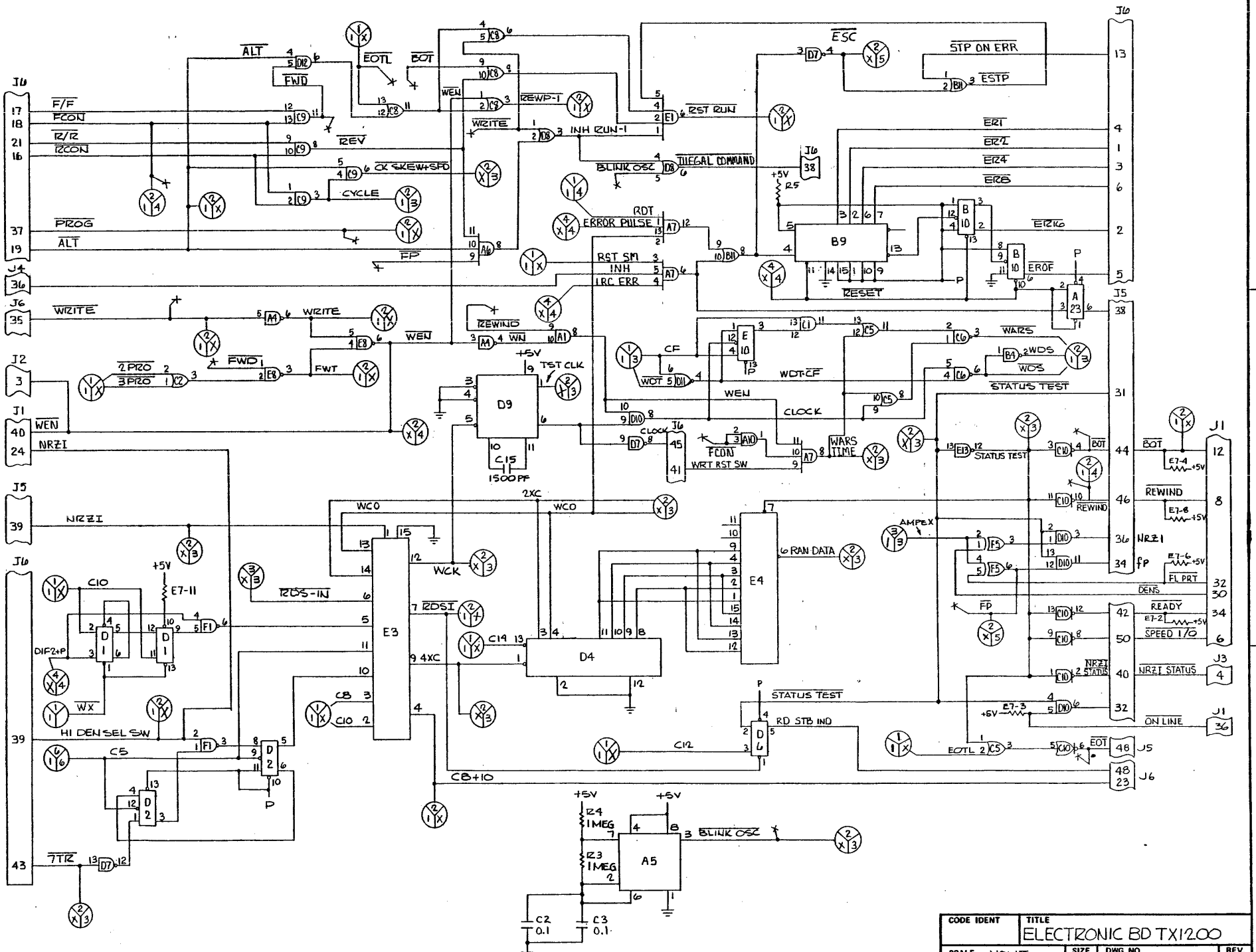
SCALE NONE	SIZE C
SHEET 1 OF 6	DWG. NO. 300022
	REV. A

5016 REV 6/71



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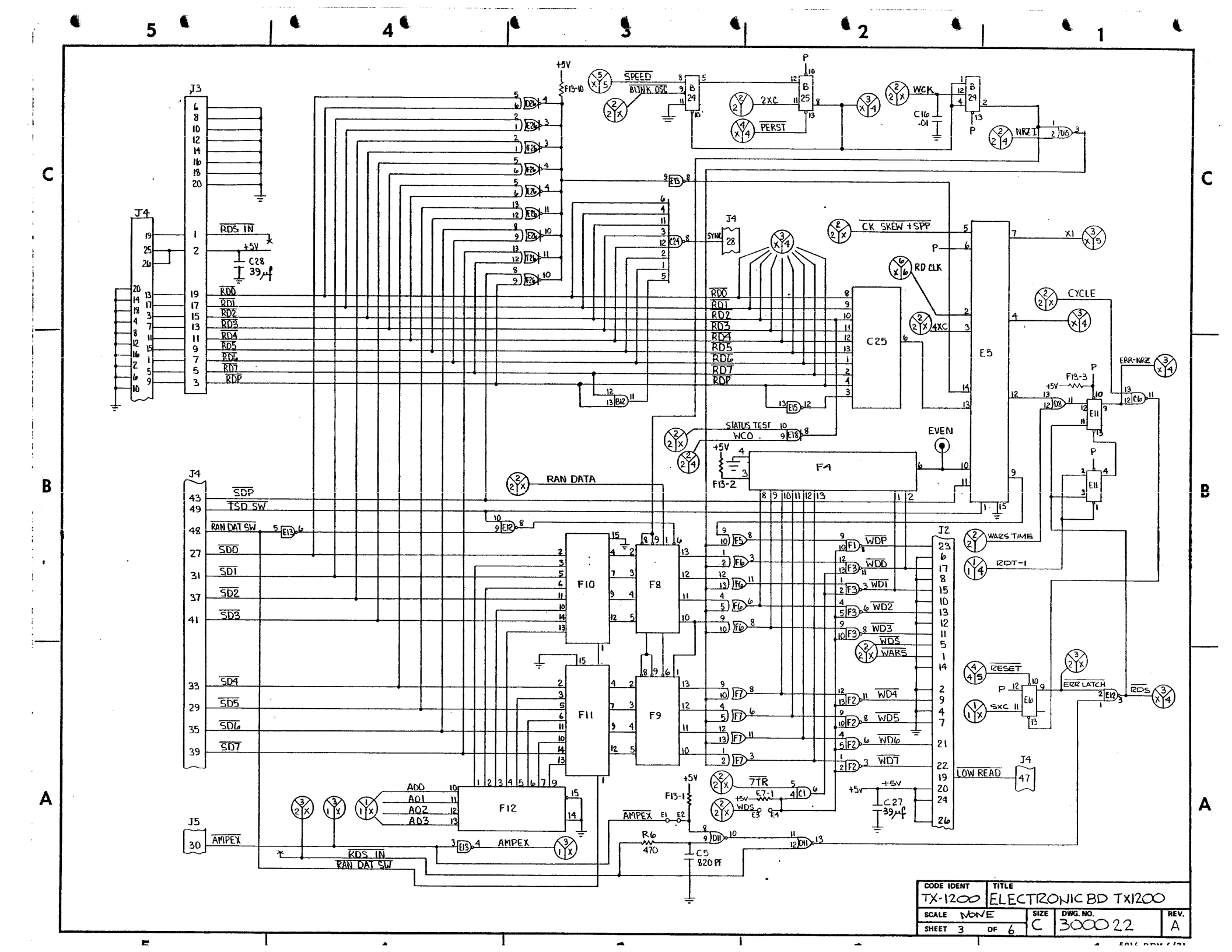
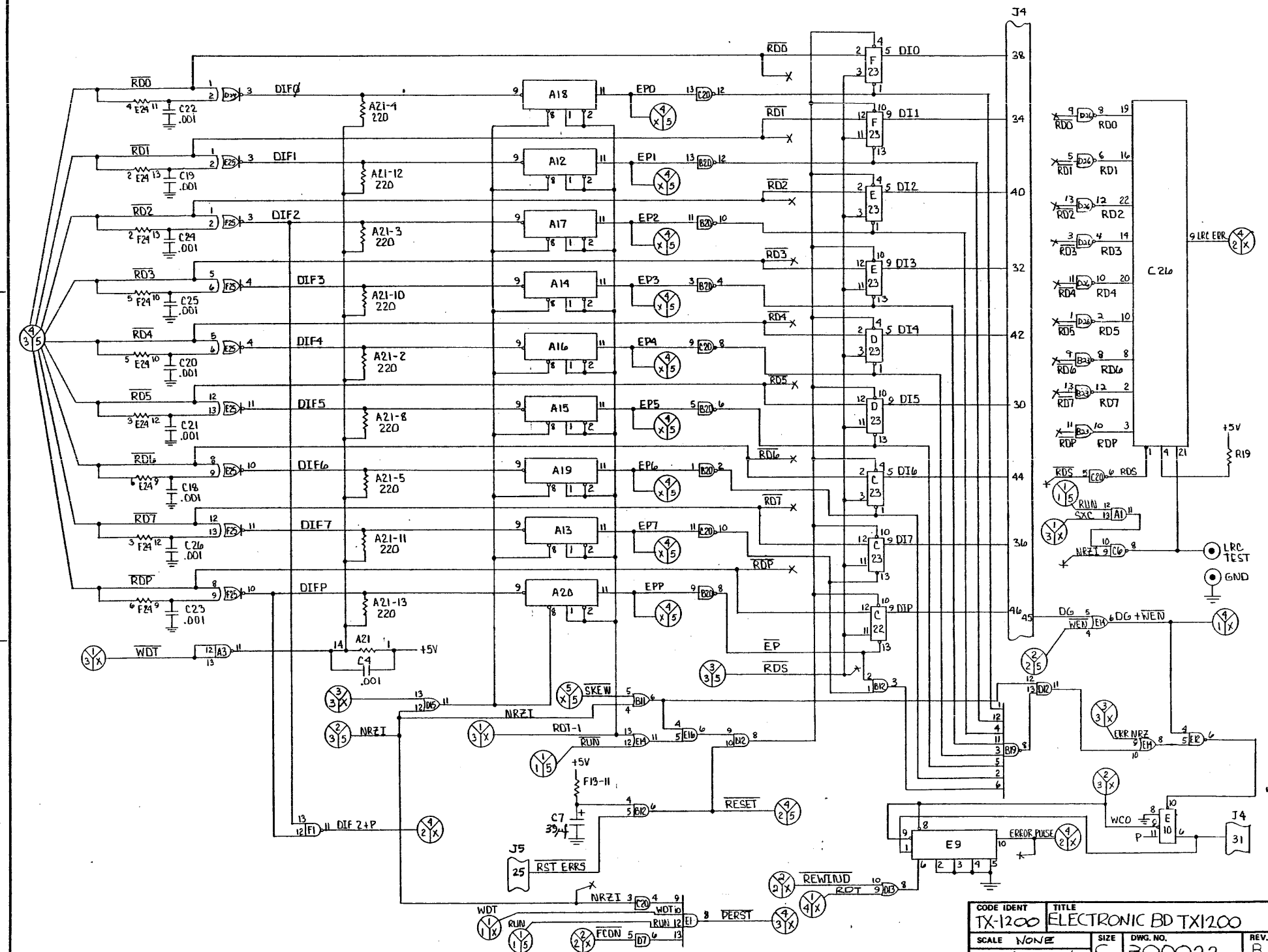
	ELECTRONIC BD TX1200			
SCALE NONE	SIZE C	DWG. NO. 300022	REV. B	
SHEET 2 OF 6				


J3
J4
J5
RDS IN
+5V
C28
39µf
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RDP
SDP
TSD SW
RAN DAT SW
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
AMPEX
SPEED
BLINK OSC
2XC
PERST
WCK
C16
.01
NRZI
CK SKEW +SPP
RD CLK
4XC
CYCLE
STATUS TEST
WC0
RAN DATA
EVEN
C25
E5
F4
F13-2
F13-3
F13-10
F13-1
F10
F11
F8
F9
F12
E11
E6
WARS TIME
RDT-1
WDP
WD0
WD1
WD2
WD3
WDS
WARS
WD4
WD5
WD6
WD7
LOW READ
RESET
SXC
ERR LATCH
ERR-NRZ
RDS
7TR
E7-1
C27
39µf
R6
470
C5
820 PF
ADD
AD1
AD2
AD3
J2
CODE IDENT
TX-1200
TITLE
ELECTRONIC BD TX1200
SCALE NONE
SHEET 3 OF 6
SIZE C
DWG. NO. 300022
REV. A



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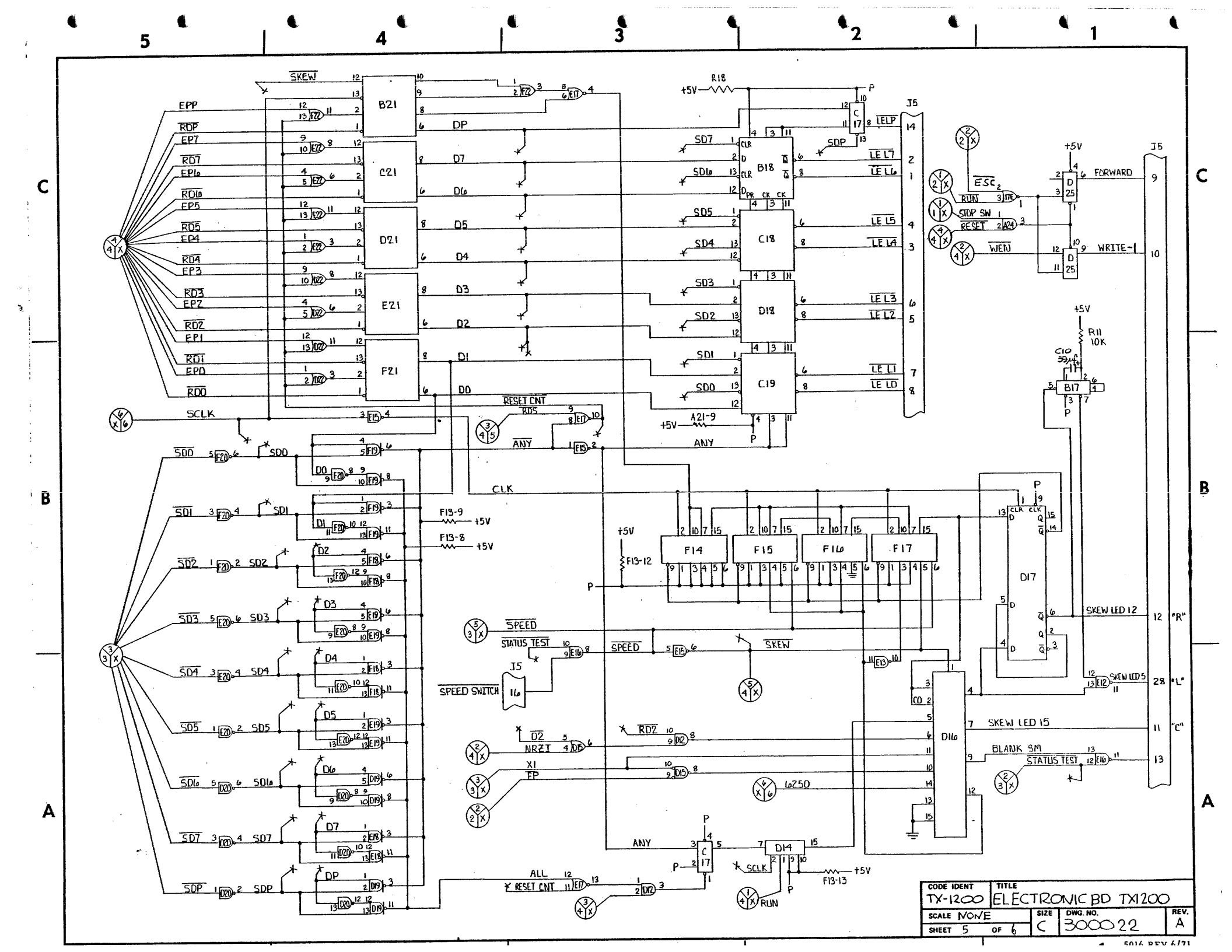
SCALE NONE	SIZE C
SHEET 4 OF 6	DWG. NO. 300022
	REV. B



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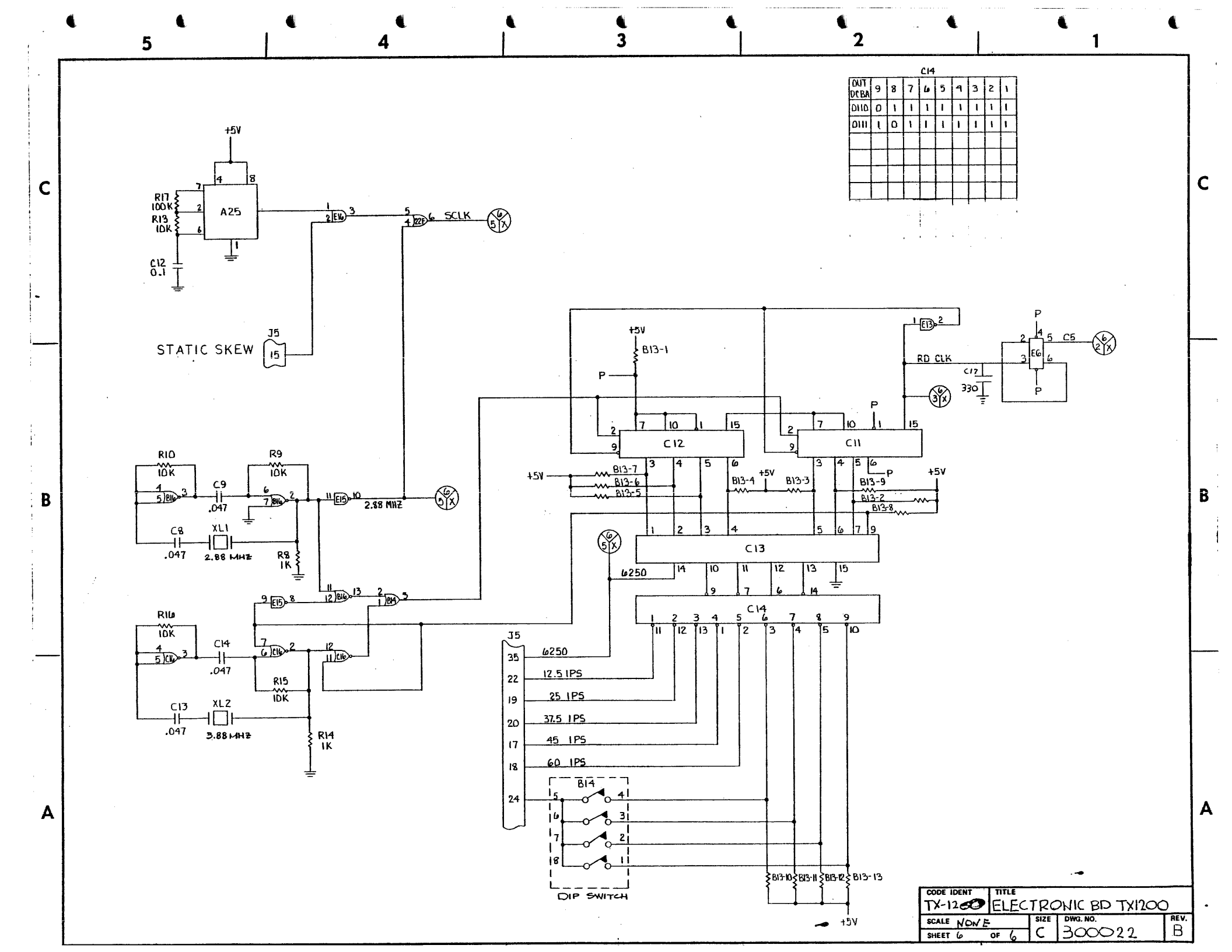
5016 REV 6/71


5
4
3
2
1
C
B
A
C14
OUT DCBA
9 8 7 6 5 4 3 2 1
0110 0 1 1 1 1 1 1 1 1
0111 1 0 1 1 1 1 1 1 1
+5V
R17 100K
R13 10K
A25
C12 0.1
SCLK
STATIC SKEW
J5
15
RD CLK
C17 330
C5
E6
P
B13-1
C12
C11
C13
C14
B13-7
B13-6
B13-5
B13-4
B13-3
B13-9
B13-2
B13-8
R10 10K
R9 10K
C9 .047
2.88 MHZ
C8 .047
XL1 2.88 MHZ
R8 1K
R16 10K
C14 .047
R15 10K
C13 .047
XL2 3.88 MHZ
R14 1K
6250
12.5 IPS
25 IPS
37.5 IPS
45 IPS
60 IPS
B14
DIP SWITCH
B13-10
B13-11
B13-12
B13-13
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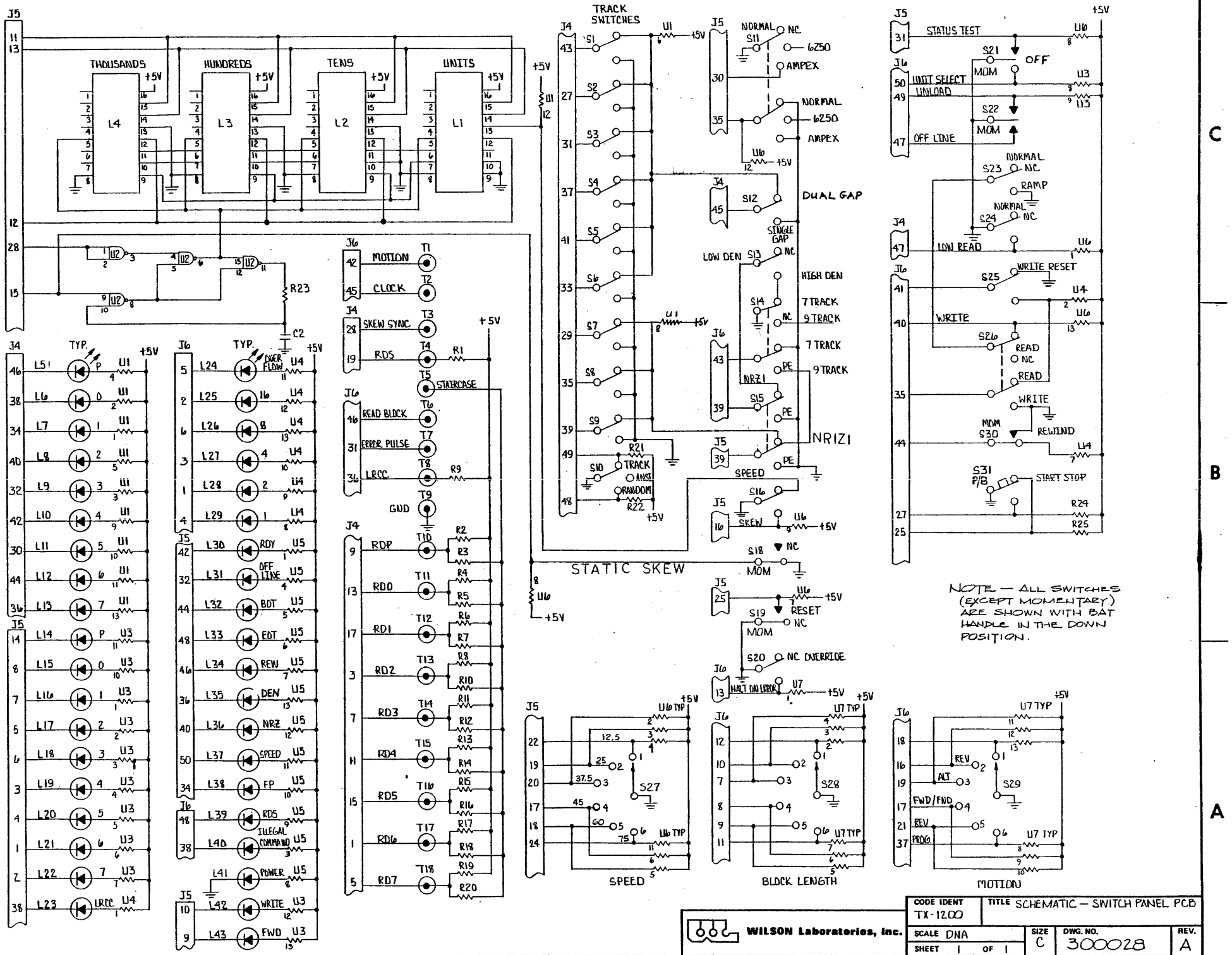
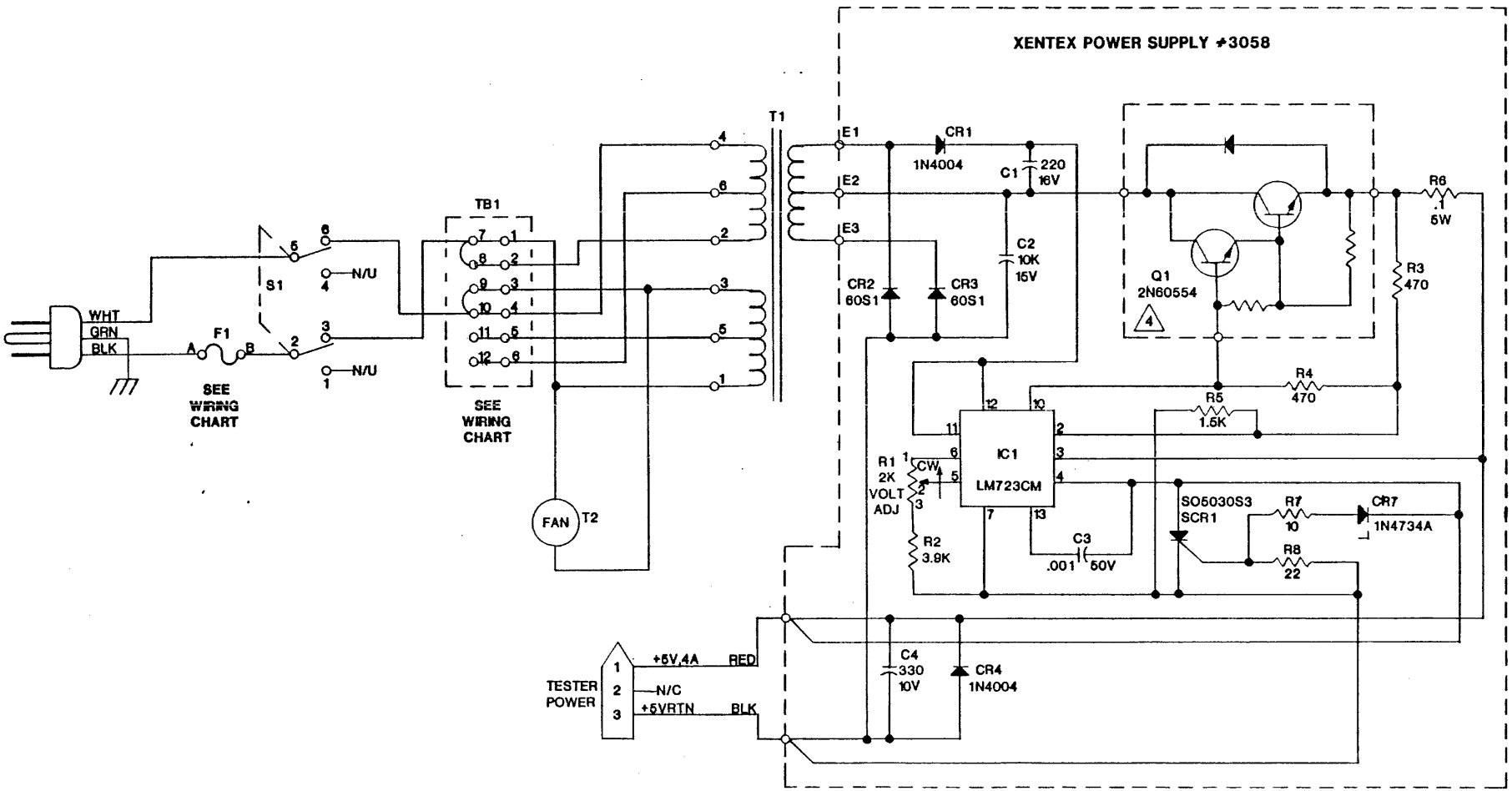
TITLE ELECTRONIC BD TX1200
SCALE NONE
SHEET 6 OF 6
SIZE C
DWG. NO. 300022
REV. B


THOUSANDS
HUNDREDS
TENS
UNITS
L4
L3
L2
L1
TRACK SWITCHES
STATIC SKEW
NRZI
DUAL GAP
SPEED
BLOCK LENGTH
MOTION
NOTE — ALL SWITCHES (EXCEPT MOMENTARY) ARE SHOWN WITH BAT HANDLE IN THE DOWN POSITION.
WILSON Laboratories, Inc.
CODE IDENT TX-12.00
TITLE SCHEMATIC — SWITCH PANEL PCB
SCALE DNA
SHEET 1 OF 1
SIZE C
DWG. NO. 300028
REV. A
5016 REV 6/71

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	X1	ENG. RELEASE		
	A	PROD. RELEASE	1/29/81	



NOTES:UNLESS OTHERWISE SPECIFIED.

1. REF TO ASSY DWG:100075
2. ALL RESISTANCE VALUES IN OHMS-5%,1/2W
3. ALL CAPACITANCE VALUES IN MICROFARADS.
4. COMPONENT MOUNTED ON CHASSIS.

WIRING CHART		
VOLTAGE	WIRING	FUSE
100V	SW AC LINE TO 7 TO 8 , 9 TO 10 , AC LINE TO 11	3/4A
115/120V	SW AC LINE TO 7 TO 8 , AC LINE TO 10 TO 9	3/4A
200V	SW AC LINE TO 7 , 8 TO 11 , AC LINE TO 12	3/8A
215V	SW AC LINE TO 7 , 8 TO 9 , AC LINE TO 11	3/8A
230/240V	SW AC LINE TO 7 , 8 TO 9 , AC LINE TO 10	3/8A

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± DEC ± ANGLES ±

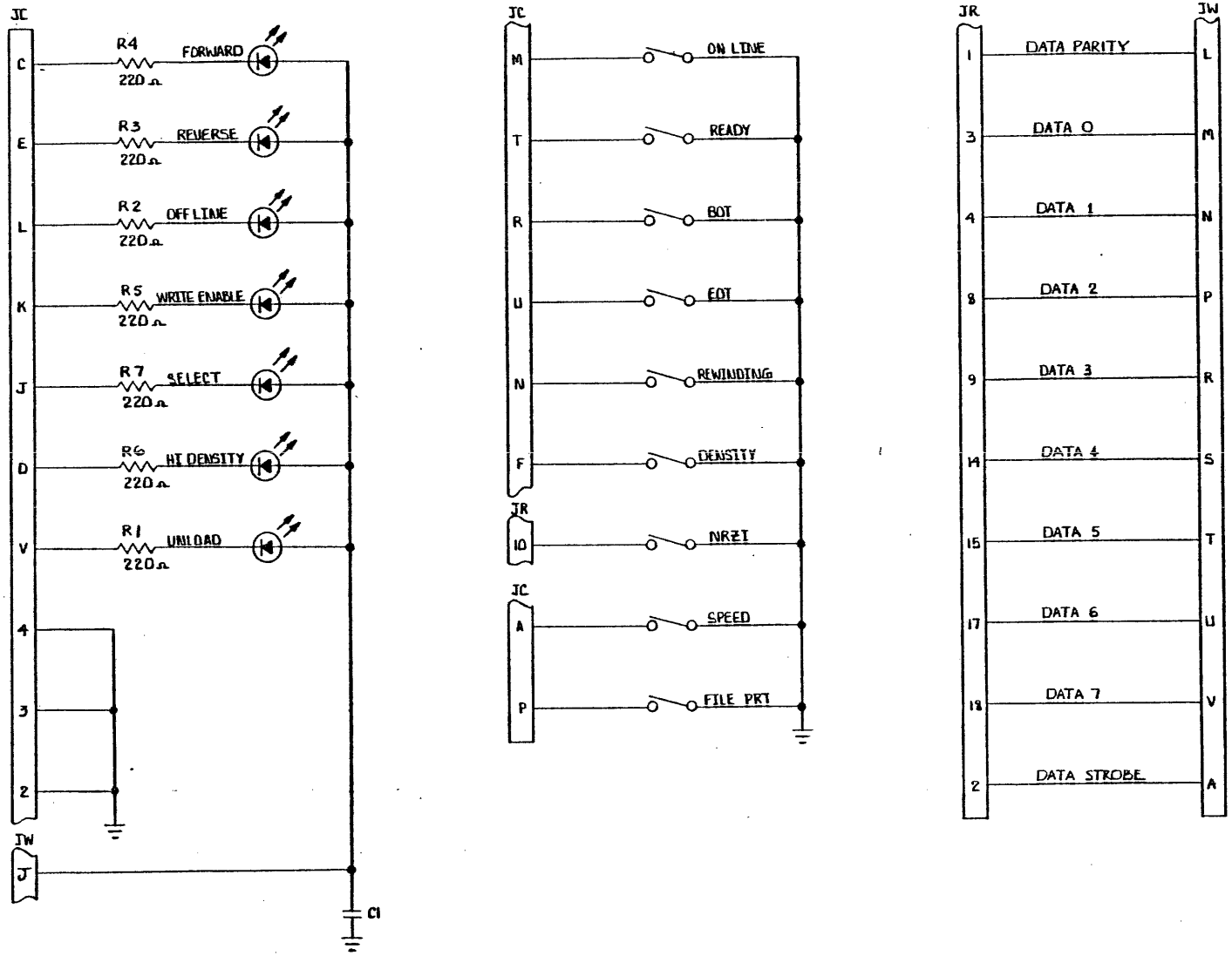
APPROVALS	DATE
DRAWN JAM	1-29-81
CHECKED	

WILSON Laboratories, Inc.

SCHEMATIC-
DX1000/TX1200
POWER SUPPLY

SCALE	SIZE	DRAWING NO.	REV
NONE	C	300029	A

DO NOT SCALE DRAWING SHEET 1 of 1



CODE IDENT	TITLE
TX-1200	SCHEMATIC- UNITESTER

SCALE	SIZE	DWG. NO.	REV.
DNA	C	300030	A

SHEET 1 OF 1

5016 REV 6/71